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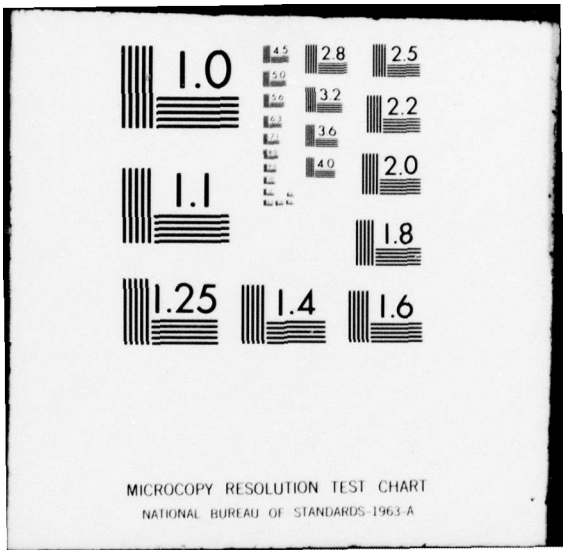
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Pulse Field Effects Measurements

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)
The pulsed field effect technique is a measurement of the surface conductance of a semiconductor under the influence of a transverse electric field and was used to investigate surface states and interface states at the silicon-oxide interfaces. The investigation studied whether the pulsed field effect technique could be used to detect fast interface and in regions close to the valence and conduction band edges. These states are able to exchange charge with the bands relatively fast, as compared to those which are closer to the (over)

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center of the energy band gap. The effects of total ionizing radiation dose on interface state density and induced oxide charge were investigated. This work resulted in the development of a pulsed field effect technique which determines the interaction of fast interface states with the channel conductance of the MOSFET. It scans a portion of the silicon band gap not obtainable using any other simple interface state analysis technique. Data which indicate that there are correlations between interface state density before irradiation and the radiation induced oxide charge are presented.

PREFACE

Since the completion of this report, other work has changed some of the conclusions and has verified the decrease with radiation of the edge state density.

The work of M. Pepper* has shown that the edge states are Anderson localization states and result from random fluctuations of the electrical potential at the surface.

A random distribution of negative and positive charges produces a density of localized states which increases with the total number of charges rather than a net charge. The number of localized states is seen to decrease with radiation. The explanation offered is that holes from the oxide cancel the negative charges decreasing the total charge, thereby the number of localized states, and increasing the positive surface charge. This effect was strong in nitrogen annealed devices and was reduced to a minimum with devices processed by the Sandia hard process. Thus at this time a positive correlation exists between these edge states and deleterious nitrogen anneals. Thus the edge state density can be used as a hardness assurance program.

*Pepper, M., "Solid State," J. Physics, Vol. 10, L445, 1977.

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CHAPTER I

INTRODUCTION

The metal oxide field effect transistor (MOSFET) enjoys a wide application in many electronic systems. Significant progress has been made in improving the device performance since its inception. D. Kahng and M. Atalla (Ref. 1) presented the device as a metal/silicon-dioxide/silicon structure in 1959. Shockley and Pearson (Ref. 2) demonstrated the field effect as early as 1948, but the greatest barrier to the MOSFET's evolution was in finding a suitable gate insulating material. The use of a silicon-dioxide film as an insulator made the MOSFET a potentially useful device, but with its accompanying problems. These include contaminants which had a drastic effect on device reproducibility. With improvements in processing technology, the production of clean silicon-dioxide films opened the way for the MOSFET's widespread use. The metal/silicon-dioxide/silicon interfacing strongly influenced the MOSFET's performance. Therefore, considerable research has been put into understanding this interfacial system. Through the understanding of the physics in this interface, improved device performance and its wider uses will be realized.

Since the use of the MOSFET is extensive, a current area of investigation is to observe device performance in abnormal environments. One of the ambients which might be subjected to this device is ionizing radiation. In particular, gamma radiation with its vast quantities in outer space and after a nuclear explosion. Detrimental effects from gamma radiation occur in the MOSFET mainly in the metal/silicon-dioxide/silicon layers. Again, the understanding of this interface system is the key to the MOSFET's susceptibility to radiation. Observation of some of these gamma radiation

effects will be the subject of this paper.

Hughes (Ref. 3) was the first to note the effects of radiation on metal-oxide-semiconductor devices which has since been studied by many investigators (Ref. 4, 5, 6, 7). Gamma radiation produces two basic changes in material properties near the silicon-silicon dioxide interface. Both interface state density and the fixed positive charge in the silicon dioxide are affected. Most often radiation will increase the positive charge (Ref. 8) and increase the density of interface states (Ref. 9, 10), as observed in this report. But it is dangerous to generalize because changes may depend upon complex factors such as process parameters (whose effects are not well understood) and upon the radiation level. Further, interface state density appears to increase in one region of the energy band gap and decrease in another region. Both the energy distribution of interface state density and the fixed positive charge determine the location of the fermi level near the interface and therefore they affect both the type and density of free majority carriers near the interface. The density and charge nature of the interface states also affects carrier mobility. The matter of making physical measurements on MOS systems and extracting information is very complex (Ref. 5). In MOSFET's, the main parameters affected by total dose are shifts in threshold or "turn on" voltage and transconductance. Threshold voltage is strongly affected by fixed charge and transconductance is strongly affected by carrier mobility.

One physical parameter which may give an indication of a MOSFET's radiation susceptibility is the density of interface states. These interface states cause a decrease in channel conductance in the MOSFET. This decrease occurs as a time dependent phenomenon due to the different

time constants of these states which interact with the mobile conduction charge in the channel. These time constants are dependent upon the position of the interface states in the band gap. Radiation can increase the density of interface states whose time constants correspond to normal circuit switching times of a MOSFET. This can cause problems in MOSFET switching circuitry exposed to ionizing radiation. It is thought, as a result of recent work by Sivo et al. (Ref. 10) and early work by Fitzgerald and Grove (Ref. 11), that radiation produced interface states are manifestations of the original interface state densities. It is also thought that the original density of fast interface states may give an indication of the magnitude of shift in MOSFET threshold voltage due to radiation. This gives a radiation susceptibility parameter.

It is thus the intended goal of this research effort to evaluate or develop a technique which would determine the density of fast interface states in the MOSFET. One major requirement of this technique is that it would be operable in a production line environment. Therefore, this technique would act as a quality control measurement which ultimately predicts a radiation susceptible parameter in MOSFET's.

CHAPTER II

TECHNIQUES USED TO INVESTIGATE INTERFACE STATES

A brief discussion of interface states and techniques used to measure them will be presented. Interface states are a result of the interruption of the periodic lattice structure at the surface of the crystal. These states appear as energy levels within the band gap which exchange charge with the valence and conduction bands of the semiconductor. They are located at the plane separating the semiconductor from the insulator. Shockley and Pearson (Ref. 2) first investigated surface states using surface conductance measurements. Since then, many other investigators have measured these states using various techniques. Before discussing a technique which is suitable, a brief review of other techniques and their limitations will be presented.

Terman (Ref. 12) developed a high frequency capacitance technique which yielded data on interface state density. The limitations of this technique are discussed by Zaininger and Warfield (Ref. 13). In order to determine the interface state density, the data must be graphically differentiated and its functional dependence on surface potential derived from an ideal capacitance voltage (C-V) curve. Also, the region of the band gap under investigation is limited by the time constant of the states which can be charged and discharged by the test frequency.

An extremely accurate technique for determining the density of interface-states was devised by Nicollian and Goetzberger (Ref. 14). This technique is known as the a.c. conductance technique. The a.c. conductance of a metal-oxide-semiconductor (MOS) diode is measured as a function of surface potential and frequency. This conductnace is a measurement of

the charge exchange of interface states with the bulk of the semiconductor. This technique requires considerable instrumentation and measurements before providing some detailed interface state information. The region of observation in the band gap is between mid-gap and the fermi level.

The Gray Brown technique (Ref. 15) is used for investigating interface states near the majority carrier band edge. This was done by measuring the flat band voltage of a MOS capacitor as a function of temperature. The band gap region of observation is limited by the temperature, because high temperatures produce oxide instability and low temperatures result in deionized impurities.

Other techniques which also employ the MOS capacitor for interface state determination were by Berglund (Ref. 16) and Kuhn (Ref. 18). Their techniques are extensions of the capacitance technique presented by Terman (Ref. 12). Berglund (Ref. 16) used very low frequency MOS capacitance measurements at thermal equilibrium and performed an integration which yields surface state density. This technique utilizes a sinusoidal phase sensitive measurement which is difficult to perform below 5 kilohertz (kHz). Kuhn (Ref. 18) was able to get around this problem by using a quasi-static method involving the measurement of the MOS displacement current in response to a linear voltage ramp. This method provides the most direct way of obtaining the interface state density across most of the band gap.

The above techniques provide extensive information on interface state densities. However, they do not meet our objective since they will not detect interface states near band edges. The reason is connected with the "method" by which induced charge is measured beneath the gate of the different devices. In the MOS capacitor, there are

three sources of charge which form the inversion layer beneath the gate. As a result of an applied gate potential, charges come from (i) surface generation (ii) generation in the depletion region (iii) and diffusion of carriers from the bulk semiconductor. In the latter, the carriers come from a region within a diffusion length of the depletion region and are swept across the depletion region. The dynamics involved as discussed by several authors (Ref. 14, 17, 18, 19, 20) indicate that the time constants of the above processes are greater than 0.01 second, which is relatively long. The MOS transistor has two relatively fast sources of charge which to form the inversion layer. These large sources of charge are the source and drain regions of the device. They can respond to an applied gate voltage on the order of 1 nanosecond according to Zahn (Ref. 21). As a result, the above techniques become invalid for measuring the effects of interface states on induced charge in the MOS transistor. It is necessary to measure interface state response times of one nanosecond or less to observe those close to band edges.

The most common type of measurement made on the MOSFET which detects the influence of interface states is a conductance measurement. Instead of making measurements across the gate and substrate terminals, as in the MOS capacitor, measurements are made across the source and drain terminals. This measurement is made under the influence of a transverse electric field from the gate which forms the inversion layer. Therefore, this approach involves measuring the conductance of the channel formed under the gate. There are several methods of monitoring this conductance and extracting the influence of interface states.

Arnold (Ref. 22) measured the channel conductance as a function of temperature. From these measurements it is possible to determine the

fixed positive charge and the charge trapped in interface states whose occupancy is a function of surface potential. Here again, varying temperature limits the region of the band gap which may be observed. The lower limit is approximately 125 K where complete ionization may be assumed for substrate doping below 10^{16} cm^{-3}. The upper limit for stable MOSFETs is approximately 500 K (Ref. 22). Also, any measurement which involves temperature variation cannot be used for production line purposes and thus should not be considered.

A very promising technique for the investigation of interface states is the pulsed field effect measurement. In this measurement, a pulse is applied to the gate and the conductance of the channel is monitored. From this measurement, information on the influence of interface states may be extracted. The details of this technique will be covered in the following chapter. There are several reasons for considering this technique as an effective tool to meet our objectives. First of all, it is simple, since it requires very little instrumentation. It also requires only one measurement which makes it inexpensive to operate. Another important feature is that it is fast, making it ideal for a production line environment. Measurements of this type can be made at thermal equilibrium which is highly desirable. Due to the above advantages, considerable time was spent evaluating the use of the pulsed field effect measurement.

CHAPTER III

PULSED FIELD EFFECT TECHNIQUES

Initial measurements which verified the existence of surface states were later developed into the pulsed field effect measurement. Shockley and Pearson (Ref. 2) verified the existence of surface states by placing an electric field perpendicular to the surface of a semiconductor and noting its influence on surface conductance. The electric field acted to fill or empty the existing surface states through accumulation or depletion. The polarity of the field determines the occupancy of the surface states. These states either trap or release mobile conduction charge and consequently change the surface conductance of the semiconductor. Surface conductance measurements of this type showed that there were various time constants associated with the surface states. Surface states became classified as either fast or slow depending on their speed and physical location. Slow states existed between the oxidized surface layer and the air, which made their exchange of charge with the valence and conduction bands of the semiconductor rather slow. On the other hand, surface states which existed between the oxidized surface layer and the semiconductor can exchange charge easily with the valence and conductions bands and are designated as fast. In this paper, these fast surface states will be known as interface states.

Low (Ref. 23) devised a circuit for measuring slow surface states. In this technique, a low frequency signal was applied to the gate and a surface conductance measurement was made. It was assumed that all slow varying states were at equilibrium with the slowly varying signal and any change in conductance was due to slow surface states. Low (Ref. 23) was able to mimimize the effects of any displacement current produced by the

applied gate signal by nulling them at the output as shown in Figure 1.

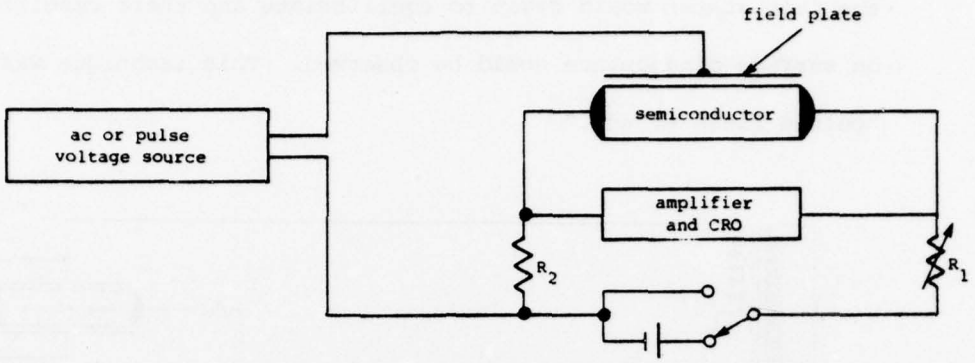


Figure 1. Circuits for minimizing the effect of the displacement current on the pulsed field effect measurement. (After Low, Ref. 23)

With the d.c. measuring voltage shorted out, the resistor R_1 is adjusted until the signal on the oscilloscope is at a minimum. Under these conditions, the displacement current is distributed evenly across the two input terminals of the differential amplifier. When the d.c. voltage is switched "on," the measured signal is due to the field effect on surface conductance. Improved signals could be obtained by increasing the current through the semiconductor thus making the field effect signal comparable to the displacement current. However, higher currents resulted in overheating the semiconductor and in contact injection. Many et al. (Ref. 24) were able to overcome this by using a pulse-activated Wheatstone bridge as shown in Figure 2.

As a result of using the measuring apparatus shown in Figure 2, it became desirable to investigate the effects of fast surface states, or interface states, on surface conductance. This involved applying a fast risetime square pulse to the gate so that it could not be followed by surface states. The pulse risetime was sufficiently small that the charge condition of many interface states could not move in equilibrium with the

the onset of a given pulse. During the pulse, the charge condition of the fast states would begin to equilibriate and their resulting effect on surface conductance could be observed. This technique was called the "pulsed field effect."

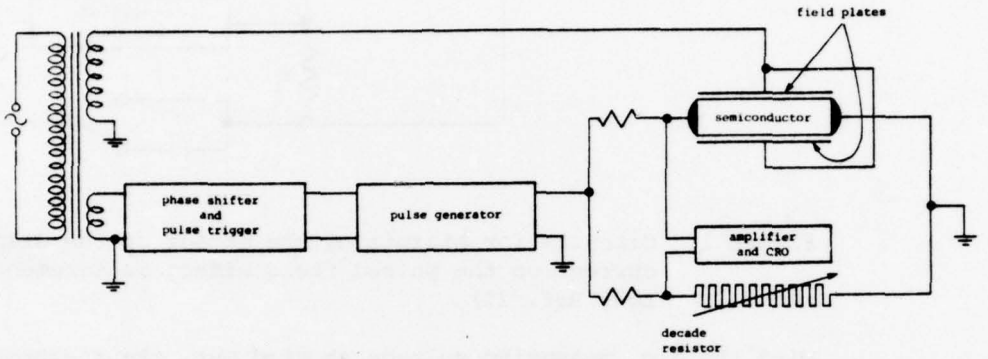


Figure 2. Pulse-activated Wheatstone bridge used for pulsed field effect measurement. (After Many and Gerlich, Ref. 24).

Harnick (Ref. 25) slightly modified the bridge circuit shown in Figure 2 in order to observe the effects of interface states. See Figure 3.

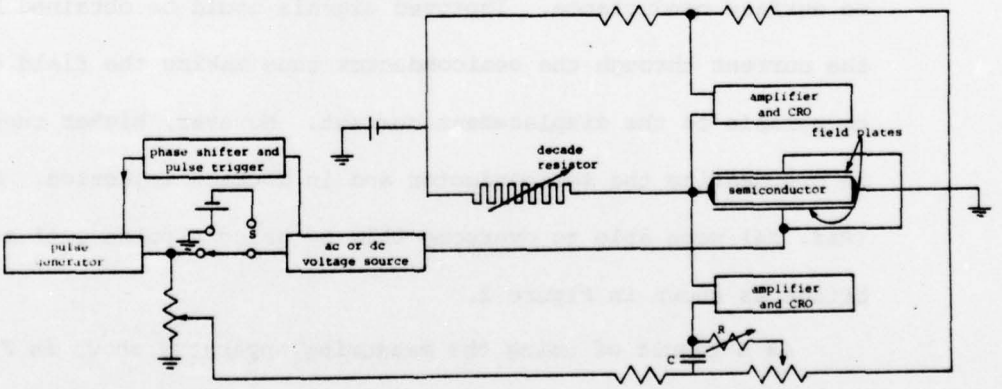


Figure 3. Modified pulsed field effect measurement to determine interface states (After Harnick et al., Ref. 25).

Note that these pulsed field effect measurements consider only majority carrier interaction. Later pulsed field effect measurements

were made which considered minority carrier effects (Ref. 25). This was done by creating an inversion layer at the surface then changing the surface potential in order to alter the minority carrier concentration in the inversion layer. This type of manipulation has an effect on majority carriers via recombination (or generation) which affects the measured surface conductance.

In the measurement techniques discussed so far, the surface conductance measurements involved the interaction of the bulk and its corresponding majority carrier density. Kingston and Statz (Ref. 26) devised an experimental measurement which isolated most of the underlying bulk from carriers at the surface. This was done by using a pnp transistor where an inversion layer was created in the base region connecting the emitter and collector regions without any rectification. Circuit in Figure 4 shows approach of Kingston and Statz (Ref. 26).

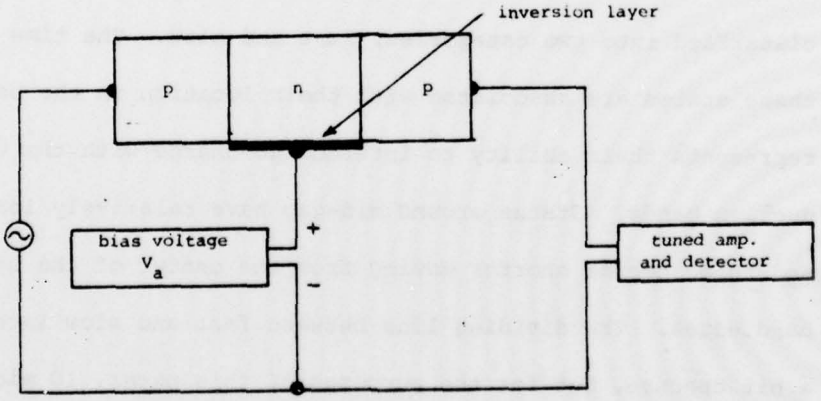


Figure 4. Circuit used to measure inversion layer channel conductance (After Statz et al., Ref. 26).

Here, the majority carrier flow was blocked by the end contacts. The bias voltage can be used to vary the surface potential of the inversion layer and any resulting change in channel conductance will be essentially that

of the surface conductance. This change in channel conductance can be used to derive the characteristics of interface states. The technology during that time made it difficult to build a device shown in Figure 4, and thus this technique was not employed extensively. It was not until the development of the MOSFET that some investigators again considered this technique for interface state analysis. Later Rupprecht et al. (Ref. 27) continued the approach by Kingston (Ref. 26) by applying this technique to MOSFETs. Rupprecht (Ref. 27) used pulsed field effect measurements in conjunction with temperature variation in order to observe interface states. Investigation of interface states in MOSFETs using the pulsed field effect technique was also done by Sequin and Baldinger (Ref. 28).

They utilized pulsed field effect measurements in order to analyze the effects of ionizing radiation on the interface state density of the MOSFET. As the investigation of interface states continued, they became classified into two categories, fast and slow. The time constants of these states are associated with their location in the band gap which represents their ability to interchange charge with the valence and conduction bands. States around mid-gap have relatively long time constants and these become shorter moving from the center of the band gap to the band edges. The dividing line between fast and slow interface states is a bit obscure, but for the purposes of this paper, 10 microseconds will be chosen. The reason being that there are fewer interface states whose time constants are greater than 10 microseconds. Also, normal switching operations in MOSFET circuitry occur at less than 10 microseconds. The area of this research is to investigate fast interface states. Sequin and Baldinger's investigation was devoted mainly to slow interface states

and the subject of fast interface states was treated briefly. Although this method for slow interface state analysis was not utilized, it is worth mentioning.

Sequin and Baldinger's (Ref. 28) technique for measuring slow interface states is merely an extension of the pulsed field effect techniques mentioned previously. Their technique consisted of choosing a gate bias whose surface potential corresponds to a certain position in the band gap. A pulse was then superimposed on the gate bias which would sweep the fermi level through some interface states. It was then necessary to measure the channel conductance during the length of the pulse in order to monitor the effects of the swept interface states. This can be done only when the device is turned "on," i.e., when the surface is inverted. Therefore, at the beginning and end of the pulse, another pulse t_m is applied which turns the device "on" and produces an output. This total applied signal is shown in Figure 5.

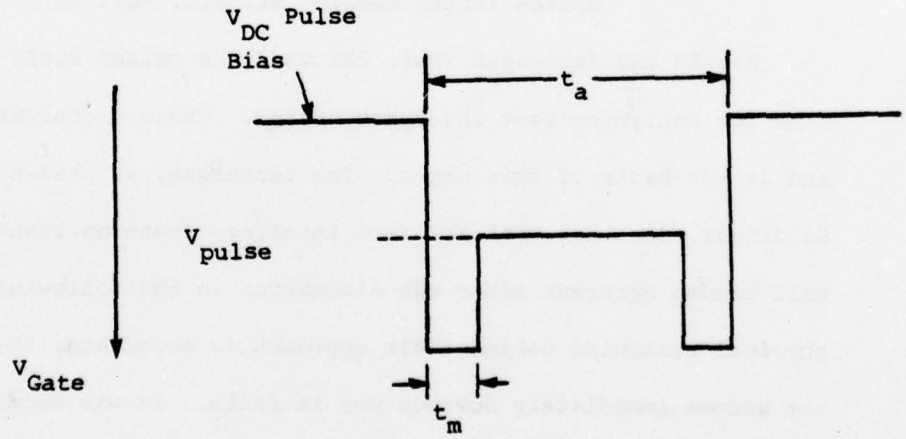


Figure 5. Applied gate pulse used to investigate slow interface states (After Sequin et al., Ref. 28).

It is assumed that only those states whose time constants are shorter than

t_a will interact during the pulse. Also, those states whose time constants are greater than t_m will not be affected by the turn-on pulse. Thus, by varying V_{DC} bias and the frequency of the pulse, Sequin and Baldinger (Ref. 28) were able to derive an energy distribution of slow interface states and their corresponding time constants. The circuit used to obtain such information is shown in Figure 6.

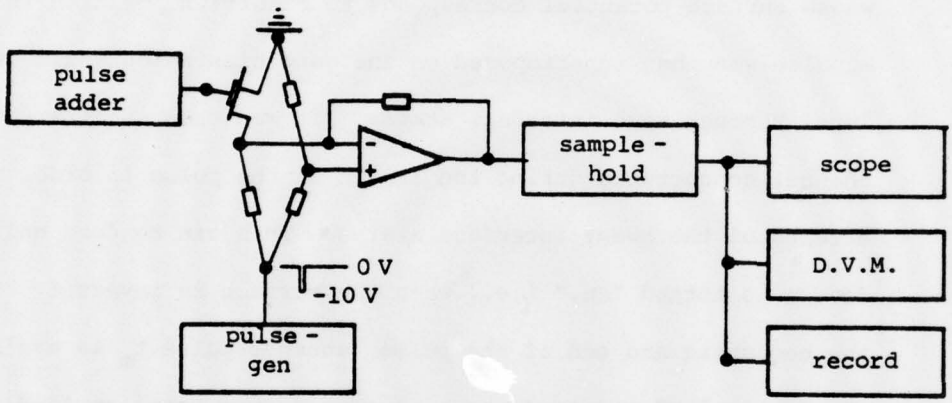


Figure 6. Circuit used for investigation of slow interface states (After Sequin, et. al., Ref. 28).

Sequin and Baldinger (Ref. 28) used the pulsed field effect measurement for analyzing fast interface states. Their technique was investigated and is the basis of this paper. The technique, as presented by Sequin and Baldinger, does not work for fast interface state analysis and the reasons will become apparent after the discussion in the following chapter. The physical reasoning behind their approach is sound and, therefore, it does not become immediately obvious why it fails. It was because of this that considerable time was spent in analyzing this technique. After much thought and analysis, a valid pulsed field effect technique evolved. This evolved technique is capable of determining fast interface states in the MOSFET. The basic circuit configuration for such a technique is shown in Figure 7.

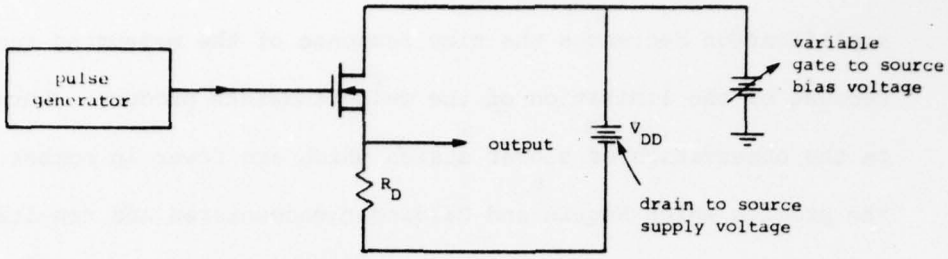


Figure 7. Basic pulsed field effect circuit used to determine fast interface states for p-channel devices.

Although the above schematic reveals a relatively simple circuit configuration, it does not reveal the sophisticated instrumentation techniques needed to obtain valid information. Before discussing the utilization of the pulsed field effect technique, some of the problems which hindered its evolution into a technique valid for present day MOSFETs will be presented.

First of all, the state-of-the-art for fabricating MOSFETs has drastically improved. What this implies is that there are orders of magnitude less interface states which may be observed for carefully manufactured MOSFETs. This in turn dictates a need for a more sensitive measurement, which produces another dilemma. As previously stated, more states exist near the band edges than at the center of the band gap, and when these are analyzed by a pulse technique, one would think it would be possible to observe a large change in channel conductance. The problem with these states is that many are faster than the risetime of the applied pulse and the time resolution of the measuring instrument at the device output. So, with these limitations, one has to resort to observing states which are a bit slower, but also fewer in number. One then amplifies the signals in order to become more sensitive to the effects of fewer states. But, there is a limit to the amount of permissible amplification since an increase in

amplification decreases the time response of the measuring instrument. Because of the limitation of the gain-bandwidth product, there is a limit on the observation of slower states which are fewer in number. This is the problem which Sequin and Baldinger encountered and resulted in observing only states around mid-gap or slow interface states.

Another problem with the pulsed field effect measurement is that the observed MOSFET response does not agree with the suggested theoretical response for an ideal MOSFET having interface states. The discrepancy is shown in Figure 8.

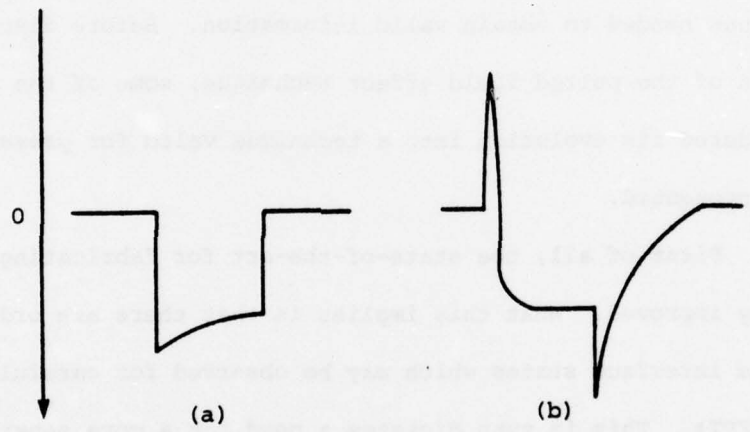


Figure 8. (a) Ideal and (b) Experimentally observed pulsed field effect responses.

The transient response in Figure 8a indicates a decrease in channel conductance due to the interaction of interface states. In order to extract interface state information from the real output response, the discrepancies between the theoretical and the experimental response must be explained.

The above problems do place serious limitations on the use of the pulsed field effect technique. In order to try and resolve these problems, the following approach was taken. It became desirable to develop a model of the observed response. This model would then provide information on

parameters which control the device response. Once these parameters are well defined, it then will be possible to see what parameters interfere with the desired device response. Then the possibility of manipulating these parasitic parameters either internally or externally will be examined. The net result being a response which contains information on density of interface states. Another benefit of such a model is that it would provide criteria for maximum gain and frequency response through minimizing parasitic parameters.

It, therefore, becomes necessary to examine such a model in depth as a solution to some of the limitations of the pulsed field effect measurements. This will be done in the following chapter.

CHAPTER IV

PULSE TECHNIQUE FOR DETERMINATION OF FAST INTERFACE STATES IN METAL-OXIDE FIELD-EFFECT TRANSISTORS

In this chapter, the circuit prescribed by Sequin and Baldinger (Ref. 28) for investigation of fast interface states will be further examined. Their technique consisted of applying a pulse to the gate of a metal-oxide field-effect transistor and observing the drain current response. This response corresponds to the channel conductance. A change in channel conductance would correspond to interface states interacting with the mobile channel conduction charge; this in turn, would provide information on the number of interface states which interact with channel conduction charge in the device. In order to maintain a fairly constant surface potential across the length of the channel, a low drain to source voltage was prescribed. Also, the linear region of device operation was recommended where there is a direct correlation between the drain current and drain to source voltage. In this region of operation, the drain current is proportional to the drain to source voltage at a given gate voltage and the constant of proportionality is the channel conductance.

Theoretically, applying a pulse would result in the corresponding drain current response shown in Figure 9. This pulse is assumed to have a finite risetime. The risetime should be fast enough to observe time constants of fast interface states. The corresponding response should also have a risetime which is fast enough to show the interaction of fast interface states with the channel conductance. The width of the pulse and the sensitivity of the measuring instrument will determine the maximum time constant of a given interface state which may be observed.

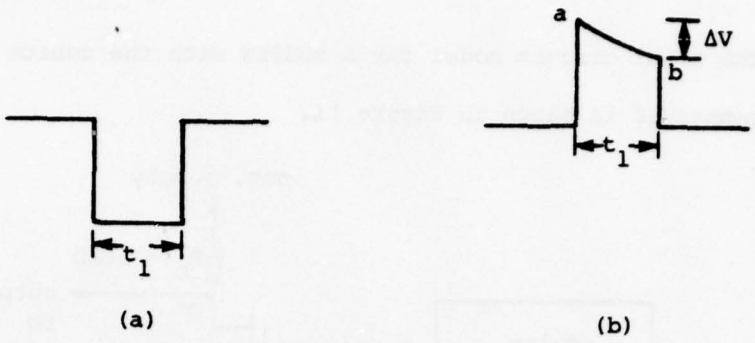


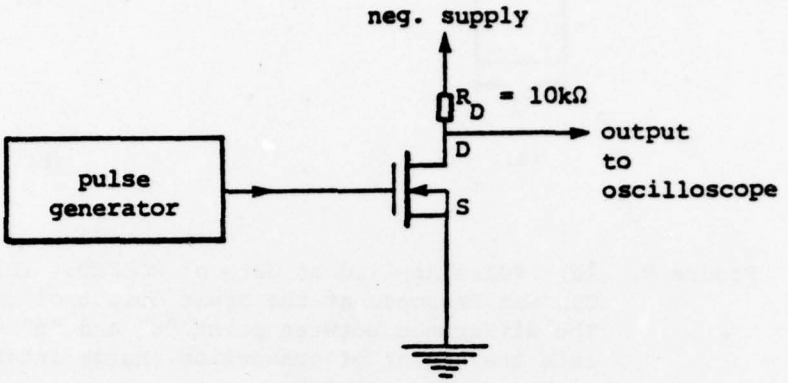
Figure 9. (a) Pulse Applied at Gate of MOSFET. (b) Drain Current Response at the Drain Output of the Device. The difference between point "a" and "b" would indicate the amount of conduction charge interacting with interface states.

The pulsed field effect technique circuit configuration and the observed response are shown in Figure 10.

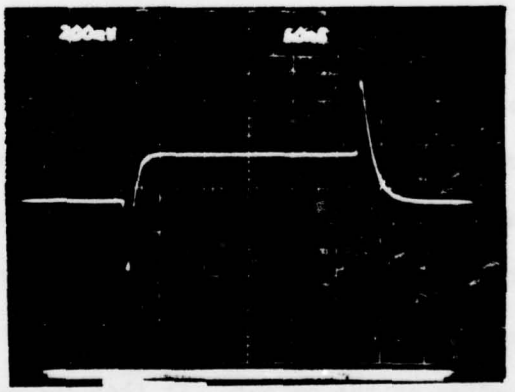
The actual response differs from the theoretical response in two ways. The device does not turn on immediately due to some transient effects. Also, once the device is turned "on," the change in conductance due to interface states may not necessarily be observed. These two effects may be interrelated.

It became necessary to make a careful examination of the experimental setup to determine what was responsible for the observed response. After a thorough analysis of both input and output signals, it was concluded that the observed response was an inherent characteristic of the device along with any loading at the output. It then became necessary to create a model for the device which would correspond to its physical parameters and explain the observed response. The model will be presented to show which device parameters are responsible for controlling the observed response.

The total circuit model for a MOSFET with the source and substrate connected is shown in Figure 11.



(a)



(b)

Figure 10. Pulse Technique Used in Determining Fast Interface States. (a) Experimental configuration using p-channel MOSFET, V_{GS} = 10 volts and V_{DS} - .2 volt. (b) Response observed at the output of the device.

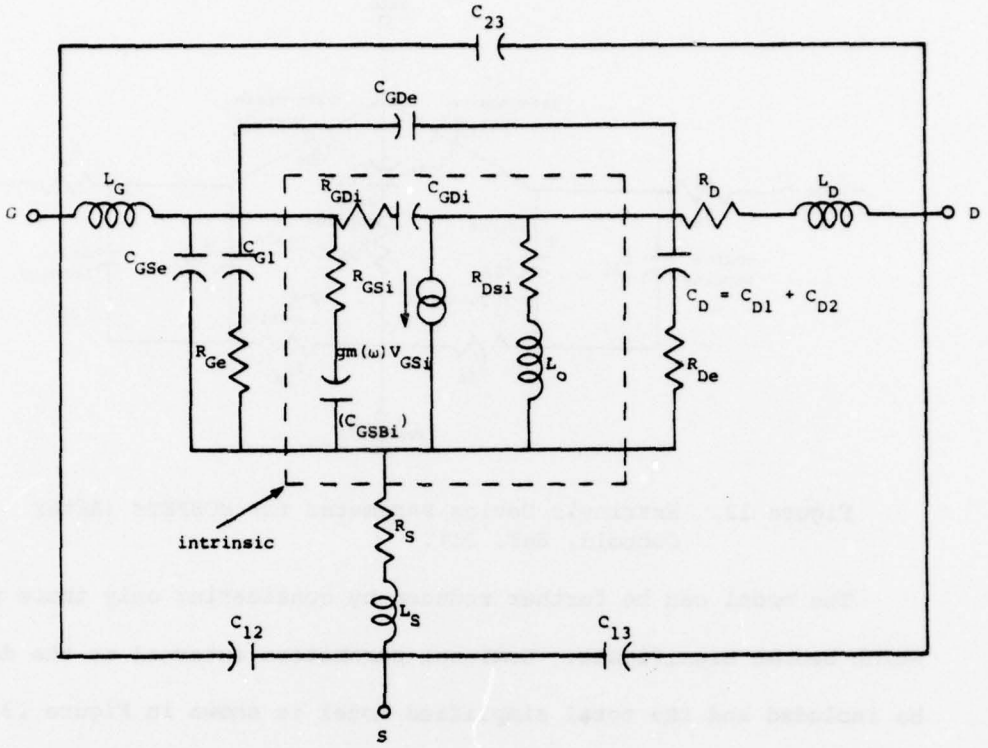


Figure 11. Total Device Circuit Model (After Cobbold, Ref. 31).

The subscripts are defined below:

G = gate

S = source

D = drain

e = extrinsic

i = intrinsic (small signal parameters)

b = bulk (substrate)

1, 2, 3 = parameters external to the device

By ignoring small signal parameters, whose effects are negligible, and noting the more significant extrinsic parameters, the above model can be reduced as shown in Figure 12.

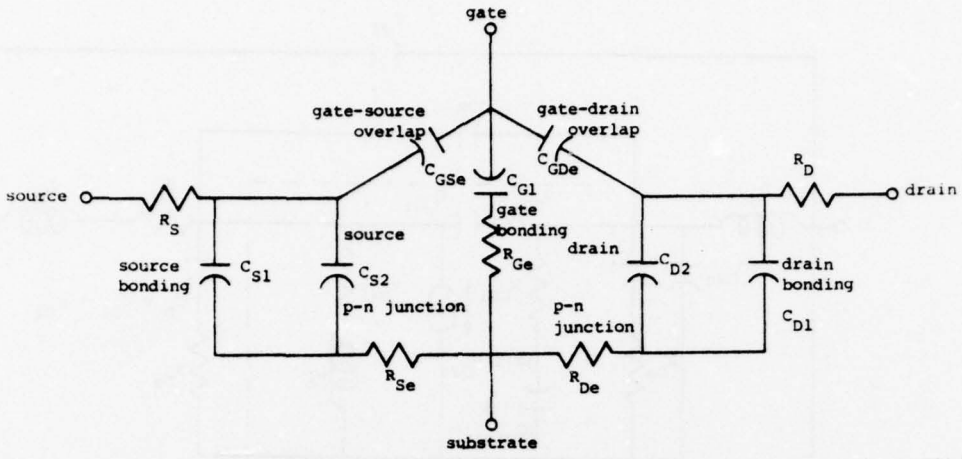


Figure 12. Extrinsic Device Parameter for MOSFETs (After Cobbold, Ref. 31).

The model can be further reduced by considering only those parameters which become significant. Dominant parameters external to the device may be included and the total simplified model is shown in Figure 13.

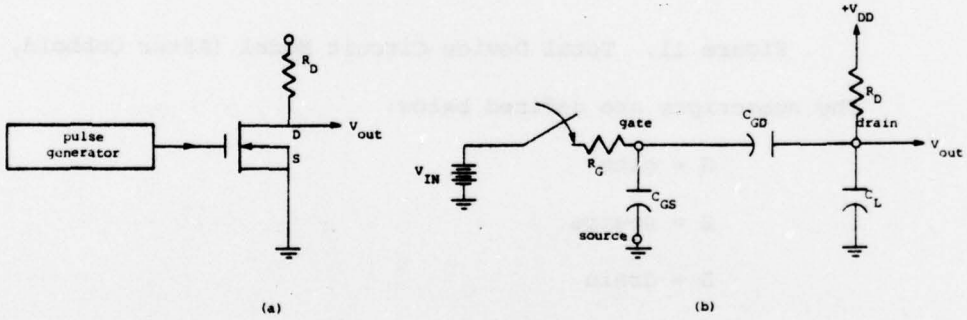


Figure 13. Approximate Model of the Pulsed Technique. (a) Circuit Configuration. (b) Simplified Equivalent Model.

The symbols for the model shown in Figure 13 are defined below.

V_{IN} = pulse input when switch closes. This is used only for analysis. Actual pulse generator was used, producing 10 V pulses with 5 nanosecond risetime, the frequency and pulse width were variable.

R_G = any resistance between pulse generator and gate of MOSFET.

$C_{GD} = C_{rss}$ where C_{rss} is the output capacitance with the input short-circuited.

$C_{GS} = C_{iss} - C_{GD}$ where C_{iss} is the input capacitance with the output shorted. Physically, C_{GD} and C_{GS} are mainly due to gate-source, gate-drain electrode overlap.

C_L = corresponds to any capacitive loading of the output. It also includes any drain to substrate capacitance which is small.

The following analysis of the simplified model provides an approximate solution which agrees with the actual response. In order to make the analysis easier, an n-channel enhancement MOSFET will be used which has positive input signal and positive drain-source supply voltage.

Start by considering $t = 0_-$ with the MOSFET off. At this point $V_{IN} < V_{threshold}$ and the channel looks like an open circuit. This means that the supply voltage (V_{DD}) will appear entirely across C_L. The output voltage at this time will verify that this is indeed the case. At $t = 0$ the voltage at the gate jumps from V_{GS_1}, where the MOSFET is "off" to V_{GS_2} which is greater than the threshold voltage necessary to turn the device "on." Since C_{GS} was initially charged, the gate voltage cannot change instantaneously to V_{GS_2}. Thus, the circuit time constant seen by the signal is

$$\tau_1 \simeq R_G \left(C_{GS} + \frac{C_{GD}\, C_L}{C_{GD} + C_L} \right) \qquad (1)$$

This is due to $R_D >> R_G$ and $C_L > C_{GD}$. Since $C_L > C_{GD}$, this will make τ_1 a fast time constant.

As C_{GS} is charging, consider what will occur at the output. At the output, C_L was initially charged to V_{DD}. As the gate pulse arrives, C_L will charge according to how a capacitive division of $V_{GS_2} - V_{GS_1}$ (ΔV_{IN}) occurs between C_{GD} and C_L. This capacitive divider of ΔV_{IN} results in

$$V_{D\ max} = \frac{C_{GD}}{C_{GD} + C_L} \Delta V_{IN} \tag{2}$$

Note that the input will divide inversely proportional to the capacitances. The output, therefore, goes from V_{DD} to $V_{DD} + V_{D\ max}$ with risetime τ_1.

Note how this will affect the experiment. The desired operating point for the device should be within the ohmic (linear) portion of the I_D vs. V_{DS} characteristic. In this range, I_D is proportional to V_{DS} yielding channel conductance as a constant of proportionality. As the channel conductance varies, it can be related to the number of interface states, as stated previously. The inverse of channel conductance, channel resistance, was used in order to calculate the proper V_{DD} to obtain the desired operating point. From the device characteristics V_{DS} = .2 volt at V_{GS_2} = 10 volts was chosen as an operating point. The operating point on the I_D vs. V_{DS} characteristic is shown in Figure 14.

The channel resistance (R_{CH}) at the operating point is 1.5 KΩ. Calculating V_{DD} in order to produce V_{DS} = .2 volt, the voltage divider equation is used across R_{CH}, assuming the load resistance (R_D) to be 10 KΩ.

$$\frac{R_{CH}}{R_{CH} + R_D} V_{DD} = V_{DS} \tag{3}$$

Solving for V_{DD},

$$V_{DD} = V_{DS} \frac{R_{CH} + R_D}{R_{CH}}$$

Substituting in values for V_{DS}, R_{CH} and R_D,

$$V_{DD} = \frac{1.5\ K\Omega + 10\ K\Omega}{1.5\ K\Omega} \times .2\ V$$

$$V_{DD} = 1.533 \text{ volts}$$

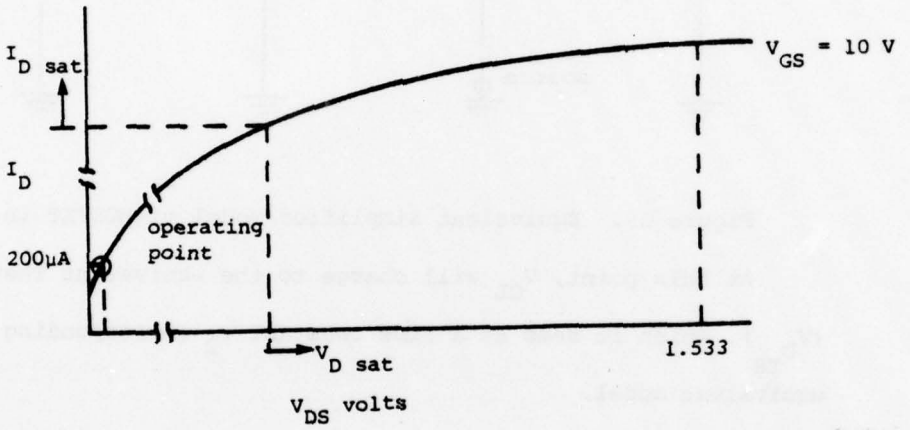


Figure 14. Operating Point Shown on the I_D vs. V_{DS} Characteristic of a MOSFET.

The V_{DD} chosen for the desired operating point forces the device into saturation before going to the linear region of operation. This can be seen from the previous analysis. Before the pulse arrived, $V_{CL} = V_{DD}$. Then, as the pulse arrived, V_{CL} charges to $V_{DD} + V_{D\ max}$ which is slightly greater than 1.533 volts which forces the device further into saturation. In other words, as soon as the device is turned on ($V_{GS_2} > V_{threshold} = 5$ volts), the output cannot change to .2 volt instantaneously due to C_L. This forces the device into a different mode of operation, that of saturation. The saturation equivalent model is shown in Figure 15.

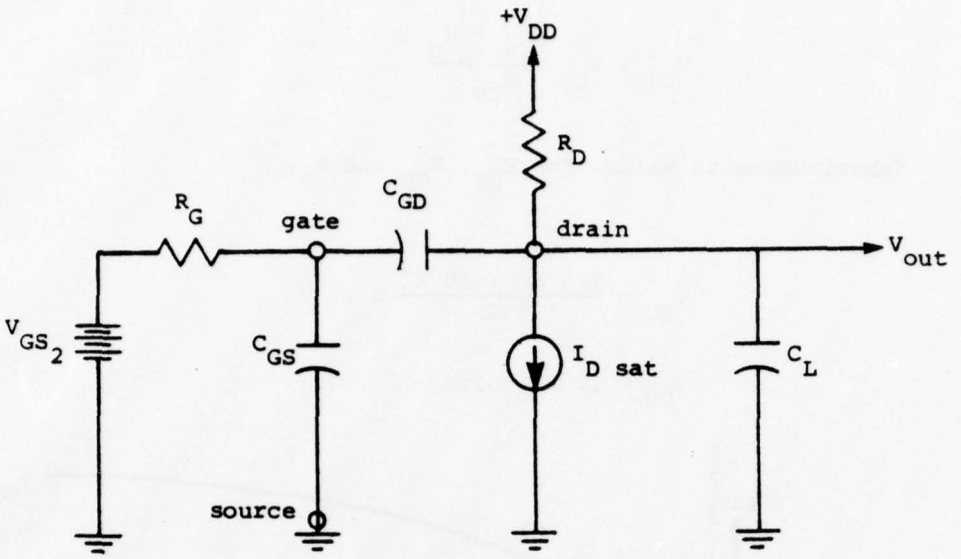


Figure 15. Equivalent Simplified Model of MOSFET in Saturation.

At this point, V_{CL} will charge to the equivalent Thevenin voltage ($V_{D_{TH}}$), which it sees at a time constant τ_2 corresponding to the new equivalent model.

$$V_{D_{TH}} = V_{DD} - I_{D\ sat}\ R_D \tag{4}$$

and $$\tau_2 \simeq R_D\ (C_L + C_{GD}) \tag{5}$$

It is now possible to write an equation for V_{CL} with initial and final conditions.

$$V_{CL}\ (\text{Initial}) = V_{DD} + V_{D\ max} \equiv \Delta V_{D\ max} \tag{6}$$

$$V_{CL}\ (\text{Final}) = V_{D_{TH}}$$

Therefore,

$$V_{CH} = V_{D_{TH}} + (\Delta V_{D\ max} - V_{D_{TH}})e^{-t_2/\tau_2} \tag{7}$$

V_{CL} will continue to go toward $V_{D_{TH}}$ until it reaches $V_{D\ sat}$ (see Figure 14). At $V_{D\ sat}$ the device enters the linear region of operation. This will occur when $V_{CL} = V_{GS_2} - V_{D\ sat}$. It is then possible to determine the time at which this will occur from the above equation for V_{CL}.

$$V_{GS_2} - V_{D\ sat} = V_{D_{TH}} + (\Delta V_{D\ max} - V_{D_{TH}})e^{-t_2/\tau_2} \tag{8}$$

$$t_2 = \tau_2 \ln \left[\frac{\Delta V_{D\ max} - V_{D_{TH}}}{V_{GS_2} - V_{D\ sat} - V_{D_{TH}}} \right]$$

At time t_2, the linear region of operation is reached and the resulting equivalent circuit shown in Figure 16.

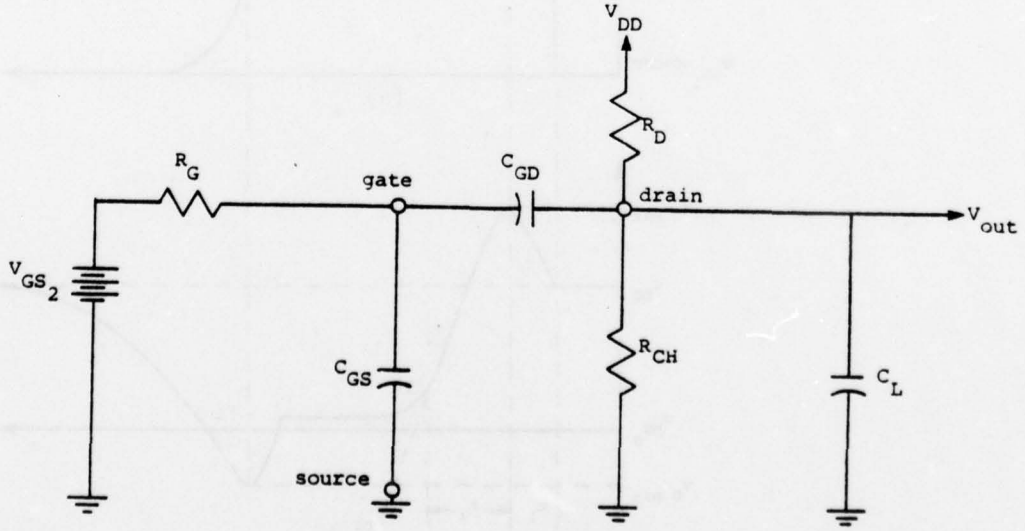


Figure 16. Equivalent Simplified Model of MOSFET in Linear Region of Operation.

Again, V_{CL} cannot change instantaneously so it will charge with a new Thevenin voltage and time constant corresponding to the equivalent circuit model.

$$V_{TH} \tilde{=} V_{DS} = \frac{R_{CH}}{R_{CH} + R_D} V_{DD} \tag{9}$$

$$\tau_3 = (R_D \,||\, R_{CH})\ (C_L + C_{GD}) \tag{10}$$

The device has now reached its desired operating point where V_{DS} = .2 volts.

Figure 17 shows the response of a MOSFET passing through various modes of operation when a pulse is applied to the gate.

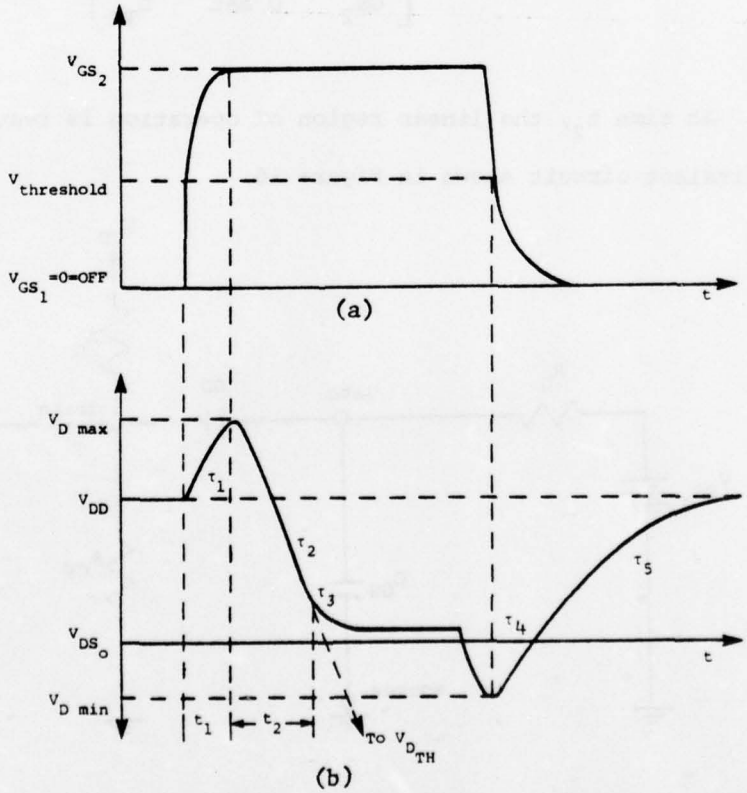


Figure 17. (a) Pulse Applied at Gate of MOSFET. (b) Analytical Response at Output of MOSFET.

Note the fast risetime overshoot response due to charging of the gate. After the gate is charged, the device heads toward $V_{D_{TH}}$ with a time constant of τ_2 while in saturation. Along the way it reaches the linear operating region. In this region the device reaches $V_{DS} = 0.2$ volt with a time constant of τ_3. After leveling off at $V_{DS} = 0.2$ volts, the device is then turned "off." At this point, V_{CL} will follow the fall of the gate voltage with a time constant of τ_4 until it reaches V_D min.

Where $$V_{D\ min} = V_{DS} - \frac{C_{GD}}{C_{GD} + C_L} (V_{GS_2} - V_{GS_1}) \tag{11}$$

$$\tau_4 \simeq (R_D \,||\, R_{CH})\ (C_L + C_{GD}) \tag{12}$$

As V_{GS_2} goes to zero, R_{CH} becomes infinite, thus causing the drain voltage to decay to V_{DD} with a time constant of τ_5.

$$\tau_5 \simeq (R_D)\ (C_L + C_{GD}) \tag{13}$$

This analytical solution, although approximate, corresponds to the actual response observed. It describes a static case where any effects due to interface states are ignored and only large signal circuit parameters are considered. Also, by changing C_L and R_D, a response predicted by this analysis is obtained. Typical values are given for the parameters involved in this analysis.

2N4120 P-channel MOSFET

R_G = less than 1 ohm

C_{GS} = 2.2 pF typical, 3.8 pF maximum

C_{GD} = .3 pF typical, .7 pF maximum

$R_{CH} \tilde{=}$ 1.5 k-ohms at V_{GS_2} = 10 volts

R_D = 10 k-ohms

C_L = relatively undefined quantity because there are many parasitic effects which would capacitively load the device.

In summary, the response to a pulsed MOSFET has been well-defined. Because of this, it is now possible to try and minimize the parasitic effects involved in the response. The attempt in doing this is to obtain a response which will correspond directly to a change in channel conductance.

CHAPTER V

MINIMIZATION OF PARASITIC PARAMETERS IN THE PULSED FIELD EFFECT MEASUREMENT

In the previous chapter, circuit parameters were defined which are responsible for the output response of a MOSFET when a pulse is applied to the gate. The model did not take into consideration the interaction of interface states. Several other techniques have verified the existence of interface states in MOS structures. The question arises, why are not these interface states readily observable when using the pulsed field effect technique on the MOSFET? After some thought, it becomes apparent that the turn-on time is not fast enough to observe interface states whose time constants are short, but greater in number. By sweeping through these interface states, their density should produce an observable effect at the output of the device. In the following discussion, parasitic parameters which can be minimized and improve the device turn-on time will be considered. The model showing large signal circuit parameters is shown in Figure 18.

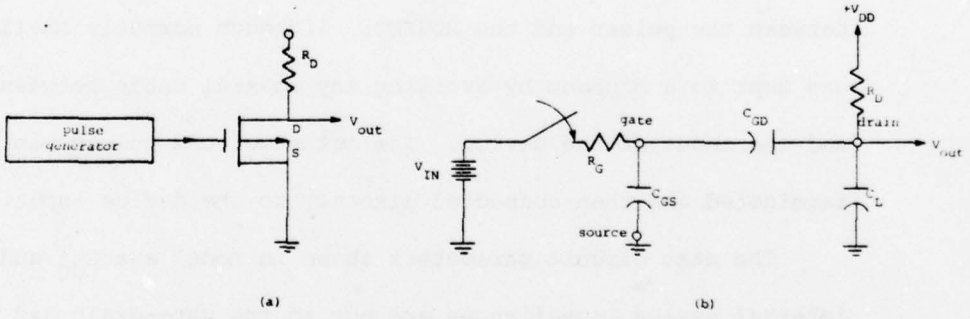


Figure 18. Large Circuit Parameters in the Pulsed Field Effect Measurement.

First of all, it is necessary to examine the applied pulse. Ideally, the pulse generator should have a risetime which is faster than the time constant of any of the interface states or at least as fast as the

circuit time constants which interfere with the measurement. This is not possible since interface states close to the band edge have time constants on the order of picoseconds, which is faster than most pulsers. Also, it is not possible to get any information out of a device until a channel is formed. The time necessary to form a channel is dependent on the distance between the source and drain regions. According to Zahn (Ref. 21), a MOSFET whose channel length is 20 μm takes more than one nanosecond to form and provide a current output. This is for an ideal device having no parasitic resistance or capacitance device parameters, so picosecond risetime pulsers are not required. Another criteria for the applied pulse is that it be well defined and flat. Mercury switched pulsers, whose risetimes are approximately one nanosecond, are normally used for fast switching applications. This type of pulser was considered, but abandoned since its signal had considerable noise. The HP 8003A pulse generator whose risetime is five nanoseconds was chosen. This pulser proved to be adequate for this analysis.

In the model shown in Figure 18, there is a series resistance R_G between the pulser and the MOSFET. Although normally small, its value was kept to a minimum by avoiding any coaxial cable between the pulser and the input of the device. The output of the pulser was properly terminated and then connected directly to the device input.

The next circuit parameters shown in model are C_{GD} and C_{GS}. These internal device capacitances are due to the gate-drain and gate-source electrode overlap. The amount of overlap capacitance is dependent on the method of fabrication. Industry has minimized these effects by using various techniques such as a self-aligned gate through the use of ion implantation. It, therefore, became necessary to purchase devices

whose specifications for C_{rss} and C_{iss} were at a minimum. C_{rss} and C_{iss} are directly related to C_{GD} and C_{GS} as stated in the previous chapter. A test die containing several devices including a standard MOSFET was built in order to do some correlative interface state analysis. The MOSFET on the test die, due to its slow turn-on time, was not usable for pulsed field effect measurements. The turn-on was approximately ten times slower than commercially available MOSFETs. The available state-of-the-art for fabricating these devices yielded unwanted gate-drain and gate-source capacitances. Also, the distance between source and drain did not allow fast channel formation which contributed to turn-on delay.

The drain load was a significant parameter which slowed the turn-on of the device, so it became desirable to minimize the load without considerable loss to signal output. A method of minimizing loading effects and providing an adequate signal output was the use of a transimpedance amplifier. The concept of such an amplifier is shown in Figure 19.

In normal application, the non-inverting input of the operational amplifier is connected to ground producing a virtual ground at the inverting input. By placing a voltage at node 2, node 1 will try to maintain the same potential as node 2 regardless of the current input. This will allow the drain-source voltage to be a constant value regardless of the mode of operation of the MOSFET. The resistive load will be zero while the amplification will be I_D x (1000 ohms). Commercially available operational amplifiers do not have the frequency response for this transimpedance application. Therefore, an operational amplifier built of discrete components which used high frequency transistors was constructed.

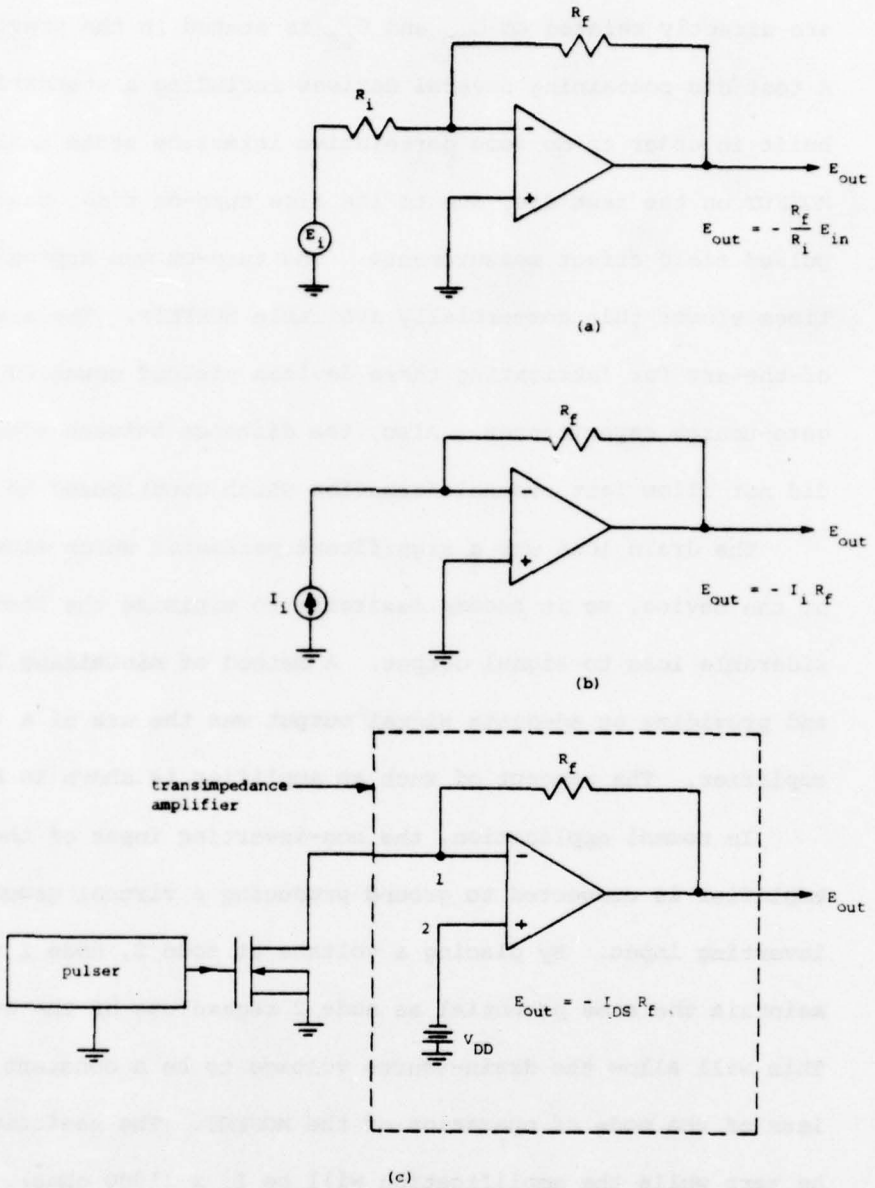


Figure 19. Operational Amplifier used in Transimpedance Configuration. (a) Typical voltage gain amplifier. (b) Replacing E_i and R_i with a constant current source. (c) Using MOSFET as a constant current source and using supply voltage at non-inverting input in order to provide drain to source voltage.

The final transimpedance amplifier is shown in Figure 20.

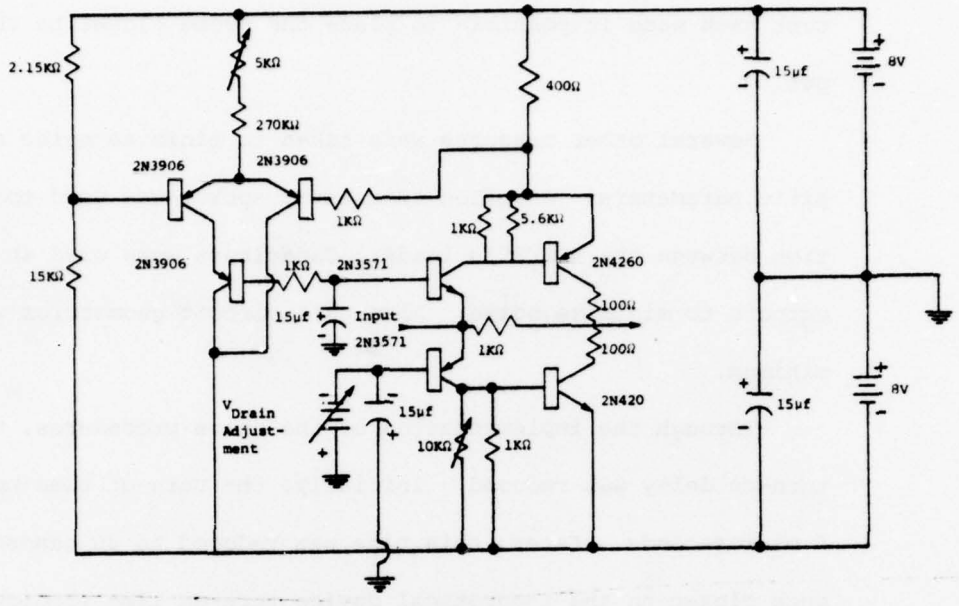


Figure 20. Transimpedance Amplifier Circuit (After Kelly, Ref. 29)

Noise and certain circuit instabilities produced in the above circuit led to its abandonment. Although the transimpedance approach is still a very promising one, time did not allow its perfection. Another approach consisted of lowering the value of the load resistor until the output signal to noise ratio became a problem. Also, noise was minimized by using a metal film resistor instead of a carbon resistor. A 500-ohm metal film resistor proved to be the best resistive load.

Another very significant device parameter is any capacitive loading at the output of the device. The oscilloscope probe and amplifier are main contributors of capacitive loading. By using a special Tektronix plug-in amplifier, the capacitive loading was minimized. This amplifier has an active probe which has a total capacitance of 5.8 picofarads at 5 millivolt sensitivity. The probe comes with a BNC connector adapter which has a capacitive loading of 1.2 picofarads. Using a special probe

test jack eliminated the BNC adapter and its capacitive loading. The test jack made it possible to place the probe closer to the device output.

Several other measures were taken to minimize noise and other parasitic parameters. A Teflon transistor socket was used to improve isolation between the MOSFET's leads. Capacitors were used at power supply outputs to minimize noise. Also, all circuit geometries were kept at a minimum.

Through the implementation of the above procedures, the device turn-on delay was reduced. Initially, the turn-on time was approximately 5 microseconds. Later, this time was reduced to 30 nanoseconds which is much closer to the theoretical device turn-on time predicted by Zahn (Ref. 22).

Once the MOSFET turn-on time was reduced, a transient response representative of the interaction of interface states was observed. An analysis continued which permitted varying the operating condition of the MOSFET and noting its effects on the observed channel conductance response. By doing this, several interesting phenomena occurred. The most important of these being that the interface state information was produced at the output only when the device was operating in the saturation region. Operating in the linear region produced no change in the observed channel conductance response. A possible explanation for this becomes apparent when examining the differences between linear and saturation pulse conditions. In the linear region, an applied "turn on" pulse, which corresponds to a change in surface potential, will cause carriers to be drawn from both source and drain to establish a channel. This may be easily seen by drawing appropriate band diagrams for a device. The channel drift current and the carriers injected from the

drain to enhance or establish the channel will constitute currents in opposite directions and these currents tend to cancel each other. This effect would tend to minimize any transient drain signal used to observe fast interface states and would unduly complicate analysis since both types of response times are very small. On the other hand, when a device is suddenly pulsed "on" in the saturation region, only the source contact supplies significant charge to establish a channel and the current observed at the drain is principally channel drift current. This channel drift current will contain a transient component which corresponds to the equilibration of those "fast" interface states which are slow enough to be resolved by the instrumentation.

In the process of pulsing the gate, several things occur:

1. A channel is established which changes the surface potential and allows many surface states to swing past the previous Fermi level in the channel without immediately reaching thermal equilibrium.
2. The channel decreases length early in the pulse, leaving unequilibriated surface states previously in the channel within the depletion region between the channel and the drain.
3. The depletion region encompassing the drain contact, the channel and the source must change its configuration.

Experimental data indicate that it is the trapped carriers within channel which produce the transient effect observed in the measurement. The transient effect of fast interface states cannot be measured when a gate is pulsed at sufficiently high voltages. Under this condition, the channel is very heavily inverted. Since the recombination rate of interface state change is directly proportional to channel carrier

concentration (or the life time is inversely proportional to channel carrier concentration) one might expect that with high voltage gate pulses, most of the interface states would equilibrate in times too short to be observed. The observed changes in channel conductance were radiation dependent and such data will be provided in a later chapter. The final pulsed field effect circuit configuration is shown in Figure 21.

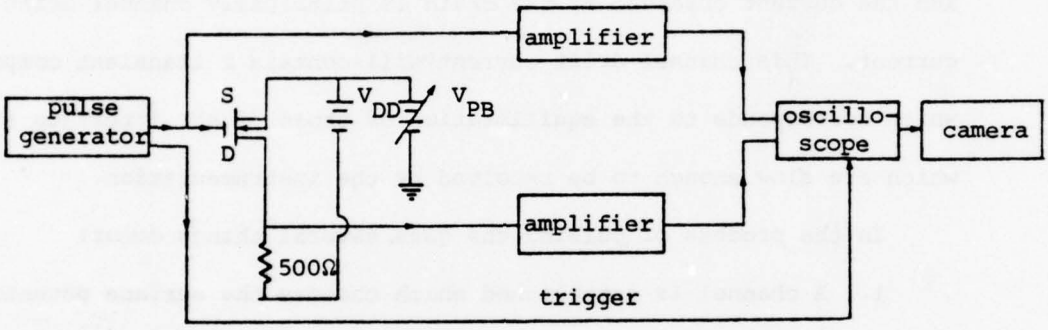


Figure 21. Schematic of Pulsed Field Effect Experimental Layout

The schematic shows little difference between this pulsed field effect technique and that presented by Sequin and Baldinger (Ref. 28). The most observable difference is in the load, which, if left at the original 10K ohm value, would have prevented any observation of fast interface states. What the above schematic does not show are all the techniques used to minimize parasitic effects. Also, Sequin and Baldinger claimed to have observed the desired response in the linear region of operation which was proved to be in error.

Now that a pulsed field effect technique has been shown to produce interface state information, it becomes desirable to make some qualitative and quantitative physical correlations. In the following chapter, such correlations of experimental procedure and device physics will be made.

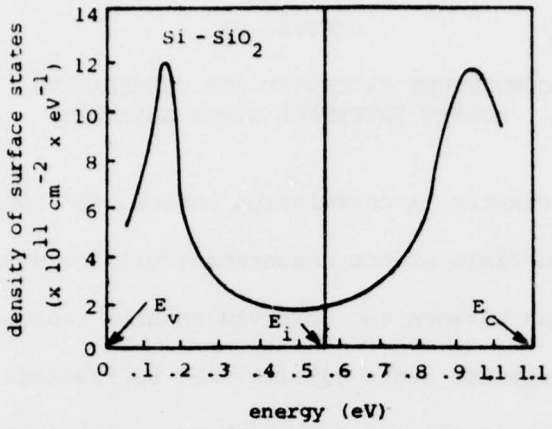
CHAPTER VI

CONSISTENT PROCEDURE FOR CORRELATIVE MOSFET INTERFACE STATE ANALYSIS

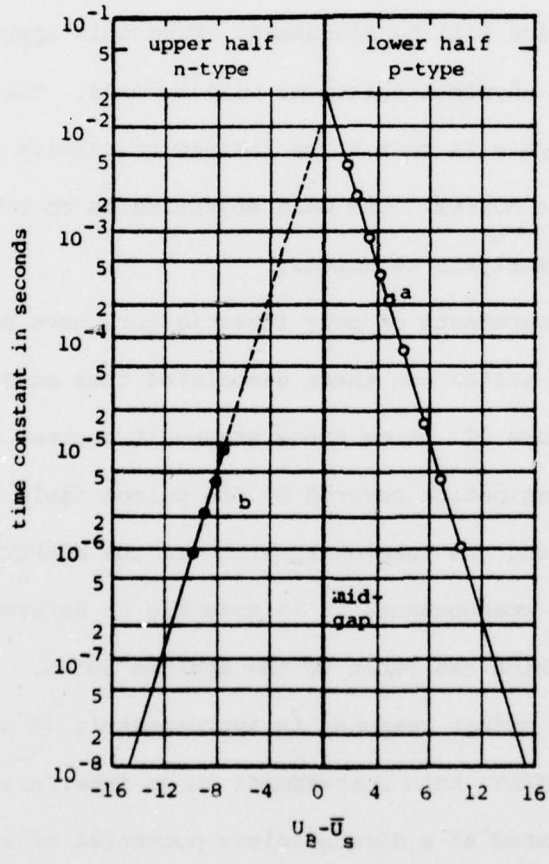
In this chapter, a correlation between the MOSFET's device physics and the pulsed field effect measurement will be discussed. Specifically, the correlation between the observed channel conductance response and the MOSFET interface state density will be treated. This is not an attempt to explain all effects which may occur in the metal-oxide-silicon system. Rather, the qualitative effects which agree with well documented surface physics will be discussed. From this approach, all possible quantitative physical relations will be made. The major constraint in such an analysis is that it be limited to results which are derivable only from the MOSFET. The main objective is to have a physically consistent MOSFET analysis technique.

The measurements of many investigators have produced the spectrum of interface states and their associated time constants in MOS structures shown in Figure 22. From these graphs it becomes desirable to locate the area of investigation covered by the pulsed field effect technique.

By knowing the turn-on risetime of the MOSFET during the pulsed field effect measurement, it is possible to determine the fastest interface state which can react to the applied pulse. Typical risetime for pulsed field effect response is approximately 30 nanoseconds. For a p-channel MOSFET, this corresponds to an interface state time constant which is located at a dimensionless potential of approximately -13.2 on the graph shown in Figure 22b. Converting into units of electron volts (eV) gives a value of approximately .21 eV from the valence band edge.



(a)



(b)

Figure 22. (a) Surface State Density of a Si-SiO_2. (b) Variation of Time Constants vs. Surface Potential. (After Nicollian and Goetzberger, Ref. 14).

Thus, the approximate location of the fastest observable interface states in the band gap is determined. It is also possible to define the area of investigation in the band gap. The sensitivity of the pulsed field effect measurement makes possible the observation of a change in channel conductance through approximately 800 nanoseconds. Therefore, the lower limit of investigation is approximately 10 (dimensionless potential) on the graph shown in Figure 22b. This corresponds to approximately .3 eV from the valence band edge. Therefore, the portion of the band gap being investigated corresponds to fast interface states between approximately .2 eV and .3 eV in the band gap. The band diagram in Figure 23 shows the relation of the various areas of interface state analysis using different techniques.

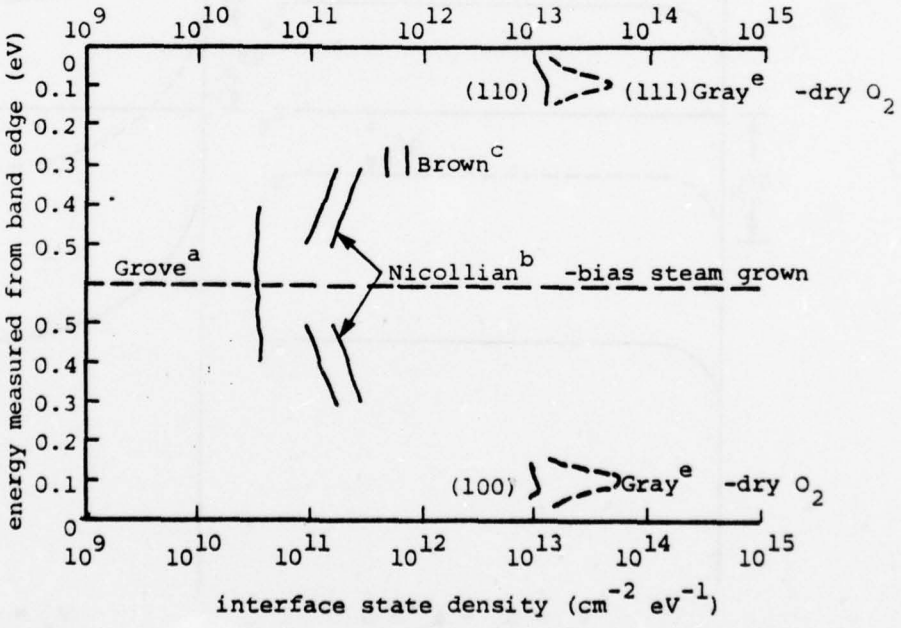


Figure 23. Oxide Silicon Interface State Densities (Ref. 32).

Figure 23 shows that the field effect technique is definitely scanning fast interface states which are not detectable using standard C-V

analysis or the more sophisticated conductance measurements by Nicollian and Goetzberger (Ref. 14).

The above conclusion indicates a specific area of investigation for using the pulsed field effect technique. It is now necessary to devise a method so that this area of investigation is consistent when a group of devices, which are generically the same, are tested. This can be done only when the change in surface potential, due to the applied pulse, sweeps the same portion of the band gap. The band diagram shown in Figure 24 shows what happens when a pulse is applied to the surface of the device.

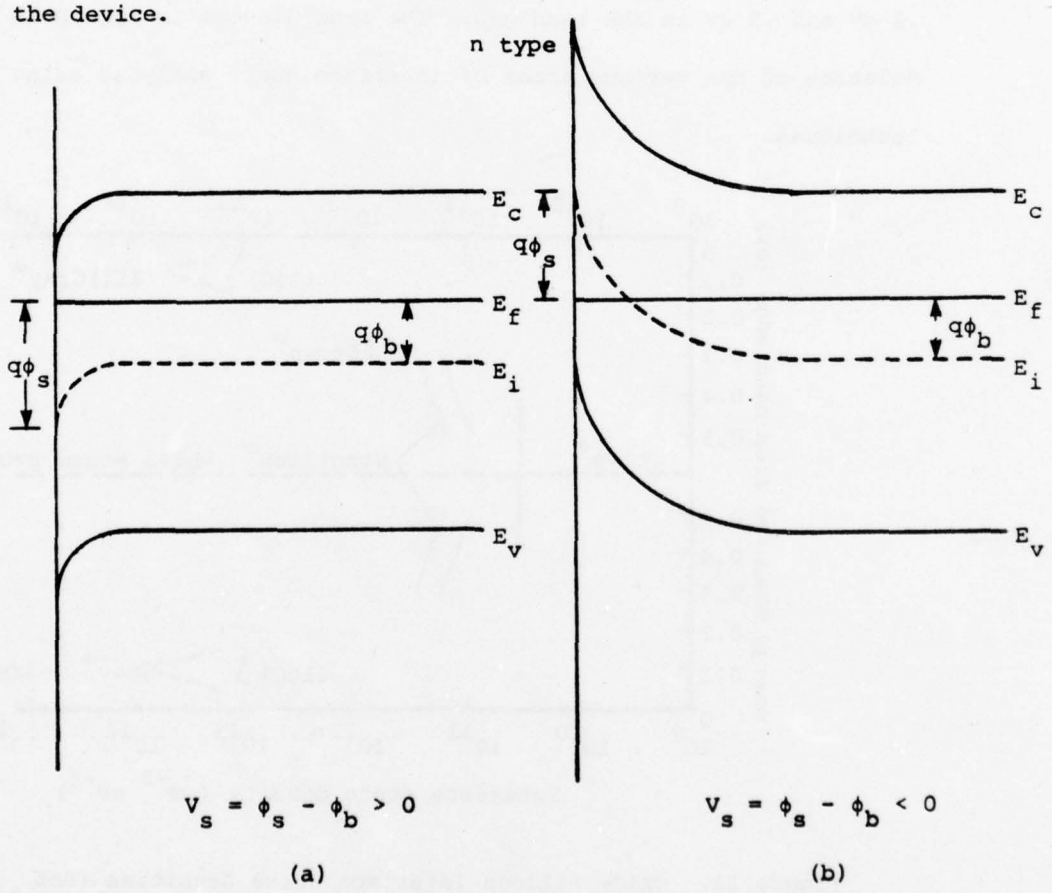


Figure 24. Simplified Energy Band Diagram for an n-type Silicon MOS Structure Showing Effects of (a) $V_G = 0$, (b) $V_G < 0$.

If all the MOSFETs in a particular test run were truly identical, the pulsed field effect technique would be relatively simple. A pulse of the same amplitude would be applied to each device and the observed responses would be identical. This is not the case for most devices. The problem is that, although these devices may be geometrically identical, variations in the interface during the same processing run can change the surface characteristics of each device. The most important of these is the fixed positive charge in the oxide which determines the distance of the band edges from the fermi level at the surface. In other words, the surface potential can be slightly different in each device before the application of identical pulses. This would cause the final surface potential due to the applied pulse to be different in each device. If the final surface potential of each of the devices is not identical, then the gate pulse causes the fermi level to be swept through different portions of the energy band gap. Although this would yield some interface-state data, it would not provide any means of comparing the devices with each other. This problem should be alleviated by superimposing the pulse upon a d.c. bias and observing the output. The amplitude of the applied pulse is not changed. When observing the output of several devices, one notices different amplitudes which correspond to the different final surface potentials. Consider the outputs shown in Figure 25.

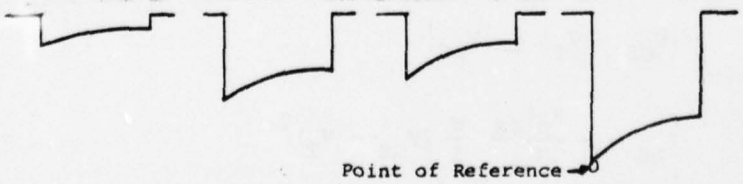


Figure 25. Various Pulsed Field Effect MOSFET Responses from Identical Inputs on Different Devices which are Generically the Same.

The largest leading edge amplitude of the response is chosen as a point of reference. The d-c bias is then adjusted on the other two inputs until the leading edge amplitude is identical for each device. This procedure assures that the portion of the band gap under investigation is consistent for each device. The observed response corresponds to an integral interface state effect and it does provide a method of comparing the interface states in identically manufactured devices.

It has been speculated that the density of "fast" interface states in an unirradiated sample may give an indication of the threshold voltage shift caused by radiation in a MOSFET. So in order to do some correlative measurements between fast interface states and the threshold voltage a method is needed to measure the threshold voltage ($V_{THRESHOLD}$).

First of all we have to define what is meant by $V_{THRESHOLD}$. $V_{THRESHOLD}$ corresponds to a surface potential which forms a channel whose majority carrier density at the surface is equal to the majority carrier density in the bulk of the material. A band diagram showing $V_{THRESHOLD}$ is shown in Figure 26C.

From the drain to source current expression (I_{DS}, Ref. 31) for a MOSFET in saturation one can extrapolate $V_{THRESHOLD}$. The saturated region for p-channel device is defined by

$$|V_{GS} - V_T| \leq |V_{DS}| \tag{14}$$

$$I_{DS} = - \frac{\mu_p \epsilon_{ox}}{2t_{ox}} \frac{W}{\ell} (V_{GS} - V_T)^2 \tag{15}$$

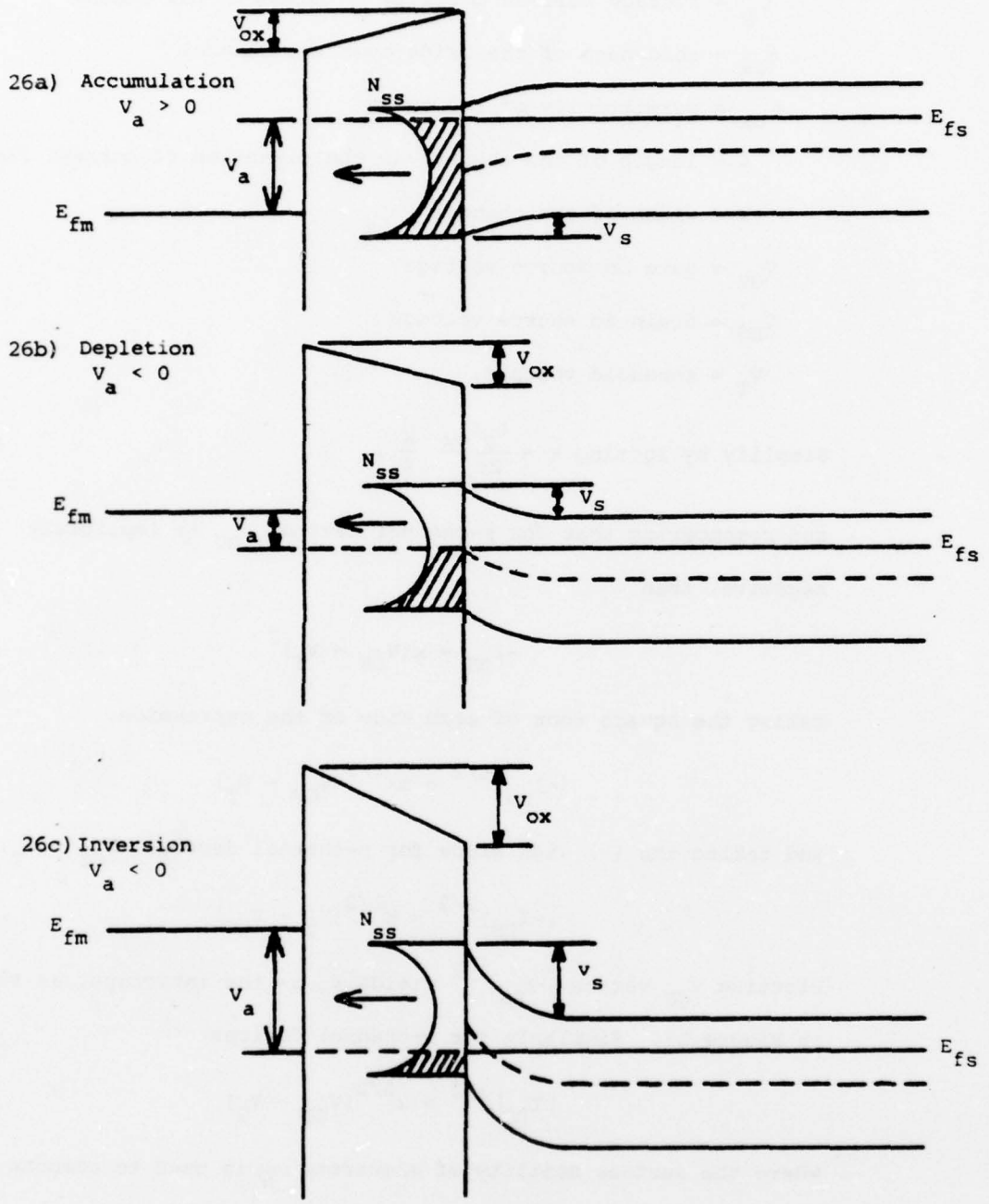


Figure 26. Band Diagrams for P-Channel MOSFET. a) Accumulation, b) Depletion, c) Threshold, with Hypothetical Surface State Distribution, N_{ss}.

where

μ_p = average surface mobility of holes in the channel

t_{ox} = thickness of the oxide over the channel

ε_{ox} = permittivity of the oxide

ℓ = length of the channel in the direction of current flow

W = width of the channel

V_{GS} = gate to source voltage

V_{DS} = drain to source voltage

V_T = theshold voltage.

Simplify by letting $k = \frac{\mu_p \varepsilon_{ox}}{2t_{ox}} \frac{W}{\ell}$, (16)

and remembering that for p-channel devices I_{DS} is implicitly negative, then

$$-I_{DS} = k(V_{GS} - V_T)^2 \tag{17}$$

taking the square root of each side of the expression,

$$(-I_{DS})^{1/2} = \pm k^{1/2}(V_{GS} - V_T) \tag{18}$$

and taking the (-) sign since for p-channel devices, $V_{GS} < V_T$;

$$|-I_{DS}|^{1/2} = k^{1/2}(V_T - V_{GS}) \tag{19}$$

Plotting V_{GS} versus $|-I_{DS}|^{1/2}$ yields V_T as the intercept, as shown in Figure 27. Similarly for n-channel devices

$$|I_{DS}|^{1/2} = k^{1/2}(V_{GS} - V_T) \tag{20}$$

where the surface mobility of electrons μ_n is used to compute k in this equation.

Measurements of I_{DS} (saturation) versus V_{GS} yield a convenient method for measuring $V_{THRESHOLD}$.

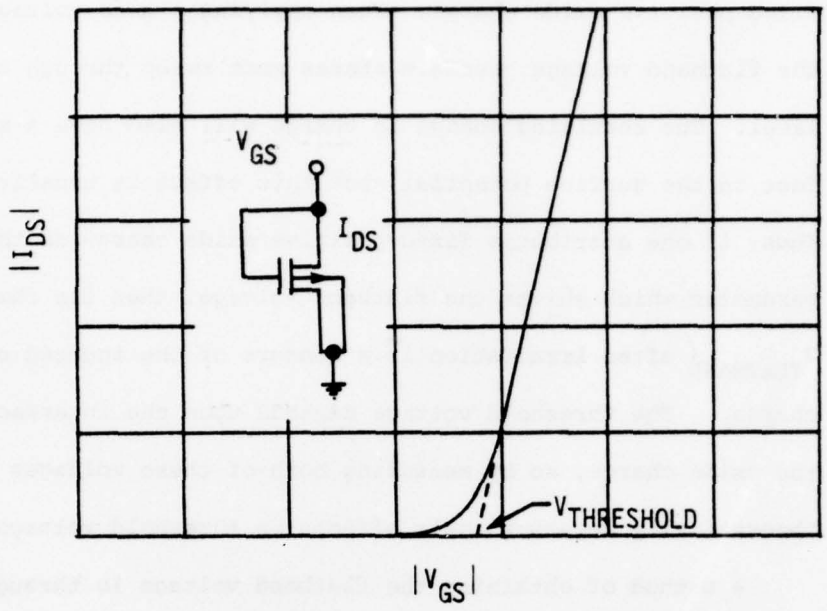


Figure 27. Typical curve for $|I_{DS}|^{1/2}$ vs. V_{GS} for saturated MOSFET operation

Physically there are two effects which influence the value of $V_{THRESHOLD}$. These two effects are the fixed positive charge in the oxide and the density of interface states. Both of these effects must be overcome when applying a gate voltage whose surface potential corresponds to $V_{THRESHOLD}$. After irradiation it becomes necessary to determine which of these two effects are responsible for a shift in threshold voltage. Therefore a method of monitoring one of the effects separately is extremely helpful.

One method of doing this is to measure the flatband voltage of the device. The flatband voltage is the applied gate voltage whose corresponding surface potential overcomes any surface band bending such that the bands are flat out to the surface of the

device. The gate voltage necessary to do this must overcome all fixed positive oxide charge. When applying a gate voltage such as the flatband voltage, surface states must sweep through the Fermi level. The resulting change in charge will also have a small effect on the surface potential, but this effect is usually ignored. Thus, if one attributes fixed positive oxide charge as the main parameter which shifts the flatband voltage, then the change in $V_{FLATBAND}$ after irradiation is a measure of the induced oxide charge. The threshold voltage depends upon the interface states and the oxide charge, so by measuring both of these voltages one can theoretically separate their effects on threshold voltage.

A method of obtaining the flatband voltage is through a capacitance-voltage (C-V) plot. As discussed in a previous chapter, C-V measurements on MOSFETS produce only low frequency plots and are therefore not very meaningful for interface state analysis. This is because the source and drain regions act as continuous sources of charge regardless of the applied signal frequency. But, from a low frequency plot it is possible to derive an approximate flatband voltage. The flatband voltage derived from a C-V plot for real and ideal devices differs slightly due to some interface state interaction (Ref. 32). But this is of no great concern since there is more interest in the shift in flatband voltage rather than its precise value. The capacitance derived from the onset of depletion is called the flatband capacitance and is shown in Figure 28.

It is possible to determine the shift in flatband voltage by

measuring the amount of translational movement of the C-V plot along the V_{GS} axis.

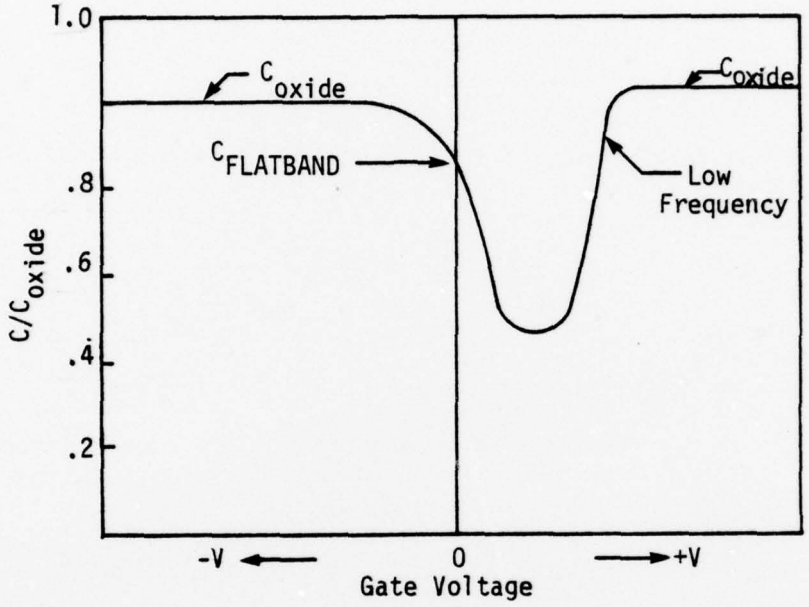


Figure 28. MOS capacitance-voltage curve at low frequency (Ref. 32)

We have established a systematic approach at making some correlative interface state analysis on the MOSFET. This procedure includes the making of pulsed field effect measurements along with $V_{FLATBAND}$ and $V_{THRESHOLD}$ measurements. Data obtained through this process should give a better understanding of the MOS interfacial system.

This approach was used successfully in generating radiation effect data. Measurements were made on both p and n channel devices. The devices were irradiated at increasing levels of radiation with measurements made between each exposure. This provides

an indication of the effects of increased radiation levels on pulsed field effect, $V_{THRESHOLD}$ and $V_{FLATBAND}$.

CHAPTER VII

EXPERIMENTAL PROCEDURES AND RESULTS

This chapter presents the experimental procedures and results for obtaining pulsed field effect data, $V_{THRESHOLD}$, and $V_{FLATBAND}$ data before and after irradiation. Some attempts to correlate pulsed field effect measurements with changes in flatband and threshold voltages are also presented.

Early Experiments

Early experiments involved examination of various techniques to observe the pulsed field effect responses from experimental MOSFET devices. One plan included correlation of data obtained from investigations reported in Volume I with pulsed data. Unfortunately the electrode overlap capacitances of these devices were so large that the turn-on time of these devices was much longer than the lifetimes of interface states and together with sensitivity limitations and signal-to-noise ratios it was impossible to perform studies with these devices. We discovered that a complete redesign of test devices would have been required, involving techniques to minimize electrode overlap capacitances. This proved to be impractical and too costly, although this was a very scientific way to proceed and should be considered for future work, considering the following results presented in this chapter.

Intermediate Experiments

A set of intermediate experiments was then performed to determine the proof of concept of using the pulse technique to obtain

a qualitative measure of fast interface states in off-the-shelf devices. In these experiments, a pulsed field effect measurement procedure was developed which formed the basis for certain final measurements including the correlation of pulsed field effect responses with radiation induced changes in flatband and threshold voltages. We shall first describe the intermediate experiments and proceed with the results of the later measurements in the next section.

This procedure was followed before and after each irradiation. A Cobalt 60 radiation source was used and each device was irradiated at 1×10^5 rad-silicon, 1×10^6 rad-silicon, and finally, 1×10^7 rad-silicon. In these experiments all device terminals were tied together during irradiation.

The schematic shown in Figure 21 shows the experimental layout. The major components of the above schematic are defined below:

Pulse Generator - Hewlett Packard 8003A pulse generator. Has 5 nanosecond risetime with variable pulse width and repetition rate.

V_{DD} - Power supply which maintains constant voltage across the device and load.

V_{PB} - Power supply which is used to shift the d.c. level of the applied pulse.

Amplifier - Tektronix 7A11 plug-in unit for 7700 series oscilloscope. Has an active FET probe and probe test jack.

Oscilloscope - Tektronix 7704. Has 150 megahertz band width

when used with 7A11 plug-in unit. Risetime resolution is 2.4 nanoseconds.

Camera - Tektronix C-40 camera with 1:.085 object to image ratio.

The experimental procedure is as follows:

(1) Adjust V_{DD}, power supply so that the device is maintained in saturation. Normally, 10 volts is adequate.

(2) Adjust the pulse generator to produce a pulse whose width is five microseconds and repeats twenty microseconds later. Five microseconds was chosen because it is beyond any observable change in channel conductance. The "off" time is four times the "on" time.

(3) Take an oscilloscope picture of this input which shows pulse width and frequency of application. This input should be maintained during an entire test run.

(4) Adjust the amplitude of the input pulse in order to produce the maximum observable response at 10 millivolts sensitivity.

(5) Choose two horizontal lines on the CRT graticule such that the output response can be displayed between them. This will serve as a point of reference for the displayed output.

(6) Adjust V_{PB} until the observed output response coincides with the two lines of reference. This is to assure a consistent output response.

(7) Take a picture of this response which should appear simultaneously with the input signal. Each vertical amplifier should have different horizontal time bases so that input and output signals do not coincide in the photograph. This allows horizontal displacement of the

two signals which makes the analysis of the output response easier. See Figure 27 for additional clarification.

(8) Take a double exposure displaying the trailing edge of the response beneath the leading edge.

(9) Repeat steps 7 and 8 at 5 millivolt sensitivity.

(10) Record the value of V_{PB} along with any additional appropriate information.

This procedure was followed for each device. In order to maintain a consistent input for the duration of a particular test series, a reference device was chosen. This device is generically the same as those being tested. Its output response and V_{PB} are recorded for a chosen test series input. The device is not irradiated and is used to make sure the applied input has not changed by identically matching its output response. This is done before any post irradiation pulsed field effect measurements are made.

The data contained in Tables 1, 2 and 3 are a sample of results from commercially available p-channel MOSFETs. The devices (2N4120, 3N174) come from two different manufacturers. These devices were chosen for their low interelectrode capacitances (C_{rss} and C_{iss}). Figure 29 is a diagram of data produced on an actual photograph. This diagram shows the applied input and output responses.

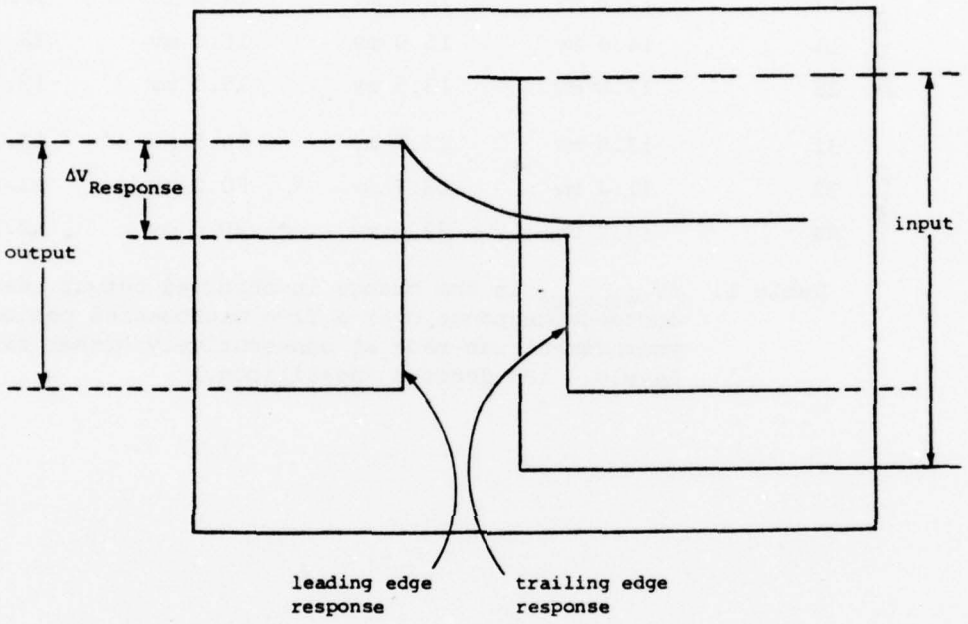


Figure 29. Diagram of Actual Photographed Data. $\Delta V_{Response}$ is the change in the observed channel conductance due to interaction of fast interface states. The applied pulse shown above is five microseconds wide. This necessitates a double exposure which shows the trailing edge output response under the leading edge input response. Typically, the transient lasts about 50 to 100 nanoseconds but is not characterized by a single time constant.

Output $\Delta V_{Response}$ (Millivolt)

	Radiation	0 RS	1×15^5 RS	1.1×10^6 RS	1.11×10^7 RS
	Device No.				
2N4120	12	12.2 mv	12.6 mv	14.0 mv	18.4 mv
	14	14.4 mv	15.0 mv	16.0 mv	23.0 mv
	25	13.0 mv	13.5 mv	15.0 mv	19.7 mv
3N174	31	13.8 mv	22.7 mv	20.5 mv	13.7 mv
	32	11.4 mv	19.7 mv	20.2 mv	13.2 mv
	33	13.7 mv	22.6 mv	20.5 mv	12.1 mv

Table 1. $\Delta V_{Response}$ is the change in observed output channel conductance response over a five microsecond period. This measurement was made at consecutively higher radiation levels. (RS denotes Rad-Silicon.)

V_{PB} - DC Pulse Bias (Volts)

	Radiation	0 RS*	1×10^5 RS	1.1×10^6 RS	1.11×10^7 RS
	Device No.				
2N4120	12	1.6 V	2.75 V	3.16 V	8.60 V
	14	.451 V	1.81 V	2.20 V	4.89 V
	25	.525 V	1.96 V	2.47 V	8.21 V
3N174	31	.427 V	4.90 V	8.04 V	13.08 V
	32	.311 V	4.08 V	7.40 V	13.92 V
	33	.245 V	4.05 V	7.33 V	13.81 V

Table 2. V_{PB} - Necessary d.c. pulse bias to obtain same leading edge output response for identical pulse inputs. This measurement was made at consecutively higher radiation levels. *RS (rads,silicon)

ΔV_{PB} - Change in d.c. pulse bias between radiation doses.

	Device No.	0 RS	1×10^5 RS	1.1×10^6 RS	1.11×10^7 RS	Total Shift
2N4120	12	0 V	Δ1.15 V	Δ .41 V	Δ5.44 V	Δ 7.06 V
	14	0 V	Δ1.36 V	Δ .39 V	Δ2.69 V	Δ 4.44 V
	25	0 V	Δ1.44 V	Δ .51 V	Δ5.74 V	Δ 7.69 V
3N174	31	0 V	Δ4.47 V	Δ3.14 V	Δ5.04 V	Δ12.65 V
	32	0 V	Δ3.37 V	Δ3.32 V	Δ6.52 V	Δ13.61 V
	33	0 V	Δ3.81 V	Δ3.28 V	Δ6.48 V	Δ13.56 V

Table 3. ΔV_{PB} - Change in d.c. pulse bias as a function of radiation dose. This value is related to the threshold voltage shift.

This study did not attempt to make correlative measurements or quantitative measurements of interface state density, but did establish that ionizing radiation produces observable changes in the transient output of p-channel MOSFETS. Further, it establishes that devices within a given family are different both before and after irradiation, and with respect to both threshold voltages and transient outputs. Further, the exponential-like transient responses as shown in Figure 30 are not simple exponentials. It would be surprising if they were. The shape of the output pulse should be heavily dependent upon the surface state density energy distribution. And, as shown in Figure 22, the time constants of the interface states vary with energy position. So, a range of time constants weighted by the surface state energy distribution, the physical/geometrical characteristics of each MOSFET, the gate input bias level, the size of the gate input pulse, the source-drain voltage all determine the shape and size of the output pulse. Therefore one

would expect that the detailed quantitative analysis of these output pulses would be rather complex.

The pulsed field effect measurement, as presented, provides a good qualitative analysis for comparing fast interface state densities in MOSFETS. To make a better correlative analysis between fast interface state density and the shift in threshold voltage would require additional measurements. These measurements are necessary in order to determine the proper cause in the threshold voltage shift. The threshold voltage shift is dependent upon the fixed positive oxide charge and the charge associated with the filled interface states at the surface of the device. Both of these charge conditions change when a device is irradiated. So it becomes necessary to separate these two effects in order to provide better correlative measurements. First of all, it is necessary to measure the threshold voltage shift accurately and consistently. Next, the flat band voltage shift needs to be measured. This can be done through low frequency capacitance-voltage measurements which would provide information on the change in the fixed positive oxide charge. The flat band voltage and threshold voltage should help considerably in evaluating the pulsed field effect technique as a MOSFET screen for radiation susceptibility. Also, irradiating the devices under bias conditions is recommended in order to enhance radiation effects which would provide more observable results.

Final Experiments

A final set of measurements was performed to determine preliminarily if there were correlations with the MOSFET transient responses before irradiation with such quantities as the flatband voltage and threshold voltage. These experiments were constrained by a number of conditions including the quantity and type of devices available, the time available to obtain these measurements, and the somewhat primitive way the data were obtained, not using modern automated techniques.

An initial quantity of devices was irradiated to 10^5 rads after extensive pre-irradiation evaluation, only to discover that some of the measurement techniques were destroying devices and that the devices should have been irradiated at lower levels before irradiating to 10^5 rads(Si).

The remaining available p-channel and n-channel devices were tested both before and after irradiation with improved technique. The following are the details of the procedures and philosophy behind these experiments:

1) Transient pulse measurements were made following the procedures of the intermediate experiments above.
2) Capacitance-voltage curves were run using equipment furnished by the Air Force Weapons Laboratory. From the discussion of Chapter II, Volume I, precise determination of the flatband voltage is impossible without both quasi-static and high frequency MOS C-V measurements. The C-V curve of a MOSFET is similar in shape to the quasi-static curve of a MOS capacitor. In these experiments, we have

chosen to take as $V_{FLATBAND}$, the intersection of the flat part of the C-V curve on the accumulation side with the tangent line of the dip of the C-V curve on the accumulation side. This intersection point should approximate the flat-band voltage and should have the qualitative behavior that its position is strongly dependent on fixed charge within the dielectric. This voltage should be weakly dependent on changes in interface state density due to irradiation. The decision to use this procedure was based primarily on the lack of other reasonable systematic choices.

3) Threshold voltages were determined using three techniques:

   a) Transistor curve tracer data

   b) Pulsed measurements using the leading edge of the MOSFET output pulse, Figure 30.

   c) Pulsed measurement using the trailing edge of the MOSFET output pulse, Figure 30.

All of the threshold measurements were based on linear extrapolations of Equations 19 and 20. With all due respect to instrument calibration and accuracy, measurements a) and c) should be equivalent if the trailing edge of the pulse were observed after a sufficiently long time. Measurement b) should give a different answer for the threshold or "turn-on" voltage for a MOSFET, primarily because this threshold value is based on the fact that not all of the fast interface states have reached thermal equilibrium. Hence both carrier mobilities in the channel and the charge state of the gate-substate capacitor should be different from the corresponding thermal equilibrum quantities. The

threshold voltage for a MOSFET is given in various treatises as approximately

$$V_T = \frac{-Q_{ss} - Q_{oxeff} - Q_{SD_{max}}}{\varepsilon_{ox}} t_{ox} + \phi_{ms} + 2\phi_F \qquad (21)$$

Here

Q_{ss} = surface state charge

Q_{oxeff} = effective fixed charge in the oxide as if it were all at the oxide-silicon interface

$Q_{SD_{max}}$ = maximum depletion layer charge

t_{ox} = oxide thickness

ϕ_{ms} = the difference in the metal and semiconductor work function

ϕ_F = the Fermi potential relative to the intrinsic Fermi level

and ε_{ox} = the dielectric constant of the oxide.

The two quantities of interest in this expression are Q_{ss} and Q_{oxeff}. For a given doping and gate metal, ϕ_{ms} and ϕ_F can be determined from existing data. Since for a given irradiation dosage Q_{oxeff}, ϕ_{ms}, $Q_{SD_{max}}$, and ϕ_F are all constants, the threshold voltages determined from the transient or leading edge of the pulse data and steady state or trailing edge of the pulse data should yield a measure of ΔQ_{ss} in the time constant range of the measuring apparatus:

$$\Delta Q_{ss} = \frac{A_G \varepsilon_{ox}}{t_{ox}} [V_{TT} - V_{Tss}] \qquad (22)$$

and

$$\Delta N_{ss} = \frac{\Delta Q_{ss}}{q}, \text{ the number density of fast interface states.}$$

V_{TT} = threshold voltage determined from the leading edge of a MOSFET pulse response

V_{Tss} = threshold voltage determined from the trailing edge of a MOSFET pulse response

A_G = MOSFET Gate Area.

It may be argued that this formulation is in error because threshold voltages are computed on the basis of thermal equilibrium values. MOSFET device mobile carriers move very rapidly to thermal equilibrium because of injection of majority carriers from their gate and source electrodes. Hence the only quantity not moving into thermal equilibrium with a fast rise time gate pulse is the quantity Q_{ss}. In contrast, an MOS capacitor depends upon thermal generation of carriers to bring the depletion charge to thermal equilibrium. Because this process is relatively slow, the device is quite frequency dependent, as discussed in Volume I, Chapter II of this report. Further, measurements of "transient" thresholds involve measuring transient data at three different gate voltages which correspond to three different surface potentials, and one would not expect that a graph of $|I_{DS}|^{1/2}$ versus gate voltage would fit a straight line. But the data did indeed fit a straight line, because fast interface states located between the Fermi level and the conduction band or within the conduction band are too fast to be observed by this technique as shown in the previous chapter. This report does not attempt to use the technique suggested above to deduce interface state density because the preliminary data obtained was not of sufficient quality or quantity to draw conclusions.

Data were taken on 15 p-channel devices and 10 n-channel devices to see if there were correlations of the interface transient pulse before irradiation with shifts in flat band voltage and

threshold voltage as a function of radiation dose. These data are summarized in the following presentation. The first of these is the data for an initial group of ten Texas Instruments 3N169 n-channel devices plus one control device. The data for the control devices, which were not irradiated, are not shown, as is the case with other control devices.

The magnitude of the leading edges of data similar to Figure 29, with the steady state values subtracted, is shown in Figure 30. This is followed by threshold data, Figure 31, and flatband data, Figure 32. Figure 30 indicates two groupings of devices, those with relatively small pre-irradiation transient signals and those with relatively large pre-irradiation transient signals. It is interesting to note the following: 1) Those devices with small pre-irradiation signals tend to have the largest post-irradiation signals, especially at 10^5 Rads. We may also say that the number of interface states has also increased with irradiation in a similar manner; 2) Those devices which had small pre-irradiation transient signals tend to be the ones with large shifts in threshold and flatband voltages. Although the causes for these "correlations" are not immediately obvious, there appears that there is some relationship between the number of interface states existing before irradiation with both the dielectric charge and interface state density after irradiation in the group of devices.

Figure 33 , 34 , 35 , and 36 are data for Motorola 4351636 n-channel devices, whose dielectric, we believe, is not silicon dioxide. The data in general do not give much indication for

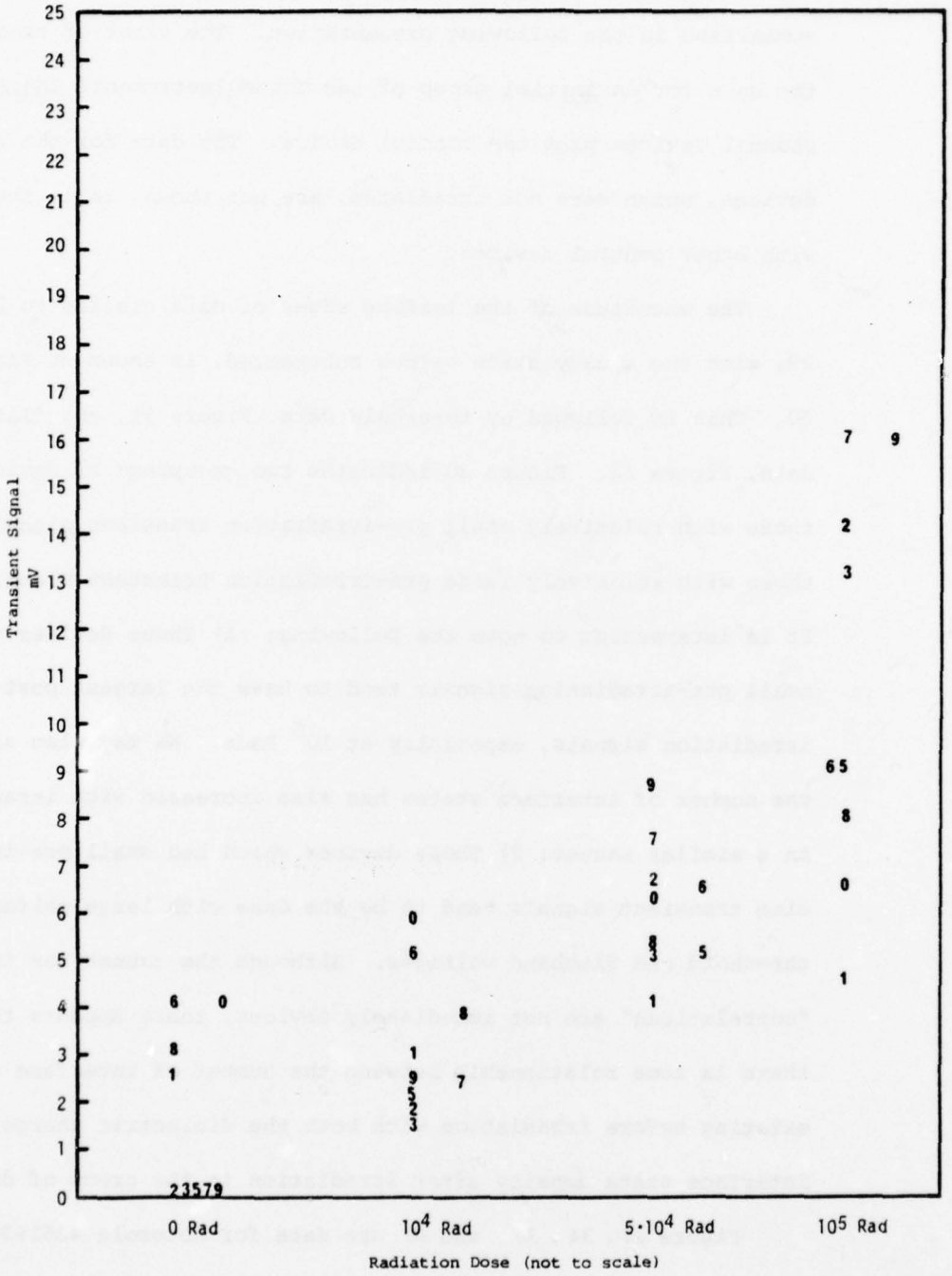


Figure 30. Transient Signal vs. Radiation Dose for 3N169 n-channel MOSFETs.

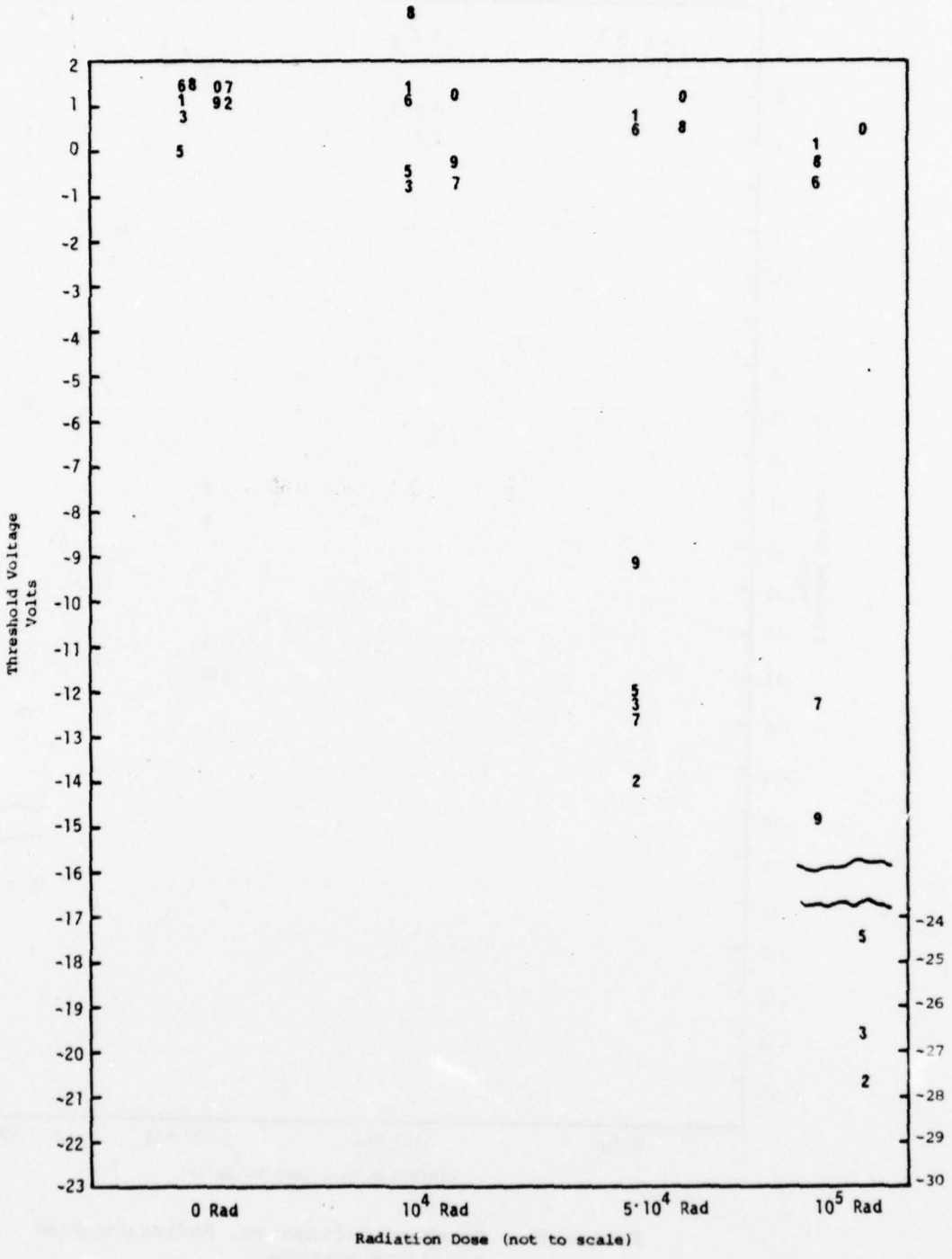


Figure 31. Threshold Voltage vs. Radiation Cose for 3N169 MOSFETs as Derived from Curve Tracer Data.

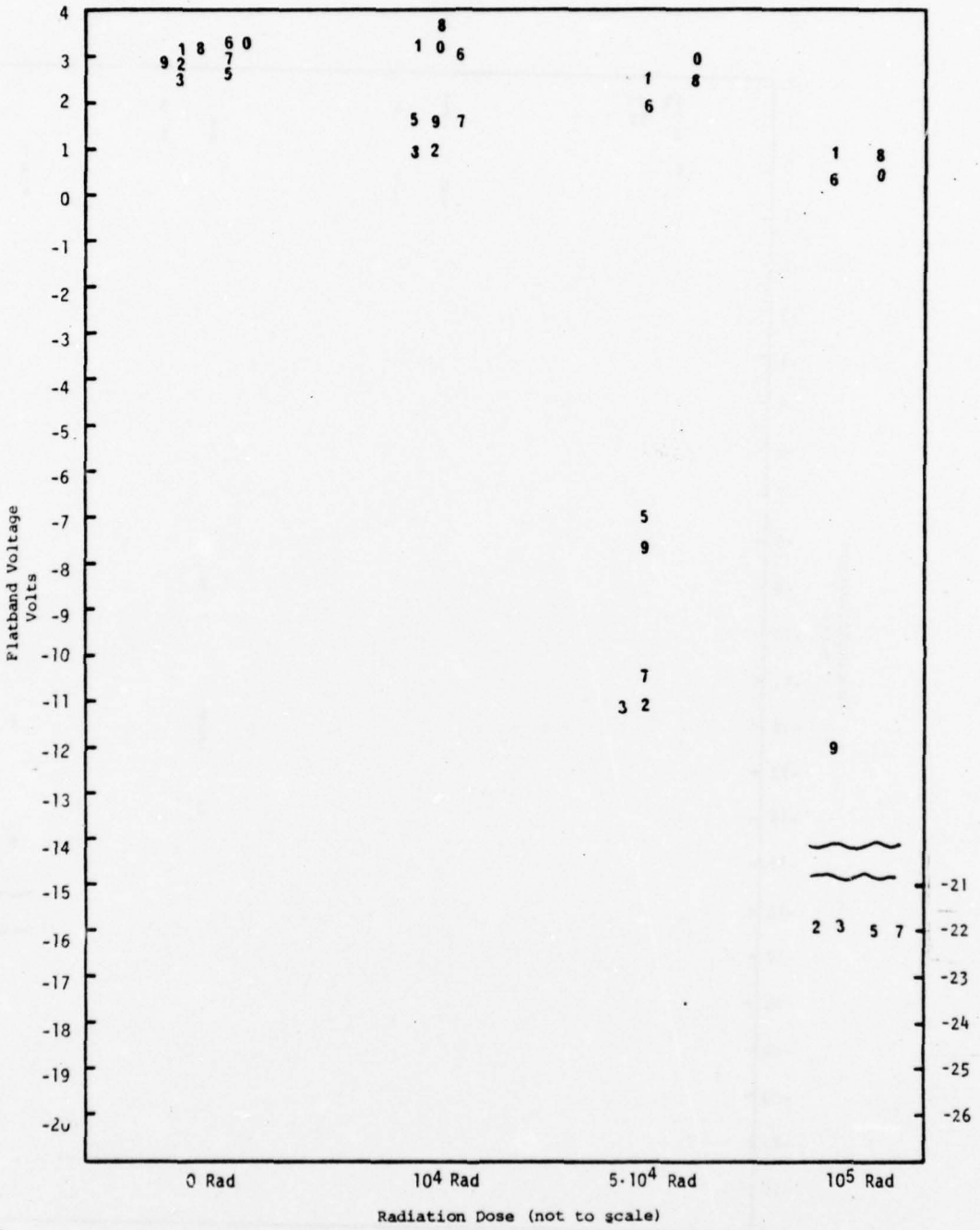


Figure 32. Flatband Voltage vs. Radiation Dose for 3N169 MOSFETs.

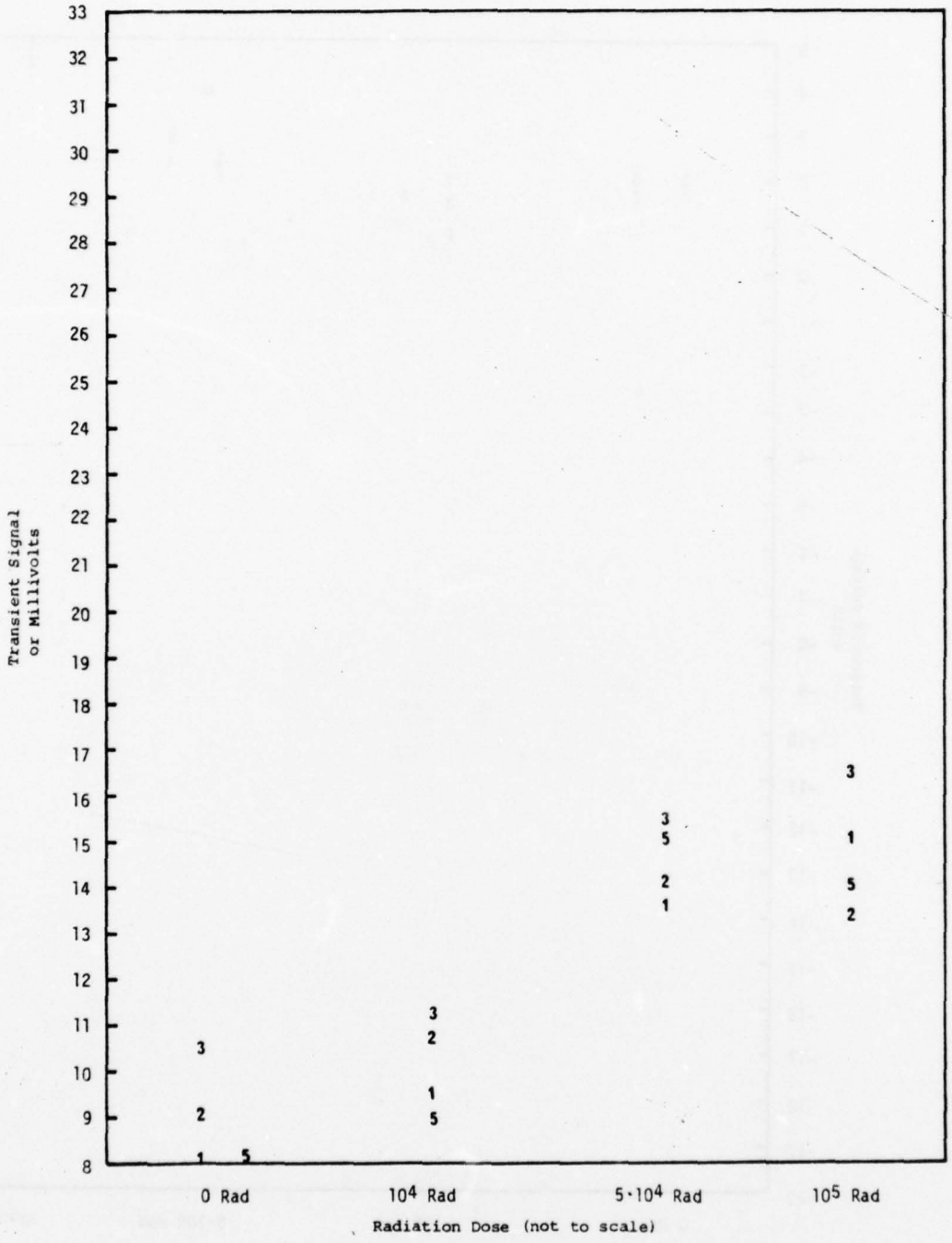


Figure 33. Transient Signal vs. Radiation Dose for Type 435 1636 11-channel MOSFETs.

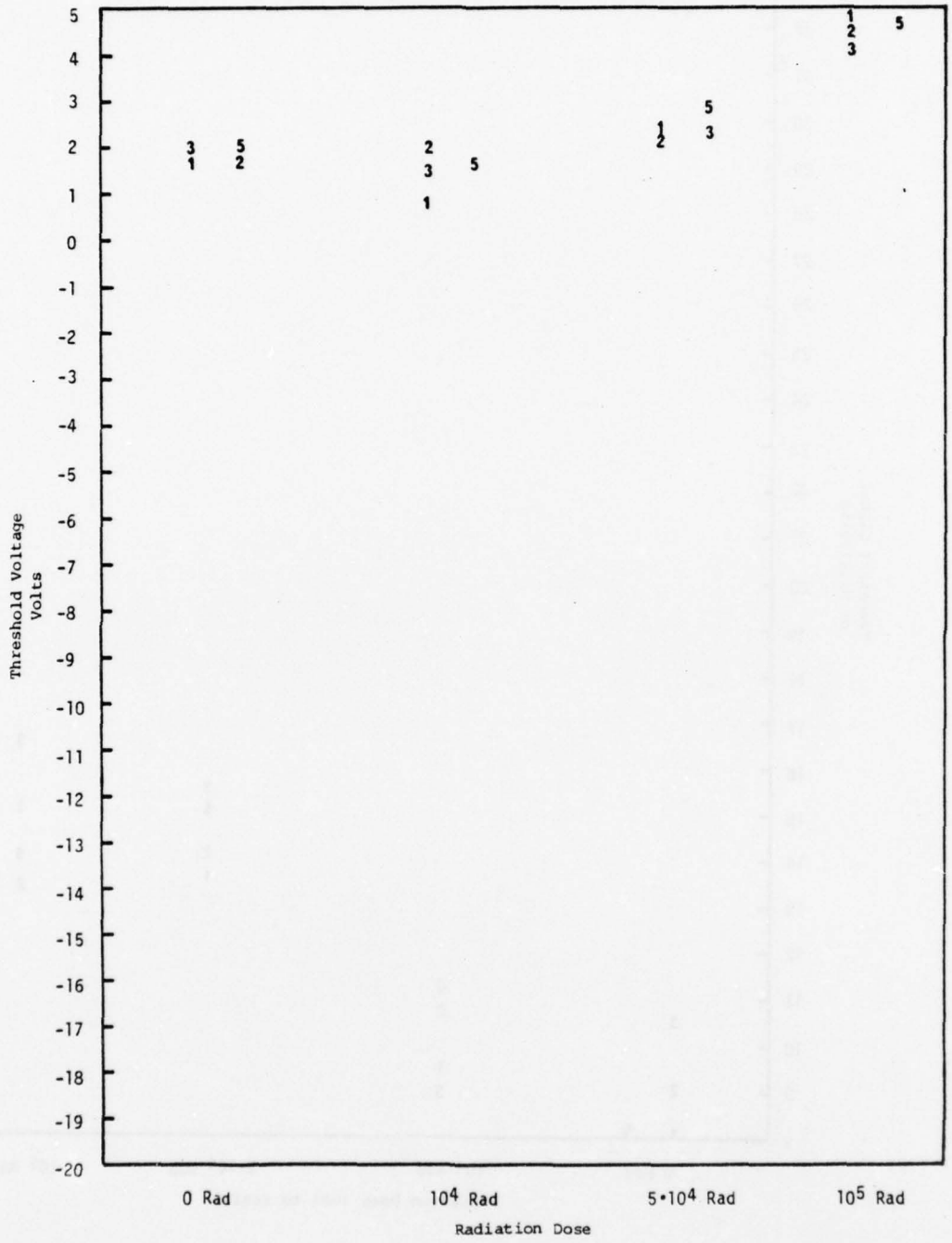


Figure 34. Threshold Voltage vs. Radiation Dose for Type 435 1636 MOSFETs as Derived from Curve Tracer Data.

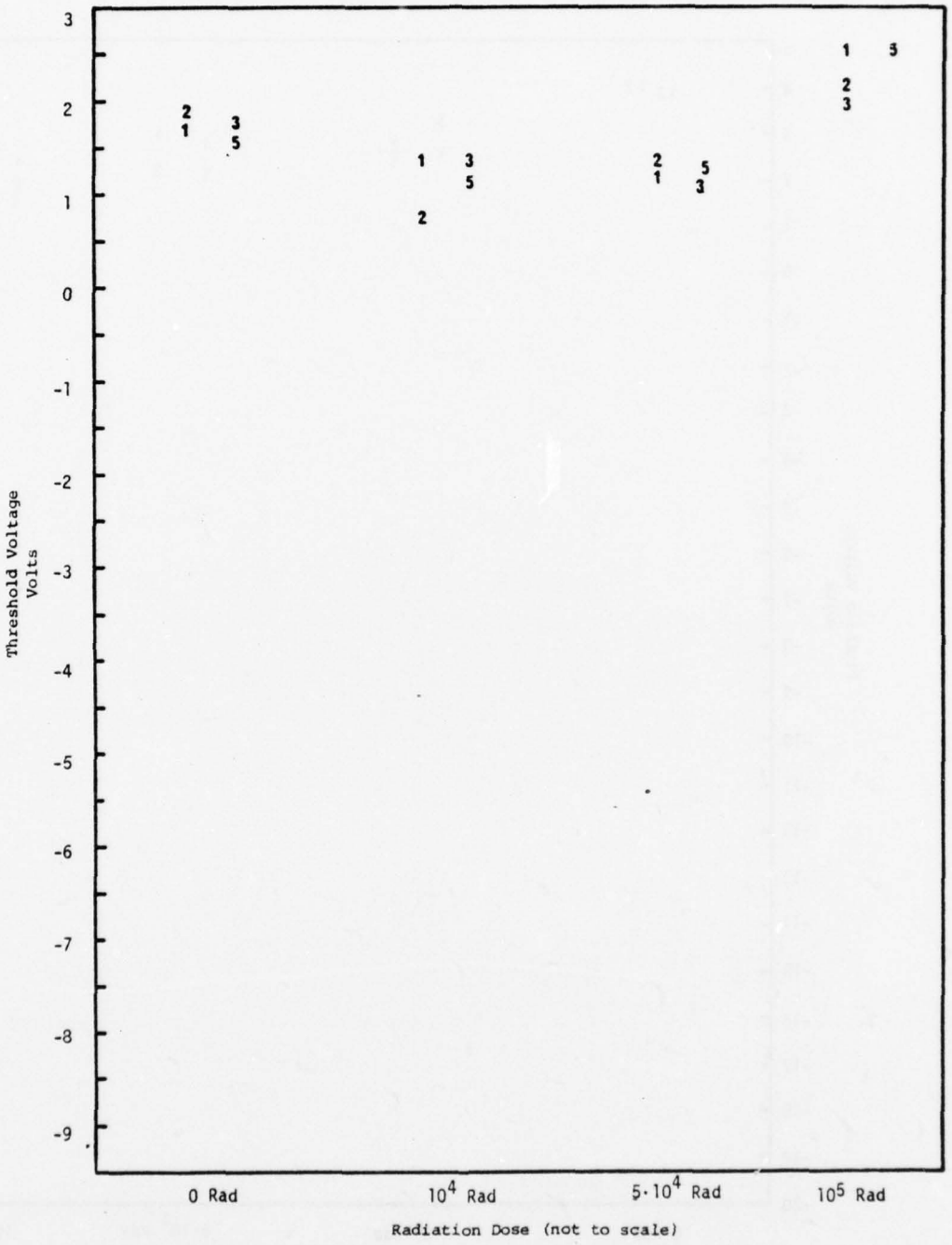


Figure 35. Threshold Voltage vs. Radiation Dose for Type 435 1636 MOSFETs as Derived from Transient Pulse Measurements.

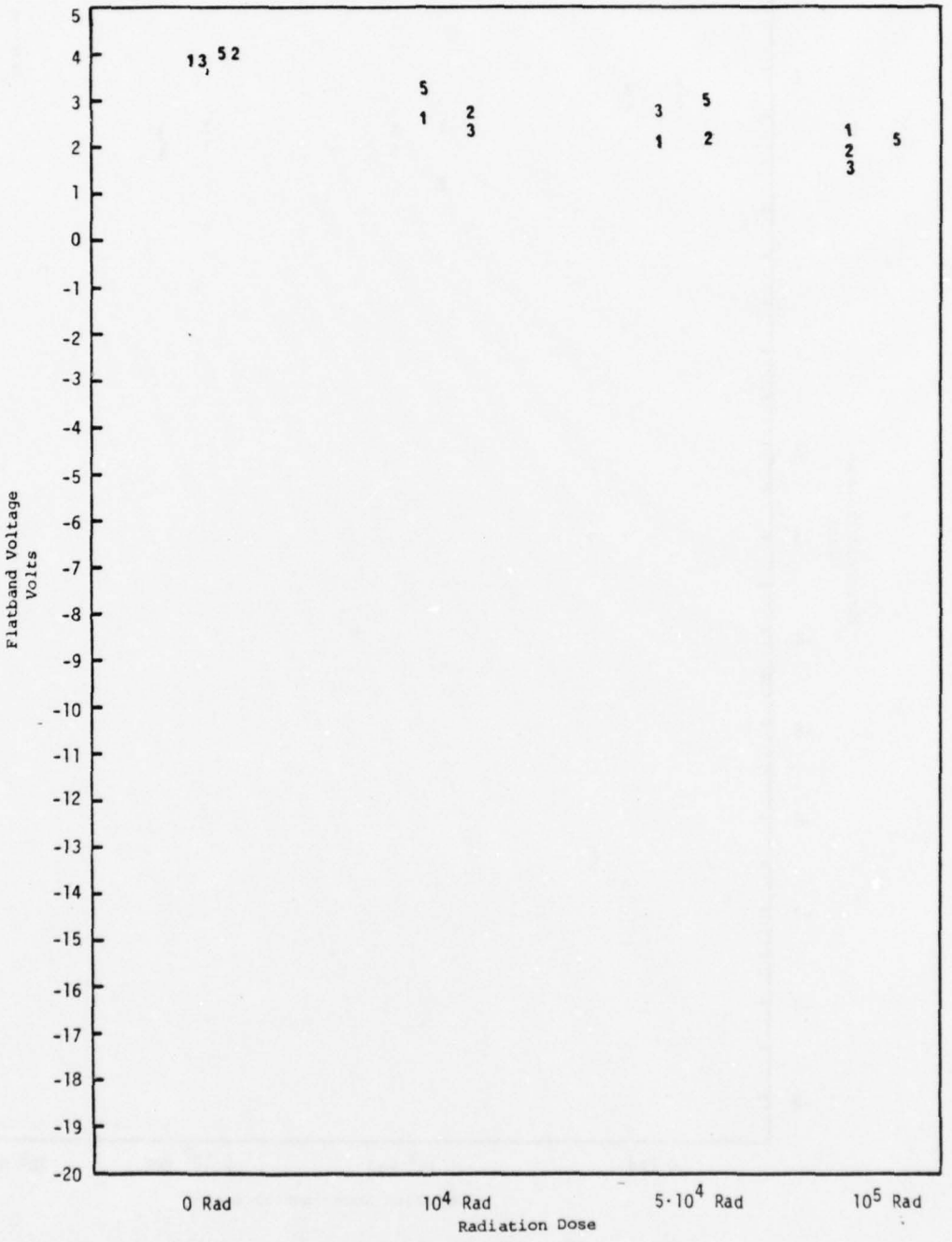


Figure 36. Flatband Voltage vs. Radiation Dose for Type 435 1636 MOSFETs.

pre-irradiation screening. This is not surprising because of the small number of devices tested.

Figures 37 to 40 show data from Texas Instruments 3N174 p-channel devices. These data indicate that relative values of pre-irradiation interface state density, as indicated by transient pulses, are related to threshold and flatband voltages in about the same way as the data for 3N169 n-channel devices. The data, however, are not as distinct. Further, the relationship between pre-irradiation interface state density and post-irradiation interface state density, if anything, is opposite to that of the 3N169 devices.

Certain inferences are made from the experiments performed:

1) There is the possibility that the pulse technique could be used for screening because there does appear to be some relationship between pre-irradiation fast interface state density and shifts in threshold and flatband voltages.
2) Fast interface state density, in the range of the pulse measurements, increases with irradiation and in some types of devices a low pre-irradiation density predicts a more rapid increase in interface state density with irradiation.
3) Although not shown in this report, interface state density appears to be related to channel carrier mobility via examination of threshold data (Equation 19, Chapter VI and Figure 27). We have observed changes in slope of

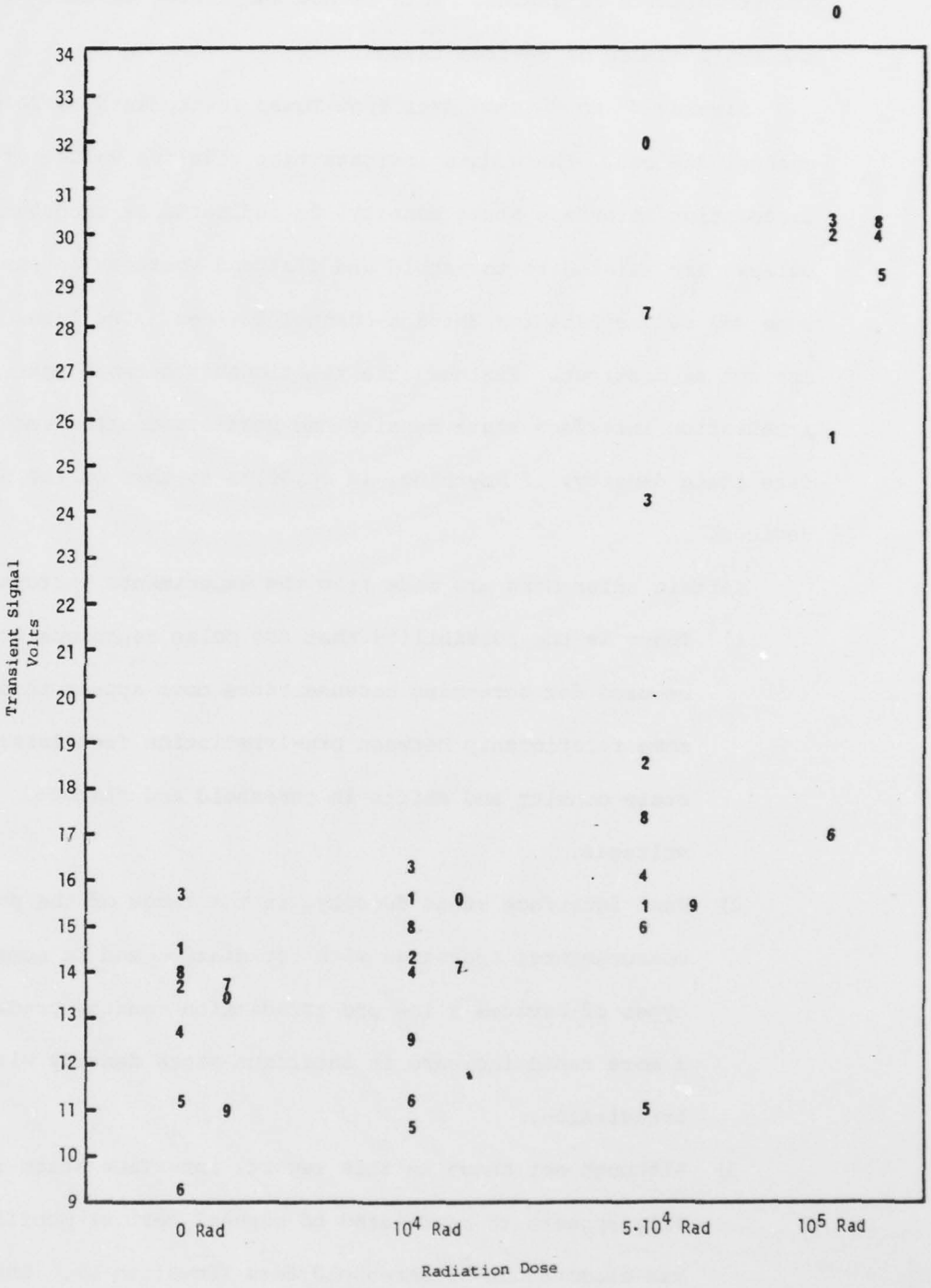


Figure 37. Transient Signal vs. Radiation Dose for 3N174 p-channel MOSFETs.

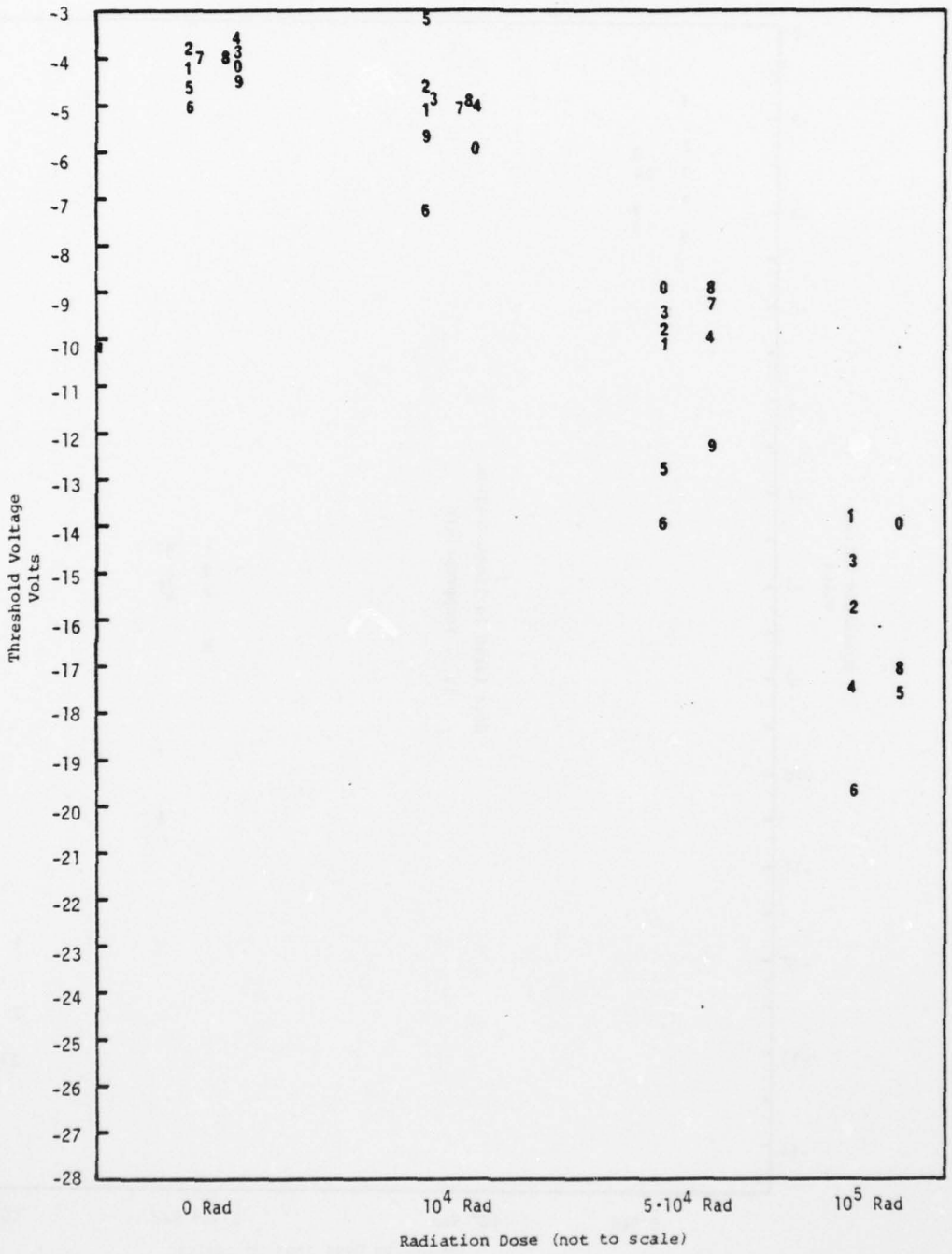


Figure 38. Threshold Voltage vs. Radiation Dose for 3N174 MOSFETs as Derived from Curve Tracer Data.

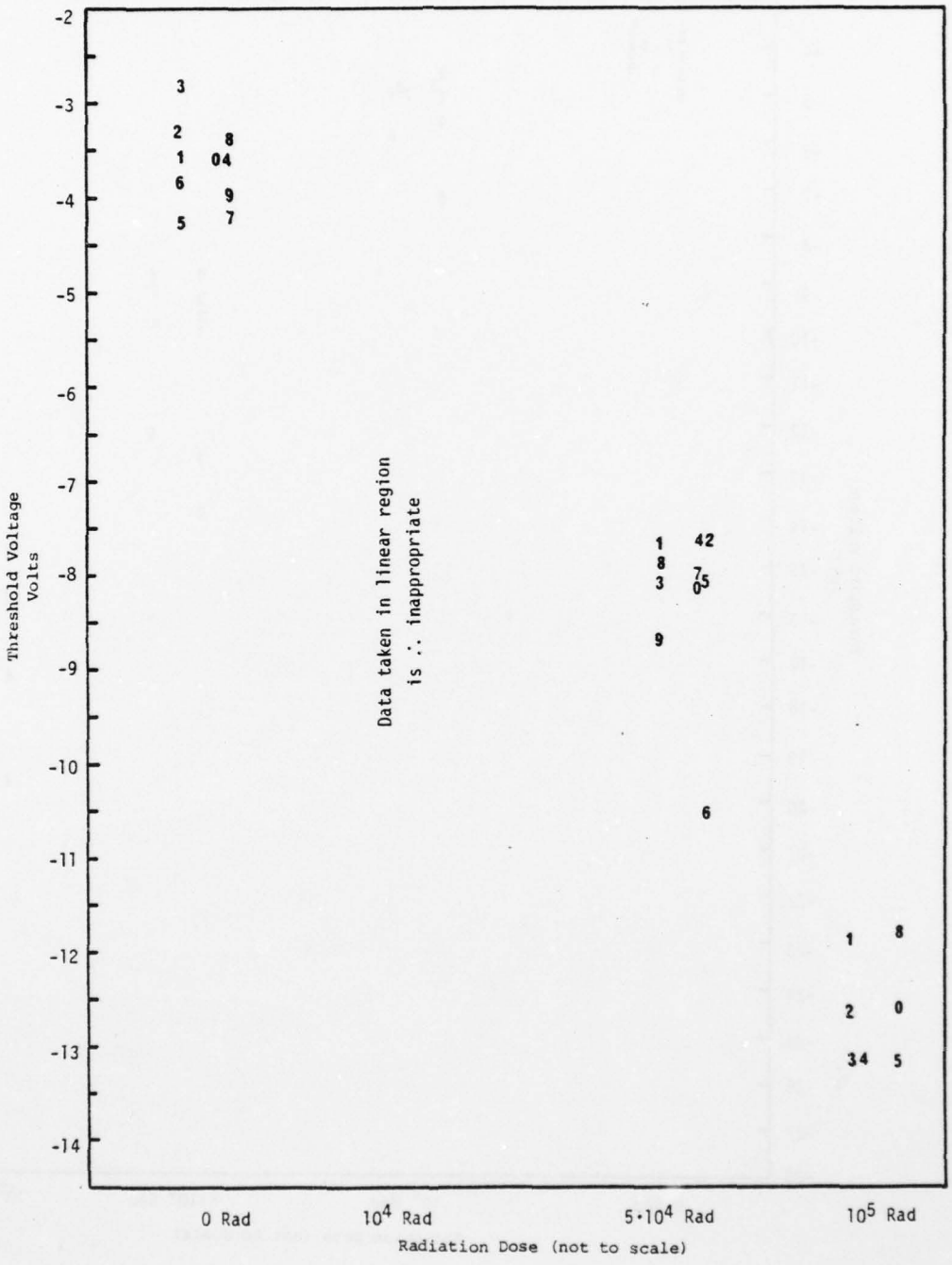


Figure 39. Threshold Voltage vs. Radiation Dose for 3N174 MOSFETs as Derived from Transient Pulse Measurements.

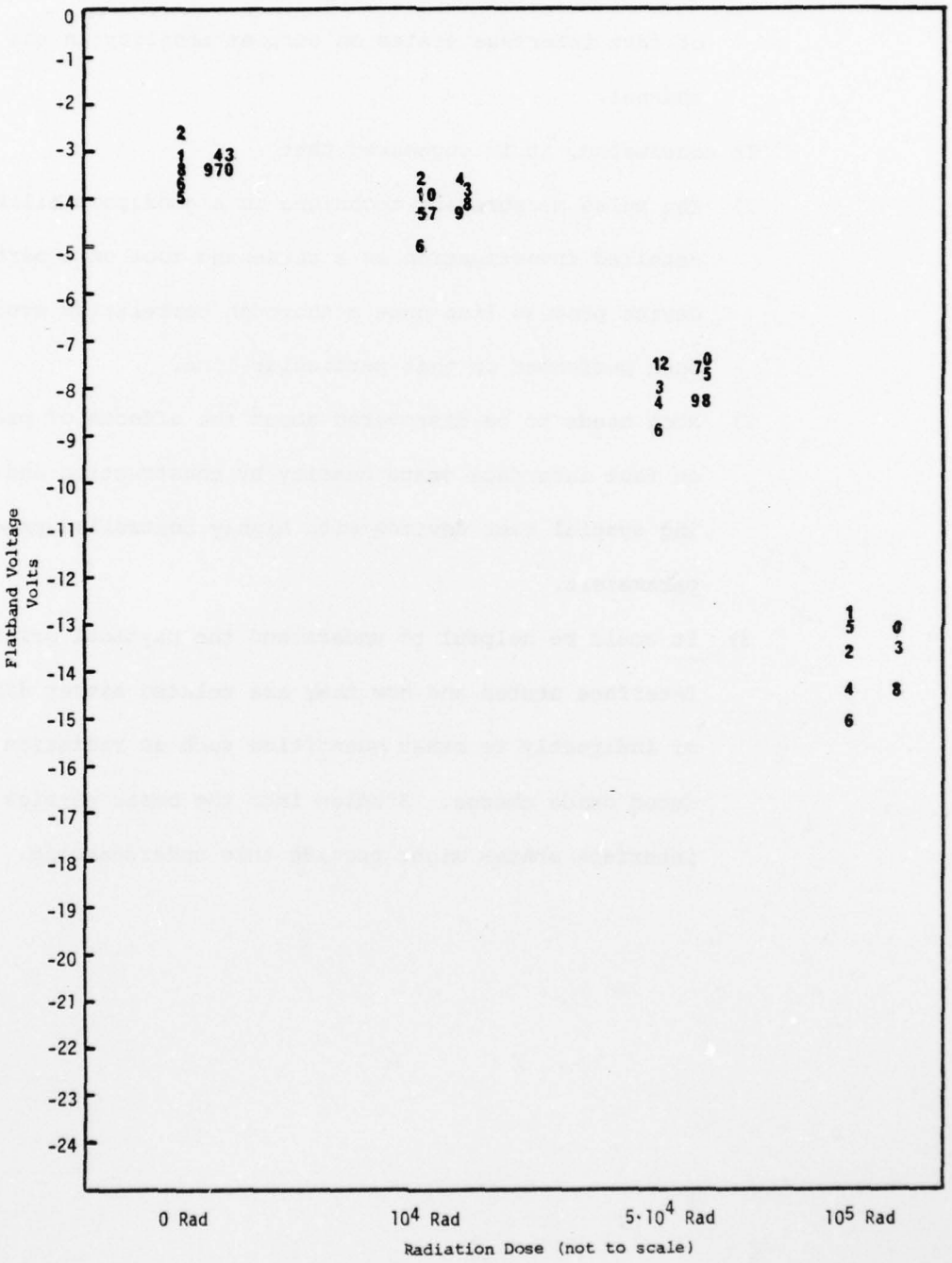


Figure 40. Flatband Voltage vs. Radiation Dose for 3N174 MOSFETs.

the $|I_{DS}|^{1/2}$ vs V_{GS} line with irradiation. This implies that changes in device gain are due in part to the effect of fast interface states on carrier mobility in the channel.

In conclusion, it is suggested that

1) The pulse measurement technique is a good possibility for detailed investigation as a screening tool on a particular device process line once a thorough correlation study has been performed on that particular line.
2) Much needs to be discovered about the effects of process on fast interface state density by constructing and testing special test devices with highly controlled process parameters.
3) It would be helpful to understand the physical origin of interface states and how they are related either directly or indirectly to other quantities such as radiation induced oxide charge. Studies into the basic physics of interface states might provide this understanding.

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LIST OF ABBREVIATIONS

A	Amperage
a.c.	alternating current
CRT	Cathode Ray Tube
d.c.	direct current
eV	electron volts
F	Farad
FET	Field Effect Transistor
HP	Hewlett-Packard
k	kilo or 1000 units
K	Kelvin
ℓn	natural log
m	meters
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
mV	millivolt
P-N	Junction between p-type and n-type material
RS	Rad-silicon

LIST OF SYMBOLS

A_G	MOSFET gate area
C_D	Total capacitance of drain and source bondings
C_{D1}	Drain bonding capacitance
C_{D2}	Drain junction capacitance
C_{iss}	Device input capacitance with output shorted
C_{G1}	Gate capacitance
C_{GDi}	Intrinsic gate-drain capacitance
C_{GDe}	Extrinsic gate-drain capacitance
C_{Ge}	Extrinsic gate capacitance
C_{GS}	Gate-source capacitance
C_{GSe}	Extrinsic gate-source capacitance
C_{GSBi}	Intrinsic gate-source-substrate capacitance
C_L	Load capacitance
C_{rss}	Device output capacitance with input shorted
C_{S1}	Source bonding capacitance
C_{S2}	Source junction capacitance
C_{12}	Gate-source lead capacitance
C_{13}	Drain-source lead capacitance
C_{23}	Gate-drain lead capacitance
D	Drain lead on MOSFET
E_C	Conduction band
E_f	Fermi level
E_i	Intrinsic energy level
E_{IN}	Input voltage

E_{OUT}	Output voltage
E_V	Valence band
g_m	Transconductance
I_D	Drain current
I_{DSAT}	Saturated drain current
I_i	Input current
L_D	Drain lead inductance
L_G	Gate lead inductance
L_O	Intrinsic gate-source inductance
L_S	Source lead inductance
ℓ	Length of the channel in the direction of current flow
ΔN_{ss}	Number density of fast interface states induced by radiation
n	Electron concentration
p	Hole concentration
Q_{ss}	Surface state charge
ΔQ_{ss}	Radiation induced state charge
Q_{oxeff}	Effective fixed charge in the oxide as if it were all at the oxide-silicon interface
$Q_{SD_{max}}$	Maximum depletion layer charge
q	Electron charge
R	Resistor
R_{CH}	Channel resistance
R_D	Drain load resistance
R_{DE}	Extrinsic drain load resistance
R_{DSi}	Intrinsic drain-source resistance
R_f	Feedback resistance

R_s	Source resistance
R_{se}	Extrinsic source resistance
S	Source
t	Time
t_a	Square pulse duration
t_{ox}	Thickness of the oxide over the channel
t_m	Square pulse duration
U_B	Bulk potential (dimensionless)
$\bar{U}_S$	Surface potential (dimensionless)
ΔV	Change in voltage
V_a	Bias voltage
V_{DC}	Direct-current voltage
V_{DD}	Drain voltage for MOS inverter
V_{DS}	drain to source voltage
$V_{D\ MAX}$	Maximum drain voltage
$V_{D\ MIN}$	Minimum drain voltage
$V_{D\ SAT}$	Saturation drain voltage
V_{DTH}	Thevenin drain voltage
V_G	Gate voltage
V_{GS}	Gate-source voltage
V_{GSi}	Intrinsic gate source voltage
V_{IN}	Input voltage
ΔV_{IN}	Change in input voltage
V_{OUT}	Output voltage
V_{PB}	Pulse bias voltage
ΔV_{PB}	Change in pulse bias voltage

V_{pulse}	Voltage pulse
V_T	Threshold voltage
V_{TH}	Thevenin voltage
V_{Tss}	Threshold voltage determined from the trailing edge of a MOSFET pulse response
V_{TT}	threshold voltage determined from the leading edge of a MOSFET pulse response
$V_{THRESHOLD}$	Threshold voltage
$V_{RESPONSE}$	Change in output response voltage
V_s	Surface voltage
W	Width of the channel
ε_{ox}	Permittivity of the oxide
μ	Micro. 1×10^{-6}
μ_p	Average surface mobility of holes in the channel
τ	Time constant
ϕ_b	Bulk potential
ϕ_F	Fermi potential relative to the intrinsic Fermi level
ϕ_{ms}	Difference in the metal and semiconductor work function
ϕ_s	Surface potential
ω	Frequency
Ω	Ohms

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