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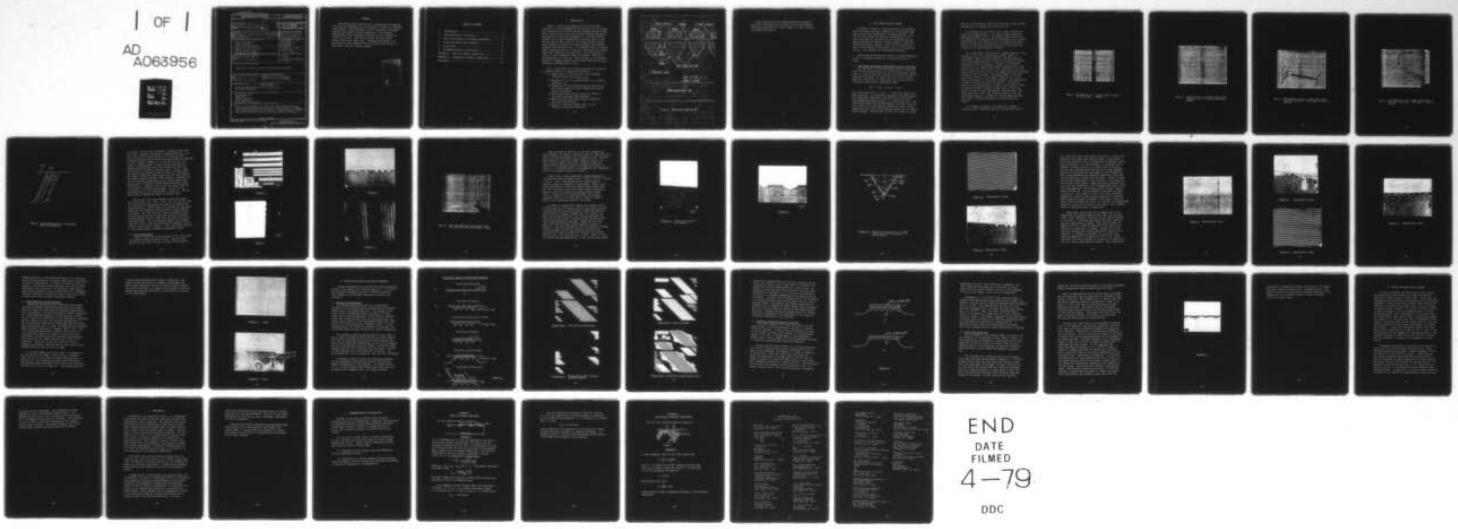

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REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER	2. GOVT ACCESSION NO. / 3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) (6) NONCOPLANAR HIGH POWER FET.	5. TYPE OF REPORT & PERIOD COVERED (9) Annual Report No. 2, Jan.-Dec. 1976
	6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) (10) S.G. Bandy, R. Sankaran, S.B. Hyder, D. M. Collins	8. CONTRACT OR GRANT NUMBER(s) (15) N00014-75-C-0303
9. PERFORMING ORGANIZATION NAME AND ADDRESS Varian Associates 611 Hansen Way Palo Alto, CA 94303	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS PE 62762N RF-54-581-001 NR 251-018
11. CONTROLLING OFFICE NAME AND ADDRESS Office of Naval Research 800 N. Quincy Street Arlington, VA 22217	12. REPORT DATE October 27, 1978 13. NUMBER OF PAGES 48
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office) (11) 27 Oct 78	15. SECURITY CLASS. (of this report) UNCLAS 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for Public Release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

(16) F54581 (17) RF54581001

18. SUPPLEMENTARY NOTES

ONR Scientific Officer
Tel (202) 696-4218

(12) 58 p.

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Noncoplanar FET
Power FET
AlGaAs substrate
GaAs regrowth
Insulating GaAs growth

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The use of low-doped tubs under the source and drain have significantly reduced the parasitic capacitances of a common-gate noncoplanar power FET structure. Submicron gate lengths were easily achieved with an etch and growth technique.

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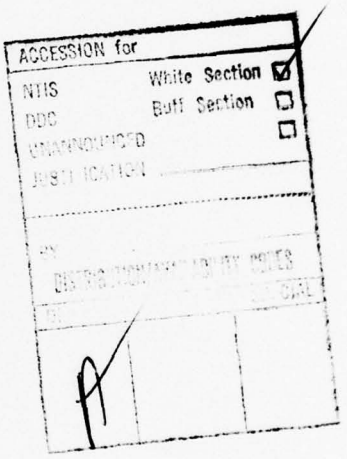
SUMMARY

Work towards the realization of a common-gate noncoplanar power FET has progressed up to the point of achieving insulated field growth. The technology to grow V-grooves of low-doped material has enabled a large reduction in the parasitic capacitances to be achieved in addition to gate lengths as low as 0.2 micron. Good active layers have been grown without the use of vapor etch. Problems with contact resistance have been observed when the ohmic contact alloy is done with a thick Au overlay present.



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1. INTRODUCTION

Figure 1 shows the proposed noncoplanar power FET structure to be investigated during this phase of the contact. This structure will not have the space-charge-limited current shunt around the gate that the structure investigated during the period covered by Annual Report No. 1 of this contract. Neither will it need the mechanical polishing step to level off the regrown tubs, which in turn uncontrollably thinned these regions and resulted in large parasitic capacitances. Although the structure in Fig. 1 has regrown tubs, no intimate photolithography contact is needed to form small gate lengths after their formation, and their small size would result in little, if any, overgrowth above the surface. The use of ion-implantation to form the insulating tubs is not feasible because of sideways channeling which would increase the gate resistance and maybe pinch it off.

Fig. 1 also offers the following advantages in addition to those accorded to a noncoplanar structure:

(1) Drain swing out to V_B (drain-to-gate breakdown voltage) rather than $V_B - V_{pinch\text{-}off}$.
(2) Reliability of a p-n junction gate (e.g.; no metal migration, etc.).
(3) Possibility of increased doping away from the gate for better linearity without compromising source contact resistance.
(4) Gate lengths less than the resolution limit of the photolithography masks employed.
(5) Small die size which means thinner substrates and better heat sinking.
(6) Ability to thin the channel after the gate formation (processing advantage).

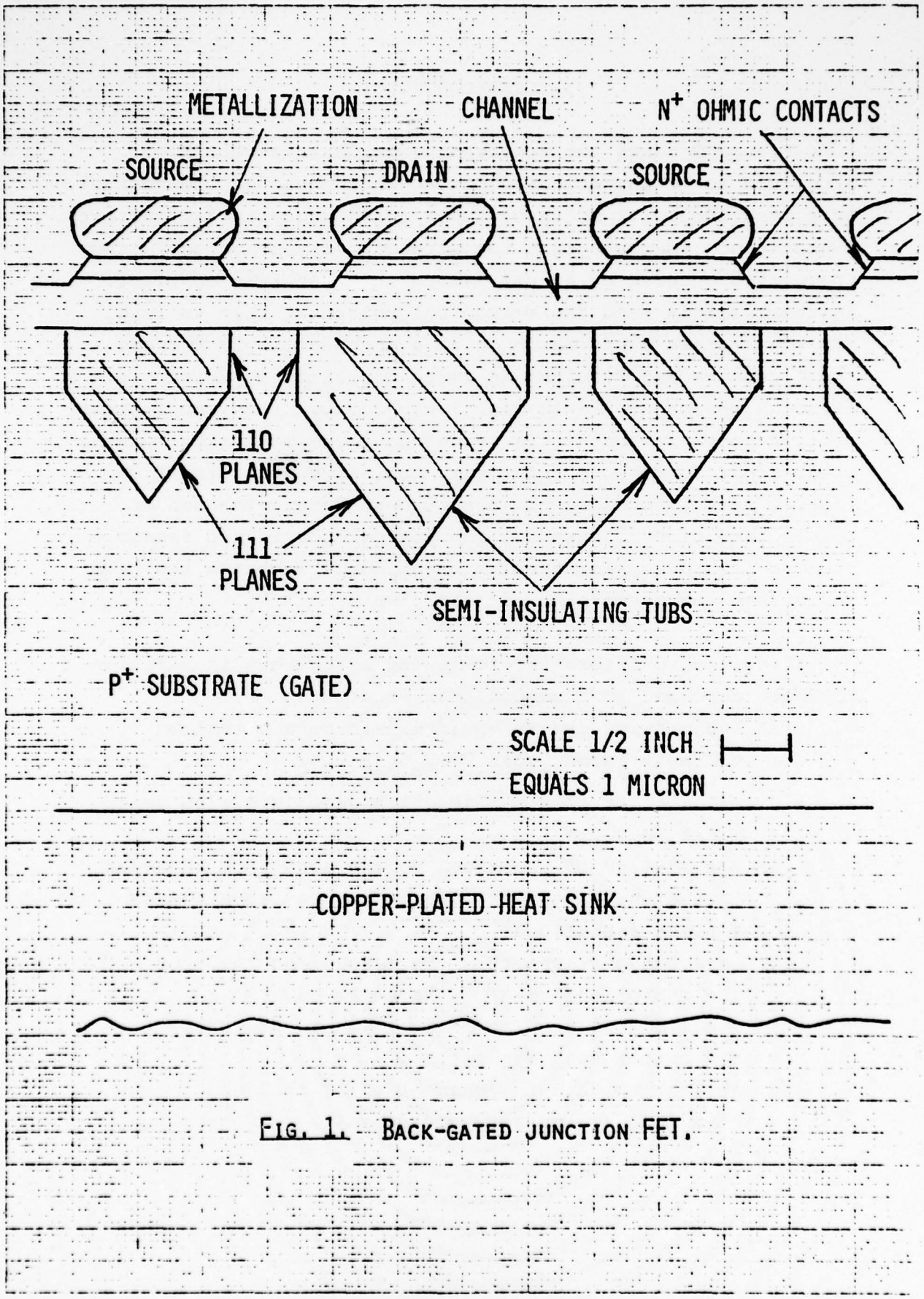


FIG. 1. BACK-GATED JUNCTION FET.

While retaining the tub growth technology developed during the first phase of this contract, the new structure incorporates features that should render it a more reliable and higher power device.

2. GATE TROUGH ETCH AND GROWTH

As shown in Figure 1, those portions of the substrate under the source and drain contacts are to be etched away and refilled with insulating or low-doped material. This will not only reduce the parasitic capacitances of the source and drain to the gate, but will determine the gate length provided the spacing of these regions is less than the source-to-drain spacing. Since the best growth will occur if the etching is also done in situ in the vapor-epi reactor, this approach was investigated initially.

This study was carried out using n^+ Te-doped substrates as the p^+ Cd-doped substrates to be used were still on order.

2.1 Gate Trough Orientation Determination Using Vapor Etch

The fabrication of the gate trough involved a detailed study of the etching behavior of various GaAs planes by HCl vapor in an $AsCl_3$ vapor-epi reactor, using different temperatures and flow rates. On planar etching with the wafers partially covered with an SiO_2 layer, the etching rates at 750°C were found to be in decreasing order

$$(110) > (100) > (111)A > (111)B$$

and in the ratio of 2.5 : 1.32 : 1 : 0.66 with typical $AsCl_3$ mole fractions. All wafers were chemically polished damage-free before SiO_2 deposition, and the A and B faces were distinguished by their reactions to a Br-methanol etch. The order found agrees with crystallographic intuition since the (111) plane is the most densely packed with lowest surface energy and (110) is the least densely packed with the largest surface energy. The etch rate of the (111)A plane is larger

than the (111)B plane as the As-rich face has a lower surface energy due to the larger size of the As atom.

To simulate the gate trough, line etches on different planes were studied using 2- to 3-micron lines photolithographically etched in SiO_2. The etching order derived from the observation of these etches can be deceptive as interface effects and gas flow kinetics tend to interfere with ideal etching relationships and slow and fast etching planes can co-exist in the early stages of etching.

For a mask about 3-microns wide, aligned along the <100> direction on the (001) wafer plane of GaAs, there is a considerable amount of under-etch below the SiO_2 mask and (110) planes predominate as is seen in the scanning electron microscope picture in Figure 2. Figure 3 is an optical picture of two 2.8-micron-wide mutually perpendicular lines aligned along the <110> and the <1$\bar{1}$0> direction on the (001) plane wafer and Figures 4 and 5 are scanning electron microscope pictures of the two lines. The etched groove in one case has vertical walls of (110) planes, together with (111)A planes terminating in (100) plane as shown in the SEM picture in Figure 5 and by the sketch in Figure 6. The etched groove is the type depicted in Figure 1, but Figure 5 shows an undercut of about a micron on both sides of the SiO_2 mask of 2.8-micron width when etched 5-microns deep. The other etch line in the <110> direction does not show any significant undercut, although the (111)B planes terminate this etch in a V-groove as seen in the SEM picture in Figure 4.

To simulate the effect of adjacent gate troughs, a "Photronic Labs" resolution mask with the smallest pair of

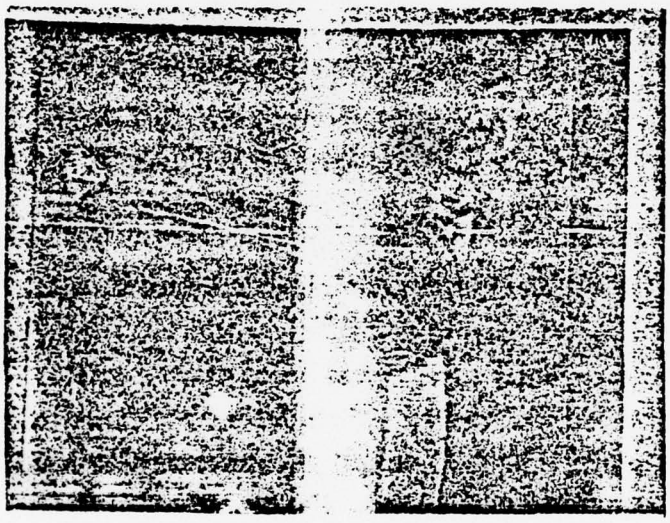


Fig. 2. SEM picture of etch along ⟨100⟩ direction on (001) plane (1040x)

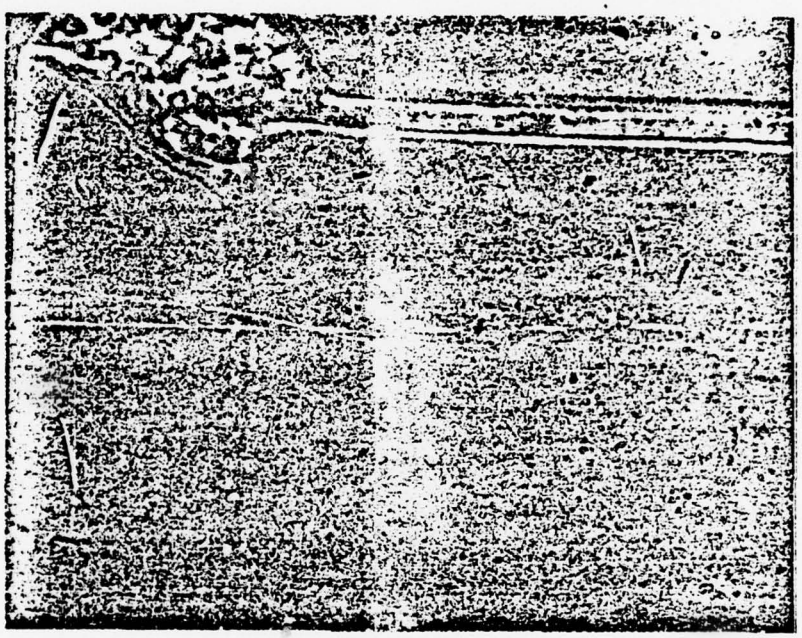


Fig. 3. Optical picture of etch on (001) plane along the ⟨110⟩ and ⟨1$\bar{1}$0⟩ directions. (1400x)

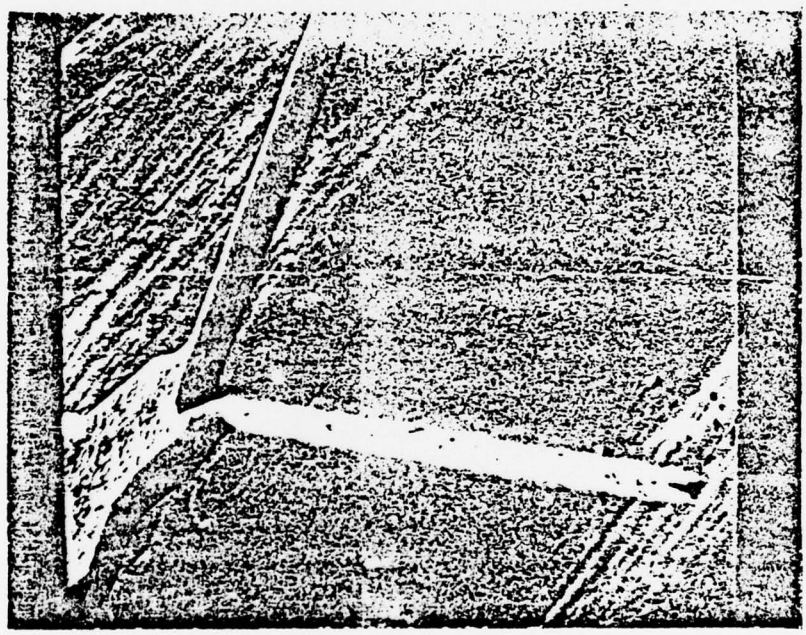


Fig. 4. SEM picture of etch on (001) wafer along the $\langle 1\bar{1}0 \rangle$ direction. Etch depth 5 microns. (1040x)

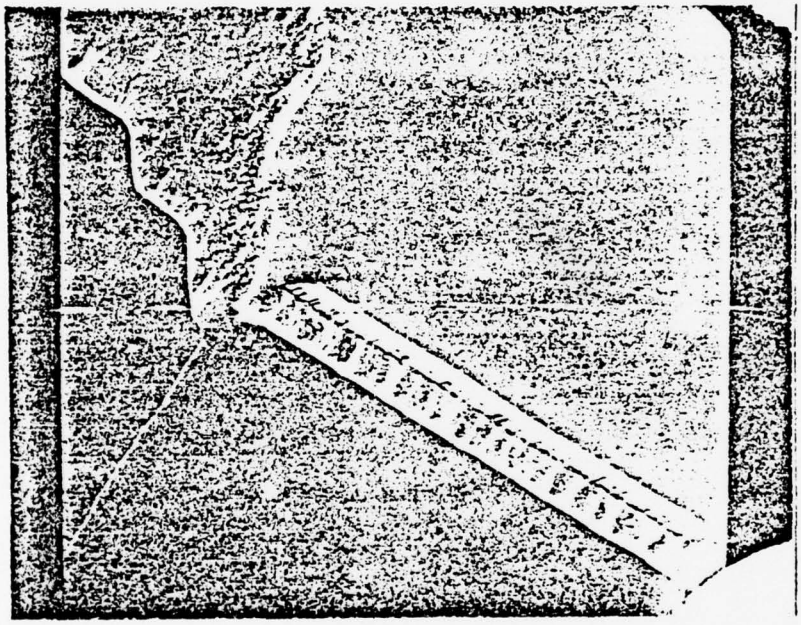


Fig. 5. SEM picture of etch on (001) wafer along the ⟨110⟩ direction. Etch depth 5 microns. (1040x)

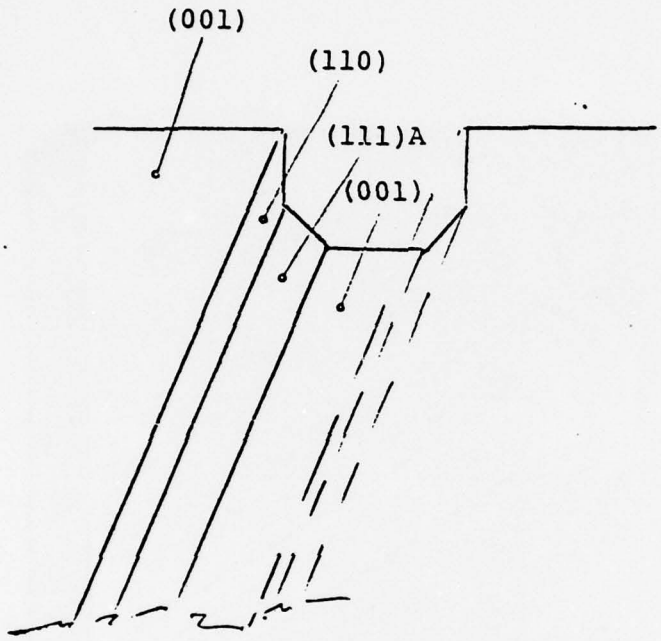


Fig. 6. Planes participating in etch along the ⟨110⟩ direction.

lines about 3-microns wide and about 1.5-microns apart was then used to deposit the pattern on 1500 Å thick SiO_2. The wafer could now be etched in-situ, in an $AsCl_3/H_2$ flow divided between the etch line and the source with the substrate at 750°C, anywhere between 5 to 9 min and still get the complete V-shaped groove. Using a 9½ min etch time the undercut below the SiO_2 mask could be made such that the grooves are as little as 0.2 micron apart. Figure 7 shows the etched lines along the $<1\bar{1}0>$ and the <110> directions, and Figure 8 shows the cleaved section of the wafer showing the etched grooves along the $<1\bar{1}0>$ direction. Although the etch was about 8-microns deep in the larger grooves, the smaller pair of lines only etched about 2-microns as seen from Figure 8. Figures 9 and 10 show the control that can be attained in etching these grooves. Figure 9 is the cleaved section of the surface shown in Figure 10. The two small pairs of grooves are about 0.2-microns apart.

Etching the $(1\bar{1}0)$ plane surface of GaAs with groove directions along <110>, <001>, <112>, and $<11\bar{1}>$ did not show any direction with desirable well shape, and undercut was always excessive. Wafers with (111) surfaces are unsuitable because of the asymmetric etching rates on either side of the trough. The (001) plane of GaAs was therefore chosen with the groove direction along $<1\bar{1}0>$ as giving the most suitably-shaped V-groove, whose etch was easily controlled and reproducible. For the same gate length, the V-shaped sides will mean a lower gate resistance as compared with the vertical sides shown in Figure 1. Also, less field crowding at the corners should increase the breakdown voltage.

2.2 Gate Trough Growth

Figure 11 shows the etch and growth on the (001) plane for mutually perpendicular mask lines. The controlled undercut of the $<1\bar{1}0>$ direction is again readily apparent.

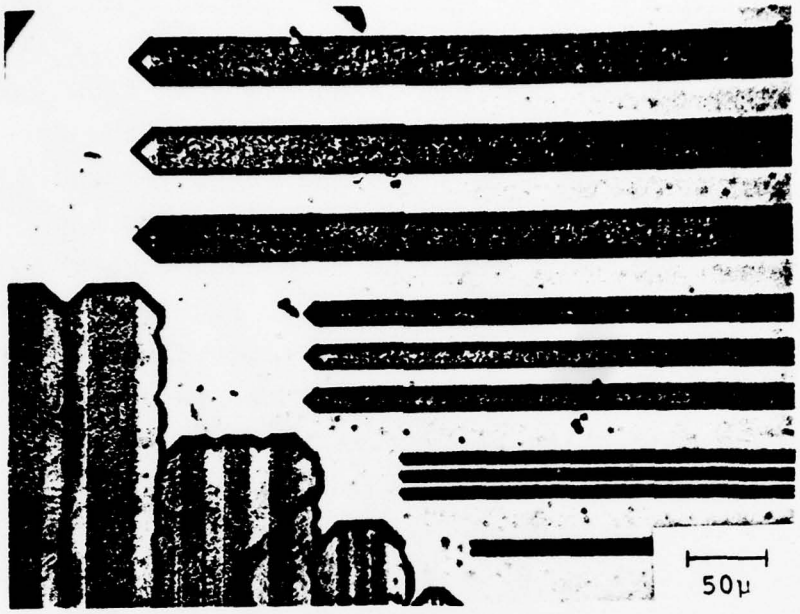


Figure 7.

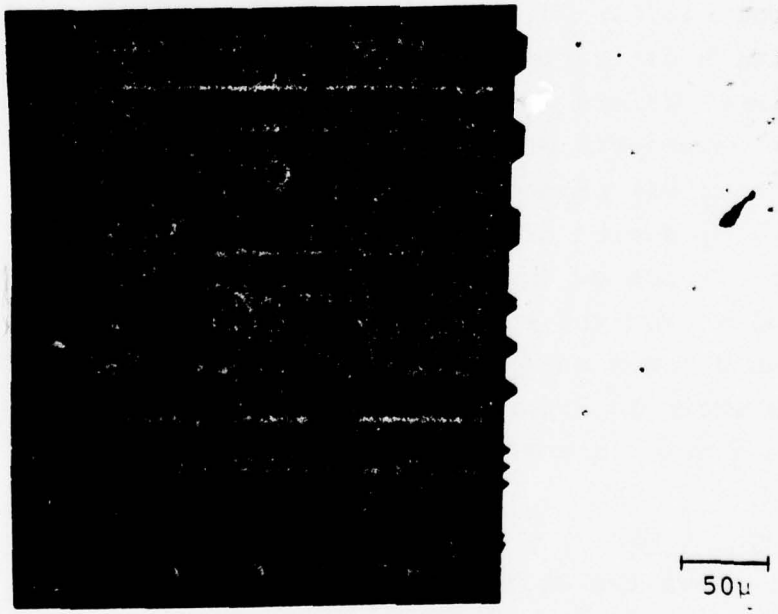


Figure 8.

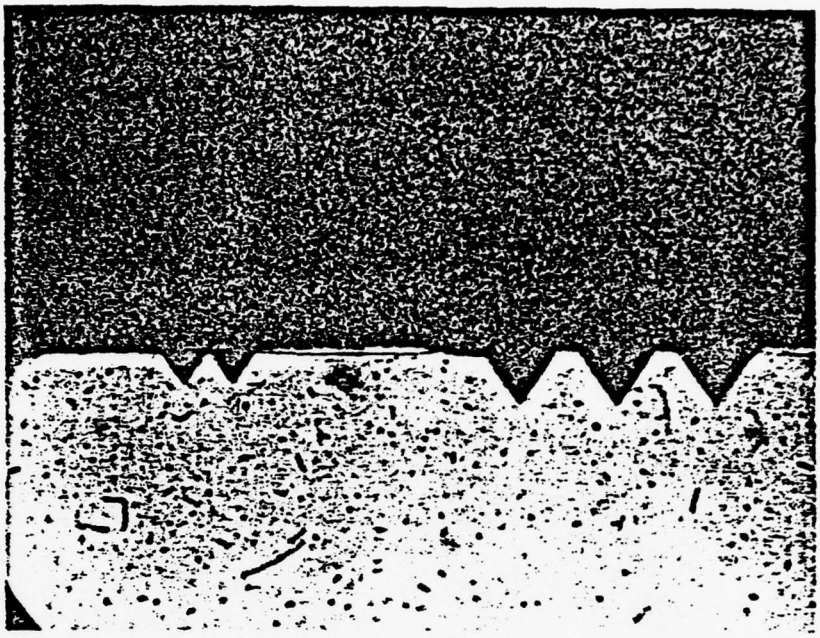


Figure 9.

Figure 10.

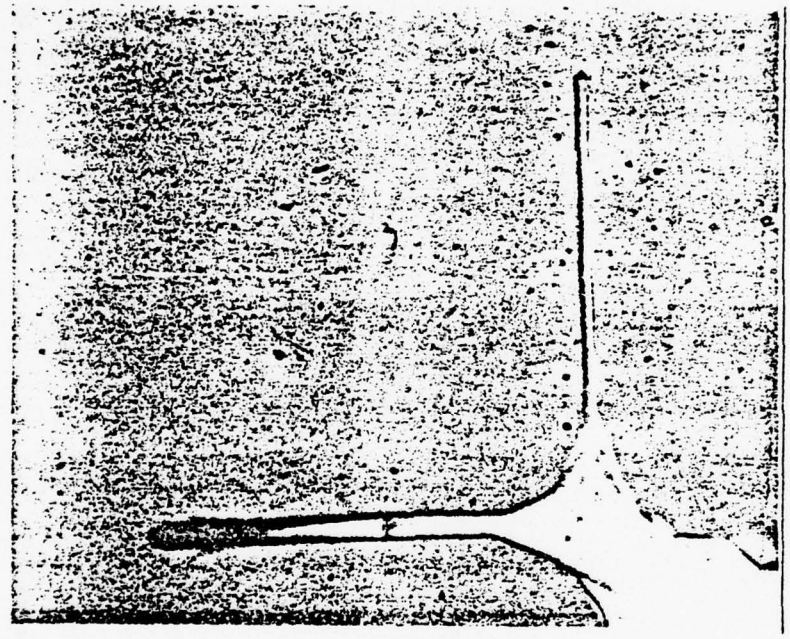


Fig. 11. Etch and growth on (001) plane along the $\langle 110 \rangle$ and $\langle 1\bar{1}0 \rangle$ directions. (544x)

Etch and growth of CVD GaAs on the (001) surface was then attempted for adjacent V-grooves along the $<1\bar{1}0>$ direction. Figure 12 shows the smallest pair of grooves on the resolution mask etched for 7 min with a vapor growth of 3½ min. The final surface is seen to be (100). Figure 13 shows the larger lines etched and filled in the same run as shown in Figure 12. The growth plane in this figure is the intermediate plane in the growth series and is (311)B.

Growth rate of vapor phase GaAs on GaAs substrates is in decreasing order on planes {111}A > {211}A > {211}B > {311}B ≃ {311}A > {100}. The growth rate on {111}B planes is negligibly small as compared to other planes. Hence in the groove terminating in the {111}B planes when aligned along the $<1\bar{1}0>$ direction on the (001) plane, growth essentially starts at the {211}B planes and continues next to form {311} B planes and on to form the higher index planes, ultimately ending in the {100} plane. Figure 14 shows a sketch of the successive growth of the planes.

In order to simulate more closely the V-groove center-to-center spacing of 4-microns and also facilitate the study of variations over the wafer surface, a mask was made with 2-micron gaps and spaces extending the full width of the mask. The starting wafer of (001) GaAs was provided with 1500 Å thick SiO_2 stripes 1.3-microns wide produced by the usual photolithographic technique. These were 4-microns apart and along the proper [110] direction as shown in Figure 15. The vapor etching was done by bubbling H_2 through the $AsCl_3$ bubbler at 20°C and directing half the flow through the Ga source at 825°C and the other half through the etch line. The substrate was at 760°C. Figure 16 shows the cleaved section perpendicular to the grooves vapor-etched

Figure 12. Etching and regrowth in V-grooves.

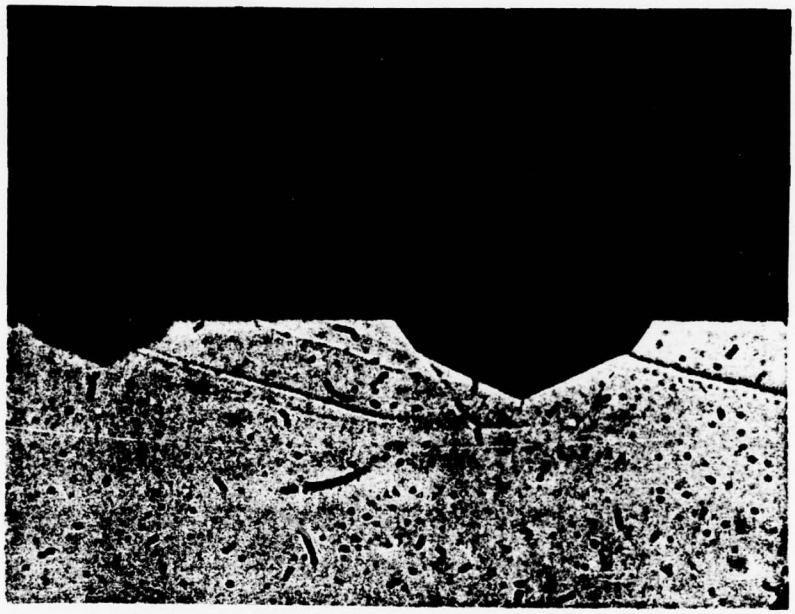


Figure 13.

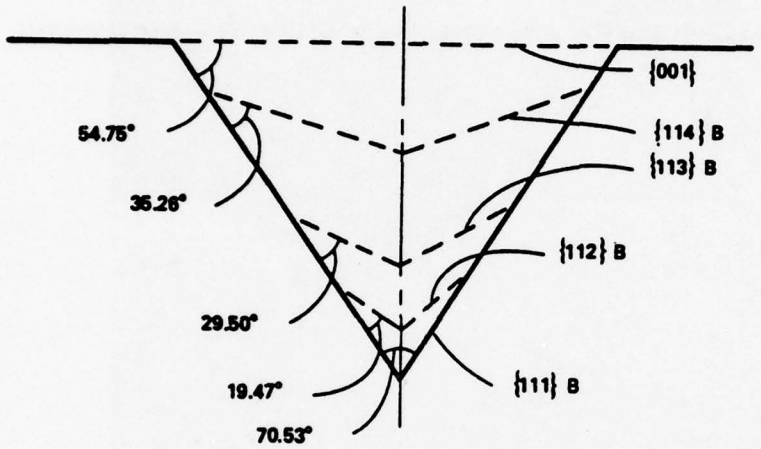


Figure 14. Growth of GaAs planes in the $[1\bar{1}0]$ directional groove bounded by {111}B planes.

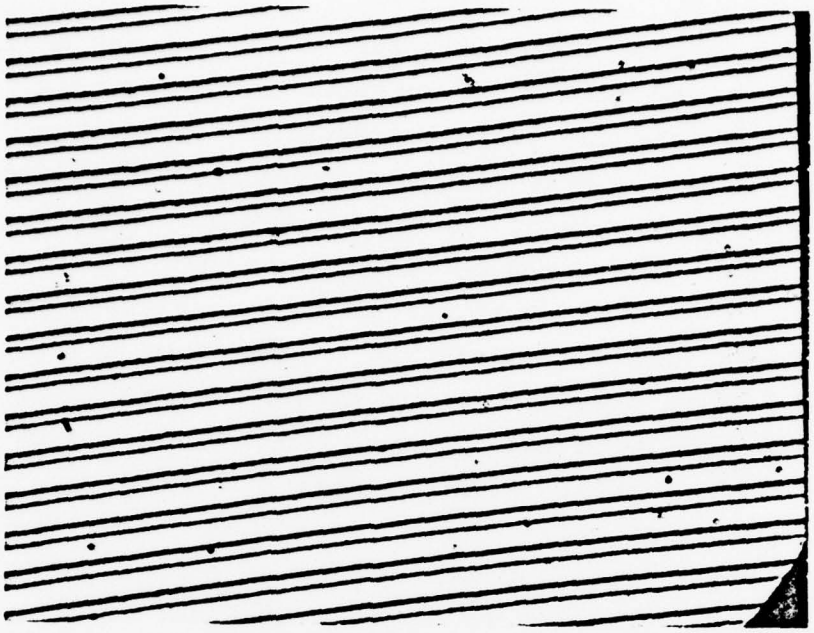


Figure 15. Magnification 1400x.

Figure 16. Magnification 1400x.

at a total flow rate of 420 cc/min for 10 min. A few of the grooves in this wafer were large as shown in this figure. Such large grooves are due to coalescence of adjacent grooves and can form due to (1) over-etching, (2) variation in the widths of the SiO_2 stripes or (3) when a few of the SiO_2 stripes come loose from the substrate due to poor adhesion. The size of the groove was also larger at the upstream end than at the downstream end suggesting depletion of HCl from the gas stream as it passes over the wafer. Figure 17 shows the refilled grooves with a 4 min etch and a 2 min growth at a flow rate of 420 cc/min. After refilling the grooves, the SiO_2 layer was removed and a 10^{17} Sn-doped GaAs layer 2500 Å thick was deposited. The cleaved section of such a wafer is shown in Figure 18. The top surface of the wafer is shown in Figure 19. The contrast is due to the small difference between the surface of the refilled region and the original wafer surface and allows alignment of the gates. Figure 20 shows a thick Sn-doped GaAs layer (1.2 microns) and demonstrates that such a layer can be grown on the "vees," with a minimum amount of vapor-etch prior to deposition.

Summarizing, the etching can be stopped just at the moment when the adjacent edges of the "vees" meet and the "vees" can be refilled to be flush with the initial surface of the wafer. It has also been shown that after removing the SiO_2 layer from this wafer, a thin layer of GaAs, Sn-doped to $10^{17}/cm^3$, could be deposited on the wafer with a minimum of etching prior to growth. Further work showed that this technique was fairly reproducible although quite sensitive to a number of variables such as source size, amount of deposits in the deposition zone of the reactor, the width of the SiO_2 windows and the quality of adhesion of the SiO_2 lines to the substrate surface. Thus although the

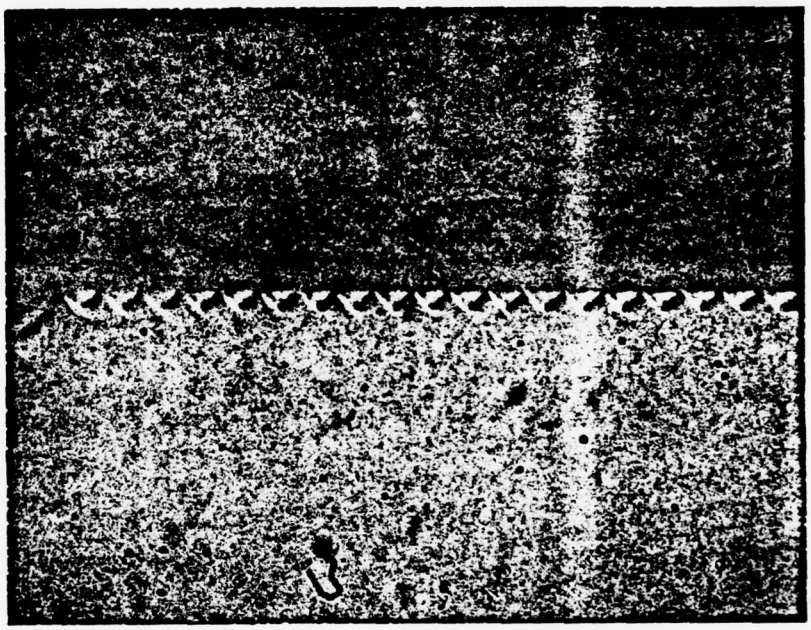


Figure 17. Magnification 1400x.

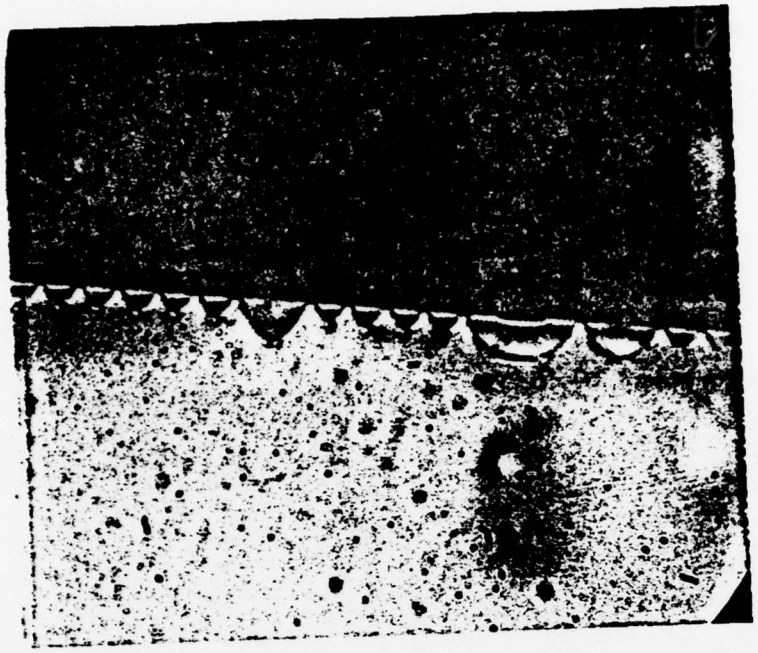


Figure 18. Magnification 1400x.

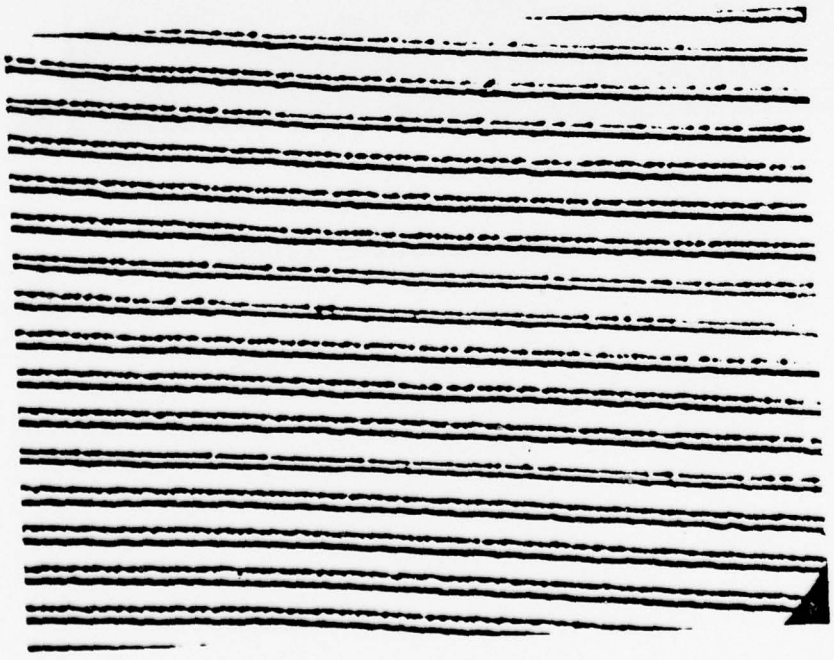


Figure 19. Magnification 1400x.

Figure 20. Magnification 3766x.

optimum conditions of etch and growth appear to be different every time the Ga source is changed, these could be determined in about 4-6 experiments. To control the width of the SiO_2 windows, a new wafer polishing technique using dilute sodium hypochlorite was instituted. This produces a much flatter wafer surface compared to that obtained using the Br-methanol polishing technique and allows the mask to make contact over a larger area during the photolithographic process.

2.3 Mesa Definition and Field Growth

Besides the insulating "vees" under the active source and drain electrodes, insulating regions must be provided under the source and drain pads and connecting metallization. This is analogous to the mesa etch used for devices fabricated on a semi-insulating substrate, and must not only insulate but also provide low capacitance to the underlying p^+ substrate. However, edges along the <110> direction perpendicular to the "vee"-direction undercut the oxide mask around 20 microns while etching down only 7 microns, and hence are not desirable edges for device fabrication. However, edges at 45° to the <110> directions were found to undercut only around 2 to 4 microns while etching to a depth of around 10 microns. Accordingly, the source and drain pads and interconnection lines will have their edges aligned at 45° to the <110> directions. These will have to be filled with GaAs in a separate run, however, since the time to fill these is quite different from the time to fill the "vees."

In the time needed to fill the "vees," the deposits in the pad area are only about 2 microns thick. Therefore these will have to be filled with semi-insulating GaAs in a separate run. The conditions of etching and refilling of the pad areas were established using a GaAs wafer containing pad areas and lines as in Figure 21. The cleaved section of

a vapor-etched and grown pad is shown in Figure 22. The surface of the refilled pad is always a little above the wafer surface because of the way in which the pad is filled. The height of the mesa is a function of the width of the SiO_2 opening and should be quite small (of the order of a micron) in the actual device.

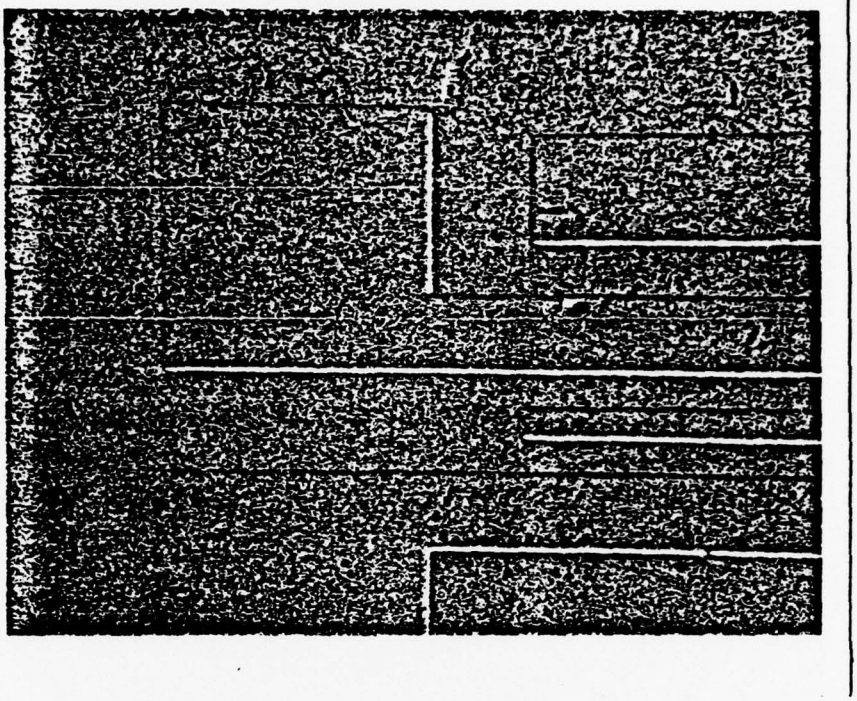


Figure 21. (290x)

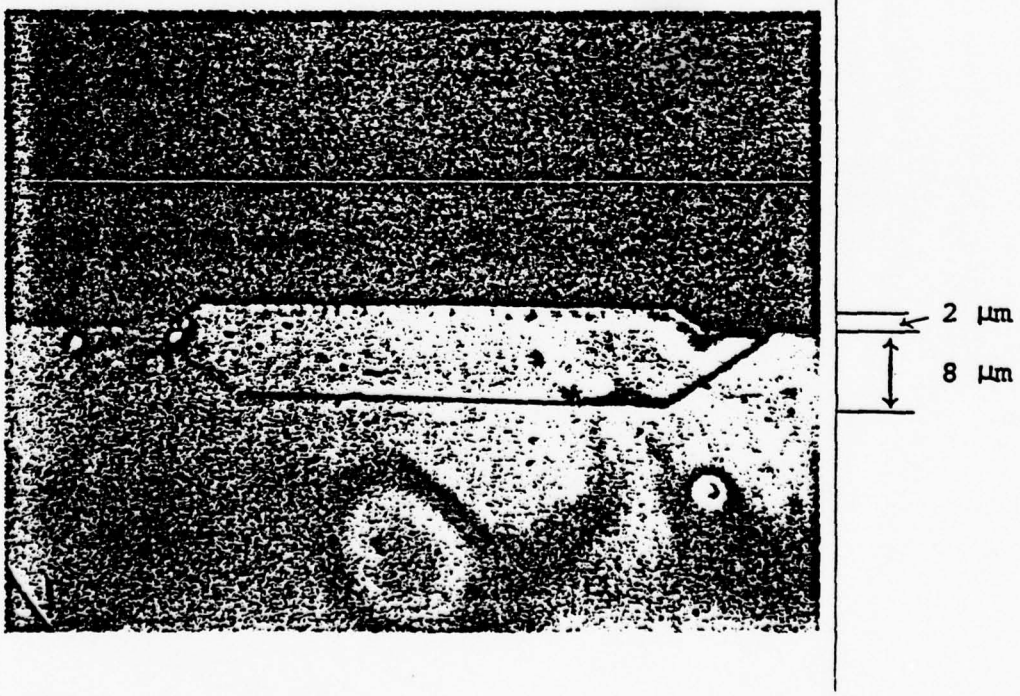


Figure 22. (1400x)

3. DEVICE FABRICATION ON Cd-DOPED SUBSTRATES

Cd-doped substrates were received from Metal Specialties, having a (100) surface and a doping range of $3 - 9 \times 10^{17} cm^{-3}$. The processes developed using the n^+ Te-doped substrates were repeated on the Cd-doped substrates to ensure their viability.

3.1 Etching Characteristics

The etching process was found to be significantly different for the Cd-doped wafers compared with the Te-doped wafers used for the preliminary work. The etching of the "vees" in the Cd-doped GaAs wafers was about five times faster than in the Te-doped GaAs. Also, after the adjacent "vees" have joined and the SiO_2 lines have fallen off, the cleaved cross section of the over-etched Te-GaAs shows large "vees" due to the coalescence of adjacent "vees." In the Cd-GaAs however the "vees" get rounded at the top edges and the surface slowly flattens out with very little coalescence.

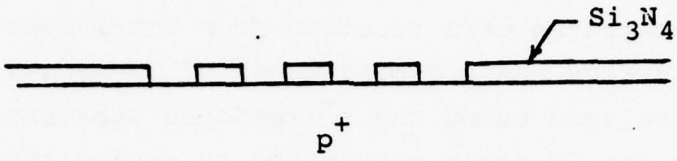
The different etching characteristics for the "vees" on the p^+ material prompted redoing the etch and growth experiment for the areas under the source and drain bonding pads. A quick etch experiment revealed that, as for the n^+ material, the <100> directions are the next slowest, and pattern edges aligned along the <100> directions gave only about 2 microns of oxide uncercut for an etch depth of 5.5 microns. The device edges will thus lie along the <100> and <100> directions.

Accordingly, Figure 23 gives the fabrication sequence for the noncoplanar power FET and Figure 24 the mask set design corresponding to this sequence. The design consists of 1.5, 3, and 6 mm gate width devices along with many test structures and alignment marks. The source and drain

NONCOPLANAR POWER FET FABRICATION SEQUENCE

"Vee" Photolithography

(1)



"Vee" Etch and Growth

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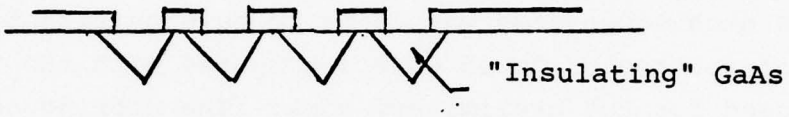

Nitride Strip and Epitaxial Growth

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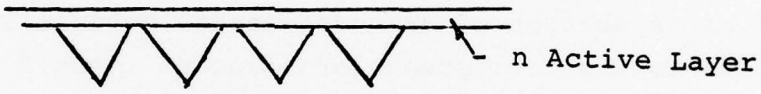
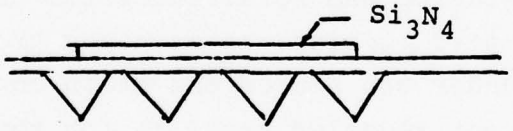


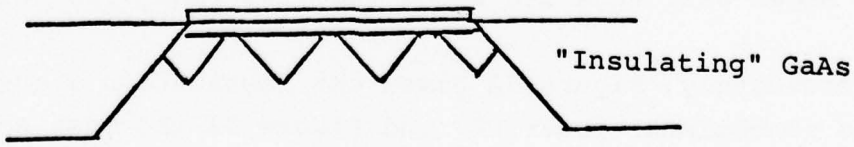
Mesa Photolithography

(4)



Mesa Etch and Field Growth

(5)



Source-Drain Metalization

(6)

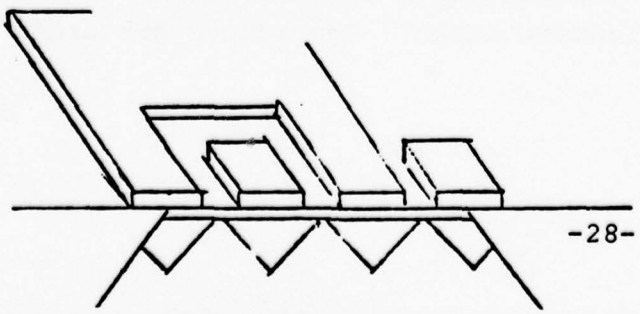


Figure 23.

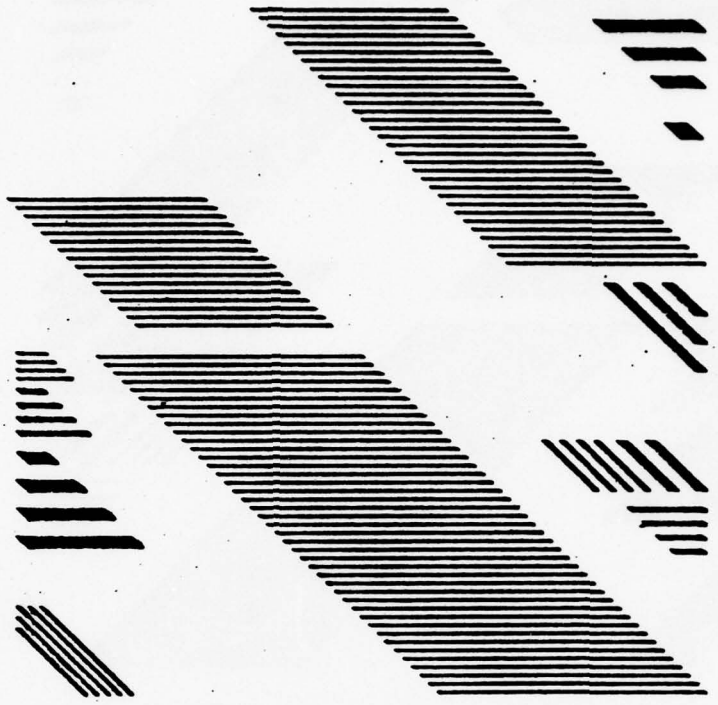


Figure 24(a). Vee etch and growth mask.

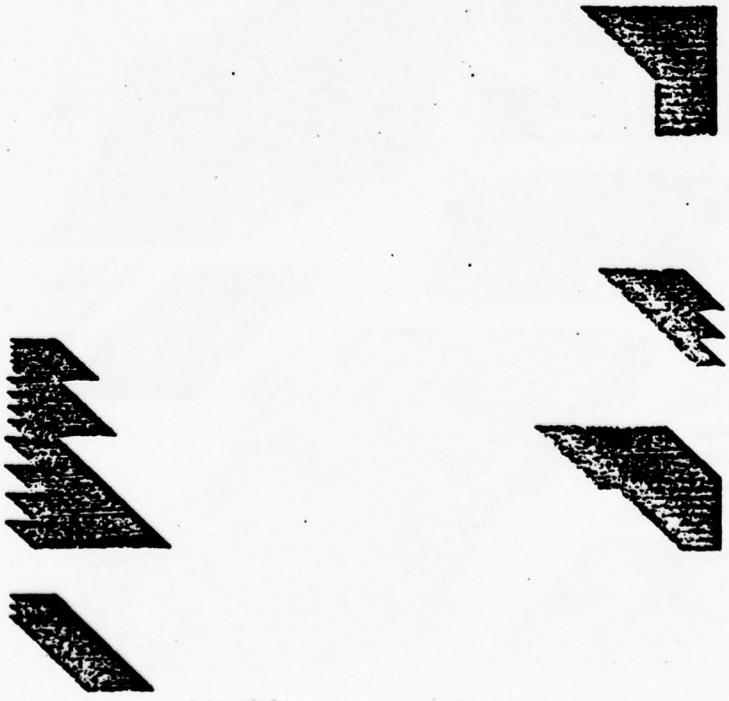


Figure 24(b). Nitride strip mask (protects alignment marks).

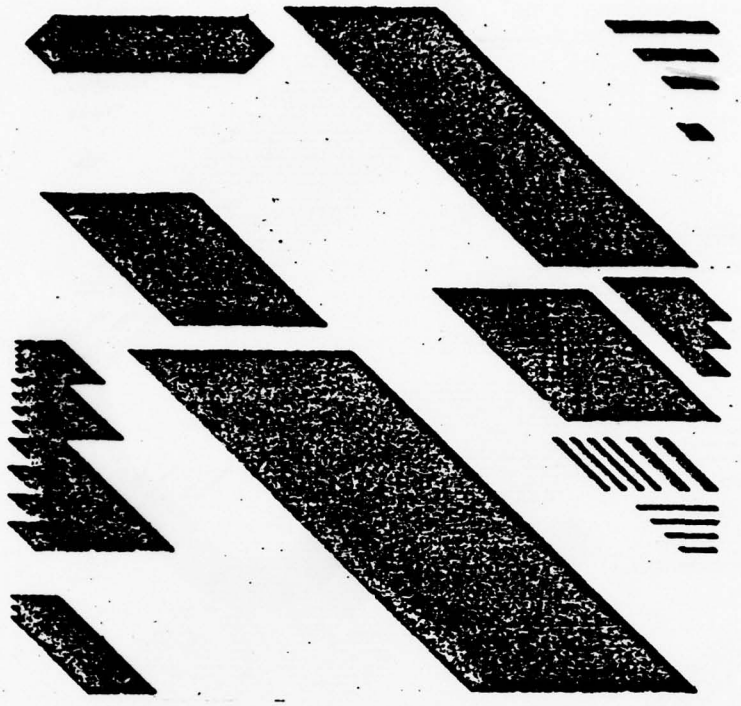


Figure 24(c). Mesa etch mask.

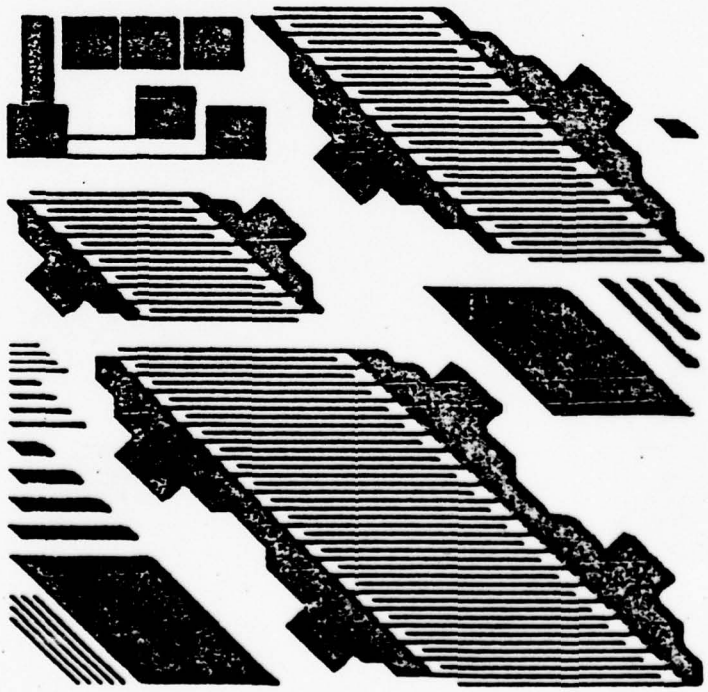


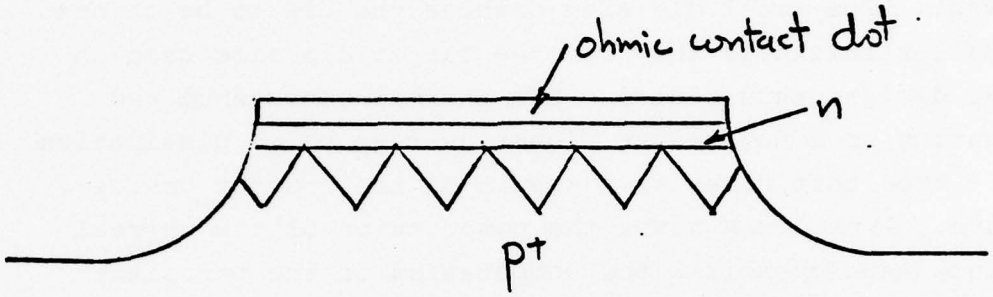
Figure 24(d). Source-drain metallization mask.

fingers are interdigitated with the gate repetition period being only 6 microns. The 1.5-mm device, for example, only occupies an area of approximately 100 x 100 microns. Not shown is the integral heat sink mask which will enable the substrates to be thinned to 1 to 2 mils and then plated up with gold to a thickness commensurate with handling and die attachment. The small die size enables the die to be thinned to a smaller thickness than can the larger die size used in coplanar design, thus reducing the thermal resistance and compensating to a degree the higher average power dissipation per unit area that comes as a result of the compact device structure. Appendix A gives the computation of the thermal resistance and Appendix B the computation of the parasitic capacitance expected for this structure.

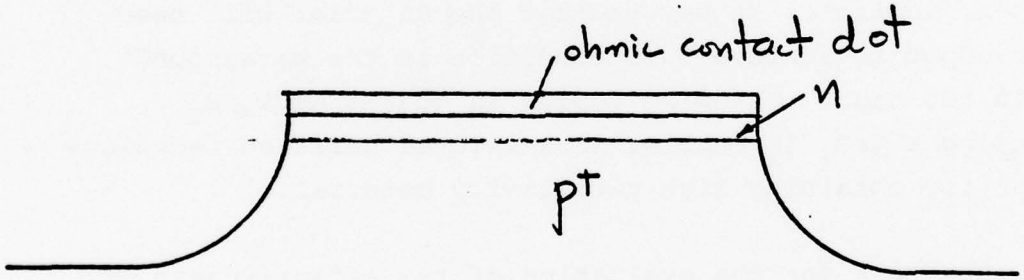
3.2 Electrical Characterization of the Vees

To be most effective, the "vees" will have to be low-doped enough to be fully depleted by the built-in voltage of the p-n junction. It may be that the material will need to be Cr-doped to achieve this condition if the background doping is too high. Chromium doping in the $Ga/AsCl_3/H_2$ system using a CrO_2Cl_2 bubbler is a well-established technique at Varian for obtaining high resistivity material.

An easy test for the evaluation of the effectiveness of the "vees" in reducing the parasitic capacitance of the p^+ gate to the n-epitaxial layer above it is shown in Figure 25. In Figure 25(a), after the "vees" have been etched and grown, the oxide mask is stripped and an n-active layer is grown, followed by a 20-mil dot ohmic contact to the n-layer and a subsequent mesa etch to isolate the dots. The capacitance of this mesa, when compared to one without the "vees" (as shown in Figure 25(b)), will give the reduction in parasitic



(a)



(b)

Figure 25.

capacitance that the "vees" effectively accomplish. The "vee" center-to-center spacing of 4 microns is so much smaller than the 20-mil diameter of the dot that alignment of the dot with respect to the "vees" is unimportant.

Accordingly, a 6 x $10^{16}cm^{-3}$ n-epi layer was grown on undoped "vees" whose edge-to-edge spacing (gate length) was around 0.2 micron, and the resulting zero-bias mesa capacitance was only 5-8 pF. This compares with 300-400 pF for the structure of Figure 25(b), for which the n-epi layer doping was 1.2 x $10^{17}cm^{-3}$. Thus, the "vees" accomplish about a factor of 50 reduction in capacitance for a gate length of around 0.2 micron. The parasitic component of the capacitance, of course, would actually be the remaining capacitance after the legitimate gate capacitance is subtracted out. It appeared that the "vees" were sufficiently low-doped to serve their intended function without resorting to Cr-doping.

3.3 Single Gate Device Run

With the masks for the structure shown in Figure 24 not yet completed, it was decided to make a dummy run using in-house masks which would simulate a single gate of the inter-digitated structure in order to be able to work out any remaining bugs in the process and to study such electrical characteristics as gate leakage and breakdown, pinchoff, etc.

"Vee" patterns were etched and grown over the whole wafer using the mask pattern shown in Figure 15. A $10^{17}cm^{-3}$ Sn-doped active layer was then grown over the whole wafer after the oxide mask was stripped. No vapor etch was used for the active layer growth lest the "vees" be eliminated. During the source saturation a highly doped Sn layer grew until the source was saturated, after which the layer was allowed to be etched. At just the point the layer was

etched off, the active layer was grown to the desired thickness. Figure 26 shows the resulting growth over the "vees."

Next, the mesa pattern for the active layer was defined with an oxide mask using the AMOS mask set intended for MOS devices on silicon. The intention was to etch out the field and regrow insulating material as depicted in Figure 23 in steps (4) and (5) and then put down the source and drain patterns on the mesa. The source and drain are spaced 5 microns apart and hence would have one gate between them to pinch off the channel. Gates would also exist under the source and drain contacts, but should not preclude the devices from showing good dc characteristics.

Although the "vees" need only be low-doped to perform well, it is imperative that the field growth be insulating lest there be parasitic conduction between the source and drain contacts. Consequently, Cr-doping must be employed in the field growth. Prior to the etch and growth of the field a routine check on the background doping of GaAs produced in the system was made. This was necessary since a background doping of less than $10^{15}/cm^3$ is needed to produce good Cr-doped GaAs epitaxial layers. It was found that the background doping had gone up to $2 \times 10^{16}/cm^3$ n-type. A number of attempts were made by changing the Ga and the $AsCl_3$ sources and cleaning the reactor components to bring the doping down. These were not successful. It was later discovered that the high background was due to a shift in the furnace profile along the Ga source, causing bare Ga to be exposed and allowing more impurities to be imparted to the gas stream. The profile was adjusted to the original shape. The background doping was now about $10^{15}/cm^3$ and excellent Cr-doped GaAs was grown on Cr-doped substrates. While recalibrating the system's growth rate after the

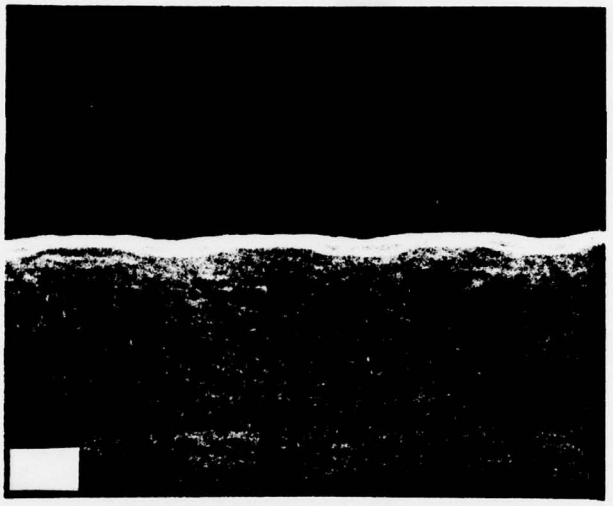


Figure 26.

source profile temperature change, the CrO_2Cl_2 in the bubbler went bad, causing the growth rate to become very low. This growth rate must be raised before the device fabrication can proceed lest by an excessive amount of time Cd diffuses through the active layer.

4. SOURCE AND DRAIN OHMIC CONTACTS

In order to minimize the power losses in the 4-micron wide source and drain fingers, the finger metallization should be at least around 0.5 micron high. In the past such thicknesses were achieved by first depositing the traditional thickness to achieve good ohmic contacts, then alloying the contacts, and finally putting down an Au overlay to achieve the desired total thickness. The overlay of course requires a second alignment in the photo-resist process. With the noncoplanar design such a realignment of the fingers would not be desirable, since there is only a 2-micron gap between the fingers to fit the gate into, and a misalignment of only 1-micron would halve this gap and perhaps result in the gate ending up under the finger rather than between the fingers as it should. It would be preferable to deposit the total metallization thickness all at once and lift it off, if this could be done without degrading the contact resistance. The standard thickness is 1000 Å of Au over 500 Å of Au-Ge/Ni, and it is desired to increase the Au thickness to around 5000 Å.

To determine the effect of increasing the thickness of the Au over the Au-Ge/Ni layers before the alloy, three different depositions were made: 1000 Å (standard), 2500 Å, and 5000 Å of Au over 500 Å of Au-Ge/Ni. After alloying, the contact resistance was determined by extrapolating a plot of resistance vs contact spacing back to zero spacing. The results were 4×10^{-6} ohm-cm^2 for the 1000 Å slice, 10^{-6} ohm-cm^2 for the 2500 Å slice, and 4×10^{-5} ohm-cm^2 for the 5000 Å slice (all of the slices were pieces from the same epitaxial wafer). In addition to a higher contact resistance, the data for the 5000 Å slice were much more scattered than

for the other two thicknesses. This experiment is being repeated to verify the unexpected 5000 Å result. The explanation may lie with Ge or Ni depletion by the thicker Au, or increased lattice strain in the GaAs. If the problem is real, it may be solved by electroplating the contacts with Au after alloying. This appears simpler than trying a barrier metal between the Au-Ge/Ni and the Au overlay.

5. CONCLUSIONS

Referring to the structure of Figure 1, no fundamental difficulties have been encountered that would preclude the realization of such a structure. The technique for etching and refilling the low-doped grooves under the source and drain contacts has been developed using a V-shape, which in fact is better than the profile shown in Figure 1 from the point of view of achieving lower gate resistance. The slow etching rate of the (111)B surfaces has been found to give good control in producing submicron gate lengths over a large wafer area. Gate lengths as low as 0.2 micron have been achieved with this technique, which certainly exceeds the original expectations. Electrical characterization of the "vees" has demonstrated on the order of a factor of 50 in the reduction of the parasitic capacitance.

Good active layer growth has been achieved over the "vees" without vapor etch, and the <100> direction was found to be the direction of minimum undercut for the formation of mesas and insulating field growth. A mask set was designed accordingly and was received at the end of this reporting period.

A dummy device run was started with in-house masks, but was stopped at the point of etching and growing the insulating field because of the high n-type background in the reactor. Eliminating the temperature gradient that had developed across the source lowered the background, at which point the CrO_2Cl_2 in the bubbler went bad and is in the process of being changed. These problems are not fundamentally related to the noncoplanar fabrication process and should not be viewed as areas of potential difficulties. As of yet,

growth and characterization of insulating GaAs on Cd-doped substrates has not been attempted. This will be done after installation of new CrO_2Cl_2, and if successful, the device run will be completed.

Problems with contact resistance were experienced when alloying was done in the presence of the needed thick overlay metal. It may be that the problem can be solved with either a barrier metal or electroplating the contacts with Au after alloying.

6. RECOMMENDATIONS FOR FUTURE WORK

Besides the previously mentioned tasks of growing insulating material on Cd-doped GaAs, completion and evaluation of noncoplanar devices, and solving the contact resistance problem when a thick Au overlay is included during the alloy, other potential problems and solutions may be as follows:

(1) Use of a p^+ buffer layer to minimize diffusion of Cd into the "vees" and the active layer (by using a slower diffuser such as Ge). Better junction characteristics may also result by use of a buffer layer.

(2) Perfection of the integral heat sink technology for the noncoplanar devices.

(3) Elimination of junction leakage problems resulting from coincidence of the p-n junction with the growth interface by the use of diffusion or ion-implantation.

APPENDIX A
POWER FET THERMAL RESISTANCE

For the structure shown in Figure A.1,

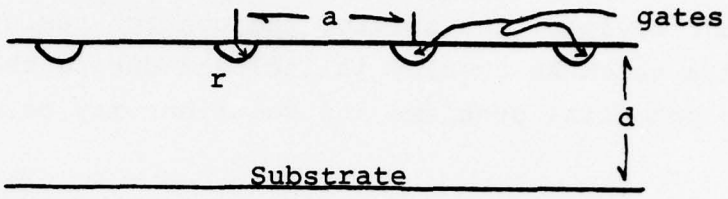


Figure A.1

if it is assumed that all the heat generated at the gate is carried away through the substrate (and none by the top contacts or through the air), then it is sufficient to solve for the capacitance from the gate cylinders to the substrate base, replace ε by the thermal conductivity k and take the reciprocal to obtain the thermal resistance. By eqs. (7.13), (7.14) of Spangenberg's Vacuum Tubes,

$$C = \frac{q_c}{V_g} = \frac{Z\varepsilon a}{d - \frac{a}{\pi}\ln\left(2\sin\frac{\pi r}{a}\right)}$$

where $q_g = -2q_c$, $d_{cg} = d_{gp}$ and $V_p = 0$. The thermal resistance per gate is thus

$$R_{th} = \frac{d - \frac{a}{\pi}\ln\left(2\sin\frac{\pi r}{a}\right)}{Z\,ka}$$

The equal temperature lines are circles around the gates and horizontal lines at the substrate base.

As an example, for the coplanar power FETs fabricated at Varian, d = 8 mils, r = 0.5 micron (one micron gates), a = 53 microns and Z = 3.5 mm, so using k = 0.4 W/cm^{o}K gives

$$R_{th} = 33.4^{o}\text{C/watt.}$$

For the noncoplanar structure of Figure 24, letting d = 1 mil (the smaller die size should enable the substrate to be thinned to this dimension), r = 0.5 micron, a = 6 micron and Z = 3.5 mm,

$$R_{th} = 31.1^{\circ}C/watt,$$

so the reduction in gate spacing will not result in a higher thermal resistance provided d is reduced accordingly. It should be easier to flip-clip the noncoplanar device because of the fewer bonds needed on the top surface.

APPENDIX B
NON-COPLANAR PARASITIC CAPACITANCE

For the "vee" structure shown in Figure B.1,

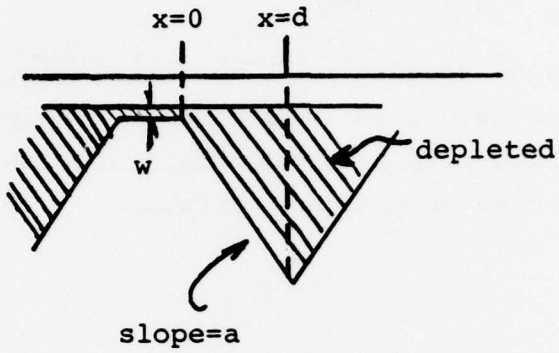


Figure B.1

if fully depleted, then for the "vee" portion only

$$C = \frac{\varepsilon Z}{a} \ln \frac{w + ad}{w} .$$

With $w \simeq 0.1$ micron for $10^{17} cm^{-3}$ material and zero gate bias, in the limit of zero gate width $d = 3$ microns and $a = \sqrt{2}$ for the design of Figure 24,

$$C = 2.67 \varepsilon Z$$

while without the "vee,"

$$C = \frac{\varepsilon Z d}{w} = 30 \varepsilon Z,$$

giving around an order of magnitude reduction in the parasitic capacitance.

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