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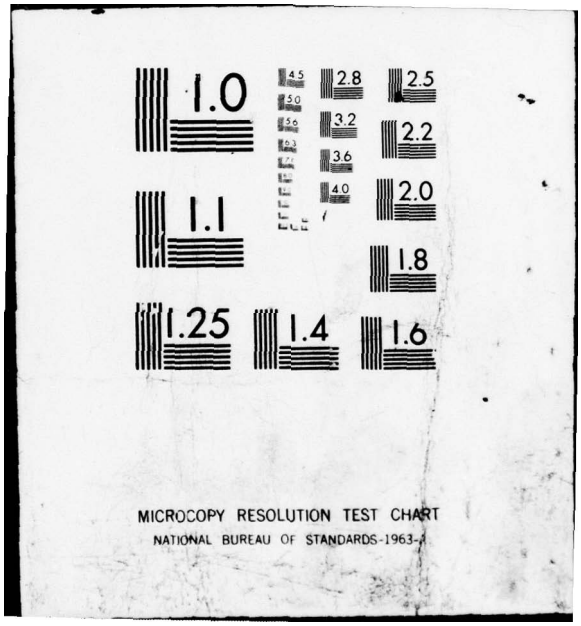
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A detailed description of CID image sensing and the various readout techniques is given. The results of theoretical and experimental studies of temporal and fixed pattern noise that affects CID imager performance are presented. The effects of feedback on amplifier noise charge are derived. A short study on the low frequency noise of buried channel MOSFETs has also been performed. The use of multiple non-destructive readout operations and off-chip signal summation has been used to demonstrate more than a factor of 10 improvement in signal-to-noise ratio. No intrinsic

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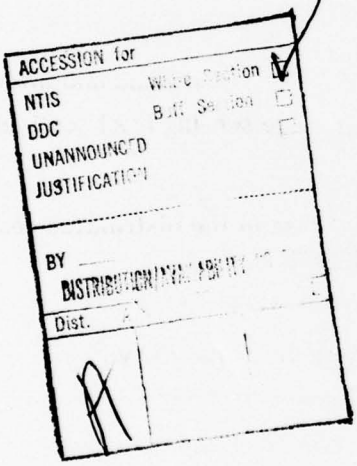
20. ABSTRACT

limitation on the dynamic range improvement that can be obtained with this technique has been identified. External limitations such as the time available for readout have prevailed to date.

Standard CID imager noise levels have been evaluated. The dynamic range measured varied between 500-to-1 for the TV compatible Pre-injection readout technique to over 30,000-to-1 for a cooled Row Readout array operating at low video rates. Uncorrected signal-to-RMS fixed pattern noise ranged from 30-to-1 for Row Readout 1000-to-1 for Sequential Injection readout. Fixed pattern noise was surpressed to below 1 part in 30,000 with off-chip cancellation circuitry.



SUMMARY

The Charge Injection Device (CID) is a conductor-insulator-semiconductor structure that employs intracell charge transfer and charge injection to achieve an image sensing function. This device is significantly different from tube and Charge-Coupled Device (CCD) image sensors and consequently has different temporal and fixed pattern noise limitations. A number of readout techniques are possible with the CID structure, each possessing separate noise performance. The general objective of this study program has been to identify the temporal and fixed pattern noise sources that affect CID imager performance, define the theoretical level of these noise sources, and determine the limiting noise components and their magnitude for the various readout techniques.

The approach used has been to evaluate the magnitude of each significant noise source theoretically and, where possible, obtain experimental verifications of the theoretical values. Existing image sensing arrays and circuit test device designs have been used for the experimental verification testing.

In order to supply the background knowledge necessary to understand and interpret the noise study results, a detailed description of CID image sensing has been included in this report.

The significant temporal noise sources are Johnson noise in the distributed resistance of array conductor materials (e.g. polysilicon), in the channel resistance of MOS multiplex selection switches, and in the video amplifier. The effects of feedback on noise performance have been investigated, and the conditions for minimum amplifier noise have been identified. Correlated double sampling can be used with two of the readout techniques, Sequential Injection and Row Readout, to avoid KTC noise. The dynamic range measured varied between 500-to-1 for the TV-compatible Pre-injection Readout technique to over 30,000-to-1 for a cooled, Row Readout array operating at low video rates (160 pixels per second).

A source of both temporal (shot) noise and fixed pattern noise is array dark current and the spatial variation in this dark current, respectively. There are two factors that lead to very low dark current in CID arrays. First, only the charge storage region, which is smaller than the photosensitive region, is depleted and contributing significant dark current. The second factor is that the interface states that result in surface leakage current are continuously quenched under normal imager operating conditions with the result that only the depleted periphery of each charge storage site contributes surface leakage. Since good quality charge transfer structures are normally surface leakage current dominated, this is an important effect.

The major sources of fixed pattern noise are different with the various readout techniques. Sequential injection is a destructive readout technique that automatically cancels multiplexer interference and array fixed pattern variations. The fixed pattern noise measured on a random access array operating with sequential injection readout was approximately a factor of 1000 below the saturation signal, lower than the temporal noise. With Pre-injection Readout, multiplexer switching noise couples directly into the video signal bus leading to a high level of fixed pattern noise. Since this component of fixed pattern noise repeats during each line of video, it is readily cancelled with the aid of one line of video storage. Fixed pattern noise after this type of cancellation has been measured as a factor of 250 below saturation. Row Readout operates through the driving of one set of array lines to cause signal charge to transfer to the orthogonal set of array lines with the result that switching noise is greatly suppressed. Raw fixed pattern noise levels of approximately three percent of saturation have been measured. In a low video rate device, fixed pattern noise was suppressed to below one part in 30,000 of saturation with this readout method.

Another significant result of this study has been the demonstration of the processing gain that can be achieved with multiple non-destructive readout operations. The extremely low-loss non-destructive readout capability of the CID structure results in the capability to read imager signals repeatedly for summation in external memory. Since the temporal noise that accompanies the signal sums incoherently, the signal-to-noise ratio improves in proportion to the square root of the number of readout operations. Noise levels below 100 carriers per pixel have resulted with this technique. No intrinsic limitation on the dynamic range improvement that can be obtained with this technique has been identified. External limitations, such as the time available to perform repeated non-destructive readout operations, have prevailed to date.

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Section 1

CID IMAGE SENSING

The Charge Injection Device (CID) is a surface channel device that employs intra-cell charge transfer and charge injection to achieve the solid state image sensing function. Photon-generated charge signals are collected and stored in an array of MOS charge storage capacitors. The level of signal charge is detected in situ so that excess charge transfer structure is avoided. Charge injection into the underlying semiconductor is used to clear the sensing region of accumulated signal charge and, in some cases, to provide a readout means.

1.1 BASIC OPERATION

The charge injection approach to solid state image sensing employs MOS capacitor structures to collect and store photon-generated charge signals. Charge is injected from the MOS storage (inversion) region into the substrate to clear the storage region and, in some cases, to provide a signal readout means. Charge storage sites can be designed for linear addressing (line imager) or for two-dimensional coincident voltage addressing (area imager).

1.1.1 Linear Structure

The simplest charge injection device is the MOS capacitor. If voltage is applied to an MOS capacitor, the underlying silicon is depleted of majority carriers and photon-generated minority carriers can be collected and stored in a surface inversion region as illustrated in Figure 1. If voltage is subsequently removed from the capacitor, the stored charge will be injected into the substrate where it can either recombine or be removed by a charge collection structure.

The magnitude of the injected charge can be determined by measuring the displacement current that flows in the external circuit. If the displacement current that flows in the substrate (and gate) circuit is integrated over the injection time interval, the waveform shown in Figure 1(d) is obtained. The difference between the levels before and after injection are proportional to the net injected charge.

1.1.2 Depletion Capacitance Loading

The charge signal in a CID is measured at the MOS storage capacitor where it was collected. The semiconductor depletion capacitance consequently is a part of the readout circuit and has a loading effect on the output signal. This effect can be seen for the injection readout of Figure 1 by considering the net change in circuit charge upon injection.

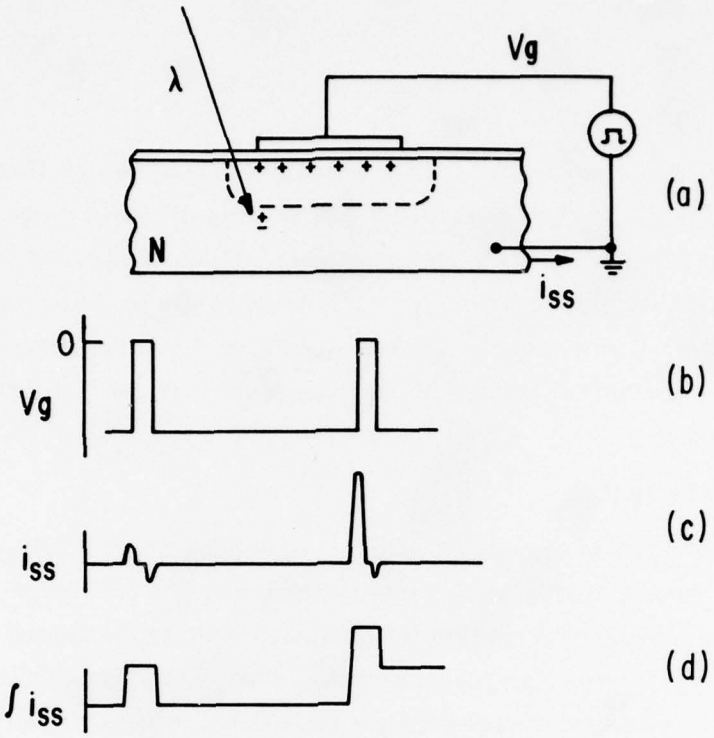

Figure 1. MOS capacitor operated in the Charge Injection mode: (a) device cross section, (b) drive voltage, (c) displacement current, and (d) integrated displacement current, without and with injected charge, respectively.

The diagram of Figure 2 illustrates the silicon surface potential and inversion layer charge before and after injection. Neglecting interface states and fixed oxide charge, the charge stored on the oxide capacitance, q_{ox} must equal the sum of the charge in the semiconductor depletion region, q_d, and in the inversion layer, q_i. The space charge in the depletion region is equal to the product of the depleted volume and the doping density. For a relatively large storage capacitor in which lateral depletion can be neglected, a one-dimensional analysis can be used to calculate the depletion region charge. The depletion width, W, is given by Grove [1] as:

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[1] A.S. Grove, Physics and Technology of Semiconductor Devices, John Wiley and Sons, 1967, p. 159.

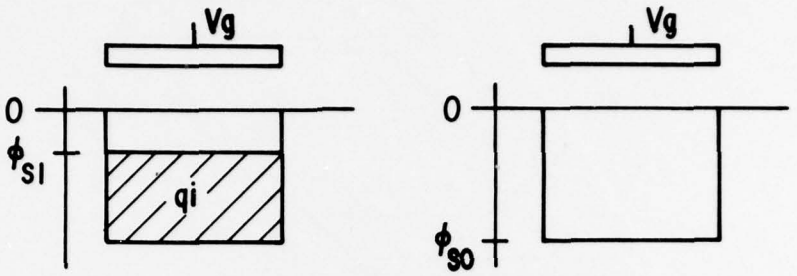

Figure 2. Semiconductor surface potential and stored charge (a) before and (b) after injection.

$$W = (2\epsilon_s \phi_s / qN_B)^{1/2} \tag{1}$$

where ϵ_s = Semiconductor dielectric constant

ϕ_s = Semiconductor surface potential

q = Electronic charge

N_B = Minority Carrier Concentration

Depletion region charge:

$$q_d = WN_B q = (2\epsilon_s \phi_s q N_B)^{1/2} \tag{2}$$

Oxide charge:

$$q_{ox} = (V_g - V_{fb} - \phi_s)C_o \tag{3}$$

where V_g = applied voltage

V_{fb} = Flat Band voltage

C_o = oxide capacitance

$$q_{ox} = q_d + q_i \tag{4}$$

The net charge that flows in the external circuit upon injection is equal to the change in surface potential multiplied by the oxide capacitance. For lightly doped silicon (5×10^{14} cm^{-3}), the charge read out is approximately 94 percent of the collected charge.

More typically, lateral depletion is not negligible. Figure 3 illustrates the volume of the space charge region under an electrode of dimensions X by Y. The loading imposed

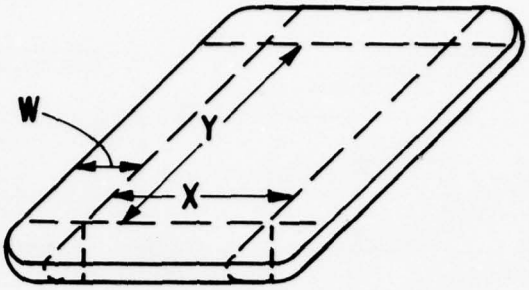

Figure 3. Depleted semiconductor volume including lateral depletion.

by the depletion capacitance is a function of electrode size. The charge readout from a storage capacitor as small as $130\,\mu^2$ is greater than 80 percent of the charge collected with this structure.

1.1.3 Interface States

When an MOS capacitor is biased above its threshold voltage, imperfections at the semiconductor-insulator interface act as traps for inversion layer charge. Trapped charge is immobile and cannot be transferred as required for a charge transfer device. If the surface region is subsequently depleted of mobile charge, the trapped charge is released after a time interval that is related to the activation energy of the specific traps present [2]. This phenomenon is responsible for one component of charge transfer loss in surface channel devices. If the storage capacitor is driven into accumulation, the surface states apparently act as recombination centers. Any charge that is trapped at the time that the region is driven into accumulation recombines and is lost. This action has been termed charge pumping by Brugler et al. [3].

The single MOS capacitor operated in the CID sensor mode does not require charge transfer for proper operation and can function with very high interface state densities. The CID sensing site that is used for two-dimensional area image sensing does require at least one charge transfer for proper operation and is somewhat sensitive to interface states.

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[2] P.G. Jespers, F. vandeWiele, and M.F. White, "Solid-State Imaging," NATO - Advanced Study Institutes Series E, No. 16, Noordhoff, pp. 295-304.
[3] J.S. Brugler and P.G.A. Jespers, "Charge Pumping in MOS Devices," IEEE Transactions on Electron Devices, ED-16, No. 3, March 1969.

1.1.4 X-4 Addressable Sensing Site

If two MOS capacitors are used at each sensing site and are coupled together so that stored charge can be transferred from one capacitor to the other, then a two-axis selection method can be used for scanning. The basic approach is to design each capacitor such that it can store the signal charge when voltage is removed from the other capacitor electrode. Injection will then occur only when both electrode voltages are switched off.

Various methods can be used to couple surface charge between adjacent electrodes. Among these are fringing fields, which require a very narrow inter-electrode gap, overlapping but insulated electrodes, or the use of an interconnecting conductive region. The last method is compatible with standard MOS processes and metal patterning capability and has been used for most of the CID imagers fabricated to date.

A very simple topological structure results with this image sensing technique. The MOS capacitors at each sensing site are coupled with a diffusion. There is no contact made to this diffusion. Array interconnections are readily made using the two-conductor level capability of self-registered MOS processes such as Silicon Gate.

Figure 4(a) shows the cross section of a sensing site with voltages applied to both electrodes. If voltage is removed from either of the electrodes [Figure 4(b)], charge stored under that electrode will transfer to the other capacitor through the coupling region. Charge is injected only from the sensing site that has both electrode voltages switched off simultaneously [Figure 4(c)]. This arrangement permits coincident, two-dimensional (X-Y) scanning, in any order. Sequential scanning can be implemented by including MOS shift registers along two edges of the array. Non-sequential ("random") scanning can be mechanized with digital decoders for row and column selection.

If array drive voltages are switched below the threshold voltage during half-select operation, charge pumping will cause a signal charge loss. A bias voltage, slightly greater than the threshold voltage, can be added to the drive levels to avoid this loss. A bias charge, similar to the CCD fat zero, will then accumulate at each site.

1.1.5 Charge Injection

Charge is removed from CID image sensors by injecting the minority carriers, which have been stored in surface inversion regions, into the underlying semiconductor. The

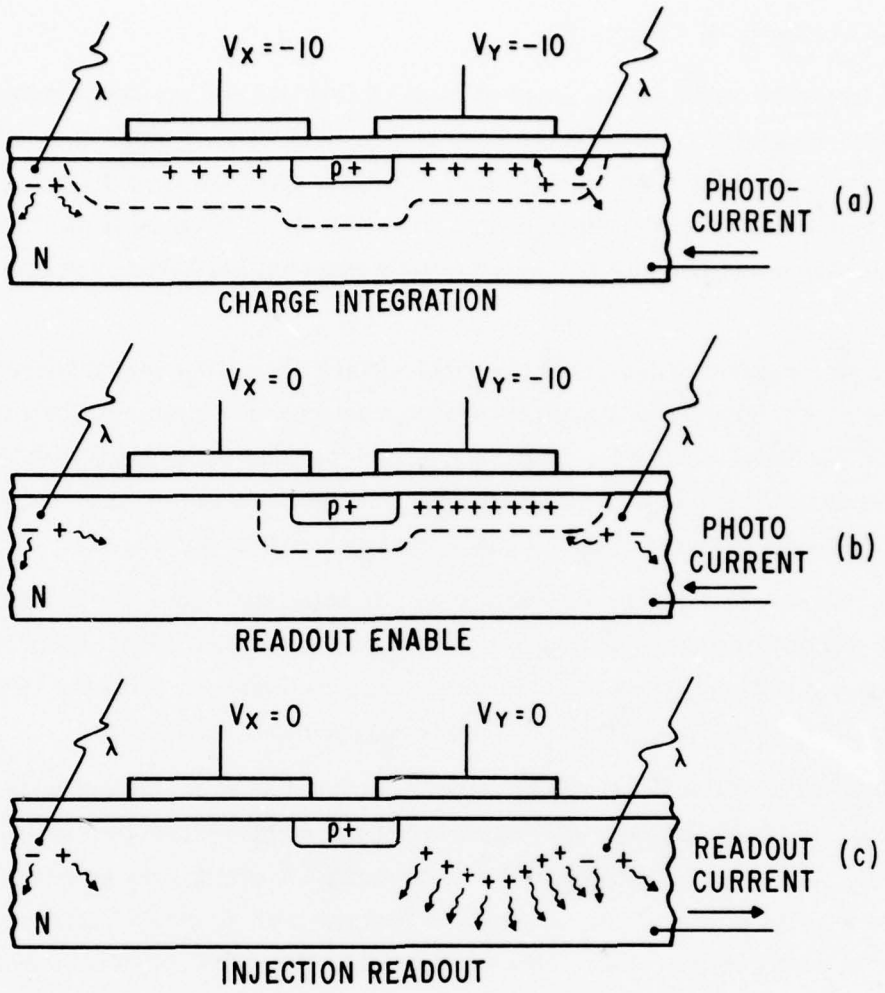

Figure 4. Cross section of X-Y addressable sensing site showing location of stored charge under (a) integration, (b) readout enable, and (c) injection conditions.

first devices [4] were constructed on bulk silicon and relied on recombination as the primary method of charge removal. In this approach there are tradeoffs among site density, dark current, and crosstalk. The diffusion length for minority carriers is proportional to the square root of carrier lifetime, while the thermal charge generation rate in depleted bulk silicon is inversely proportional to lifetime [5]. If the spacing between

[4] G.J. Michon and H.K. Burke, "Charge Injection Imaging," ISSCC Digest of Technical Papers, February, 1973, pp. 138-139.
[5] Grove, op. cit. p. 124, p. 174.

sensing sites is much less than the diffusion length, a portion of the charge injected at one site will be collected by adjacent sites with a resulting loss of resolution. In addition, the injection pulse width cannot be much shorter than carrier lifetime or else part of the injected charge will be re-collected and result in image lag.

The solution to these problems has been to fabricate CID imagers on epitaxial wafers [6]. The epitaxial junction, which underlies the imaging array, acts as a buried collector for the injected charge. If the thickness of the epitaxial layer is less than, or comparable to, the spacing between sensing sites, the injected charge will be collected by the reverse-biased epi-junction, and injection cross talk is avoided. The rate at which charge injected at the surface is removed from the epitaxial layer can be determined analytically. The results of an approximate analysis are shown in Figure 5. Diffusion of a quantity of charge, from the surface to the epitaxial depletion region boundary, has been calculated assuming low level injection and infinite carrier lifetime. Figure 5(a) shows the charge distribution in the epitaxial layer at various times after injection. Measured injection efficiency (percent of stored charge injected) as a function of injection pulse width is shown in Figure 6 for bulk and epitaxial imagers.

The epitaxial collector also affects imager sensitivity. Part of the charge generated in the silicon between sensing sites will be collected by the epi-junction instead of by the storage capacitors. This is particularly important for long wave-length radiation which generates charge farther from the imager surface.

1.2 READOUT METHODS

The signal charge stored in CID imaging arrays can be sensed by measuring either the charge that flows upon injection or the voltage change induced by charge transfer between the two storage capacitors that comprise the X-Y addressable storage site. If charge is injected for readout, then the readout process is destructive because the injection operation clears the sensing sites of signal charge. This readout method will be called Injection Readout. Sequential Injection and Pre-injection are examples of this technique.

Readout can also be implemented by measuring the voltage induced by charge transfer between the two storage capacitors that are used at each sensing site in an array [7]. In an X-Y addressable array the transfer can be performed on all sensing sites along

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[6] G.J. Michon and H.K. Burke, "Operational Characteristics of CID Imager," ISSCC Digest of Technical Papers, February 1974, pp. 26-27.

[7] G.J. Michon, H.K. Burke and D.M. Brown, "Recent Developments in CID Imaging," Proceedings of Symposium on Charge-Coupled Device Technology for Scientific Imaging Applications (JPL), March 6-7, 1975, pp. 106-115.

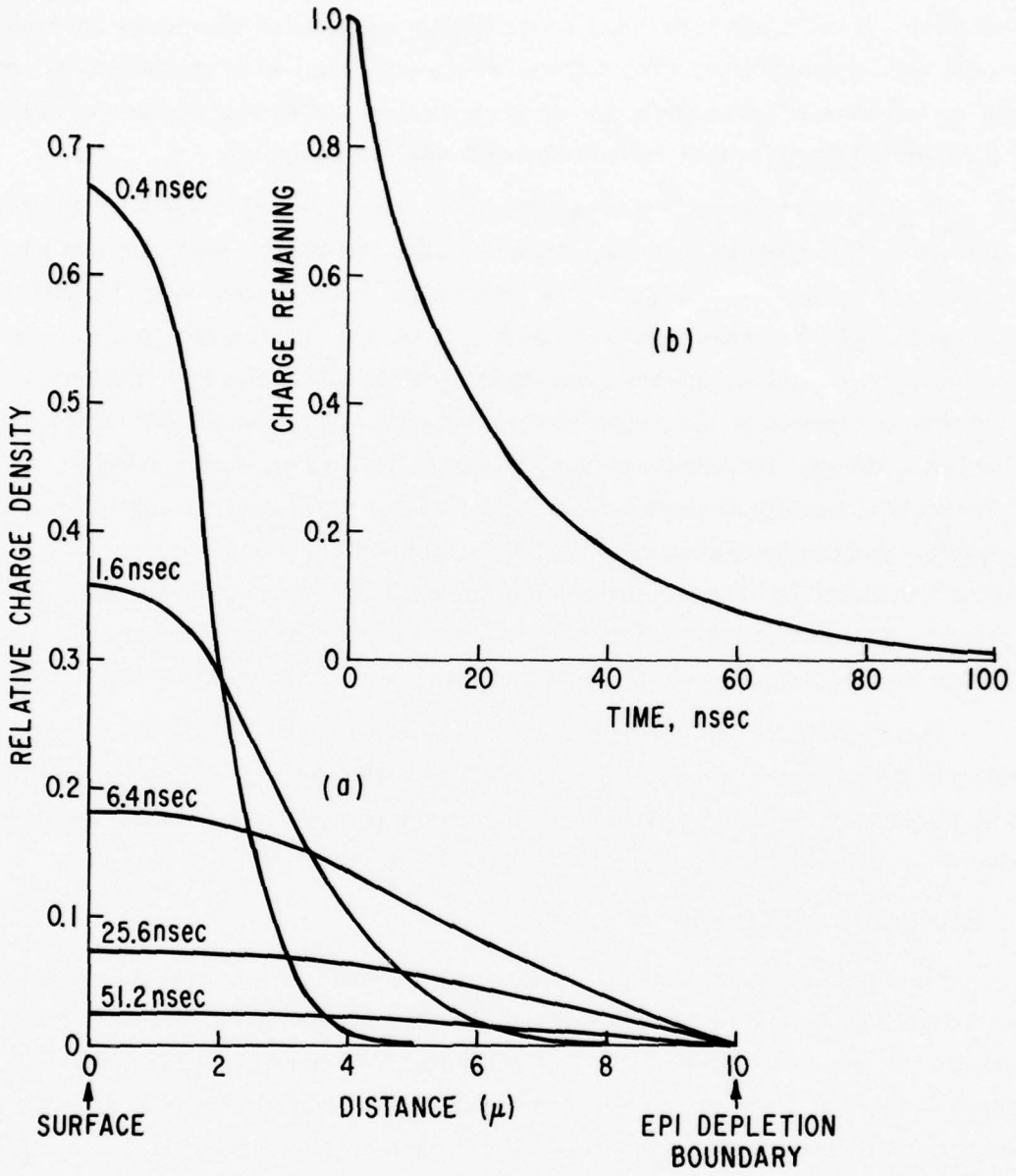


Figure 5. Plot of the calculated charge-collection characteristics of an epitaxial junction: (a) shows the distribution of the injected charge in the epitaxial layer at various times after injection, while (b) shows the relative amount of charge remaining as a function of time.

a row in parallel. Each row can also be cleared of signal charge by performing the injection operation in parallel at all sites in the addressed row. This readout technique will be called Transfer Readout. It is non-destructive because the readout function has been separated

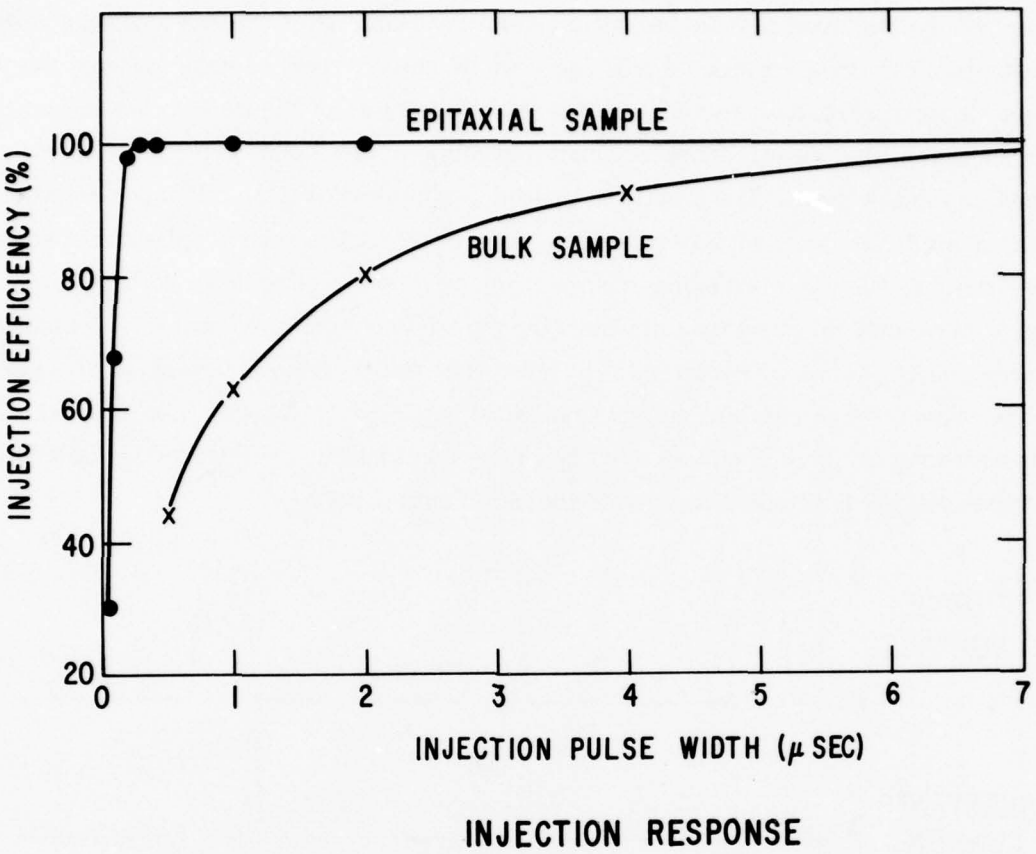


Figure 6. Measured injection efficiency (percent of stored charge injected) of bulk and epitaxial imaging devices.

from the injection operation. Image charge can be read out and retained or injected dependent upon the array drive voltage conditions. Parallel Injection and Row Readout are examples of this second technique.

1.2.1 Sequential Injection

The initial charge injection imagers utilized the substrate as a readout port common to all array sensing sites. With this approach, scanning can be implemented by first removing voltage from an array row (X-line) and then pulsing each column (Y-line) in sequence to read out the selected row. All rows can be read out in this manner, with or without interlace, dependent upon the order of row selection.

Video signal waveforms obtained using substrate readout are illustrated in Figure 7. The raw video signal consists of the substrate charge injected from each sensing site in sequence. This signal appears as a displacement current in the presence of drive line

interference that results from parasitic capacitive coupling of the drive voltage to the substrate. The drive voltage interference can be made to cancel itself through the use of an integrating readout technique. The first pulse time of Figure 7 shows the substrate current signal that results from capacitive coupling of the Y-line drive pulse in the absence of signal charge. The substrate current is simply $C(dV_Y/dt)$. If this current signal is integrated, the drive voltage waveform is recovered. The second pulse time shows the substrate current when signal charge is injected upon Y-line drive voltage turn-off. The positive current pulse contains both the parasitic capacitance charge and the signal charge. The negative substrate current pulse that results from the re-application of Y-line drive voltage contains only the parasitic capacitance charge. The integral of this current waveform results in a net signal proportional to the injected signal charge. This net voltage is sampled to provide the video output voltage.

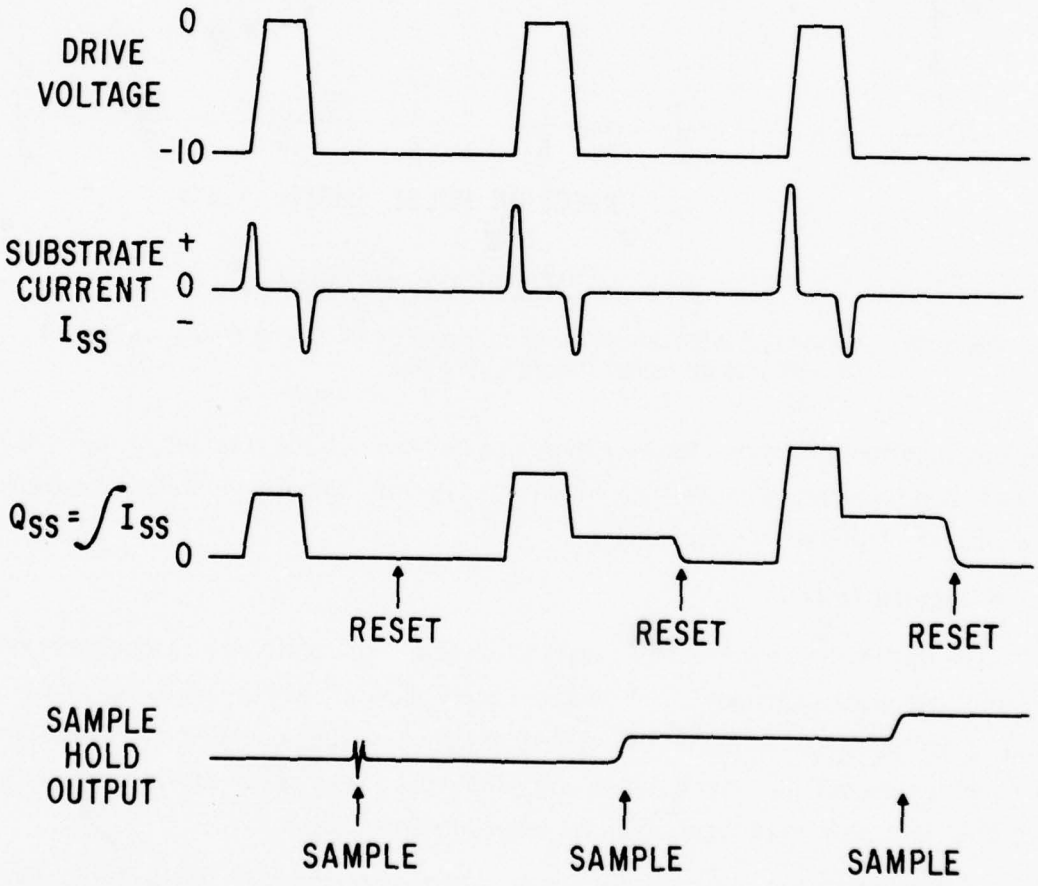


Figure 7. Video signal waveforms for substrate readout illustrating column drive voltage, substrate current, net injected charge, and sampled video for different levels of injected charge.

This signal recovery system results in self-cancellation of the parasitic drive line interference. For complete cancellation it is only necessary that the drive voltage return to its initial state - variations in the magnitude of the drive voltage or individual variations in line capacitance do not affect cancellation.

The signal voltage developed at the output of the image sensor is equal to the net injected charge divided by the total load capacitance. Capacitive loading imposed by the array lines can be minimized by allowing all but the selected row and column conductors to float during each line scan interval. If scanning circuitry is integrated into the imaging array, then capacitance between the scanning shift registers and substrate will represent the bulk of the load capacitance. Images obtained from early 32 line by 32 element self-scanned imagers using substrate readout are shown in Figure 8.

Figure 8. Images obtained from 32x32 self-scanned imagers employing substrate readout.

The displacement current that flows in the substrate upon charge injection also flows in the driven array line. The capacitive load of on-chip scanning circuitry can be avoided by sensing current in the driven line instead of the substrate.

An array designed for drive line readout which includes integral shift registers is diagrammed in Figure 9(a). A larger voltage is applied to the row electrodes than to the column electrodes so that photon-generated charge collected at each site is stored under the row electrode thereby minimizing the capacitance of the column lines. The sensing site cross sections of Figure 9(b) illustrate the silicon surface potentials and locations of stored charge under various applied voltage conditions.

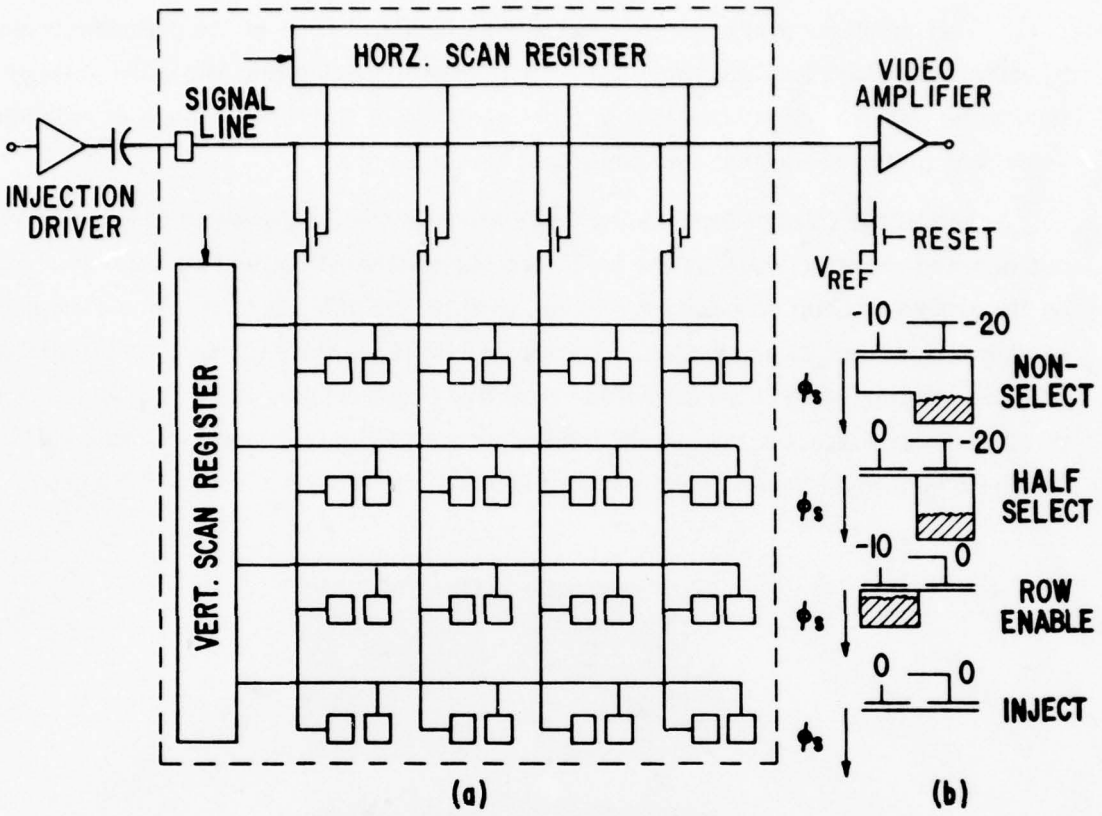


Figure 9. Diagram illustrating basic X-Y accessing scheme for a CID imager: (a) is a schematic diagram of a 4x4 array, while (b) shows the sensing site cross-section showing silicon surface potentials and location of stored charge for various operating conditions.

A line is selected for readout by setting its voltage to zero by means of the vertical scan register. Signal charge at all sites of that line is transferred to the column capacitors, corresponding to the Row Enable condition shown in Figure 9(b). The charge is then injected by driving each column voltage to zero, in sequence, by means of the horizontal scan register and the signal line. The net injected charge is measured by integrating the displacement current in the signal line, over the injection interval. Charge in the unselected lines remains under the row-connected electrodes during the injection pulse time (column voltage pulse). This corresponds to the half-select condition of Figure 9(b).

One method for measuring the net injected charge is shown in Figure 10. After column selection the signal line is reset and allowed to float. A sample of the signal after reset is taken to eliminate KTC noise by pulsing the "restore" switch. The signal line is then driven by the capacitively coupled drive pulse to inject the signal charge

at the selected imager site. After the drive voltage returns to its initial value, the net change in voltage on the signal line is proportional to the injected charge. This voltage is sampled to form the video signal.

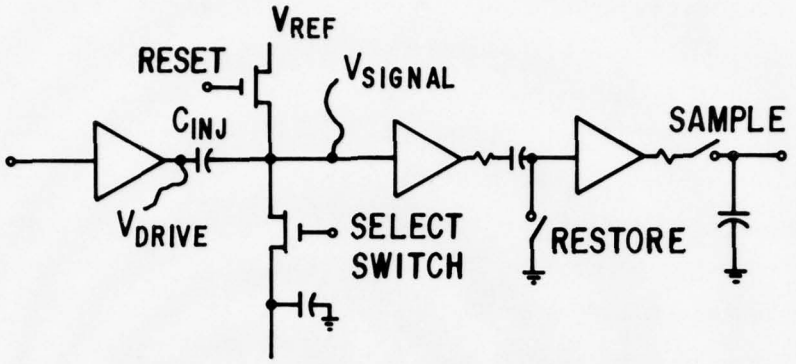


Figure 10. Sequential Injection imager readout.

The image obtained with a 100 line by 100 element array employing drive line sensing is shown in Figure 11.

Figure 11. Image obtained from a 100x100 self-scanned imager constructed on an epitaxial substrate and employing drive line sensing.

1.2.2 Pre-Injection

The pre-injection readout technique is based upon the measurement of the change in charge that occurs at each addressed sensing site when a complete row of sites is cleared (injected) simultaneously. The schematic diagram of an array configured for pre-injection readout is shown in Figure 12. Equal row and column bias levels are normally used with this readout method with the result that about half of the signal charge is stored under the row-connected electrode and half under the column-connected electrode at each array site.

Charge is read out by first setting all column electrodes to a reference potential and then allowing them to float. During the horizontal retrace interval, voltage is momentarily removed from the selected row to clear that row of sites to a bias charge level. Row voltage is reapplied before line scanning commences. This injection operation is illustrated in Figure 12 for row X_3. Since half of the signal charge in the addressed row was stored under the column-connected electrode when the column potentials were reset, the removal of signal charge by the injection operation results in a voltage being induced on the floating column lines that is proportional to the injected signal charge. The induced voltage signals are then read out by operating the column scanner. The video signal consists of the current required to reset the column lines to their reference level during the column scan (line scan) operation.

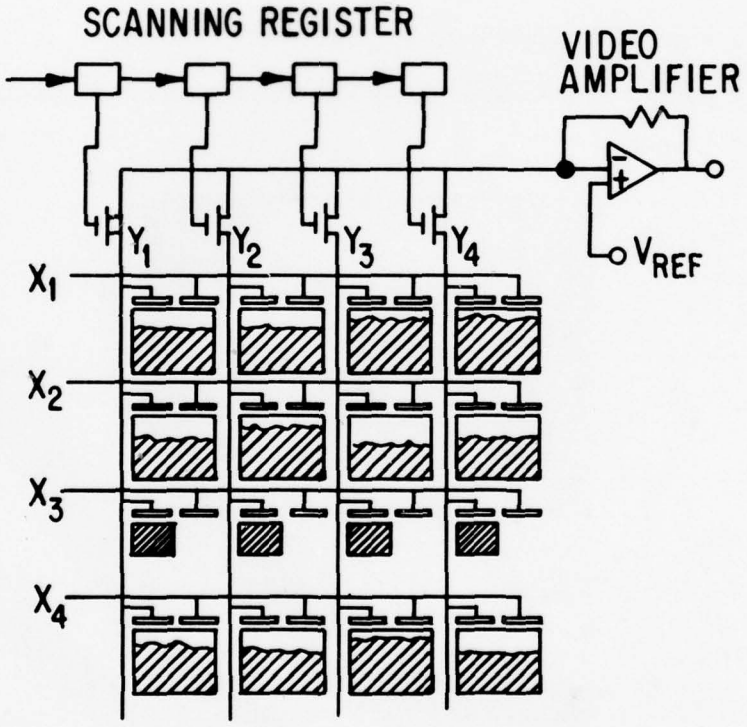


Figure 12. Schematic diagram of a 4x4 CID array designed for pre-injection readout. Silicon surface potentials and signal charge locations are indicated schematically.

This pre-injection readout method has a number of advantages and some limitations. Array fixed pattern noise is automatically rejected since the only net change in array charge levels prior to each video line scan is the injection of signal charge. The technique is compatible with high-speed sampling of the induced column signals as required

for TV compatible operation. The main disadvantage with this readout technique is the switching noise coupled into the video signal by the column scanner. This component of fixed pattern noise repeats for each video line and can be rejected if one line of video storage is provided. This pattern noise cancellation technique also rejects any crosstalk resulting from the sharing of signal charge between row- and column-connected storage electrodes.

1.2.3 Parallel Injection

The Parallel Injection technique allows the functions of charge injection and charge detection to be separated. Signal charge levels can be sensed at high speed during a line scan, and during the line retrace time interval all of the charge in the selected line can be injected in parallel. Since the charge need not be injected, the readout can be non-destructive. The parallel injection technique is well adapted to TV scan formats in that the signal is read out line by line. It is not compatible with random scan.

In an array of MOS coupled-capacitor pairs, as is used in the present charge injection imagers, all of the signal charge will be stored under the row-connected electrodes if the row voltages are larger than the column voltages. This condition is illustrated in Figure 13 for rows X_1, X_2, and X_4. This method of biasing effectively prevents the charge stored under the row-connected electrodes from affecting column voltages. The voltage on all array columns, Y_1 through Y_4 in Figure 13, can be set to a reference value either by means of a previous column scan readout, or through the use of the column switches, S_1 through S_4.

If the voltage on a row electrode is then switched to zero, signal charge will transfer from the row-connected electrodes to the column-connected electrodes in the selected row of sensing sites. This is diagrammed in Figure 13 for row X_3. The voltage on a given column line will then be reduced by an amount equal to the signal charge of the addressed site divided by the column capacitance.

The signal can be sensed by sequentially connecting each column line to a video amplifier by the use of a scanning register and MOS switches. The readout operation consists of resetting the video amplifier input to the reference voltage, and then stepping the scanning register to the next column line. After all columns of the array have been scanned, charge can be returned to the row-connected electrodes by reapplying voltage to the previously selected row. This action retains the signal charge for future processing.

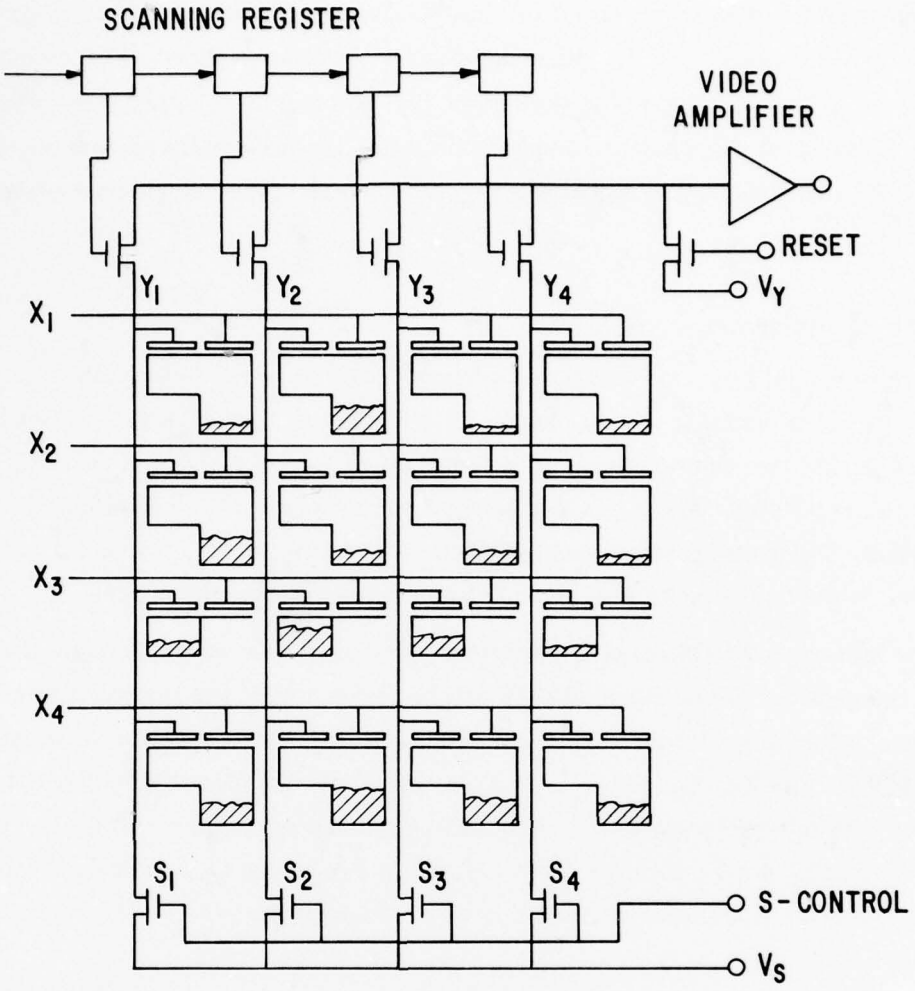


Figure 13. Schematic diagram of a 4x4 CID array designed for parallel-injection readout. Silicon surface potentials and signal charge locations are indicated schematically.

Alternately, at the end of readout of the selected row, while the row voltage is maintained at zero volts, the signal charge can be injected from the selected row to the substrate, all sites in parallel, by switching all column voltages to zero simultaneously. This action clears the sensing sites of charge and allows the start of a new signal integration time interval for that row.

Two experiments were performed to identify the precision to which the readout is nondestructive. First, the charge pattern of an image was generated and stored by momentarily opening a shutter, and then the image was read out continuously at 30 frames per second, until image degradation was noted. At a chip temperature of 200 ^{o}K, images were read out for three hours (324,000 NDRO operations) with no detectable charge

loss. The charge lost during each NDRO operation was, on the average, much less than one carrier per pixel per frame.

The second experiment was performed to test whether charge could be generated and stored at very low light levels under continuous (30 frames per second) NDRO conditions. A series of time exposures was made at successively lower light levels and the time required to reach a given level of signal voltage was measured. The results, Figure 14, show that the exposure time is inversely proportional to light level with no measured charge loss for exposure times up to three hours. The lowest light level used was equivalent to about two carriers per pixel per frame in the highlight regions of the image. Here again the readout loss was not detected and was much less than one carrier per pixel per frame.

Subsequent to the measurements described above, an image was stored on a 128x128 array for 65 hours while being continuously read out non-destructively at 30 frames per second. The initial and final images are shown in Figure 15.

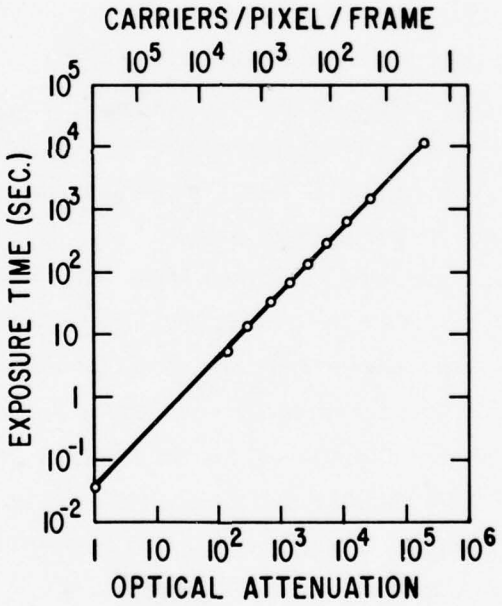


Figure 14. Plot showing exposure time required to accumulate a given quantity of signal charge as a function of incident light level. Time is plotted as a function of optical attenuation. Measurements were made on a 244x248 array, cooled to 200 ^{o}K and operated at 30 frames per second, NDRO.

INITIAL IMAGE

AFTER 7 X 10^6
NDRO (65 hr)

Figure 15. NDRO image readout.

1.2.4 Row Readout

Row Readout is a second charge transfer readout method. If a larger voltage is applied to the column electrodes than is applied to the row electrodes, signal charge will be stored under the column-connected electrode at each sensing site. This case is illustrated for three of the four columns shown in Figure 16. A row is selected for readout by the vertical scanning register which connects the addressed row to the video amplifier. The horizontal scanning register is then operated to connect sequentially each array column to the column drive input. During readout of each site in the addressed row, the row voltage is reset to a reference voltage, allowed to float, and a sample of the floating row voltage is taken for KTC noise suppression. The addressed array column is then driven to cause signal charge to transfer from column to row electrodes at all sites connected to the driven column. The quantity of charge transferred to the addressed row is sensed by taking a second sample of the floating row voltage. The difference between the first and second samples is the video signal without KTC noise. This process is repeated for each site in the addressed row during each line scan. At the end of each line scan, the addressed row can be cleared of charge by removing voltage from that row and all column lines to inject charge from all sites of that row simultaneously. This row injection operation is omitted during nondestructive readout of the array.

It is also possible to operate the array in an inverse manner, storing charge under the row-connected electrodes and transferring charge from row to column electrodes for readout. One desirable feature of this inverse mode of operation is that, at the end of each line scan, the column lines do not have to be driven to cause injection from the selected row since they are biased at the injection level. Only the addressed row needs to be driven to clear it of signal charge.

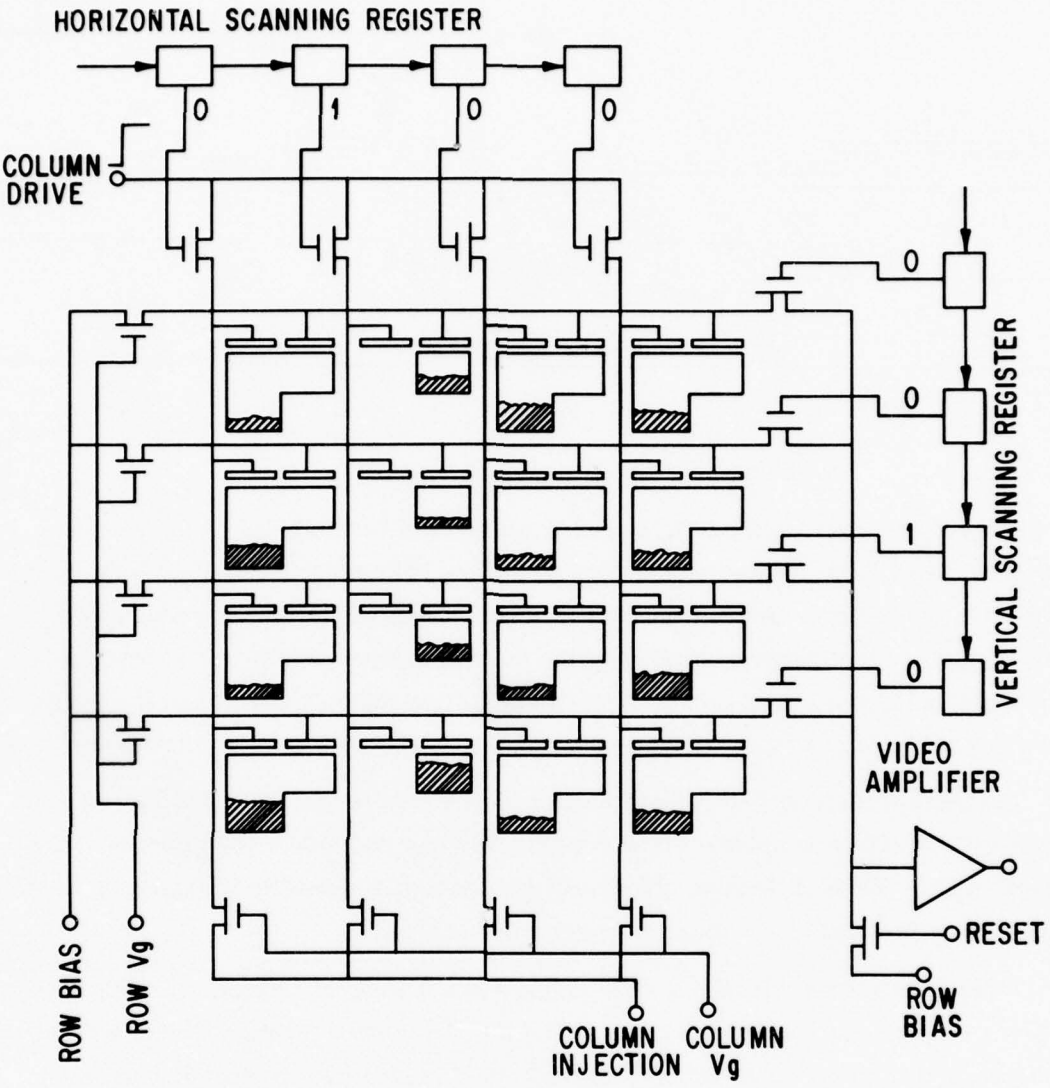


Figure 16. Row Readout array diagram illustrating sensing of the third row, second column.

The advantages of this readout method over previously described techniques are that the horizontal scanner is isolated from the video signal, KTC noise can be easily rejected, and non-destructive readout can be readily mechanized.

1.3 PERFORMANCE CHARACTERISTICS

Localized charge transfer and injection result in sensitivity, crosstalk, and blooming characteristics that are different from other solid state image sensing techniques.

1.3.1 Sensitivity

A cross section sketch of the CID image sensing structure is shown in Figure 17. Since signal charge is detected at the sensing site and removed by diffusion across the

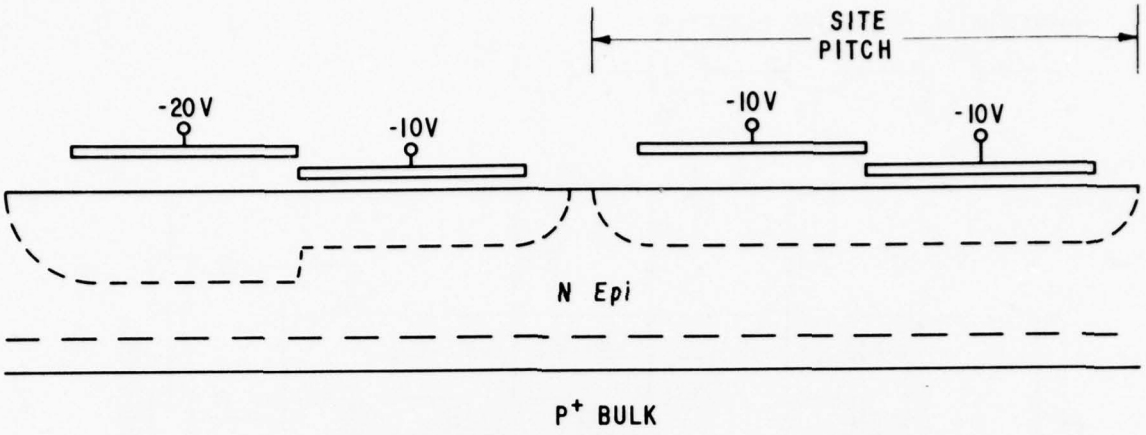


Figure 17. Sensing site cross section.

epitaxial layer and collection by the epitaxial junction, essentially all of the semiconductor area is available for photon charge generation. The response of the semiconductor is, of course, modified by the transmission characteristics of the surface conducting and insulating films. Charge generated in the neutral semiconductor is transported by diffusion and collected either at a sensing site or lost to the epitaxial collector. Sensing site spacing and epitaxial layer thickness consequently affect charge collection efficiency.

The absorption length of radiant energy into silicon ranges from 0.2 micron at a wavelength of 400 nanometers to 5 microns at 700 nanometers to 100 microns at 1000 nanometers [8]. Good collection efficiency has been obtained with the epitaxial layer thickness roughly equal to the space between sensing sites.

Three conductor materials have been used in CID imager fabrication. The silicon gate process employs a lower level of polysilicon and an upper level aluminum conductor. Imagers have also been fabricated with two levels of polysilicon. A recent innovation [9] has been the incorporation of transparent metal oxide conductors into an overlapping electrode structure with polysilicon as the lower level conductor. The spectral transmission characteristics of these films (on quartz) is shown in Figure 18. The range of collection efficiencies that can be achieved using these techniques is shown in Figure 19 for the sensing site layouts of Figure 20. The 30 micron square (1.2 milx1.2 mil) sensing site employs a double level polysilicon electrode structure on an epitaxial layer. The spacing between thin oxide regions is approximately equal to the undepleted epitaxial layer thickness.

[8] S.M. Sze, Physics of Semiconductor Devices, Wiley-Interscience, 1969, p. 661.

[9] D.M. Brown, M. Ghezzo and P.L. Sargent, "High Density CID Imagers," IEEE Transactions on Electron Device, ED-25, No. 2, February 1978.

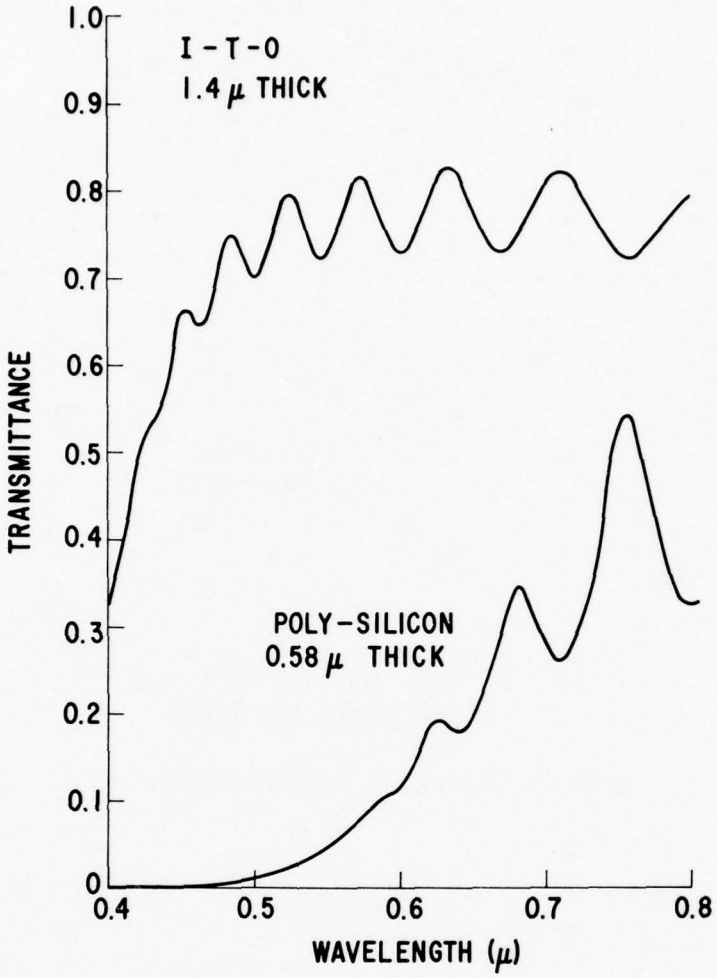


Figure 18. Metal oxide and polysilicon film spectral transmittance.

The 35 micron by 42 micron (1.4x1.7 mil) site uses polysilicon for the lower conductor and metal oxide for the upper conductor. The spacing between thin oxide regions can be large on this array without loss in collection efficiency because it has been fabricated on bulk silicon.

1.3.2 Point Spread Function, Crosstalk, and Lag

The array cells are designed to allow charge transfer between the two storage capacitors at each sensing site but not between adjacent sites. Two mechanisms exist, however, which can result in signal crosstalk between adjacent sites. Charge generated in the undepleted silicon between sensing sites will divide between the sites as long as the distance to be traveled is less than the minority carrier diffusion length. This effect

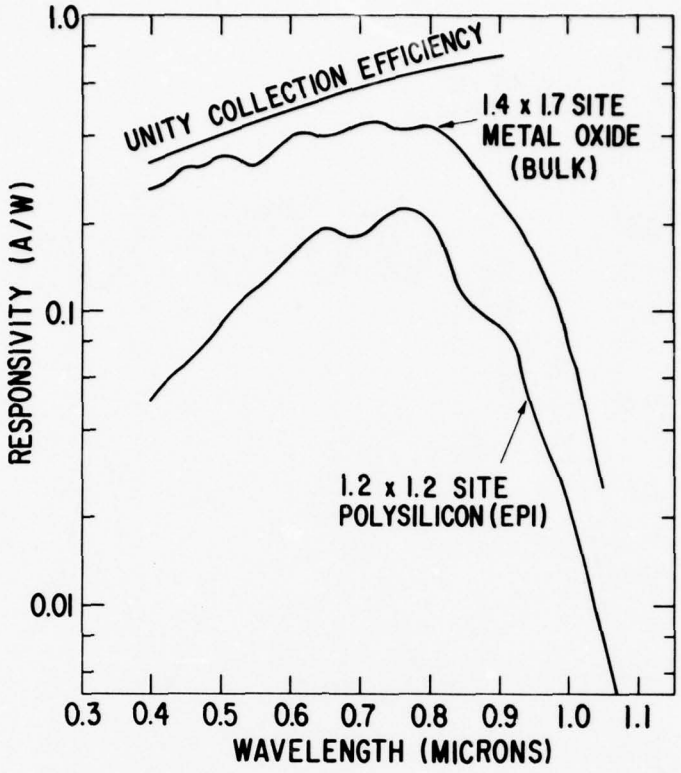


Figure 19. Sensing site collection efficiency.

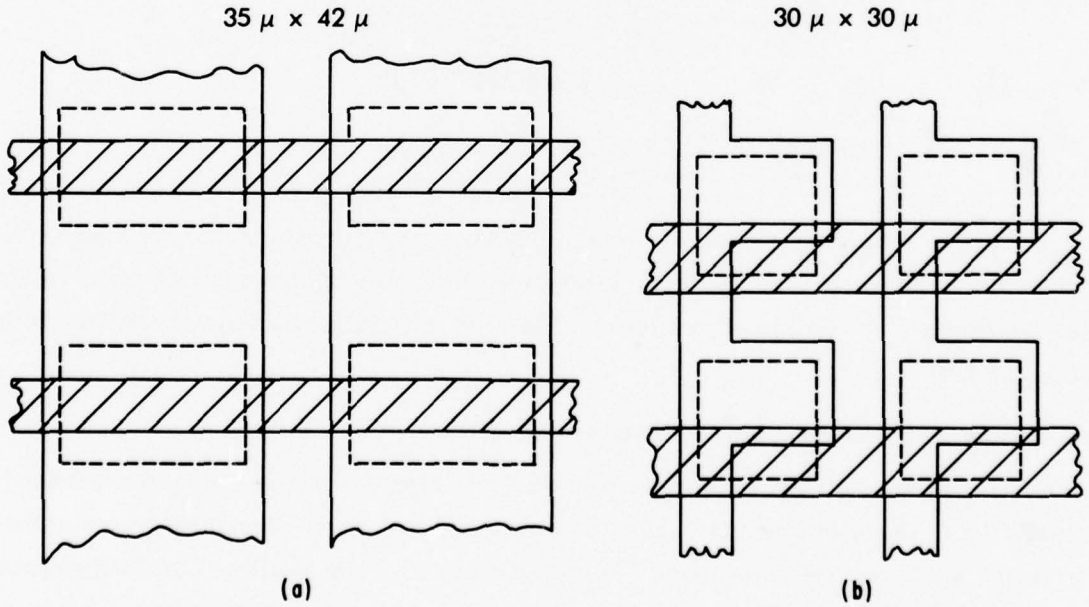


Figure 20. Sensing site layouts: (a) lower polysilicon row conductors, upper metal oxide conductors, and (b) double level polysilicon conductors.

can be attenuated in epitaxial imagers if the distance between the surface and the buried collector is made less than, or comparable to, the spacing between sites.

The second crosstalk mechanism is the migration of injected charge to neighboring sites. Proper placement of the epi-collecting junction also reduces this effect.

Horizontal and vertical point spread functions for the 30 micron square sensing site of Figure 20 is shown in Figure 21. These measurements were made using a 0.1 mil diameter spot from a tungsten arc lamp.

Lag can occur in CID imagers through two mechanisms: 1) recapture of the injected charge by the injecting site upon reapplication of the storage electrode voltage; and 2) migration of injected charge to adjacent sites that are not to be read out until the following field. Image lag resulting from the second mechanism occurs to the same degree as crosstalk (loss of MTF). Recapture of charge by the injecting site is a function of the time allowed for injection (see Figure 6). This can vary from virtually zero recapture to full recapture of the injected charge (NDRO, for example). In practice, the injection pulse width is adjusted to insure that image lag is consistent with system requirements.

1.3.3 Dark Current

The CID approach permits significantly more silicon area to be used for photon charge generation than for charge storage. This results in an advantageous dark current situation because the thermal charge generation rate in nondepleted bulk silicon is orders of magnitude less than in the depleted storage region [10]. Consequently, each image sensing site collects and stores photon-generated charge from essentially the total site area as long as the site spacing is less than the minority carrier diffusion length but generates dark current only in the storage area. Also, no separate storage area is required for image readout, so that a dark current contribution from this source is avoided.

The use of bias charge in the storage area tends to minimize dark current since the surface thermal generation rate in MOS structures is much smaller under inversion conditions than under depletion conditions [11]. Measured thermal charge generation rates for a 100x100 imager are shown in Figure 22. Minimum dark current results from biasing the array such that charge is stored under both electrodes, as seen in Figure 22(a). Figure 22(b) shows the effect of operating with one storage region depleted. These data were obtained by operating the device in a "burst" mode in which the sensing sites were

[10] Grove, op. cit., pp. 173-180.

[11] D.J. Fitzgerald and A.S. Grove, "Surface Recombination in Semiconductors," Surface Science, Vol. 9, 1968, pp. 347-369.

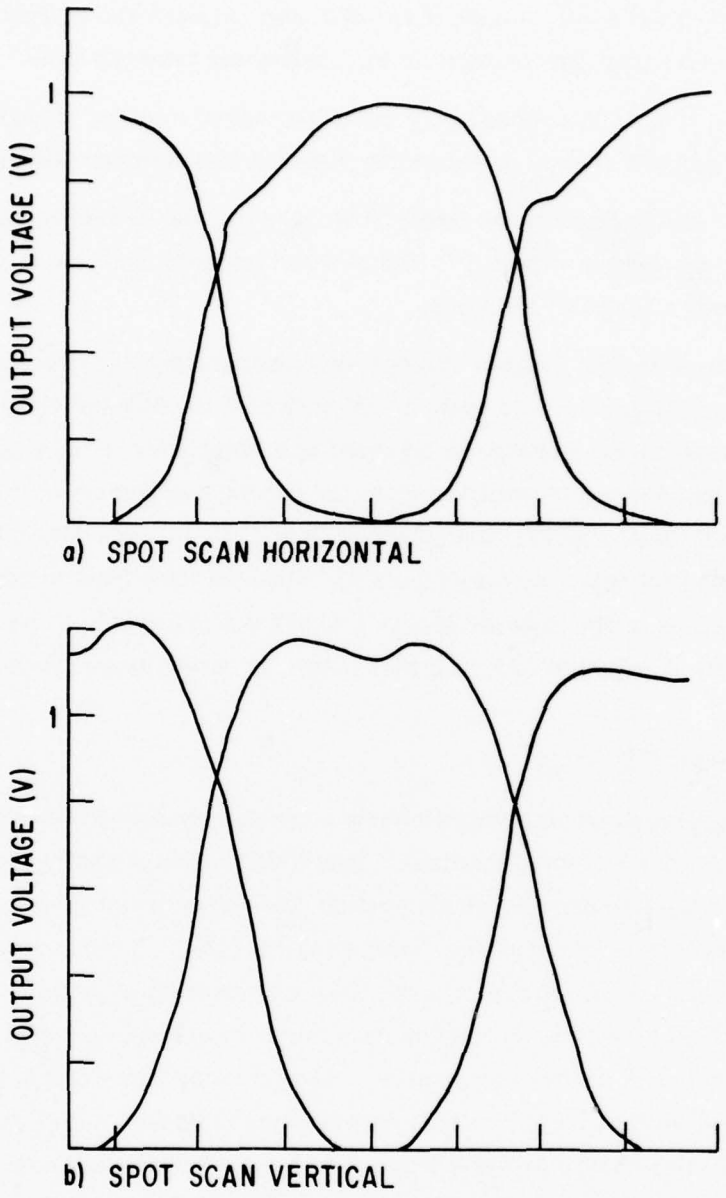


Figure 21. Point spread function data.

allowed to integrate charge for the appropriate time which the entire array was read out in 1/30 sec. The average accumulated charge for the entire array was recorded.

The 100x100 imager is normally operated with one storage region depleted, so that the conditions of Figure 22(b) apply. The peak signal-to-dark current ratio exceeds 100:1 under these conditions at 30 frames/s. For lower frame rates, it is feasible to operate under the conditions of Figure 22(a), thereby doubling the useful integration time.

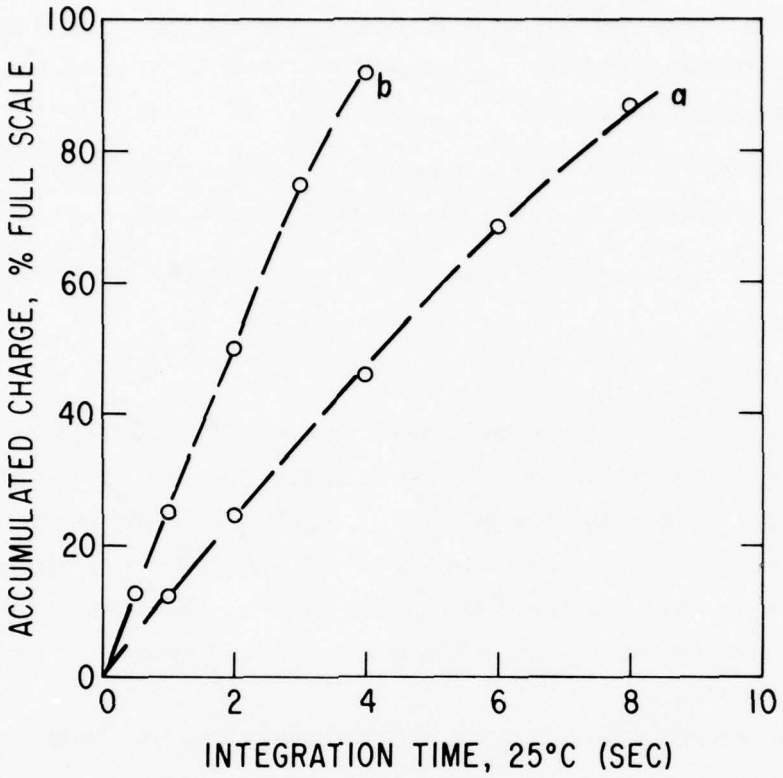


Figure 22. Thermal charge buildup versus time in 100x100 CID imager at 25 °C, for curve (a), both storage regions inverted, and for curve (b), one storage region depleted.

1.3.4 Blooming

The epitaxial CID structure is resistant to image blooming since each sensing site is electrically isolated from its neighbors. Charge spreading in the substrate is minimized by the underlying charge collector.

In Sequential Injection, blooming of the displayed image occurs if charge is injected from a half-selected site during readout of another site on the same column. This excess injected charge is detected as signal and adds to the displayed video. This results in brightening of the affected column upon overload of a single site.

The image displayed in the Parallel Injection approach exhibits relatively little blooming as a result of sensing site overload. This is because the half-select and injection operations occur during the horizontal blanking interval. While excess charge can

accumulate during a line scan interval and cause column brightening for overloads occurring in the right-hand portion of the image field, this effect is attenuated by the line-to-frame integration time ratio.

During NDRO, virtually no blooming occurs since the charge is not injected. The affected sites simply fill to capacity and cease collecting charge.

In all cases, radial spreading of excess charge is prevented by the underlying charge collector.

1.3.5 Noise Sources

The circuitry used to select and provide readout of CID image sensors contains a number of Johnson noise sources. The distributed resistance of the array lines used for signal sensing, the line selection switch, and the first preamplifier stage each contribute temporal noise to the video signal. In addition capacitor reset noise (KTC noise) can be significant when certain readout methods are used. Shot noise in the dark current and/or junction leakage current in the MOS line select multiplexers can be significant under certain conditions.

The Johnson noise sources usually are dominant in large arrays operating at megahertz video rates.

If a switch is used to set the voltage across a capacitor, thermal noise in the resistance of the switch results in an uncertainty in the final capacitor voltage. The magnitude of this uncertainty [12] is

$$V_n = (KT/C)^{1/2} \tag{5}$$

or

$$Q_n = (KTC)^{1/2} \tag{6}$$

where K=Boltzmann's constant = 1.38×10^{-23} W - s/^{o}K and T=temperature in degrees kelvin. Sequential injection CID imagers are not limited by this noise component because it is possible to reference the net injected charge signal to the input capacitor voltage after reset has been completed. This technique, called correlated double sampling [13],

[12] J.E. Carnes and W.F. Kosonocky, "Noise Sources in Charge-Coupled Devices," RCA Revision 33, June 1972, pp. 327-343.

[13] M.H. White, D.R. Lampe, F.C. Blaha, and I.A. Mack, "Characterization of Surface Channel CCD Imaging Arrays at Low Light Levels," IEEE Transactions Journal on Solid-State Circuits, SC-9, 1, 1974.

results in the substitution of KTC noise on a clampling capacitor for KTC noise on the array output capacitance. The level of KTC noise referred to the array can be made arbitrarily small, however, since gain can be used between the array output and the clamp capacitor. The Parallel Injection technique does not allow complete elimination of KTC noise. The column reset transistors introduce KTC noise that is not rejected. Voltage noise at the input of the preamplifier results in an equivalent input charge that is directly proportional to the array output capacitance ($q = cv$). Theoretical preamplifier noise levels of a few hundred carriers result from array output capacitance levels in the 10-pF region. KTC noise can be either negligible or can be the predominant temporal noise source, depending upon the specific array design and readout method.

Under low video rate readout conditions, Johnson noise can be minimized by restricting the noise bandwidth of the video amplifier. Shot noise originating in array dark current and line select multiplexer junction leakage can be limiting under these conditions. Reduction in array operating temperature can be used to control these thermally generated currents and consequently the resultant shot noise.

Solid-state imaging sensors can exhibit a fixed non-uniform spatial background in the reproduced image. The major sources of fixed pattern noise in CID image sensors are transistor switching interference, array photolithographic variations, and bias charge variations. Non-uniform coupling of the MOS transistor scanner output voltage to the video signal results in a component of fixed pattern noise that repeats from scan to scan. Variations in row-to-column crossover capacitance arising from either insulator thickness or photolithographic variations cause a two-dimensional component of fixed pattern noise. Variations in bias charge from site-to-site, caused by differences in storage capacitance or threshold voltage, also result in a two-dimensional component of fixed pattern noise. Differential sensing and signal processing can be used to minimize these effects.

Dark current nonuniformity can be an important source of pattern noise, particularly at room temperature. The inherently low dark current performance of CID imagers can be an advantage under these conditions.

1.4 SPECIAL FEATURES

The organization and non-destructive readout capability of the CID imager gives rise to a number of specialized functions. The X-Y addressable organization allows random access to array pixels [14]. The non-destructive readout feature combined with X-Y access allows linear combinations of pixel signals to be sensed giving rise to spatial transform readout [15]. Finally, signals can be repeatedly read and summed to improve dynamic range [16].

[14] H.K. Burke, G.J. Michon, and T.L. Vogelsong, "Random Access CID Imager," Conference on Laser and Electro-Optical Systems (LEOs), San Diego, CA, February, 6-9, 1978.

[15] G.J. Michon, H.K. Burke, T.L. Vogelsong and P.A. Merola, "Charge Injection Device (CID) Hadamard Focal Plan Processor for Image and Width Compression," Proceedings of the Agard Symposium on Compact of CCD and SAW Devices on Signal Processing and Imagery in Advanced Systems, Ottawa, Canada, October 11-15, 1977.

[16] R.S. Aikens, C.R. Lynds and R.E. Nelson, "Astronomical Applications of Charge Injection Devices," Society of Photo-Optical Instrumentation Engineers, Vol. 781 (1976) Low Light Level Devices, pp. 65-71.

Section 2

TEMPORAL NOISE

CID image sensors consist of an interconnected array of MOS charge collection and storage sites. Integrated MOS selection circuitry is used to access sensing sites. A number of Johnson noise sources, such as array conductors, selection switches and preamplifiers, are active during operation of this device. In addition shot noise from thermally generated charge is present in the array dark current and in multiplexer junction leakage current.

The temporal noise levels and the noise performance of the various readout techniques are identified in this section. In addition, study results on amplifier noise optimization and signal-to-noise ratio improvements through multiple non-destructive readout operations are included.

2.1 JOHNSON NOISE

A portion of a typical CID imager is shown in Figure 23. The charge collection-storage array consists of an X-Y addressable matrix of charge storage capacitors. Two levels of array conductors are used with each level usually used both for interconnections and for capacitor electrodes. MOS switching circuitry is used for site selection and readout. The electrical equivalent circuit of a sensor with a single row and column selected is shown in Figure 24(a). The significant thermal noise sources are shown in the noise equivalent circuit of Figure 24(b).

2.1.1 Distributed Array Conductors

All array interconnect materials have finite (non-zero) resistance and, consequently, generate thermal noise. The magnitude of the array line resistance can be significant for the polysilicon and metal oxide materials used in present-day CID imagers. The distributed nature of the noise-generating resistance and the attenuating effect of the distributed line capacitance and load capacitance require a detailed calculation to define the net output noise level.

The conductance of the line select switch is usually high compared to the total line conductance. If the select switch resistance is neglected, the distributed line R-C network and load capacitance (C_A) can be modeled as shown in Figure 25(a). The load capacitance is the total capacitance of the multiplex signal line, reset switch drain, and amplifier input capacitance.

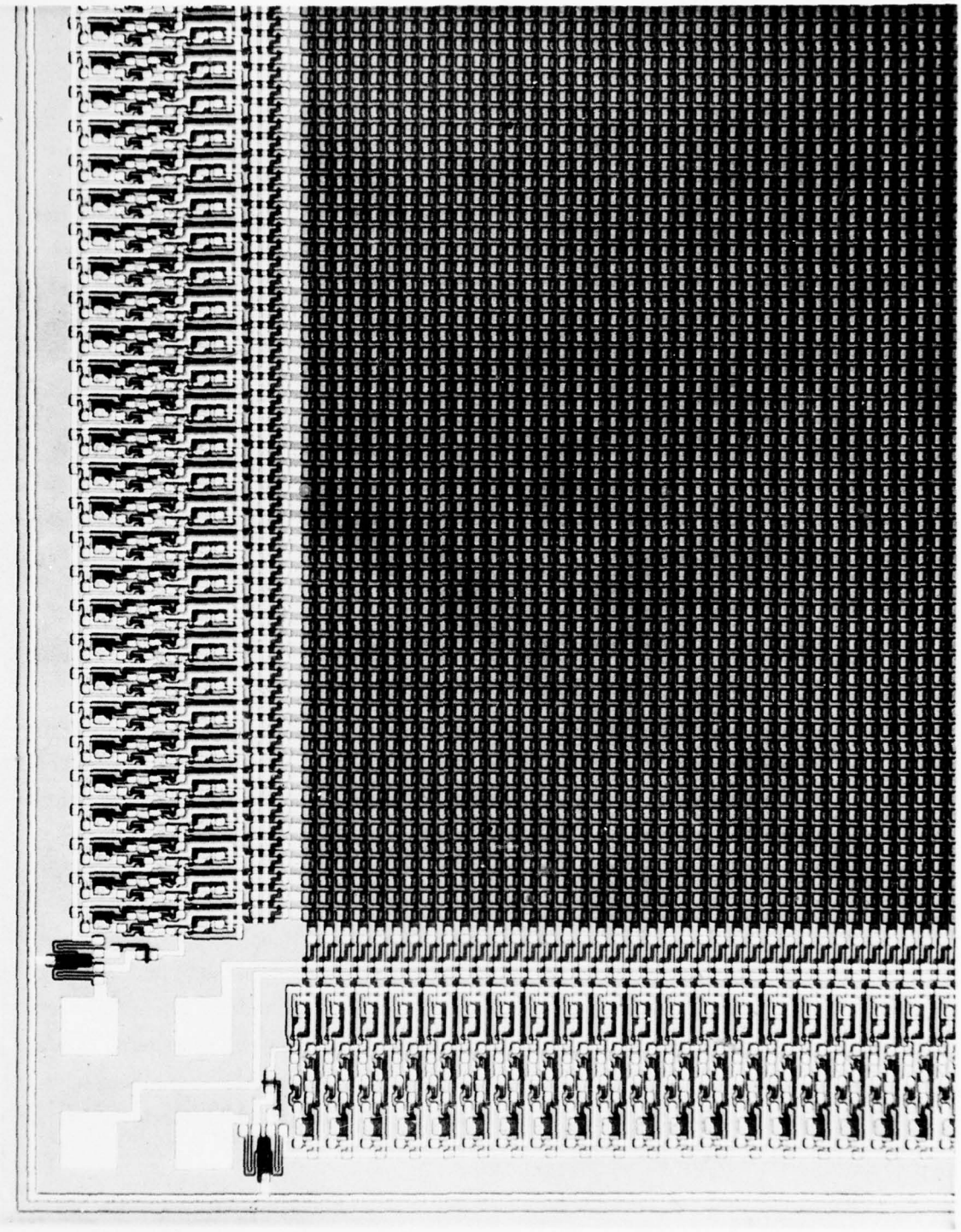
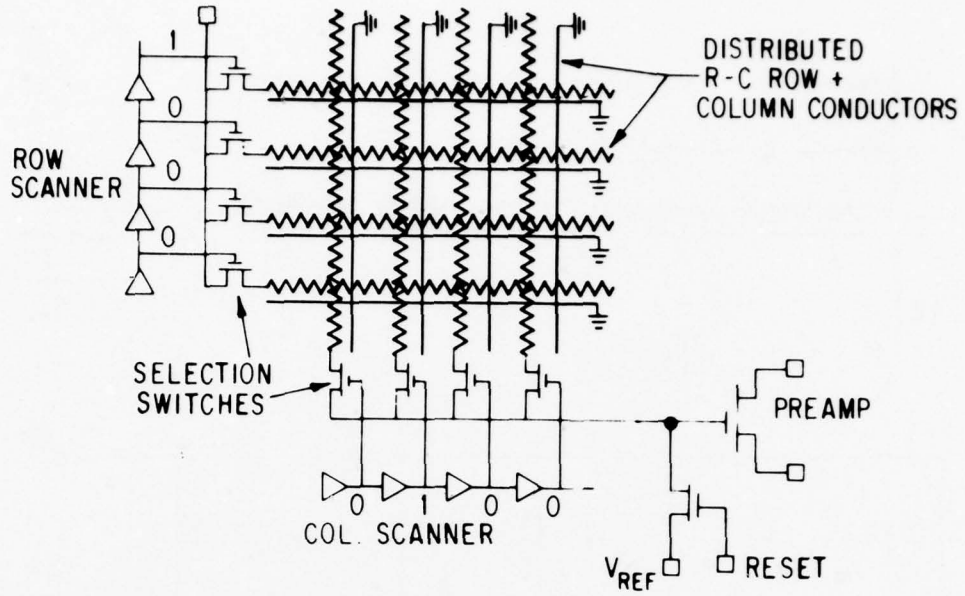
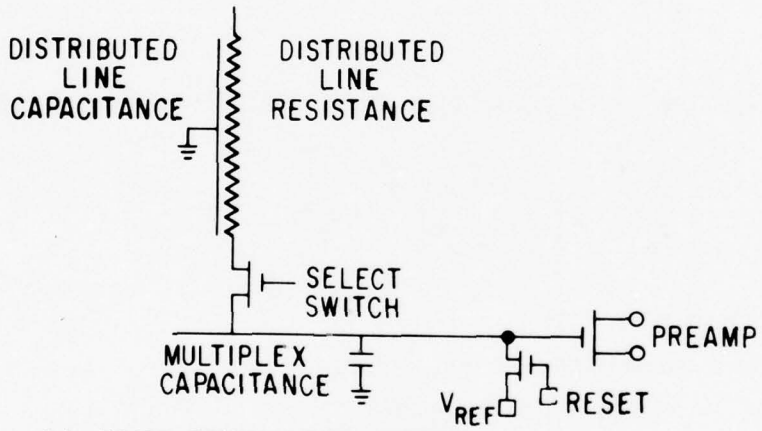


Figure 23. Photomicrograph of one corner of a CID imager showing scanning registers and array structure.



a) ELECTRICAL EQUIVALENT CIRCUIT



b) NOISE EQUIVALENT CIRCUIT

Figure 24. Array equivalent circuits (a) electrical equivalent circuit with one row and column selected and (b) noise equivalent circuit.

The noise equivalent circuit of Figure 25(b) applies if the distributed row time constant does not define the system noise bandwidth. It can be seen that this will usually be the case since a typical line sheet resistivity of 10 ohms/square coupled with distributed capacitance ranging from 3 to 10 nF/cm^2 gives rise to distributed time constants in the range of 30 to 100 nsec for a 1 cm long line. Total noise power can be derived by summing the noise power that appears on the load capacitance from each elemental noise generator, $d(v_n^2)$.

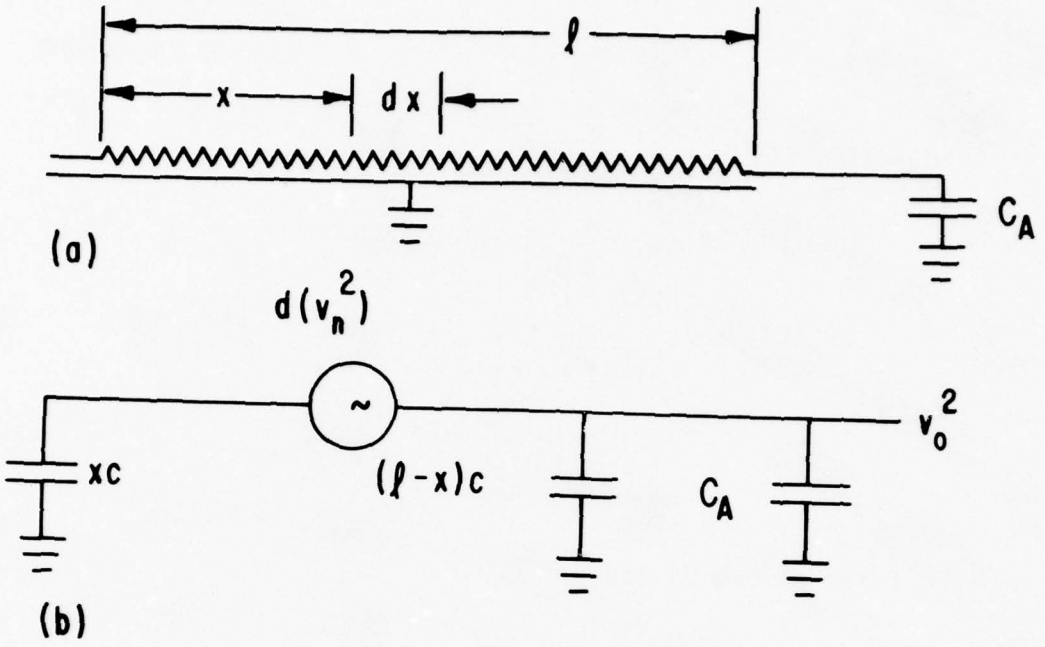


Figure 25. Distributed array conductor (a) electrical circuit and (b) noise model.

$$V_o^2 = \int_o^l \left[\frac{XC}{(C_A + lc)}\right]^2 d(V_n^2) \tag{7}$$

and $$d(V_n^2) = 4\,KT\Delta f\, r\, dx \tag{8}$$

where c = capacitance per unit length

r = resistance per unit length

$$V_o^2 = \left[\frac{4\,KT\Delta\, f\, rl}{3}\right] \left[\frac{lc}{(lc + C_A)}\right]^2 \tag{9}$$

$$V_o^2 = \left(\frac{4\,KT\Delta\, f\, R}{3}\right) \left(\frac{C}{C + C_A}\right)^2 \tag{10}$$

$$V_o^2 = \left(\frac{4\,KT\Delta\, f\, R}{3}\right) \left(\frac{C}{C_T}\right)^2 \tag{11}$$

where $R = rl$ = line resistance

$C = cl$ = line capacitance

$C_T = C + C_A$ = total capacitance

A physical model of a distributed r-c line was constructed, and the output noise was measured as a function of load capacitance and compared with the forgoing derivation. The results are summarized in Figure 26 which has the theoretical values shown as dashed lines and measured values as plotted points.

2.1.2 Line Select Switch

The line select switch is mechanized with an MOS transistor operated as an analog switch. Under these conditions, the drain-source voltage is near zero and the device is operating in its triode region. Channel resistance can be derived from the triode region equations [17] as follows:

$$I_{ds} = \mu C_o \, W/L \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right] \tag{12}$$

where I_{ds} = drain-source current

μ = surface mobility

C_o = oxide capacitance

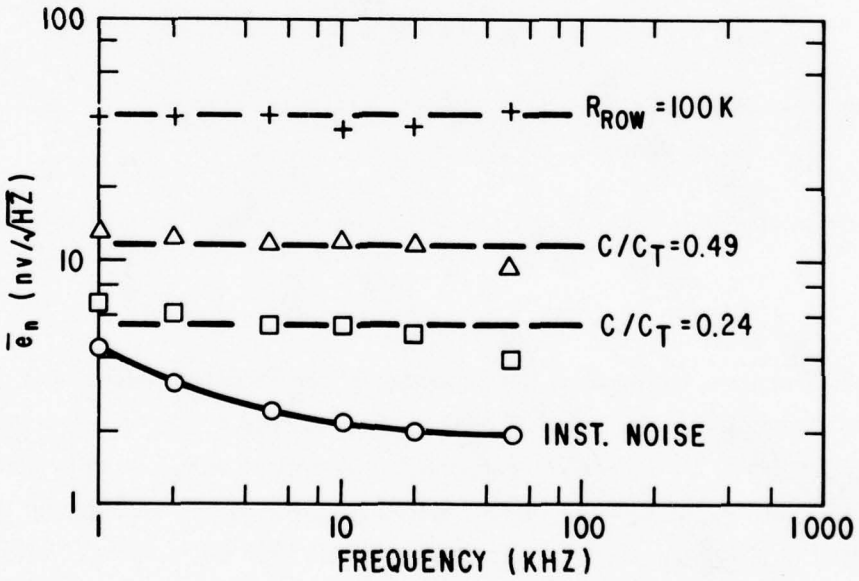


Figure 26. Distributed array conductor effective spot noise for different ratios of distributed capacitance (C) to total capacitance (C_T). Measured values are plotted points; theoretical levels are dashed lines.

[17] Sze, op. cit, p. 519.

L = channel length
V_{gs} = gate-source voltage
V_t = threshold voltage
V_{ds} = drain-source voltage

The channel resistance, r_c, is equal to the derivative of drain voltage with respect to drain current.

$$r_c = \left(\frac{1}{\mu C_o W/L \, (V_{gs} - V_t)} \right) \quad \text{at } V_{ds} = 0 \tag{13}$$

Parasitic source and drain resistance resulting from the non-zero sheet resistance of the source and drain doped regions must be added to the channel resistance to obtain the total selection switch resistance.

Through reference to Figure 24(b), it can be seen that a capacitive voltage divider exists, consisting of the line capacitance (C) and the load (multiplex and preamp) capacitance (C_A), which results in a fraction of the noise generated in the selection switch being delivered to the preamplifier input. The fraction of the select transistor noise voltage, v_s, delivered to the preamp input gate (v_g) is:

$$v_g = v_s \, \frac{C}{C + C_A} \tag{14}$$

where $v_s = (4KTR_s\Delta f)^{1/2}$
R_s = selection switch resistance

The noise charge is equal to the product of noise voltage (V_g) and total capacitance ($C + C_A$).

$$q = V_s C \tag{15}$$

A test transistor included on the periphery of the FPP-128 imager was measured to verify the theoretical noise level. This device has a gate length of 7-1/2 microns and a channel width of 50 microns, a size that is compatible with line selection switch requirements. The "on" resistance was measured for gate-source voltages up to -20 volts which resulted in channel resistance values as small as 1000 ohms. The noise spectral density was measured with the channel resistance set at 1000 ohms and 8000 ohms to span the range of selection switch "on" resistance that can be reasonably achieved. The results, Figure 27, show that theoretical noise levels have been achieved with no excess low frequency (1/f) noise effects.

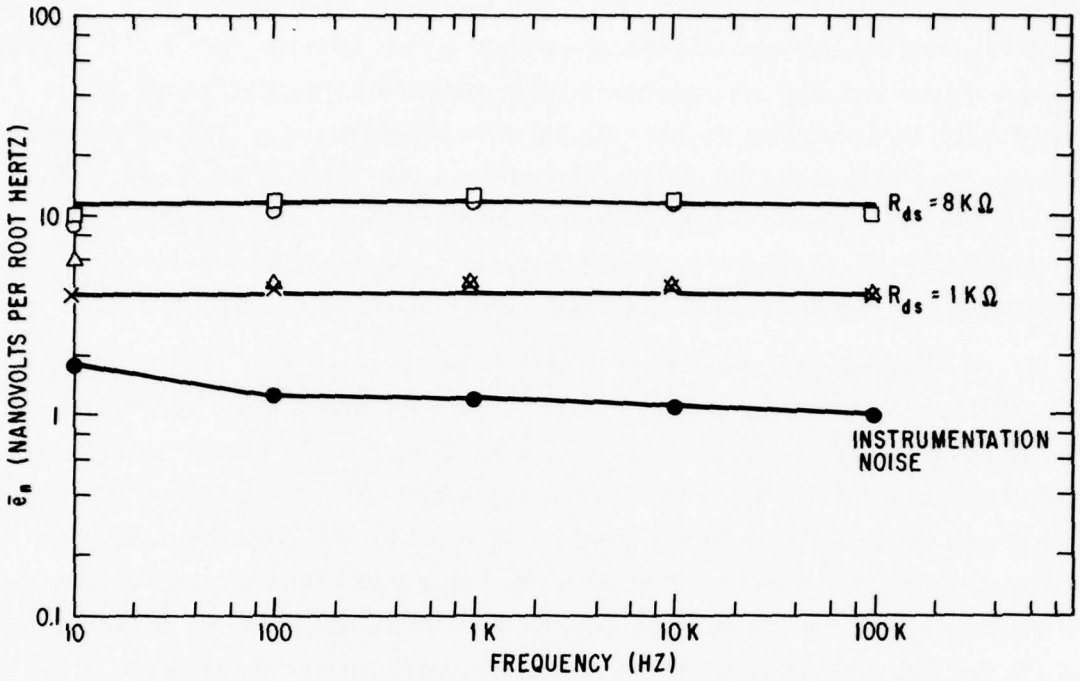


Figure 27. Select switch spot noise. Measured values are plotted points. Theoretical levels are shown by solid lines.

2.1.3 KTC Noise

The uncertainty in the voltage across a capacitor that has been set with a Johnson noise limited switch and allowed to float has been derived by Carnes [18] and is given by:

$$v^2 = KT/C$$

where K = Boltzmann Constant
T = Absolute Temperature
C = Capacitance

This noise voltage can be directly introduced into the video signal should the signal capacitance be reset or it can be introduced indirectly through scanning of array lines that are capacitively coupled to the video line.

The degree to which this noise affects CID imager performance is dependent upon the readout technique used. KTC noise introduced directly into the video signal by a reset operation can be suppressed to a large degree by employing correlated

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[18] Carnes, loc. cit.

double sampling [19]. This is a technique that allows the signal charge to be measured relative to the floating capacitor voltage after reset has been completed. This is accomplished by first sampling the capacitor voltage after reset but before signal charge transfer and then obtaining a second sample after charge transfer. The difference between samples does not contain the KTC offset noise. This procedure results in the substitution of the KTC noise in the sampling circuits for the reset KTC noise. Since sampling can be done after amplification of the array signals, the sampling KTC noise level, referred to the amplifier input, can be made quite small.

An additional potential source of noise in the reset circuitry [20] is fluctuations in partitioning of transistor channel charge between the source and drain electrodes. A test was previously made to measure the level of reset transistor partitioning noise and to evaluate the effectiveness of correlated double sampling for CID image readout. The circuit shown in Figure 28 was built and operated for this noise measurement. The reset MOS transistors have channel dimensions suitable for the reset function in image sensing arrays. These particular devices have a channel width-to-length ratio of 10. A differential junction FET pair was selected for low-noise performance to serve as the test video amplifier input stage. The reset switches and J-FET were operated at low temperature, approximately -20 ^{o}C, to minimize J-FET gate leakage current and its associated shot noise. The differential circuit configuration was chosen because it allows the direct feed-through of the reset pulse to be rejected as a common mode signal while the uncorrelated KTC offset noise power will be summed.

The noise level across the input capacitors was measured as a function of capacitance without and with correlated double sampling. The results, shown in Figure 29 demonstrate, first, that the reset operation does not generate noise in excess of the expected KTC level and, second, that the double sampling technique can effectively reject the reset noise. The residual noise after sampling is a linear function of input capacitance which indicates that it is caused by the amplifier, not the reset operation.

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[19] White, loc. cit.

[20] A.M. Mohsen, M.F. Tompsett, and C.H. Sequin, "Noise Measurements in Charge-Coupled Devices," IEEE Transactions on Electron Devices ED-22, No. 5, May 1975, p. 209.

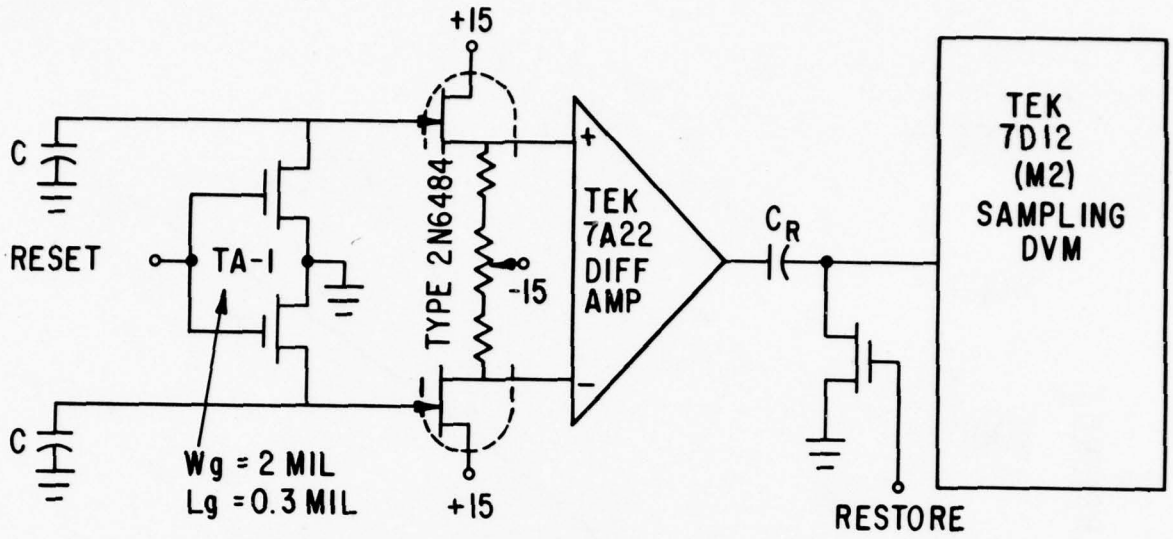

Figure 28. KTC noise measurement circuit.

The select-drive/sense-unselect sequence used during the scanning of a row of imager signals results in KTC offsets on each column after the unselect operation. While these offsets are introduced directly into the signal path with Pre-injection Readout, as previously described, they are indirectly coupled into the video signal in the case of Row Readout. Column KTC noise is coupled to the row conductors via the column-row crossover capacitance, and a noise level proportional to the summation of column KTC noise power can appear on each row conductor at the end of each row scan.

If correlated double sampling is used on each pixel signal, this indirectly coupled KTC noise can be rejected. Additionally, the noise induced on the row conductors is highly correlated. Differential sensing with any extra array row conductor can be used to reject this noise component.

2.1.4 Amplifier Noise

Insulated gate and junction field effect transistors are normally used for the first amplifier stage because of the high output impedance of CID imagers. The Johnson noise level encountered with these devices has been shown by van der Ziel [21, 22] to depend upon channel resistance.

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[21] A. Van der Ziel, "Thermal Noise in Field Effect Transistors," Procedures of the IEEE 50, 8, August 1962, pp. 1808-1812.

[22] A. Van der Ziel, Gate Noise in Field Effect Transistors at Moderately High Frequencies, Procedures of the IEEE 51, 3, March 1963, pp. 461-167.

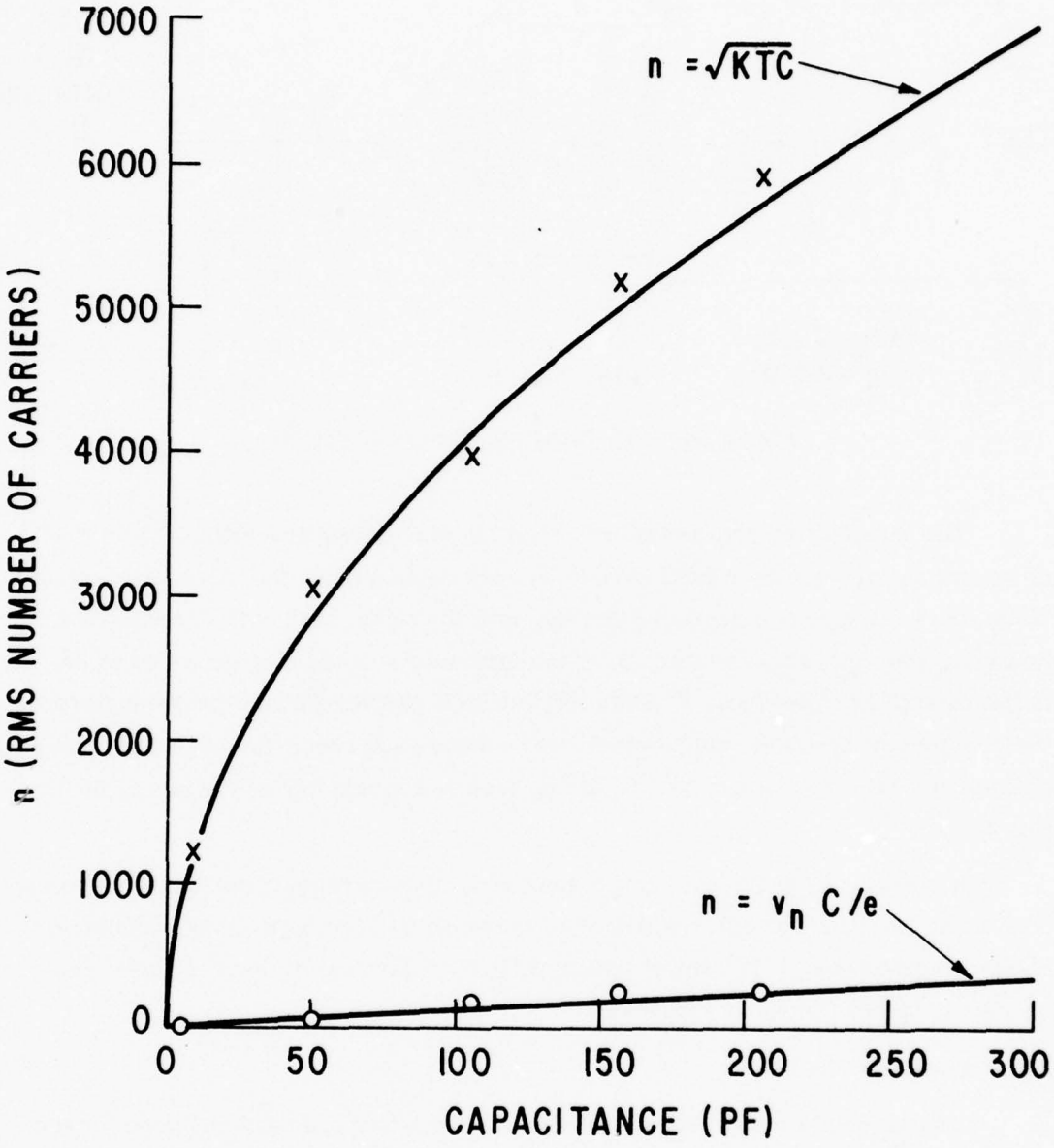

Figure 29. KTC noise. Measured values are plotted points. Theoretical level are shown by solid line.

The equivalent noise resistance is:

$$R_n = (2/3)(1/g_m)$$

This value of noise resistance is used in the normal Johnson noise voltage equation.

$$e_n = (4\ KTR_n\ \Delta f)^{1/2}$$

Excess low-frequency noise, called 1/f noise, is present to some extent in all field effect transistors but is particularly prevalent in surface channel insulated gate transistors.

The equivalent amplifier input noise charge is given by the product of equivalent input noise voltage and the total capacitance connected to the input node. A detailed description of the noise levels of surface and buried channel insulated gate field effect transistors, junction field effect transistors, the effect of feedback, and an optimization procedure are given in Section 2.3.

2.2 SHOT NOISE

Variations in the quantity of charge generated and collected in solid state imagers, either as a result of photon or thermal generation are the source of a noise component called "shot noise." Thermally generated charge that is collected and stored at the imager sensing sites will be called "dark current" during this discussion to separate it from thermally generated charge that is collected by the FET selection switch and amplifier junctions. Junction reverse current will be termed "leakage current."

2.2.1 Dark Current

The interfering effect of shot noise in imager dark current varies with imager organization and readout strategy. The lower limit of dark current shot noise is that instance in which only variations in the dark charge collected and stored at each sensing site contribute noise to the output from that site. Since the CID imager consists of an array of charge storage capacitors interconnected with row and column conductors, an image of the dark current collected and stored under any electrode will appear on the array conductor connected to that electrode. This image current is not normally integrated as is the dark current collected at each sensing site. The image current on the array conductors can, however, interfere with signal readout under certain conditions. If one set of conductors, say the row conductors, is used for signal detection, and the column conductors are biased at a lower voltage magnitude than the row conductors, then dark current collected at all sites along each row will be stored under the row-connected

electrodes. An image of the sum of the dark current for all sites of each row will flow in the row conductors. This dark current induced interference has a shot noise variation.

$$i_s = (2\, q_e\, I\, \Delta f)^{1/2} \tag{16}$$

This noise current can degrade image performance.

It is possible, however, to bias all un-addressed column conductors at a voltage that is larger in magnitude than the row bias level. Dark charge will then accumulate under the column-connected electrodes and, if the column bias voltage is maintained, this charge will not affect the signal on the row conductors. It is not necessary to include special on-chip circuitry to maintain a constant bias voltage on the un-addressed column lines to avoid the interfering effect of the array conductor dark signals. If the column lines are allowed to float during a line scan interval, the dark charge collected under the column-connected electrodes will slightly discharge these lines. The resultant change in column voltage will couple into all row lines because of the column-row crossover capacitance. The row interference, however, is the same on all row lines and can easily be rejected with differential sensing (Row Readout).

The structure and bias levels used for CID image sensing result in a favorable (low) dark current level. Surface dark carrier generation rates are lower under inversion conditions than under depletion conditions [23]. Since bias and signal charge is normally stored under one of the pair of storage capacitors at each sensing site, the inverted surface contributes little surface generated dark charge. In addition, for television applications, charge is transferred from the storage electrode to the opposing electrode at all sites in the array during each line scan. Since the time required for the surface generation rate to reach its steady state depletion value, after being initially inverted, is tens of milliseconds [24] at room temperature and the line scan time is normally 63 μsec, surface generation should be negligible under both electrodes. Only the depleted periphery of the storage region is expected to generate significant surface dark current.

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[23] Fitzgerald, loc. cit.

[24] Dewitt G. Ong and R.F. Pierret, "Thermal Charge Generation in Charge-Coupled Devices," IEEE Transactions on Electron Devices Vol. ED-22, No. 8, August 1975, pp. 593-602.

This effect has been demonstrated by operating an imager under static bias conditions and under scanning conditions. A typical array dark current density value measured was 2.8 nA/cm^2 with static bias and 0.7 nA/cm^2 under scanning conditions, both measurements at room temperature.

2.2.2 Junction Leakage Current

Thermally generated charge is collected by the MOS transistor source and drain junctions that form the readout multiplexer. Junction FET gate reverse current adds to the imager leakage current when these devices are used for the first-stage preamplifier. Under normal conditions, this leakage current is in the tens of picoamps and is completely negligible. Under very low readout rate conditions junction leakage current can interfere with sensor operation. The major effect is that of preamplifier bias level disturbance which is more troublesome than shot noise variations in the leakage current.

2.2.3 Bias Charge

A bias charge level is maintained at each sensing site to avoid a sensitivity loss through charge pumping as mentioned in Section 1.1.4. This charge is maintained by applying a bias voltage, slightly in excess of the threshold voltage, to the injection drive voltage. When voltage is first applied to a CID imager, either dark current or photon-generated charge provides the initial quantity of bias charge. Charge in excess of the bias level is injected once per frame under normal operating conditions. A temporal variation from frame-to-frame would be expected in this bias charge level.

The process by which any given packet of bias charge is formed is through injection of excess photon or thermally generated charge. Injection of charge from a potential well should be a shot-noise-dominated process as is injection across a forward-biased diode. Under steady state illumination conditions, during which signal charge is accumulated in excess of the bias charge level, shot noise on the signal charge should dominate. Similarly, under steady state dark conditions, dark current shot noise is the dominant noise mechanism. Only under transient conditions, when the illumination is reduced, could the shot noise in the injection current be a limiting noise source. However, if during any interval of time shot noise leads to an excess amount of charge injected, then this action reduces the charge remaining and, consequently, reduces the driving potential and, hence, the current that flows subsequently. Variations in the quantity of charge injected at various times during this process are not independent events. The noise associated with this process consequently must be less than the shot noise associated with the injection current.

In summary, frame-to-frame temporal noise on the bias charge can only be a dominant noise under transient, light-to-dark, image-dynamic conditions. Photon or dark current shot noise would be greater than the noise associated with the injection current under steady state conditions. This noise component has not been observed to date.

2.3 AMPLIFIER NOISE OPTIMIZATION

Transistor amplifiers are usually characterized by determining an equivalent input noise voltage and noise current. Bipolar transistor equivalent input noise voltages and currents lie in the nanovolt and picoamp per root hertz range, respectively. Field effect transistors also exhibit equivalent input noise voltage levels in the nanovolt per root hertz range, but equivalent input noise current levels are at least three orders of magnitude lower, in the femptoamp per root hertz range [25]. The high output impedance of charge transfer devices, in the tenths of picofarad to tens of picofarad range, almost always leads to selection of a field effect transistor for the first stage to achieve lowest amplifier noise.

The noise characteristics of the various types of field effect transistors are examined later in this section. The relationship between device output impedance, transistor input impedance, and negative feedback on equivalent noise charge is described first so that transistor parameters can be properly assessed.

2.3.1 Configuration

The most common first-stage configuration used with charge transfer devices is the source follower. This configuration is first analyzed to relate equivalent input noise charge to transistor equivalent input noise voltage and circuit capacitance. The results are then applied to a very high input impedance series feedback amplifier. Theoretical and measured noise levels for this amplifier are compared. The noise characteristics of amplifiers employing both capacitive and resistive shunt feedback are also derived. Finally, the conditions for minimum equivalent input amplifier noise charge are defined.

A source follower circuit is shown in Figure 30(a) and its noise equivalent circuit in Figure 30(b). The current balance at the source node gives:

$$g_m(V_g + e_n - V_s) = V_s\,(G_L + jwC_1C_2/(C_1 + C_2)) \qquad (17)$$

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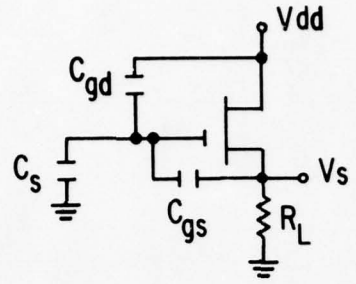
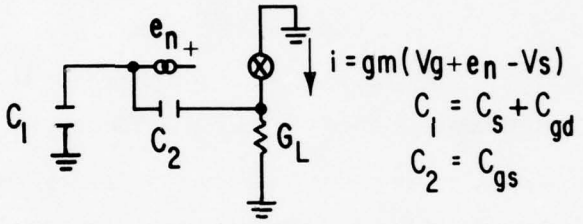
[25] C.D. Motchenbacher and F.C. Fitchen, Low-Noise Electronic Design, John Wiley and Sons, 1973, pp. 307-330.



(a) SOURCE FOLLOWER CIRCUIT



(b) NOISE EQUIVALENT CIRCUIT

Figure 30. Source follower (a) electrical circuit and (b) noise equivalent circuit.

The capacitive divider between the source, gate and ground results in:

$$V_g = \frac{V_s C_2}{C_1 + C_2} \tag{18}$$

Substituting (18) in (17) and reducing:

$$V_s = \frac{g_m e_n}{G_L + g_m \left(1 - \frac{C_2}{C_1 + C_2} + \frac{jwC_1C_2}{C_1 + C_2}\right)} \tag{19}$$

The response of this circuit to a charge signal, q_s, can be derived by again writing the current balance equation for the source node.

$$g_m (V_g - V_s) = V_s \left(G_L + \frac{jwC_1C_2}{C_1 + C_2}\right) \tag{20}$$

The charge balance at the gate node gives:

$$q_s = \frac{\frac{g_m q_s}{C_1 + C_2}}{G_L + g_m\left(1 - \frac{C_2}{C_1 + C_2}\right) + \frac{jwC_1C_2}{C_1 + C_2}} \tag{21}$$

The amplifier noise can be expressed as an equivalent noise charge by equating equations (19) and (21):

$$q_s = e_n(C_1 + C_2) \tag{22}$$

The equivalent input noise charge is equal to the product of the equivalent input noise voltage and the total capacitance connected to the input node.

At this point it is necessary to discuss the measurement of equivalent input noise voltage. As illustrated in Figure 30(b), the transistor noise is represented as a voltage generator in series with the gate. This noise voltage can be measured with a number of commercial transistor noise analyzers such as the Quan-tech Model 2173C. This instrument operates by measuring transistor drain noise current, in the grounded source configuration, and displaying an equivalent input noise voltage equal to the noise current divided by the transistor transconductance. When the transistor is operated as a source follower, with the gate floating, the source-drain noise current is increased because of the bootstrapping effect of the source-gate capacitance.

The important result of this analysis is given by equation (22). The equivalent input noise charge of the amplifier has not been altered by the degeneration (negative feedback) of the source follower configuration even though the capacitance seen looking into the gate terminal has been reduced. This reduction in input capacitance is offset by the increase in noise voltage through source-gate bootstrapping.

A very low input capacitance amplifier, achieved through the use of series negative feedback, was constructed and evaluated to measure quantitatively this bootstrapping effect. The circuit is shown in Figure 31 with the operational amplifier positive input bias network replaced with a battery for clarity.

The circuit values used for the experimental evaluation result in a closed loop gain of 10, and a source voltage equal to 20/21 of the input voltage. This results in a factor of 21 reduction in gate-source capacitance and, because the source voltage is applied to this transistor drain by the operational amplifier feedback network, a factor of 21 reduction in gate-drain capacitance. The measured noise spectral density of this amplifier

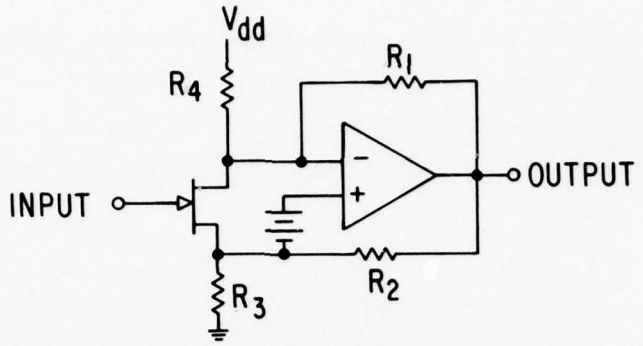


Figure 31. Low input capacitance amplifier.

is shown in Figure 32. Note that the product of mid-band equivalent input noise voltage and total input capacitance is approximately constant and equal to the product of the grounded gate equivalent input noise voltage (transistor noise) and the total transistor capacitance (Cgs + Cgd). The excess low-frequency noise observed with the gate floating is assumed to be caused by input noise current.

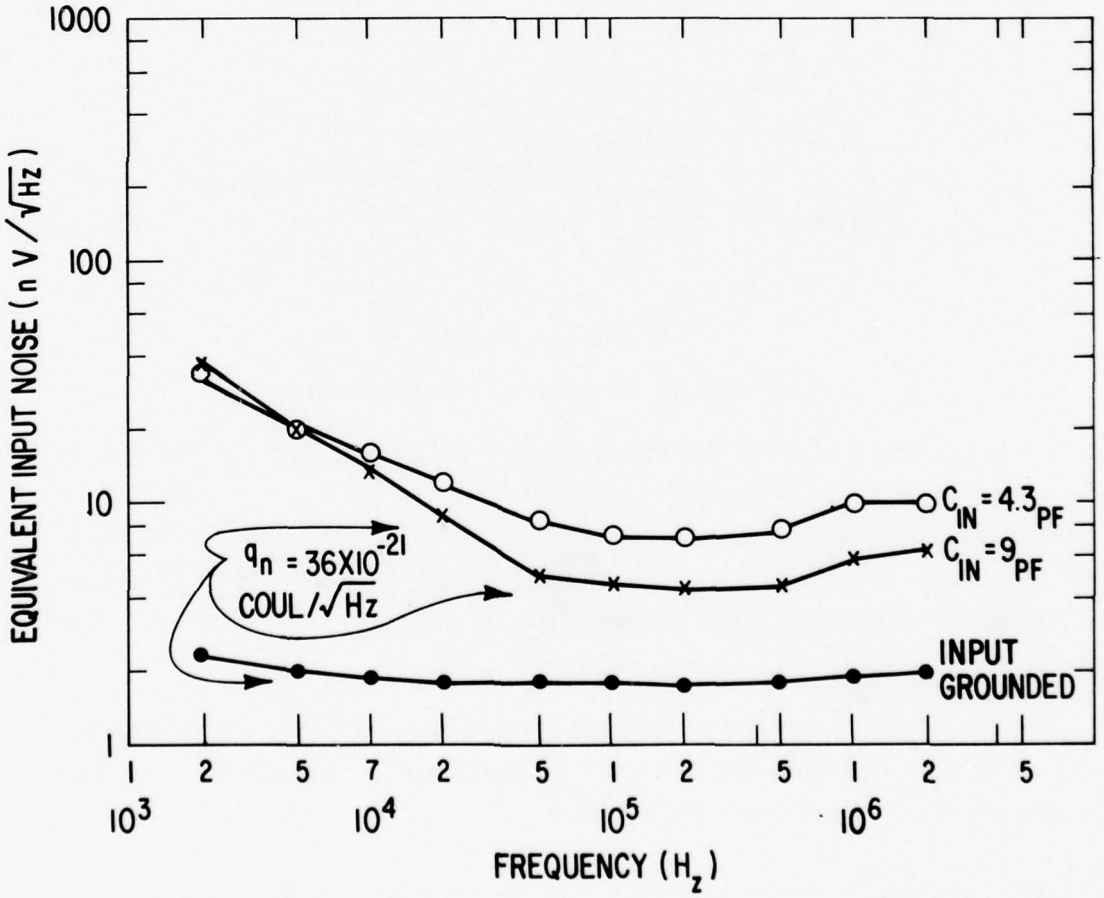


Figure 32. Measured noise of low input capacitance amplifier illustrating that noise charge (q_n) does not vary with feedback.

The effect of shunt feedback was investigated by analyzing a current amplifier of the type used with videcons and the Pre-injection CID camera. This configuration has been thoroughly investigated by other workers, for instance Hall [26], and is included here for completeness. The equivalent input noise current for the circuit of Figure 33 is given by:

$$i_n = e_{nt}\left(\frac{1}{R_f} + JwC\right) + i_{nt} \tag{23}$$

It is usually practical to use a feedback resistor that is much larger than the capacitive reactance at the maximum video frequency to minimize the noise-current magnitude. The noise voltage term in usually dominant for large CID imagers operating at video rates in the megahertz range. As in the series feedback case, noise charge is determined by the product of the equivalent input noise voltage and the total input node capacitance.

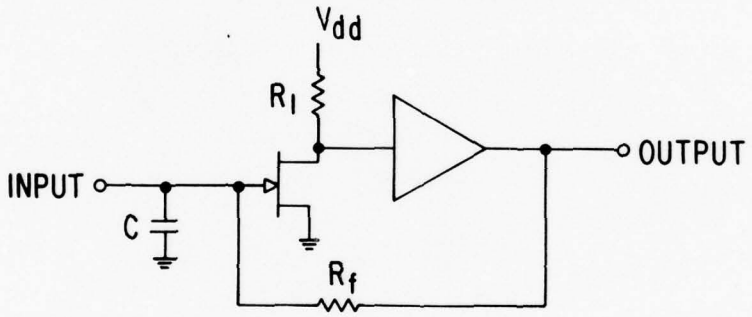


Figure 33. Shunt feedback current amplifier.

It has been suggested that the effect of output capacitance of the CID imager could be circumvented by the use of feedback amplifier, by means of which the output charge could be caused to appear across a much lower value of capacitance, thus enhancing the signal. Aside from the practical difficulties of devising an amplifier system with sufficient gain-bandwidth, stability, and recovery characteristics, it can be shown that such a system degrades the signal-to-noise ratio.

The circuit is shown in its simplest form in Figure 34; here C_s is the source capacitance, q_s the signal charge to be detected, and C_{fb} the feedback capacitor across which the signal charge is to appear.

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[26] P.G. Jespers, F. Van de Wiele and M.H. White, Solid State Imaging, Noordhoff International Publishing, Legden, 1976, pp. 535-559.

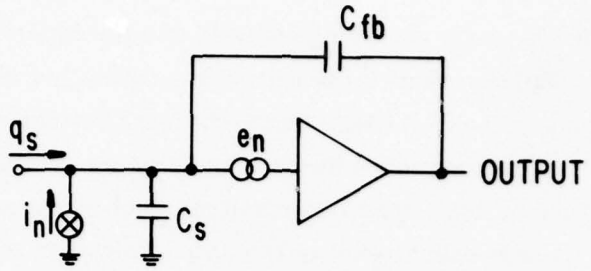

Figure 34. Capacitive feedback amplifier.

The effective capacitance seen by the input charge, q_s, is easily derived and is given by

$$C_{in} = C_s + (A_v + 1)\, C_{fb} \tag{24}$$

where the second term is the familiar "Miller" capacitance.

To obtain an expression for the system gain to the noise voltage, one can write

$$e_o = -A_v \left(\frac{C_{fb}}{C_s + C_{fb}}\ e_o + e_n \right) \tag{25}$$

from which can be derived

$$\frac{e_o}{e_n} = \frac{-A_v}{1 + \dfrac{A_v C_{fb}}{C_s + C_{fb}}} = \frac{-A_v (C_s + C_{fb})}{C_{in}} \tag{26}$$

The total signal appearing at the output is then

$$e_o = -A_v \left[\frac{q_s}{C_{in}} + \frac{i_n}{jwC_{in}} + \frac{e_n (C_s + C_{fb})}{C_{in}} \right] \tag{27}$$

and the signal-to-noise ratio is

$$S/N = \frac{q_s}{\dfrac{i_n}{jw} + e_n (C_s + C_{fb})} \tag{28}$$

which shows that while the effect of the noise current is unchanged by feedback (as might have been inferred from the schematic), the effect of the noise voltage is dependent on C_{fb} and S/N is a maximum when $C_{fb} = 0$; that is, no feedback.

It has been concluded from the foregoing analyses and the experimental measurements that, for the circuit configurations investigated, the equivalent input noise charge is determined by the product of the first-stage transistor noise voltage and the total input node capacitance. Feedback does not reduce this noise charge. Equivalent input noise charge can be increased by noise from other sources, such as the second amplifier stage, or by increasing input node capacitance in the case of negative capacitive feedback.

2.3.2 Field Effect Transistors

Minimum equivalent input noise charge can obviously be achieved by minimizing the input node capacitance-noise voltage product. The theoretical Johnson noise level of field effect transistor is:

$$e_n = (4KTR_{eq}\Delta f)^{1/2} \tag{29}$$

where K = Boltzmans constant
T = absolute temperature
Δf = noise bandwidth

and $$R_{eq} = (2/3)(1/g_m) \tag{30}$$

The equations describing surface channel MOS transistor operation are well known. In the saturation region drain current and g_m are given by Sze [27] as:

$$I_{ds} = \left(\mu C_o/2\right)\left(W/L\right)\left(V_{gs} - V_t\right)^2 \tag{31}$$

$$g_m = \mu C_o \left(W/L\right)\left(V_{gs} - V_t\right) \tag{32}$$

$$C_g = WLC_o \tag{33}$$

where I_{ds} = drain - source current
μ = surface mobility
C_o = oxide capacitance
W = channel width
L = channel length
V_{gs} = gate-source voltage

[27] S.M. Sze, op cit, pp. 515-523.

V_t = threshold voltage
g_m = transconductance
C_g = gate capacitance

For an array source capacitance of C_s, the total noise charge is given by:

$$q_n = ((8/3)\ KT\Delta f/g_m)^{1/2}\ (C_g + C_s) \tag{34}$$

Substituting (32) for g_m and (33) for C_g

$$q_n = \left[\frac{(8/3)\ KT\Delta f}{\left(\frac{\mu C_o W}{L}\right)\left(V_{gs}-V_t\right)}\right]^{1/2} \left[WLC_o + C_s\right] \tag{35}$$

It can be seen that the noise voltage decreases with transistor gate width while capacitance increases. The minimum noise charge can be found by setting the partial derivative of q_n with respect to W equal to zero. The minimum noise charge occurs when $C_g = C_s$.

If, instead of maintaining constant gate-source voltage, transistor power dissipation is limited, as is often the case with on-chip amplifiers, equations (31) and (32) can be combined to define transconductance in terms of drain current.

$$g_m = \left(\frac{2I_{ds}\mu C_o W}{L}\right)^{1/2} \tag{36}$$

Noise charge can be calculated as before:

$$q_n = \frac{((8/3)\ KT\Delta f)^{1/2}\ (WLC_o + C_s)}{\left(\frac{2I_{ds}\mu C_o W}{L}\right)^{1/4}} \tag{37}$$

The minimum noise charge occurs when $C_g = C_s/3$. The variation in noise charge with the ratio of input capacitance to source capacitance is plotted in Figure 35 for both cases. A similar situation exists with junction field effect transistors. Transconductance and input capacitance are linear functions of gate width so that the same optimization criteria apply under constant gate-source voltage conditions.

The noise spectral density of a properly processed P-channel surface FET is shown in Figure 36. Note that the theoretical level of high-frequency noise has been obtained. The 1/f corner frequency of approximately 100 kHz is typical for these devices. N-channel

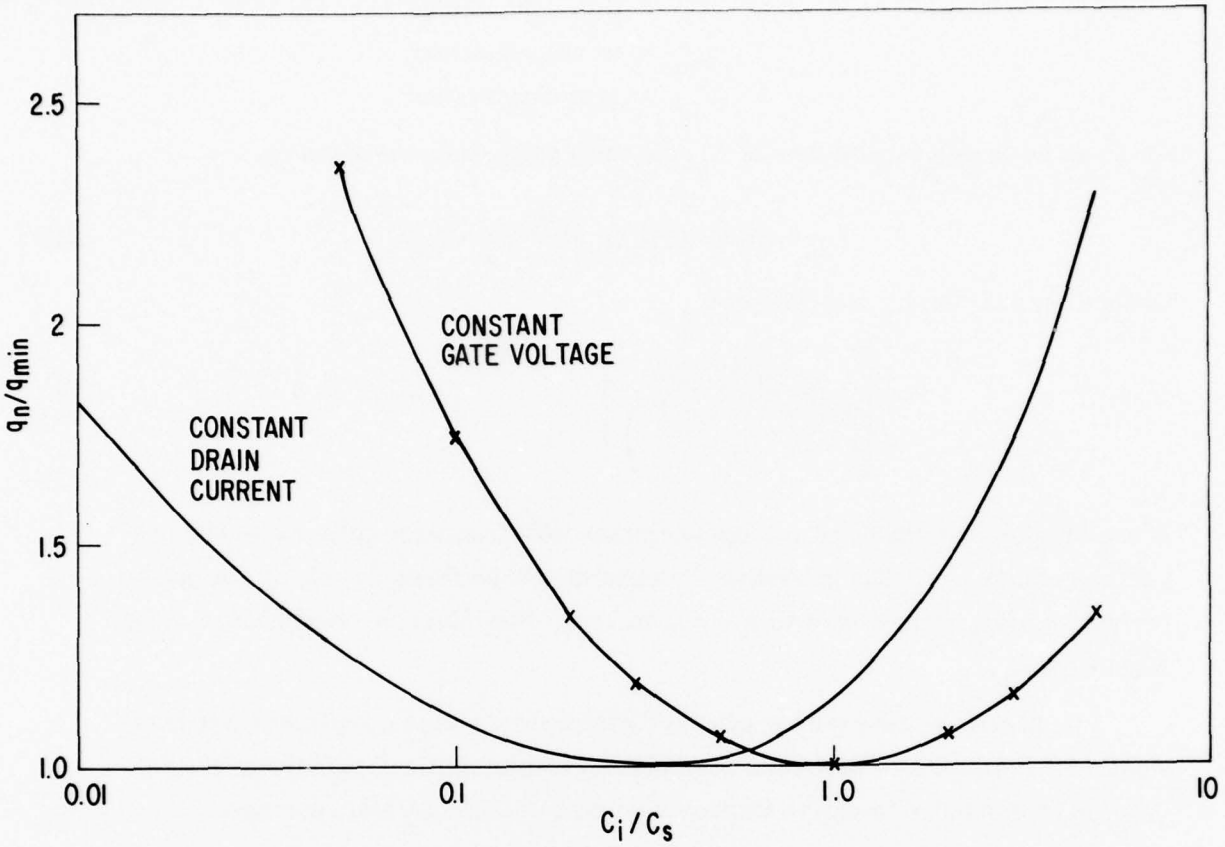

Figure 35. Ratio of noise charge (q_n) to minimum noise charge (q_{min}) as a function of the ratio of FET input capacitance (C_i) to array capacitance (C_s).

surface FETs have exhibited somewhat higher low frequency (1/f) noise (see Section 2.3.3 Figure 42). A junction FET selected for low-frequency operation of CID imagers has been evaluated. Measured noise spectral density for these devices are shown in Figure 37.

2.3.3 Buried Channel MOSFETs

This portion of the report consists of a comparative study of 1/f noise of surface channel MOSFETS and buried n-channel MOSFETs. This study is based on many A1-gate processed MOSFETs with ion implantation to achieve the desired buried channel.

Buried channel MOSFETs fabricated using ion implantation have potentially low-noise characteristics [28,29,30]. In a previous report [31], 1/f noise in P-buried channel

[28] K.Nakamura, O. Kudoh, M, Kamoshida, and Y. Haneta, "Noise Characteristics of Ion-Implanted MOS Transistors," in Procedures of the 4th International Conference on Ion Implantation in Semiconductors and Other Materials, S. Namba, ed, Plenum, N.Y. 1975, p. 709, also in Journal of Applied Physics, Vol. 46, pp. 3189-3193, 1975.

[29] R.W. Brodersen and S.P. Emmons, "Noise in Buried Channel Charge-Coupled Devices," IEEE Transactions on Electron Devices, Vol. ED-23, 1976, pp. 215-223.

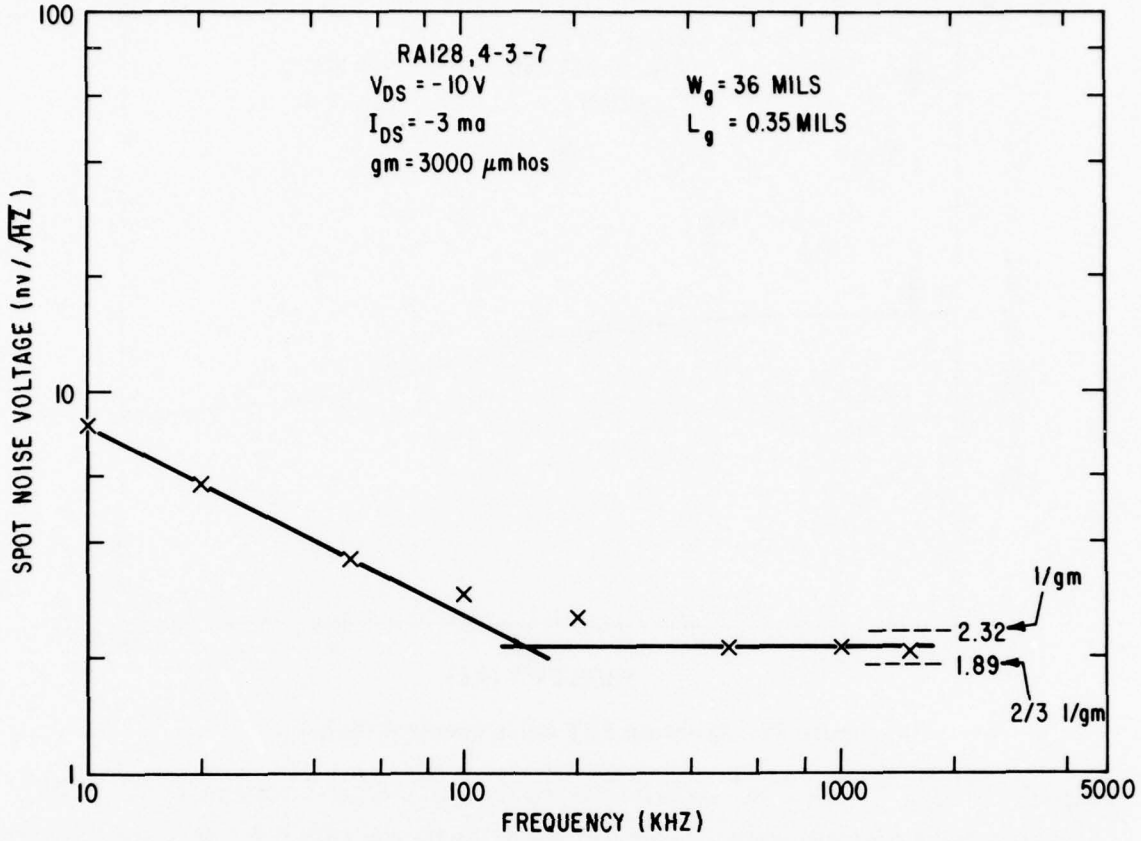

Figure 36. Measured noise spectral density of P-type surface channel FET processed on random access CID imager.

MOSFETs fabricated using an Al-gate process was reported. The reduction of 1/f noise in comparison with the surface channel MOSFETs was demonstrated in the high-current region of operation. A detailed investigation regarding the excess noise at low current was carried out. It was concluded that the unique residual defects in $^{11}B^{+}$ implantation cause the increase of 1/f noise in low current operation. The work was then extended to n-buried channel devices with the prospect that the residual defects in $^{31}P^{+}$ implanted MOSFETs would be small.

The experimental n-channel MOSFETS were fabricated using Al-gate processing. The field implant of $1x10^{14}$ $^{11}B^{+}cm^{-2}$ at 30 KeV was carried out in order to prevent the surface from inverting. The implant fluence appears to have been high. As a result, the p-n junctions at the source and the drain exhibit a premature avalanche breakdown. The

[30] L.J. Essen, "Peristatic Charge-Coupled Devices: A Type of Charge - Transfer Devices," Electron letter Vol. 8, 1972, pp. 620-621.

[31] K.L. Wang, "Measurements of Residual Defects and 1/f Noise in Ion-Implanted P-Channel MOSFETs," IEEE Transactions on Electron Devices ED-24, 1978, p. 478.

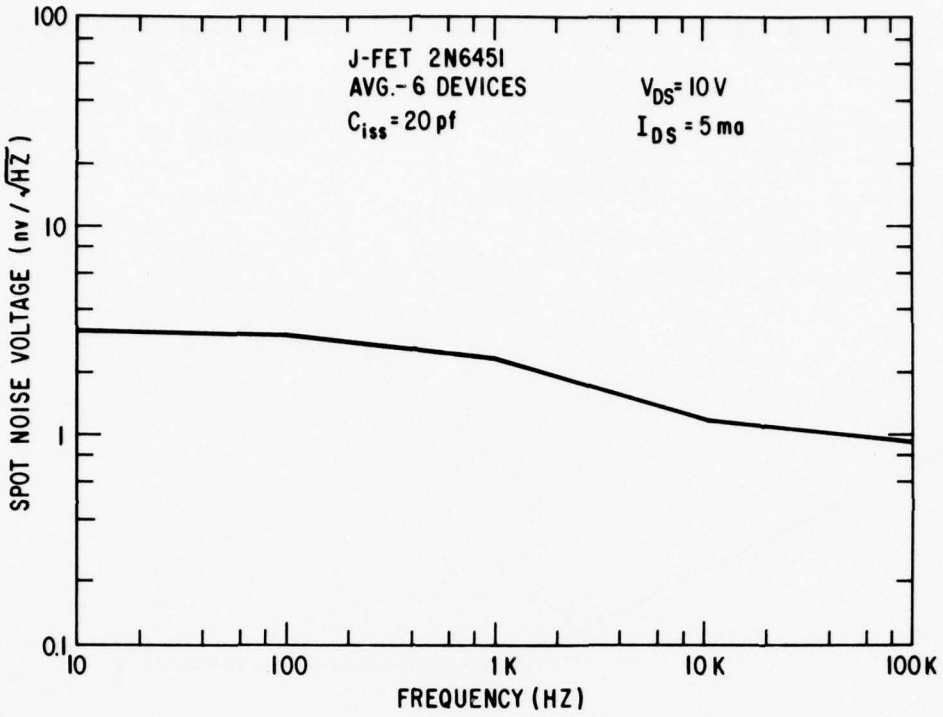

Figure 37. Junction FET noise spectral density.

ion species, $^{11}B^+$, $^{31}P^+$ or $^{28}Si^+$, were implanted through the gate oxide of 1200Å. The $^{31}P^+$-implanted structures were prepared to study the doping effect for creating the buried channel, while the $^{28}Si^+$ implanted samples were used for investigating damage as a result of ion implant. In the case of the $^{28}Si^+$ implant, the $^{28}N_2^+$ background contribution is less than one percent of the total fluence. The unimplanted and implanted MOSFETs were processed identically in the same wafer with the exception of implantation masking.

The equivalent gate noise voltage was measured at room temperature for all the samples using a Quan-Tech noise analyzer Model 2173C. The noise spectrum for 10 Hz to 100 kHz as a function of the drain current was obtained in the common-source configuration.

Typical C (v) curves for 5×10^{11} $^{31}P^+ cm^{-2}$ implant and for the control surface channel are illustrated in Figure 38. The C (v) curves and the threshold voltage shift due to the implant can also be numerically obtained from the solution of Poisson's equation. The solution may be obtained with assumed Gaussian implant profile or any other more appropriate function. The numerical routine for one-dimensional n-channel structures was established. By comparison with the calculated results, it is observed that the C (v) curves for some lots show apparent high interface state density for the implanted as well as control surface channel devices.

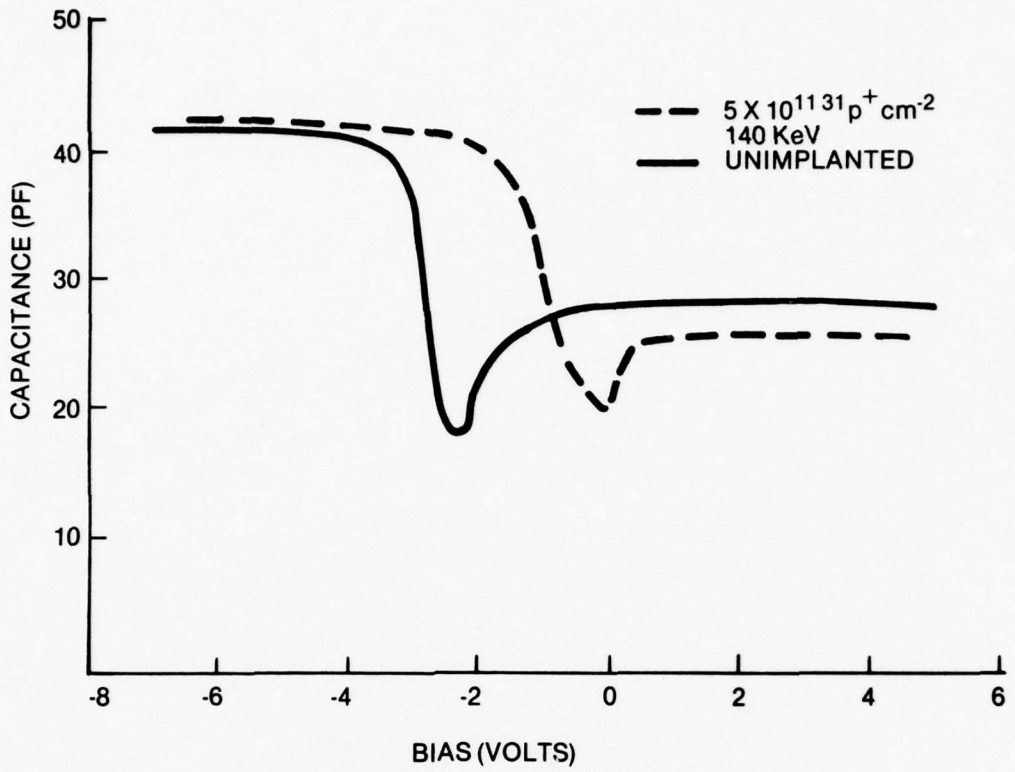

Figure 38. C (v) curves for $5 \times 10^{11}\ ^{31}P^{+}\ cm^{-2}$ implanted and unimplanted samples.

The measured 1/f noise data for the $^{31}P^{+}$ implanted buried channel and the controlled surface channel devices are illustrated in Figures 39 and 40 for two different wafers under the same implanted condition. Figure 39 shows a slight reduction of 1/f noise value while Figure 40 does not show this clearly. For a high $^{31}P^{+}$ implanted fluence, the device yield is poor and has either high leakage or high contact resistance. Thus, the 1/f data are not consistent. For $1 \times 10^{12}\ ^{11}B^{+}$ implanted structures, 1/f noise is shown in Figure 41 showing a sporadic data scattering. This prevents us from drawing any conclusion.

The overall noise power is higher than the corresponding P-channel structures (aspect ratio = 32, area = 0.0013 cm^2, and gate oxide 1200 Å thick).

It is likely that the avalanche breakdown is contributing the excess noise. The reduction of avalanche breakdown voltage of the P-N junctions results from the high field implant fluence. It is observed that the breakdown voltage of the junctions is about 5V and the junction leakage current is in the order of microamperes.

The resulting 1/f noise voltage shows a great deal of scatter. This is possibly the result of soft junctions and some processing difficulties.

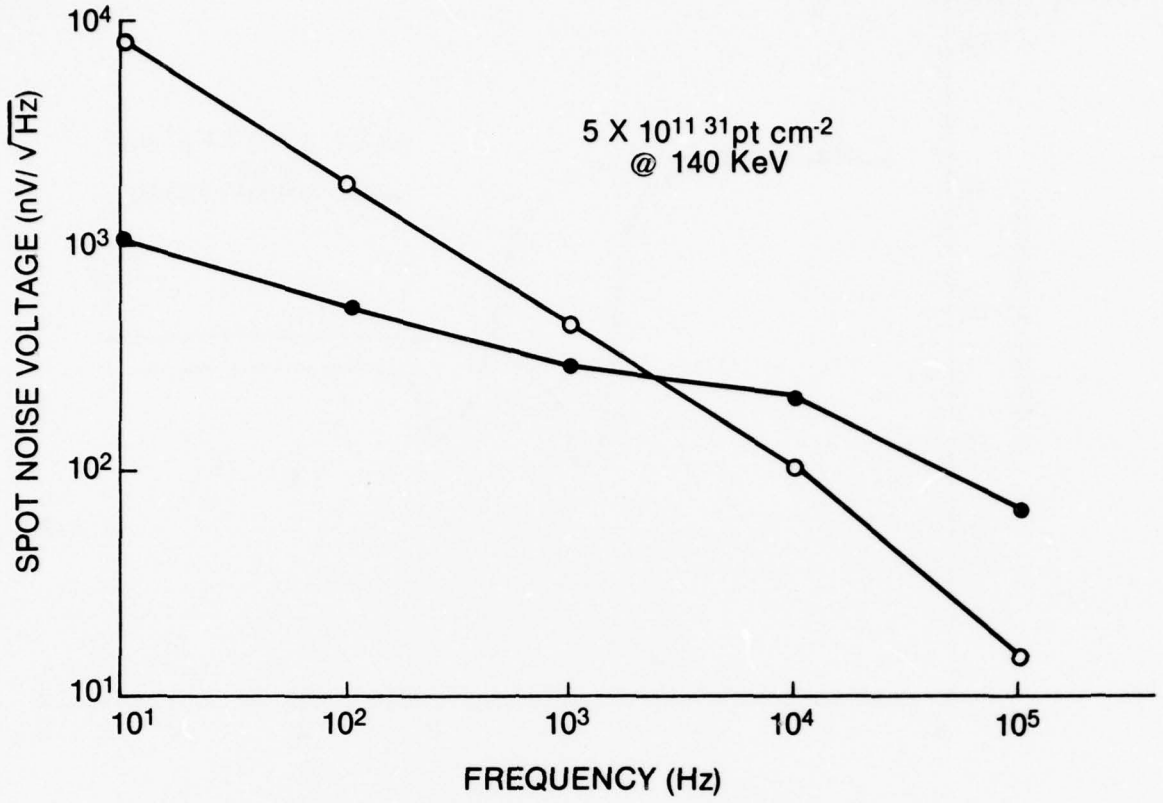

Figure 39. 1/f noise spectrum for the 5 x 10^{11} $^{31}P^{+}$ cm^{-2} implanted case (solid data points). The reduction of 1/f noise below that of the control sample (open data points) was observed.

The 1/f noise in surface and buried n-channel MOSFETs was investigated comparatively. Some reduction of low-frequency noise in the buried channel MOSFETs was observed. However, the overall noise power is higher than the corresponding P-channel structures. In addition, the 1/f noise data for the control MOSFETs scattered among the wafers tested. This scattering of the data may be attributed to the soft avalanche breakdown of the P-N junctions, which is probably resulted from the too high fluence implant for the field control. In addition some threshold variation among control MOSFETs in different wafers suggests some difficulties in fabrication control. Thus, the study cannot be treated conclusively.

The transistors used in this study were aluminum gate, interdigitated devices. A recently published report on low noise buried channel MOSFETs [32] shows that a similar low avalanche voltage also was obtained with interdigitated devices. The data on stripe geometry devices from that report have been plotted in Figure 42 along with measured noise on a P-surface channel device with the same gate area, under the same bias conditions.

[32] P.G. Carrigan, T.F. Cheek, H.S. Fu, W.F. Stephens, and A.F. Tasch, Integrated Low Noise Buried Channel MOSFET Preamplifier Technology, Report No. AFAL-TR-77-235, December 1977.

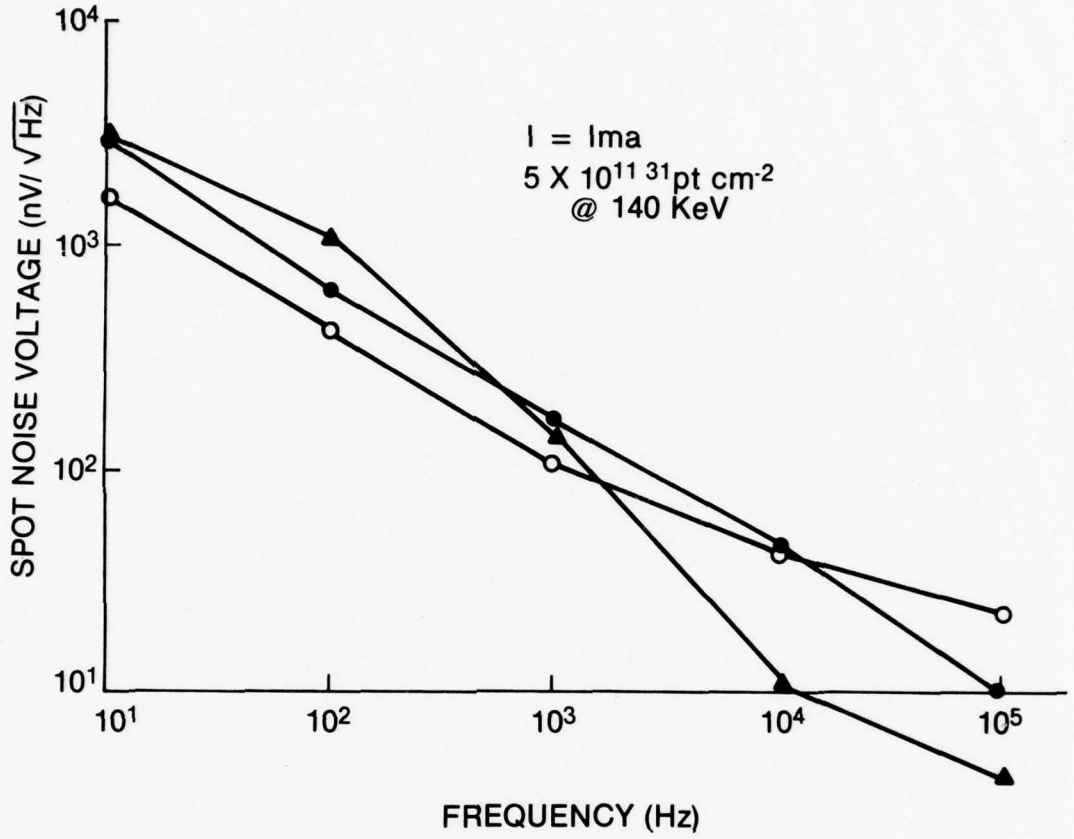

Figure 40. 1/f noise spectra for the same implant conditions as Figure 39. No clear reduction in noise was demonstrated. Note that the noise voltage for the control sample is higher than shown in Figure 39 indicating the avalanche associated noise.

The P-channel device exhibits lower 1/f noise over all but a narrow band of frequencies between 400 Hz and 8 kHz.

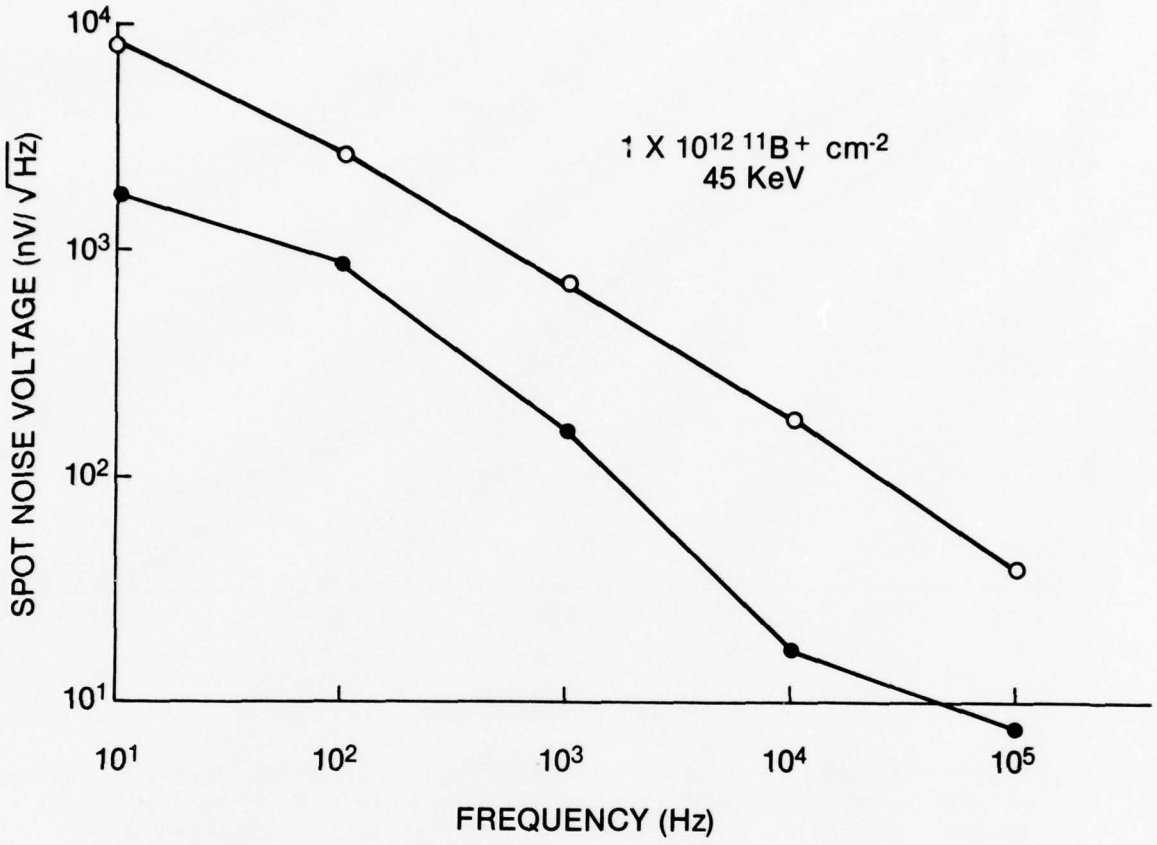

Figure 41. 1/f noise spectra for 1 x 10^{12} $^{11}B^{+}$ implant. Although the implanted sample showed a noise voltage reduction below the control sample, the control sample exhibited higher noise (open data points) than that shown in Figure 40.

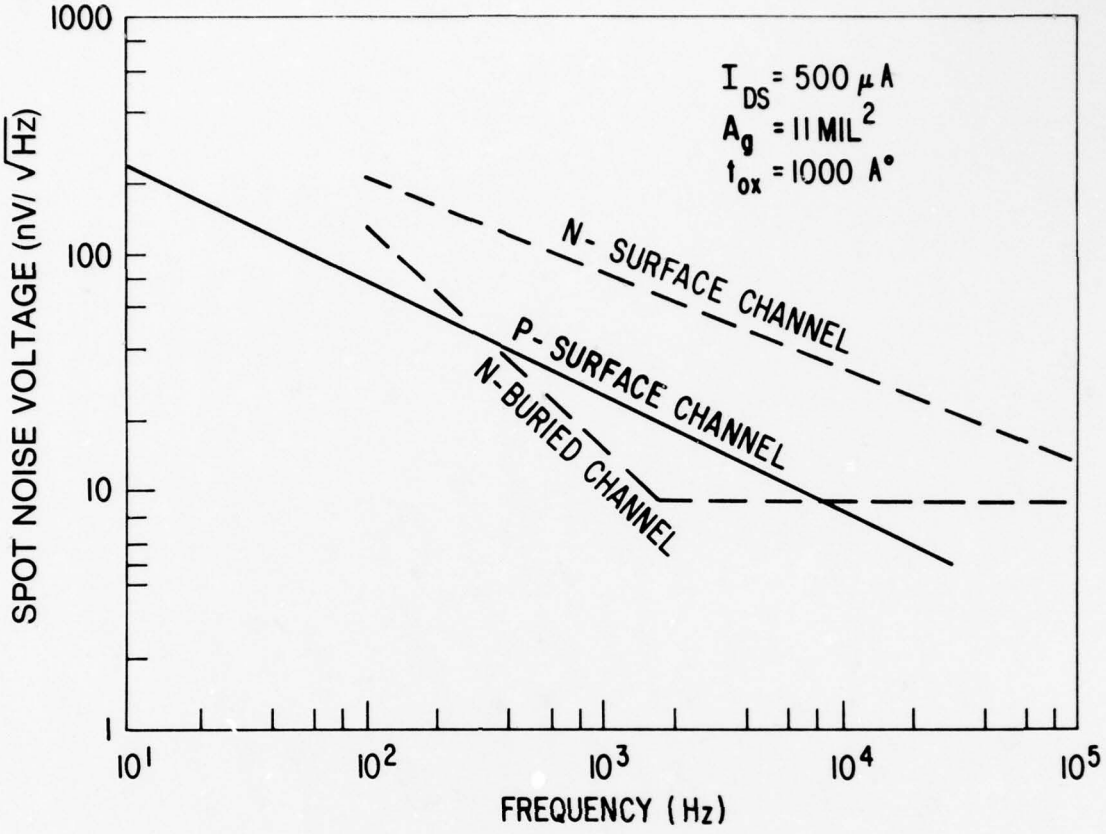

Figure 42. Comparison of low-frequency noise performance of P-type surface channel FET with N-type surface and buried channel FETs.

Section 3

FIXED PATTERN NOISE

The term "fixed pattern noise" is used to designate those signal variations that repeat frame-to-frame to give rise to a fixed background pattern in the displayed image. While usually unrelated to the optical input (and generally most noticeable with no input), some FPN is image-related in that it varies to some degree with the magnitude of the video signal.

The sources of these video defects are many including silicon material imperfections, contaminants, process-inducted imperfections, and deficiencies in the readout techniques and mechanization. Silicon material imperfections, such as resistivity striations, etc., will not be directly addressed here, as they have been rather extensively studied by others [33] . In addition, these effects are generally not present in epitaxially grown silicon such as is used for most CID imagers.

Unlike thermal noise, whose causes are well understood and amenable to analysis and which can be described in understandable terms with respect to its effect on final system performance, FPN is difficult to describe definitively as to either quantity or quality. In order to obtain a quantitative measure of FPN, a liberty has been taken. It is assumed that while the FPN is unvarying temporally, it varies in a random way spatially, and can be represented by an RMS value of pixel samples taken over the image. The justification for this approach is that it tends to weigh each individual variation with respect to its amplitude and frequency of occurrence, and more importantly, it permits the use of automatic data acquistion and processing circuitry.

3.1 BACKGROUND FIXED PATTERN NOISE

Background FPN means that portion of the total FPN that is unrelated to the readout signal, to a first order, and appears in the displayed image as an unvarying background. The major sources of this effect are structural imperfections in the array, site-to-site variations in bias charge, and dark current, and parasitic interference from servicing electronics (switching noise). While these effects appear in the video signal as a composite signal, they can be separated to some extent by appropriate readout methods and a measure of their contributions taken.

[33] S. Yoshikawa and J. Chikawa, "Electrical Effect of Growth Striations in the Silicon Videcon-type Camera Tubes," Applied Physics Letters, Vol. 23, No 11, December 1, 1973.

3.1.1 Switching Noise

Because of the relatively low level of the charge-induced signal as compared to the drive voltages, the opportunity for drive voltage interference is great. The use of on-chip MOS transistors to raise the power level of the video signal will, to a great extent, alleviate off-chip interference effects, assuming suitable care is taken in the design and layout of the peripheral circuitry. On-chip, electrical coupling can exist between the driven scanner or decoder lines and the array or signal buses. The various readout methods differ in their susceptibility to this interference. The Row Readout technique, in which the signal is sensed on the lines orthogonal to the driven lines, exhibits the best performance with respect to switching noise.

3.1.2 Bias Charge Variations

As described above, a bias charge is introduced under the storage electrodes by maintaining the row and column drive voltages above the device thresholds. Since the bias voltage levels must be such as to accommodate the worst-case threshold in the array, variations in thresholds across the array introduce a variation of net bias charge. In those readout methods involving sensing of the charge transferred between the storage wells, this bias charge is sensed in addition to the signal charge, resulting in a background FPN proportional to site-to-site threshold variations. As with structural imperfections, this source of FPN is yielding to processing improvements. A measure of this component of FPN can be obtained by operating the imager with and without bias charge. The results of such a test will be discussed below.

3.1.3 Structural Variations

There are many process-induced imperfections that can introduce non-uniformities in the readout signal. These include mechanical surface damage, photolithographic imperfections, variations in layer thickness, layer-to-layer registration errors, pattern definition (etching) errors, etc. In many cases, a cause-effect relationship can be established, as in the case illustrated in Figure 43(a). This image photograph of a 128x128 array taken at wafer probe, shows several irregular blotches in the upper part of the image. The amplitude of this artifact is a few percent of full scale, as indicated by the superimposed image (the bright vertical line is a gross defect that would, of itself, result in rejection of the device and is not defined as pattern noise). Examination of the array in the area of interest by means of a scanning electron microscope revealed the offending photolithographic defect. This is evidenced in Figure 43(b) as an enlargement of the upper level (white) conductor as seen in the upper portion of the SEM photograph. This effect, which probably resulted from a photoresist non-uniformity, covered an area of the array that

coincided with that of the optical defect observed in the displayed image. The electrical result of this structural variation was an increase in row-column capacitance. This type of defect is becoming rarer as the state-of-the-art of integrated circuit processing and quality control measures improve.

3.1.4 Dark Current Variations

Since thermally generated charge is indistinguishable from signal charge under any circumstances, it is an ever-present component of the readout signal, and variations in the rate of thermal charge generation over the array will appear as a background variation in the image. The many forms of these image defects are familiar to all those involved in imaging, and their causes extensively studied [34]. As with other process-related effects, dark current can be expected to improve with improvements in the art. At the present time CID imagers, with average dark currents of less than $1nA/cm^2$, are produced regularly, with concomitant uniformities.

Dark-current-induced FPN can be evaluated by noting the reduction in FPN as device temperatures are lowered since dark current is a strong function of temperature. The results of such a test is discussed in Section 4.3.

3.1.5 Measured Results

The net effect of the various components of FPN is dependent upon the type of readout used. The measurements to be described in this section were made on a device employing the Row Readout technique. This approach tends to reject switching noise but is more sensitive to array patterning variations. A brief description of this test array follows.

The Focal Plane Processor (FPP-128) array was developed under U.S. Air Force sponsorship to demonstrate on-focal plane analog signal processing for direct readout of spatial (Hadamard) transform data [35]. The array contains 128 rows and 128 columns, selected by groups of four on both axes, as shown in Figure 44. Selection of the subgroups is by means of scanning registers. As each 4x4 group is selected, the column lines are driven to cause the transfer of charge either into or out of row-connected electrodes of the four selected rows. In this manner, an algebraic sum of the four charge packets on each selected row is effected. Normal (sequential) readout is obtained by

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[34] Y. Hokari, H. Shiraki, "Video Defects in Silicon," Japanese Journal of Applied Physics, Vol. 16, No. 4, April 1977, pp. 584-590.

[35] G. Michon and H. Burke, CID Processor Chip Development, Report No. AfAL-TR-77-135, May 1977.

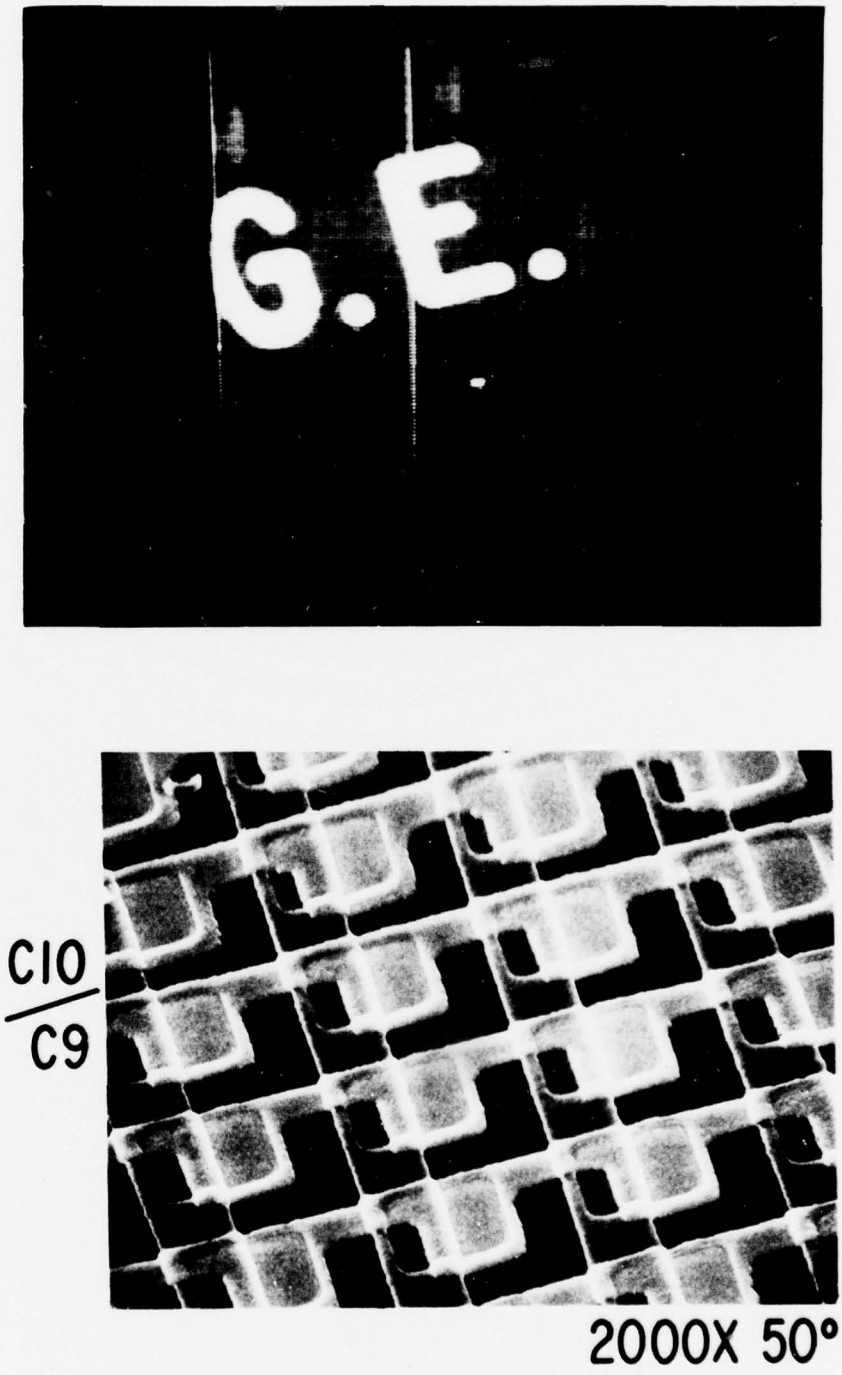


Figure 43. Array lithographic induced fixed pattern noise: (a) probe test image and (b) SEM photograph of defect.

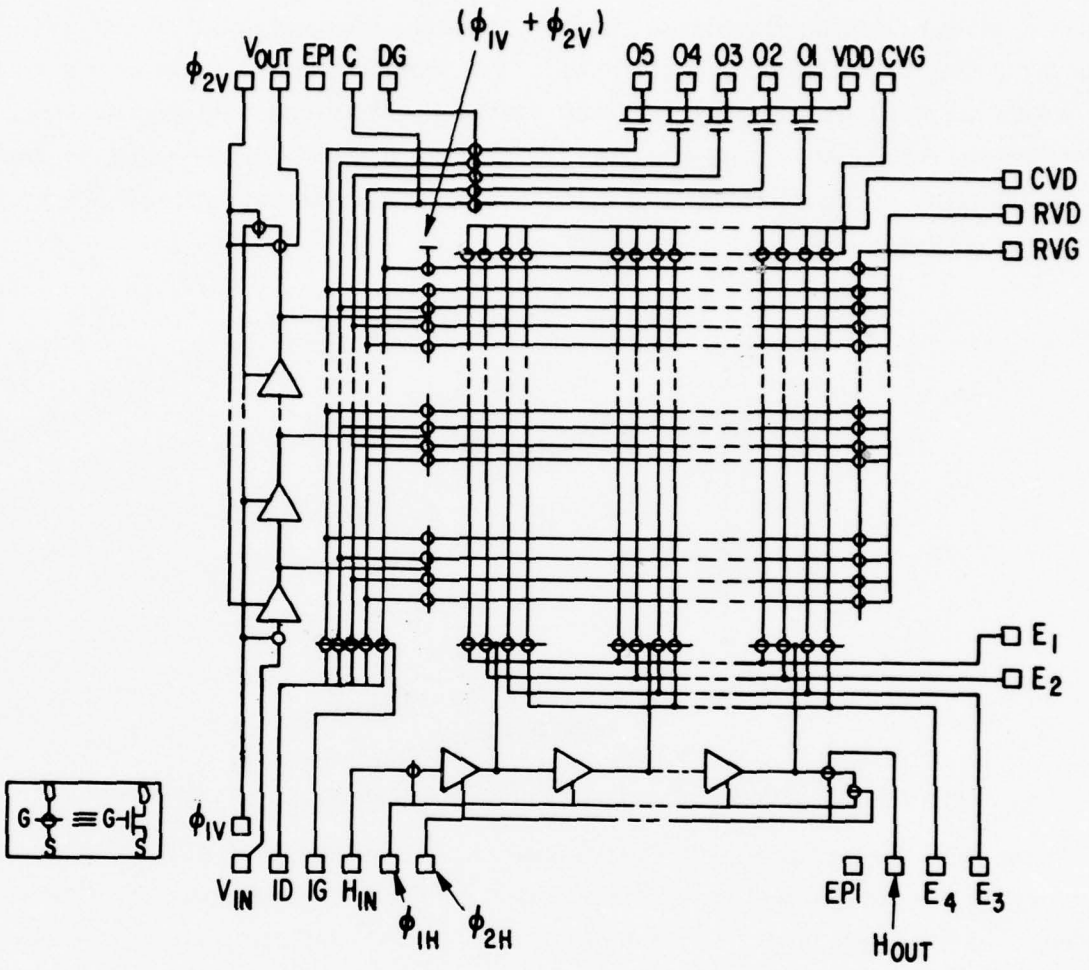


Figure 44. Focal Plane Processor array schematic.

driving the columns sequentially and multiplexing the video outputs onto a single output channel.

In addition to the 128 active rows, an additional row is used to provide differential cancellation of column drive interference. This row is selected for every row address and cleared whenever a row is cleared. The output of the compensation row is subtracted from each of the signal outputs so that the relatively large offset created by the parasitic coupling of the column drives to the rows is cancelled. The primary purpose of this feature is to reduce the dynamic range requirements on the sense circuitry and does little to reduce pattern noise, except to the extent that the pattern noise is correlated along the columns. This effect is small except for those rows very near the compensation row.

Fixed pattern noise was measured on the FPP-128 array operating at 30 frames/sec in the normal mode. This was done by first taking the mean of 25 readings at each of

50 sites along an un-illuminated row. This was to reduce temporal noise. The 49 differences between the mean background values for adjacent sites along the row were averaged to obtain the mean pixel-to-pixel variation. This process was repeated for a number of rows and the results plotted in Figure 45. The decrease in FPN with increasing row number is the result of the increasing effectiveness of the compensation line (Row 128). Note that this was total FPN, taken between adjacent pixels.

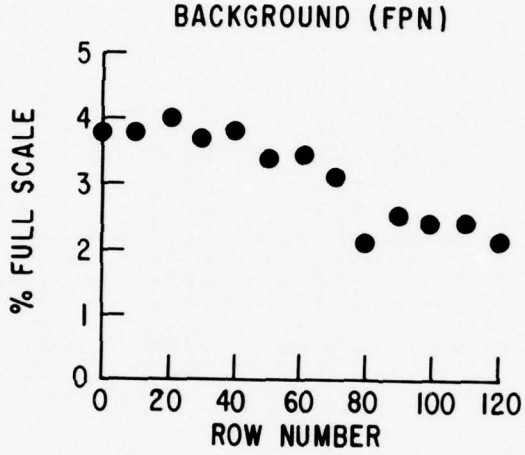


Figure 45. Background fixed pattern noise versus array row number.

In order to evaluate the effect of the various sources of FPN, a FPP-128 array was operated under different conditions of bias charge and drive voltages. This time the video waveforms were photographed in order to display FPN effects in what is perhaps a more familiar form. The resulting waveforms are shown in Figure 46. The top oscillograph traces, Figure 46(a), show the video waveforms for a normal readout. This corresponds to the conditions for which the numerical results reported above were obtained. In all cases in Figure 46 the video signal would be negative-going with full scale about coincident with the lower graticule line. To obtain the signals shown in Figure 46(b), the substrate (EPI) voltage was adjusted downward so that the positive excursions of the column drive voltages were less than the threshold voltage. Under this condition, this storage wells are emptied of bias charge by the "charge pumping" effect of interface state trapping under the column electrodes.

The absence of bias charge is evidenced by the reduction of the average value of the signal and a reduction in the amplitude of the noise envelope. This observed reduction in FPN cannot be contributed in its entirety to bias charge alone since some reduction in thermally-generated charge occurs due to charge pumping.

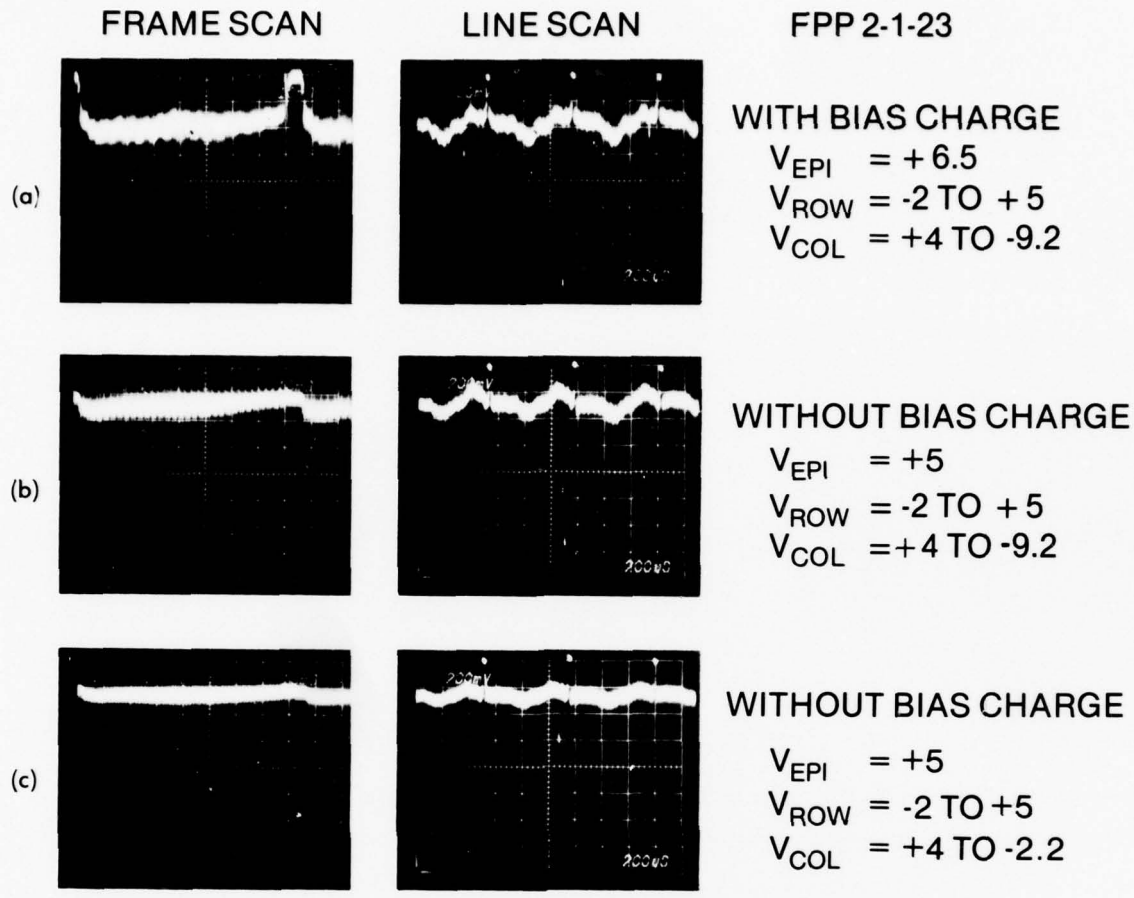


Figure 46. Background fixed pattern noise video with and without bias charge and at reduced drive voltage level without bias charge.

To obtain a measure of the amount of structurally generated FPN present in the residual signal of Figure 46(b), the column drive voltage excursions were reduced by one-half, and the waveforms of Figure 46(c) resulted, indicating that the remaining FPN was largely due to variations in column-to-row electrical coupling.

Yet another perspective of the effects described above can be had by examination of the same video signals of Figure 46 displayed on a TV monitor (Figure 47). As before, the upper photographs correspond to normal readout, while the lower pictures are for the condition of no bias charge. Both conditions are shown for normal and high gain (contrast) conditions. Several bright spots attributed to localized high dark current sources

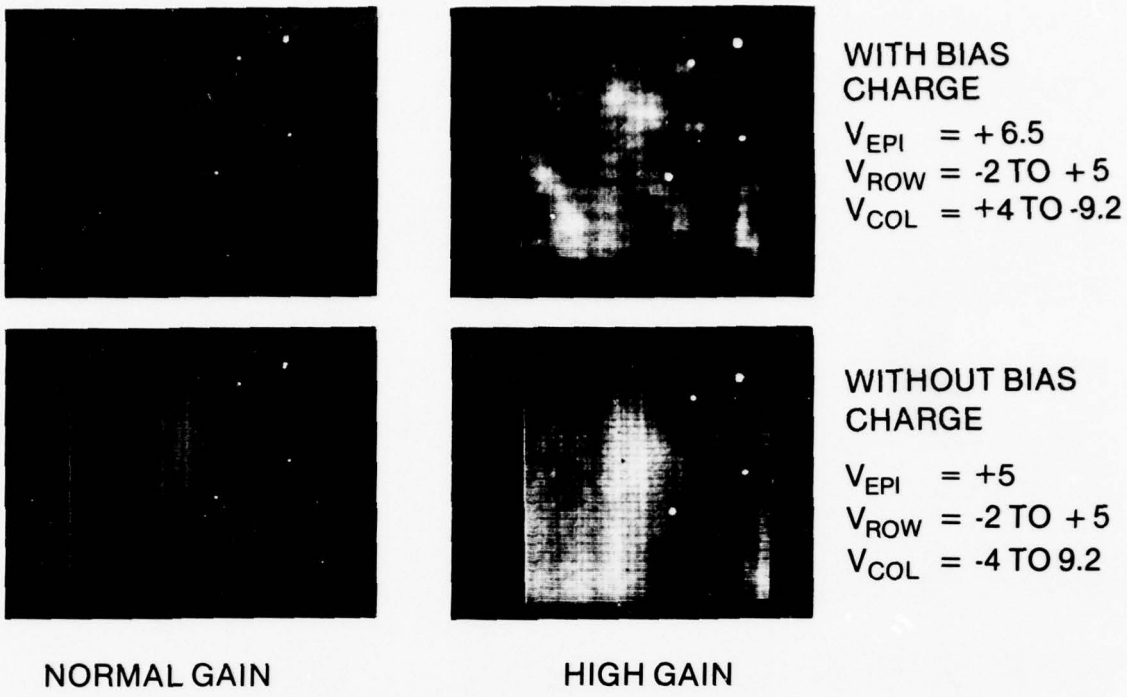


Figure 47. Background fixed-pattern-noise images with and without bias charge.

appear in the displayed image, as well as in the waveforms shown above. These are somewhat reduced in the lower images, indicating that some reduction in dark current has occurred. The repetitive variations in the displayed rows noticeable in the high contrast images are externally caused.

Figure 48 shows the total background noise of Figure 46 (a) superimposed on an image. The highlight portions of the image are somewhat less than full scale.

3.2 SENSITIVITY VARIATIONS

Site-to-site variations in sensitivity will result in the appearance of FPN that is more pronounced in the highlight portion of the image. This effect could result from patterning variations in any opaque or semi-opaque layers on the array surface. In some instances, this might result from gain differences of amplifier channels that are subsequently multiplexed onto a single video line. The latter cause can be corrected by suitable adjustment, and is not considered as a fundamental FPN source. Sensitivity variations of the FPP-128 array were measured by first finding the mean signal for 25 readings at 3/4 full-scale illumination for each of 50 sites along a row. From these values was subtracted similar values measured for no illumination. The 49 differences of these signal-minus-background values were then averaged to determine the pixel-to-pixel sensitivity variation which is plotted in Figure 49. The FPN contribution of sensitivity variations is thus seen to be relatively small.

Figure 48. Image superimposed on fixed pattern noise.

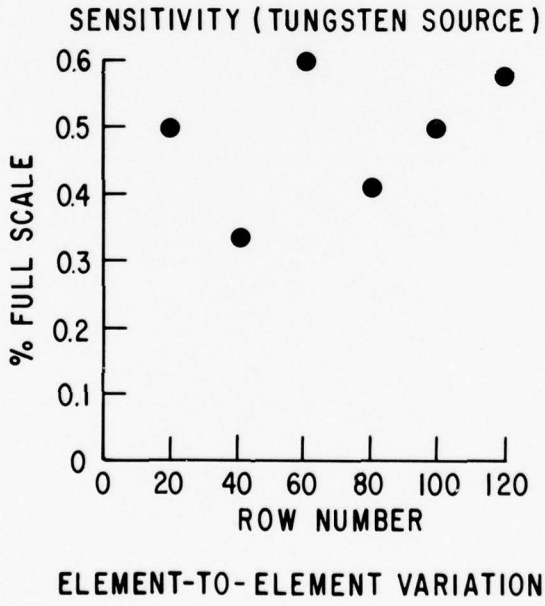


Figure 49. Sensitivity variation versus row number.

Section 4

IMAGER PERFORMANCE

The temporal noise levels that can be obtained with CID imagers are a strong function of operating conditions such as video rates, imager size, and readout technique. Johnson noise in selection switches and amplifiers usually is the dominant temporal noise source when these imagers are operated at television rates. Non-destructive readout and low video rates can be used to obtain low noise for special applications such as astronomical measurement.

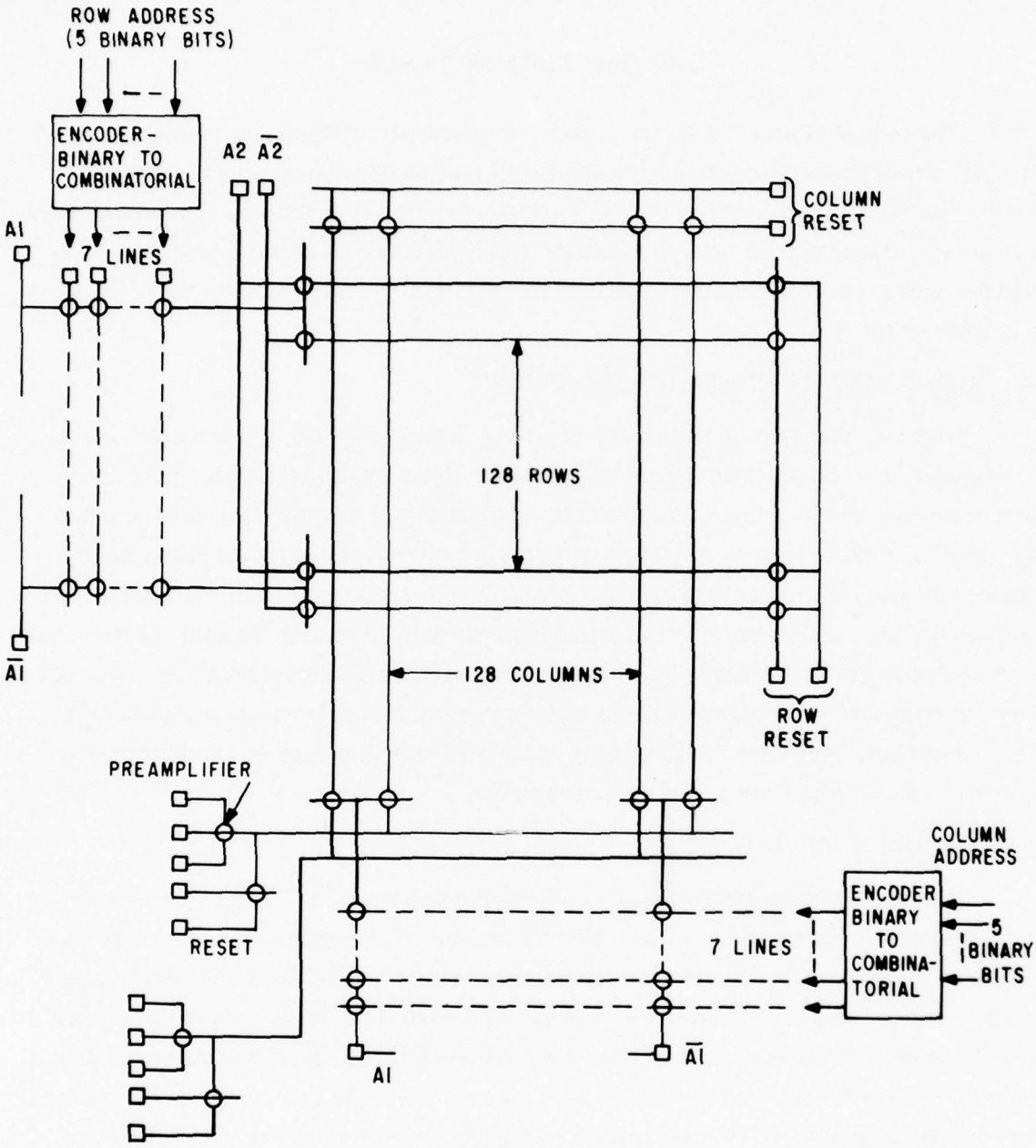
4.1 NOISE VERSUS READOUT TECHNIQUE

Three of the readout techniques that have proven most useful have been selected for evaluation of operational imager noise levels. Sequential Injection has been used with a random access imager, the RA-128. This technique has the advantage of pixel-by-pixel fixed pattern noise cancellation and hence can be used with a random access device. Pre-injection readout is compatible with high-speed television compatible readout and has been incorporated into certain commercially available General Electric CID Cameras such as the TN-2000. The Row Readout technique is most promising for achievement of both low temporal noise and a high degree of fixed pattern noise cancellation. The Focal Plane Processor image sensing array (FPP-128) employs one variant of Row Readout and has also been selected for evaluation.

4.1.1 Sequential Injection

A random access 128 row by 128 column imager, called the RA-128, incorporates combinatorial decoders for row and column selection. The organization of this array is shown in Figure 50. On-chip 3-of-7 combinatorial decorders are used to select 1-of-32 outputs per decoder. Two decoders, separately enabled with the A1 and $\overline{A1}$ inputs, are used to select one of 64 pairs of rows. The final level of row selection is mechanized with the odd/even enable lines A2/$\overline{A2}$. Columns are selected in a similar manner except that the final level of column selection (odd/even) is performed by selecting which of the two video channels is sampled. Off-chip binary-to-combinatorial code converters ("read only" memories) are used for interfacing with binary address inputs.

The video channel equivalent circuit after selection is diagrammed in Figure 51 along with the basic readout waveforms. After column and row selection, the video channel is reset, allowed to float, and a sample of the floating signal line voltage is taken during the restore interval for KTC noise rejection. The selected column is then pulsed



128 X 128 RANDOM ACCESS ARRAY SCHEMATIC DIAGRAM

Figure 50. 128x128 random access array schematic diagram.

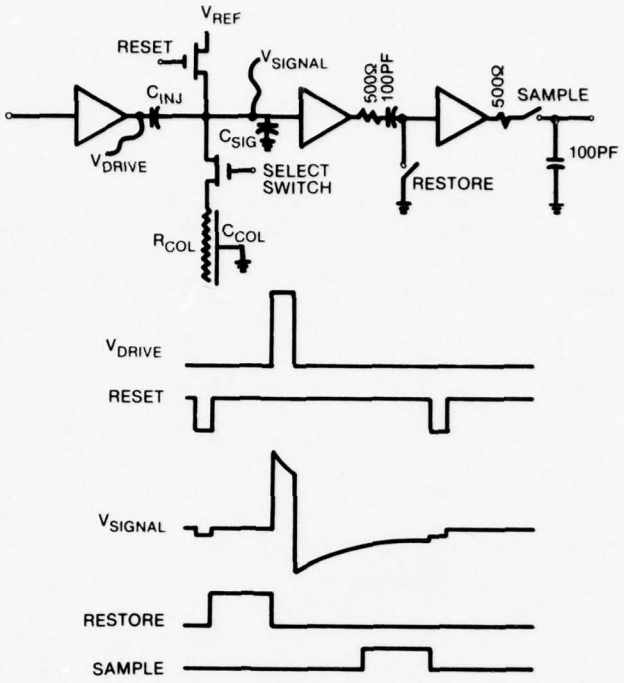


Figure 51. Video channel equivalent circuit after selection and basic readout waveforms.

to inject the signal charge. A second sample is then taken, after amplifier recovery from the injection overload, during the sample interval to extract a video signal that is proportional to the net injected charge.

The significant temporal noise sources are listed in Table 1. In this case temporal noise is dominated by the off-chip amplifier which was not designed for low noise. A dynamic range in excess of 1500 could be obtained if a low noise off-chip amplifier were built into this camera.

Pixel-to-pixel background variations were measured using the method described in Section 3.1.5. The sequential injection technique is very effective in rejecting fixed-pattern background noise. The peak signal-to-mean pixel-to-pixel background variation, excluding the column odd/even pattern, was measured as 960-to-1. The design of this random access imager, which incorporates separate video amplifier channels for the odd and even array columns, exhibits a relatively large odd/even column pattern noise. The measured peak signal-to-mean column odd/even pattern noise was 59-to-1. This design deficiency can easily be corrected with a chip re-design.

Pixel-to-pixel sensitivity variations were measured as described in Section 3.2. A mean pixel-to-pixel sensitivity variation of 0.22 percent was measured on the RA-128 using a flat field light box illuminated with tungsten lamps. The image was defocused to obtain the most uniform imager illumination.

TABLE 1. RA-128 TEMPORAL NOISE SUMMARY

Source	Spot Noise ($nV/Hz^{1/2}$)	Noise Voltage* (μv)	Effective Capacitance (pf)	Noise Carriers
Column Resistance (8K)	6.6	20.7	6.9	893
Column Select Switch (2.3K)	6.1	19.3	6.9	832
On-chip Source Follower	2.1	6.6	35.5	1464
Off-chip Amplifier	8.0	25.3	35.5	5613
			Root Mean Square	5928

Saturation Signal = 3.1×10^6 Carriers

Dynamic Range: Calculated 536

Measured 600

*Calculated for a noise bandwidth of 10^7 Hz, which includes correlated double sampling.

The image quality that was obtained with this device is illustrated in Figure 52 in which variations in the order of array addressing were made to demonstrate the random access feature.

4.1.2 Pre-Injection

The TN-2000 CID Camera utilizes a 244 row by 188 column array which is read out with a television compatible format using the Pre-injection read method. As described earlier in Section 1.2.2 a high speed scanner is used to multiplex the array column signals on to a pair of signal lines that are connected to low input impedance current amplifiers. This line scan operation resets the array columns to the amplifier reference voltage and, upon opening of each multiplex transistor, introduces a KTC offset on each column. The significant temporal noise sources encountered with this imager are column reset KTC noise, column select transistor Johnson noise, and preamplifier noise. The column lines in this array are aluminum which results in negligible distributed column resistance noise. Fixed pattern noise is rejected by reading each array row twice, with and without signal charge. One line of video delay is then used to extract a differential signal that is free of fixed pattern noise. This signal processing results in the rejection of fixed pattern noise at the expense of increased temporal noise. Table 2 lists the significant temporal noise sources, theoretical levels, and the measured performance.

Figure 52. Random access images with variations in array address order.

Fixed pattern noise encountered with Pre-injection Readout is primarily switching noise coupled directly from the high-speed column scanner to the video signal line. While the level of interference is high, it is readily rejected with the delay line canceller since it repeats line-to-line. Peak signal-to-mean pixel-to-pixel background noise has been measured as 250-to-1 after cancellation. Sensitivity variations of 0.3 percent were measured on the same array.

4.1.3 Row Readout

The FPP-128 imager, which was described in Section 3.1.5, has been used to evaluate the noise performance of the Row Readout technique. The equivalent circuit-after-row selection is shown in Figure 53. The significant temporal noise sources are listed

TABLE 2. TN2000 TEMPORAL NOISE SUMMARY

Source	Spot Noise ($nV/Hz^{1/2}$)	Noise Voltage* Current ($\mu V/nA$)	Effective Capacitance (pf)	Noise Carriers
Column KTC	---	---	21	1824
Column Select Switch (1.6 K)	5.1	6.1* V	21	793
Preamp Noise Current	---	0.5 nA	---	1761
			Root Mean Square	2656
		Line-to-line differencing for FPN cancellation (x 1.414)		3757

Saturation signal = 1.72×10^6 carriers

Dynamic range: Calculated 458

Measured 500

*Noise bandwidth = 1.4×10^6 Hz

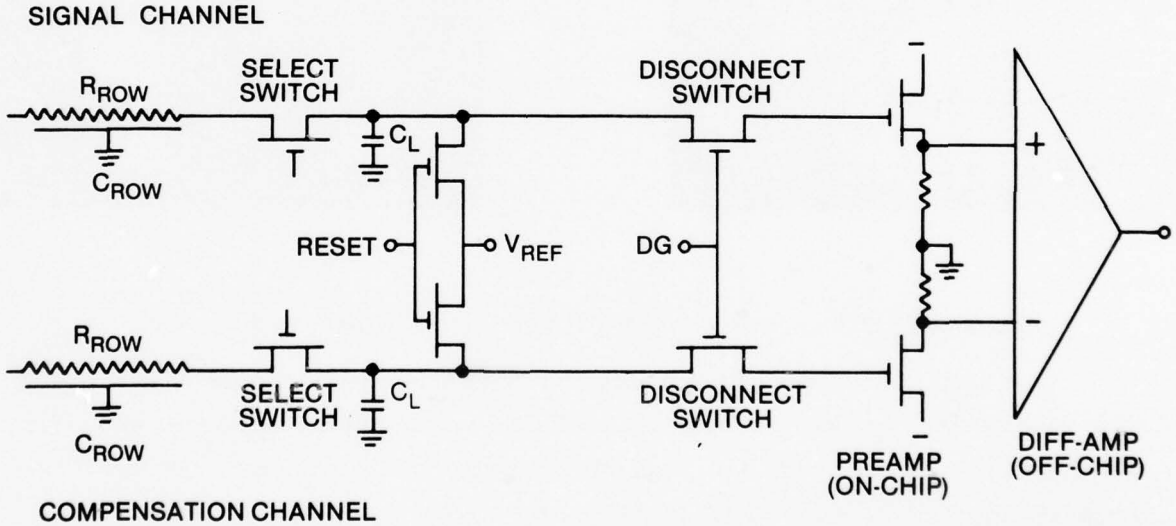


Figure 53. Row Readout equivalent circuit after selection.

in Table 3 along with the measured noise level. One of the most significant noise sources is the disconnect switch which was included to minimize amplifier overloading during the injection operation. This function can be implemented off-chip after some amplification to eliminate this noise source in future designs. In addition, a lower noise differential amplifier would improve performance. Note that all of the noise identified in Table 3

TABLE 3. FPP - 128 TEMPORAL NOISE SUMMARY

Source	Spot Noise ($nV/Hz^{1/2}$)	Noise Voltage* (μV)	Effective Capacitance (pf)	Noise Carriers
Row Resistance (5 K)	5.2	12.4	6.0	464
Row Select Switch (3 K)	7.0	16.6	6.0	624
Disconnect Switch (2.4 K)	6.3	15.0	10.4	975
Preamplifier	2.4	5.7	11.9	424
Differential Amplifier	5.7	13.5	11.9	1004
			Root Mean Square	1656
			Differential Noise (x 1.414)	2342

Saturation Signal = 1.5×10^6 Carriers

Dynamic Range: Calculated 640

Measured 500

*Noise bandwidth = 5.7×10^6 Hz including correlated double sampling

is Johnson noise, which is bandwidth dependent. The opportunity exists to achieve low temporal noise with this readout technique by reducing video noise bandwidth and operating at low pixel rates. The results of an experimental evaluation of low pixel rate image sensing is given in Section 4.3.

The fixed pattern noise performance of the Row Readout technique has been described in detail in Section 3.1.5.

4.2 PROCESSING GAIN VIA NON-DESTRUCTIVE READOUT

A series of tests was made on the FPP-128 imager utilizing a microcomputer as a processor/analyzer. This allowed precise measurement of noise levels and showed the reduction of temporal noise with multiple readings of the image using the unique nondestructive readout capabilities of the CID imager.

The test system included a television camera designed to run the FPP-128 imager in a two frame-per-second raster scan mode, a high-speed 12-bit analog-to-digital converter and a Cromemco Z-2 microcomputer for analyzing the digitized video data. The microcomputer contained a 4 MHz Z-80 microprocessor, 56 kilobytes of static RAM, 8 kilobytes of PROM, two RS 232 serial I/O ports, and six programmable parallel I/O ports.

A board was also designed and assembled to read the processed video data directly out of memory, through an eight-bit digital-to-analog converter, and display it on a television monitor at 60 frames per second.

Assembly language programs were written which synchronized the timing of the A/D converter with that of the camera, stored the video data, processed this data, and formatted the data in memory for display on the television monitor. One such program performed a histogram analysis of the pixel brightness levels of an image stored in memory. The 128 pixel x 128 pixel x 8-bit image is stored in one 16 kilobyte block of memory, and the histogram data is computed and stored in another 16 kilobyte block of memory from which it can be displayed graphically on the television monitor as seen in Figure 54. The horizontal axis is the grey level with the left side signifying a grey level of zero or black and the right side a grey level of 255 or white. The vertical axis displays the number of elements of the image at the corresponding grey level. The image itself or the brightness distribution may then be displayed on the monitor.

The purpose of the test for this study was to find out if the effects of the dominant temporal noise sources could be reduced through an average of multiple reads of the same image, and, if reductions are possible, to what extent are they possible and what are the limitations to further reductions. This assumes that the noise sources are independent from one reading to the next, such as shot noise or Johnson noise, as opposed to correlated noise, such as thermal drift of the camera circuitry.

The procedure used to accomplish this task was as follows. The imager was housed in an evacuated, LN_2 Dewar so that it could be cooled to about 77 ^{o}K to eliminate dark current. The imager was read out in a raster scan mode with a frame time of about 0.5 second so that the A/D converter and computer program could maintain synchronism. An average of a 2^N (N = 1,2, . . .7) readings of signal plus background (fixed pattern noise) minus an average of 2^N readings of background alone could be made, leaving only signal plus temporal noise. This was done by summing 2^N successive frames of a 128 pixel x 128 pixel by 12 bit image negatively in memory with the lens closed down, the result being truncated to 16 bits when necessary. After a snapshot image was taken where a controlled amount of light entered the imager, the lens was closed, and the image read out nondestructively 2^N times and summed positively with the accumulated background. The result was again truncated to 16 bits. The upper eight bits or the lower eight bits of the resulting image could then be displayed on the monitor or analyzed with the histrogram program.

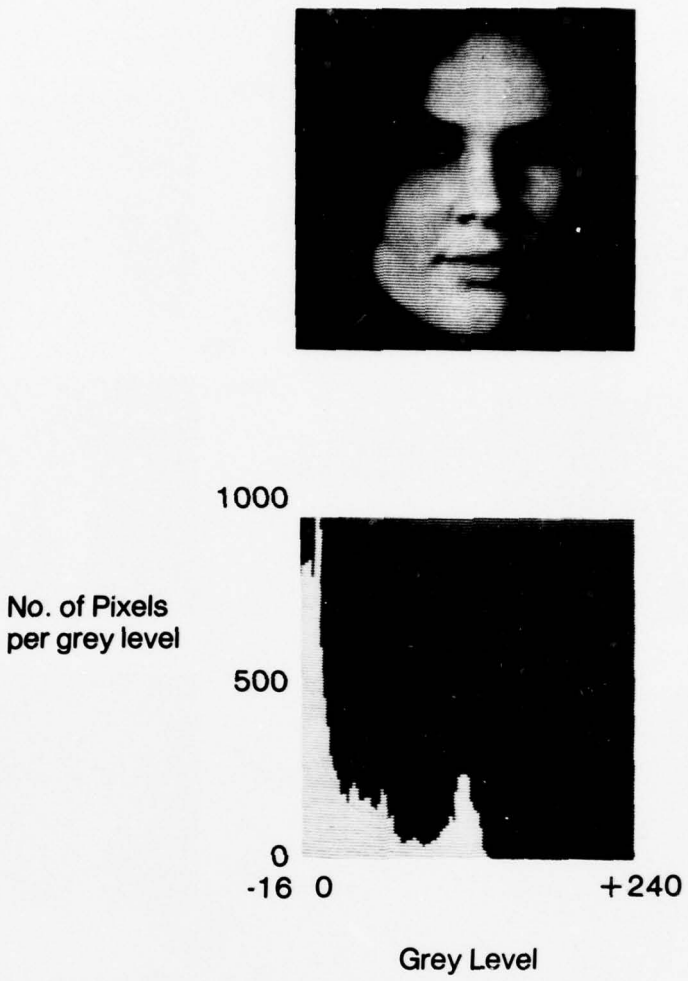


Figure 54. Typical image and its brightness histogram.

The first test utilizing this procedure was performed to verify that the temporal noise level of the average of a number of readings would decrease by $\sqrt{2^N}$ as the number of readings increased by 2^N, as would happen with Gaussian-distributed noise such as Johnson noise. The series of pictures shown in Figure 55 display the results. The pictures shown on the left are of the least eight significant bits of the difference between an average of 2^N images with the lens closed minus another average of 2^N images with the lens closed which yields a picture of the temporal noise. The pictures on the right are of the corresponding histograms. A bias was added to the picture in order to center the histogram. Also, the absolute scale of the vertical axis of the histogram was changed from one picture to the next in order to normalize the curves to a constant peak value.

The Gaussian nature of the noise is shown by the bell-shaped distribution of the histogram. As the number of readings was increased the standard deviation (or the RMS

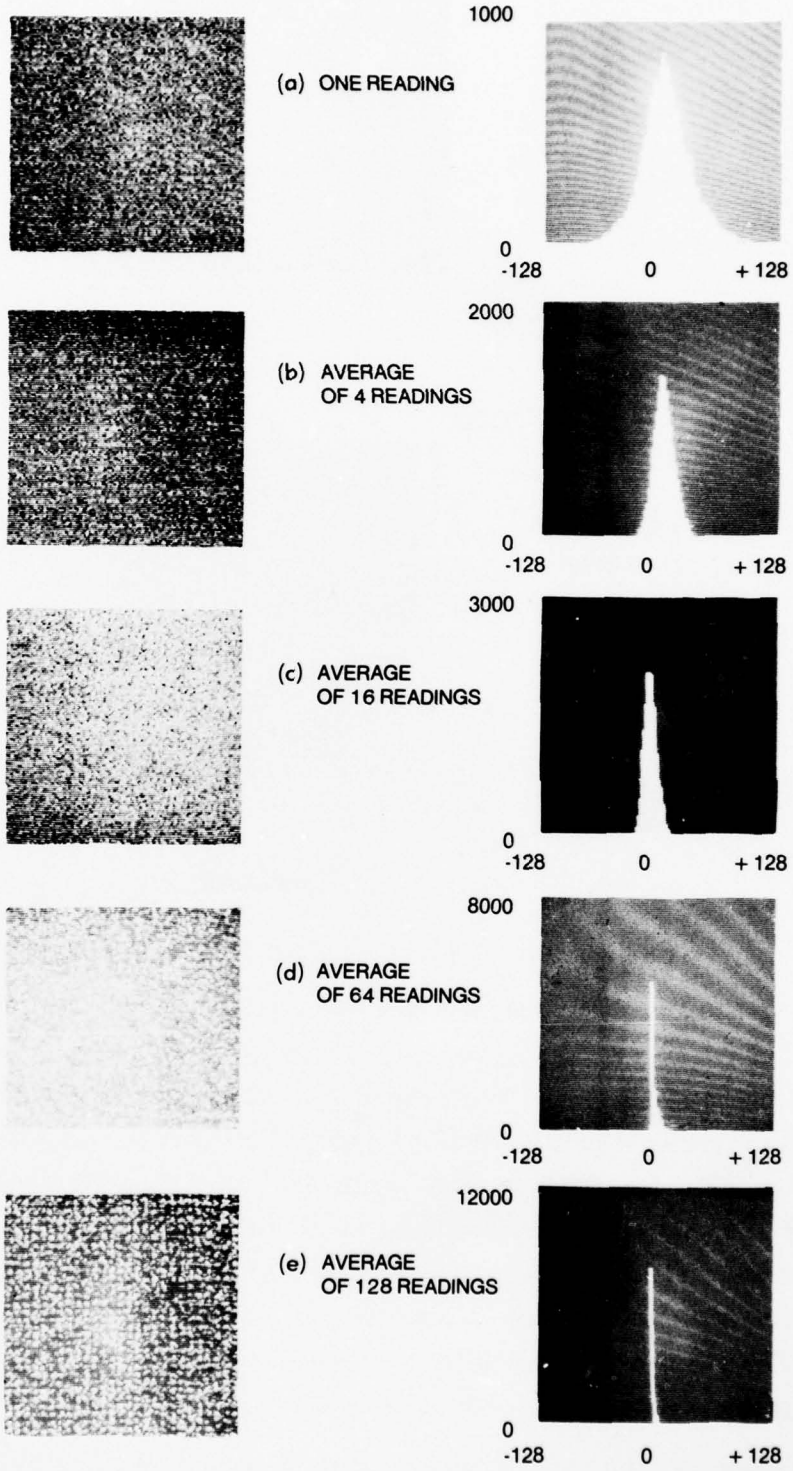


Figure 55. Reduction of temporal noise through averaging multiple non-destructive readings.

noise) of the curves decreased as expected, with the 128-reading picture approaching a single grey level. The pictures and histograms for 64 and 128 readings show a tendency for bright spots. This was later found to be due to an occasional pulse of noise external to the camera coupling into the video.

If this bright spot effect is removed, it is seen that the method of averaging a large number of successive non-destructive readouts of a shuttered CID imager could be a useful method or reducing the noise level of an image so that low light level scenes which are buried in the noise could still be recovered, thus providing a greatly improved dynamic range. To test the extent of the improved dynamic range, a series of images were analyzed with the light level continually decreasing until the image became lost in the noise. Then the number of readings was increased to bring the picture out of the noise. A subset of these pictures and their corresponding histograms are shown in Figures 56, 57, and 58.

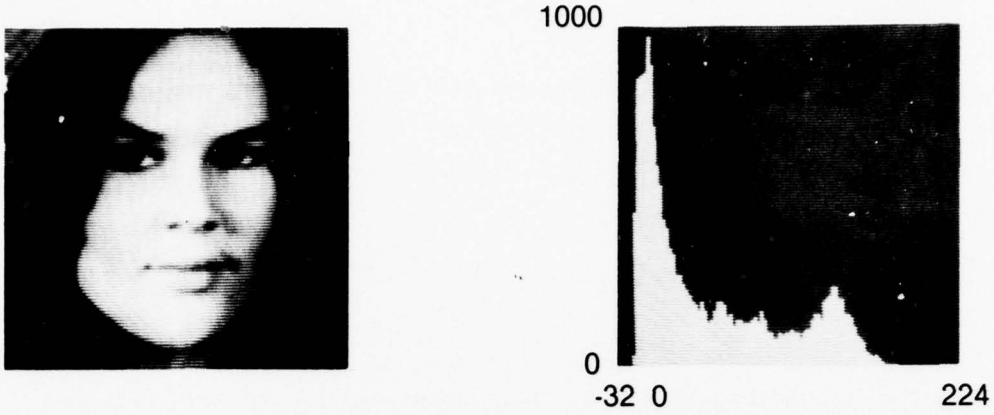
Figure 56(a) shows a picture with light level in the bright areas of about 3/4 of saturation level. The eight most significant bits of the 12-bit image are displayed. Figures 56(b) and 56(c) show 1/8 and 1/32 brightness (where saturation = 1) and their histograms. For Figure 56(c) and subsequent pictures the camera gain was raised by a factor of four to make full use of the A/D converter's range.

For Figure 57 the brightness level has been cut down using neutral density filters to 1/160 of full scale. In this series the eight least significant bits of the 12-bit image are shown, and a bias was added to center the histogram. Figures 57(a), (b), and (c) show the noise level is reduced while maintaining the signal level using the method of averaging multiple readings.

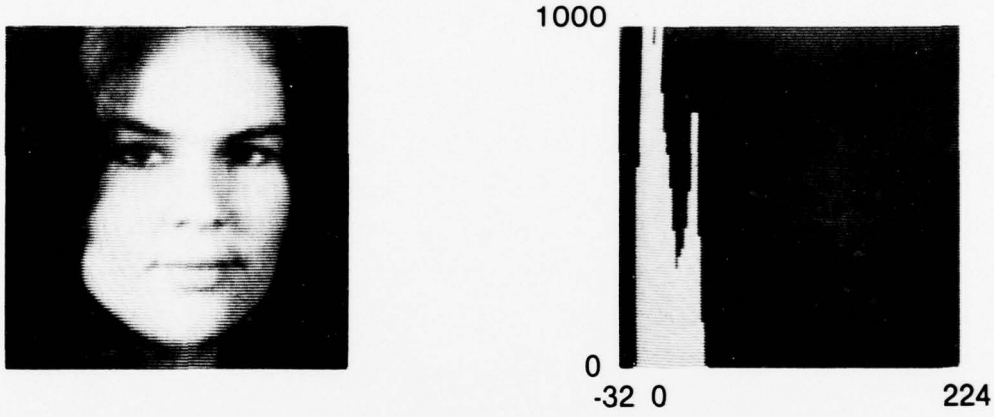
For Figure 58 the image brightness level was cut another factor of four giving a brightness level of 1/640. Again the image was brought out of the noise using the multiple readout technique.

The results of these experiments show that the method of averaging successive non-destructive readouts of the CID imager is successful in decreasing the temporal noise and thereby increasing the dynamic range of the imager. The limitations of this method were not reached as the number of bits of resolution of the analog-to-digital converter limited the extent of improvement possible as the noise level was decreased to less than one quantization level [Figure 56(c)]. It was shown that the dynamic range was increased well above the initial value of 500:1.

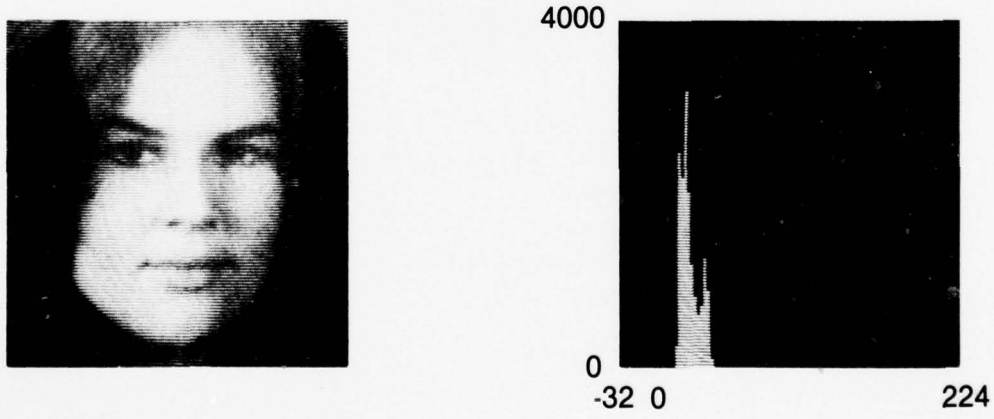
Following completion of this study a letter was received from Dr. Roger Lynds of Kitt Peak National Observatory in Tucson, Arizona. In using the CID imager for stellar



(a) LIGHT LEVEL = 3/4 SATURATION

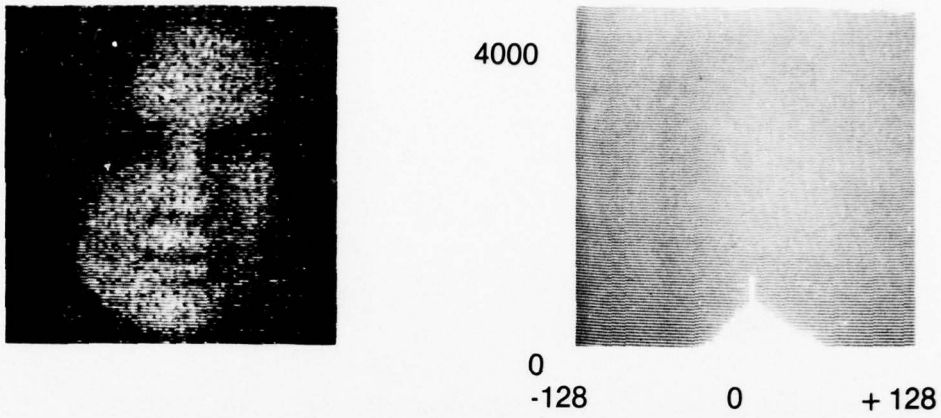


(b) LIGHT LEVEL = 1/8 SATURATION

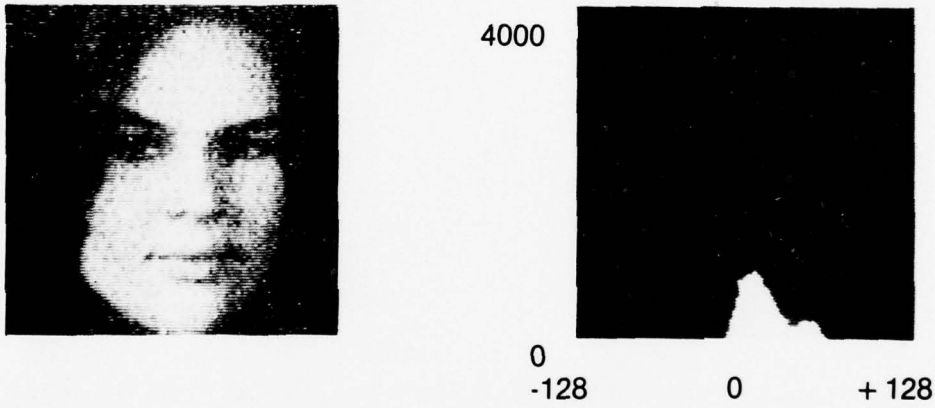


(c) LIGHT LEVEL = 1/32 SATURATION

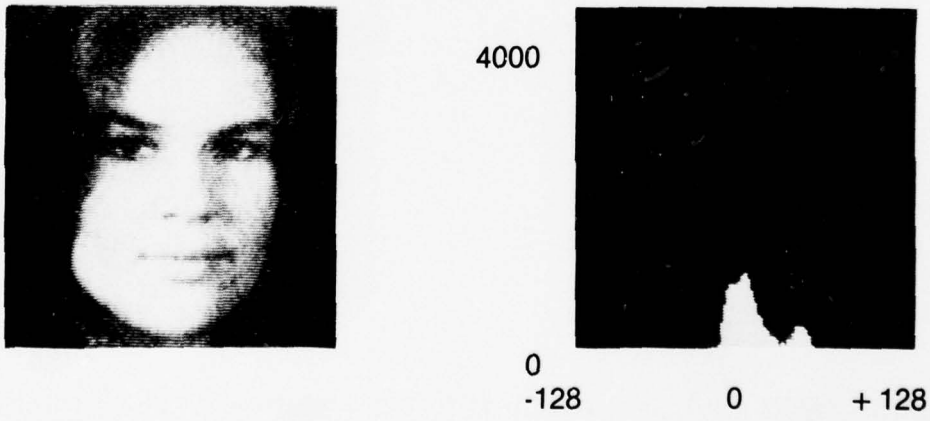
Figure 56. Images and their histograms with decreasing light level.



(a) BRIGHTNESS LEVEL = 1/160 SATURATION: ONE READING

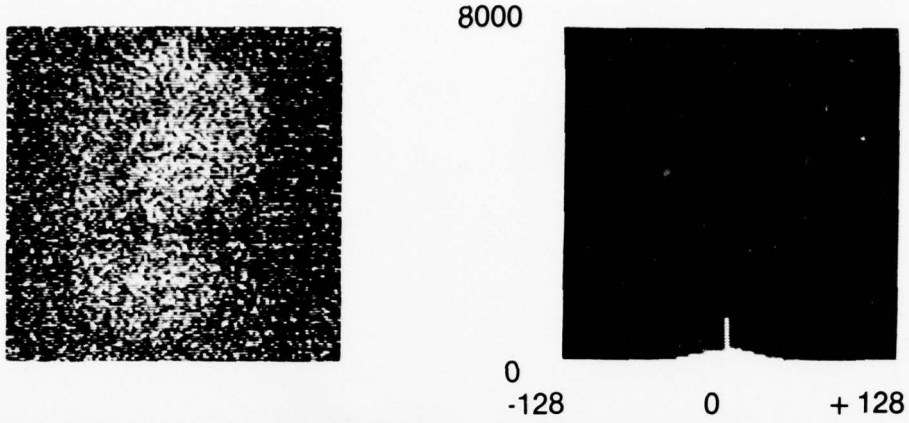


(b) BRIGHTNESS LEVEL = 1/160 SATURATION: AVERAGE OF 4 READINGS

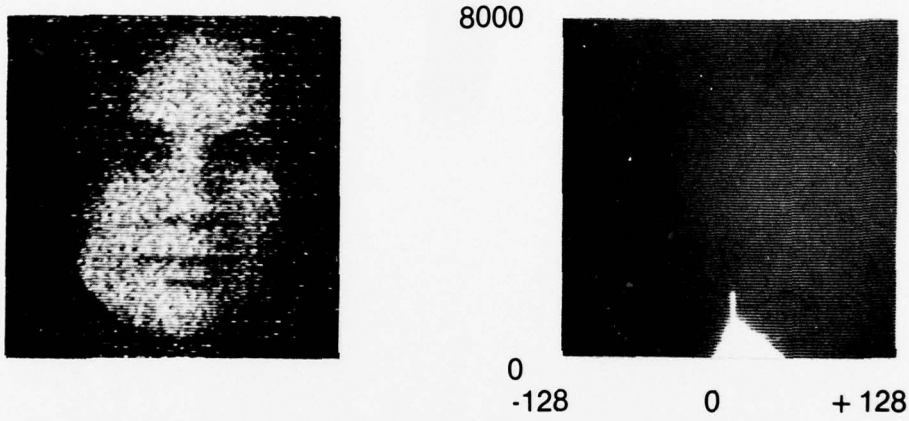


(c) BRIGHTNESS LEVEL = 1/160 SATURATION: AVERAGE OF 16 READINGS

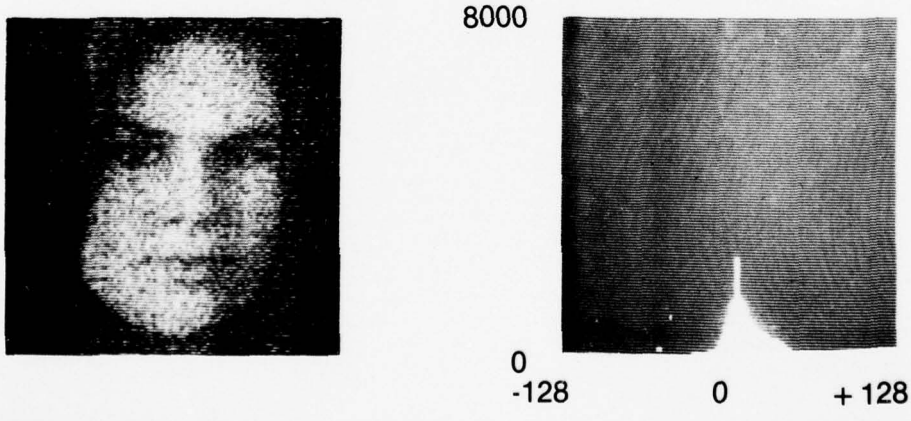
Figure 57. Improvement in signal-to-noise by averaging multiple non-destructive readouts.



(a) BRIGHTNESS LEVEL = 1/640 SATURATION: ONE READING



(b) BRIGHTNESS LEVEL = 1/640 SATURATION: AVERAGE OF 16 READINGS



(c) BRIGHTNESS LEVEL = 1/640 SATURATION: AVERAGE OF 64 READINGS

Figure 58. Improvement in signal-to-noise by averaging multiple non-destructive readouts.

observation and spectral measurements, he is using the average of multiple readings method with a 14-bit A/D converter to increase the dynamic range to over 100,000-to-1. The limitation encountered at Kitt Peak was the sporadic generation of charge from an external radiation source believed to be high-energy cosmic rays.

4.3 LOW-FREQUENCY OPERATION

The dominant temporal noise encountered with Row Readout at high video rates is from Johnson noise sources (resistors, switches, field effect transistors). As the operating frequency is reduced, noise bandwidth can be narrowed with a reduction in Johnson noise proportional to the square root of bandwidth. At lower rates, however, low frequency excess noise (1/f noise) and leakage current begin to interfere with the sensing operation. It would appear that these low-frequency noise effects would dominate below some video rate and limit the improvement that could be achieved with this approach. This is not the case. There is a strategy that allows these low-frequency effects to be circumvented and the effective noise bandwidth to be reduced with, at this writing, no known limit. The strategy is to choose the imager operating frequency for lowest noise, somewhat above the point where low-frequency effects become significant, and then use multiple nondestructive readout operations and external signal summation to further reduce the effective noise bandwidth. Since signals sum coherently and uncorrelated noise incoherently, the effective noise is reduced in proportion to the square root of the number of non-destructive readout operations. This strategy is effective in reducing all temporally un-correlated noise including Johnson noise, KTC noise, charge transfer noise, and leakage current shot noise.

An experimental evaluation of low video rate noise, both temporal and fixed pattern noise, was performed under NASA sponsorship [36]. The results of this evaluation are included here because they demonstrate an important characteristic of the noise behavior of CID imagers.

One method used for space vehicle attitude pointing and stabilization is to track optically the position of one or more stars. The random access capability of CID imaging combined with low noise at low-readout rates result in an attractive sensor for this class of applications. The FPP-128 array was operated in a track mode in which a sub-array

[36] Design, Fabrication and Delivery of a Charge Injection Device as a Stellar Cracking Sensor, Contract No. NA58-32801. Final Report.

of 16 pixels was read out, ten times per second. Low noise junction field effect transistors were used as the preamplifier first stage to minimize 1/f noise. The imager was operated at a pixel rate of 24 kilohertz (4-6 kHz channels in parallel) and 64 non-destructive readouts of each pixel were summed after amplification and analog-to-digital conversion. The sub-array was read out twice each frame to allow the fixed pattern noise to be cancelled. The resulting temporal and total noise (temporal plus fixed pattern noise) is shown in Figure 59 as a function of temperature. The slight increase in total noise at higher temperatures (+25 ^{o}C) is caused by spatial variations in dark current across the array. Shot noise on this dark current can be seen on the temporal noise plot. At -40 ^{o}C fixed pattern noise introduced by some uncontrolled outputs of the particular scanner used with this array increases. This effect could be avoided in an array designed specifically for this application.

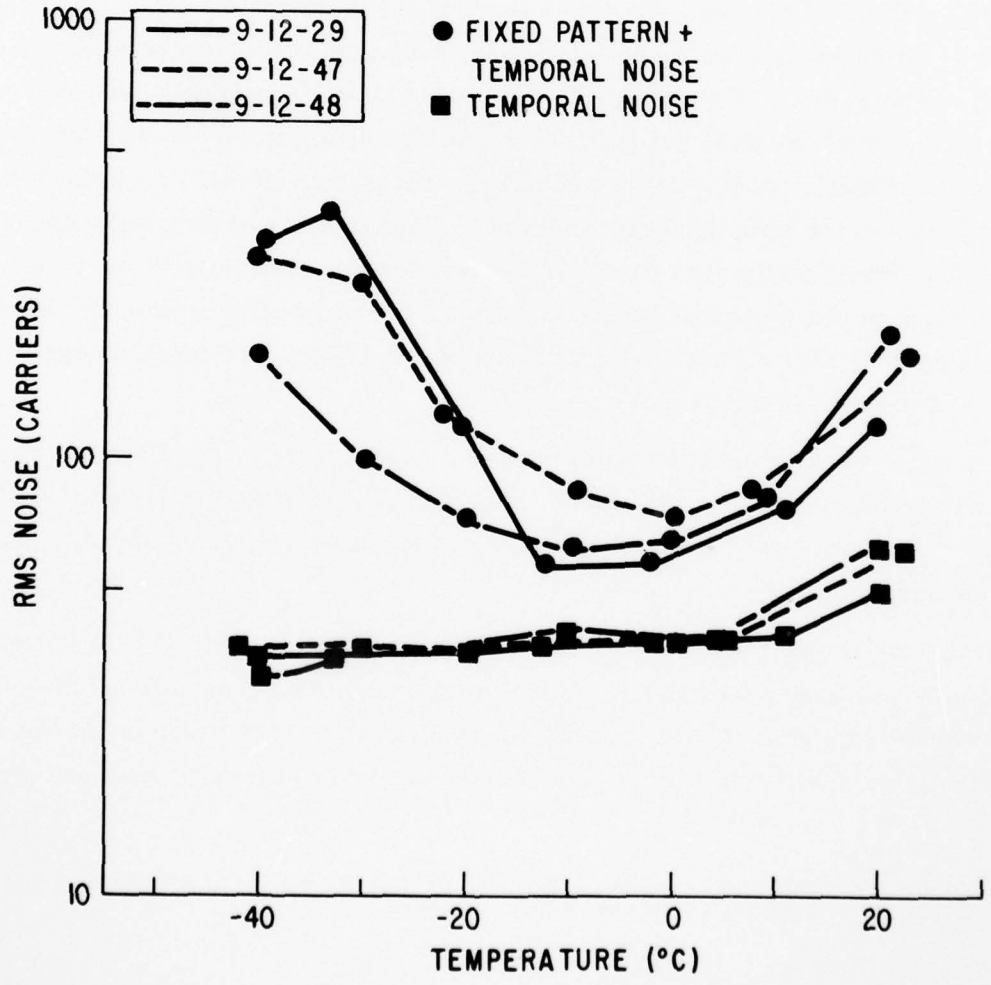


Figure 59. Low-video-rate temporal and total noise versus temperature.

The important result of this experimental evaluation is that temporal noise levels of 40 carriers and total noise levels of 60 carriers were achieved at moderate temperatures (0 ^{o}C). In addition, a number of deficiencies in the experimental array were identified that, if corrected, would result in even lower noise levels.

4.4 PERFORMANCE PROJECTIONS

The temporal and fixed pattern noise levels of existing CID imagers employing three of the most useful readout techniques were theoretically and experimentally evaluated (see Section 4.1). This evaluation revealed the limiting noise sources in these devices, thus providing the information necessary for performance optimization. For instance, the Johnson noise contributed by the distributed resistance of the array lines can be minimized through the use of metal strapping, select switch resistance can be minimized with the proper choice of transistor topology; and the amplifier can be optimized as described in Section 2.3. Fixed pattern noise can be minimized by employing sensing site layouts that are insensitive to registration errors, and symmetrical array line addressing structures. Finally, array structural uniformity can be improved and signal sensing capacitance load can be minimized by using modern fine line lithographic fabrication techniques.

Since CID imager performance is a strong function of application requirements, such as array size and operating rates, performance has been projected for imagers structured for three prime application areas: television sensing, automation, and tracking.

A 488 line by 388 element television sensor employing differential Row Readout at standard NTSC operating conditions has been analyzed. The peak signal-to-rms temporal noise is projected to be in excess of 900-to-1. Uncorrected fixed pattern noise should be below 1/2 percent of full scale and be easily corrected to below the temporal noise level.

One major problem encountered in applying machine vision to automatic inspection, measurement, and control of industrial processes is the large mismatch between normal imager data rates and the computational speed of microprocessors. The random access CID image sensor with nondestructive readout would eliminate the need for a large, high-speed buffer memory between the image sensor and processor and also eliminate the high-speed data sorting that is now required in this class of equipment. A 256 by 256 random access array incorporating a 20 micron square sensing site has been analyzed to predict noise performance for this application. A basic pixel rate

of 650 kilohertz has been chosen to allow the full frame to be read out at ten frames per second. More typically, subsets of pixels would be addressed at a much higher sub-frame rate. This sensor would be designed to operate in two modes, Sequential Injection for truly random scan and transfer readout (Row Readout) for nondestructive readout.

The signal-to-temporal noise ratio would exceed 1000-to-1 under both readout conditions. The signal-to-fixed-pattern noise ratio would exceed 1000-to-1 with Sequential Injection readout and 200-to-1 under nondestructive readout conditions.

A 400 by 400 array configured for star tracker operation has been analyzed during the NASA contract referred to earlier [36]. Under tracking conditions, at a read rate of 160 pixels per second, a temporal noise level below 25 carriers rms should be achieved. Fixed pattern noise would be suppressed below the temporal noise level.

Section 5

CONCLUSIONS

Temporal and fixed pattern noise levels in CID image sensors are a strong function of operating conditions such as video rates and the readout technique used. The basic temporal noise sources are Johnson noise in array distributed conductors, multiplexer selection switches, transistor amplifiers, and KTC noise. Johnson noise sources are usually dominant in large arrays operating at standard television rates. Shot noise in array dark current and multiplexer junction leakage current become significant at low video and frame rates. Measured noise levels ranged from 60 carriers rms at low video rates to a few thousand carriers for TV compatible devices.

Amplifier input noise charge was unaffected or degraded by the use of negative feedback. Buried channel MOSFETs offer marginal improvement in low-frequency (1/f) noise but only over a narrow frequency range.

One of the more significant results of this study has been the demonstration of dynamic range extension through the use of multiple nondestructive readout operations and off-chip signal summation. This technique is effective in suppressing all temporally uncorrelated noise, such as Johnson noise in amplifiers and switches, KTC noise, charge transfer noise, and leakage current shot noise.

The basic sources of fixed pattern noise are array threshold voltage variations, which result in a spatial variation in bias charge; structural variations, such as interlevel dielectric thickness and conductor patterning variations; spatial dark current variations, and switching noise. The various readout methods vary in their sensitivity to fixed pattern noise. The Sequential Injection Readout Method results in a high degree of fixed pattern noise suppression. The Pre-injection Readout technique is dominated by switching noise, which can be readily cancelled with off-chip signal processing, and Row Readout is most sensitive to array variations.

A source of both temporal (shot) and fixed pattern noise is array dark current and the spatial variation in this dark current. The CID structure exhibits very low dark current because only a fraction of the photosensitive area contributes dark current and the interface states that contribute surface leakage current can be continuously quenched.

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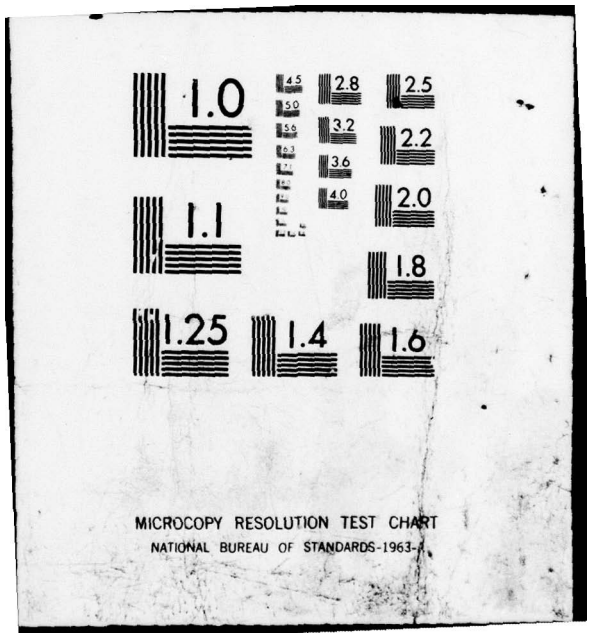
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