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RELIABILITY STUDY OF MICROWAVE POWER TRANSISTORS UNDER TRANSIEN--ETC(U)
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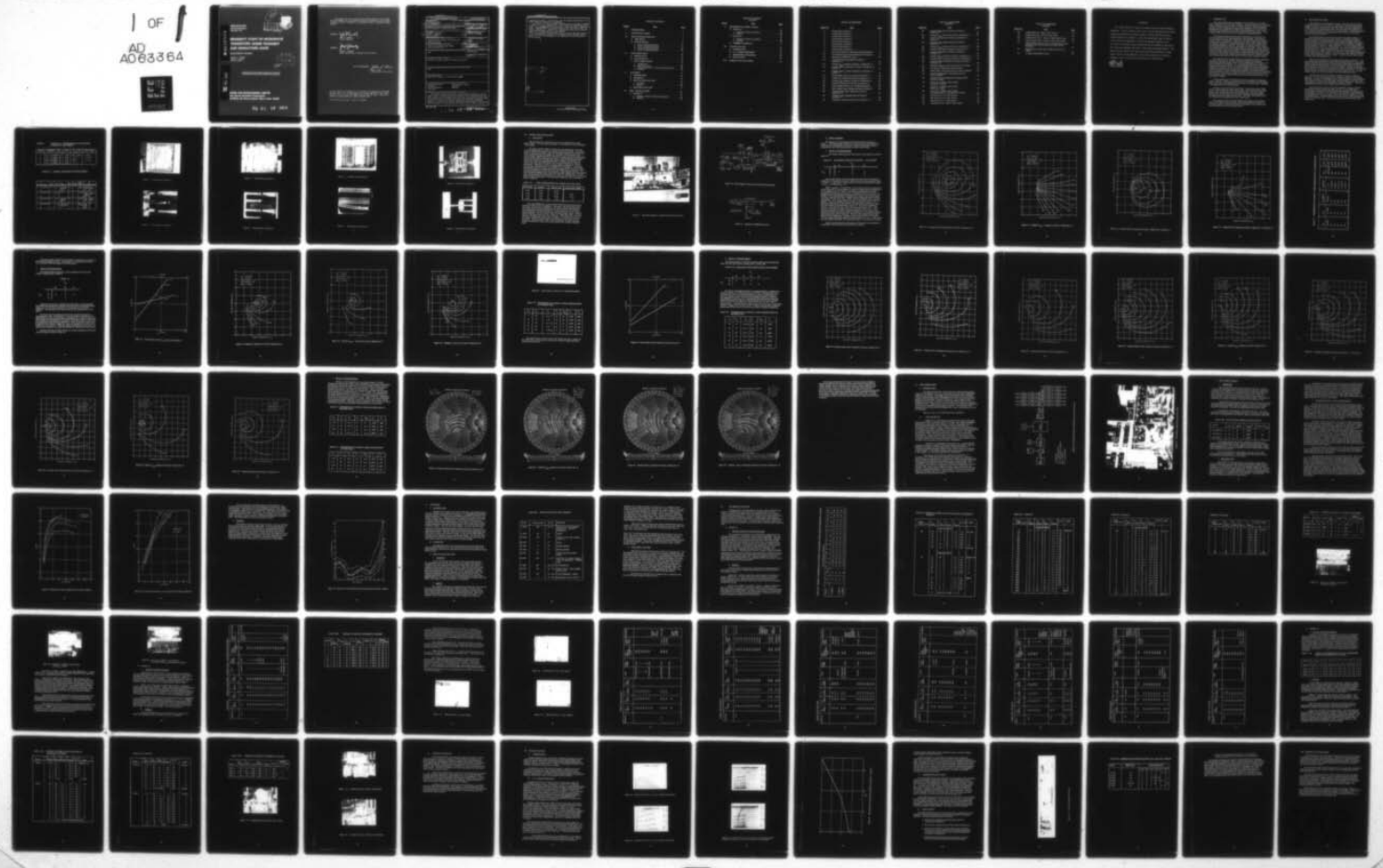

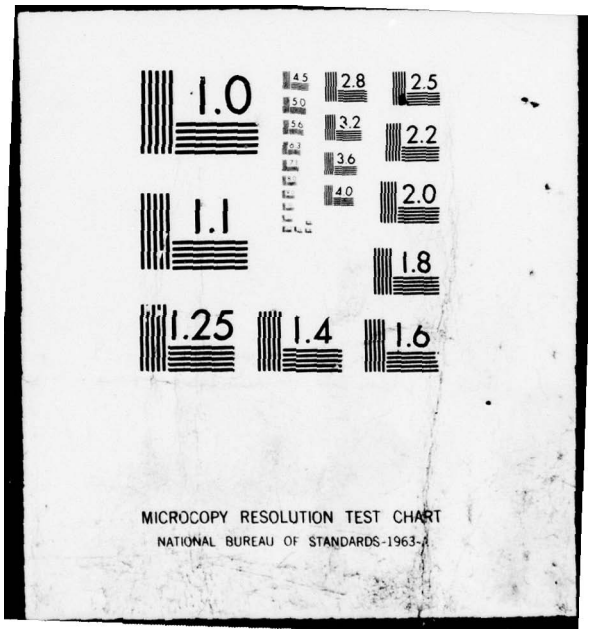
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RADC-TR-78-226
Final Technical Report
November 1978

LEVEL II

RELIABILITY STUDY OF MICROWAVE TRANSISTORS UNDER TRANSIENT AND MISMATCHED LOADS

General Electric Company

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Life Tests	

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report presents the results of study of the reliability of current state-of-the-art transistors under non-ideal conditions, including output mismatch, excess collector voltage, and error drive. Four different device types were characterized to determine their electrical performance and junction temperature as a function of collector voltage, drive, and output impedance. Samples of the devices were taken to destruction under extremes of these variables and analyzed. It was observed that failure occurred when the junction

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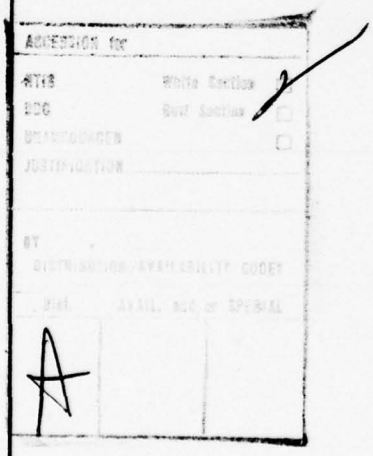
temperatures exceeded a critical value, with the variables giving rise to the excess temperature making little difference.

Life tests of one device type were carried out with the collector voltage in excess of the $V_{CBD/2}$ nominal value. Little evidence of degradation was observed. Most devices failed catastrophically a short time after a temperature change. There was little correlation between the hot cell and the cell location of maximum damage. Some DC device degradation, which could be cured by baking at an elevated temperature, was observed.

It was concluded that catastrophic failure observed under high collector voltage conditions was probably due to mechanical defects (cracks, lifted metal, etc.) which were propagated in the temperature cycling environment of the life tests.



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EVALUATION

This report describes a study of microwave transistors under overstress conditions. From the results of the study it can be concluded that collector voltage and mismatch are the major causes of failure with failure being rather insensitive to overdrive. Due to the catastrophic type of failure, it was difficult to determine if failure was caused by defects in the transistor die although lifting of metallization was observed on one device. This study was performed under TPO-5, "Solid State Device Reliability." The results of the study will be used in the reliability prediction for these types of devices in MIL-HDBK-217C, "Reliability Prediction of Electronic Equipment," and in reliability specifications for these devices.

JOHN F. CARROLL
Project Engineer

I. INTRODUCTION

This report describes an investigation of the reliability of microwave power transistors under non-ideal conditions. Previous studies (1, 2) concerned with the evaluation of similar devices under conditions of rated input power, nominal collector voltage and matched output impedance, have indicated that degradation can be expected as a result of electromigration, or as a result of emitter-base shunting by metal movement along the silicon surface. Both of these effects were found to occur in aluminum metallized devices.

The actual conditions that microwave transistors are subjected to in systems applications can vary significantly from the ideal. For instance, the input power to an amplifier module may vary significantly from module to module because of variations in coupling or line loss. In most applications, the amplifier modules are multistage modules in which there is little control on interstage impedance matching. Therefore, the output mismatch of the first stage transistors can deviate appreciably from the ideal. This situation can be aggravated further as the output transistors degrade. Finally, while the collector voltage can be well controlled, in some applications it is deliberately raised above the nominal value in order to obtain increased output power. This is common in short-pulse communication systems where the collector voltage may be significantly greater than half the collector base breakdown voltage.

The objective of the present study was to evaluate the effect of excess input power, high collector voltage, and output mismatch on the failure mechanisms observed in state-of-the-art microwave power transistors. The work consisted of three phases: (1) a characterization phase in which the electrical and thermal behavior of several different devices were measured as a function of mismatch, drive, and collector voltage; (2) a step/stress phase in which several devices of one type were subjected to increasing levels of drive and collector voltage to determine the levels at which failure or degradation occurs within a short time; (3) a phase in which life tests were carried out on this same type of device under fixed conditions of junction temperature, drive and collector voltage.

Failure analysis of all the failed devices was conducted to assess the cause of failure. Finally, several devices (of three types) were deliberately failed under controlled conditions in an attempt to relate the cause of failure to the appearance of the failed samples.

Overall, four device types were studied. Two of these were L-band devices in the 50-100 watt power output range, another was a 100 watt UHF device, and the fourth was a six-watt S-band device. One of the L-band devices (No. 2) was selected as the prime test subject on this program — the subject of the step stress and life tests. The other three devices were characterized for comparison with the L-band device.

The results of each of the three phases of the study are described in detail in the following three sections: Section VI describes the results of the failure analysis. Section VII contains a discussion of the results of the overall program and the conclusions derived.

II. THE DEVICES STUDIED

Four transistors were selected for study. These devices are medium to high-power parts for use at UHF, L, and S-band. Since the devices were designed to operate over different frequency bands, they differ considerably in their geometry, packaging and size. Thus, the intent of the selection is not to compare directly devices from the various vendors. Instead the devices were selected because they represent state-of-the-art devices with wide potential military application.

The RF performance of the devices tested is presented in Table I. A summary of the physical features of the devices is presented in Table II. Two L-band devices of approximately the same power capability, and from different vendors, were tested. Both of these parts are capable of developing 100 watts under short pulse ($\sim 50\mu s$) operation and 50 to 60 watts at longer pulsed operations. Device 1, shown in Figure 1 , is a gold-metallized device that uses 28 cells in an in-line configuration. The device has input and output matching and uses a single emitter and base wire to serve a pair of cells. The cell geometry, shown in Figure 2, is basically an interdigitated design with emitter sites served by 11 fingers. The active area is 38.4 square mils/cell. Emitter finger ballasting is thin film metal. A gold-refractory metal system is used for the chip metallization.

The second L-band device tested (Device 2) is shown in Figure 3 . The gold-refractory metallized device has input and output matching. Two stages of input matching are provided, while the collector capacitance resonates with inductors that are partly printed. The base transistor is wired to a bridge that is connected to ground via holes in the substrate. Individual flying leads serve each cell. The active area of each cell, shown in Figure 4, is 43 sq. mils Twelve cells are combined for a total active area of 516 sq. mils. The fifty emitter fingers per cell are ballasted in pairs by diffused resistors.

The UHF device (Device 3) that was evaluated is shown in Figure 5 . The device is a 100-watt long pulse part, designed to operate in the 420-450 MHz band. Again the interdigitated device is gold-refractory metal metallized. The transistor active area of 1800 square mils is divided into 24 cells. The cell geometry is shown at high magnification (100X) in Figure 6 . Twenty-five independently ballasted emitter fingers feed the emitter sites.

The S-band device (Device 4) that was evaluated is shown in Figure 7 . The device is rated to deliver six watts over the 3.1 to 3.5 GHz band. Several stages of sophisticated matching networks transform the input and output impedance to 50 ohms. The transistor is an eight cell, in-line chip with a single base wire serving cell pairs. Each cell, shown in Figure 8, is of the interdigitated type. No finger ballasting is used on the 10 emitter fingers that serve the cell emitter sites. The total active area of the eight cells is 90 square mils.

TABLE I. TYPICAL R.F. PERFORMANCE OF THE DEVICES AS RATED BY THE VENDOR

Device	Frequency	V_{cc}	Gain	P_o	Eff	Pulse Length
1	1.2 - 1.4 GHz	32	7 dB	100	45%	$\leq 50\ \mu s$
2	1.2 - 1.4 GHz	28	7 dB	55		$\leq 2\ \mu s$
3	420 - 450 MHz	31	8 dB	100		$\leq 6\ \mu s$
4	3.1 - 3.5 GHz	28	6 dB	6		

TABLE II. PHYSICAL FEATURES OF DEVICES TESTED

Device	Geometry	No. of Cells	Cell Size	Cell Configuration	Active Area	Emitter Fingers	Emitter Finger Ballast	Matching	Metallization
1	Interdigitated	28	9.6 × 4.0	In-line single emitter wire serves two cells	1075	11	Thin film metal	2 stage & collector shunt	Au & refractory metal
2	Interdigitated	12	17.2 × 2.5	In-line	516	50	diffused	2 stage input & printed collector shunt	Au & refractory metal
3	Interdigitated	24	25 × 3.0	Quad single base wire serves four cells	1800	25	diffused	Input single stage	Au & refractory metal
4	Interdigitated	8	4.5 × 2.5	In-line single base wire feeds cell pair	90	10	Not ballasted	Multi-stage input and output	AL

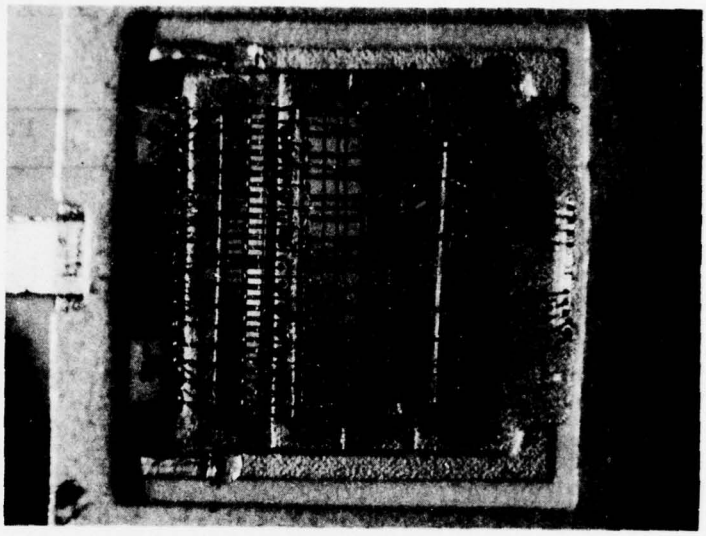

Figure 1. Overall View of Device 1

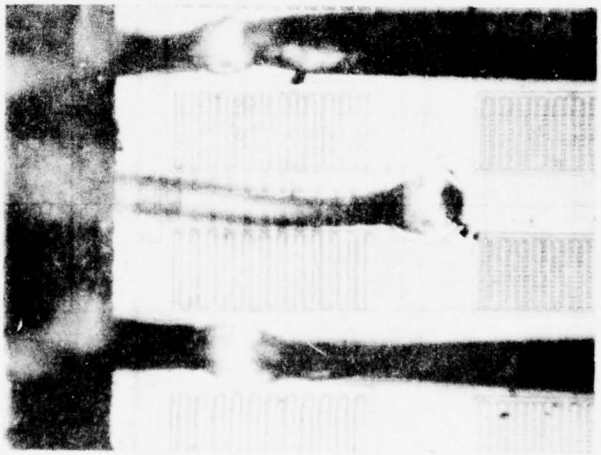

Figure 2. Cell Geometry of Device 1

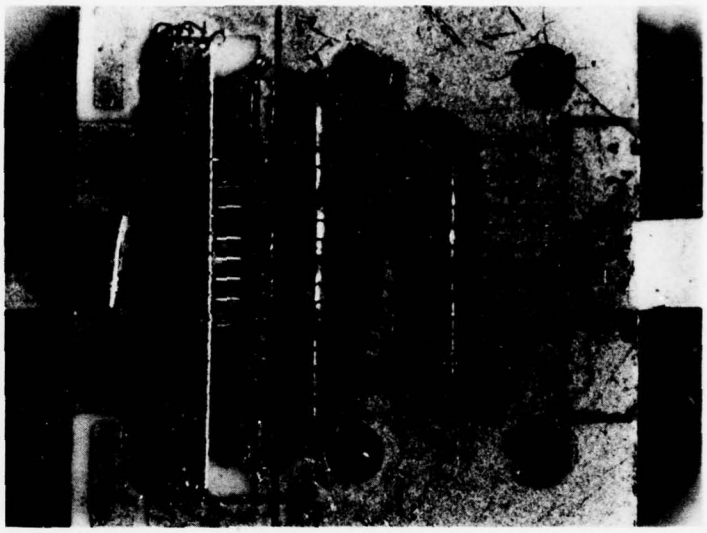

Figure 3. Overall View of Device 2.

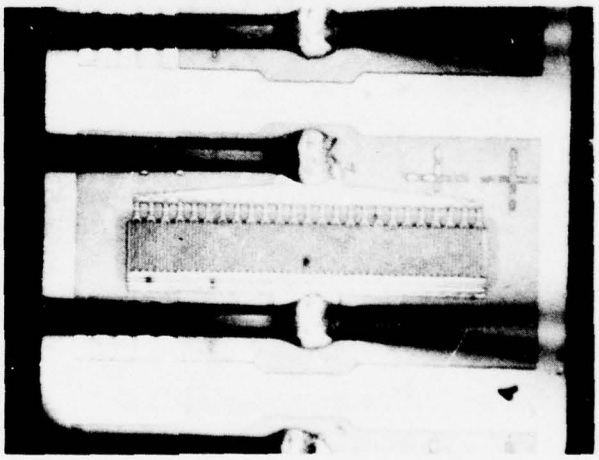

Figure 4. Cell Geometry of Device 2.

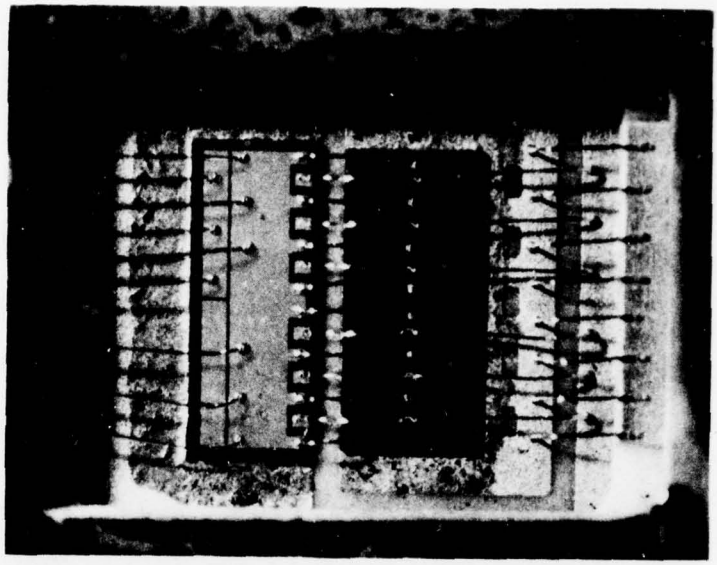

Figure 5. Overall View of Device 3.

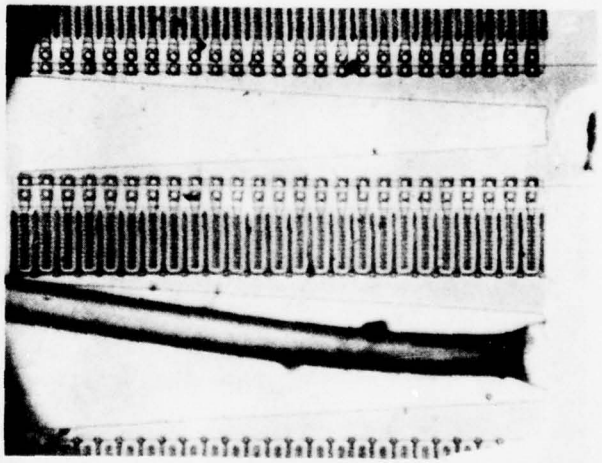

Figure 6. Cell Geometry of Device 3.

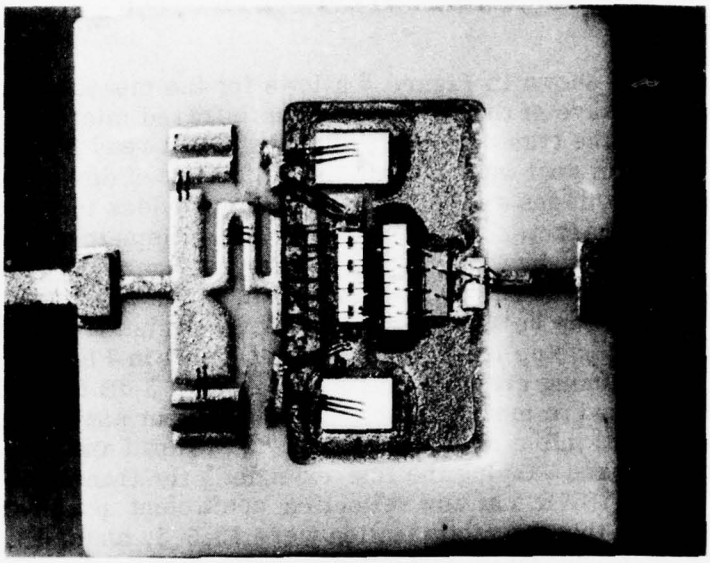

Figure 7. Overall view of Device 4

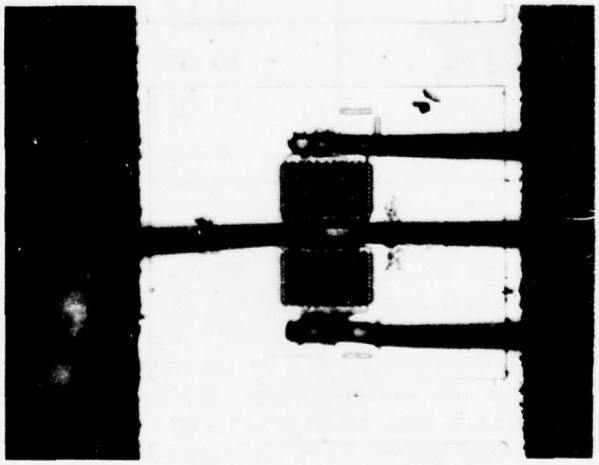

Figure 8. Cell Geometry of Device 4

III. DEVICE CHARACTERIZATION

A. TEST SETUP

The method used to characterize devices was developed on another RADC contact. It is described here again, in some detail, for the convenience of the reader.

The setup, shown in Figure 9 allows for the measurement of the peak junction temperature of the device using an infrared microscope. The microscope is used in the transient mode with the output read from an oscilloscope. Since the program goal was to study the reliability of devices under high drive, collector voltages and VSWR, the setup provides for desired mismatches and the proper characterization of the device. Mismatches are presented to the device under test by the apparatus shown in Figure 10 enclosed by the dashed line. When the output 50-ohm load is replaced with this setup the device under test can be terminated into various mismatches by varying attenuators. This setup is shown in greater detail in Figure 11. The transistor output matching circuit is terminated into a 3 dB hybrid. The hybrid throughport is used to measure the transistor output power, while the coupled port is terminated into a short through an "X" dB pad and line extender. By changing the pad and varying the line extender, the transistor can be terminated into a variety of VSWR's at any reflection coefficient phase angle. The four pads used during this characterization were 10, 6, 3, and 0 dB, which sucessively produce larger mismatches. The approximate VSWR for each of the pads is shown in Table III .

TABLE III. VSWR CORRESPONDING TO VARIOUS COUPLER LOADS

"X" dB Pad	Coupler	Return Loss	Approximate VSWR
10 dB	3 dB	26 dB	
6 dB	3 dB	18 dB	1.29:1
3 dB	3 dB	12 dB	1.67:1
0 dB	3 dB	6 dB	3:1

The actual VSWR seen by the transistor differs from that shown above because of losses in the line extender. Therefore, the setup transmission loss along, with the exact impedance at the carrier output reference plane, was measured on a network analyzer at 30^{o} intervals of the line extender. Characterization was then performed by loading the device into 48 collector load impedances. For the various loads, the device power output, collector current, and input return loss were measured. From these data, the device efficiency and dissipated power were calculated. The infrared microscope was used to measure the peak junction temperature of the hottest cell on the device. Constant power output, power dissipated, efficiency and peak junction temperature contours were then plotted on the complex impedance plane.

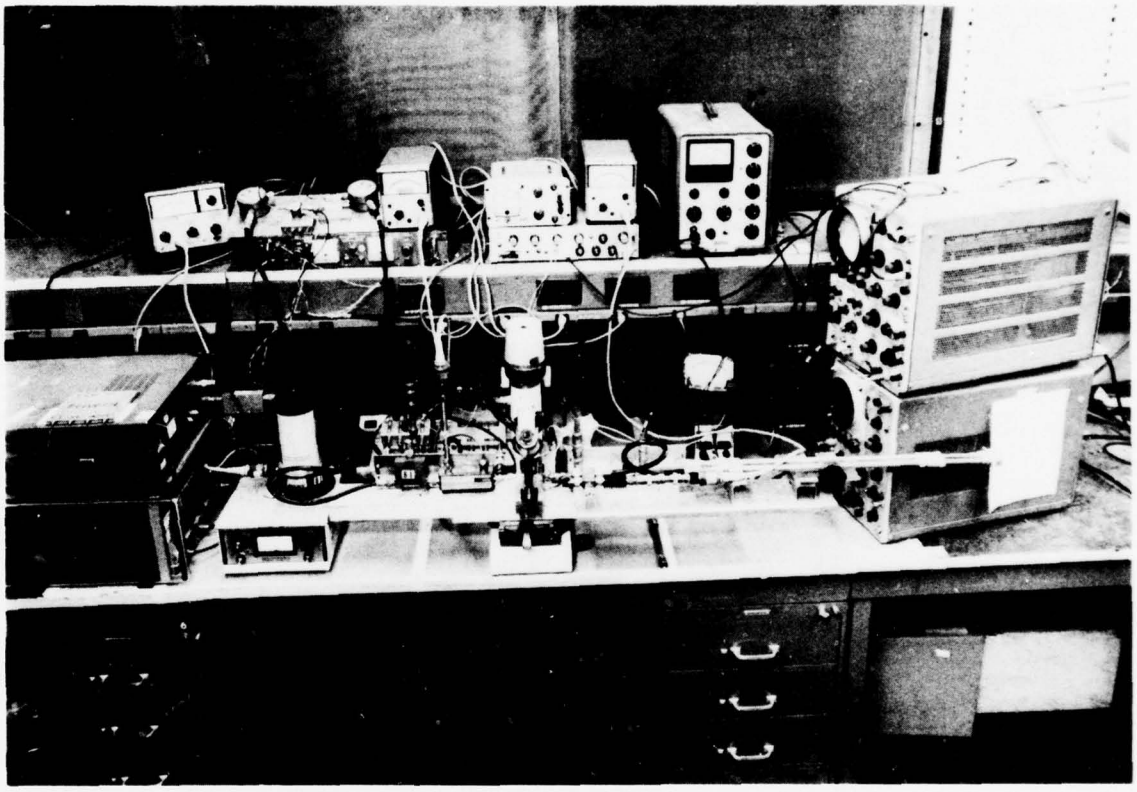

Figure 9 . Microwave Setup for L-Band Device Characterization

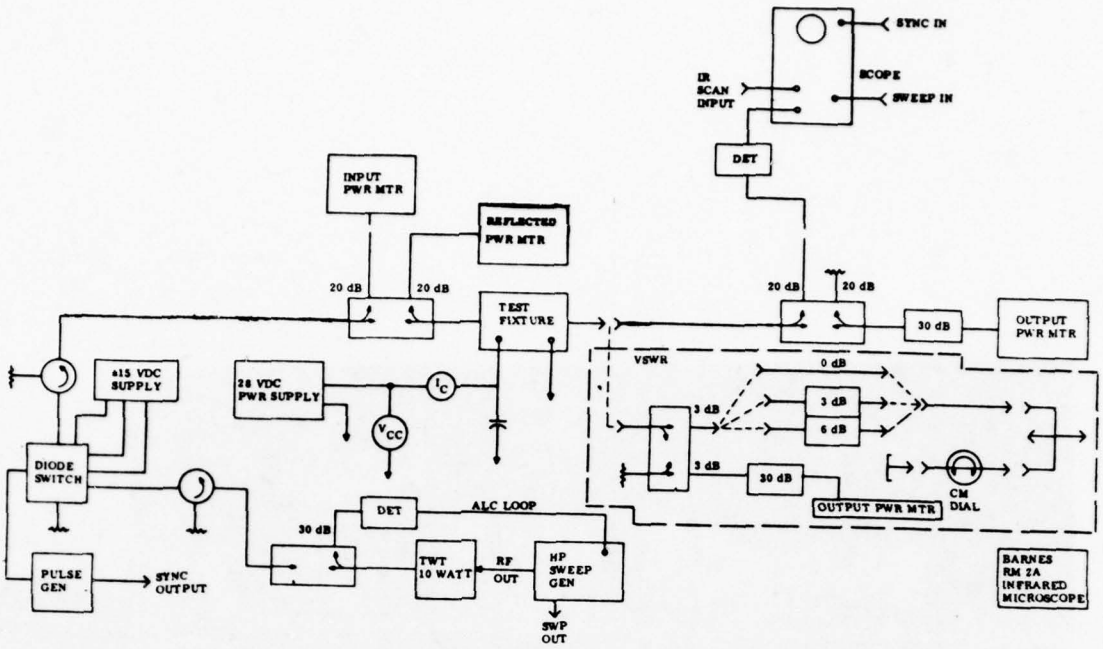

Figure 10. Block Diagram of Microwave/Thermal Test Facility

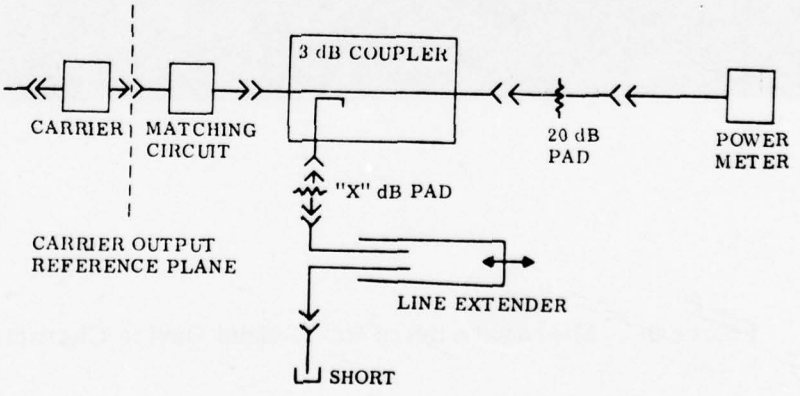

Figure 11. Schematic of VSWR Test Circuit

B. DEVICE TESTING

The typical R.F. performance of the devices tested are shown in Table I . Characterization of the devices was performed under these conditions prior to testing under high drive, collector voltage and mismatch. A detailed review of the characterization of each device follows.

1. Device # 1 Characterization

The stress conditions under which Device 1 was tested are shown in Table IV.

TABLE IV. CONDITIONS UNDER WHICH DEVICE 1 WAS TESTED

		V_{cc}		
		30	35	40
P_{in}	20		X	
	25	X	X	X
	30		X	X

Sets of power output, power dissipated and peak junction temperature contours were obtained for two units, under each of the test conditions listed in Table IV. A partial set of these contours is shown in Figures 12 through 15 for V_{cc} = 40 volts and P_{in} = 25.

While, normally, it is sufficient to record only the junction temperature of the hottest cell, it was necessary to monitor the peak junction temperature for two adjacent cells of Device 1, because of an anomalous transistor temperature profile that was observed. Profiling the 28-cell transistor revealed that the cell temperature alternated from hot to cool from cell to cell. Further, it was observed that the position of the hottest cell varied between two cells at one end of the chip. These cells are designated cells 1 & 2 for convenience. Also, the T_j contours for the two cells follow quite a different pattern. This is accounted for by noting that, although the cells are not physically separated from one another, the separation is sufficient to transform the collector load differently to each cell. Of greater consequence, however, is the fact that each cell is fed by the same emitter wire. This results in cells that are either inside or outside an emitter wire. If the junction temperature profiles are plotted separately, for the cells located toward the interior and exterior side of an emitter wire, two distinct profiles that fluctuate with load are observed. While no clear explanation has been found for these phenomena, it appears that the cells interior to an emitter wire are loaded differently than those located exterior to a wire. If the device was more heavily ballasted, this anomalous behavior may not have occurred.

Table V summarizes the performance of the device when operated into an optimum load at various drive and collector voltages.

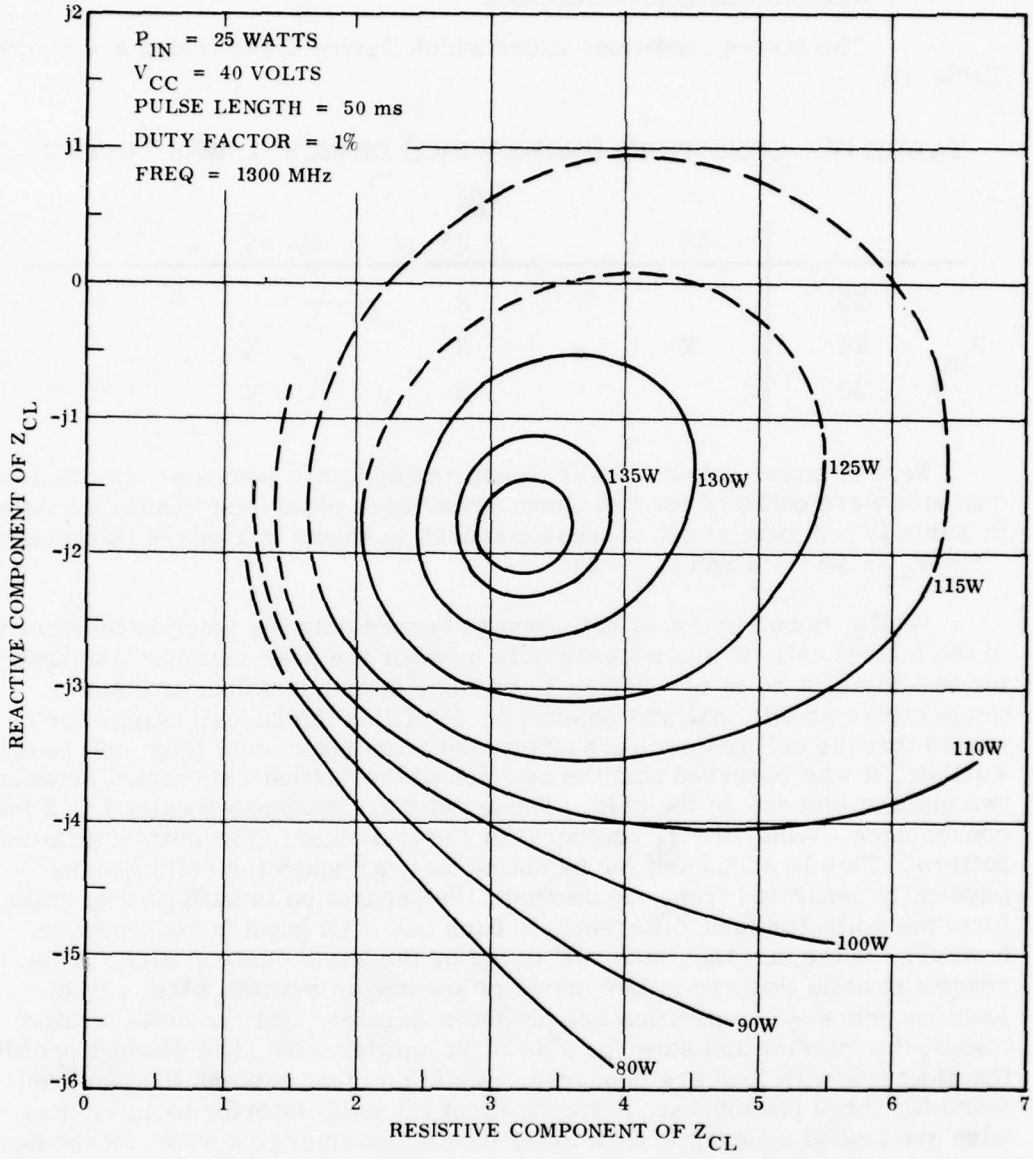

Figure 12. Constant Power Out Contours For Device 1 (Serial No. 3)

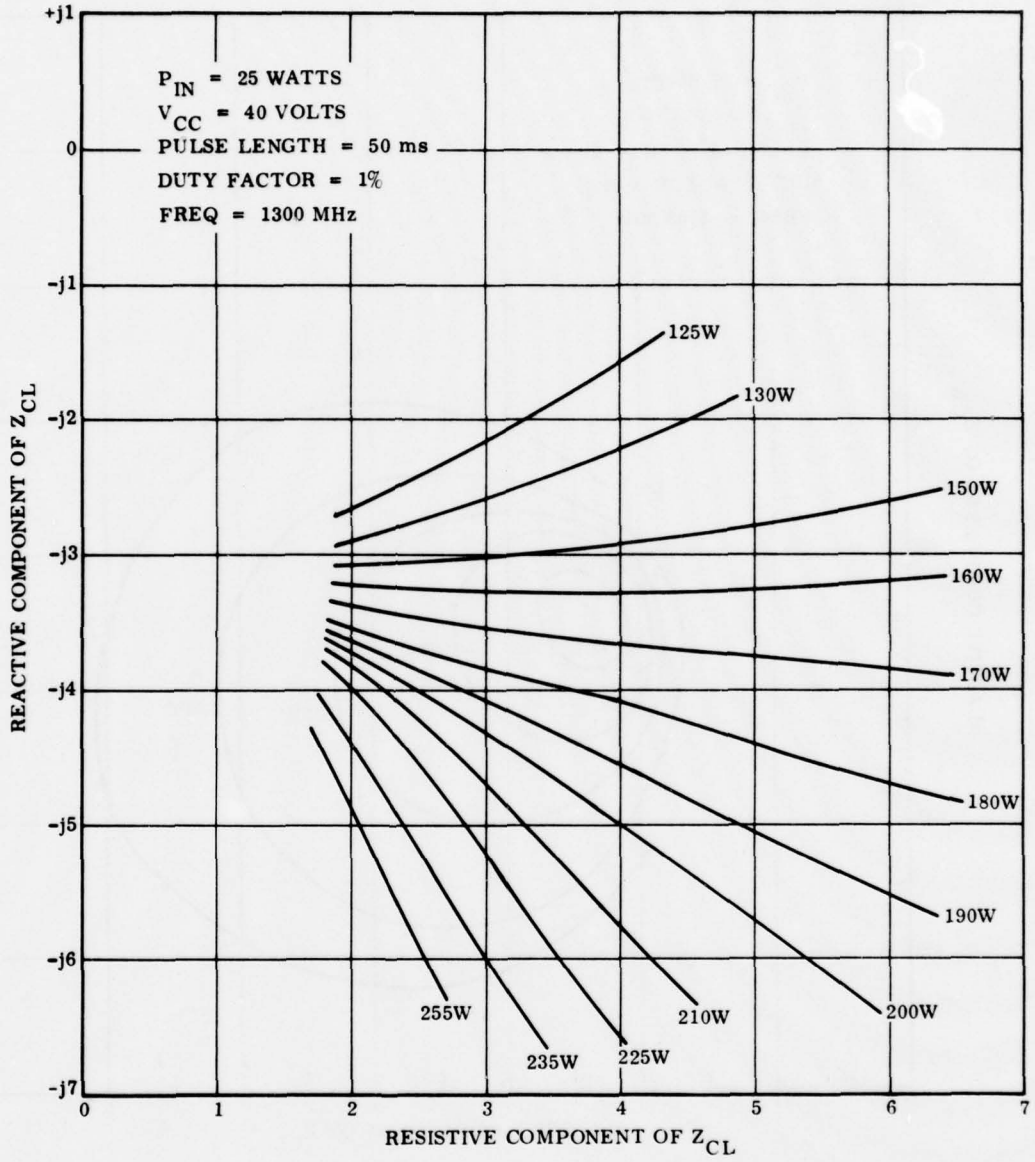

Figure 13. Constant P_{diss} Contours for Device 1 (Serial No. 3)

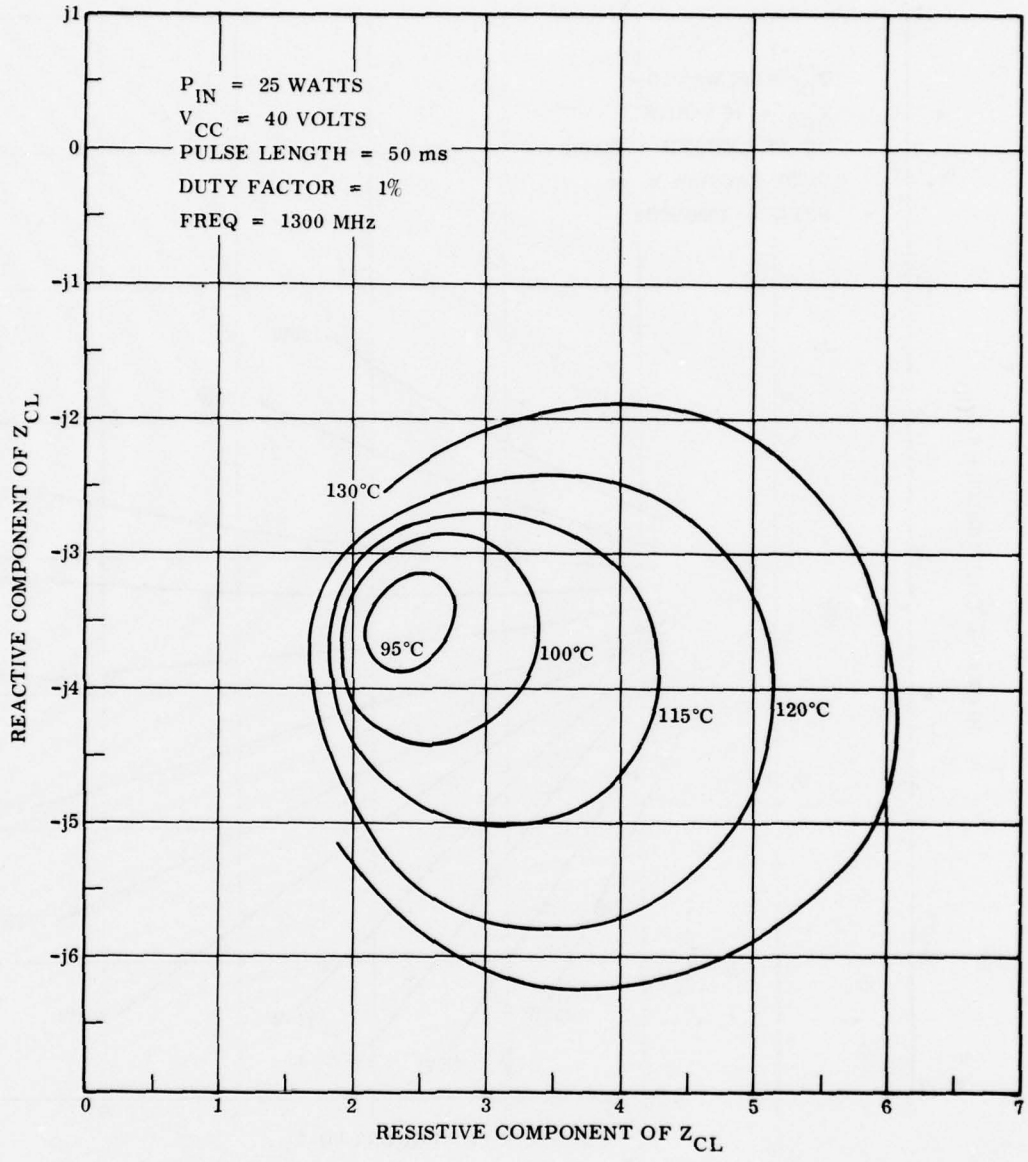

Figure 14. Constant Peak T_j Contours For Device 1 (Serial No. 3) Cell No. 1

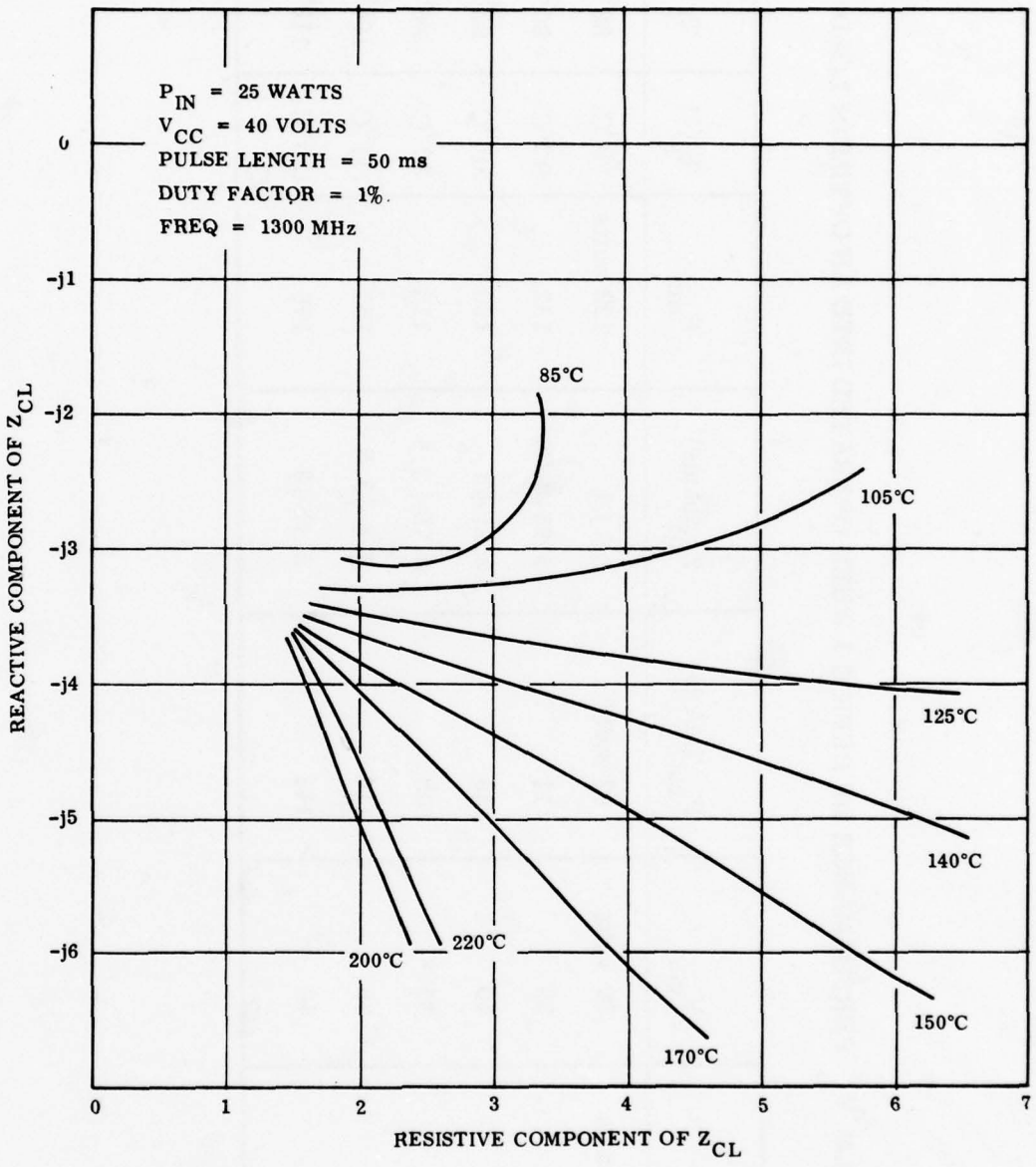

Figure 15. Constant Peak T_j Contour for Device 1 (Serial No. 3) (Cell No. 2)

TABLE V. PERFORMANCE OF DEVICE 1 WHEN OPERATED INTO AN OPTIMUM LOAD

P_{in}	V_{cc}	P_{out}(MAX)	Z_{cl}(ohms)	$P_{\phi is}$	T_j (1)	T_j (2)
25 watts	30 volts	92 watts	3 - j 4	122 watts	79°C	82°C
25	35	111	3.25-3.25	132	97°C	90°C
25	40	139	3.25-j3	150	105°C	93°C
20	35	105	2.75-j 3.5	110	80°C	85°C
30	35	116	3.5 -j3.5	157	111°C	106°C
30	40	141	3.75-j3	176	120°C	113°C

The power output is plotted on log-log paper in Figure 16 as a function of both collector voltage and drive. As indicated, the output power varies as $V_c^{1.3}$ and $P_I^{0.34}$ over the range of the measurement.

2. Device #2 Characterization

The characterization of device # 2 was conducted at the drive and collector voltage shown in Table VI.

TABLE VI

		V_{cc}		
		26	28	30
P_{in}	7		X	
	10	X	X	X
	13		X	

Again two devices were evaluated and power output, power dissipated and peak junction temperature contours were plotted for the conditions shown. Figure 17 to 19 are a set of contours for the nominal device operating conditions. The nominal load at which the device was operated was 4.25-j3 ohms.

The device was then operated into the three indicated mismatches — approximately 1.29:1, 1.67:1 and 3:0. At the two higher mismatches it was observed that the detected video pulse was breaking up, as shown in Figure 20. The breakup was accompanied by an increase in the power output of the device and a decrease in peak junction temperature. While no spurious outputs could be observed with a spectrum analyzer, there was an apparent increase in the noise level of the baseline. While the region of instability is quite close to the optimum load condition, the region was avoided for subsequent stress testing.

Optimum operation of Device #2 for the various combination of drive and collector voltage is shown in Table VII.

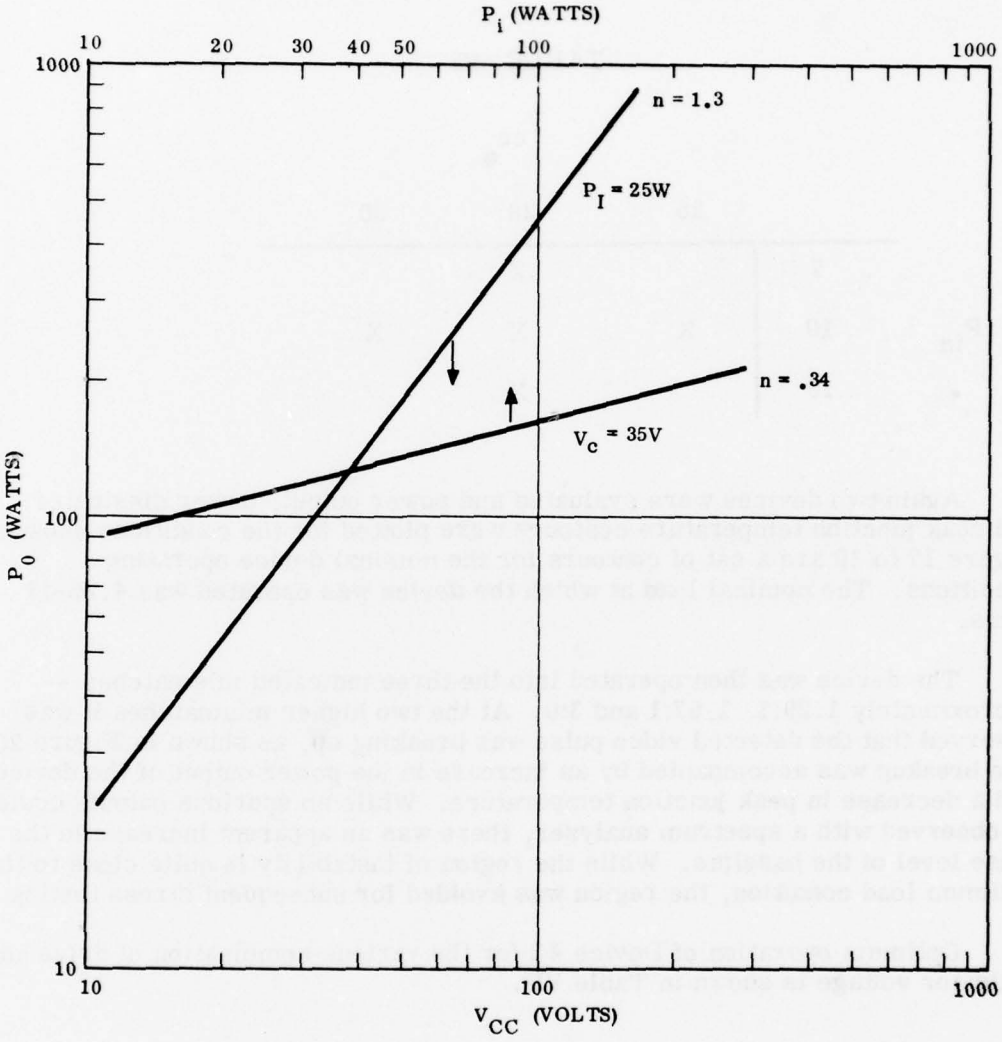

Figure 16. Power Output versus V_{cc} and P_I for Device No. 1

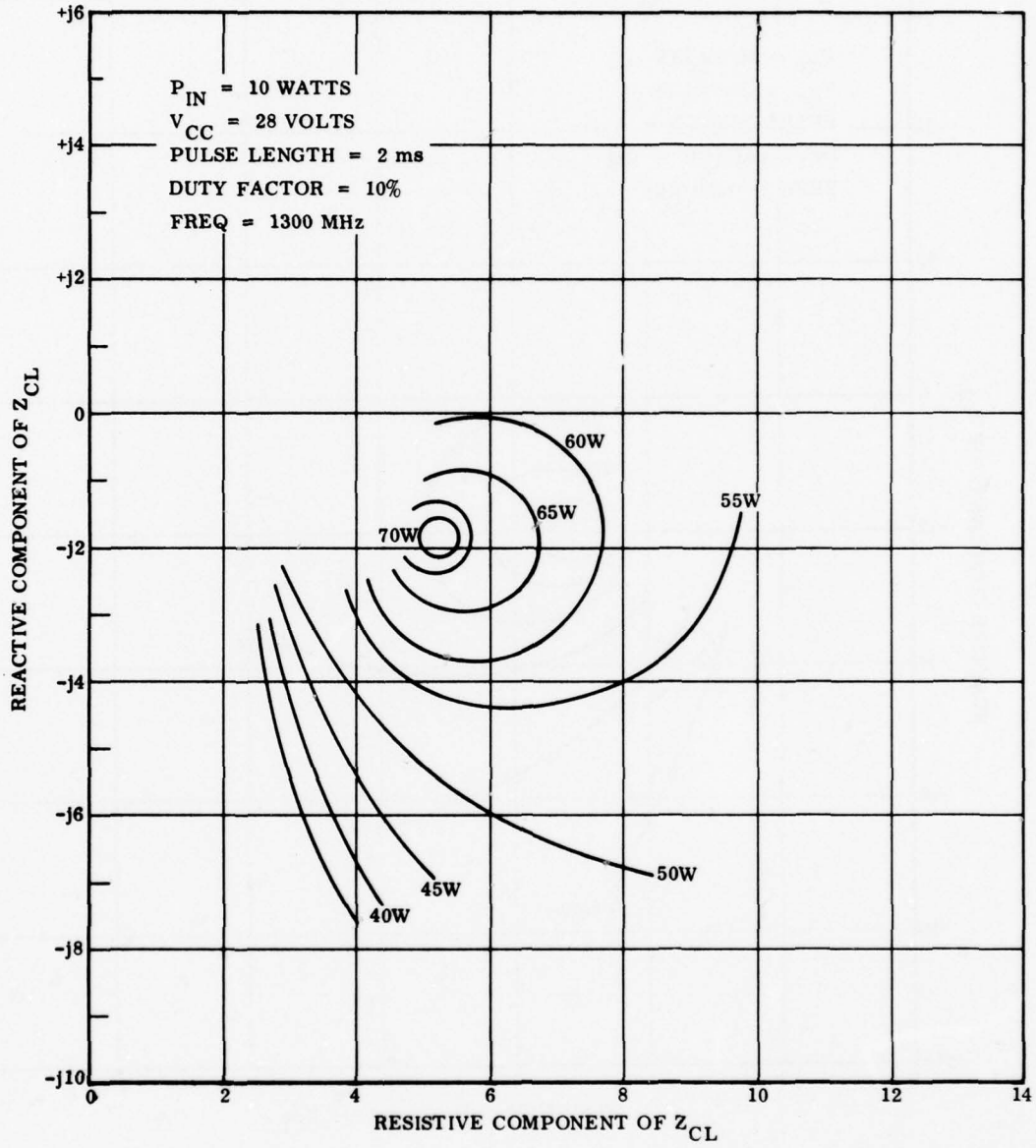

Figure 17 Constant P_o Contours for Device 2 (Serial No. 8)

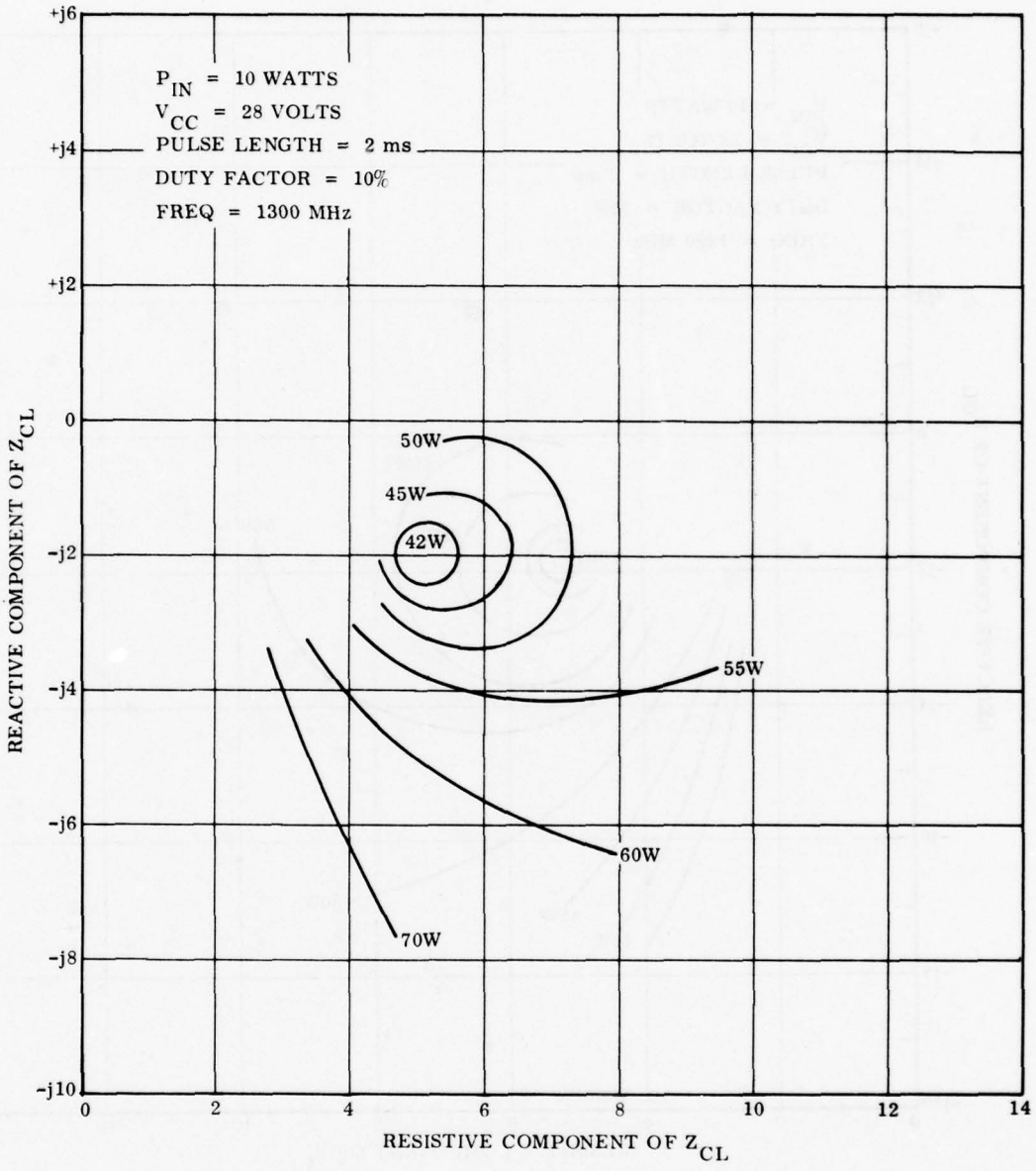

Figure 18. Constant P_{diss} Contours for Device 2 (Serial No. 8)

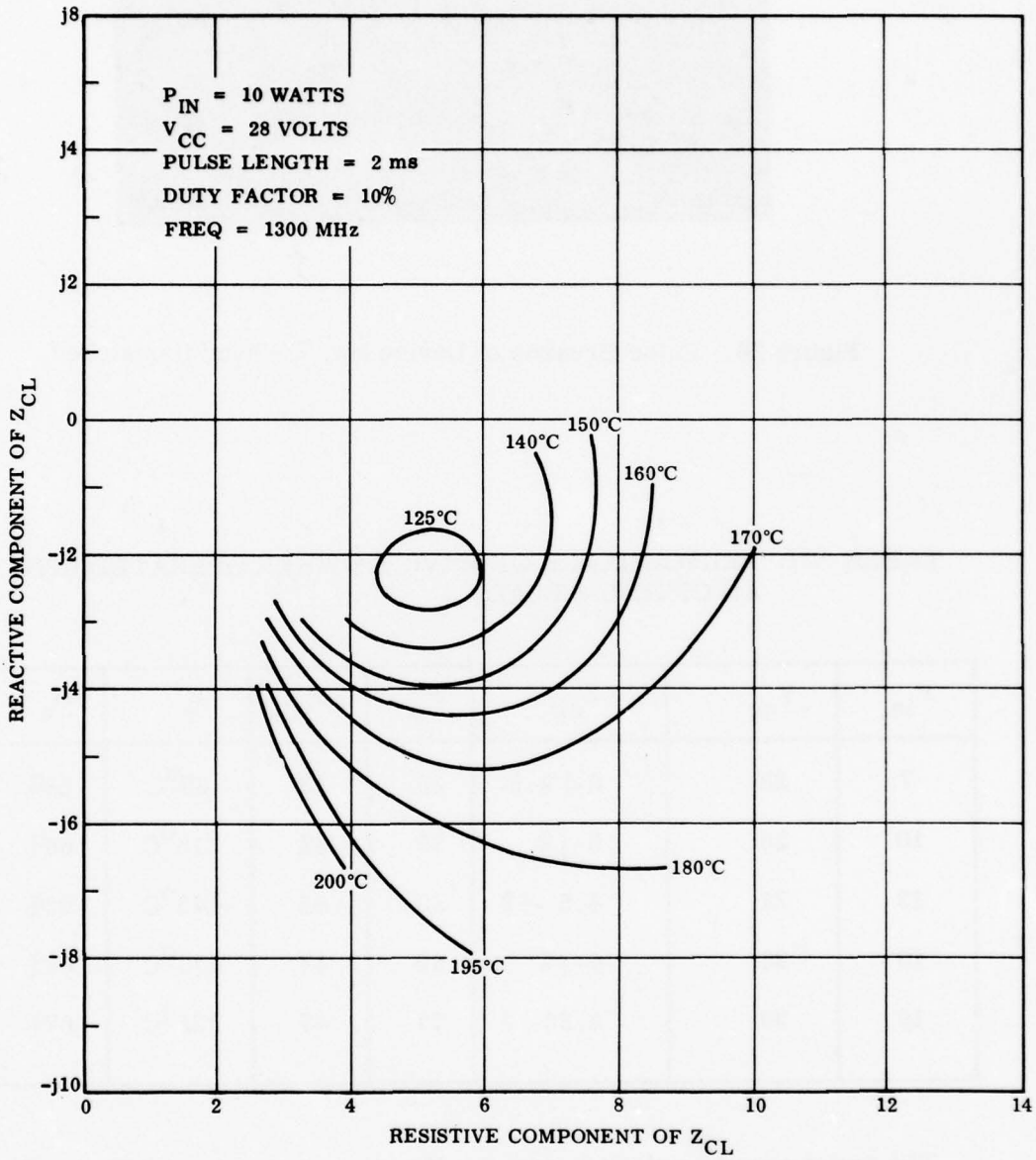

Figure 19. Constant T_j Contours for Device 2 (Serial No. 8)

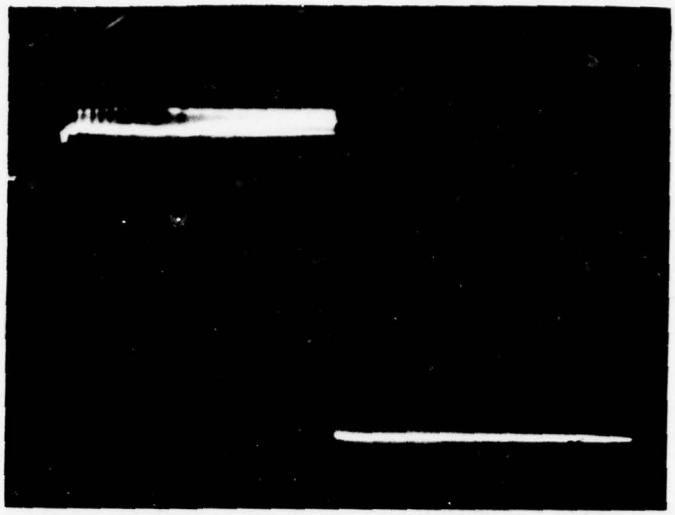

Figure 20. Pulse Breakup of Device No. 2 When Mismatched

TABLE VII. PERFORMANCE OF DEVICE 2 WHEN OPERATED INTO AN OPTIMUM LOAD.

P_{in}	V_{cc}	Z_{cl}	P_o	P_{Dis}	T_j	N_e
7	28	6-j 1.5	56	43	95°C	68%
10	28	5-j 2	70	42	115°C	68%
13	28	4.5 -j 2	80	55	145°C	65%
10	26	4-j 2	65	47	110°C	64%
10	30	5.25-j 2	77	47	135°C	67%

The power output is plotted versus both voltage and drive in Figure 21. The output power varies almost linearly with collection voltage and as the square root of the drive.

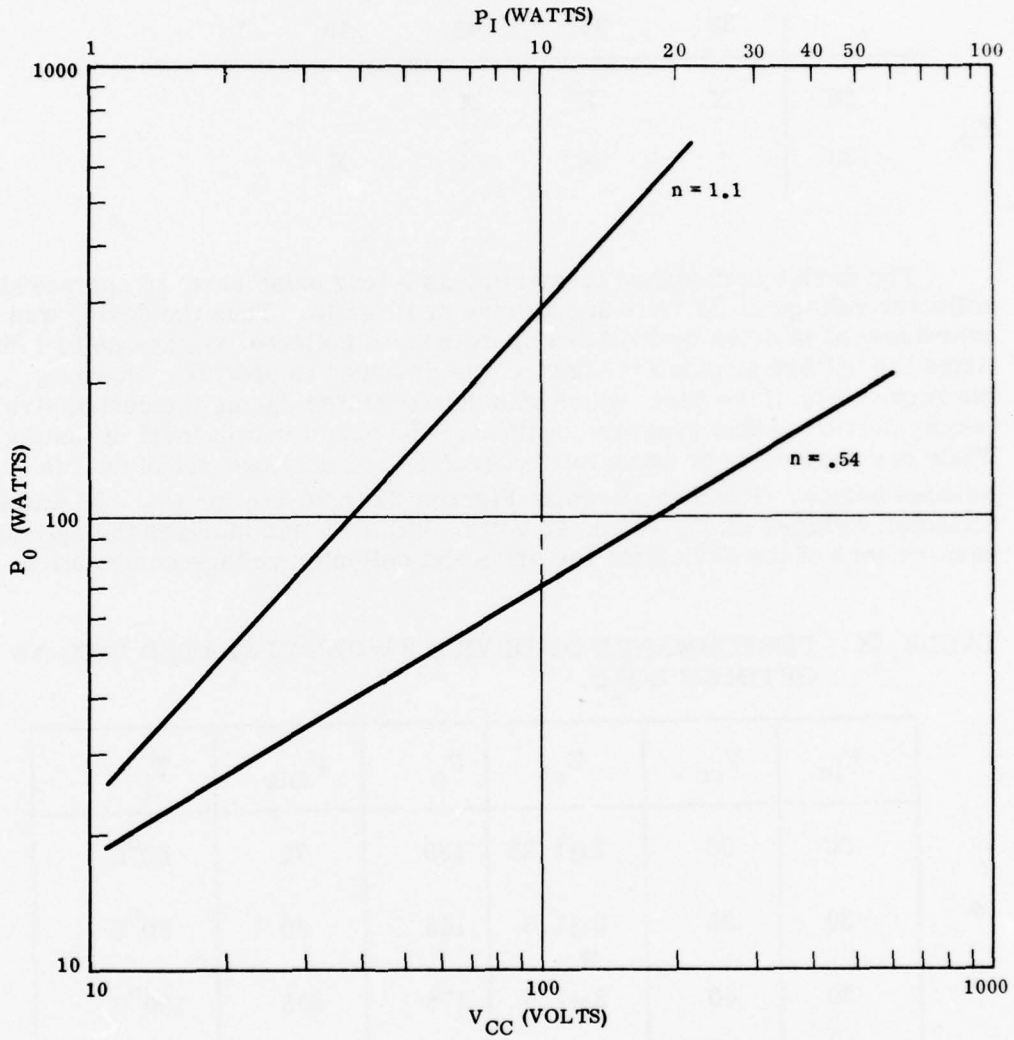

Figure 21 Power Output versus Voltage and Drive for Device 2.

3. Device # 3 Characterization

The characterization of the UHF transistor (Device 3) was performed under the drive and collector voltage outline in Table VIII.

TABLE VIII. CONDITIONS UNDER WHICH DEVICE 3 WAS TESTED

		V_{cc}			
		30	35	40	45
P_{in}	30	X	X	X	
	35		X	X	X

The device is designed primarily, as a long pulse part, to operate at a collector voltage of 31 volts and a drive of 16 watts. Thus the device was overstressed in drive by 3 dB and operated at a collector voltage up to 1.5 times the voltage at which the device was designed to operate. However, the ruggedness of the part, which was demonstrated during the destructive testing portion of this program, validated the need for this level of testing. While two devices were again fully characterized only one set of data is included herein. The data shown in Figures 22 to 30 are for P_{in} = 35 watts and collector voltages of 35, 40 and 45 volts. Table IX summarizes the optimum performance of the device for the drive and collector voltage combinations.

TABLE IX. PERFORMANCE OF DEVICE 3 WHEN OPERATED INTO AN OPTIMUM LOAD.

P_{in}	V_{cc}	Z_{cl}	P_o	P_{Dis}	T_j
30	30	2+j1.25	130	75	60°C
30	35	2+j1.5	145	80	80°C
30	40	2+j1.5	175	105	100°C
35	40	2+j1.5	180	95	90°C
35	40	2+j1.5	200	115	115°C
35	45	2+j1.75	210	150	130°C

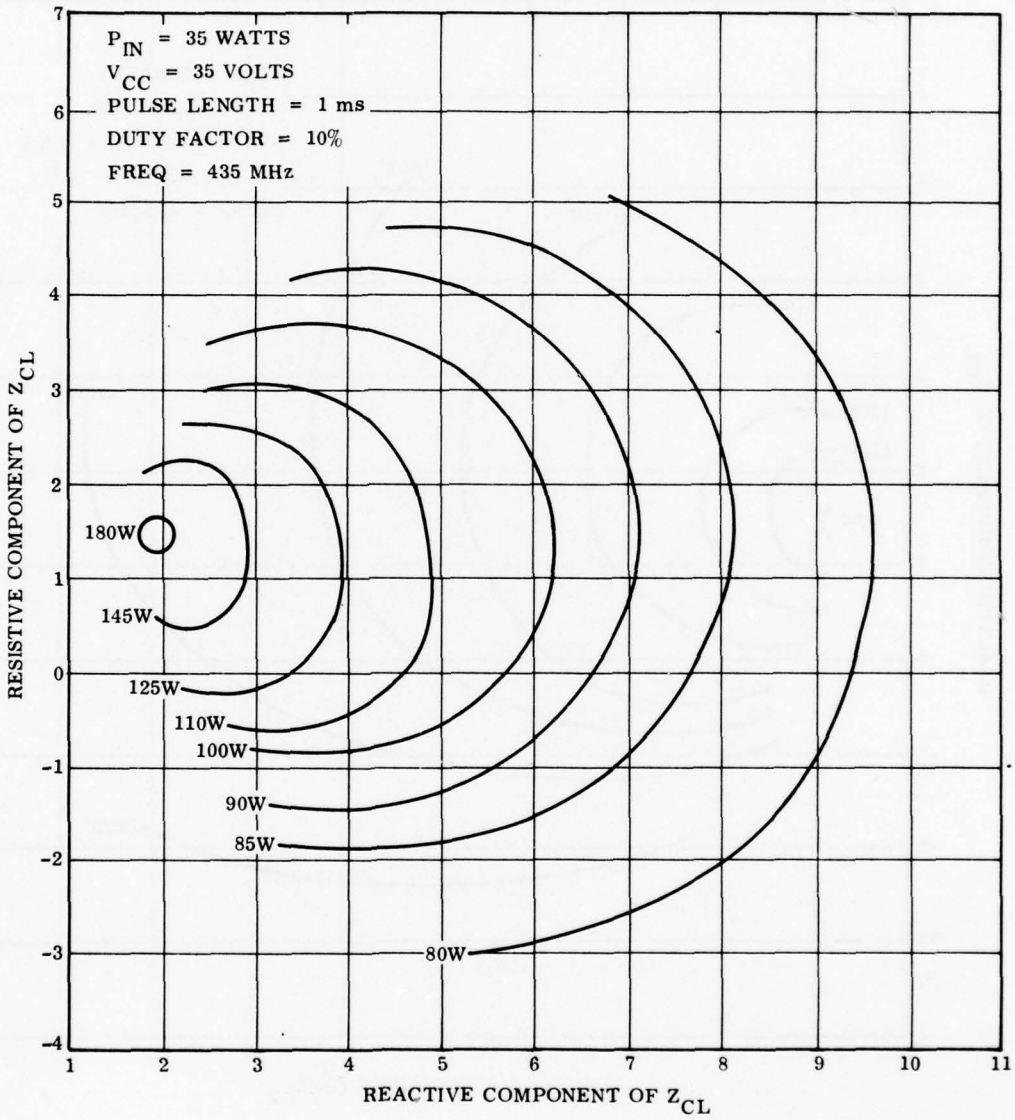

Figure 22 Constant Output Power Contours for Device 3 (Serial No. 7)

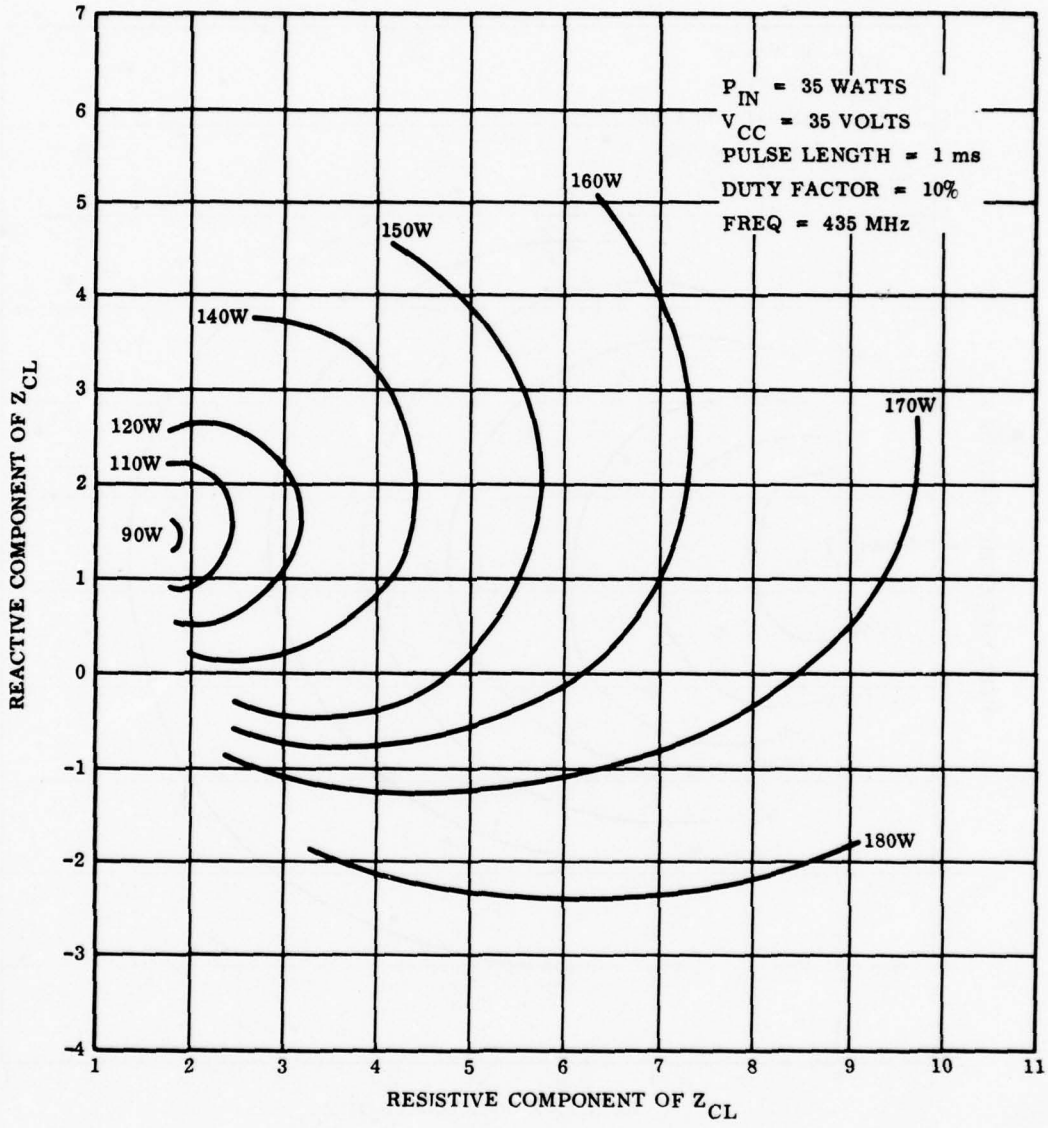

Figure 23. Constant Power Dissipated Contours Device 3 (Serial No. 7)

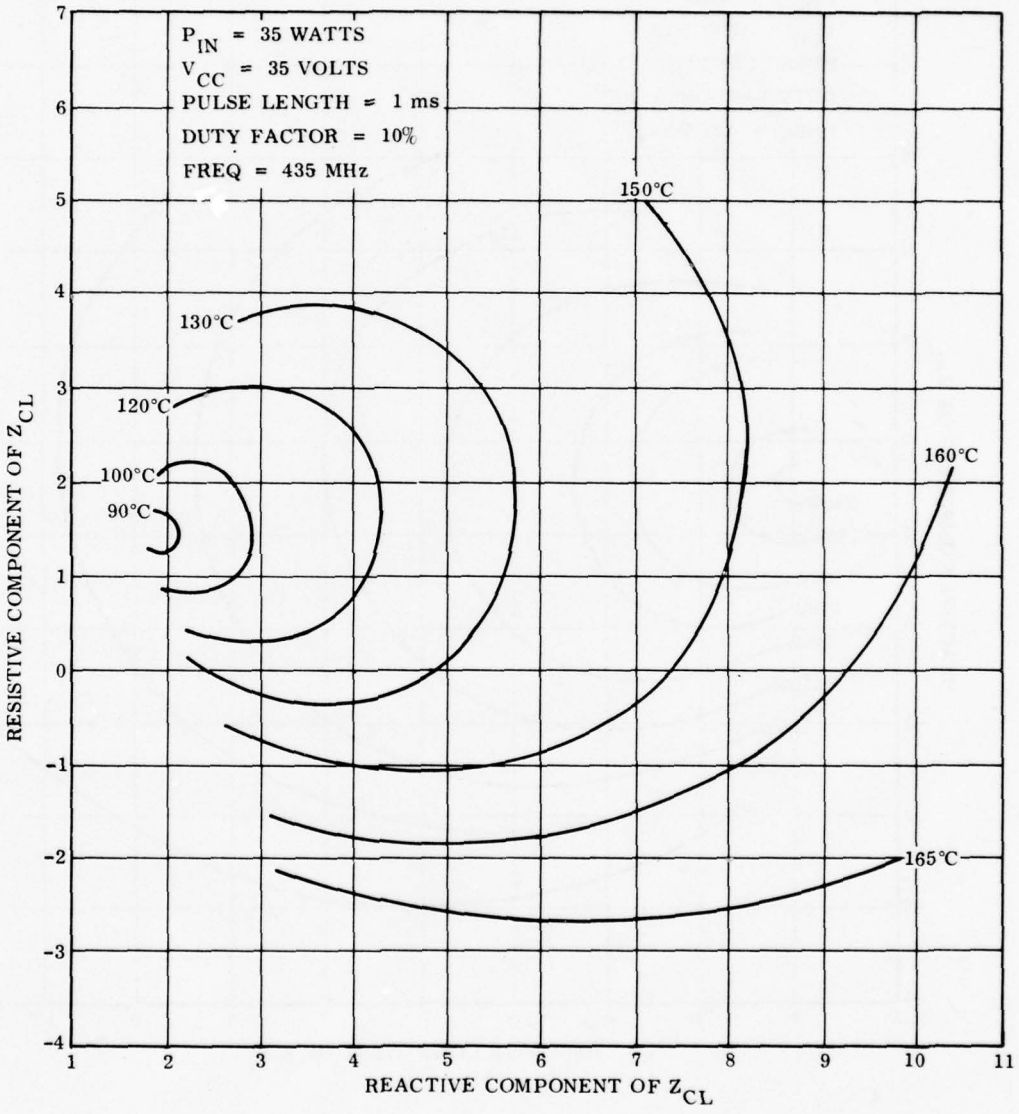

Figure 24. Constant T_j Contours For Device 3 (Serial No. 7)

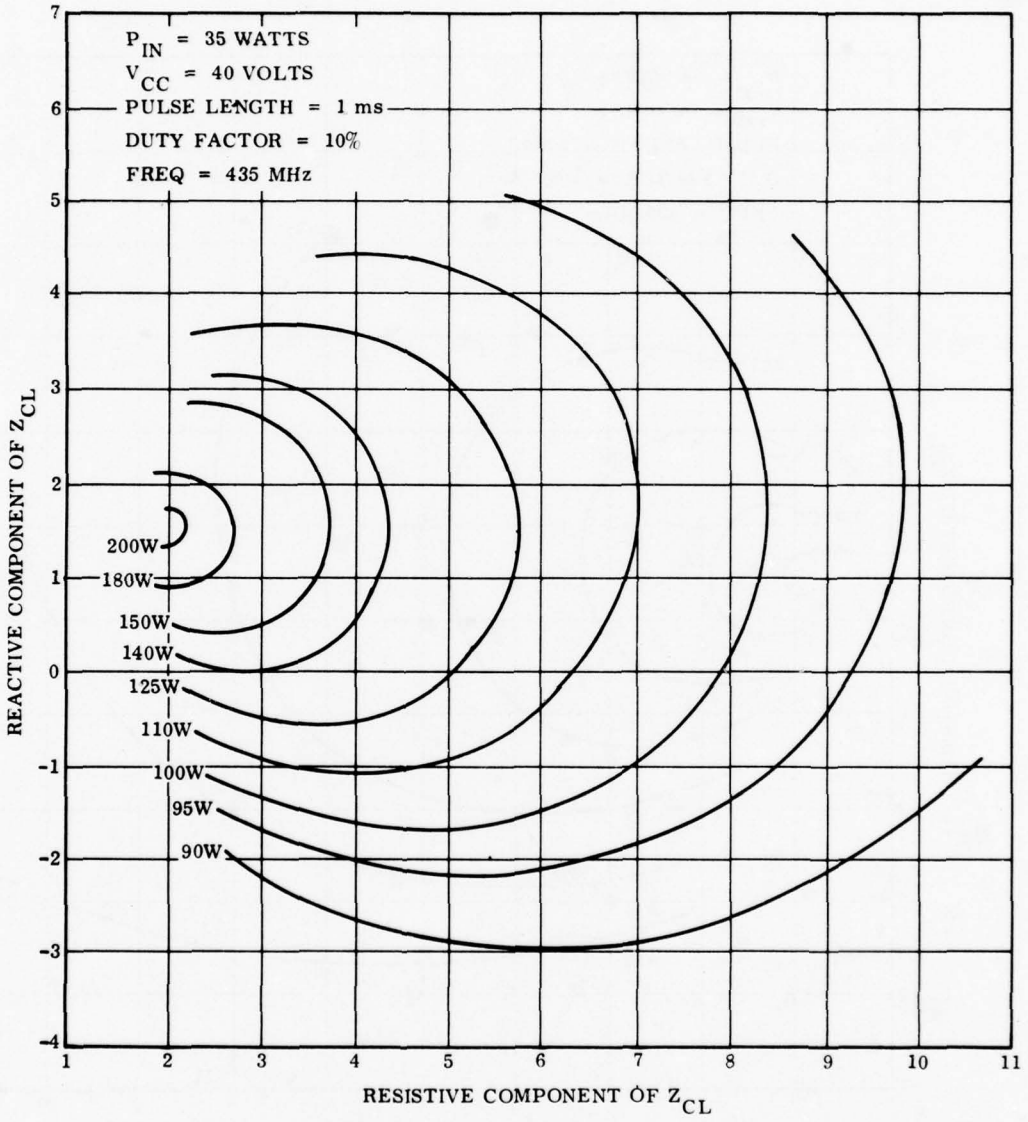

Figure 25. Constant Output Power Contours for Device 3 (Serial No. 7)

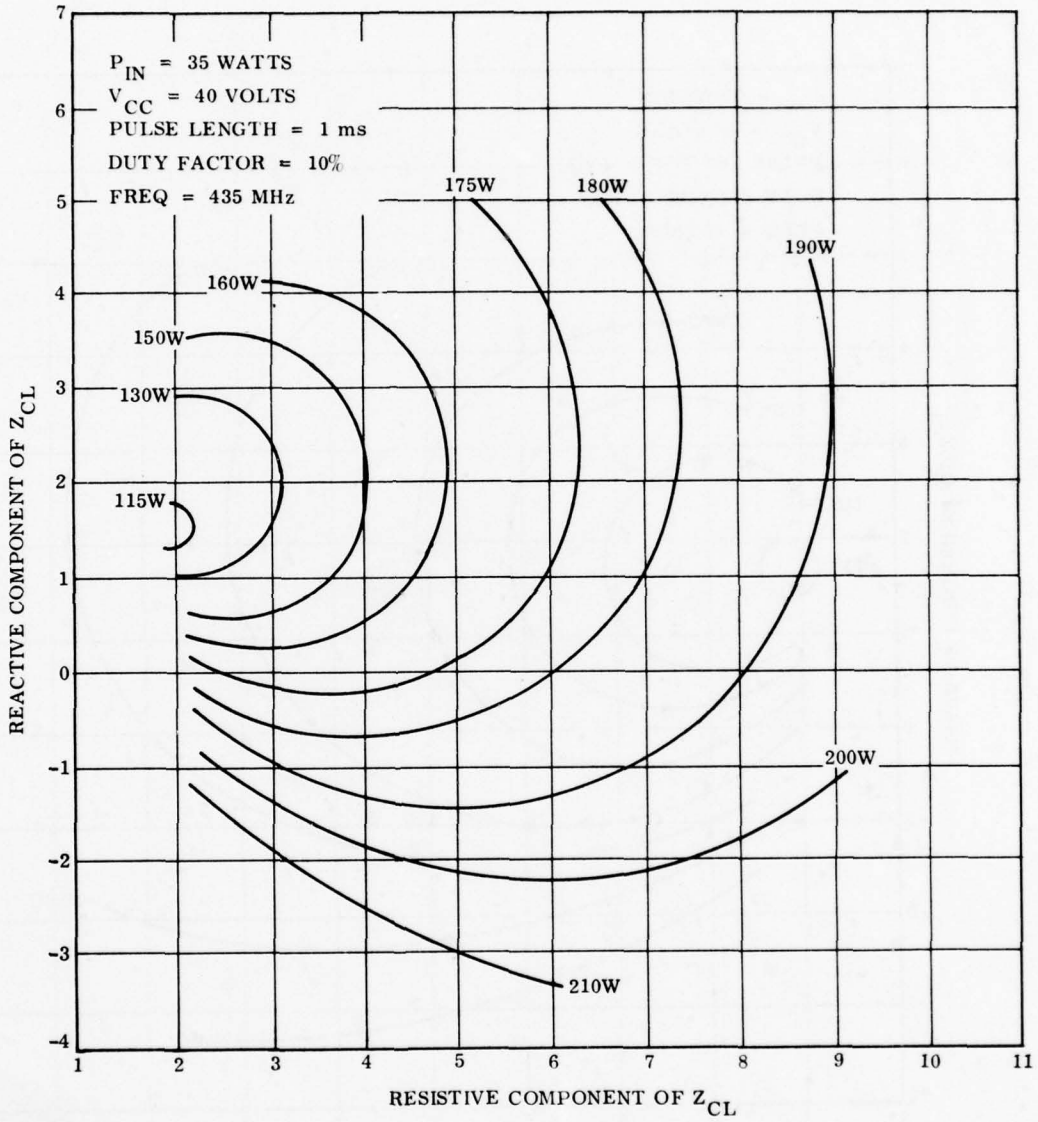

Figure 26. Constant P_{diss} Contours for Device 3 (Serial No. 7)

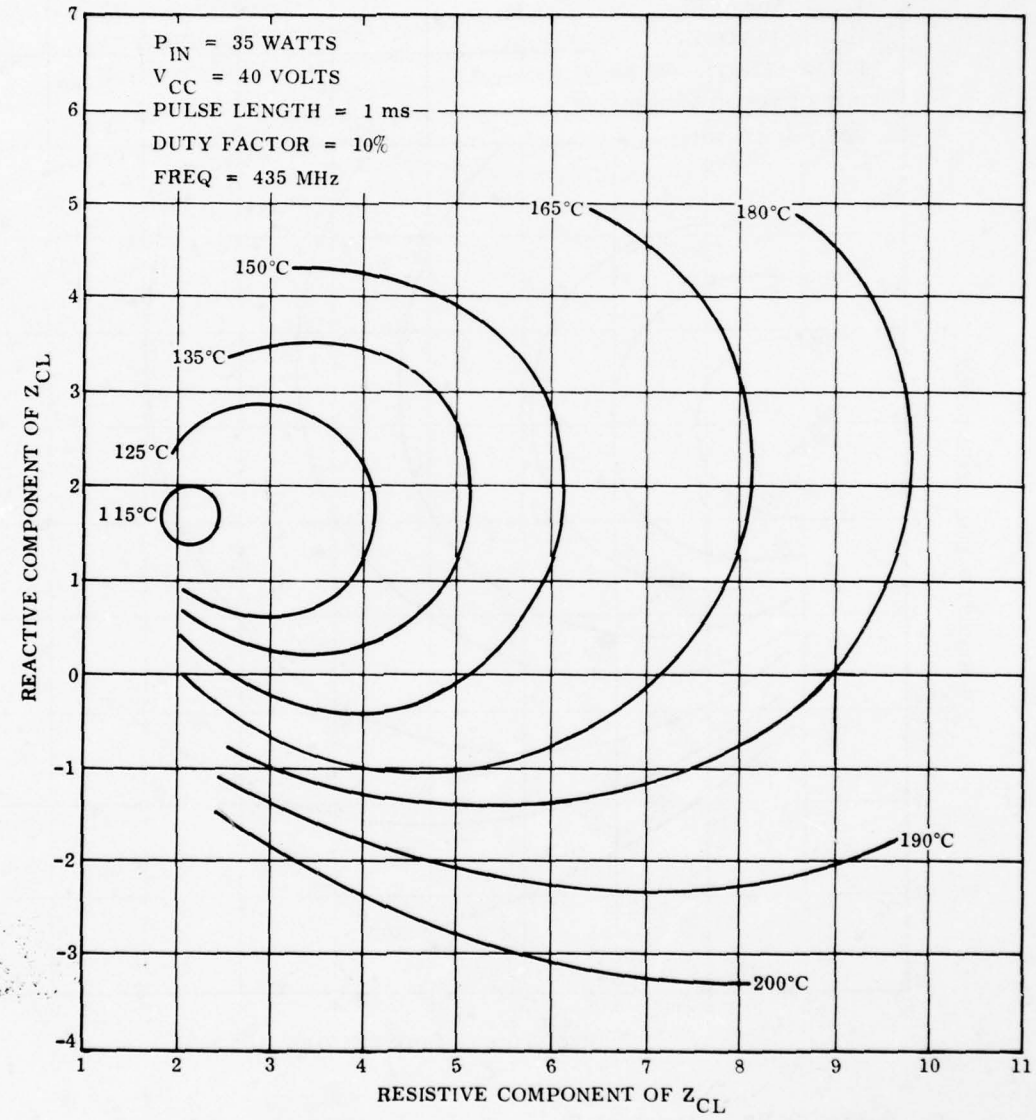

Figure 27. Constant T_j Contours for Device 3 (Serial No. 7) Cell No. 21

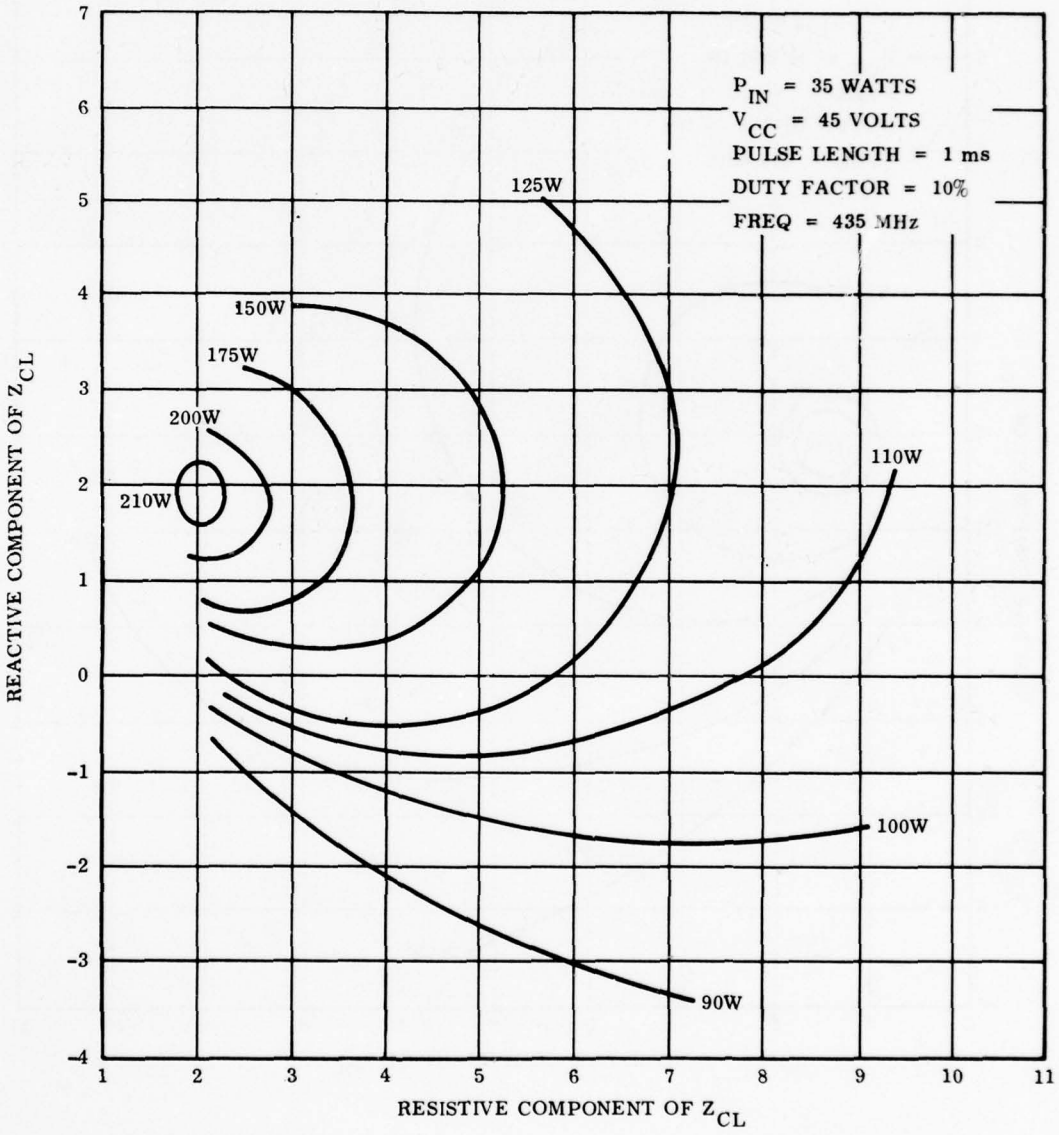

Figure 28. Constant Power Output Contours For Device 3 (Serial No. 7)

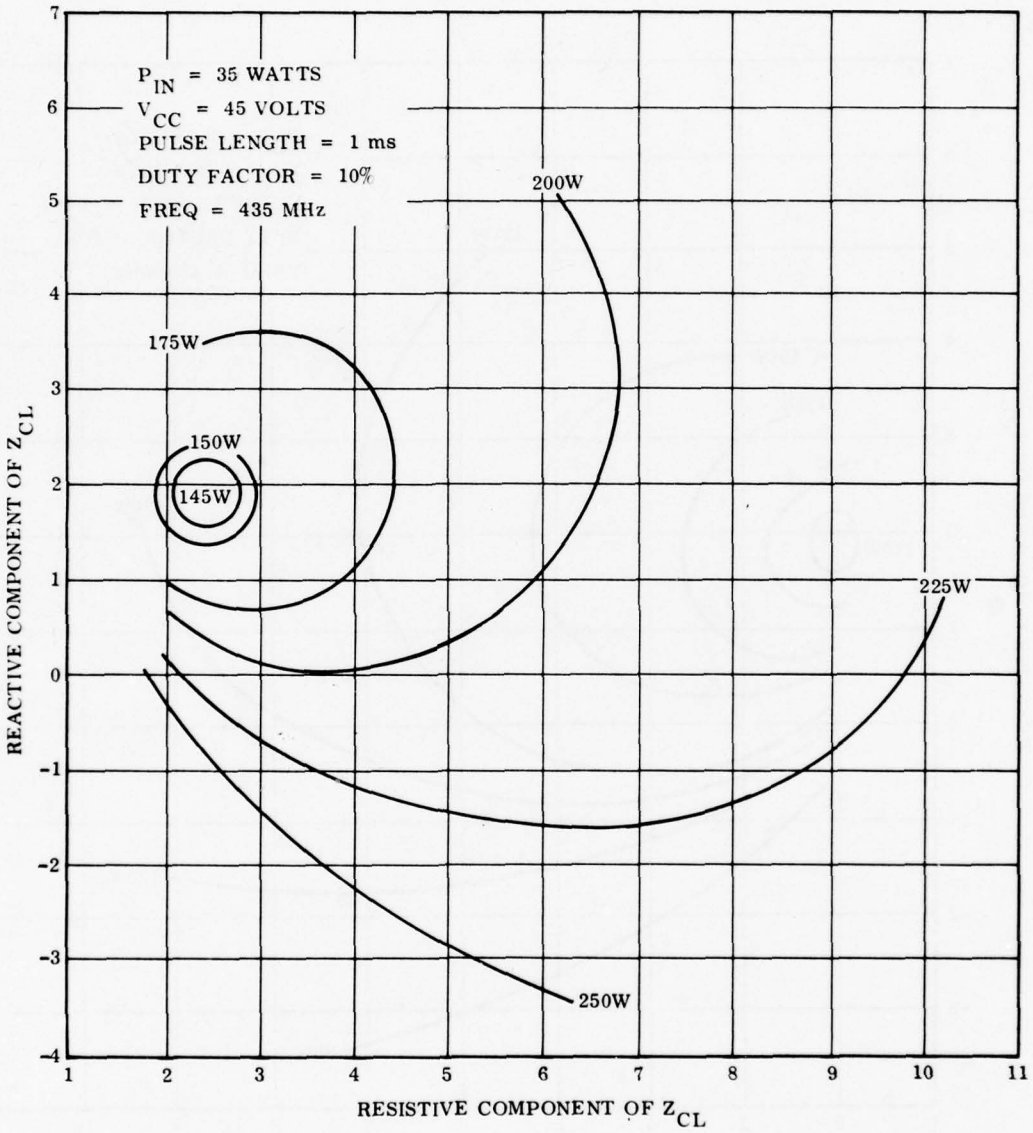

Figure 29 Constant P_{diss} Contours for Device 3 (Serial No. 7)

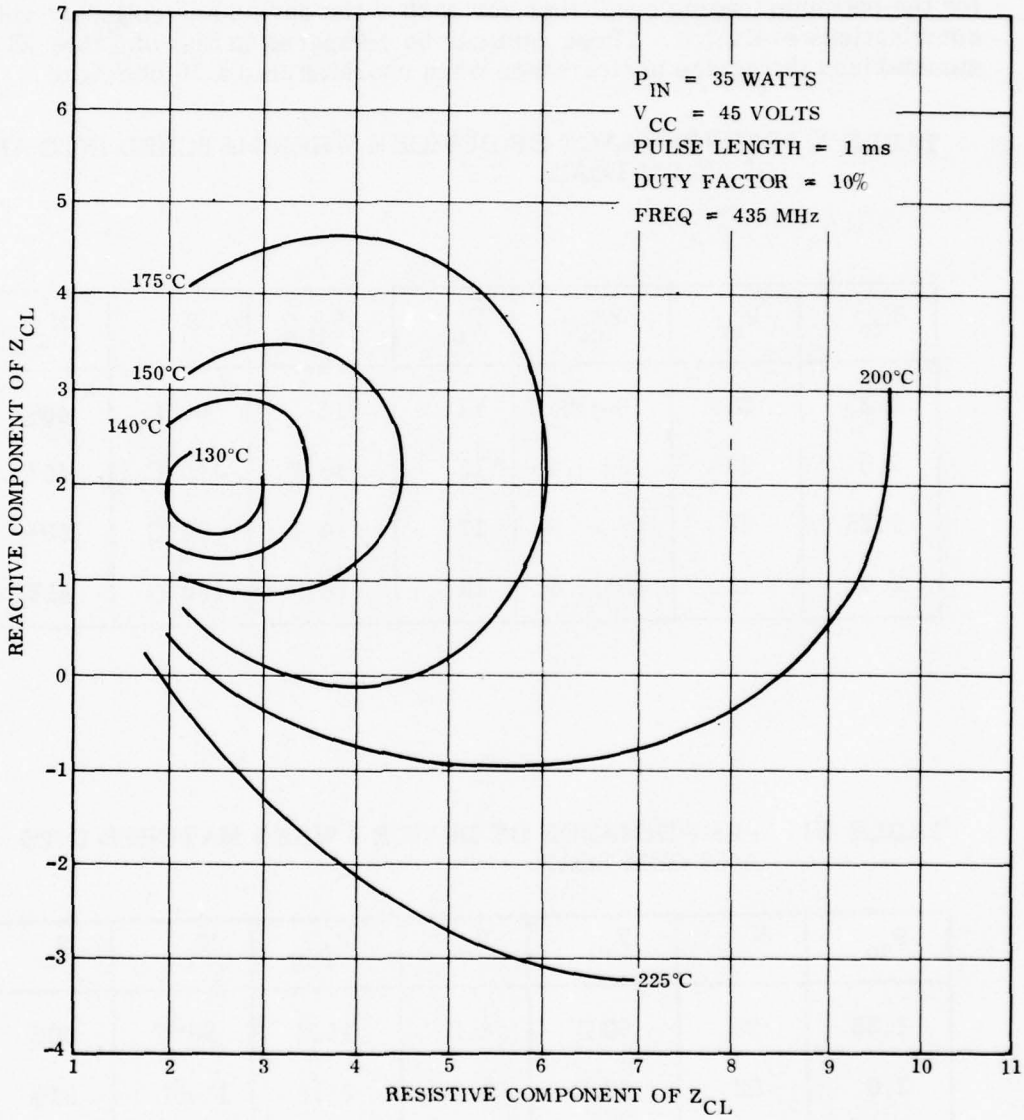

Figure 30. Constant T_j Contours For Device 3 (Serial No. 7)

4. Device # 4 Characterization

Device #4, the S-band device, was characterized at 3.3 GHz. Contours or constant power output, power dissipated, peak junction temperature and efficiency are shown in Figures 31 to 34 for a collector voltage of 28 volts and an input drive of 1.25 watts. Since the transistor carrier is matched to 50 ohms, the contours are plotted on a Smith chart. While the devices deliver 6 watts into a 50-ohm load, an increase in output power and efficiency can be obtained by adjusting the load to .8 - j · 6 ohms. It is suspected that the output matching circuit of this device is adjusted to flatten the power output of the device at six watts across the 3.1 to 3.5 GHz band and, consequently, the devices is intentionally detuned at 3.3 GHz. Table X lists the performance for the optimum loading conditions for each of the device and collector voltage combinations evaluated. These data can be compared to that of Table XI, which summarizes the device performance when operated into a 50 ohm load.

TABLE X. PERFORMANCE OF DEVICE 4 WHEN MATCHED INTO AN OPTIMUM LOAD.

P_{in}	V_{cc}	Z_{cl}	P_o	P_{Dis}	T_j	N_c
1.25	28	.8-j.6	11	14	90°C	46%
2.0	28	.65-j.4	12	15.7	110°C	46%
1.25	32	.6 - .7	13	14.1	96°C	50%
2.0	32	.55-j.4	13	18.0	120°C	45%

TABLE XI. PERFORMANCE OF DEVICE 4 WHEN MATCHED INTO A 50 OHM LOAD.

P_{in}	V_{cc}	Z_{cl}	P_o	P_{Dis}	T_j	N_c
1.25	28	50 Ω	6.2	15.2	98°C	30%
2.0	28	50 Ω	9.5	21.8	150°C	31%
1.25	32	50 Ω	7.0	19	137°C	28%
2.0	32	50 Ω	9.2	27.0	195°C	27%

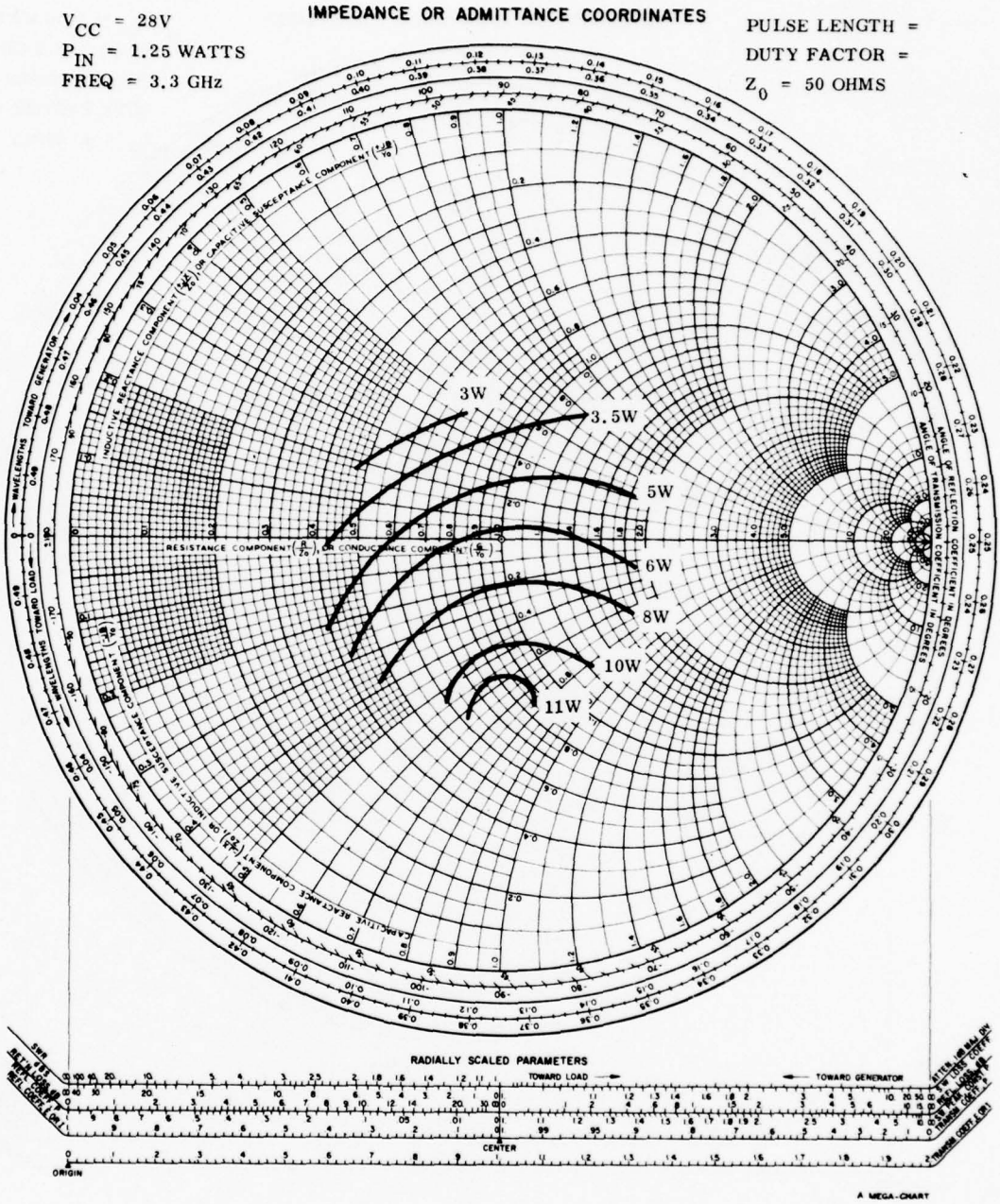

Figure 31 Constant Output Power Contours for Device 4 (Serial No. 2)

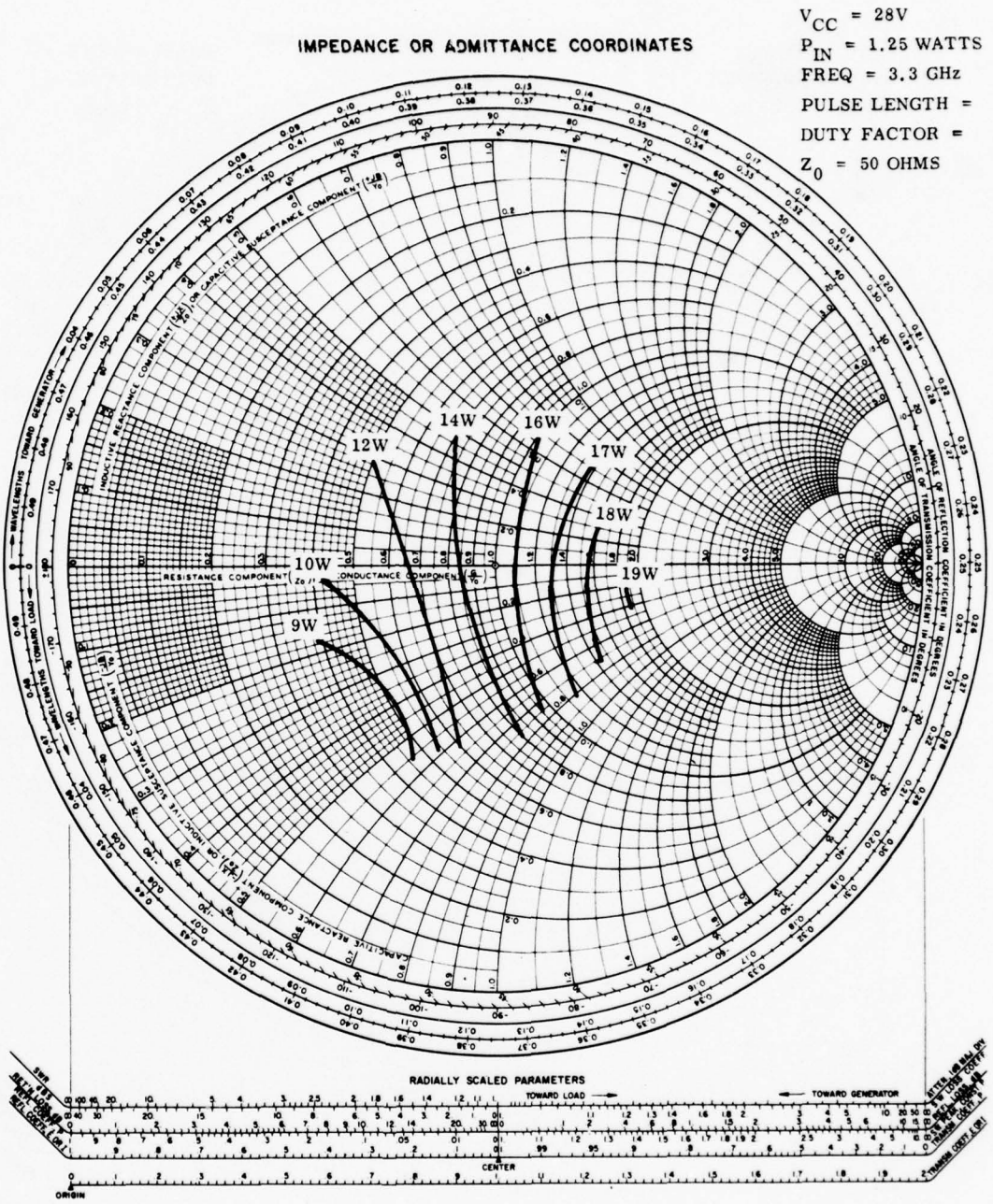

Figure 32. Constant P_{diss} Contours for Device 4 (Serial No. 2)

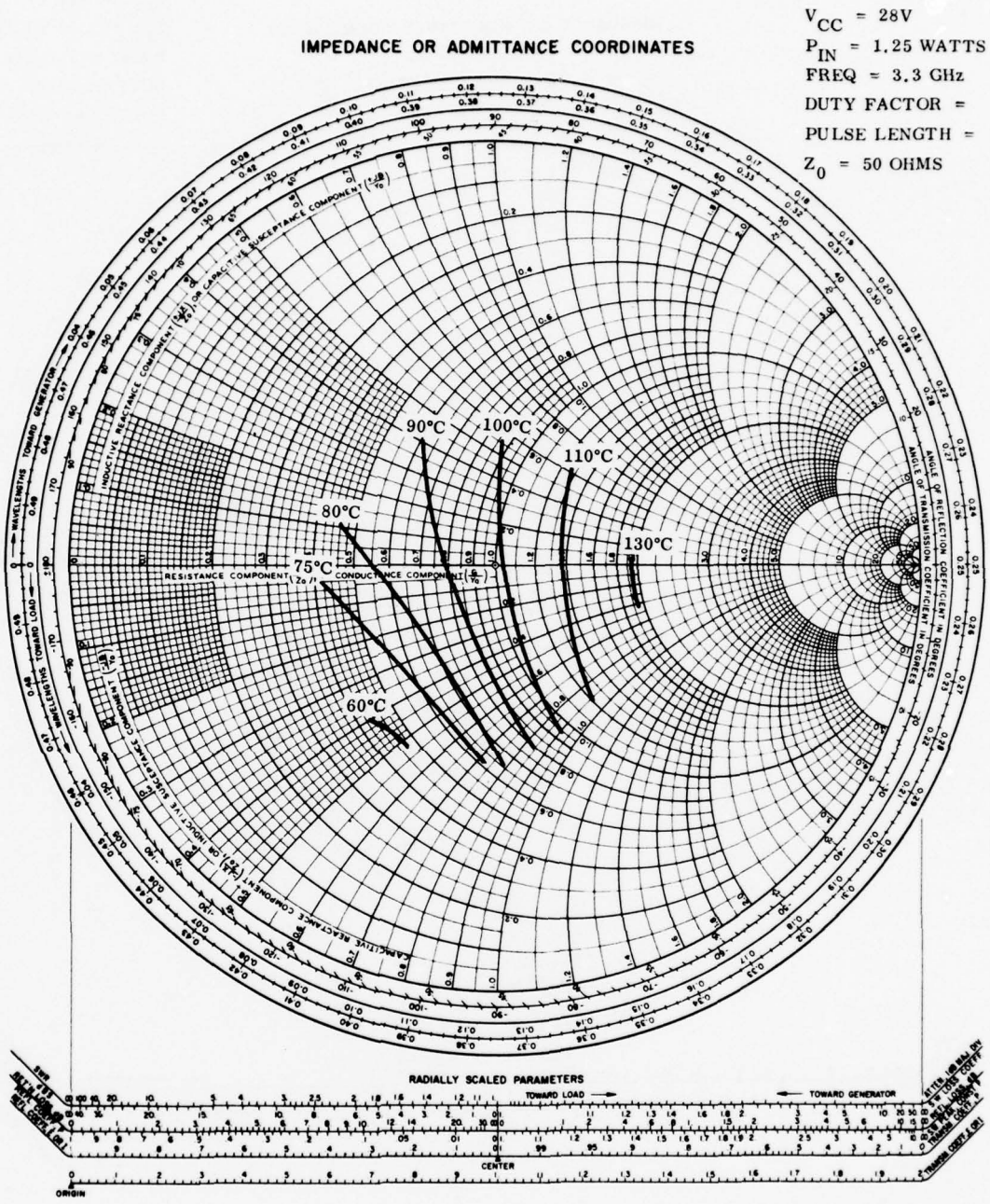

Figure 33. Constant Peak T_j Contours for Device 4 (Serial No. 2)

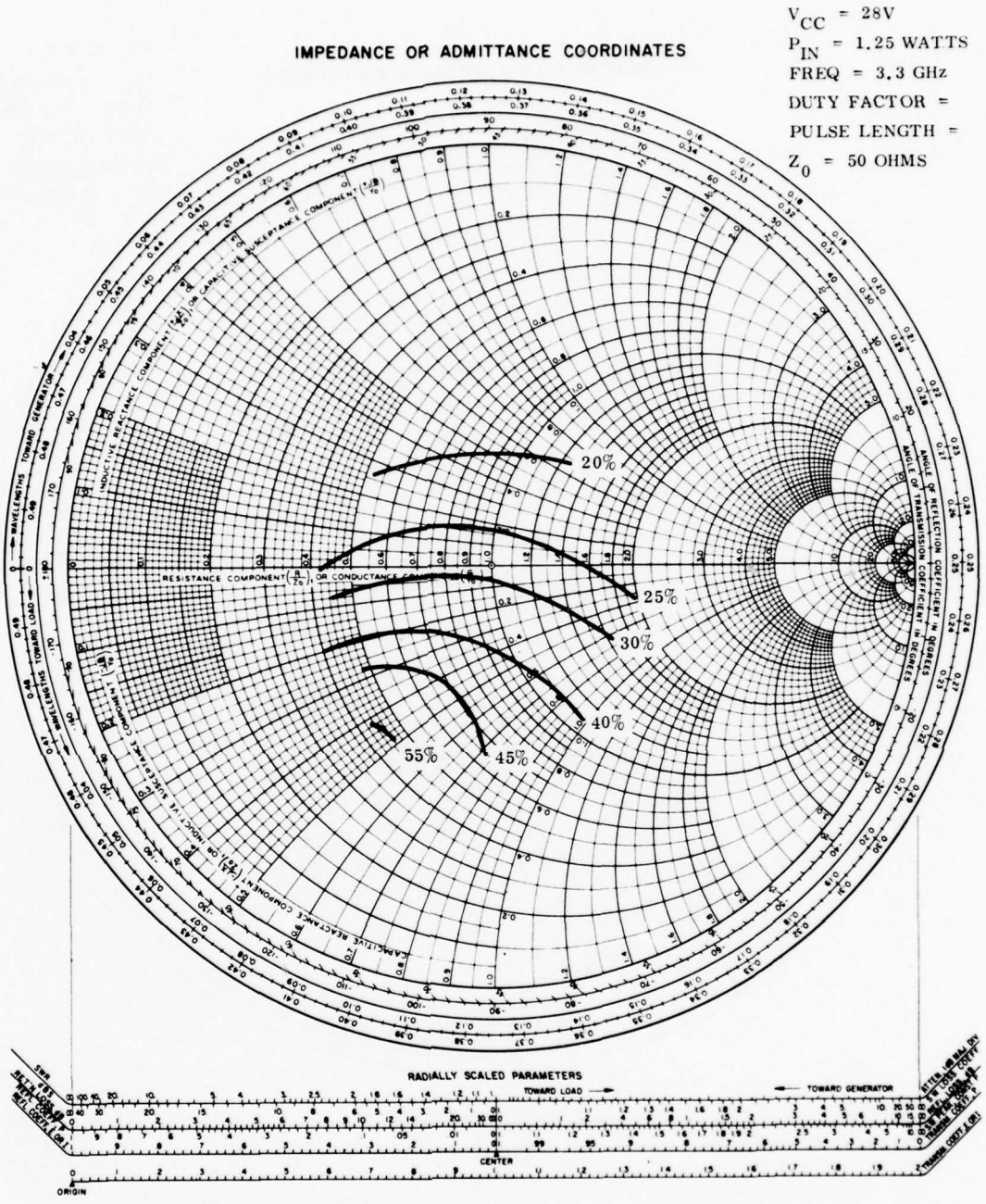

Figure 34. Constant Collector Efficiency Contours for Device 4 (Serial No. 2)

No attempt has been made with any of the four devices evaluated to analyze the change in the optimum collector load with drive and collector voltage changes. Such an analysis would require precise modelling of the output matching circuit to understand the impedance transformation when moving from the transistor carrier edge to the transistor chip itself. Since the purpose of the device evaluation was solely to adquately characterize the devices, so that appropriate conditions could be determined for failing devices under overstress conditions, an analytical model of the movement of the optimum collector load with drive and collector voltage was not deemed necessary.

IV STEP STRESS TESTS

A. INTRODUCTION

The objective of the step stress tests was to determine the levels of the three variables (drive, V_{cc}, and mismatch) at which device degradation begins to occur rapidly. Knowledge of these levels would make it possible to select conditions that yield a measurable degradation over the anticipated duration of the subsequent life tests (5000 hours). Three separate tests were planned in which the drive, collector voltage and output mismatch would gradually be increased, a step at a time, and held at each step for an interval of about 48 hours. Output power would be monitored for evidence of degradation. This would be continued until degradation occurred. The base plate of the modules was to be held at 60°C throughout these tests, simulating worst-case use conditions.

Only device No. 2 was tested under these conditions.

B. THE APPARATUS

Figure 35 is a block diagram of the RF chain used for the step/stress and life tests. The prime source of RF power was a Rhode and Schwarz CW generator capable of 3 watts output at 1.3 GHz. The output from this source was pulse modulated by a pin diode switch and amplified by an AN/TPS-59 50 watt power module. Further amplification was provided by a solid-state power module developed by the Heavy Military Equipment Department. It is capable of 200 watts output at 2ms with a 10% duty cycle. The output of the 200 watt module is split by a hybrid and is used to feed a 4-way and a 6-way splitter. The 4-way splitter was to be used for the high drive tests, while the 6-way splitter was to be used for the high V_{cc} and mismatch tests. A variable attenuator (not shown) was placed before one of the splitters so that the input to the two splitters could be varied independently.

Figure 36 is a photograph of the test set up. A Barnes RM-2A infrared microscope is located in the center between two splitters. The test modules are mounted on water-heated blocks maintained at 60°C by a circulating constant temperature water source. Each module has a separate dc power supply. A 25-channel recorder continuously monitors the current to the modules, as well as the input power to the splitters.

The infrared microscope was calibrated for Device No. 2 as follows: the voltage output of the infrared microscope was measured while focused on a transistor cell, with the device held at a known temperature. Because of the narrowness of the transistor cell, an objective lens with a 0.7 mil resolution was used for this and all subsequent measurements. The variation in the voltage was measured as a function of temperature, between 50° and 350°C, and a curve of response voltage versus temperature was obtained. The voltage measurements were made using the same oscilloscope used for subsequent temperature measurements. Similar curves were also plotted for the black paint used to determine flange temperature and for the calibrated black body reference source.

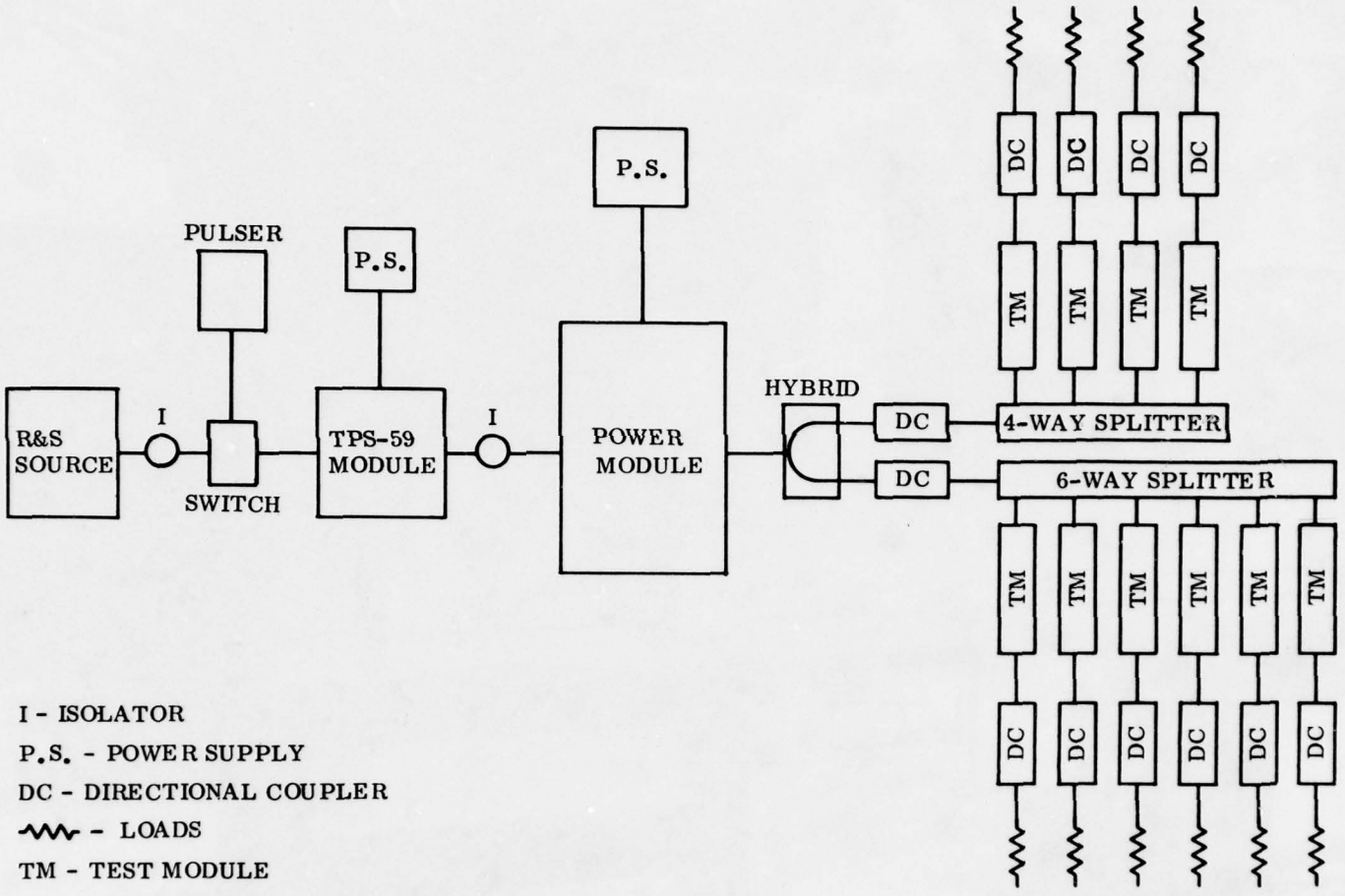

Figure 35. Schematic Diagram of RF Chain used for Life Tests

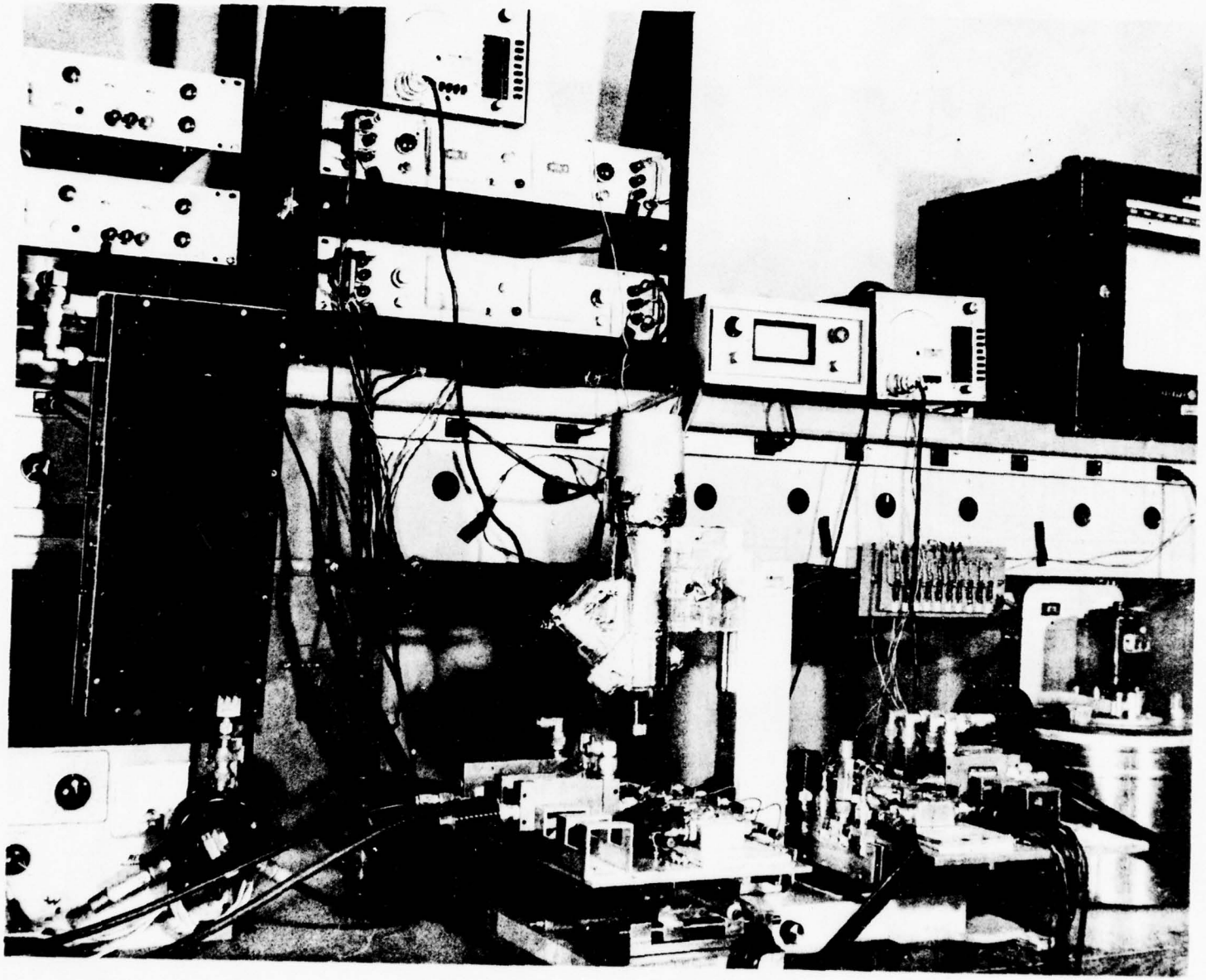

Figure 36. Test Setup for Step Stress and Life Tests

C. STEP STRESS TESTING

1. Voltage Test

The voltage step stress test was the first to be done. Initially a 1 millisecond pulse length was used with a peak input power of 10 watts and a 10% duty cycle. However, it was observed that at this pulse length very high junction temperatures were attained at relatively low values of V_{cc}. Since the objective of the tests was to stress the devices at moderate temperatures ($<180^{o}C$) and high collector voltages ($>35V$), it was decided to reduce the pulse length to 100μsec. The duty cycle remained at 10%.

During these tests a 24-hour step interval was used and the collector voltage was raised by approximately two volts at each step. The baseplate of the module was held at 60°C, and the temperature of the hottest cell was monitored continuously. The test was continued until the device failed.

Five devices were subjected to this step stress test. Two of the five failed for unknown reasons during the time the 1 ms pulse was employed. There were three apparently valid failures; these are described in Table XII.

TABLE XII. VOLTAGE STEP STRESS FAILURE SUMMARY

Device	V_{max}	V_{BD}(N)	T_{jmax}(°C)	Hours at V_{max}
Lot 5776-#11	37	58	218°C	1
Lot 5777-#7	46	59	260°C	12
Lot 5784-#7	37	58	232°C	2

The results indicate that there is significant variability in the voltage at which different devices fail. While two of the three devices failed after a short time at 37 volts, one operated for 12 hours at 46 volts. These results indicated that it may not be possible to select a single life-test voltage that is suitable for all devices.

All of the failures were catastrophic, with one or more cells destroyed at the time of failure. It was observed that the failed cells were not necessarily the hottest cell prior to failure.

2. Input Power Test

Device 5777-#14 was subjected to an input power step stress in which the input power was gradually raised as the collector voltage was held constant at a nominal 28 volts. The drive was gradually raised to 30 watts (compared to a 10-15 watt nominal level) over a period of 260 hours, and held there for 64 hours with no evident degradation. The device was then removed from stress and its dc characteristics were measured. No degradation in the junction leakages or dc charateristics were observed. The device was damaged in handling during these measurements.

The objective of the input power step stress and the planned high input power life test was to evaluate the effect of excessive drive on the failure mechanisms and the useful life of the device. The results would be used to assess the effect of the input power variability, which can be encountered in a microwave amplifier system in practice. The results of the input power step stress test indicated that the input power can be raised well above the range of any expected system variation for an appreciable length of time, with no apparent adverse effect on the device. This would indicate that a high input power life test may not be meaningful.

3. Combine Step Stress - Device Characterization

Because of the results of the voltage and input power step stress tests, a new approach was taken, with the concurrence of the RADC program monitor. Device 5777-#9 was subjected to a combined step stress in which the input power was raised from 10 to 16 watts as the voltage was increased to 40 volts. It failed after five minutes under these maximum conditions. The pulse length was held at 50μsec, with a 10% duty cycle. The peak power output was 70 watts. During the test it became clear that the device had become saturated in power output and that an increase in either the collector voltage or the drive did not yield an increase in power output

In order to evaluate the behavior of the devices under short pulse, high-drive and high-voltage conditions, in more detail, a series of characterization tests were done, with the devices mounted in the test fixture. Figures 37 and 38 present the results for device 5784-#20. In figure 37 the output power is plotted as a function of the input power for several values of collector voltage. In Figure 38 the junction temperature is plotted versus the input power for several values of V_{cc}. Figure 37 indicates that the device is saturated for drives above about 11 watts. Increasing the collector voltage increases the power out at saturation; however, above 32 volts the increase in power is very small. The device failed at V_{cc} = 34 volts, when the drive was increased from 15 to 17 watts. Figure 38 indicates that the rate of rise of junction temperature with drive was increasing under these conditions and that failure probably results from thermal runaway. Several other devices were characterized with similar results.

These results differ significantly from those described in Section III for the same devices. The devices saturate at a much lower drive and peak power output than during the earlier tests. An extensive effort was made to determine the cause of this discrepancy.

The discrepancy was traced to three separate causes. First, there was some difference in the calibration of the power meters at the two test sites. It was found that meters from two different manufacturers did not agree, whereas different meters from the same manufacturer did agree. Second, it was found necessary to use a small electrolyte capacitor at the V_{cc} terminal on the module to prevent the device from being charge limited during high pulsed-power operation. This capacitor had not been used in the Laboratory. Third, it was found that the contact between the substrate ground plane and the fixture ground was not adequate in the Laboratory modules. When the substrate was soldered to the fixture, the output power increased significantly. When these modifications were made, the agreement between the two locations was adequate.

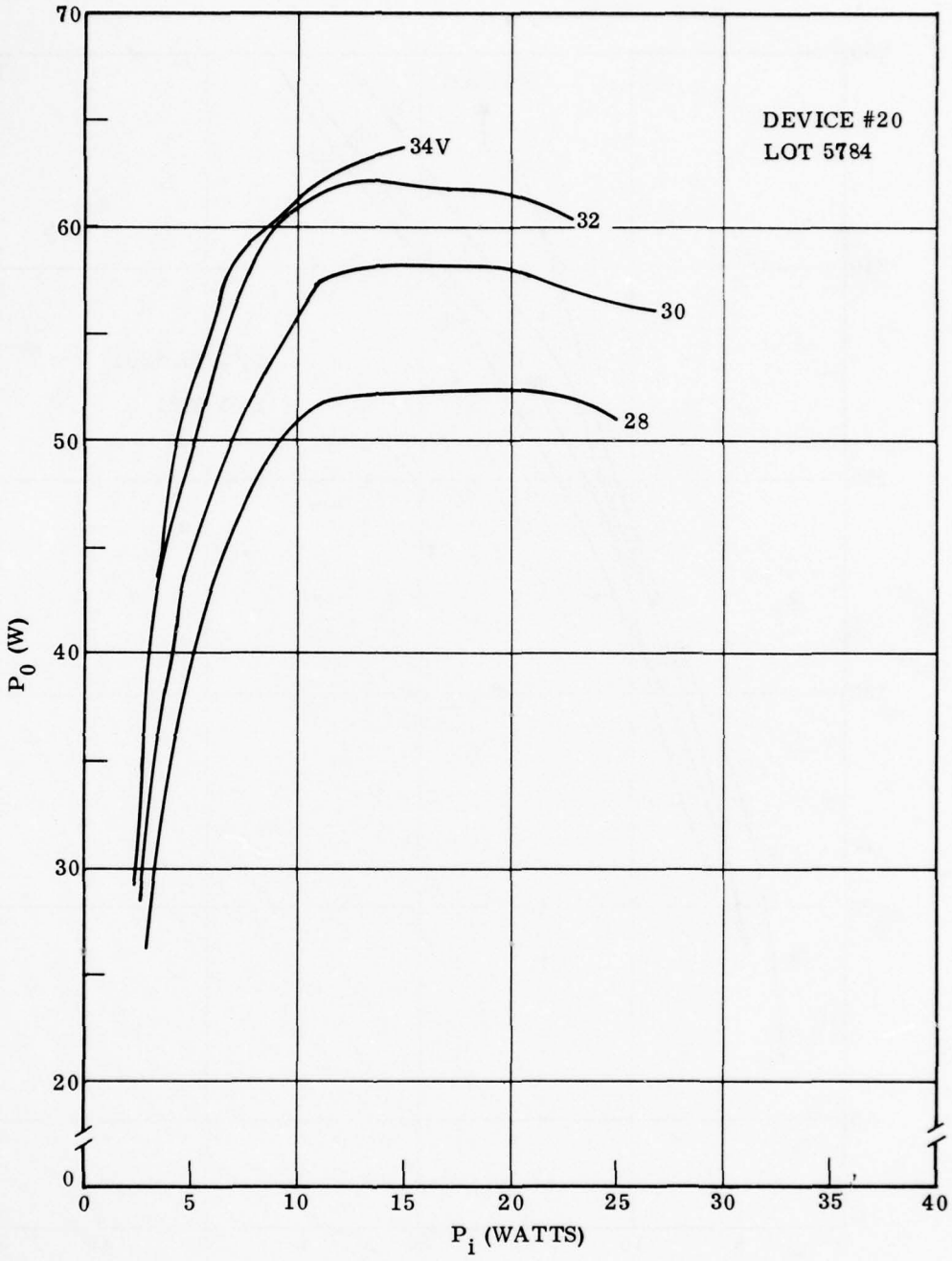

Figure 37 Output Power versus Input Power for Device 5784-20

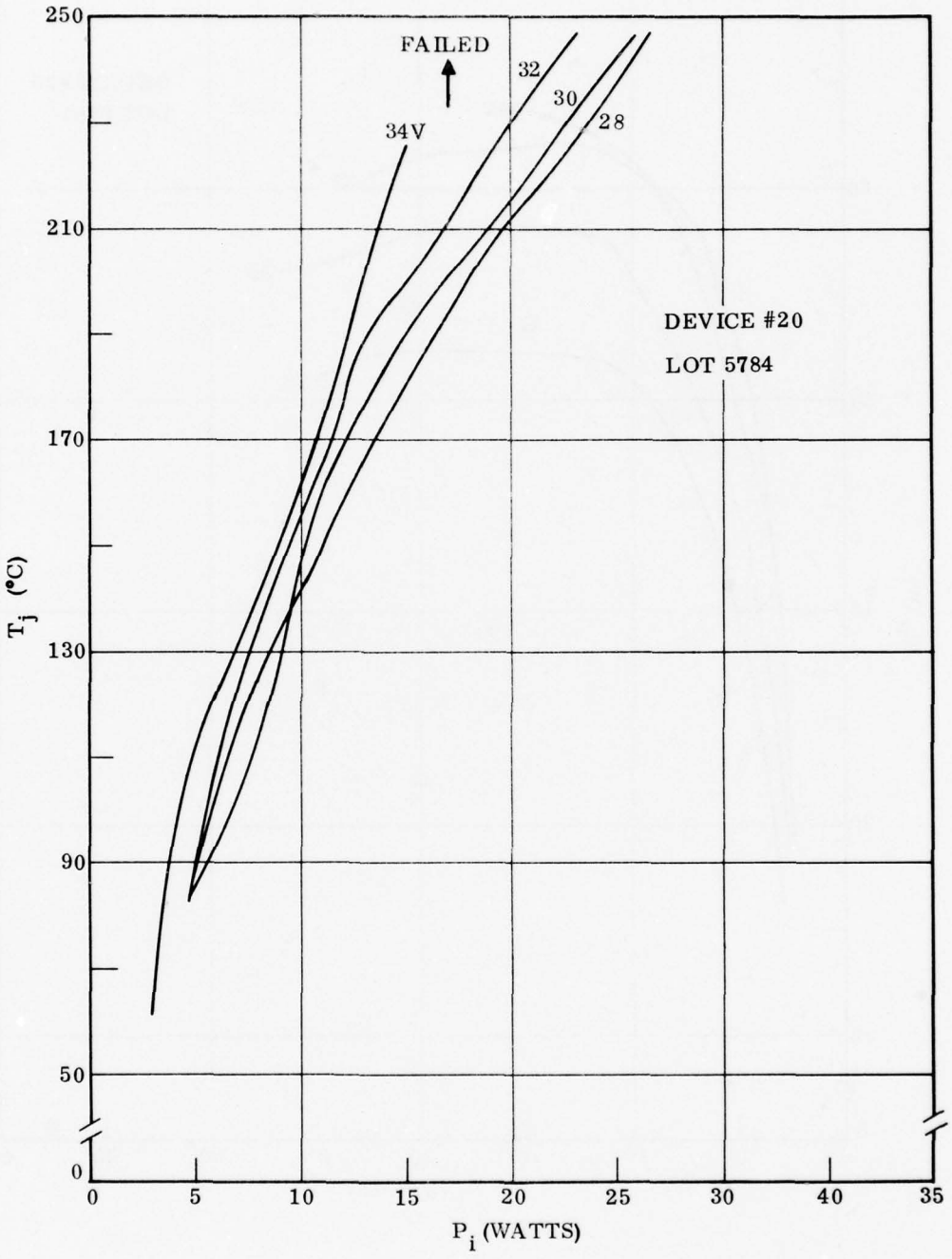

Figure 38. Junction Temperature versus Input Power for Device 5784-20

As part of the device characterization in the Laboratory, the temperatures of the different cells were measured as the collector voltage was increased. This was done for several different devices. The results are presented in Figure 39 for a typical device. Invariably, the end cell (#12) is significantly hotter than the rest at 28V. The other end cell (#1) is also hotter than the interior cells. As the voltage is increase, cell #12 remains hottest, but there is some variation in the relative temperature of the other cells. The detailed behavior varies from device to device.

4. Summary

The results of the step stress tests on the No. 2 device described above indicated that the original program plan, in which three separate life tests were to be performed, made little sense. It was demonstrated that very high drive alone does not cause failure or degradation after several hundred hours. Likewise, the collector voltage can exceed the nominal value by a large amount without failure. In both cases, the range over which these parameters could vary without failure was much larger than any that would actually be experienced. Therefore, life tests run under these conditions would not be representative of use stresses or overstresses.

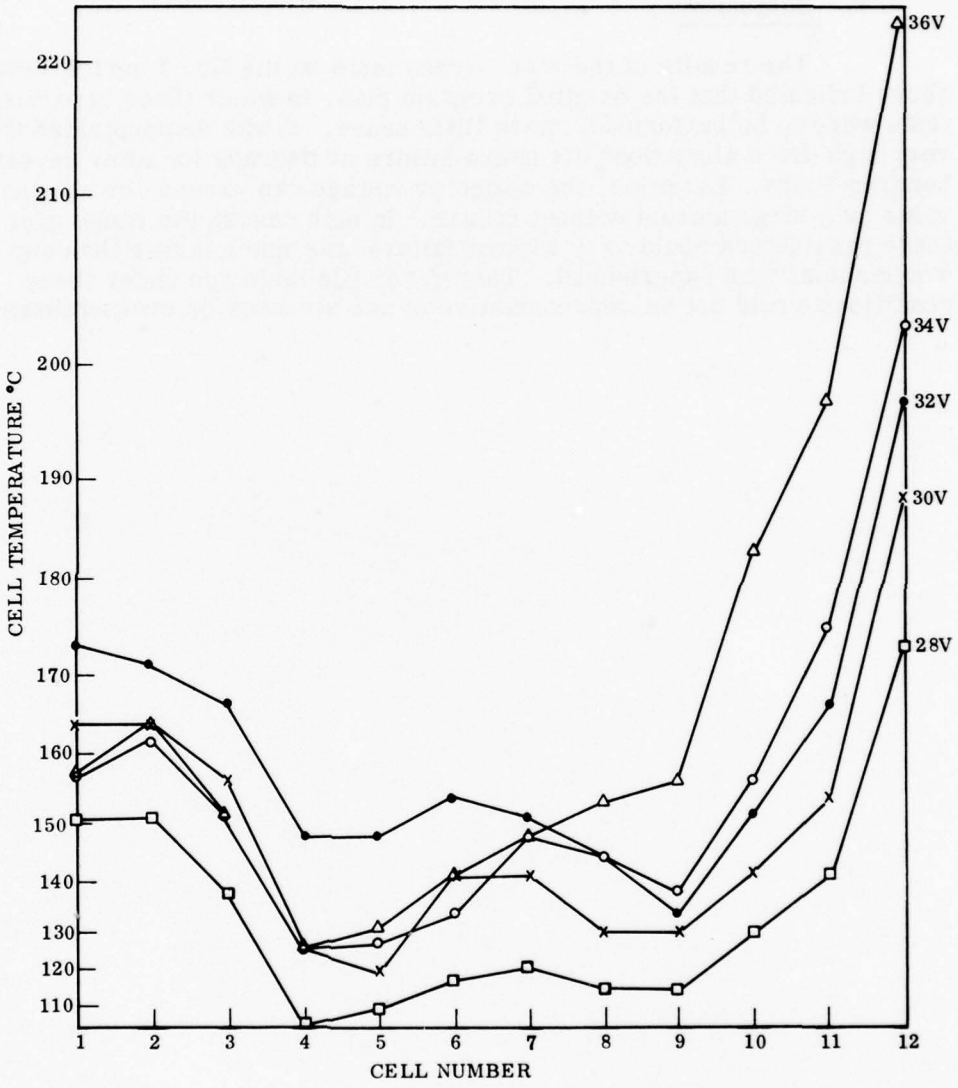

Figure 39 Variation of Cell Temperature Distribution With Collector Voltage

V. LIFE TESTS

A. INTRODUCTION

Because of the results of the step stress tests, the original plan for the life test phase of the program was altered. At the suggestion of the RADC program monitor, these tests were redesigned to evaluate the reliability and failure mechanisms when the devices are operated in the short pulse-high collector voltage mode. These and similar devices are operated in this mode in communication systems applications. Little is known of the long term reliability of these devices when operated in this mode in which the collector voltage substantially exceeds the nominal value of one half the collector-base breakdown voltage. Two life tests were planned. In one the devices would operate at 50 microseconds pulse length and 20% duty cycle, with a 15 watt input power, and at a collector voltage such that the junction temperature was approximately 180°C. The other test was run with the same pulse length and duty cycle, but with a 28V collector voltage. In this test the 180°C junction temperature was obtained by increasing the input power. The objective of the two tests was to determine whether any failure mechanisms occur under the high-voltage conditions, that do not occur at nominal voltages.

B. APPARATUS

The apparatus used was the same as that used for the step stress test described in Section IV-B. The six-position test rack was used for the high-voltage test, while the four position rack was used for the nominal voltage-high drive test.

C. HIGH VOLTAGE LIFE TEST

1. Procedure

Twelve (12) devices were stressed in the high-voltage life test. The procedure was as follows: Each device was mounted in the module on the heated block and slowly brought up in both input power and collector voltage to 15 watts and 28 volts, respectively. The cells of the device were scanned with the infrared microscope and the hottest cell was determined. Each cell temperature was recorded. The device was allowed to operate under these conditions, usually overnight, and its stability was noted. The collector voltage was then gradually increased until the hottest cell was approximately 180°C. Daily, all of the cell temperatures, the power input and the collector current were recorded. If the temperature drifted away from 180°C, the collector voltage was adjusted to compensate.

2. Results

The results of the tests are summarized in Table XIII. The maximum test time for any device was 745 hours (Device 3-5782). Ten (10) of the twelve devices failed catastrophically. The circumstance of failure varied from device to device, but some common features were noted. Most of the devices failed within a few hours of the time the voltage was raised. For example, device 14-5783 was slowly raised in voltage, over a 120 hour

TABLE XIII . HIGH VOLTAGE LIFE TEST SUMMARY

Device	Time on Test	V_{cc}(V)	Comments
3-5783	745	39 - 41	Failed 4 hrs. after bringing back to 41 V - 12 watts degradation.
8-5784	20	38	Failed
14-5783	120	37	Failed 1.5 hrs. after raising to 37.5 V.
20-5782	1	41	Failed
21-5782	< 1	28	Reason unknown
17-5783	< 1	32	Reason unknown
18-5783	150	33	Failed when power supply failed.
20-5783	568	35 - 39	Failed 91.5 hrs after raising to 39 V. No degradation. Unstable input.
11-5784	464	38.5-41.5	No degradation.
13-5784	312	34 - 35.5	Down 17 watts - after bringing back on test.
14-5784	497	39 - 43.5	6 watt degradation - failed.
12-5783	8	37 - 39.5	Failed after 4 hrs. at 39.5 V.

period, to 37.5 volts, and failed 1.5 hours later for no apparent reason. Likewise, No.12-5783 failed after 4 hours at 39.5 volts. Some devices, such as No. 20-5783, had operated for many hours at elevated voltage, but failed in a few hours after increasing the voltage. Device No. 3-5782 operated for hundreds of hours at 41V, was turned off for dc evaluation, and failed a few hours after it was brought back to 41V. Rarely did a device fail after an extended time at a constant voltage. This behavior is consistent with the step stress test results, in which two of the three devices failed a few hours after raising the voltage to 37 volts.

Only three of the devices had any apparent RF degradation prior to failure. Device No. 3-5782 was observed to be down in power after 300 hours at 41 volts. It was removed from test for dc evaluation and failed four hours after resuming the test.

Device No. 13-5784 showed no RF degradation after 312 hours at 34 to 35.5 volts. The test was shut down temporarily and, when resumed, the device was 17 watts lower in power output. It is obvious that the life test itself did not cause the degradation It may have been due to the temperature cycling accompanying shutdown. Device No. 14-5784 was observed to be degraded by six watts in power output after 497 hours at 39 to 43.5 volts. It subsequently failed.

D. HIGH DRIVE LIFE TEST

The high drive-28 volt life test was started with three devices. The test continued for several hours, at which time, the power available from the input power module decreased significantly. An investigation showed that one or more of the power amplifiers in the power module had failed. Since this power module was of a unique design, and no replacement modules or devices were available to replace the failed units, repair was impossible within the period of this program. As an alternative, it was decided to place one unit on test using the single cell test facility at the Heavy Military Equipment Department (HMED), where the characterization test had been done. This device was operated at 41 watts input power, 50 microseconds, 20% duty cycle, and 28 volts for 625 hours. No RF degradation was observed. The junction temperature was approximately 195°C during this interval.

The device was removed for dc evaluation and a comparison was made with the high voltage life test survivors.

VI. DELIBERATE FAILURES

Following device characterization, several, each of devices No. 2, 3 and 4 were deliberately overstressed by increasing either the drive, collector voltage or load VSWR, while constraining the other two variables to the nominal operating level. In this way, failures were induced which were known to be due to a particular overstess. Failure analysis was then performed to determine subtle differences in the failed units, which could then be related to the specific overstress. As expected with this type of testing, all of the failures were catastrophic and occurred after a relatively short operating time.

A. DEVICE #2

1. Summary of Device #2 Failure Conditions

Four Device #2 transistors were deliberately caused to fail by increasing the input drive, the collector voltage and the load VSWR. The performance of the devices into a 50-ohm load is shown in Table XIV. Following this characterization, the overstress testing was performed while the peak junction temperature of the hottest cell was monitored. The stress testing consisted of incrementally increasing the drive or collector voltage until the transistor was destroyed. The transistor was operated for several minutes at each stress level and the operation the device was recorded. The details of the stress testing for the group of Device #2 transistors is shown in Table XV. The table lists the drive, collector voltage and VSWR combination under which each transistor was progressively tested until failure. The summary of the actual failure conditions for the group of Device #2 overstress failures is shown in Table XVI. Failure occurred for all devices when a peak junction temperature of approximately 300°C was reached regardless of how the device was overstressed.

2. Analysis

All four of the #2 devices were analyzed and compared visually in an attempt to determine the distinguishing characteristics of failed devices from different causes.

Device No. S-1686-2, which failed under high drive conditions, is shown in Figure 40. All cells of the device were melted as were all the emitter and base wires. The molten gold wires have fallen across the metallization gap on the substrate, between the collector pad and the ground, and shorting the gap.

Device No. S-1688-2, the high V_{cc} failure, is shown in Figure 41. The cell damage is limited to six end cells, and their connecting wires. Once again, the metallization gap is shorted. The wires to one of the collector shunt capacitors are fused open. The metal bridge adjacent to the failed cells is melted, as is the collector metallization beneath it, indicating that arcing occurred between the bridge and the metallization.

TABLE XIV. NOMINAL PERFORMANCE OF DEVICE 2 TRANSISTORS WHICH WHERE DELIBERATELY FAILED

				Cell Temperature Profile O_c											
Device	P_{in}	P_{out}	I_c	1	2	3	4	5	6	7	8	9	10	11	12
S-1686-2	8.5	55	3.2	82	82	70	70	58	58	58	70	70	70	82	82
	11.5	55	3.2	82	82	70	70	58	58	58	70	70	75	82	82
S-1686-4	8.5	55	3.2	82	82	75	70	70	58	58	70	70	75	82	82
S-1686-3	8.5	55	3.2	75	75	70	70	70	58	58	58	70	70	75	82

TABLE XV. HISTORY OF STRESS LEVELS FOR DEVICE 2 DELIBERATE FAILURES.

Pulse Length (μsec)	P_{in} (watts)	V_{cc} (volts)	P_o (watts)	I_c (amps)	T_j (^oC)	LOAD
		Device S-1686-2				
100	20	28	79	5.1	85	50 ohms
	30	↓	77	6.0	135	↓
	40		69	6.5	160	
	50		60	6.9	190	
	60		53	7.3	220	
	70	↓	46	7.6	255	↓
	80	28	41	7.9	295	50 ohms
		Device S-1686-4				
50	10	28		3.5	90	VSWR=3.0:1
	15	↓		4.6	108	↓
	20			5.2	118	
	25			5.7	144	
	30			6.2	155	
	35			6.3	174	
	40			6.5	190	↓
	10			3.3	110	VSWR=
	15			4.4	132	
	20			5.2	158	
	25			5.9	174	
	30	↓		6.4	186	
	25	Failed Into VSWR = ∞ :1				

TABLE XV. (Continued)

Pulse Length (μsec)	P_{in} (watts)	V_{cc} (volts)	P_o (watts)	I_c (amps)	T_j (^oC)	LOAD
		Device S-1686-3				
50	30	28	10	3.4	124	VSWR=3:1
100	↓	↓	↓	3.4	149	↓
150				3.5	165	
200				3.6	180	
250				3.6	192	
300				3.6	195	
400				3.6	200	
500				3.6	210	
600				3.6	212	
700				3.6	215	
800				3.6	226	
900				3.6	227	
1000				3.6	231	
1200				3.5	255	
1400				3.4	258	
1600				3.4	264	
1800				3.4	267	
2000				3.4	267	
2500			↓	3.4	267	
3000			10	3.4	272	
2000			12	3.9	290	
2000			13	4.1	300	
2000	↓	↓	13.5	4.2		↓
2000	30	28	14	4.3		VSWR=

TABLE XV. (Continued)

Pulse Length (μsec)	P_{in} (watts)	V_{cc} (volts)	P_o (watts)	I_c (amps)	T_j (^oC)	LOAD
		Device S-1686-2				
100	12	28	57	3.4	90	50 ohms
		29	59	3.45	90	
		30	61	3.5	90	
		31	61	3.5	90	
		32	63	3.5	94	
		33	64	3.5	94	
		34	65	3.55	104	
		35	65	3.55	110	
		36	65	3.55	110	
		37	66	3.55	110	
		38	66	3.55	110	
		39	67.5	3.55	117	
		40	68.5	3.6	125	
		41	68.5	3.6	132	
		42	69	3.6	136	
		43	70	3.6	141	
		44	70.5	3.6	146	
		45	71	3.6	150	
		46	71	3.6	156	
		47	71.5	3.65	158	
		48	72	3.65	162	
		49	72	3.7	174	
		50	73	3.7	180	
		50.5	73	3.7	186	
100	12	51	74	3.75	188	50 ohms

TABLE XV. (Continued)

Pulse Length (μsec)	P_{in} (watts)	V_{cc} (volts)	P_o (watts)	I_c (amps)	T_j (^oC)	LOAD
100	12	52	75	3.75	196	50 ohms
↓	↓	53	78	3.8	204	↓
↓	↓	54	76	3.85	222	↓
↓	↓	55	76	3.85	231	↓
↓	↓	56	75	3.90	240	↓
↓	↓	57	74	3.9	247	↓
↓	↓	58	73	3.95	261	↓
↓	↓	59	71	4.0	267	↓
↓	↓	60	69	4.05	285	↓
100	12	61	67	4.15	308	50 ohms

TABLE XVI. SUMMARY OF DEVICE 2 DELIBERATE FAILURES

Device	P_{in}	V_{cc}	$\tau(\mu s)$	Duty Factor	VSWR	T_j °C	Failure		
							P_{in}	V_{cc}	VSWR
S-1686-2	80	28	100	10%	1:1	295	X		
S-1686-3	14	28	2000	10%	3:1	≈300			X
S-1686-4	30	28	50	10%	∞:1	≈295	X		X
S-1688-2	12	61	50	10%	1:1	≈308		X	

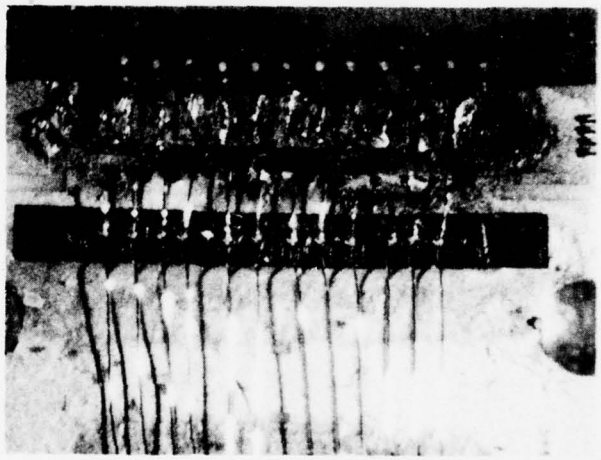

Figure 40. Device No. S-1686-2, After Failure
A High Drive Failure

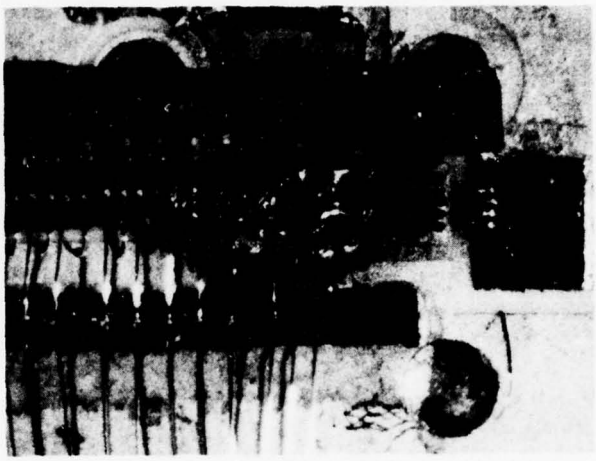

Figure 41. Device No. S-1688-2, After Failure
A High V_{cc} Failure

Device No. S-1686-4, a high drive and high VSWR failure is shown in Figure 42 . The eight center cells are melted, along with their connecting wires, and the metallization gap is shorted.

Device No. S-1686-3, the VSWR failure, was similar to other failures, with nothing to distinguish it from them. The only difference noted in the four failures were the arcing to the bridge in the high V_{cc} failure, and the fact that all of the cells on the high drive failure were melted, compared with 6 or 8 cells on the other failed devices. It is probable that all devices involved a thermal runaway of the hot cells, resulting in cell melting, a high collector-base current, and wire melting. Once the wires fell across the metallization gap, the resulting short formed a direct path from collector to ground, bypassing the chip.

The arcing between the bridge and the collector metallization on the high V_{cc} failure may have been initiated by the vaporized metal and silicon emanating from the chip at the time of failure. It is also possible that the arcing could have caused the failure.

The similarity in the failed devices is consistent with the observation that the hot cell temperature at the time of failure was nearly the same for all devices ($\sim 300^{o}C$). This would indicate that failure did result from overheating of the cells, followed by thermal run away, and that the cause of the overheating does not appreciably effect the end result.

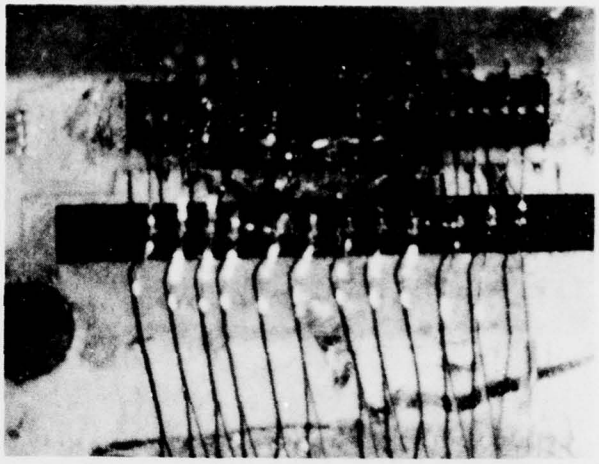

Figure 42. Device No. S-1686-3, After Failure
A Combined High V_{cc} and High Drive Failure

B. DEVICE #3

1. Summary Of Failure Condition

Eight Device #3 transistors were overstressed to induce failure following characterization under normal operating conditions. Each device was again stressed at a particular level for several minutes to allow the device junction temperature to equilibrate. Performance data were recorded and then the stress level was increased by raising the input drive or the collector voltage. This process was repeated until the device failed.

Device #3 is a particularly rugged UHF transistor, designed to operate under long-pulse conditions. Initial testing indicated that the transistor could easily handle a 3 dB increase in the input drive when operated at a pulse length of one millisecond. Consequently, all stress testing was initially started with an input drive level of 35 watts. This is approximately 3 dB over the normal drive of 16 watts, at which the transistor is designed to operate.

The stress level history of the devices tested is shown in Table XVII. In all cases an increase in a single test parameter (i.e. P_{in}, V_{cc} or VSWR) could not induce failure. Table XVIII summarizes the stress levels at which each device failed. In all cases the input drive was 3 to 6 dB above normal, and the collector voltage was above 80% of the collector-base reverse breakdown voltage. In most cases the VSWR = 3:1 was also required.

2. Analysis

Three of the failed devices were analyzed (#12, #21 and #11). These three represented the full range of P_{in}, V_{cc}, and VSWR.

TABLE XVII. DEVICE 3 OVER DRIVE, OVERVOLTAGE AND HIGH VSWR FAILURES

Serial No.	P_{in} (Watts)	V_{cc} (Volts)	I_c (Amps)	P_{out} (Watts)	Load	Pulse Length	Peak Junction Temperature T_j °C	Time at Each Level	Remarks
#3	35	40	6.85	174	50 ohms	1 μsec	130	10 min. at each level	Cell #24
	40	40	7.35	180	↓	↓	142	↓	
	44	40	7.65	185			155		
	50	40	8.0	188			177		
	50	45	8.3	220			190		
	55	45	8.6	222		1 μsec	210		
	55	50	8.9	240		1 μsec	240		
	35	40	7.0	180		2 μsec	132		
	40	40	7.3	185			143		
	44	40	7.7	190			156		
	50	40	8.0	190			171		
	55	40	8.3	191			190		
	55	45	8.6	225			225		
	62	45	8.9	222	↓		247		
	62	50	9.1	240	50 ohms	2 μsec	285	↓	
	35	40	6.9		3:1 Mismatch	1 μsec	200	10 min at each level	

TABLE XVIII. SUMMARY OF DEVICE 3 DELIBERATE FAILURES

Device	P_{in} (Watts)	BV_{CES}	V_{cc} (Volts)	τ (μs)	Duty Factor	VSWR	T_j °C	Failure		
								P_{in}	V_{cc}	VSWR
3	58	61	50	1000	10%	3:1	≈235	X	X	X
5	35	61	55	1000	10%	3:1	142	X	X	X
7	60	66	52	1000	10%	3:1	≈313	X	X	X
8	55	64	55	1000	10%	3:1	267	X	X	X
11	35	63	60	1000	10%	3:1	≈320	X	X	X
12	55	62	50	1000	10%	3:1	≈308	X	X	X
14	50	63	50	1000	10%	3:1	≈335	X	X	X
21	62	62	50	1000	10%	3:1	345	X	X	X

Figure 43 shows device No. 12, after failure. Damage was confined to one cell and its associated wires. This cell was on the output side of the chip and the gap between the collector metallization on the substrate and the ground metallization at the output edge of the carrier was shorted by melting base wires. The wires connecting the collector metal at the top of the carrier with the chip bonding pad were also melted, indicating a high collector current.

Figure 44 shows device No. 21. One half the cells have melted, as well as the collector and emitter wires. The gap between the chip bonding pad and the ground metallization on the input side of the chip is shorted by metal from the wires.

Figure 45 shows device No. 11. A single cell has failed along with the emitter wire and the two base wires associated with it. The input gap was shorted by the falling wire.

Once again, while there are differences in the detailed failure characteristics, these differences seem to be associated more with the location of the failed cell, rather than the cause of failure. The highest drive failure had the most widespread damage, as with the device type-2 failures. Cell overheating, in all three cases, would seem to be the cause of failure. This is consistent with the observation that the temperature of six of the eight failed devices had hot cell temperatures in the 308°C to 345°C range at the time of failure.

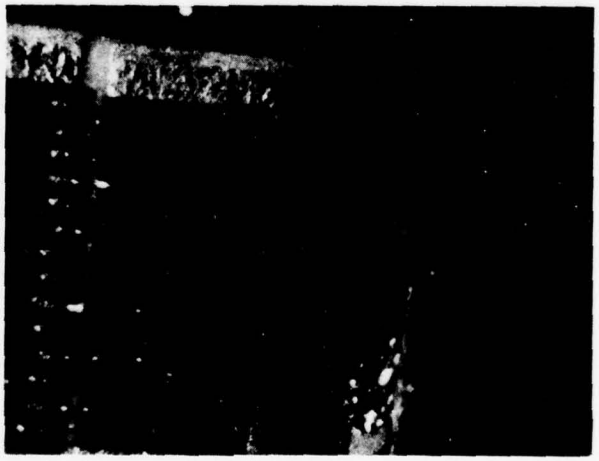

Figure 43. UHF Device No. 12, After Failure

Figure 44. UHF Device No. 21, After Failure

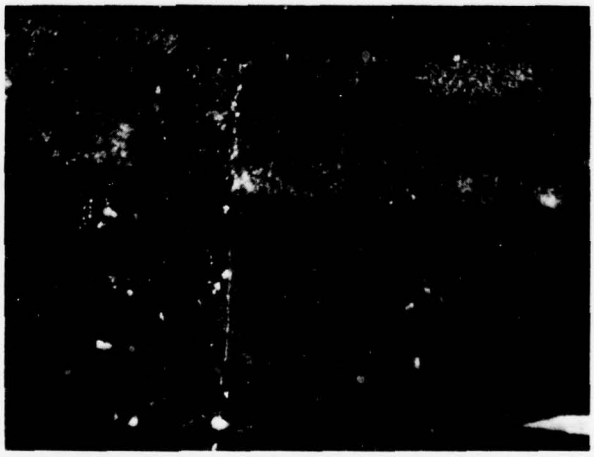

Figure 45. UHF Device No. 11, After Failure

TABLE XVII (Continued)

Serial No.	P_{in} (Watts)	V_{cc} (Volts)	I_c (Ampls)	P_{out} (Watts)	Load	Pulse Length	Peak Junction Temperature T_j °C	Time at Each Level	Remarks
	35	45	7.1		3:1 Mismatch	1 μsec	230		
	35	50	7.3		↓	↓	265		
	40	50	7.6				277		
	44	50	8.0				295		
	50	50	8.3				315		
	55	50	8.7		3:1 Mismatch	1 μsec	335		
	58								Failed when pin raised
# 7	35	50	6.9		3:1 Mismatch	1 μsec	243	1 min.	Cell # 20
	48	50	8.6				283	17 hours	
	60	50	9.3				313	4 hours	
					3:1 Mismatch	1 μsec			
	60	52							Failed when voltage raised

TABLE XVII (Continued)

Serial No.	P_{in} (Watts)	V_{cc} (Volts)	I_c (Amps)	P_{out} (Watts)	Load	Pulse Length	Peak Junction Temperature T_j °C	Time at Each Level	Remarks
#11	35	40	6.8	178	50 ohms	1 μsec	115	1 min	Cell #13
	35	45	7.1	205			122	1 min	
	35	50	7.3	219			145	1 min	
	35	55	7.5	221			180	1 min	
	40	55	8.0	234			200	7 min	
	45	55	8.4	242			213	5 min	
	50	55	8.8	246			235	5 min	
	55	55	9.0	246			240	6 min	
	55	60	9.1	236			300	5 min	
	55	60	9.1	242			300	24 min	storage capacitor failed on power supply
	55	60	9.5	258			285	21 hours	
	55	60	9.4	256			280	6 hours	CAP replaced
	55	60	8.7	241			272	66 hours	
	55	60	8.7	241			272	7 hours	

TABLE XVIII. (Continued)

Serial No.	P_{in} (Watts)	V_{cc} (Volts)	I_c (Amps)	P_{out} (Watts)	Load	Pulse Length	Peak Junction Temperature T_j °C	Time at Each Level	Remarks
	55	60	8.7	234			272	20 hours	
	55	60	8.7	239			273	21 hours	
	55	60	8.7	234	50 ohms		273	45 min	
	35	40	6.8		3:1 Mismatch		165	1 min	
	35	60	7.2		3:1 Mismatch	1 μsec	320		Failed when power in was increased slightly
#12	35	40	6.8	175	50 ohms	1 μsec	140	10 min	Cell# 1
	40	40	7.2	180			153		
	44	40	7.5	184			166		
	50	40	7.9	187			180		
	55	40	8.3	187			203		
	62	40	8.6	185			225		
	62	45	8.8	212			255		

TABLE XVII (Continued)

Serial No.	P_{in} (Watts)	V_{cc} (Volts)	I_c (Amps)	P_{out} (Watts)	Load	Pulse Length	Peak Junction Temperature T_j °C	Time at Each Level	Remarks
	62	50	8.9	230		1 μsec	297		
	40	40	6.75	172		2 μsec	157		
	44	40	7.1	178			173		
	50	40	7.4	180			190		
	55	40	7.8	182			203		
	55	40	8.1	182			225		
	55	45	8.3	212			264		
	55	50	8.5	230	50 ohms	2 μsec	308		Unit failed when power was increased .1 dB
#14	35	40	6.7	160	50 ohms	1 μsec	212		Cell #7 was 2.5 × as hot as next hottest cell

TABLE XVII. (Continued)

Serial	P_{in} (Watts)	V_{cc} (Volts)	I_c (Amps)	P_{out} (Watts)	Load	Pulse Length	Peak Junction Temperature T_j °C	Time at Each Level	Remarks
#14	40	40	7.0	164	50 ohms	1 μsec	237	10 min	
	44	40	7.3	165	↓	↓	250	↓	
	44	45	7.4	185			290		
	44	50	7.5	195			335		
	50	50			↓	↓		↓	Failed After Approximately 10 sec.
#5	35	40	6.5	156	50 ohms	1 μsec	142	10 min	Cell #5
	35	55			3:1 Mismatch				Failed While Increasing V_{cc} to 55 volts
#8	35	40	6.4	153	50 ohms		116	10 min	Cell #24
	55	50	8.1				285	24 hrs.	
	55	50	8.1		3:1 Mismatch	1 μsec	267	2 hrs.	

TABLE XVII (Continued)

Serial No.	P_{in} (Watts)	V_{cc} (Volts)	I_c (Amps)	P_{out} (Watts)	Load	Pulse Length	Peak Junction Temperature T_j°C	Time at Each Level	Remarks
#8	55	55	Failed						Failed While increasing V_{cc} to 55 volts
#21	35	40	7.1	185	50 ohms	1 μsec	120	10 min at each level	Cell #24
	35	45	7.3	212			135		
	35	50	7.6	225			165		
	40	50	8.0	236			175		
	44	50	8.5	246			185		
	50	50	8.8	252			200		
	55	50	9.2	256			220		
	62	50	9.5	258	50 ohms		245		
					3:1 Mismatch				
	35	40	7.0		VSWR = 3.1		188		
	35	45	7.2						

TABLE XVII (Continued)

Serial No.	P_{in} (Watts)	V_{cc} (Volts)	I_c (Amps)	P_{out} (Watts)	Load	Pulse Length	Peak Junction Temperature T_j °C	Time at Each Level	Remarks
#21	35	50	7.3				247		
	40	50	7.75				260		
	44	50	8.1				277		
	50	50	8.5				297		
	55	50	8.8				320		
	62	50	9.1				335		145 cm
	62	50	9.3				350	4 hrs	150 cm
	62	50	9.3		3:1 Mismatch	1 μsec	345	10 min	Failed

C. DEVICE #4

1. Summary Of Failure Conditions

Failures were deliberately induced in four Device #4 transistors. These S-band devices were test at 3.3 GHz with a 500 microsecond pulse length and 10% duty factor. Before testing at elevated stress levels began, the devices were characterized into a 50 ohm load under normal input drive and collector voltage. The temperature profiles for the 8-cell parts are shown in Table XIX along with the RF data. Following characterization; the devices were tested to the levels shown in Table XX. Two devices were subjected to increased collector voltages and a single device was subjected to high drive and mismatch. A summary of the stress testing is shown in Table XXI.

TABLE XIX. NOMINAL PERFORMANCE OF DEVICE 4 TRANSISTORS WHICH WERE DELIBERATELY FAILED.

Device	P_{in}	P_{out}	I_c	1	2	3	4	5	6	7	8
1100-3	1.25	6.7	.69	75	86	75	86	75	86	95	79
1100-5	1.25	7.2	.71	86	86	75	86	82	79	79	79
1100-12	1.25	8.2	.72	75	86	75	75	79	77	79	79
1100-4	1.25	7.6	.75	86	95	79	79	79	79	92	86

2. Analysis

All four failed No. 2 devices were inspected. Figure 46 shows device No. 1100-3, the high VSWR feature. It is characterized by localized cell melting, near the base wire contact, collector wire melting resulting in shorting of the metallization gap between the die bond pad and the ground metallization at the output side of the carrier. The collector metallization on the top of the carrier is also melted near the series inductor.

Figure 47 shows device No. 1100-5, a high V_{cc} failure. It is very similar to No. 1100-3, except that the damage to the collector metallization is much widespread. Device No. 1100-4, the other high V_{cc} failure was almost identical.

Figure 48 shows device No. 1100-12, the high drive failure. Once again, the appearance is similar to the previous samples, with the damage to the collector metallization limited to the input inductor.

Again, all of the failures are quite similar. The major difference lies in the extent of the damage to the collector metallization. The greatest damage occurs at the higher collector voltages, which is not surprising. The damage may be due to the current surge accompanying device failure. The high rate of current rise may cause the voltage across the series inductor to become high enough for breakdown to occur across the inductor. The resulting arcing may have caused the observed damage.

TABLE XX. HISTORY OF STRESS LEVELS FOR DEVICE 4 DELIBERATE FAILURES.

Device	P_{in} (Watts)	V_{cc} (Volts)	P_o (Watts)	I_o (Amps)	T_j (°C)	Load
1100-3	1.25	32		.95	187	VSWR = 3:1
	↓	33		.96	195	↓
		34		.98	214	
		35		.99	238	
		36		.99	260	
		37		.99	285	↓
	↓	37.2		.98		Failed
1100-4	1.25	28	7.7	.68	81	50Ω
	↓	29	8.2	.7	85	↓
		30	8.4	.73	86	
		31	8.6	.75	103	
		32	8.6	.77	111	
		33	8.9	.79	129	
		34	9.0	.81	142	
		35	8.8	.81	146	
		36	8.7	.81	158	
		37	8.6	.82	174	
		38	8.4	.84	190	
		39	8.3	.8	206	
		40	7.8	.87	232	
		41	7.3	.89	275	↓
	↓	41.3	Failed at Approximately 295°			

TABLE XX. (Continued)

Device	P_{in} (Watts)	V_{cc} (Volts)	P_{out} (Watts)	I_c (Amps)	T_j (^oC)	Load
1100-12	1.25	28	9	.7	75	50 ohms
	1.5	28	11	.83	92	↓
	2.0	28	12	.96	111	
	2.5	28	12	1.08	141	
	3.0	28	11	1.2	183	
	3.5	28	10	1.26	198	
	3.5	29	10	1.26	204	
	3.5	30	10	1.28	227	
	3.5	31	9.5	1.30	265	↓
	3.5	31.8	Failed		290	50 ohms
1100-5	1.25	28	8	.7	81	50 ohms
	↓	32	8.7	.75	96	↓
		33	9.2	.78	111	
		34	9.4	.79	119	
		35	9.4	.79	129	
		36	9.6	.82	142	
		37	9.6	.83	147	
		38	9.6	.84	158	
		39	9.5	.85	174	
		40	9.4	.86	187	
		41	9.3	.88	202	
	↓	42	9.0	.91	218	↓
	1.25	43	Failed			50 ohms

TABLE XXI. SUMMARY OF DEVICE 4 DELIBERATE FAILURES

Device	P_{in} (Watts)	V_{cc} (Volts)	τ (μs)	Duty Factor	VSWR	T_j (^oC)	Failure		
							P_{in}	V_{cc}	VSWR
1100- 3	1.25	37.2	500	10%	3:1	285			X
1100- 5	1.25	43	500	10%	1:1	218		X	
1100-12	3.5	31.8	500	10%	1:1	290	X		
1100- 4	1.25	41.3	500	10%	1:1	295		X	

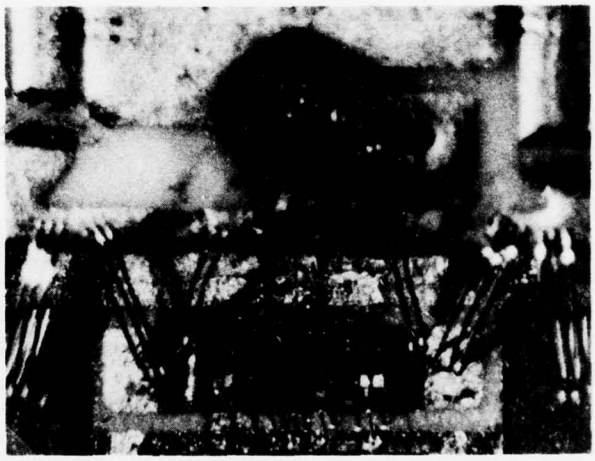

Figure 46. S-Band Device No. 1100-3, After Failure

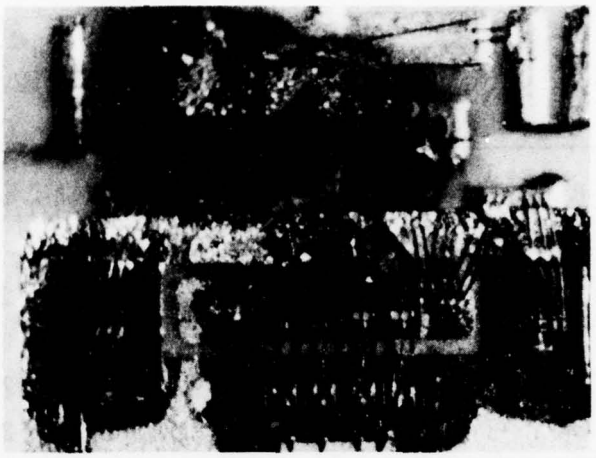

Figure 47. S-Band Device No. 1100-5, After Failure

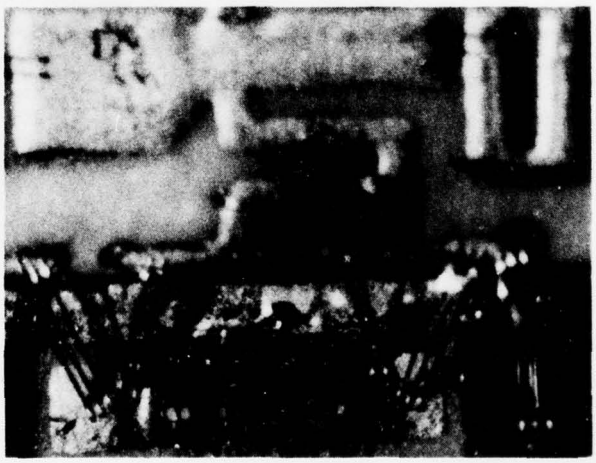

Figure 48 . S-Band Device No. 1100-12, After Failure

D. SUMMARY OF RESULTS

The results indicate that catastrophic failure of the device studied may be primarily a matter of reaching a critical junction temperature and that the means of reaching that temperature may not be of great significance. This temperature would appear to be in the 300°C to 350°C range, as measured by the IR microscope. The actual hot-spot temperature may be somewhat greater, since the IR measurement is averaged over a finite area on the surface of the devices. The failure mechanism may be the equivalent of second breakdown in lower frequency devices.

There is also evidence that, when the critical temperature is reached by means of excess input power, the failure is often more widely distributed over the transistor cells than if excess VSWR or V_{cc} are responsible. This is probably due to the emitter ballasting, which tends to distribute the input power more evenly, particularly under high-drive conditions. The S-Band device, which is not emitter ballasted, did not exhibit the tendency.

It should be noted that a device with a localized defect, may behave differently than those studied here. For example, a crack propagating across a cell can result in a localized breakdown and failure at much lower temperatures. It is believed that many of the failures observed in the life-test portion of the program were defect related.

VII. FAILURE ANALYSIS

A. INTRODUCTION

Failure analysis on this program was complicated because most of the devices failed catastrophically; thus evidence of the cause of failure was difficult to obtain. None of the survivors of the high-voltage life test were degraded, with the exception of No. 13-5784. As discussed in Section V, the observed degradation of that device is suspect.

The analysis of the failed devices consisted of extensive electrical probing of surviving cells, visual characterization of all devices, and comparison of thermal data taken during the life tests with the visual and electrical observations. The results of these studies enable us to make some tentative conclusions relative to the possible causes of failure.

B. D.C. CHARACTERIZATION

During the life tests, two devices were removed from stress after several hundred hours on test, without failure. Device No. 3-5782 was removed after 500 hours, examined visually, and its d.c. characteristics were measured. It was observed at that time that, although the low-level junction leakage characteristics were unchanged, the d.c. gain of the device had decreased by an order of magnitude. Figures 49 and 50 are curve tracer photos showing the characteristic curves for this device before and after stress. At the time of this evaluation the device had degraded six watts in output power. As discussed earlier, the device subsequently failed catastrophically. Device No. 13-5784 was removed after 317 hours on test and a similar gain degradation was observed.

Similar measurements were made on most of the devices used on the high voltage lift tests. Cells that showed no damage and those of non-failed devices were isolated and probed individually. Figure 51 shows curve tracer photographs of the characteristic curves of a typical failed cell for two different ranges of base current. The gain degradation is greater at the lower base current, consistent with a low-level emitter base leakage mechanism. Nearly all of the cells that had been on stress for any length of time showed this type of degradation. The amount of gain decrease was similar for most devices; approximately one order of magnitude (40 initial to 4 final).

Two devices with reduced gain were heated in an oven at 225°C and retested at convenient intervals over a period of several hundred hours. One non-stressed device was also subjected to this heat soak. In all cases, the gain increased with time at temperature. After 150 hours the degraded cells increased in gain from four to more than 20. The unstressed device also increased somewhat for the first few hours bake. Typical results for one cell are shown in Figure 52 .

These results indicate that the gain degradation is most likely a surface effect, probably due to mobile surface charge in the oxide. During the life test the device was held at an elevated temperature under bias,

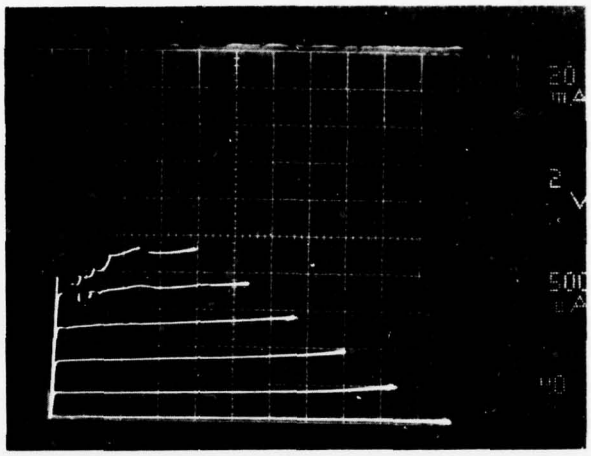

Figure 49. Characteristic Curve - Device 3-5782, Before Stress

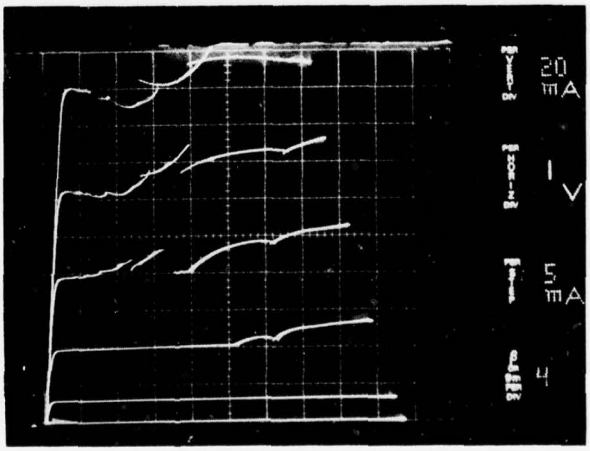

Figure 50. Characteristic Curve - Device 3-5782, After Stress

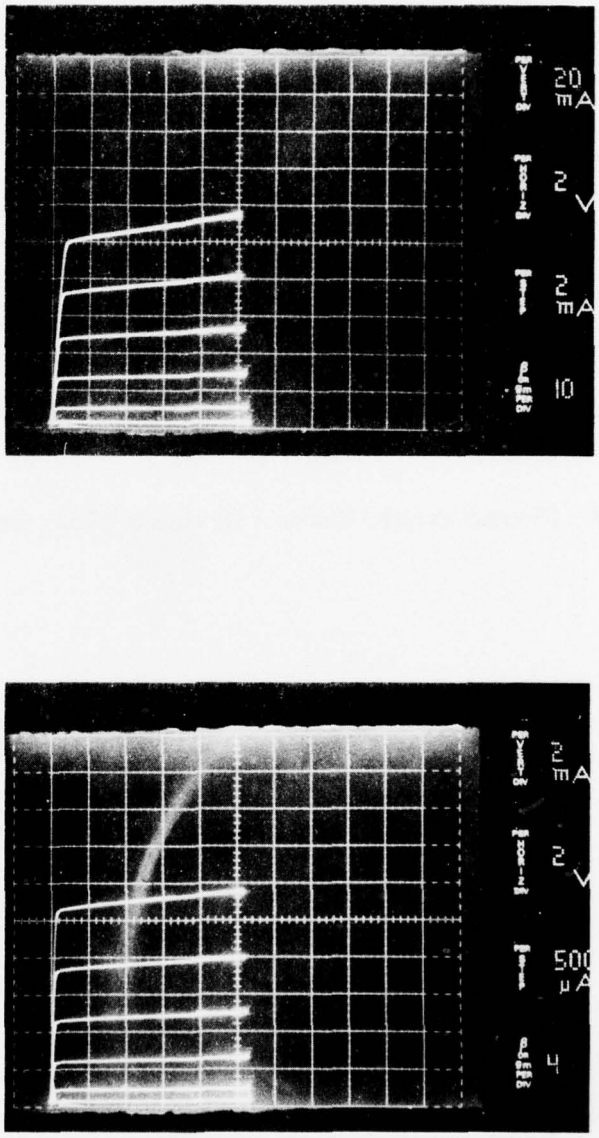

Figure 51. Characteristic Curves for Device 14-5783 After Stress Showing the Decrease in Gain at the Base Current Decreaser

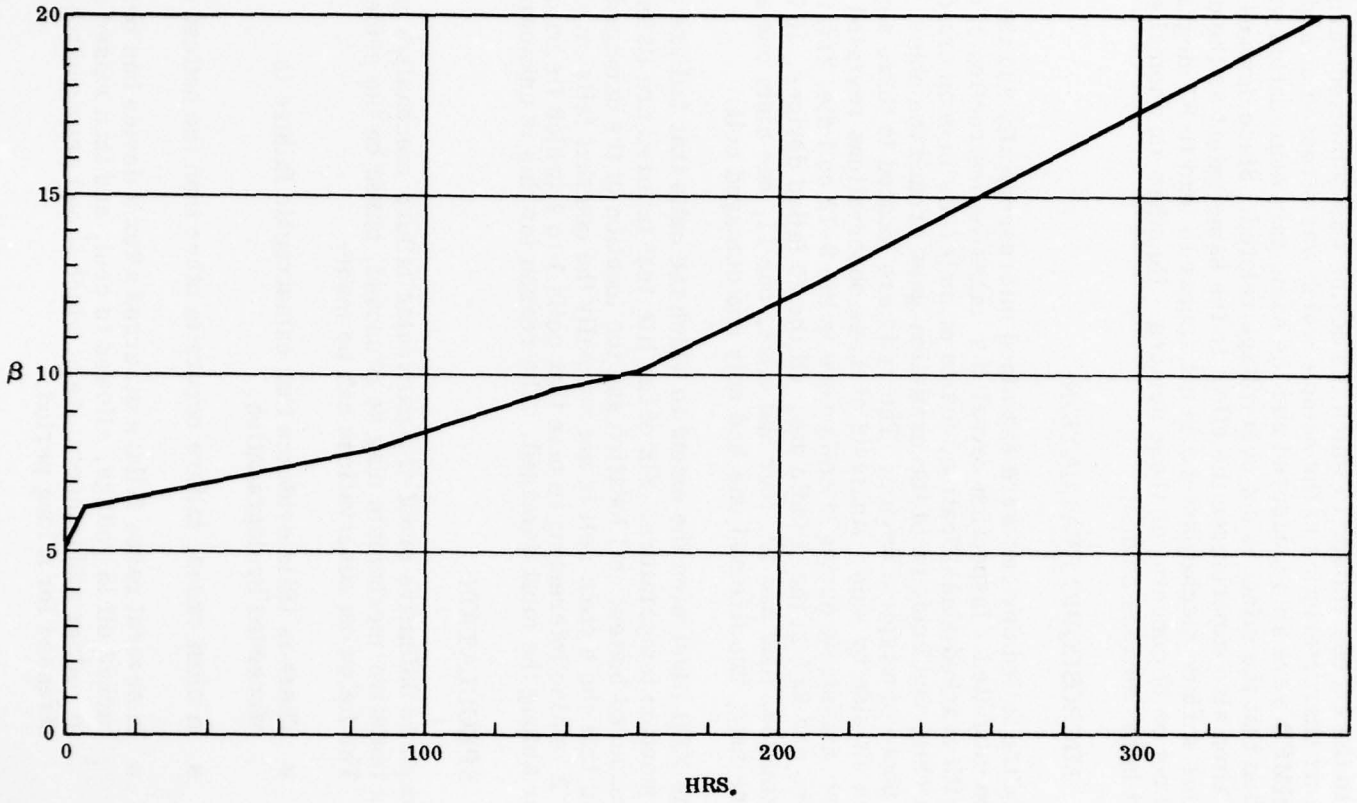

Figure 52. Gain Recovery versus Time at 225°C for Device No. 5782-21

allowing charge redistribution and a resulting increase in surface leakage, which leakage causes gain reduction.

If this mechanism is responsible for the gain loss, it should be unrelated to the excess voltage to which the device was subjected during the test. The dc characteristics of the sample which was stressed at high drive and at 28V at HMED were also measured and the same gain degradation was noted. This verifies that the effect is not overvoltage related. Since devices with no RF degradation also experienced the effect to the same extent as the degraded devices, this surface mechanism would not appear to lead to RF degradation and should not be of concern for these devices. No other dc anomalies were noted in the devices studied.

C. MICROSCOPIC EVALUATION

All of the failed devices were examined microscopically and the resulting observation tabulated. Inspection revealed a massive destruction of cell integrity with cracked glassification, fusion of materials in deep craters into the silicon chip, and bridging of the insulation gaps around the chips. Figure 53 is a photo of a typical device. The cells are located in three separate dies, which sit side by side. Analysis of these observations revealed that 48% of most massively damaged cells were in the 9-12 cell die; 31% in the 1-4 cell die, and 22% in the middle die. Of the 26 failed devices, 10 had all 12 cells damaged, four had 10, four had eight, one 11, one nine, one seven, one six, one four, two five and one had only one damaged cell.

Table XXII illustrates the extent to which the cells that fail are correlated with their junction temperature. Six of the life test failures are listed along with the measured hottest cell location and the location of the damaged cells. It is evident that the hottest cell is not normally the one that fails or is most damaged. It is also interesting to note that cells 1 to 4 (which lie on one die) were never among the most damaged. The reason for this is unknown.

D. SPECULATION

Although no definitive proof of a particular failure mechanism has been obtained, a tentative mechanism may be proposed, based on the evidence available. The following observations can be made:

- There is little evidence that catastrophic failure is proceeded by degradation.
- In most cases, failure occurs in other than the hottest cell.
- In several cases failure occurred after a device has been backed off in voltage, allowed to cool, and than raised again to voltage and temperature at which it had previously been stressed for a long period.
- Catastrophic failure nearly always occurred a short time after the voltage and temperature had been increased.

Figure 53. A Typical Catastrophic Failure

TABLE XVII. CORRELATION BETWEEN HOTTEST CELL AND CELL DAMAGE

Device	Hottest Cell	Most Damaged Cell											
		1	2	3	4	5	6	7	8	9	10	11	12
3-5782	12										X	X	
14-5703	12							X					
20-5783	12						X	X	X	X			
14-5784	12							X		X	X	X	
12-5783	1 and 12							X					X
18-5783	12										X	X	

- There is no evidence that the failures were caused by external causes, such as mismatches or line transients.

The evidence indicates that failure is not associated with a thermally activated degradation mechanism. Since it usually occurs after a temperature rise, or after the temperature has been decreased and than increased, it may be associated with the result of the temperature excursion. It is speculated that a defect, such as a microcrack in the chip, is propagated as a result of the temperature excursion until it intersects the active area of the cell, causing the failure. It is also possible that the temperature excursion or cycling causes the chip metallization to lift, leading to cell failure. At least one device showed evidence of metal lifting on the cells near the failed cells. It is not known whether this was the cause or the result of the failure.

VIII. SUMMARY AND CONCLUSIONS

This study did not reveal any failure mechanisms which may be attributed to operation at excessive electrical stress. The results of the experiments in which deliberate failures were induced indicated that, in a defect free device, failure occurs when the hot cell temperature exceeds 300-350°C, as measured by the IR microscope. This happens regardless of the stress which causes the cell to become overheated.

The life test and step stress failures occurred at a much lower temperature (180°) and may very well be related to defects, such as propagating cracks or lifting metallization.

The result of the tests of the No. 2 device indicate that they are capable of operation for hundreds of hours at collector voltages in excess of 40 volts and at drives of 30 watts. Failure, when it occurs is usually associated with an increase in temperature, indicating that it may be the result of temperature cycling or thermal shock. This is speculative, at the present time. If it is true, a temperature cycling or thermal shock screen may be effective in eliminating defective devices.

Failure may also be due to a diffusion defect, barrier layer defect, or other similar phenomenon, not related to a mechanical weakness. Unfortunately, since the failures were almost always catastrophic, it was impossible to directly determine the cause, after the fact. With few exceptions, there is no evidence that the failures were caused externally.