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Seventh Quarterly Report

IC FABRICATION USING ELECTRON-BEAM TECHNOLOGY

Period Covered
1 March 1978 – 1 June 1978

Contract No. DAAB07-76-C-8105

Technical Support Activity
U. S. Army Electronics Research and Development Command
Fort Monmouth, New Jersey 07703

Texas Instruments Incorporated
P.O. Box 225012
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A new positive electron resist (TI-313) has been implemented for fabrication of 256-bit bipolar RAMs. This TI-313 resist has allowed plasma etching at each oxide removal step in the process. The pinhole data on this resist after oxide etch is comparable with that measured on the best standard negative photoresists. Previous attempts at fabricating the 256-bit bipolar RAMs have failed due to the high number of defects in the oxide caused by an inherent problem with PBS electron resist during wet etching. In addition, a change was made from the double-level metal 256-bit bipolar RAM (54S300) to the single-level metal 256-bit bipolar

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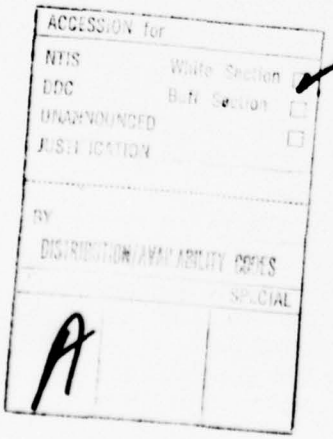
20. ABSTRACT (Continued)

RAM (74S301A). This change was made because the TI-Houston production facility was achieving extremely low yields on the 54S200/300 and had discontinued production. These changes have allowed fabrication of functional devices during this quarter.



IC FABRICATION USING ELECTRON-BEAM TECHNOLOGY

Seventh Quarterly Report

1 March 1978 – 1 June 1978

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SECTION I
PURPOSE

The overall objective of the program is to implement e-beam writing technology for the fabrication of microcircuits. The technical and economic impact of electron-beam direct slice printing will be demonstrated on 256-bit bipolar RAMs. The elimination of mask masters, masks, and the masking process will eliminate the most significant source of yield loss. This will permit greater circuit design complexity and flexibility which will lead to lower device costs with increased reliability. The complete implementation program is divided into three tasks. Task A, Yield Improvement Through Direct E-Beam Writing, is directed toward developing the manufacturing technology required for e-beam writing with existing equipment and existing resist processes and demonstrating the yield benefits of this technique. Task B, Cost Reduction for E-Beam Writing Through High Speed Resist Implementation, is directed toward implementing identified high speed e-beam resists in order to significantly decrease cycle time and thus reduce the IC bar cost. Task C, Cost Reduction for E-Beam Writing Through Automatic Beam Diameter Control and Automatic Handling, is directed toward utilizing EBMIII's capability of computer-controlled beam size (large and small) on high density circuit ($\leq$0.1 mil) geometries. This program also included implementation of an automated handling system for slices to reduce cycle time and thus further reduce bar cost.

SECTION II
TECHNICAL DISCUSSION

A. INTRODUCTION

A significant program milestone was achieved this quarter with the fabrication of fully functional 256-bit bipolar RAMs by direct e-beam slice writing. These devices were fabricated using TI-313 positive electron resist and C_4F_8 plasma etching. All pattern levels utilized positive resist and plasma etching with the exception of the metal level. This represents one of the first LSI devices fabricated by all e-beam and dry processing. In addition high-speed electron resists ($<3\ \mu coul./cm^2$ sensitivity) were used at each level. Electron resists of this sensitivity are mandatory before e-beam direct slice writing can become economically feasible.

Permission was granted during this quarter to change the 256-bit bipolar RAM being fabricated from the 54S301 to the 54S201. These two devices differ only in their metal patterns, with the former having an open collector output and the latter having a tri-state output. The reason for the change is that the 54S301 is seldom made in production while the more versatile 54S201 is in constant production and has a well defined yield history. However, the 54S201 built in standard production at Texas Instruments does not meet the military operating specifications for operations over the temperature range of $-25°C$ to $125°C$. Consequently it was necessary that the operating temperature range be changed to $0°C$ to $70°C$. The specification change necessary to cover the 54S201 for operation over the reduced temperature range was granted this quarter.

Because the CF_4/O_2 plasma etch process developed previously for the DUF and isolation levels cannot be used at the base, emitter or contact levels, a major emphasis this quarter has been on establishing a C_4F_8 plasma etch process for etching SiO_2 which is compatible with TI-313 positive resist.

Fabrication of the first article devices has been completed. All the required environmental and electrical tests have been successfully completed except the 1000 hour operating and storage tests. These last two tests are in progress and will be completed early in July.

B. PROCESS DEVELOPMENT

In this quarter the first lot of 74S201A 256-bit bipolar RAM slices processed using TI-313 resist and plasma etching has been successfully completed.

The complete process flow for using TI-313 resist together with relevant details and data was presented in the sixth quarterly report. Despite the narrow exposure window which causes problems with crosslinking in overlapped or multiply scanned areas such as alignment marker areas, all levels except metal were patterned with this TI-313 process with good results. Figure 1 shows an

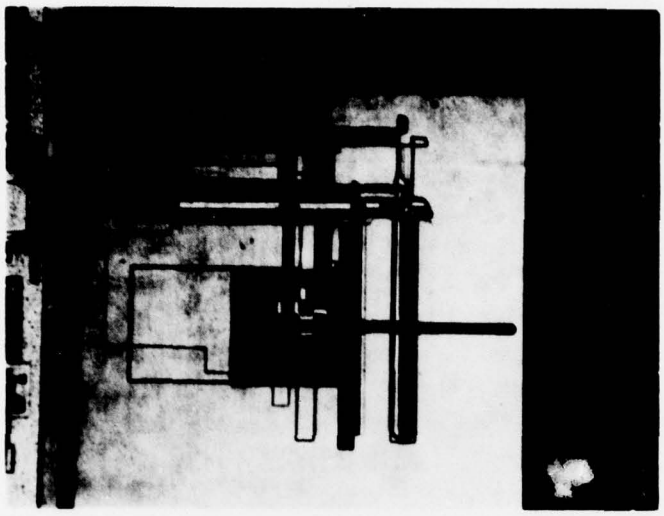


Figure 1. Alignment Marker Area After Scanning

alignment marker area after completion of a slice. Notice the numerous scan lines which are left because of this crosslinking. The metal was patterned and etched using II-309 negative resist as described in several previous reports.

The CF_4/O_2 plasma etching process developed for DUF O.R. and isolation O.R. cannot be used at the base, emitter or contact levels because there are at least two different oxide thicknesses to etch at each level. When the thinnest oxide has completed etching, the silicon beneath is exposed to the very vigorous CF_4/O_2 plasma and is etched at ten times the rate of the oxide remaining to be etched in other areas.

This problem has been solved by implementing a C_4F_8/CO_2 plasma etch process which etches Si at only one fourth the rate of SiO_2. The etching is done in a parallel plate reactor described previously using the flows and conditions outlined in Table I. The process is sensitive to the ratio of C_4F_8 to CO_2. Enough CO_2 must be used to eliminate deposition but too much CO_2 cuts down on the etch rates. The rates obtained using the conditions shown in Table I are given in Table II. Although the etch rate of II-313 is high, it is still low enough to allow etching to completion at any level of the process without using up all the resist. Also, the Si etch rate is low enough to allow for the overetching which must occur to be sure that all windows are open, without fear of etching through any junctions.

Table I. C_4F_8/CO_2 Plasma Etch Conditions

Flow Rates:	C_4F_8 – 150 cc/min
	CO_2 – 50 cc/min
Pressure:	0.35 Torr
Power:	900 Watts
Temperature:	55° ± 5°C

Table II. C_4F_8/CO_2 Plasma Etch Rates

SiO_2	200 Å/min
TI-313	175 Å/min
Si	50 Å/min

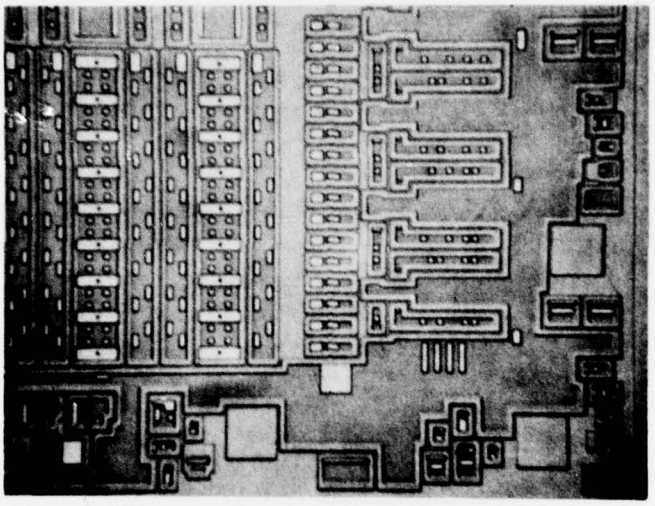
To illustrate the effectiveness of the TI-313/C_4F_8 process, photomicrographs of the S201 patterns from the first lot are shown in Figures 2-5 at each level of processing immediately after etching. Figure 2 shows the base pattern after etching and its alignment with the DUF and isolation levels. Figures 3 and 4 show patterns after the emitter and contact levels were etched, respectively. Note that due to an operator error during plasma etching, some thinning of the oxide in the emitter areas was experienced and in places may be as thin as 1000Å instead of the nominal 2000Å. It is not certain that this thin oxide will cause performance or reliability problems.

Figures 5 and 6 show examples of the metal patterning. It can be seen that the edge definition and step coverage are extremely good.

C. SLICE PROCESSING

The first lot of 545201 using e-beam lithography was completed this quarter. Unfortunately a complete set of contact print photoresist masks was not available in time to process a lot with photoresist to accompany this first e-beam lot. Instead a lot of material processed in standard production in Houston through emitter O.R. was brought to Dallas and completed in the Pilot Line. This lot had a multiprobe yield of 20%, confirming that the process for the 548201 was established in the Pilot Line. Shortly after this photoresist lot was completed the first e-beam lithography lot was also completed. It yielded 170 GEBs at multiprobe from six slices for a yield of 9%. This lot utilized TI-313 positive electron resist and plasma etching for all levels except metal.

Subsequent to running the material above a completed set of contact print masks were received and a lot of material using conventional photoresist was totally processed in the Pilot Line. This lot had a multiprobe yield of 27%.



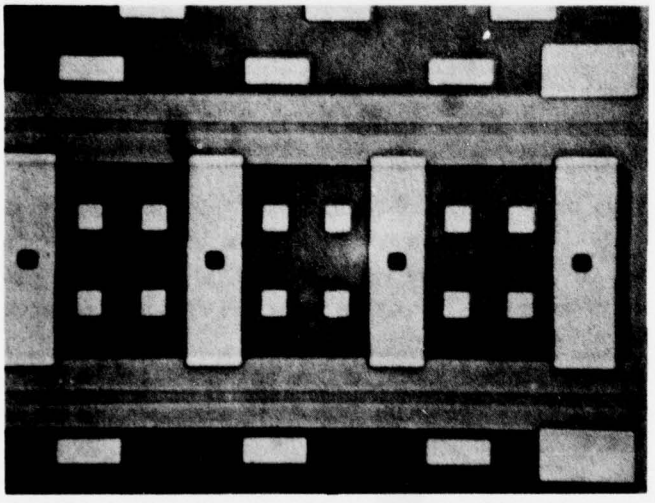
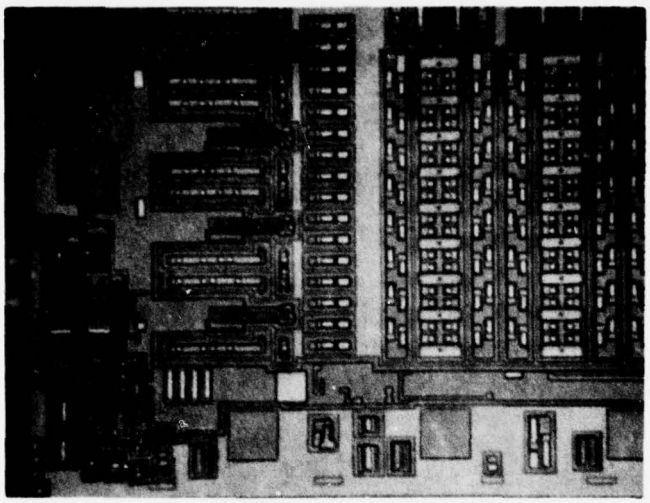


Figure 2. Base Patterns After Etching (74S201A)



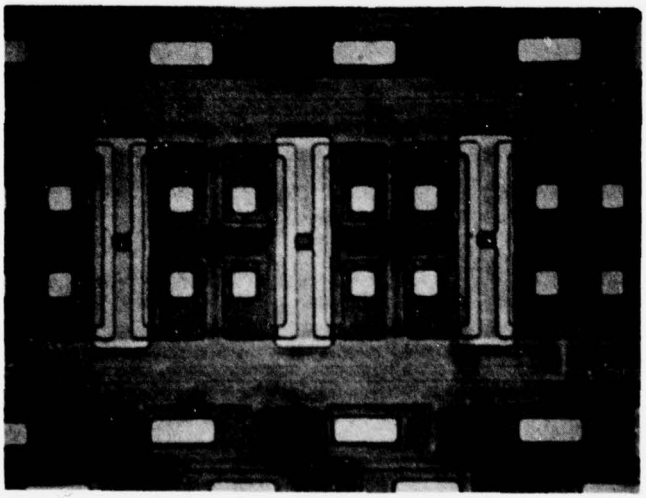
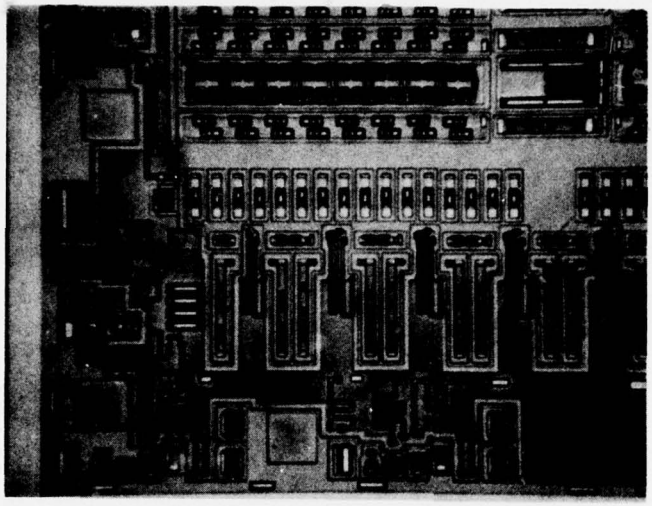


Figure 3. Emitter Patterns After Etching (74S201A)



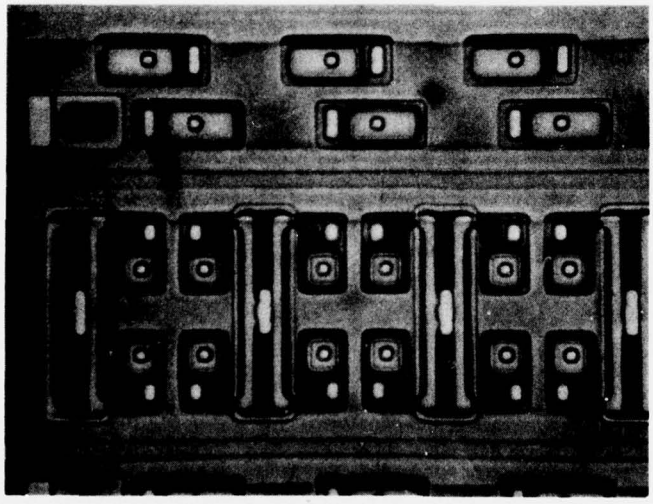


Figure 4. Contact Patterns After Etching (74S201A)

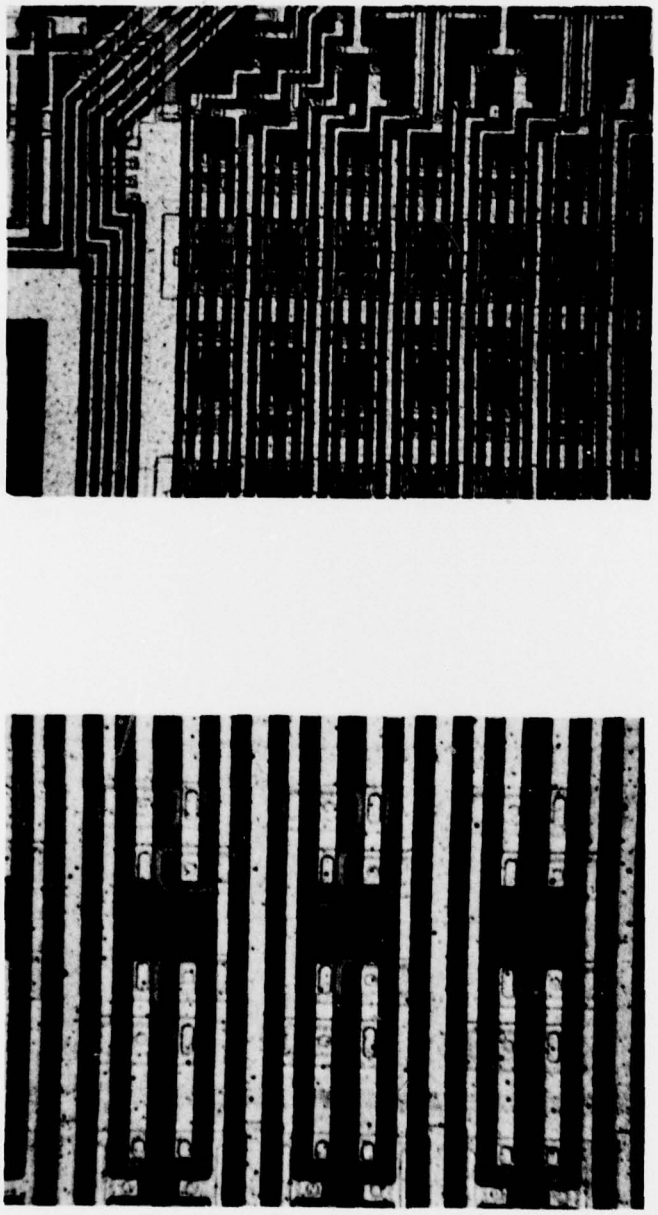
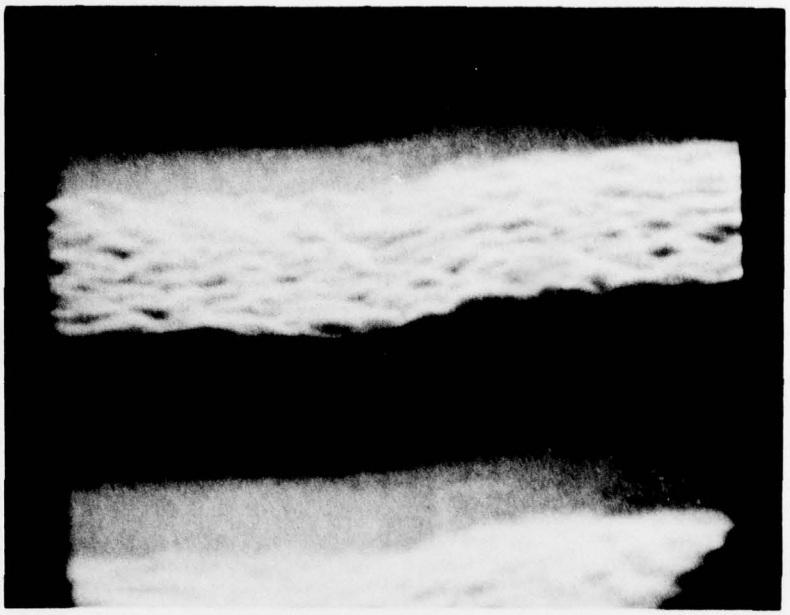


Figure 5. Metal Patterns After Etching (74S201A)



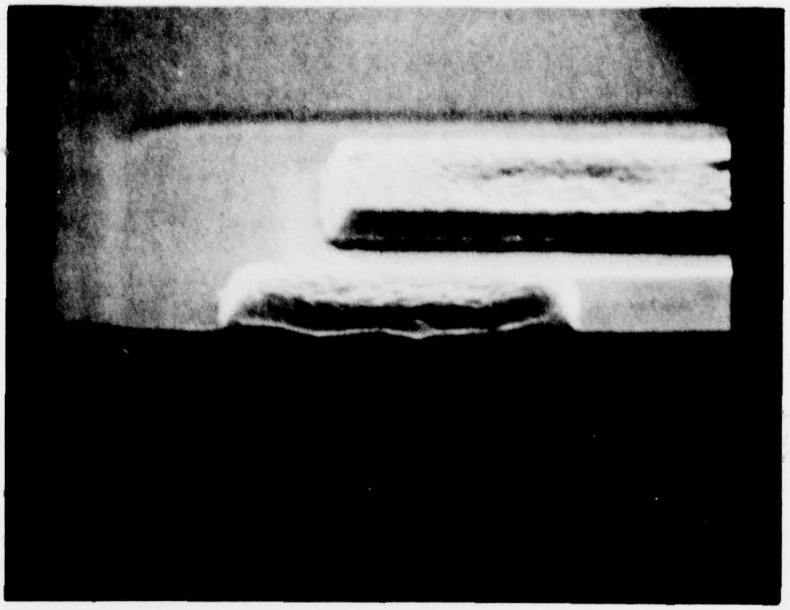


Figure 6. SEM of Metal Profiles, Step Coverage and Contact Coverage (74S201A)

A split lot using e-beam resist on one half the lot and photoresist on the other half was also started and has presently been processed through second oxide. The results from this lot will give a direct yield comparison between e-beam and photoresist systems.

D. ELECTRICAL TESTING

The first lot of material using electron resist was completed and tested with a High Speed Measurements (HSM) System. The HSM was used to test the memories initially while they were in slice form and subsequently when they were packaged. It performs all the dc test listed in Table I, i.e., V_{OL}, V_{OH}, I_{OS}, etc. It also performs functional testing on the memory cells and peripheral circuitry. This test in slice form yielded 170 GEBs from six slices for a yield of 9%.

The good bars were then cut from the slices and packaged in a 16-pin side-brazed ceramic package. Ten bars were lost during this packaging process. Also five units were pulled from the lot prior to capping for use in the bond strength test.

After packaging, the individual units were tested on the HSM for operation at 0°C, 25°C and 70°C to ensure that all the devices were fully operational. They were tested at the above temperatures on the Numerical Exerciser for Memories (NEM). The NEM is a functional memory tester with timing measurements capability for performing the ac measurements shown in Table I, i.e., t_{AA}, t_{EA}, t_{ER}, etc. The dc and ac measurements shown in Table I were taken from the specification SCS-517, dated 27 April 1978. That document contains details of the measurements performed on the HSM and NEM. All interim and final electrical test were made in accordance of Tables II and III of the specification SCS-517.

E. FIRST ARTICLE UNITS

After performing HSM and NEM tests discussed in the previous section, 157 devices were found to be qualified as possible first article devices. These devices were then screened as required in Section 4.4 of the specification SCS-517, April 27, 1978. As required, the screening was conducted in accordance with Class B of Method 5004 of MIL-STD-883.

In brief these requirements are:

1) Internal visual
2) Stabilization bake, 24 hours at 150°C
3) Temperature cycling
4) Centrifuge
5) Hermeticity, fine and gross
6) Burn-in test, 168 hours @ 70°C
7) Final electrical test
8) External visual

Table III. Electrical Performance Characteristics

TEST	SYMBOL	CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNIT
Low Level Output Voltage	V_{OL}	V_{CC} = 5 V, I_{OL} = 20 mA, D_{in} = 4.5 V		.5	V
High Level Output Voltage	V_{OH}	V_{CC} = 5 V, D_{out} = −10.3 mA	2.5		V
Short Ckt Output Current	I_{OS}	V_{CC} = 5.25 V	−32	−95	mA
Input Low Current	I_{IL}	V_{CC} = 5.5 V, V_{in} = 0.5 V		−510	µA
Input High Current	I_{IH1}	V_{CC} = 5.5 V, V_{in} = 2.4 V		25	µA
Input High Current	I_{IH2}	V_{CC} = 5.5 V, V_{in} = 5.5 V		1	mA
Input Clamp Diode Voltage	V_{IC}	T_A = 25°C, I_{in} = −18 mA		−1.5	V
Power Supply Current	I_{CC}	V_{CC} = 5.25 V, all inputs at 4.5 V, CE1, CE2, CE3 = GND outputs open		145	mA
Output Leakage High Impedance State	I_{OZL}	V_{CC} = 5.25 V, V_O = 0.4 V, D_{in} = 4.5 V		±30	µA
	I_{OZH}	V_{CC} = 5.25 V, V_O = 2.4 V, D_{in} = 4.5 V		±30	µA
Address Access Time	t_{AA}	See Note 1 and Figure 6(b)		100	ns
Enable Access Time	t_{EA}	See Note 2 and Figure 6(c)		45	ns
Enable Recovery Time	t_{ER}	Figure 6(d)		35	ns
Minimum Write Pulse Width	t_{WP}	See Note 3 and Figure 6(e)	120		ns
Propagation Delay Low to High (From R/W)	t_{PLH}	See Note 3 and Figure 6(f)		110	ns
Propagation Delay High to Low (From R/W)	t_{PHL}	See Note 3 and Figure 6(g)		55	ns

The internal visual inspect was conducted in the assembly and package area. The stabilization bake, temperature cycling, centrifuge and hermeticity tests were performed in the Environmental Laboratory of the Quality and Reliability Assurance Department. The burn-in test at 70°C for 168 hours was performed in the Linear and Military Products Branch of QRA. All interim and final electrical tests were made with the HSM and NEM.

After screening, the memory devices were tested in accordance with Method 5005 of MIL-STD-883 as specified in the specification SCS-517. In compliance with the Group A inspection of these documents, the dc and ac tests listed in Table I herein were performed at 0°C, 25°C and 70°C.

In compliance with the Group B inspection of the above documents, the following tests were conducted.

1) Physical dimensions of the package
2) Resistance to solvents
3) Bond strength
4) Solderability
5) Lead integrity

The physical dimensions of all the units were measured and found to be proper. Also, bond strength tests were successfully performed on the five units which, as previously mentioned, were pulled from the lot prior to packaging. As a part of the Group B inspection, the package resistance to solvents, solderability and lead integrity tests were performed. Six units were successfully tested in each of these three tests.

The Group C inspection of Method 5005 of MIL-STD-883 requires the following subgroup tests be performed. Also shown is the number of devices used in each test.

Subgroup 1	Thermal shock, moisture resistance, seal	5 Devices
Subgroup 2	Mechanical shock, vibrations constant acceleration, seal	5 Devices
Subgroup 3	Salt atmosphere	5 Devices
Subgroup 4	High-temperature storage 1000 hours at 150°C	5 Devices
Subgroup 5	Operating life 1000 hours at 70°C	5 Devices
Subgroup 6	OMITT	
Subgroup 7	Switching test at 70°C	4 Devices
Subgroup 8	Switching test at OPC	4 Devices

Although Subgroups 1 and 2 above require only the HSM dc electrical test at 0°C, 25°C and 70°C for completion, they have also been tested with the NEM to verify they satisfy the ac requirements for the memory at 0°C, 25°C and 70°C. Subgroup 3 requires a visual inspection only and has been completed as have Subgroups 1 and 2. It is noted that Subgroups 7 and 8 are mere repeats of the Group A test and thus have also been completed.

The devices In Subgroups 4 and 5 are presently under test and will complete this 1000 hours on July 10. At that time they will be tested at 0°C, 25°C and 70°C with the HSM and NEM to determine if they meet the dc and ac requirements of the memory.

SECTION III
MANPOWER

The following professionals worked on this program 1 March 1978 – 1 June 1978. The percentage of time worked is also shown.

Mr. P. L. Whelan	20%
Dr. G. L. Varnell	10%
Dr. J. L. Bartelt	50%
Dr. R. A. Owens	20%
Dr. J. Reynolds	50%
Dr. R. A. Robbins	Consultant
Mr. C. D. Winborn	Consultant

In addition, three technicians worked on the program.