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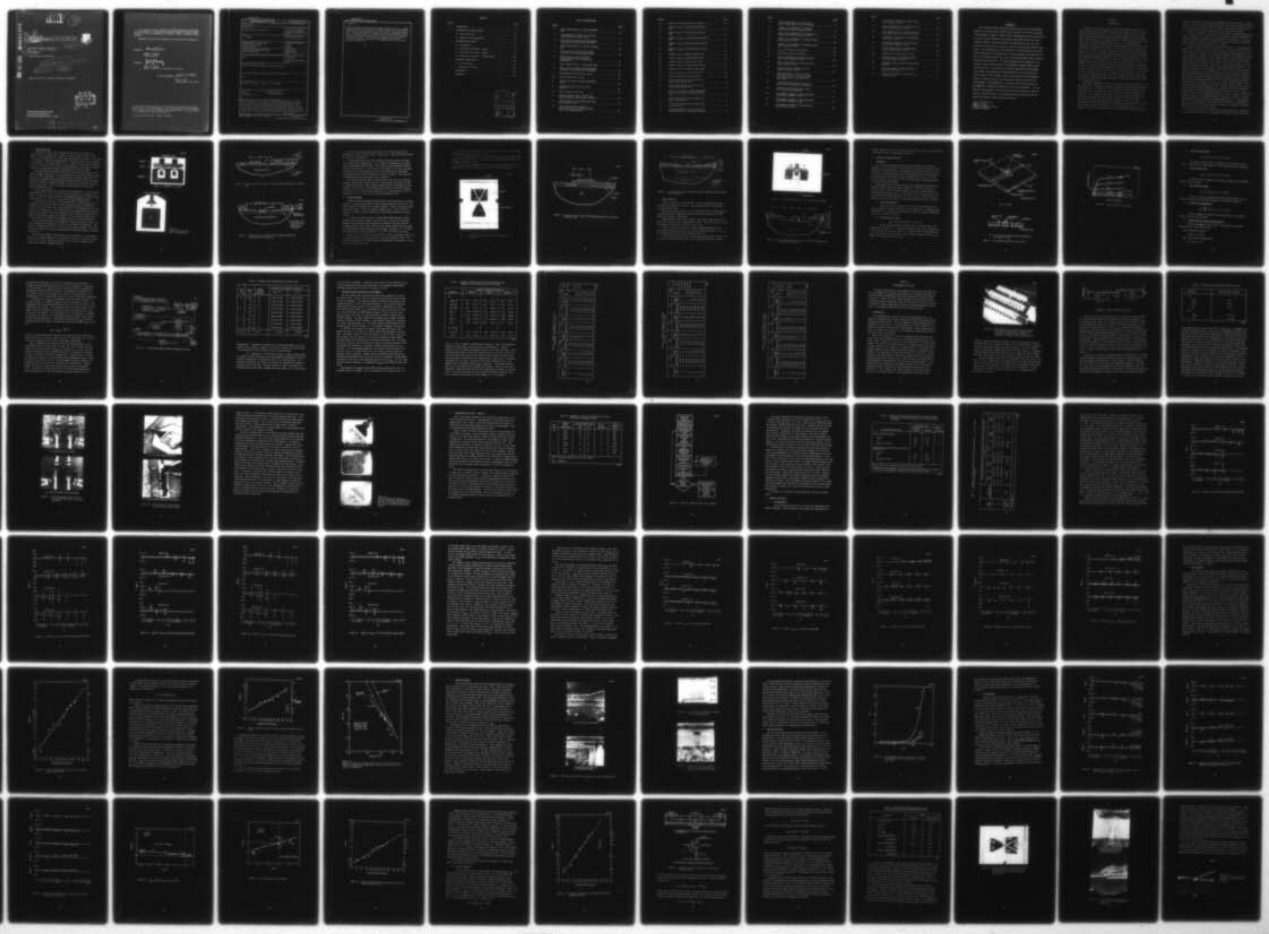

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6 RELIABILITY STUDY OF GaAs FET

10 R. Lundgren

Hughes Research Laboratories

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The reliability of three types of low-noise GaAs field-effect transistor (FET or MESFET) was investigated. Types A and B incorporate Al Schottky-barrier gates; Type C has a "gold" gate structure (Ti/Cr/Pt/Au). FETs were tested to determine the ability of their gates to withstand electrical stress. Catastrophic failure occurred at approximately 3 ergs and 0.8 ergs input energy for positive and negative dc pulses, respectively; contrary to other reports, the Au-gate devices were not more robust. With either cw or

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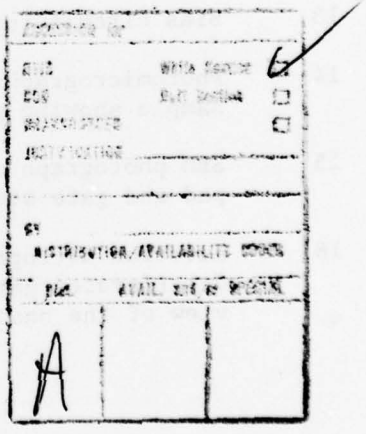
pulsed rf stress, the Type-A devices failed at between 1 and 3 W. Constant-stress accelerated life tests were performed at temperatures between 200°C and 245°C, using both unbiased and dc-biased samples. The biased gold-gate devices failed relatively early because of electrical degradation of their gates. The Type-B devices, with Au-Ge/Pt Ohmic contacts, failed because of increasing parasitic resistance; they failed faster than the Type-A FETs, with Au-Ge/Ni contacts. The biased Type-A samples failed because of structural changes in the Al gate; a poor SiO_2 glassivation layer is suspected to be the cause.

CONTENTS



LIST OF ILLUSTRATIONS

EVALUATION

This technical report describes the reliability of low noise microwave GaAs FET chip devices which includes their potential reliability, operating life and modes of failure. Vendor devices representative of the state-of-the-art and of various fabrications and designs were selected for this investigation; however, the types of devices and quantities of each were very limited by the high cost of the devices and the limited funds allotted to this effort. The resulting data is not conclusive, but does provide cursory data. and excellent basics for further work. This work supports the objectives of TPO-5, "C^3 Systems Availability," and the associated project 2338, "Assurance Technology for Electronics." The data generated in this program will contribute to hybrid specifications in MIL-M-38510D, "General Specifications for Microcircuits," and hybrid test procedures depicted in MIL-STD-883B, "Test Methods and Procedures for Microelectronics," discrete transistor specifications in MIL-S-19500F, "General Specifications for Semiconductor Devices," discrete transistor test procedures depicted in MIL-STD-750, "Test Methods for Semiconductors," and device reliability prediction in MIL-HDBK-217B, "Reliability Prediction of Electronic Equipment." This program will be expanded in FY79 to include reliability studies on power FET devices, detailed studies of failure mechanisms associated with GaAs FET devices and further studies on low noise devices.

Edward J. Calucci

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Reliability Physics Section
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SECTION 1

INTRODUCTION

Within the last several years, the GaAs Schottky-barrier-gate field-effect transistor (FET or MESFET) has become the leading contender for application in low-noise amplifiers over the frequency range from 4 to 30 GHz. Other microwave applications (such as digital integrated circuits (digital ICs), power sources, and power amplifiers) are also undergoing rapid development. Major remaining questions with respect to system applications, especially in long-life systems such as communications satellites, are device reliability and operational lifetime. Most state-of-the-art low-noise GaAs FETs are very similar in terms of design, dc parameters, and rf performance. However, they all use slightly different materials and fabrication processes. As a result, the several preliminary GaAs FET reliability studies that have been performed[1-11] have generally not resolved the reliability issue. Initial estimates from some of these studies indicate that mean times to failure (MTTFs) of 10^7 hr or more can be expected under benign operating conditions; however, the primary failure modes and activation energies differ from study to study and it has not been determined which metalizations or processes yield the most reliable devices. This uncertainty is not surprising in the relatively young, rapidly developing GaAs FET technology, but until these issues are resolved, there will be some reluctance to using these devices in critical or long life systems.

This report describes a 22-month investigation of the reliability of low-noise GaAs FETs, including the testing of samples produced by several different manufacturers. The purpose of the study was to identify their failure mechanisms and to determine and compare their potential reliabilities and operating lives. Within the limited scope of this program, approximately 230 devices (representing three different manufacturers) were tested. The FETs all had 1-μm gate lengths and were obtained in chip form. Both aluminum-gate and gold-gate FETs were represented. Approximately 150 samples were fabricated by HRL and supplied to this program without charge. In addition, two sets of 40 samples each were purchased from other manufacturers

so that a comparison of alternative technologies could be obtained. The major portion of the effort on this program was directed toward environmental stress (accelerated life) testing of the FET samples. Some brief electrical stress tests were also performed to determine dc and rf failure thresholds.

Section 2 describes the three types of GaAs FETs investigated during this study. Samples of the purchased FETs were analyzed to confirm manufacturer-supplied information regarding their geometry and metalizations. Electrical characterization included dc parameters, minimum noise-figure and associated gain at 10 GHz, and S-parameters from 2 to 18 GHz.

The accelerated life tests are described in Section 3. During preliminary Phase-I tests, two groups of HRL devices were tested at 240°C and 270°C; however, gate pad failures in the 270°C group caused these preliminary tests to be terminated. During the more definitive Phase-II test sequence, 120 FETs were stressed at temperatures between 200°C and 245°C; both low-noise-biased samples and unbiased samples were included. Failure criteria were based on allowed changes in specified dc parameters. Noise figure and gain at 10 GHz were also monitored to measure their correlation with the dc parameters. The results from these life tests suggest that Au-Ge/Ni Ohmic contacts are more reliable than Au-Ge/Pt, and aluminum gates are more reliable than gold gates. Poor SiO_2 glassivation layers can degrade aluminum gates; however, properly designed gate bond pads effectively eliminate the danger of Al gate failures due to Au-Al intermetallic formations. Gate failure mechanisms accelerate significantly in the presence of dc bias. The MTTF values obtained to date fall near previously published results;[4,6] however, neither an MTTF curve nor a failure-mode activation energy (E_a) were obtained for the HRL fabricated FETs because of conflicting results from the 245°C and 231°C test groups. A flaw in the 231°C oven is suspected of being the cause. Testing of the lower temperature groups is continuing beyond the end of this contract to obtain the additional data required for determining MTTF and E_a. An environmental stress test, during which the FETs are rapidly switched (at a 100-kHz rate) between pinchoff and saturation, showed no evidence of increased electromigration at pulsed 40-mA current levels.

Section 4 describes the electrical stress tests performed. Positive dc pulses applied to the gates of aluminum-gate FETs showed that their failure

SECTION 2

DESCRIPTION OF DEVICES TESTED

A. DEVICE SELECTION

All state-of-the-art low-noise microwave GaAs FETs are very similar in most respects. All source and drain electrodes are based on Au-Ge Ohmic contacts, differing only in the additive and the overlayers used. The critical gate and channel dimensions are essentially identical, and the FETs all employ Schottky-barrier gates. However, if one is forced to divide FETs into two separate groups, it would have to be on the basis of their gate materials. Most MESFETs use aluminum for their Schottky-barrier gates. The most common alternative structure is a "gold" gate: a multilayer structure consisting of a refractory-metal Schottky layer, one or more barrier metal layers, and a gold layer on top to provide low gate resistance. Although the particular materials, design, and processing steps used in fabricating any given GaAs FET often have only a subtle influence on its rf performance, these differences can strongly influence its reliability.

This investigation attempted to test representative samples of the various fabrication alternatives. The HRL GaAs FET (Type-A below), which was the principal test device in this study, has an aluminum gate stripe. Two other types of GaAs FETs were purchased from well-known manufacturers. One has an aluminum gate and the other a gold gate. Forty chip samples of each were purchased for testing along with the HRL devices. The manufacturers also cooperated by providing nonproprietary information regarding the materials, structures, and processing steps used in fabricating their devices. We also attempted to confirm this information by examining the FETs with optical microscopy, scanning electron microscope (SEM) analysis, and electron microprobe analysis. The test devices are described below. The salient features of each are summarized in Table 1.

Table 1. Construction Details of Tested GaAs FETs

FET Element	Type of FET		
	A	B	C
Substrate	Purchased after qualification tests	Purchased after qualification tests	Purchased
Buffer layer	None	High-resistance VPE[a] 3 μm	None
Active N-layer (channel)	Ion implant (Si) 2×10^{17} cm^{-3} 2500 Å	S-doped VPE 1.5×10^{17} cm^{-3} 2000 Å	Sn-doped LPE[b] (750°C)
Source/drain: Ohmic contact	Au-Ge/Ni/Au (1500/400/500 Å) Alloyed 30 sec at 450°C	Au-Ge/Pt (1500/400 Å) Alloyed at 400°C	Ge-Au/Ni/Au (1400/200/500 Å) Alloyed 45 sec at 475°C in H_2
Overlayer	Cr/Pd/Au (1000/1000/8000 Å)	Ti/Pt/Au (2000/2000/2000 Å)	
Gate:			
Gate	Al (6000 Å) 1 x 300 μm	Al (4500 Å) 1 x 300 μm	Ti/Cr/Pt/Au (100/100/400/1700 Å)
Bond pad	Cr/Cr/Pd/Au (3000/1000/1000/ 8000 Å)	Ti/Pt/Au (2000/2000/2000 Å)	1 x 250 μm gate
Glassivation	SiO_2 (1500 Å) (Type-A2 only)	SiO_2 (1500 Å)	SiO (2000 Å)

[a] VPE = vapor-phase epitaxy
[b] LPE = liquid-phase epitaxy

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1. Type-A GaAs FETs

The HRL FETs used in this program were specifically designed for high-reliability applications. Figure 1 shows a photomicrograph of this device. The device has a 1 x 300 μm gate and two gate bond pads. The Al gate is connected to the Au bonding pads with Cr links to avoid Al-Au intermetallic formation. As shown in Figure 2, the Au and Al are physically separated by the Cr link (i.e., they do not overlap anywhere). This avoids the possibility of Au penetration through the barrier metal during bonding.

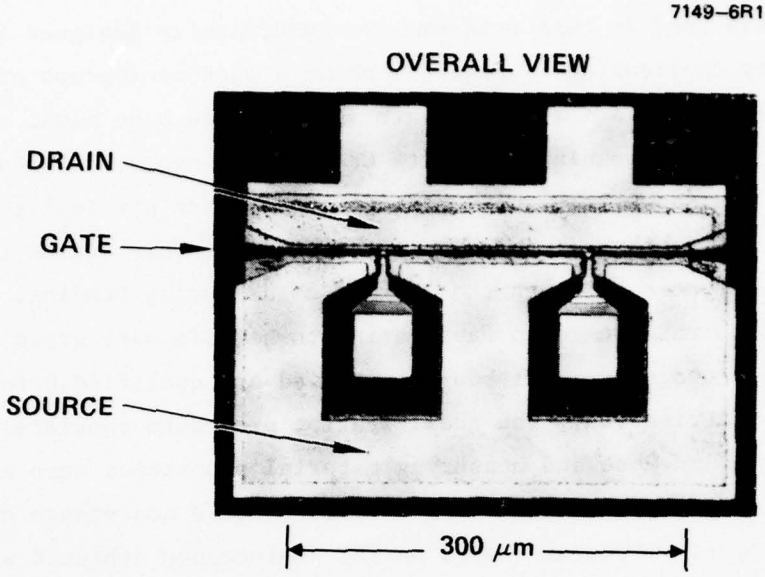
The GaAs substrates used in fabricating these FETs were grown by horizontal Bridgman techniques. All boules received are qualified before acceptance for device fabrication. The qualification procedure consists of ion implanting a standard dose and measuring material properties such as doping profile, mobility, and sheet resistance. Strict boule acceptance criteria have been developed. These are based on FET performance achieved with several different boules.

The FET channel layers are formed by ion implantation. Silicon ions are implanted directly into the substrate without growth of an epitaxial buffer layer. The implant yields a profile with maximum doping of 2×10^{17} cm^{-3} and a thickness at a 1×10^{17} cm^{-3} doping level of approximately 2500 Å.

All metalization patterns for these GaAs FETs are formed by the liftoff technique, which involves definition of a desired pattern in photoresist, evaporation of the metal layers, and rejection of the unwanted metal by dissolution of the photoresist. This process allows the definition of micrometer-dimension structures without great difficulty and eliminates the need for the tight process controls required to achieve such structures by wet etching. A cross section of the HRL FET metalization patterns is shown in Figure 3.

The source-drain metals are sequentially evaporated layers of Au-Ge, Ni, and Au deposited with thickness of 1500, 400, and 500 Å, respectively. This contact is alloyed at 450°C for 30 sec to produce Ohmic behavior. These contacts are covered by the overlay metalization, as described below, to improve conductivity.

The gate metalization on these devices is Al deposited to a thickness of 6000 Å. Before this deposition, the GaAs under the gate is etched to control device final current. This etch procedure also results in reduced source resistance and higher breakdown voltage.



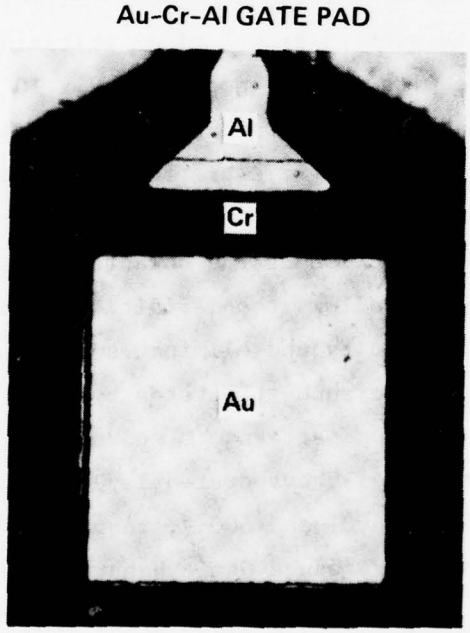


Figure 1.
Type-A GaAs FET with 1 x 300 μm aluminum gate.

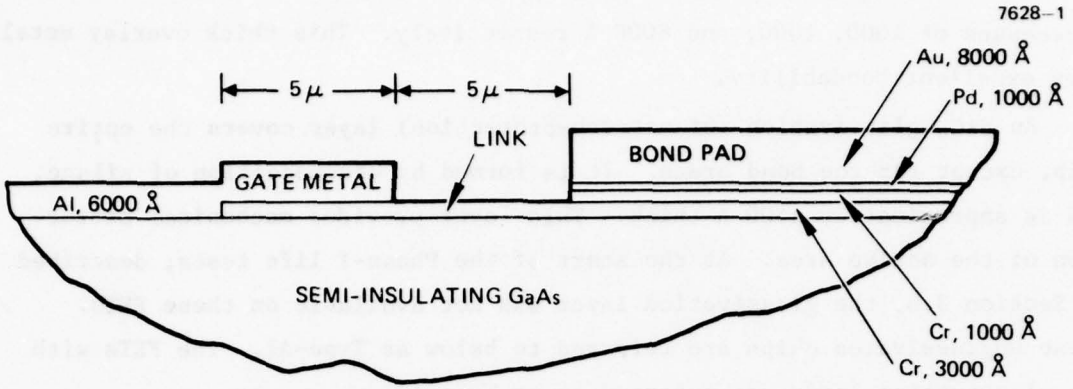


Figure 2. Cross section of Al gate – Au bond pad interconnection of Type-A FET.

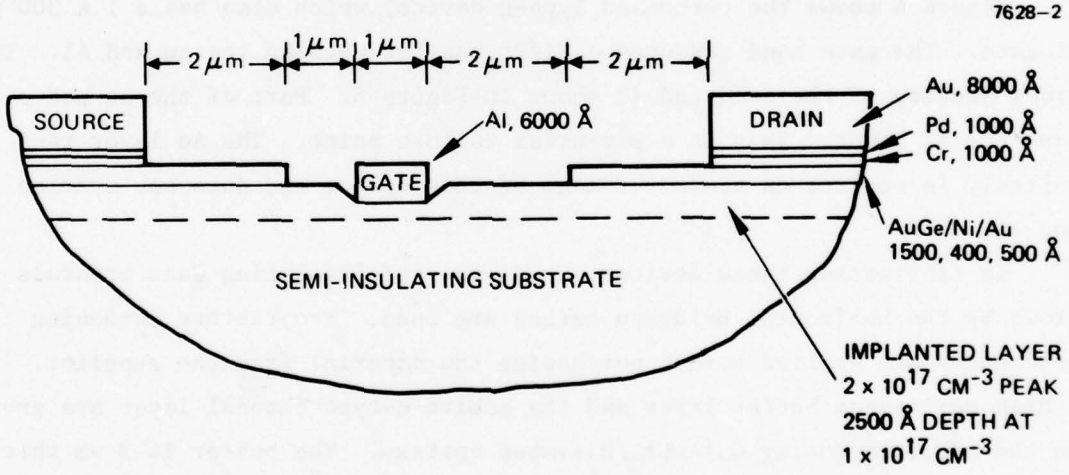


Figure 3. Cross section of Type-A GaAs FET showing dimensions and metalization thickness.

The overlay metalization on these FETs is a Cr-Pd-Au sequence with thicknesses of 1000, 1000, and 8000 Å respectively. This thick overlay metal gives excellent bondability.

An SiO_2 glassivation (or scratch-protection) layer covers the entire chip, except for the bond areas. It is formed by decomposition of silane, and is approximately 1500 Å thick. This layer provides mechanical protection of the active area. At the start of the Phase-I life tests, described in Section 3.B, the glassivation layer was not available on these FETs. These unglassivated chips are referred to below as Type-A1. The FETs with the glassivation layer are referred to as Type-A2.

The screening process used in selecting FET chips for this study consisted of 100% optical inspection using a high-quality microscope at 200X to 1000X magnification. Those samples passing optical inspection were then tested on a curve tracer for saturated drain current and pinchoff voltage. The controls on our processing are such that if a sample passes optical inspection, it nearly always passes electrical inspection also.

2. Type-B GaAs FETs

Figure 4 shows the purchased Type-B device, which also has a 1 x 300 μm Al gate. The gate bond pad uses a Ti/Pt barrier between the Au and Al. The cross section of the bond pad is shown in Figure 5. Part of the Au pad overlaps the Al layer. This is a potential failure point. The Au layer reportedly is shorter on newer versions of this device and does not overlap the Al.

In fabricating these devices, Cr-doped semi-insulating GaAs crystals grown by the horizontal Bridgman method are used. Proprietary screening procedures are applied before purchasing the material from the supplier. A high-resistance buffer layer and the active n-type channel layer are grown on the substrate using $Ga/AsCl_3/H_2$ vapor epitaxy. The buffer is 3 μm thick. The active layer is sulfur doped ($N = 1.5 \times 10^{17}$ cm^{-3}) and 0.2 μm thick.

Figure 6 shows the device cross section. Au-Ge/Pt (1500/400 Å) Ohmic contacts are used for the source and drain. They are alloyed at 400°C. The overlay metalization is Ti/Pt/Au having 2000/2000/2000 Å thicknesses; it also serves as the gate bond pad.

The Al gate is 4500 Å thick. The gate length is 1 μm. The source-gate and gate-drain separations are each 1 μm.

The SiO_2 glassivation layer is 1500 Å thick and covers the entire chip, except for the bond areas. It is deposited by decomposition of SiH_4 in an atmosphere containing oxygen.

After scribing and breaking the wafer into FET chips, the lot is put through Group A tests, bond pull tests, and 100% visual inspection.

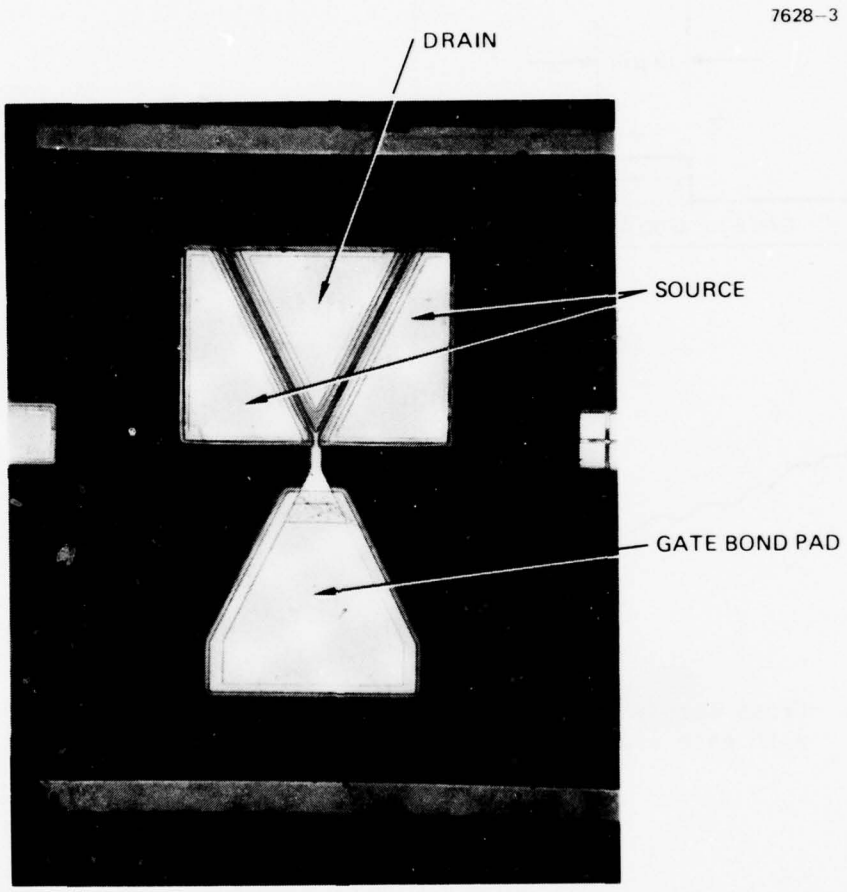


Figure 4. Type-B GaAs FET with 1 x 300 μm, V-shaped gate (200X).

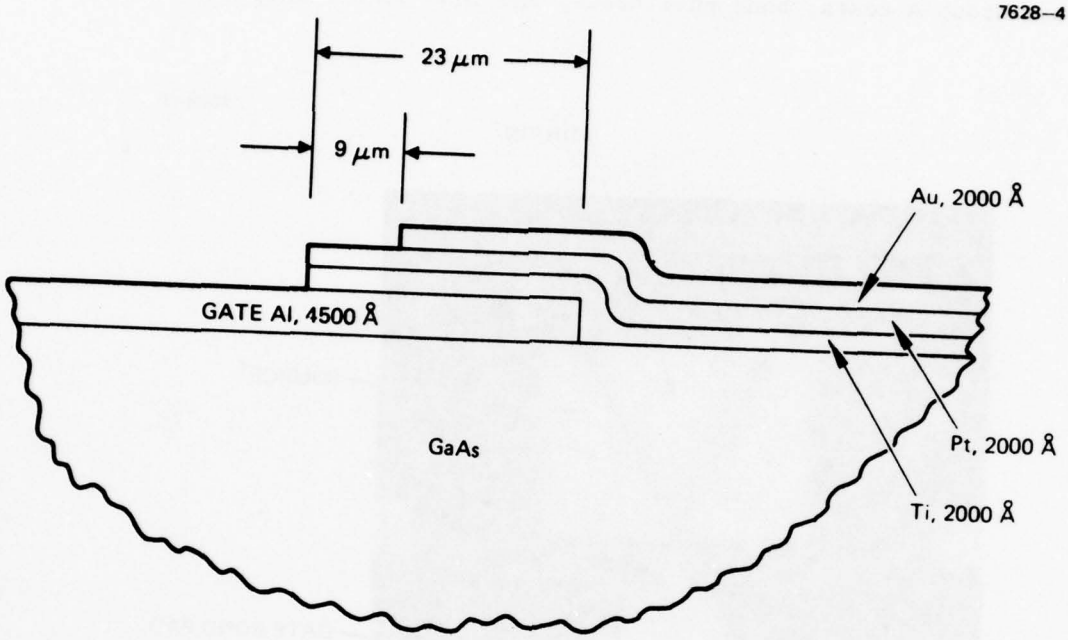


Figure 5. Cross section of Type-B GaAs FET gate bond pad at interface with gate lead.

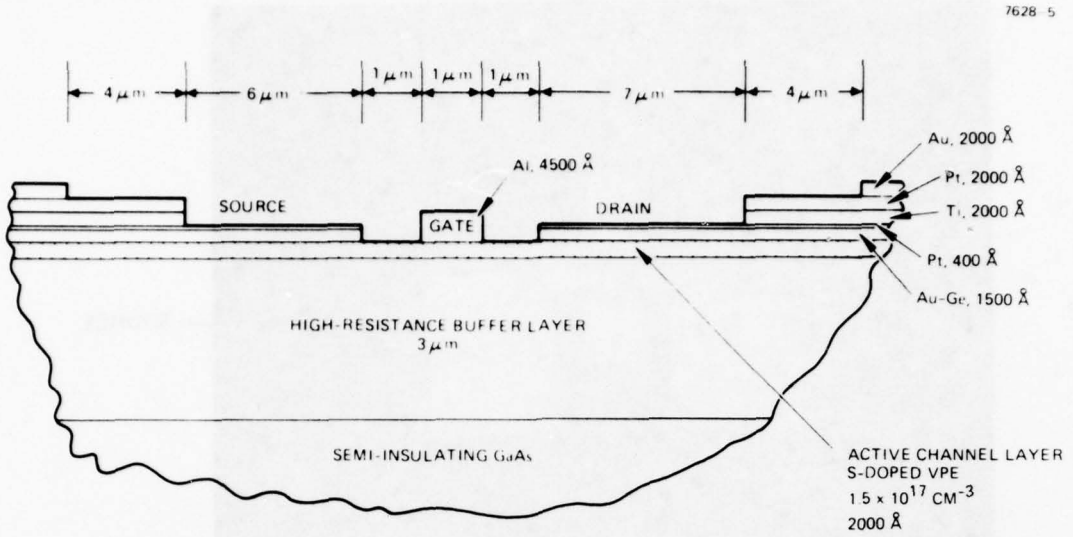


Figure 6. Cross section of Type-B GaAs FET showing dimensions and metalization thicknesses.

3. Type-C GaAs FET

Figure 7 shows the Type-C GaAs FET. It has a four-layer gold gate structure that measures 1 x 250 μm. The gate bond pad is an extension of the gate metalizations.

The active Sn-doped channel layer is grown directly on a semi-insulating substrate using liquid-phase epitaxy (slide-bar technique) at 750°C. Mesas are formed by a 3000 Å etch.

Figure 8 shows the FET cross section. The Ohmic contacts consist of Ge-Au (5% Ge)/Ni/Au layers 1400/200/500 Å thick. They are formed by a lift-off process and alloyed at 475°C for 45 sec in H_2.

The gate consists of Ti/Cr/Pt/Au layers 100/100/400/1700 Å thick. These layers simultaneously form the source and drain overlayers. The gate and overlayer patterns are again formed by lift off.

A 2000 Å SiO protection layer is evaporated and the excess lifted. The SiO does not cover the entire chip; a 36 x 280 μm area protects the FET

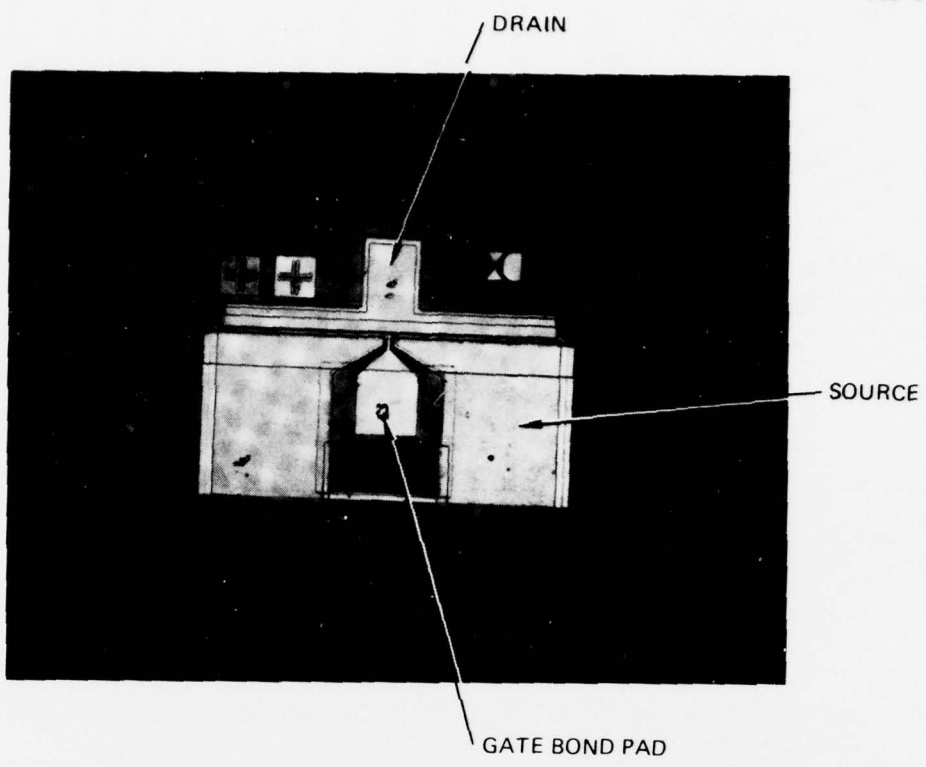


Figure 7. Type-C GaAs FET with 1 x 250 μm gold gate (200X).

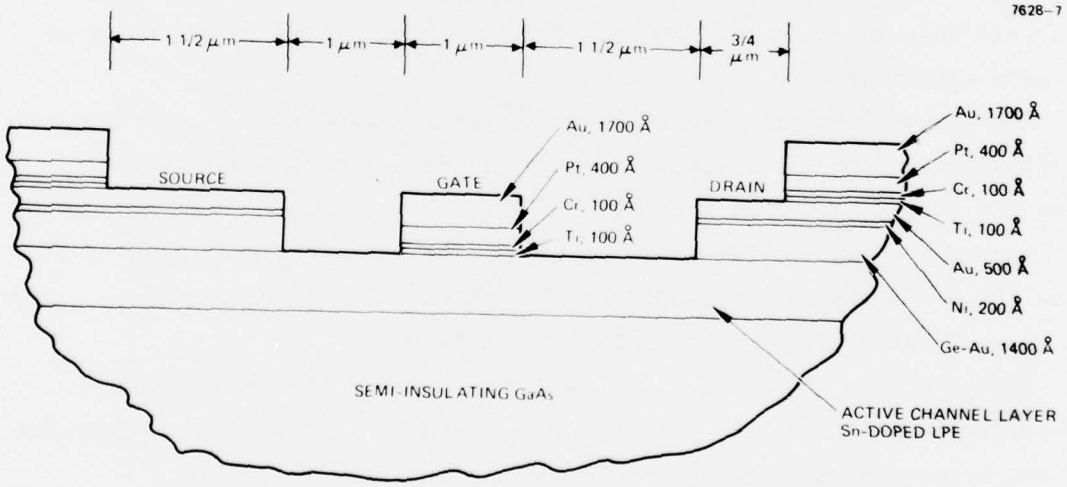


Figure 8. Cross section of Type-C GaAs FET showing dimensions and metalization thicknesses.

channel region, and a 50 x 50 μm area protects part of the source metalization from being touched by sagging gate bond wires.

B. ELECTRICAL CHARACTERIZATION

1. Procedures

All of the test samples used for this investigation were measured (generally with a Tektronix 576 Curve Tracer) to determine several of their important dc characteristics. Most were also measured for several rf characteristics, primarily minimum noise figure and associated gain at 10 GHz, but many were also measured for their S-parameters over the 1 to 18 GHz frequency range. The several dc and rf characterization procedures generally used are described below.

Before being used, each FET chip sample was permanently mounted on an NEC-type alumina microstrip carrier (Figure 9) using Au-Sn eutectic and gold wire bonds. These carriers provide a safe and convenient means of handling and testing the devices. The microstrip is a good medium for both dc and microwave characterization of the FET, and the life test ovens are designed to use the carriers for locating and applying dc bias to the FETs.

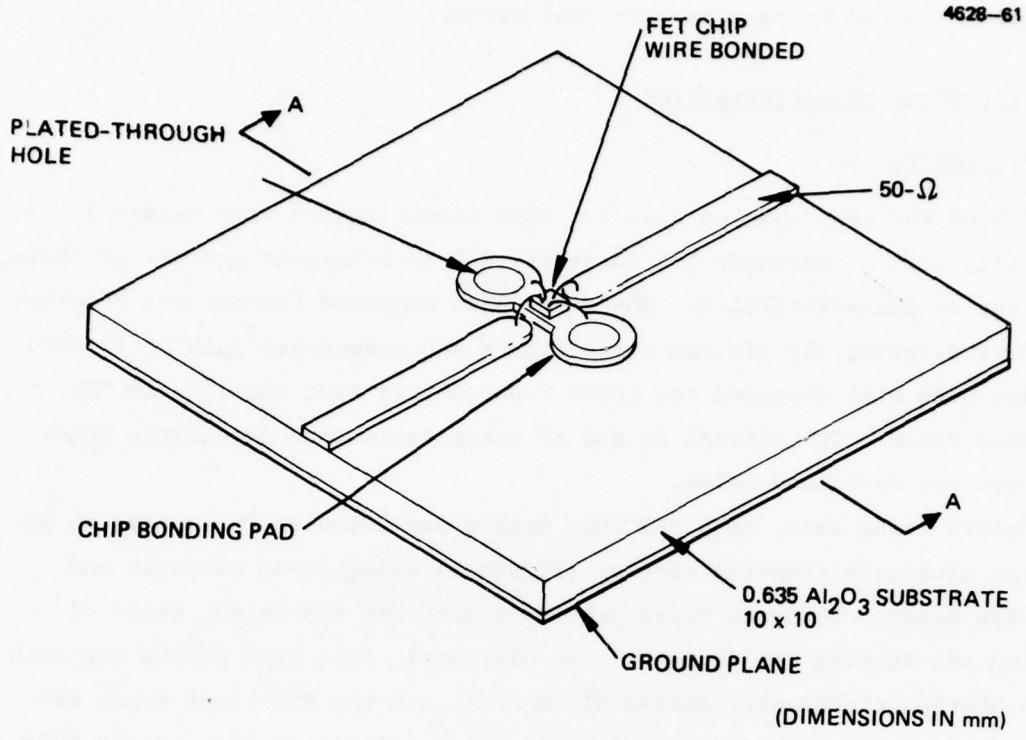
a. DC Characterization

Figure 10 shows a typical set of GaAs FET current-voltage (I-V) curves as seen on a curve tracer with the FET connected in the common-source configuration. The primary dc characteristics that are generally important to low-noise operation include:

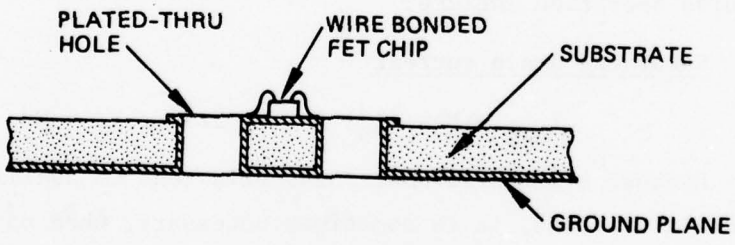
- Saturated drain current

$$I_{DSS} = \text{Max } (I_D) \text{ for } V_D \leq 3 \text{ V}, \; V_G = 0\text{V}.$$

Because high-performance GaAs FETs tend to oscillate near their maximum drain currents, it is sometimes necessary, when using a curve tracer, to decrease the drain voltage below 3 V to obtain stable dc measurements of I_{DSS}. Whenever this is necessary, the actual drain voltage at which I_{DSS} is measured is recorded along with I_{DSS}.



(a) Top view.



(b) Cross section through center perpendicular to microstrip lines.

Figure 9. NEC-designed microstrip chip carrier.

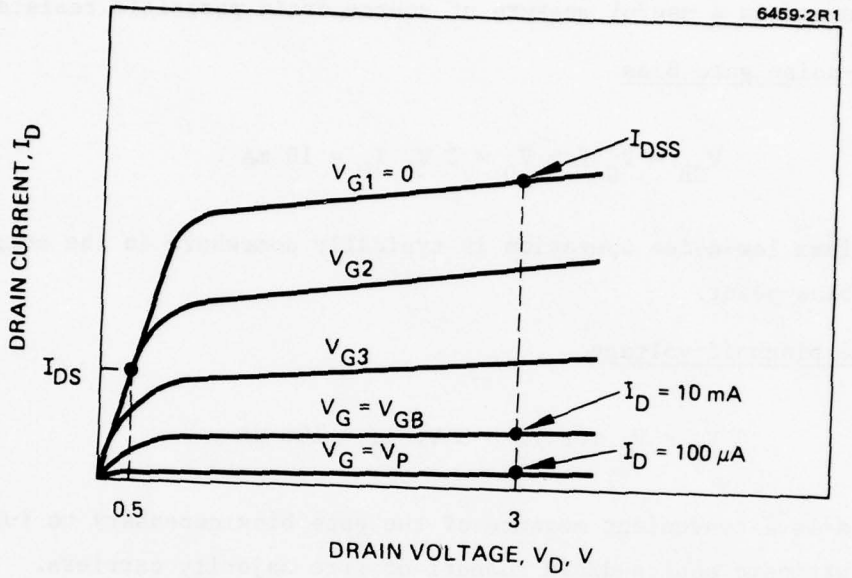


Figure 10. Typical GaAs FET I-V curves.

- Specific drain current

$$I_{DS} = I_D \text{ for } V_D = 0.5 \text{ V}, V_G = 0\text{V} .$$

The specific drain current is measured in the linear portion of the I-V curves and is a useful measure of source-drain parasitic resistance.

- Low-noise gate bias

$$V_{GB} = V_G \text{ for } V_D = 3 \text{ V}, I_D = 10 \text{ mA} .$$

Optimum low-noise operation is typically somewhere in the neighborhood of this bias point.

- Gate pinchoff voltage

$$V_P = V_G \text{ for } V_D = 3 \text{ V}, I_D = 100 \text{ μA} .$$

This is a convenient measure of the gate bias necessary to fully deplete the intrinsic source-drain channel of free majority carriers.

- Low-noise transconductance

$$g_m = \frac{\partial I_D}{\partial V_G} \text{ for } V_D = 3 \text{ V}, I_D = 10 \text{ mA} .$$

This is a measure of the gain of the transistor in the neighborhood of the low-noise bias point.

- Forward and reverse gate characteristics

Several measurements can be used to characterize the Schottky-barrier gate of a GaAs FET; we used:

V_{GF} = forward gate voltage

= V_G for I_G = 20 mA

I_{GR} = reverse gate leakage current

= I_G for V_G = -5 V

BV_G = gate breakdown voltage

= V_G for I_G = -10 μA .

In all cases, the drain is shorted to the source (V_D = 0 V).

The above values are generally measured using a Tektronix 576 Curve Tracer operated in the 300-μsec pulse mode. In addition to these specific parameter measurements, a photographic record of the full family of I-V curves is also made for backup purposes.

During the Phase-II accelerated life tests (see Section 3.C), control FETs were always characterized along with the test samples to calibrate and monitor the dc and rf characterization measurements. These control FETs were never exposed to the accelerated stresses of the life tests. Their parameters can be assumed, therefore, to have remained relatively unchanged throughout the test period, and their measurement data can be used to determine the repeatability or measurement error associated with each parameter measurement. Table 2 shows the results of this analysis for the dc measurements. For each of the nine control FETs, Table 2 lists the approximate number of times the FET was dc characterized, the average measured value of each parameter, and the standard deviation of each parameter measurement. At the bottom of the table, the standard deviations are shown for all of the measurements; these values are shown both in absolute terms and as percentages of the average parameter values. The measurement errors are small relative to the typical 10% failure criteria placed on the dc parameters (Section 3.A). These measurement errors can be reduced still further by using the photographic records of I-V curves to correct or reject questionable recorded values. In the case of the specific drain current I_{DS}, which has the largest associated error, most gross errors can be attributed to poor probe contact. This error could be reduced by making contact more than once and observing if the linear slope of the I-V curve changes.

b. RF Characterization

(1) Minimum Noise Figure and Associated Gain — The minimum noise figure F_{min} and associated gain G_a are measured at 10 GHz. These device characteristics are tracked not only because they are a direct indication

Table 2. Summary of DC-Parameter Measurements for Control FETs

FET Type	Control FET	No. of Times Measured	Average Value (Standard Deviation)									
			I_{DSS}, mA		I_{DS}, mA		V_{GB}, V		V_P, V		g_m, mmho	
A2	A2-C1	59	49.41	(0.35)	33.38	(0.70)	-1.327	(0.010)	-2.317	(0.026)	19.21	(0.16)
	-C2	31	36.36	(0.33)	25.58	(0.28)	-0.896	(0.009)	-1.797	(0.009)	20.40	(0.14)
	-C3	46	44.78	(0.36)	30.32	(0.79)	-1.275	(0.008)	-2.334	(0.014)	17.56	(0.15)
B	B-C1	19	44.57	(0.59)	22.02	(0.21)	-1.623	(0.020)	-2.539	(0.022)	16.98	(0.18)
	-C2	19	27.65	(0.25)	15.71	(0.16)	-0.792	(0.012)	-1.673	(0.012)	17.64	(0.18)
	-C3	15	38.01	(0.28)	19.89	(0.27)	-1.268	(0.011)	-2.163	(0.016)	17.55	(0.13)
C	C-C1	20	36.97	(0.28)	18.79	(1.05)	-1.472	(0.019)	-2.864	(0.041)	12.67	(0.18)
	-C2	12	37.32	(0.40)	19.44	(0.20)	-1.468	(0.011)	-2.737	(0.013)	13.54	(0.11)
	-C3	19	27.57	(0.19)	15.51	(0.17)	-0.979	(0.010)	-2.211	(0.017)	13.65	(0.92)
A11	A11	240	38.07	(0.35)	22.29	(0.59)	-1.233	(0.012)	-2.293	(0.021)	16.58	(0.29)
				(0.9%)		(2.6%)		(1.0%)		(0.9%)		(1.7%)

6256

of operational performance, but also to investigate the correlations between the aging characteristics of the dc and rf parameters. Measuring rf characteristics is considerably more expensive and time consuming than measuring dc characteristics; therefore, if significant correlations can be obtained, cost and time savings can be made by relying primarily on dc measurements, with rf measurements used only for spot checks and confirmation.

A schematic of the F_{min}/G_a measurement system is shown in Figure 11. The device under test (DUT) is mounted between two double-slug tuners. This combination forms a single-stage amplifier, which is manually tuned for minimum 10-GHz noise figure. The calibrated noise source and precision noise figure meter are connected to the amplifier input and output ports, respectively, for this purpose. The associated gain of the amplifier is measured by switching its input to the 10-GHz sweep oscillator signal and its output to the microwave power meter. The measured noise figure F_{meas} and associated gain G_a are then used to calculate the minimum noise figure F_{min} of the FET:

$$F_{min} = F_{meas} - \frac{F_o - 1}{G} \quad ,$$

where F_o is the measured noise figure of the output circuitry consisting of the output bias tee, isolator, switch, mixer, i.f. amplifiers, etc. No correction is attempted for the losses of the double-slug tuners.

Table 3 summarizes the results of these F_{min}/G_a measurements on the accelerated-life-test control FETs (Section 3.C). The rf failure criteria adopted for the life tests are ΔF_{min} = 0.5 dB and ΔG_a = -1.0 dB. The combined rf measurement errors (standard deviations), as shown at the bottom of Table 3, are thus 26% and 32%, respectively, of these limits. At least two factors contribute to these relatively large measurement errors. First, the SMA coaxial connectors used in the measurement system are sensitive to mechanical stresses and can have relatively poor repeatability. Second, tuning the input and output double-slug tuners is subject to operator error. Because of the difficulty and cost of making these measurements, some investigators have used fixed-tuned single-stage amplifiers for rf

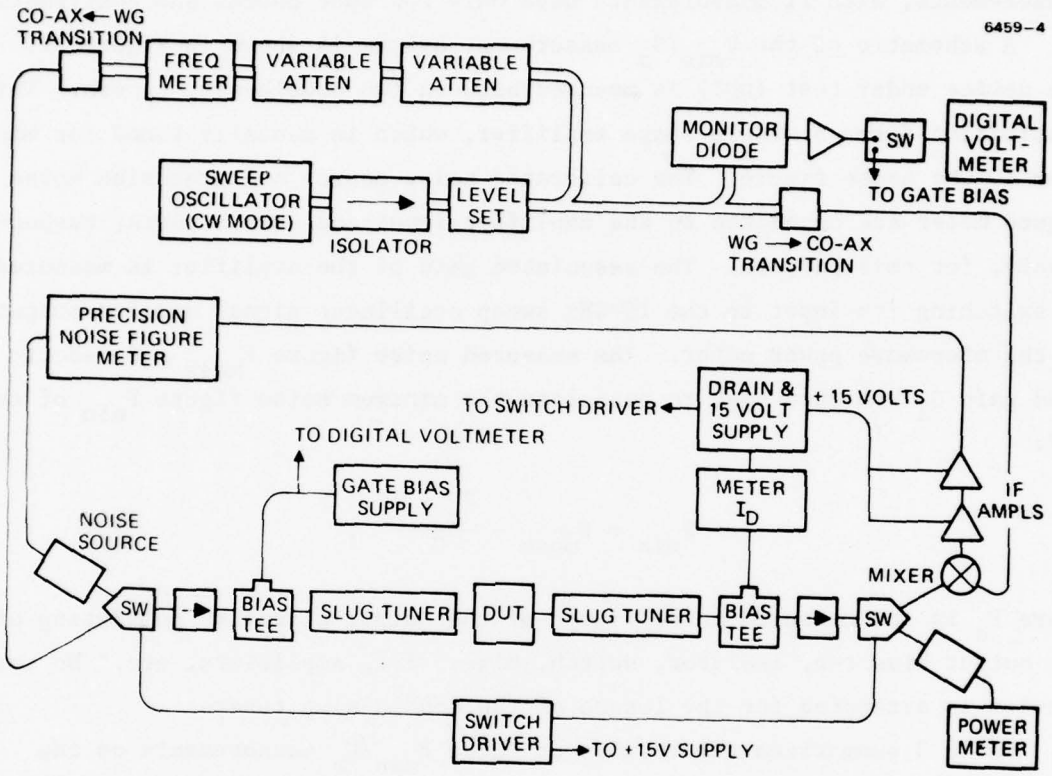


Figure 11. 10-GHz noise figure and gain measurement system.

Table 3. Summary of RF Measurements for Control FETs

FET Type	Control FET	Number of Times Measured	Average Value (Standard Deviation)	
			F_{min}, dB	G_a, dB
A2	A2-C1	18	3.097 (0.127)	5.990 (0.309)
	-C2	12	3.070 (0.122)	6.132 (0.361)
	-C3	14	3.381 (0.169)	6.006 (0.313)
B	B-C1	8	3.119 (0.122)	6.659 (0.219)
	-C2	6	3.332 (0.140)	7.400 (0.491)
	-C3	8	3.086 (0.082)	7.000 (0.256)
C	C-C1	9	3.623 (0.112)	6.499 (0.406)
	-C2	6	3.455 (0.194)	7.103 (0.340)
	-C3	8	3.466 (0.124)	6.793 (0.380)
All	All	89	(0.129)	(0.324)

6256

measurements.[7] Although this significantly reduces measurement error and operator time required, it makes it difficult to extract the actual device rf characteristics from the overall circuit characteristics.

(2) S-parameters — The HP 8542B automatic network analyzer (ANA) is capable of making detailed scattering-parameter measurements to 18 GHz. The ANA configuration is standard and will not be described here. The measured S-parameters can be used to calculate the impedance or admittance characteristics of the DUT. The data can also be used to calculate the maximum available gain (MAG), maximum stable gain (MSG), etc. of the device

as a function of frequency. Because for this study we are interested in the low-noise operation of the tested GaAs FETs, all S-parameter measurements were made with dc bias set at V_D = 3 V and I_D = 10 mA.

2. Electrical Characterization of Test Devices

The test samples were characterized before being subjected to any of the stress tests. Table 4 lists the average values measured for the usual dc and rf parameters. The measured parameter spreads are indicated by the standard deviations (σ's), shown parenthetically. The three FET types are quite similar in most respects, but some specific differences are noted. The specific drain current I_{DS} is 50% higher for Type A2 than for the other two. The former uses an etched-channel process to thin the active layer under the gate only; thus, its source and drain parasitic resistances are probably smaller. The Type-C FETs have 57% higher gate voltages, probably because of slightly thicker channels. These higher voltages are reflected in a lower transconductance g_m. The Type-A2 gates had the highest forward voltage V_{GF} and reverse leakage (i.e., the smallest breakdown voltage BV_G).

At 10 GHz, the minimum noise figure of the Type-C FETs was 0.5 dB higher than that of the other two, and the Type-B FET had almost 1 dB more gain. Two points should be noted with respect to this rf data. First, the data probably does not indicate the optimum performance of these devices. The measurements were performed with the devices mounted on the 1 cm square microstrip carriers, and the double-slug tuners were mounted outboard of the coax-microstrip transitions. Therefore, optimum tuning probably was not achieved. In a well-designed amplifier, the tuning circuits would be situated very close to the GaAs FET chip so that better source and load impedances could be provided. Second, data was presented above showing that significant measurement errors can occur in these rf parameter measurements, especially in the case of the associated gain G_a, where σ_{meas} = 0.3 dB. Care should be taken, therefore, in comparing the F_{min}/G_a data of these three FET types.

Approximately 18 samples of each FET type were measured for their S-parameters from 2 to 18 GHz. All of the devices were dc biased at V_D = 3 V

Table 4. Average Parameter Values and Standard Deviations Measured for the GaAs FETs prior to Testing

Parameter	Average (Standard Deviation)					
	Type A2		Type B		Type C	
DC						
I_{DSS}, mA	45.3	(5.6)	38.4	(6.5)	43.0	(12.2)
I_{DS}, mA	30.4	(3.4)	20.2	(2.6)	20.7	(4.6)
g_m, mmho	19.4	(1.0)	17.2	(0.3)	12.3	(1.5)
V_{GB}, V	- 1.18	(0.18)	- 1.26	(0.30)	- 1.90	(0.78)
V_P, V	- 2.24	(0.32)	- 2.16	(0.31)	- 3.48	(0.98)
V_{GF}, V	1.69	(0.17)	1.12	(0.06)	0.89	(0.02)
BV_G, V	- 5.90	(0.49)	-20.2	(0.6)	-19.1	(6.9)
RF (10 GHz)						
F_{min}, dB	3.10	(0.14)	3.06	(0.14)	3.63	(0.12)
G_a, dB	6.40	(0.47)	7.32	(0.47)	6.53	(0.62)

6256

and I_D = 10 mA to simulate low-noise-bias conditions. Thus, the measurement results only approximate optimum low-noise characteristics. Tables 5 through 7 list the average S-parameter values for the three FET types. Phase corrections were made to place the reference planes at the ends of the carrier microstrip lines where the FET chips are wire bonded; no other corrections were made for the carriers or coax-microstrip transitions. The listed S-parameters can be used to calculate other device parameters (e.g., impedance matrix, admittance matrix, gain, stability). The maximum available gain G_A was calculated and is included in the tables. Since, at the lower frequencies, these FETs typically are not unconditionally stable, G_A is undefined. At these frequencies, we have listed the unilateral gain G_U. Note that at 18 GHz these devices are still capable of 5 or 6 dB gain.

Table 5. Average S-Parameeters of Type-A2 GaAs FETs: V_D = 3V, I_D = 10 mA

Frequency, GHz	S_{11}		S_{21}		S_{12}		S_{22}		Gain	
	Magnitude	Angle, deg	Magnitude	Angle, deg	Magnitude	Angle, deg	Magnitude	Angle, deg	G_A, dB	G_U, dB
2	0.957	-21	1.596	156	0.039	77	0.713	-12	-	-
4	0.926	-37	1.441	139	0.060	72	0.728	-18	-	14.96
6	0.793	-51	1.347	126	0.074	69	0.644	-19	10.07	9.24
8	0.785	-66	1.392	113	0.086	65	0.606	-29	10.72	9.04
10	0.681	-91	1.287	85	0.092	50	0.605	-48	7.50	
12	0.627	-112	1.137	74	0.091	47	0.520	-58	5.05	
14	0.698	-130	1.092	57	0.101	52	0.528	-69	6.18	
16	0.608	-142	0.872	41	0.102	50	0.479	-98	2.48	
18	0.703	-125	0.801	49	0.106	80	0.668	-87	5.53	

6256

Table 6. Average S-Parameters of Type-B GaAs FETs: V_D = 3V, I_D = 10 mA

Frequency, GHz	S_{11}		S_{21}		S_{12}		S_{22}		Gain	
	Magnitude	Angle, deg	Magnitude	Angle, deg	Magnitude	Angle, deg	Magnitude	Angle, deg	G_A, dB	G_U, dB
2	0.968	-18	1.530	161	0.018	83	0.805	-6	-	20.13
4	0.948	-31	1.429	145	0.025	92	0.830	-7	-	18.08
6	0.811	-44	1.361	134	0.031	104	0.757	-5	11.89	11.02
8	0.785	-61	1.448	123	0.031	101	0.718	-5	11.40	10.56
10	0.655	-89	1.443	94	0.045	100	0.814	-20	11.67	
12	0.586	-116	1.268	80	0.048	93	0.698	-26	7.42	
14	0.627	-136	1.182	64	0.070	101	0.749	-27	8.77	
16	0.551	-154	1.071	49	0.093	90	0.674	-50	6.15	
18	0.598	-143	0.943	46	0.104	108	0.786	-56	-	

6256

Table 7. Average S-Parameters of Type-C GaAs FETs: V_D = 3V, I_D = 10 mA

Frequency, GHz	S_{11}		S_{21}		S_{12}		S_{22}		Gain	
	Magnitude	Angle, deg	Magnitude	Angle, deg	Magnitude	Angle, deg	Magnitude	Angle, deg	G_A, dB	G_U, dB
2	0.975	-15	1.211	163	0.019	84	0.799	-6	-	18.61
4	0.969	-25	1.153	150	0.027	87	0.828	-7	-	-
6	0.843	-35	1.130	140	0.038	100	0.751	-6	10.82	10.07
8	0.826	-48	1.222	129	0.037	85	0.712	-8	10.36	9.84
10	0.745	-73	1.251	101	0.048	84	0.798	-24	11.18	
12	0.633	-96	1.135	88	0.053	73	0.692	-29	6.49	
14	0.683	-116	1.097	71	0.061	78	0.706	-31	7.61	
16	0.566	-136	0.982	53	0.080	71	0.647	-54	4.52	
18	0.642	-124	0.854	52	0.076	93	0.760	-61	6.36	

6256

SECTION 3

ACCELERATED LIFE TESTS

The aging characteristics and operational life times of the GaAs FETs were investigated by subjecting test samples to accelerated life tests at elevated ambient temperatures, under both unbiased and low-noise-biased conditions. Visual, dc, and rf characteristics of the devices were monitored periodically during these tests, and the results were used to measure the degree of aging, signal device failure, and determine primary failure modes. This section describes these tests and their results.

A. INTRODUCTION

The accelerated life tests were of the constant-stress type. The samples were subjected to constant temperature and electrical stress levels throughout the test period. The only changes in stress occurred when the samples were brought down to room temperature and bias was removed for the purpose of periodic characterization measurements. After being characterized, the samples were returned to their designated elevated stress levels and the next cycle was started.

The constant-stress life tests were performed in HRL-developed bias ovens of the type originally used for our INTELSAT-funded GaAs FET reliability study.[6] Figure 12 shows one of these ovens with its insulated cover removed. The heart of the oven consists of a stainless-steel block, which is heated along its full length by a cartridge heater. The GaAs FET test samples, mounted on their alumina microstrip carriers, are mounted in the chamber of the stainless-steel block and covered by a quartz lid. During operation, the oven chamber is continuously purged with slowly flowing dry nitrogen derived from a liquid source. Each oven has 10 positions for dc-biased samples and approximately 20 positions for unbiased samples. Gate and drain bias is brought into each sample position with $\sim$ 50-Ω coaxial transmission lines consisting of stainless-steel and glass tubing and nickel wire. These coaxial lines extend through the insulated walls of the oven to the outside where, at room temperature, the coaxial lines

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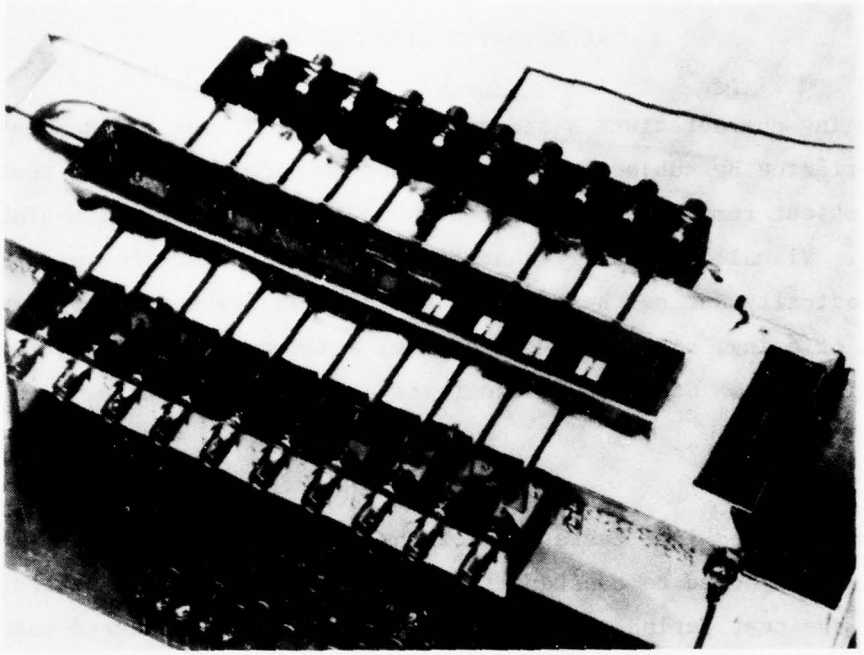


Figure 12. HRL-developed bias oven with cover removed. The samples in positions 1 through 6 are covered by hold-down clamps; those in positions 7 through 10 are shown uncovered.

connect to gate and drain bias filters. These are essentially low-pass RC filters that act to reduce any tendancy of the biased FETs to oscillate. The bias circuit for an oven is shown in Figure 13. All of the biased FETs in an oven share common gate and drain dc power supplies. Individual voltage dividers are inserted between the gate supply bus and the individual gate bias filters. This allows separate control of each test sample.

The low-noise-bias conditions used throughout these tests are V_D = 5 V and I_D = 10 mA. Hughes Space and Communications Group has found this bias state to be close to optimal for low-noise GaAs FET amplifiers when noise figure, gain, and third-order intermodulation are considered. It thus represents a realistic electrical stress level for simulating actual operational bias stress.

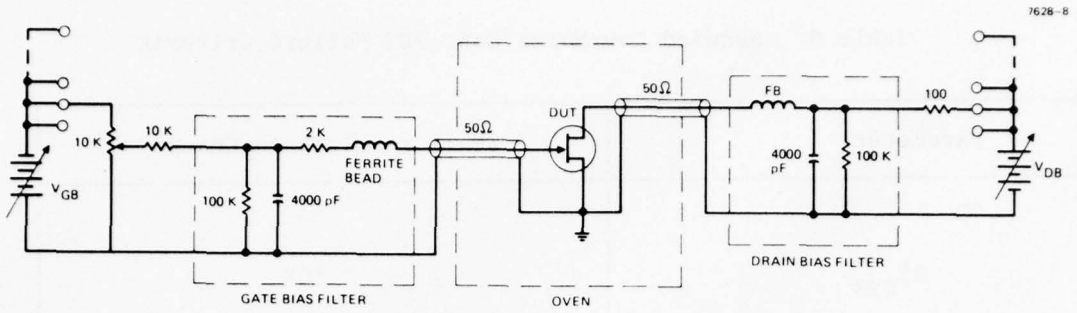


Figure 13. Bias circuit for test oven.

Two objects of this investigation were to estimate the expected MTTF for operational GaAs FETs and to estimate the activation energies E_a of the primary failure modes. To do these required that we specify criteria for determining when a device has failed. The criteria adopted for this program are listed in Table 8. For two of the important dc parameters, I_{DSS} and g_m, functional failure of the GaAs FET is assumed to have occurred if one of these parameters has changed by 10% or more. The specific drain current I_{DS}, however, is allowed a larger variation (20%). These criteria are similar to those selected by NEC,[4] which were based on the results of a sensitivity analysis of the equivalent circuit model for a low-noise NEC GaAs FET. Because most state-of-the-art FETs have similar equivalent circuits, in spite of differences in layout or processing, the NEC failure criteria, if valid for their devices, should also be reasonably valid for others.

Ultimately, of course, the microwave aging characteristics of the FETs become of greater operational importance than the dc characteristics. For low-noise amplifier applications, we have assumed, as shown in Table 8, that an increase of 0.5 dB or more in minimum noise figure or a decrease of 1 dB or more in the associated gain represents reasonable limits for signifying rf operational failure. These failure criteria apply to measurements of device minimum noise figure, in which the bias and input/output

Table 8. Assumed Low-Noise GaAs FET Failure Criteria

Parameter	Failure Limit on Change
DC	
ΔI_{DSS}	± 10%
ΔI_{DS}	± 20%
Δg_m	± 10%
RF	
ΔF_{min}	+ 0.5 dB
ΔG_a	- 1.0 dB

6256

tuning conditions are adjusted each time to obtain F_{min}. An argument can be made for defining failure on the basis of measurements performed with specific fixed bias and tuning conditions since these would represent the most likely conditions of circuit application. This was not done on this program, however, because (1) considerable effort and expense would have been required to design, fabricate, and tune the necessary single-stage amplifiers; and (2) we were more interested in the aging characteristics of the FETs themselves than of circuits incorporating them. The techniques involved in measuring the rf parameters of a GaAs FET are generally more difficult, expensive, and time consuming than those required to measure its dc parameters. And, as shown in Section 2.B, rf measurement errors are significantly larger with respect to the failure criteria than are the dc measurements. Therefore, throughout the accelerated-life tests, we rely only on the dc failure criteria for determining device failure. The rf measurements, when used, are made on a more limited basis and are used to investigate the relationships between dc and rf aging characteristics. Even though some investigators[7] have concluded that there is no reliable or consistent relationship between dc parameter changes and rf failure,

we believe that the dc data still provides valuable information with respect to device aging. Our data[6] also shows that there is some statistical correlation between dc and rf changes, although the considerable scatter tends to obscure this relationship for any single device.

B. ACCELERATED LIFE TESTS — PHASE I

The Phase-I accelerated life tests were intended to provide preliminary reliability information on the Type-A GaAs FETs and test data for use in planning the more complete Phase-II tests to follow. The Type-A1 FETs, which have no SiO_2 protection layer, were selected to be tested because, at the time these tests were started, the Type-A2 FETs were not available. The device characteristics monitored during these tests were limited to visual appearance and the usual dc I-V parameters.

Table 9 shows the planned test sample distribution and stress schedule. Three ovens were to be used, each containing 10 low-noise-biased samples and 10 unbiased samples. The Phase-I tests were intended to be limited to several months duration. Since dc-biased Type-A1 GaAs FETs had previously been tested successfully for 400 hr at 260°C ambient, it was expected that 270°C was a reasonable maximum stress temperature to use. Both the 270°C and 240°C test groups were started, and each oven completed at least four stress cycles. Before the 255°C test groups could be started, nearly all of the 270°C samples, including both biased and unbiased devices, had experienced catastrophic gate failure caused by Au-Al intermetallic formations. This interaction involved Al from the gate leads and Au from the gate bond pads. This interaction causes the gate lead aluminum to be consumed, which eventually causes open circuits to develop. This results in a loss of gate control over source-drain current and device failure. Almost at the same time, catastrophic gate failures began occurring in another GaAs FET reliability study[6] that we were conducting at 270°C. At or below 260°C, however, this failure mechanism was not occurring. Because this gate failure mechanism is important only at high test temperatures, the results from the 270°C test groups cannot be used to estimate the operational lifetimes of GaAs FETs at

Table 9. Phase-I Accelerated Life Test Schedule

Ambient Stress Temperature	Initial Sample Size	
	LNB[a]	UB[b]
270°C	10	10
255	10	10
240	10	10

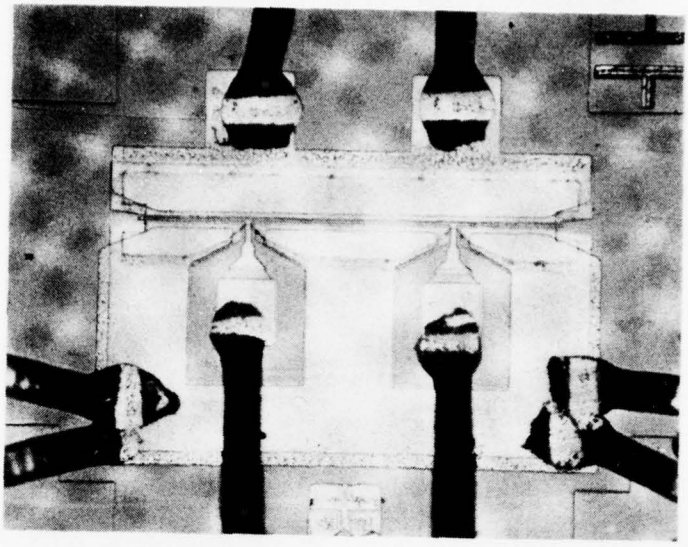
[a] LNB = low-noise biased (V_D = 5 V, I_D = 10 mA).

[b] UB = unbiased.

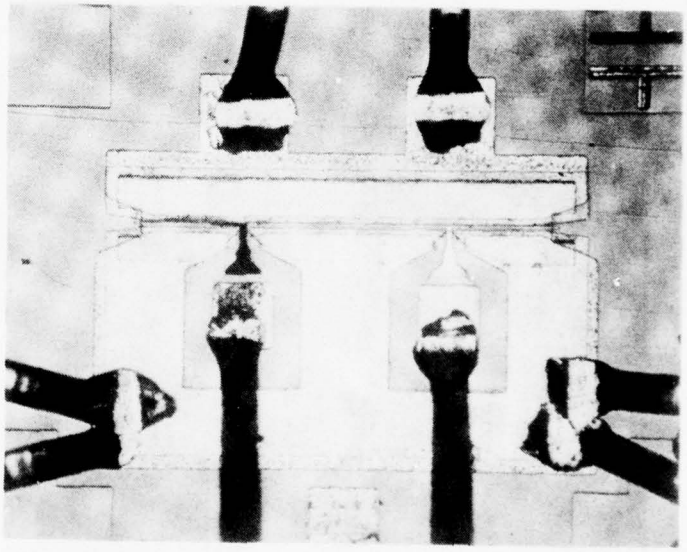
6256

lower ambient temperatures. Therefore, it was decided to terminate the Phase-I life tests and concentrate our efforts on the more extensive Phase-II life tests. Consequently, the 255°C Phase-I test groups were never started.

The gate-pad failure mechanism can be illustrated with photomicrographs taken during the GaAs FET reliability study reported on in Ref. 6. Figure 14(a) shows an FET prior to the start of accelerated life tests. Figure 14(b) shows the same device after 431 hr at 270°C ambient. The left-hand gate bond pad and a portion of the gate itself are severely degraded by Au-Al plague, to the point where there was partial loss of gate control. The right-hand gate pad appears unaffected. The black, lava-textured Au-Al plague extends from the bottom edge of the aluminum, where it overlays a portion of the chromium "bridge," up to the gate stripe, and left along the aluminum gate. In addition, the gate-pad gold layer has become dark and roughly textured. The foot of the gold wire bond is also pitted. Only the chromium bridge between the gate aluminum and bond-pad gold appears undisturbed. An SEM photo of the left gate-pad region of the same device is shown in Figure 15; here the Au-Al



(a) BEFORE START OF LIFE TESTS.

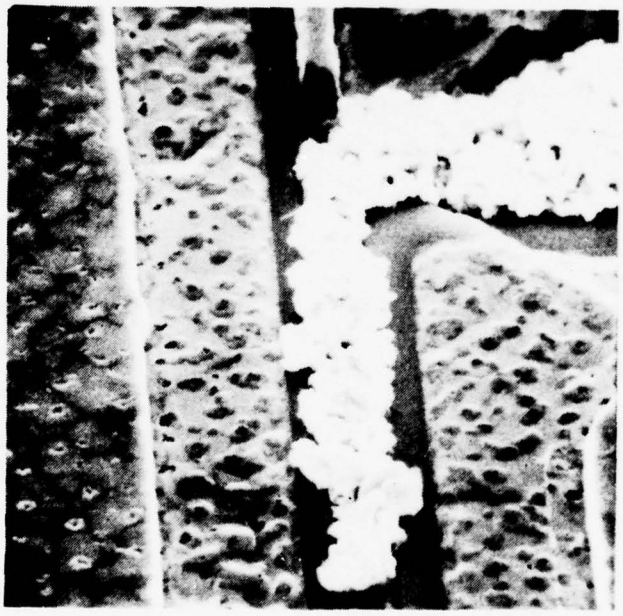


(b) AFTER 431 HOURS AT 270°C, UNDER BIAS.

Figure 14. Photomicrographs (200x) of 200°C test sample showing gate pad plague formation.

6459-21

(a) LEFT GATE-PAD REGION (1050 X).



(b) PLAGUE FORMATION ON GATE STRIPE (5300 X).

Figure 15. SEM photograph of deteriorated left gate pad and gate stripe.

plague is white. In the roughly textured gold areas of the gate pad, some of the gold has been removed down to the underlying chromium layer. This region has been the source of gold to feed the growth of the plague along the aluminum metalization. Pits in the foot of the gold-wire bond have also been sources. Plague growth along the gate stripe is shown in Figure 15(b). SEM examination of the good region, the right-hand gate pad, gave no evidence of any changes occurring.

The gate pad design used in these FETs was selected because tests had indicated that chromium would act as an effective barrier between gold and aluminum metalizations. This conclusion has been supported by our GaAs FET life tests performed at temperatures below 270°C ambient. An electron microprobe analysis of the same sample was performed. Figure 16(a) shows the SEM image of the deteriorated left gate pad as scanned by the microprobe analyzer. This view is identical to that scanned during constituent analysis, and there is an exact one-to-one spatial correspondence between the SEM image and the following elemental scan images. The microprobe gold scan (AuLα) is shown in Figure 16(b); the gold count density is nearly uniform throughout the nominal gold, chromium, and aluminum regions. Similarly, Figure 16(c) shows that aluminum exists throughout the same regions. Thus, both gold and aluminum have been transported across the chromium "barrier" and throughout the gate pad region, leading to the Au-Al interaction formations. In contrast, chromium (CrKα), gallium (GaLα), and arsenic (AsLα) scans indicated no unexpected distribution patterns and no evidence of any transport. Similar microprobe scans were also performed on the undeteriorated right-hand gate pad of the same device. These showed no evidence of transport of any of the scanned elements. This is common: one gate pad will develop the plague before the other. Only infrequently do both pads develop the plague during the same stress cycle. However, if a device is kept in test after its first pad has deteriorated, the second pad will ultimately develop plague also.

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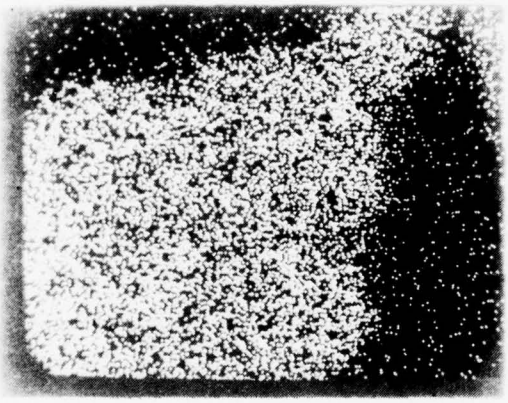
(a) SEM VIEW OF SCANNED AREA.



(b) Au SCAN

(c) Al SCAN

Figure 16.
Electron microprobe analysis of a deteriorated gate pad showing the SEM view of the analyzed area, plus the gold and aluminum element scan results.

C. ACCELERATED-LIFE TESTS: PHASE II

Most of the effort expended in the reliability investigation was put into the Phase-II life tests. Approximately 120 GaAs FETs (from three manufacturers) were tested. Electrical characterization included rf noise figure and gain measurements and the usual dc measurements. Both low-noise-biased and unbiased samples were used.

Table 10 shows the device distribution and the stress schedule for the several test groups. Each test group occupied a separate test oven, except for the 200°C test groups, in which all three FET types occupied a single oven. The table also shows the total number of stress cycles completed by each group and the total accumulated stress time. Some samples had received up to 3625 hr of stress by May 1978. It was originally planned that all three FET types would have test groups stressed at 245°C to permit their test results to be more easily compared. However, after the Type-C 245°C tests were under way, it was discovered that the high-temperature gate leakage current of the Type-B FETs is significantly greater than those of the other two FET types. To make the maximum leakage currents and possible electromigration effects approximately equal for the three FET types, a maximum stress temperature of 216°C was selected for Type B.

The Phase-II constant-stress test procedure (Figure 17) was basically the same as for the Phase-I tests. However, the characterization procedures were more extensive for Phase II. In addition, unstressed control FETs were introduced to monitor characterization-measurement fluctuations and drifts, and a special measurement procedure was instituted to determine if the results of the dc characterization of the low-noise-biased devices is sensitive to the time delay between the removal of electrical stress and the actual start of dc measurements. The results of using the control FETs to characterize dc and rf measurement errors is discussed in Section 2.B. The findings regarding immediate versus delayed dc characterization are presented below.

Table 10. Breakdown of Phase-II Accelerated-Life Test Groups and Accumulated Stress

FET Type	Ambient Stress Temperature	Initial Sample Size		No. of Cycles Completed	Total Accumulated Hours
		LNB[a]	UB[b]		
A2	245°C	10	10	6	2827
	231°C	10	10	7	2637
	216°C	10	10	5	2607
	200°C	4	4	5	3531
B	216°C	10	10	8	3625
	200°C	3	3	5	3531
C	245°C	10	10	8	3408
	200°C	3	3	5	3531

[a] LNB = Low-noise biased (V_D = 5V, I_D = 10mA).

[b] UB = Unbiased.

6256

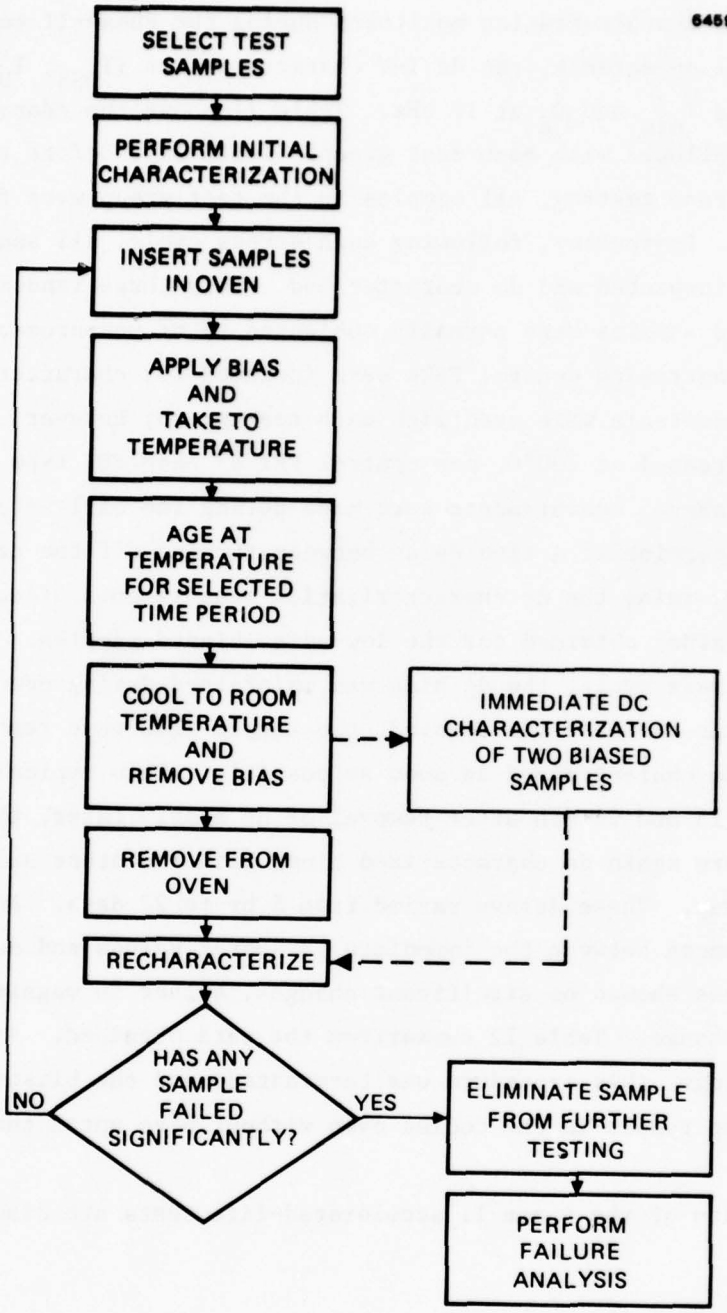


Figure 17. Phase-II constant-stress test procedure.

The device characteristics monitored during the Phase-II tests included visual appearance, the dc I-V characteristics (I_{DSS}, I_{DS}, V_{GB}, V_p and g_m), and F_{min} and G_a at 10 GHz. Table 11 shows the characterization routine followed with each test group. Initially, before the start of constant-stress testing, all samples in the test group were fully characterized. Thereafter, following each stress cycle, all samples were visually inspected and dc characterized. Only three randomly selected biased samples were normally subjected to rf measurement, however. Also, unstressed control FETs were included for characterization. Normally, two controls were used with each test group; however, for the mixed group stressed at 200°C, one control FET of each FET type was used.

As noted above, measurements were made during the early stages of Phase II to determine if a time delay between turning off the dc bias stress and performing the dc characterization measurements affected the dc parameter values obtained for the low-noise-biased samples. At the end of each stress cycle, the dc bias was maintained during oven cool down. Then, as soon as the bias was removed, two sample FETs were removed from the oven and dc characterized as soon as possible. This typically took place between 13 and 23 min after removal of dc bias. Later, the same two samples were again dc characterized along with the other samples in their test group. These delays varied from 5 hr to 27 days. Analysis of the differences between the immediate parameter values and delayed parameter values showed no significant changes, either in magnitude or direction of change. Table 12 summarizes the data obtained. As a result of these findings, this procedure was terminated, and the biased samples were allowed to remain in the cooled oven without bias until they were characterized.

The results of the Phase II accelerated-life tests are discussed below.

1. Type-A2 Life Tests

a. DC Parameters

The most extensive series of life tests were performed on the Type-A2 GaAs FETs. Four test groups were stressed at temperatures of

Table 11. Phase-II Life Test Characterization Schedule Showing the Number of Samples Examined for Each Characterization Class

Characterization Class	FET Bias State		Control FETs Included
	Low-Noise Biased	Unbiased	
Initial characterization			
Visual	All	All	2
DC	All	All	2
F_m/G_a at 10 GHz	All	All	2
Subsequent characterizations following stress cycles			
Visual	All	All	0
DC	All	All	2
F_{min}/G_a at 10 GHz	3[a]	None[b]	2

[a] Three samples were randomly selected from biased group.

[b] Randomly selected samples from unbiased group were included, if necessary, to make up for insufficient numbers of unfailed biased samples.

6256

Table 12. Changes in Measured Parameters Following Bias Removal: t_1 = 13 to 23 min, t_2 = 5 hr to 27 days

FET Type	No. of Measurements	Average Measurement Change (and Standard Deviation) between Times t_1 and t_2									
		ΔI_{DS}, mA		$\Delta \lvert V_{GB} \rvert$, V		$\Delta \lvert V_P \rvert$, V		Δg_m, mmho		ΔI_{DSS}, mA	
A2	9	-0.1	(0.3)	0.0	(0.02)	0.0	(0.01)	-0.2	(0.3)	-0.2	(0.3)
B	7	0.6	(1.3)	0.02	(0.01)	0.01	(0.02)	0.4	(0.2)	0.0	(0.6)
C	5	0.3	(0.6)	0.0	(0.05)	~0.15	(0.10)	0.2	(0.5)	~0.5	(0.9)
Typical σ of meas.[a]	240		(0.6)		(0.01)		(0.02)		(0.3)		(0.4)

[a] From Table 2.

6256

245°C, 231°C, 216°C, and 200°C. Figures 18 through 22 show how the dc parameters of the low-noise-biased FETs changed with time. The changes are shown as percentage changes from the initial values measured at t = 0 hr. The solid circles represent the median percentage changes for the test groups. In cases where the median is for a group of reduced size, open circles are shown. This can occur if samples have been removed from the group because of failure or if a particular parameter can no longer be measured for some members of the group. The full sample size N is noted on the curves. If a data point represents less than N, the number in the reduced group is shown parenthetically. In addition to the median change, the maximum and minimum changes for the group are shown by the short horizontal lines connected by a vertical line. Whenever appropriate, the designated failure limits FL, as specified in Table 8, are marked on the ordinate axes. Finally, in most cases, the change of each parameter with time is approximated by a least-squares linear fit to the median-change data points. These linear fits are represented by the dashed curves. They appear to be curved in the figures because of the use of semilogrithmic plots. In calculating the linear fits, each median data point is weighted according to the number of devices contributing to the determination of the median value (i.e., the parenthetically shown numbers).

Figure 18 shows how the specific drain current I_{DS} changed with time for the four low-noise-biased test groups. The specific drain current decreased gradually with time. This is the expected change with age because degradation of the source and drain Ohmic contacts (i.e., increasing resistance) will cause I_{DS} to decrease. Increases in the resistance of the active GaAs channel layer will also decrease I_{DS}. Also, as expected, the rate of degradation increases with stress temperature. Only one device exceeded the ± 20% failure limits designated for this parameter during these measurements. Because this failure was a case of increasing I_{DS} (i.e., $\Delta I_{DS} > 20\%$), it is suspected of being the result of a measurement error.

Figure 19 shows the change in the transconductance g_m with time. Again, g_m decreases with time and the rate of degradation increases with temperature over the range from 216°C to 245°C. The fact that g_m decreases faster

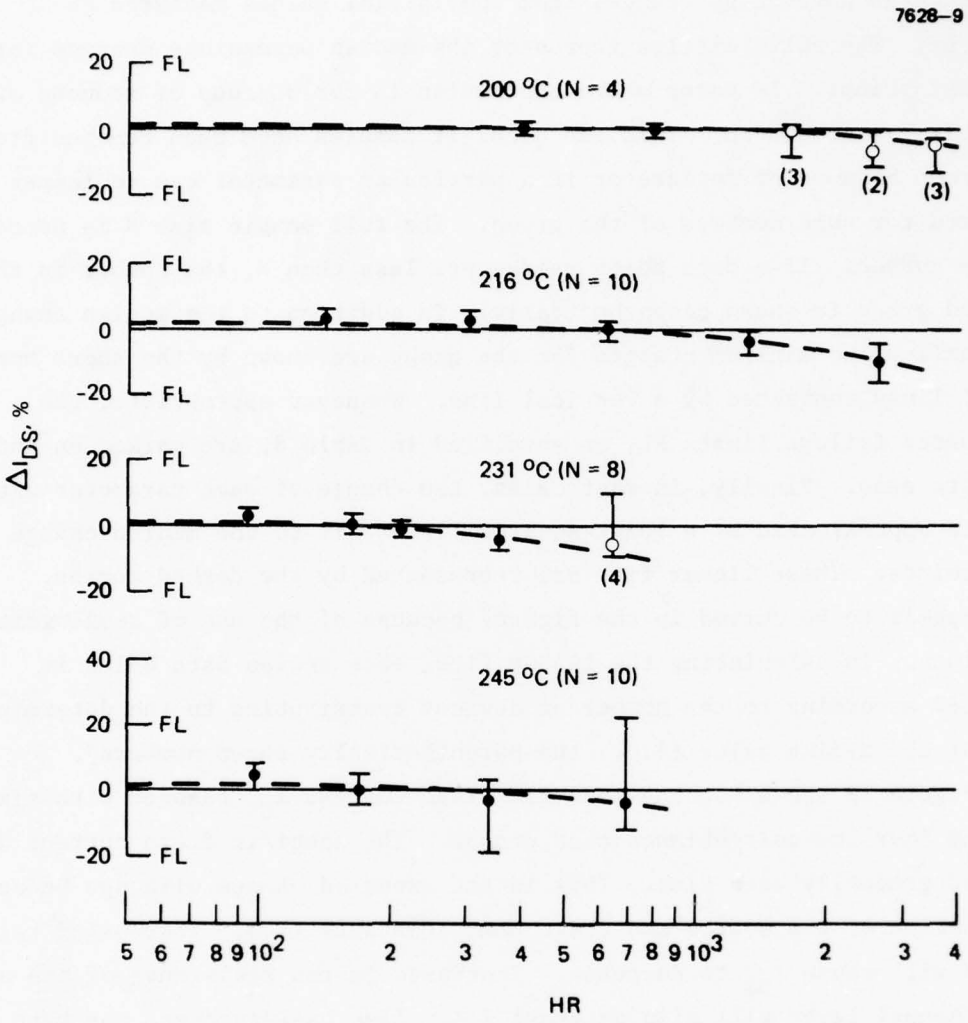


Figure 18. Change in I_{DS} of low-noise-biased Type-A2 FETs.

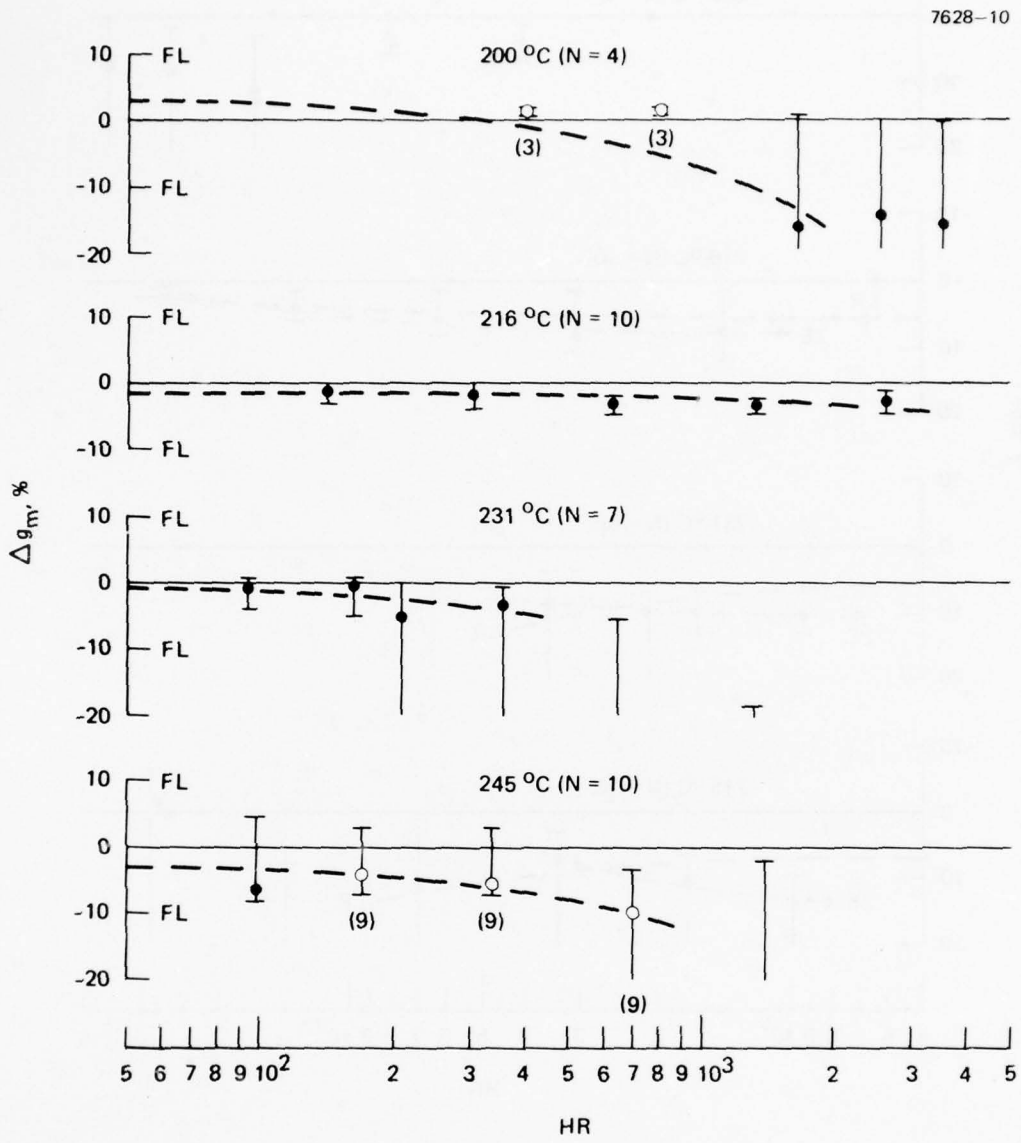


Figure 19. Change in g_m of low-noise-biased Type-A2 FETs.

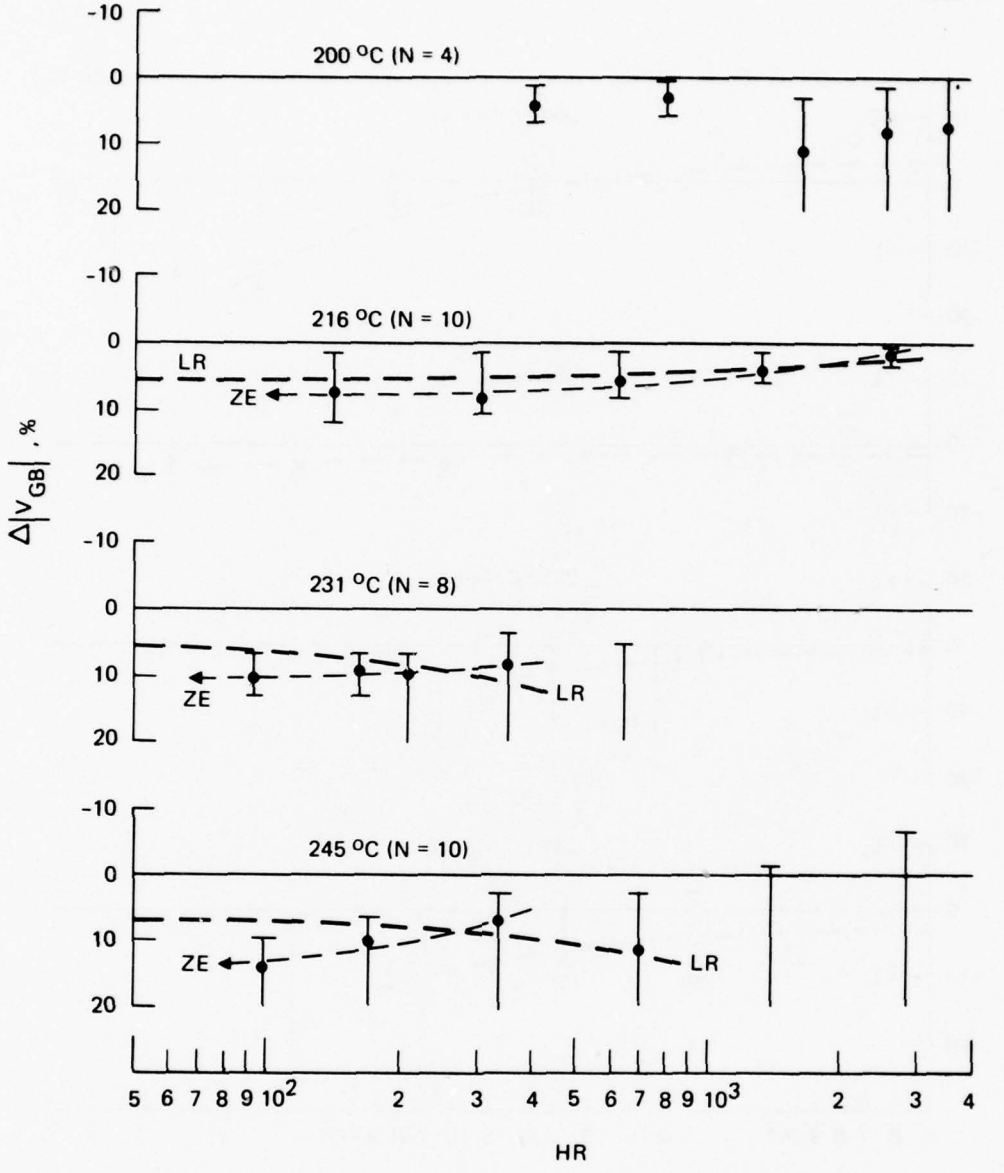


Figure 20. Change in $|V_{GB}|$ of low-noise-biased Type-A2 FETs.

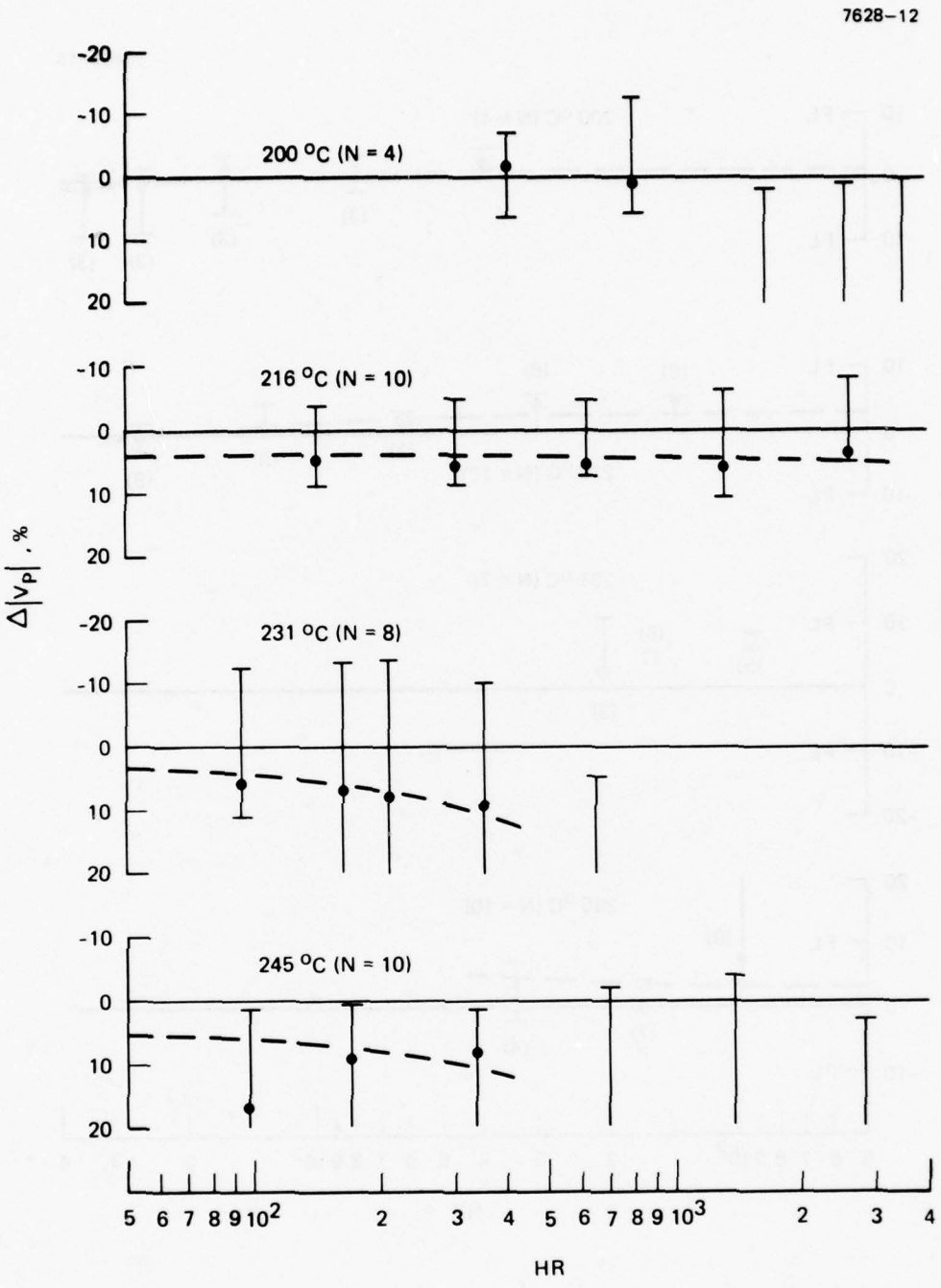


Figure 21. Change in $|V_p|$ of low-noise-biased Type-A2 FETs.

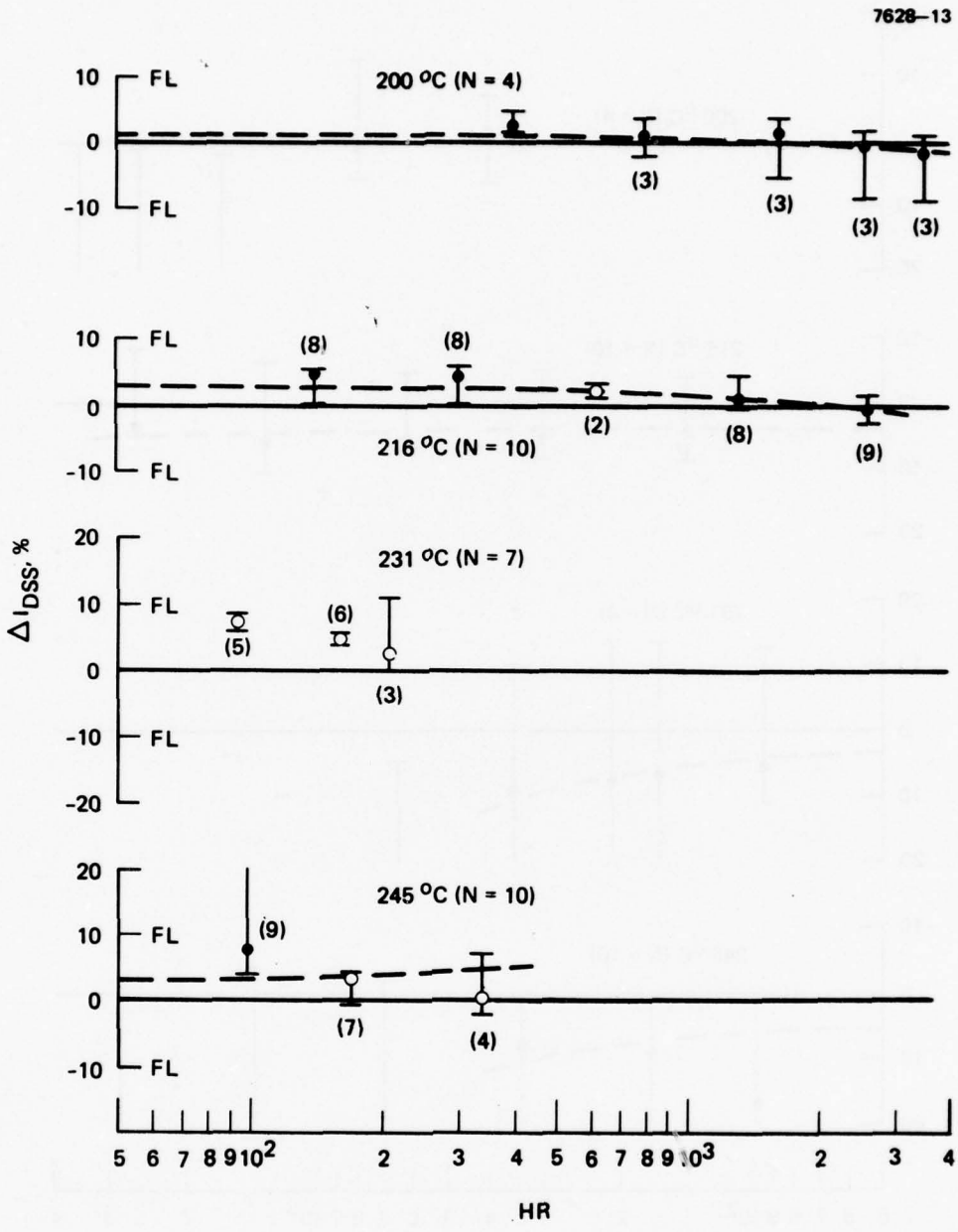


Figure 22. Change in I_{DSS} of low-noise-biased Type-A2 FETs.

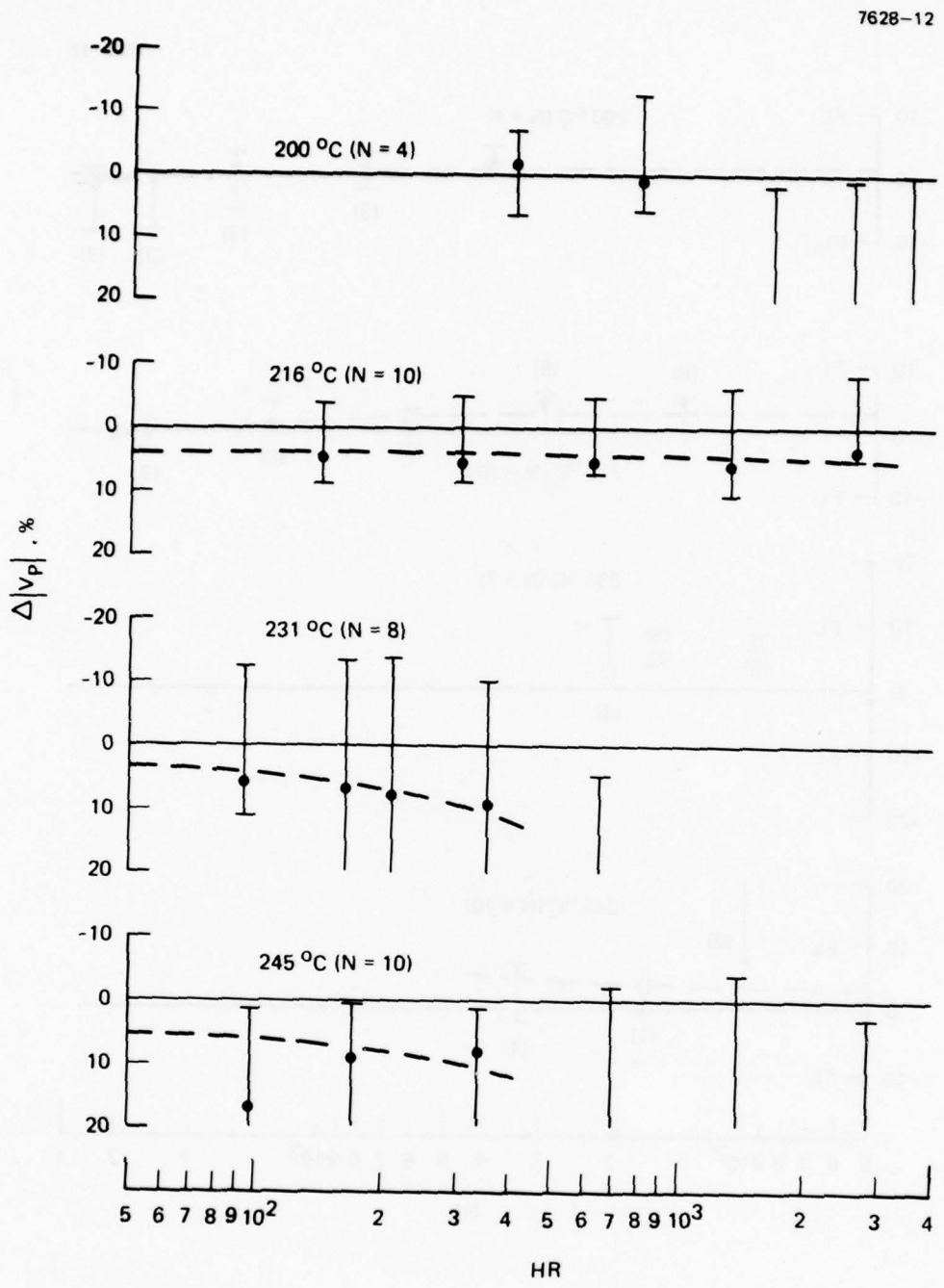


Figure 21. Change in $|V_p|$ of low-noise-biased Type-A2 FETs.

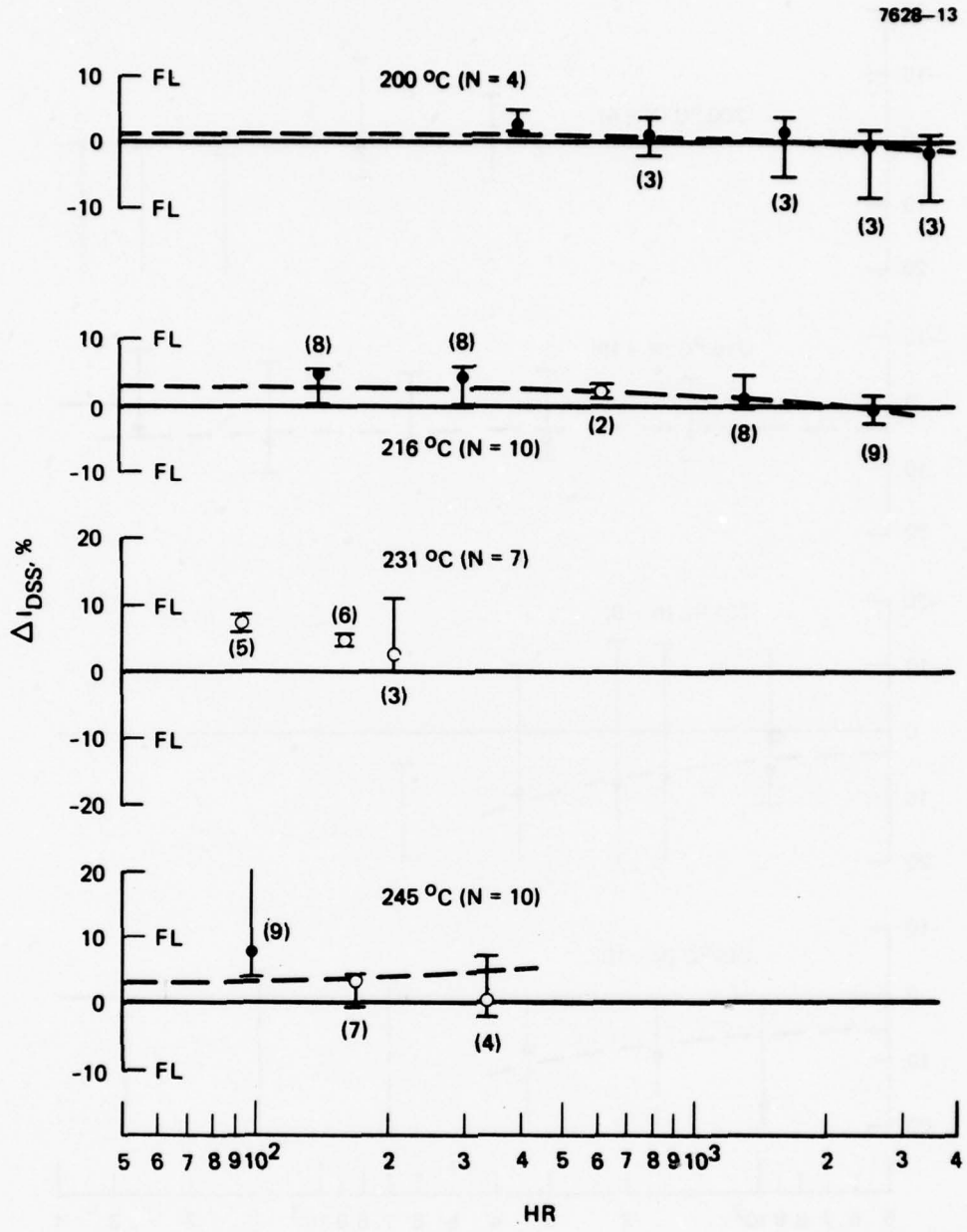


Figure 22. Change in I_{DSS} of low-noise-biased Type-A2 FETs.

in the 200°C group than in the 216°C group is believed to be due to the much smaller 200°C sample size (4 at 200°C versus 10 at 216°C). Several devices exceeded the Δg_m failure limits during these tests. In fact, this is the primary failure mode for these devices. Their rf gain, which should be strongly dependent on g_m, can be expected to decrease with operating lifetime.

The changes in gate voltage characteristics are not direct indicators of device failure because high-quality, low-noise GaAs FET amplifiers, especially those designed for long-life systems, contain bias circuits that adjust gate voltage to achieve constant dc drain current and voltage, not constant gate voltage. The gate parameters are important with respect to the details of device aging, however, and can provide insight into the causes of failure. This is the case with the Type-A2 GaAs FETs tested. Figure 20 shows the changes in gate bias voltage $|V_{GB}|$ with time. This parameter was generally found to increase with time, eventually leading to the failure of g_m. If the failed devices were aged still further, they eventually reached the point where the drain current could no longer be reduced to 10 mA, the specified low-noise bias point. The increase of $|V_{GB}|$ with time is generally shown by the linear regression (LR) fits to the data points of Figure 20. However, after the first stress cycle, there is usually a step increase in $|V_{GB}|$ followed by a steady decrease for the next several stress cycles. Eventually, $|V_{GB}|$ begins to increase again. For the 216°C case, the accelerated-life tests have apparently not progressed long enough for this second increase in $|V_{GB}|$ to appear. The initial step increase in $|V_{GB}|$, as seen for the 216°C to 245°C test groups, suggests the possibility that the gates or SiO_2 layers of these devices might not have been optimally processed. The initial change in $|V_{GB}|$ can be estimated by using the data from the first few stress cycles to extrapolate $|\Delta V_{GB}|$ back to t = 0 (i.e., the fact that $|\Delta V_{GB}| = 0$ at t = 0 is ignored in this extrapolation). The linear curve for this zero-time extrapolation (ZE) is shown in Figure 20 by the dotted curves marked ZE. The zero-time estimates for the 216°C, 231°C, and 245°C groups are $|\Delta V_{GB}|$ = 7.9%, 11.2%, and 15.7%, respectively.

Figure 21 shows the changes in gate pinchoff voltage V_p with time. The general behavior of this parameter is similar to that of V_{GB}, but the changes are generally larger and occur somewhat sooner. When the gate is in the process of losing partial or full control over the drain current, it is to be expected that this will be reflected in V_p sooner than it is in V_{GB}.

The measured changes in the saturated drain current I_{DSS} are shown in Figure 22. Although the long-term trend of this parameter is to decrease, it does display an apparent initial step increase similar to that of the gate voltages. I_{DSS} then decreases steadily from this "initial" value. Several devices eventually exceeded the ±10% failure limits on ΔI_{DSS}, but this failure mode was insignificant relative to Δg_m failure.

The results of the dc parameter measurements on the unbiased test groups are shown in Figures 23 through 27. In general, the rates of change are much slower than for the low-noise-biased test groups. At this writing, only one unbiased test sample has failed; it is in the 245°C group, and its transconductance g_m has decreased by more than 10%.

Figure 23 shows how ΔI_{DS} changed with time for the unbiased devices. For the three highest temperatures, I_{DS} clearly is decreasing; however, at almost 3000 hr, there is still no significant difference in the rates of decrease for these three groups. The saturated drain current I_{DSS} measurements, shown in Figure 24, exhibit even smaller changes than I_{DS}, and there is only a slight hint at a trend toward decreasing values.

Figure 25 shows the changes in g_m with time. The median values of the 216°C and 231°C groups are still virtually unchanged at 3000 hr. The 245°C group displays an initial step decrease, similar to that of the biased devices, but followed by an almost flat profile. One of these devices failed between 1388 hr and 2827 hr. It is the only unbiased device that has failed so far. The transconductance of the small (N = 4) 200°C group is increasing slowly, but, judging by the higher temperature groups, it is too early to expect a true trend.

The results of the gate bias voltage V_{GB} and pinchoff voltage V_p are shown in Figures 26 and 27, respectively. $|V_{GB}|$ is relatively unchanged

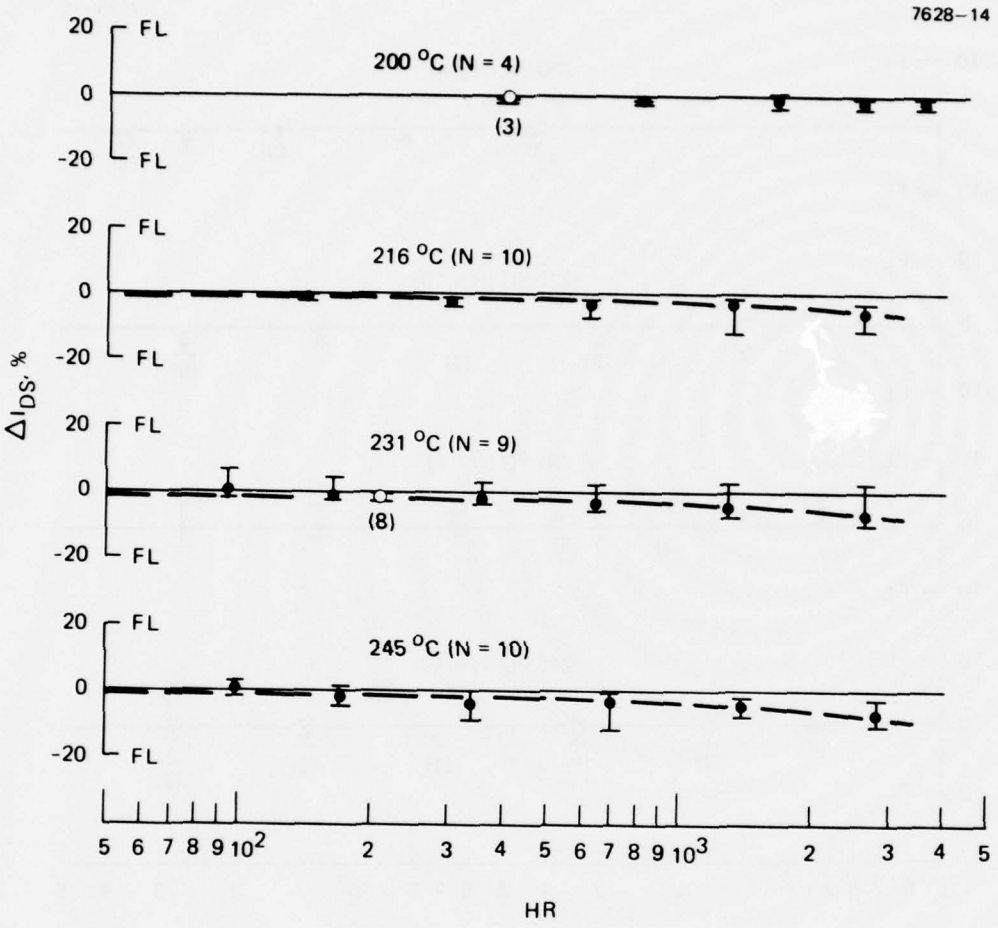


Figure 23. Change in I_{DS} of unbiased Type-A2 FETs.

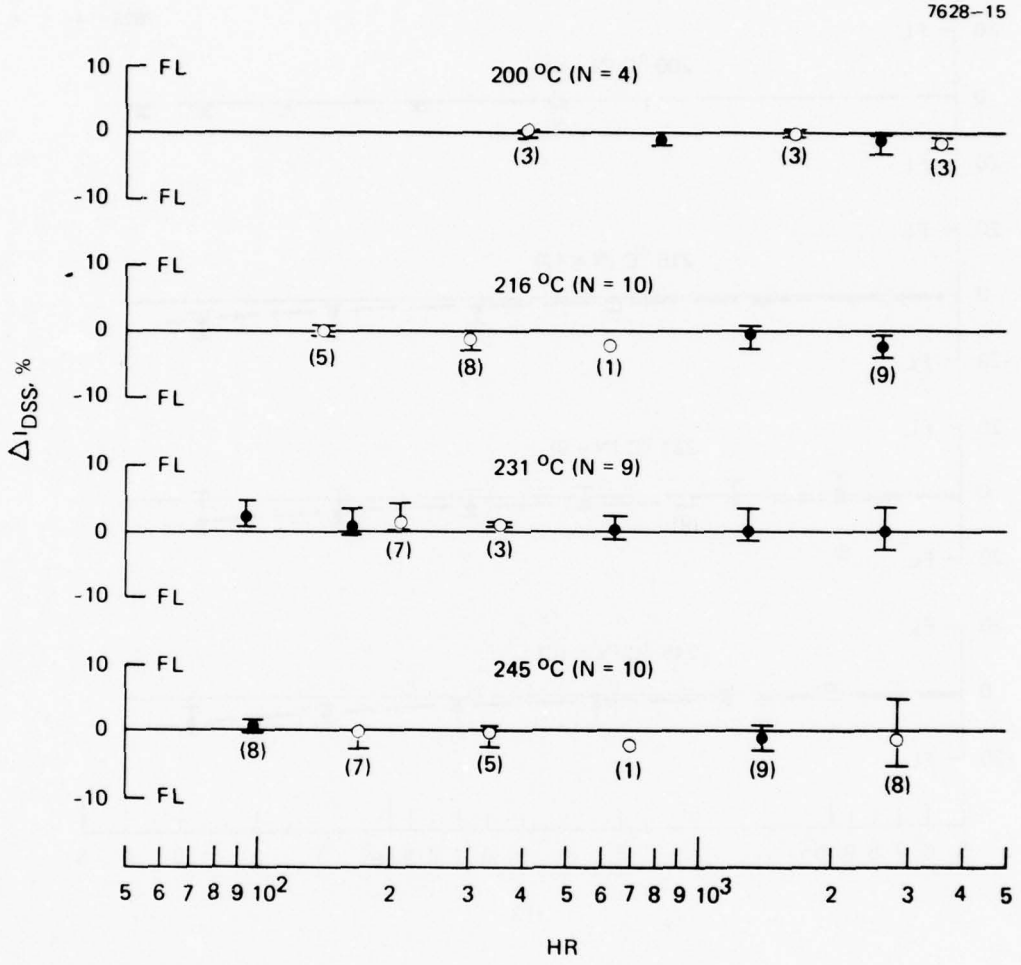


Figure 24. Change in I_{DSS} of unbiased Type-A2 FETs.

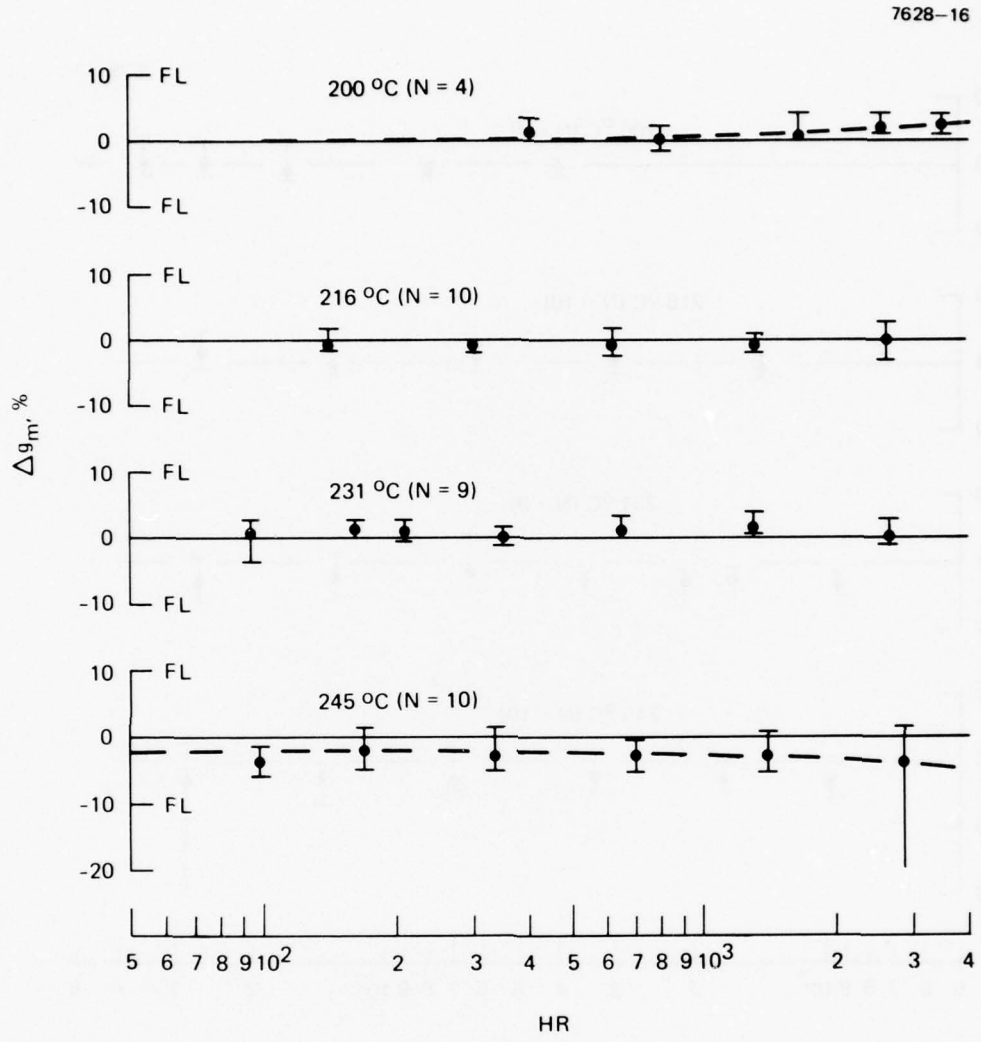


Figure 25. Change in g_m of unbiased Type-A2 FETs.

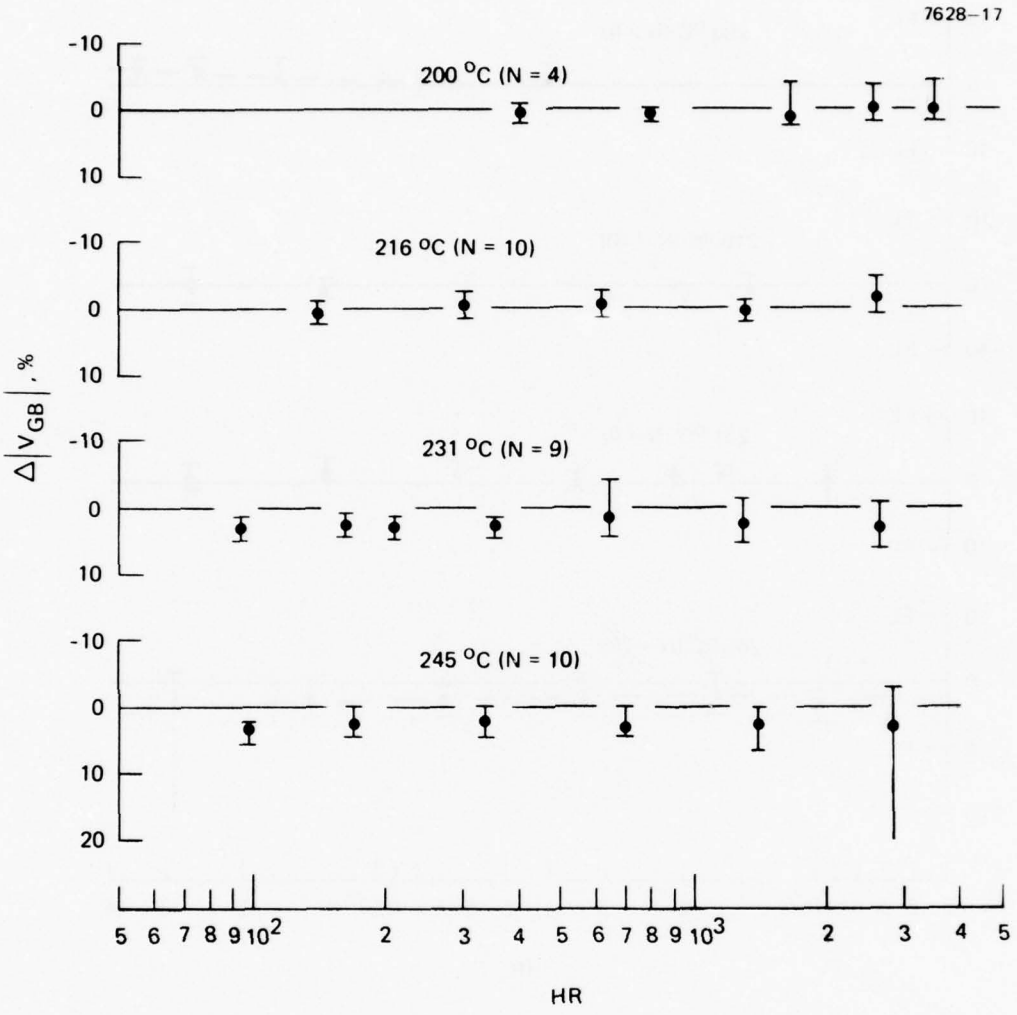


Figure 26. Change in $|V_{GB}|$ of unbiased Type-A2 FETs.

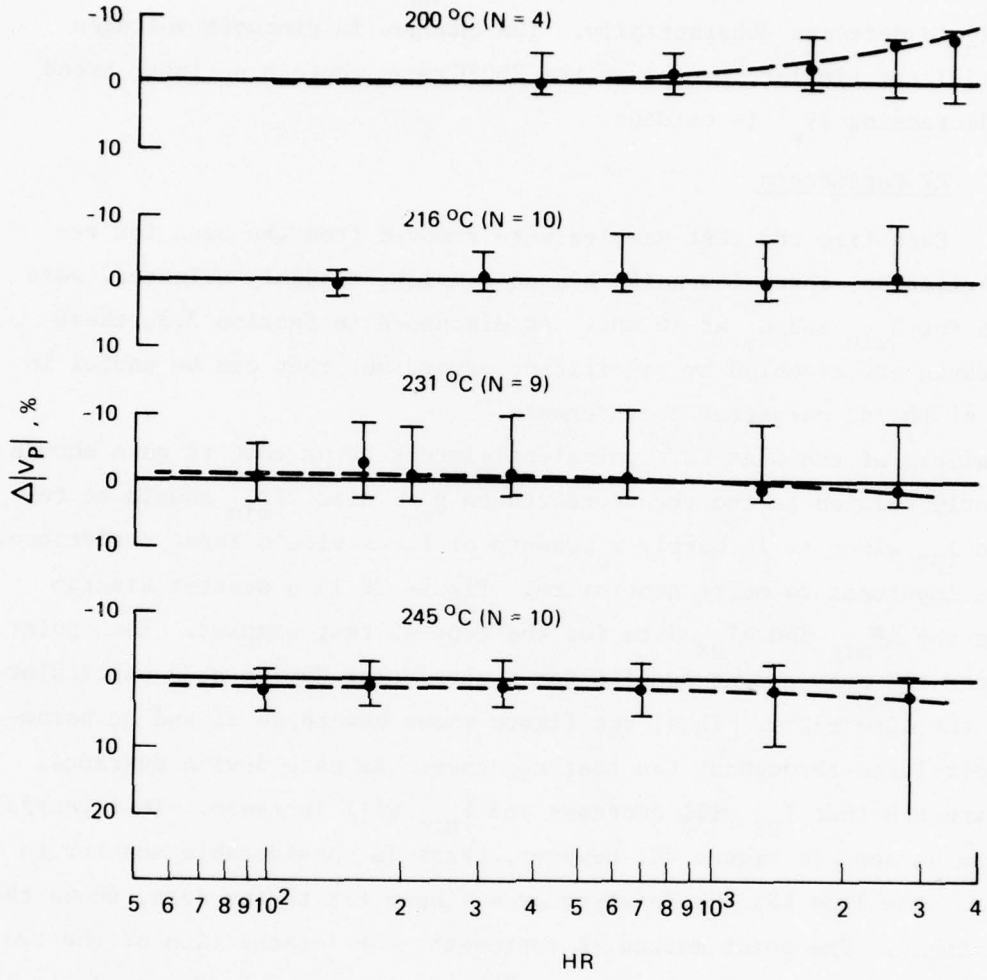


Figure 27. Change in $|V_p|$ of unbiased Type-A2 FETs.

for the 200°C and 216°C unbiased groups, whereas both the 231°C and 245°C groups show an initial step increase in $|V_{GB}|$ of about 2.6%, followed by a relatively flat profile. The one device in the 245°C group that failed did so because of a dramatically increased $|V_{GB}|$ (86%), which in turn caused g_m to decrease substantially. The changes in pinchoff voltages (Figure 27) are similar, except in the 200°C case, where a definite trend toward decreasing $|V_p|$ is evident.

b. RF Parameters

Each time the test samples were removed from the oven for re-characterization, three low-noise-biased samples, randomly selected, were measured for F_{min} and G_a at 10 GHz. As discussed in Section 2.B, these measurements are troubled by significant error, but they can be useful in support of the dc parameter measurements.

Analysis of the GaAs FET equivalent circuit shows that rf gain should be directly related to the transconductance g_m. Also, F_{min} should be related to I_{DS} since it is partly a measure of the device's input resistance, which is important to noise generation. Figure 28 is a scatter diagram relating the ΔF_{min} and ΔI_{DS} data for the Type-A2 test samples. Each point represents the measurement results for a particular device at a particular time in the life tests. Thus, the figure shows how these rf and dc parameters correlated throughout the test sequence. As each device degrades, it is expected that I_{DS} will decrease and F_{min} will increase. This general trend can be seen in Figure 28; however, there is considerable scatter to the data. The line LF, the least-squares linear fit to the data, shows the average trend. The point marked FL represents the intersection of the two assigned failure limits (i.e., ΔI_{DS} = -20% and ΔF_{min} = 0.5 dB; see Table 8). LF passes close to FL, and its slope is, in fact, close to the value expected. It does not pass through the origin, however. An ellipse is shown in the figure to indicate the expected 1-σ measurement error as given in Tables 2 and 3. Thus, the rf data appears to partially support the assigned dc failure limit for ΔI_{DS}. This agrees with a finding we made on an earlier program.[6]

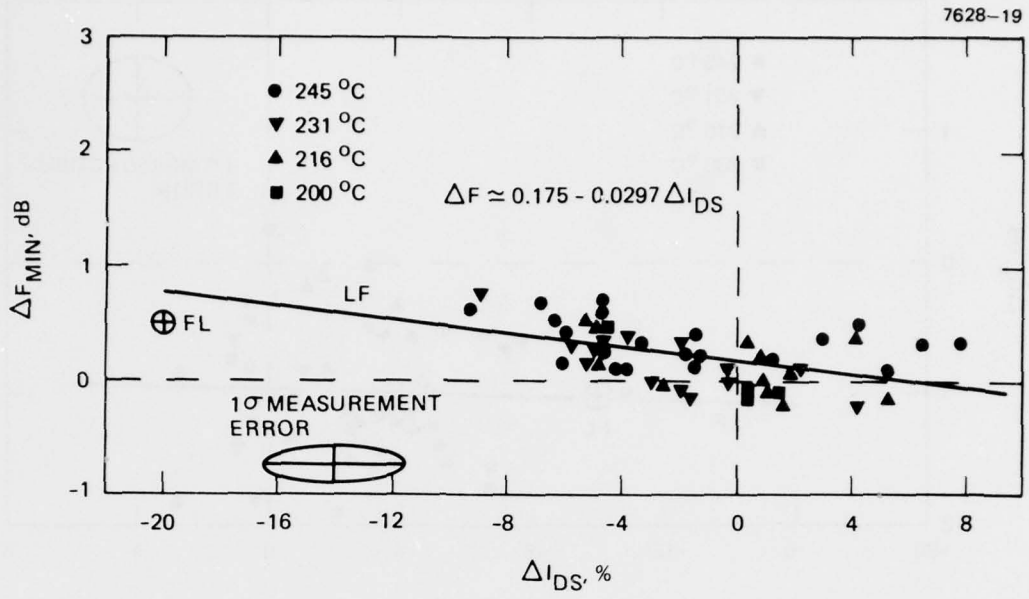


Figure 28. ΔF_{min} versus ΔI_{DS} for the Type-A2 FETs.

The scatter diagram relating ΔG_a and Δg_m (Figure 29) shows no such agreement, however. There is so much scatter in the data that almost no trend exists. Part of the ambiguity in this relationship is probably due to the fact that during rf measurement the devices were tuned for minimum F_{min}, not maximum G_a. Other possible explanations include: (1) considerable measurement error existed in measuring one or both of these parameters or (2) the mode of failure of these Type-A2 FETs (gate failure) led to erratic parameter variations. Some investigators of GaAs FETs have found that the dc and rf parameters do not correlate well and have chosen to ignore the dc parameters and rely strictly on rf measurements.[7] This is not entirely satisfactory if one is interested in determining the causes of failure.

c. Failure Rates

The failure distribution for the 245°C low-noise-biased FETs is plotted in Figure 30. The failures appear to follow the usual log-normal distribution. Most of the failures are due to decreasing g_m, caused

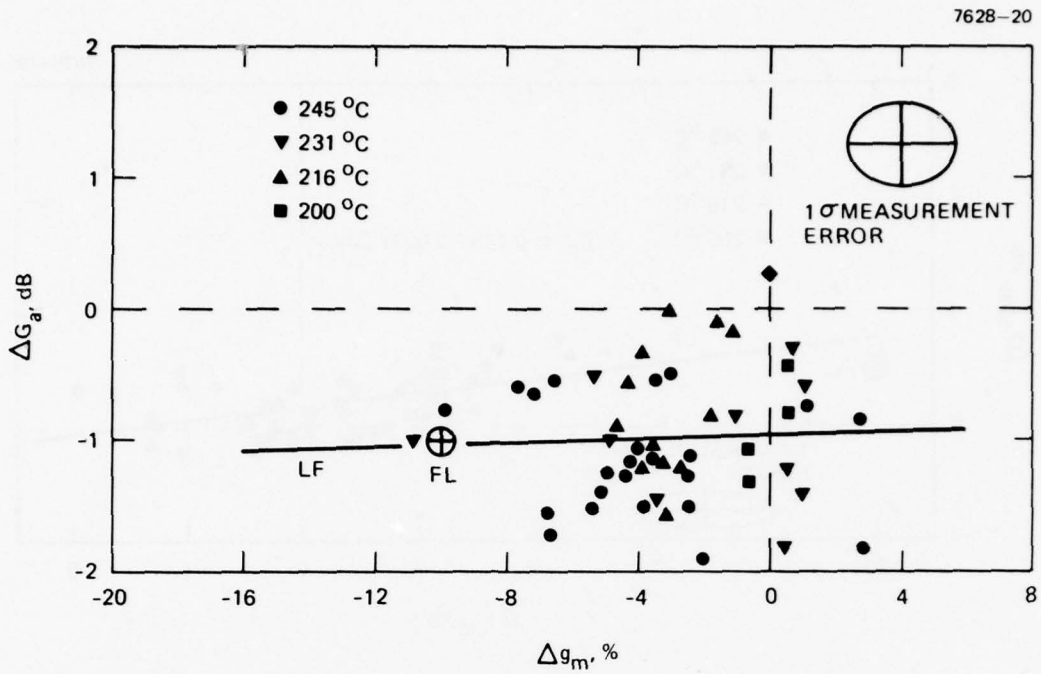


Figure 29. ΔG_a versus Δg_m for the Type-A2 FETs.

primarily by deteriorating gate characteristics. Nine of the ten samples had failed by 2827 hr. Two methods were used to estimate the time of failure. For catastropic gate failure, the time of failure can be determined from the oven log book by the time at which step changes were required in the applied bias. For a more gradual failure, the failure time can be estimated by assuming a linear rate of parameter degradation during the stress cycle.

The times at which the ovens were turned off and the devices recharacterized are marked by arrows along the right-hand axis (time) of Figure 30. There was also a year-end shutdown (S) of HRL facilities that required turning off the ovens. Several device failures occurred within one or two days of the returns of the oven to stress temperature. Although precautions are always taken to prevent sudden changes in bias levels, especially during oven start-up and shut-down procedures, the devices may be sensitive even to gradual stress changes once their gates have degraded beyond a certain point.

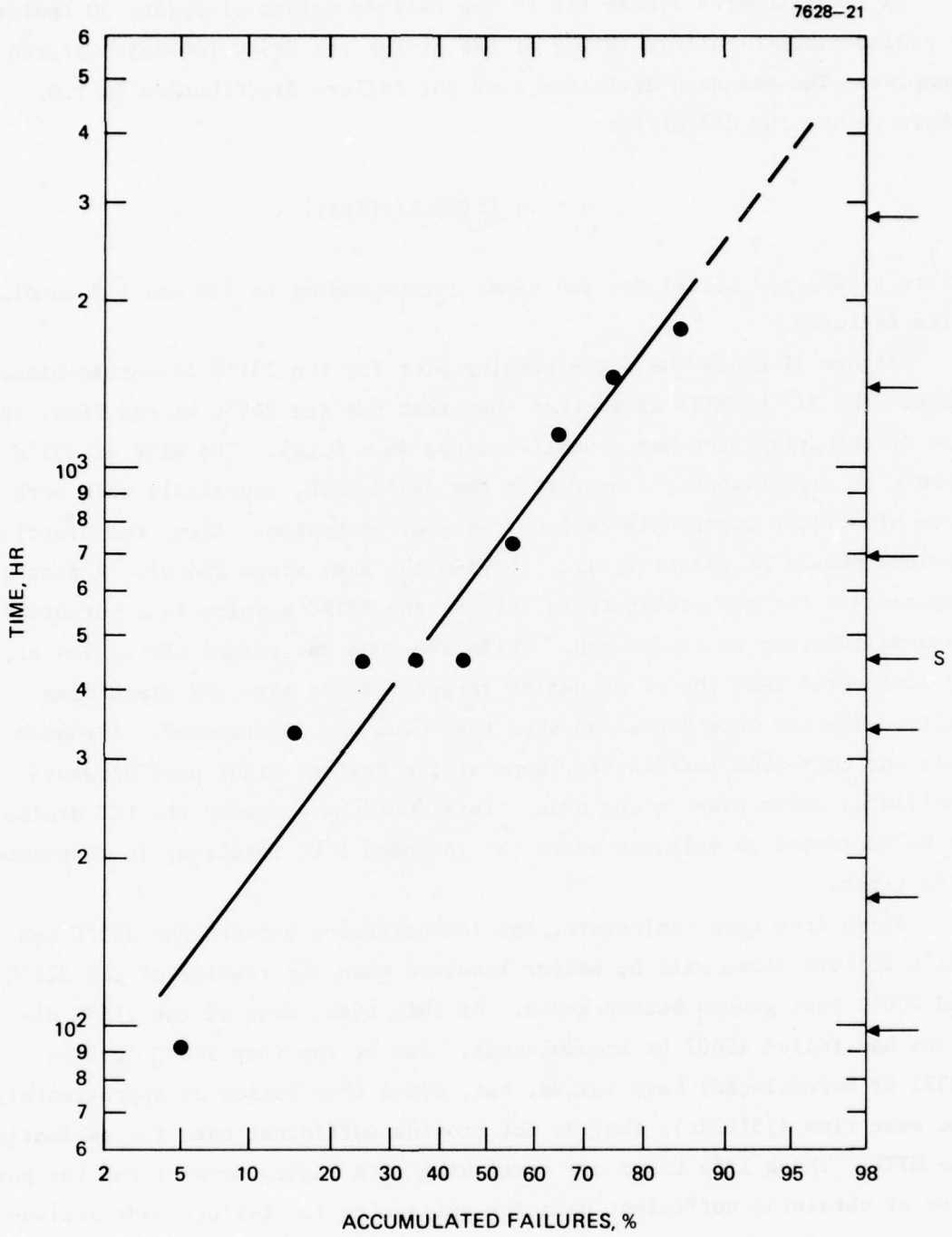


Figure 30. Failure distribution for the 245°C low-noise-biased Type-A2 FETs.

A least-squares linear fit to the failure points of Figure 30 indicates a median-time-to-failure (MTTF) of 686 hr for the 245°C low-noise-biased samples. The standard deviation s of the failure distribution is 1.0, where we use the definition

$$s = \ln [t(50\%)/t(16\%)] ,$$

where t(50%) and t(16%) are the times corresponding to 50% and 16% cumulative failures.

Figure 31 shows the corresponding plot for the 231°C low-noise-biased FETs. The 373 hr MTTF is shorter than that for the 245°C biased FETs, and the distribution line has a smaller slope (s = 0.44). The MTTF at 231°C should be significantly longer than the 245°C MTTF, especially when both sets of devices apparently fail by the same mechanism. Also, the distributions should be parallel (i.e., having the same slope and s). A possible explanation for the premature failure of the 231°C samples is a potential oven malfunction we discovered. While the oven was turned off at 354 hr, we discovered that the rf grounding straps for the gate and drain bias filters had not been installed when that oven was constructed. Although this was corrected immediately, some of the devices might have already oscillated under bias in the oven. This could have caused the FET drains to be subjected to voltages above the intended 5 V, resulting in shortened life times.

Aside from this conjecture, the inconsistency between the 245°C and 231°C failure rates will be better resolved when the results of the 216°C and 200°C test groups become known. At this time, none of the 216°C devices has failed (2607 hr accumulated). Two of the four 200°C devices (3531 hr accumulated) have failed, but, since they failed at approximately the same time (1319 hr), they do not provide sufficient data for estimating the MTTF. These life tests are continuing with Hughes support for the purpose of obtaining sufficient data for estimating the failure mode activation energy E_a and the MTTF as a function of temperature.

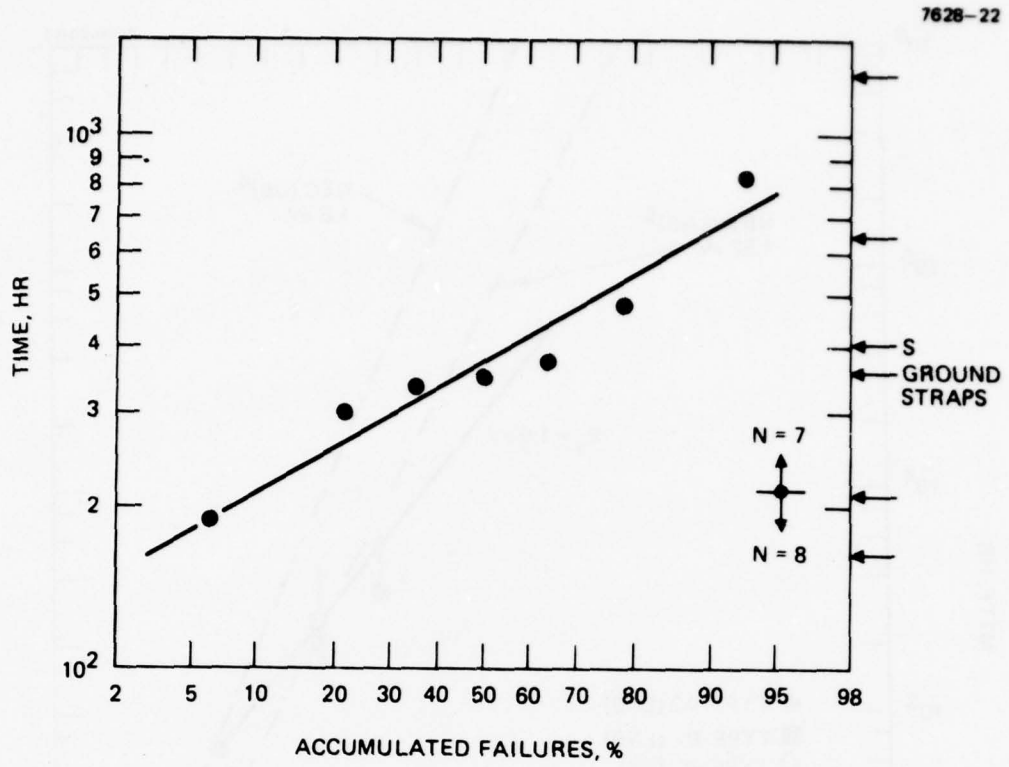


Figure 31. Failure distribution for the 231°C low-noise-biased Type-A2 FETs.

The MTTFs determined for the 245°C and 231°C low-noise-biased test groups are shown in Figure 32. The present status of the 216°C and 200°C groups is also shown; vertical arrows are attached to these points to indicate that their MTTFs are somewhere above the already accumulated stress times. A preliminary MTTF curve is shown for these biased Type-A2 FETs; it is derived from the 245°C point and the present location of the 216°C point. The corresponding activation energy E_a is 1.0 eV. This agrees with Irvin and Loya,[7] who describe several GaAs FET failure mechanisms with activation energies near 1 eV. Our results will be updated as additional data is accumulated from the continuing life tests. Also shown in Figure 32 for comparison are previously published results for unbiased NEC GaAs FETs[4] and for low-noise-biased HRL GaAs FETs.[6]

There is insufficient data to present on the failure of the unbiased Type-A2 FETs. Only 1 of the 245°C group has failed.

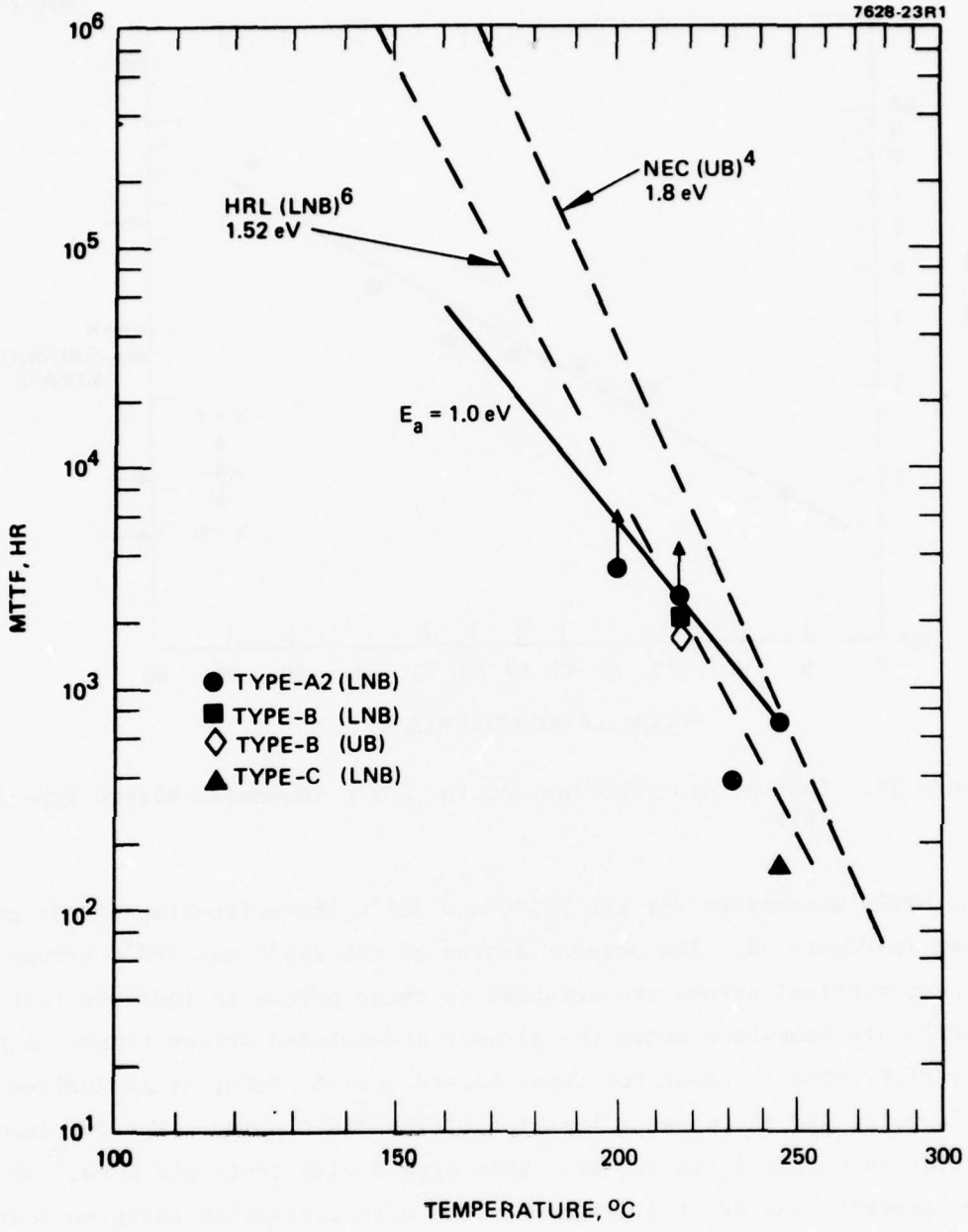


Figure 32.
MTTF as a function of ambient temperature for low-noise-biased (LNB) and unbiased (UB) GaAs FETs. Published NEC and HRL results shown for comparison.

d. Failure Analysis

The low-noise-biased Type-A2 FETs failed when their transconductances decreased below the assigned limit ($\Delta g_m < 10\%$). This was caused by gate deterioration, the result of which was that continually increasing gate bias was required to obtain low-noise-bias or pinchoff conditions. Examination by optical microscopy showed that all of the biased FETs were developing flaws along the gate stripe. These appeared initially as one or two individual spots along the gate; as time progressed, the number and extent of these flaws increased. With optical microscopy, even at 1000X, we were unable to determine if these flaws were due to bumps developing on the aluminum gate stripe, separation of the SiO_2 layer from the gate, or flaws in the SiO_2 layer itself. A second change was also observed with the optical microscope: the exposed Ohmic-contact layer was developing pits or voids. These tended to concentrate along the edge of the Cr/Pd/Au overlayer, but were not limited to that area. These are possibly related to the increase in contact resistance (decrease in I_{DS}).

The degradations were examined by SEM after the SiO_2 glassivation layer had been removed by plasma etching. The gate flaws were determined to be restructuring and migration of the gate aluminum. Figure 33(a) shows an SEM view of a portion of the gate line containing a restructured section $\sim$ 5 μm long; other small spots can be seen. Figure 33(b) shows an intersection of the gate stripe and one of its bond pad leads. Here, in addition to the restructuring along the gate stripe, a hillock is growing at the intersection, a relatively frequent occurrence. They probably are caused by electromigration and occur at intersections because these are areas of maximum gate leakage current density. The gate restructuring to the left of the intersection is believed to have developed an open circuit, thereby electrically isolating the left wing of the gate. This belief is supported by the I-V curves of this device (Figure 34), which show partial gate failure and the ability to pinch off only three-fourths of the source drain current. Figure 33 also shows several of the voids which have formed in the exposed Ohmic contact layer. Finally, Figure 35 shows three pits in the GaAs between the source and gate. These appear to be the result of a gate-source breakdown.

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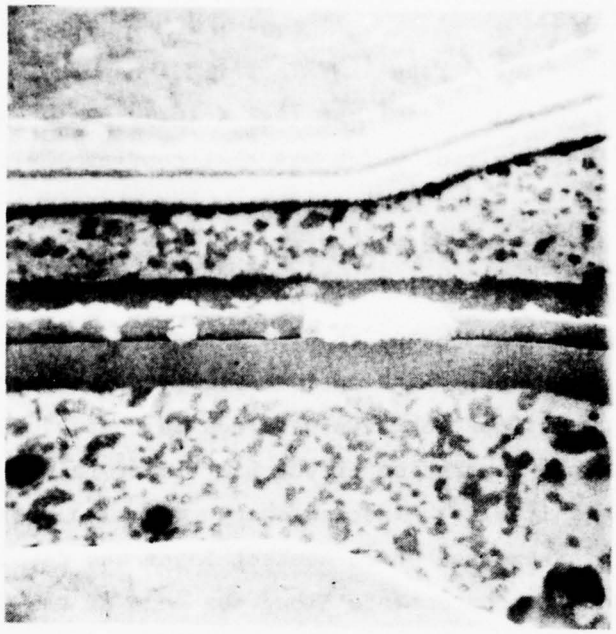
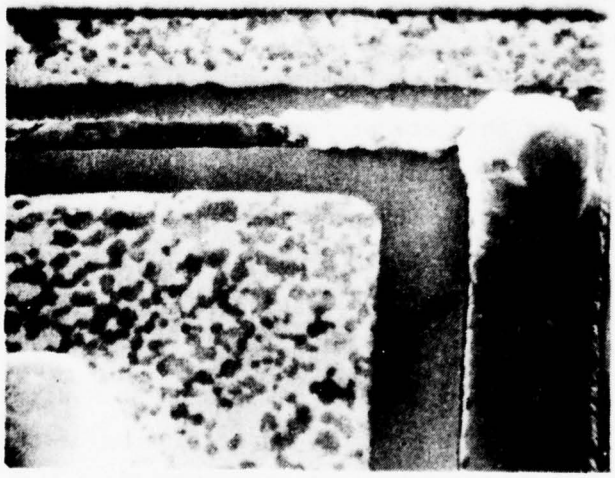


(a) SECTION OF GATE STRIPE (6100 x)



(b) INTERSECTION OF GATE LEAD
AND GATE STRIPE (6000 x)

Figure 33. Restructuring and hillock formation on gate of Type-A2 FET.

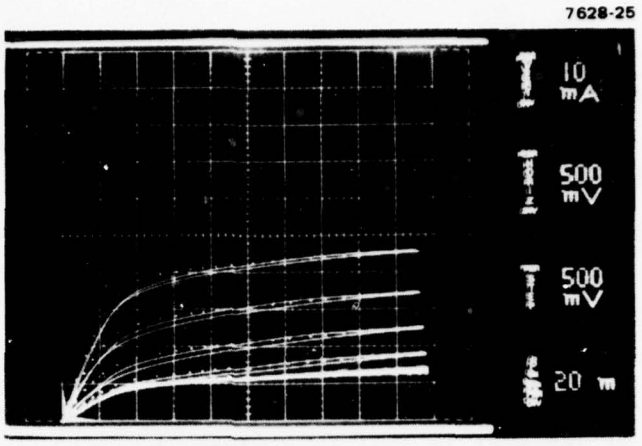


Figure 34. I-V curves of Type-A2 FET showing effect of gate failure.

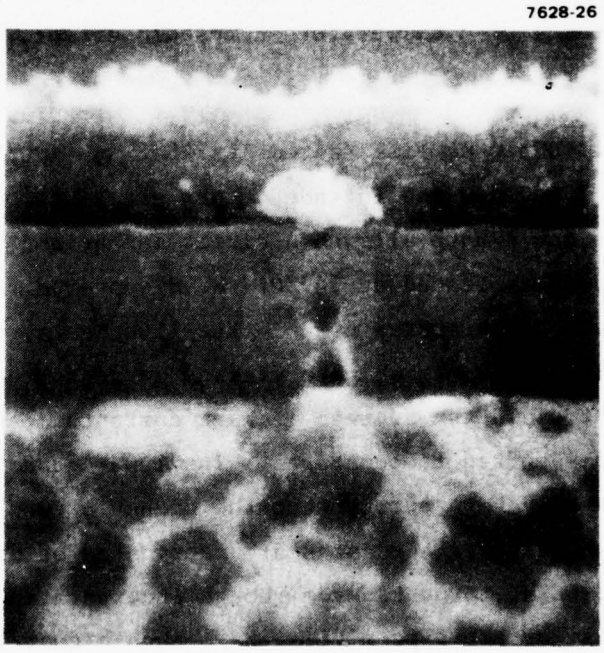


Figure 35. Source-gate region of Type-A2 GaAs FET showing evidence of gate-source breakdown (24,000x).

The unbiased Type-A2 FETs all exhibited void formation in the exposed Ohmic contact layer, but very few showed any signs of deterioration along the gate stripe. Thus, the gate deterioration mechanism is strongly dependent on electromigration. We also believe that the particular SiO_2 glassivation layer on these devices led to this failure mechanism. In all of our previous testing of nonglassivated aluminum gate FETs, this form of gate failure never occurred. In addition, the Type-B FETs, which also have aluminum gates and SiO_2 protection, did not exhibit any of these flaws (Section 3.C.2). Thus, it seems clear that the gate deterioration experienced is not inherent to this technology, but rather is the result of one or more faulty processing steps. Improving the fabrication procedure should significantly improve gate reliability.

Finally, one of the 245°C unbiased Type-A2 samples failed sometime after 1388 hr as a result of Au-Al plague formations (Section 3.B) on one of its gate bond pads and the adjacent section of gate. This mechanism rarely occurs at temperatures below 270°C, either because of a large activation energy or because of a temperature threshold effect.

2. Type-B Life Tests

The Type-B GaAs FETs were life tested at 216°C and 200°C. In the original test plan, 245°C was the intended upper stress temperature for these devices. This would have allowed a direct comparison with the Type-A2 and Type-C devices tested at 245°C. We discovered, however, that, at the elevated stress temperatures used in the life tests, the low-noise-biased Type-B FETs have much higher gate leakage currents than do the other two types. Figure 36 shows the average leakage currents measured with the several FET types at elevated temperatures. The Type-A and Type-C GaAs FETs have similar gate leakage currents at the higher stress temperatures, even though their Schottky-barrier gates are fabricated of different metal systems. The Type-B FETs, however, even though incorporating aluminum gates similar to those of the Type-A FETs, have much higher leakage currents at these temperatures. The reasons for this difference are not known; either material or processing differences could be the cause. To avoid

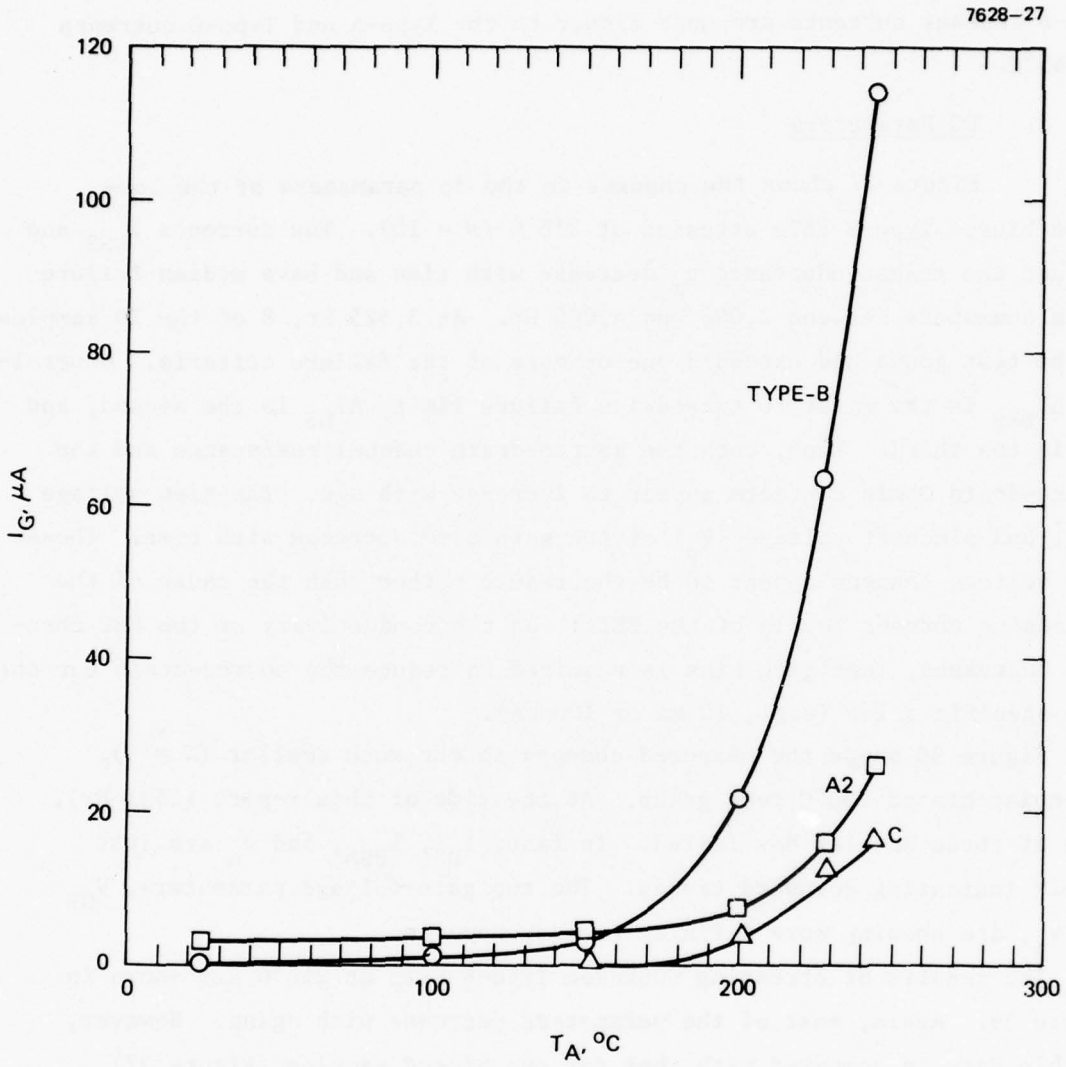


Figure 36. Gate leakage current as a function of ambient temperature for the 3 FET types: V_D = 5 V, I_D = 10 mA.

the possibility of introducing significantly greater electromigration effects into the accelerated aging of the Type-B devices, 216°C was selected to be the upper stress temperature. At this temperature, the Type-B leakage currents are much closer to the Type-A and Type-C currents at 245°C.

a. DC Parameters

Figure 37 shows the changes in the dc parameters of the low-noise-biased Type-B FETs stressed at 216°C (N = 10). The currents I_{DSS} and I_{DS} and the transconductance g_m decrease with time and have median failure times somewhere between 2,000 and 4,000 hr. At 3,625 hr, 8 of the 10 samples in the test group had exceeded one or more of the failure criteria. Generally, ΔI_{DSS} is the first to exceed its failure limit, ΔI_{DS} is the second, and Δg_m is the third. Thus, both the source-drain channel resistance and the source-drain Ohmic contacts appear to increase with age. The bias voltage $|V_{GB}|$ and pinchoff voltage $|V_p|$ of the gate also decrease with time. These gate voltage changes appear to be the result rather than the cause of the decreasing current levels of the FETs: as the conductivity of the FET channels decreases, less gate bias is required to reduce the source-drain current to a specific value (e.g., 10 mA or 100 μA).

Figure 38 shows the measured changes in the much smaller (N = 3), low-noise-biased 200°C test group. At the time of this report (3531 hr), none of these samples has failed. In fact, I_{DS}, I_{DSS}, and g_m are just barely indicating downward trends. The two gate-voltage parameters, V_{GB} and V_p, are showing more definite trends, however.

The results of stressing unbiased Type-B FETs at 216°C are shown in Figure 39. Again, most of the parameters decrease with aging. However, if this data is compared with that for the biased samples (Figure 37), several differences become apparent. The saturated drain current I_{DSS} of the unbiased devices decreases at about one-fourth the rate of the biased devices. Therefore, electrical stress plays an important part in this aging mechanism. In contrast, I_{DS}decreases two-thirds as rapidly for the

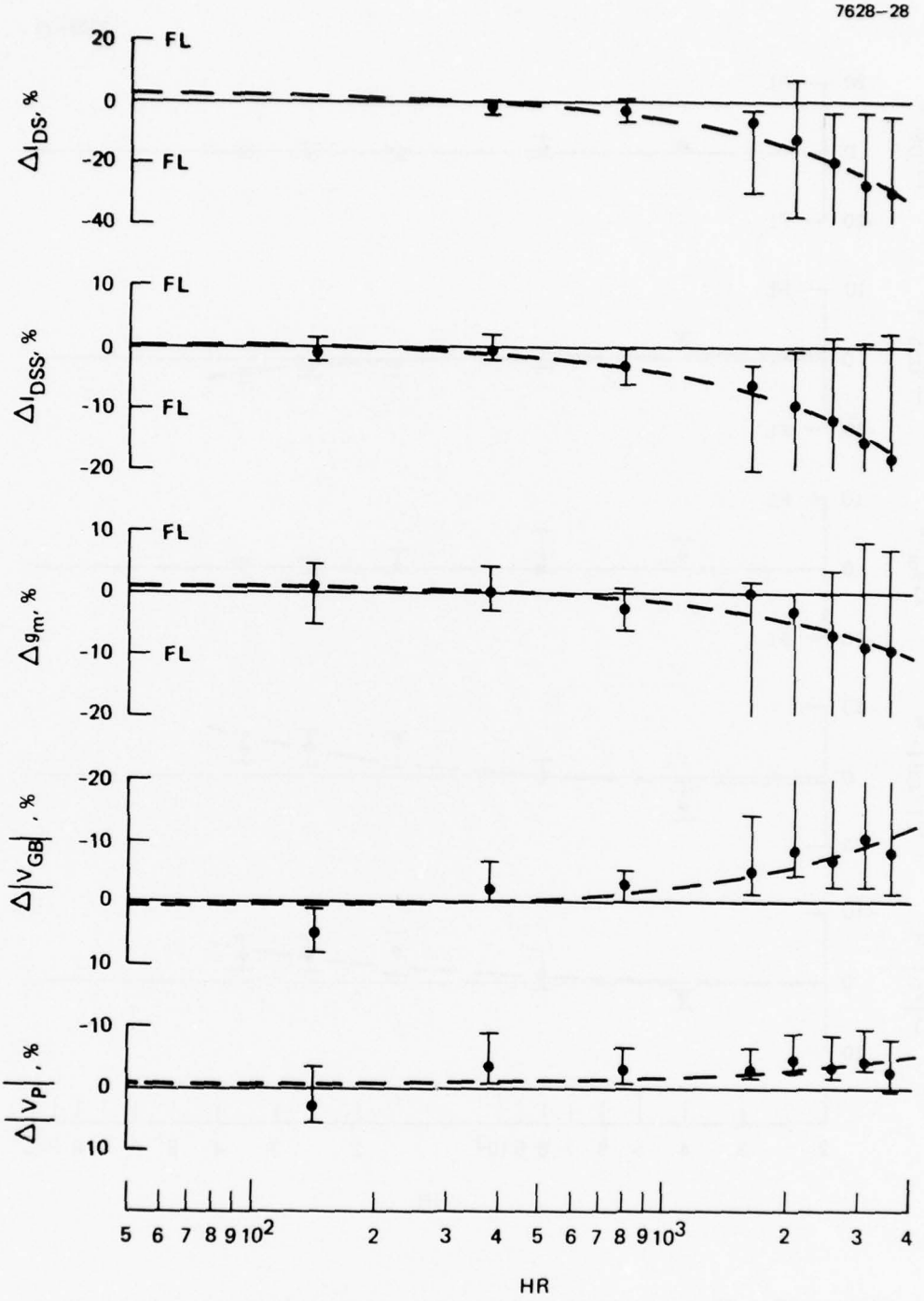


Figure 37. Changes in dc parameters of low-noise-baised Type-B FETs stressed at 216°C (N = 10).

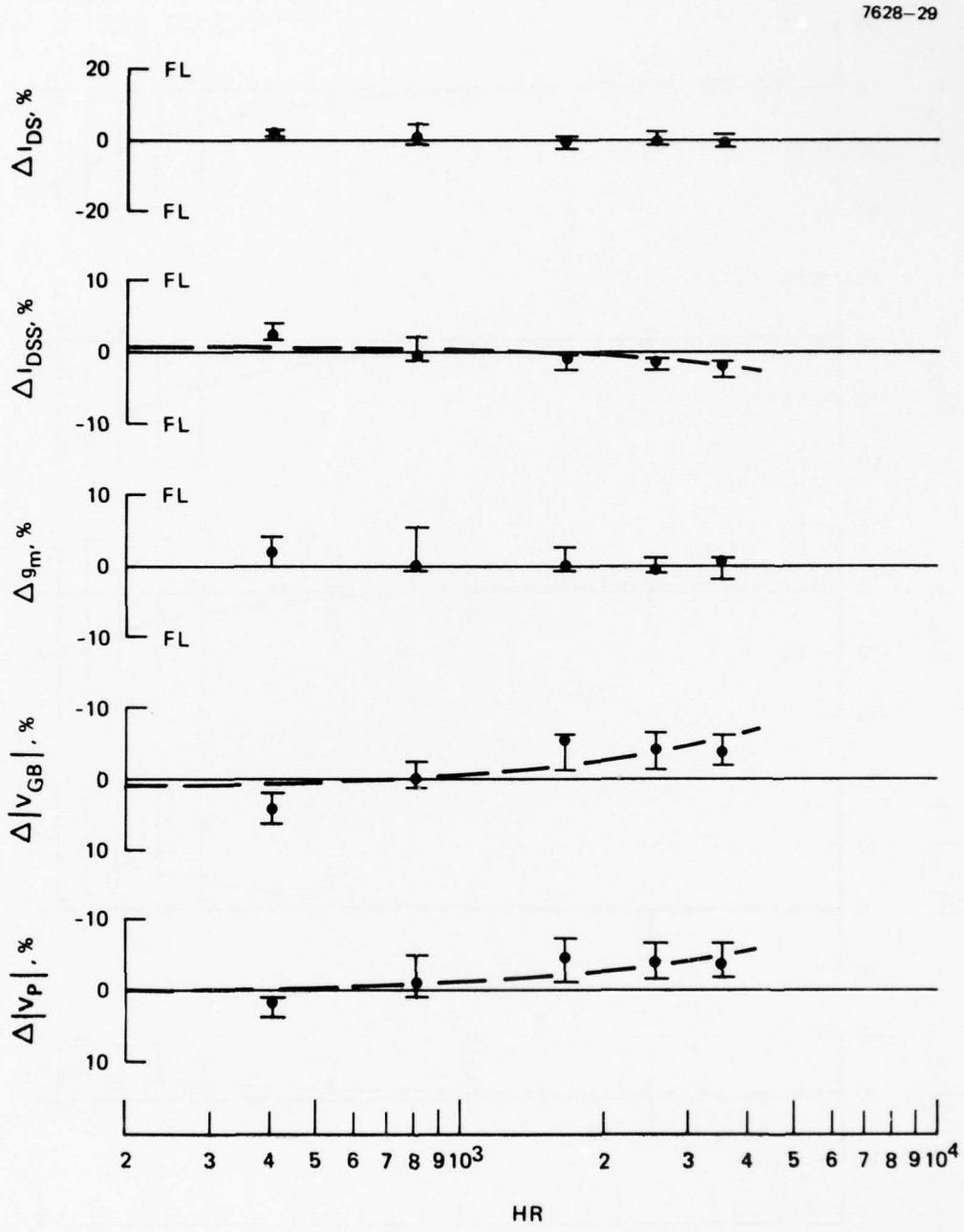


Figure 38. Changes in dc parameters of the low-noise-baised Type-B FETs stressed at 200°C (N = 3).

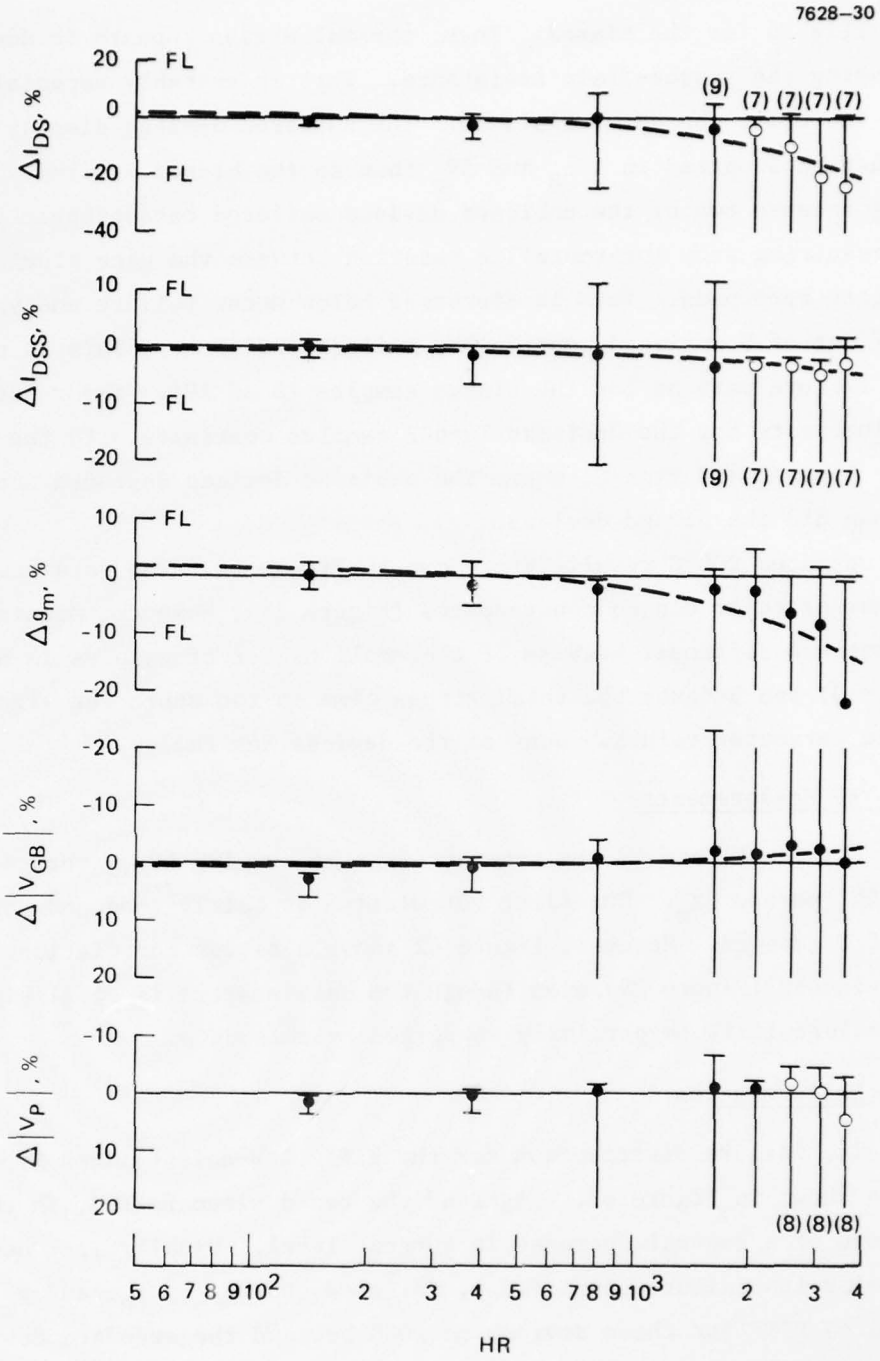


Figure 39. Changes in dc parameters of unbiased Type-B FETs stressed at 216°C (N = 10).

unbiased FETs as for the biased. Thus, thermal stress appears to dominate in increasing the source-drain resistance. This is probably especially true for the Ohmic contact resistance. The unbiased devices display a much larger data spread in ΔV_{GB} and ΔV_p than do the biased samples. This is partly because two of the unbiased devices suffered catastrophic gate failure resulting from intermetallic reaction between the gate aluminum and the gate bond pads. This is discussed below under failure analysis. In all, 7 out of 9 unbiased samples had failed by 3625 hr. This is roughly the same failure rate as for the biased samples (8 of 10). The relatively high failure rate for the unbiased Type-B samples contrasts with the results for Type-A2 and Type-C, where the unbiased devices degraded much more slowly than did the biased devices.

The unbiased 200°C results are shown in Figure 40. The data are similar to that of their biased counterparts (Figure 38); however, meaningful comparisons are difficult because of the small number of samples in each group (N = 3) and because the total stress time is too short for significant changes in parameter values. None of the devices has failed.

b. RF Measurements

Figures 41 and 42 are scatter diagrams showing ΔF_{min} versus ΔI_{DS} and ΔG_a versus Δg_m. The first correlation is fairly good and comparable to that of Figure 28. However, Figure 42 shows a better correlation than found previously (Figure 29) even though the data scatter is still significant. The Δg_m failure limit is partially supported by this data.

c. Failure Rates

The failure distribution for the 216°C low-noise-biased Type-B samples is shown in Figure 43. Eight of the ten devices failed, in each case because of a general decrease in current level. Usually I_{DSS} decreases below its failure limit first, followed shortly by I_{DS} and g_m. The estimated MTTF for these devices is 2000 hr, and the standard deviation is s = 0.49.

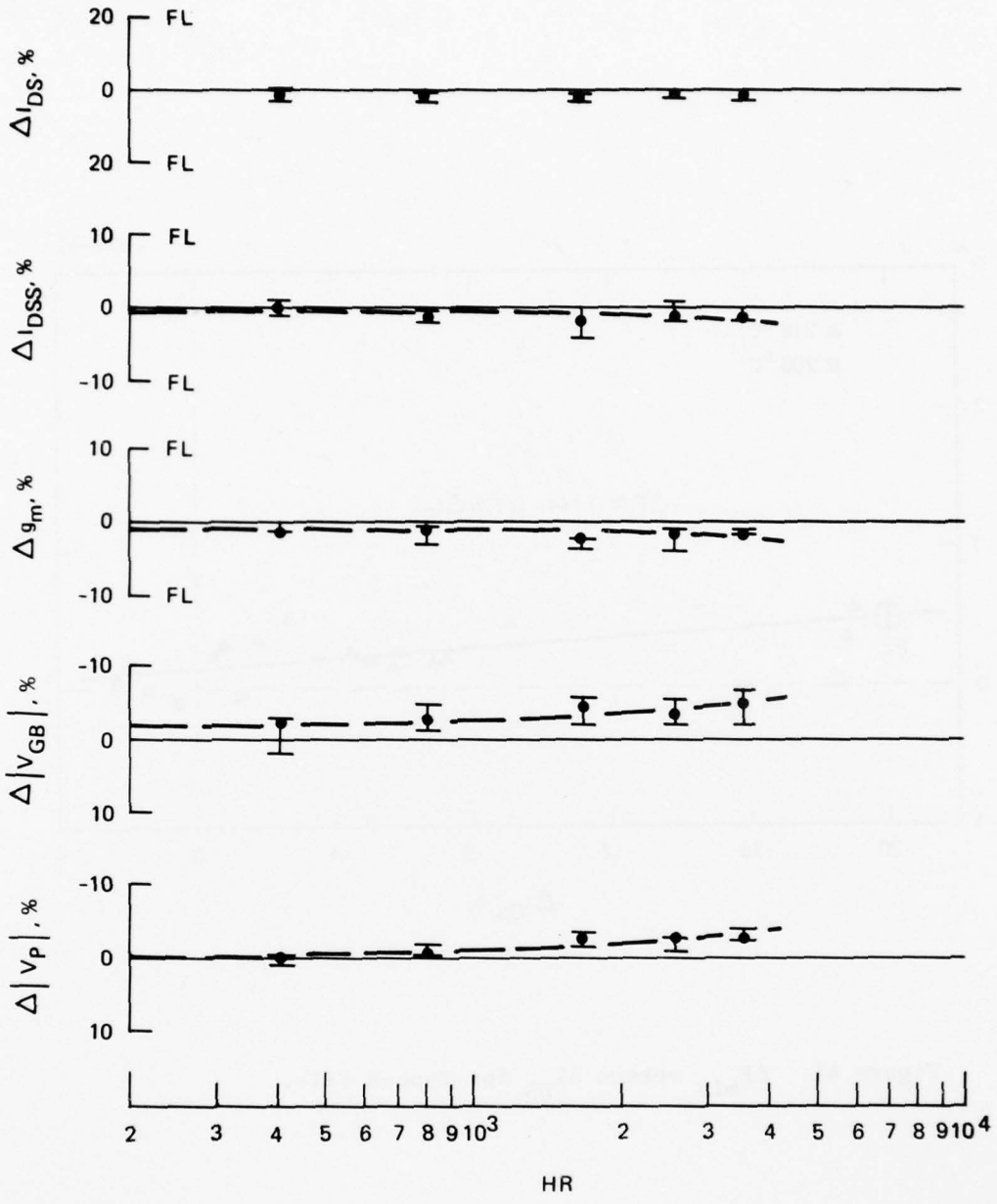


Figure 40. Changes in dc parameters of unbiased Type-B FETs stressed at 200°C (N = 3).

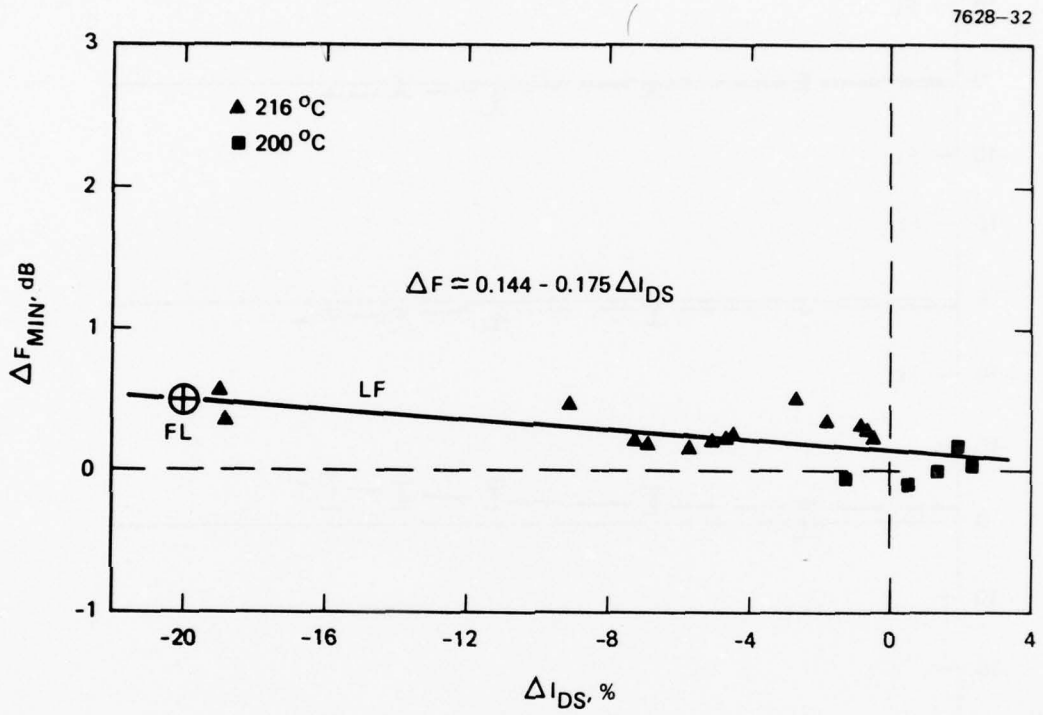


Figure 41. ΔF_{min} versus ΔI_{DS} for Type-B FETs.

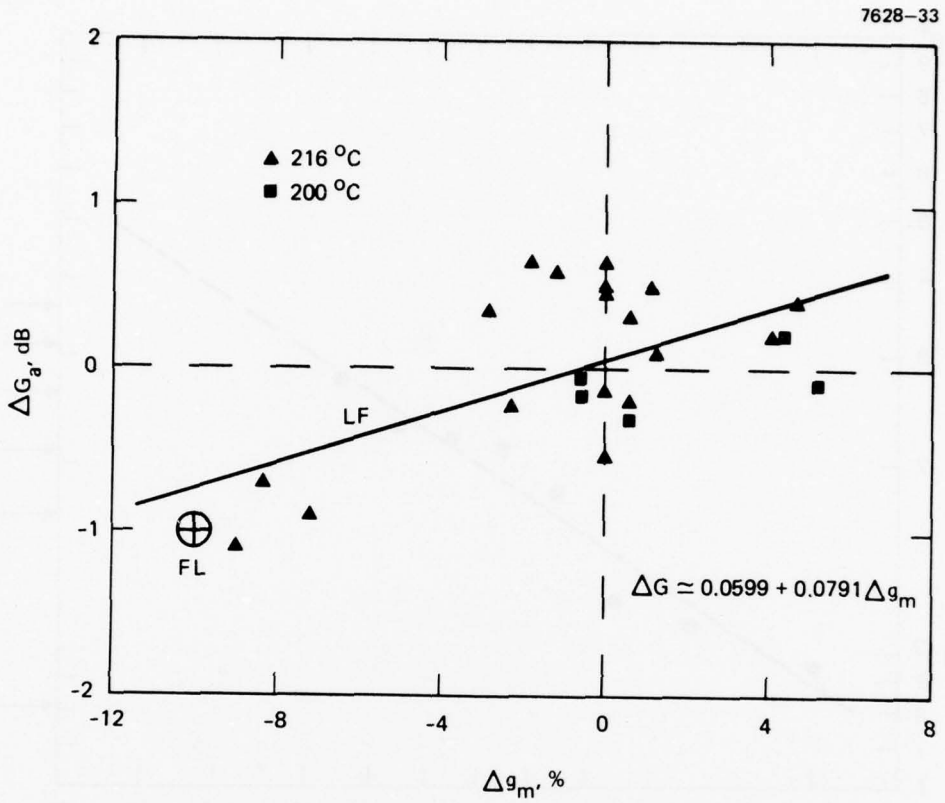


Figure 42. ΔG_a versus Δg_m for Type-B FETs.

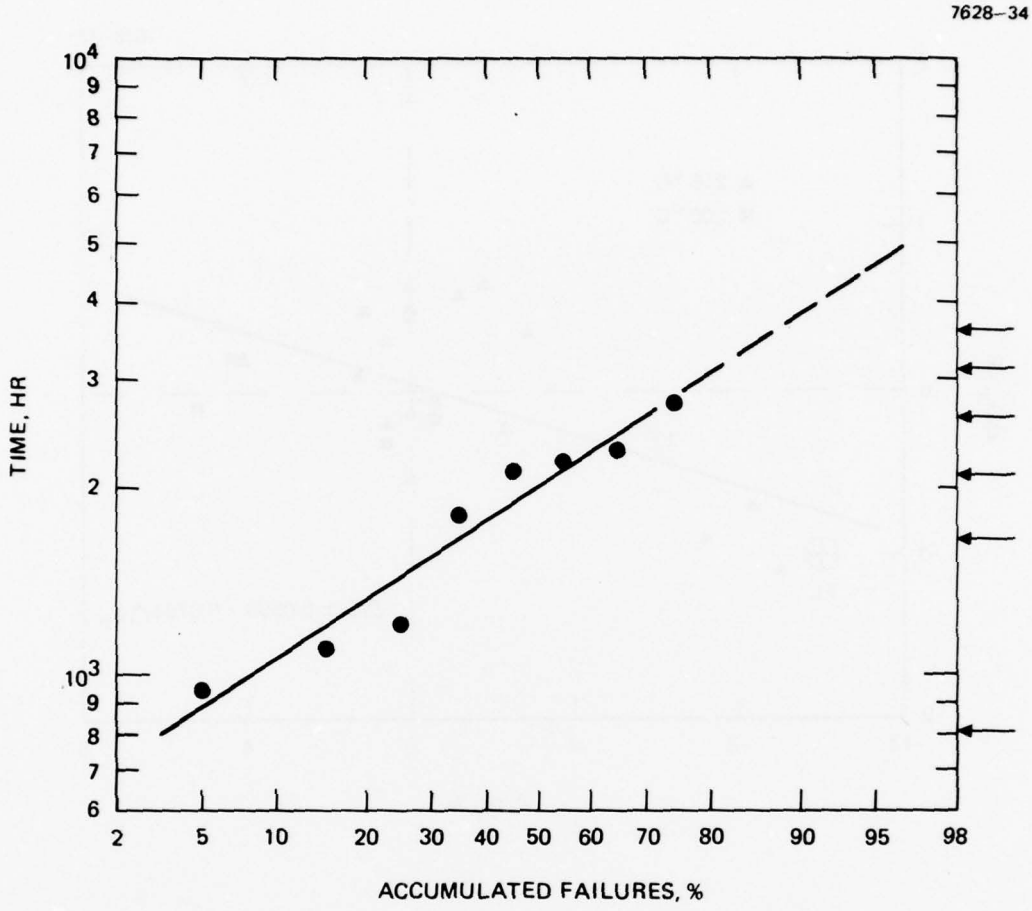


Figure 43. Failure distribution of low-noise-biased Type-B FETs stressed at 216°C.

Comparing these results with those for the Type-A2 devices stressed at 216°C, none of the latter had failed by 2607 hr. The Type-A2 FETs use Au-Ge/Ni Ohmic contacts; the Type-B FETs use Au-Ge/Pt contacts. During high-temperature storage tests, we had found that the resistance of Au-Ge/Pt contacts increased significantly faster than that of Au-Ge/Ni contacts.[6] This would cause a faster decrease in I_{DS} and, to a lesser extent, in I_{DSS}. The other major difference between these device types is that the Type-A2 active channel layer is formed by ion implantation, whereas in the Type-B FETs it is grown by vapor-phase epitaxy. It is unlikely that this process difference would inherently yield different failure rates.

An unusual feature of the Type-B tests is that the unbiased samples failed at a rate slightly faster than that of the biased samples. The unbiased failure distribution is shown in Figure 44. The MTTF estimate is 1816 hr (s = 1.1). Seven of nine samples have failed. Five of the failures were due to decreasing current, as with the biased devices, but the first and third failures were due to catastropic gate failure. The open circuits in the gates developed as a result of intermetallic reactions at the gate bond pad interface with the gate Al.

The Type-B 216°C MTTF points are plotted in Figure 32. None of the 200°C Type-B FETs has failed.

d. Failure Analysis

The large majority of the Type-B FETs failed because I_{DSS}, I_{DS}, and g_m decreased below their assigned failure limits. We believe that these decreases were probably caused by increasing source-drain Ohmic contact resistance and, perhaps, channel resistance. Similar findings had been reported previously, and analysis of our data supports this interpretation. Figure 45(a) shows the source-drain resistive components. R_S and R_D are the parasitic source and drain resistances, respectively, including the Ohmic contact resistances. R_{CH} is the resistance of the intrinsic channel, and X is a multiplier that accounts for the increase in resistance when gate bias is applied. The dc parameter I_{DS} is a measure of the total source-drain resistance. From the definition for I_{DS}, it follows that

$$R_S + XR_{CH} + R_D = 0.5/I_{DS}$$

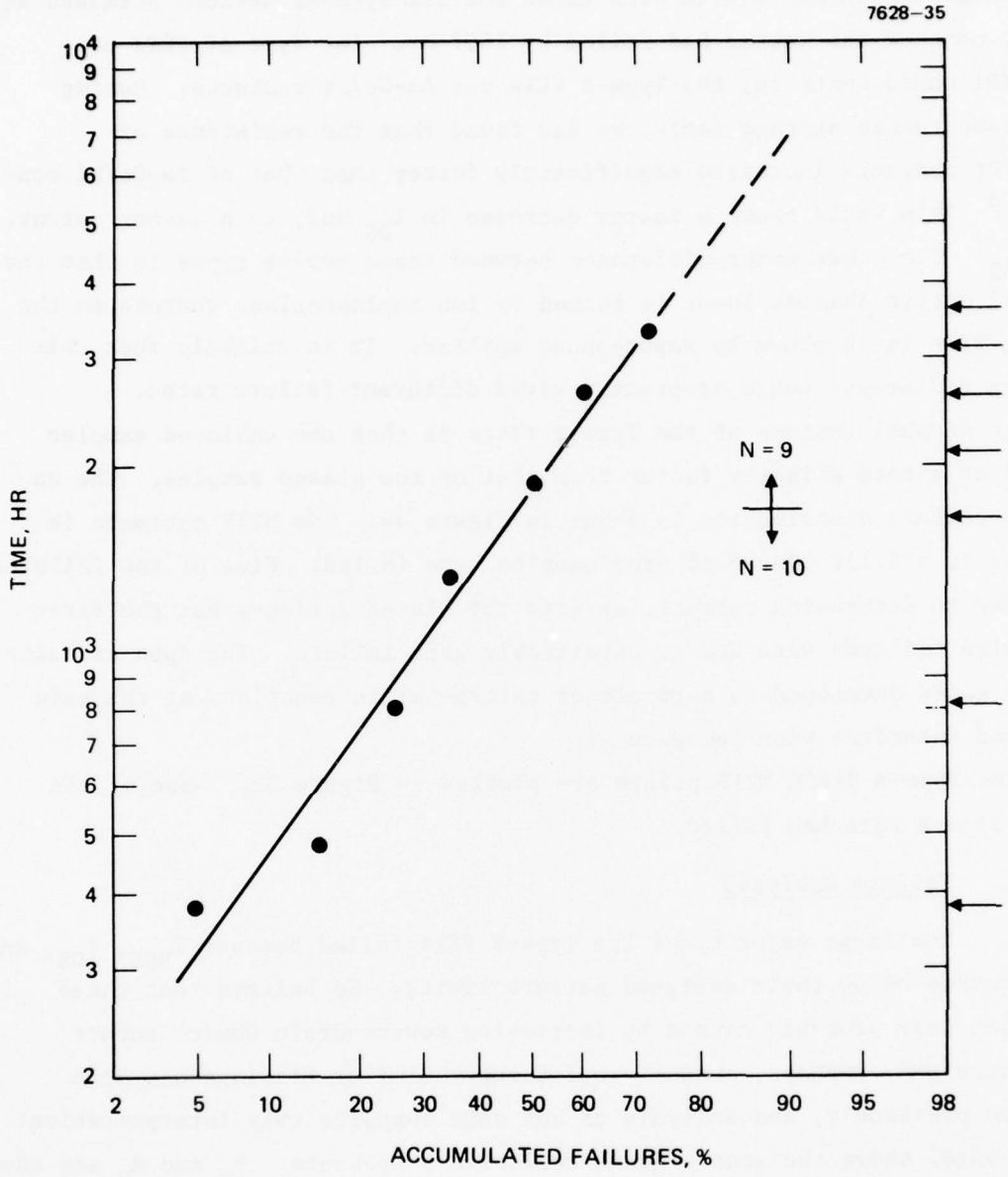


Figure 44. Failure distribution for unbiased Type-B FETs stressed at 216°C.

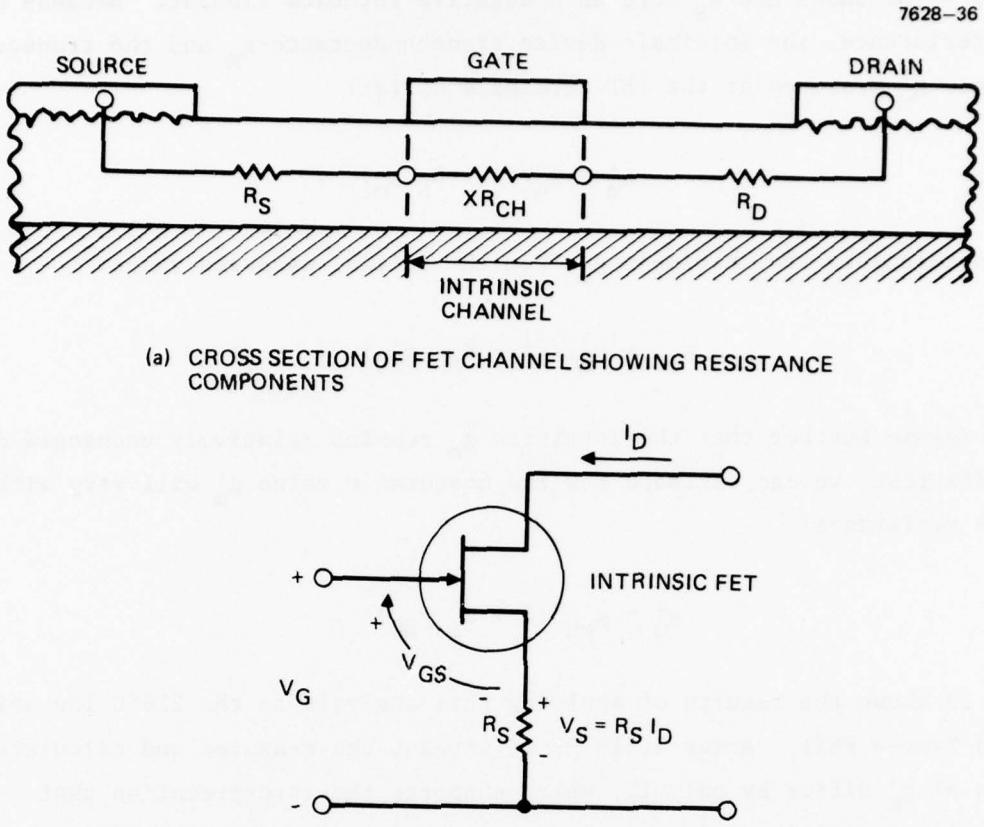


Figure 45. Parasitic source resistance and its negative feedback effect.

Initially, before the device has been life tested, we make the rough approximation that the three resistance components are equal. The initial resistances are then

$$R_{S0} = (XR_{CH})_0 = R_{D0} = 1/(6\ I_{DS})_0 \quad .$$

With stress, we assume that the source and drain resistances increase equally, primarily because of degrading Ohmic contacts, but that the intrinsic channel resistance remains relatively unchanged; thus, the new source resistance is

$$R_S = 0.5\ [(0.5/I_{DS}) - R_{CH_0}] \quad .$$

Figure 45(b) shows how R_S acts as a negative feedback element. Because of this resistance, the intrinsic device transconductance g_m and the transconductance g'_m measured at the FET terminals differ:

$$g'_m = g_m/(1 + R_S\ g_m) \quad .$$

We can calculate the intrinsic g_m from the initial measured value:

$$g_{m0} = g'_{m0}/(1 - R_{S0}\ g'_{m0}) \quad .$$

If we assume further that the intrinsic g_m remains relatively unchanged during the life test, we can estimate how the measurable value g'_m will vary with source resistance:

$$g'_m = g_{m0}/(1 + R_S\ g_{m0}) \quad .$$

Table 13 shows the results of applying this analysis to the 216°C low-noise-biased Type-B FETs. After 3,119 hr of stress, the measured and calculated values of g'_m differ by only 1%, which supports the interpretation that increasing parasitic resistance is the primary cause of Type-B FET failure. In addition, using the model of Figure 45(b), the expected decrease in saturated drain current I_{DSS} due to increasing R_S can be estimated. This result is also shown in Table 13. The model predicts a decrease of 2.7 mA. This is 40% of the actual measured decrease. The remainder is possibly due to changes in the intrinsic FET.

Examination of the tested samples shows little physical evidence of any changes. Some samples show a slight discoloration of the source-drain metalization surrounding one or more of the gold wire bonds; Figure 46 shows an FET with such discoloration around the drain bond and one side of the source. There are also very slight textural changes in these discolored areas. These changes are probably associated with degradation of the Ohmic contacts, especially since none of the gate bond pads exhibit similar discolorations; however, only one-half the samples are so marked.

Table 13. Estimated and Measured Parameters for Low-Noise-Biased Type-B FETs Stressed at 216°C.

Parameter	Value	
	Initial	After Stress
Stress time, hr	0	3,119
I_{DS}, mA	20.4	15.1
R_S, Ω	8.17	12.5
g_m, mmho	19.9	19.9
g'_m, mmho (measured)	17.1	15.7
(calculated)	--	15.9
I_{DSS}, mA (measured)	38.6	31.6
(calculated)	--	35.9
ΔI_{DSS}, mA (measured)	--	-7.0
(calculated)	--	-2.7

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The rates of degradation of I_{DS}, I_{DSS}, and g_m are much more rapid for the Type-B FETs stressed at 216°C than for the Type-A2 FETs at 216°C. Previously we compared Au-Ge/Ni Ohmic contacts with Au-Ge/Pt contacts and found that the latter degraded faster when stressed in high-temperature storage tests.[6] We did not consider those tests definitive because we had not gone through the process of optimizing the Au-Ge/Pt deposition and alloying steps. However, the present results appear to provide further evidence that Au-Ge/Ni is a more reliable Ohmic contact for GaAs than is Au-Ge/Pt.

Three of the unbiased 216°C samples failed because of gate failures caused by intermetallic formations; none of the biased samples have developed this symptom. Figure 47 shows two SEM views of one of these failed devices. Voids can be seen (Figure 47(a)) in the aluminum gate lead adjacent to where it necks down to go between the two halves of the source. These voids have grown to the extent that the gate is open circuited. There is an intermetallic formation in the area where the aluminum first goes under the Ti/Pt layers of

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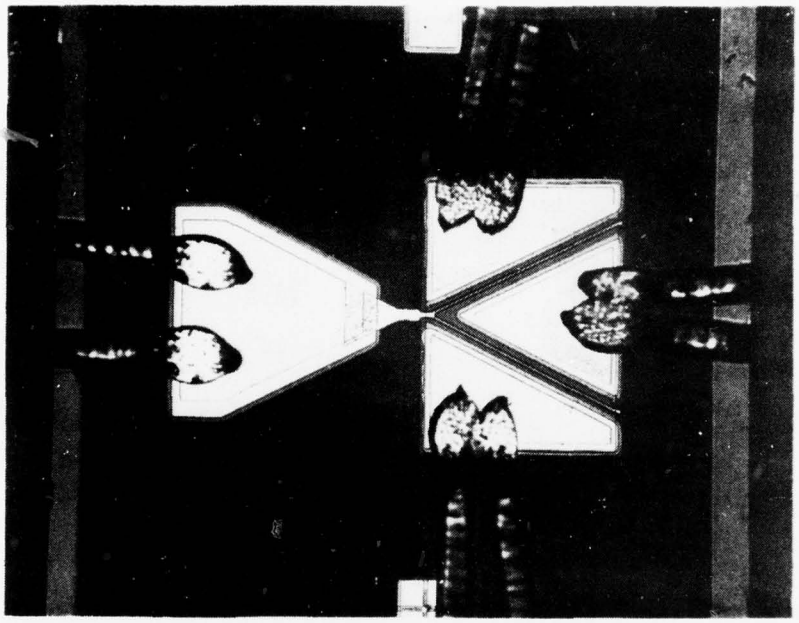
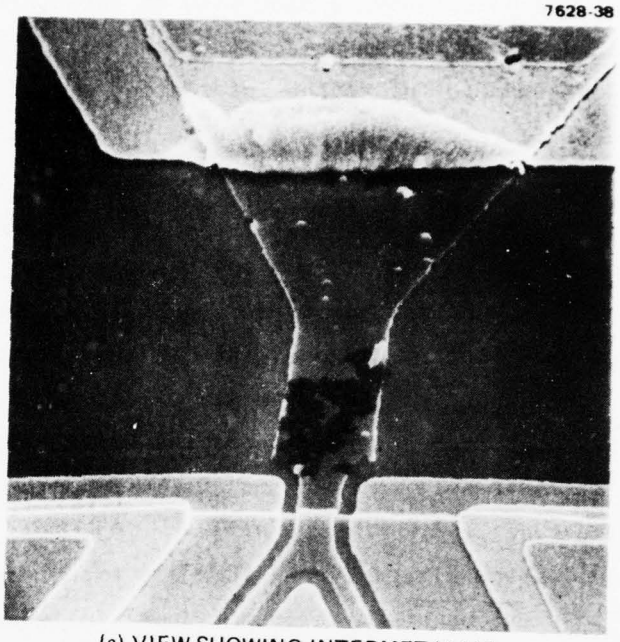
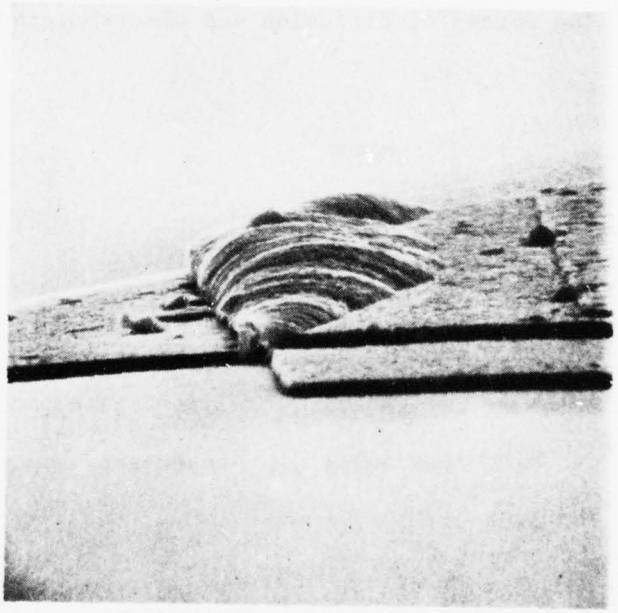


Figure 46. Photomicrograph of Type-B FET showing some discoloration of the source and drain metalization surrounding gold wire bonds.



(a) VIEW SHOWING INTERMETALLIC FORMATION ON BOND PAD AND VOIDS IN GATE LEAD (2370 x)



(b) SIDE VIEW OF GATE BOND PAD – Al INTERFACE (5600 x)

Figure 47. A Type-B FET which failed because of gate bond pad intermetallic formations.

the gate bond pad. Figure 47(b) shows a side view of this formation. There are also several small voids in the Al adjacent to the formation. All of the voids are the result of Al diffusing to the interaction site (Kirkendall effect). The intermetallic reaction is believed to be between the Al and Pt. A previous study of alternative gate-bond-pad metalizations determined that Al and Pt were highly reactive.[6] Normally, the Ti layer is expected to be an effective barrier between the Al and Pt, but any pinholes could allow this barrier to be breached. In addition, in these Type-B FETs, the edge of the Pt layer is not pulled back from the edge of the Ti; therefore, it is possible that some Pt overlaps the Ti and contacts the Al. Also, as seen in Figure 48, some of these FETs have poor step coverage where the Ti/Pt steps down from the Al to the GaAs surface; the resulting break in the Ti layer could allow Pt to contact the Al from the side.

The fact that none of the biased Type-B FETs has experienced this gate failure runs counter to previous observations of Au-Al failures by us and by Irvin and Loya.[7] Biased devices normally fail sooner than unbiased ones, and it is not expected that Pt-Al failures should differ. In fact, Irvin and Loya suggest that the opposing forces of diffusion and electromigration are what

Figure 48.
Type-B gate pad showing Ti/Pt overlay of Al and poor step coverage.

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cause the Al voids to appear, as they often do, where the Al lead necks down. It is possible, of course, that all of the devices that were capable of intermetallic failure (i.e., 3 of 20) were placed in the unbiased group by chance.

3. Type-C Life Tests

The Type-C GaAs FETs were constant-stress tested at 245°C and 200°C. The low-noise-biased samples had gate leakage currents at 245°C roughly one-third less than those of Type-A2.

a. DC Parameters

Figure 49 shows the dc aging characteristics of the 245°C biased samples. Both I_{DS} and I_{DSS} decreased with time, but it was the rapid decrease in g_m that led to device failure. Eight of the ten samples were found to have failed before 144 hr, and all ten by 1165 hr. As the figure shows, the transconductance failed because the characteristics of the gate degraded. Both $|V_{GB}|$ and $|V_p|$ increased rapidly, indicating that the gate was losing control over the source-drain current. The change in g_m merely reflected the V_{GB} degradation; I_{DSS} was essentially unchanged during this early period.

The same process appears to be taking place with the biased devices stressed at 200°C, as shown in Figure 50, but at a slower rate. At this writing, only one of the three samples has failed.

Figure 51 shows the changes measured in the unbiased 245°C samples. The transconductance and both gate voltage parameters are changing much slower than their biased counterparts, which indicates the importance of electrical stress level on these parameters. None of these unbiased samples has failed yet. Judging by the linear approximations to the median data points, it appears that the specific drain current I_{DS} is close to signaling a significant number of failures. Several samples are also close to failing because of g_m changes.

None of the unbiased Type-C FETs has failed at 200°C either. Figure 52 shows their measured changes. Both g_m and I_{DS} are approaching their lower failure limits.

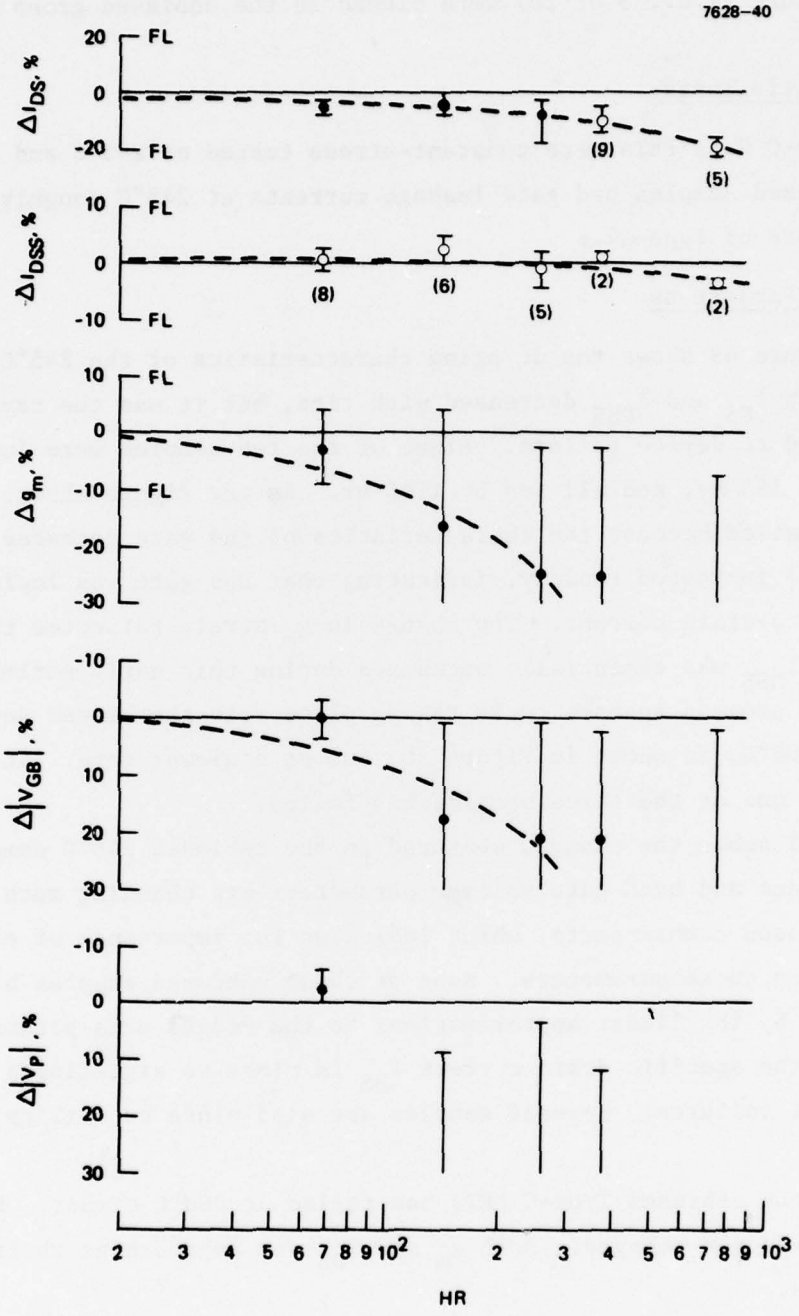

Figure 49. DC parameter changes for low-noise-biased Type-C FETs stressed at 245°C (N = 10).

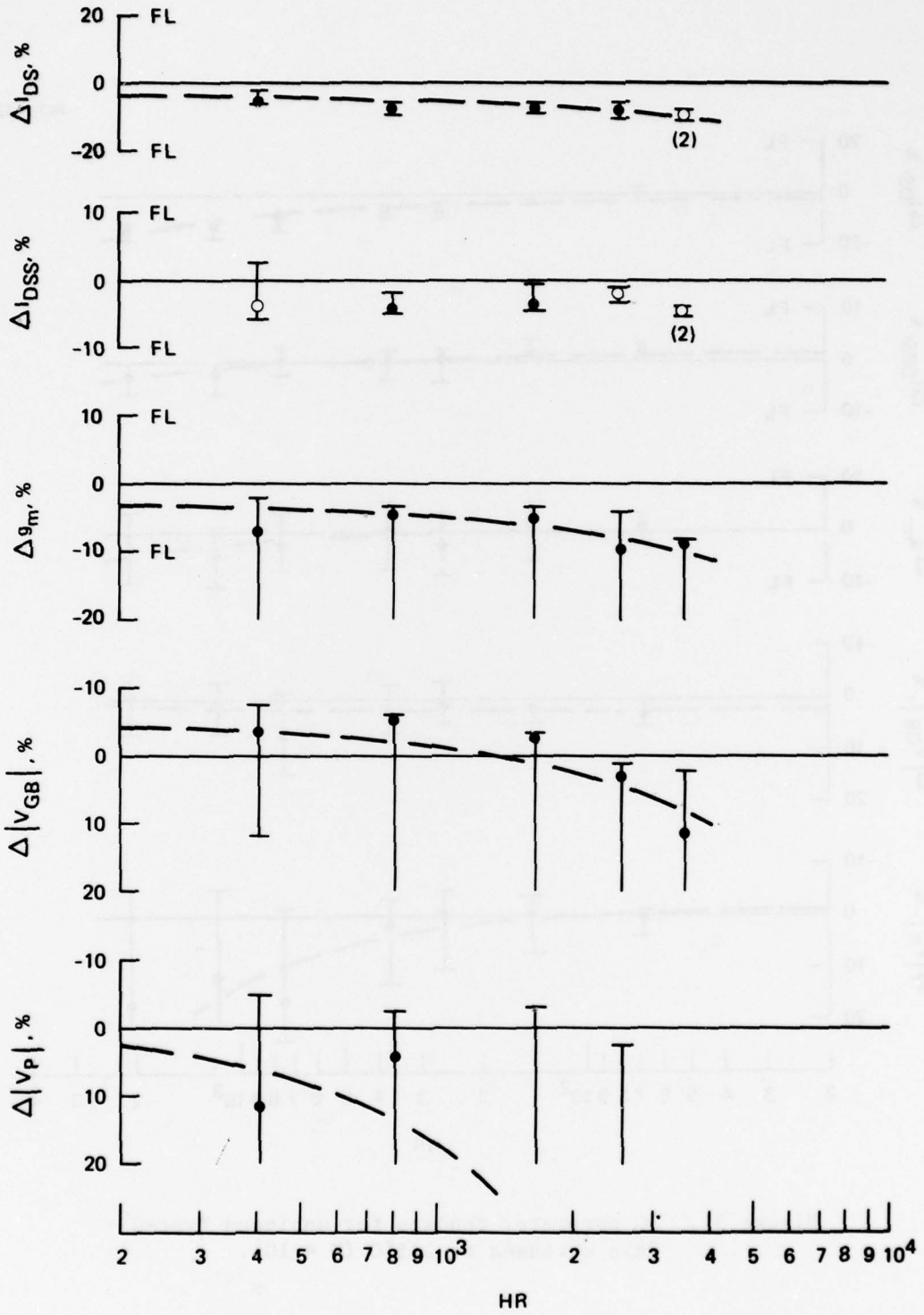

Figure 50. DC parameter changes for low-noise-biased Type-C FETs stressed at 200°C (N = 3).

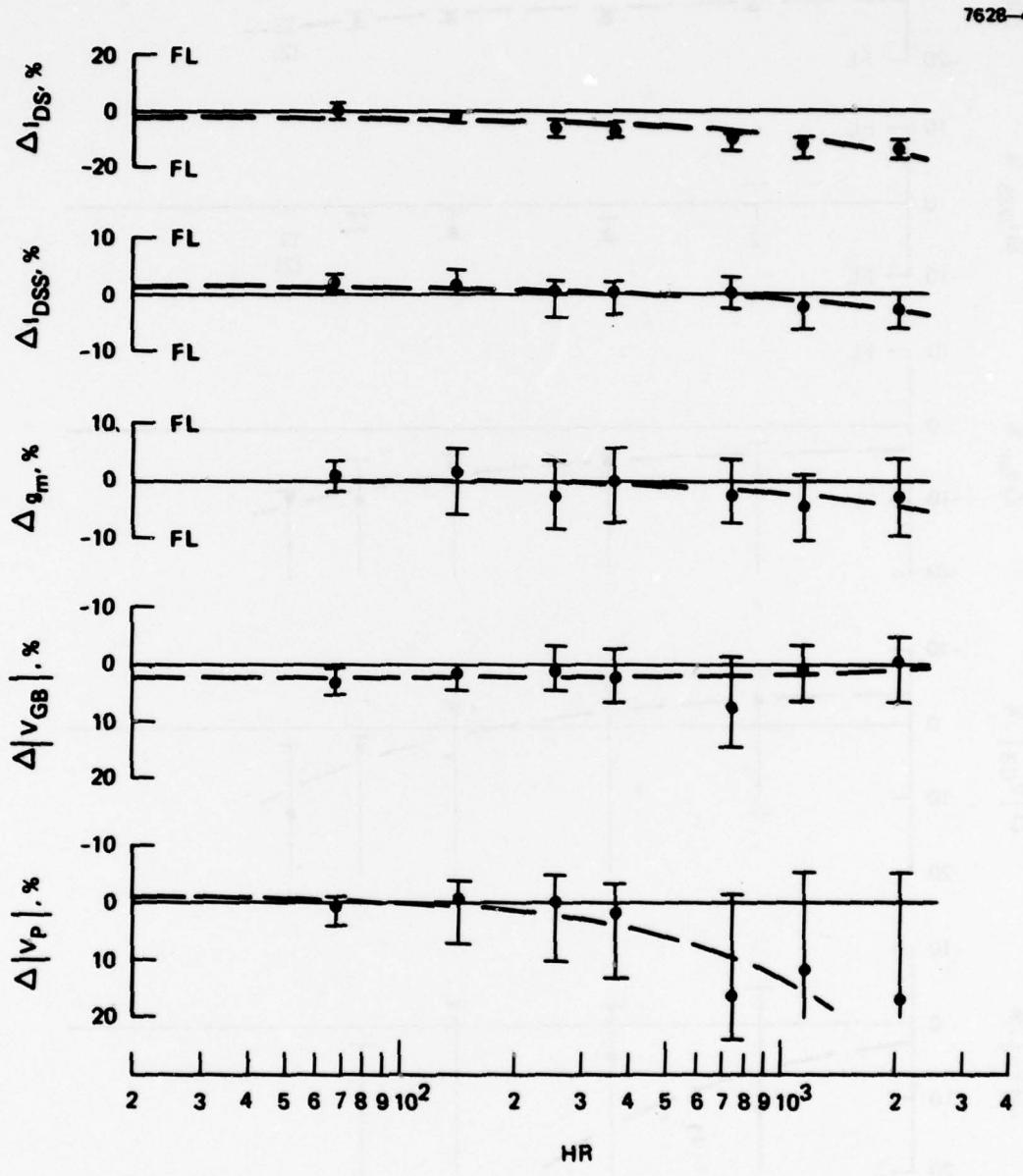

Figure 51. DC parameter changes for unbiased Type-C FETs stressed at 245°C (N = 10).

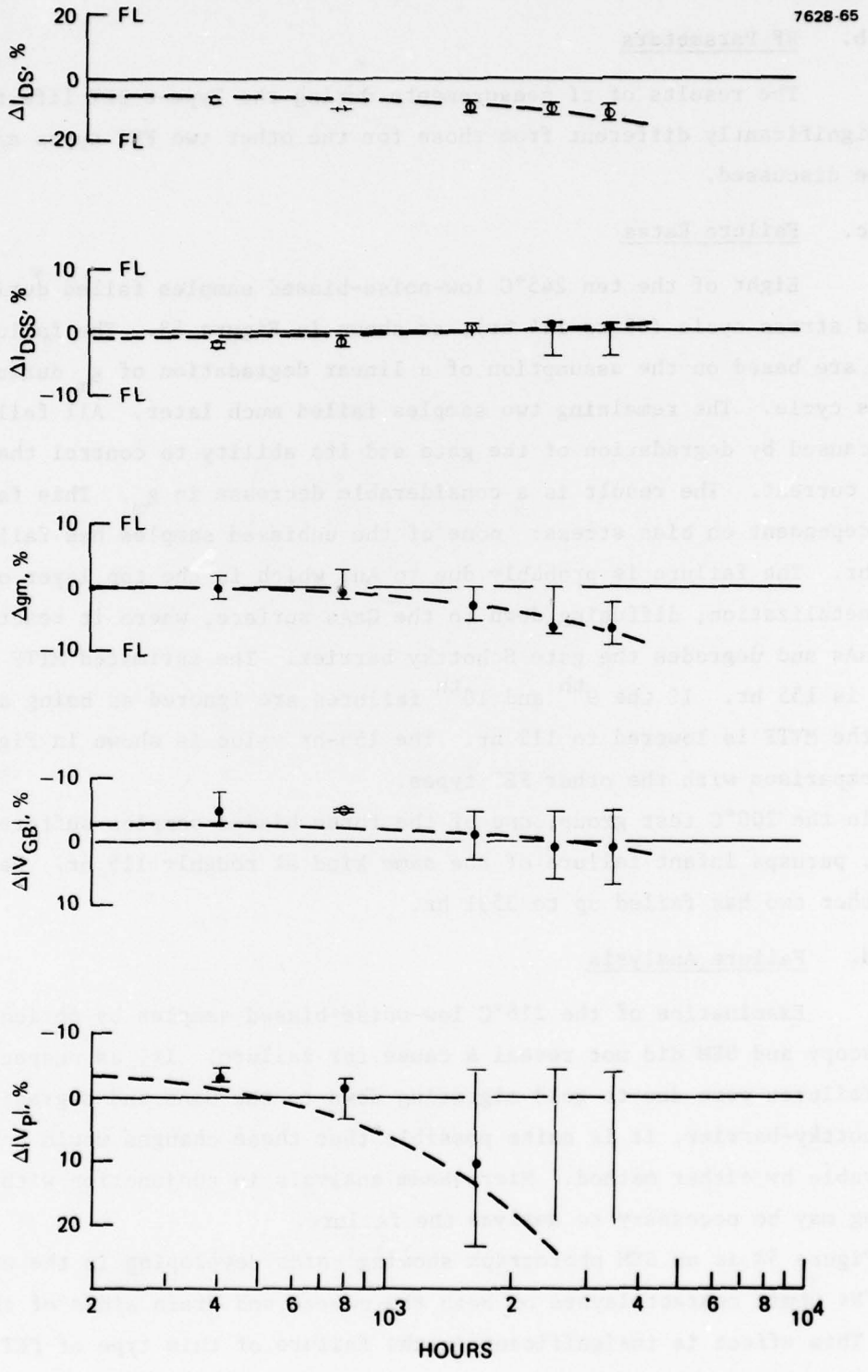

Figure 52. DC parameter changes for unbiased Type-C FETs stressed at 200°C (N = 3).

b. RF Parameters

The results of rf measurements during the Type-C FET life tests are not significantly different from those for the other two FET types and will not be discussed.

c. Failure Rates

Eight of the ten 245°C low-noise-biased samples failed during the second stress cycle (69 to 144 hr), as shown in Figure 53. The failure times shown are based on the assumption of a linear degradation of g_m during the stress cycle. The remaining two samples failed much later. All failures were caused by degradation of the gate and its ability to control the source-drain current. The result is a considerable decrease in g_m. This failure is very dependent on bias stress: none of the unbiased samples has failed up to 2073 hr. The failure is probably due to Au, which is the top layer of the gate metalization, diffusing down to the GaAs surface, where it reacts with the GaAs and degrades the gate Schottky barrier. The estimated MTTF for this group is 155 hr. If the 9^{th} and 10^{th} failures are ignored as being atypical, then the MTTF is lowered to 112 hr. The 155-hr value is shown in Figure 32 for comparison with the other FET types.

In the 200°C test group, one of the three biased samples suffered an early, perhaps infant failure of the same kind at roughly 115 hr. Neither of the other two has failed up to 3531 hr.

d. Failure Analysis

Examination of the 216°C low-noise-biased samples by optical microscopy and SEM did not reveal a cause for failure. If, as suspected, the gate failures were due to gold migrating down to the GaAs and degrading the Ti Schottky-barrier, it is quite possible that these changes would not be observable by either method. Micro-beam analysis in conjunction with plasma etching may be necessary to analyze the failure.

Figure 54 is an SEM photograph showing voids developing in the exposed Au-Ge/Ni Ohmic contact layers on both the source and drain sides of the channel. This effect is insignificant in the failure of this type of FET.

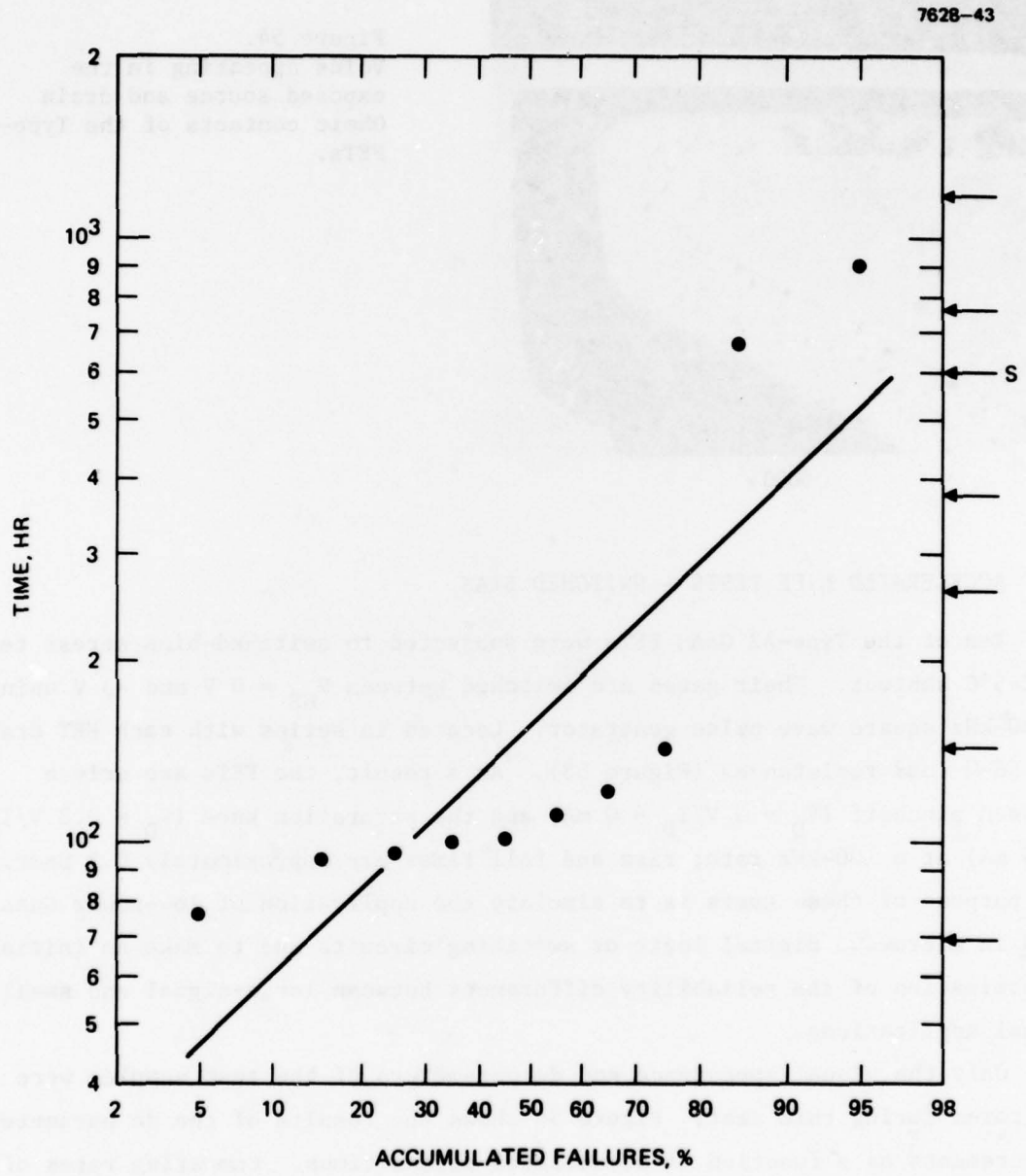

Figure 53. Failure distribution of low-noise-biased Type-C FETs stressed at 245°C.

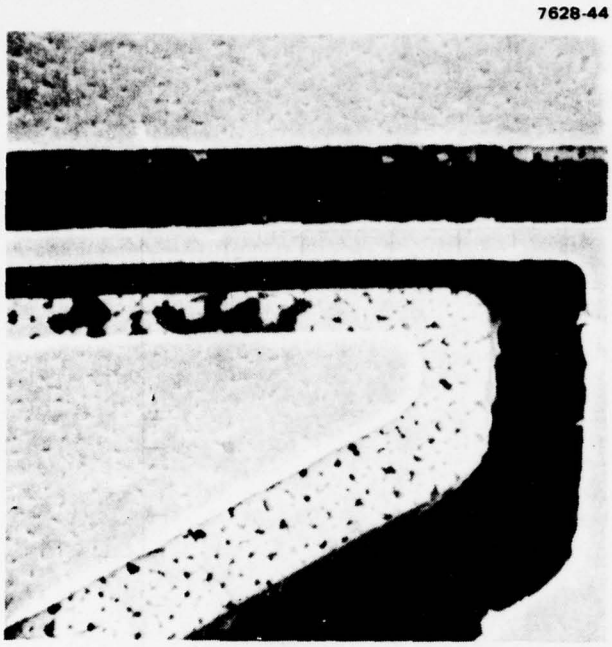

Figure 54.
Voids appearing in the exposed source and drain Ohmic contacts of the Type-C FETs.

D. ACCELERATED LIFE TESTS — SWITCHED BIAS

Ten of the Type-A2 GaAs FETs were subjected to switched-bias stress tests at 245°C ambient. Their gates are switched between V_{GS} = 0 V and -3 V using a 100-kHz square wave pulse generator. Located in series with each FET drain are 56-Ω load resistances (Figure 55). As a result, the FETs are driven between pinchoff (V_D = 3 V/I_D = 0 mA) and the saturation knee (V_D = 0.8 V/I_D = 40 mA) at a 100-kHz rate; rise and fall times are approximately 0.5 μsec. The purpose of these tests is to simulate the application of low-power GaAs FETs in microwave digital logic or switching circuits and to make an initial determination of the reliability differences between large-signal and small-signal applications.

Only the visual appearance and dc parameters of the test samples were monitored during this test. Figure 56 shows the results of the dc parameter measurements as a function of accumulated stress times. Comparing rates of change of these parameters with the rates for the 245°C low-noise-biased Type-A2 FETs of Figures 18 through 22 brings out several differences. Primarily, for the switched-bias case, the gate voltage parameters are increasing at a much slower pace, almost approaching the rates of the unbiased samples

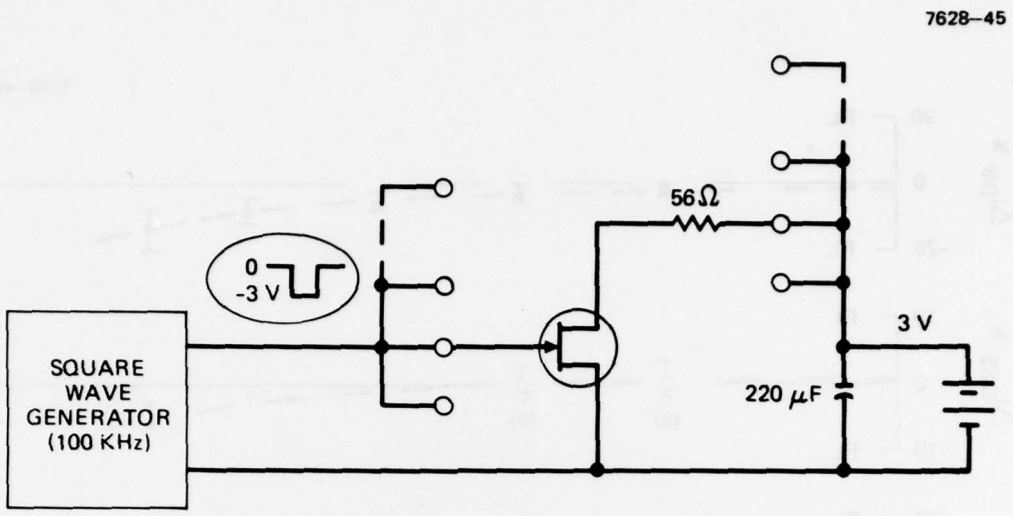

Figure 55. Schematic of switched-bias environmental stress test circuit.

(Figures 26 and 27). This is undoubtedly because the switched devices see a maximum drain voltage of only 3 V as compared to 5 V for the low-noise-biased devices and because the gate parameters are sensitive to voltage stress. As a result of the slower V_{GB} and V_P changes, the transconductance g_m is degrading much slower also. The specific drain current I_{DS} is decreasing at about the same rate; thus, the maximum source-drain current I_D = 40 mA through the switched-bias samples is not large enough, compared to the 10 mA of the low-noise-biased samples, to show any significant increase in the rate of degradation of the Ohmic contact resistance or channel resistance.

Microscopic examination of the switched-bias samples revealed no visual changes different from those of the low-noise-biased Type-A2 devices. The salient changes are the development of bumps along the Al gate stripe and some pitting or voiding of the Ohmic contacts near the channel edges. No evidence of Au electromigration caused by the higher current levels has appeared.

Because of the lower degradation rate of the switched-bias FETs, only 4 of the samples had failed by 2,356 hr. This compares to 9 out of 10 at the same time for the 245°C low-noise-biased case and 1 out of 10 for the unbiased. Thus, the difference in drain voltage stress between V_D = 3 V and 5 V appears substantial. As before, however, all failures have been due to decreasing g_m caused by gate degradation. The failure distribution for the switched-bias

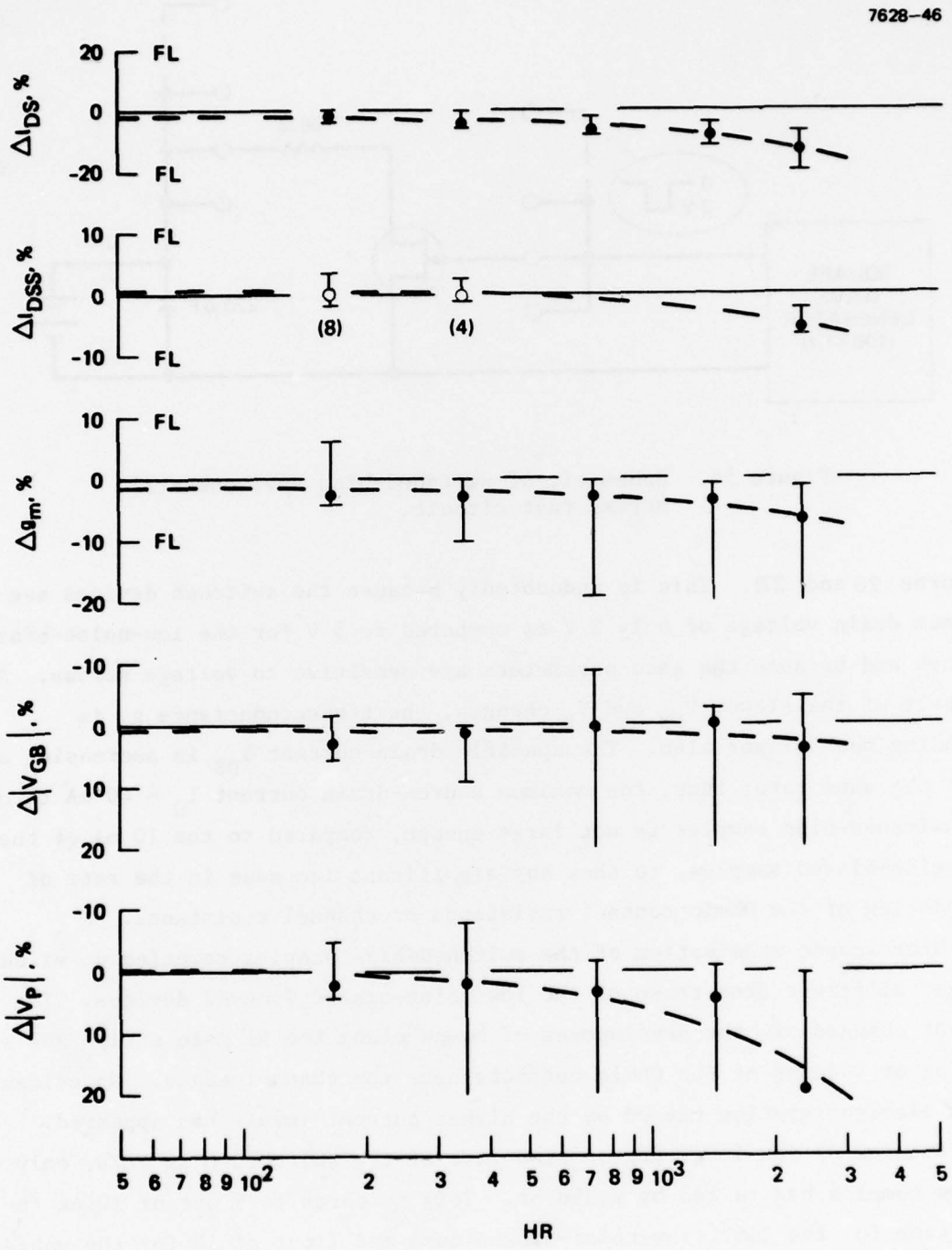

Figure 56. DC parameter changes for switch-biased Type-A2 FETs stressed at 245°C (N = 10).

samples is shown in Figure 57. A preliminary extrapolation to an estimated median-time-to-failure yields MTTF = 2,333 hr.

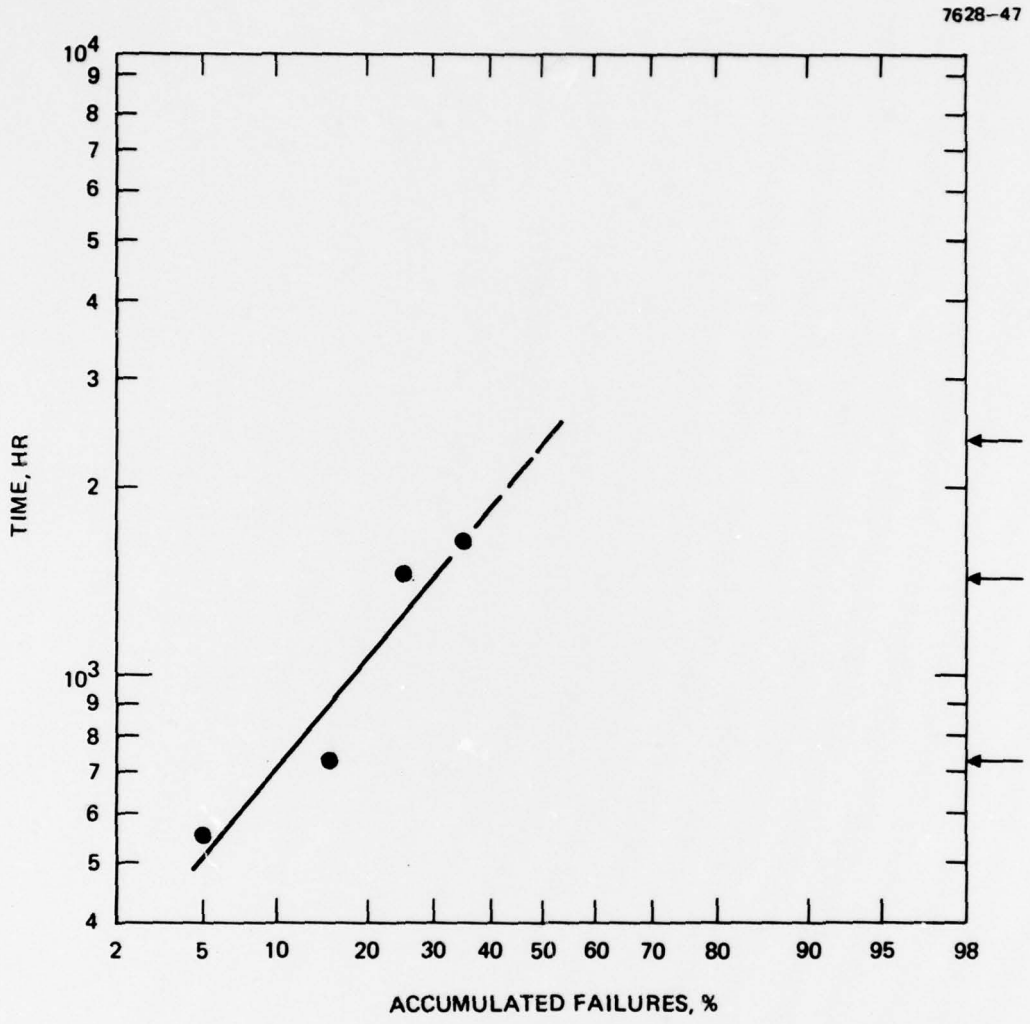

Figure 57. Failure distribution of switched-bias Type-A2 FETs stressed at 245°C.

SECTION 4

ELECTRICAL STRESS TESTS

Samples of the GaAs FETs were subjected to high-voltage dc pulses and high-power rf signals to determine their damage threshold levels. In both cases, it was generally found that no operational degradation was observed in the Al-gate FETs until the stress levels exceeded the thresholds for catastrophic, irreversible failure. These tests and their results are described below.

A. DC PULSE STRESS

When the gate of a GaAs FET is overstressed with a dc pulse, the result is polarity dependent.[1] Positive voltages lead to forward biasing of the gate diode, and failure can occur either at points of low resistance to ground or at points of high gate resistance. Negative voltages lead to failure at points of lowest reverse breakdown voltage.

The gates of the test samples were subjected to high-voltage dc pulses (using the circuit shown in Figure 58). This test is similar to one performed by previous investigators.[1,3] The dc power supply charged the capacitor C to a test voltage V_C. The switch then discharged the capacitor through the gate of the FET. Both the source and drain of the FET were grounded. A mercury-wetted relay was used as the switch to minimize contact bounce and resistance.

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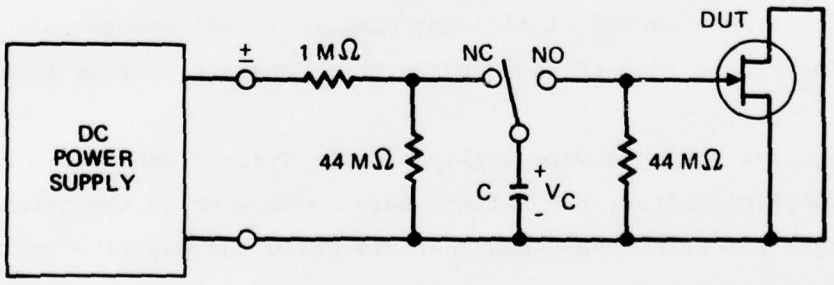

Figure 58. Schematic of dc-pulse stress circuit.

At each voltage setting, the capacitor was discharged through the FET five times, with 5 sec intervals between pulses. The voltage V_C was increased until the FET failed. A 100-pF capacitor was normally used. Since this is approximately the same capacitance as the human body,[1] the test in some ways simulates the static discharges that can occur if the devices are not handled carefully; however, static voltage levels can be much larger than the levels used here. A 1000-pF capacitor was also used to determine if the damage thresholds were energy or voltage constant.

To monitor changes in the test devices, their I-V characteristics were displayed on a curve tracer and photographed. Their pinchoff voltages V_p were also measured and recorded. Following each five-pulse discharge sequence, the I-V characteristics and pinchoff voltages were compared with the initial characteristics. Failure normally occurred with the development of either a source-gate short or a gate-drain short.

Table 14 summarizes the results of these tests. For positive voltages on the gate, the Type-A2 and Type-B FETs required about 70 V and 78 V on the 100-pF capacitor to fail, and all samples failed within ∿5 V of these values. The corresponding failure energies were about 2.5 and 3.0 ergs. When the 1000-pF capacitor was used, the failure thresholds changed to 52 V (13.5 ergs) and 27 V (3.6 ergs), respectively. The Type-B FETs, therefore, failed at a relatively constant energy level, whereas the Type-A2 were closer to constant voltage than constant energy. In all cases, the I-V characteristics and pinchoff voltages of these samples remained essentially unchanged until the failure threshold was reached and the shorts developed. The Type-C FETs behaved differently, however. Their burnout threshold voltages for 100 pF varied between 42 and 65 V, and in several cases their I-V characteristics and pinchoff voltages showed significant changes (∿10%) before burnout occurred. The single 1000-pF test indicates a constant voltage threshold for Type C.

When negative voltages were applied to the Type-A2 and Type-B FETs, using the 100-pF capacitor, the failure thresholds were in the neighborhood of 40 V (0.8 ergs) for both types, considerably below the positive voltage values.

Table 14. Summary of Results of Gate Failure Tests Using DC Pulse Stresses

Pulse Polarity	FET Type	Number of Samples	Capacitance (C), pF	Approximate Failure Voltage (V_F), V	Stored Energy ($CV_F^2/2$), ergs	Failure Mode
+	A2	3	100	70	2.5	Gate-drain short
		2	1000	52	13.5	
+	B	3	100	78	3.0	Source-gate short
		1	1000	27	3.6	
+	C	3	100	42-65	0.9-2.1	
		1	1000	47	11.0	
-	A2	2	100	38	0.7	Gate-drain short
-	B	2	100	40	0.8	Source-gate short

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All of the failed samples were examined to determine the cause of the electrical shorts that developed on failure. All of the Type-A2 FETs developed gate-drain shorts, and these were invariably located at one of the gate tees (i.e., where a gate lead from a gate bond pad connects to the gate stripe (see Figure 59). At these tie points, the gates bulge slightly toward the drain, creating a region of either minimum gate-drain resistance or of increased electrical field strength. These bulges are caused by the increased light levels in these regions when the photo resist is being exposed with the gate pattern. If the gate pattern is notched at these intersections, the bulges can be eliminated. The Type-B FETs developed source-gate shorts, usually in the immediate vicinity of the fork of the gate (see Figure 60). These are regions of higher field strength and minimum gate resistance. The

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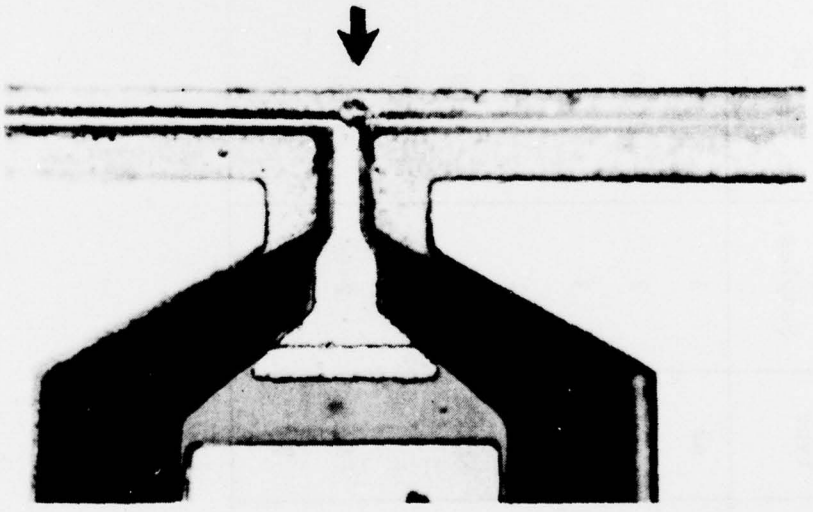

Figure 59. Gate-drain short at gate intersection of Type-A2 GaAs FET (1000X).

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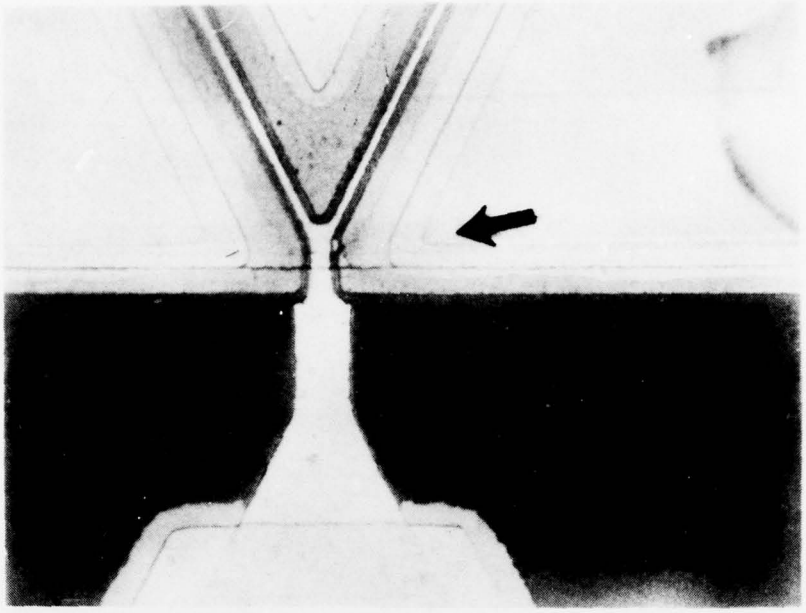

Figure 60. Gate-source short at fork of Type-B GaAs FET gate (1000X).

Type-C FETs also developed source-gate shorts but they appeared at random weak points along the gate or gate lead (see Figure 61). The Type-C gates are generally much closer to the source than the drain.

Our results can be compared to those of other investigators. For positive pulses, Bellier et al.[1] report Al gate failure at 20 ergs (200 V), significantly higher than our findings for Types A2 and B. However, their devices appear to have had larger source-drain separations (6 μm). Cooke[5] found the failure of gold gates to be energy constant at about 4 ergs. In contrast, the Type-C FETs failed at lower energies (1 to 2 ergs with 100 pF) and appeared to be more voltage constant, but only one sample was tested with 1000 pF. For negative pulses, the Type-A2 and Type-B Al-gate FETs required 2.5 times the 0.3 ergs reported by Abbott and Turner[3] but only one-third the 2 ergs reported by Bellier et al.[1] for FETs with longer channels. In all cases reported, only the Type-C FETs had samples that degraded significantly at stress levels below failure threshold. Our results do not support previous findings[3,5] that gold gates are more rugged than Al gates.

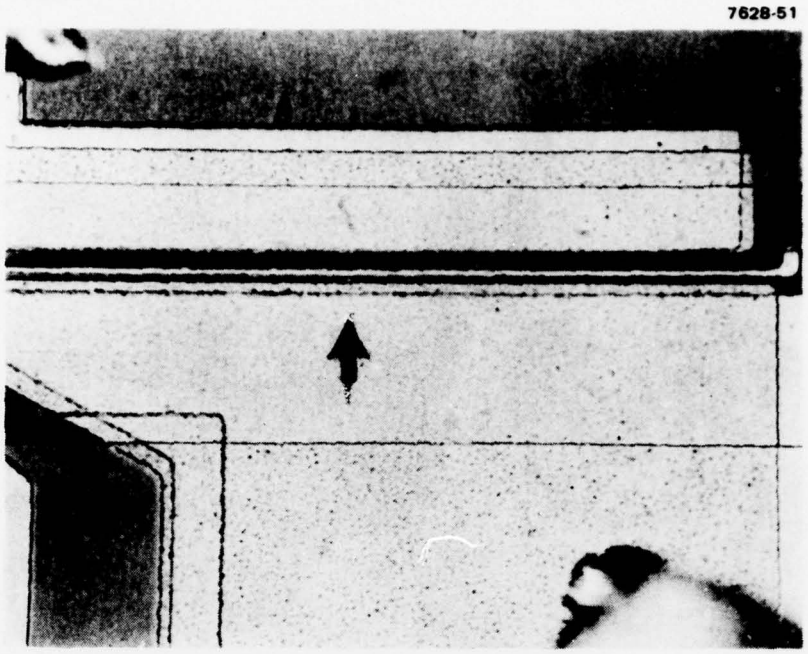

Figure 61. Gate-source short located at middle of Type-C GaAs FET gate (1000X).

B. HIGH-POWER RF STRESS

The Type-A2 GaAs FETs were tested to determine what input rf power levels are required to cause damage. These measurements were performed at 9.7 GHz, using both cw and fast-rise-time pulse signals. The high-power microwave equipment necessary to perform these tests was available to this program for only a very short period; therefore, there was insufficient time available to perform the same tests on the Type-B and Type-C FETs. To simulate typical GaAs FET operation, the test samples were epoxy mounted and wire bonded to 0.5 in. x 1 in. microstrip carriers. Each FET was then dc biased (V_D = 3 V) and tuned for minimum noise figure at 9.7 GHz by placing small capacitive chips on the input and output microstrip lines and adjusting the chip positions and drain current for F_{min}. Each of the tuning chips was then bonded in place with a drop of Kodak 910. The result was a set of simple, single-stage low-noise amplifiers for use in the rf stress tests.

1. CW Stress

Using the microwave circuit shown in Figure 62, five test samples were exposed to a series of increasing levels of cw input power. The samples were dc biased at their optimum low-noise values. Measurements were made of the minimum noise figure and associated gain before and after each exposure to high-level input power. Each exposure lasted 1 min.

The cw stress results are summarized in Table 15. No changes were detected in the rf parameters up to 1 W of input power. In the 1 to 2 W region, small changes began to appear. At 3 W and above, device failure ocurred ($\Delta F_{min} > 0.5$ dB, $\Delta G_a < -1$ dB); burnout was observed in one case at 10 W. These values are approximate and varied with device, but they are indicative of the general trend.

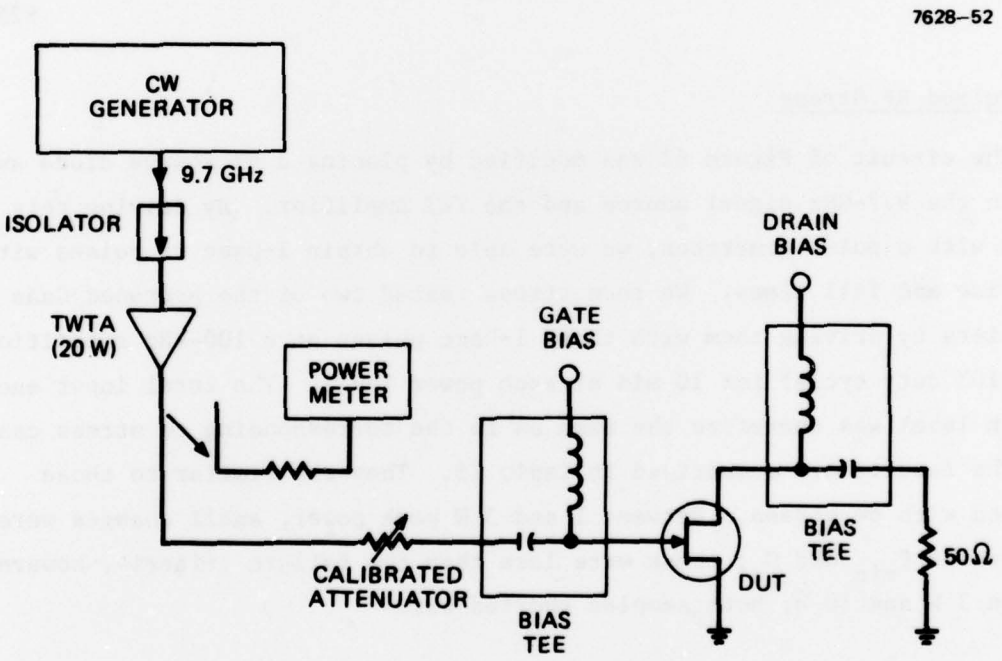

Figure 62. Simplified schematic of circuit for cw rf-stress tests.

Table 15. Results of CW and Pulsed RF Stress Tests on Type-A2 FETs (f = 9.7 GHz)

RF Stress Test	Input Power, W	Effect on FET
CW (N = 5)	<1	None
	1-2	Small changes (∿0.2 dB) in F_{min} and G_a
	≥3	F_{min}/G_a failure Burnout
Pulsed (N = 2)	<1	None
	1-3	Small changes
	3-10	Burnout

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2. Pulsed RF Stress

The circuit of Figure 62 was modified by placing a microwave diode switch between the 9.7-GHz signal source and the TWT amplifier. By driving this switch with a pulse generator, we were able to obtain 1-μsec rf pulses with fast rise and fall times. We then stress tested two of the pretuned GaAs FET amplifiers by driving them with these 1-μsec pulses at a 100-kHz repetition rate (10% duty cycle) for 10 min at each power level. The total input energy at each level was therefore the same as in the corresponding cw stress case.

The results are summarized in Table 15. They are similar to those obtained with cw stress. Between 1 and 3 W peak power, small changes were observed in F_{min} and G_a; these were less than the failure criteria, however. Between 3 W and 10 W, both samples shorted out.

SECTION 5

CONCLUSIONS

The purposes of this study were to investigate the reliability of low-noise microwave GaAs FETs to determine their potential reliability and operating life and to identify their failure mechanisms. Within the limited scope of this program, we were able to test approximately 230 state-of-the-art GaAs FET chips having 1-μm gate lengths. The major portion of these, the approximately 150 Type-A FETs, were fabricated by HRL and supplied to this study without charge. These devices incorporate aluminum gates. In addition, 80 FET chips were purchased from other manufacturers so that a sampling of alternative technologies could be tested. Forty of these devices (Type B) also use aluminum gates. The other 40 (Type C) are gold-gate FETs. At the time of purchase, they were the only FETs with gold gates available on the commercial market, although at least one other manufacturer was known to be fabricating gold gate FETs for internal use only. The Type-B and Type-C FETs were examined by optical microscopy, SEM, and electron microprobe to confirm published and manufacturer-supplied information regarding the geometry and metalizations used. The only discrepancy uncovered was that the Type-C gate lengths were a full 1 μm long although they had been advertised to be 0.5 μm gate FETs. This was not a total surprise since the production of 0.5 μm gates by photolithography is a difficult process to control.

The samples were electrically characterized for their dc parameters. They were also measured for minimum noise figure and associated gain at 10 GHz. These dc and rf parameters were also used to monitor the aging characteristics of the FETs during the accelerated life (environmental stress) tests. Approximately 20 samples of each type of FET were characterized for their 2 to 8 GHz S-parameters under approximate low-noise-bias conditions (V_D = 3 V, I_D = 10 mA). These S-parameters can be used to calculate alternative impedance and admittance matrices, gain parameters, stability factors, etc. or to design appropriate input and output matching networks. All three types of FET had similar state-of-the-art electrical characteristics.

Samples were subjected to electrical stress tests to determine their failure threshold levels. All three types of FET were tested for their ability to withstand high-voltage dc pulses applied to their gates. For positive pulses, the aluminum gate failure energy was in the neighborhood of 3 ergs; however, the Type-A2 FET failure threshold was somewhere between constant voltage and constant energy. Neither aluminum gate FET showed any significant change in dc parameters until catastrophic failure occurred. In contrast to the results of another study,[3] the threshold levels for the gold-gate FETs were not essentially different from those for Type-A2, and several gold-gate samples showed considerable changes in dc characteristics at stress levels significantly below catastrophic failure levels. For negative pulses, the aluminum gate FETs failed at 0.8 ergs energy. In GaAs FET applications, proper design of bias circuitry should protect the FETs from dc pulse damage. Because of limited availability of high-power rf test equipment, only the Type-A2 FETs were subjected to rf stress tests. The devices were low-noise-biased during these tests. Essentially no difference was found between the effects of cw stress and fast-rise 1-μsec rf pulse stress. For both cases, the threshold power level for failure was 1 to 3 W peak.

The most extensive test effort was directed to the environmental stress tests. Both low-noise-biased (V_D = 5 V, I_D = 10 mA) and unbiased samples were tested. The Type-A2 FETs had test groups stressed at 245°C, 231°C, and 216°C. A Type-B group was stressed at 216°C, and a Type-C group was stressed at 245°C. Each group started with 10 biased and 10 unbiased samples. The plan had been to stress all three FET types at 245°C; however, the high-temperature gate leakage current of the Type-B FETs was significantly higher than that of the other two, causing the reduction in stress temperature to 216°C to avoid excessive electromigration effects. Finally, there was a mixed oven containing all three types stressed at 200°C. Failure criteria were based on specified changes in certain dc parameters. Noise figure and gain at 10 GHz were also monitored to measure correlation with the dc changes. The dc biased Type-A2 FETs generally fail because of degrading gate characteristics. This failure is believed to be due to a poor SiO_2 glassivation layer, because previous nonglassivated FETs of the same design and fabrication process have not failed in this manner. A good SiO_2 process should eliminate this failure mode or at least significantly lengthen its MTTF. The Type-B FETs demonstrated

this stable Al-gate characteristic. The unbiased Type-A2 FETs age at a much slower rate than the biased.

The Type-B FETs, both biased and unbiased, fail because of increasing parasitic source and drain resistances, primarily Ohmic contact resistance. These FETs have Au-Ge/Pt Ohmic contacts, which appear to be less reliable than the Au-Ge/Ni contacts used in the Type-A and Type-C FETs. Several of the unbiased Type-B FETs suffered catastrophic gate failure because of intermetallic formations at the gate bond pad. A Pt-Al reaction is suspected. These FETs do have a Ti barrier layer between the Pt and Al, but it can be breached with the proper conditions. A slight pad redesign should allow the Ti to provide a more effective barrier. Improved step coverage by the Ti/Pt layers would also improve reliability.

The dc biased Type-C FETs failed relatively early because of rapid gate deterioration. The unbiased FETs have not demonstrated this degradation. It is suspected that the gold top layer of the gate stripe is migrating down to the GaAs and degrading the Ti Schottky barrier. This remains unconfirmed, however. The Ti/Cr/Pt layers under the gold are all relatively thin (100/100/400 Å); increasing their thicknesses might improve the gate reliability. However, another possibility is that the gold migrates down the side surfaces of the gate. Further study of this problem is necessary.

Ten samples of the Type-A2 FETs were subjected to switched-bias stress tests at 245°C. They were switched between pinchoff (V_D = 3 V, I_D = 0 mA) and saturation (V_D = 0.8 V, I_D = 40 mA) at a 100-kHz rate to simulate large-signal applications in microwave digital logic or switching circuits. These samples failed at a rate somewhere between that of the low-noise-biased and unbiased Type-A2 FETs at 245°C. This is explained by the fact that the maximum drain voltage seen by the switched FETs is 3 V, significantly less than the 5 V on the low-noise-biased samples. The 40-mA maximum current has not increased the rate of degradation of the Ohmic contact resistance or channel resistance, and no signs of electromigration have been observed.

The environmental stress tests on the Type-A2 FETs are being continued to obtain additional data for improved estimates of their MTTFs and the failure-mode activation energy E_a. Both the 245°C and 231°C biased groups have failed, but the results are conflicting: the 231°C group failed sooner than the 245°C group. A possible explanation is the fact that the bias circuitry

on the 231°C oven was faulty. The 216°C test group is still proceeding with no failures, however, and appears to be confirming the 245°C results. We are continuing these tests with Hughes support, and will report the findings when obtained. A preliminary MTTF curve has been derived (see Figure 32). The corresponding activation energy E_a is 1.0 eV, which agrees with Irvin and Loya,[7] who describe several GaAs FET failure mechanisms with energies near 1 eV. These high-temperature test results can be extrapolated to lower, normal operating temperatures, provided that the same failure mechanisms and activation energies remain dominant at low temperature. It is possible, however, that other failure mechanisms, with lower activation energies, dominate at operational temperatures but are not revealed during high-temperature testing because they are overshadowed by high-energy mechanisms. Although long-term, low-temperature tests are required to evaluate this possibility, it is encouraging that the room-temperature tests that have been reported[3-5,7,8] failed to uncover any such new failure mechanisms.

All of the MTTF data points accumulated to date for the three types of FET are falling in the general neighborhood of the previously published data for biased HRL FETs[6] and unbiased NEC FETs,[4] but obvious differences do exist in the aging characteristics of the different devices. Judging by the results of this study, a GaAs FET design with improved reliability would incorporate:

- Au-Ge/Ni Ohmic contacts
- An Al gate with either a Type-A Cr/Au bond pad or an improved Type-B Ti/Pt/Au bond pad
- Type-B SiO_2 glassivation layer.

Continuing the present environmental stress tests by HRL will provide additional valuable data, but further GaAs FET reliability investigations are necessary. One purpose would be to expand from this study and test a broader sample of GaAs FET types (e.g., additional gold-gate devices should be life tested). A second purpose would be to eliminate some of the contradictions and uncertainties apparent in the current literature, many of which are due to the variety of test methods and conditions used in the different investigations. Standardizing environmental stress test procedures and failure criteria would allow more meaningful analyses and comparisons of test results. This would accelerate the convergence toward fabrication of GaAs FETs having improved overall reliability and predictable operating life times.

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