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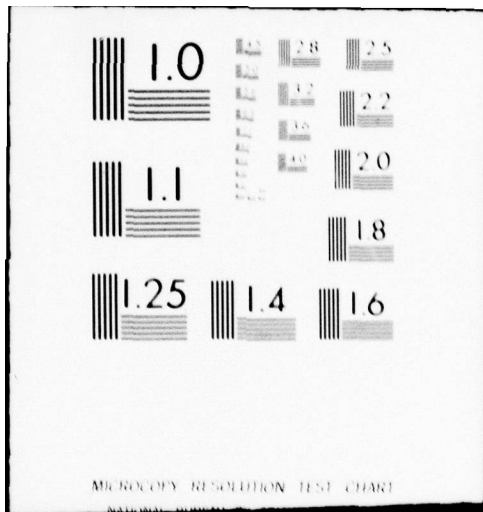
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INTEGRATED THERMAL AVIONICS DESIGN (ITAD)

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WESTINGHOUSE DEFENSE AND ELECTRONIC SYSTEMS CENTER
SYSTEMS DEVELOPMENT DIVISION
BALTIMORE, MARYLAND

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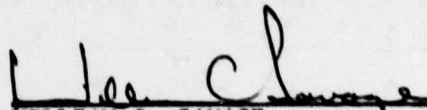
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FOREWORD

This report presents results of a study conducted by Westinghouse Electric Corporation, Baltimore, Maryland, under Air Force Contract F33615-77-C-2074, "Integrated Thermal Avionics Design" during the period of September 1, 1977 to June 1, 1978. This contract was conducted under the sponsorship of the Air Force Flight Dynamics Laboratory, Wright-Patterson Air Force Base, Ohio with Dr. A. H. Mayer (FEE) as project engineer.

The results of the study and recommendations for further study are presented herein. The Westinghouse Program Manager was R. F. Porter. Other major contributors were R. T. Dolbeare, E. R. Levitt, R. H. Warsham, R. J. Bennett, J. T. Prichard, Y. Lord, R. A. Marlett.

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SECTION I

INTRODUCTION

The primary goal of Integrated Thermal Avionics Design (ITAD) is the development of a system of software programs to accomplish optimum life cycle cost (LCC) design of avionics systems. Accomplishing this goal means ultimately making all necessary trade-off decisions, not only concerning the avionics system design itself, but also concerning the aircraft environmental control system (ECS).

This final report details the studies and progress made toward these goals within the constraints of this initial phase of the project. This initial phase was not intended to yield a working software system. It is a study phase intended to design, in an architectural sense only, the software system required to accomplish LCC optimization.

One of the major ground rules of this study is to use existing software wherever possible. Thus a survey of existing computer programs has been made to determine which are most applicable to the ITAD system. In the initial phase of the program, it was recommended that the ITAD software should be designed for eventual implementation on the CDC-6600 computer located at Wright-Patterson Air Force Base (WPAFB). Therefore, part of the choice of computer programs is based on their applicability to this hardware facility as well as their applicability to the ITAD system.

Many functions required to be performed by the LCC optimization process or to accomplish some peripheral tasks are non-existent. In these cases, algorithms have been defined to fill these gaps. Software code has not been written in this phase of the study except where it was convenient or made completion of this study easier.

Three separate groups of effort are reported herein. These are divided into two major tasks with one task having two separate phases. Task I involves the definition and design of the ITAD software system. Task II involves an actual reliability optimization of an existing pair of Printed Wiring Boards (PWB) and predictions of the influence this optimization process has on total LCC.

Although optimization of LCC for every type of electronic component and subassembly is desirable and eventually possible, it became immediately apparent that effort should initially be concentrated on the digital PWB area. Since the majority of parts in modern avionics systems are contained in the digital area, large gains in total system reliability and Logistics Support Cost (LSC) can be realized. Automated wire routing programs are best suited for wiring digital circuitry. Also, thermal optimization techniques are relatively straight forward since modern digital packaging

techniques allow consideration of optimum arrangement on a row by row basis. Interactions between rows are a second order effect for most packaging techniques commonly used. In contrast, most analog boards (or boards consisting of discrete devices instead of microelectronic devices (MED's) have very complex arrangements requiring computations of temperatures and resulting reliability based on complex interactions between all the components on the PWB. In addition, changing the location of one component may require a complete rearrangement of all the components in a board - probably not in any systematic manner.

The optimization algorithms developed in this study for digital Printed Wiring Assemblies (PWA) have the necessary flexibility that they can be used to determine positions of PWA's relative to each other within a unit. In addition, they can be extended to the placement of each unit making up the total avionic system. Initially this total optimization cycle can be performed by the manufacturer of each avionic system going into the receptor aircraft. Finally, the same procedure can be used for the entire aircraft avionic systems either by the airframe manufacturer, the customer, or an avionics integration subcontractor.

SECTION II

TASK I - ITAD DEFINITION

Task I of the ITAD study was divided into two efforts. The first, to recommend the hardware system on which to implement the ITAD software. The second to define the ITAD software. These separate goals are entitled Phase I and Phase II respectively and are discussed in detail in sections 2.1.1 and 2.1.2.

2.1 PHASE I, COMPUTER FACILITY DEFINITION

The initial phase of the ITAD was aimed at choosing the best computer site for initial installation of the ITAD software. Three alternatives were explored:

- 1) The DEC-10 computer at WPAFB Avionics Lab
- 2) The CDC-6600 at WPAFB
- 3) A third alternative

Among those systems considered for the third alternative were the Westinghouse Univac 1110, a commercial timeshare system, and a combination of both WPAFB systems.

The commercial systems were eliminated due to expense and because they were CDC machines similar to those at WPAFB ASD and thus had no advantage in machine type. The Westinghouse Univac 1110 system was eliminated because access to the computer from terminals at WPAFB could not be provided.

The remaining computer sites, i.e., DEC-10, ASD CDC-6600, or a combination of the two were compared on the basis of the following criteria:

1) Conversion/installation costs

Most of the software to be used is located on the CDC-6600. Those which are not are easily converted from the DEC-10 or is available in a form compatible with the 6600.

2) Availability

This is an assessment of the availability of lack of the candidate machines at the given time a user tries to start an ITAD run.

3) Additional facilities required

This criteria considered the need for additional equipment such as graphics terminals, microprocessors, available memory, etc. The

CDC-6600 system presently has all the foreseeable facilities required. The inclusion of STAGING on the DEC-10 would require at least one additional terminal.

4) Ease of Use

This considered the amount of knowledge and experience required by the user to use ITAD on each of the three systems under consideration. A combination system would require a higher level of knowledge and more difficulty for the user.

5) Response time

Response time is defined as the time between starting the problem and obtaining an answer. This is dependent on availability. Machine speed, loading of the machine.

6) Software Maintainability

Maintainability expenses may vary between the candidate sites. This includes costs of updating as well as eliminating bugs found during use.

7) Difficulty in installation in another facility at later date.

The ease of installation of ITAD on other computer sites after having been installed at WPAFB will depend on the original site chosen.

A combination of machines is felt to be undesirable because of difficulties of intermachine interactions with the Data Base Manager (DBM) and because of increased maintenance costs. Also, since the ITAD software will be used by various avionics manufacturers, it will need to be converted to their computer systems. This will be more difficult if the original software is split between two machines.

Thus the combination of machines was eliminated as the final ITAD hardware facility. However, much of the software required for ITAD is currently resident on Wright-Patterson computers but is split between the Flight Dynamics Lab facility (ASD) and the Avionics Lab facility.

There are at the present time some facility problems with both of these sites. The DEC-10 at AFAL is dedicated to real time simulation causing frequent unacceptable turn-around times. The AFFDL CDC-6600 permanent and scratch file systems are overloaded causing frequent periods of inaccessibility. Elimination of these problems is a matter of speculation, but it seems that the most likely system to overcome these problems is the AFFDL CDC-6600 since its primary mission is to provide the entire base and the Flight Dynamics Lab in particular with required computational facilities.

Although the objective of this phase of study was only to choose a computer site, a parallel investigation was undertaken to determine the particular software and their interactions required to meet the second phase goals. This was necessary to make an intelligent judgement of the type of system and capabilities required of the site. Based on this study, the block diagram shown in figure 1 was developed.

Based on these requirements, a two-step implementation was decided to be most advantageous. The wire routing program, PCPRA, is currently resident on the AFAL DEC-10 system. In addition, the personnel with the expertise to use this program (which does require some interactive manipulations) is also at the AFAL. It is also felt that some period of study is required before this optimization loop will become completely automated. Therefore, the first step of implementation was chosen to put all required ITAD functions on the ASD AFFDL CDC-6600 facility except the wire routing program. This allows the utilization of the expertise at AFAL. Once the best implementations of the PCPRA program in the ITAD system has been defined and AFFDL personnel are familiar with its use, the program can be converted to the CDC-6600 and integrated into the ITAD system to run in an automatic optimization algorithm.

Thus figure 1 will initially have a break at the input to and output of the wire routing program representing a change of computer hardware facilities. In step two, this break will be eliminated by installing PCPRA on the CDC-6600.

2.2 PHASE II, ITAD SOFTWARE DEFINITION

Phase II of Task I is dedicated to the definition and description of the software required and their interactions required to accomplish the various functions needed to optimize avionics designs for minimum LCC, perform various environmental analyses, and various reliability and statistical calculations. The exact nature of these functions is described in the section. Wherever possible, existing software is used. The choice of software is biased toward those existing at WPAFB or its compatibility with the CDC-6600 computer at WPAFB.

Where existing software has not been found to apply to a function required by ITAD capability requirements, algorithms are defined.

2.2.1 LCC Optimization Loop

For purposes of the discussion of the optimization loop, the example will be centered on the optimization of the Printed Wiring Assembly (PWA) type shown in figure 2 which will be referred to as "coplanar cooled." This assembly consists of the boards and heat is transferred from the fins to the air.

All of the programs require some modification to facilitate interfacing with the data base management system described in section 2.2.7.

ITAD Flow Schematic

- Cooling Technique & Parameters
- Power vs Part no. (Circuit Symbol?)
- Initial Arrangement & Part No.
- Board Geometry
- Board Properties

- $T_j = f(x,y)$
- Part no. $f(x,y)$
- $\delta T / \delta x, \delta T / \delta y$
- Power = $f(x,y)$

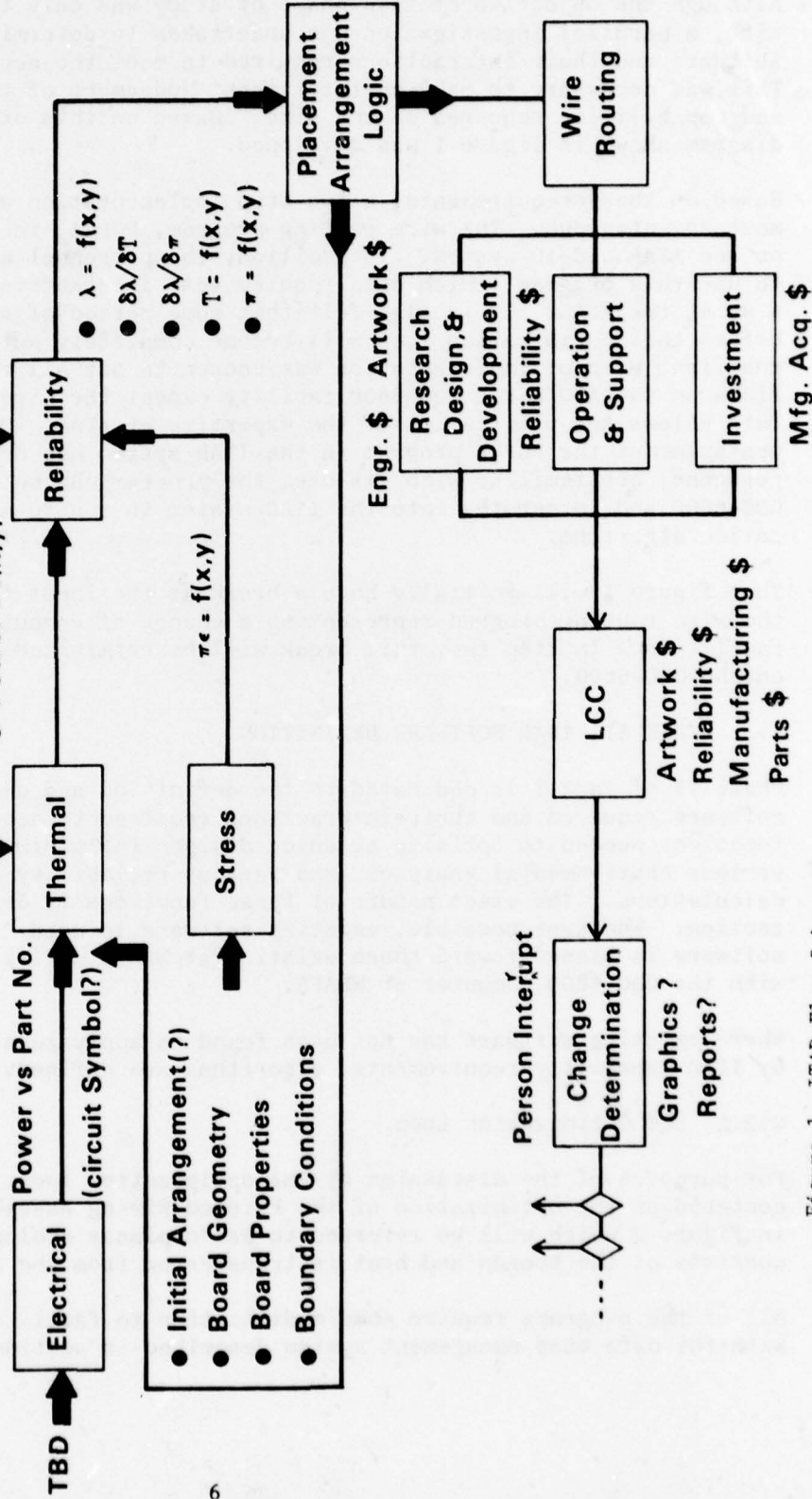


Figure 1 ITAD Flow Schematic

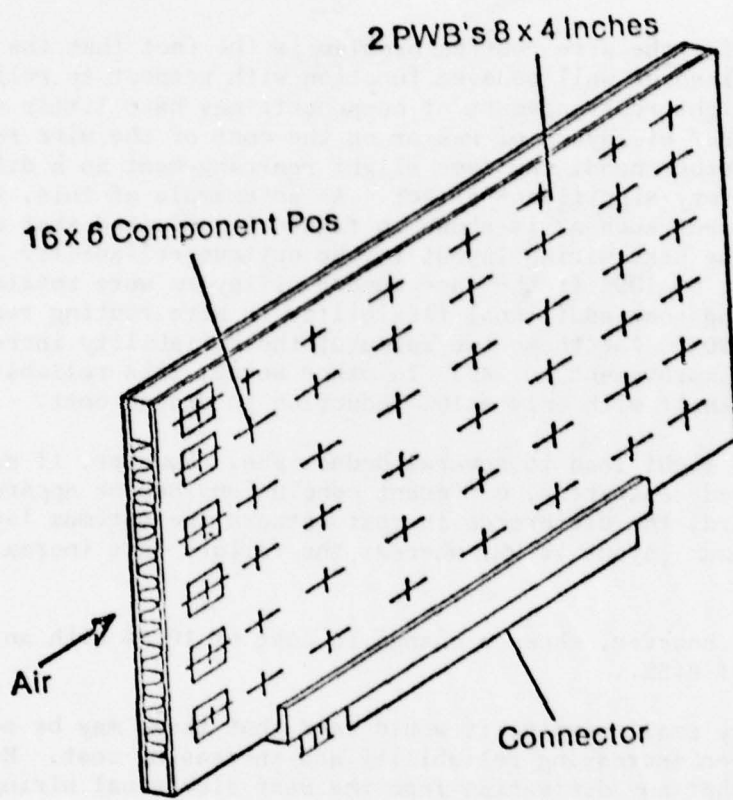


Figure 2. Air Cooled Printed Wiring Board

It became obvious at the outset of the study that the major difficulty in developing an efficient optimization algorithm was the magnitude and inefficiency of the automated wire routing process. This process usually takes several hours of computer central processor time and then still requires some manual intervention to complete the circuitry. The wire routing processes determine two major costs which must enter into the trade-offs required for optimum design. Even one pass through the wiring routing process is expensive. To make repeated passes to define an optimum layout is so expensive and time consuming that it is untenable for a production design process.

Further complicating the wire routing problem is the fact that the process is not a well defined or well behaved function with respect to reliability. For example, a slight rearrangement of components may have little or no effect on the number of layers of PWB or on the cost of the wire routing process. On the other hand, the same slight rearrangement on a different board may have a very significant effect. As an example of this, the trial optimization of a PWA such as is shown in figure 2 indicated that changing the layout from the best wiring layout to the optimum reliability layout increased the cost by 109% if the same number of layers were retained (see Table 1). Allowing some additional flexibility in wire routing reduced the cost increase to 90%. For these two layouts, the reliability increase changed from 23% improvement to 14%. In other words, this reliability gain was cut almost in half with only a 10% reduction in design cost.

The above results might lead to several deductions. However, if each board is considered separately, different conclusions become apparent. For the first board, the difference in cost between the optimum layout and the modified optimum layout is 9%, whereas the failure rate increased by 6.7%.

The second board, however, shows a change in cost of 10.5% with an increase in failure rate of 8.5%.

Based on this very small sample, it would seem that there may be some correlation between increasing reliability and increasing cost. However, it also appears that any derivation from the best electrical wiring layout causes a sharp (100%) rise in cost. The same sort of behavior is evident when the number of layers is allowed to increase, but there is a slightly lower maximum cost.

For purposes of optimization trade-off calculations, the wire routing routine should consider at least four different layouts. They would include:

- 1) Best wiring layout
- 2) A perturbation of (1) in the direction of 10% improved reliability
- 3) Optimum reliability layout
- 4) A perturbation of (3) in the direction of 10% reduced reliability (improved routeability).

Table 1. BOARD DESIGN COSTS

BOARD PART NUMBER	CONSTRAINT SET	FAILURE RATE	NUMBER OF LAYERS	DESIGN PRICE \$
644R407	Optimized	4.5	10	6700
644R407	Optimized	4.5	12	3800
644R407	Semi-Optimized	4.8	10	6200
644R407	Semi-Optimized	4.8	12	3800
644R408	Optimized	7.1	10	7600
644R408	Optimized	7.1	12	4800
644R408	Semi-Optimized	7.7	10	6800
644R808	Semi-Optimized	7.7	12	4800
644R407	Not Optimized*	6.4	10	2970
644R408	Not Optimized*	8.7	10	3870

*The Original Design was done to keep the Power in each Row Equivalent

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The design cost of each of these layouts for at least two different numbers of PWB layers must be predicted. It is completely impractical to completely wire route a PWB this many times. For this reason, a simplified procedure that is able to predict the relative costs of various layouts without actually completing the wire routing process is needed. Investigations (primarily discussions) with a leading corporation in the automated wire routing business indicate this is a viable approach. In the following discussion, it is assumed that such an estimation technique will be used in the ITAD system. It is, of course, recognized that there may be several possible perturbed layouts (items 2 and 4 above) which will give the same reliability predictions and have various impact on wire routing. Depending on the efficiency of the developed estimation software, a search can be made to attempt to find a "best" layout for the same perturbed reliability.

The LCC optimization block diagram is shown in figure 3. This diagram is shown as though data were passed directly from one program to another although it is, in actuality, passed via the data base management system (DBM) discussed in detail in section 2.2.7. An attempt to represent this is shown in figure 4 where the circles represent data in the DBM.

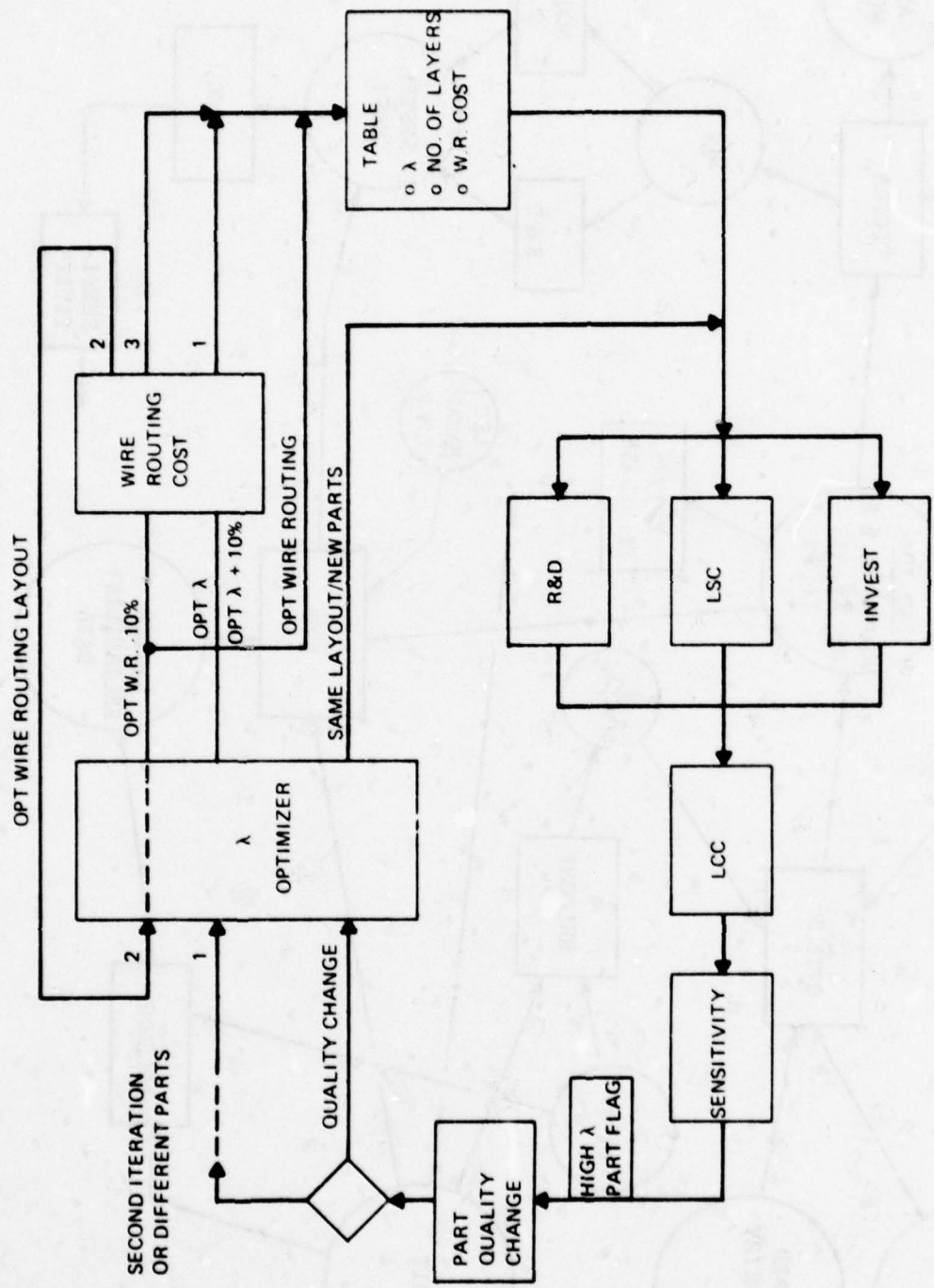
The optimization routines can be initiated by starting either at the existing computer program OPTEMP which calculates and optimizes reliability by inputting the PWA part number, cooling technique, and sink temperatures. Other required information is obtained from the data base management system. OPTEMP rearranges the component layout to obtain minimum failure rate. During this process, arrangements are stored at 5% improvement increments so that when optimum placement is attained, "snapshots" of approximately 10% suboptimal layouts can be retained for wire routing cost trade-offs.

These layouts are transferred to the wire routing cost program which calculates the number of layers of PWB circuitry required and associated costs of doing the wire routing and artwork.

The wire routing cost program then determines the best layout for ease of wire routing and associated costs. All of this data is stored in the DBM and the best wiring layout data is passed to OPTEMP where reliability calculations are made. Then OPTEMP perturbs this layout until reliability has been improved by approximately 10%. This fourth layout is returned to the wire routing cost program for costing information.

At this point a table has been established in the DBM as shown in Table 2. This data allows R & D costs and fabrication costs of the PWB at eight different points (eight designs). By adding the costs of parts and connectors, the investment cost is established.

The LSC for the four layouts can be calculated using the modified AFLC LSC model. Then adding the various costs yields an eight point LCC lattice from which the lowest LCC is picked.



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Figure 3. Optimization Loop

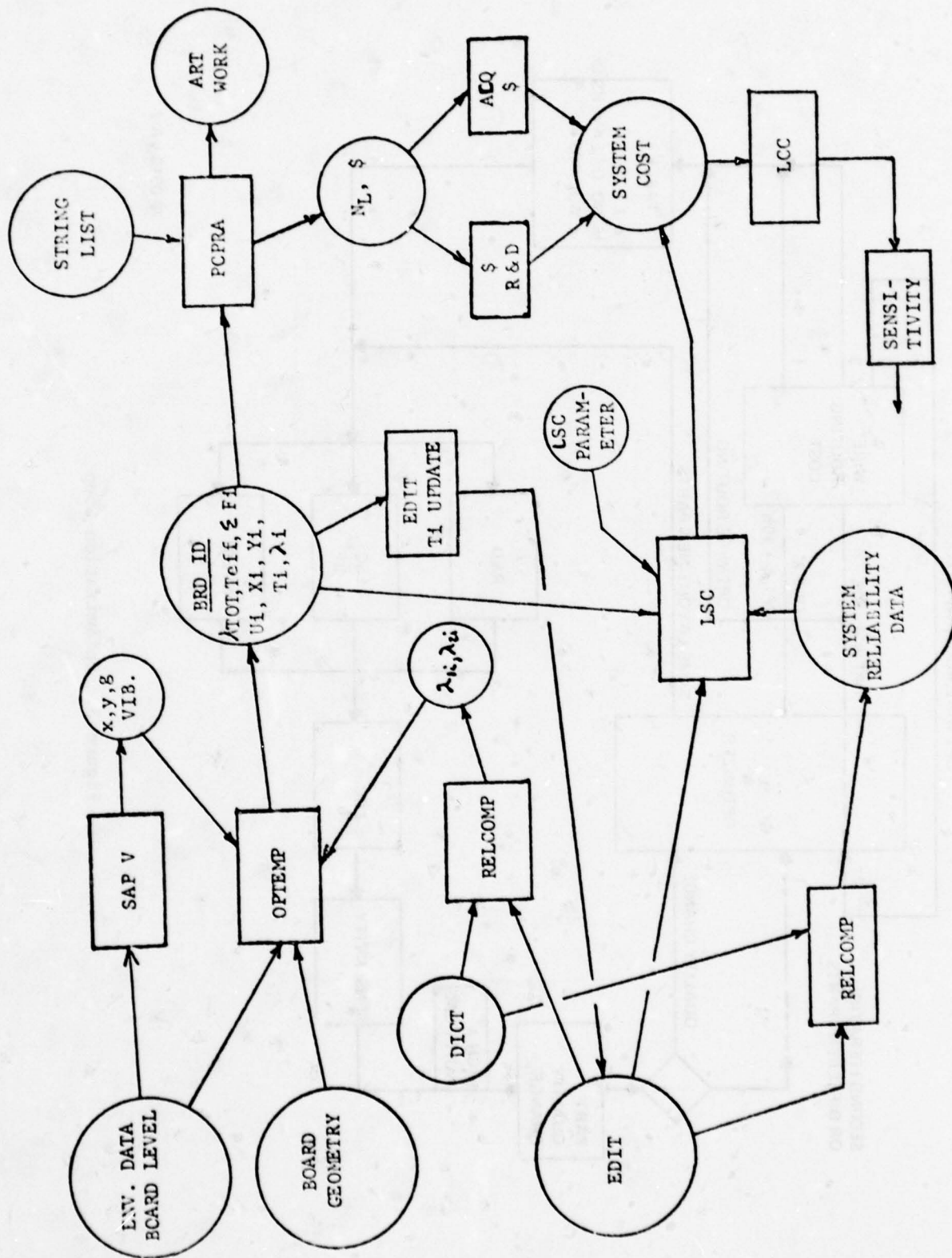


Figure 4. Optimization Loop

Table 2. COST TRADEOFF TABLE

CONDITION	FAILURE RATE	NUMBER OF LAYERS	DESIGN COST (\$)	NUMBER OF LAYERS	DESIGN COST (\$)
OPTIMIZED	λ_1	10	$(\lambda_1, 10)$	12	$(\lambda_1, 12)$
OPTIMIZED + 10%	λ_2	10	$(\lambda_2, 10)$	12	$(\lambda_2, 12)$
BEST WIRE ROUTING - 10%	λ_3	10	$(\lambda_3, 10)$	12	$(\lambda_3, 12)$
BEST WIRE ROUTING	λ_4	10	$(\lambda_4, 10)$	12	$(\lambda_4, 12)$

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A sensitivity analysis is now performed to determine relative sensitivity of LCC to PWB acquisition cost, parts acquisition cost, PWB R & D cost, or reliability. At this point the only parameter that can be further optimized in a reasonable manner is the parts on the PWB. Thus, if the sensitivity analysis shows LCC to be most sensitive to either part cost or reliability, lower quality parts can be exchanged for the better quality parts. If reliability is more sensitive than part cost, then better quality parts can be used.

With these changes, the optimization cycle returns all the layouts with the new parts to OPTEMP where new PWA reliability calculations are made and the table updated. The wire routing cost program is bypassed since the part change does not affect the wiring. If a completely different part is substituted (and this would be done manually) which does change the routing, the entire cycle must be repeated. The LCC cost matrix and sensitivity is performed and compared with the previous minimum LCC to determine if an improvement has been made. This process continues until no improvement is shown. Then a new optimum layout is defined and the entire cycle repeated.

This algorithm does not necessarily provide an absolute minimum LCC since there may be some particular layout which will give a slightly better result. However, this algorithm will give a near *minimum* LCC with a few iterations. Better optimization can, of course, be obtained by using 5% reliability increments and more data points in the lattice at the sacrifice of more computation.

An alternate technique which has the potential of coming closer to an absolute minimum but may require more or less iterations is to do a gradient search based on the sensitivity analysis starting first at the best wiring layout until no improvement is shown. Then start at the optimum reliability layout and reduce reliability until no improvement is shown. Then compare the two best LCC designs obtained from the two starting points. Again there are many layouts possible to obtain the same reliability and some increment must be used so this still does not guarantee an absolute minimum.

The optimization loop can be integrated with the aircraft LCC optimization routine to make aircraft ECS design decisions. This can be done by including the avionics optimization loop within the aircraft optimization loop. Thus different optimum avionics designs and LCC's which can be compared with the ECS LCC to find the best integrated design.

An approximation of this technique which would reduce the cost but not yield as good an optimum would be to not change the original PWB layouts. This would then only require recalculating reliabilities for the already established layouts. R & D costs and bare board acquisition cost would remain constant. The most desirable layout may change and the part quality will change with changes in coolant parameters i.e., flow rate, temperature, and pressure drop to provide a new LCC to compare with the aircraft LCC at each iteration.

It is obvious that the optimum avionics design considered by itself, is one where the aircraft ECS is supplying air at a high rate and cold temperature which will make the reliability completely insensitive to layout. This would allow the least expensive wire routing and the minimum number of layers with a very low failure rate. From the overall weapon system's point of view, the restriction of not altering the layout is not generally or strictly valid. However, within a range of values reasonable for the aircraft ECS performance and LCC, the approximation may be reasonable.

2.2.2 Thermal Environment Software

2.2.2.1 OPTEMP

The existing computer program OPTEMP which has been developed at the Flight Dynamics Laboratory, Wright Patterson AFB, will provide the means for optimizing component positions on the printed circuit boards. The existing version of OPTEMP will optimize both the component locations and the spacing between components for coplanar cooled printed circuit boards. Additional features which will be added to this program are:

- 1) Calculation of coefficients F and α .
- 2) Calculation of PWB equivalent temperature (this is defined below)
- 3) Identification of components via circuit symbols
- 4) Capability of handling additional cooling schemes
 - a. In-line conduction
 - b. Natural convection
 - c. Forced convection
 - d. Heat pipes
 - e. Thermoelectric devices
- 5) Choosing best cooling technique
- 6) Orienting PWB based on equivalent temperatures
- 7) Interface with DBM

The coefficients F and α used in the expression $\lambda = Fe^{\alpha T}$ will be calculated for each component based on two data points obtained from RELCOMP, i.e.,

$$\alpha = \left(\frac{1}{T_2 - T_1} \right) \ln \left(\lambda_2 / \lambda_1 \right) \quad \text{and} \quad F = \lambda_1 / e^{\alpha T_1}$$

where λ_2 is evaluated at T_2 and λ_1 is evaluated at T_1 . T_1 and T_2 are input by the user for RELCOMP failure rate calculations.

Components on each printed circuit board will be arranged in groups of constant α . Normally only 2 or 3 values of α will be encountered. An equivalent temperature will then be determined for each group of components

$$\text{by } T_{EQ} = 1/\alpha, \ln \left(\lambda_{Sum} / F_{Sum} \right) \alpha_i \quad @ T_{Sink} = T_1$$

where λ_{sum} = sum of failure rates of all components having $\alpha = \alpha_i$ calculated at a sink temperature $T_{\text{sink}} = T_1$.

The physical meaning of the equivalent temperature is given as the answer to the following question. If all components were at the same temperature, what temperature would yield the same failure rate as that calculated using the actual temperature distribution? That temperature is the equivalent temperature calculated as previously described. In addition to having a physical meaning, the equivalent temperature provides a means of treating an entire printed circuit board as a component, i.e.,

$$\lambda_{\text{BD}} = F_{\text{sum}} e^{\alpha_1 T_{\text{EQ}} + (T_{\text{sink}} - T_1)}$$

where T_1 = sink temperature at which T_{EQ} was evaluated and T_{sink} = new sink temperature.

If a printed circuit board has components with 3 different values for α , then $\lambda_{\text{BD}} = (\lambda_{\text{BD}}) \alpha_1 + (\lambda_{\text{BD}}) \alpha_2 + (\lambda_{\text{BD}}) \alpha_3$

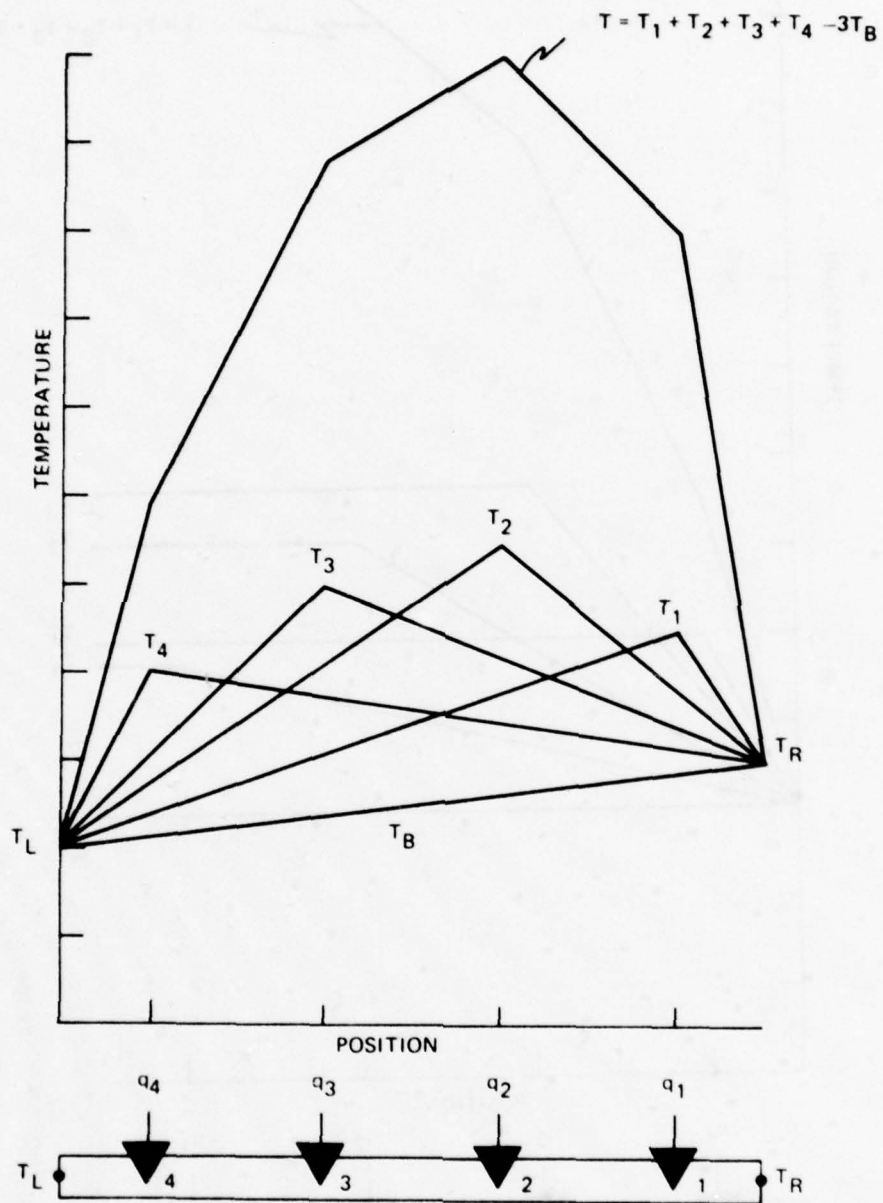
The OPTEMP program currently has an equivalent temperature routing. However, it is based on the α coefficient of the first component read into the input data.

The addition of circuit symbol numbers for component identification has already been added to OPTEMP and was used for the Task II effort. This feature requires the entry of the circuit symbol along with other component data such as power dissipation and size. This will be modified so that only the PWB part number need be entered and all required data will be obtained from the DBM.

The ability to optimize printed circuit board layouts with cooling schemes other than coplanar, will be incorporated into OPTEMP. In-line cooling is a common technique in which components are placed on heat conducting metal strips which conduct the component heat to the ends of the board which interface with a heat sink. The temperature profile of the conductors will be calculated by superposition whereby the contribution of each component is summed with the baseline conductor temperature. This is shown graphically in Figure 5 and 6 for two cooling schemes. Figure 5 is a general case of a board with heat sinks at each end which are at different temperatures. Figure 6 is a simplified case of only one heat sink. Optimization of the in-line boards will be achieved by the modified bubble sort technique described herein.

Natural convection cooling will also be added to OPTEMP. This cooling technique is often preferred because of its simplicity but is not often practical for boards with substantial heat dissipation.

It is assumed that the p.c. board will be oriented in a vertical direction in an unbounded fluid medium and that dissipation will be uniform. Components will be closely spaced and of uniform size and power dissipation. This allows the use of the experimental correlation of the local Nusselt number of a vertical flat plate with uniform heat flux as described in



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Figure 5. Temperature Profile for Conduction Cooled PWB With Sinks at Both Ends

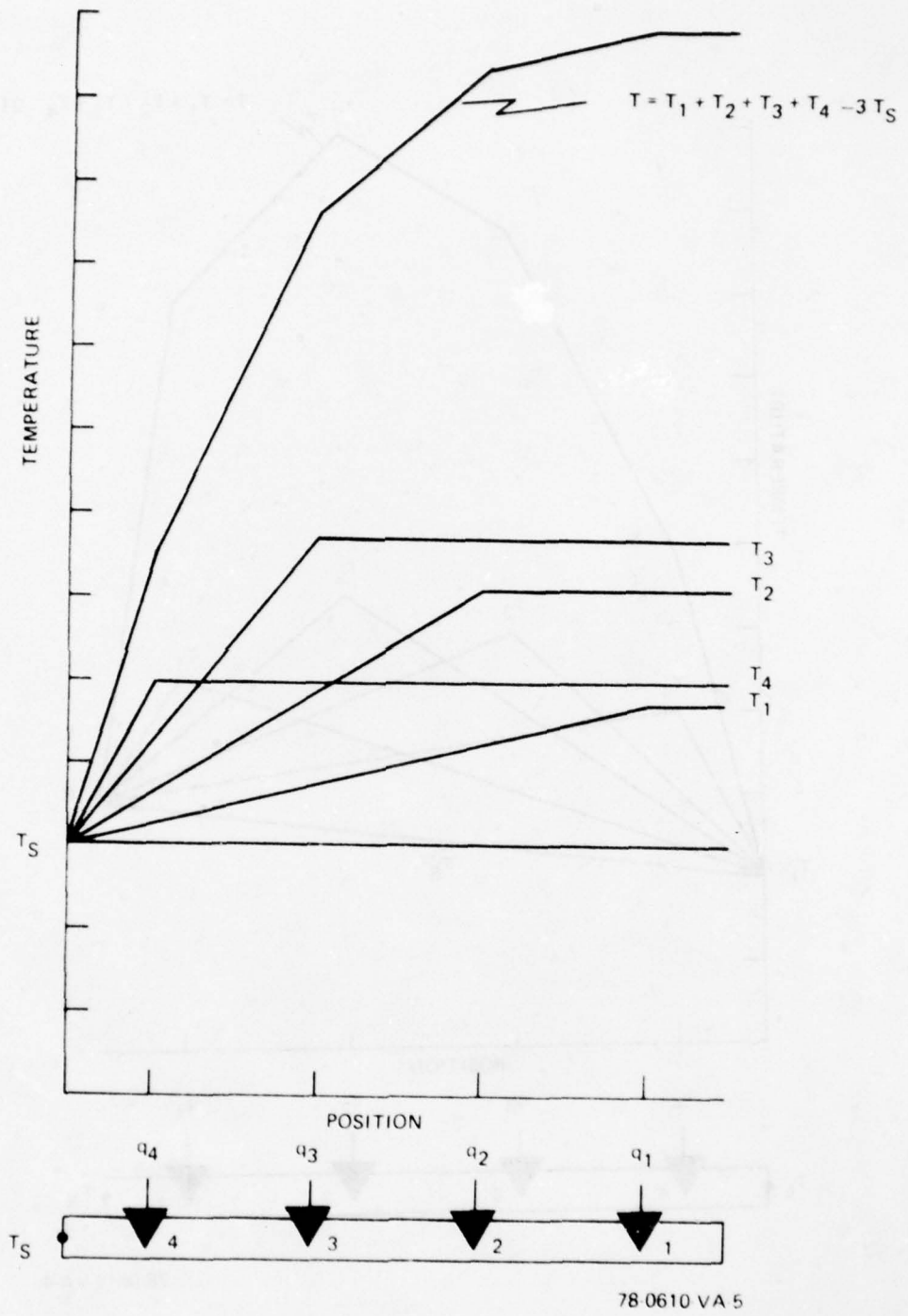


Figure 5. Temperature Profile for Conduction Cooled PWB With Sink on One End

Reference 1/ and 2/. Depending upon whether the induced convection currents are laminar or turbulent, one of the following equations will be employed.

$$\begin{array}{ll} \text{NU}_x = 0.60 (\text{Gr}_x^* \text{Pr})^{1/5} & 10^5 < \text{Gr}_x^* < 10^{11} \\ & \text{(Laminar)} \\ \text{NU}_x = 0.17 (\text{Gr}_x^* \text{Pr})^{1/4} & 2 \times 10^{13} < \text{Gr}_x^* \text{Pr} < 10^{16} \end{array}$$

where

$$\text{NU}_x = \text{Local Nusselt Number} = \frac{hx}{K}$$

$$\text{Gr}_x^* = \text{Modified Grashoff Number} = \frac{g B q x^4}{k \nu^2}$$

$$\text{Pr} = \text{Prandtl Number} = \frac{M C_p}{K}$$

$$h = \text{Local film coefficient (BTU/hrft}^2\text{°F)}$$

$$x = \text{Distance from bottom of board (ft.)}$$

$$K = \text{Thermal conductivity of fluid (BTU/hrft}^2\text{°F)}$$

$$g = \text{Gravitational constant (ft/hr}^2\text{)}$$

$$B = \text{Volume coefficient of expansion (1/°R)}$$

$$\nu = \text{Kinematic viscosity of fluid (ft.}^2\text{/hr.)}$$

$$M = \text{Absolute viscosity of fluid (lb. sec./ft.}^2\text{)}$$

$$C_p = \text{Specific heat of fluid (BTU/lb. °F)}$$

The local film coefficient, component area, and component heat dissipation are all that is needed to determine the component case temperature, i.e.,

$$T_c - T_{\infty} = \frac{q}{ha}$$

Component junction temperature will be calculated based on the junction to case thermal resistance which is obtained from DBM or by user input and can be obtained from MIL-SPEC's or from vendor catalogs. This technique assumes that the board is in an unbounded fluid medium and neglects any turbulence which might be generated due to spacing between components or due to variations in component heights. User judgement will be necessary for the case (considered unlikely) of a series of closely spaced boards.

For forced convection, the mass flow is defined and is input by the user. The junction to case thermal resistance obtained from sources described for free convection. The case to ambient thermal resistance will be determined by $\theta_{CA} = (1/ha) (273) (\text{°C/W})$ where h is the film coefficient (BTU/hr ft² °F) and a is the component area exposed to the

1/ HEAT TRANSFER DATA BOOK, General Electric Corp., Section 504.2, pg. 14

2/ HEAT TRANSFER, Holman, J. P., McGraw Hill, New York, 1976.

cooling area (in²). The constant 273 is a unit conversion factor.

The film coefficient h is determined by evaluation of the dimensionless Nusselt number $Nu = (hL/k)$ (1/12) where L = component length measured in the direction of air flow (inches) and K = thermal conductivity of air (BTU/hr ft °F).

The value of Nu depends upon the values of the Prandtl number (Pr) and the Reynolds number (Re). The dimensionless Prandtl number has previously been defined as $Pr = Cp/K$. The dimensionless Reynolds number is defined as $Re = (\rho v L / \mu)$ (1/12)

where ρ = air density (LBm/ft³)
 C = air velocity (ft/sec)
 L = component length as previously defined
 μ = air viscosity (LBm/ft hr)

The equations for the Nusselt number are (Ref. 2)

$$Nu = 0.664 \rho^{1/3} Re^{1/2} \quad Re \leq 5 \times 10^5$$

$$Nu = Pr^{1/3} (.037 Re^{.8} - 850) \quad 5 \times 10^5 < Re \leq 10^7$$

$$Nu = Pr^{1/3} \left[\frac{.227 Re}{(\log Re)} - 2.58 \right] - 850 \quad 10^7 < Re \leq 10^9$$

Optimization of component placement is accomplished by the existing OPTEMP routine.

Printed circuit boards which are configured with heat pipes for cooling do not require optimization of component placement because component temperatures are unaffected by position. However, provisions will be added to OPTEMP by which to calculate component temperatures and failure rates so that this cooling technique can be compared with others. Component junction temperatures will be calculated by

$$T_J = T_{H/P} + q_{comp} (\theta_{C-H/P} + \theta_{JC})$$

$$\text{where } T_{H/P} = T_{sink} + \frac{q_{TOTAL}}{hA_{condenser}} + \frac{q_{comp}}{hA_{evaporator}}$$

The user may input values for the hA 's. If no value is input, a default value of 1500 BTU/hr ft² °F, a commonly used "rule of thumb" used to size heatpipes, will be used for the h of both condenser and evaporator but the areas must still be input.

Two cases have been conceived wherein thermoelectric devices might be used and the capability of handling these cases will be contained in OPTEMP.

Case 1 considers a printed circuit board with a cooling scheme resulting in a few components which are too hot. The basic cooling scheme can be maintained and the problem components can be lowered in temperature by the

use of thermoelectric devices. Such a device can suppress the temperature locally, but in the process it generates considerable heat which adds to the total heat load of the board. These factors can be accommodated by redefining the component junction to case thermal resistance (θ_{jc}) and the component heat dissipation (q) as follows: $\theta_{jc}^* = (\theta_{jc}) (q) \frac{1}{q} \Delta T_{TED} / q^*$

$$q^* = q + q_{TED}$$

Where the subscript "TED" refers to properties of the thermoelectric device. The value of the temperature suppression (T_{TED}) is to be input by the user. A default value of 20°C will be included. Similarly, q_{TED} must be input, but a default value of 1.2 x q will be used. These values are chosen because they are a common near optimum design point for TED's. Ref. 3/. The sum of the two q 's will then be used as the equivalent component dissipation. Optimization of component locations can proceed based upon that applicable for the main cooling scheme with the redefined values accounting for the thermoelectric device.

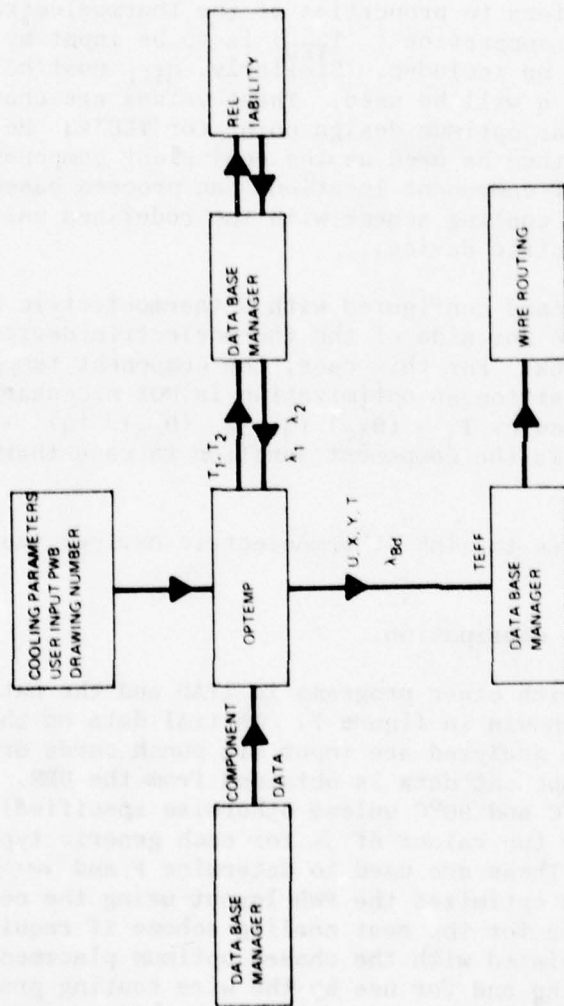
Case 2 considers an entire board configured with a thermoelectric device (or many small ones) with the hot side of the thermoelectric device attached to a constant temperature sink. For this case, the component temperature will not be a function of position so optimization is not necessary. Temperature will be calculated by $T_j = (\theta_{jc}) (q) + (\theta_{cs}) (q) + (T_{sink} - T_{TED})$ where θ_{jc} is the component junction to case thermal resistance

θ_{cs} is the component case to sink (thermoelectric device) thermal resistance

q is the component heat dissipation.

The relationship of OPTEMP with other programs in ITAD and the Data Base Management System (DBM) is shown in figure 7. Initial data on the cooling parameters and the PWA to be analyzed are input via punch cards or interactive remote terminal. Component data is obtained from the DBM. Two temperatures, T_1 and T_2 (40°C and 90°C unless otherwise specified) are used by RELCOMP to calculate two values of λ for each generic type of component on the assembly. These are used to determine F and α for the component type. OPTEMP then optimizes the PWB layout using the cooling scheme designated or searches for the best cooling scheme if required data is provided. The data associated with the chosen optimum placement is passed to the DBM for updating and for use by the wire routing program (PCPRA) or the routing cost estimating program, or the LCC program if parts type optimization is being done.

3/ CAMBION THERMOELECTRIC HANDBOOK, Cambridge Thermionic Corp., Cambridge, Massachusetts, Second Edition



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Figure 7. OPTEMP Flow Diagram

2.2.2.2 Optimization Algorithms

The optimization routine used in OPTEMP to arrange components is a straightforward "bubble search" routine amply described in reference 4/. This algorithm was designed specifically for the coplanar cooling technique described but is applicable to forced and natural convection cooling schemes. In all of these schemes, except unbounded natural convection, the air temperature at the component being examined is a function of only the sum of the dissipations of upstream components. The temperature of the k^{th} component can thus be expressed as

$$T_k = T_o + \sum_{i=1}^k \frac{q_i}{\dot{m}C_p} + \theta_{jc} q_k + \theta_{ca} q_k$$

where T_o is air inlet temperature

θ_{jc} is junction to case resistance of component k

θ_{ca} is case to air resistance of component k

$i = 1$ is at the air inlet end of the PWB

This can be expressed as

$$T_k = T_o + \theta_{ja} q_k + \frac{1}{\dot{m}C_p} \sum_{i=1}^k q_i$$

In the case of unbounded natural convection, this can be replaced by

$$T_k = T_o + \theta_{jc} q_k + \frac{q_k}{h(x_k) A}$$

i.e., the temperature of the k^{th} component is a function only of its location and power.

In the case of conduction cooling, the present algorithm cannot be used because the temperature of each component is affected by the position of every other component. Referring to figure 5, the temperature at any location is the sum of the temperature rises at this location caused by all the other components at other locations and the temperature rise caused by the component located at this position.

The temperature rise at location i due to a component to the right of i in figure 5 (components are numbered from right to left) can be expressed as:

$$\Delta T_{ij} = \left(\frac{R_{jr} R_{jl}}{R_{jr} + R_{jl}} \right) q_j \frac{R_{il}}{R_{jl}} ; i \geq j$$

4/ COMPUTER AIDED THERMAL DESIGN OF AVIONICS FOR OPTIMUM RELIABILITY AND LIFE CYCLE COST, Dr. Arnold H. Mayer, Wright-Patterson AFB, March 1978.

R_{il} = resistance from i to left sink

R_{ir} = resistance from i to right sink

R_{jl} = resistance from j to left sink

R_{jr} = resistance from j to right sink

q_i = heat dissipation of component i

The temperature at i due to components to the left of i can be expressed as

$$T_{ij} = \left(\frac{R_{jr} R_{jl}}{R_{jr} + R_{jl}} \right) q_j \frac{R_{ir}}{R_{jr}} ; i < j$$

In the case where the left and right sink temperatures, T_l and T_r , are not equal, another term is required.

$$T = \frac{(T_r - T_l) R_{il}}{R_{il} + R_{ir}}$$

Thus, the temperature at i , T_i , is expressed as:

$$T_i = T_l + \frac{(T_r - T_l) R_{il}}{R_{il} + R_{ir}} + \sum_{j=1}^i \frac{R_{jr} R_{il}}{R_{jr} + R_{jl}} q_j + \sum_{j=i+1}^n \frac{R_{jl} R_{ir}}{R_{jr} + R_{jl}} q_j$$

For a single sink on either end, this expression reduces to:

$$T_i = T_l + R_{il} \sum_{j=1}^i q_j + \sum_{j=i+1}^n R_{il} q_j$$

If component positions are numbered from left to right then

$$T_i = T_l + R_{il} \sum_{j=1}^n q_j + \sum_{j=1}^{i-1} R_{jL} q_j$$

The failure rate is expressed as:

$$\lambda = \sum_{k=1}^n F_k e^{-kT_k}$$

and the object is to minimize λ .

Initially, an attempt was made to use a dynamic programming approach to assure a global optimum solution. This has been done and is explained in detail in Appendix B. However, this approach requires substantially more computer time (in fact for more than 10 components it is impractical) and there is an intuitive feel that an appropriate bubble sort routine will yield comparable answers even if the rigor of dynamic programming is not present.

The sorting technique to be incorporated in OPTEMP for conduction cooled PWA's involves simply renumbering the components in order of increasing temperature, whatever their location, as shown in figure 8. The bubble sorting technique can now be used by comparing the sum of the failure rate of components one and two in their original and switched positions. If the total λ is lower when switched, they are left that way. Then 1 and 3 are compared in the same manner and the process continues until the last component is compared with its adjacent component.

The process can continue until completion in two ways. A complete pass can be made and then the components again renumbered for the next pass. This process continues until no switches are made in the last pass. This technique is illustrated in figure 9 and 10.

A second method is to renumber the components each time a switch is made and work backward switching and comparing all components until component 1 is reached. Then the comparison can resume at the location of the original switch.

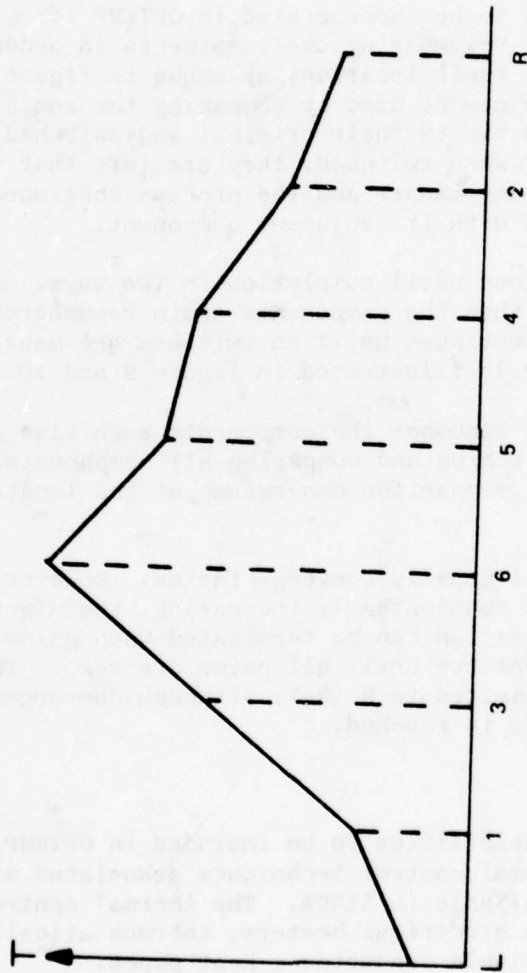
The latter method will usually converge faster. However, because the objective function is monotonically increasing, the algorithm will always converge. The optimization can be terminated when gains become insignificant or allowed to continue until all gains are zero. The maximum number of passes should be limited to N (N-1) although convergence should occur long before this limit is reached.

2.2.2.3 SINDA

In addition to the capabilities to be included in OPTEMP, the ability to model certain thermal control techniques associated with avionics equipment will be available in SINDA. The thermal control techniques required for ITAD are electrical heaters, thermostatically controlled flow devices, and variable conductance heat pipes.

Electrical heaters, constant, time dependent, or temperature dependent are easily simulated by several options within SINDA. The "SIT" and "SIV" options used in the heat source definition block allow respectively time and temperature varying source interpolated from any table input into the array data block. Alternately, the "D1DEG1" subroutine can be used in the VARIABLES 1 block to describe varying heat sources.

The simulation of thermostats is also included as a SINDA subroutine called THRMST. This routine returns a "1" or a "0." These can be used



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Figure 8. Number Components With Increasing Temperature

III. PERFORM ONE PASS THROUGH COMPONENTS NUMBERED IN THIS FASHION, WITH STANDARD BUBBLE SEARCH SCHEME.

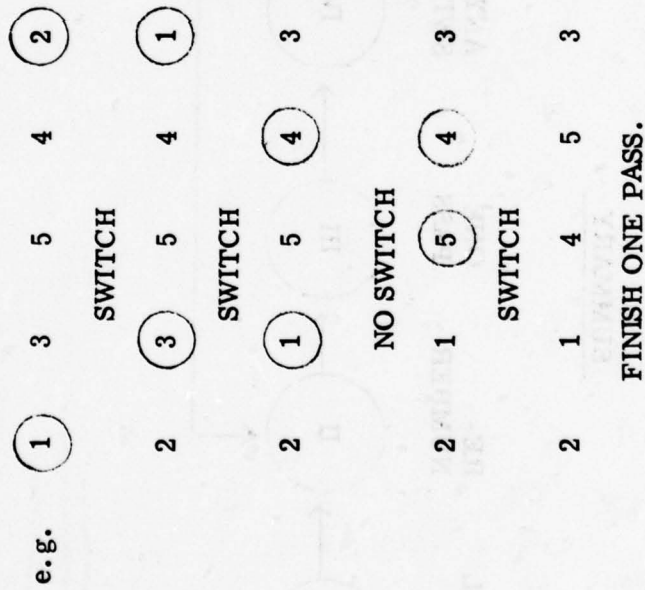


Figure 9. Optimization Routine

IV. IF THERE WERE ONE OR MORE SWITCHES, GO TO II.
IF NO SWITCHES, STOP.

SUMMARY

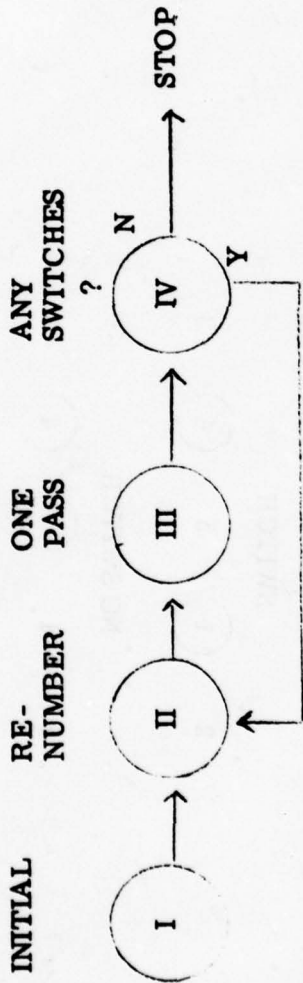


Figure 10. Optimization Flow Diagram

either as "flags" to turn on and off a heater, or can be used with a multiplier to give direct calculation of the heater or flow controlled by the thermostat. A description of this subroutine is included in Appendix A.

Variable Conductance Heat Pipes (VCHP) can be simulated in SINDA by using the temperature dependent conductance option. Using the "SIV" conductor option, the condenser area can be varied with condensate temperature.

The simulation of phase change cooled systems is also a standard subroutine in SINDA. Actually, three subroutines are available to simulate expendable ablation, expendable boiling, and non-expendable melt and freeze types of phase change material. These subroutine descriptions are also included in Appendix A.

Evaluation of temperatures achieved with air having free moisture will be accomplished by an iterative solution to the First Law of Thermodynamics.

$$\begin{aligned} \left[\dot{q} - \dot{m} c_p (T_2 - T_1) \right]_{\text{AIR}} &= \left[(w c_p T)_2 - (w c_p T)_1 \right]_{\text{LIQUID}} \\ &+ \left[(w c_p T)_2 - (w c_p T)_1 \right]_{\text{VAPOR}} \\ &+ \left[(w_2 - w_1)_{\text{VAPOR}} (h_{fg}) \right] \end{aligned}$$

q	= heat input (BTU/hr)	GIVEN
\dot{m}	= mass air flow (Lb _m /min)	GIVEN
c _p	= air specific heat (BTU/lb °F)	GIVEN
T ₂	= exhaust temp (°F)	UNKNOWN
T ₁	= inlet temp (°F)	GIVEN
w _{LIQUID}	= $\dot{m}_{\text{LIQUID}} / \dot{m}_{\text{AIR}}$	UNKNOWN*
w _{VAPOR}	= $\dot{m}_{\text{VAPOR}} / \dot{m}_{\text{AIR}}$	UNKNOWN*
c _{pLIQUID}	= specific heat of liquid (BTU/lb °F)	GIVEN
c _{pVAPOR}	= specific heat of vapor (BTU/lb °F)	GIVEN
h _{fg}	= latent heat of vaporization (BTU/lb)	GIVEN (1025 ± 5%)

$$P_s = (P_c)(10)^{\frac{-x}{T}} \left[\frac{a + bx + cx^3}{1 + dx} \right]$$

where a, b, c, d, P_c, T_c are constants

$$x = T_c - T$$

$$P_s = \text{VAPOR PRESSURE}$$

$$T = \text{TEMP (}^\circ\text{K)}$$

$$P_v = P_s \text{ if } W_{\text{LIQUID}} > 0$$

$$W_{\text{VAPOR}} = .622/(P/P_v - 1)$$

$$W_{\text{LIQUID}} = W_{\text{H}_2\text{O}} - W_{\text{VAPOR}}$$

*CAN BE CALCULATED BY SEPARATE EQUATIONS

2.2.3 Dynamic Environment Software

The capabilities of a number of computer programs were analyzed relative to their applicability to determine the vibration environments at equipment boundaries and the equipment response. All programs that were analyzed are in the public domain of available programs. A summary of the capabilities of the candidate programs along with other comments is given below.

SAP-IV - SAP-IV is a general purpose finite element program that performs static, modal, transient, frequency response and spectrum analysis. The program has an extensive library of elements and has both modal and proportional damping. "The unique feature of SAP IV is that it is the only general purpose program that is simple enough so that users have tried to modify it for their needs.^{5/} Additionally, SAP-IV is currently resident at the WPAFB computer facility at the Avionics Lab.

^{5/} SUM-10, SHOCK AND VIBRATION CONTROLS COMPUTER PROGRAM REVIEWS AND SUMMARIES, Edited by Walter and Barbara Pikley, 1975, Shock and Vibration Information Center, U. S. Department of Defense.

One difficulty encountered with SAP-IV is that it has no random vibration response analysis capability. This difficulty can be overcome, however, by using the frequency response option of SAP-IV with a suitable subroutine ^{6/} that calculates the output power spectral densities (PSD's) and RMS response of specified degrees of freedom for a given input PSD.

NASTRAN - A large versatile general purpose finite element program, NASTRAN, contains extensive linear dynamic analysis capabilities. Due to the versatility of the program and the bulk of the documentation, considerable experience is required for its use. In addition, NASTRAN is very inefficient (costly) for small problems. NASTRAN Level 15 is available at WPAFB on the CDC 6600.

FLEX^{7/} - A WPAFB computer program for vibration prediction of fighter aircraft equipments, FLEX is currently available on the CDC 6600 and Cyber 73 computers. This program predicts vibration spectra at equipment mounting locations on fighter aircraft due to boundary layer (aerodynamic) inputs for straight and level flight, buffet turns, take off, and landing.

This program is very useful in predicting the vibration environments for a large class of aircraft. In addition, several future work areas were listed which means the program will be expanded and improved and that it should be continually supported and maintained by WPAFB personnel.

PURDUE PROGRAM^{5/ 8/} - This program estimates the response of a linearly elastic system under random or deterministic steady state excitation. An approximate method based on relaxation techniques (conjugate gradient method) is used. Natural frequencies and normal modes are not computed. To use this program, the mass damping and stiffness matrices are calculated outside the program and input into it. The most obvious use of the program is to fill the void in the SAP-IV capabilities due to its lack of a random analysis capability.

RSPC^{9/} - A WPAFB computer program for the random response analysis of structures subjected to multiple random loads. To use the program eigenvectors, natural frequencies, generalized forces, masses, and damping are computed outside the program and then read into the program.

^{6/} VIBRATION CONTROL FOR AIRBORNE OPTICAL SYSTEMS, AFFDL-TR-76-145, WPAFB.

^{7/} COMPUTER PROGRAM FOR VIBRATION PREDICTION OF FIGHTER AIRCRAFT EQUIPMENT, AFFDL-TR-77- , WPAFB.

^{8/} A NEW METHOD FOR PREDICTING RESPONSE IN COMPLEX LINEAR SYSTEMS II, J. L. Bagdanoff, et al, Journal of Sound and Vibration, Vol. 53, 1977, pp 459-469.

^{9/} BUFFET DYNAMIC LOADS DURING MANEUVERS, AFFDL-TR-72-46, WPAFB.

No user's manual or other documentation could be obtained for this program although it was possible to get a listing and program deck. It was discovered during the course of this investigation, however, that certain portions of the program had not been successfully debugged and that caution should be exercised in using the program.

SAP V - SAP V is basically SAP IV with added capabilities. Primary among these additional capabilities are the inclusion of a bandwidth minimization routine, a graphics package, and rigid elements. In addition, a 1978 objective of the SAP V Users Group is the addition of a random response analysis option.

The recommended choice for a general purpose FEA (finite element analysis) program is SAP V due to its small size, ease of use, and good static and dynamic capabilities. The proposed inclusion of a random response analysis package remedies the deficiencies of the previous SAP IV program.

NASTRAN has capabilities that exceed those seen as necessary under the present requirement of an optimum design oriented FEA program.

It is also recommended that the FLEX program be included in the ITAD software. The FLEX program, while being limited to one particular class of vehicles (i.e., fighters) represents a significant contribution in the determination of the onboard fighter vibration environment to be used as input to the avionics system.

Rationale for the Adjustment of the Applications Environment Factor

The failure rate model from MIL-HDBK 217B ($\lambda = \pi_1 \pi_q \pi_p (C_1 \pi_t + C_2 \pi_E)$) contains a temperature dependent factor π_t and an application environment factor π_E . The π_t factor is well defined analytically, and its value can be minimized thru the optimum placement of components for maximum reliability. The application environment factor, or π_E as it is called, is a general factor based on vibration levels and other parameters such as sand, dust, humidity, and temperature cycling. The breakdown of what percentage of the π_E factor is due to each parameter is not clearly defined though some work in this area has been undertaken^{10/} and is presently being studied at RADC.

As the current state of the art exists, the exact contribution of the structural reliability to the overall reliability calculation is unknown, and much more study and testing is needed in the area of the structural reliability as it relates to the overall system reliability figure.

It is obvious that a P.W. board or other piece of electronic equipment that has been well designed structurally to minimize vibration effects will be more reliable than one that has been poorly designed.

^{10/} DEVELOPMENT OF HIGHLY RELIABLE SOLDER JOINTS FOR PWBs, Westinghouse Final Report on Contract No. NAS8-21233, 1968.

For this reason it is assumed that: (1) the structural design of a P.W. board affects the total board reliability and should therefore be optimized as much as possible and (2) that this reliability is quantifiable. That is, that it makes up some unspecified fraction of the E factor (14% based on Grumman study) that remains to be determined through future study. For the present, it is sufficient to say that the effect exists, and to arbitrarily pick a percentage (say 15%) as being typical and then proceed from there.

To quantify the failure rate due to the vibration environment, it is first necessary to identify the board failure modes and the factors that affect these failure modes. Some, but by no means all, of the mechanical failure modes are:

- o P.W. board dynamic stresses and fatigue
- o Component electrical lead wire stresses and fatigue
- o Thermal expansion between the board and lead wires
- o Solder joint thermal stress and fatigue
- o Plated through holes thermal stress fatigue

Board Failure Modes

The dynamic bending stresses in a printed wiring board is determined at the resonance by considering the resonant mode shape of the circuit board, its transmissibility and the input load condition. From these factors the maximum bending moment in the board can be determined and hence the dynamic stress. From this data and the board material properties the fatigue life of the board can be calculated.

Component Electrical Lead Wires Stresses

Electronic component parts such as resistors, capacitors, and flatpack I.C.'s are often mounted to P.W. boards by their electrical lead wires. Failures can occur in these lead wires due to the large deflections and bending stresses that are developed as the board bends back and forth. Every time the P.W. board bends, it forces the lead wires to bend since the wires are normally soldered to the board. The greater the PW board deflection, the higher the bending stresses in the lead wires.

Stresses in the component lead wires can be determined by examining the geometry of the electronic component, the fundamental resonant frequency of the boards and the input forcing function. The relative slope of the electric lead wires, where they are soldered to the circuit board, will not change as the board vibrates. That is, the wires remain perpendicular to the board. The wires also remain perpendicular to the component body where the lead joins the body as the body of the component is much stiffer than the lead. Therefore, as the circuit board bends back and forth the

electrical lead wires will bend as shown in Fig. 11. From these curves the stress in the lead wires and the solder can be determined by analyzing the lead wires as a beam.^{10/ 11/}

Thermal Expansion

Due to the mismatch of the expansion coefficients between the P.W. boards and the metals used in the component leads and solder thermal induced stresses arise in the solder joints. These stresses can cause cracking of the solder joints and failure of the components due to cold solder joints. The stresses due to thermal cycling of solder joints has been studied extensively and there exist analytic means to calculate these stresses.^{10/}

Fatigue of Solder Joints

Even when solder joints are properly made, high bending or shear stresses coupled with the stress reversals due to vibration can lead to fatigue failure. Many solder joint fatigue failures are due to a "shear tear-out" type of failure induced by the bending of the electrical lead wires. This type of condition as well as others can be analyzed and then automated.^{10/}

Factors that Affect the Failure Mechanisms

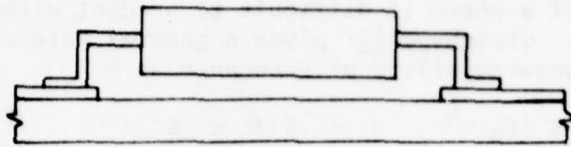
Knowing the potential failure mechanisms that can occur helps the designer to avoid possibly major problems that can occur due to the component layout on the boards. It is necessary, however, for the board designer to be aware of the factors that affect the failure mechanisms. A few of the primary factors will be discussed below:

Probably the greatest factors that affect the mechanical reliability of a P.W. board are the board orientation and geometry. The orientation of the board determines the dynamic loads that the board will see. For this reason it is logical that the plane of the board should be coplanar with the two axes that have the highest vibration input loads and normal to the axis with the smallest dynamic input whenever feasible. The board geometry will determine the fundamental mode shapes of the board which in turn determines the board deflections and also the board and component stress.

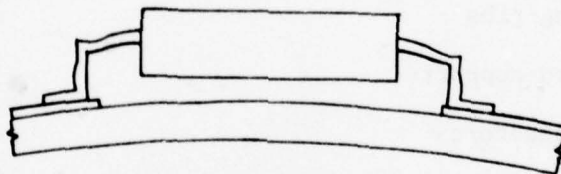
The material properties of the board along with any ribs, heat sinks, or other mechanical stiffeners determine the stiffness of the board. These factors in conjunction with the board geometry and the boundary conditions determine the natural frequency of the board.

The material properties of the electronic components leads as well as the solder used also affect the thermally induced vibrational stresses.

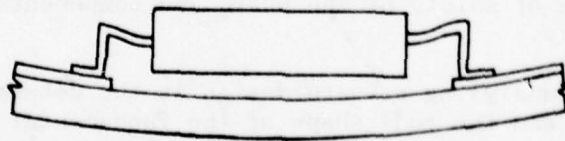
^{11/} VIBRATION ANALYSIS FOR ELECTRONIC EQUIPMENT, Dave Steinberg, John Wiley & Sons, N. Y., 1973



a. Undeflected PW Board



b. Positive Board Deflection



c. Negative Board Deflection

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Figure 11. Deflection of Flat Pack Lead Wires During Vibration

The degree of damping in a P.W. board affects the transmission of the input forcing function to the board and thus has a significant effect upon the dynamic load the board and the components experience. Unfortunately, the transmissibility of a board is difficult to predict without physically testing the board. Steinburg 11/ gives a general rule of thumb for predicting the transmissibility at resonance as

$$Q = K (f_n)^{1/2} \quad .5 \leq K \leq 2$$

where f_n is the natural frequency of the board in Hertz and K is a constant based on the board type and mounting. Some of the factors that affect the selection of K are given below (see Ref. 2 for an extensive list).

- o P.W. board natural frequency
- o Multiple layer boards
- o Heat sink straps
- o Stiffening ribs
- o P.W. board supports
- o Board connectors

With an estimate of the transmissibility and the board natural frequencies, it is therefore possible to calculate for a known forcing function the environmentally induced stresses in the board and the components using standard analysis procedures. It is also possible to computerize this analysis, thus relieving the design engineer of the tremendous volume of calculations. The engineer can thus be made aware of the effect of changes to his board design or layout and any potential problem areas.

Method of Implementation

This section will deal with the steps necessary to calculate the stress levels and margins of safety of the board and components that make up a P.W. board assembly.

The first step in analyzing a board design is the determination of the natural frequency and the mode shape of the fundamental board resonance as in most cases the effect of the fundamental mode usually dominates the other board resonance effects. To determine the board natural frequency, certain information should be defined. This information consists of the following. Board Geometry - The board geometry is basically the shape of the given board - its length, width and thickness, plus any additional structure such as stiffener ribs, heat sinks, multiple layers, etc.

Board Material Properties - The board material properties is a broad term that describes not only the composition of the board itself but also the properties of any ground planes, conformal coatings, stiffening ribs,

etc. that will contribute to the overall stiffness of the board (the effect of the stiffness of any components will be neglected in determining the natural frequency). Needed for the different materials that comprise the board are the modulus of elasticity (E), Poisson's ratio (ν) and the material density (ρ).

Board Weight - The weight of the board must be known to determine the natural frequency. This weight consists of the weight of the board due to the density of the material making up the board as well as the weight of any electrical components or connectors that are mounted on the board. In practice it will be assumed that the total weight of the board is uniformly distributed over the board area and that the location of individual components has no effect on the board natural frequency.

Boundary Conditions - The boundary conditions specify whether an edge of the board is fixed (can't translate or rotate) free (can both translate and rotate) or simply supported (can rotate but not translate) or some combination of all three boundary conditions. An accurate representation of the board boundary conditions is critical in determining both the resonant frequency, mode shape and stress levels in the board and the components. Therefore, the boundary conditions must be determined accurately as even the expected input level can affect the boundary condition. For example, a board edge that can be assumed clamped under a low vibrational input level may become simply supported under a higher input level.

Once the above information has been specified, it is possible to calculate the natural frequency and mode shapes of the P.W. board using one of two procedures. The first procedure is to model the board as an assembly of finite elements and then use the SAP V computer program to determine the mode shape information. The SAP V program will determine the normalized board displacements and rotations at each mode point in the model. This information can be saved for later use in determining the board stress and moments.

The second method consists of using analytic approximations based on the previous given information and an assumed mode shape that satisfies the boundary conditions to obtain the natural frequency of the board. The Raleigh method of equating the board strain energy to its kinetic energy is one method of obtaining the board natural frequency. The assumed mode shapes used in the Raleigh method would be based on trigonometric or polynomial series approximation. Appendix C illustrates the derivation of the board natural frequency based on the Raleigh method.

By using the analytical approximation approach, it is possible to build up a catalog of board mode shapes and natural frequencies based on common board geometries such that the design engineer could quickly make calculations. If a new board configuration came up that could be analyzed by this means its approximation could then be added to the catalog or design table. This approach would eliminate the need for performing a time consuming finite element analysis with each new board configuration.

With the knowledge of the board mode shape and natural frequency, the response of the board to a sine or random loading could be determined. If the SAP V computer program was being used, the board displacements and rotations as well as the bending moments in the board itself could be obtained directly from the program. If an analytic approximation had been used to obtain the board natural frequency, additional calculations would have to be done to obtain the dynamic loads and response of the P.W. board. These calculation, while not as precise as those obtained using the SAP V program, would nonetheless provide adequate information to the engineer regarding the loads in the board.

Finally, by knowing the dynamic loads and moment distributions on a board, the board stress levels and component stress levels can be calculated. These calculation would be implemented as follows. Each component on the board would have its mechanical properties such as component weight, lead wire material, separation, area, and area moments of inertia stored along with its electrical properties. By defining the location and orientation of the component on the board as well as the method of mounting the component, it is a relatively straight forward procedure to calculate the stresses in the component leads and solder joints using the previously determined board deflections and bending moments.

The numerous analytical formulas that have been derived for determining component stress will not be presented here.^{10/ 11/ 12/}

Proposed Technique for Adjusting $\overline{\pi}_E$

While it is obvious that the makeup of the $\overline{\pi}_E$ factor is not known, it is proposed that there be more latitude given to the designer to influence the factor than the fatalistic approach given in MIL-217B. This proposal is based on the previously given arguments regarding effect of board orientation etc. To include the effect of the board design in the selection of the $\overline{\pi}_E$ factor requires that a baseline board and orientation be selected for each of the possible environments based on the statistical analysis of experimental data relating board mechanical failures to the environmental condition. With this baseline board defined, the definition of which would include the board orientation, size mounting conditions, and stiffness, it would be possible to account for the effects of good design practices (and poor ones depending upon the design constraints) to incrementally affect the baseline value of $\overline{\pi}_E$. With this latitude allowed, however, it then becomes possible to optimize the design and layout of a board for both mechanical and thermal reliability. Psychologically, the allocation of credit for sound design would act as an incentive to promote it.

In the case of boards using all the same type of components, e.g., of identical size and construction, the mechanical stress is the same on any

^{12/} FORMULAS FOR STRESS AND STRAIN, Roak, R. J., McGraw Hill, 4th Edition, New York, 1965.

of the components at a given board location. Different components will have different stresses at corresponding locations. Assuming that the calculated stresses can be correlated with values of some portion of the $\overline{\pi}_E$ factor, the board can be divided into 2 dimensional sectors with corresponding $\overline{\pi}_E$ values. For example, in the equation for failure rate

$$\lambda = \overline{\pi}_L \overline{\pi}_q \overline{\pi}_p (C_1 \overline{\pi}_T + C_2 \overline{\pi}_E)$$

the $\overline{\pi}_E$ can be partitioned into

$$\overline{\pi}_E = \overline{\pi}_{E/S} + \overline{\pi}_{E/t}$$

where $\overline{\pi}_{E/S}$ = that portion of $\overline{\pi}_E$ affected by stress

$\overline{\pi}_{E/t}$ = that portion of $\overline{\pi}_E$ affected by other factors

A table of values is then generated relating the x, y location on the PWB with a $\overline{\pi}_{E/S}$ value which can be used in the optimization algorithm.

A similar table is established for each type of component on the board.

In the case where all components on a board are identical in size, construction, and materials (this is rare), the sum of all the $\overline{\pi}_{E/S}$ will be constant no matter what layout changes are made. Thus, only the $\overline{\pi}_{E/t}$ optimization need be considered.

While only an outline of a technique is presented here with a minimum of supporting evidence, it is clear that a large gray area exists that bears extensive investigation.

2.2.4 Reliability Software

For the various reliability capabilities required within ITAD, two existing software programs were investigated: The RADC Optimized Reliability and Component Life Estimator (ORACLE) and the Westinghouse Reliability Computational Program (RELCOMP). Both programs are computerized MIL-HDBK-217B's and both must be modified and recompiled for inclusion as an integral part of the ITAD program. ORACLE is optimized for a time-share operation, particularly with regard to the input and output functions, where the failure rate of a part is sought given certain modifying conditions. RELCOMP, on the other hand, is the more versatile of the two programs, being geared towards processing parts indented to a module, a printed circuit board, a line replaceable unit (LRU), and/or a system. RELCOMP is particularly well structured to allow trade-off studies involving such reliability dependent variables as part quality and cooling provisions. Additionally, Westinghouse is naturally already familiar with the RELCOMP program and in-house funds are used in part to update the program to the latest version of MIL-HDBK-217B and to refine RELCOMP to meet new requirements such as ITAD. For these reasons, RELCOMP was chosen for inclusion in the ITAD program. The following paragraphs describe RELCOMP in more detail.

RELCOMP provides a flexible method of computing the reliability parameters for electronic systems, both existing and proposed. As depicted in figure 12, the program accepts data from either parts lists and application data for existing systems (referred to by Westinghouse as the EDIT file whose development and maintenance are described in figure 13 or engineering data prepared for proposed or developmental systems.

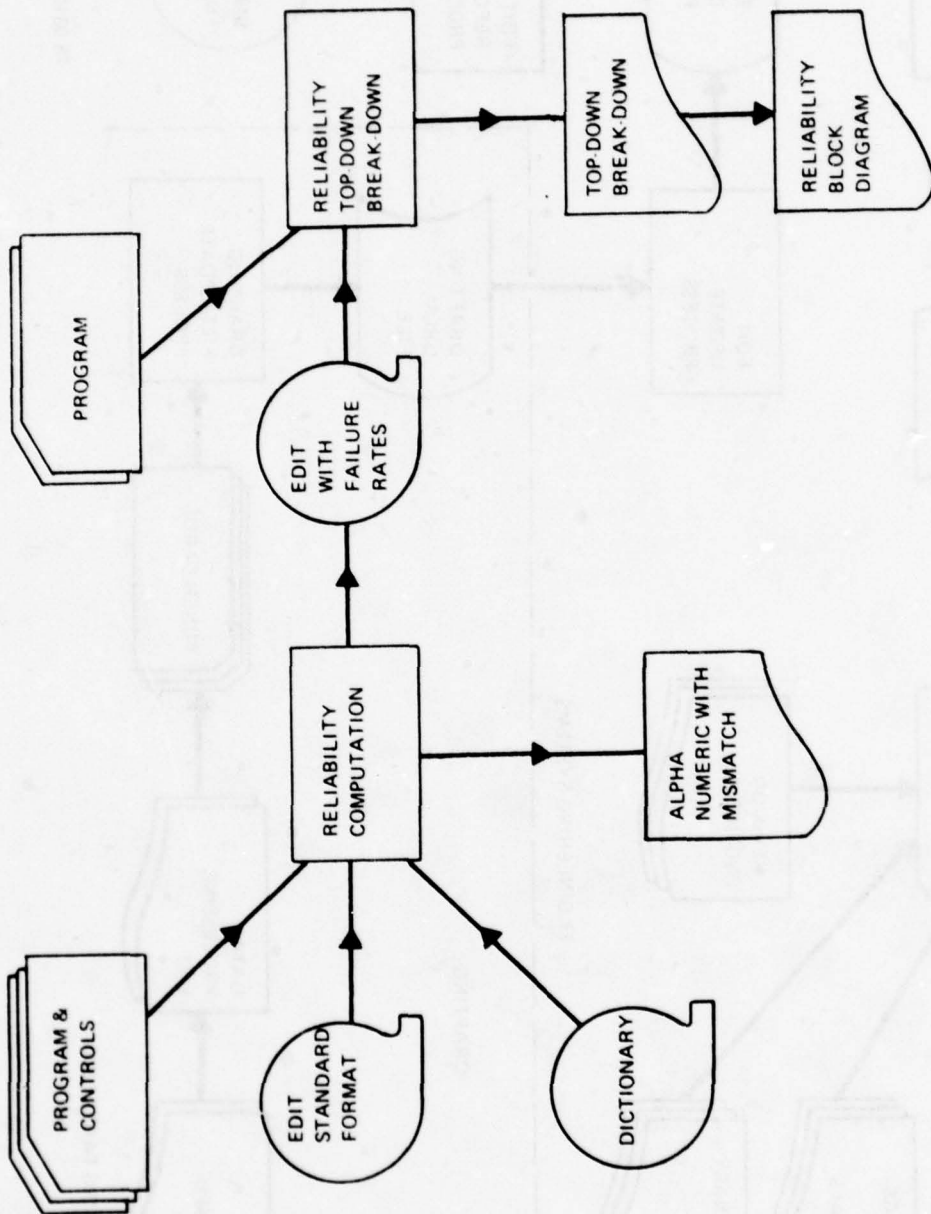
The program orders the data provided (either the EDIT data or engineering data) in part number order and compares it to the reliability dictionary tape (figure 14). The dictionary tape has the descriptive data required to determine the failure rate of each part type. The program then computes the failure rate (λ equal to the number of failures per million hours) for each part application in accordance with the component parts parameters provided by the dictionary. The appropriate application adjustment factors (actual or assumed) are also applied. This data is listed in part number order and indicates where the part is used in the system.

The failure rates are for the most part computed by the methods of MIL-HDBK-217B with all parts not covered by the dictionary tape being listed so that manual failure rate entries can be made.

The part failure rates are combined in accordance with the system configuration and lists all failure rates from the component level to the system level by assembly. The program will take the assembly failure rates and combine them in accordance with the system reliability model to arrive at a system reliability prediction.

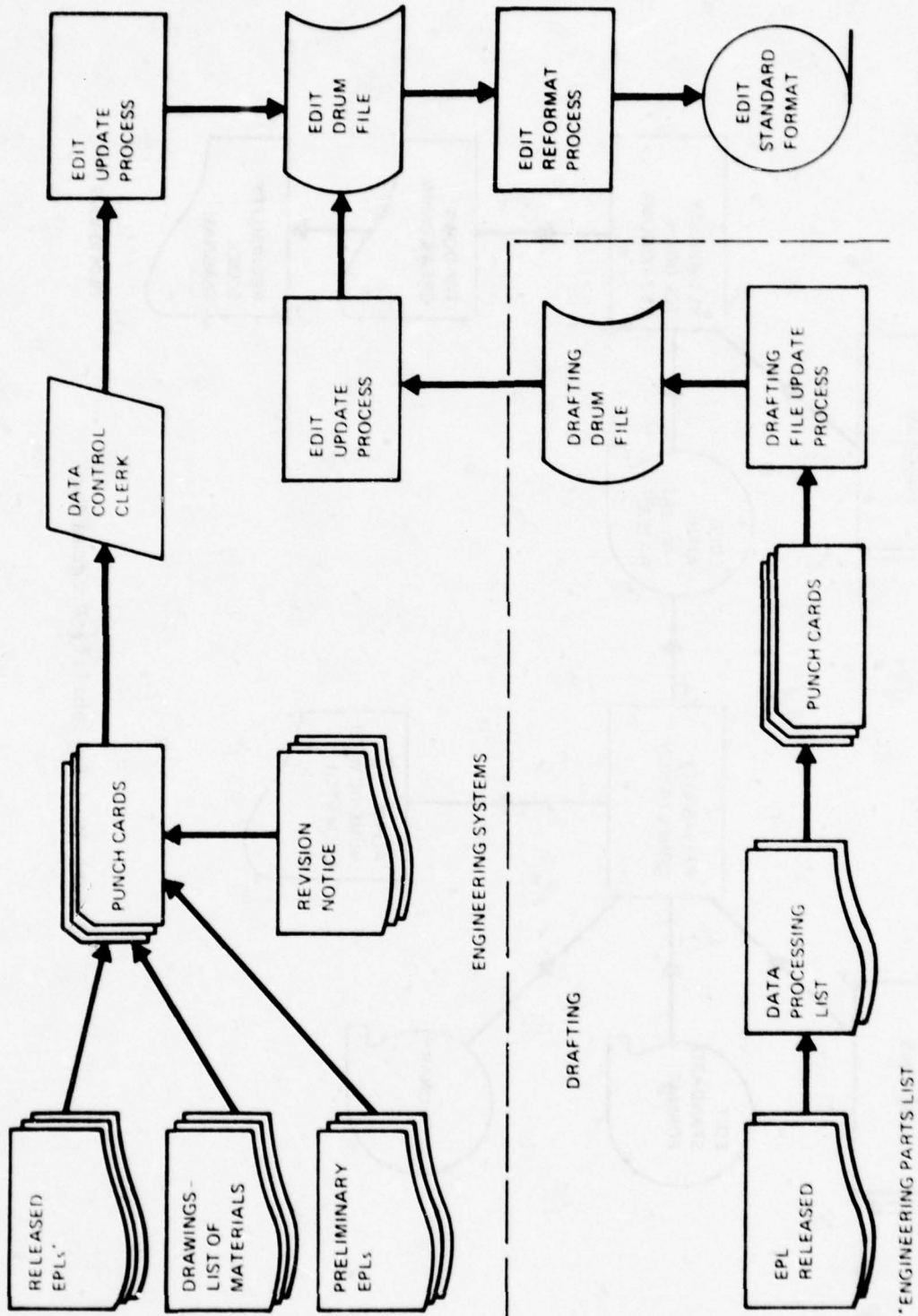
For the purposes of analysis and trade-off studies, the program has the capability of computing for any combination of application parameters (temperature or stress) and providing matrices to illustrate individual or combined effects upon component, assembly, system, or math model.

To integrate RELCOMP with the ITAD system, it is only necessary to interface it with the new Data Base Management System (DBM) which will be used in place of the old EDIT and DICTIONARY files.



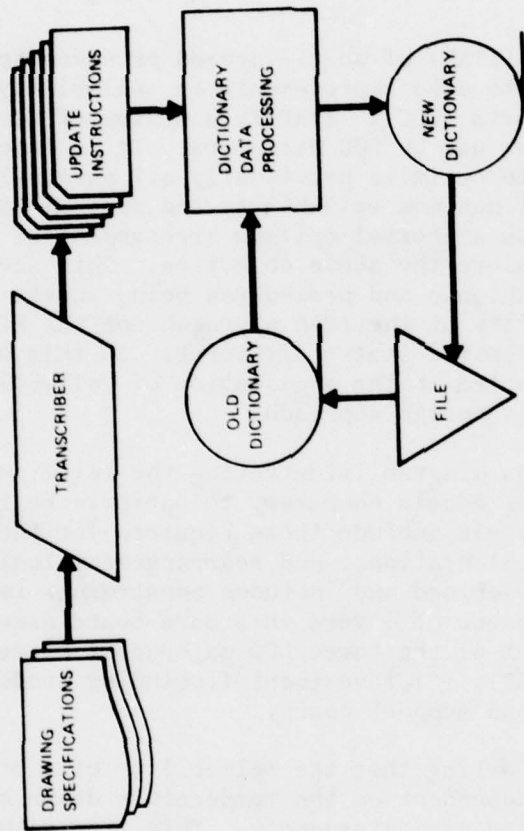
78-0610-VA-9

Figure 12. Reliability Program Run



78 0610 VA 10

Figure 13. Configuration Record (EDIT)



78 0610 VA 11

Figure 14. DICTIONARY (Part Description)

2.2.5 LCC Software

The Westinghouse approach to developing an ITAD LCC software system is based on maximum utilization of existing computer programs. This approach is described in the following paragraphs. In addition to defining a suitable approach, Westinghouse has developed a preliminary ITAD LCC model. This model, which is based on the AFAL EAR LSC model with developments by Westinghouse, is also described and illustrated in this section. This preliminary ITAD LCC model was used as the primary tool to quantify LCC for the design trade studies in task II of this program.

2.2.5.1 LCC Approach

Integrated thermal avionic (ITAD) of multi-layered printed circuit boards (PCB's) is intended to make improvements in reliability and reductions in life cycle costs (LCC). ITAD is a system of computer programs being developed for use by PCB designers. It is intended to provide an effective tool to optimize practically all physical parameters to achieve the objective of maximum reliability and minimum LCC. It results in a PCB design with a thermal optimum arrangement of the parts on a multi-layer PCB to achieve the above objective. This section describes a variety of techniques and procedures being investigated to demonstrate the feasibility of the ITAD approach for the Flight Dynamics Laboratory of the United States Air Force. In this approach, particular emphasis is directed to the application of reliability and LCC computer models for this design approach.

This section includes a flow diagram illustrating the relationship and sequence of various computer models necessary to optimize reliability and LCC. These computer models include those required for thermal calculations, reliability calculations, and rearrangement logic. The LCC optimization loop is described and includes constraints imposed by wire routing, and the number of layers in a bare board assembly. Also described is the impact of the three LCC major cost elements: (1) research and design (R&D), (2) investment (including production costs), and (3) operation and support costs.

ITAD optimizes LCC by considering that the reliability of a printed wiring assembly is highly dependent on the temperature distribution of the components on the printed wiring assembly. This temperature distribution can thus be modified by a rearrangement of components. ITAD rearranges the components in a systematic manner to yield a minimum life cycle cost.

In order to use ITAD to optimize life cycle costs, it is necessary to complete certain prerequisites. The omission of any prerequisite step makes it impossible to produce valid life cycle costs. These steps are listed below in the sequence in which they are performed:

- 1) Circuit Analysis
- 2) System Design Configuration

- 3) Mechanical and Thermal Stress Analyses
- 4) System Reliability
- 5) System Costs
- 6) Maintenance Engineering Analysis
- 7) Optimum Repair Level Analysis and Spares Analysis
- 8) Life Cycle Costs

The relationship between these steps is shown in Figure 15, Relationship Between Decision Making Models and Techniques. Each of these steps is briefly explained in the following paragraphs, including their application in the ITAD approach.

System Design Configuration

The design configuration is the basic starting point. Initially the system design evolves as a block diagram for all functions to be performed in the design. ITAD requires a design configuration down to the level of a PCB with all component parts identified. For this application, it is mandatory that the design configuration be mechanized so that a computer can be used to generate a system top-down breakdown, and an alpha-numeric part number listing of all parts in the design.

System Reliability

The computer program used to calculate system reliability, (either RELCOMP, or ORACLE is based on MIL-HDBK-217B, Reliability Prediction of Electronic Equipment and is used to compute the system reliability for the initial design. In the past the designs for each PCB were accepted once they were successfully tested. This baseline reliability also locked in both the system operational availability and resultant recurring maintenance costs. The ITAD approach further improves the design reliability of each PCB with a thermal optimum arrangement of the parts on a multi-layer PCB.

The reliability model stores a dictionary of unit failure rates for all component parts in the design. The initial run of the model is used to identify any missing failure rates not contained in the dictionary. Such items are added in an update to the dictionary. OEACLE would flag such additions for validation.

Many equations from MIL-HDBK-217B are contained in the reliability model, including the failure rate equations for microelectronic devices such as:

$$\lambda_P = \pi_L \pi_Q \pi_P (C_1 \pi_T + C_2 \pi_E)$$

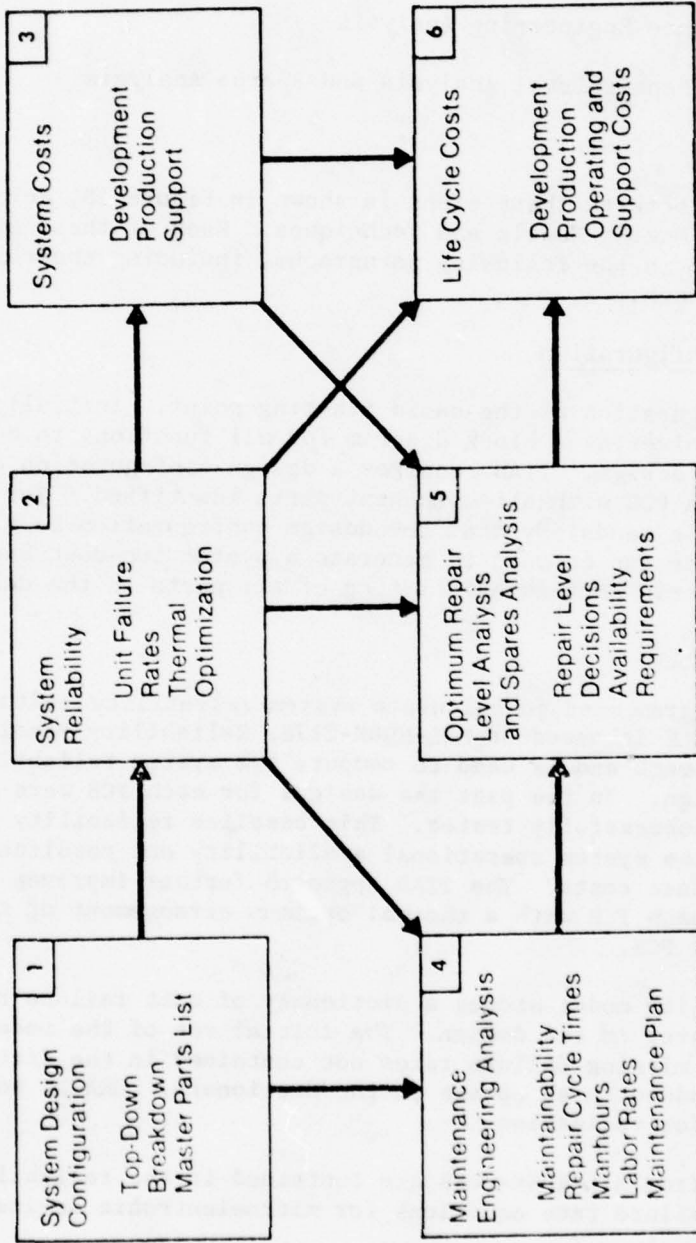


Figure 15. Relationship Between ITAD LCC Decision Making Models and Techniques

where:

λ_P is the device failure rate

π_L is the device learning factor

π_Q is the quality factor

π_P is the device pin quantity factor

π_T is the device temperature acceleration factor

π_E is the application environment factor

C_1, C_2 are circuit complexity factors

The reliability model makes it possible to rapidly mechanize the computation of failure rate predictions for all PCB's and other assemblies in an entire electronic subsystem. This design tool makes it feasible to perform any quantity of reliability calculations required in the ITAD design optimization.

System Costs

The ITAD approach requires the computation of costs for (1) the basic design effort, and ITAD design iterations, (2) production, and (3) support spares. The costs for ITAD design iterations are the only costs which change when the quantity of board layers is unchanged. If the quantity of board layers increases, costs for production and support spares also increase. Therefore, it is desirable to accomplish a thermal optimization of parts without increasing the quantity of board layers. The cost of the basic design effort includes all research, design, test, and evaluation tasks involved in the basic design effort. Production and support spares costs reflect all costs for labor and materials involved in the production effort.

Maintenance Engineering Analysis

The maintenance engineering analysis (MEA) includes the calculations and estimates for all maintenance tasks required to support the avionic subsystem. The MEA includes maintainability elements such as estimates for time, in hours, for access, fault isolation, replacement, repair, and test of a PCB. It also includes estimates of repair cycle times, in months, at both intermediate and depot levels of maintenance. Applicable labor rates, in dollars per hour, for the intermediate and depot levels. The MEA also includes the establishment of the maintenance plan. This has a direct bearing on all support costs.

If the ITAD design involves a change in the quantity of board layers, then related changes, such as mean time to repair, must be reflected in the MEA data.

Optimum Repair Level and Spares Analyses

In the ITAD approach the normal Optimum Repair Level Analysis (ORLA) has been combined with a spares analysis. The ORLA is a computer program designed to make comparative logistic support cost calculations. The result is an optimum repair level decision based on the selection of the overall minimum LSC for (1) repair at intermediate, (2) repair at depot, or (3) discard at failure. Investigations of ORLA decisions for PCB's on many different avionic systems resulted, in almost every case, of repair at depot. Since ITAD involves only the design of PCB's, it was decided to code all PCB's for repair at depot. Thus, for the ITAD approach it is necessary to only code an ORLA decision to avoid the unnecessary expense for actually running the ORLA model for each PCB.

A spares analysis is highly desirable for the purpose of deciding the level of sparing necessary to achieve a required operational availability for the avionic subsystem. The spares analysis involves a plot of spares cost versus operational availability. Figure 16 is a sample characteristic curve of these two parameters. The spares analysis provides the visibility of costs necessary to assure the required quantity of spares at minimum cost. If the baseline operational availability is adequate, it can be inserted as a constraint for the ITAD design. The result is a reduction in spares quantities, and costs, caused by the improved reliability of an ITAD design.

Life Cycle Costs

The Logistic Support Cost (LSC) Model, developed by the U.S. Air Force Logistics Command, was selected to calculate the LSC portion of life cycle costs (LCC). This model was modified to include improvements developed through the efforts of the Avionics Laboratory at Wright P Patterson Air Force Base. For ITAD applications, additional changes, including development costs and production cost equations, were added to create an LCC model suitable for performing ITAD LCC design trade studies. Thus, this ITAD LCC model includes the three major cost elements: (1) research and design, (2) acquisition (production), and (3) support costs.

This LCC model generates the following output reports at the option of the user:

- 1.) Input data file
- 2.) System variables
- 3.) LRU/SRU (PCB) input data

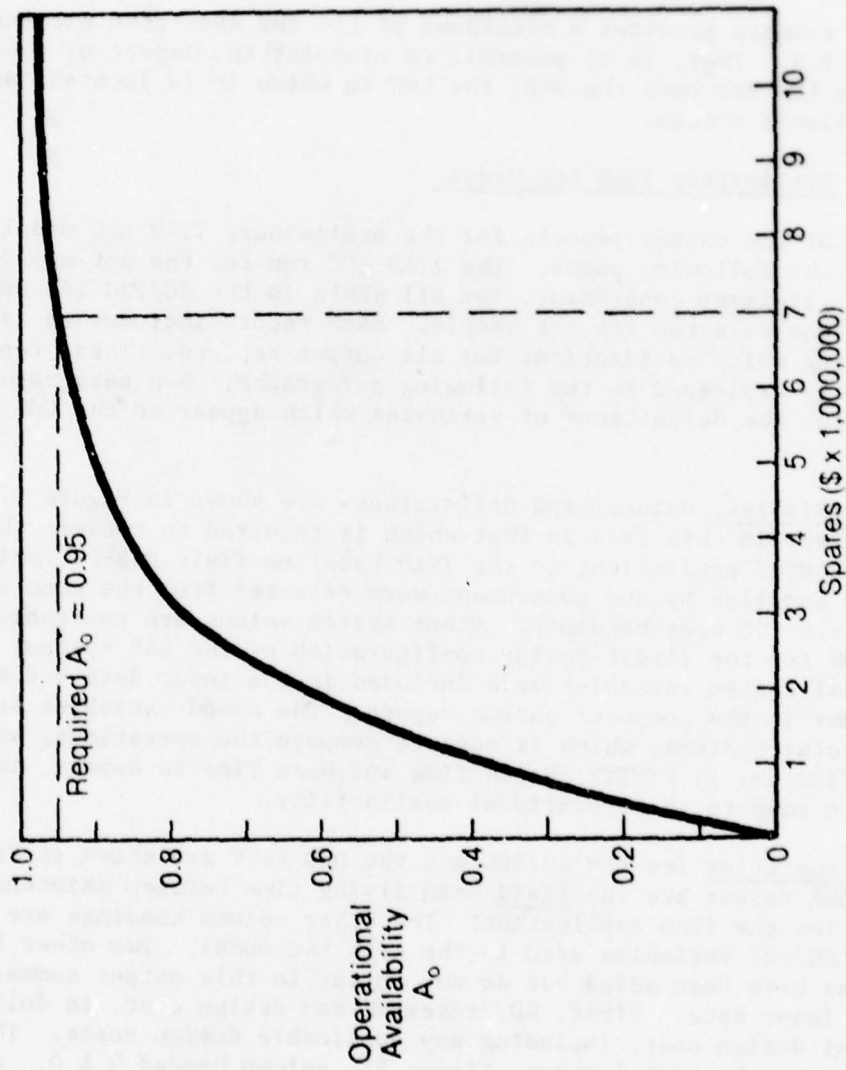


Figure 16. Sample Characteristic Curve of Spares Acquisition Cost vs. Operational Availability

- 4.) Spares summary
- 5.) Availability summary
- 6.) Cost summary
- 7.) Cost summary by percentage

The cost summary provides a breakdown of LCC for each cost element and for each PCB. Thus, it is possible to pinpoint the impact of the ITAD design on LCC for both the PCB, the LRU in which it is located, and the entire avionic system.

2.2.5.2 Preliminary ITAD LCC Model

A sample of the output reports for the preliminary ITAD LCC model is shown on the following pages. The ITAD LCC run for the optimum design, low flow, 12-layer constraint, for all SRU's in the SC/PRG LRU and the DIG ASSY LRU was selected for the sample. Each report includes an identifying heading which is identical for all output reports. These reports are briefly explained in the following paragraphs. See paragraph 2.2.5.3 for the definitions of variables which appear in the LCC output reports.

System variables, values, and definitions are shown in Figure 17. The MTBF divisor in this case is that which is required to convert the original EAR MTBF predictions to the ITAD baseline field MTBF. Variables normally supplied by the government were selected from the same variables in the AFLC LSC user handbook. Other system values are contractor estimates for the latest design configuration of the EAR system. Two additional system variables were included in the input data but do not yet appear in the computer output report. The added variables are: 1) TS, Total Systems, which is used to compute the operational availability for one system, 2) FTMTR, Fetch Time and Mean Time to Repair, is also needed to compute the operational availability.

LRU/SRU variables for the SC/PRG and the DIG ASSY are shown in Figure 18. The MFTBMA values are the field mean flying time between maintenance actions for the ITAD application. The other column headings are identical to the LRU/SRU variables used in the AFLC LSC model. Two other LRU/SRU variables have been added but do not appear in this output summary of the LRU/SRU input data. First, RD, research and design cost, in dollars, is the total design cost, including any applicable design costs. These data do appear in the cost Summary, Figure 21, column headed R & D. Second, UCM unit cost multiplier is used to apply a learning curve for a given production quantity.

ITAD OPT., LOW FLOW, 12-LAYER, ALL SRUS DA & SC/PRG
 *** SCENARIO: 13 BASES, ZOR SYSTEMS, PFFH=16608, TFFH=1604285 ***
 *** UNIT RLD=8600/LRU-SFU, ACQ=UC9.85, XLRU=1605 4-8-78 ***

SYSTEM VALUES (CONSTANT FOR ALL MODULES)

LRU MTRF DIVISOR (FIELD FACTOR)	6.23	
SRU MTRF DIVISOR (FIELD FACTOR)	6.23	
TOTAL COST OF SPECIAL BASE FACILITIES	680.	BA
TOTAL ACTIVE HOURS PER MONTH IN BASE REPAIR	168.	BAA
BASE LABOR RATE PER HOUR INCL OVERHEAD	11.21	RLP
TOTAL NUMBER OF UNIQUE PARTS STORED AT BASES	11.77	CS
TOTAL COST OF COMPUTER SOFTWARE FOR AGE	368842.	DA
TOTAL COST OF SPECIAL DEPOT FACILITIES	3325050.	DA
TOTAL ACTIVE HOURS PER MONTH IN DEPOT REPAIR	168.	DAA
DEPOT LABOR RATE PER HOUR (INCLUDING OVERHEAD)	14.91	DLR
TOTAL LABOR RATE PER HOUR (INCLUDING OVERHEAD)	10000.	FLA
TOTAL COST OF UNIQUE FLIGHT LINE EQUIPMENT	32.80	IAC
INITIAL COST FOR ENTRY OF NEW ITEMS IN GOV INVE	29200.	IMC
TOTAL COST OF INTERCONNECTING HARWARES	32.80	IPC
INITIAL COST FOR ENTRY OF CONSUMABLES	9500.	JJJ
TOTAL NUMBER OF PAGES OF TECHNICAL DOCUMENTS	208.	H
NUMBER OF BASES AT WHICH SYSTEM IS DEPLOYED	13	M
MAN HOURS REQUIRED TO COMPLETE OFF-EO FORM	.24	MRF
MAN HOURS REQUIRED TO COMPLETE ON-EO FORM	.08	MRO
VALUE OF OPTION FLAG FOR COMPUTING SPARES	.00	OPT
OVERSEAS DEPLOYMENT (FRACTION)	.00	CS
PEAK FORCE FLYING HRS PER MONTH (PFFH)	16608.	PFFH
PROJECTED INVENTORY USAGE PERIOD (PIUP IN YRS)	16608.	PIUP
PRODUCTIVE MANHOURS PER YEAR AT PASE	1500.	PHR
PACKING AND SHIPPING COST PER PND (CONUS)	1500.	PMD
PACKING AND SHIPPING COST PER PND (OVERSEAS)	.35	PSC
RECURRING COSTS PER YEAR FOR NON-CONSUM INVENT	.77	PSO
RECURRING COSTS PER YEAR FOR CONSUMABLES INVENT	73.50	PAC
ANNUAL COST PER BASE FOR SCHEDULED MAINTENANCE	73.50	RPC
MAN HRS REQUIRED FOR SCHEDULED MAINTENANCE	25.75	SA
SCHEDULED MAINTENANCE INTERVAL (IN FLYING HRS)	127.03	SMH
MAN HRS TO COMPLETE SUPPLY TRANSACTION FORM	920.00	SMI
COST OF TRAINING ONE MAN AT BASE	.25	SR
COST OF TRAINING ONE MAN AT DEPOT	2640.	TCR
COST PER PAGE OF TECHNICAL DOCUMENT	19500.	TCD
TOTAL FORCE FLYING HOURS FOR LIFE (TFFH)	160.000	TD
MANHRS TO COMPLETE SUPPLY TRANSACTION FORMS (FRACTION)	15000.	TE
ANNUAL TURNOVER RATE AT BASE (FRACTION)	1604285.	TFFH
ANNUAL TURNOVER RATE AT DEPOT (FRACTION)	.330	TRB
OPTION FLAG FOR SPARING	.150	TRD
FLIGHT LINE (SHIFTS/DAY)/(TECHNICIANS/SHIFT)	1.	D
PEAK AVERAGE FLYING HOURS PER MO PER A/C	79.846	2.
		PAFHM

Figure 17. ITAD LCC System Variables

LRU/SRU Spares Summary was added by Westinghouse to provide complete visibility to arrival rates, spares allocations, expected backorders, and weighted MLDT. Figure 19 is a sample of this summary and includes a breakdown of base, depot, and condemnation spares. The arrival rates at the base and depot are indicated by the columns headed STKB and STKD. The sum of base and depot spares indicated by R & D, and condemnation quantities are shown under COND. The TOTAL spares quantity is the sum of (R & D) and COND. Spares quantities were calculated with a Poisson subroutine, and an LRU/SRU expected backorder constraint of 0.05. The columns headed EXPECTED BACKORDER indicate the base (XBOB) and depot (XBOD) expected backorders resulting from the allocation of base and depot spares. Weighted MLDT is the LRU/SRU prorated portion of the system MLDT. The sum of the individual LRU/SRU MLDT values is the system MLDT.

The Availability Summary, Fig. 20 is a brief listing of the calculated variables, MLDT and MFTBMA, followed by the system inherent availability, operational availability, and operational readiness. ITAD design optimizations will always cause an increase in availability when spares are computed with the same expected backorder constraint as used for the baseline design.

AVAILABILITY SUMMARY	
SYSTEM MTR=	1.50
SYSTEM MLDT=	.3669
SYSTEM MFTBMA=	17.39
INHERENT AVAILABILITY=	
OPERATIONAL AVAILABILITY=	.920575
OPERATIONAL READINESS=	.968092

FIG. 20 ITAD LCC Availability Summary

The ITAD LCC Cost Summary (in thousands of dollars), Fig 21 is a listing for each LRU/SRU with columns for the eight LSC equations, Total LSC, R & D, Unit Acquisition Cost, System Acquisition Cost, and Total System (SUBSYS) LCC. The LRU-TOTAL for each column is shown at the bottom line, labeled LRU-TOTAL in the first column, for each LRU. There are two exceptions which will be changed at a future date; the subtotals for LRU Unit Acquisition and System Acquisition appear on the top line for each LRU. The LCC TOTAL SUBSYS is the sum of LOGIST TOTAL, R + D, and SYSTEM ACQUIS. For example, the LCC TOTAL SUBSYS for the DIG ASSY LUR in Fig. 21, is 10461. (LOGIST TOTAL), plus 221.8 (R + D), plus 26845.3 (SYSTEM ACQUIS) for a total of 37528.4 (TOTAL SUBSYS). In addition, the ITAD field MTBF, calculated in the model from the SRU and chassis MTBF's, is shown under the column heading MFTBMA. The last column shows the LRU and SRU unit weights in pounds.

The ITAD LSC Cost Summary by Percentage, Fig 22, shows the LRU LSC percentage for each of the eight LSC equations, and the LSC total. This table is useful in quickly identifying major cost drivers in an electronic system.

ITAD OPT., LOW FLOW, 12-LAYER, ALL SRUS DA & SC/PRG

SCENARIO: 13 BASES, 208 SYSTEMS, PFFH=16608, TFFH=1604285
UNIT REQD=\$8600/LRU-SRU, ACQ=UC*.85, XLRU=.1605, 4-8-7A

LRU/SRU SPARES SUMMARY

LRU/SPU NAME/NO.	APPRIVAL STKR	RATES STKD	PIPELINE & REPLENISHMENT BASES DEPOT B + D COND.	SPARES TOTAL	EXPECTED BACKORDER XB0B XB0D	WEIGHTED MLDT
SC/PRG	.035	2.558	0.	1.	.0345	.001295
CONVTR	.065	4.892	6.	2.	.0021	.000146
CONT PR	.049	7.769	14.	2.	.0048	.000517
OUTP PR	.111	8.642	15.	2.	.0059	.000712
MEM PR	.146	11.333	18.	3.	.0102	.001610
MGTD PR	.133	10.338	17.	2.	.0084	.001215
LOG PR	.108	8.340	14.	2.	.0056	.000663
ALOG PR	.313	24.645	35.	5.	.0443	.015101
TACS SC M	.208	16.336	25.	3.	.0202	.004566
MPSW CNT	.065	4.922	22.	2.	.0034	.000149
TASN CNT	.083	6.464	12.	2.	.0067	.000304
SCCV MEM	.180	14.120	22.	3.	.0153	.003003
TFC SYNC	.041	17.106	13.	2.	.0040	.000399
DIG ASSY	.059	4.458	9.	0.	.0017	.000110
BS PR/EO	.160	12.335	20.	5.	.0121	.002097
BS PS/TM	.108	8.230	11.	4.	.0056	.000660
BS IO/TM	.163	12.567	20.	5.	.0126	.002235
BS PWGLE	.197	15.306	24.	6.	.0183	.003919
BS CSPPM	.044	5.107	17.	3.	.0022	.000160
SP RFOP	.044	5.259	17.	3.	.0036	.000269
SP MAC	.135	10.386	17.	3.	.0088	.001290
SP IFLP	.080	6.027	11.	3.	.0031	.000266
SP TBLP	.084	6.435	12.	2.	.0034	.000313
SP IMG	.187	14.470	23.	3.	.0164	.003322
SP DTA	.041	2.935	6.	1.	.0009	.0001815

Figure 19. ITAD LCC Spares Summary

ITAD OPT., LOW FLOW, 12-LAYER, ALL SRUS DA C SC/PRG P

*** SCENARIO: 13 BASES, 208 SYSTEMS, PFFM=16608, TFFM=1604285 ***
 *** UNIT RLD=86600/LRU--SRU, ACC=UC*.85, XLRU=.1605 4-8-78 ***

COST SUMMARY BY PERCENTAGE

LRU	C1	C2	C3	C4	C5	C6	C7	C8	LOGIST	R + D	UNIT	SYSTEM	TOTAL
SRU	PIPLN	RPLMNT	ON-MNT	OF-PNT	IN-ENT	SUP-EQ	TRNING	MNGMNT	TOTAL	ACQUIS	ACQUIS	ACQUIS	SUBSYS
SC/PRG	1.84	.18	.03	1.30	.09	.00	.14	.08	3.66				
DIQ ASSY	9.93	.65	.13	5.43	.20	.00	.60	.36	17.31				
TOTAL	38.71	5.20	4.79	37.49	1.51	6.69	2.18	3.43	100.00				

Figure 22. ITAD LSC Cost summary by Percentage

2.2.5.3 Definitions of Variables Used in ITAD LCC Model

The following list include all the variables used in the ITAD LCC model and which appear in the LCC output reports used as illustrations in this report.

BA	Cost of new and peculiar base support equipment related to sub-system.
BAA	Total active work time in hours, in the base shop per moth
BLR	Average base level labor rate in dollare/manhours
BMC	Average base material cost per maintenance action expressed as a fraction of the unit cost of the LRU. The material cost shall include the mean dollar value of the consumables utilized in repairing the LRU and any subordiante repairables.
BMH	Average manhours expended at base to diagnose and repair, or attempt to repair, the LRU or SRU
BRCT	Average base repair cycle time in months
BSTOC	Number of unique parts and assemblies which are to be stocked at the base as spares, including standard parts
CS	Cost of software to utilize existing automatic test equipment (ATE) for the subsystem
C1	Initial and pipeline spares cost
C2	Replacement spares cost
C3	On-equipment maintenance or removal costs
C4	Off-equipment maintenance cost
C5	Inventory entry and supply management cost
C6	Support equipment cost
C7	Cost of personnel training and training equipment
C8	Cost of management and technical data
COND	Fraction of depot arrivals condemned
DA	Cost of new and peculiar depot support equipment related to subsystem

DAA Total active work time in the depot per month

DLR Average depot labor rate in dollars/manhour

DMC Average depot material cost per depot maintenance action expressed as a fraction of the unit cost of the LRU. The material cost shall include the mean dollar value of the consumables utilized in repairing the LRU and any subordinate repairables of the LRU.

DMH Average manhours expended at depot to diagnose and repair, or attempt to repair, the LRU or SRU.

DRCT Average depot repair cycle time in months for the LRU or SRU

EBOB Maximum allowable base back order

EBOD Maximum allowable depot back order

FIB Probability that LRU can be fault isolated to an SRU at the base level when the SRU fails and LRU removal results

FLA Cost of unique flight line AGE (common and peculiar) to support the subsystem

H Number of pages of depot level T.O.'s and special repair instructions

IAC Initial inventory management cost to introduce a new coded repairable assembly into the Air Force inventory.

IH Cost of interconnection hardware to utilize existing ATE for the subsystem

IMH Average time in manhours to perform corrective maintenance in place for the LRU or SRU

IPC Initial inventory management cost for consumable items

JJJ Total number of pages of T.O.'s (H & J)

M Number of bases expected to be utilized in the deployment of the system

MFTBMA Mean flying time between maintenance actions for each LRU/SRU

MLDT Mean logistics down time in hours per maintenance action

MRF Average manhours/maintenance action for completing off-equipment maintenance records

MRO Average manhours/maintenance action for completing on-equipment maintenance records

NPLR Probability that an LRU will be fault isolated to a faulty SRU at aircraft due to BITE, CITS, or other detection methods

NRTS Fraction of LRU/LRM removals which, once removed, are expected to be returned to depot for repair

OS Fraction of total force deployed in overseas locations

OST The number of days to order and ship the LRU or the SRU to the depot

PA Number of new "P" coded repairable assemblies within the LRU

PFFH Expected peak force flying hours/month

PIUP Operational service life of the system in years.

PLR Probability that an SRU (LRM) failure can be fault isolated and replaced at the flight line.

PMB Direct productive manhours/man/year at base level (includes both "Touch Time" and time used in getting to and from job, getting tools, AGE, etc.)

PMD Direct productive manhours/man/year at depot level (includes both "Touch Time" and time used in getting to and from job, getting tools, AGE, etc.).

PP Number of new "P" coded consumables within the LRU

PSC Packaging and shipping costs for continental locations in dollars/pound

PSO Packaging and shipping costs for overseas locations in dollars/pound

QPA Quantity of the LRU/LRM contained in the next highest assembly

RAC **Recurring inventory management cost to maintain a repairable assembly in the wholesale system (expressed in dollars/item/year)**

RIP **Fraction of failures for the LRU/LRM which can be repaired in place given that the LRU/LRM has been fault isolated**

RMH **Average time in manhours to remove and replace the faulty LRU/LRM for subsequent report**

RPC **Recurring inventory management cost to maintain a repairable assembly in the wholesale system (expressed in dollars/item/year)**

RTS **Fraction of removals of LRU or SRU which, once removed, are expected to be repaired at base**

SA **Annual base supply inventory management cost in dollars/item/year**

SMH **Average time in manhours to perform scheduled maintenance (including preventive maintenance, preflight, postflight, and periodic inspections of the subsystem)**

SMI **Scheduled maintenance interval in flying hours for the subsystem (including preventive maintenance, preflight, post-flight, and periodic inspections of the subsystem)**

SR **Average manhours/maintenance action for completing supply transaction records**

STKB **Expected number of arrivals at each base**

STKD **Expected number of arrivals at each depot**

TCB **Cost of peculiar training per man at base level (including both instruction and training materials)**

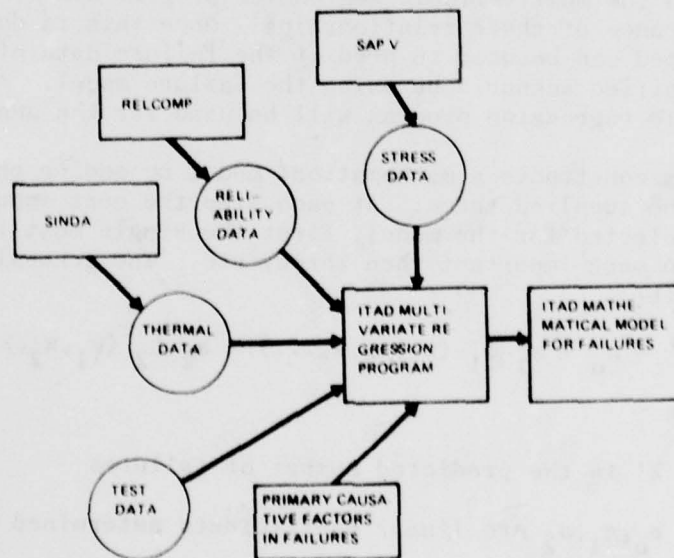
TCD **Cost of peculiar training per man at depot level**

TD **Cost per original page of technical documentation**

TE **Cost of peculiar training equipment required for the subsystem**

TFFH **Expected total force flying hours over life cycle**

TR	Average manhours/maintenance action for completing transportation forms	
TRB	Annual turnover rate for base personnel	
TRD	Annual turnover rate for depot personnel	
UC	Unit cost of LRU or SRU	
W	Weight in pounds of the LRU or SRU	
XBOB	Computed LRU/LRM back orders at base	
XBOD	Computed LRU/LRM back orders at depot	9d
XTYPE	Number of different LRU's/SRU's that can be closely approximated by one given data set. Note: XTYPE is useful during the development phase of a program; when the system configuration is fully defined XTYPE would equal 1.	



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Figure 23. Multivariable Regression Program

2.2.6 Statistical Software

The ITAD regression analysis requires that a mathematical model be formulated for failure data of various electronic equipments. This model in conjunction with the other analysis programs identified in the ITAD study will attempt to provide a quantitative insight into the mechanisms affecting failures and to predict the performance of these electronic equipments in their operational and non-operational environments. The data from this analysis should provide additional tradeoff data in the life cycle cost analysis for ITAD, by highlighting the dependence of failures on the mix and levels of combined environments.

A computer program will be generated to interface with the other ITAD programs and will use the RLSTEP/RLFORL step wise regression program. This program is part of the IMSL library which is available at the AFSC/ASD Computer Center facility at WPAFB. (See Figure 23).

2.2.6.1 Multivariable Regression

Development of the Multivariable regression model requires two tasks. The first task is to determine a set of causal factors which have a significant impact on the failure rate. Existing failure data from CERT tests or from equipment in the field can be analyzed to propose suspected relationships between failures and mixes and levels of environmental factors, and the Multivariable Regression program can be used to determine the significance of these relationships. Once this is done, the model thus developed can be used to predict the failure data of some equipment under a specified scenario by using the failure model. A stepwise multivariable regression program will be used for the analysis.

This program constructs a mathematical model by adding one term at a time from the supplied terms. At each step the most important set of terms are selected for the model, first the single most important, then the two most important then three, etc. The general form of this model would be:

$$\lambda' = a_0 + a_1 \phi_1 (x_1, x_2, x_3, \dots) + a_2 \phi_2 (x_1, x_2, x_3, \dots) + \dots$$

where

λ' is the predicted number of failures

a_0, a_1, a_2 are linear coefficients determined by RLSTEP

ϕ_j are general functions of any of our measurable variables

(temperature, humidity, vibration, etc).

The primary term in this formula is expected to be the failure rate model as proposed in MIL HDBK 217B. The parameters for this model will be generated by the ITAD programs (such as SINDA and RELCOMP) based on the

given scenario.

These parameters will be available to the Multivariable Regression Program thru the ITAD Data Base Manager. For example, suppose we have some failure data for a particular microelectronic board, λ_1 for scenario 1, λ_2 for scenario 2... λ_n for scenario n. These scenarios could be essentially identical boards subject to a CERT test procedure or boards operational in the field. For each scenario compute the ϕ_1 (MIL 217B prediction model) where, say, x_1 would be the temperature from SINDA, at each point in the scenario, x_2 would be the σ_e term etc. A model to explain the failure data

$$\lambda = (\lambda'_1, \lambda'_2, \dots, \lambda'_n) \text{ would be}$$

$$\lambda' = a_0 + a_1 \phi_1(x_1, x_2, \dots, x_n)$$

Once a_0 and a_1 were determined for this board, a new improved prediction (over MIL-HDBK-217B) could be made for this board subject to some new proposed scenario (i.e. 10 years in the field or other).

A second example could be the board layout problem. Let the λ_i be the sum of observe failure data for individual components in a given layout for several scenarios and ϕ_1 be the RELCOMP predictions for these scenarios and the other ϕ 's determined (such as vibration level versus position on the board). Now the model could be used to predict for the life cycle scenario.

Other terms will be studied which are not specifically treated by the MIL 217B term and will be included in the model. Our reference material indicates that some major sources of discrepancy between projected reliability and that realized in the field include, failures related to rapid and slow thermal cycling and temperature extremes in both operating and non operating modes, equipment maintenance, and equipment interfaces or combined environments such as altitude - humidity and humidity with cold temperature. These functions would be expressed:

$$\phi_1 = \frac{\sum_{[T]} \lambda'_p}{T}$$

where T is total life time and [T] is a partition of T into identifiable conditions of MIL 217B

λ'_p is the predicted number of failures for the specific device under MIL 217B

ϕ_2 - is a factor due to rapid thermal cycling for each operating and non-operating condition to be determined empirically as a set of factors similar to π_c . Later, a functional relationship involving, rate of temperature change, amount of change, accumulative number of cycles, duration of temperature extremes, etc. may be found.

ϕ_3 - is a maintenance term based on quality of maintenance personnel, frequency of maintenance, etc. and equipment type.

ϕ_4 - a factor due to interface type and complexity

ϕ_5 - other factors to be determined.

We expect the values of these functions to be a table of factors for each equipment type, based on the conditions of the scenario, similar to the current method used in MIL-HDBK-217B (see Figure 24). In the future, if a mathematical formula can be determined for any of the factors, it would be substituted for the table.

In addition, the partitioning of factors such as π_E (from MIL-HDBK-217B) into effects of humidity and vibration can be investigated by proper selection and partitioning of the test data. For example, if the model for microelectronic components were rewritten:

$$\lambda' = a_0 + a_1 \left[\begin{array}{ccccc} \pi_L & \pi_Q & \pi_P & \pi_T & C_1 \end{array} \right] + a_2 \left[\begin{array}{ccccc} \pi_L & \pi_Q & \pi_P & \pi_E & C_2 \end{array} \right]$$

and were generated by using data under controlled humidity variation with other parameters held constant, the a_2 coefficient would be compared to the model generated by data for full variation of all parameters in π_E .

The regression analysis will have the flexibility to handle additional terms or refined terms including cross product terms, such as humidity-altitude or humidity - cold temperature as more data becomes available and as the ITAD analysis proceeds.

2.2.6.2. Calculation of Means and Variances of Environmental Factors

A computer program will be written to interface with the DBM and arrange data for computation of means, variances, and cross correlation coefficients

π_E , ENVIRONMENTAL FACTOR BASED ON ENVIRONMENTAL
 SERVICE CONDITION

Environment	Symbol	π_E
Ground, Benign	G	0.2
Space Flight	S _F	0.2
Ground Fixed	G _F	1.0
Airborne, Inhabited	A _I	4.0
Naval, Sheltered	N _S	4.0
Ground, Mobile	G _M	4.0
Naval, Unsheltered	N _U	5.0
Airborne, Uninhabited	A _U	6.0
Missile, Launch	M _L	10.0

Figure 24. π_E Factors from MIL-HDBK-217B

for the environmental parameters (such as temperature, vibration, humidity, etc) for a specified scenario. The values of each parameter will be obtained from the ITAD Data Base Manager as a vector, V , of parameters at various points along the scenario.

For each variable of interest, to compute the mean, take samples of each v_j in order of increasing time from each V , a time varying vector with components v_j and use the right end point of $(v_{j_i}, v_{j_{i+1}})$, $v_{j_{i+1}}$ as the value of v_j in the interval, and $(t_{i+1}-t_i)/T$ as the interval length, over t , the total simulation time.

For the mean of v_j use $a_i = \frac{t_{i+1} - t_i}{T}$ then

$$\mu_j (v_j) = \mathcal{E} (v_j) \approx \sum_{i=1}^n v_{j_{i+1}} \cdot a_i$$

This algorithm does not require equally spaced data and it retains information about variable extreme values (as opposed to an average value over the interval).

For a variable such as ambient temperature, a corresponding temperature value for each component must be generated from the mission temperature profile.

The variance of v_j would be calculated as

$$\begin{aligned} \sigma_j^2 (v_j) &= \mathcal{E} (v_j - \mu_j (v_j))^2 \\ &\approx \left[\sum_{i=1}^n (v_{j_{i+1}})^2 \cdot a_i \right] - \mu_j (v_j)^2 \end{aligned}$$

where a_i and μ are defined as above.

In order that a finite number of data points adequately represent a distribution some restriction must be placed on the data points used for V . For example, if the AGREE 9 profile for altitude were used, then:

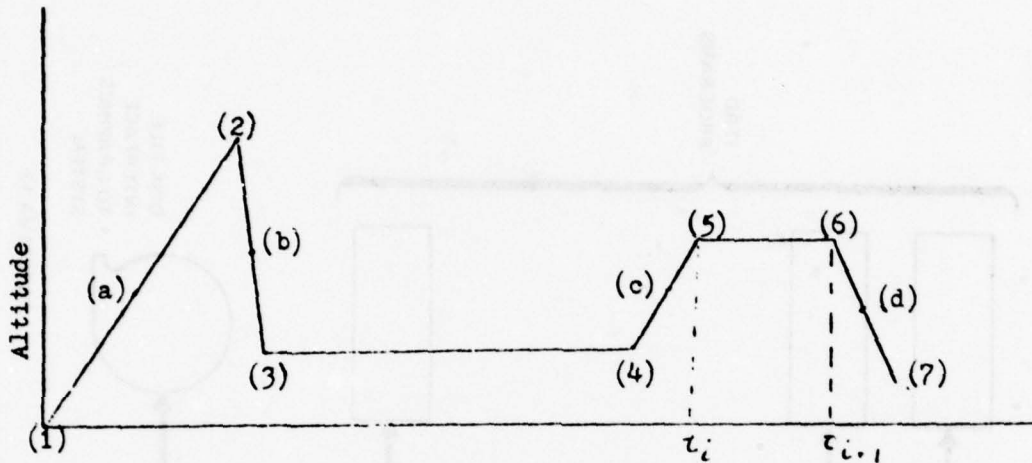


Figure 25. Agree 9 Profile

at least the 7 points shown in 25 must be used. In addition, if the value of v_j changes rapidly, points such as (a), (b), (c), (d) should be included, based on availability, the length of the interval $(t_{i+1}-t_i)$ and the size of the change of v_j from point i to $i+1$.

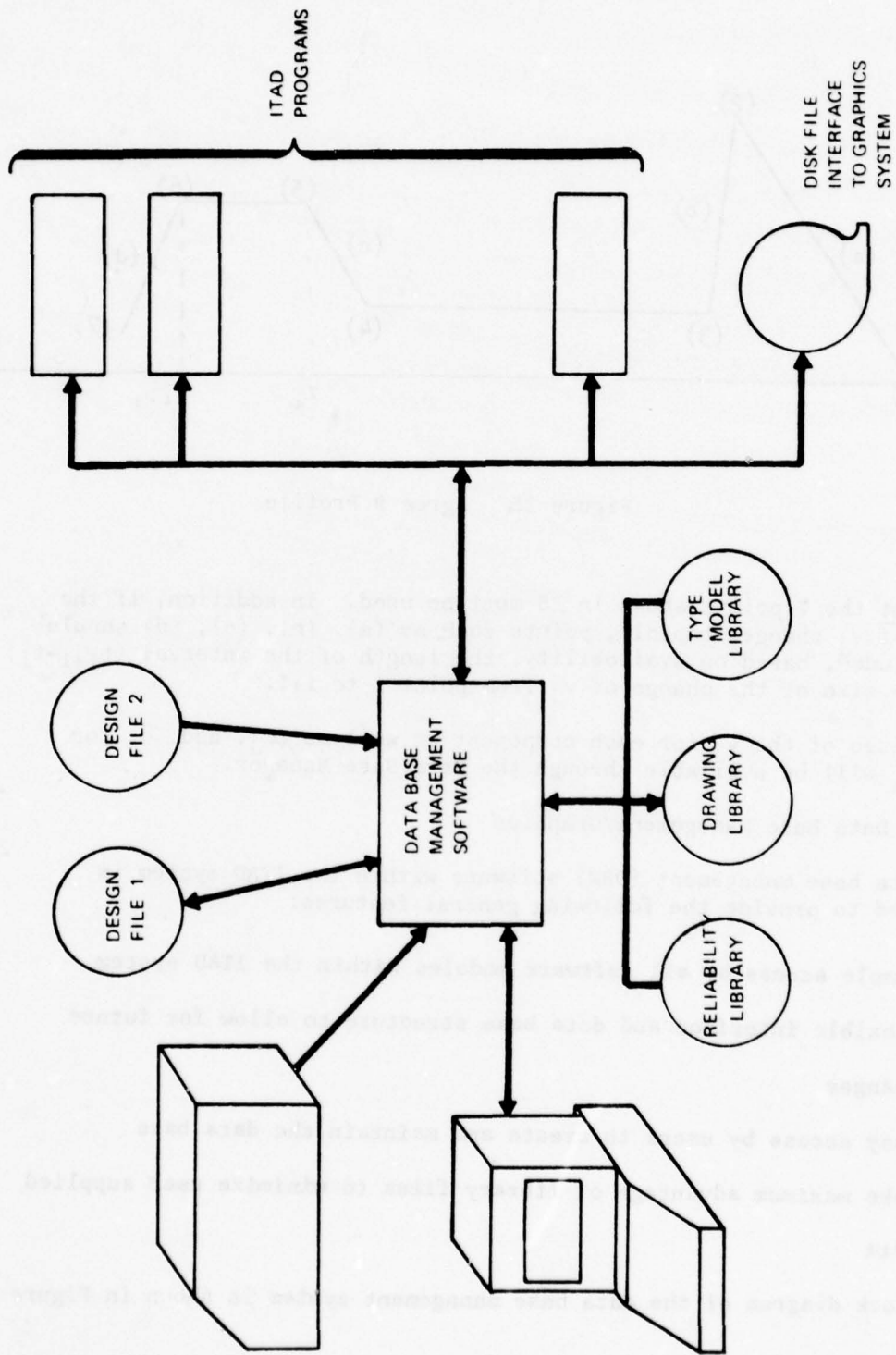
The values of the v_j for each component as well as μ_j , and τ_j for each v_j will be available through the Data Base Manager.

2.2.7 Data Base Management/Graphics

The data base management (DBM) software within the ITAD system is designed to provide the following general features:

- Simple access by all software modules within the ITAD system
- Flexible interface and data base structure to allow for future changes
- Easy access by users to create and maintain the data base
- Take maximum advantage of library files to minimize user supplied data

The block diagram of the data base management system is shown in Figure 26.



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Figure 26. Data Base Management Block Diagram

The user specifies a design for subsequent ITAD analysis by means of two design files designated as DF1 and DF 2 whose contents are defined in Figures 27 and 28.

2.2.7.1 Design File

The structural design file, Design File 1 (DF1), specifies, for each assembly in a system, the specific characteristics of that assembly at the latest point in the design cycle as well as information to customize each usage of a component part of that assembly. The assembly characteristics:

Configuration specification

Life Cycle cost information

Cost, MTBF, MTTR

Drawing information

Lines, circles, test characters (i.e., all graphics necessary to draw the assembly excluding the component parts)

Routing information

Parts area, restricted areas

The assembly header information thus contains all information about the assembly excluding the component parts. The drawing information specifies in the case of a printed wiring board, the board outline, the various tooling holes and text (e.g., the assembly drawing number which is to appear on the silk screen).

The parts list information specifies not only the parts on an assembly but also the customizing information relating to each particular use of a component. The parts lists include:

- 1) Circuit symbol such as U61 and symbol location and orientation
- 2) Part no.
- 3) X, Y, Z, i.e., location of the part origin with respect to the assembly origin.
- 4) Fixed location flag (flag set if part location fixed by designer)
- 5) θ orientation of the part with respect to the coordinate system of the assembly.
- 6) Part power dissipation
- 7) Part temperature

Assembly drawing Number

Configuration information

Revision List

Cost --- LCC information

Failures

Drawing data

Parts list

Item #, CS, P#, XYZO, T,

.

.

.

.

Figure 27. Physical Characteristics (DF1)

Part failure rate
Part environmental factors
The part number used in the parts lists is the name by which the various library files may be accessed to obtain additional, generic data about a part such as:

Assembly drawing number

Signal name - Socket pin list

Signal name - Socket pin list

-
-
-

All library files are accessed by part number and are designed to store related types of information. Thus, the parts drawing file contains graphical data which when extracted for a particular part on a part-number search, provides all data necessary to draw that component. The reliability file contains the coefficients and other parameters which, when combined with the customer's temperature and environmental factors allow failure rates to be calculated and subsequently stored

Figure 28. String List Data (DF2)

Sub-1.3 Design File 2
The second design file specifies electrical information for each printed wire board. The file is accessed by assembly drawing number as shown in Figure 28.

- 8) Part failure rate
- 9) Part environmental factors

The part number used in the parts lists is the means by which the various library files may be accessed to obtain additional, generic data about a part such as:

- 1) reliability factors
- 2) Voltage current ratings/stresses
- 3) Part Thermal resistance, θ_{jc}
- 4) Part size
- 5) Part weight
- 6) Part cost
- 7) Part thermal capacity

2.2.7.2 Library Files

All library files are accessed by part number and are designed to store related types of information. Thus the parts drawing file contains graphical data which when materialized for a particular part on a particular assembly specifies all data necessary to "draw" that component. The reliability file contains the coefficients and other parameters which, when combined with the customizing temperature and environmental factors allow failure rates to be calculated and subsequently stored back in the design file for use by other programs in ITAD.

2.2.7.3 Design File 2

The second design file specifies electrical information for each printed wire board. The file is accessed by assembly drawing number as shown in Figure 29.

Assembly drawing # X

Signal name i socket pin, socket-pin...

Signal name j socket-pin...

.
.
.

Assembly drawing # Y

.
.
.

Figure 29 - DF2 Format

The data in design file 2 for a given assembly is organized by signal name or net and lists all the component socket pins having that particular signal name where socket is a circuit symbol designator such as U39 and pin refers to a pin number on that socket.

In order to explain the file structure further, the interfacing mechanism to OPTEMP, wire routing (PCPRA) and an interactive graphics system will be presented.

2.2.7-4 OPTEMP Interface

The component placement optimization process requires P.C. board data, component data, and cooling data. The steps listed below define in general terms how this data is obtained assuming initiate run.

- 1) Read system name
- 2) Read PC board assembly number: PCN (from user)
- 3) Access design file 1 (DF1) to get data for PCN

PC Board Data

- 1) Read board dimensions
- 2) Read routing data to get parts placement area

Component Data

1) Read parts list for PCN to obtain:

- a. Part number
- b. Circuit symbol
- c. Part location
- d. Fixed location flag

NOTE: If the flag is not set, then the part location information, if present, implies initial location. If the flag is set, the location must be present and preserved by OPTEMP.

- e. Orientation
- f. Failure rate

2) Access the parts graphic library for each part to obtain component size information

Cooling Data

1) Read user supplied cooling parameters and boundary conditions

The results of an OPTEMP run are updated component location information temperature and failure rate which are stored in DF1 overwriting the initial information.

2.2.7.5 PCPRA Interface

The wire routing process requires PCB data, component data and inter-connection information. The following steps are required:

Initiate Run

- 1) Read system name: DF1
- 2) Read PC board assembly number: PCN
- 3) Access design file DF1

PCB Data

- 1) Read DF1 to get routing area information including restrictions such as "keep out areas"

Component Data

- 1) Read parts list to get:
 - a) Part number
 - b) Circuit symbol
 - c) Part location
 - d) Part orientation
- 2) Read reliability library for each listed part number to get part type (5400, 54161, etc.), package type (DIP) and number of pins
- 3) Create the "BUCKET Category" which relates circuit symbol to type (5400 U31, etc.) for input to PCPRA
- 4) Read the TYPE-MODEL library for each component type to create the "TYPE-MODEL Category" which relates type to component pin pattern template. (All 14 pin dips have one pin pattern, 16 pin dips have another, etc.)
- 5) Read the GRAPHIC DATA library for each model type to create the "MODEL Category" specifying the pin locations, with respect to the model origin.

- 6) Read design file 2 for PCN to get the interconnect information in terms of signal name, circuit symbol and pin number to create the "STRING LIST Category" for PCPRA.

Thus all information required for running PCPRA can be obtained from the design files and the generic data library files.

Graphic Interface

The data necessary to drive an interactive graphics systems such as STAGING is obtained from the ITAD design and library files by the following steps.

- 1) Read system name: DFI
- 2) Read assembly number: PCN
- 3) Access DFI for PCN
- 4) Read and output assembly drawing information
- 5) For each item in the assembly parts lists to obtain
 - a) Part #
 - b) Part location
 - c) Part orientation
 - d) Circuit symbol
- 6) For each part # read the graphic library file and perform the following steps:
 - a) Read the graphic information for a part
 - b) Calculate the absolute coordinates for each graphical primitive (lines, circles, etc.) by applying the translation and rotation specified in the assembly parts list.
 - c) Output the "materialized" data.

2.2.7.6 Data Base Management Software

A variety of approaches to providing the software capable of handling the wide range of ITAD requirements have been considered. The study concluded that the required DBM software is commercially available with sufficient capability, documentation, availability, and maturity. One such system, system S2000 from Management Resources, Inc., examined in depth, can elegantly handle the storage, maintenance, retrieval, and interfacing requirements. S2000 currently requires 52K₁₀ words of core storage, but MRI is currently developing an overlay version which should substantially reduce this number. The entire ITAD system will require approximately 60K₁₀ words if the overlay version is not used. If it is used, SINDA is the program controlling memory size. The memory required for SINDA depends on the size of problem for which SINDA is used. For most requirements, 40K₁₀ is adequate.

The VENUS data base management system currently installed at WPAFB was also examined but found to be unacceptable since no provision exists for software interfacing with FORTRAN programs.

The second viable possibility concluded from the study is that the DBM requirements can be provided by writing a new software system specifically designed for ITAD. In so doing advantage can be taken of known structural relationships and interfacing requirements, thus resulting in a more efficient solution both in terms of compactness of storage and computer run time. The disadvantage is the longer term maintenance considerations given the anticipated evolution of ITAD with associated modifications to the DBM and the significantly higher initial cost. The current price of S2000 is \$45,000 without any discount which will be available through 1979. It is estimated that the custom solution will be five times more expensive than the S2000 solution.

Since the S2000 system can adequately meet the requirements of ITAD and has the flexibility to meet future requirements, at much less cost than a custom system, it is recommended that S2000 (available for the CDC hardware) be used as the ITAD Data Base Management system.

2.2.8 Task I-Summary and Conclusions

During Phase I of Task I a study was conducted to determine which computer site was most applicable to the ITAD system. The site chosen is the ASD CDC-6600 at WPAFB. Before the wire routing program, PCPRA, at AFAL is converted to the CDC-6600, a study will be conducted to gain experience with the sensitivities of those parameters affecting LCC.

The parameters affecting LCC which must be optimized are, quality of component parts, number of PWB layers, cost of wire routing, and reliability. In the initial (Task II) study of a coplanar cooled PWA, based on 208 system with a ten year life, there are indications that the number of layers must be minimized even at large increases in the cost

of wire routing. This may not be true for systems used in small quantities, but for these systems LSC gains through increased reliability will also be small.

Whether the number of layers is a reasonable optimization parameter can only be determined by trial optimization of a larger sample of systems than has been undertaken in this study. An algorithm has been presented which will optimize all of the above parameters based on the development of an economical (in real time and computer time) method of estimating the number of layers and routing difficulty. A larger scale study might indicate whether or not the number of layers need be considered. If not, savings in development of the wire routing cost estimating routine will be seen. Also a savings in computer time to optimize the PWA each and every time ITAD is used could be significant.

Several computer programs have been recommended to accomplish various functions of the ITAD system and are described in detail. These programs are listed in Table 3. In addition, where existing software is not available and existing knowledge and techniques allow, algorithms have been defined to accomplish these tasks. The algorithms presented allow the calculations shown in figure 30.

Algorithms to rigorously define wire routing cost estimation and π_E variation, have not been presented due to a large unknown area. The estimation of the number of layers of printed wiring required to route a PWB and the calculation of actual costs to do this for various numbers of layers has not been attempted in a completely automated manner. Although it is not beyond the state of the art to do this, it was beyond the scope of this study to attempt to define this algorithm.

An outline of a scheme for affecting the π_E factor used in present reliability calculations has been presented. However, due to the uncertainty surrounding the exact nature of this parameter, a precise optimization algorithm would be conjecture.

Table 3. RECOMMENDED COMPUTER PROGRAMS

Thermal

SINDA

ØPTEMP

Structural

SAP V

Reliability

RELØMP

Statistical

RLSTEP/RLFØRL

Data Base Management

MRI, S2000

Life Cycle Cost

AFLC LSC

Wire Routing

PCPRA

Graphics

STAGING

1. LCC Optimization of PWA's
2. Reliability Optimization of Conduction Cooled PWA's
3. Calculation of Temperatures for PWA's Cooled by:
 - conduction
 - natural convection
 - forced convection
 - heat pipes
 - thermoelectric devices
4. Calculating Equivalent Temperatures
5. Optimizing PWA's with Respect to Each Other
6. Taking into Account Free Moisture in Cooling Air
7. Calculation of Means and Variances of Environmental Factors
8. Interactive Graphics Interface

Figure 30. Defined Algorithms

SECTION III

TASK II- OPTIMAL CIRCUIT BOARD DESIGN AND COST STUDY

A design and cost study was undertaken for a pair of multilayer coplanar air-cooled circuit boards used in 12 locations in the Electronically Agile Radar (EAR) built by Westinghouse. This study has given a preliminary measure of the life cycle cost payoff resulting from the optimization of component arrangement on the printed circuit boards.

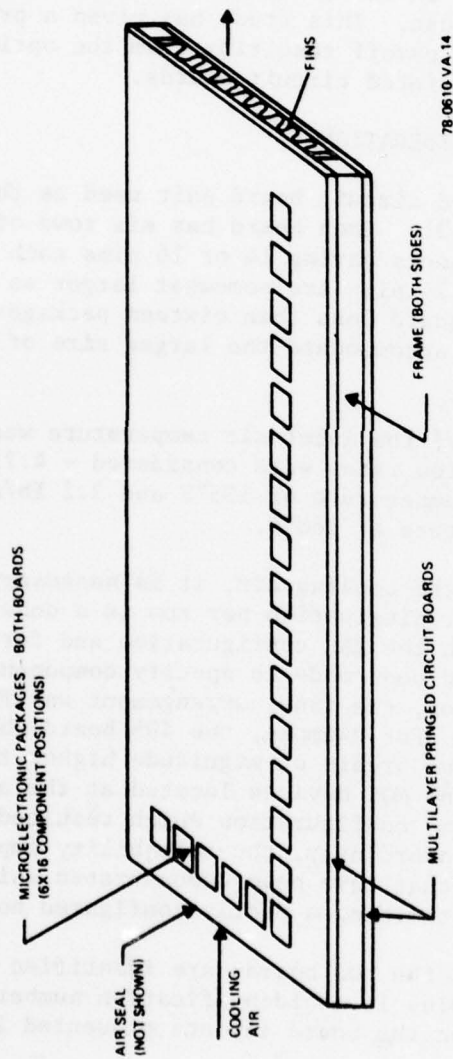
3.1 THERMAL/RELIABILITY CONSIDERATIONS

The construction of the printed circuit board pair used as the basis for this study is shown in Figure 31. Each board has six rows of components. Up to sixteen flat pack components having 14 or 16 pins each can be located in each row. Flat packs with 24 pins are somewhat larger so that rows with these components will accommodate less than sixteen packages. In addition, only four of the six rows can accommodate the larger size of the 24 pin flat packs.

For the purposes of this study, the inlet air temperature was held constant at 85°F. Two different air flow rates were considered - 4.75 lb/min/kw which results in an exhaust temperature of 135°F and 3.2 lb/min/kw which results in an exhaust temperature of 160°F.

For effective utilization of the cooling air, it is necessary to group the components such that the power dissipation per row is a constant for each board. This was done for both the EAR configuration and for the ITAD configuration. No attempt had been made to specify component locations for the EAR configuration. However, the final arrangement was fairly good from a reliability viewpoint. For example, the 408 board which has 18 MOS devices with a failure rate two orders of magnitude higher than most other devices was arranged with these MOS devices located at the air inlet region of the board. This is the same configuration which resulted from the ITAD optimization of the board. Accordingly, the reliability improvements and life cycle cost improvements that have been demonstrated using ITAD would be even more dramatic when optimizing a poorly configured board.

Components located on each of the two boards are identified in Tables 4 and 5. Included in these tables is an identification number which can be used to identify components on the board layouts presented later.



78 0610 VA 14

Figure 31. Multilayer Coplanar Air Cooled Circuit Board Pair

The arrangement of components for maximum reliability (minimum failure rate) was accomplished by the computer program OPTEMP. This program was developed at the Air Force Flight Dynamics Laboratory, Wright-Patterson AFB and furnished to Westinghouse for this study. Component failure rates are calculated by the equation $\lambda = F e^{\alpha T}$ which for the temperature range of this study is a good approximation of the temperature sensitive part of the failure rate defined in MIL-HDBK-217B. The coefficients F and α are constant for each component. Inspection of Tables 4 and 5 reveals that the value of F is different for most all components and that only 3 values of α were encountered. One of the 3 values is associated only with a resistor pack used once on each board. Figure 32 provides a measure of the accuracy of the failure rate approximation $\lambda = F e^{\alpha T}$ for monolithic micro-electronic devices. The semi-logarithmic graph used in this figure will result in a straight line for an exponential such as $F e^{\alpha T}$. The two solid curves are based on MIL-HDBK-217B. The dashed lines represent the approximation used in OPTEMP with the values of F and α evaluated based on data at 40°C and 90°C. The approximation is within 15% of the MIL-HDBK-217B values over the temperature range of 30°C to 100°C. The majority of component temperatures were found to be in this range.

Several component placement techniques were investigated. These included: 1) unconstrained component arrangement, 2) 100% specified component arrangement for optimum reliability, 3) zone specified component arrangement for semi-optimum reliability, and 4) constant junction temperature arrangement. The last technique (constant junction temperature arrangement) is one which arranges components in a manner which minimizes the temperature spread in each row. This technique was found to yield a poorer reliability than the original arrangement. Accordingly, no life cycle cost studies were undertaken for this placement technique.

Complete life cycle cost studies were undertaken for the first three placement techniques. The unconstrained component arrangement forms the baseline for the life cycle cost studies. This configuration shown in Figures 33 and 34 is the one actually used for the EAR radar which had no thermal placement requirements. The 100% specified component arrangement represents a maximized reliability configuration as determined by OPTEMP. This configuration is shown in Figures 35 and 36. The zone specified component arrangement techniques was conceived in response to anticipated wire routing problems with the 100% specified case. The zone arrangement technique divided the board into zones and allowed components in a zone to be swapped with any other component in that zone. This was allowed on a row by row basis only. Component swapping from one row to another was not allowed because this could cause a heat imbalance in the rows. The configuration resulting from this technique is shown in Figures 37 and 38. Figures 39 and 40 illustrate the actual swapping within the specified zones.

Table 4. 407 BOARD COMPONENT INFORMATION

Identification Number	Quantity	Generic Number	Power (watts)	F	α	λ @ 149°F* (Failures Per Million Hrs.)
1	2	54S08	.125	.00031	.0234	.010
2	1	54S86	.250	.00031	.0234	.010
3	1	54S74	.150	.00066	.0234	.022
4	1	54S04	.114	.00041	.0234	.013
5	2	54S00	.075	.00012	.0234	.004
6	1	54S20	.038	.00021	.0234	.007
7	4	54LS04	.012	.00041	.0234	.013
8	1	54S37	.165	.00031	.0234	.010
9	1	54S153	.225	.00080	.0234	.026
10	12	25S09	.375	.00143	.0234	.046
11	3	25S10	.525	.00119	.0234	.049
12	3	54157	.150	.00036	.0234	.012
13	1	54LS283	.103	.00138	.0234	.045
14	4	54S174	.450	.00138	.0234	.045
15	1	54S151	.225	.00083	.0234	.027
16	1	RP1K	.187	.22533	.0045	.441
17	1	54S138	.245	.00076	.0234	.025
18	3	54LS174	.080	.00138	.0234	.045
19	2	54368	.295	.00050	.0234	.016
20	6	54S181	.600	.00200	.0234	.065
21	15	25S05	.600	.00250	.0234	.082

*Temperature related failures only.

Table 5. 408 BOARD COMPONENT INFORMATION

Identification Number	Quantity	Generic Number	Power (watts)	F	α	@ 149°F* (Failures Per Million Hrs.)
1	8	54LS04	.012	.00041	.0234	.013
2	3	54S74	.150	.00065	.0234	.021
3	2	55363	.237	.00031	.0234	.010
4	1	54S00	.075	.00012	.0234	.004
5	1	54S08	.125	.00031	.0234	.010
6	1	54S37	.165	.00031	.0234	.010
7	1	54S04	.114	.00041	.0234	.013
8	5	54S174	.450	.00138	.0234	.045
9	6	54LS153	.031	.00080	.0234	.026
10	12	82S11	.600	.01227	.0234	.401
11	1	54S157	.180	.00076	.0234	.025
12	1	54LS157	.049	.00089	.0234	.029
13	1	54S153	.225	.00080	.0234	.026
14	8	54LS174	.080	.00138	.0234	.045
15	1	RP1K	.187	.22533	.0045	.440
16	6	25LS09	.055	.00143	.0234	.047
17	3	25S09	.375	.00143	.0234	.047
18	2	54367	.325	.00050	.0234	.016
19	18	4060	.500	.00888	.0397	3.291

*Temperature related failures only.

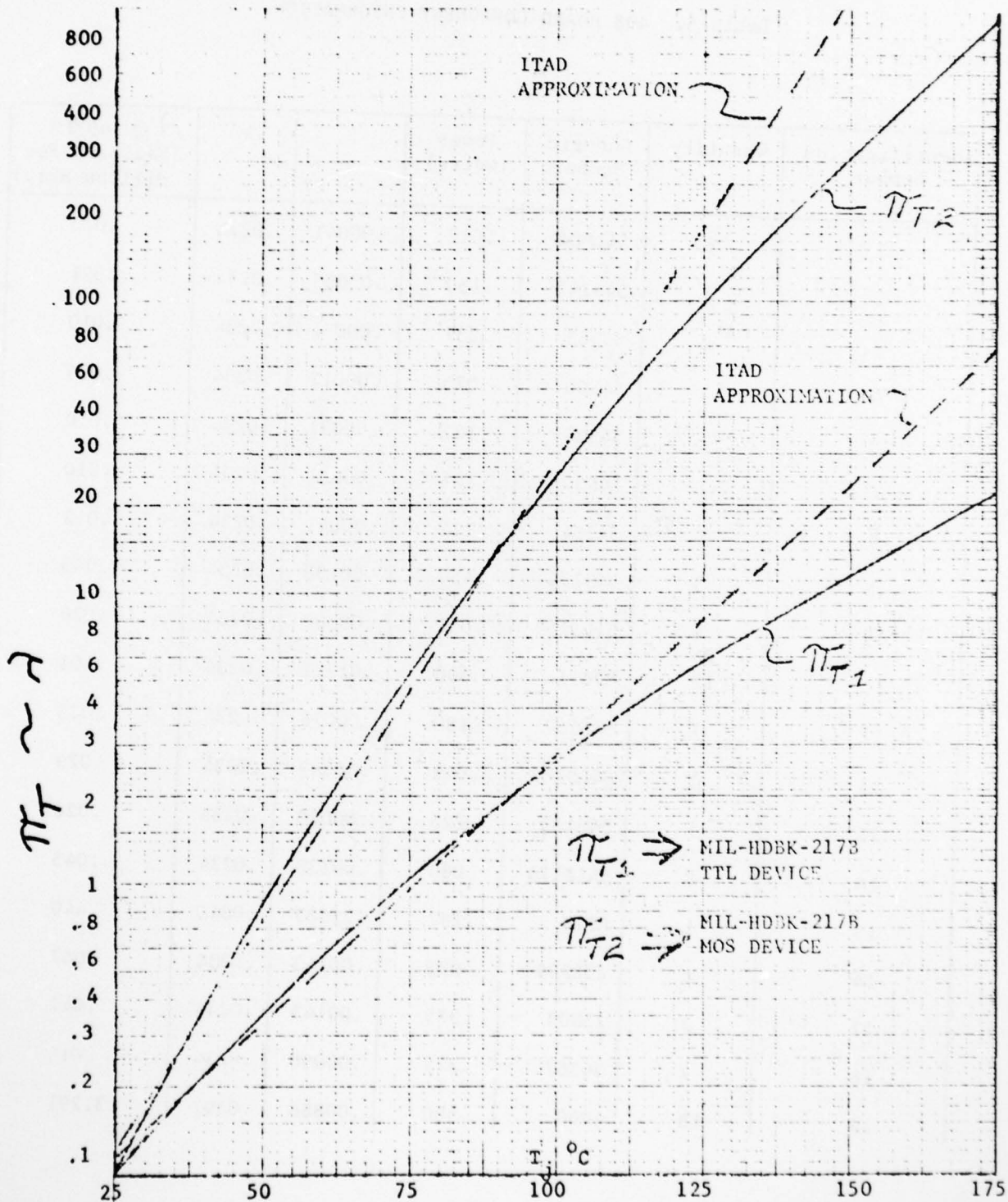
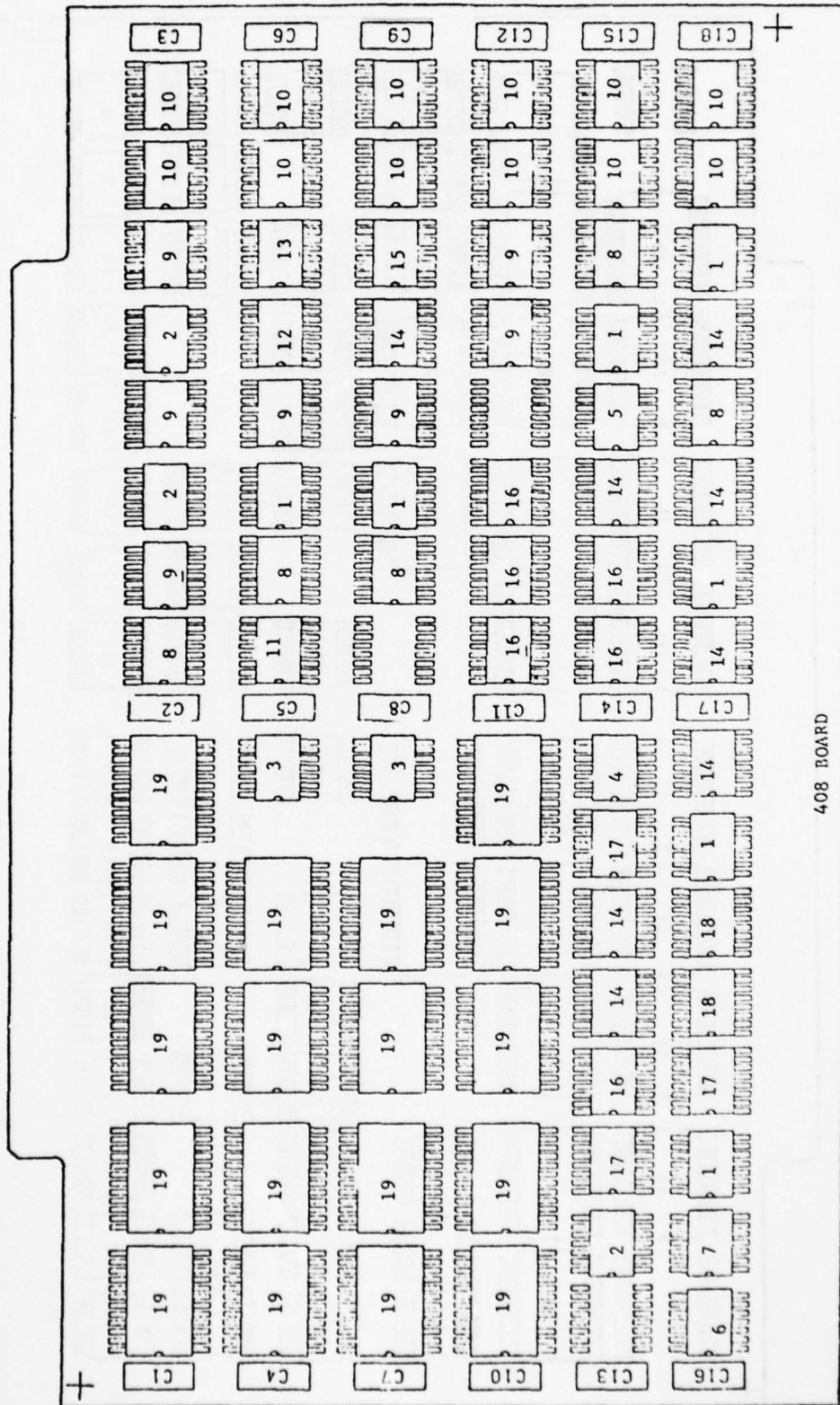
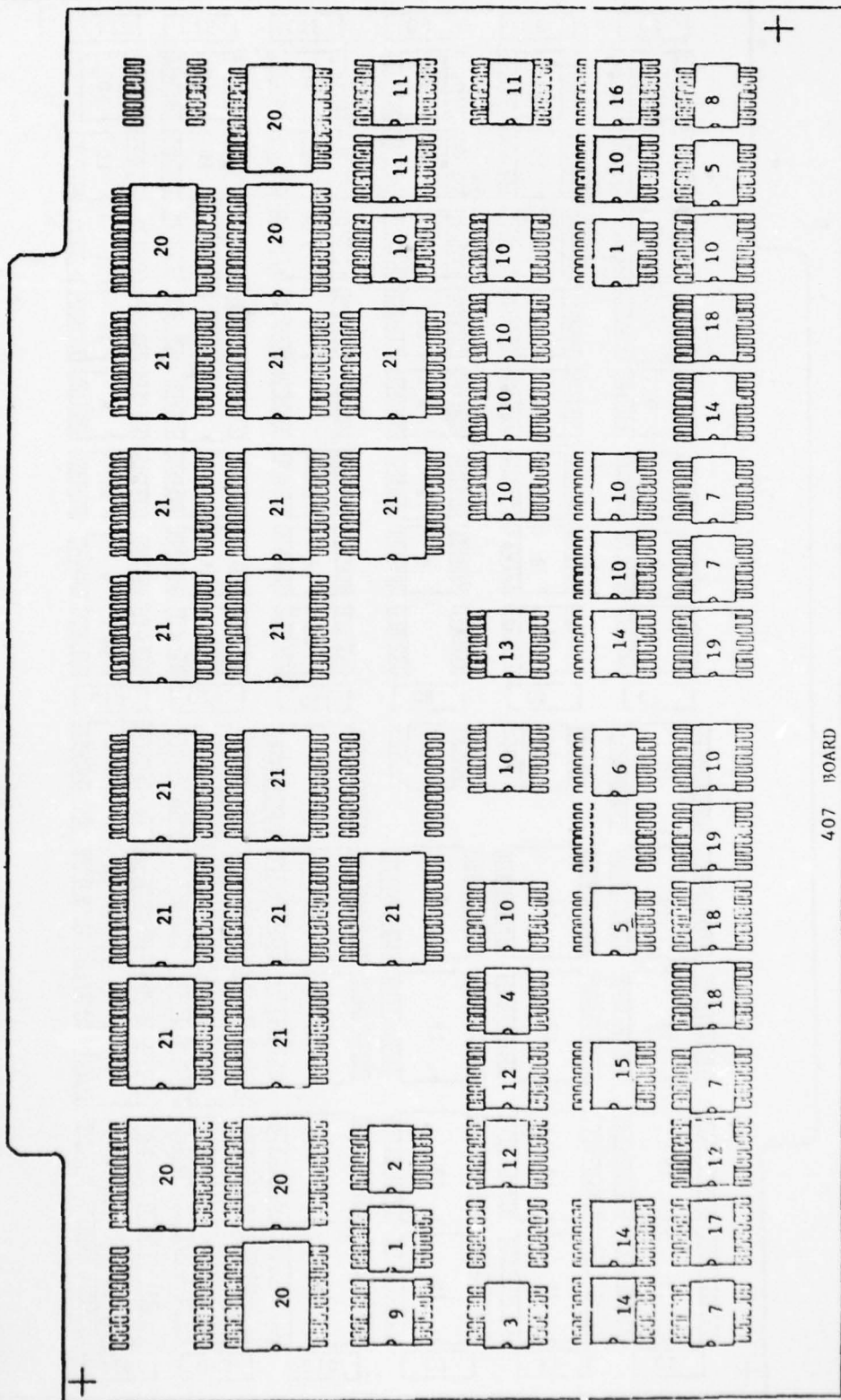


Figure 32. Monolithic Microelectronic Device Failure Rate With Junction Temperature



408 BOARD

Figure 33. Original Layout



407 BOARD

Figure 34. Original Layout