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BIT SYNCHRONIZER SYSTEM PERFORMANCE EVALUATION STUDY.(U)
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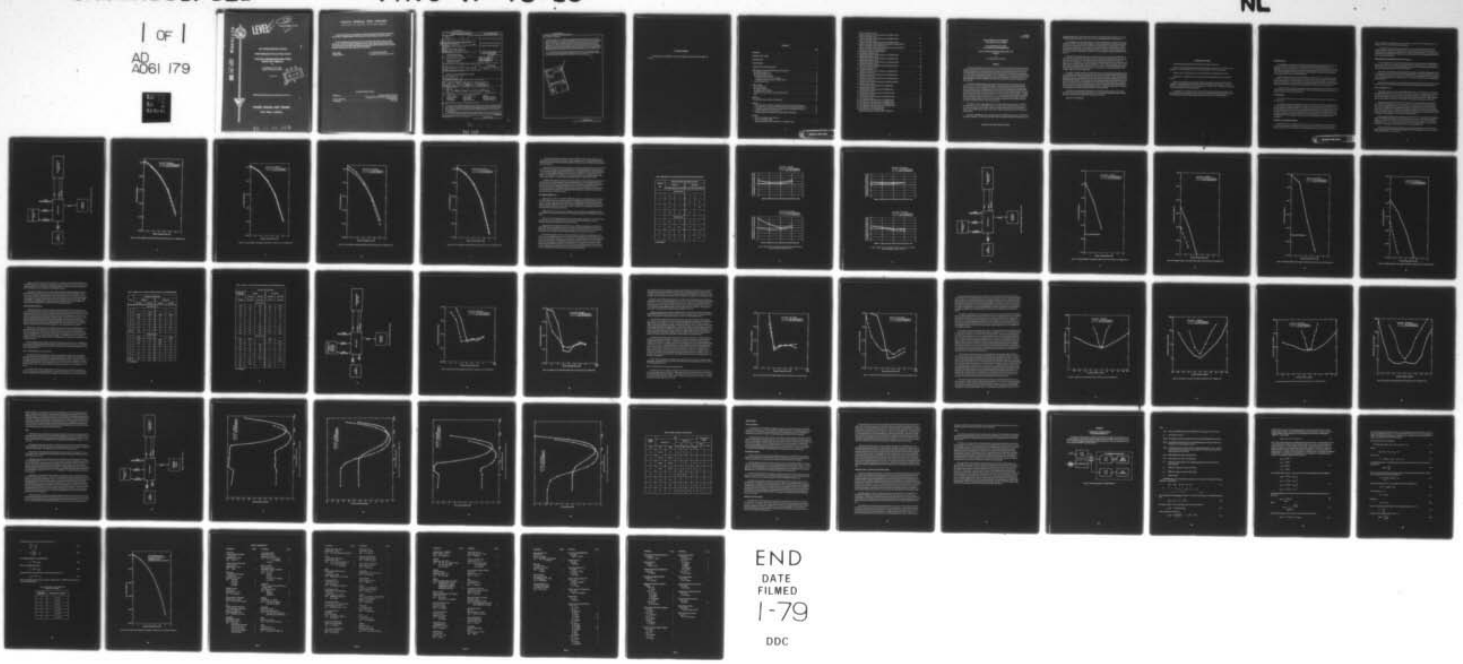

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Technical Publication TP-78-15

BIT SYNCHRONIZER SYSTEM

PERFORMANCE EVALUATION STUDY

(AIRTASK A6306302-054D-7WSL770000, WORK UNIT A6302D-2)

By

E.T.KIMBALL and D.R. HUST
Weapons Instrumentation Division

15 July 1978

PACIFIC MISSILE TEST CENTER

Point Mugu, California

PACIFIC MISSILE TEST CENTER

AN ACTIVITY OF THE NAVAL AIR SYSTEMS COMMAND

This report describes work accomplished under AIRTASK A6306302-054D-7WSL770000, Work Unit A6302D-2, Technical Support to the Telemetry Group of the Range Commander's Council.

Mr. M.A. Beckman, Electronic Design Branch; Mr. V.E. Orris, Head, Weapons Instrumentation Division; Mr. E.L. Law, Task Engineering Manager; Mr. R.S. Nelson, Associate Head, Weapons Systems Test Department; Mr. M.H. Cain, Project Engineering Manager; and CAPT D.D. DeWitt, Director, Systems Evaluation Directorate have approved this report for publication.

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Bit synchronizer	PCM bit synchronizer	PCM signal restoration

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Experimental investigations conducted with state-of-the-art bit synchronizer systems have shown that variations in performance exist between modes of operation within a system and between systems made by different manufacturers. Generalized and limited performance specifications and instructions do not provide sufficient performance data to determine expected performance in the wide range of systems applications.

Performance measurements were made using a 2047 bit pseudo random non-return-to-zero-level (NRZ-L) pulse code modulation (PCM) input signal at two bit rates and two loop bandwidth selections.

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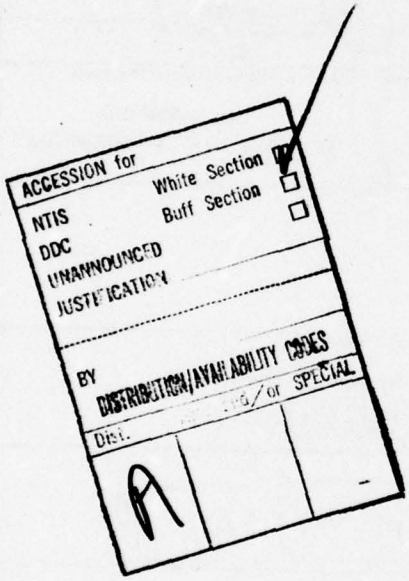
20. ABSTRACT *(Concluded)*

The two bit rates, 0.1 and 1.0 megabits, were selected to determine responses in the low- and mid-range data rate selections. The two loop bandwidths, 0.3 and 1.0 percent, were selected to determine responses with narrow- and mid-range loop selections which were common to the bit synchronizers tested. The loop bandwidth selections chosen for testing were the only two that were the same between systems. The input signal was filtered at a cutoff frequency equivalent to 0.75 x bit rate selected and the signal-to-noise ratio (SNR) was changed as required per the specific test requirement. Measurements were made to determine characteristic responses relative to bit error probability (BEP), bit slippage probability (BSP), acquisition (as a function of SNR and bit rate offset), and input bit jitter.

The results of the experimental investigations with state-of-the-art bit synchronizer systems have shown that variations in performance characteristics exist. The results also indicate the need to establish performance standards and test methods for bit synchronizer systems.



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BIT SYNCHRONIZER SYSTEM PERFORMANCE EVALUATION STUDY

(AIRTASK A6306302-054D-7WSL770000, WORK UNIT A6302D-2)

By
E.T. KIMBALL and D.R. HUST

SUMMARY

Experimental investigations conducted with state-of-the-art bit synchronizer systems have shown that variations in performance exist between modes of operation within a system and between systems made by different manufacturers. Generalized and limited performance specifications and instructions do not provide sufficient performance data to determine expected performance in the wide range of systems applications. The results of the investigation indicate a need for standardization of performance characteristics and the methods used to determine overall bit synchronizer system performance. The Telemetry Group of the Range Commanders Council has published a set of Bit Synchronizer Test Procedures as a supplement to Document 118.

Performance measurements were made using a 2047 bit psuedo random non-return-to-zero-level (NRZ-L) pulse code modulation (PCM) input signal at two bit rates and two loop bandwidth selections. The two bit rates, 0.1 and 1.0 megabits, were selected to determine responses in the low- and mid-range data rate selections. The two loop bandwidths, 0.3 and 1.0 percent, were selected to determine responses with narrow- and mid-range loop selections which were common to the bit synchronizers tested. The loop bandwidth selections chosen for testing were the only two that were the same between systems. The input signal was filtered at a cutoff frequency equivalent to 0.75 x bit rate selected and the signal-to-noise (SNR) ratio was changed as required per the specific test requirement. Measurements were made to determine characteristic responses relative to bit error probability (BEP), bit slippage probability (BSP), acquisition (as a function of SNR and bit rate offset), and input bit jitter.

The results of the performance measurements reveal that the BEP response is similar to the BEP response predicted by theory for filtered PCM data. The results also show that BEP is affected by data rate, loop bandwidth selection, and input SNR. All BEP test results indicate that the 0.3% loop bandwidth selection provides BEP responses which are better than or equal to those derived with the 1.0% loop bandwidth selection.

The results of the BSP performance measurements show that BSP increases abruptly as the SNR of the input signal is degraded. The data shows that BSP is affected by loop bandwidth and bit rate selections and

that the bit synchronizers produced different results when tested under identical conditions. It is noted that improved BSP performance occurs with the 0.3% loop bandwidth selection at both data rates.

The acquisition time measurements made as a function of SNR show that acquisition time increases abruptly as the SNR of the input signal is degraded. The data also reveals that an acquisition time threshold exists beyond which improvements in the SNR of the input signal do not cause significant changes in the measured acquisition times. The data shown in the figures reveals that with input signal constraints held constant the performance between the bit synchronizers is not uniform. However, the best acquisition time response at low SNR values was observed to occur when using the 0.3% loop bandwidth at both bit rates.

Acquisition time measurements made as a function of offset input bit rates with the SNR held constant show that acquisition time performance is affected by data rate and loop bandwidth selections. The results show that acquisition time increases abruptly as the input data rate departs from the data rate selected on the bit synchronizer. The minimum acquisition times measured were nearly constant when the input data rate was varied through a range corresponding to $\pm$ 20% of the bit synchronizer system tracking range. Improved acquisition times were observed to occur with the 1.0% loop bandwidth selection relative to the 0.3% loop bandwidth when the input data rate was offset in a range corresponding to $\pm$ 40% through $\pm$ 100% of the system tracking range.

The results of the jitter performance measurements show the effects of adding sinusoidal, Δf and f_m, jitter components to the signal at the input of the bit synchronizer. The SNR of the input signal was held constant for these tests. The measured results show that one bit synchronizer provides a constant relationship between Δf and loop bandwidth and the other bit synchronizer provides an increasing Δf as the loop bandwidth is made narrower. It is noted that the tracking range selected directly affects the Δf jitter component and therefore must be clearly defined to be used effectively in systems applications. An apparent immunity to the effects of input jitter (high frequency) may be observed when using only BSP as the criterion for performance; therefore, BEP measurements should be considered simultaneously with BSP when making judgments concerning overall bit synchronizer system performance.

The results of the experimental investigations with state-of-the-art bit synchronizer systems have shown that variations in performance characteristics exist. The results also indicate the need to establish performance standards and test methods for bit synchronizer systems.

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DEFINITION OF TERMS

The definitions used during the bit synchronizer performance evaluation are:

Bit error: A bit error has occurred when the expected level is not present; e.g., a "zero" level occurring when a "one" level is expected or a "one" level occurring when a "zero" level is expected.

Reference clock: The reference clock is the 0^{o}clock signal from the PCM generator/test set.

Delayed clock: The delayed clock is the reconstructed 0^{o}clock signal from the bit synchronizer system.

Bit slip: The equipment used to make performance measurements for this report determines bit slippage by comparing the phase of the reference clock with the phase of the delayed clock. A bit slip is defined to occur when the phases of the two clocks differ by more than $\pm 180^{o}$. Additional bit slips cannot occur until the phase difference passes through 0^{o}.

Acquisition time: Acquisition time is measured in bit periods and is defined as the number of bit periods required by a bit synchronizer system to achieve clock synchronization (phase difference between the reference clock and delayed clock signals remains less than 90^{o}) with the input PCM signal.

INTRODUCTION

An investigation to identify and measure the important performance characteristics of state-of-the-art bit synchronizers was conducted under AIRTASK A6306302-054D-7WSL770000, Work Unit A6302D-2, to provide technical support to the Telemetry Group of the Range Commanders Council. The AIRTASK is a continuing program of test and evaluation that provides the Telemetry Group with information to keep the publication of Telemetry Standards and Test Methods for Telemetry Systems and Subsystems updated and abreast of technological advances.

Missile test ranges and facilities involved in PCM data handling rely upon the characteristics of bit synchronizers to provide uniform and expected performance in data recovery operations. The Telemetry Group recognizes the need for maintaining close control of performance characteristics and therefore requested the investigation. A primary purpose of the study and experimentation was to gather information which may be used by the Telemetry Group to determine bit synchronizer performance standards.

A series of tests were conducted to measure the characteristic responses of bit synchronizers of state-of-the-art design. The tests included measurements of bit error probability, bit slippage probability, acquisition time, and the effects due to input bit jitter.

TEST METHODS

The objective of the study was to measure the important characteristic responses of state-of-the-art bit synchronizers.

The important performance characteristics of the bit synchronizers were measured using the bit synchronizer test procedures generated during the investigation. The test procedures require measurements of bit error probability, bit slippage probability, acquisition time, and the effects due to input bit jitter. Variations in signal-to-noise ratio, bit rate offset, and sinusoidal jitter components were included with each test procedure as required. The equipment arrangement for each test is included with the description of each test. Many preliminary tests were made to assure that test conditions were correct and the procedures gave repeatable results. The test equipment and bit synchronizers were dedicated for the duration of the investigation.

GENERAL TEST CONSIDERATIONS

Since the PCM test set is the central feature of the test setup, it was necessary to conduct numerous tests to verify its performance characteristics. Tests were conducted to determine the dynamic range of input/output electronics, spectral content of the output signals, accuracy of performance specifications,

accuracy of calibration and signal-to-noise ratio attenuators, readout adequacy for signal detection in all modes of operation, and system interface characteristics.

A very important requirement to measurement accuracy is that the input signal-to-noise ratio be carefully established. Additive, white, gaussian noise was used during these tests to provide a base for making performance comparisons, a common practice in the bit synchronizer industry. The signal-to-noise ratio in these tests is based upon establishing the correct relationship between the signal energy per bit and the noise power spectral density.

PERFORMANCE MEASUREMENTS AND TEST RESULTS

The test procedures used to characterize the performance of the bit synchronizers included measurements to determine bit error probability, bit slippage probability, acquisition time, and the effects due to input bit jitter. Each of the four test procedures requires a separate set of performance measurements to be made while maintaining rigid control over the test conditions.

Performance measurements were made using a 2047 bit pseudo random NRZ-L PCM signal at 1.0- and 0.1-megabit rates, and with 1.0% and 0.3% loop bandwidth selections. The input signal was either filtered or not filtered as per the specific test requirement. The purpose for each test and the results of the measurements are described separately in the following sections. Each section is identified by title corresponding to the test performed.

Data for each test are plotted to show response characteristics and trends. Data comparisons are made to determine uniform and expected response and major differences between bit synchronizer systems.

Bit Error Probability Test

The purpose of the test is to determine the BEP characteristics of a bit synchronizer as a function of input SNR. Measurements were made to determine the number of bit errors occurring in the reconstructed bit stream at the output of the bit synchronizer. The bit errors measured at each SNR setting were converted to BEP and plotted to show the effect of SNR on BEP for each bit synchronizer. BEP is defined as the ratio of the number of bits in error to the number of bits transmitted during a given time interval.

Data characterizing the performance of the bit synchronizers were taken using a 2047 bit pseudo random NRZ-L PCM input signal at 1.0- and 0.1-megabit rates with 1.0 and 0.3% loop bandwidth selections. The input signal was filtered when required with the cutoff frequency set at a value equivalent to 0.75 x bit rate. The SNR of the input signal was changed over a range of 0 through 12 dB with measurements taken at 3-dB intervals. The results of the performance measurements for bit synchronizers A and B are shown in figures 2 through 7. Measurement repeatability with the system used was held within $\pm$0.5 dB during testing. The arrangement of test equipment is shown in figure 1.

The data plotted in figure 2 shows the response of bit synchronizer A to 1.0-megabit, 2047 bit pseudo random, filtered NRZ-L PCM signal for input SNR settings of 0, 3, 6, 9, and 12 dB, and loop bandwidth selections of 1.0% and 0.3%. Figure 3 shows the results for bit synchronizer B with 1.0% and 0.3% loop bandwidth selections.. It is noted that the general shape of the plotted data is similar to that predicted by theory (refer to the appendix for methods used to derive theoretical BEP values).

The data plotted in figures 4 and 5 reveals the response of bit synchronizers A and B to a 2047 bit pseudo random 100 kilobit, filtered NRZ-L PCM signal for input SNR settings of 0, 3, 6, 9, and 12 dB, and loop bandwidth selections of 1.0% and 0.3%.

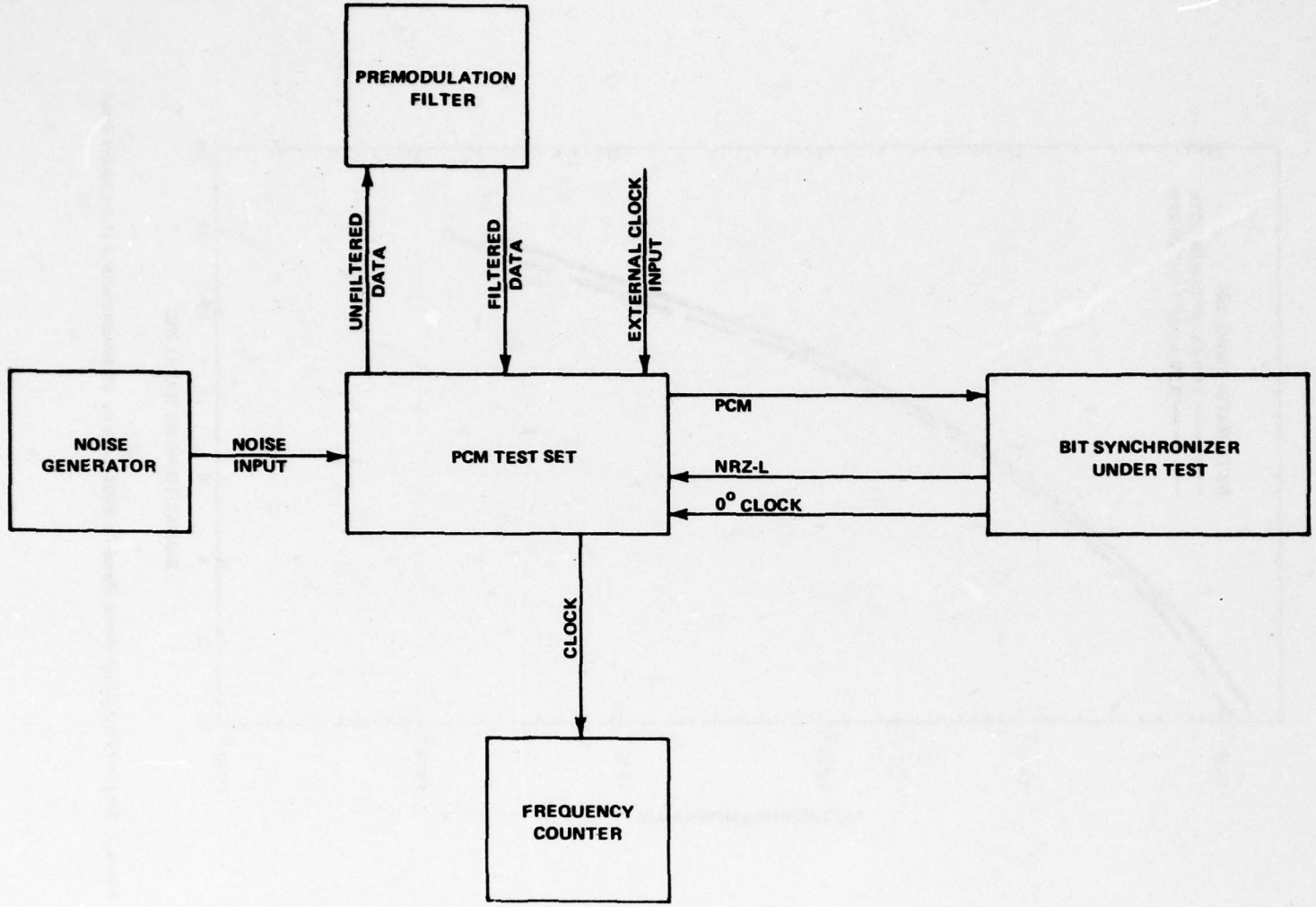


Figure 1. Bit Error Probability Equipment Setup.

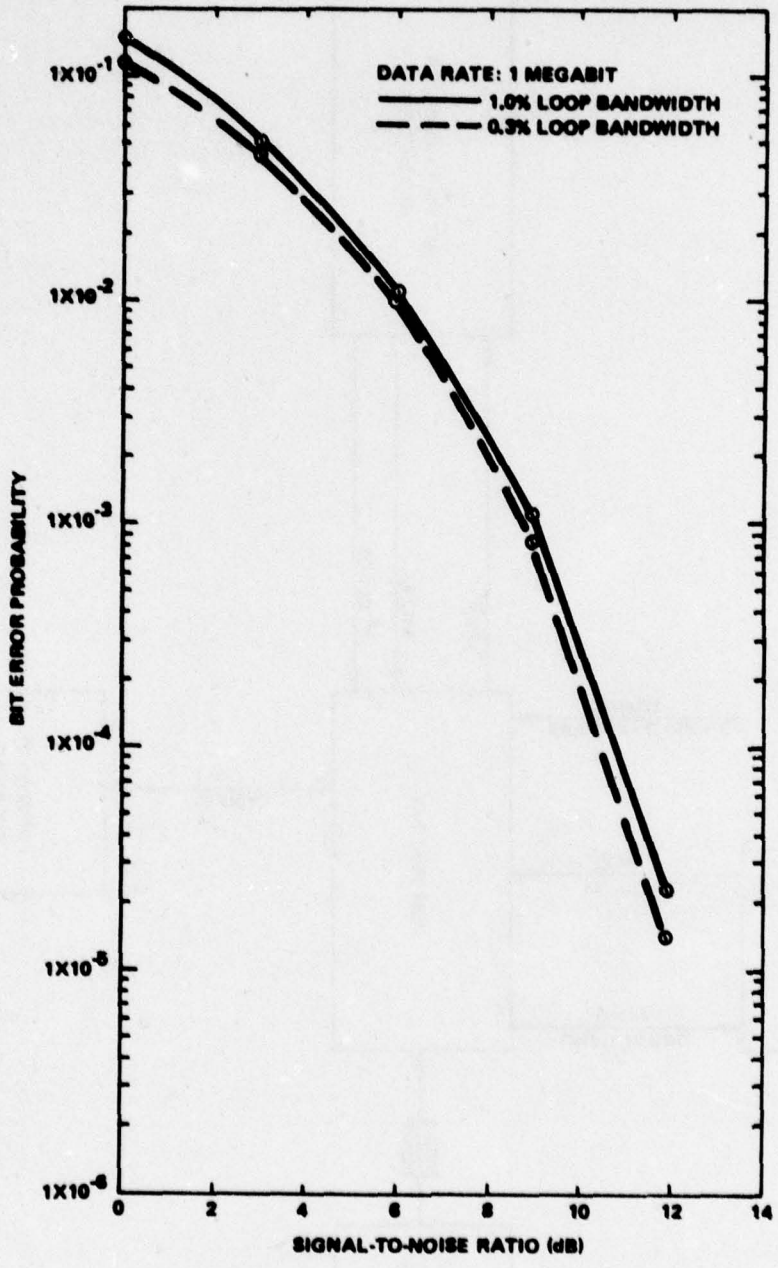


Figure 2. Bit Error Probability Versus Signal-To-Noise Ratio for Bit Synchronizer A (1.0-Megabit Rate).

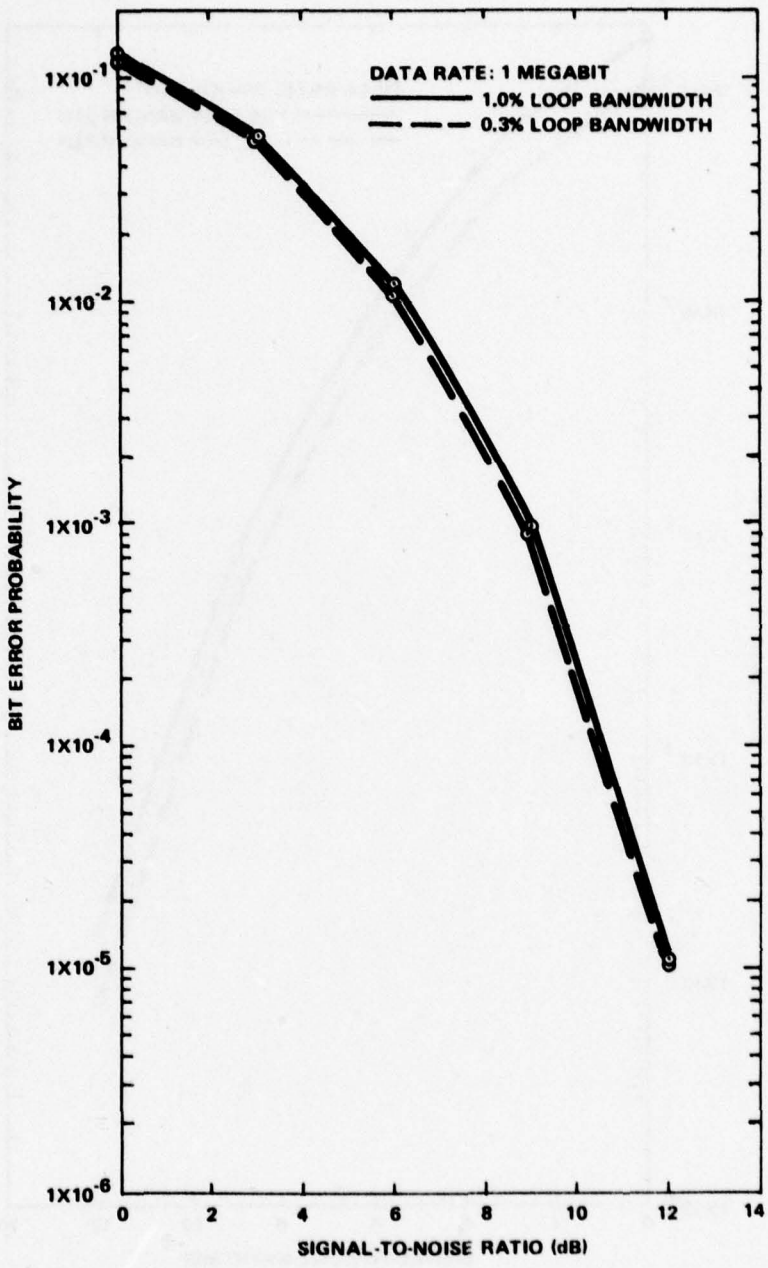


Figure 3. Bit Error Probability Versus Signal-To-Noise Ratio for Bit Synchronizer B (1-0 Megabit Rate).

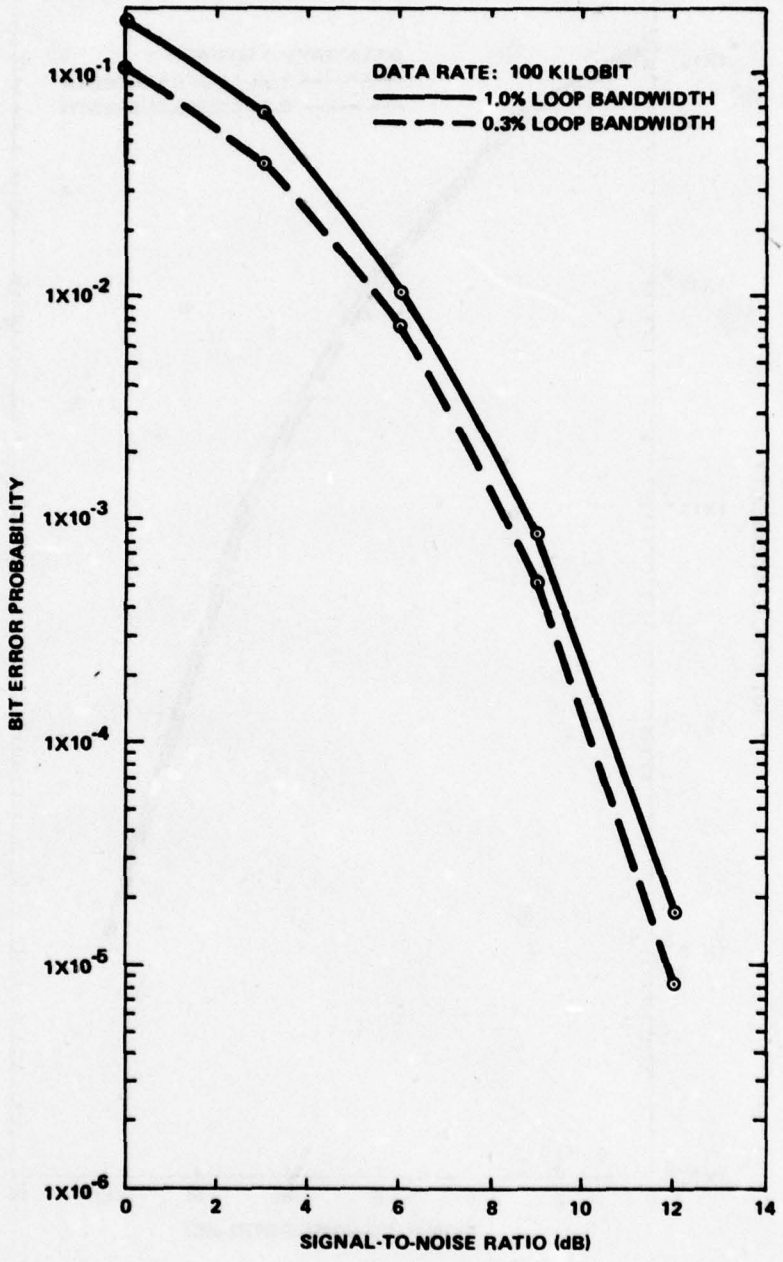


Figure 4. Bit Error Probability Versus Signal-To-Noise Ratio for Bit Synchronizer A (100-Kilobit Rate).

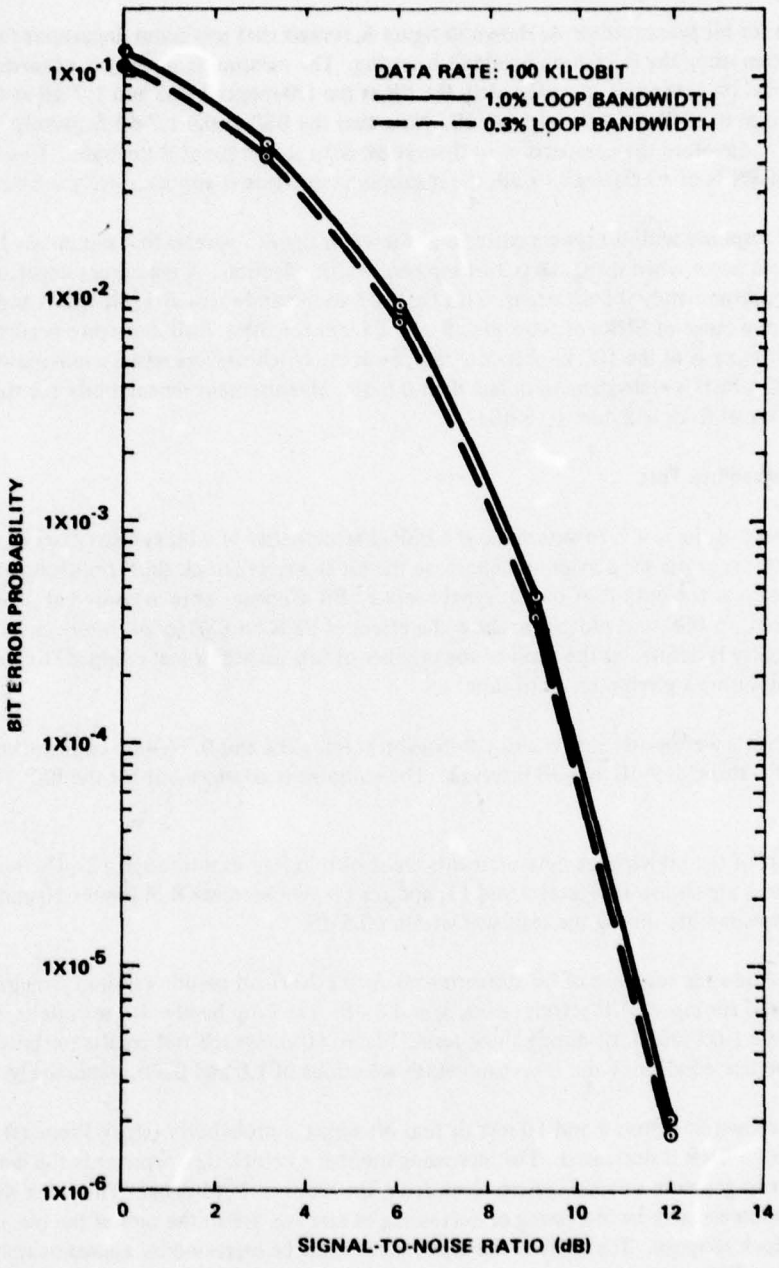


Figure 5. Bit Error Probability Versus Signal-To-Noise Ratio for Bit Synchronizer B (100-Kilobit Rate).

A summary of the differences in SNR for equivalent BEP performance between experimental and theoretical results (filtered data) is presented in table 1 and figures 6 and 7. The differences between experimental data and the theoretically calculated values are plotted for each combination of loop bandwidth and bit rate selection.

The data for bit synchronizer A, shown in figure 6, reveals that minimum departures from theoretical values occur when using the 0.3% loop bandwidth setting. The maximum departure, occurring with the 1.0% loop bandwidth setting, is approximately 0.6 dB at the 1.0-megabit rate and 1.7 dB at the 100-kilobit rate over the range of SNRs of 0 through +9 dB. Note that the BSP at the 1.7-dB departure is approximately 9×10^{-2}; therefore the comparison to theoretical data at that point is not valid. However, when using a range of SNRs of +3 through +9 dB, the maximum departure is approximately 0.6 dB.

The BEP response with bit synchronizer B as shown in figure 7 reveals that minimum departures from theoretical values occur when using the 0.3% loop bandwidth selection. A maximum departure from theoretical of approximately 0.5 dB occurs with the 1.0% loop bandwidth at 1.0-megabit and 100-kilobit data rates over the range of SNRs of 0 through 9 dB. Except for the 1.7-dB departure occurring with bit synchronizer A at the 100-kilobit data rate, both bit synchronizers reveal a maximum departure from theoretical which is equivalent to or less than 0.6 dB. Measurement repeatability for these tests is approximately equal to or less than ±0.5 dB.

Bit Slippage Probability Test

The purpose of the test is to determine the BSP characteristics of a bit synchronizer as a function of input SNR. Measurements were made to determine the bit slippages (clock slips) occurring in the reconstructed bit stream at the output of the bit synchronizer. Bit slippages were measured at selected SNR settings, converted to BSP, and plotted to show the effect of SNR on BSP for each bit synchronizer. Bit slippage probability is defined as the ratio of the number of bits gained or lost (slipped) to the number of bits transmitted during a given interval of time.

Measurements were made at 0.1- and 1.0-megabit rates, 1.0% and 0.3% loop bandwidths with variations in SNR of 0 through 9-dB in 3-dB intervals. The equipment arrangement for the BSP test is shown in figure 8.

The results of the bit slippage measurements are shown in figures 9 through 12. The test results using bit synchronizer A are shown in figures 9 and 11, and for bit synchronizer B in figures 10 and 12. Measurement repeatability during the tests was within ±0.5 dB.

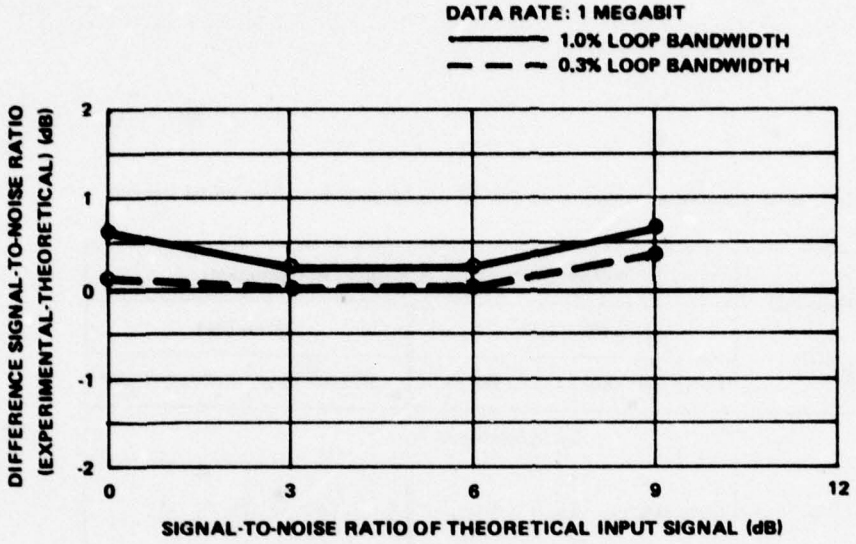
Figure 9 shows the response of bit synchronizer A to a 2047 bit pseudo random 1-megabit filtered NRZ-L PCM signal for input SNR settings of 0, 3, and 6 dB. The loop bandwidth selections of the bit synchronizer were 1.0% and 0.3% during these tests. Figure 10 shows the test results for bit synchronizer B using the same test conditions and loop bandwidth selections of 1.0 and 0.3%, respectively.

The data shown in figures 9 and 10 reveals that bit slippage probability (clock slippage) increases rapidly as the input SNR is decreased. The increasing number of clock slips represents the inability of the bit synchronizer to generate a stable system clock from the received PCM signal. The clock signal generated by the bit synchronizer may be increasing or decreasing in rate relative to the rate of the received PCM signal causing clock slippage. The SNR of the input signal must be increased by approximately 6 dB to achieve equivalent BSP values between the 1.0% and 0.3% loop bandwidth selections for bit synchronizer A at the 1-megabit data rate. Bit synchronizer B requires an increase in SNR of approximately 2 to 3 dB to achieve equivalent BSP results between the two loop bandwidth selections.

Table 1. SNR Differences for Equivalent BEP Results (Experimental-Theoretical Results)

Theoretical SNR	Difference SNR (dB) (Experimental-Theoretical)			
	1-Mb Rate		100-kb Rate	
	1.0% LBW* (dB)	0.3% LBW (dB)	1.0% LBW (dB)	0.3% LBW (dB)
Bit Synchronizer A				
0	0.6	0.1	1.7	0
3	0.2	0	0.6	-0.3
6	0.2	0	0	-0.3
9	0.6	0.3	0.3	0
Bit Synchronizer B				
0	0.5	0.2	0.5	0
3	0.4	0.2	0.2	0
6	0.3	0.2	0	-0.2
9	0.4	0.4	-0.1	-0.4

*Loop bandwidth.



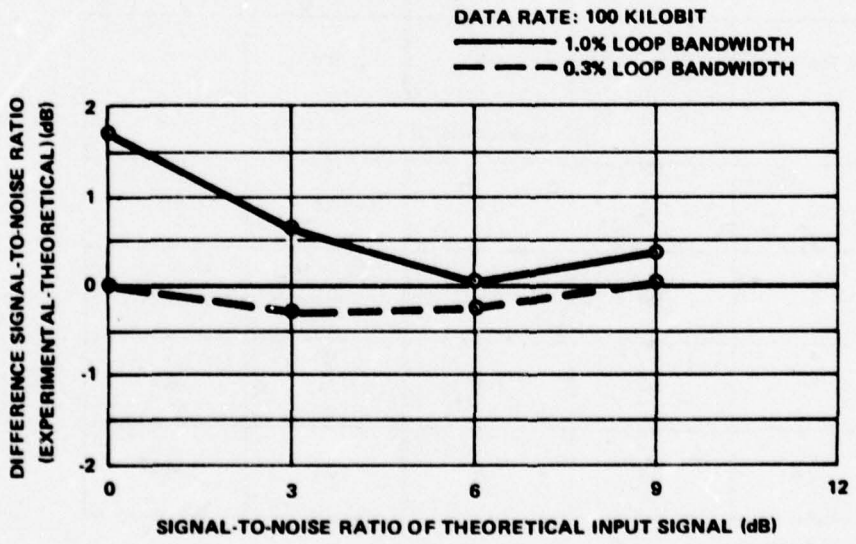
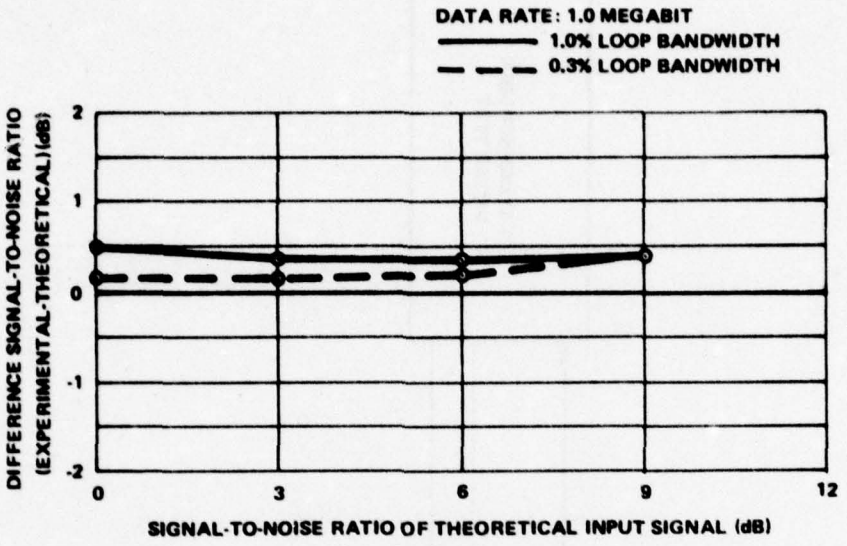


Figure 6. Signal-To-Noise Ratio Difference Between Theoretical and Experimental Bit Error Probability for Bit Synchronizer A.



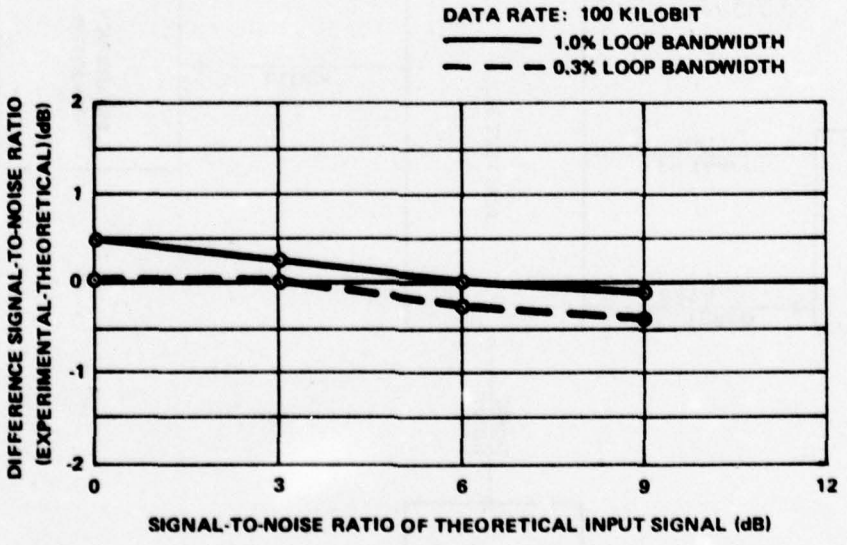


Figure 7. Signal-To-Noise Ratio Difference Between Theoretical and Experimental Bit Error Probability for Bit Synchronizer B.

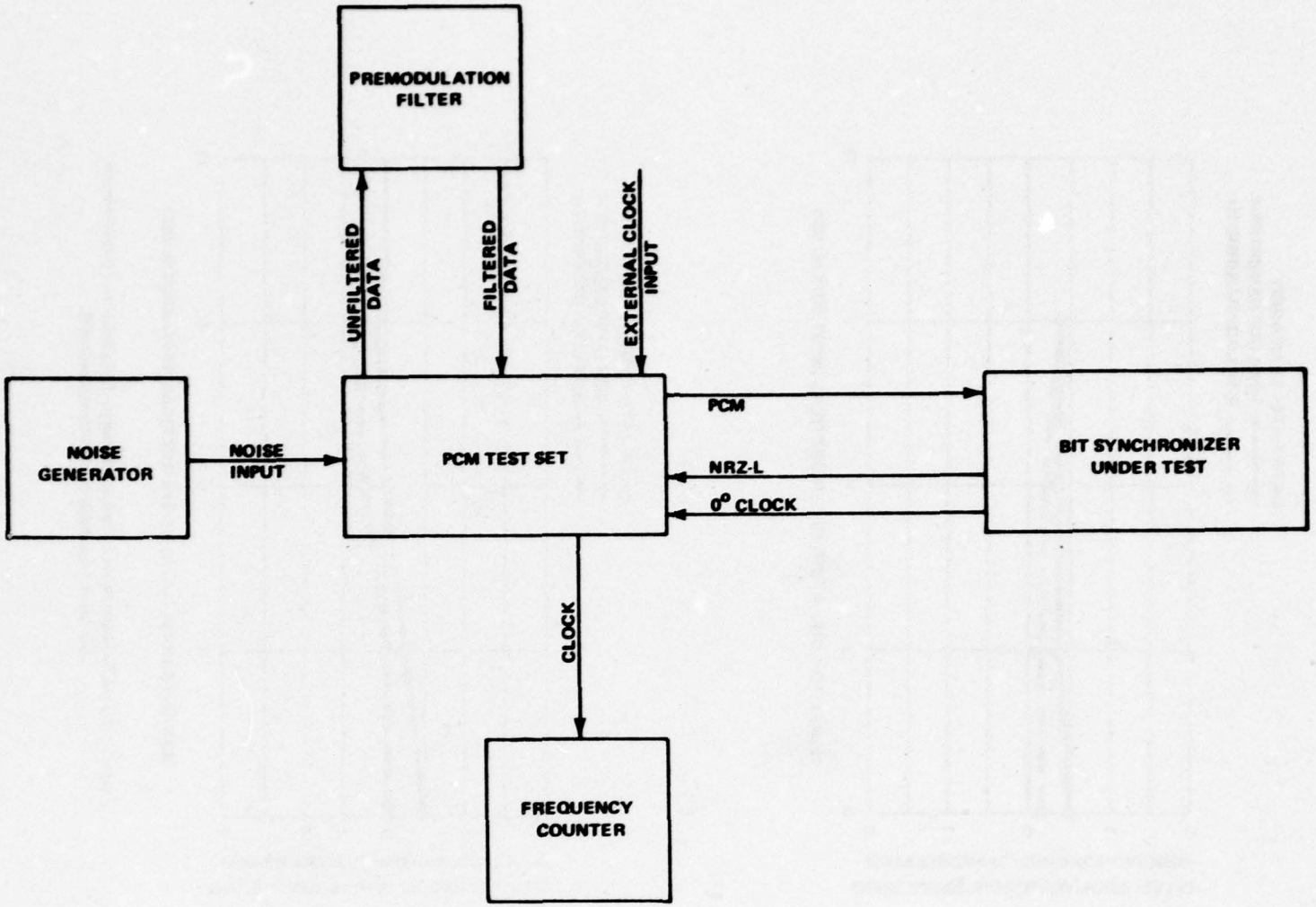


Figure 8. Bit Slippage Probability Equipment Setup.

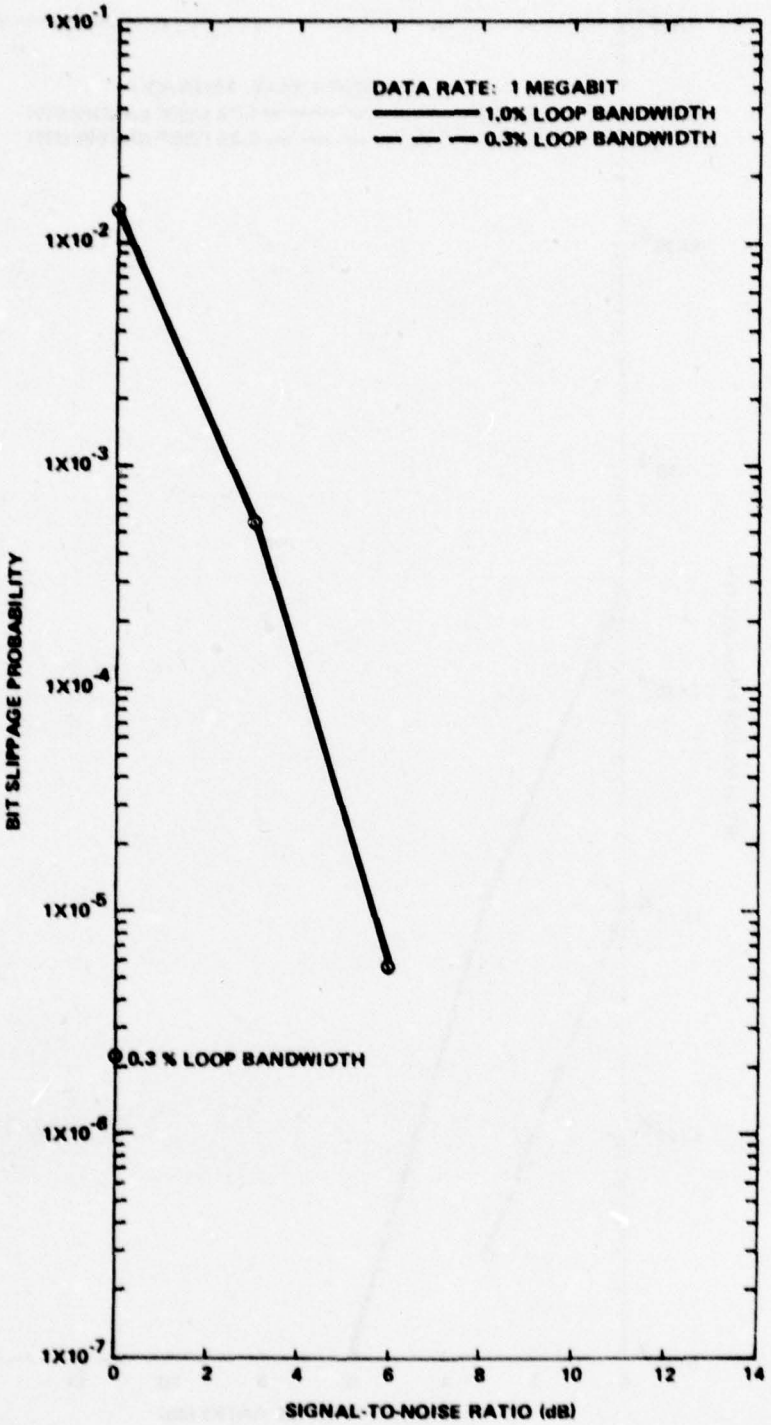


Figure 9. Bit Slippage Probability Versus Signal-To-Noise Ratio for Bit Synchronizer A (1.0-Megabit Rate).

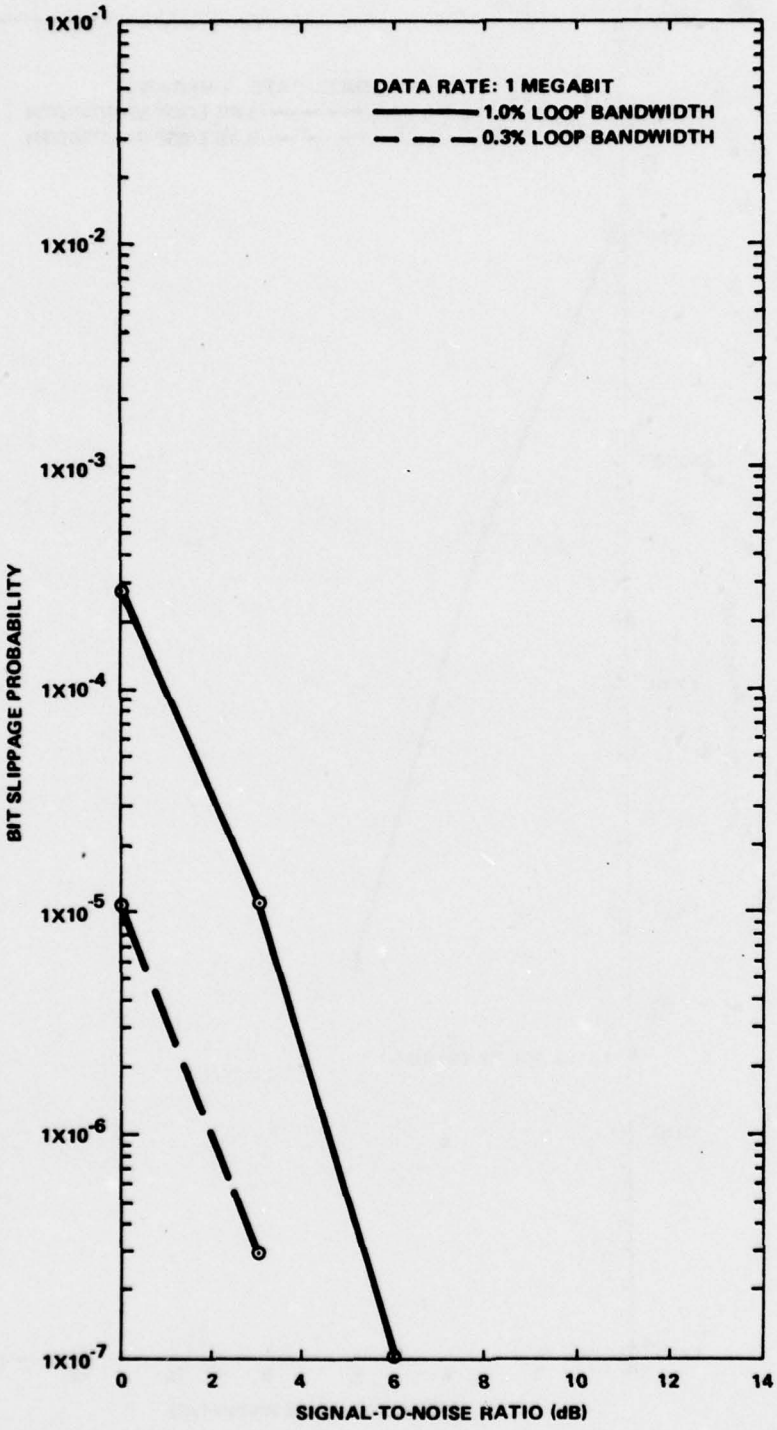


Figure 10. Bit Slippage Probability Versus Signal-To-Noise Ratio for Bit Synchronizer B (1.0-Megabit Rate).

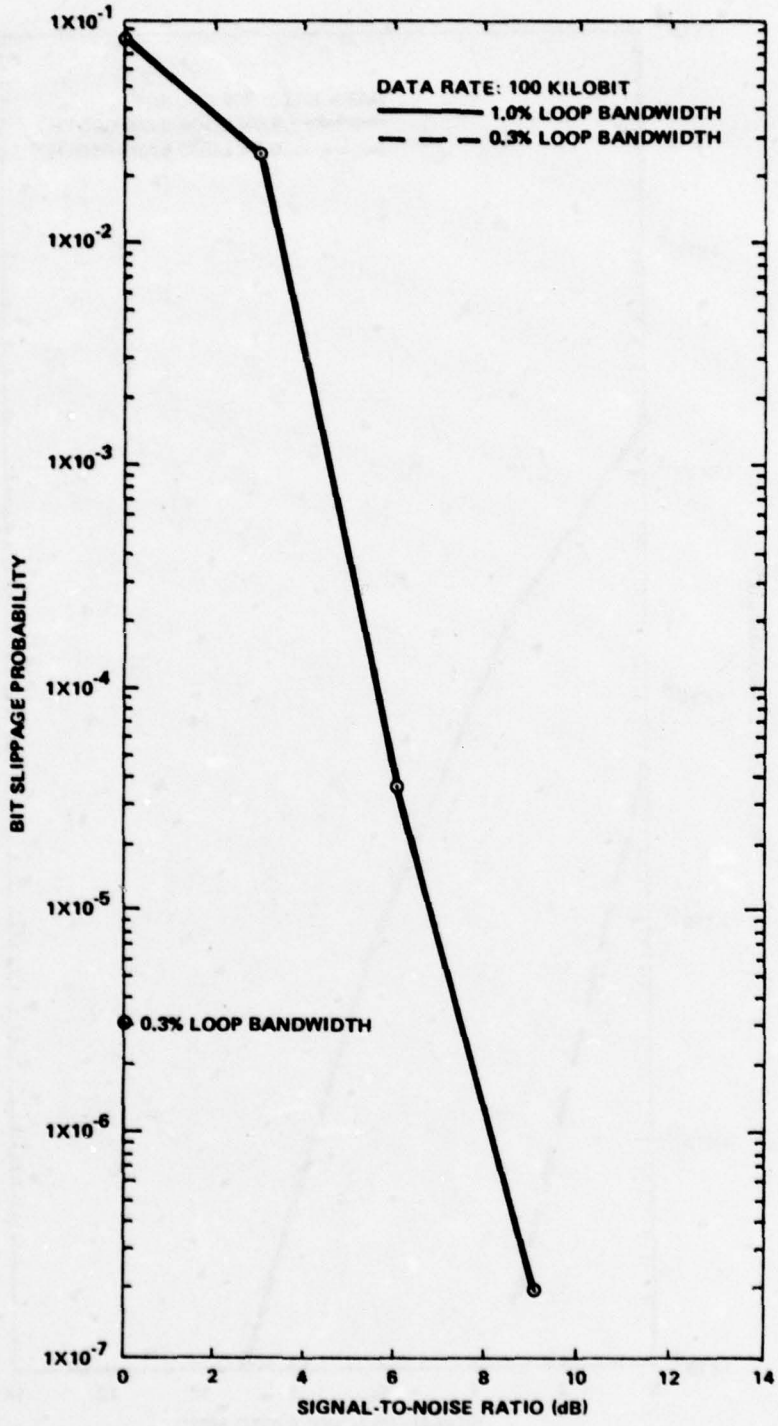


Figure 11. Bit Slippage Probability Versus Signal-To-Noise Ratio for Bit Synchronizer A (100-Kilobit Rate).

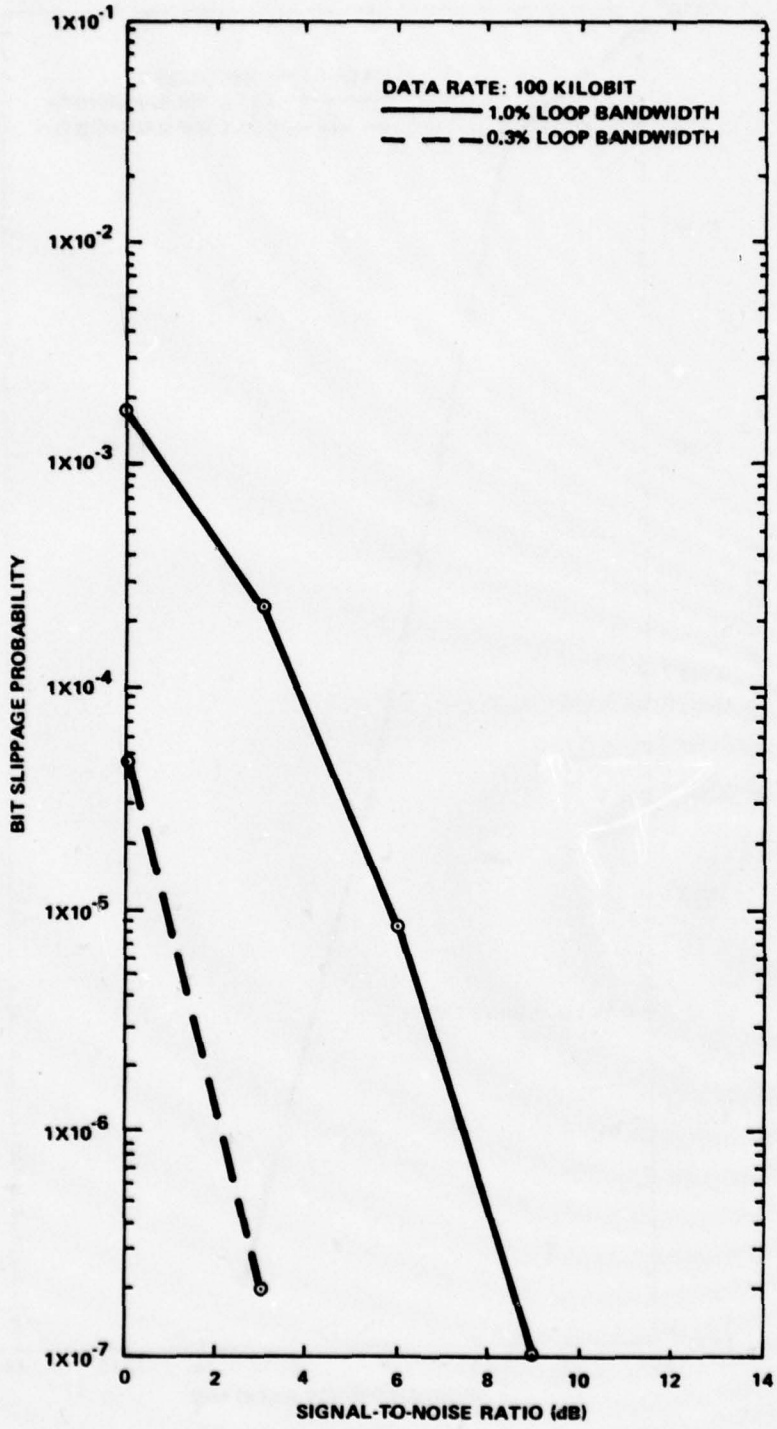


Figure 12. Bit Slippage Probability Versus Signal-To-Noise Ratio for Bit Synchronizer B (100-Kilobit Rate).

Figure 11 shows the response of bit synchronizer A to a pseudo random 100-kilobit PCM signal for input SNR settings from 0 through 9 dB. Bit slippage measurements were made with bit synchronizer loop bandwidth selections of 1.0% and 0.3%. Figure 12 shows the test results for bit synchronizer B using the same test conditions and bit synchronizer loop bandwidth selections.

The data shown in figures 11 and 12 reveals a rapid increase in bit slippage probability as the input SNR is decreased. Again, the rapid increase in the number of clock slips reveals the inability of the bit synchronizer to generate a stable system clock from the input bit stream. The reconstructed clock from the bit synchronizer may be increasing or decreasing in rate relative to the rate of the input signal causing clock slippage. A comparison of the measurements made at an SNR of 0 dB reveals a difference in BSP corresponding to an SNR difference of approximately 7 dB for bit synchronizer A and 4.4 dB for bit synchronizer B when going from the 1.0% to the 0.3% loop bandwidth selection.

Acquisition Performance Tests

Acquisition performance tests were conducted to determine the ability of the bit synchronizer to acquire clock synchronization when the input signal contained additive white, gaussian noise and when the input signal is offset in bit rate. One set of measurements was made to determine the number of bit periods required to acquire clock synchronization when the bit rate of the input signal was set at the bit rate selected on the bit synchronizer; but subjected to changes in SNR. A second set of measurements was made using a specific SNR and changing the bit rate of the input signal to the bit synchronizer; the bit rate selection on the bit synchronizer was not changed during this test. Data measurements are presented in plots of acquisition time (bit periods) versus SNR and acquisition time versus bit rate offset. Acquisition, measured in bit periods, is the interval between application of the input signal and bit acquisition.

Measurements of acquisition time, in bit periods, were made as a function of SNR and bit rate. The test results are presented in two parts: part I relates acquisition time as a function of different SNR settings at a fixed bit rate, and part II relates acquisition time as a function of variations in the input bit rate at a fixed SNR setting. The measurement results of part I for bit synchronizers A and B are presented in figures 14 through 17 and of part II in figures 18 through 21. The PCM test set used to measure the acquisition time had an upper measurement limit of 10,000 bit periods. A summary of the measured values is presented in table 3.

Data characterizing the performance of the bit synchronizers were taken at 0.1- and 1.0-megabit rates with variations in SNR of 0 through 21 dB and with bit rate offsets from 0 to a maximum of ± 100-kilobits. Bit synchronizer loop bandwidth selections included 1.0% and 0.3%. The equipment arrangement for these tests is shown in figure 13.

Part I: Acquisition Time as a Function of SNR

The number of bit periods required by bit synchronizers A and B to achieve clock synchronization with the input bit stream were measured over a range of input SNRs of 0 through 21 dB. An additional measurement was made with the additive noise signal disconnected, and is shown as "PCM only" (a reference data point only). The measurements were made using a 2047 bit pseudo random, premodulation filtered, input NRZ-L PCM signal at 0.1- and 1.0-megabit rates, with bit synchronizer loop bandwidths of 1.0% and 0.3% respectively. The cutoff frequency of the premodulation filter was set at a value equivalent to 0.75 x bit rate.

The results of the performance measurements for bit synchronizers A and B using 1.0-megabit rate and the 1.0% and 0.3% loop bandwidth selections are shown in figures 14 and 15. The data taken with the 1.0% loop bandwidth reveals an abrupt change in acquisition time with SNR settings of 6 through 12 dB for

Table 2. Acquisition Time as a Function of SNR by Bit Rate and Loop Bandwidth Selections

SNR	Acquisition Time (Bit Periods)			
	1-Mb Rate		100-kb Rate	
	1.0% LBW*	0.3% LBW	1.0% LBW	0.3% LBW
Bit Synchronizer A				
0	–	–	–	–
3	–	4500	–	–
6	8200	1200	6900	2000
9	1000	30	20	31
12	31	38	38	44
15	44	50	51	46
18	38	53	44	52
21	80	62	29	60
"PCM"	68	54	66	52
Bit Synchronizer B				
0	8945	4770	–	5780
3	6730	197	9580	193
6	785	71	6478	51
9	8	18	330	19
12	7	14	5	22
15	20	20	6	10
18	26	34	10	21
21	25	24	17	29
"PCM"	29	26	15	18

*Loop bandwidth.

Table 3. Acquisition Time for Offset Bit Rates by Bit Rate and Loop Bandwidth Selections

Bit Rate Offset (Percentage of Tracking Rate)	Acquisition Time (Bit Periods)			
	1-Mb Rate		100-kb Rate	
	1.0% LBW*	0.3% LBW	1.0% LBW	0.3% LBW
Percentage	Bit Periods	Bit Periods	Bit Periods	Bit Periods
Bit Synchronizer A				
+100	416	1850	1610	5600
+80	280	1170	442	1300
+60	157	680	197	715
+40	89	292	95	262
+20	54	81	58	60
0	42	51	60	70
-20	50	54	57	51
-40	64	110	78	140
-60	98	390	115	450
-80	160	760	155	859
-100	233	1300	210	1460
Bit Synchronizer B				
+100	4256	–	2196	–
+80	471	–	430	9043
+60	128	3086	17	1943
+40	48	782	6	414
+20	20	105	6	38
0	10	18	7	11
-20	14	61	5	53
-40	38	943	5	619
-60	147	–	107	3519
-80	789	–	183	–
-100	–	–	7055	–

*Loop bandwidth.

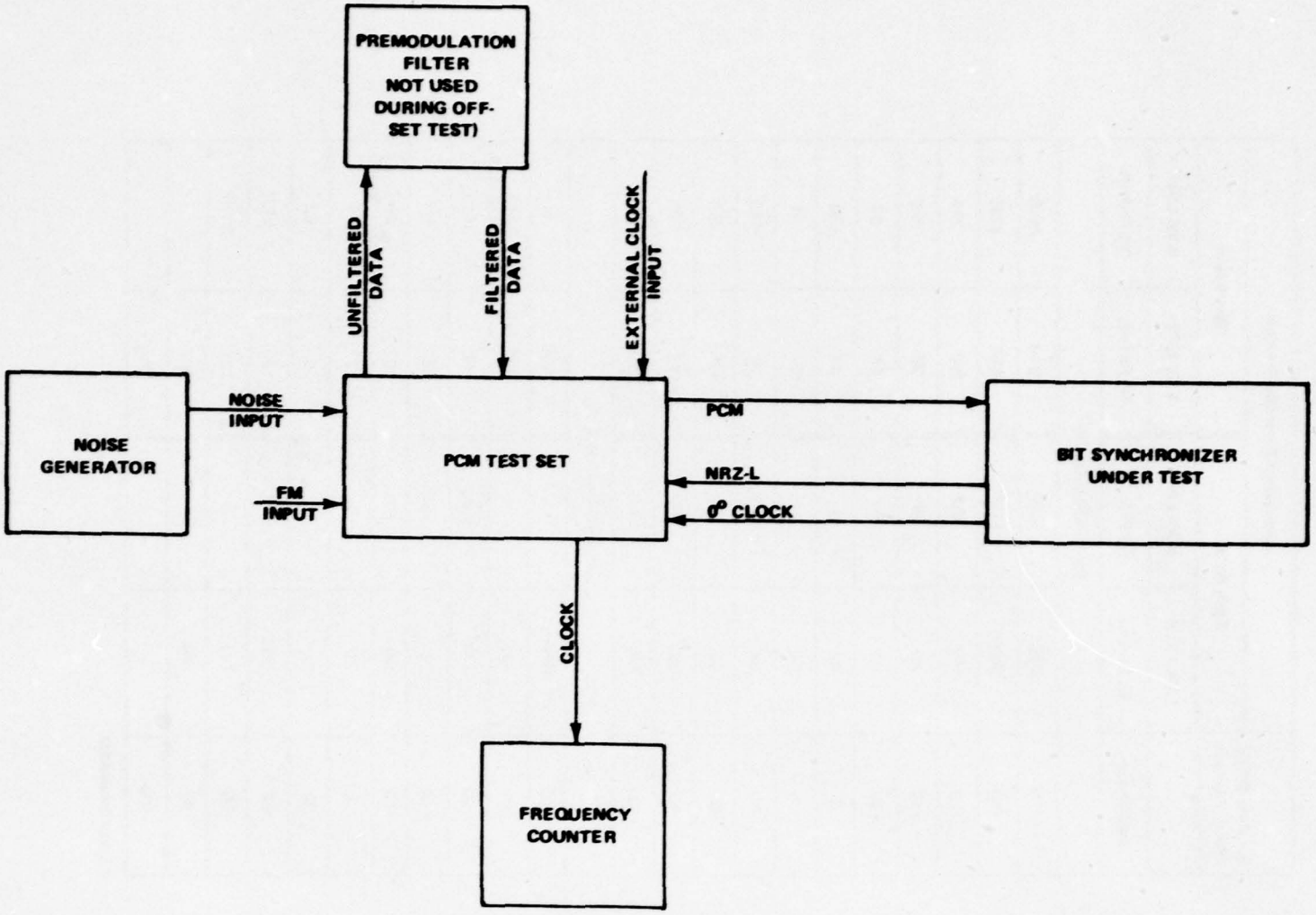


Figure 13. Acquisition Equipment Setup.

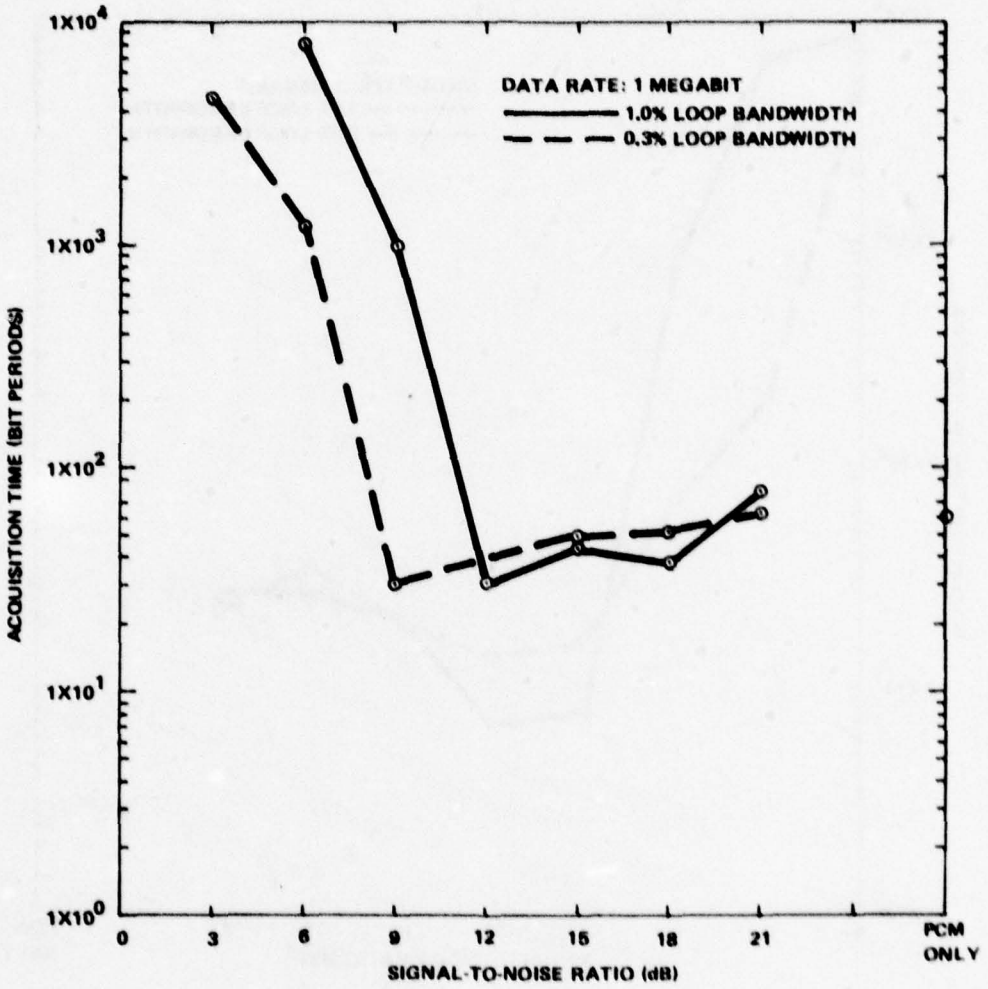


Figure 14. Acquisition Time Versus Signal-To-Noise Ratio for Bit Synchronizer A (1-Megabit Rate).

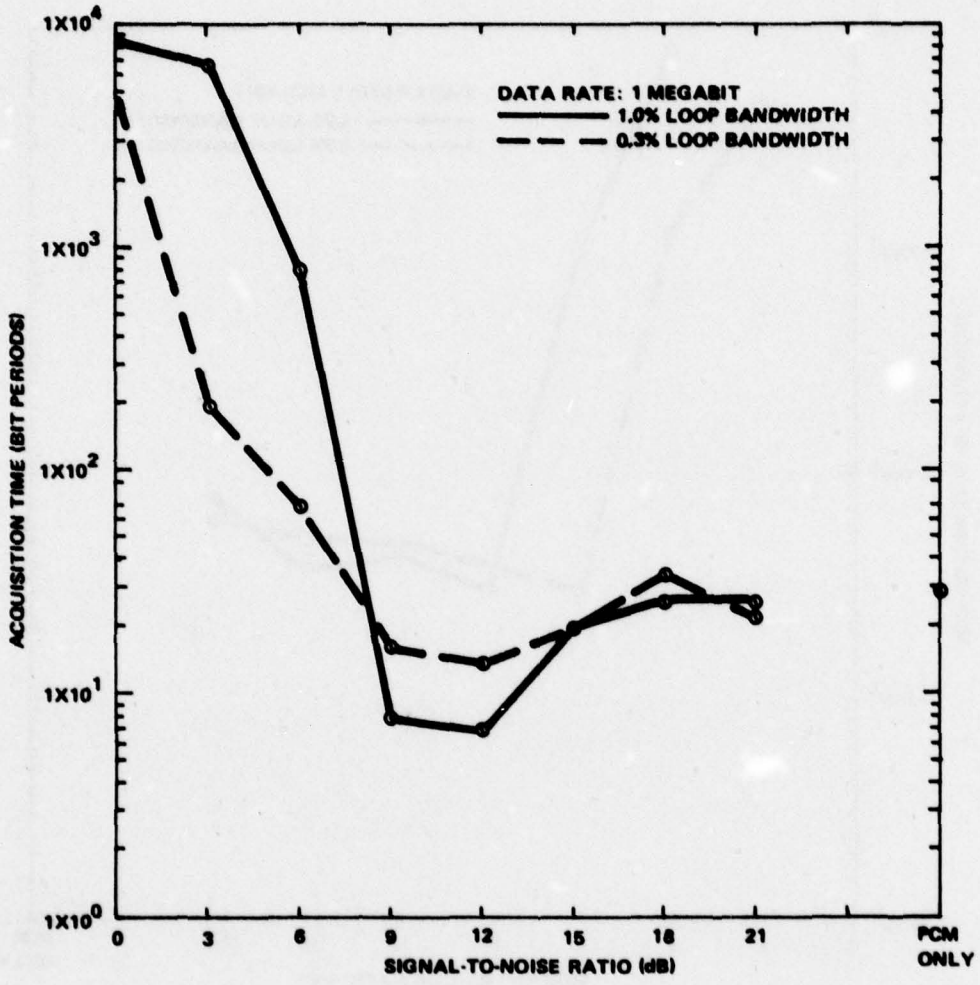


Figure 15. Acquisition Time Versus Signal-To-Noise Ratio for Bit Synchronizer B (1-Megabit Rate).

bit synchronizer A and 0 through 9 dB for bit synchronizer B. Measured acquisition times are in a range of 8 through 8500 bit periods with SNRs of 0 through 21 dB. The spread in acquisition time measurements decreased to 8 through 80 bit periods for both bit synchronizers when SNRs were set in the range of 9 dB through 21 dB. The acquisition time measurement for "PCM only" was within the 8 to 80 bit period range.

The shape of the data plotted in figures 14 and 15 for the 0.3% loop bandwidth selection is similar to that measured with the 1.0% loop bandwidth selection. However, the 0.3% loop bandwidth data show SNR differences of 2.7 to 3.8 dB with bit synchronizer A and 1.6 to 4.2 dB with bit synchronizer B to achieve the same acquisition times. The acquisition time measurements for both bit synchronizers reveal a spread of 15 to 60 bit periods with SNRs in a range of 9 dB to 21 dB. Again, the "PCM only" measurement appears within the acquisition time spread resulting from SNRs of 9 to 21 dB.

Performance measurements made with a 100-kilobit rate, 2047 bit pseudo random, premodulation filtered NRZ-L PCM input signal are shown in figures 16 and 17. Figures 16 and 17 show the measurement results for bit synchronizers A and B when using a 1.0% and 0.3% loop bandwidth selection.

The performance measurements shown in these figures reveal similar tendencies as those measurements taken at the 1.0-megabit rate. Abrupt changes in acquisition time are observed at low SNR settings. The acquisition times measured as a function of changing the SNR from 6 dB to 9 dB show a spread of 7000 to 20 bit periods, indicating the number of bit periods required to achieve clock synchronization with the input signal. Measurements made at SNRs of 9 dB through 21 dB show acquisition times in a range of 20 to 65 bit periods. Again, the "PCM only" measurement appears within this range of SNR settings. Comparison of the measurements made with the 1.0% and 0.3% loop bandwidth selections, shown in figure 16, reveals a difference of approximately 5000 bit periods at an SNR of 6 dB. However, with SNRs that are greater than 6 dB the comparison reveals similar results between loop bandwidth selections.

The performance measurements for bit synchronizer B are shown in figure 17. The data shown are a function of loop bandwidth selections of 1.0% and 0.3%, respectively. The data measurements show that changes in SNR over a range of 3 dB to 12 dB decreases the number of bit periods for synchronization acquisition from 9500 to 5. In addition, the range of bit periods required for acquisition with SNR settings in the range of 12 dB to 21 dB is approximately 5 to 16; the "PCM only" data point appears within this range of acquisition times. Comparing the 0.3% loop bandwidth data with the 1.0% loop bandwidth data, figure 17, reveals that the SNR must be increased approximately 2 to 6 dB at the low SNR settings to achieve similar acquisition times when using the 1.0% loop bandwidth selection. A comparison of the data between the 100-kilobit and 1.0-megabit data rates reveals a relative improvement in SNR for a given acquisition time of approximately 3 dB at the lower SNR settings when using the 1.0-megabit data rate and the 1.0% loop bandwidth.

Table 2 contains acquisition time measurements in bit periods made as a function of different input SNR settings. Data measurements are included for the 100-kilobit and 1.0-megabit data rates and 1.0% and 0.3% loop bandwidth selections.

Part II: Acquisition Time as a Function of Bit Rate Offset

Performance tests were conducted to determine the acquisition time in bit periods of a bit synchronizer when the input signal was offset in rate. Measurements were made using an unfiltered 2047 bit pseudo random, NRZ-L-PCM input with an SNR of 15 dB. Data were taken for two bit rates, 0.1- and 1.0-megabit, and for loop bandwidth selections of 1.0% and 0.3%. The bit rate setting on the bit synchronizers remained unchanged as the input signal was offset in rate.

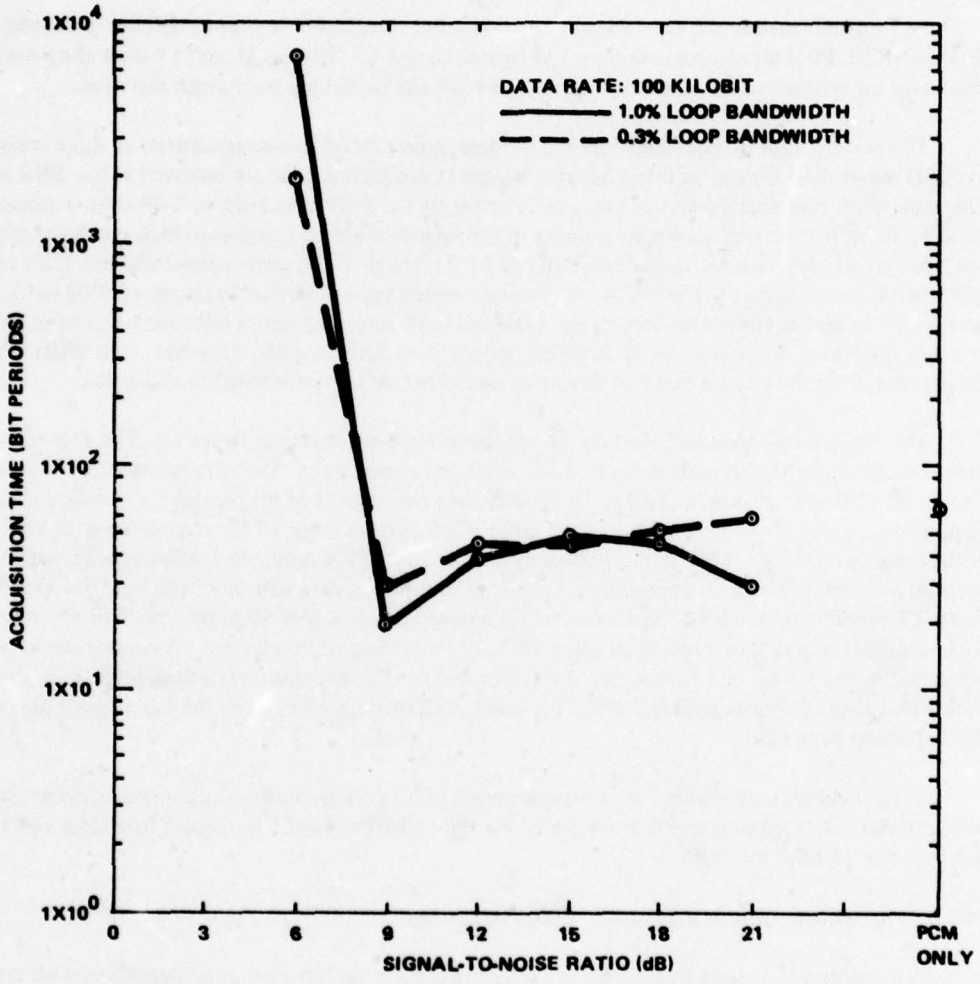


Figure 16. Acquisition Time Versus Signal-To-Noise Ratio for Bit Synchronizer A (100-Kilobit Rate).

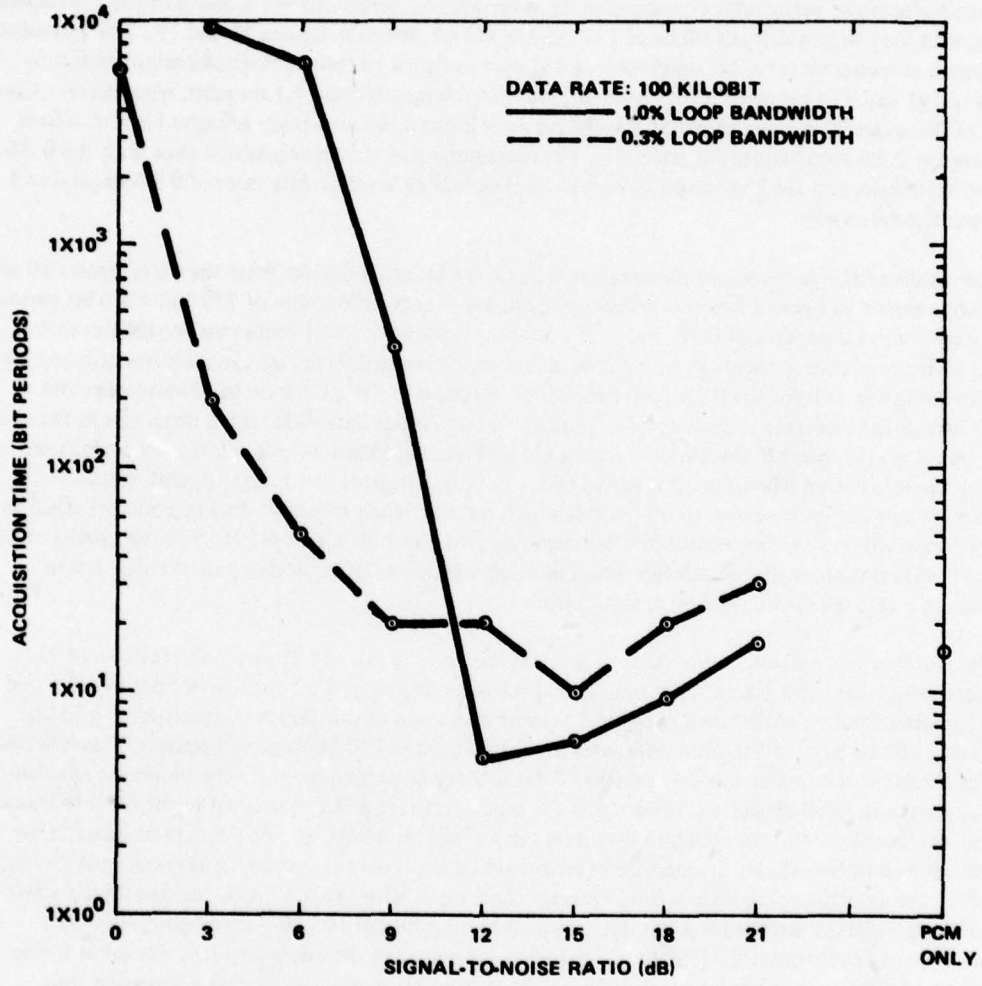


Figure 17. Acquisition Time Versus Signal-To-Noise Ratio for Bit Synchronizer B (100-Kilobit Rate).

The acquisition times shown in figures 18 through 21 are the result of bit rate offsets to ±100, ±50, and ±30-kilobits at the 1.0-megabit data rate and to ±10, ±5, and ±3 kilobits at the 0.1-megabit (100-kilobit) data rate. The bit rate offsets used are based upon the design relationships between the manually selectable loop bandwidths and the automatically selected tracking ranges of the bit synchronizers. The manufacturer of bit synchronizer A specified a tracking range in percentage of the selected bit rate equivalent to ten times the selected loop bandwidth (%). The tracking range for bit synchronizer B was specified to be equivalent to 5 percent of the selected bit rate for all loop bandwidths. The limit of acquisition time measurements by the design of the PCM test set is 10,000 bit periods. A summary of the measured values is presented in table 3.

The results of the performance measurements made with bit synchronizers A and B at the 1.0-megabit data rate, with loop bandwidth selections of 1.0% and 0.3%, are shown in figures 18 and 19. The acquisition time response measurements for bit synchronizer A shown in figure 18 reveal maximum acquisition time increases of 191 and 374 bit periods for input data rates of 0.9 megabit and 1.1 megabit, respectively. Comparisons of the acquisition times shown in the figures reveals increased sensitivity to input bit rate offsets when using the 0.3% loop bandwidth selection. The maximum increases in acquisition time with the 0.3% loop bandwidth selection are 1249 and 1799 bit periods occurring at input data rates of 0.97-megabit and 1.03-megabit, respectively.

The results of the performance measurements made for bit synchronizer B are shown in figures 19 and 21. The data shown in figure 19 reveals maximum increases in acquisition time of 779 and 4246 bit periods occurring with input data rates of 0.96 and 1.05 megabit, respectively. The minimum acquisition time is shown as 10 bit periods and occurs at an input data rate which is equal to the bit synchronizer selected bit rate. Comparing the data for the 0.3% loop bandwidth selection to the 1.0% loop bandwidth selection in figure 19 reveals the increased sensitivity of acquisition time to input data rates which depart from the rate selected on bit synchronizer B. Maximum increases in measured acquisition times of 925 bit periods and 3068 bit periods occurred when the bit rate was offset to 0.980 megabit and 1.030 megabit, respectively. The minimum acquisition time was 18 bit periods which resulted when the input data rate was set equal to the bit rate selected on the bit synchronizer, corresponding to a zero data rate offset. The test results at the 1.0-megabit data rate show that acquisition times increase whenever the input data rate is either less or greater than the rate selected on the bit synchronizer.

The performance measurements made at the 100-kilobit data rate are shown in figures 20 and 21. Again, data were taken with bit synchronizers A and B while using loop bandwidth selections of 1.0% and 0.3%. The data measurements shown in figure 20 reveal maximum acquisition time increases of 150 bit periods and 1550 bit periods for input data rates of 90 kilobits and 110 kilobits, respectively. The selected bit rate of the bit synchronizer was set at a 100 kilobit rate for all measurements. The minimum acquisition time of approximately 60 bit periods occurred at the input data rate which was equal to the bit rate selected on the bit synchronizer, corresponding to zero data rate offset. A comparison of the data in figure 20 by loop bandwidth selection shows the increase in sensitivity to input data rate changes when using 0.3% loop bandwidth. The maximum acquisition time measurements made with the 0.3% loop bandwidth are 1390 bit periods and 5530 bit periods for input data rates of 97 kilobits and 103 kilobits, respectively. The minimum time of approximately 51 to 70 bit periods occurred when the input data rate was set at the selected bit rate (±500 bits) of the bit synchronizer. The data measurements show that acquisition time increases as the input data rate departs from the selected bit rate of the bit synchronizer.

Performance measurements made with bit synchronizer B at the 100-kilobit selected data rate are shown in figure 21. Again, the data is taken with loop bandwidths of 1.0% and 0.3%. Maximum acquisition time increases of 7048 bit periods and 2189 bit periods, shown in figure 21, occurred at input data rates of 95 kilobits and 105 kilobits, respectively. The bit rate selection of the bit synchronizer was 100-kilobits. The minimum acquisition times measured were 5 to 7 bit periods occurring with input rates of 98 to 102

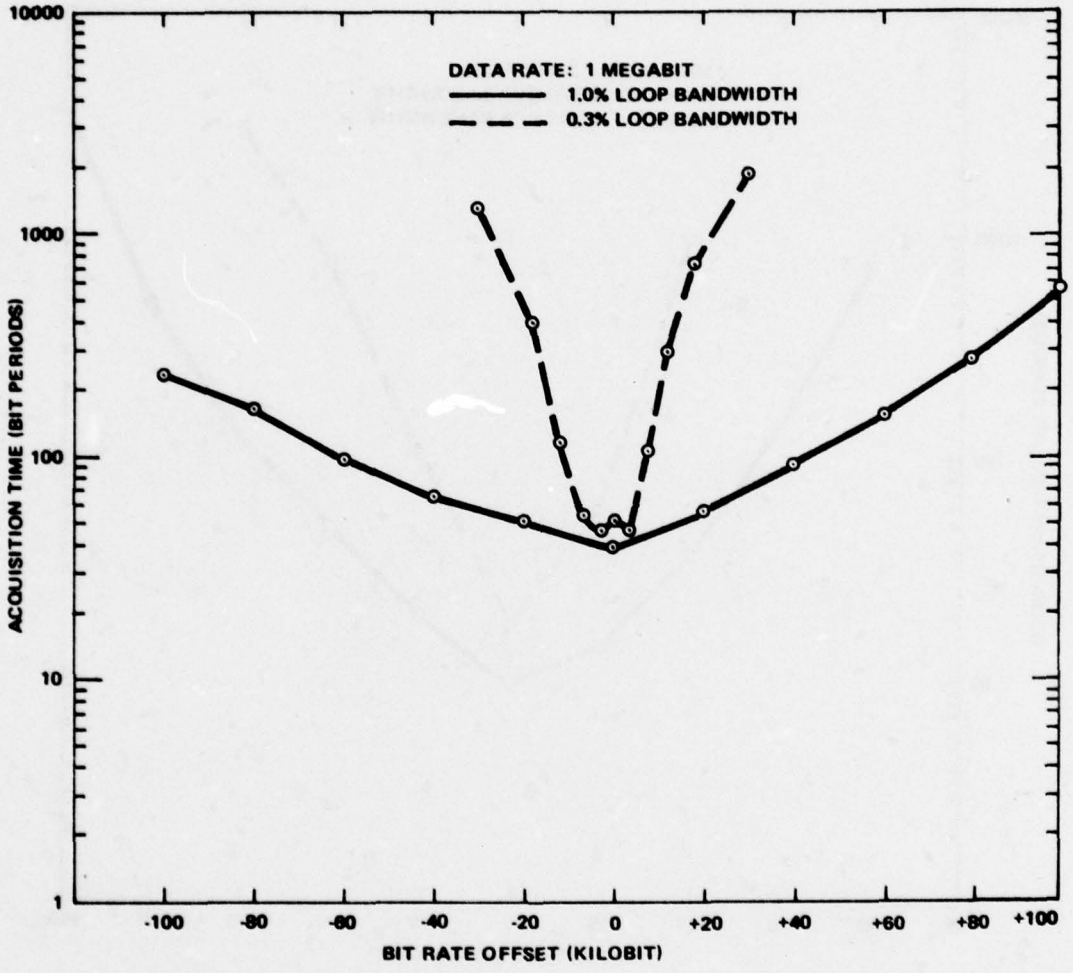


Figure 18. Acquisition Time Versus Bit Rate Offset for Bit Synchronizer A (1-Megabit Rate).

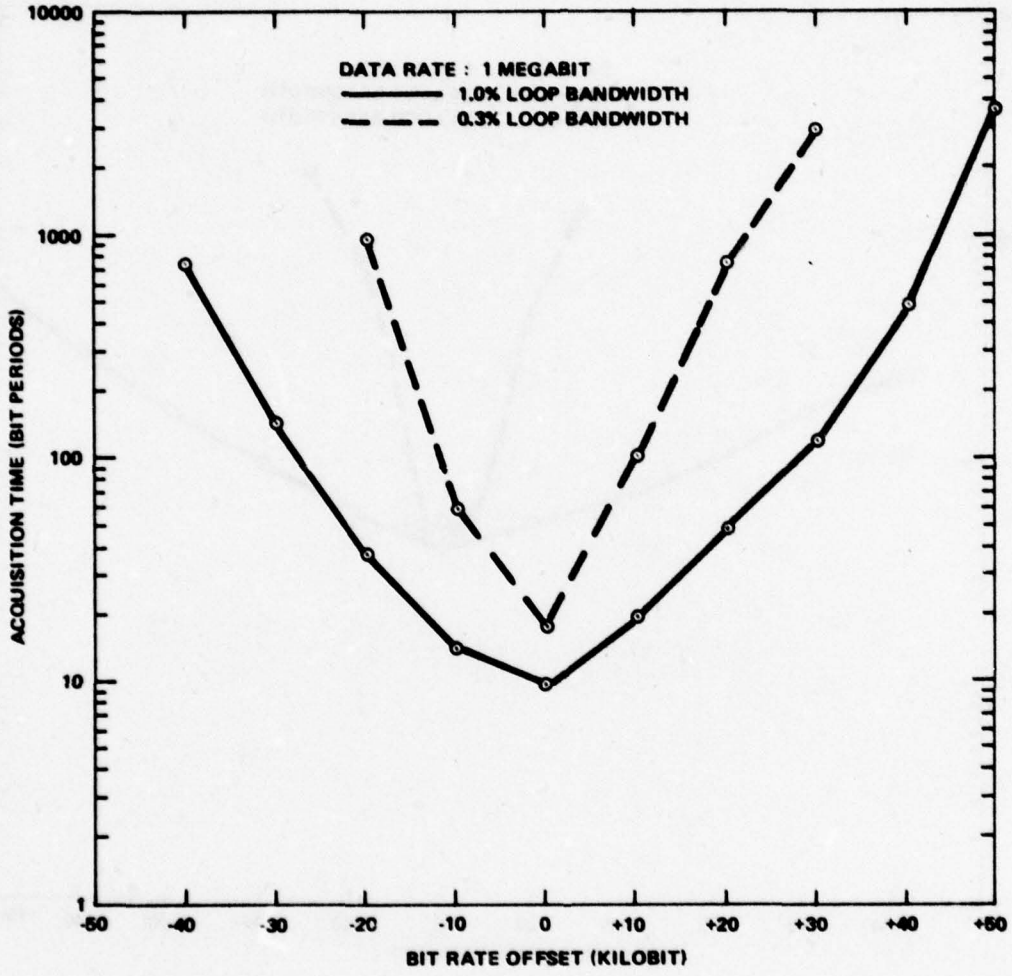


Figure 19. Acquisition Time Versus Bit Rate Offset for Bit Synchronizer B (1-Megabit Rate).

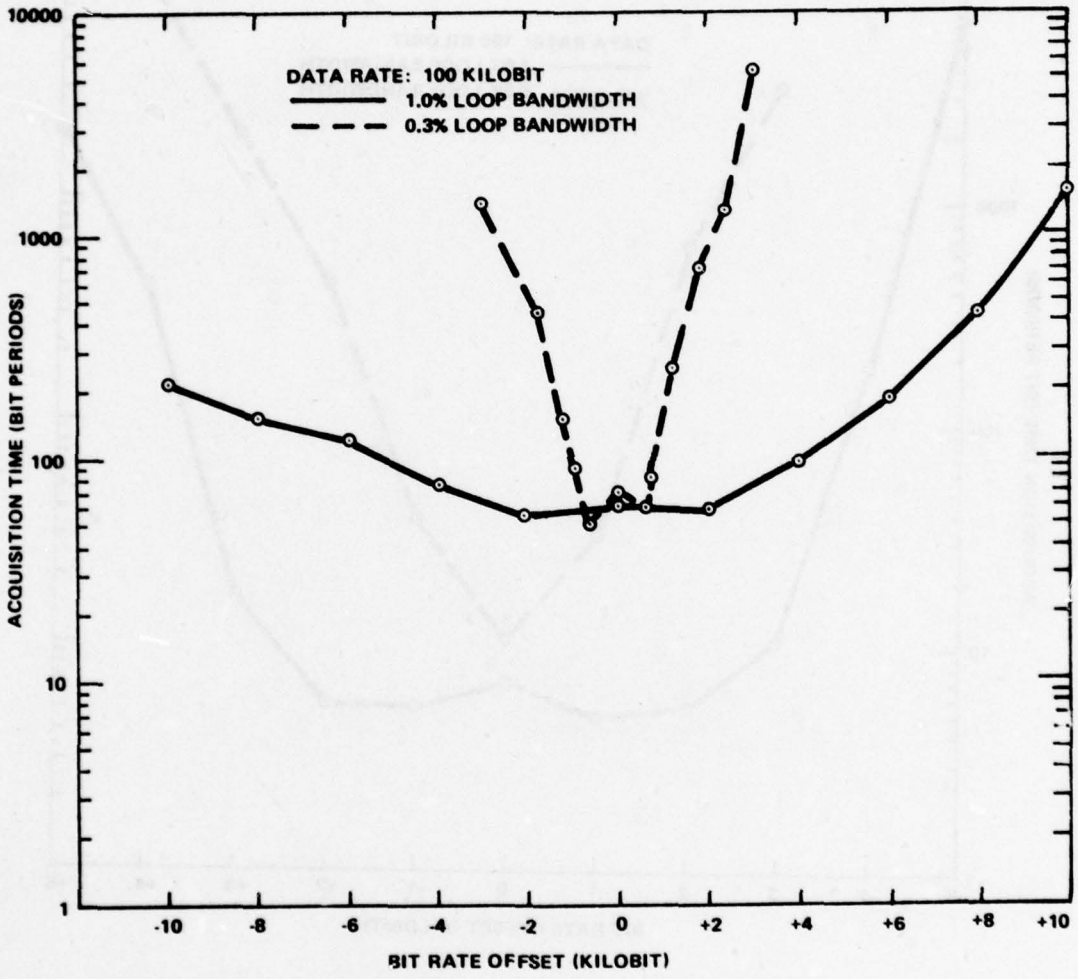


Figure 20. Acquisition Time Versus Bit Rate Offset for Bit Synchronizer A (100-Kilobit Rate).

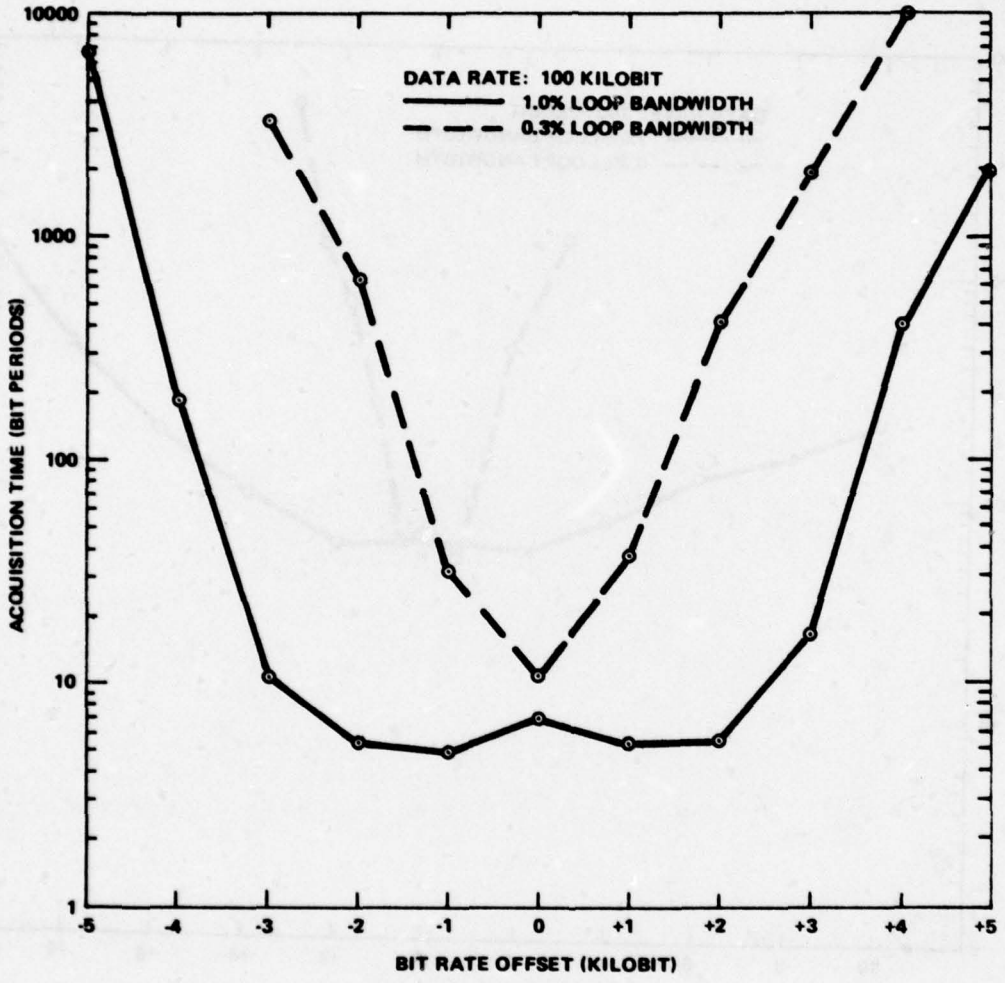


Figure 21. Acquisition Time Versus Bit Rate Offset for Bit Synchronizer B (100-Kilobit Rate).

kilobits, respectively. A comparison of the 0.3% loop bandwidth data to the 1.0% loop bandwidth data, figure 21, reveals increased sensitivity of acquisition time to input data rate changes with the 0.3% loop bandwidth selection. The data taken with the 0.3% loop bandwidth show that maximum acquisition time increases of 3508 bit periods and 9032 bit periods occur at input data rates of 97 kilobits and 104 kilobits, respectively. A minimum acquisition time of approximately 11 bit periods was measured when the input data rate was set equal to the selected bit rate of the bit synchronizer, corresponding to a zero data rate offset. The data measurements reveal that acquisition time increases as the input data rate departs from the selected bit rate of the bit synchronizer, but that the 1.0% loop bandwidth is less sensitive to changes in the input data rate in the region near the selected bit rate.

Jitter

Performance tests were conducted to determine how well a bit synchronizer can maintain clock synchronization when the input data rate is modulated with sinusoidal jitter components. Measurements were made to determine the peak bit rate deviation (Δf) and modulation frequency (f_m) at which the bit synchronizers could produce an output signal having a bit slippage probability (BSP) in the range of 1×10^{-6} to 1×10^{-5}.

Performance measurements were taken for two input data rates, with two loop bandwidth selections and an input SNR of 15 dB. The input data rates and loop bandwidths used were 1.0 and 0.1 megabit and 1.0% and 0.3%, respectively. The equipment set up for these tests is shown in figure 22.

The results of the jitter performance measurements are shown in figures 23 through 26. The area shown below the line connecting the measured data points represents bit slippage probability performance which is better than 1×10^{-5}.

Measured data are plotted in the figures to show the response of the bit synchronizers to Δf and f_m while maintaining a BSP of 1×10^{-6} to 1×10^{-5}. The data shown in the figures reveals that bit synchronizers A and B were able to maintain clock synchronization over a wide range of variations in the jitter components. The measured responses exhibit similar tendencies in that the values of Δf remain constant, decrease, and then increase abruptly as the f_m component is progressively increased. Each measured data point represents the maximum value of Δf for a constant f_m under which the bit synchronizer can produce data with a BSP in the range of 1×10^{-6} to 1×10^{-5}. A summary of the measured Δf and f_m values is presented in table 4.

Examination of the data listed in table 4 and shown in the figures reveals correlations between loop bandwidth and the values of Δf and f_m. The data for bit synchronizer A reveals a Δf (peak jitter) for low values of f_m which is approximately equal to 10 to 11 times the loop bandwidth selected; this represents the expected tracking range. This relationship appears to be the same for both bit rates and for both loop bandwidth selections. The data for bit synchronizer B indicates the existence of a similar relationship between Δf and loop bandwidth; but the results are not the same as those for bit synchronizer A. The data taken for bit synchronizer B reveals the Δf for low values of f_m to be in an order of 5 to 6 times the 1.0% loop bandwidth and 32 times the 0.3% loop bandwidth. These measured Δf values correlate to approximately 5% of the selected bit rate with the 1.0% loop bandwidth selection and to 10% of the selected bit rate with the 0.3% loop bandwidth.

Continued examination of the data in the table and figures reveals a correlation between the f_m value appearing at minimum Δf and the loop bandwidth selected. The data taken for bit synchronizer A reveals a direct 1:1 relationship between the f_m value at minimum Δf and the loop bandwidth selection. The data for bit synchronizer B shows a similar relationship, but with more variations in the measured f_m values.

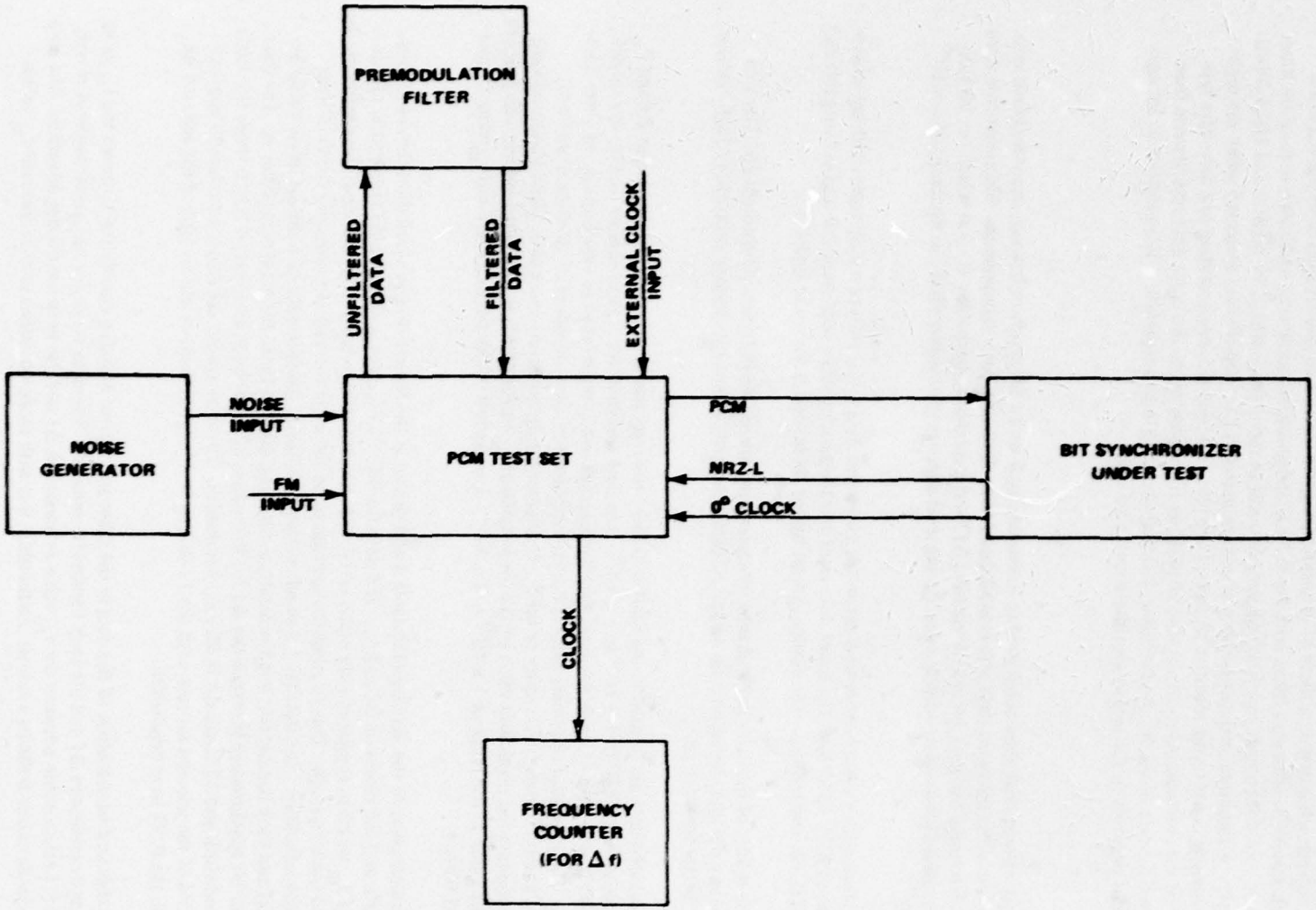


Figure 22. Jitter Equipment Setup.

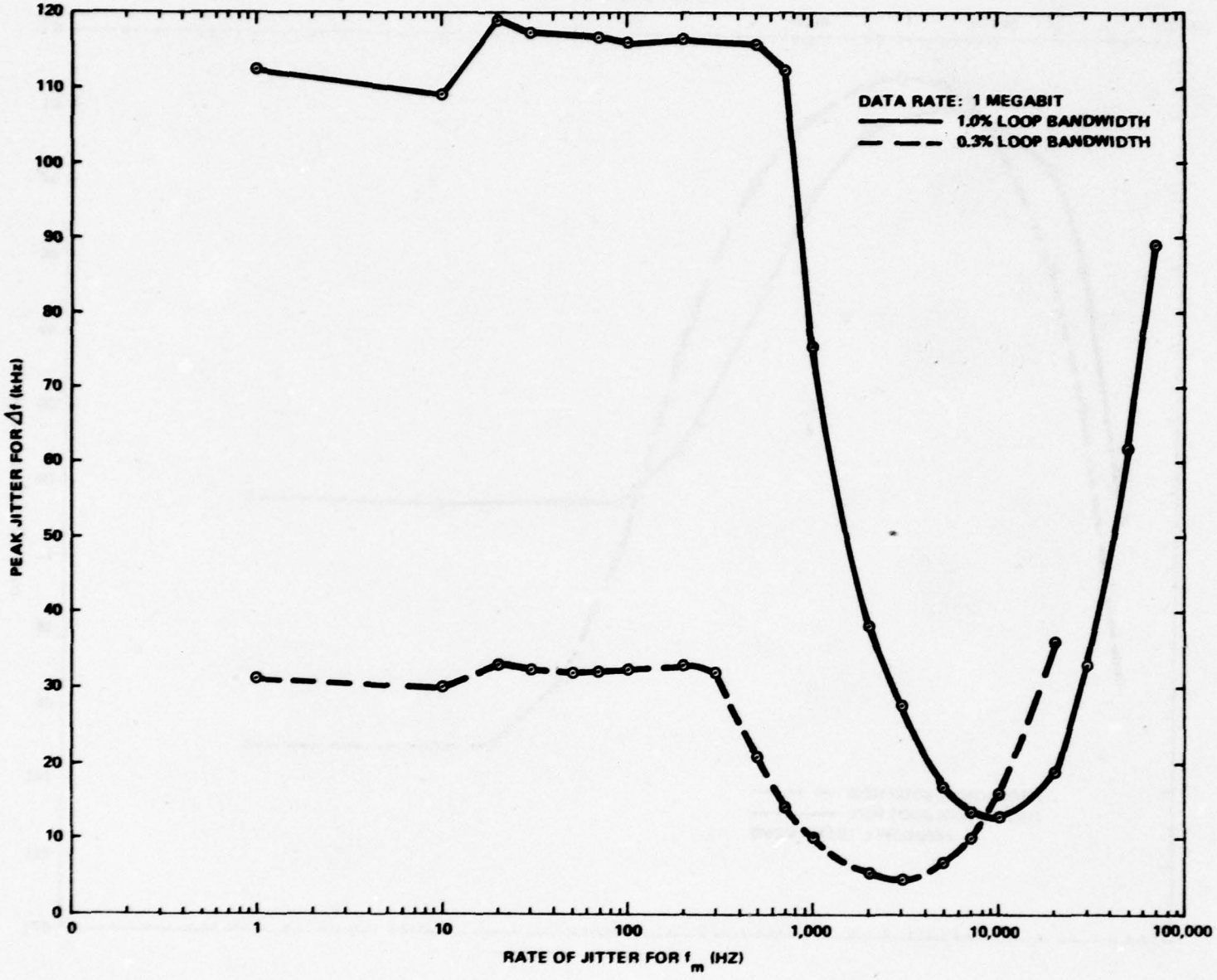


Figure 23. Jitter Response for Bit Synchronizer A (1-Megabit Rate).

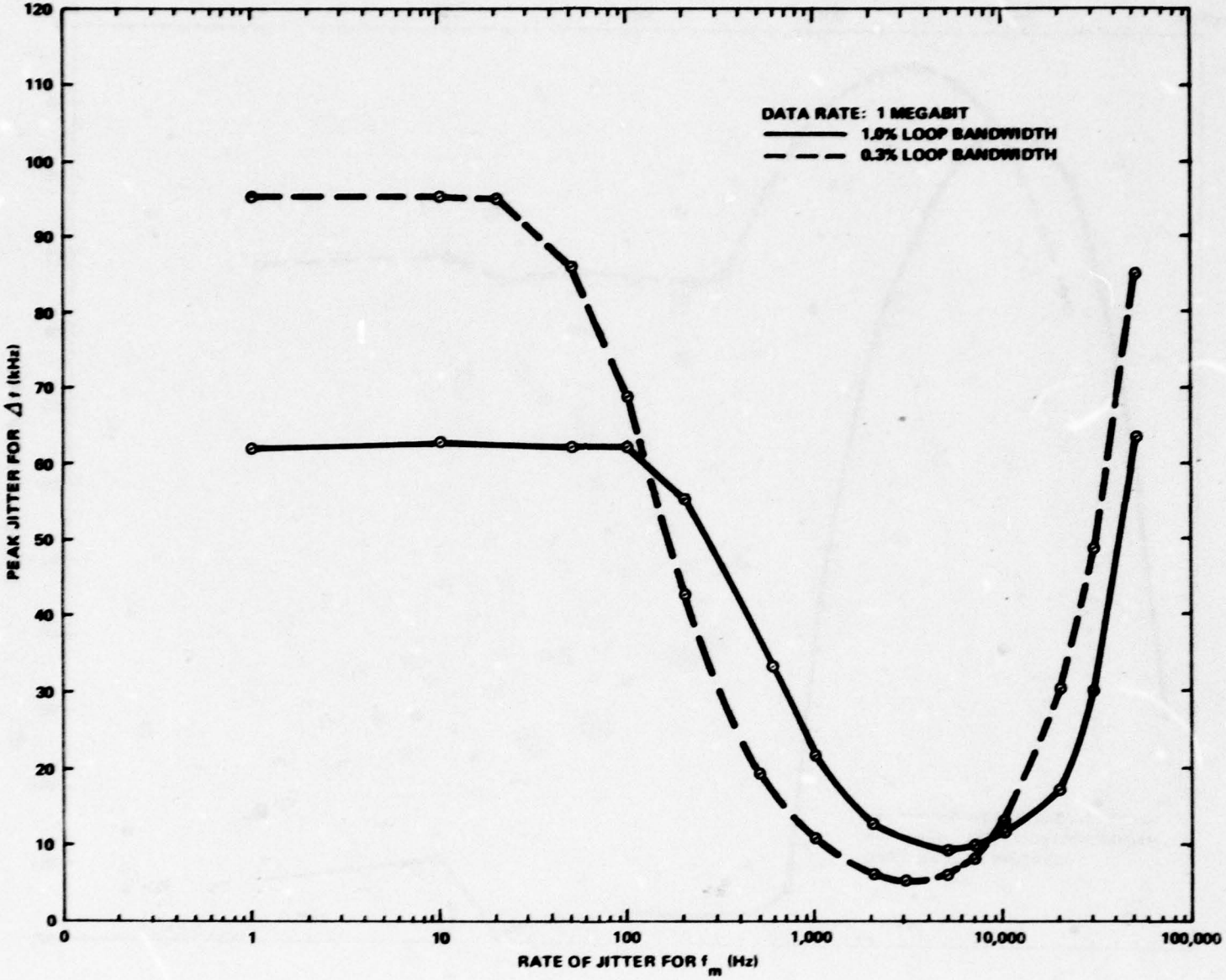


Figure 24. Jitter Response for Bit Synchronizer B (1-Megabit Rate).

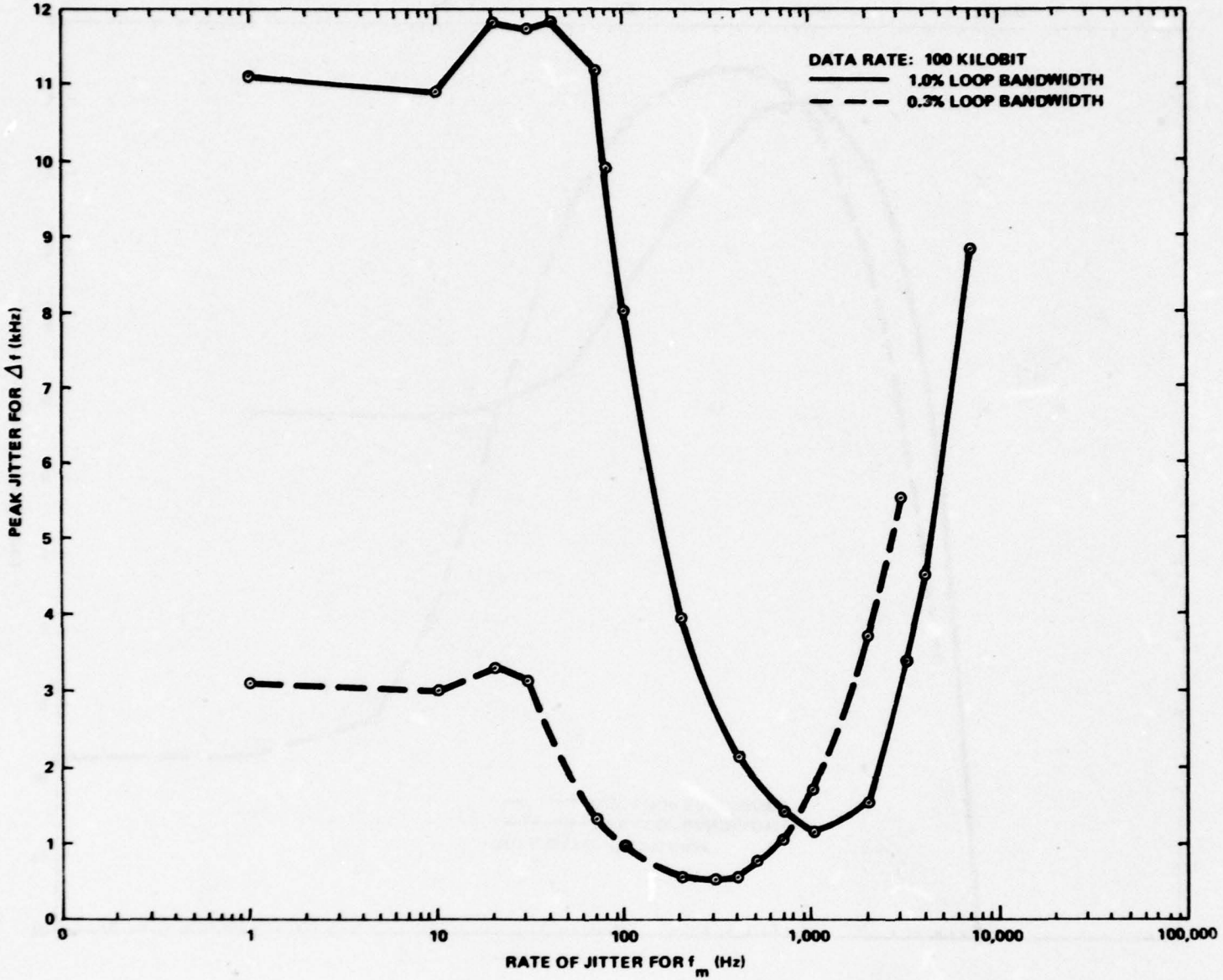


Figure 25. Jitter Response for Bit Synchronizer A (100-Kilobit Rate).

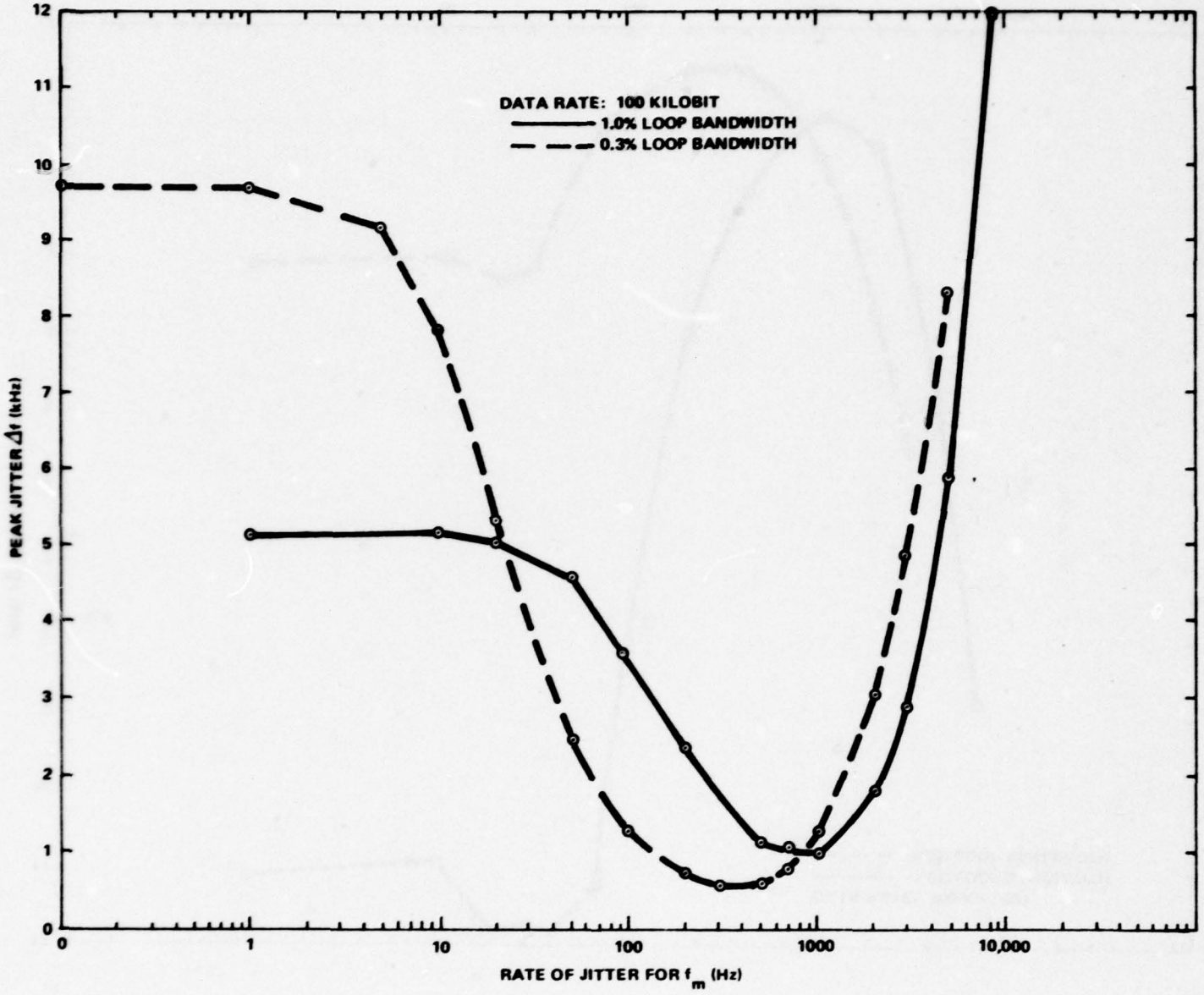


Figure 26. Jitter Response for Bit Synchronizer B (100-Kilobit Rate).

Table 4. Summary of Maximum Jitter Components

Selected Bit Rate	Jitter						Bit Synchronizer Setting	
	Maximum Δf		Minimum Δf					
			Δf		f_m		LBW	A or B
Mb	kHz	%BR	kHz	%BR	kHz	%LBW	%	
1.0	110-120	11-12	12.5	1.25	10	1	1	A
0.1	10.9-11.8	10.9-11.8	1.1	1.1	1	1	1	A
1.0	30-32.5	3.0-3.25	5	0.5	3	0.3	0.3	A
0.1	3.0-3.3	3.0-3.3	0.5	0.5	0.3	0.3	0.3	A
1.0	62	6.2	9.8	0.98	7	0.7	1	B
0.1	5.15	5.15	1	1	1	1	1	B
1.0	95	9.5	5	0.5	3	0.3	0.3	B
0.1	9.7	9.7	0.55	0.55	0.4	0.4	0.3	B

CONCLUSIONS

Bit Error Probability

The general shape of each BEP versus SNR plot is similar to that predicted by theory for ideal BEP response. The results of the tests indicate that BEP is affected by data rate, loop bandwidth selection, and input SNR. All of the BEP test results indicate that the 0.3% loop bandwidth selection provides BEP responses which are better than or equal to the responses measured with the 1.0% loop bandwidth.

Comparisons were made to show the differences between experimental measurements and theoretical response of filtered data for each bit synchronizer. The comparison revealed that both bit synchronizers did produce output signals having a BEP within 1 dB of theoretical. However, to evaluate overall system performance, it is also necessary to consider bit slippage probability as an important measure of response. Bit errors occurring within the frame synchronization word, worst case, can result in loss of an entire frame of data. However, bit slippage does indeed cause the loss of entire frames of data. It is therefore important to consider both BEP and BSP when making judgments concerning overall systems performance.

Bit Slippage Probability

The data in figures 9 through 12 show that BSP increases abruptly as the SNR of the input signal is degraded. The data also show that BSP is affected by loop bandwidth and bit rate selections and that the two bit synchronizers do not produce the same results when tested under identical conditions.

The most apparent observation is that both bit synchronizers produced different BSP results with the 1.0% loop bandwidth selection at the 1.0- and 0.1-megabit data rates. The performance measurements made with bit synchronizer A using the 1.0% loop bandwidth are different for each data rate. The slope of the data taken at the 100-kilobit data rate increases more rapidly than at the 1.0-megabit data rate. Improved BSP performance occurs with the 0.3% loop bandwidth selection at both data rates.

The performance measurements made with bit synchronizer B using the 1.0% loop bandwidth are also different for each data rate; however, the difference remains approximately constant over the range tested. Again improved performance results when using the 0.3% loop bandwidth at both data rates.

In general, the bit synchronizer instructions and specifications defined synchronization in terms of maintaining bit synchronization at specific threshold limits. Observations of the BSP results from the two bit synchronizers reveal differences in performance characteristics. The differences in the basic definitions for maintaining synchronization do not provide the expected compatibility required by users of PCM synchronization systems, thus promoting the need for special testing to determine performance characteristics. Since BSP performance is affected by loop bandwidth and data rate selections, an important requirement would be to have knowledge of BSP performance over a range of input signal SNRs at various bit synchronizer control settings.

Acquisition Time Versus SNR

Experimental test results show that the acquisition time, as measured in bit periods, of bit synchronizers A and B is affected by the SNR of the input signal. The data measurements reveal abrupt changes in acquisition times at low SNR settings. Measurements also reveal that an apparent SNR threshold exists beyond which insignificant changes in acquisition time occur with increasing SNR. The results obtained during this investigation provide performance information that would be difficult to determine from specifications given by equipment manufacturers.

The manufactures of bit synchronizers A and B provide performance specifications which cannot be easily related to experimental performance evaluation. Manufacturer specifications indicate that synchronization will occur within a specified acquisition time if the input signal has a transition density of 50% and if the input bit rate is within ±2% of the selected rate. In addition, the specifications for bit synchronizer A include a minimum SNR of greater than or equal to 15 dB at a loop bandwidth of 1.0%. The specifications for bit synchronizer B do not include the SNR and loop bandwidth requirements. Performance measurements indicate that bit synchronizer A does indeed meet its acquisition time specifications, but a degree of uncertainty exists regarding the performance of bit synchronizer B due to the absence of signal and loop bandwidth constraints. When the signal and bandwidth constraints given for bit synchronizer A are applied to the test results, both bit synchronizers would provide acceptable acquisition time response.

Observations of performance were made to determine the sensitivity of acquisition time to loop bandwidth selection and input data rate. The data shown in the figures reveal that bit synchronizer A and bit synchronizer B do not provide the same response when subjected to identical test constraints. Bit synchronizer B provided the most uniform and best acquisition time responses at both bit rates when using the 0.3% loop bandwidth selection. The acquisition times for bit synchronizer A at the two loop bandwidth settings were nearly the same at the 100-kilobit rate. The acquisition time response of bit synchronizer A with the 0.3% loop bandwidth selection was greater than for bit synchronizer B; however, the acquisition times were approximately the same at both bit rates. The acquisition time response for bit synchronizer A and the 1.0% loop bandwidth improved at the lower bit rate. Bit synchronizer B provided degraded response times with the 1.0% loop bandwidth at the lower bit rate. Therefore, the data shown in the figures reveal that with the same input signal conditions the results between the two bit synchronizer systems are not the same.

Acquisition Time as a Function of Input Bit Rate Offsets

Performance measurements made with bit synchronizers A and B show that acquisition time is a function of data rate, the difference between the input data rate and the data rate selected on the bit synchronizer (bit rate offset), and the loop bandwidth selection. The results of the performance tests show the measured acquisition times increasing abruptly as the input data rate departs from the selected bit rate of the bit synchronizer. Minimum measured acquisition times for bit synchronizers A and B with either loop bandwidth are in ranges of 42 through 70 bit periods and 7 through 18 bit periods, respectively, and occurred with input data rates which were at or very near the selected bit rate of the bit synchronizers. The minimum acquisition time response for both bit synchronizers appeared to be somewhat constant over a range of input data rate changes corresponding to ±20% of the system tracking range. Both bit synchronizers provided acquisition times which were equal to or less than 105 bit periods within the ±20% input data range.

Improved acquisition time performance measurements occurred between the 1.0% and 0.3% loop bandwidths when using the 1.0% loop bandwidth selection with input data rate offsets in the ranges corresponding to ±40% through ±100% of the system tracking ranges. However, the improved acquisition time response was more significant when using bit synchronizer B than when using bit synchronizer A. The response differences measured during the tests would be difficult to determine from equipment specifications.

The manufacturer's acquisition time specifications given as a function of input data rate offsets (bit rate offset) for bit synchronizers A and B are limited in scope and definition. A few generalized examples of limitations include performance specifications for one loop bandwidth when three selections are available, and acquisition time performance relative to two ranges of input data rate offset. Limitations in definition include specification statements which do not include appropriate reference or signal condition

information. In general it becomes difficult to determine specified performance characteristics of bit synchronizers without the references with which to make comparisons.

Jitter

The performance measurements show the characteristic responses of bit synchronizers A and B when input data contains sinusoidal jitter components. The results of the measurements reveal the relationships between loop bandwidth, tracking range, input data rate, and Δf to f_m components of jitter for an input SNR of 15 dB.

The Δf jitter component which may be combined with the input data when using bit synchronizer A is approximately 10 to 11 times, at low f_m values, the loop bandwidth selected by both data rates and both loop bandwidths. The data for bit synchronizer B show relationships which are different from bit synchronizer A and also different for each loop bandwidth selected. The Δf, when using bit synchronizer B, appears in the order of approximately 5 to 6 times, at low f_m values, the loop bandwidth of 1.0% and approximately 32 times the loop bandwidth of 0.3%. The results show that bit synchronizer A provides a fixed relationship between maximum Δf and loop bandwidth and that bit synchronizer B provides an increasing Δf as the loop bandwidth is narrowed (0.3%). Since the tracking range of the loop bandwidth selection determines the Δf jitter component that can be tracked out at low jitter frequencies, it must be clearly defined so that it can be used effectively in telemetry system applications.

Bit synchronizers A and B exhibited an apparent immunity to the effects of high frequency data jitter when BSP was used as the criterion for performance measurements. The phase-locked loop in the bit synchronizer does not respond to the high frequency jitter components; therefore, bit slips are detected only when the phase difference between the average clock frequency and the actual clock frequency exceeds $\pm 180^{o}$. The phase error is proportional to the product of the frequency deviation (Δf) and the amount of time (period) that a frequency difference exists. Since the period is inversely proportional to the modulating frequency (f_m), the phase error is proportional to the ratio of Δf and f_m ($\Delta f/f_m$). Therefore, as f_m is increased the Δf for a given phase error is also increased. The result is that the phase-locked loop does not track the changing bit rate; hence, the system cannot correctly determine the bit boundaries necessary to establish sampling intervals. With this condition the BEP can increase significantly while the BSP remains constant. BEP is a very important measure of data quality and must be considered simultaneously with BSP when attempting to relate overall bit synchronizer system performance.

APPENDIX

THEORETICAL DERIVATION OF BIT ERROR PROBABILITY

The purpose of this appendix is to outline the method used to calculate the theoretical bit error probability (BEP). A table listing the BEP versus signal-to-noise ratio (SNR), values is included for the case of a filtered PCM signal containing additive, white, gaussian noise.. The block diagram model used for the theoretical derivation is shown in figure 27.

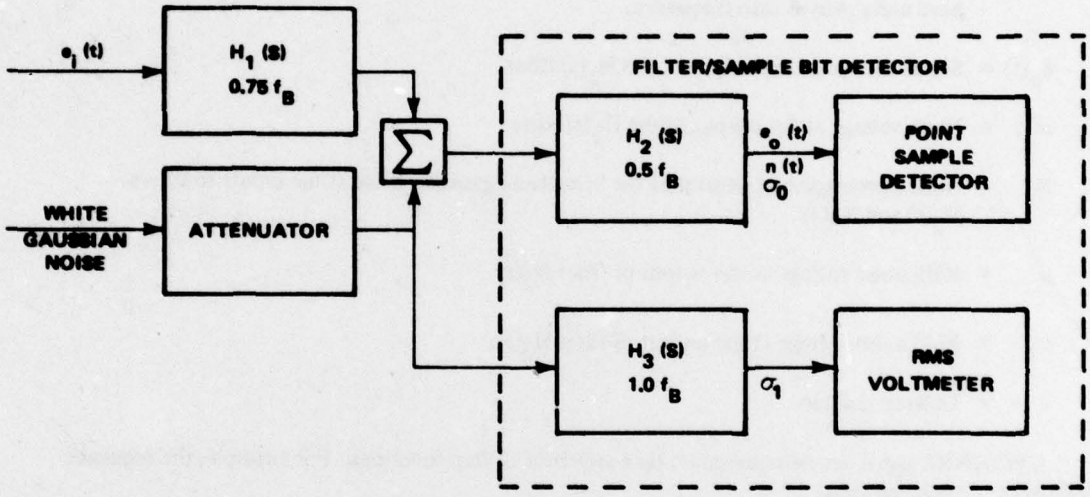


Figure 27. Block Diagram Model for Theoretical Derivation.

where

$e_i(t)$ = Random PCM/NRZ signal with peak amplitude of E volts ($V_{pp}/2$ in body of report).

f_B = Bit rate (bits per second).

$H_1(s)$: 6 pole Bessel low pass premodulation filter with the -3 dB bandwidth equal to 0.75 f_B.

$H_2(s)$: 6 pole Bessel low pass filter with the -3 dB bandwidth equal to 0.50 f_B. This filter is an integral part of the filter/sample bit detector.

$H_3(s)$: 4 pole Butterworth low pass filter with the -3 dB bandwidth equal to 1.0 f_B. This filter is used to determine the noise power spectral density N. All three filters are assumed to have unity gain at zero frequency.

$e_o(t)$ = Signal voltage at the output of the $H_2(s)$ filter.

$n(t)$ = Noise voltage at the output of the $H_2(s)$ filter.

N = Noise power spectral density of the broadband gaussian noise at the inputs to filters $H_2(s)$ and $H_3(s)$.

σ_o = RMS noise voltage at the output of filter $H_2(s)$.

σ_1 = RMS noise voltage at the output of filter $H_3(s)$.

s = Laplace variable.

A PCM/NRZ signal can be represented by a sequence of step functions. For example, the sequence ...00010111... can be written

$$e_i(t) = u(t) - u(t - T) + u(t - 2T) \qquad (1)$$

where time begins at the leading edge of the first "1" bit and T is the bit period. The Laplace transform of (1) is

$$E_i(s) = \frac{1}{s} (1 - e^{-Ts} + e^{-2Ts}) \qquad (2)$$

The Laplace transform of the output signal $e_o(t)$ can now be expressed as

$$E_o(s) = H_1(s) H_2(s) E_i(s) \qquad (3)$$

which combined with (2) becomes

$$E_o(s) = \frac{H_1(s) H_2(s)}{s} (1 - e^{-Ts} + e^{-2Ts}) \qquad (4)$$

The first term of (4) is seen to be the Laplace transform of the step response a(t) of the two filters $H_1(s)$ and $H_2(s)$ in cascade. The second and third terms of (4) are seen to be the Laplace transforms of delayed versions of the step response. Thus the response of the two filters to the bit sequence ...00010111... can be written.

$$e_o(t) = a(t) - a(t-T) + a(t-2T) \tag{5}$$

and it is clear that the response to any desired sequence can be easily written. Computer programs exist for inverting high order Laplace transforms. Simple programs can be written for performing the summations involved in (5). For the conditions shown in figure 1 the calculated response to various bit sequences showed that only the preceding and following bits significantly influenced the output amplitude at the time of sampling. Thus, concentrating on the amplitude of a "1" bit, only the four bit sequences 010, 011, 110, and 111 had to be examined. It was also found that the optimum sampling time was delayed by 1.95 bit periods from the leading edge of the unfiltered bits. The amplitudes of the central "1" bit for these four sequences were found to be

$$\begin{aligned} e_{010} &= 0.755E \\ e_{011} &= 0.862E \\ e_{110} &= 0.893E \\ e_{111} &= 0.999E \end{aligned} \tag{6}$$

The probability that the central "1" bit is in error for each of these sequences can be expressed by

$$\begin{aligned} P_{010} &= P\left|n(t) > e_{010}\right| \\ P_{011} &= P\left|n(t) > e_{011}\right| \\ P_{110} &= P\left|n(t) > e_{110}\right| \\ P_{111} &= P\left|n(t) > e_{111}\right| \end{aligned} \tag{7}$$

and these probabilities can be expressed in terms of the normal probability density function p(n). For example

$$P_{010} = \int_{e_{010}}^{\infty} p(n)dn \tag{8}$$

where

$$p(n) = \frac{1}{\sigma_0\sqrt{2\pi}} e^{\frac{-n^2}{(2\sigma_0)^2}} \tag{9}$$

or (8) can be expressed in terms of the error function (often found in tables)

$$P_{010} = 0.5 - \text{erf}\, e_{010} = \text{erfc}\, e_{010} \tag{10}$$

Equation (10) gives the probability that a bit error occurs given that the sequence 010 has occurred. Let P_{010} be the probability that a given "1" bit is preceeded and followed by "0" bits. Since the signal and noise are independent the probability that an arbitrary bit error is associated with the bit sequence 010 is $P_{010}\,P_{010}$ and likewise for the other bit sequences.

Thus the expected bit error probability is

$$P_e = P_{010}\,P_{010} + P_{011}\,P_{011} + P_{110}\,P_{110} + P_{111}\,P_{111} \tag{11}$$

and since

$$P_{010} = P_{011} = P_{110} = P_{111} = 1/4 \tag{12}$$

(11) becomes

$$P_e = 1/4\,(P_{010} + P_{011} + P_{110} + P_{111}) \tag{13}$$

If the SNR (signal-to-noise ratio) is defined as the ratio of the signal energy per bit to the noise power per hertz then

$$SNR = \frac{E^2T}{N} \tag{14}$$

The power spectral density N (watts per hertz) is related to the mean square noise voltage σ_1^2 (watts for a 1 Ω load) at the output of the $H_3(s)$ filter by

$$\sigma_1^2 = \frac{N}{2\pi}\int_0^B |\,H_3(jw)\,|^2\,dw \tag{15}$$

which can be expressed in terms of the equivalent noise power bandwidth f_e by

$$\sigma_1^2 = N\,|\,H_3(0)\,|^2 f_{e3} \tag{16}$$

or since $|\,H_3(0)\,| = 1$ as

$$\sigma_1^2 = N\,f_{e3} \tag{17}$$

and likewise

$$\sigma_0^2 = N\,f_{e2} \tag{18}$$

From (17) the noise power spectral density can be expressed in terms of σ_1 by

$$N = \frac{\sigma_1^2}{f_{e3}} \tag{19}$$

from which (14) can be expressed in terms of σ_1

$$SNR = \frac{E^2\,Tf_{e3}}{\sigma_1^2} \tag{20}$$

By dividing (18) by (17) σ_0 is also expressed in terms of σ_1

$$\frac{\sigma_0^2}{\sigma_1^2} = \frac{f_{e2}}{f_{e3}} \tag{21}$$

or

$$\sigma_0 = \sqrt{\frac{f_{e2}}{f_{e3}}}\ \sigma_1 \tag{22}$$

From published tables for a 6 pole Bessel filter

$$f_e = 1.0381\ f_{3dB} \tag{23}$$

and for a 4 pole Butterworth filter

$$f_e = 1.0262\ f_{3dB} \tag{24}$$

which permits (22) to be written with a numerical proportionality factor

$$\sigma_0 = 0.7112\ \sigma_1 \tag{25}$$

The theoretical BEP values are listed as a function of SNR in table 5. The BEP values are plotted as a function of SNR in figure 28.

Table 5. Theoretical Bit Error Probabilities for a Filtered NRZ-L PCM Signal

Signal-to-Noise Ratio (dB)	Theoretical Bit Error Probability
0	1.1×10^{-1}
3	4.5×10^{-2}
6	8.9×10^{-3}
9	5.4×10^{-4}
12	3.8×10^{-6}
15	3.9×10^{-10}
18	6.2×10^{-18}

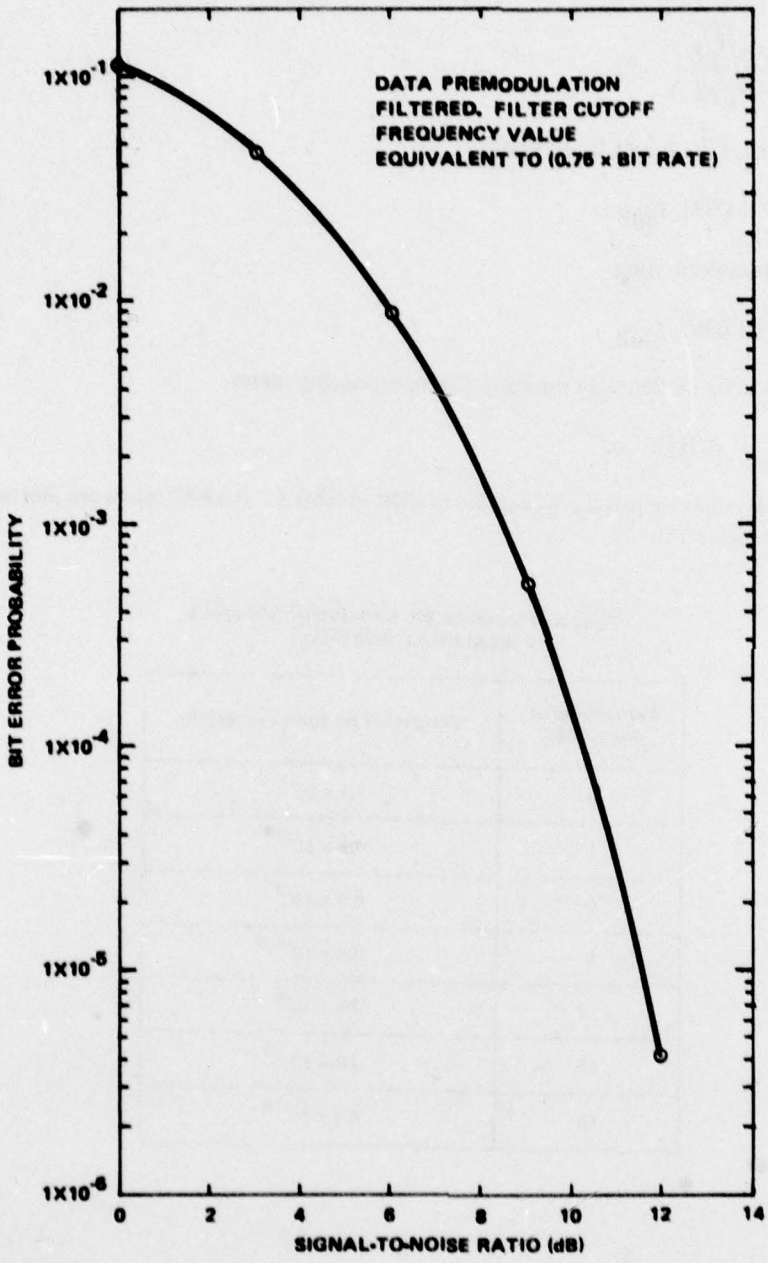


Figure 28. Theoretical Bit Error Probability Versus Signal-To-Noise Ratio for a Filtered NRZ-L PCM Signal.

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