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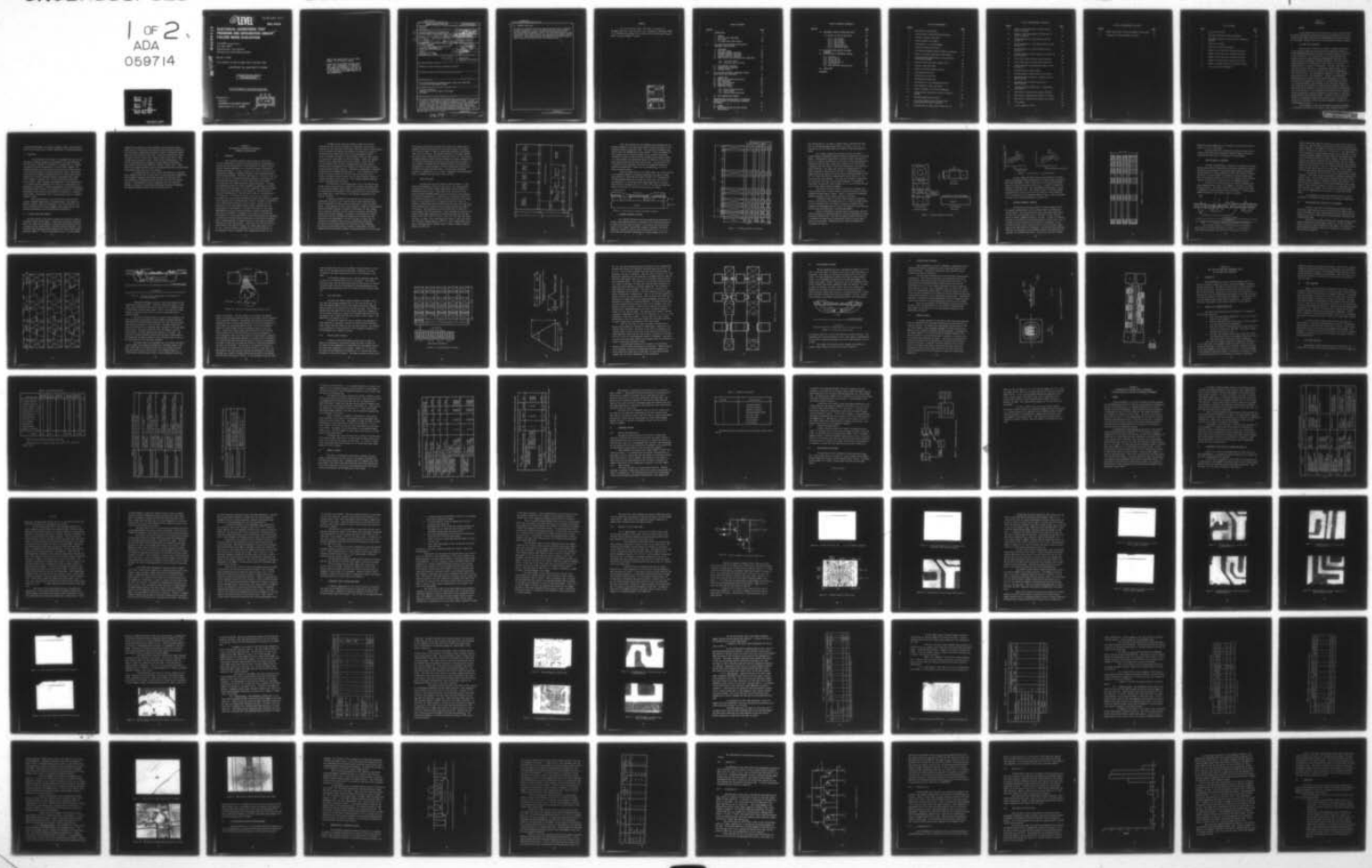

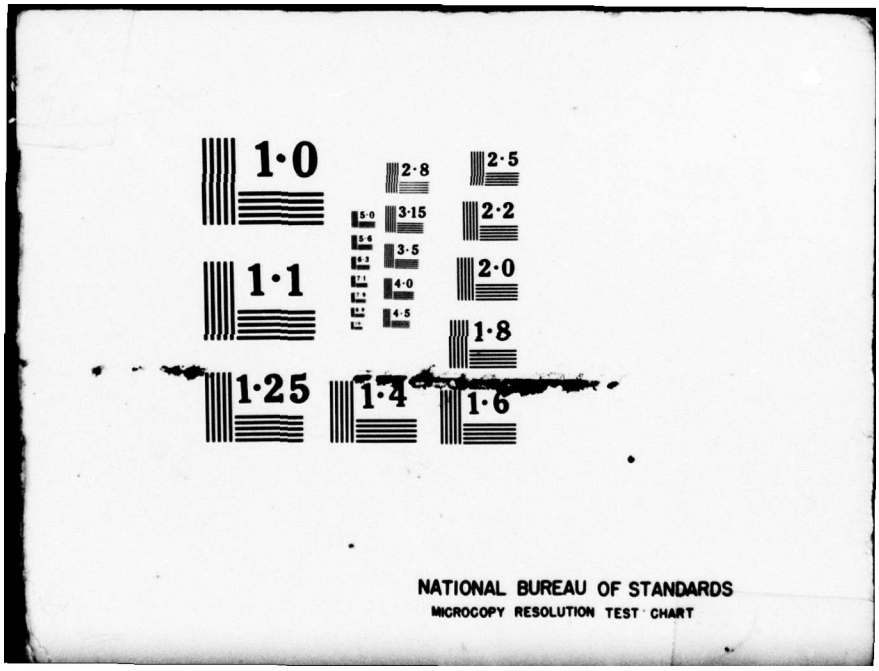
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DNA 4467F

ELECTRICAL OVERSTRESS TEST PROGRAM AND INTEGRATED CIRCUIT FAILURE MODE EVALUATION

The BDM Corporation
P.O. Box 9274
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Albuquerque, New Mexico 87119

26 April 1978

Final Report for Period May 1977—October 1977

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This final report describes the SOS diode test structures which will be used for empirical investigation of electrical overstress failure. The test structures, in which important physical parameters are varied, are described in detail and a test plan is presented for the overstress testing that will generate failure data for a sensitivity analysis of pulse power failure level as a function of junction area, epitaxial thickness, junction radius of curvature, doping level and metallization and diffusion spikes.

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20. ABSTRACT (Continued)

An electrical overstress failure mode and distribution study in integrated circuits is presented. Data on over 1200 devices which were tested on previous programs was analysed to determine failure modes on DTL, RTL, TTL, ECL, MOS and linear integrated circuits. The failure distributions on over 3,000 devices from several different test programs were reviewed to identify "mavericks." These "mavericks" were investigated for distinctive failure modes or unusual preirradiation electrical characteristics.

PREFACE

The following final report (CDRL A002) is submitted by The BDM Corporation, 2600 Yale Blvd., S.E., Albuquerque, New Mexico 87106 to the Defense Nuclear Agency in accordance with the deliverable requirements of Contract DNA001-77-C-0156.

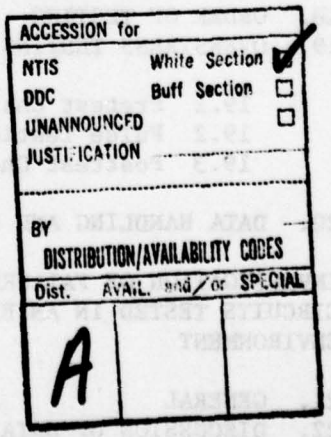


TABLE OF CONTENTS

Section		Page
I	INTRODUCTION	9
	1. GENERAL	9
	2. SOS DIODE TEST STRUCTURES	9
	3. TEST PLAN	10
	4. IC FAILURE MODE STUDY RESULTS	10
II	SOS DIODE TEST STRUCTURES FOR EMPIRICAL OVERSTRESS INVESTIGATIONS	12
	5. BACKGROUND	12
	6. TEST CHIP LAYOUT	14
	7. STANDARD REFERENCE STRUCTURE	16
	8. ENCLOSED REFERENCE STRUCTURE	20
	9. JUNCTION RADIUS OF CURVATURE	22
	10. METALLIZATION AND DIFFUSION SPIKE STRUCTURES	23
	10.1. Half Size Spikes	27
	10.2. Multiple Spike Structure	27
	11. FOUR-TERMINAL STRUCTURE	32
	12. INTERDIGITATED STRUCTURE	33
	13. EXPECTED RESULTS	33
III	TEST PLAN FOR ELECTRICAL OVERSTRESS TESTING ON SOS DIODE TEST STRUCTURES	36
	14. INTRODUCTION	36
	15. OVERALL TEST PROGRAM DESCRIPTION	36
	16. TEST STRUCTURES	37
	17. TEST DIODE SELECTION	37
	18. ORDER OF TESTING	41
	19. OVERSTRESS TESTING	44
	19.1 Pretest Characterization	44
	19.2 Pulse Testing	44
	19.3 Posttest Characterization	46
	20. DATA HANDLING AND STORAGE	46
IV	INVESTIGATION OF FAILURE MODES IN INTEGRATED CIRCUITS TESTED IN AN ELECTRICAL OVERSTRESS ENVIRONMENT	49
	21. GENERAL	49
	22. DISCUSSION OF DATA BASE FOR FAILURE MODE ANALYSIS	50

TABLE OF CONTENTS (CONCLUDED)

Section		Page
23.	INTEGRATED CIRCUIT FAILURE MODE STUDY	55
	23.1 Results of Failure Mode Study	58
	23.1.1 DTL Circuits	58
	23.1.2 RTL Circuits	68
	23.1.3 TTL Circuits	73
	23.1.4 ECL Circuits	75
	23.1.5 Linear Circuits	77
	23.1.6 MOS Failure Modes	80
24.	IC FAILURE MODE ANALYSIS ON OTHER PROGRAMS	82
25.	INVESTIGATION OF "MAVERICK" DEVICES	83
	25.1 N7400 Unit 4	87
	25.2 912 HC Unit 83	87
	25.3 945 HC Unit 67	89
	25.4 CD 4000 AE Unit 21	89
	25.5 μA747 Unit 67	90
	25.6 Other Maverick Identification	90
26.	CONCLUSIONS	93
	REFERENCES	97

LIST OF ILLUSTRATIONS

Figure		Page
1	SOS diode test chip layout.	15
2	Cross section of basic SOS diode structure.	16
3	Standard reference structures.	17
4	Typical geometry for diodes.	19
5	Anticipated $J_f - N_D$ relationships.	20
6	Enclosed reference structures.	21
7	IC Transistor showing junction radius of curvature.	22
8	Radius of curvature structure in SOS diodes.	24
9	Cross-sectional representation of metallization and diffusion spikes.	25
10	Details of diffusion spike from p+ to n++.	26
11	Multiple spike structures.	28
12	Details of multiple spike structure.	29
13	Four-terminal structure.	31
14	Lateral base current flow.	32
15	Interdigitated transistor.	34
16	SOS structure of an interdigitated device.	35
17	Block diagram of pulse test setup.	47
18	Circuit schematic of one 946 HC NAND gate.	59
19	Pretest curve tracer photo of unit 50 (input to ground).	60
20	Photomicrograph of 946 HC chip.	60
21	Curve tracer photo of unit 50 after third overstress pulse (input to ground).	61
22	Junction short on input diode, 946 HC unit 50.	61

LIST OF ILLUSTRATIONS (Continued)

Figure		Page
23	Pretest curve tracer photo of 946 HC unit 52 (input to ground).	63
24	Posttest curve tracer photo of 945 HC unit 52 (input to ground).	63
25	Photomicrograph of D_1 junction short on 946 HC unit 52.	64
26	Photomicrograph of Q, (EB) junction short on 946 HC unit 52.	64
27	Photomicrograph of D_2 junction short on 946 HC unit 52.	65
28	Photomicrograph of output transistor C-E short on 946 HC unit 59.	65
29	Curve tracer photo of 946 HC unit 59 pretest.	66
30	Curve tracer photo of 946 HC unit 59 posttest.	66
31	Photomicrograph of metallization burnout on 946 HC unit 69.	67
32	Photomicrograph of 908 HC adder.	71
33	Photomicrograph of 908 HC buffer chip unit 50.	71
34	Photomicrograph of resistor - resistor short on 908 HC unit 50.	72
35	Photomicrograph of emitter base short on 908 HC unit 50.	72
36	Photomicrograph of N7400F unit 7, illustrating clamp short.	75
37	SEM picture of diode junction short on N5710T.	81
38	SEM picture of metallization burnout on a µA747.	81
39	SEM picture of metallization burnout on an LM111.	82
40	I^2L inverter.	84
41	Circuit diagram of 912 HC.	88

LIST OF ILLUSTRATIONS (Concluded)

Figure		Page
42	MC846 Input failure voltage histogram, 44-μsec pulse.	91
43	Histogram of failure voltages for μA723	94

LIST OF TABLES

Table		Page
1	SOS diode structures.	38
2	SOS diode structures physical dimensions.	39
3	SOS diode structures to be tested for sensitivity analysis.	42
4	Priority of testing.	45
5	Electrical overstress programs.	51
6	Summary of DTL electrical overstress failures.	69
7	Summary of RTL electrical overstress failures.	74
8	Summary of TTL electrical overstress failures.	76
9	Summary of ECL electrical overstress failures.	78
10	Summary of LINEAR electrical overstress failures.	79
11	List of potential "MAVERICKS."	86

SECTION I
INTRODUCTION

1. GENERAL

The following final report documents the results of the Electrical Overstress Phenomenology Program conducted by The BDM Corporation for the Defense Nuclear Agency (DNA) under the DNA/MIRADCOM (Army Missile Research and Development Command) Electrical Overstress Hardness Assurance Program.

2. SOS DIODE TEST STRUCTURES

The first part of this report presents a detailed description of the test structures that will be used for the empirical studies in the DNA/MIRADCOM program and discusses the rationale behind the selection of each test device. The test structures are diodes fabricated on a sapphire substrate using conventional complementary metal oxide semiconductor/silicon on sapphire (CMOS/SOS) processing. The SOS structure permits fabrication of a physical test device which is a horizontal representation of a vertical cross section. This thin (less than 1 μm) cross section, when laid out on a transparent sapphire wafer, can be observed optically for hot spot formation and eventual filamentation which causes failure. The experimental arrangement for these studies is described fully by Dr. Paul Budenstein[1]. Because this experimental method allows one to study the basic physical mechanisms of hot spot formation and filamentation it provides an excellent means to explore, in a controlled fashion, the dependence of the electrical overstress pulse power failure threshold on certain physical parameters which have been identified by analytical or empirical investigations as influencing failure distributions. Such parameters include junction area, background doping concentration, epitaxial thickness, junction radius of curvature, and metallization and diffusion spikes. Structures are also included to allow for investigation of how the location and size of hot spots are effected by lateral base current flow and the geometric variables in an interdigitated structure.

Each category of structures representing a parameter variable is discussed with respect to the analytic and/or empirical basis for

selecting the parameter, the range of parameter values, and any limitations on the structure due to either fabrication or testing constraints.

3. TEST PLAN

The second part of the report is a proposed test plan for the electrical overstress testing to be performed on the test structures. The test plan is intended to be general in the sense that it discusses the overall empirical investigation of the SOS diodes, however, the detailed portions of the plan are directed toward the testing required to obtain data necessary to generate sensitivity curves. These sensitivity curves are graphical representations of the pulse power failure threshold (P_f) versus a physical parameter (epitaxial width, doping level, radius of curvature, etc.) for several different values of a third variable. These parametric representations of the sensitivity of P_f to various physical parameters will allow one to judge whether the dependence is sufficient to require investigation of terminal electrical measurements which correlate to the parameter in question. Such terminal measurements would be used to help identify the location of a specific device within a distribution of P_f's and thus would serve as a hardness assurance screen.

The detailed portion of the test plan for the sensitivity analysis addresses sample sizes, testing preference (with respect to physical parameter variation represented by the test structure), electrical overstress testing (test equipment, pulse widths and pre- and posttest measurements), and data handling and transferral.

4. IC FAILURE MODE STUDY RESULTS

The final section of the report presents the results of a study of integrated circuit failure modes. In this study electrical overstress data on over 3000 ICs was examined to determine failure mode as well as to examine failure distributions to identify "maverick" behavior. Data from electrical overstress programs conducted for the Air Force Weapons Laboratory (AFWL),[2, 3] Rome Air Development Center,[4] and the Boeing

Company[5] were reviewed and, where possible, failure modes were determined from pre- and posttest electrical data and microscopic examination. The failures were categorized and listed in terms of predominant failure modes for diode-transistor logic (DTL), resistor-transistor logic (RTL), transistor- transitor logic (TTL), emitter-coupled logic (ECL), linear and MOS devices stressed in input, output and V_{CC} configurations. The failure distributions were examined to identify devices whose pulse power failure level was well below the "nominal" failure level. These devices were examined carefully for any distinguishing pretest characteristics which might explain their low failure levels.

The primary objective of the failure mode study was to identify which component within the IC failed first in each overstress configuration. Any topological variations which might influence the electrical overstress hardness of otherwise electrically identical ICs were of special interest. Preirradiation electrical parameters were also carefully examined to determine if devices with abnormally low failure thresholds had exhibited abnormal pretest electrical characteristics.

SECTION II
SOS DIODE TEST STRUCTURES FOR EMPIRICAL OVERSTRESS INVESTIGATIONS

5. BACKGROUND

Some fundamental empirical work directed at identifying the basic mechanisms of electrical overstress failure in semiconductor devices has been performed by Dr. Paul Budenstein[1] of Auburn University using an improved application of a technique originally developed by Sunshine and Lampert.[6] In this technique, thin lateral junction diodes, fabricated by Rockwell on sapphire substrates, were observed optically during second breakdown. The diode, fabricated in an epitaxial film less than 1 μm thick on a transparent sapphire substrate, was strobed with a high intensity light source at various times during an electrical overstress pulse and viewed through an ordinary microscope. By repeatedly pulsing the diode into second breakdown and observing it at different times from the initation of the pulse, Budenstein studied the growth of hot spots and their physical characteristics. This was possible since the transmissivity of the thin silicon film is a strong function of temperature. In studying the nature of the hot spot formation and growth, the test structure dimensions and the overstress test conditions in the original work by Budenstein were chosen on the basis of availability and for good optical resolution of the hot spots. Neither the test structures nor the test conditions were totally consistant with real system devices or environments. The empirical portion of the present DNA/MIRADCOM electrical overstress program is aimed at extending the application of Budenstein's technique to the study of structures more representative of actual semiconductor devices and exploring the dependence of electrical overstress failure threshold on various physical parameters which, through analytical or empirical results, have indicated possible influence on failure distributions. These structures will be tested at pulse widths in the range of interest for systems application (0.1 to 10 μs). Previous studies by Budenstein were conducted primarily at pulse widths of 100 μs or greater with a minimum pulse width of 5 μs.

Although the SOS structure provides a means for optically observing hot spots and is convenient for simulating vertical cross sections in a well controlled "horizontal" structure, several characteristics of the structure will require both analytical and empirical studies to correlate the SOS diode results with actual semiconductor devices. First, the sapphire subtrate is a better thermal conductor than silicon and thus acts as a heat sink for thin film diodes. Second, the sapphire substrate has a rather high surface defect density. Thus, when the silicon epitaxial layer is grown, stacking faults and other defects associated with the mismatch of the sapphire and silicon latices result in short minority carrier lifetime. This makes it impossible to fabricate transistors with reasonable characteristics. A third limitation is due to the "horizontal" rather than vertical junction structure, which results in an abrupt junction rather than the graded junction typical in a planar diffused vertical structure. Thus, doping gradient variations cannot be simulated with SOS diodes.

The discussion of the rationale which led to the selection and design of each test structure is organized by structure type rather than by the physical parameter being studied. This organization facilitates the presentation of the details of each individual set of test structures, even though there is some overlap in the variables represented by the specific structure.

In general the design of the SOS diode test structures was established to provide a set of test devices in which important device physical parameters or effects could be simulated in a well controlled manner. The parameters for which either analytic or empirical investigations indicated possible influence on failure distributions are area, doping level, epitaxial thickness, junction radius of curvature, metallization spiking, and diffusion spiking. In addition, the influence of lateral base current flow and interdigitated geometries on hot spot size and location will be investigated. An effort was made to insure that all structures and parameter values were as representative of bipolar structures as was possible within the limitations of SOS technology. All devices are being fabricated by Rockwell International, and their suggestions proved extremely valuable in defining several of the structures.

The principal fabrication constrait which limited the usable range of parameter values was encountered in the junction radius of curvature (r_j) structure where, in order to assure good resolution, the minimum value of r_j was limited. The lateral diffusion of the dopant material may cause a loss of definition for values less than 5 μm. The primary testing constraints concern epifilm thickness (to assure transparency of the film) and metallization pad size (to assure good probe contact). A 0.6-μm (which is standard for the CMOS/SOS process) film thickness is acceptable for testing although, in terms of simulating actual devices, a thicker film would have been better. The probe pad requirement resulted in a minimum size of 4 x 4 mils. Reasonable yield requirements lead to a maximum test chip size of 200 x 200 mils.

6. TEST CHIP LAYOUT

The SOS diode test chip layout is shown in Figure 1. The overall chip dimensions are 169.2 x 205.2 mils. The section labeled processing test structure contains CMOS devices used by Rockwell to characterize their process. These devices and the devices in the section labeled "Rockwell Devices" will not be tested in this program. The structure labeled DLTS is a doping-level test structure which will be tested electrically on each chip to monitor variations in the doping level of the epitaxial film. All sapphire wafers are 2 inches in diameter, yielding about seventy usable chips per wafer after edge loss. Three diffusion lots of wafers will be processed during the course of the program. Each processing lot will contain wafers in which the n-type implant level has been varied. Each processing lot delivered for electrical overstress testing will contain five wafers with one each doped to 10^{14}, 10^{15}, 10^{16}, 10^{17} and 5×10^{17} cm^{-3}. The basic SOS diode structure, as shown in the cross section of Figure 2, will have the p++ and n++ contact regions doped to 10^{20} cm^{-3}. The p+ region which forms the p-n junction with the variable doped n region is doped to approximately 5×10^{18} cm^{-3}.

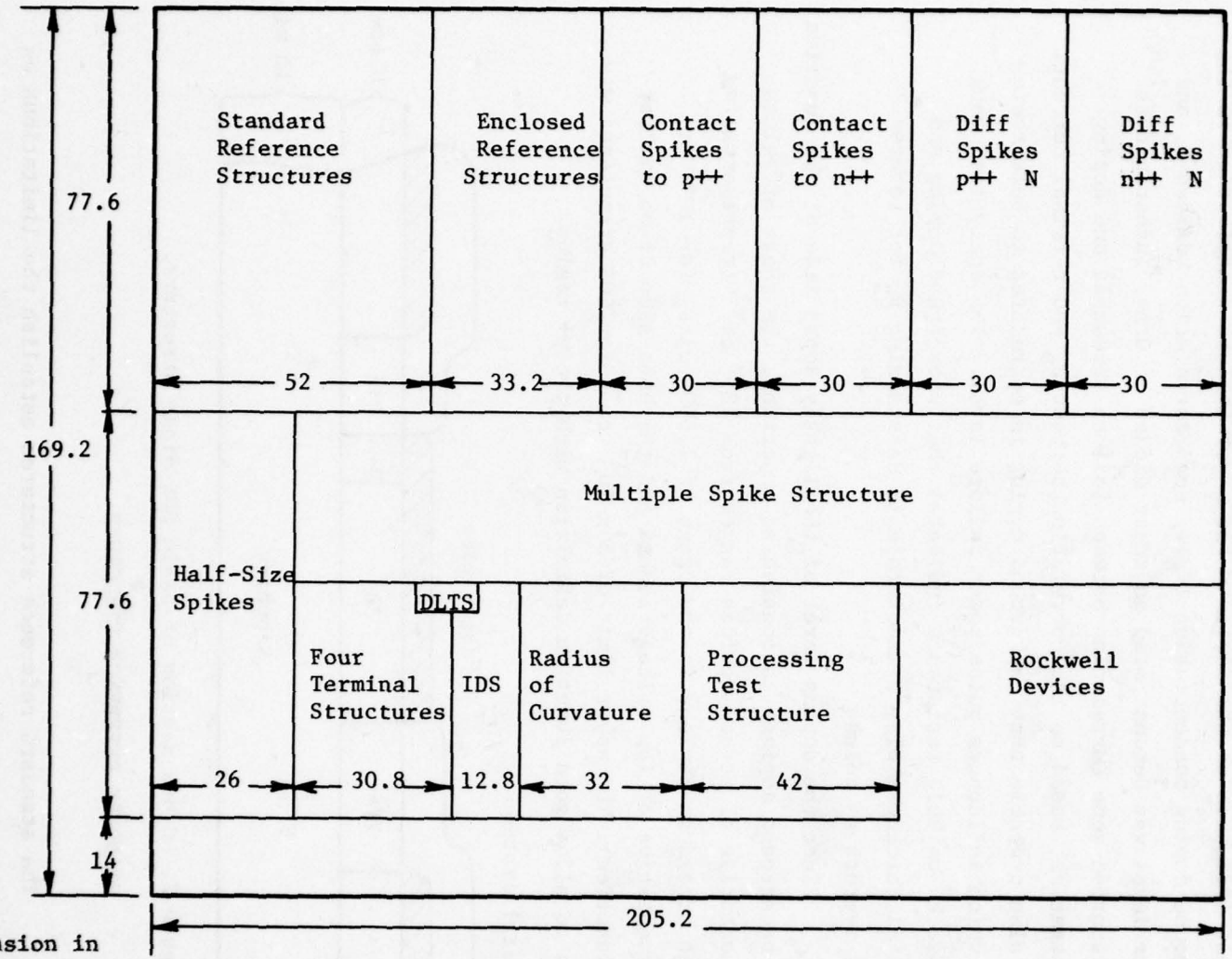


Figure 1. SOS diode test chip layout.

Other than junction area the parameter which probably has the greatest influence on the device pulse power failure distribution is the background doping concentration (N_D). Good correlation between N_D and failure level was demonstrated on zener diodes[3]. Other investigators[7,8] have reported some correlation between failure threshold and doping concentration, based on the correlation between N_D and terminal current. It is also probable that background doping is correlated to bulk resistance which influences pulse power failure level. The analytical work of Neudeck[9] on bulk resistance indicates that background doping and epitaxial thickness play a major role in determining R_B for reverse biased overstress pulses.

Since the doping level of the lightly doped side of the junction (i.e. background doping) is considered important, the range of values representative of actual devices ranges from 10^{14} cm^{-3} (representative of high breakdown devices in the range of 1,000 volts) to $\sim 10^{19}$ cm^{-3} (representative of low voltage zeners and the base side of an emitter base junction). The upper limit of 5×10^{17} cm^{-3} for SOS structures was chosen to allow good junction definition with the p+ region.

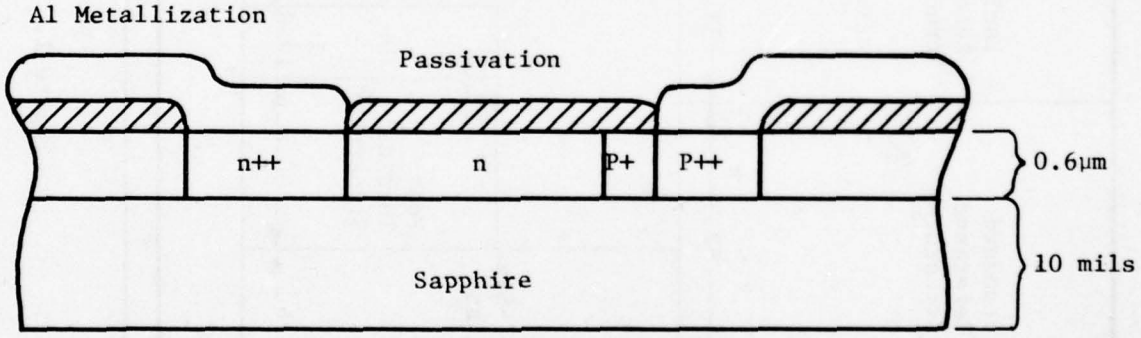


Figure 2. Cross section of basic SOS diode structure.

7. STANDARD REFERENCE STRUCTURE

The standard reference structures establish the limitations on overall diode dimensions which are repeated in the remaining strucutres. In these structures, shown in Figure 3, the width of the junction and length of the n region (representing epitaxial thickness) are varied. There are 25 diodes in this set with junction widths of 1.2, 2, 4, 8, and 20 mils and epitaxial thicknesses or n region lengths of 10, 30,

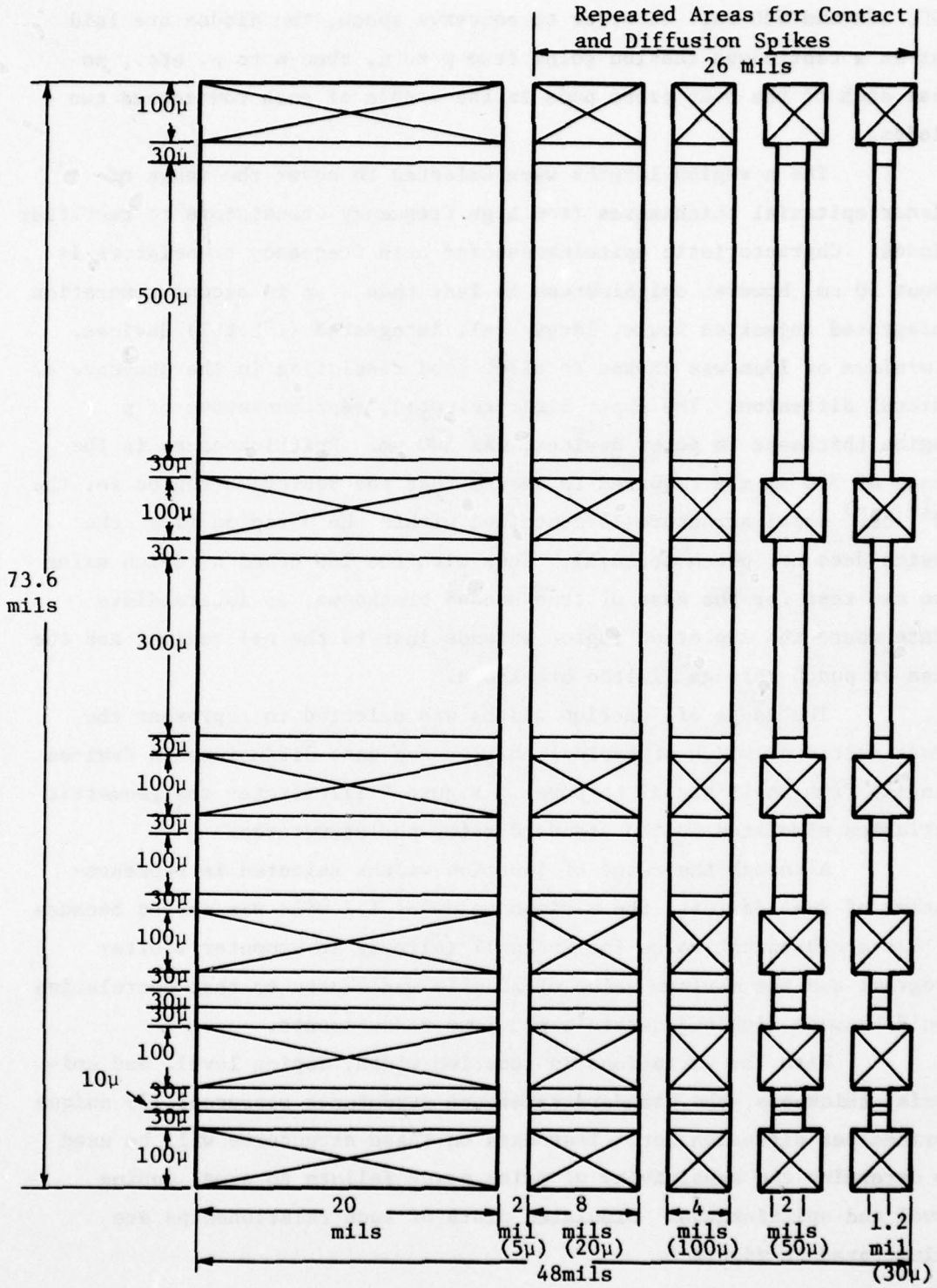


Figure 3. Standard reference structures.

100, 300 and 500 μm. In order to conserve space, the diodes are laid out in a continuous fashion going from p to n, then n to p, etc., so that each of the four probe pads in the middle of each row serves two diodes.

The n region lengths were selected to cover the range of planar epitaxial thicknesses from high frequency transistors to rectifier diodes. Characteristic epithickness for high frequency transistors is about 10 μm, however epithickness is less than 2 μm in second generation integrated injection logic, large scale integrated (I^2L LSI) devices. A minimum of 10μm was chosen to allow good resolution in the presence of lateral diffusion. The upper limit selected, representative of n region thickness in power devices, was 500 μm. Epithicknesses in the range of 500 μm are required to assure that the depletion region for the 10^{14} cm^{-3} doped structure is contained within the n region (i.e. the device does not punch through). Thus with the low doped n region wafer one can test for the case of true second breakdown, an intermediate state where the depletion region extends just to the n++ region, and the case of punch through limited breakdown.

The range of junction widths was selected to represent the cross sectional width of typical emitter and base diffusions in devices ranging from small signal to power. Figure 4 illustrates the geometric variables simulated in the standard reference structures.

Although the range of junction widths selected is representative of real devices, the minimum value of 1.2 mils was chosen because it was a convenient value for Rockwell (already in computer plotter program) and the maximum value of 20 mils was chosen so that correlation could be made with Budenstein's previous measurements.

With the variations in junction width, doping level, and epitaxial thickness, the standard reference structures represent 125 unique devices per diffusion lot. Test data on these structures will be used to determine the sensitivity of pulse power failure to area, doping level and epithickness. Simulated plots of such relationships are illustrated in figure 5.

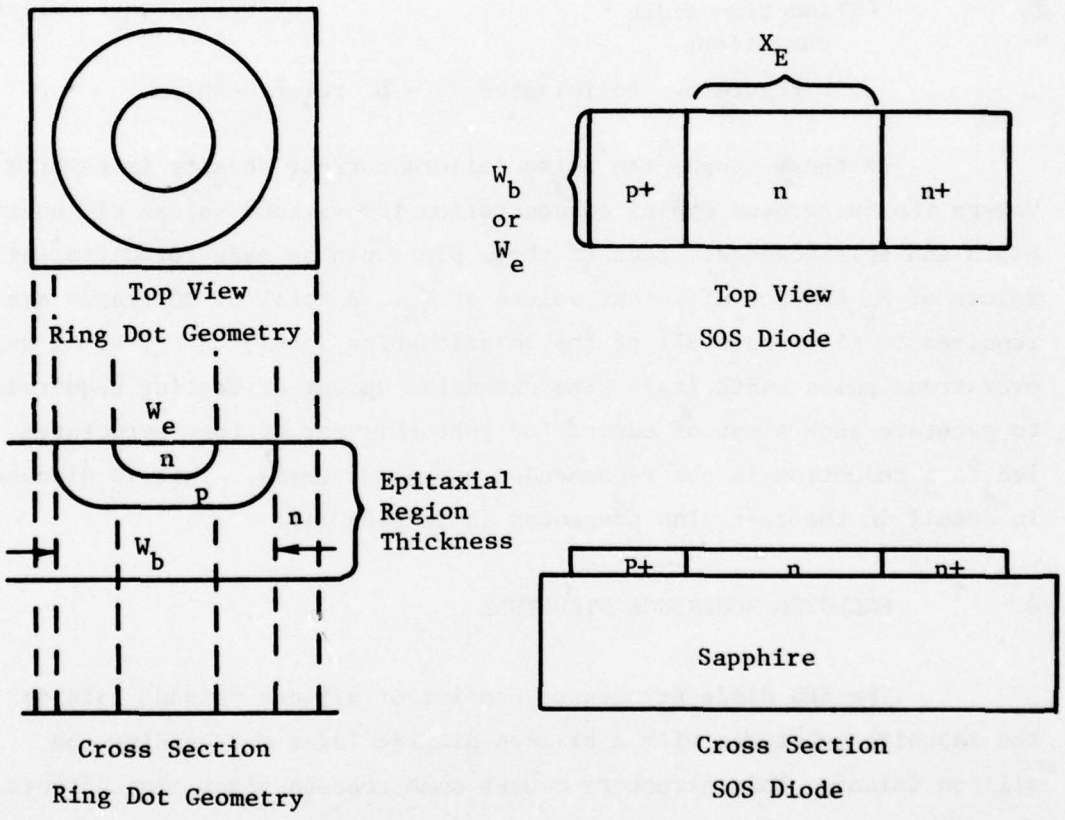
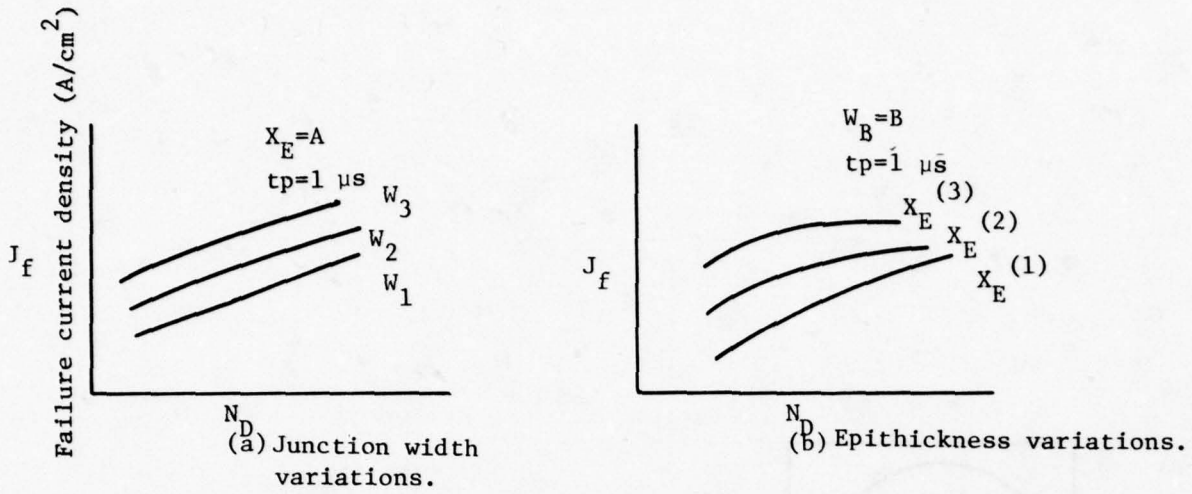


Figure 4. Typical geometry for diodes.



(a) Junction width variations.

(b) Epithickness variations.

Figure 5. Anticipated J_f - N_D relationships.

In these graphs the pulse failure current density is plotted versus the background doping concentration for various values of junction width and epithickness. Each of those plots can be made for different values of X_E and for different values of W_B. A total of 30 graphs are required to illustrate all of the relationships involving N_D, W, X_E and overstress pulse width (tp). The extensive amount of testing required to generate such a set of curves for just this set of test structures led to a reduction in the recommended number of tests. This is discussed in detail in the test plan presented in Section III.

8. ENCLOSED REFERENCE STRUCTURE

The SOS diode structures consist of silicon islands laid on the sapphire substrate with a silicon dioxide layer surrounding the silicon island. This structure causes some concern about edge effects. The fact that the island edge lies in a different crystal plane may result in reduced breakdown voltage at the edge. In order to determine the impact of the edge on either failure mode or failure level, a set of enclosed structures (Figure 6) are included in the program. In the enclosed structure the p-n junction is set in from the silicon island edge so that edge effects are eliminated. The enclosed diode structures duplicate the dimensions of the standard reference structures with the exception of the 20-mil wide device. There are a total of 20 devices

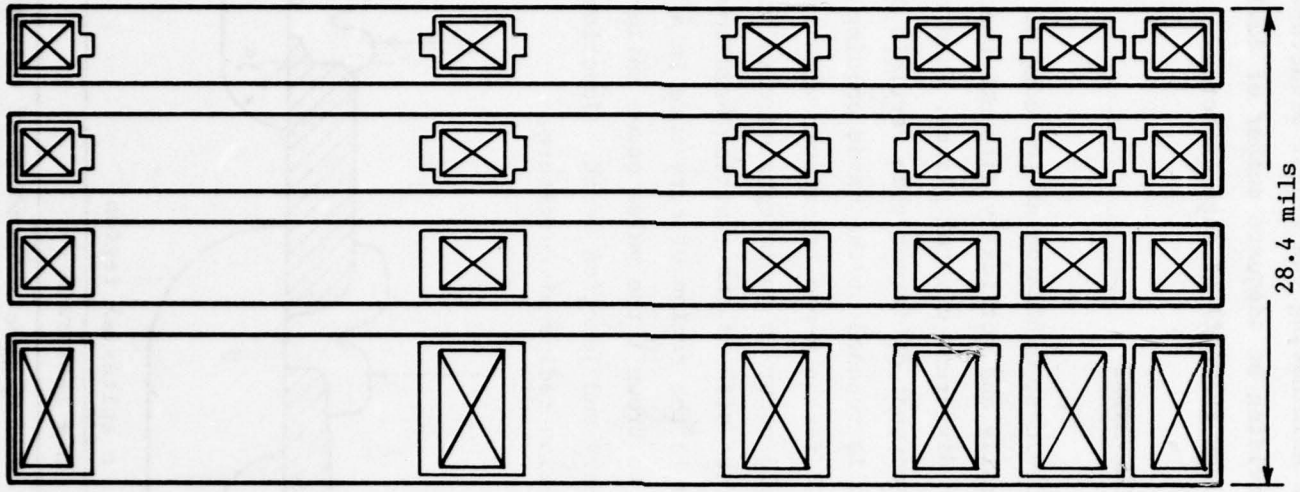


Figure 6. Enclosed reference structures.

having the same X_E dimensions as the standard structures and junction widths of 1.2, 2, 4 and 8 mils.

The basic reason for eliminating the widest structure was to conserve space while still providing an adequate number of devices to establish the importance (or lack thereof) of edge effects.

9. JUNCTION RADIUS OF CURVATURE

In planar diffused devices, diffusion at the edge of the oxide opening takes place both laterally and vertically although the diffusion coefficients are different for different crystal planes. Even though lateral diffusion is usually somewhat different than verticle diffusion the result is a junction which is rounded at the oxide opening edge. This is illustrated in Figure 7 for an n-p-n transistor with a diffused collector contact (such as would occur in an integrated circuit).

The radius of curvature affects the junction breakdown value since breakdown usually occurs in the region of curvature in a planar diffused junction. According to Brown[10] the pulse power failure level is dependent on emitter periphery and junction depth. Junction depth is roughly equivalent to the junction radius of curvature.

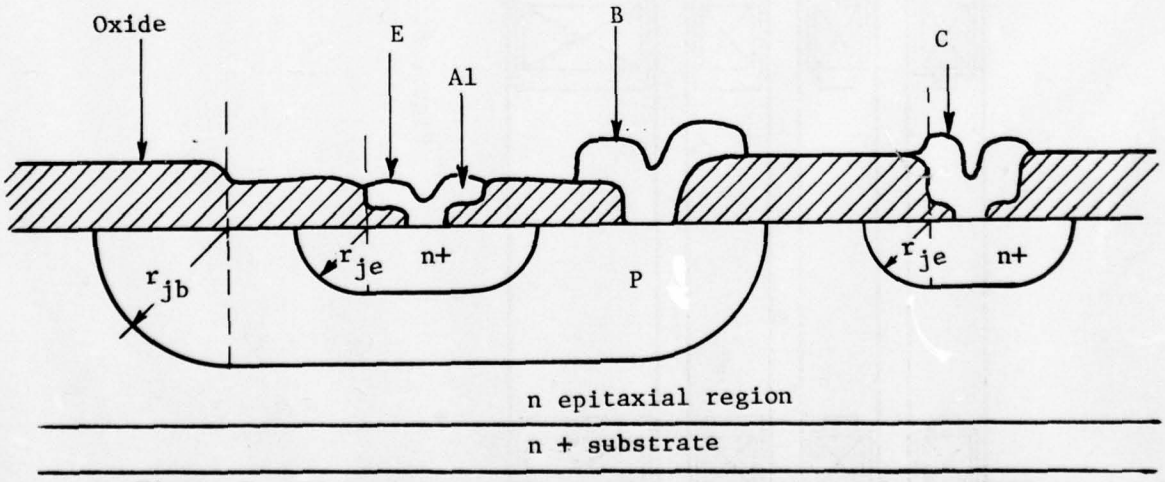


Figure 7. IC Transistor showing junction radius of curvature.

The situation simulated in the SOS diode test structures is illustrated in the right hand portion of Figure 7. For collector to base overstress pulsing, the current flow is from the n+ collector

contact region with radius of curvature r_{je} to the p base region with radius r_{jb}. The SOS diode structures used to simulate this effect are shown in Figure 8. The radius of curvature for the n+ contact diffusion area is 5 μm and the p+ radii are 5, 10, and 30 μm. The separations of radii (distances of closest approach) measure 10, 30 and 100 μm. This structure underwent extensive revision before being finalized since it is one of the more difficult in terms of design. The rather unique shape of the structure resulted from the constraint that the p region metallization contact should be in intimate contact with the simulated junction at the curvature. This is to avoid any voltage drops from the contact through the p+ region to the radius edge. The p++ contact diffusion lies beneath the metallization with a metal overlap of 2 μm.

The selection of the values of r_j were constrained by lateral diffusion. Since these structures represent a horizonal simulation of a vertical effect, there is some lateral diffusion away from the oxide opening, tending to make the simulated curvature less distinct. 5 μm was considered the minimum r_j for which good resolution could be maintained. Actual contact diffusion r_j values in IC transistors are somewhat less than 5μm; however, the functional relationship between P_f and r_j can be established with the range of r_j values used in this study.

The dependence of pulse power failure level on r_j can be determined for variations in doping level and distance of separation.

10. METALLIZATION AND DIFFUSION SPIKE STRUCTURES

There are three sets of metallization and diffusion spike structures; single spike structures including the full range of N_D, W, and X_E variations; half size, single spike structures covering the full range of X_E but with a fixed width; and multiple spike structures with varying spike length.

The first set of spike structures uses the same pattern as the standard reference structures shown in Figure 3. All but the 20-mil wide structures are used as indicated in the figure. The nature of the metallization and diffusion spikes are illustrated in the transistor cross section of Figure 9.

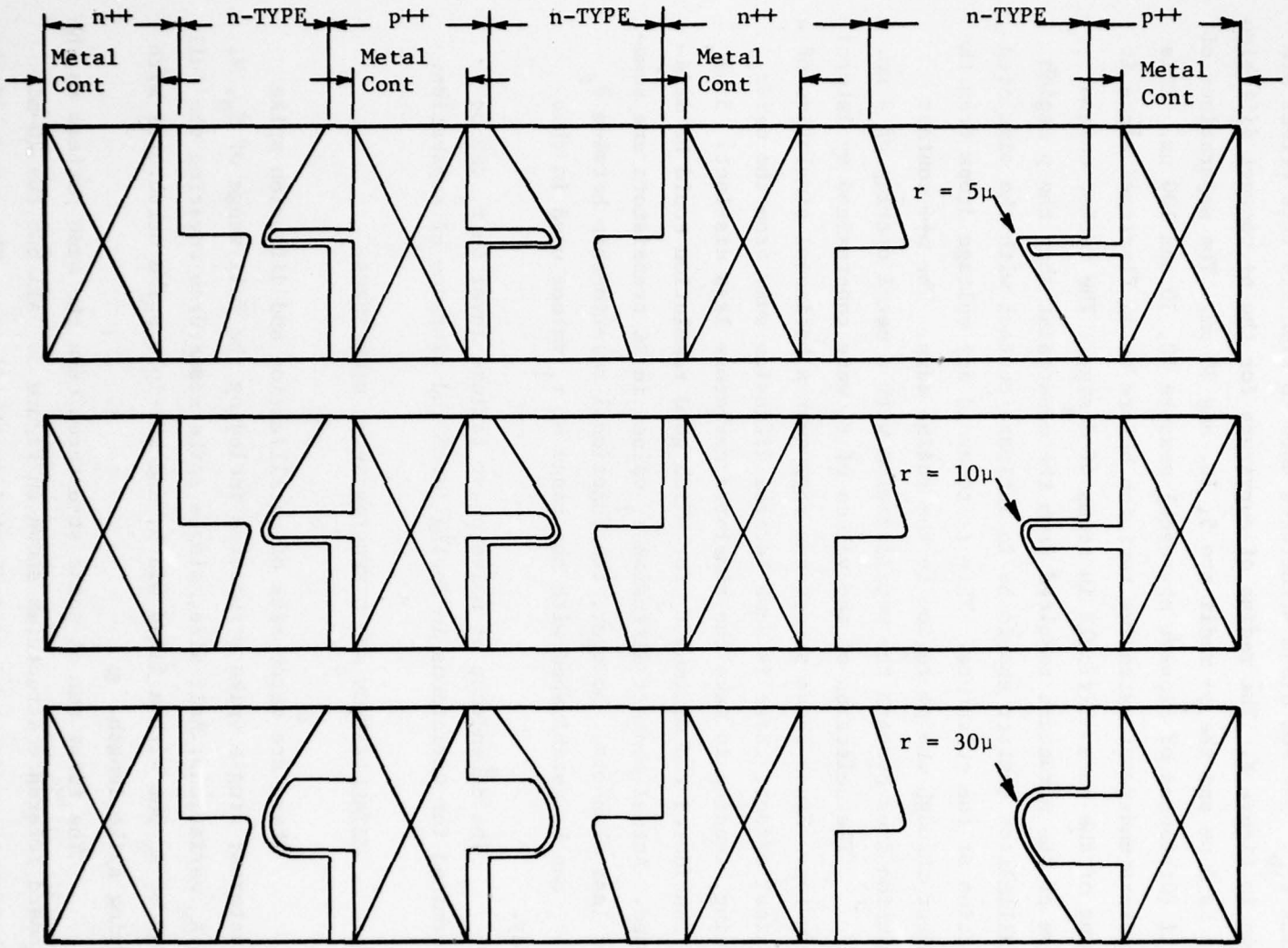


Figure 8. Radius of curvature structure in SOS diodes.

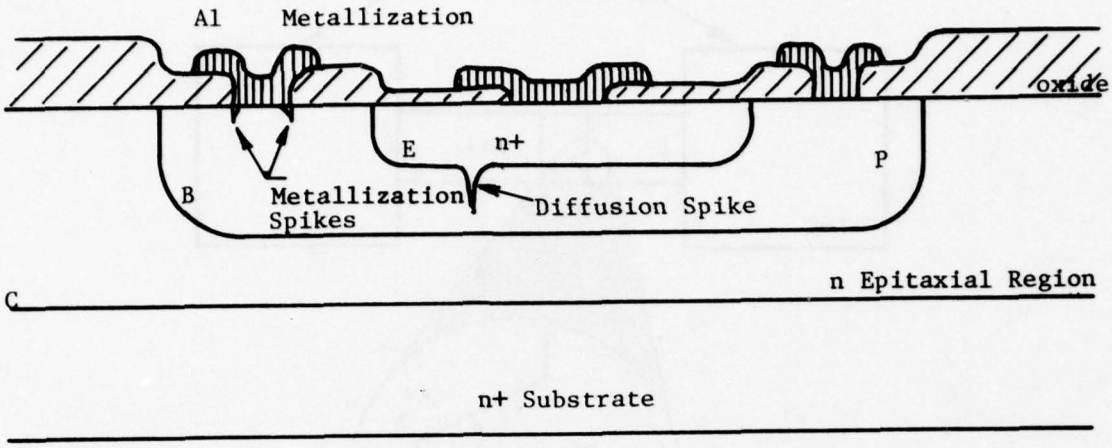


Figure 9. Cross-sectional representation of metallization and diffusion spikes.

Metallization spikes can occur at oxide edges during the high temperature sintering process[11]. Diffusion spikes are thought to occur along crystal dislocation lines and can result in C-E transistor shorts if they extend across the base region. Much of the yield loss in high density LSI devices may well result from such catastrophic defect diffusion spikes.

The type of diffusion spike of concern in this program is one which may extend only partially into the region of opposite polarity. Both diffusion and metallization spikes may alter the field and current distributions and affect hot spot locations. The major objective of spike test structures is to determine their influence on the pulse power failure level. The factors which went into the design of the test structure were the shape, amplitude and location of the spike. The first set of contact/diffusion spike structures uses a single spike of fixed amplitude as shown in Figure 10 for a diffusion spike on the 1.2-mil wide diode with 10-μm epitaxial thickness.

The spikes, which are programmed into the diffusion and metallization masks, are triangularly shaped with a 60-degree angle at the apex. Each spike is 5 μm high and located 1/4 the distance from the left hand (lower) edge of the junction. The triangular shape is a rather obvious selection based on what is known empirically about the

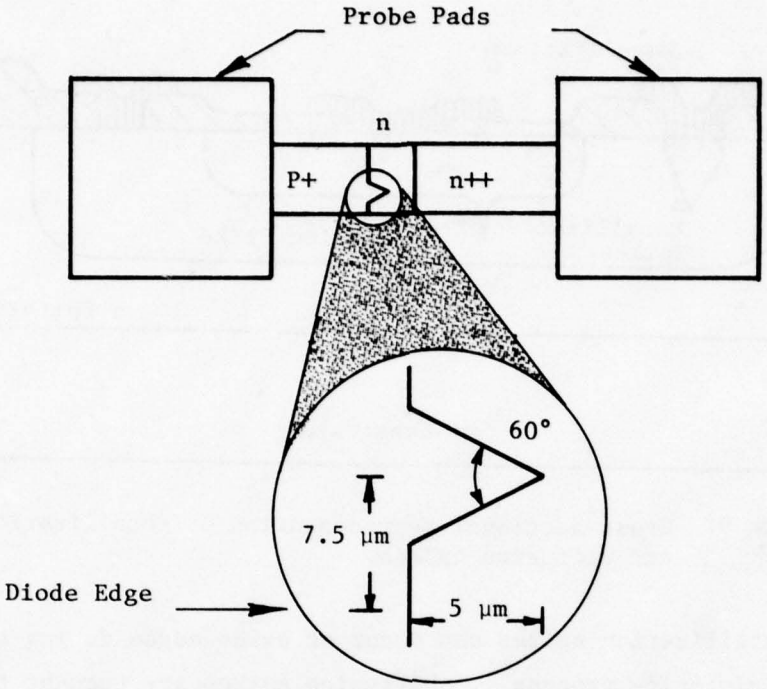


Figure 10. Details of diffusion spike from p+ to n++.

nature of the spikes. The exact shape of the triangle was selected mostly to facilitate the ease with which the structure could be simulated in the analytical programs. The amplitude was selected to guarantee a significant effect on the minimum geometry structure and to appear as a subtle defect in the maximum geometry diode. At 5 µm the diffusion spike will extend halfway across the epitaxial region in the 10-µm diode. There was no obvious spike amplitude based on data from real devices because of the wide variation in actual device geometries. A 0.2-µm diffusion spike in the base region of a high frequency transistor would probably be catastrophic whereas a 5-µm spike in the p diffusion of a high voltage diode would have essentially no effect on performance. The choice of amplitude was therefore selected to facilitate analysis of the effect of the spikes. The location of the spike was selected so that it would not coincide with a natural location of a hot spot. The photographs of hot spot locations generated by Budenstein[1] on previous programs were studied to determine normal spacing based on the thermal and electronic properties of silicon. It was determined from this study

that hot spots never occur (in the absence of major defects) at a distance of 1/4 the diode width from the edge. Therefore, a hot spot occurring at the spike location will be due to the influence of the spike.

The diffusion spikes are built into the diffusion masks both in the p++ to n direction and the n++ to n direction. The contact spikes are built into the metalization mask in both the p++ to n and n++ to n directions. With the 20 variations of diode dimensions and four different spike definitions there are a total of 80 test diodes in this set.

10.1 Half Size Spikes

The half size spike structures consist of 20 diodes, each 4 mils wide with varying epilengths (10, 30, 100, 300 and 500 μm). As with the standard spikes, the half size spikes are single triangular spikes located 1/4 the distance from the junction edge. They include a metallization mask spike from the n++ contact toward the n region and the p++ contact toward the n region and a diffusion mask spike from the n++ region to the n region and from the p+ region to the n region. The amplitude of the spikes is 2.5 μm.

The half size spikes are used to determine the dependence of spike amplitude on the manner in which the spike influences the pulse power failure threshold and/or hot spot size and location. The influence of the spike may be a strong function of the epilength, therefore all five epilengths were included in the set.

10.2 Multiple Spike Structure

A layout of the multiple spike structure set is given in Figure 11 and details of the multiple spikes are given in Figure 12. The spikes are all designed into a mask which has a continuous junction or contact edge background of 1-μm spikes. Spikes of 2, 4, and 8 μm are placed in this background at distances of 2, 4, and 6.8 mils from the edge of an 8-mil wide junction. The spike structures are built into

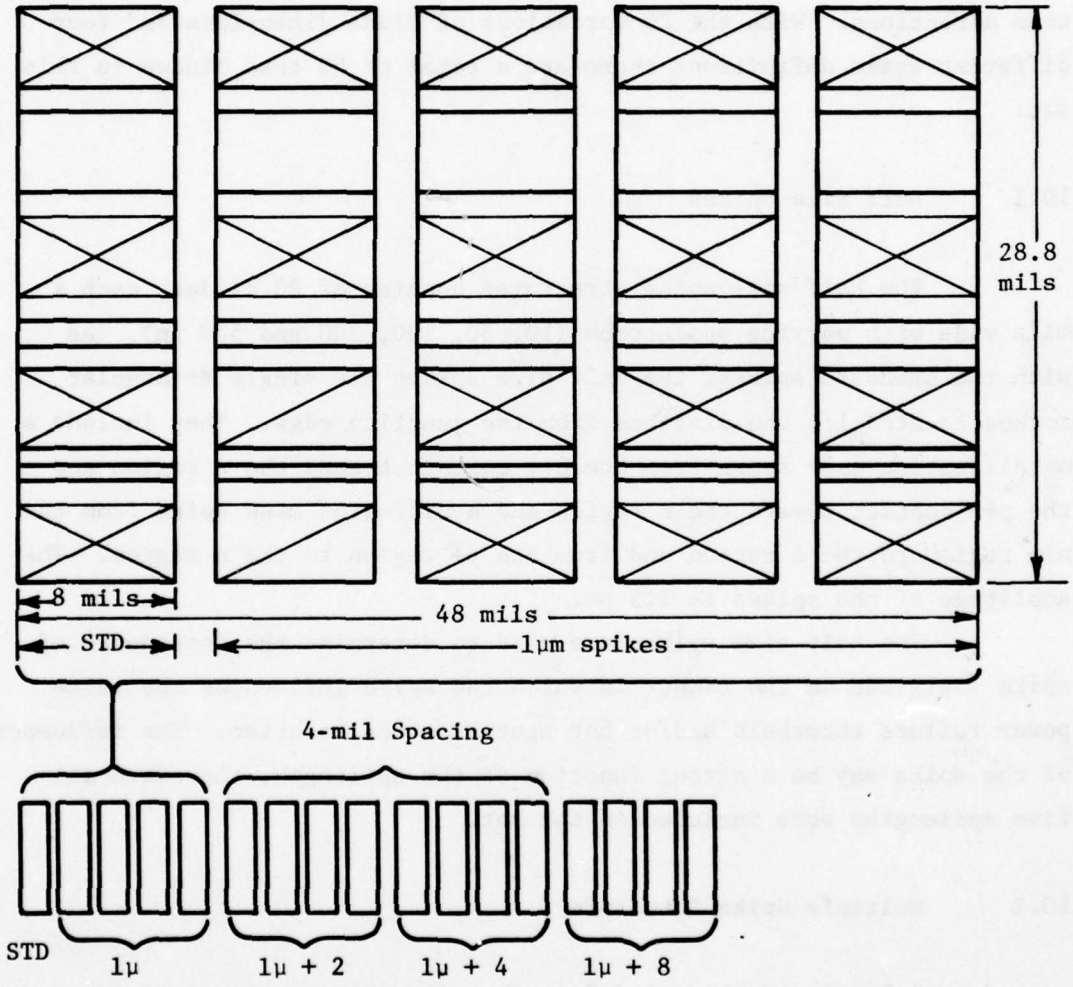
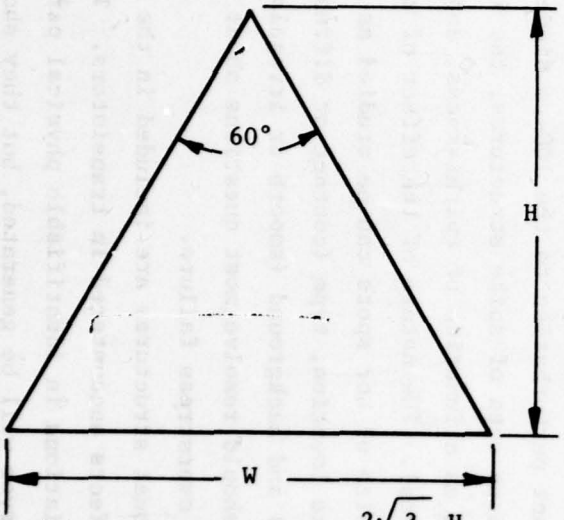
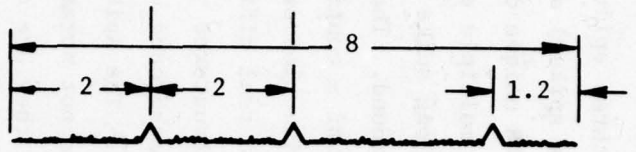


Figure 11. Multiple spike structures.



(a) Spike shape, $W = \frac{2\sqrt{3}}{3} H$



(b) Multiple spike locations on junction.
(Dimensions in mils)

(c) Multiple spike construction detail.
H = 2, 4 or 8

Figure 12. Details of multiple spike structure.

10-, 30-, and 100-μm epilength diodes and include all four combinations of spike type (contact and diffusion) and spike direction (n++ to n and p+ to n). A set of three standard 8-mil wide diodes without spikes is included in the set as a baseline. With the three epilengths, four spike amplitudes (including only the background 1-μm spikes) and four type and direction combinations, there are a total of 48 unique diodes plus the three reference diodes. The objective of the multiple spike structures is to study the influence of having more than one spike arranged in a nonuniform pattern against an irregular background. The influence of spike amplitude is also included. The choice of a continuous 1-μm spike background was to simulate a realistic junction or contact region having a continuum of irregularities. Since a real diffused junction or contact interface has irregularities, these structures will allow one to determine if a larger spike on an irregular background would have the same effect as a spike on a smooth background. The spike locations were selected to appear at sites where hot spots do not normally occur (1/4 distance from the junction), a location where they are often found (1/2 distance) and a semirandom position to avoid a consistant geometric pattern (1.2 mil from the edge). The amplitudes were chosen to provide a geometric progression in height from the background of 1 μm (i.e. twice background, 4 times and 8 times). The 8-μm spike will cause a major perturbation to the 10-μm long diode whereas the 2-μm spike represents an almost insignificant perturbation to the 100-μm diode.

With the three sets of spike structures, the influence of spikes can be studied as a function of epithickness, doping level, and junction width (or area). The nature of the effect of spiking on the location, shape and size of hot spots can be studied as a function of spike amplitude, spike location, type (contact or diffusion), direction (n++ to n or p+ to n) and background (smooth or irregular). Test data on these structures should resolve most questions about the influence of spikes on electrical overstress failure.

Two additional structures are included in the program to simulate specific effects encountered in transistors. These structures do not represent variations in identifiable physical parameters for which sensitivity curves will be generated, but they should provide insight into the failure mechanisms in real transistors.

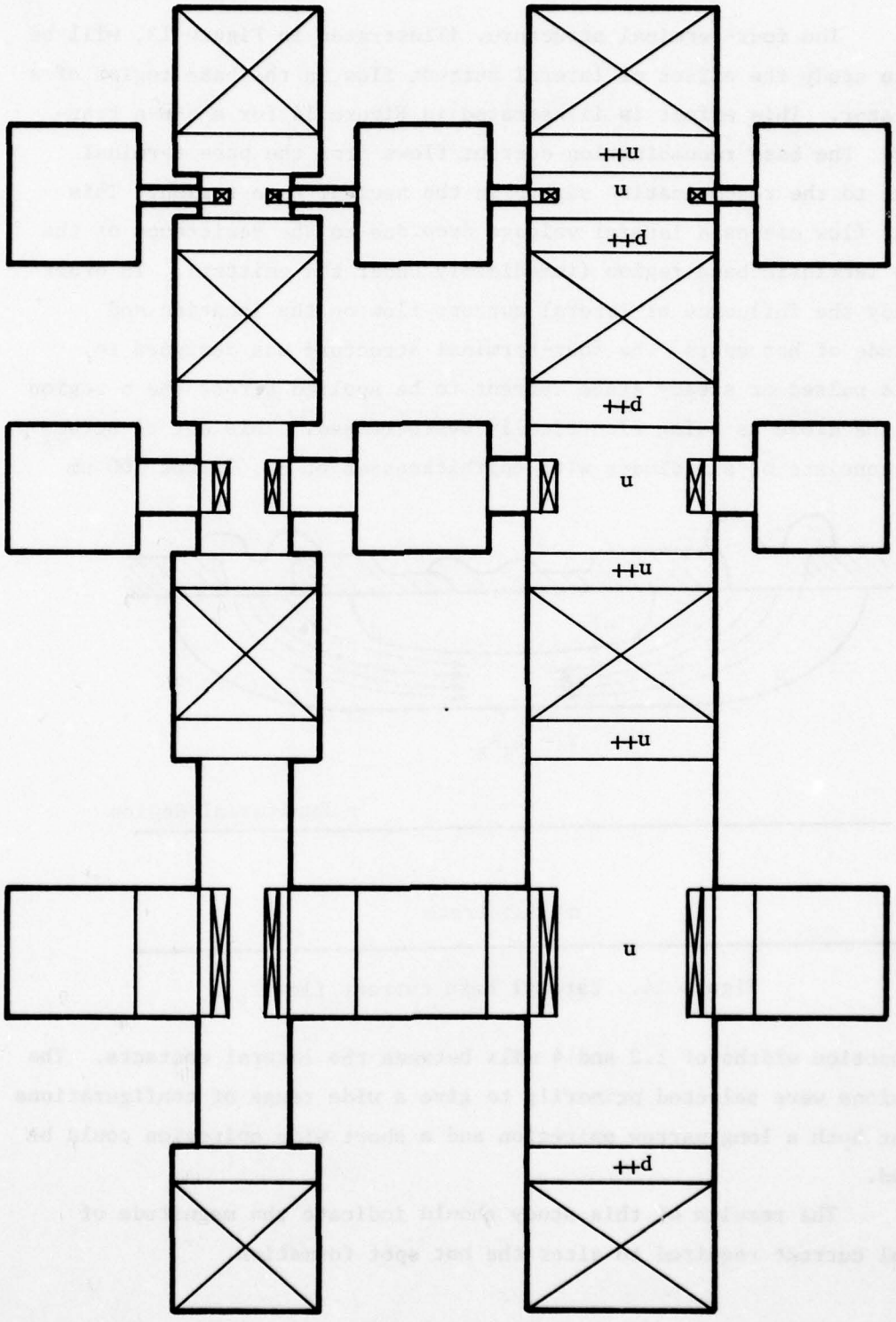
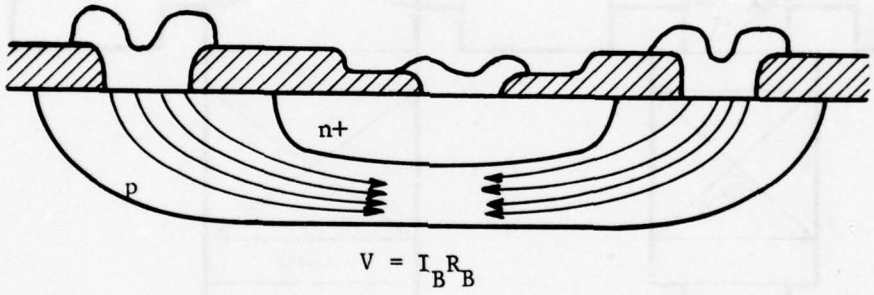


Figure 13. Four-terminal structure.

11. FOUR-TERMINAL STRUCTURE

The four-terminal structure, illustrated in Figure 13, will be used to study the effect of lateral current flow in the base region of a transistor. This effect is illustrated in Figure 14 for a n-p-n transistor. The base recombination current flows from the base terminal contact to the recombination sights in the neutral base region. This current flow causes a lateral voltage drop due to the resistance of the narrow intrinsic base region (immediately under the emitter). In order to study the influence of lateral current flow on the location and magnitude of hot spots, the four-terminal structure was designed to allow a pulsed or steady state current to be applied across the n region while the diode is being electrically overstressed. This set of structures consists of six diodes with epithicknesses of 30, 90 and 300 μm



$V = I_B R_B$

n Expitaxial Region

n+ Substrate

Figure 14. Lateral base current flow.

and junction widths of 1.2 and 4 mils between the lateral contacts. The dimensions were selected primarily to give a wide range of configurations so that both a long narrow epiregion and a short wide epiregion could be studied.

The results of this study should indicate the magnitude of lateral current required to alter the hot spot formation.

12. INTERDIGITATED STRUCTURE

The interdigtated structure is designed to simulate the interdigitated emitter-base configuration used in many high frequency and power transistors. The surface topology and cross section of such a transistor is shown in Figure 15.

This structure is simulated with the SOS diode structure shown in Figure 16. This structure consists of two diodes each with three base contacts (n++) and two emitter diffusions and contacts (p+). One device has 20-μm separations between contacts and in the other the separation is 40 μm. The n++ contact diffusions into the n region are 30 μm wide by 5 μm deep. The p+ diffusions are 60 μm wide by 10 μm deep with a 20-μm separation between diodes. In these structures the nature of the hot spot nucleation can be studied for lateral electrical overstress current flow as would occur in a real emitter-base junction. Additionally, the effect of having the current distribution spread out between multiple contacts as would occur in the interdigitated structure can be studied.

Both the four-terminal and interdigitated structures will also be used to test the applicability of the analytical code predictions with respect to the nature of the second breakdown phenomona in two dimensional structures.

13. EXPECTED RESULTS

In several instances the SOS lateral diode structures described above are approaching the technology limitations and some reduction in yield is expected. The diodes with n type doping concentrations of 10^{14} cm^{-3} were selected to give breakdown voltages of several hundred volts. Whether this is actually achievable with SOS technology is problematical. The spike heights of 2.5 μm and less will be somewhat rounded by the photolithographic and diffusion processes. However, a few devices with the designed characteristics are likely. These should be identified in pretest characterization and singled out for special handling during destructive testing. In general, the design approach was to include both device designs which could be achieved with almost 100 percent certainty and device designs which would have much lower yields but would be important due to their relevance to practical bipolar device geometries.

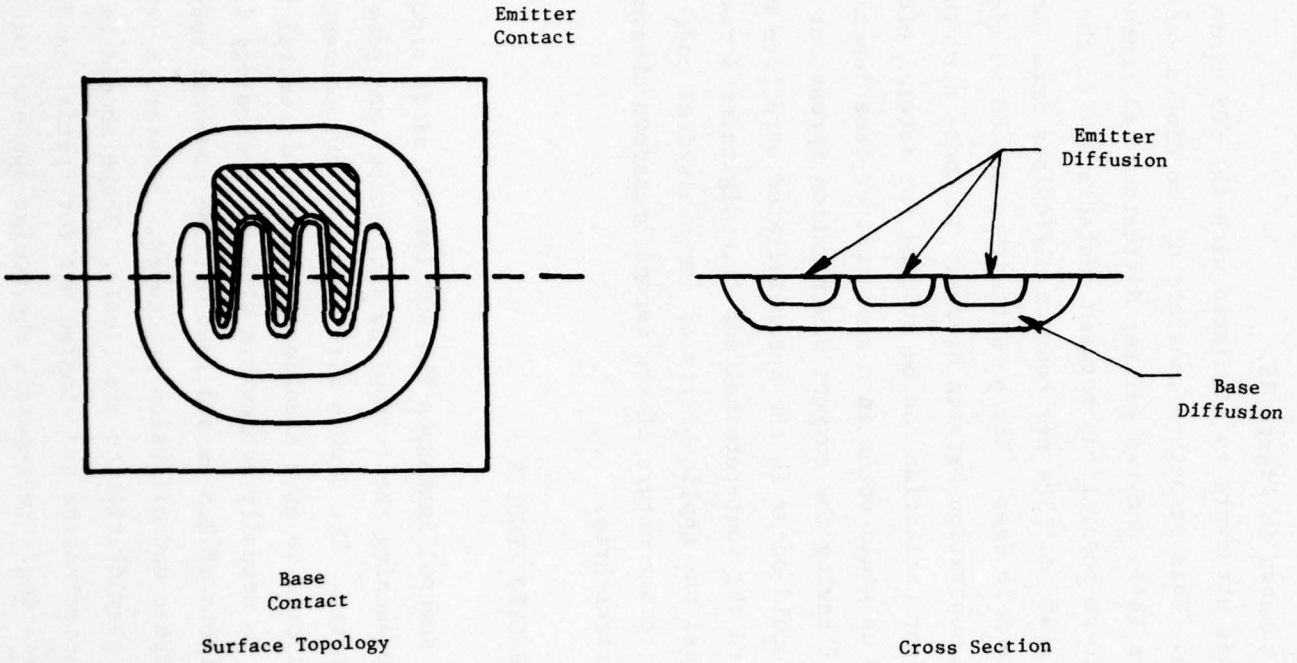


Figure 15. Interdigitated transistor.

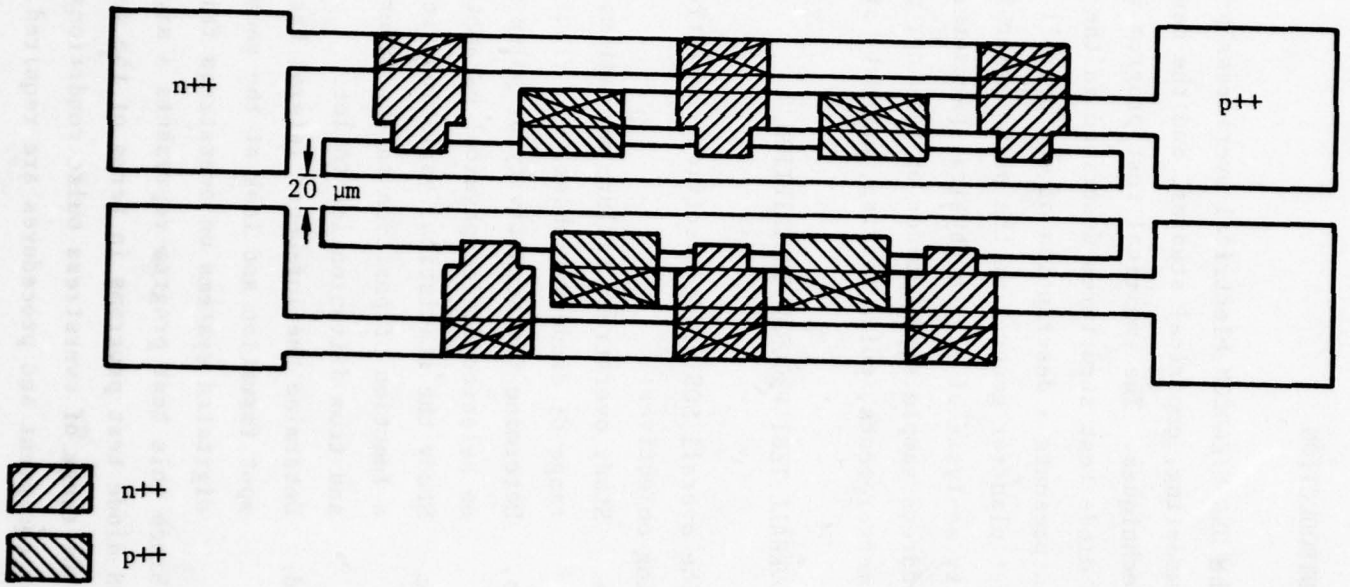


Figure 16. SOS structure of an interdigitated device.

SECTION III
TEST PLAN FOR ELECTRICAL OVERSTRESS TESTING ON SOS DIODE TEST STRUCTURES

14. INTRODUCTION

The DNA/MIRADCOM electrical overstress program consists of analytical modeling, empirical studies, and the development of hardness assurance techniques. The empirical test program is being conducted on special SOS diode test structures described in the previous section. This section presents a description of the overall test program and a detailed test plan for generating the pulse power failure data to perform a sensitivity analysis of device physical parameters. The detailed test plan will address sample sizes, order of testing, pre- and posttest electrical measurements, pulse testing, and data storage handling.

15. OVERALL TEST PROGRAM DESCRIPTION

The overall SOS diode electrical overstress test program has the following objectives:

a. Study overstress failure mechanisms in detail over a wide range of diode variables.

b. Determine the sensitivity of pulse power failure threshold on selected device physical parameters.

c. Study the statistical variations in pulse power failure as a function of position on the wafer, from wafer to wafer, and from diffusion lot to lot.

d. Determine the influence lateral base current has on hot spot formation and look at the geometric effects of interdigitated systems on overstress failure mechanisms.

Since this test program represents a significant extension of earlier SOS diode test programs in terms of the variety of test structures and the range of overstress pulse conditions, extensive revisions of the test equipment and procedures are required. In the early stages of the program a significant amount of testing will be required in order to develop and perfect the test procedures necessary to perform the

quantity testing for the sensitivity analysis. Once the test equipment, techniques and procedures have been well established, the sensitivity analysis testing will begin. The following sections describe in detail how the sensitivity testing will be performed. After this task is completed the remaining test structures can be utilized for statistical variation tests.

16. TEST STRUCTURES

Special test structures as discussed in the previous section are being fabricated by Rockwell for use in this study. These structures consist of lateral diodes fabricated on sapphire substrates. The diodes have been designed to permit observation of the sensitivity of various semiconductor physical parameters to electrical overstress. The total test sample consists of approximately 75,000 separate diodes per diffusion lot. These diodes are fabricated in three lots of five wafers each (five different doping concentrations). Each wafer contains approximately 70 identical dice. Each die is divided into 12 sections which contain diodes of similar structure but varying physical dimensions. Table 1 gives a breakdown of the SOS diode structures. Table 2 gives a breakdown of the physical dimensions of each of the structure types found in every die.

To assure that the highest quality data are obtained in a timely manner, a consistent test methodology is required. The methodology presented in this section has evolved over a period of several years and has been proven on many large scale component test programs. The remainder of this section covers in detail the selection of the quantities of diodes to be tested, the priority of testing, test conduct, and data storage and handling.

17. TEST DIODE SELECTION

Approximately 75,000 separate diodes per diffusion lot are available for testing. Because of time constraints, it will be impossible

Table 1. SOS Diode Structures.

Structure Type	Devices[a] Per Die	Dice Per Wafer	Wafers[b] Per Lot	Devices Per Wafer	Devices Per Lot
Standard Reference	25	70	5	1750	8750
Enclosed Reference	20	70	5	1400	7000
Contact Spikes to p++	20	70	5	1400	7000
Contact Spikes to n++	20	70	5	1400	7000
Diff Spikes p++ to n	20	70	5	1400	7000
Diff Spikes n++ to n	20	70	5	1400	7000
Multiple Spikes	51	70	5	3570	17,850
Half Size Spikes	20	70	5	1400	7000
Four Terminal	6	70	5	420	2100
Doping Level	1	70	5	70	350
Interdigitated	2	70	5	140	700
Radius of Curvature	9	70	5	630	3150
Totals	214	70	5	14,980	74,900

[a]Each diode has different physical dimensions.

[b]Each wafer has a different doping level (10^{14}, 10^{15}, 10^{16}, 10^{17}, $5x10^{17}$, cm^{-3}).

Table 2. SOS diode structures physical dimensions.

Standard Reference Structures	n region length = 10, 30, 100, 300, 500 u Structure width = 1.2, 2, 4, 8, 20 mils
Contact/Diffusion Spike Structures	n region length = 10, 30, 100, 300, 500 u Structure width = 1.2, 2, 4, 8 mils Spike length = 5 u Spike direction = n++ contact → n-type; P++ contact → n-type n++ diffusion → n-type; P++ diffusion → n-type
Enclosed Reference Structures	n region length = 10, 30, 100, 300, 500 u Structure width = 1.2, 2, 4, 8 mils
Half Size Structures	n region length = 10, 30, 100, 300, 500 u Structure width = 4 mils Spike length - 2.5 u Spike direction - n++ contact → n-type, p++ contact → n-type n++ diffusion → n-type, p++ diffusion → n-type
Multiple Spike Structures	n region length = 10, 30, 100 u Structure width = 8 mils Spike Length = 1, 2, 4, 8 u Spike direction = n++ contact → n-type, p++ contact → n-type n++ diffusion → n-type, p++ diffusion → n-type
Four Terminal Structures	n region length = 30, 90, 300 u Structure width = 1.2, 4 mils Spacing between control and contact regions = equal

Table 2. SOS diode structures physical dimensions (concluded).

Doping Level Test Structures	Length between contacts = 100 u Structure width = 200 u
Interdigitated Structures	n++ diffusion length x width = 5 u x 30 u p++ diffusion length x width = 10 u x 60 u n++ - p++ diffusion separation = 20, 40 u
Radius of Curvative Structures	Radius of p++ diffusion = 5, 10, 30 u Radius of n++ diffusion = 5 u Minimum separation = 10, 30, 100 u

to test all of these devices. It is necessary therefore to restrict the number of test structures examined to allow testing of a broad sample of different structures so that the maximum information can be obtained from the tests in the alloted time.

The quantity of devices selected for testing is based on a test rate of two diodes at three pulse widths per hour. This rate was selected for planning purposes after discussions with Dr. Paul Budenstein of Auburn University. Additional time has been allotted for changes in the test setup required during testing when a diode burns out. Since much of the testing is to be performed in new areas (i.e., short pulse widths and high breakdown voltages), time will also be required to improve the test techniques in this area.

Table 3 presents a breakdown of the quantity of the various diode structures to be tested in this program and the approximate time required to perform these tests. The number of diodes per wafer is based on being able to test each diode at three pulse widths (0.1, 1.0, 10 msec). Should a diode burn out during a test, additional dice will have to be tested. The sample size for each diode of given physical dimensions is five. The total number of diodes shown is for each lot of five wafers (five doping levels).

The Doping Level Test Structure will be tested on each die used in the test program. Since only a V-I measurement is made on this structure, little time will be required for this test. As a check on consistency, the Doping Level Test Structure will be tested each time a given section of a die is tested.

18. ORDER OF TESTING

The order of testing the various diode structures has been chosen to provide sufficient data early in the program to proceed with the sensitivity analysis task. Although other test sequences may allow more diodes to be tested, they would delay the sensitivity analyses and correlation study until very late in the program and could leave insufficient time available for the completion of those tasks.

Table 3. SOS diode structures to be tested for sensitivity analysis.

Standard and Dimensional Variations	Diodes Per Die	Diodes Per Wafer[a]	Total Diodes[b]	Test Time
Standard Reference Structure n-region lengths = 10, 30, 100, 500 μ Structure widths = 1.2, 4, 8, 20 mils	16	80	400	5 weeks
Enclosed Reference Structures n-region lengths = 10, 30, 100, 500 μ Structure widths = 1.2, 4, 8 mils	12	60	300	4 weeks
Radius of Curvature Structures Radii of p++ diffusions = 5, 10, 30 μ Radius of separations = 10, 30, 100 μ	9	45	225	3 weeks
Contract/Diffusion Spike Structures n-region lengths = 10, 30, 100 μ Structure widths = 1.2, 4, 8 mils				
Spike directions = n++ contact → n-type	9	45	225	3 weeks
p++ contact → n-type	9	45	225	3 weeks
n++ diffusion → n-type	9	45	225	3 weeks
p++ diffusion → n-type	9	45	225	3 weeks
Multiple Spike Structures n-region lengths = 10, 30, 100 μ Spike lengths = 1, 8 μ				
Spike directions = n++ contact → n-type	6	30	150	2 weeks
p++ contact → n-type	6	30	150	2 weeks
n++ diffusion → n-type	6	30	150	2 weeks
p++ diffusion → n-type	6	30	150	2 weeks

Table 3. SOS diode structures to be tested for sensitivity analysis (concluded).

Total Test Structure and Dimensional Variations	Diodes Per Die	Diodes Per Wafer[a]	Diodes[b]	Time
Half Size Spike Structures				
n-region lengths = 10, 30, 100 μ				
Spike directions = n++ contact to n-type	3	15	75	1 week
p++ contact to n-type	3	15	75	1 week
n++ diffusion to n-type	3	15	75	1 week
p++ diffusion to n-type	3	15	75	1 week
Doping Level Test structure (One per die)	1	c	c	1 week
Totals	109	545[a]	2725[b]	37 weeks

[a]Assuming each diode is tested at three pulse widths (5 dice per wafer) any diode failures will require that additional dice be tested.

[b]Each lot contains 5 wafers.

[c]The number of diodes depends on the number of dice tested.

The priority of testing the various diode structure types is given in Table 4. The Standard and Enclosed Reference Structures will be tested first to establish a baseline for the remaining tests and to assess the sensitivity of Pf to ND, epithickness and diode width. The priorities for testing the remainder of the structure types have been chosen so that those structures representing physical variables that have the higher probability of providing a good correlation with actual device overstress data are tested first.

The tests will be performed so that all data on a given structure type will be taken before proceeding to the next structure type. This order of testing will require that each wafer be inserted and removed from the test fixture several times during the course of the program. Extreme care will be required in handling to insure that none of the wafers is damaged.

19. OVERSTRESS TESTING

19.1 *Pretest Characterization*

The pretest characterization will consist of forward and reverse V-I charactertistics taken on each diode to be pulse treated. A Tektronix Model 576 curve tracer will be used to characterize the structures and the results will be photographically recorded. Each photograph will be marked with the device identification number to allow correlation of diode prepulse characteristics with its overstress behavior.

Since Rockwell will pretest only a small sample of diodes (five diodes per wafer), it is essential that the pretest characteristics be performed in order to assure that the test diodes are functional and that their characteristics are as assumed. The analysis of the results of these tests could be significantly altered if diodes of different or unusual characteristics are inadvertently included in the test sample.

19.2 Pulse Testing

The basic procedure is to step stress each diode. Wherever possible, a constant current pulse source will be used to bring about the onset of filamentation. The filamentation process will be photographically recorded using the procedures developed by Dr. Paul Budenstein[1].

Table 4. Priority of testing.[a]

Priority	Structure Type
1	Standard reference
2	Enclosed reference
3	Radius of curvature
4	Contact/diffusion spike
5	Half size spike
6	Multiple spike
7	Interdigitated
8	Four terminal

[a]A doping level test structure will be tested each time a die is tested.

In addition to the photomicrographs, the pulse voltage and current response of each diode will be recorded using a Tektronix WP2221 Waveform Digitizing system with two R7912 Transient Digitizers and a CP112 Floppy Disc. An identification number will be assigned to each diode and recorded along with the digitized data for each pulse. A block diagram of the test setup is shown in Figure 17.

Within each test structure type and doping concentration, five diodes having the same physical dimensions (see table 4) will be tested at each of three pulse widths (0.1, 1.0, and 10 usec). Testing at all three pulse widths will be performed on each diode provided no damage occurs during pulse testing. In the event of damage, a diode having the same physical dimensions but from a different die will be substituted for the damaged device. Degradation or failure is most likely to occur on the lightly doped wafers (high breakdown voltage), particularly if the pulsed current source is not adequately regulated.

19.3 Posttest Characterization

Posttest characterization will consist of running the curve tracer I-V characteristics of each diode following testing at each pulse width. No waveforms will be recorded unless damage, such as increased leakage current or decreased breakdown voltage, has occurred. Since each diode is to be tested at more than one pulse width and a high probability of failure exists for many of the diodes, the posttest characterization is essential to insure that only good devices are used in every test.

20. DATE HANDLING AND STORAGE

All pulse data will be recorded on a Tektronix CP112 Floppy Disc. The recorded data will consist of a device identification number, the digitized pulse current, and the digitized pulse voltage. The identification number will consist of eight digits and have the following format:

A B C C D D E E

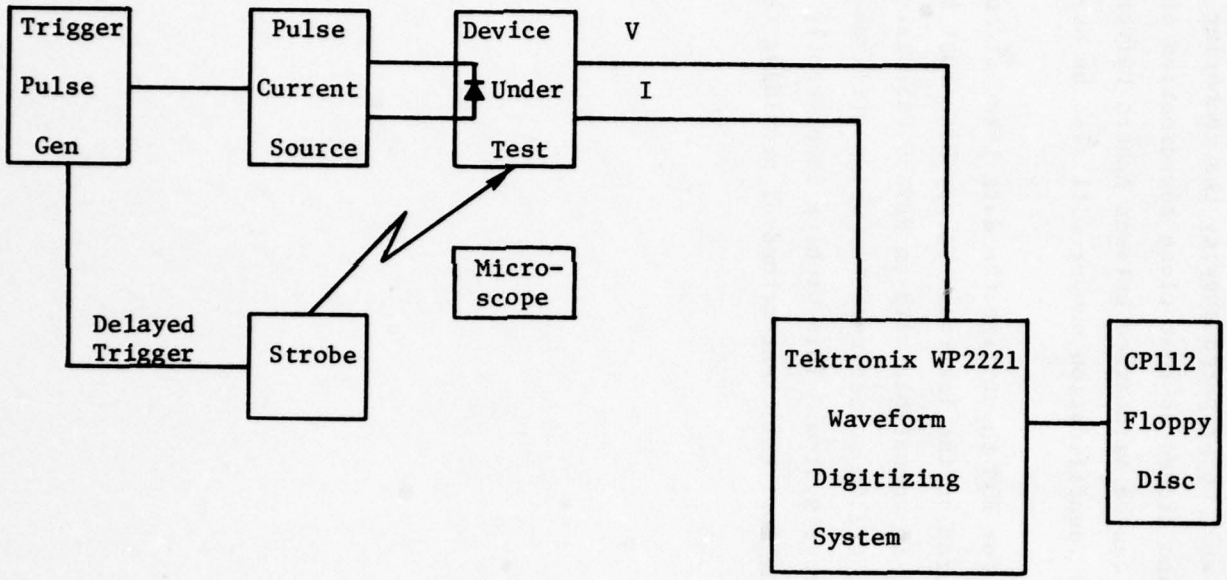


Figure 17. Block diagram of pulse test setup.

where A is the lot number (1, 2), B is the wafer number (1-5), CC is the die number (01-70), DD is the structure type (01-12), and EE is the diode number (01-51). A list will be prepared showing the numbering of the dice, structure types, and diodes so that close coordination of the various test structures can be maintained between Auburn University, Rockwell, and BDM. This identification number will also be used on all photographs.

In order for BDM to utilize the data taken at Auburn University, the data stored on the Tektronix Floppy Disc must be converted to a storage medium that is compatible with an HP9830 Calculator System (Cassette Storage) or an HP2100 series computer which utilizes a nine track magnetic tape storage system. This problem is presently being examined to determine the most efficient method of providing this interface.

SECTION IV
INVESTIGATION OF FAILURE MODES IN INTEGRATED CIRCUITS TESTED IN AN ELECTRICAL OVERSTRESS ENVIRONMENT

21. GENERAL

In the development of an effective hardness assurance program for the EMP-generated electrical overstress environment for semiconductor devices, the ultimate goal is a screening technique based on pretest terminal electrical measurements. Much difficulty has been encountered in achieving this goal for discrete devices, and indeed the problem is more complex for integrated circuits (ICs). One of the first steps in pursuit of this goal is a basic understanding of the nature of junction and metallization burnout failure in discrete devices and a correlation of the pulse power failure levels to basic device physical parameters. This step must be reached before there is any hope of arriving at an effective screen for integrated circuits.

A reasonably good understanding of the nature of the junction burnout mechanism has been established.[10-14] The physical parameter dependencies of metallization burnout have also been well documented, and predictions of current density failure thresholds can be made if the cross sectional area of the metal runs, the nature of the surrounding medium and the specifications for oxide step coverage, allowable scratching, etc. are known. Test patterns have been designed at Rome Air Development Center (RADC) for use as metallization burnout screens. In most discrete devices the pulse power failure level for metallization burnout is much greater than for junction burnout. Thus the major emphasis is given to junction burnout. This is not necessarily the case with certain ICs, especially MOS devices. Previous studies have shown that metallization burnout is the predominent failure mode in some MOS devices.[3] The pulse power failure levels for these devices, however, are generally greater than for other categories of ICs having junction burnout as the predominant failure mode.

For most IC types the main concern is with junction burnout. An effective hardness assurance screen, therefore, must necessarily be able to relate terminal electrical measurements to the junction pulse power failure threshold. In order to establish what type of terminal measurements might lead to a reasonable hardness assurance screen, one must first identify the most vulnerable component in an IC for a given test condition. In this study failure data were from several programs were analyzed to determine the predominant failure mode in different types of small and medium scale ICs representative of RTL, DTL, TTL, I^2L, ECL, MOS and linear bipolar technologies.

Most of these programs have concentrated on characterizing the pulse power failure thresholds for a number of IC types without identifying the failure mode. When failure mode data was included it was generally performed as a special test on a selected sample of devices and not included in the scope of the general test program.

The purpose of this study was to review the data generated on these programs to (1) identify the failure modes for each device by analysis of the pre- and posttest electrical data, pre- and posttest curve tracer data and posttest microscopic examination of the semiconductor chip and (2) identify devices whose pulse power failure threshold was on the extreme low end of the distribution to determine if these devices had either a distinctive failure mode or any distinguishing pretest electrical characteristics.

22. DISCUSSION OF DATA BASE FOR FAILURE MODE ANALYSIS

Table 5 is a list of the programs used as a data source for this investigation. It includes the type and quantity of ICs tested and the type of supplemental data recorded.

In the first two programs listed in Table 5, the objective was to characterize a large number of different types of ICs at various pulse widths, various test conditions and for both pulse polarities.[3] From this data a fit was made to the general relationship

Table 5. Electrical overstress programs.

Program	Circuit types tested	Quantity of each type tested	Pre- and posttest data
1. "Modeling and Testing of Integrated Circuits," Boeing subcontract G806701-9567, Prime contract from AFWL F29601-72-C-0028	TTL - 10 types DTL - 2 types Linear - 6 types	Typically 24 (2 for each of 2 polarities, 3 pulsewidths and 3 test conditions.)	dc specification tests (recorded), curve tracer (recorded) Microscopic inspection and photos on selected devices.
2. "Modeling and Testing of Integrated Circuits and Discrete Semiconductor Components," Boeing subcontract 6845058-9167, AFWL contract F29601-74-C-0008	TTL - 7 types RTL - 5 types DTL - 16 types ECL - 3 types MOS - 4 types Linear - 7 types	Same as above	Same as above
3. "MOS Model Development," AFWL Contract F29601-74-C-0106 Sponsored by DNA	MOS - 3 types	Same as above	Same as above with microscopic inspection of all failed devices.
4. "EMP Assessment and Hardening of E-4 Subsystems," Boeing subcontract	TTL - 3 types DTL - 2 types MOS - 2 types Linear - 1 types	50 each (open circuit voltage - 2 pulsewidths)	dc specification (go - no go) No curve tracer or microscopic inspection
5. "Electrical Overstress Screen Development," RADC contract F30602-76-C-0308	40 types including DTL, RTL, MOS, Linear and I^2L	15 each (one test condition and two pulsewidths)	dc specification (go - no go) curve tracer on selected devices (not photographically recorded) Microscopic inspection on selected devices

$$P_f = At^{-B}$$

where P_f is the pulse power failure level, t is the time to failure, and A and B are constants to be determined from the data.

The test methodology used in these programs consisted of a pretest analysis, pretest electrical characterization, pulse test, post-test electrical characterization, and cosmetic analysis. In the pretest analysis an evaluation of the circuit schematic was made to determine the worst case pulse polarity and weakest terminal. Also the electrical characterization, failure criterion and starting pulser level were established. The pretest electrical characterization consisted of all of the dc specification tests which were run on a Fairchild 5000. These data were measured and recorded before pulsing and after each overstress pulse. In addition to the Fairchild 5000 data, a curve tracer test was made from the pin being stressed to the ground pin. This curve was photographically recorded for each overstress pulse before and after the test. The electrical overstress tests were performed using a step stress approach on a sample of two devices for each set of variables. The variables included three different pulse widths (10 μs, 1 μs and 0.1 μs) and three different test configurations (input to ground, output to ground and V_{CC} to ground). For each test configuration the worst case pulse polarity was used for all three pulse widths. In addition, the opposite polarity was used for the 10 μs pulsewidth. These combinations yielded a total of 24 test devices for each device type. In some cases variations were made in the test conditions because of system considerations. Occasionally, additional samples were tested when it was not clear which pulse polarity was worst case or where devices failed on the first pulse. However, at least eight devices were tested per test condition.

The failure criterion was generally that of exceeding the manufacturer's dc electrical specification, although in some cases a radical change in the curve tracer characteristic constituted a failure even though the device passed the manufacturer's specifications. Since

for many parameters, especially leakage currents, typical parameter values are orders of magnitude below the specification limit, large shifts in parameter readings can take place before the device fails. Thus in many cases the pulse power to initiate degradation of some component in the IC is far below the power level required to cause circuit failure per the specification limits.

The pulse power level for each pulse was determined from oscilloscope photographs of the device current and voltage. These data were reduced and recorded for the highest no fail pulse and the failure pulse.

Two special tests were conducted to (1) determine the variation of pulse power failure with manufacturing techniques and packaging and (2) investigate the failure modes in selected device types. In these special tests CMOS inverters (model 4000) were obtained from two manufacturers in each of two package types (plastic and ceramic) and TTL NAND gates (model 7400) were obtained in ceramic packages from three manufacturers. All of the devices in ceramic packages tested to failure were opened and examined microscopically to determine any surface visual evidence of failure. This information, along with the Fairchild 5000 and curve tracer data, was used to determine failure category. Several other test program devices which were packaged in either metal cans or ceramic packages were opened and photographed but these data have not been analyzed.

In the "MOS Model Development" program with AFWL and DNA,[15] three types of MOS ICs were subjected to a thorough analysis and testing program. These included a CD4051 eight channel multiplexer/demultiplexer, an MC14024 seven-bit binary counter and an FS3349 hex 32-bit shift register. The objective of the electrical overstress portion of the program was a definition of a model to predict the pulse power failure level for an MOS IC. This model was experimentally verified on the three circuits. Since the modeling effort involves a thorough analysis and understanding of the circuit with predicted failure threshold for specific circuit components, particular interest was paid to failure modes in the experimental verification of the model. Therefore a complete cosmetic analysis was performed on each device along with pre- and post-test electrical characterization to determine failure mode. The analysis

indicated electrical overstress failure from three mechanisms: junction shorts, metallization burnout (in cases where the current exceeds a threshold value for a given pulsewidth), and gate oxide punchthrough. All three of these mechanisms were verified experimentally.

In the EMP assessment of E-4 subsystems, over 1,000 devices were tested for open circuit voltage failure level.[5,16,17] Seven different types of IC's were analyzed; 50 devices were tested for each test condition. The nature of the electrical overstress testing was determined from system considerations and involved open circuit voltage tests with a source impedance of 100 ohms at pulse widths of 44 μs and 0.44 μs.

Devices were first characterized on an ALMA IC tester for dc electrical specification parameters to insure that the devices were electrically good. They were then subjected to an electrical overstress pulse and rechecked on the ALMA to determine if they still passed the specification. The failed units were removed from further tests and the open circuit failure voltage was recorded. The 50 devices in a test group were sequenced through this procedure until all failed. None of the electrical characterization data was recorded and no packages were opened for microscopic inspection. The data was presented in the form of histograms of the number of failed devices versus the incremental open circuit failure voltage.

The electrical overstress screen development program with RADC involves electrical overstress testing on 40 types of ICs, including newer technologies such as integrated injection logic (I^2L). In this program the overstress pulsing was designed to simulate both static electrical pulses and system generated pulses. These are represented by double exponential pulses with time constants of 150 ns and 10 ms respectively. The testing sequence and data reduction were similar to that of the E-4 assessment tests. Devices were first characterized on an ALMA IC tester, then subjected to electrical overstress pulses of increasing amplitude and rechecked after each pulse on the IC tester. The open circuit peak voltage of the exponential pulse was incremented in 2.5-volt steps to give good resolution to the failure levels. When a device failed to meet the electrical specification, the failing parameter (but

not the value) was recorded. The tests involved 15 devices of each type for each test condition. Selected failed devices were subjected to an analysis both by curve tracer measurements and microscopic inspection to determine failure mode. Typically three devices of each type were subjected to curve tracer analysis and one to three devices were opened for microscopic analysis.

The objective of this study was to survey data from the aforementioned programs to identify failure modes and to determine distinguishing characteristics of devices whose pulse power failure level is well below that of the "nominal" level for that device type. In addition, the data were surveyed to determine differences between circuit types from different manufacturers having widely different "nominal" failure levels for the same circuit type.

Most of the effort involved an examination of the data from the two AFWL-sponsored integrated circuit test programs (Table 5, Programs 1 and 2). These programs involved a large number of device types and also provided recorded variables data as well as photographs of selected failed devices for posttest analysis.

The MOS modeling program included detailed analysis of failure mode but only involved a relatively small sample of three device types.

The E-4 program involved large sample sizes, but no pre- or posttest data was recorded. Microscopic examination of the failed devices would be extremely difficult since all but one device type was packaged in plastic dual in line packages. Chemical etching of these packages is tedious and often results in damaging the chip to the extent that identification of failure modes is not possible.

23. INTEGRATED CIRCUIT FAILURE MODE STUDY

A complete examination of all of the IC electrical overstress data taken on the "Modeling and Testing of Integrated Circuits and Discrete Semiconductor Components" program was performed to identify and categorize pulse power failure modes. The raw data on the program included:

a. A listing of the Fairchild 5000 dc electrical test program with test conditions and limits.
b. A circuit schematic of the IC showing the electrical overstress test conditions.
c. Digitized plots of the current and voltage waveforms for the highest no fail pulse and the failure pulse with calculated average power and energy curves.
d. Oscilloscope photographs of the current and voltage waveforms for each of the overstress pulses.
e. Copies of the pre- and posttest Fairchild 5000 dc electrical test data.
f. Curve tracer photographs of pre- and posttest electrical characteristics.

In addition to these data, photomicrographs were taken of chips from selected devices.

The procedure for determining the failure mode for each device type first involved a careful examination of the circuit schematic and photomicrograph of the chip (when possible) to identify the most susceptible components. In such an analysis the most vulnerable junction was assumed to be a reverse biased emitter-base junction; reverse biased junctions were assumed to be more vulnerable than forward biased junctions; smaller area junctions were assumed to be more vulnerable than larger area junctions; junctions closest to the terminal being pulsed were assumed to experience greater power dissipation than those farther away. All parasitic junctions (primarily involving isolation regions and diffused resistors) were also identified to determine the lowest resistance path for both positive and negative pulses from the stressed terminal to ground so that a proper interpretation could be made of the curve tracer photographs.

The second step in the failure mode determination included an examination of the dc electrical specification tests to determine what individual component electrical characteristics are represented by the test. For example, in a DTL gate the input leakage current is representative of the reverse current of the input diode, and the output voltage low is representative of the collector-emitter saturation voltage

of the output transistor. After understanding of the dc electrical tests was reached, examination of the changes in these parameters helped to identify the circuit components affected by the electrical overstress.

After a reasonable understanding of the curve tracer and Fairchild 5000 tests was acquired, individual device data were examined to determine the parameters that showed degradation from pulse to pulse and the parameter changes that eventually constituted failure. In this program the failure criterion was defined in the pretest analysis. In most cases this criterion was a failure to meet the manufacturer's specification on any of the dc electrical tests. Occasionally a failure was determined from a dramatic change in the curve tracer characteristic even through the device passed the Fairchild 5000 tests.

For each device type a list was formed giving the unit number, overstress test condition, pulse polarity and width, pulse power failure level, and a description of the changes observed in the Fairchild 5000 and curve tracer data. Large parameter shifts or curve tracer characteristic changes observed after nonfailure pulses were also recorded. The description of the Fairchild 5000 data shifts included a list of all parameters that failed the specifications and noted whether the shift was small or caused an overrange on the readout (implying a large but undefined shift). In the case of the curve tracer data, the characteristics of the failure were noted in terms of whether the overstress pulse caused a short, a resistive path, an open circuit, a change in breakdown, a change in slope, increased leakage, or no change.

The noted changes in the dc electrical tests and the curve tracer photos were coupled with the circuit analysis in order to determine the probable cause of failure. After the probable cause of failure was determined from this analysis, the photomicrographs (when available) of the device were inspected to confirm or deny the analysis. Since only a selected number of devices was inspected microscopically, an attempt was made to obtain the uninspected failed devices in order to extend the microscopic analysis to include all units packaged in either metal cases or ceramic packages.

The only device types remaining in storage at AFWL which could be easily opened for inspection were the MC317 ECL device and the MC1530G linear device. These devices were opened and visually inspected for damage using a 280-power Bosch and Lomb microscope.

23.1 Results of Failure Mode Study

23.1.1 DTL Circuits. A total of 14 different types of DTL circuits were analyzed in this study. Several of these circuits were obtained from two different manufacturers representing different packages, generally platic dual in-line and metal cases.

The predominant failure mode for DTL circuits with the input terminal stressed was a junction failure of the input diode. The electrical test evidence for this mode was an increase in the reverse current (IR) test for the input pin under test. The input diode on a DTL circuit is generally formed by an emitter and base diffusion, with a typical breakdown voltage of 6 to 8 volts. Since in general the emitter-base junction of a transistor is the most susceptible to electrical overstress, the input diode would be expected to be the most vulnerable, especially for the positive pulse polarity that would result in a reverse bias on the input diode.

The 946 HC device illustrates this type of failure. Figure 18 is a circuit diagram for one of the four two-input NAND gates that constitute the 946 HC. In the positive input stressed condition the current passes through the reversed biased input diode and then through three forward biased junctions. For the negative stressed input, the current path is through the forward biased diode; resistors R_1, R_2, and R_3; the forward biased collector-base junction of Q_2; and resistor R_4. The curve tracer photo of Figure 19 illustrates these current paths from pin 3 to ground in the positive and negative directions. As shown in Figure 19, the breakdown voltage of the input diode is about 6 volts. Figure 20 is a photomicrograph of the 946HC chip.

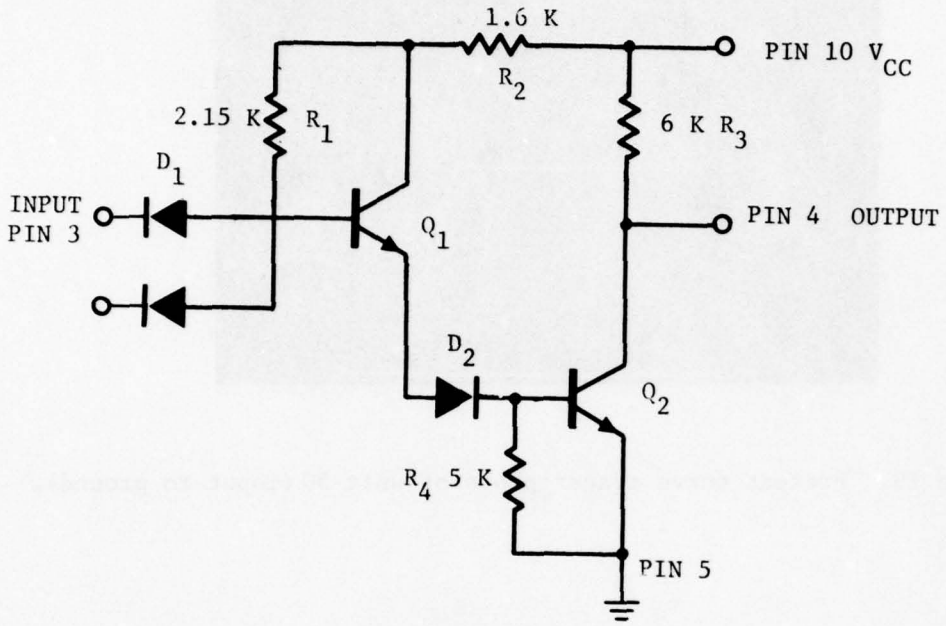


Figure 18. Circuit schematic of one 946 HC NAND gate.

Unit 50 was exposed to negative 10-μs overstress pulses and failed on pulse 3 at a pulse power of 48.9 watts. The Fairchild 5000 indicated no change in any of the electrical tests up to pulse 3. Failure occurred on pulse 3 when I_R overranged, indicating a current in excess of 16 μA. V_{OL} increased from a pretest value of .207 volts to .240 volts. These data would indicate a failure of the input diode. Figure 21 is a curve tracer photo of unit 50 for the input to ground terminal after pulse 3. It is clear that the reverse-biased input diode is gone and the other two forward junctions Q_1 (E-B) and D_1 remain. These data also indicates that only the input diode was shorted.

Figure 22 is a close up of the input diode on unit 50 showing the damaged area. The region of damage shown by the arrow is rather small and subtle, a characteristic of junction shorts seen on other devices.

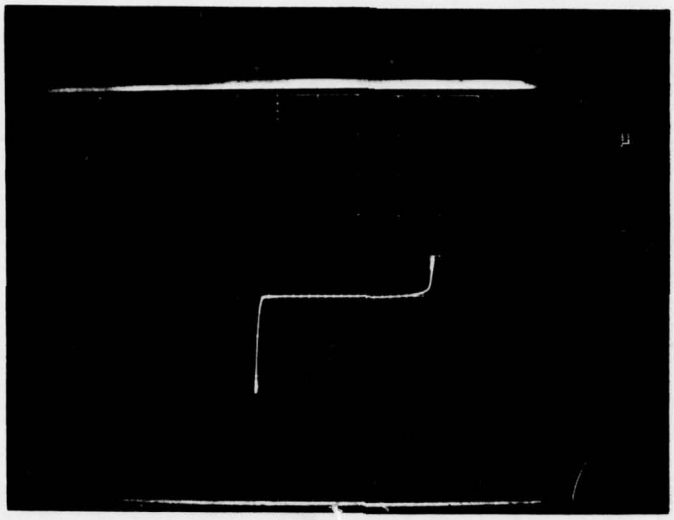


Figure 19. Pretest curve tracer pho of unit 50 (input to ground).

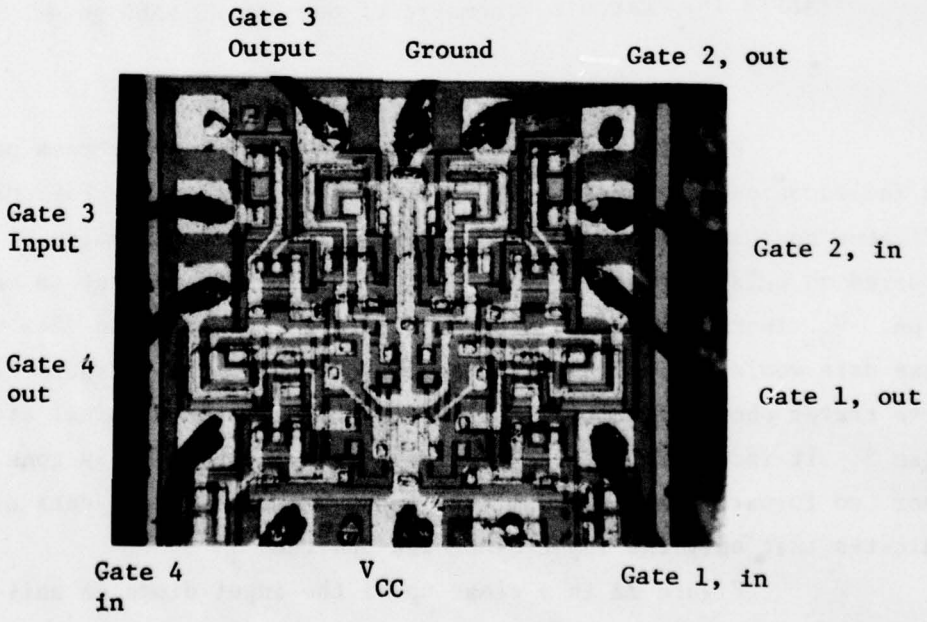


Figure 20. Photomicrograph of 946 HC chip.

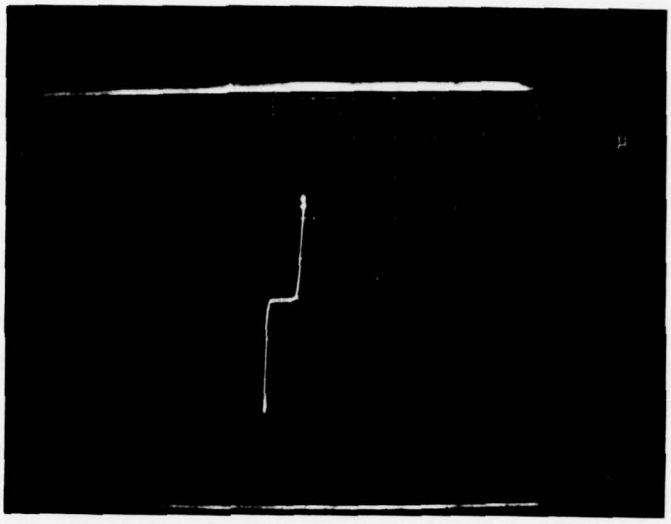


Figure 21. Curve tracer photo of unit 50 after third overstress pulse (input to ground).

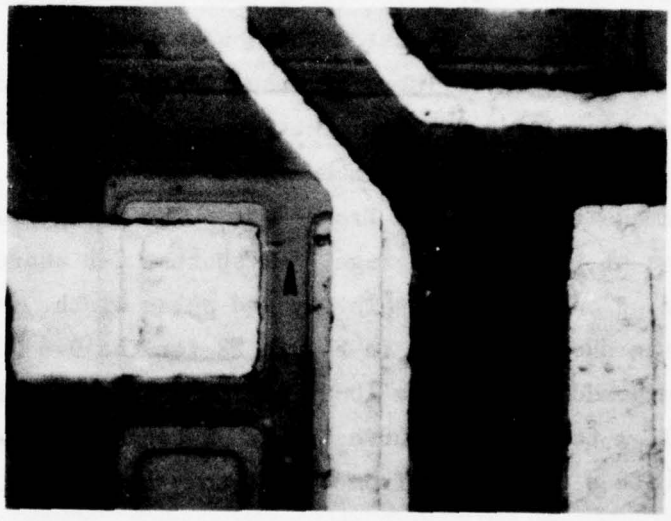


Figure 22. Junction short on input diode, 946 HC unit 50.

Another type of failure observed on DTL circuits with the inputs stressed was that of multiple junction shorts. This case is illustrated by unit 52, which was subjected to positive 10-μs pulses and failed on pulse 6 at a power of 23.9 watts. In this case the Fairchild 5000 data showed an overrange of I_R plus a failure of V_{OH}, I_{CEX}, a decrease in V_{OL} and an increase in I_{SC}. These data would indicate that the input diode was damaged and the output transistor would not assume the high state. In order for the output transistor to go high for the V_{OH} test the input transistor must be turned off. This cannot be achieved if the emitter-base junction of Q_1 is shorted. The pre- and posttest curve tracer photos shown in Figures 23 and 24 indicate shorts not only at the input diode and the Q_1 (E-B) junction but at D_1 as well. The photomicrographs of Figures 25, 26, and 27 illustrate the junction shorts of junctions D_1, Q_1 (E-B) and D_2 respectively on unit 52.

The only other clearly distinguishable input stressed DTL failure mode was metallization burnout. Resistor shunting and internal junction shorts may have occurred in certain devices but the pre- and posttest data were not sufficient to clearly identify the damaged area. The only photomicrographs taken of DTL devices were those taken on the 946 HC devices and none of the tested units were located so that further analysis could be performed. Therefore the identification of failure modes in DTL was based primarily on electrical characterization.

The primary failure mode for output stressed DTL circuits was junction damage to the output transistor. The damage involved all three variations of transistor damage (C-E shorts, C-B shorts, and E-B shorts), depending on the pulse polarity and pulse width. An illustration of a C-E junction short is shown in Figure 28 for the 946 HC unit 59. This unit was exposed to negative 10-μs pulses and failed the posttest V_{OH}, I_{SC}, and I_{CEX} tests. The curve tracer photographs shown in Figures 29 and 30 indicate a dead short from output to ground after the failure pulse.

Other failure modes for DTL devices stressed at the output terminals included resistor shunts (characterized by increased power supply currents with no corresponding change in input or output parameters) and metallization burnout (indicated by an open circuit in either the

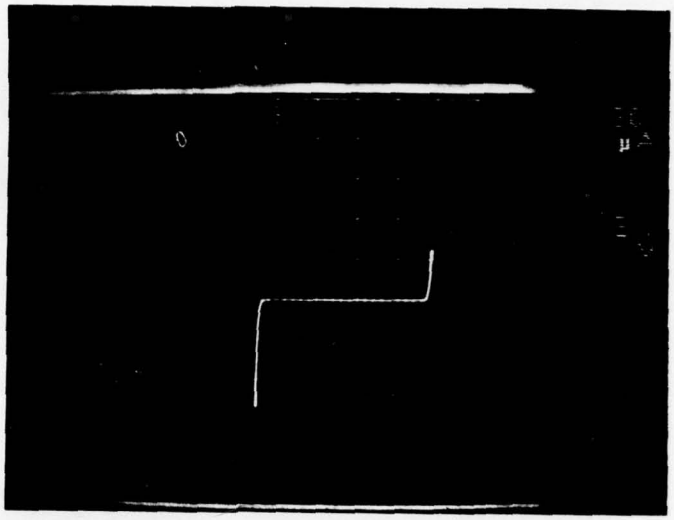


Figure 23. Pretest curve tracer photo of 946 HC unit 52 (input to ground).

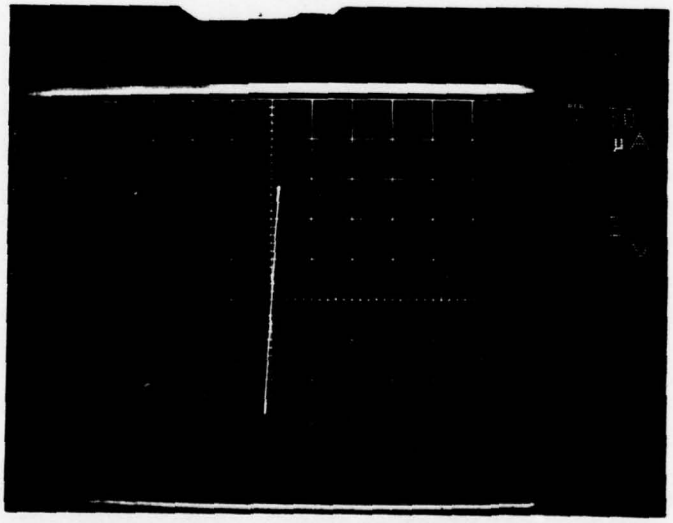


Figure 24. Posttest curve tracer photo of 946 HC unit 52 (input to ground).

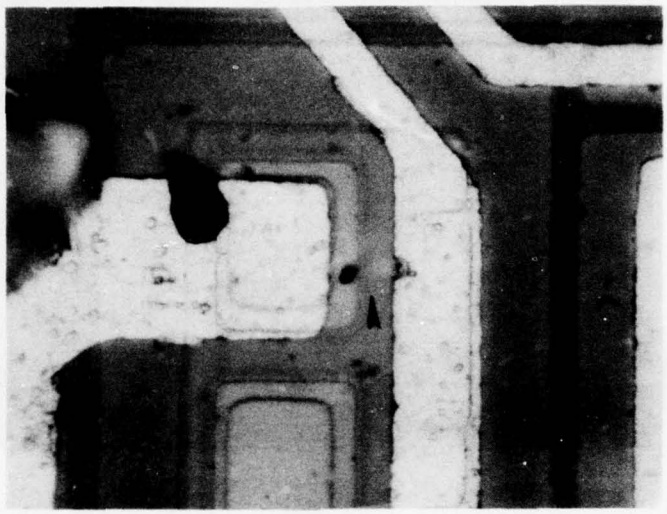


Figure 25. Photomicrograph of D_1 junction short on 946 HC unit 52.

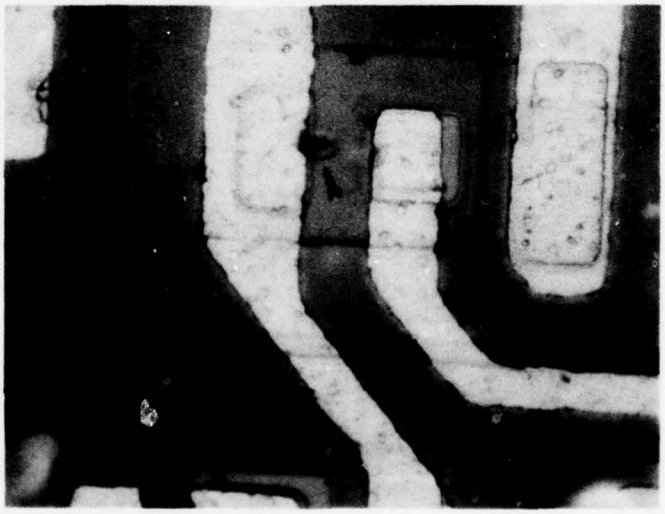


Figure 26. Photomicrograph of Q, (EB) junction short on 946 HC unit 52.

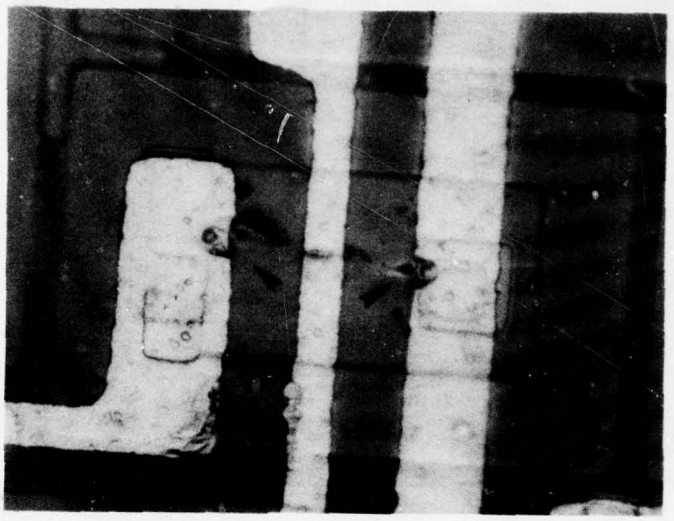


Figure 27. Photomicrograph of D_2 junction short on 946 HC unit 52.

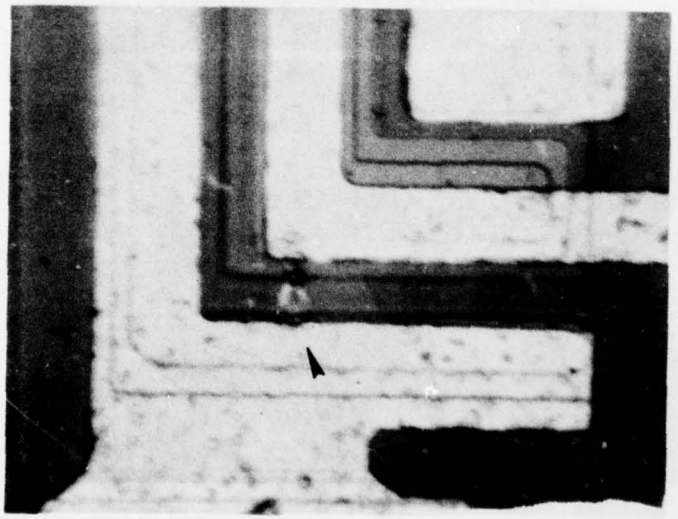


Figure 28. Photomicrograph of output transistor C-E short on 946 HC unit 59.

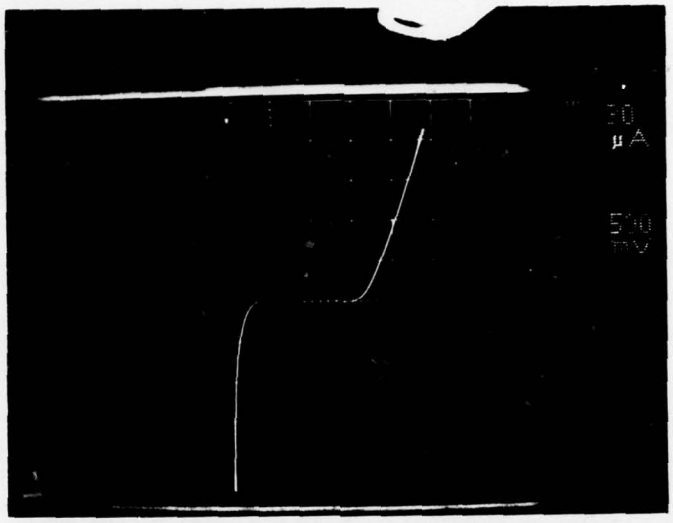


Figure 29. Curve tracer photo of 946 HC unit 59 pretest.

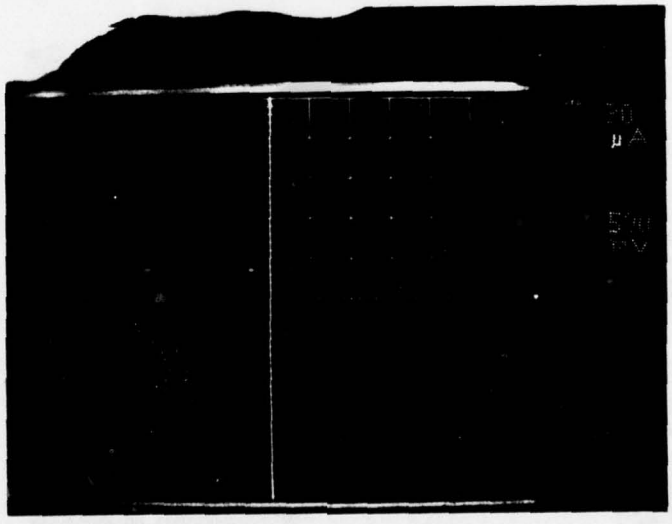


Figure 30. Curve tracer photo of 946 HC unit 59 posttest.

positive or negative direction on the curve tracer photo). The metallization burnout failure mode often accompanies junction damage[11] and often occurs at an oxide step or where the metallization path crosses over a junction dissipating a great amount of heat. Without photomicrographs it is difficult to distinguish when the burnout is accompanied by junction damage. Therefore all metallization burnout failures were classified under one heading whether they occurred alone (generally at the short pulse widths) or were accompanied by junction damage.

DTL failure modes caused by stressed power supply terminals were generally more difficult to ascertain. For this test condition, the power failure levels were generally much greater than for either the input or output test conditions since the power is distributed over a greater number of components. Most of the circuits tested were dual or quadruple circuits contained in a single package with a single V_{CC} terminal supplying voltage to each circuit.

The predominent failure mode for the V_{CC} terminal was the output transistor with no consistancy as to which of the multiple gates within a package was affected. Other failure modes were resistor shunts, metal burnout, and multiple junction shorts involving internal transistors. A rather dramatic example of metallization burnout is shown in Figure 31

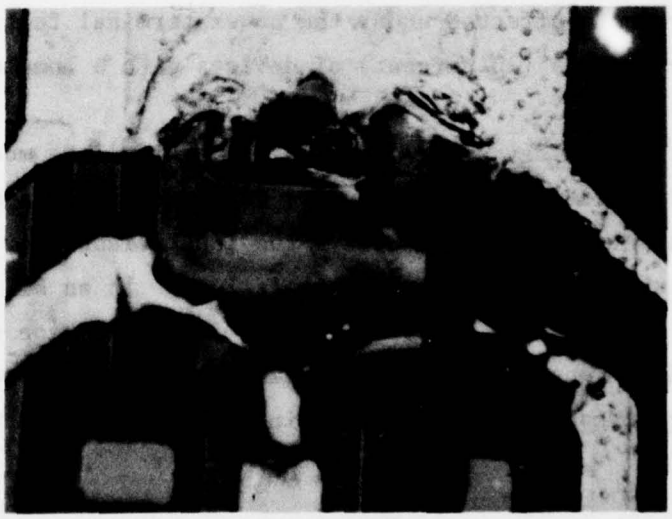


Figure 31. Photomicrograph of metallization burnout on 946 HC unit 69

for unit 69 (946 HC), which was stressed with negative 10-μs pulses and failed at 123 watts. The large metallization area at the top of Figure 31 is the V_{CC} line and the three-branch path at the bottom is the ground line.

A summary of the results of the failure mode identification for DTL devices is given in Table 6. The left column of Table 6 is a list of the device types analyzed. The "HC" refers to a metal case package and the "DM" indicates a plastic dual in-line package. The summary indicates the total number of devices tested and the number of device failures in each indicated category. For the input stress condition multiple junction failures which involved the input diode were listed under input diode failures since it is most probable that the input diode was the first junction to go. Had the incremental power levels been small enough, the single junction failure would have been observed at the failure threshold.

The results of the summary show that 90 percent of the input stressed DTL circuits failed because of the input diode and 80 percent of the output stressed devices failed because of the output transistor. The percentages of metallization failures are consistant with previous reports[11] for the input and output terminals but were much higher at 18 percent for the power terminal. Because of the number of potential components affected under the power terminal test, there was a rather high percentage (30 percent) of devices with a complex or unidentified failure mode.

23.1.2 RTL Circuits. The predominant failure mode for the input stressed condition on RTL circuits was junction damage on the input transistor. However it was not always the input transistor connected to the input pin stressed that resulted in failure. In an RTL circuit the input lead is connected to a resistor which feeds the base of an input transistor. This input resistor dissipates much of the power during an electrical overstress test, thus affording some protection to the input

Table 6. Summary of DTL electrical overstress failures.

Type	Description	Input Terminal Stressed				Output Terminal Stressed				V_{CC} Terminal Stressed			
		Total Tested	Input Diode	MBO[a]	Other	Total Tested	Output Transistor	MBO RS[b]	Other	Total Tested	Output Transistor	MBO RS	Other
RC930	Dual 4 input NAND gate	8	7	1	0	10	10	0	0	6	6	2-RS	0
930HC	Dual 4 input NAND gate	8	8	0	0	10	8	2-MBO	0	7	7	2-RS	0
932HC	Dual 2 input NAND buffer	10	10	0	0	9	9	0	0	8	8	0	0
DM944	Dual 2 input NAND buffer	10	9	0	1	8	8	0	0	9	1	5-RS	3
944HC	Dual 2 input NAND buffer	8	8	0	0	10	10	0	0	8	2	6-RS	0
945HC	RS flip flop	9	3	0	6	9	4	2-RS	3	13	0	7-MBO	6
DM945	RS flip flop	12	12	0	0	10	6	0	4	10	0	1-MBO 1-RS	8
DM946	Quad 2 input NAND gate	10	10	0	0	8	8	0	0	8	5	3-RS	0
946HC	Quad inverter	8	8	0	0	8	8	0	0	8	4	3-MBO 1-RS	0
HC948	RS flip flop	8	8	0	0	9	9	0	0	8	0	7-MBO	1
DM948	RS flip flop	12	11	1	0	8	4	0	4	12	0	0	12
SE156N	Dual 4 input line driver	13	11	1	1	0				0			
SE180	Quad 2 input NAND gate	17	17	0	0	0				0			
MC1488	Quad 2 input line driver	8	8	0	0	12	11	1-RS	0	0			
MC1489	Quad line receiver	14	9	0	5	8	8	0	0	0			
SN7413	Schmitt trigger	8	8	0	0	8	0	0	8	0			
	Totals	163	147	3	13	127	103	2-MBO 3-RS	19	101	33	20-RS 18-MBO	30
	Percent		90	2	8		81	1.5-MBO 2.5-RS	15		33	20-RS 18-MBO	30

[a] MBO = metallization burnout
[b] RS = resistor shunt

transistor. In some of the RTL circuit layouts, however, the connection to the input pin side of the resistor on one input is in close proximity to the connection to the base side of the resistor on another input. This is illustrated by the photomicrograph of a 908 HC adder circuit shown in Figure 32.

Several devices failed when a short developed from the stressed input to the transistor of an adjacent input, causing a junction short on the adjacent input. This failure mode is shown in Figure 33 for a 908 HC buffer circuit (unit 50) which was stressed on pin 1 with negative 10-μs pulses. The initial short is from the stressed input side of the diffused resistor through the isolation to the base side of an adjacent resistor (Figure 34). Once this path was established, the emitter base junction of the adjacent transistor was shorted (Figure 35). The same failure mode was also observed on the 908 HC for positive overstress pulses. The only other failure mode for the input stressed condition was a substantial drop in the input resistor value, observable on the curve tracer photos. This drop was generally observed before the actual failure pulse but probably contributed to failure of the input transistor by lowering the resistive path to the input transistor.

The output terminal stressed failure mode for RTL circuits was predominantly degradation of the output transistor. This degradation did not always occur in the form of a junction short. Analysis of the electrical tests indicated several cases in which the gain of the output transistor was degraded to the point where the device would not pass a V_{OUT} test but would pass a V_{SAT} test. These two tests differ only with the externally applied voltage at the base of the output transistor. In both tests the output voltage is low but the turn on current is higher on the V_{SAT} test. Since the turn on current sets the forced gain of the output transistor, a higher forced gain will cause the device to fail if the actual transistor gain drops below this value. In many cases the device failed V_{OUT} with the higher forced gain but passed V_{SAT}. No metallization burnout or resistor shunting was observed for the output stressed condition.

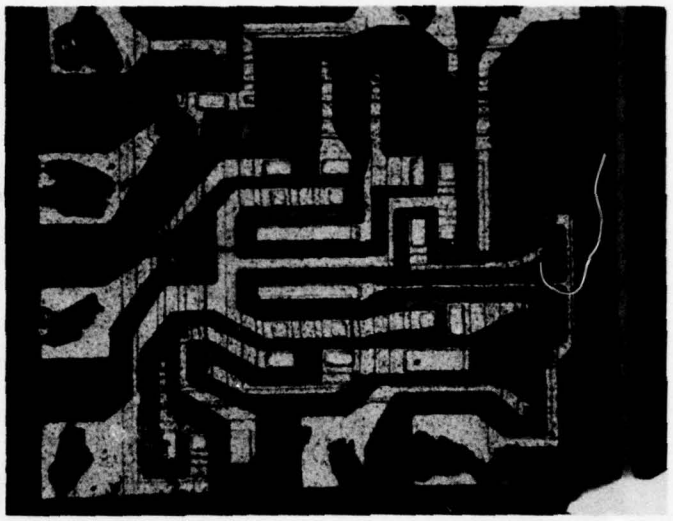


Figure 32. Photomicrograph of 908 HC adder.

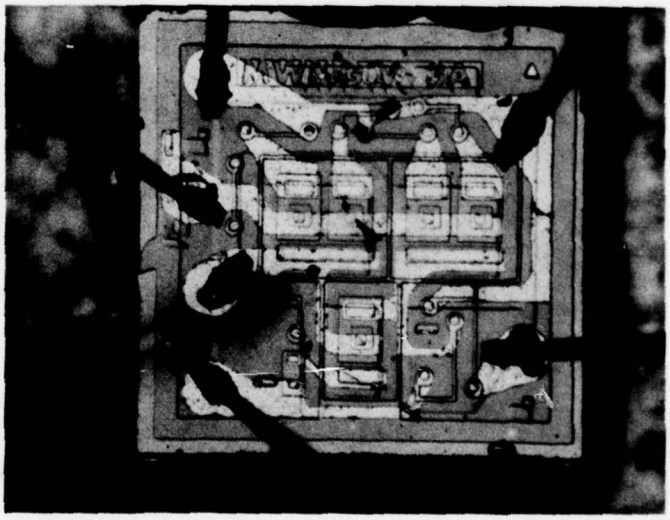


Figure 33. Photomicrograph of 908 HC buffer chip unit 50.

Figure 34. Photomicrograph of resistor-resistor short on 908 HC unit 50.

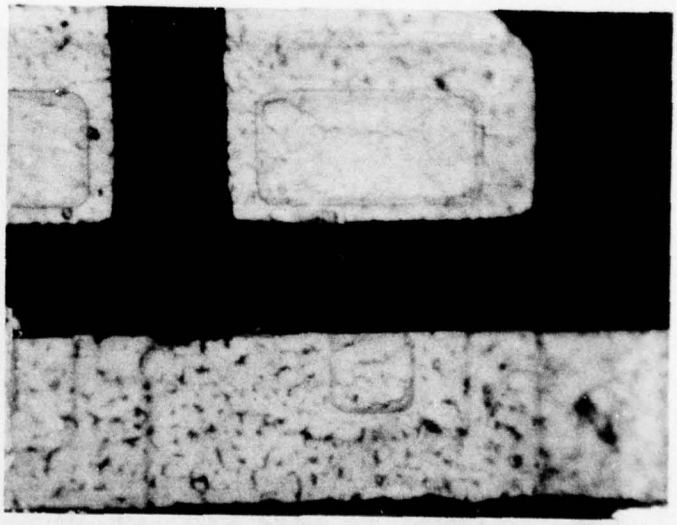


Figure 35. Photomicrograph of emitter base short on 908 HC unit 50.

For the VCC terminal tests, both output transistor damage and metallization burnout were observed. In several devices the failure mode was not clearly identifiable.

A summary of the failure mode determination for RTL is given in Table 7.

Of the 141 RTL devices examined only two clear cases of metallization burnout were observed. As with the DTL circuits most of the analysis of the RTL circuit was based on the curve tracer and Fairchild 5000 test results; only 10 percent of the devices were examined microscopically. The major conclusion regarding failure modes of RTL devices is that one failure mode (which constituted 26 percent of the input failures) was due to the chip layout and could be eliminated by appropriate redesign. Spacing the contact ends of the input diffused resistors farther apart would eliminate the shorting problem described earlier. This would raise the pulse power failure level for the input terminal.

23.1.3 TTL Circuits. Junction shorting of the input clamp diode constituted the major failure mode for the five types of TTL circuits analyzed in this study. This failure mode was much more predominant than failure of the input transistor, the only other failure mode observed on these circuits for the input stressed condition. An analysis of the failure modes in the 7400 Quad 2 input NAND gate is given in reference 3. These devices were purchased from three different vendors, all in a 14-pin ceramic dual in-line package so that cosmetic analysis could be performed. All of the other TTL devices tested under this program were in plastic packages and thus were not microscopically analyzed.

An illustration of the clamp diode short is given in Figure 36 for the N7400F unit 7 which was overstressed with positive 1-μs pulses and failed on pulse 9 at 114 watts.

The diode clamp short in Figure 36 can be seen next to the pad on lead 1 with the short extending over to the isolation region. The input diode clamp short was easily observed on the curve tracer photos, appearing as a dead short from input to ground.

Table 7. Summary of RTL electrical overstress failures.

Type	Description	Input Terminal Stressed				Output Terminal Stressed				VCC Terminal Stressed			
		Total Tested	Input Transistor	Adjacent Input Transistor	Other	Total Tested	Output Trans. Shorted	Output Trans. Degraded	Other	Total Tested	Output Transistor	MBO RS	Other
908	Adder	10	10	0	0	8	7	1	0	8	5	1-RS	2
909	Buffer	10	3	7	0	8	8	0	0	10	2	0	8
910	Dual 2-input NOR gate	10	6	4	0	8	4a	4a	0	10	4[a]	0	6
911	4-input gate	10	8	2	0	11	4	7	0	8	0	0	8
912	Half adder	10	7	0	3	10	7	3	0	10	0	2-MBO	8
	Totals	50	34	13	3	45	30	15	0	46	11	2-MBO 1-RS	32
	Percent		68	26	6		67	33	0		24	4-MBO 2-RS	70

[a]There is no "output" transistor on the 910 gate since the two collectors of the input transistors are tied together to form the output. Therefore, one of the two inputs is here considered the "output" transistor.

For the output terminal stressed condition the major failure mode was junction damage to the output transistor. Resistor shunting and metallization burnout failure modes were also observed for this test.

Only one of the TTL circuits (SN7490 decade counter) was tested for the V_{CC} terminal, and in this case the failure mode was indeterminate. No metallization burnout or damage to the output transistor was evident. The most probable cause of failure was junction shorting on one or more of the internal transistors.

Table 8 is a summary of the TTL failure mode determination. Only the input and output stressed conditions are given since in only one case was the V_{CC} terminal stressed and the failure mode was indeterminate.

23.1.4 ECL Circuits. Three ECL circuits were investigated in this program. For the input stressed condition two failure modes were

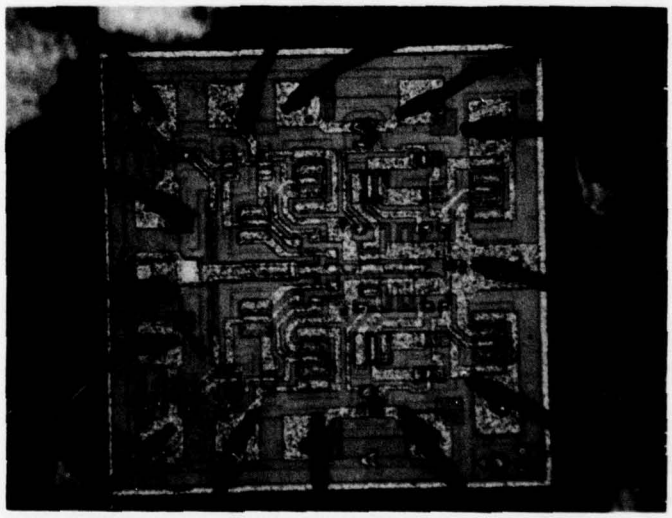


Figure 36. Photomicrograph of N7400F unit 7, illustrating clamp short.

Table 8. Summary of TTL electrical overstress failures.

Type	Description	Input Terminal Stressed			Output Terminal Stressed		
		Total Tested	Input Diode Clamp	Input Trans.	Total Tested	Output Trans.	MBO
MC4043	Line selector	8	8	0	6	4	2
MC7400L	Quad 2-input NAND gate	12	2	10	7	7	0
7400DC	Quad 2-input NAND gate	8	8	0	6	6	0
N7400F	Quad 2-input NAND gate	7	7	0	9	4	5
SN74H60	Dual 4-input expander	15	2	13	0	0	0
SN7490	Decade counter	8	8	0	6	6	0
SN74163	4-bit counter	16	16	0	8	8	0
	Totals	74	51	23	42	35	7
	Percent		69	31		83	17

easily identifiable: junction damage on the input transistor and metallization burnout. Junction damage was the predominant mode.

For the output stressed condition the predominant mode was output transistor junction damage. Metallization burnout was observed in two cases, and junction shorting of an internal diode was the cause of failure in two other units.

For the V_{CC} to V_{EE} stressed condition the predominant mode of failure was metallization burnout. This mode of failure resulted because of the high pulse power level required to cause failure. For the 308 J-K flip flop, the average 1-μs power failure for V_{CC} was 659 watts compared to 67 watts for the input and 17 watts for the output.

None of the failures could be unequivocally related to the output transistor; however, failure of an internal diode was evident on one device.

All of the ECL devices were packaged in either metal or ceramic packages which allowed for microscopic analysis. Of the stressed units 85 percent were examined but in 65 percent of the units examined no evidence of failure was observed.

A summary of the ECL failure mode analysis is given in Table 9.

23.1.5 Linear Circuits. The predominant failure mode for the linear circuits with the input terminal stressed was junction damage to the input transistor. Metallization burnout was also observed for this test condition. In several instances the failure modes were not clearly distinguishable from the Fairchild 5000 or curve tracer data. For the output stressed condition the two predominant failure modes were junction damage to the output transistor and metallization burnout. In the case of the VCC stressed terminal tests, junction damage to internal transistors occurred frequently, as did metal burnout.

A summary of the results of the linear circuit overstress failure mode analysis is given in Table 10. The circuits given in Table 10 were tested under the more recent Boeing contract. In the earlier program several other linear circuits were tested, including the N5710T

Table 9. Summary of ECL electrical overstress failures.

Type	Description	Input Terminal Stressed				Output Terminal Stressed				V_{CC} Terminal Stressed			
		Total Tested	Input Trans.	MBO	Other	Total Tested	Output Trans.	MBO D_1[a]	Other	Total Tested	MBO	D_1	Other
304	Bias driver	8	7	1	0	9	3	2-MBO	4	8	4	0	4
308	J-K flip flop	12	5	5	2	8	8	0	0	10	8	0	2
317	Logic translator	8	8	0	0	8	4	2-D_1	2	7	0	1	6
	Totals	28	20	6	2	25	15	2-MBO 2-D_1	6	25	12	1	12
	Percent		72	21	7		60	8-MBO 8-D_1	24		48	4	48

[a] D_1 = Internal diode junction short.

Table 10. Summary of LINEAR electrical overstress failures.

Type	Description	Input Terminal Stressed				Output Terminal Stressed				V_{CC} Terminal Stressed			
		Number Tested	Input Trans.	MBO	Other	Number Tested	Output Trans.	MBO	Other	Number Tested	Internal Trans.	MBO	Other
709HC	Op amp	12	10	0	2	9	6	0	3	7	2	2	3
µA715	Op amp	8	5	0	3	0				8	8	0	0
µA740	Op amp	8	6	2	0	0				8	0	6	2
µA776	Op amp	12	0	6	6	8	2	2	4	0			
SN75107	Line receiver	9	9	0	0	0				0			
MC1530G	Op amp	9	9	0	0	8	0	3	5	9	3	1	5
	Totals	58	39	8	11	25	8	5	12	32	13	9	10
	Percent		67	14	19		32	20	48		41	28	31

voltage comparator, LM103 voltage regulator and LM302 and μA 747 operational amplifiers. Although the electrical data were not analyzed on these circuits to determine failure mode, several of these devices have been subjected to a posttest examination with a scanning electron microscope (SEM). SEM pictures reveal much more detail about the damaged areas than can be observed with an optical microscope and thus can give insight into the nature of the physical mechanisms involved.

One such damaged area is shown in the SEM picture of Figure 37. In this photo a diode junction short on an N5710T voltage comparator is shown. At the surface of the chip a raised area is evident between the emitter and base diffusions which form the diode. The depressions at either end indicate that silicon material has melted and moved toward the center of the damaged region. The ball at the center is most likely resolidified molten silicon which escaped through a ruptured region at the center of the short.

Another failure mode is well illustrated by the SEM picture of Figure 38. Here a metallization lead which crosses over a diffused resistor has been splattered with a substantial amount of cratering into the silicon. Whether this failure was caused by a current constriction in the metallization resulting from the oxide step or a scratch or whether it resulted from excessive heating in the silicon beneath the metal cannot be determined.

Figure 39 shows an example of metallization burnout which did not occur at an oxide step or over a p-n junction. It is not known whether the crack down the center of the metal stripe was there before the overstress failure. This cracking of the metal next to a burned out region has been observed in several other devices.

23.1.6 MOS Failure Modes. The only MOS device tested in the Boeing program was the 4000 inverter plus complementary pair. This device was purchased from two vendors in both plastic and ceramic packages. The ceramic packages were opened and subjected to a cosmetic analysis with the results published in reference 3. The predominant failure mode for these CMOS circuits was metallization burnout. Another failure mode was that of gate oxide punch through even though this device

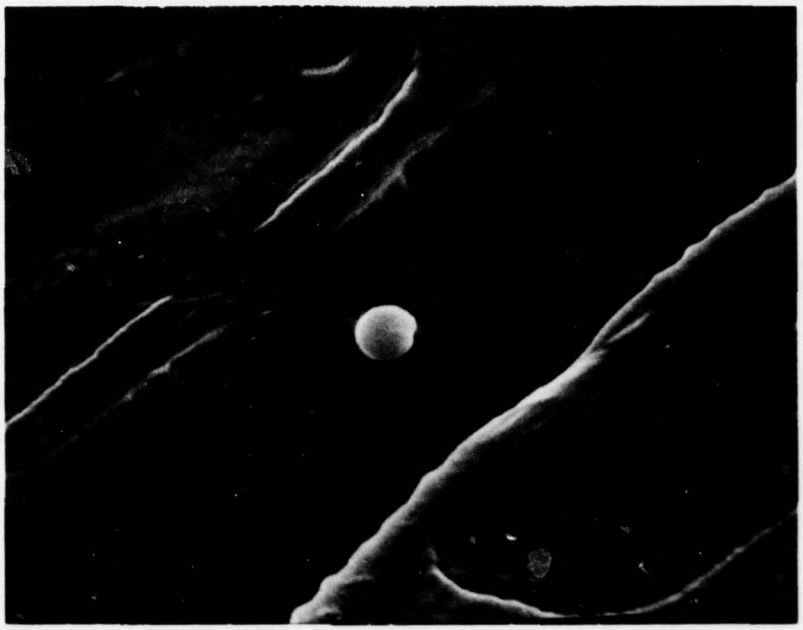


Figure 37. SEM picture of diode junction short on N5710T.

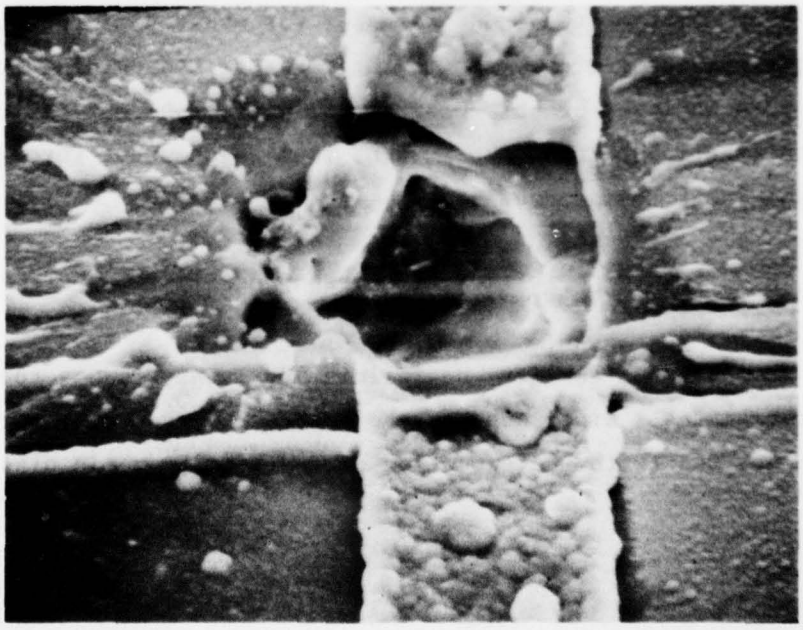


Figure 38. SEM picture of metallization burnout on a μA747.

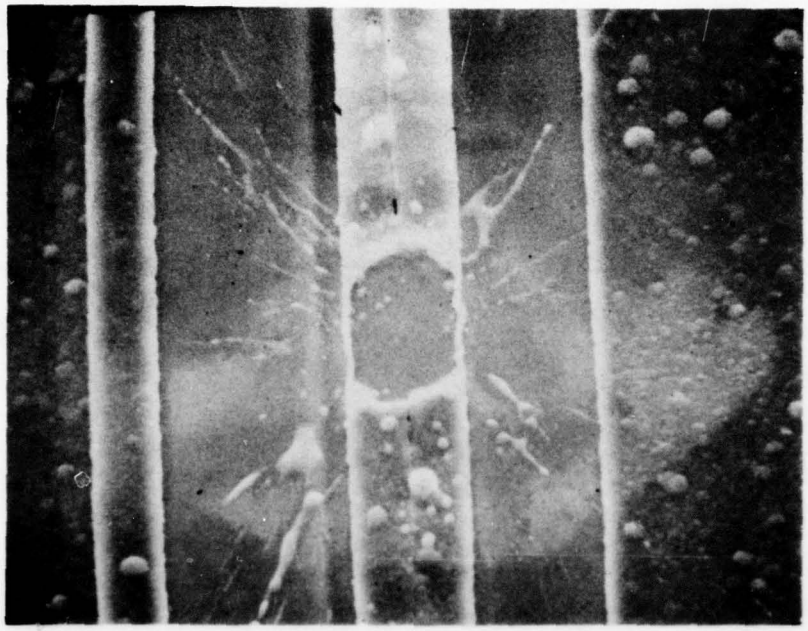


Figure 39. SEM picture of metallization burnout on an LM111.

had input protection. An unexpected failure mode was observed on the CD 4000 from RCA. Part of the input resistor was shorted to the V_{DD} base causing an excessive current flow in the resistor and burning it out. Of the 38 devices analyzed on this program, 63 percent of the failures were due to metallization burnout, 26 percent from oxide punch through, and 11 percent from input resistor burnout.

24. IC FAILURE MODE ANALYSIS ON OTHER PROGRAMS

As mentioned earlier, no failure mode analysis was conducted on the E-4 program tests since none of the posttest data were recorded and all of the devices (with the exception of one type) were in plastic

packages. The overstress failure analysis on the MOS modeling program involved three CMOS circuits. The failure modes were modeled and verified experimentally and included input protection diode failures, gate oxide punchthrough and metallization burnout. No tabulation was made as to the freqeuncy of occurrence of these failure modes.

The IC failure mode analysis on the "Electrical Overstress Screen Development" program consisted of a listing of the electrical parameters which failed, a pin-to-pin curve tracer analysis on selected devices, and microscopic analysis on selected devices. This study identified various failure modes for each devices type but did not determine frequency of occurrence.

In this program several integrated injection logic (I^2L) devices were tested. The I^2L devices consisted of inverters which were bonded out from a large array of I^2L gates. These units were fabricated using a conventional double diffused isolated I^2L structure as shown in Figure 40. The I^2L inverters were pulsed input to ground, output to ground, and injector to input. In the input stressed condition the failure mode, as determined from curve tracer measurements, was a junction short across the input-to-n epitaxial region. In the output stressed condition, the output collector base junction shorted. This junction consists of what would be the emitter and base diffusions of a conventional device. For the injector-to-input stressed condition the failure occurred at the same junction as for the input stressed condition. This is the emitter base junction of the vertical n-p-n transistor or the collector-base junction of the lateral p-n-p injector transistor. No failures were observed for the emitter-base junction of the injector.

25. INVESTIGATION OF "MAVERICK" DEVICES

In any hardness assurance program the objective is to develop the means to eliminate those devices of a specific device type and manufacturer whose radiation response is well below that of the nominal device. The preferable solution to the hardness assurance problem would

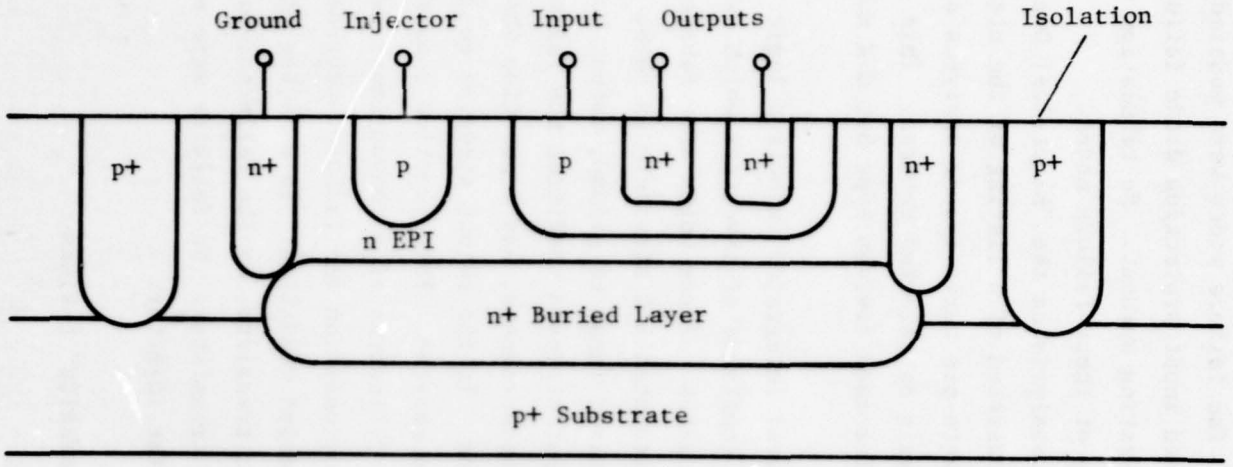


Figure 40. I^2L inverter.

be a device terminal electrical test which relates directly to the relative hardness of the part. In order to have a high confidence that the terminal electrical test will produce the desired results, there needs to be a firm theoretical foundation relating physical mechanisms of the radiation damage to the physical properties which determine the value of the electrical parameter. Very often, however, the process of establishing an electrical "screen" is worked totally on empirical grounds. This approach consists of monitoring various device electrical parameters and determining the correlation between the value (or in some cases rank within a group of samples) of the parameter and the failure level of the device in a particular environment. In order to have a high degree of confidence in the results of such an empirical approach, a very large number of devices must be tested to guarantee that a high correlation coefficient does not result from random processes.

In this investigation, data from all five of the programs listed in Table 5 were reviewed to identify devices whose pulse power failure or open circuit failure voltage was clearly outside a nominal distribution for that device type. For the data presented in the first three programs this consisted of reviewing plots of pulse power failure versus failure pulse width.

Since only two devices were tested at each pulse width the individual data points were compared to the curve fit using the relation $P_f = At^{-B}$. All power failure points which were a factor of ~3 or greater below the line were investigated. It should be pointed out that a test requirement in these programs was that the ratio of the pulse power failure to the pulse power of the highest no fail pulse be less than two. This criterion would allow for a factor of 2 experimental error difference in the data points at a single pulse width. This was taken into consideration by reviewing both the power failure level and highest no fail level for each potential "maverick."

Table 11 is a list of the devices which were labeled as possible mavericks and investigated for distinguishing characteristics. In the three programs which were surveyed to generate the list in Table 11 over 1200 devices were tested. A total of five mavericks were located from the test data; the worst case deviation from the norm was a factor of 5.

TABLE 11. List of potential "MAVERICKS."

Device Type	Test Cond.	Pulse Width and Polarity	Unit Number	Pulse Power Failure Level P_f (Watts)	Failure Time t_f (μsec)	Best Fit P_f (Watts) @ t_f	Ratio of best fit P_f to Actual P_f
N7400F	Input	+10 μs	4	13.7	2.3	49.1	3.6
912 HC	V_{CC}	+ 1 μs	83	63.6	0.4	312	4.9
945 HC	Output	- 1 μs	67	16.0	1.0	50	3.1
CD400AE	V_{DD}	+10 μs	21	94.3	0.5	347	3.7
μA 747	Test G	+ 1 μs	67	52.5	1	200	3.7

The investigation of these devices revealed the following results.

25.1 N7400 Unit 4

An examination of the pulse failure data showed that the maverick unit 4 survived a 10.4-watt pulse at 10 μs on pulse 9 before failing on pulse 10 at 13.7 watts, 2.3 μs. Unit 3 failed on the first pulse at 9.75 watts, 10 μs. The maverick appearance of unit 4 resulted from the manner in which the test data were plotted. The "failure" pulse width was determined by the time to failure on the failure pulse and did not take into consideration the previous step stress data. It can be realistically concluded that unit 4 was not a maverick.

25.2 912 HC Unit 83

The pulse power failure data on the RTL 912 half adder unit 83 was a factor of 3 below the failure power of unit 84, which was tested under the same conditions. In addition it failed early in the pulse (0.4 μs for a 1-μs pulse). The failure mode for unit 83 appeared to be a short from the V_{CC} line to output pin 7. This caused damage to the emitter-base junction of the output transistor Q7 shown in the circuit diagram of Figure 41. The Fairchild 5000 data showed that the output current high (test I_{A3}) dropped out of specification, changing from a value of -.47 mA to -.30 mA. This would result from a leaky E-B junction on Q7, as indicated by the curve tracer photos, which would draw current from the pin 7 output thus reducing I_{A3}.

The failure mode for unit 84 was a short of the collector-base junction of input transistor Q3, as verified by the photomicrograph of the chip. The Fairchild 5000 data indicated damage to Q5 and Q6 as well since the V_{SAT} test at pin 7 exceeded the specification limit and the current at pin 7 went up considerably for the off condition.

Other than the fact that the failure modes were different for units 83 and 84 the only distinguishing characteristic noted about the

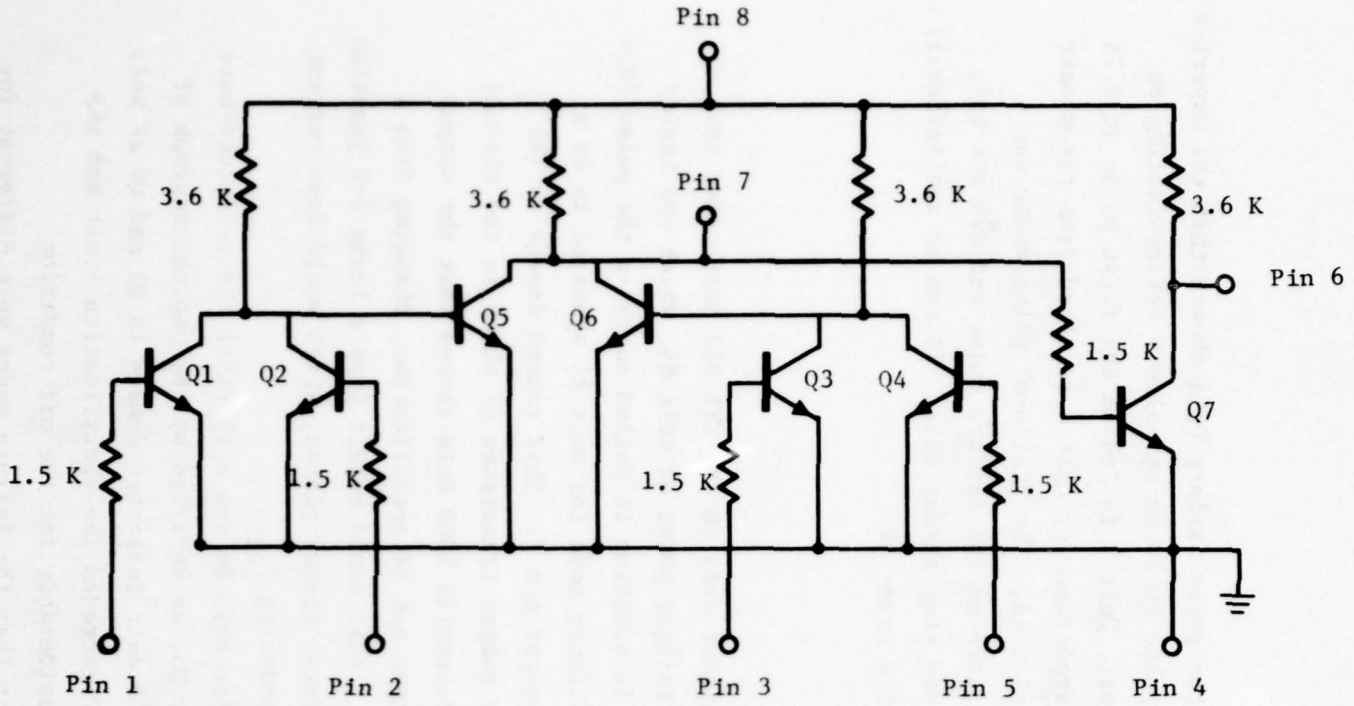


Figure 41. Circuit diagram of 912 HC.

maverick was the pretest values of V_{SAT} for both outputs (pins 6 and 7). The range of values of V_{SAT} for pin 6 for the other devices was 60 to 70 mV whereas unit 83 read 100 mV. The range of V_{SAT} readings on pin 7 was typically 110 to 120 mV but read 180 mV for unit 83. This would indicate that either the resistor values on unit 83 were significantly different, causing a higher forced gain condition, or that the gain of the output transistors were substantially less than the nominal value. If the gains were much lower, there remains the question of correlation to overstress failure level. No verified correlation has been established between preirradiation gain or saturation voltage and overstress failure level. Therefore, the connection between the high V_{SAT} values on unit 83 and the low pulse power failure level may be circumstantial.

25.3 945 HC Unit 67

The 945 HC RS flip flop unit 67 was subjected to negative 1-μs pulses at the Q output terminal (pin 4) and failed on the fourth pulse at 16 watts. Unit 79, tested under the same conditions, failed on the sixth pulse at 55.5 watts. The failure parameter for unit 67 was V_{OH} on pin 4 whereas unit 79 failed V_{OL} on pin 4. The failure mode for unit 64 appears to be a junction short C-B on the output transistor. This supposition is supported by the curve tracer photo which shows a direct low resistive path from output to ground. The failure mode for unit 79 could not be determined. Neither of the devices was available for microscopic analysis. The only distinguishing characteristic of unit 67 was a high pretest value of leakage current at pin 7 (S_D). This would have no bearing on failure at the output. No conclusion could be drawn as to why unit 67 had a low pulse power failure level compared to the "nominal" value.

25.4 CD 4000 AE Unit 21

The CD 4000AE unit 21 turned out to be in the same category as the N7400F maverick. Unit 21 failed at 94.3 watts at 0.5 μs for a 10-μs

pulse. It did not fail at 77.3 watts for a full 10-μs pulse, whereas unit 20 failed at 82.1 watts at 4.7 μs for a 10-μs pulse and the same test condition. It can be concluded that unit 21 was not a maverick and only appeared to be one because of the nature of the data analysis.

25.5 μA747 Unit 67

The μA747 dual op amp unit 67 failed on the first pulse at 52.5 watts for a positive 1-μs pulse into both inputs with the power supplies and output grounded. The only data which could be found on this device were pretest Fairchild 5000 data and pre- and posttest curve tracer data. No photomicrographs were taken and the device could not be located for microscopic analysis. From the curve tracer photos the failure mode appears to be the same for unit 67 as for other devices tested under the same conditions, namely a junction short on the E-B junction of a p-n-p transistor between the inputs and V_{CC} positive terminal.

Four other units were tested under the same conditions. These devices had pulse power failure levels of 124, 148, 315, and 340 watts, a rather large spread. However, no distinguishing characteristics could be found to explain the low failure level of unit 67.

25.6 Other Maverick Identification

The data taken on the E-4 and electrical overstress screen development programs were taken in terms of open circuit failure voltage. Histograms of the number of failures versus the failure voltage were plotted. All of the histograms were reviewed to identify devices clearly outside the distribution.

Only two device types (one from each program) met the criterion. The MC846, tested on the E-4 program and reported in reference 17, had two units which had an open failure voltage will below the mean for the 44-μs input test condition. The histogram for the distribution which totaled 50 samples is given in Figure 42. The failure mode for the two low voltage failures was the same as for the other devices, a junction short on the input diode.

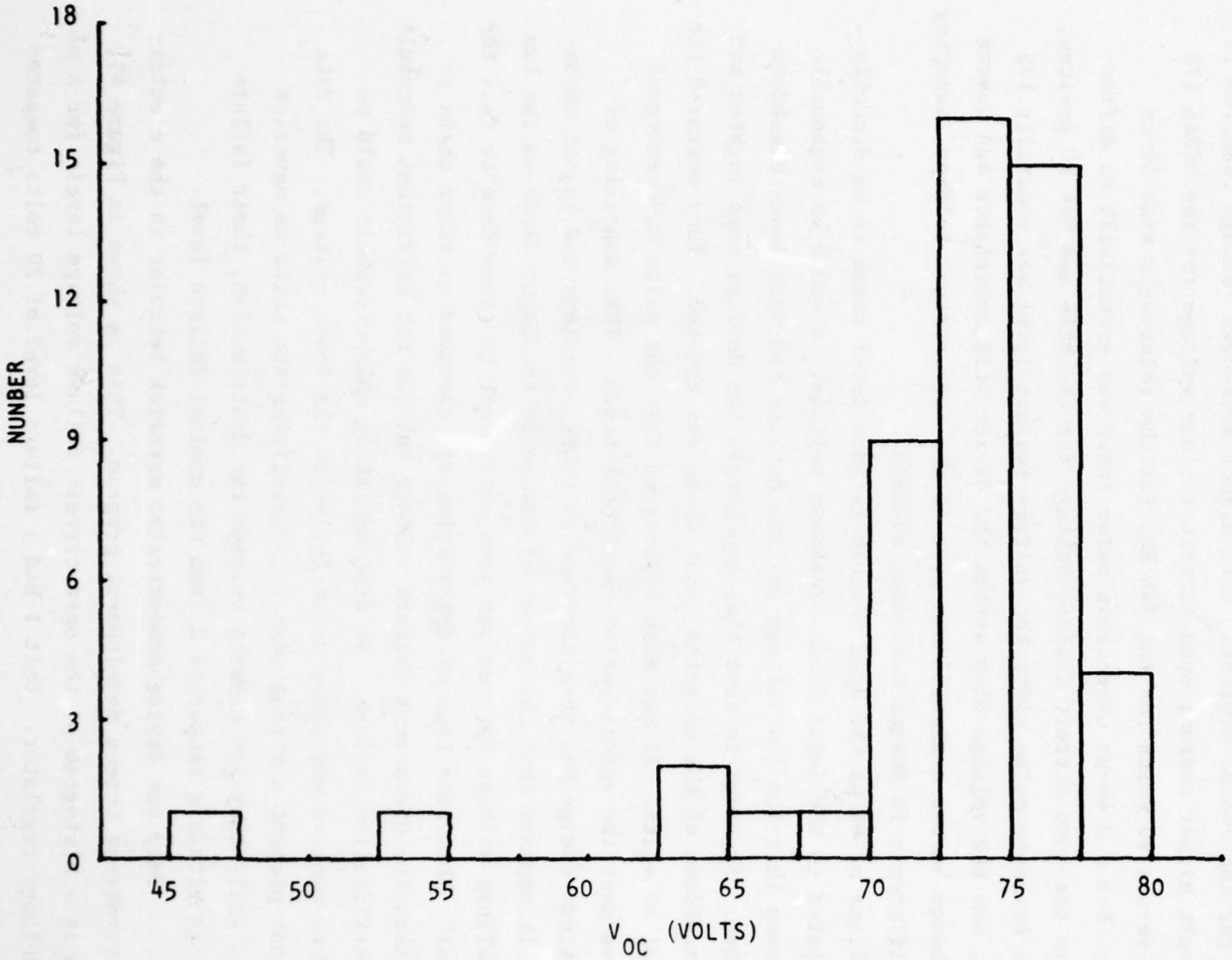


Figure 42. MC846 Input failure voltage histogram, 44-μsec pulse.

As discussed in reference 17, the breakdown voltage for the input diode of the MC846 devices was nominally 40 volts compared to 10 volts for the 946 HC devices. This higher breakdown voltage resulted in a 30-volt higher nominal open circuit failure voltage for the MC846 (70 volts versus 40 volts for the 946 HC) for the relatively wide 44-μs pulse. For a 0.44-μs overstress pulse there was essentially no difference in the open circuit failure voltage for the M846 and 946 HC devices. At the narrower pulse width the voltage failure level was nominally 175 volts, and the voltage drop across the device bulk resistance and source resistance became a significant part of the open circuit voltage, swamping the difference in device breakdown voltage.

Since at 44 μs the open circuit failure level seems to be directly correlated to the input diode breakdown voltage, it would be reasonable to assume that the low voltage failure devices had much lower breakdown voltages. In order to test this hypothesis the devices were located and the breakdown of the untested input diode was checked. They measured the nominal 40 volts. It was also discovered that the units had recovered and now meet the specification electrical tests. This annealing of overstress damage has been observed on other occasions and is not uncommon. It appears that the amount of damage to the input diode on the two low-failure voltage devices was just sufficient to cause them to fail the I_R test. This same type of degradation was observed on other units at less than the overstress failure voltage but was not sufficient to result in specification failure. No distinguishing characteristic could be found to explain why these units failed at the lower voltage. The data does not present a strong case for classifying the units as maverick since, while they are clearly outside the distribution, their failure level is within a factor of 2 from the nominal failure level.

Only one device demonstrated maverick behavior in the electrical overstress screen development program. This is shown in Figure 43, which is a histogram of the open circuit failure voltage levels for a μA 723 voltage regulator. Unit 1 had a failure level of 20 volts compared to a nominal 50 volts.

Unit 1 failed due to metallization burnout which showed up on the curve tracer as an open circuit between the two inputs. All other devices showed junction shorts on the reverse biased stressed emitter-base junction of the input transistor. This device would appear to be a true maverick, having a unique failure mode at a voltage level well below the nominal value. Microscopic inspection of the device revealed that the burnout occurred in one of the input leads (connected to the base of the input transistor) over an oxide step. It is reasonable to assume that this was due to thinning of the metal over the step resulting in a very high current density at that point.

26. CONCLUSIONS

An analysis of electrical overstress data on integrated circuits from five programs has been reviewed to determine failure modes for different categories of ICs and to investigate "maverick" failures to identify distinguishing characteristics.

The following general conclusions can be drawn from this analysis concerning failure modes:

a. For DTL circuits the predominant failure mode for the input stressed condition is input diode junction failure (90 percent). For the output stressed condition junction damage to the output transistor was the major failure mode (81 percent).

b. For RTL circuits the predominant input failure mode was junction damage on the input transistor. However in several cases (26 percent) an input transistor adjacent to the stressed input was damaged due to a short from the stressed input resistor to the base side of an adjacent input resistor causing a low resistance path to the adjacent input. This failure mode could easily be eliminated by a mask change. For the output stressed condition, failure was caused by either a short in the output transistor (67 percent) or degraded gain of the output transistor (33 percent).

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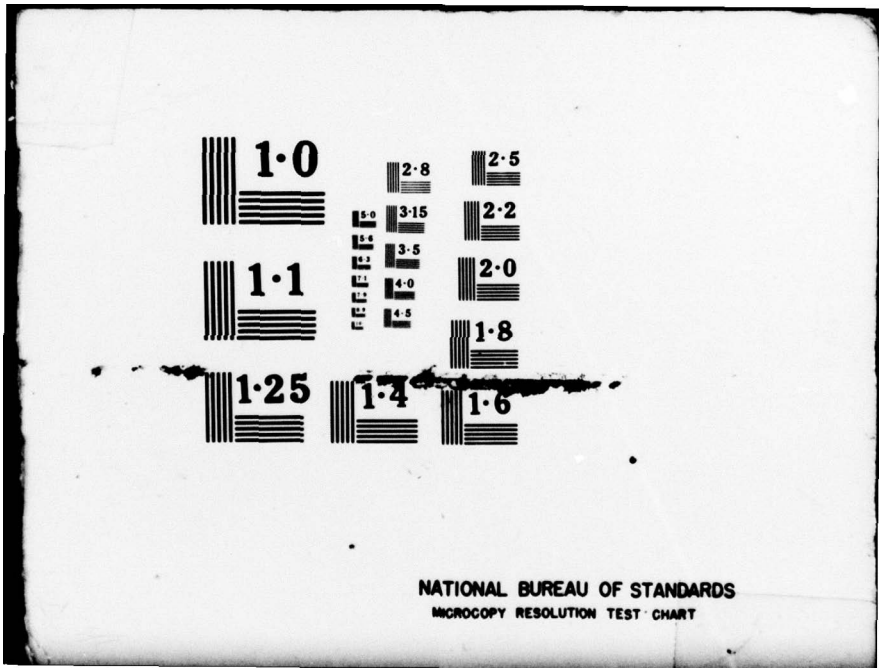
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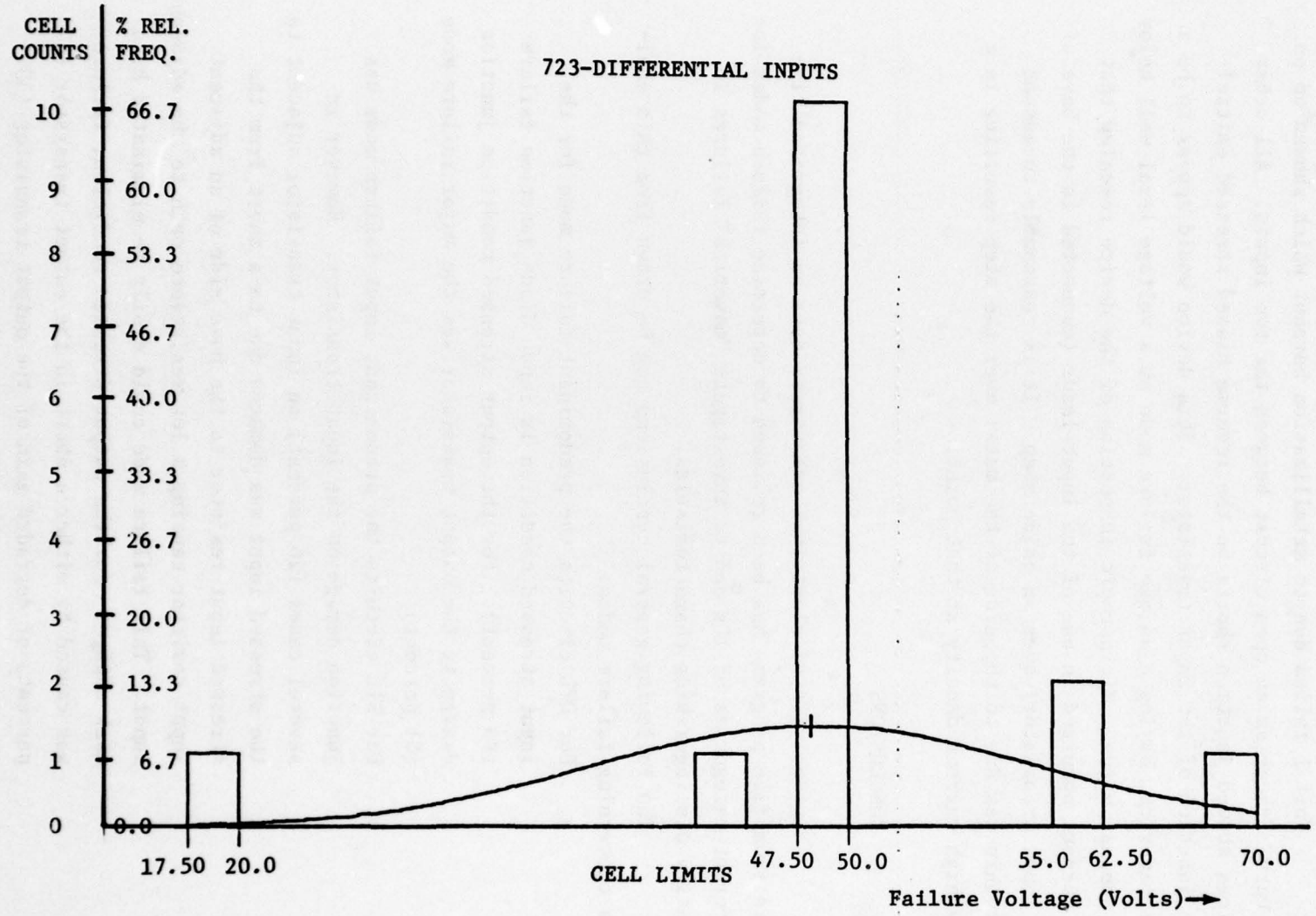

Figure 43. Histogram of failure voltages for μA723

c. The predominant failure mode for TTL circuits with stressed input was junction damage to the input clamp diode (69 percent), whereas for the output condition 83 percent of the failures were due to junction damage on the output transistor.

d. For ECL devices the predominant failure mode on the input was junction failure of the input transistor (72 percent); for the output stressed condition, the output transistor was damaged in 60 percent of the devices.

e. For the input stressed condition on linear devices the major failure mode was input transistor junction damage (67 percent), whereas there was no clearly distinguishable predominant failure mode for stressed output. The output transistor was involved in 32 percent of the failures and metallization burnout accounted for 20 percent. The other 48 percent involved several additional failure modes.

f. In MOS devices the major failure mode was device type dependent, generally being a function of the input protection network for the input stressed condition. A high incident of metallization burnout was observed on some circuits while oxide punchthrough or junction failure of the input diodes or resistors was observed on other devices.

g. For the VCC stressed condition on all types of ICs, the pulse power failure levels were much higher than for the input or output stressed conditions, and the failure modes often involved multiple junction burnout, failure of internal transistors, and metallization burnout.

h. In relatively few instances the failure mode appeared to be a change in resistor value of the diffused resistors. This was inferred from failure to meet the power supply current test with little change in other electrical parameters. No microscopic validation of this mode was obtained.

The investigation of maverick behavior did not yield any insight into what caused the low pulse power failures. The criterion used to

identify mavericks in three of the five programs investigated (nominal P_f divided by device P_f greater than three) only yielded five devices in over 1200 tested. Of these five devices, two appeared to be mavericks because of the manner in which the data was presented. Of the three remaining devices no distinguishing characteristics in the pretest measurements or failure modes could be found which related to the observed failure levels. In the other two programs, representing over 2000 test devices, only two incidents of maverick behavior were identified. In one case, involving two devices well outside the nominal distribution (but only having a failure voltage level a factor of 2 below the norm), the failure mode was the same as others in the test lot. These devices, when analyzed for any distinguishing characteristics, were found to have annealed and no longer failed the specification test requirements.

The other case yielded what is probably true maverick behavior. A μA 723 voltage regulator which had a failure voltage a factor of 2.5 below the norm displayed a unique failure mode for the lot. The input metallization lead burned out over an oxide step on this unit, whereas all other devices failed from input transistor emitter-base junction damage. No terminal electrical pretest measurement would have identified this failure mode.

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