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A BREADBOARD MODEL USED TO DEMONSTRATE THE FEASIBILITY OF RECORDING NATIONAL AIRSPACE SYSTEM ENROUTE DISPLAY DATA

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DDC

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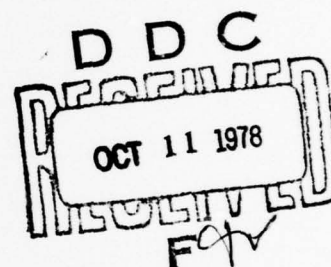
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SEPTEMBER 1978

FINAL REPORT

Prepared for

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16. Abstract

A feasibility investigation was made of various techniques for providing the capability of re-creating or replaying on demand air traffic histories for operational or incident analysis. To demonstrate feasibility, the best technique was selected and a single-thread breadboard model designed and fabricated. It was concluded that the single-channel breadboard model, employing the digital recording technique and utilizing the Display Control Vector Generator input area as the data recording point, adequately demonstrated the feasibility of recording, storing, and reproducing NAS en route air traffic control display data. Based upon this successful demonstration, it was recommended that a full-scale multiple-channel engineering model be designed, fabricated, and evaluated.

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METRIC CONVERSION FACTORS

Approximate Conversions to Metric Measures

Symbol	When You Know	Multiply by	To Find	Symbol
		LENGTH		
in	inches	*2.5	centimeters	cm
ft	feet	30	centimeters	cm
yd	yards	0.9	meters	m
mi	miles	1.6	kilometers	km
		AREA		
in²	square inches	6.5	square centimeters	cm²
ft²	square feet	0.09	square meters	m²
yd²	square yards	0.8	square meters	m²
mi²	square miles	2.6	square kilometers	km²
	acres	0.4	hectares	ha
		MASS (weight)		
oz	ounces	28	grams	g
lb	pounds	0.45	kilograms	kg
	short tons (2000 lb)	0.9	tonnes	t
		VOLUME		
tsp	teaspoons	5	milliliters	ml
Tbsp	tablespoons	15	milliliters	ml
fl oz	fluid ounces	30	milliliters	ml
c	cups	0.24	liters	l
pt	pints	0.47	liters	l
qt	quarts	0.95	liters	l
gal	gallons	3.8	liters	l
ft³	cubic feet	0.03	cubic meters	m³
yd³	cubic yards	0.76	cubic meters	m³
		TEMPERATURE (exact)		
°F	Fahrenheit temperature	5/9 (after subtracting 32)	Celsius temperature	°C

*1 in = 2.54 (exactly). For other exact conversions and more detailed tables, see NBS Misc. Publ. 286, Units of Weights and Measures, Price $2.25, SD Catalog No. C13.10:286.

Approximate Conversions from Metric Measures

Symbol	When You Know	Multiply by	To Find	Symbol
		LENGTH		
mm	millimeters	0.04	inches	in
cm	centimeters	0.4	inches	in
m	meters	3.3	feet	ft
m	meters	1.1	yards	yd
km	kilometers	0.6	miles	mi
		AREA		
cm²	square centimeters	0.16	square inches	in²
m²	square meters	1.2	square yards	yd²
km²	square kilometers	0.4	square miles	mi²
ha	hectares (10,000 m²)	2.5	acres	
		MASS (weight)		
g	grams	0.035	ounces	oz
kg	kilograms	2.2	pounds	lb
t	tonnes (1000 kg)	1.1	short tons	
		VOLUME		
ml	milliliters	0.03	fluid ounces	fl oz
l	liters	2.1	pints	pt
l	liters	1.06	quarts	qt
l	liters	0.26	gallons	gal
m³	cubic meters	35	cubic feet	ft³
m³	cubic meters	1.3	cubic yards	yd³
		TEMPERATURE (exact)		
°C	Celsius temperature	9/5 (then add 32)	Fahrenheit temperature	°F

Temperature scale:

°F -40   32 98.6 212
°C -40 -20 0   20 37 40   60   80   100

PREFACE

The following personnel have contributed significantly to the success of this project in the following areas:

Fabrication

Samuel Faktor, ANA-140
Nandor Dressnandt, Co-op student
Dave Henry, Co-op student
Al Rovner, Co-op student
Steve Sharp, Co-op student
Thomas Vanderpool, Co-op student
Joel Young, Co-op student

Testing and Demonstrations

Gerard Chiasson, ANA-110
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INTRODUCTION

PURPOSE.

The Federal Aviation Administration (FAA) has a need to re-create or replay on demand air traffic histories for operational or incident analysis. As a step toward satisfying this need, a feasibility investigation was made into various techniques and methods to record, store, and reproduce FAA en route air traffic control display data. To support this investigation, a bread-board model was designed and tested at the National Aviation Facilities Experimental Center (NAFEC), Atlantic City, New Jersey.

BACKGROUND.

In 1975, Air Traffic Service (ATS) requested Systems Research and Development Service (SRDS) to determine the feasibility of recording air traffic control display data. A task was assigned to the Air Traffic Systems Division at NAFEC to survey government and industry to determine the present state-of-the-art in display recording and recommend possible alternatives. As a result of the survey and review of the possible alternatives, NAFEC was tasked by SRDS to design and build a breadboard model using digital tech-niques. The effort was directed toward the National Airspace System (NAS) Stage A En Route System.

DISCUSSION

FEASIBILITY INVESTIGATION.

INITIAL STUDY. The initial study was divided into two study areas; a government/industry search for similar efforts and an in-house study of the type of data to be recorded.

First, to avoid repeating work that might have already been done, a search of other government agencies and industrial firms was undertaken for similar efforts that could be applicable to FAA equipment. Within the United States (U.S.) Government, the National Aeronautics and Space Administration (NASA)/ Goddard and the U.S. Navy/Johnsville were contacted. Both have used digital approaches in recording their displays, but their techniques were not directly applicable to the FAA effort. A vast amount of recording is done by the U.S. Government intelligence-gathering agencies, but this work is classified and not available. Of the electronic systems and minicomputer manufacturers, Raytheon, Hughes, Plessey, Varian, Lockheed, Bendix, and Westinghouse were contacted. These companies offered various systems. Hughes proposed a digital recording system to the Navy for shipboard displays. Westinghouse mentioned a television (TV) scan system for recording Coast Guard harbor radar data. Plessey and Varian indicated that a minicomputer or microprocessor could act as a digital controller/buffer for recording the data digitally. Conversations were conducted with several recorder manufacturers to obtain an adequate pic-ture of the state-of-the-art in both fixed-head instrumentation recorders and

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rotary-head video recorders. These firms were Ampex, Bell and Howell, Echo Science, American Videonetics, Emerson Electric, Honeywell, and Sangamo/Weston.

The second study area was concerned with the data types and signal paths within the Radar Display Subsystem (RDS) to gain a working-level background. To accomplish this, numerous technical conferences were held with Raytheon/NAFEC and AAF-640 personnel.

Information from the two investigations was combined to determine if the signal types present in the RDS could be recorded on any of the currently available recorders. A detailed analysis of the various data points within the subsystem that were considered as recording points will be discussed later.

SYSTEM DESIGN CONSTRAINTS. As a result of coordination with ATS and SRDS, a number of technical guidelines were developed for any system that would be used to record the en route plan view display (PVD) presentation. They were as follows:

1.   All information within the PVD tube diameter shall be recorded, including the blinking conflict alert and handoff data blocks.

2.   There shall be no additional software workload placed on the display computer, and a minimum of add-on hardware.

3.   The data recording point shall be after all software processing of the PVD data has been completed.

4.   No software shall be used in any record or playback "black boxes" by which the data integrity can be compromised.

5.   Playback shall be on a standard PVD to re-create, as closely as possible, the original viewing environment.

6.   The recording device shall run for a minimum of 4 hours unattended.

DATA RECORDING POINTS. Figure 1 shows a simplified block diagram of the display subsystem and the various data points that were investigated to accomplish this data recording. The Radar Keyboard Multiplexer data were not considered for recording in this investigation.

Data Point A--TV Technique. It is desirable to record the data as close to the PVD surface as is feasible. The first method considered was the use of a television (TV) system, which would view the display cathode-ray tube (CRT) surface either from the front of the PVD or through an optical window in the rear of the CRT. (See point A in figure 1.) An advantage in using this technique is that it would be capable of recording display data even when the display subsystem is operating in its backup scan conversion mode. However, this would cease to be an advantage when the present backup system is replaced by

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the Direct Access Radar Channel (DARC). An obvious problem with this technique is the possible blockage of the TV camera's viewing area by the controller if the system views the data from the front of the PVD. Although a rear-port viewing of the ATC pattern would eliminate this situation, this would require redesign of the PVD.
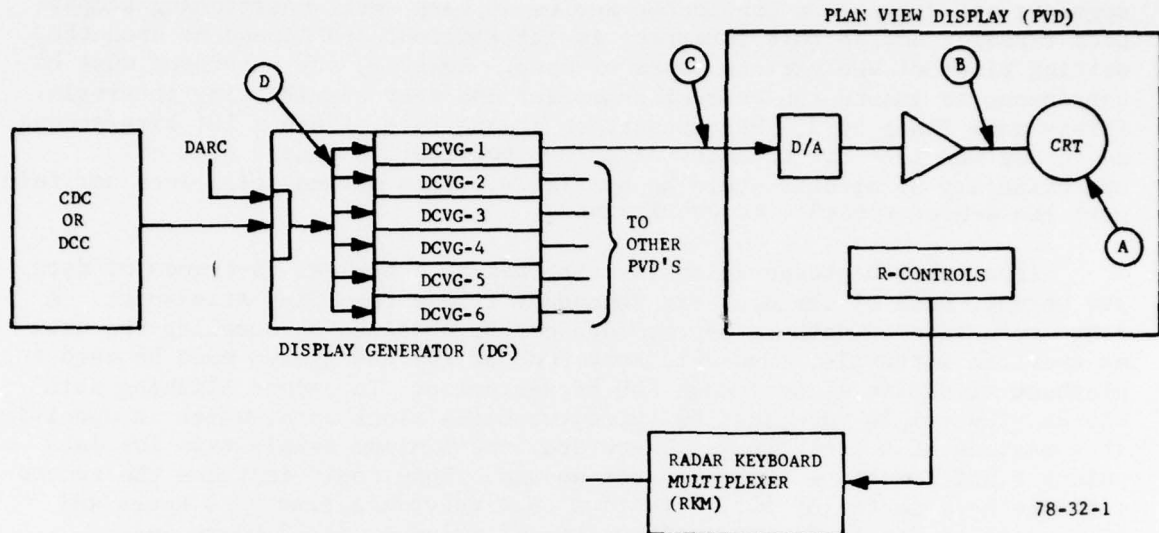

FIGURE 1.   RADAR DISPLAY SUBSYSTEM (RDS)

Some basic tests were performed using a high-resolution 945-line TV camera borrowed from a BRITE-4 display system. Two PVD's were used; one was operating normally with various test patterns, the other was used as a TV monitor. The TV camera viewed the test pattern presentation on the first PVD, and the resolution on the second PVD was compared to the original. It was found that the high-resolution 945-line TV system could not provide sufficient resolution for differentiating between several types of 1/8-inch characters, i.e., an "8" and a "B," a "5" and an "S," a "D " and an "O," etc. The use of higher resolution TV scan rate (greater than 945-line) would mean the data could not be reproduced on a standard PVD. The resulting higher bandwidth would also present recording difficulties.

Data Point B--Analog Technique. The next point taken under consideration was data point B in figure 1. This point contains the X and Y deflection signals driving the CRT yoke, each having a 3.5-megahertz (MHz) bandwidth. The unblanking or Z-axis signal, which also must be recorded, has a 12.5-MHz bandwidth. Combining the three signals for recording using a frequency division multiplex technique will result in a signal whose minimum bandwidth is 19.5 MHz which is beyond the range of currently available video recorders.

Digitizing the three analog signals and recording the result on a high-density digital (HDD) recorder was considered. The minimum Nyquist sampling rate utilizing this technique would have been 40 MHz, and with the total bit capacity of an HDD recorder being 10^{11} bits, the record time would be approximately 40 minutes, which is considerably less than the 4-hour design constraint. This digitizing technique would also be impractical, since the analog data at point B were derived from the digital PVD input.

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Data Point C--Digital Technique. The PVD is controlled by the signals
sent to it by the Display Control/Vector Generator (DCVG). The digital input
to the PVD, point C, is a 30-line parallel bus operating at a 3.3-MHz clock
rate. This interface is quite active; for example, vectors or straight-line
segments are drawn as a continuous series of very small positioning steps.
Data transfer across this interface is intermittent and dependent upon the
writing times of the various types of data. However, any recording must be
continuous to insure the correct character and vector write time intervals.
Thirty data lines at 3.3 MHz convert to a data rate of 6.6×10^7 bits/second,
and using the 10^{11} bit capacity of an HDD recorder, a record time of
approximately 25 minutes would be available. This method still does not ful-
fill the 4-hour record time constraint.

Since the PVD presentation is refreshed at a nominal 55-frames of data
per second, much of the data are redundant from a recording standpoint. A
large reduction in data to be recorded can be obtained by sampling the data
at specific intervals. However, some type of refresh system must be used on
playback to obtain a continuous PVD presentation. To record blinking data
blocks, the sample rate must be twice the blink clock rate, which is specified
at a maximum of 5 hertz (Hz). Therefore, the minimum sample rate for data
points B and C must be 10 frames per second. This could increase the record-
ing time by a factor of 5.5, resulting in a recording time of 3 hours and
40 minutes by digitizing the analog data at point B, and 2 hours and
17 minutes at point C, still below the required 4-hour record time.

Data Point D--Digital Technique. The last point to be investigated
before software control becomes involved in the data flow is the DCVG input
(point D in figure 1). This interface contains the display data being trans-
ferred to the DCVG's from either the Refresh Memory (RM) in the Computer
Display Channel (CDC) or a display element in the Display Channel Complex (DCC).
This 16-line bus is a common input to the six DCVG's in a display generator
(DG). Control lines select the proper DCVG for the particular data on the bus.
Data are transferred to each DCVG at 4.4 MHz in groups or banks of one to four
64-bit words in each access time (16 bits per byte, 4 bytes per word). Each
word is an instruction to execute vectors or generate alphanumerics. Access
time for each DCVG occurs every 10.8 microseconds (μs) or multiples thereof.
If, at access time, the DCVG is still busy executing its last series of
instructions, it will not use that access time to request additional data.
Assuming a DCVG uses each access time, it will receive a maximum of 1,680
64-bit words in a normal 18.2-millisecond (ms) refresh cycle. Sampling one
refresh cycle each second results in an equivalent data rate for recording
of 2.5×10^5 bits per second. Again using the 10^{11} bit capacity of an HDD
recorder, there are approximately 257 recording hours available. This
translates to recording 64 PVD's for 4 hours; this is a maximum figure and
will be somewhat less in actual practice. In this technique, blink informa-
tion is available as an inherent part of the data, and therefore sampling at
twice the maximum blink rate is not necessary.

Another advantage to using point D for data recording is that it is after
the DARC enters the RDS. This means that when the DARC system is being
utilized, data will continue to be recorded.

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Selected Data Point. It was decided the DCVG input (point D) was the point with the most concentrated data meeting all the design constraints. The breadboard model described in the following paragraphs was built and tested to demonstrate that a PVD recording system is feasible and practical using data taken from the DCVG input.

BREADBOARD MODEL.

The breadboard model, known as the NAFEC Display Recording System (NADIRS), is shown within the dotted lines in figure 2 and utilizes the refresh sampling technique as discussed above. Due to the high data rate at the DCVG input, the HDD recorder cannot directly record a single refresh frame each second, so the frame is temporarily stored in the Record Interface Buffer (RIB). The RIB then sends the frame data at a slower rate to the recorder. Playback is accomplished using a Playback/Refresh Alternating Memory (P/RAM) and a standard unmodified NAS en route DCVG and PVD. The P/RAM stores each frame as it comes off the tape and refreshes the PVD to provide a smooth playback presentation of the display information. All the logic is transistor-transistor logic (TTL) unless otherwise stated.

A 1-second sample rate was determined to be adequate, since the 9020 Central Computer Complex updates the data base in the display computer nominally every second and the radar inputs to the NAS en route system only provide new target position data every 6 to 10 seconds.
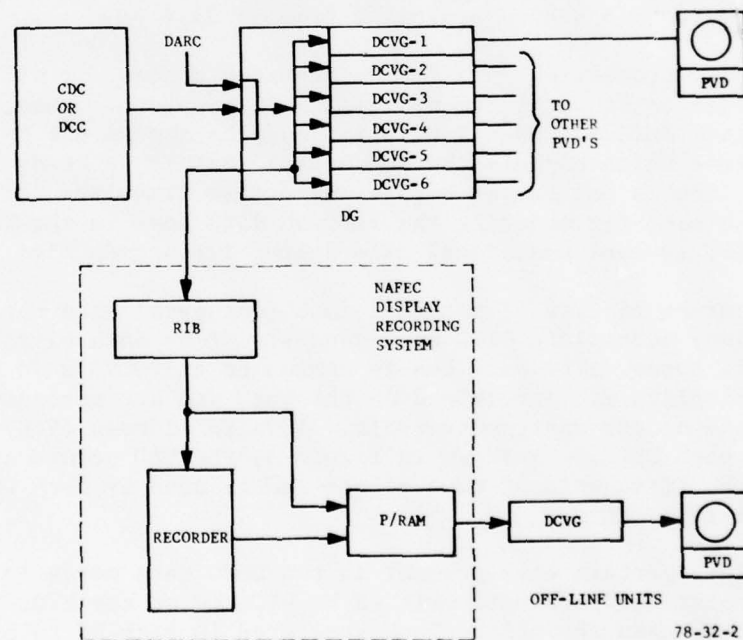


FIGURE 2. NAFEC BREADBOARD SYSTEM

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DATA BUS. This section covers, in more detail, the DCVG input bus discussed earlier. It is at this point that the data are sampled for recording, and it is the point the P/RAM simulates to provide data on playback to an offline DCVG and PVD.

The refresh subsystem refreshes each PVD at a maximum rate of 55 Hz. This rate allows the refresh subsystem approximately 18.2 ms (one refresh cycle) to display a complete frame of data on the PVD. The actual time taken to display a complete frame of data shall be defined as a refresh period. This period is variable, depending upon the amount of data being displayed. If the refresh period is less than 18.2 ms, then the refresh subsystem is able to display the frame 55 times each second. This is the synchronous refresh mode. If the refresh period is longer than 18.2 ms, then the refresh subsystem must use an extended refresh cycle to display the frame. Consequently, the refresh rate depends upon the amount by which the refresh cycle is extended. In this situation, the display is said to be in the asynchronous refresh mode. The refresh subsystem can refresh each display independently in either mode. In the refresh subsystem, access to the RM, which is controlled by the Refresh Memory Input/Output Control (RMIOC), is time shared between the display computer and the displays in the system. Each is given access to the RM according to the access assignment table. This table allows a DCVG to obtain data from the RM at a maximum rate of one word every 10.8 μs. Each DCVG can receive up to four 64-bit words each time it accesses the RM. The number of words or words-per-bank (W/B) depends on the number and configuration of RM modules. The time between accesses increases 10.8 μs for each W/B increase; i.e., two W/B's have a minimum time of 21.6 μs.

If a DCVG is busy processing data from a previous access, it will skip all accesses assigned to it until the processing is complete. Then, it will use its next assigned access. When a DCVG is ready to access the RM, it raises a DCVG request line which signals the RM control that it is ready to accept data. If the line is not raised before the access time, the RMIOC will use the access time slot for updating the refresh data base in the RM. If it is raised, the DCVG is sent additional data during its access time.

The RMIOC transfers 16 bits of parallel data (one byte) at a rate of 4.444 MHz. Since a complete DCVG word consists of 64 data bits, each word has four 16-bit bytes. The data bus is common to all DCVG's in a DG. The data for six displays are intermixed on the bus, and are arranged in order according to the access assignment table. A Valid Address (VAD) is generated by the DG for each DCVG. As shown in figure 3, the VAD occurs at the first byte time of the first word of each access and is used by each DCVG to detect the data it is to receive.

The DCVG examines certain bits present in the DCVG data words to determine if a specific piece of information is to be blinked on the PVD. If the bits are set, the DCVG uses the blink clock generated in each DG to blink that data on the PVD. The blink clock is adjustable between 0.25 and 2.5 Hz, and is independent of the other DG's.

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FIGURE 3. DCVG INTERFACE TIMING--TWO WORDS PER BANK TRANSFER
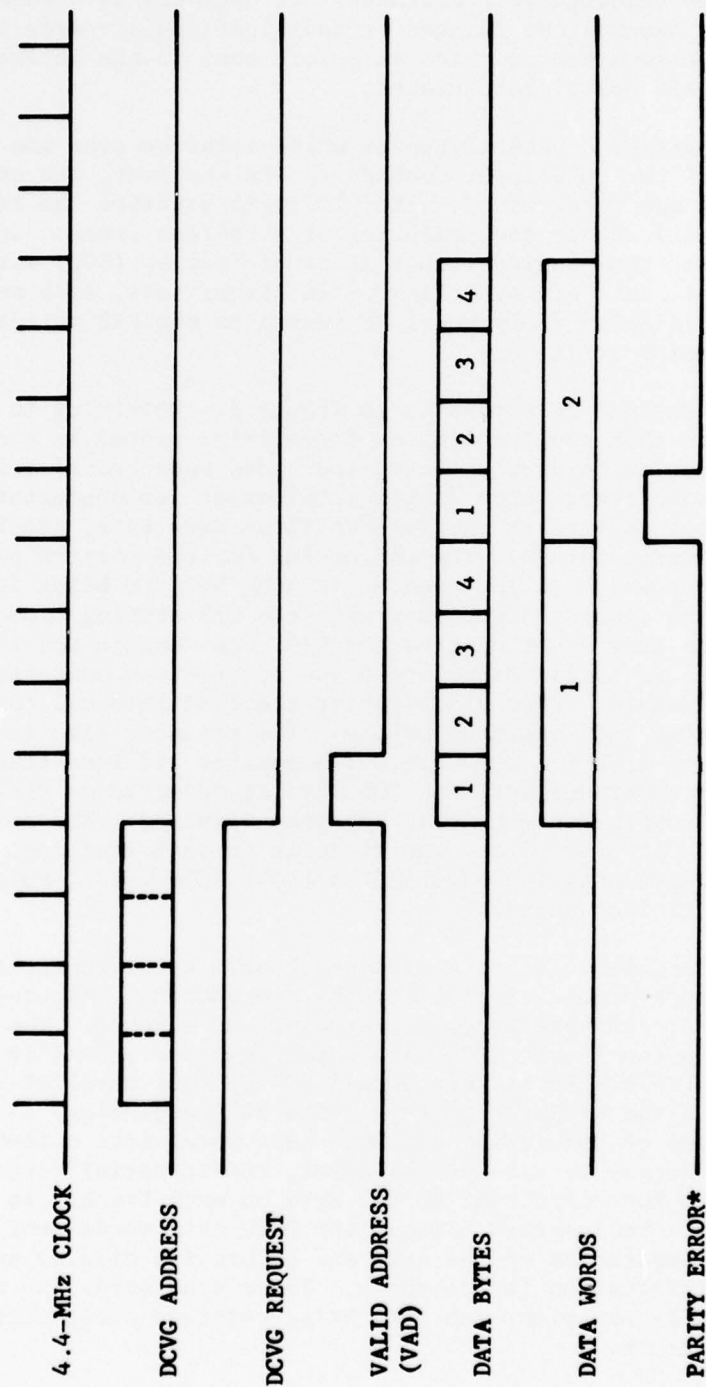
* IF WORD 1 HAS A PARITY ERROR

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RECORD INTERFACE BUFFER (RIB). The RIB is a digital device used to slow down the particular frame selected for recording. It operates as a sequential first-in, first-out memory. No changes or modifications are made to the refresh frame or the sequence in which data were sent to the active DCVG/PVD. Figure 4 shows the RIB and pickoff header.

The RIB input consists of a pickoff header which attaches over the wire-wrap posts on the back of the DCVG input connector. In this way, the normal operation of the DCVG is not interrupted. The RIB logic monitors the incoming data for words which indicate the beginning of a refresh frame. In the DCC system, each refresh frame begins with a start-of-display (SOD) word. In the CDC system, trackball data are sent first. In either case, each refresh cycle ends with an end-of-display (EOD) word. A switch on the RIB selects which display subsystem is being utilized.

A block diagram of the RIB is presented in figure 5. Referring to this diagram, it can be seen that the incoming data are first stored in a small 16-byte scratch pad memory which holds the one-to-four word bank transfer each access cycle. Since the main memory uses static metal-oxide semiconductor (MOS) technology and cannot operate at the 4.4-MHz input data rate, the TTL scratch pad acts as a temporary storage. The addressing for the scratch pad is provided by a counter which is incremented as each byte is being loaded. A comparator checks the counter's contents with the W/B setting from the display subsystem. When the byte count matches the W/B, the scratch pad is full, and a transfer operation is initiated to store the scratch pad contents in the main memory. The transfer takes place during the time interval that the RMIOC bus is servicing the remaining DCVG's. The transfer rate is 900 nanoseconds (ns) per byte or a 1.1-MHz rate. The scratch pad load-transfer operation to main memory continues until an EOD word is detected on the input bus, indicating that an entire refresh frame has been acquired. The main memory has a capacity of 2,048 DCVG words, and since it is estimated that an average air traffic control presentation uses 600 to 1,000 DCVG words, this was considered to be a sufficient capacity.

Recording 16-line parallel data on a standard 28-track instrumentation recorder is poor track utilization; 12 tracks are unused. Therefore, various other track and data configurations were studied and weighed. The result was a technique in which the 64-bit DCVG data words that are stored in the RIB main memory as four 16-bit bytes, are turned 90° by four parallel-in, serial-out registers called the output registers. The 90° terminology is used to designate the process of converting the DCVG data words from a 16-bit parallel, 4-byte serial format to a 4-byte parallel, 16-bit serial format. Thus, data are recorded on four tape tracks; one byte on each track. In addition, a 16-bit sync word will be inserted between the DCVG data words sent to the recorder to enable separation of the data and to provide display address information and parity information for playback. These sync words are organized into four, four-bit bytes, with each byte being recorded along with a data byte on a separate track.

As shown in figure 6, RIB output data lines 1 and 4 contain the sync pattern 0111, while line 2 contains a parity bit for each byte of the preceding data
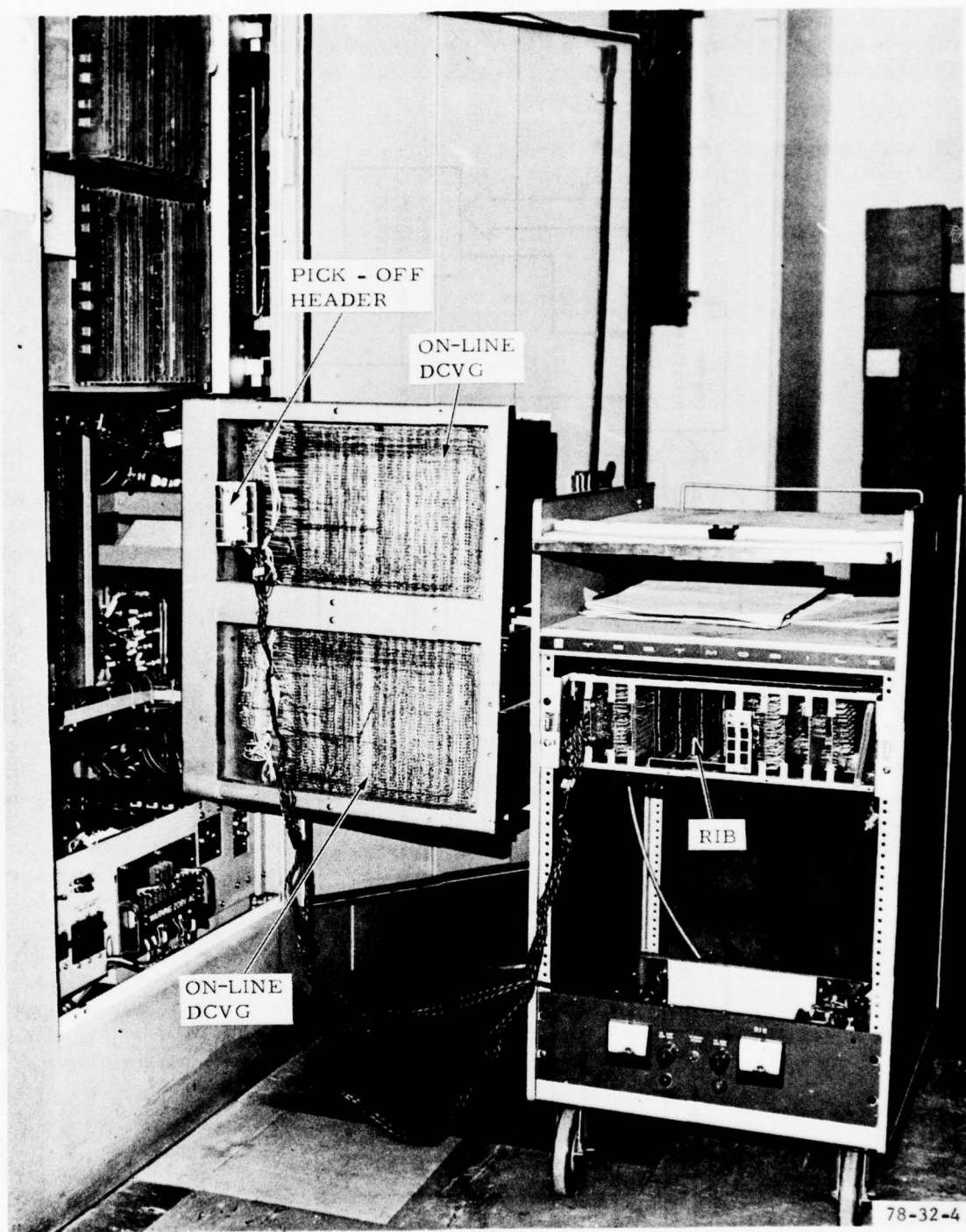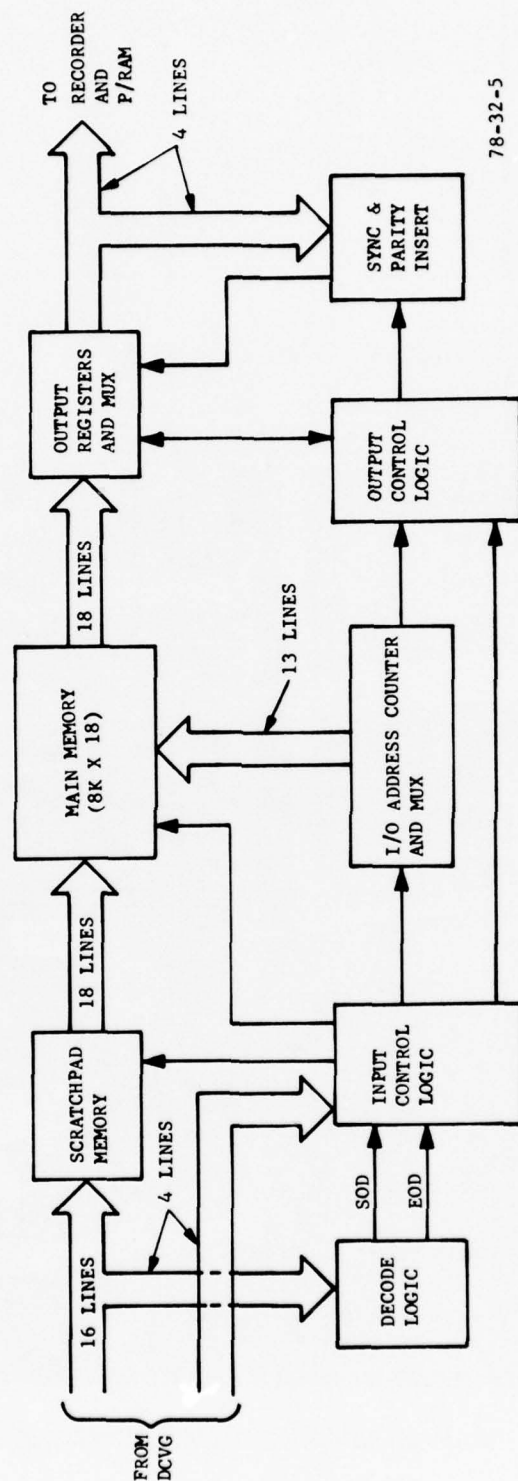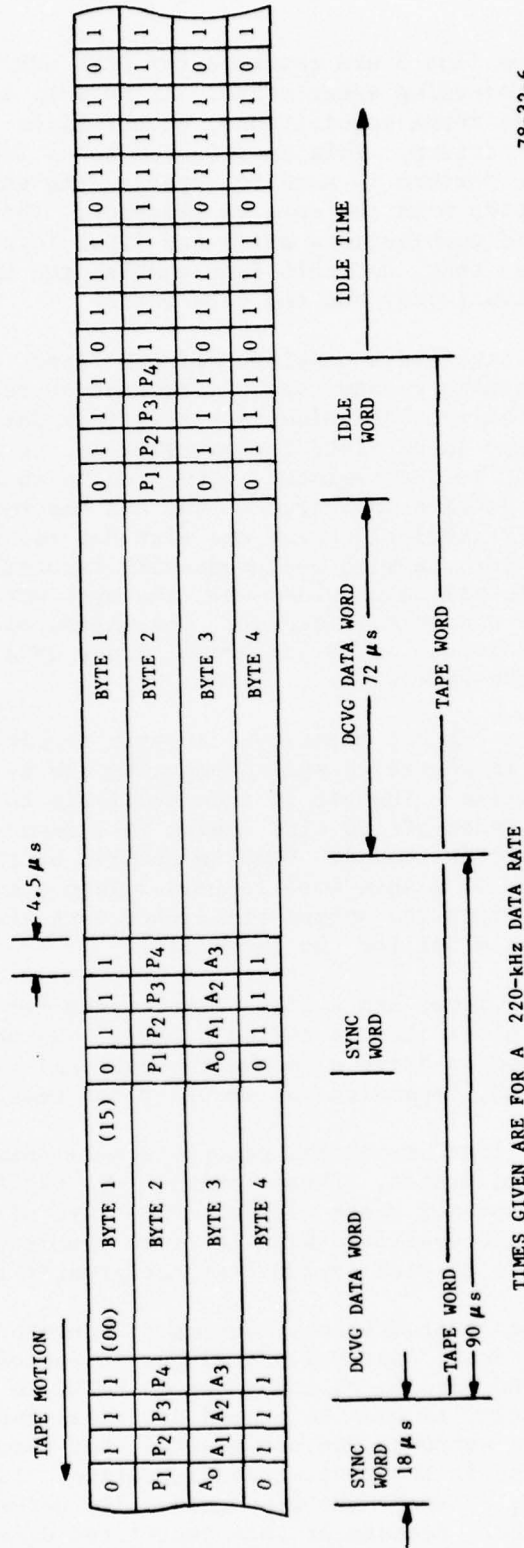
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PICK - OFF HEADER

ON-LINE DCVG

ON-LINE DCVG

RIB

78-32-4

FIGURE 4.   BREADBOARD MODEL RECORD INTERFACE BUFFER

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FIGURE 5. RECORD INTERFACE BUFFER (RIB)

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TO
RECORDER
AND
P/RAM

4 LINES

SYNC &
PARITY
INSERT

OUTPUT
REGISTERS
AND MUX

OUTPUT
CONTROL
LOGIC

18 LINES

MAIN MEMORY
(8K X 18)

13 LINES

I/O ADDRESS COUNTER
AND MUX

18 LINES

SCRATCHPAD
MEMORY

4 LINES

INPUT
CONTROL
LOGIC

16 LINES

SOD

EOD

DECODE
LOGIC

FROM
DCVG

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TAPE MOTION

0	1	1	(00)	BYTE 1 (15)	0	1	1	1
P₁	P₂	P₃	P₄	BYTE 2	P₁	P₂	P₃	P₄
A₀	A₁	A₂	A₃	BYTE 3	A₀	A₁	A₂	A₃
0	1	1	BYTE 4	0	1	1

← 4.5 μs

BYTE 1 → | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
BYTE 2 → | P₁ | P₂ | P₃ | P₄ | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
BYTE 3 → | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
BYTE 4 → | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |

SYNC WORD
18 μs

DCVG DATA WORD

TAPE WORD
90 μs

SYNC WORD

DCVG DATA WORD
72 μs

IDLE WORD

IDLE TIME

TAPE WORD

TIMES GIVEN ARE FOR A 220-kHz DATA RATE

78-32-6

FIGURE 6. TAPE DATA FORMAT

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word, and the four bits on line 3 are reserved for DCVG address information in future multiple display recording experiments. If no data are available for recording, such as between frame acquisitions, output lines 1, 3, and 4 continually repeat the sync pattern. This is referred to as idle time. Line 2 is a logic "1." The sync pattern is used to separate the data words and keep the P/RAM in synchronization with the data on playback. This unique pattern is excluded from the valid combinations which the first four bits of the first byte of each data word can take, and this fact enables the playback section to distinguish between the sync words and the data words.

Once the main memory has acquired a complete refresh frame, the output logic begins unloading the main memory onto tape via the output registers. The unloading is done sequentially, beginning with the first data word loaded into memory. One word at a time is put into the parallel-in, serial-out output registers, each byte into its own register. The data in each are then clocked out serially onto its respective tape track. The RIB has two output clocks available, a 220-kilohertz (kHz) clock for use with HDD recorders and a variable 15- to 75-kHz clock for use with medium-density recorders. The unload operation (memory to register) takes place when the sync word is being inserted between data words by the output multiplexer. The unload operation requires 3.6 µs, and the sync word length is 18 µs; hence, a new data word is ready for recording at the end of the sync word.

The main memory has an 8 x 18k bit capacity. As each 16-bit is acquired from the DCVG bus, odd parity is generated and accompanies the byte through the scratch pad and main memories. The bit is then available to the output logic for parity checking. An index bit is also loaded into memory at the same time the first byte of each word is loaded. This is checked by the output logic to verify that the first byte of a data word is loaded into the first byte register. Therefore, two additional bits are stored along with each 16-bit data byte; one for the parity bit and the other for the index bit.

The RIB provides four data lines and a clock line to the recorder. This group of four data lines and a clock line is called a port. Two other parallel ports were provided; one was used to drive a second recorder and another was used as a direct input to the P/RAM, bypassing the recorder for test purposes.

RECORDERS. There are HDD instrumentation recorders available from several manufacturers in the United States. These machines are capable of packing 33,000 bits per inch of tape per track with an error rate of better than one error in 10^6 bits. They are available with 14 or 28 tracks on 1-inch wide tape. Most can accommodate 14-inch (9,200 feet) or greater reels.

In order to have an HDD recorder available during breadboard testing, two options were available. First, approval was sought to retrofit one of the FAA-owned medium-density (5,000 bits/inch) recorders at NAFEC to a high-density configuration. This recorder is used to record digitized radar in the NAS en route system. Retrofit approval was not granted, but permission was received to use the machine in its present configuration. Since it lacked the necessary deskewing logic, 15 to 25 kHz was empirically determined to be its maximum practical data rate. Because of this restricted data rate, it was used only as a backup recorder for limited testing and demonstrations.

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Second, a lease procurement of an HDD recorder was initiated. Each of the major recorder manufacturers, Ampex, Bell and Howell, Honeywell, and Sangamo, loaned FAA/NAFEC one of their recorders for a period of several months at no cost to the Government. In order to have maximum availability of the recorders for project use, a flexible schedule was arranged to stagger the delivery times 2 to 3 months apart. The first recorder received was a Sangamo Sabre IV, followed by a Bell and Howell VR-3700B, then an Ampex HBR-3000, and a Honeywell Model 96. Each recorder was configured for a four-track parallel recording/ playback operation. The tape speed used was 7 1/2 inches/second (ips) which allowed a 4.1-hour record time and a packing density of 29.3 kilobits/inch at a 220-kHz data rate.

To the RIB and P/RAM, the recorder was viewed as a "black-box" storage device. The RIB supplied the recorder with four parallel data lines and a clock line, while the recorder provided the P/RAM with four deskewed data lines and a clock line. Data deskewing was accomplished by the recorder reproduce electronics.

Skew is the sum of all the time displacements of parallel signals induced by the record/reproduce electronics and the tape/head interface variations. An example of tape skew is shown in figure 7. The recorder performs internal deskewing by compressing the incoming data on the record side and periodically inserting deskew bit patterns. This amounts to 16 to 32 deskew bits being inserted approximately every 512 incoming data bits. The data are first decoded, stored in large buffer registers, and each track is examined for its deskew pattern. The deskew words are then used to realign or synchronize the parallel data and are stripped out without any noticeable interruption of the data flow to the P/RAM. Error indicators are provided to show in-sync or out-of-sync conditions.

PLAYBACK/REFRESH ALTERNATING MEMORIES. The P/RAM accepts data from the recorder and stores these data alternately in two semiconductor memories for use in refreshing a playback display via a DCVG. The P/RAM contains two interfacing sections, one between the recorder and the memories and the other between the memories and the DCVG. A block diagram is shown in figure 8. Data from the P/RAM are provided to an offline DCVG and PVD which are standard unmodified NAS en route equipments. The breadboard P/RAM is illustrated in figure 9.

The P/RAM accepts data from one recorder port at a time. A recorder port consists of four data lines corresponding to four tape tracks used by the RIB to record display data. The port also has a common clock signal which is derived from the data by the recorder.

The sync words in the data stream are used to synchronize the data as they are received by the P/RAM and to provide parity and display address information. Each sync word contains a four-bit code on data line 3, specifying with which display the next DCVG word is associated (display address). Four P/RAM address switches allow an operator to select a specific display of a port for review. However, in the breadboard model, only a single display was recorded, and it had the address "0000." Three additional switches are used to select a specific port.
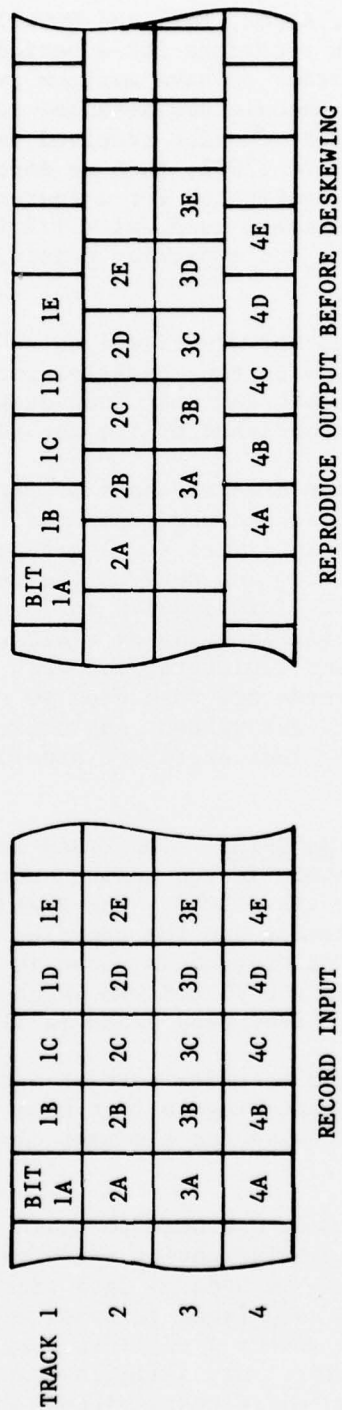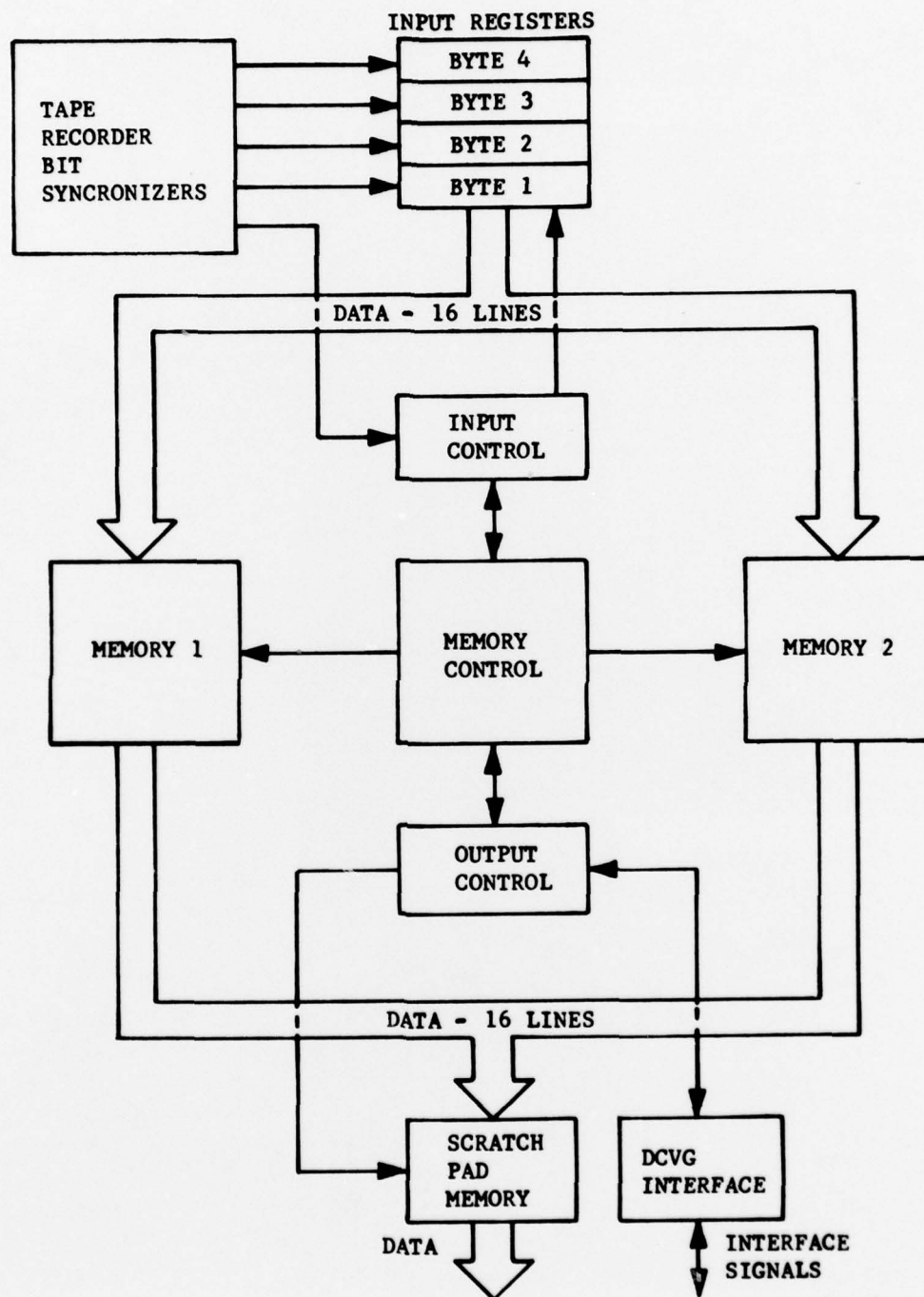
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RECORD INPUT

TRACK 1	BIT 1A	1B	1C	1D	1E
2	2A	2B	2C	2D	2E
3	3A	3B	3C	3D	3E
4	4A	4B	4C	4D	4E

RECORD INPUT

REPRODUCE OUTPUT BEFORE DESKEWING

BIT 1A	1B	1C	1D	1E		
	2A	2B	2C	2D	2E	
		3A	3B	3C	3D	3E
		4A	4B	4C	4D	4E

REPRODUCE OUTPUT BEFORE DESKEWING

FIGURE 7. TAPE SKEW EXAMPLE

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FIGURE 8.   PLAYBACK/REFRESH ALTERNATING MEMORIES (P/RAM)

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PLAYBACK PVD

OFF - LINE DCVG

P/RAM

78-32-9
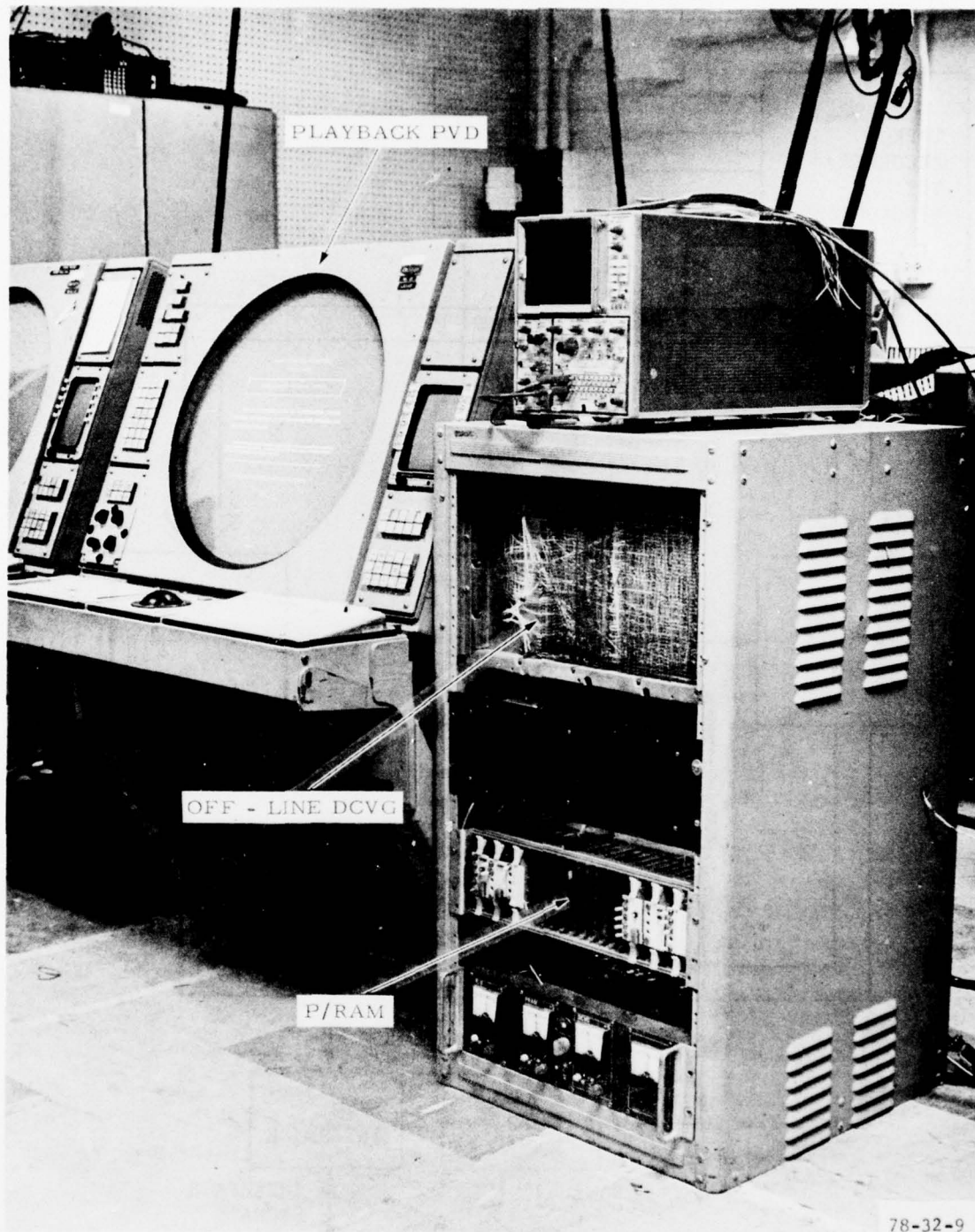
FIGURE 9.   BREADBOARD MODEL P/RAM

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The parity information on line 2 in the sync word contains an odd parity bit for each preceding data byte. The P/RAM input logic performs a parity check on each data byte and compares it against the sync parity bits. If there is a parity error on any or all lines, the P/RAM provides a visual alarm. The sync pattern on lines 1 and 4 is detected by the P/RAM input logic and used to initiate control and timing signals for the input logic. The sync word is stripped out of the data at this point. Idle time is also detected, and a visual indicator is set.

The input data are converted from a four-line, bit-serial format to the original 16-line, bit-parallel format by the P/RAM input registers. The data are then stored in one of two semiconductor memories, each with an 8,192-byte capacity. Two memories are used because of the requirement to store data from tape and refresh the playback PVD simultaneously. When the first memory has received a complete frame of data, the P/RAM uses the data in this memory to refresh the playback PVD via a DCVG. While the P/RAM is refreshing the display with data stored in the first memory (M1), it is storing the next frame of data in the second memory (M2).

When M2 has acquired a complete frame of data, the P/RAM waits until M1 has completed a refresh cycle and then switches over to M2 for refreshing the display. Then the next frame from tape is loaded into M1. The P/RAM alternates between M1 and M2 in this manner, as long as data are being received from the recorder or until manual intervention. A memory is full when it has received a complete frame of data, as determined by the decoding of the EOD word. The P/RAM will alternate between memories (and between frames) at a rate which is nominally equal to the sample rate used by the RIB. Each memory has its own address counter so that the input and output sections of the P/RAM can operate independently. Since the read access time for the memories is not fast enough to match the 4.4-MHz data rate needed to interface with the DCVG, interim storage is accomplished with a scratch pad memory. This memory is similar to the RIB input scratch pad and holds the one to four words used in each DCVG access cycle. It accepts data from the main memories and, under the control of the output section, transmits the data to the DCVG at the proper 4.4-MHz data rate.

The P/RAM is designed to operate in three display update modes; real time, freeze, and twice-real-time. In the real-time mode, the playback tape speed is the same as the record tape speed. For the HDD recorder, this was 7 1/2 inches per second (ips), while for the medium-density recorder 7 1/2 or 15 ips was used. In this mode, the data frames for the playback display are updated at the same rate as the data frames were sampled by the RIB. In the freeze mode, the P/RAM is continuously refreshing the display from a single memory without alternating. When the operator initiates the freeze mode, the P/RAM continues to refresh the playback PVD with its current frame while it continues loading the other memory with the next frame from the recorder. When the second memory is full, the P/RAM ignores any further new data sent by the recorder. In the freeze mode, the operator may manually switch between the two memories and can view either of the two stored frames for any length of time. When released from the freeze mode, the P/RAM will refresh the display from the alternate memory while it loads the next frame from tape into the memory from which it had been refreshing prior to the release.

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When the playback tape speed is twice that of the record speed, the display presentation is updated at twice the rate at which the data were sampled, and the P/RAM is operating in the twice-real-time mode. The P/RAM will automatically adapt to the doubled data rate, which results from the increased tape speed, as long as it does not exceed the 275-kHz input limitation. This 275-kHz input data rate limitation permits the P/RAM to operate in this mode only when using the medium-density recorder.

In refreshing the display, the P/RAM was designed to simulate the refresh subsystems of the CDC and the DCC. The P/RAM has a refresh rate clock which is adjustable about the 55-Hz point. Also the P/RAM was designed so that whenever the data load places the playback PVD in the asynchronous mode, the output circuitry of the P/RAM allows two refresh cycles to complete the frame, instead of just extending the one refresh cycle by the minimum amount needed to complete the frame. Thus, the refresh rate drops to 27.5 Hz in the asynchronous mode. This causes noticeable flickering of the PVD presentation and will be corrected in future designs. Figure 10 illustrates the synchronous and asynchrous modes of refresh for both the refresh subsystem and the P/RAM.

The P/RAM output section was designed to simulate the display refresh subsystem access assignment table, by using the same timing constraints to determine when the DCVG can access the refresh frame stored in memory.

In order for the DCVG to blink data on the display on playback, it is only necessary to supply the DCVG with the recorded data and a blink clock. The blink clock generated by the P/RAM is adjustable over a range of from 0.2 to 2.5 Hz, which is similar to the usable range of the CDC and DCC blink clocks.

The P/RAM was designed to transfer 16-bit bytes at a 4.44-MHz rate. It also supplies the VAD to the DCVG during the first byte time of a data transfer. In the P/RAM, the DCVG bus is not common with any other DCVG. Therefore, the VAD is used only to initiate the receiving of data and not to distinguish between the data for various displays.

The P/RAM was designed to examine the parity of each 64-bit word transferred between the alternating memories and the DCVG, and generate an error signal at the proper time. However, this circuit caused interference for other circuits in the output section and disconnected.

Other interface signals presented to the DCVG are the W/B setting (2 bits) and the master reset line. The W/B bits are set using two toggle switches on the output board, and the master reset is activated using a pushbutton switch on the clock board.

TESTING.

INITIAL TESTING. In order to facilitate the debugging of the NADIRS, a number of test patterns were developed. These test patterns consisted of groups of data of the type used by the DCVG to form a presentation on a PVD. Since it was considered inefficient to schedule computer time (CDC or DCC) each time it was necessary to debug or checkout the NADIRS, a Lockheed MAC-16 minicomputer was utilized to interface with a standard DCVG/PVD and simulate either the CDC or DCC system.
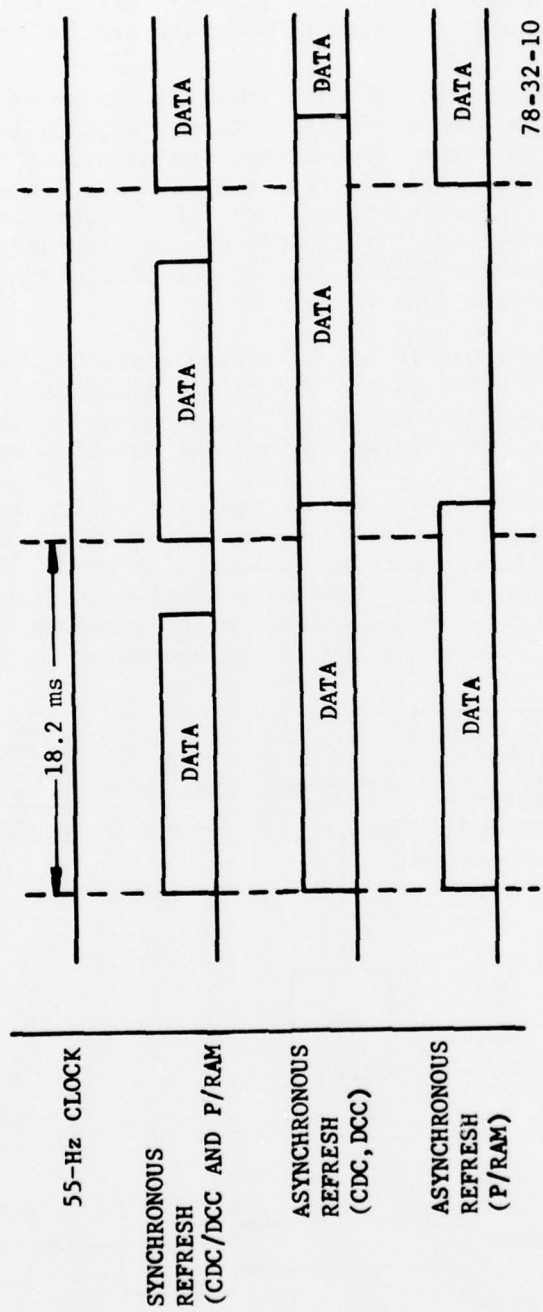
18

FIGURE 10.   REFRESH RATE TIMING

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The minicomputer, being a dedicated piece of equipment for the project, permitted the use of the test patterns whenever they were needed, without the problems associated with CDC or DCC use. It also greatly facilitated the modification of the data through the use of a support software program called "DEBUG."

Another support program, called "CARGEN," was used to store the data patterns on tape cartridges for future use, using a tape system built into the minicomputer. When using the patterns for testing, the data were stored in the memory of the minicomputer and then transferred to a DCVG via the direct memory access bus of the minicomputer. The interface logic that controlled the transfer was called the Display Data Generator (DISDAG) and was designed and built at NAFEC as a unit to drive a standard DCVG. Many of the DISDAG circuits are the same as those in the P/RAM output logic.

With this arrangement, the MAC-16 simulated the refresh memory of CDC or DCC, acting as a repository for the data. The DISDAG simulated the DG input/output (I/O) bus transferring the data to the DCVG upon request, with timing similar to a live DCVG bus. A block diagram of the test bed is shown in figure 11.

The test patterns are primarily fixed patterns (no moving data) but can be varied in size and complexity to simulate different data loads. One dynamic pattern, with variable symbol velocity, was used to check updating of playback data. The evaluation of the breadboard model consisted primarily of visually checking for errors or deviations in the patterns on the P/RAM-driven PVD. The test patterns used are shown in the appendix.
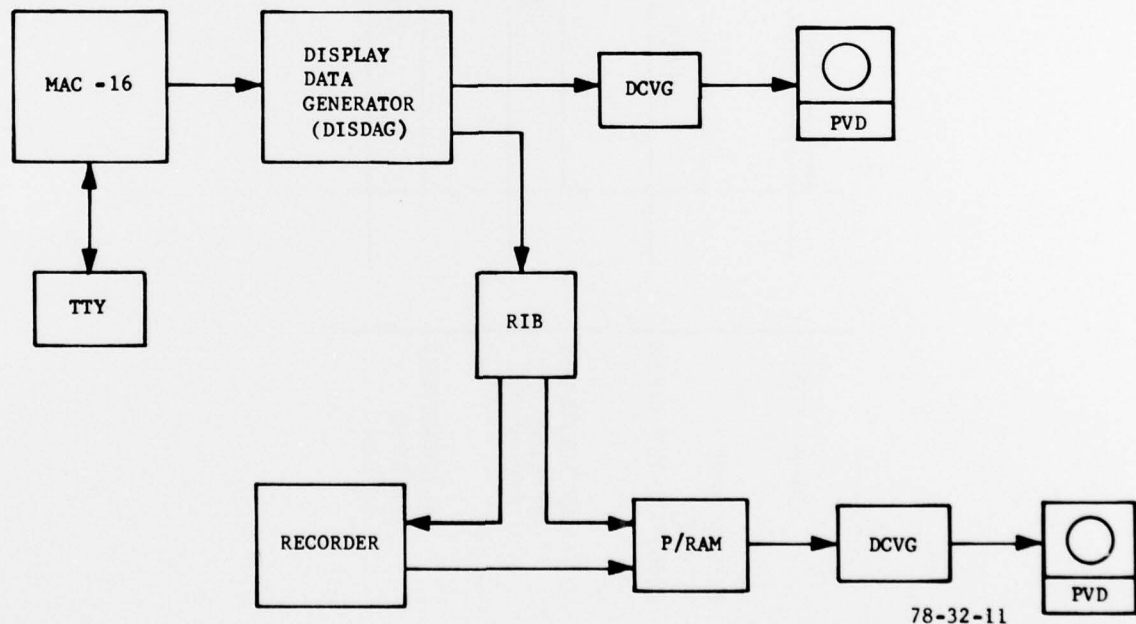

78-32-11

FIGURE 11.   NADIRS TEST BED UTILIZING MAC-16

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LIVE TESTING. Once the system was thoroughly checked out in the lab, the RIB was moved to the DG area of the System Support Facility (SSF) for recording "live" data from the input to a DCVG in an active DG. The PVD which was being driven by this active DCVG was remoted to the recording lab area.

A second PVD was used to display recorded data processed through the NADIRS so that a side-by-side, visual comparison between the original and recorded data could be performed. This was possible since the recorder reproduce electronics can be active while the recorder is in the record mode.

RESULTS. During the tests that were conducted, and during the numerous demonstrations that were provided to FAA and nongovernment personnel, the NADIRS, utilizing the digital recording technique, performed satisfactorily. Although all the system design constraints were met, there were minor differences between the live and record/playback presentations. These differences were as follows:

   a.   Brightness and focus were the only active controls on the playback PVD.

   b.   The trackball symbol did not move as smoothly on the playback PVD as on the "live" PVD. This is due to the sampling rate of the RIB.

   c.   The blink rate on the playback PVD may not be the same as the "live" PVD, but it can be adjusted to match the "live" presentation.

CONCLUSION

As a result of this project activity, it is concluded that the single-channel breadboard model, employing the digital recording technique and utilizing the Display Control Vector Generator input area as the data recording point, adequately demonstrated the feasibility of recording, storing, and reproducing NAS enroute air traffic control display data.

RECOMMENDATION

It is recommended that, based upon the successful demonstration of the single-channel breadboard model, a full-scale multiple-channel engineering model be designed, fabricated, and evaluated.

APPENDIX

PVD Test Patterns

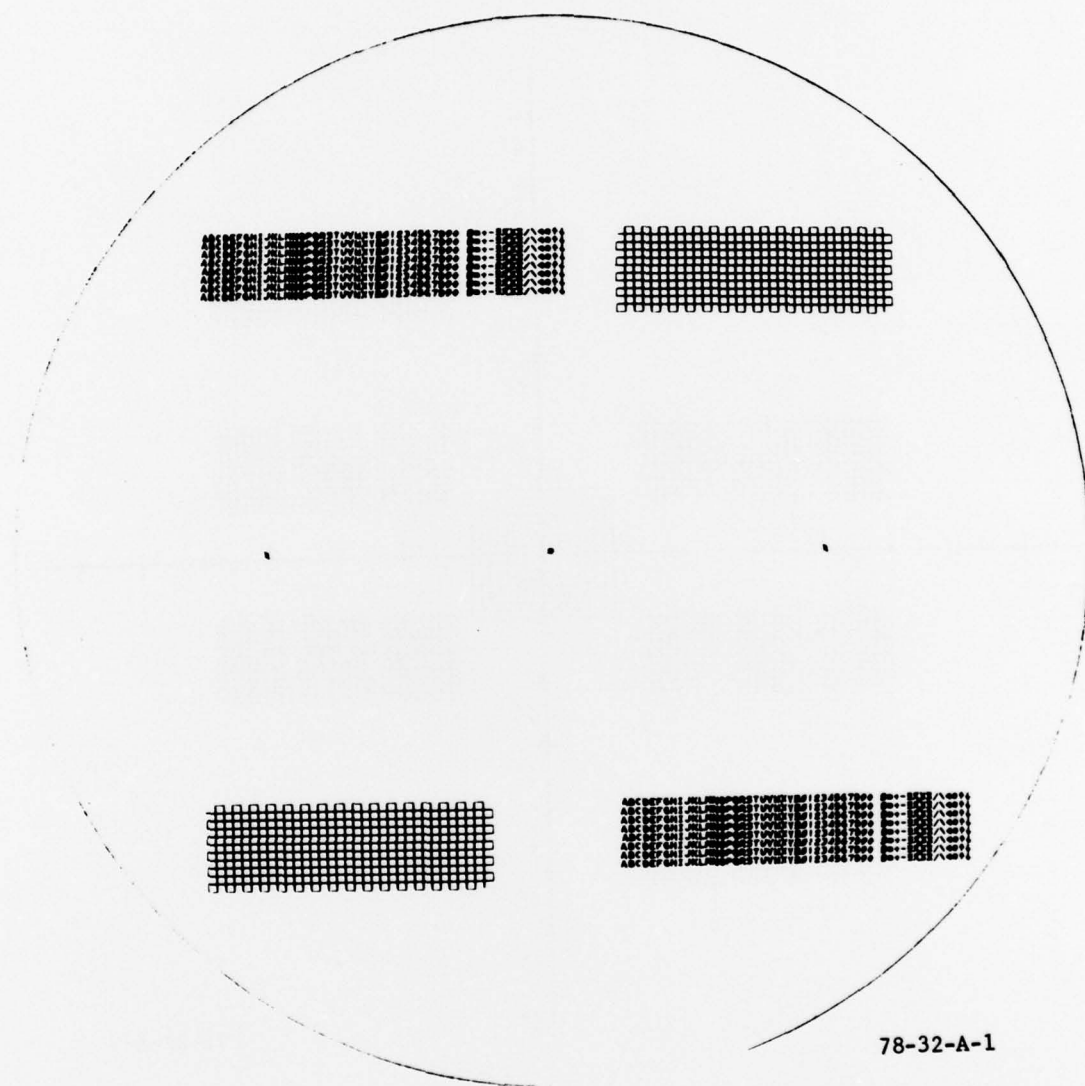## LIST OF ILLUSTRATIONS

78-32-A-1

FIGURE A-1. ALPHANUMERIC/GRID TEST PATTERN, 1,001 DCVG WORDS,
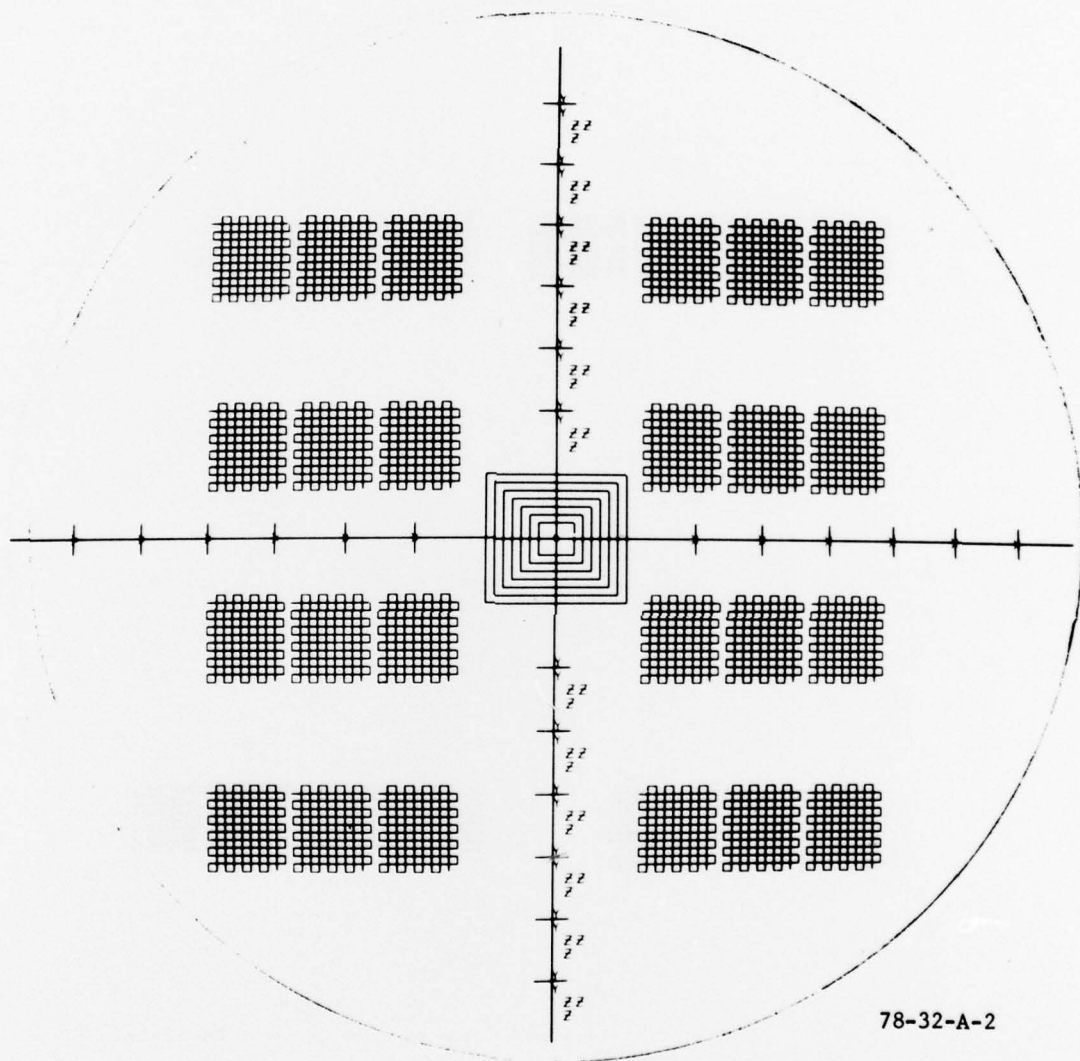PROGRAM NAME: MP(sp)A, 11.2-ms REFRESH

A-1

FIGURE A-2.   GRID TEST PATTERN, 1,000 DCVG WORDS. PROGRAM
NAME: MP(sp)B, 11.9-ms REFRESH
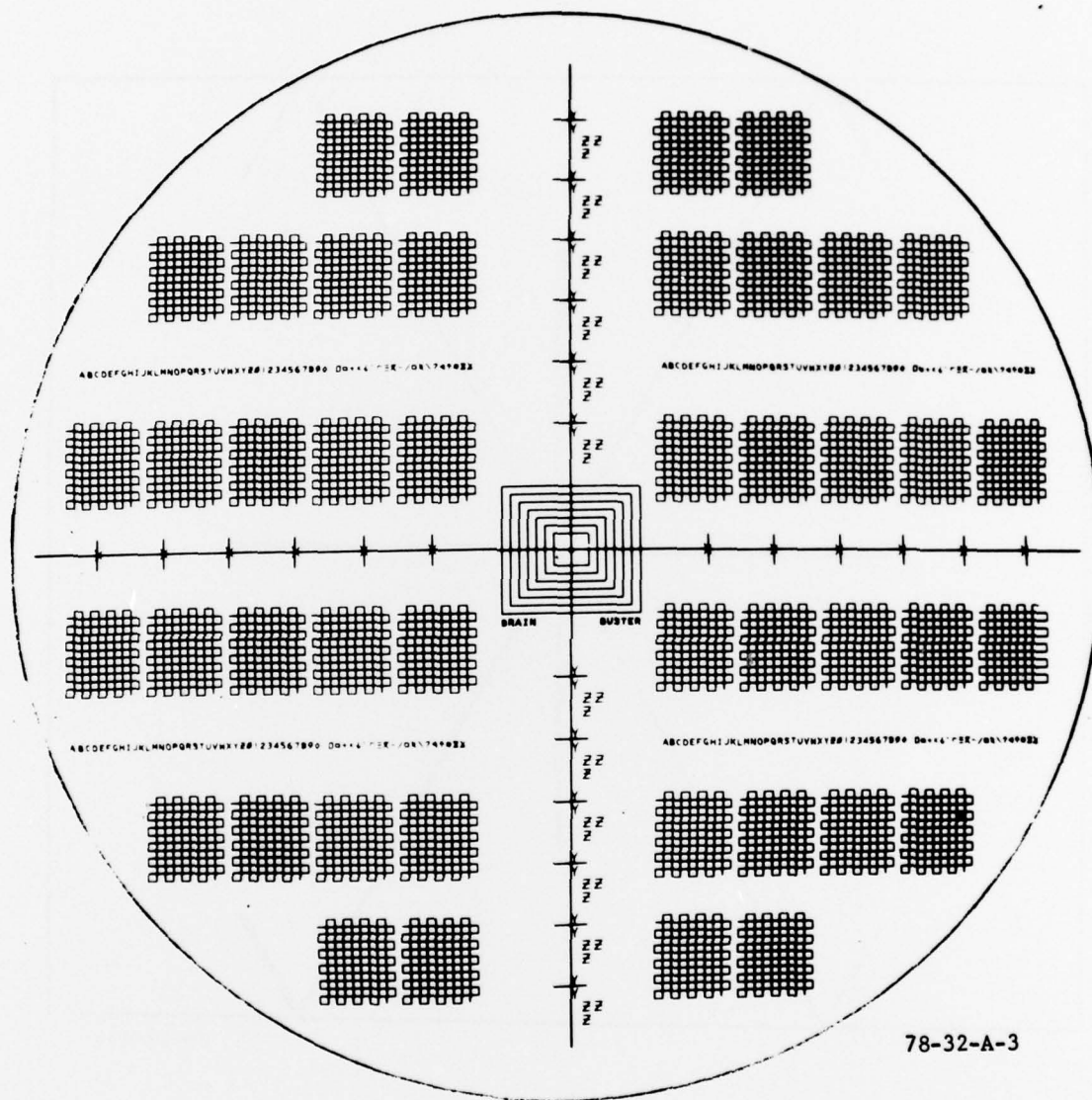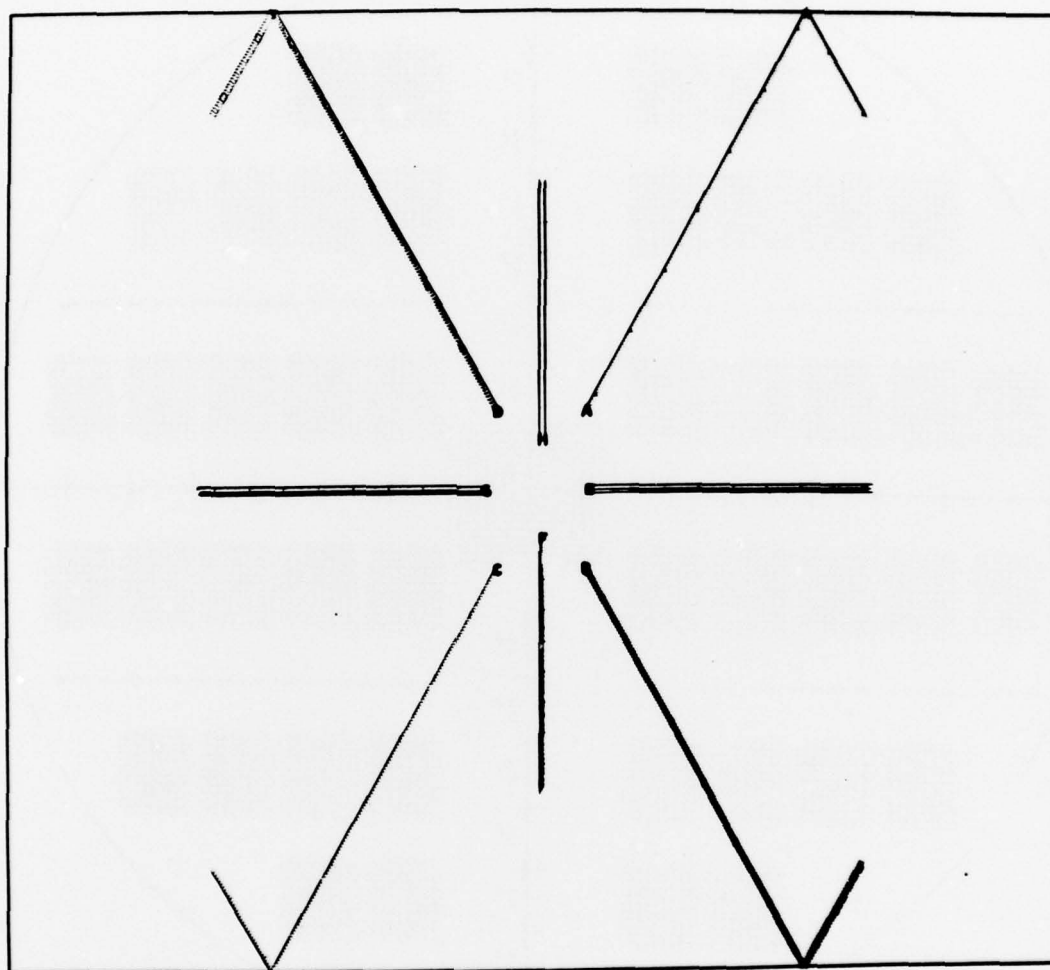
A-2

78-32-A-3

FIGURE A-3.   HEAVY GRID TEST PATTERN, 2,026 DCVG WORDS,
              PROGRAM NAME: MP(sp)BB, 23.3-ms REFRESH

A-3

78-32-A-4

FIGURE A-4.   DYNAMIC TEST PATTERN (TIME EXPOSURE), 13 DCVG WORDS,
PROGRAM NAME: ADP(sp)A, 430-ms REFRESH

A-4

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