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JAN 78 J W AMOSS, E L MEEKS, N W COX N00173-76-C-0044
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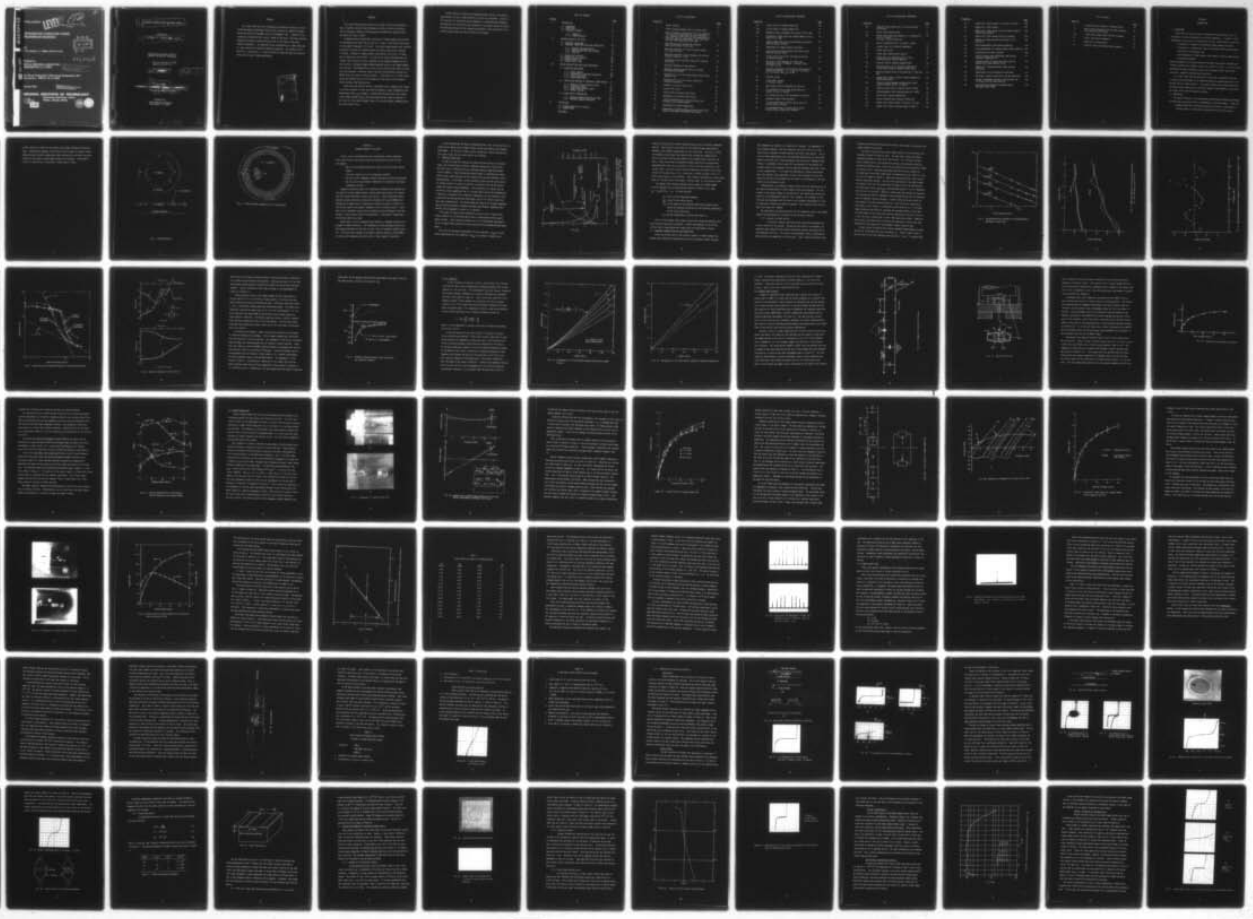

FINAL REPORT

LEVEL III

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INTEGRATED VARACTOR TUNED MICROWAVE SOURCES

By

J. W. Amoss, E. L. Meeks, and N. W. Cox

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Prepared for

NAVAL RESEARCH LABORATORY
WASHINGTON, D. C. 20375

For Period 15 September 1975 through 30 September 1977
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Atlanta, Georgia 30332

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Engineering Experiment Station
Georgia Institute of Technology

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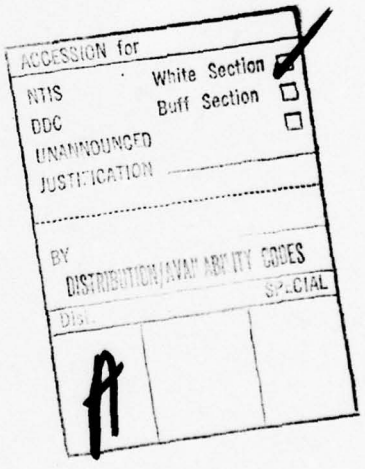
PREFACE

This report describes work performed at the Georgia Institute of Technology Engineering Experiment Station under Contract No. N00173-76-C-0044 during the period 15 September 1975 to 30 September 1977. Funding for the program was provided by Mr. Larry W. Sumney of the Naval Electronics Systems Command with technical administration by Mr. Eliot Cohen of the Naval Research Laboratory. Ion implantation was performed by Dr. James Comas and Dr. Harry Dietrich of the Naval Research Laboratory. The authors wish to thank Dr. B. Fank and Dr. S. Long of Varian for supplying Gunn and varactor chips used in some of these experiments.



ABSTRACT

This report describes the results of a study in which the objectives were to develop varactor-tuned microwave oscillator circuits and planar device technology leading to minimum parasitic monolithic varactor-tuned microwave oscillators (VCOs).

A wideband varactor-tuned Gunn oscillator of lumped element construction was developed which tuned from 6.0 GHz to 11.5 GHz, a 63% tuning range based on the midband frequency of 8.75 GHz. This tuning range exceeds that reported previously by others for varactor-tuned oscillators with center frequency in X-band. Although of lumped element construction, the circuit is adaptable to monolithic construction. It consists of series-connected Gunn and varactor chips which are series resonated at the midband frequency by an inductive wire, a wideband lumped element matching section, and lumped element bias sections. Performance data of this circuit using various types of varactors are presented. Excellent tuning linearity occurred when low-high-low IMPATT chips were used as tuning varactors. A deviation of $\pm$ .5% from linear tuning was obtained over a 2.5 GHz range with less than 15 volt change in tuning voltage using these devices.

Planar Gunn and varactor devices, developed on this program, were tested in various microwave circuits and found to operate at lower frequencies than conventional Gunns. For example, a planar Gunn-varactor device was tested in the lumped element circuit described above and was found to operate in the 2 GHz to 4 GHz range at power levels of a few milliwatts, depending upon Gunn and varactor bias.

Initial efforts to develop ion-implanted planar varactors and planar Gunn devices for use in GaAs monolithic circuits are presented. Control of the varactor C-V relation by device geometry is considered and procedures developed for the fabrication and isolation of the planar devices are given. Detailed descriptions of the problems encountered in the fabrication of implanted planar diodes and the solutions are discussed.

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SECTION I

INTRODUCTION

1.1 BACKGROUND

During the past few years great improvements have been made in the instantaneous and tuning bandwidth of microwave components. In general, these improvements can be directly attributed to circuit simplifications involving;

- elimination of dispersive transmission media whenever possible,
- elimination of transmission lines of dimensions that are appreciable fractions of a wavelength, and
- the replacement of these elements with lumped or nearly lumped tuning and matching elements.

Notable examples of this design approach include 50 ohm coaxial switches and limiters covering the frequency range from 100 MHz to 18 GHz. A similar design philosophy has been successfully applied to microwave devices such as the multicell, internally matched power-transistor.

It is well known that the potential of microwave semiconductor devices is seldom realized because of the combined effects of package parasitics, dispersion and line length effects. A particular device where careful attention to these factors should have a significant impact on performance is the varactor tuned, solid-state microwave oscillator.

1.2 OBJECTIVES

The overall efforts of this program were aimed toward advancing technology in three areas which would lead to improvements in VCO performance. These are:

- Lumped element VCOs (voltage controlled oscillators) constructed in minimum parasitic configuration compatible with MIC construction.

- A new planar tuning varactor in which the C-V relationship is controlled by the device geometry.
- Completely integrated monolithic VCO circuits.

The work efforts during the first part of the program were divided into two distinct tasks - one classified as Minimum Parasitic VCO Study and the other as Planar Varactor and Gunn Diode Development.

Specific objectives of the Minimum Parasitic VCO study were to:

- demonstrate both theoretically and experimentally the capabilities and limitations of lumped element VCO.
- improve the thermal characteristics of VCOs by mounting Gunn and varactor chips on same or adjacent diamonds.
- compare the performance of lumped element VCOs with that of more conventional VCOs (microstrip, coaxial, etc.).
- provide design data for the development of planar monolithic VCO circuits.

Specific objectives of the Planar Varactor and Gunn Diode Development study were to:

- formulate decisions regarding material for initial demonstration and fabricate epi-layers.
- perform theoretical analysis of structures and develop model.
- design masks and perform ion implantation.
- process, mount and evaluate devices.
- evaluate diodes in microwave VCO.

The objectives of the second part of the program were to develop and test a planar varactor diode and Gunn device on a common chip. If successful, the planar Gunn-varactor (pGv) chip would then be incorporated into a completely integrated monolithic circuit.

1.3 Technical Approach

1.3.1 Circuits

Although the main program goal was to advance technology in the area of monolithic VCOs, initial circuit efforts during the first part of the program were concentrated on circuits constructed with discrete elements. These circuits were used to investigate the effects of parasitics and distributed circuit elements on VCO characteristics and to establish a prototype design for a completely monolithic VCO.

Individual Gunn and varactor chips, obtained from commercial vendors, were mounted on diamond heat spreaders (the diamond providing the d.c. electrical isolation required for series connection). The combined Gunn-varactor devices were used to develop lumped-element circuits which would be compatible with monolithic realization later in the program. Concurrently with the circuit development efforts, efforts to develop planar Gunn and varactor devices to replace the above combination were conducted. Results of the circuits and the planar Gunn-varactor efforts were combined in the latter part of the program in an attempt to develop a monolithic VCO.

1.3.2 Planar Varactor

Part of the work on this program has been directed towards the fabrication of a planar varactor diode with an implanted p-n junction that is normal to the surface of the device. The device structure is shown in Figure 1. An n-type epitaxial layer .5 μm thick is grown on a semi-insulating GaAs substrate and implanted with Be(p^+) and Se(N^+) in selected regions by using photoresist masks. A p-n junction is formed in the n-type epitaxial layer close to the p^+ implant when the implant damage is annealed. The active part

of this junction is normal to the surface and extends through the epitaxial layer. Changing the geometry of the device such as shown in Figure 2 should change the way the space charge moves under applied bias and thus allow modification of the diode's capacitange voltage (C-V) relation. Optimization of the C-V relation will allow better linearization of VCOs.

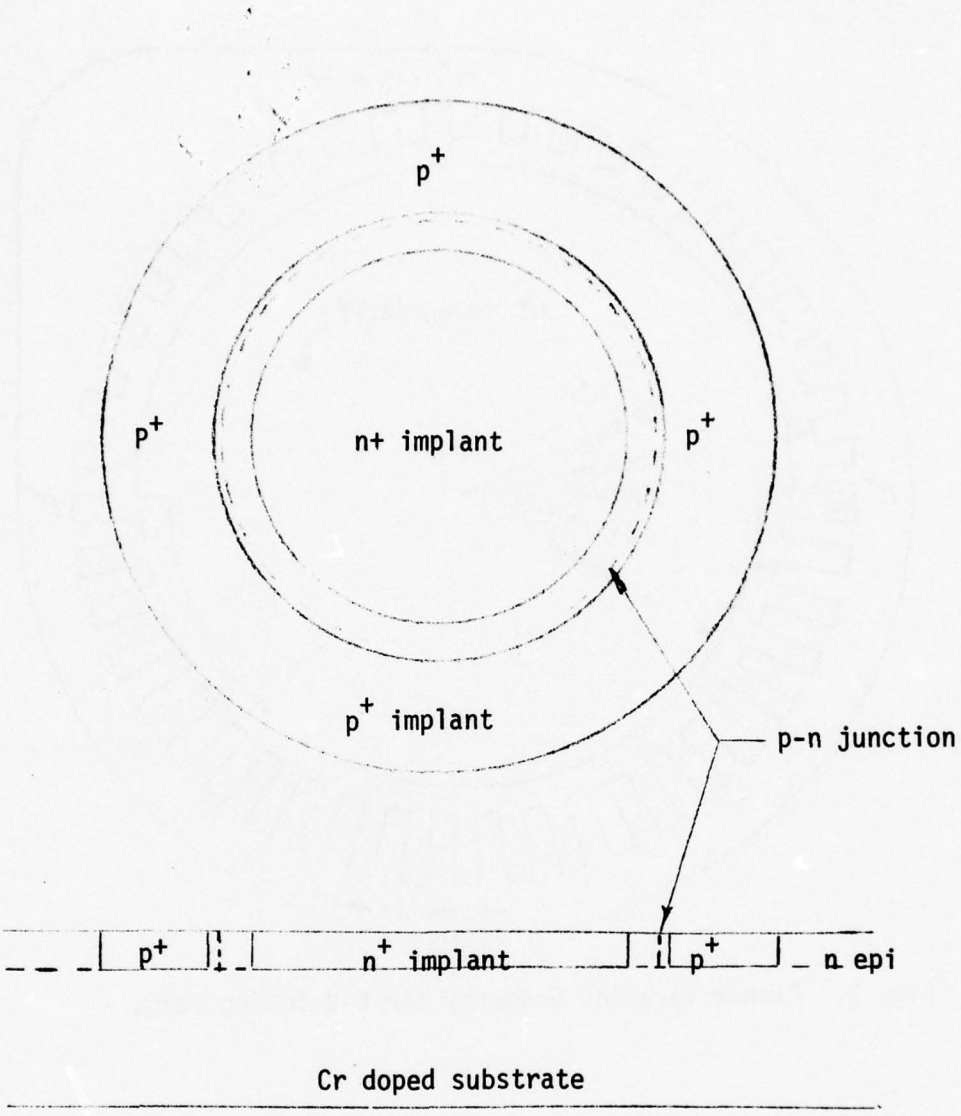

Fig. 1 Planar Varactor

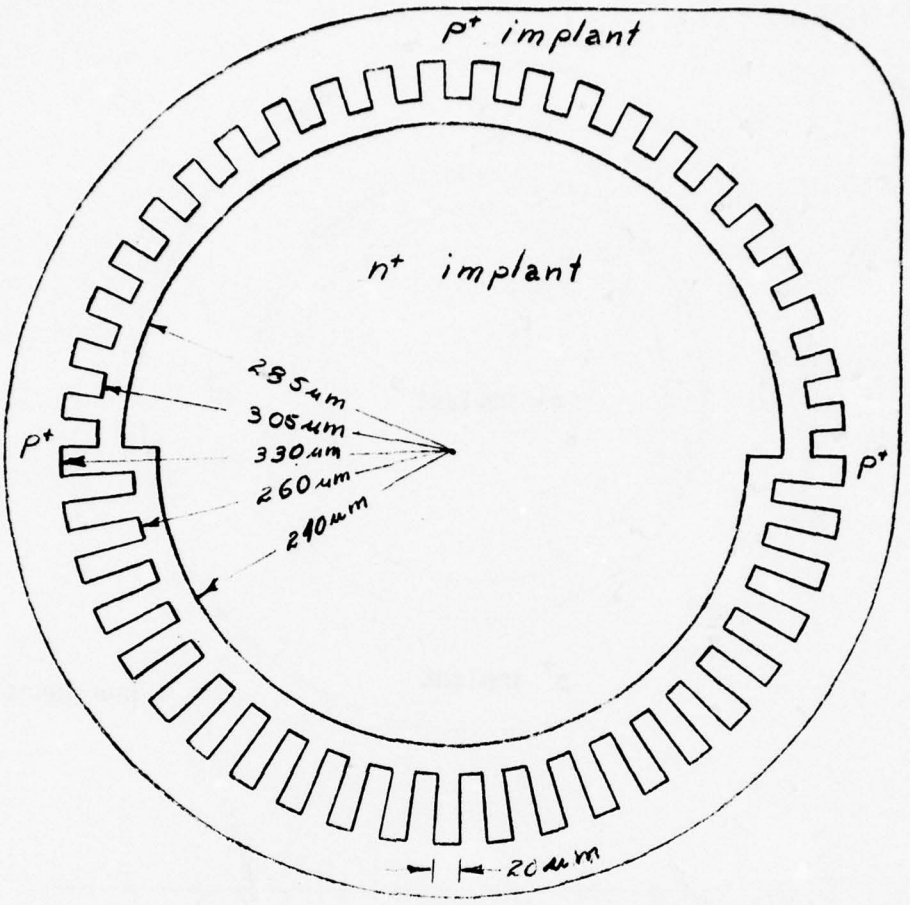

Fig. 2. Planar Varactor Geometry for C-V Tuning Tests.

SECTION II

MINIMUM PARASITIC VCO STUDY

Initial circuit investigations were influenced by several questions which arose prior to the actual design and construction of test circuits. For example:

- What circuit topology would most likely yield the largest tuning range?
- Could the complete circuit be adequately modeled?
- Are the circuit components readily available or easily constructed?
- Are the circuit and elements compatible with monolithic microwave integrated circuits?

Computer simulations were first conducted to determine the expected tuning range of various lumped element circuits which were chosen to be compatible with planer monolithic circuit construction. These simulations used a computer program (previously developed at Georgia Tech) called EMBED which enabled one to embed chips of known device properties within a certain circuit and to compute the terminal impedance of the resulting circuit. Individual circuit parameters were varied to examine how each affected circuit performance. During these initial investigations, a "best guess" lumped model for the Gunn device was used.

Concurrently, circuit components were mounted in standard microwave pill packages of known parasitics. The impedances of these packaged devices were then measured between 6.0 GHz and 12.0 GHz, using an automatic network analyzer. These data were reduced using another computer program, called DEMBED, to obtain chip impedances which was used in later computer simulations.

Circuit simulations and device characterizations, were used extensively to guide circuit design and to compare actual circuit performance with expected performance. The results of these circuit simulations, device characterization, and circuit tests are described in this section.

2.1 COMPUTER SIMULATIONS

In order to study the interactions among the Gunn device, the varactor diode, and the associated circuitry, computer simulations of the various possible circuit configurations were performed assuming idealized lumped circuit elements. These simulations proved helpful in establishing, among other things, specifications for the varactor chip for the different circuit configurations. Of the many circuits analyzed, those with the tuning varactor either directly in series or directly in parallel with the Gunn device showed the largest tuning bandwidths. This conclusion, of course, was due partially to the assumptions that (1) the Gunn device could be represented by a capacitor in parallel with a negative conductance, (2) all parasitics associated with the two devices were negligible, and (3) all other circuit elements were nondispersive. The tuning range was found to be strongly dependent upon the relative values of varactor and Gunn capacitances, depending upon whether the two appeared in series or in parallel.

The curves of Figure 3 were plotted for use as an aid in choosing the tuning varactor for a given Gunn device and in interpreting initial experimental results. These curves are based on a C vs V relationship characteristic of an ideal abrupt junction silicon varactor and the assumptions mentioned above.

The ratio of equivalent capacitance for bias condition 1 (C_{eq1}) to equivalent capacitance for bias condition 2 (C_{eq2}) is plotted in Figure 3 as a

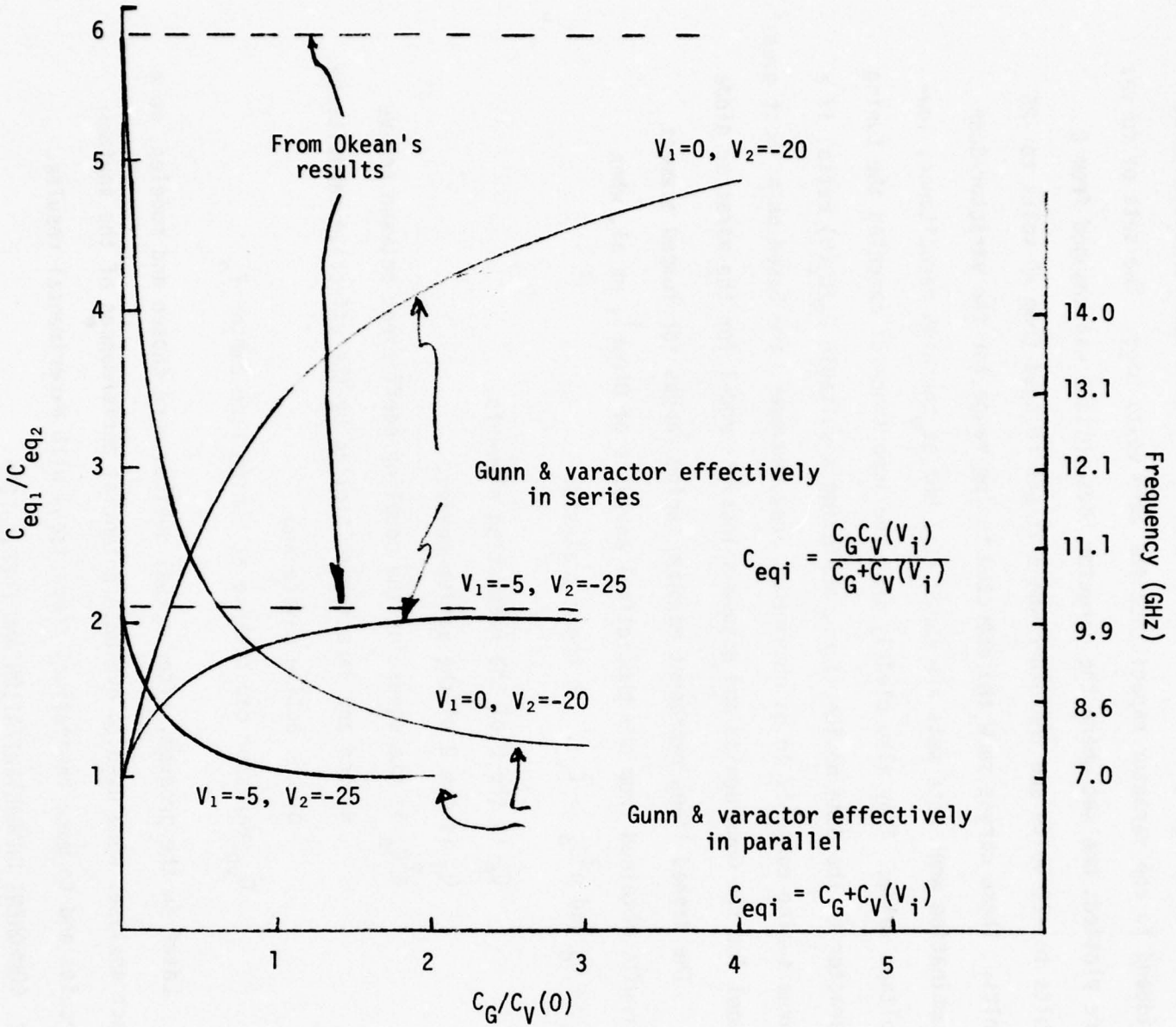

Fig. 3. Ratio of effective capacitance for bias condition 1 to effective capacitance for bias condition 2 as a function of the ratio of Gunn capacitance to zero bias varactor capacitance. The right hand ordinate shows expected tuning range.

function of $C_G/C_v(0)$ for series connected devices and for parallel connected devices. Here $C_G/C_v(0)$ is the ratio of the effective Gunn capacitance at midband to the varactor capacitance for zero volts bias. Two sets of curves are plotted; one set where the varactor bias voltage was changed from 0 volts to -20 volts and the other where it was changed from -5 volts to -25 volts. These curves show the expected tuning range for the varactor-Gunn combination when both sets are tuned to 7 GHz at the high capacitance, low-voltage value. They also clearly show the importance of matching the tuning varactor to the Gunn device (i.e., achieving a suitable $C_G/C_V(0)$ ratio) if a large tuning range is to be obtained. They, however, are based on a "best guess" model for the Gunn device and assume a lossless model for the varactor diode.

The dashed lines represent maximum tuning ranges for lumped element circuits obtained from the theoretical analysis of Okean[1], et al, when $Q_m << Q_d$ and $n^2C_d >> C_{vo}$. In their analysis:

Q_m is the Q of the resonating elements,

Q_d is the Q of the active device,

N^2C_d is the square of the coupling coefficient between active device and varactor multiplied by the effective capacitance of the active device and

C_{vo} varactor capacitance at tuning band center f_o.

Later in the program, after actual devices were chosen and modeled, more exact analyses were used to evaluate potential performances of the various circuits and to make theoretical comparisons with experimental results.

2.2 COMPONENT CHARACTERIZATION AND FABRICATION

During the initial part of the program, samples of lumped element components were prepared and characterized using an automatic network analyzer.

Each component was mounted in a standard pill package. The impedances of the packaged components were then measured over the 6.0 GHz to 12.0 GHz range using an automatic network analyzer and special test mounts. The results of these measurements were then modified theoretically by extracting readily calculable test fixture parameters from the overall impedance data. Finally, a reasonable circuit model for the remainder of the network was assumed, based on the geometry, and the modified impedance data were fitted to this assumed model. It has been the experience of these investigators that this approach gives equivalent circuits that represent not only the electrical effects of the network but the physical significance of the individual circuit elements as well.

Unfortunately, the automatic network analyzer was not functioning at its best when the admittances of these elements were being measured. This was evident in the unusual amount of periodicity in the reduced data giving the effect of an uncompensated length of line. However, the "average" of the data gave good agreement with the data of low frequency measurements or that of theoretical calculations based on geometry, thus indicating that the elements did indeed act "lumped".

The fabrication and characterization of the components used in the lumped element VCO experiments are discussed in the following sections.

2.2.1 Varactor and Gunn Devices

A variety of varactor and Gunn devices were used throughout the circuits portion of the program. During the early part of the program, experiments were conducted using devices previously secured from Sperry Microwave Components Division. The results of measurements taken to characterize these devices are summarized in this section. Later, varactor and Gunn chips,

obtained from Microwave Associates and Varian, were tested in microstrip and lumped element VCO circuits.

The Sperry varactors were nearly abrupt junction silicon devices with breakdown voltages of about 40 volts. On each chip, various size mesas (diameters between 0.5 and 6 mils) were etched. This multimesa arrangement allowed circuits to be tested with various size varactors simply by connecting different mesas to the circuit without having to physically remove and replace chips. Measured capacitance data versus total voltage for selected mesas (there were eight mesas of graduated size per chip) of a typical chip are shown in Figure 4. These data were measured at 1 MHz, using a Boonton capacitance Bridge. The zero bias capacitance of the mesas ranged from about 2.50 pF for the largest mesa to about 0.25 pF for the smallest. The capacitance ratio, C_{max}/C_{min}, varied between about 6:1 to 4:1, depending upon the size of the mesa. Samples of these chips were mounted in microwave pill packages and the net impedance of the packaged device was then measured using an automatic network analyzer. Figure 5 shows the reactive part of the varactor chip when reversed biased to -1 and -20 volts, respectively. Also shown in this figure is a theoretical curve based on that of an ideal lumped capacitor and chosen to represent the average behavior of the data. The capacitance of this particular mesa was measured as 0.74 and 0.25 pF at -1 and -20 volts, respectively, on the 1 MHz capacitance bridge. Comparing these values with those used to generate the theoretical curves gives some indication of the accuracy of the automatic network analyzer data.

A major reason for making the microwave impedance measurements on these devices was to estimate the loss resistance, R_s. Figure 6 shows a plot of the real part of the chip impedance when biased to -1 volt. In reducing the

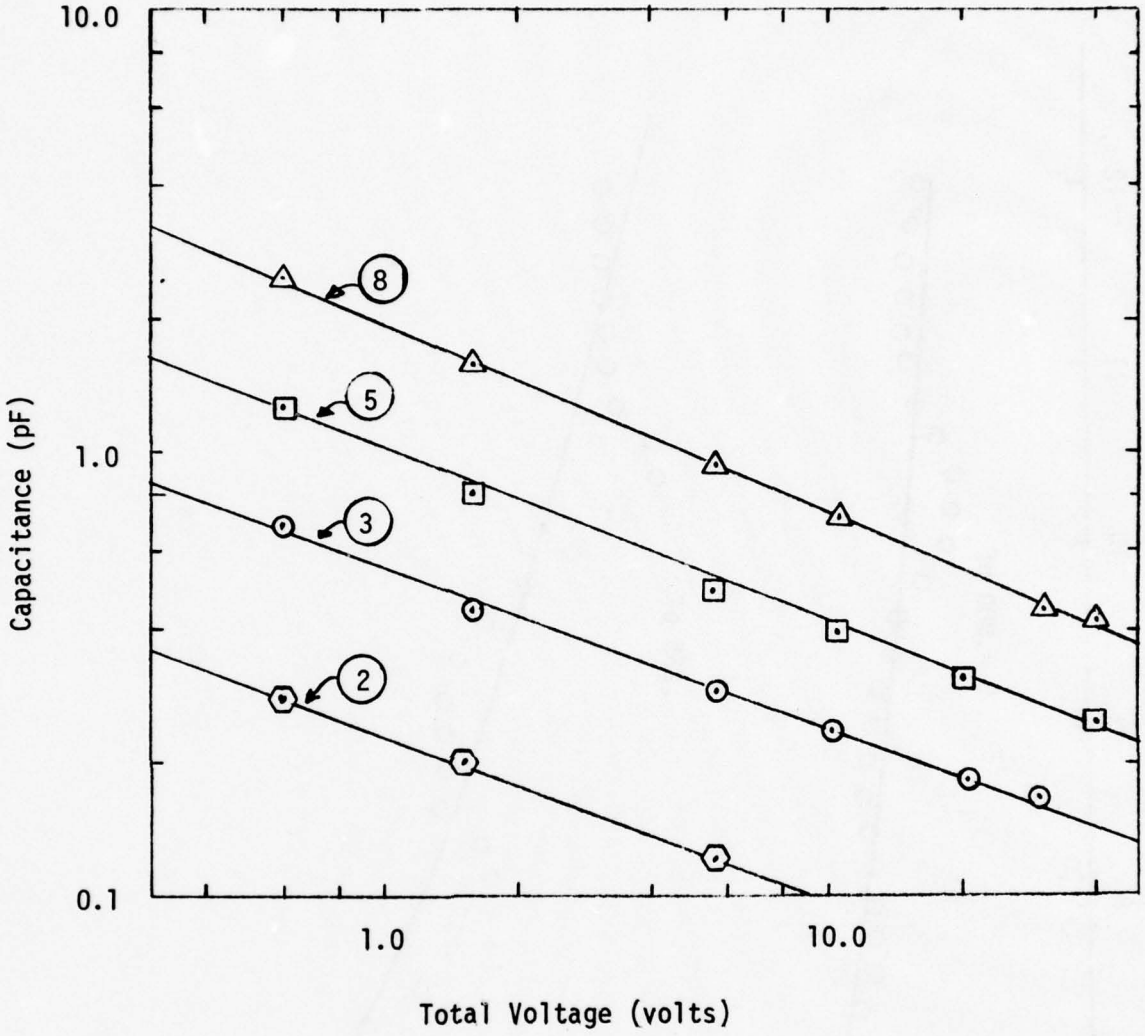

Fig. 4. Capacitance Versus Voltage for Selected Mesas of Multimesa Silicon Chip.

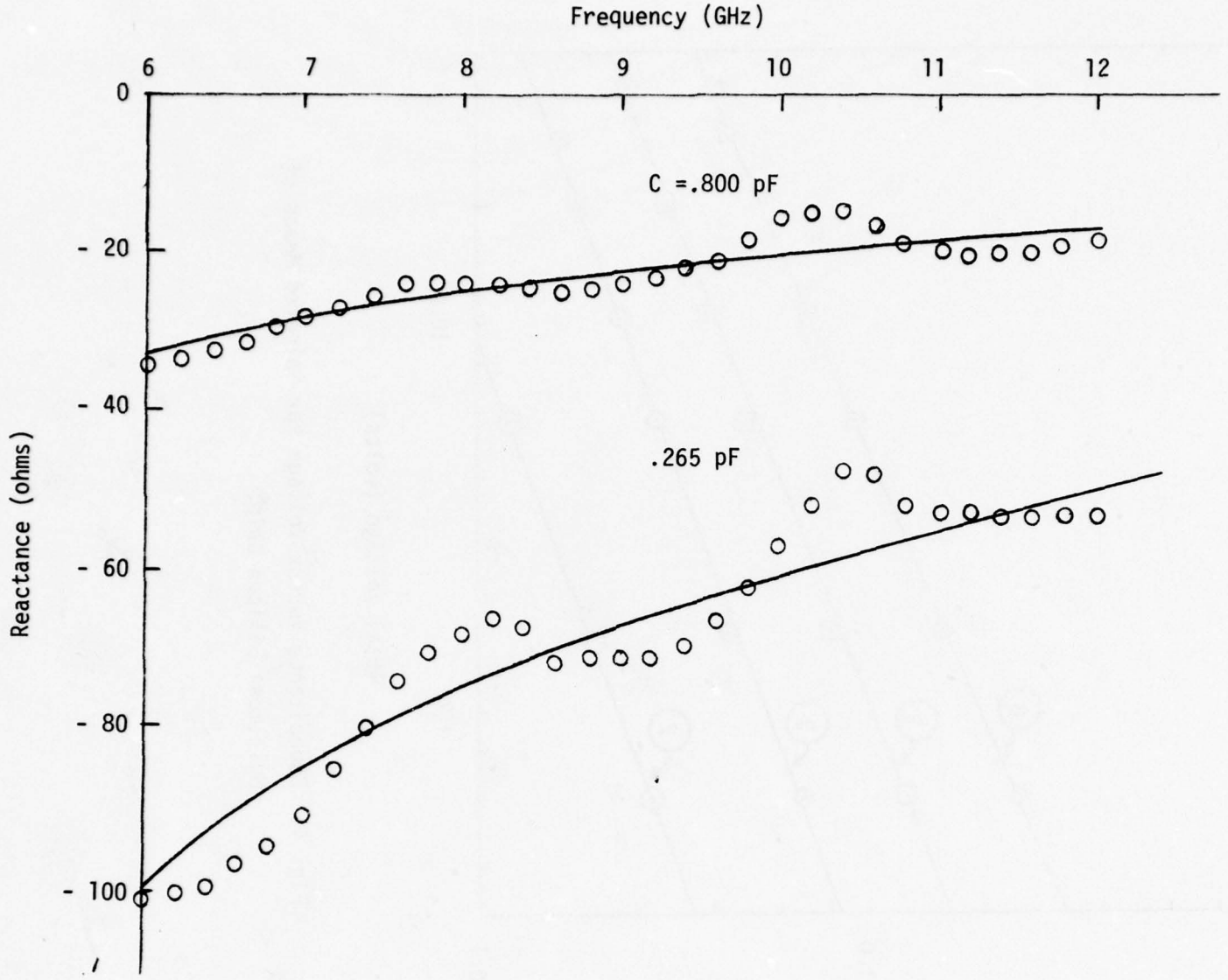

Fig. 5. Measured Reactance of Silicon Varactor Biased to -1 and -20 volts, type E-73-15.

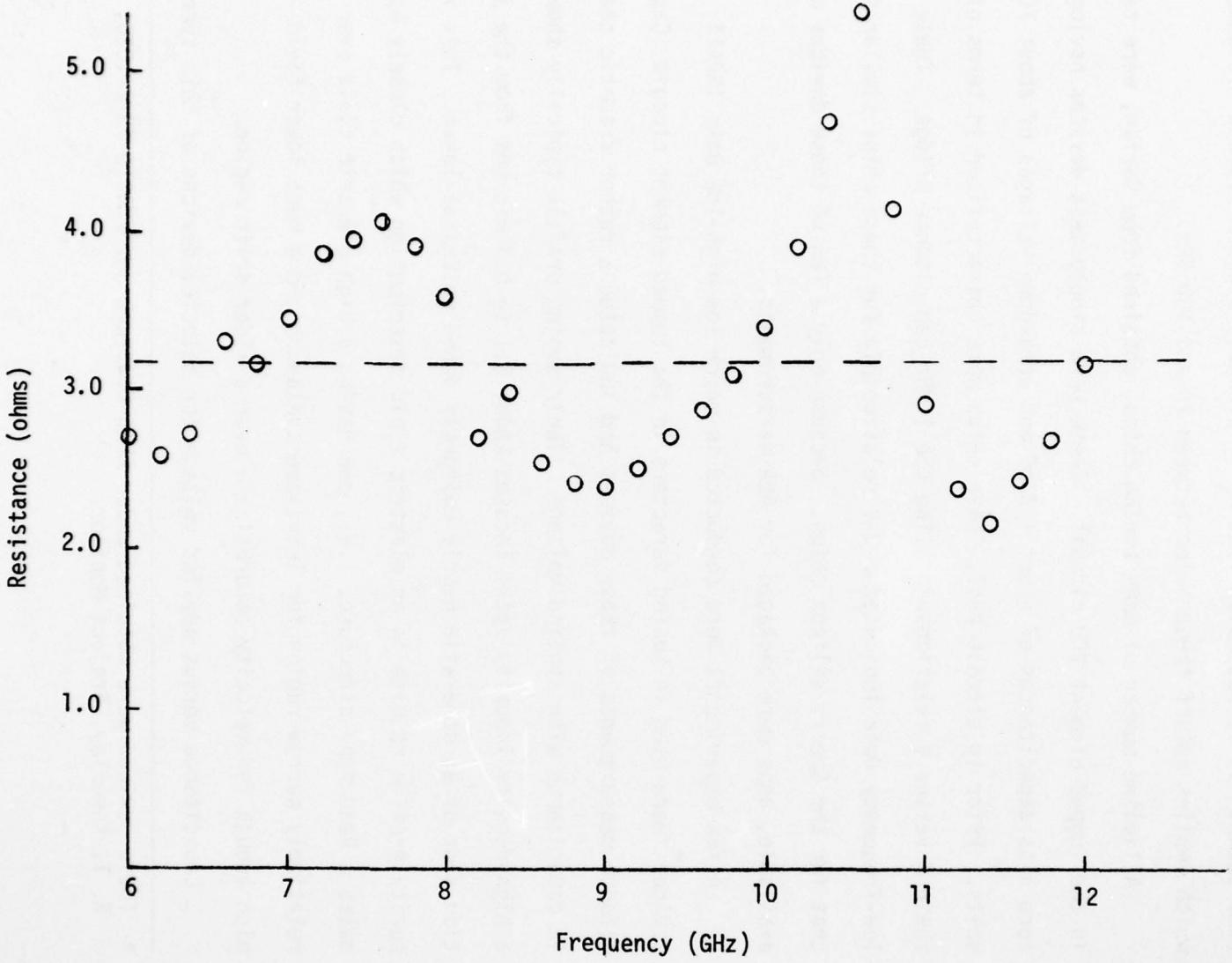

Fig. 6. Measured Resistance Versus Frequency for Silicon Varactor Biased to -1 Volt.

network analyzer data, the transformation from the reference plane to the chip was assumed lossless. The data of Figure 6 include some circuit losses and, consequently, the loss resistance of the chip itself will be less than that shown. It is estimated that R_s is probably between 2.0 and 3.0 ohms which implies cutoff frequencies between 70 and 100 GHz.

A limited number of GaAs tuning chips, obtained from Varian, were tested in the lumped element VCO circuit. These were single mesa devices having zero bias capacitances of about 1.3 pF and breakdown voltages of about 70 volts. Prior to circuit test, these chips were characterized in terms of their C versus V relationship using the 1 MHz capacitance bridge. These low-frequency data indicated a C-V relationship for these chips similar to that for the Sperry silicon chips. Because only a few of these devices were available, none were packaged for ANA measurements.

A few experiments were conducted in which low-high-low GaAs IMPATT devices* were used as tuning varactors in the lumped element circuit. Capacitance measurements of these devices had indicated a rather dramatic change in capacitance with applied voltage. Their doping profile typically shows a high-density impurity spike located about 0.1 to 0.3 microns from the junction side of an otherwise nearly uniformly doped epitaxial layer. This impurity profile results in an electric field distribution which closely approximates a Read type structure, i.e., one having a high electric field over a relatively narrow region for localized avalanche and a much lower field - yet high enough for velocity saturation - over a wider drift region.

Capacitance versus applied voltage for selected devices of this type

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* These devices were obtained under AFAL Contract No. F33615-75-C-1020, R. T. Kemerley, Project Monitor.

are shown in Figure 7. Also shown are two lines corresponding to idealized inverse square root and inverse square relationships. As seen, these devices are more nearly inverse square and better than a 10:1 change in capacitance is indicated for one device. Again, no microwave impedance data were obtained for these devices.

Automatic network analyzer data were also obtained for a number of Gunn devices which were on hand at the start of the program. Reduced Gunn chip impedance data for a C-band Varian device and a Ku-band Sperry device are shown in Figure 8. These small-signal impedance curves were difficult to interpret in terms of an equivalent circuit model. Even if an equivalent circuit valid over the frequency range of interest could be obtained, it would be of questionable value since the device operates under large-signal conditions as an oscillator. In the theoretical calculations of section 2.5, an equivalent circuit consisting of a -60 ohm negative resistor in parallel with a 0.3 pF capacitor was used to represent the Gunn device. This would correspond to a -30 ohm resistor in series with a capacitive reactance of -30 ohms at 9.0 GHz. This impedance is indicated on the curves for the Varian device.

2.2.2 Capacitor and Resistor Elements

The microstrip and lumped element VCO circuits described in a subsequent section required various miniature capacitors and resistors which were not available commercially.

Resistive elements in series with high Q ceramic chip capacitors were used in the bias circuit of the microstrip VCO to suppress low frequency oscillations. The resistors were of thin-film construction, etched from previously metallized chrome and gold on diamond substrates. A chrome

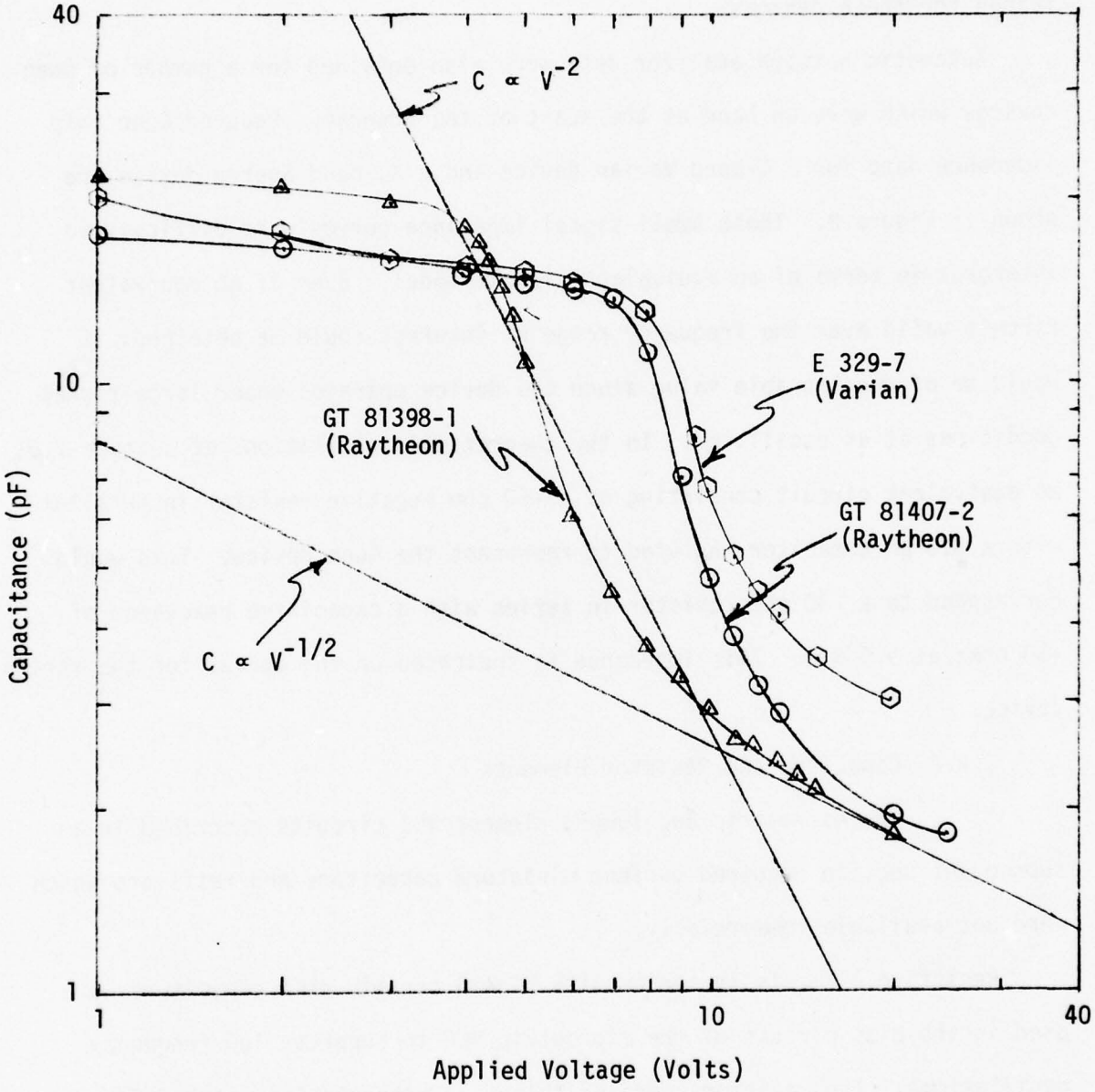
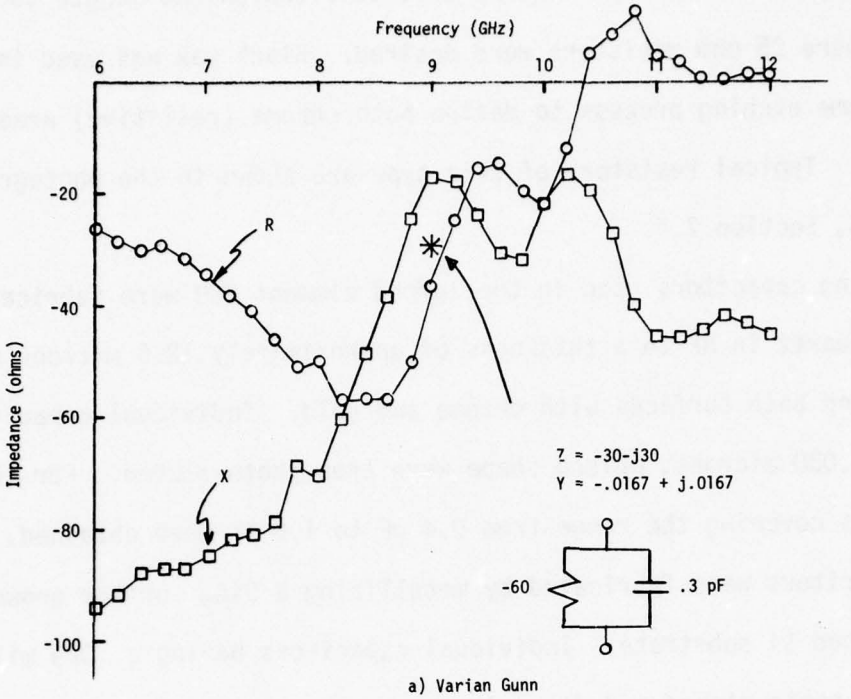
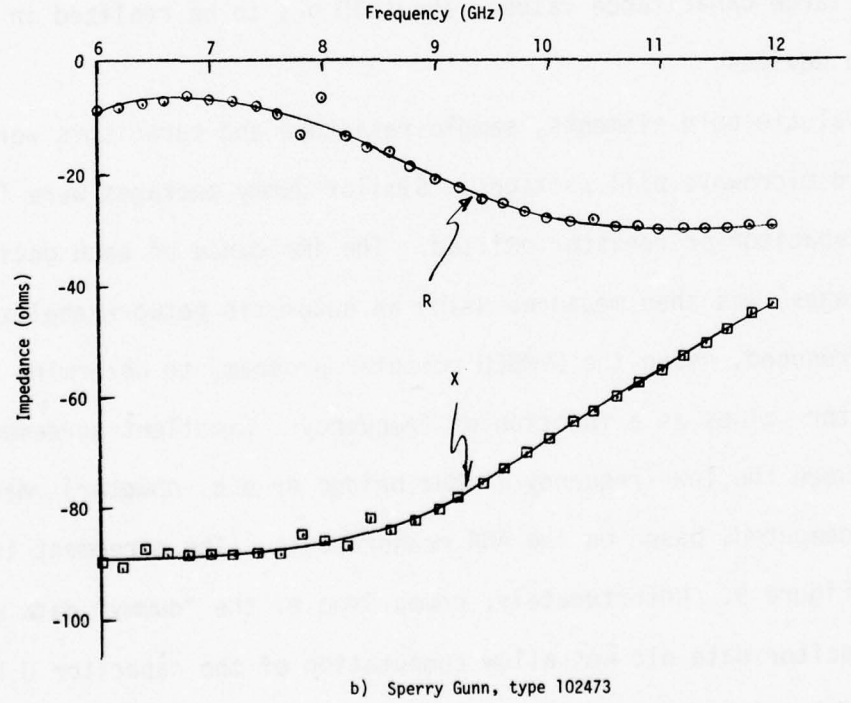


Fig. 7. Capacitance Versus Applied Voltage for Low-high-low Devices.



a) Varian Gunn



b) Sperry Gunn, type 102473

Fig. 8. Measured Impedance of Gunn Devices

resistivity of 100 ohms per square allowed a convenient length to width ratio of 1:4 where 25 ohm resistors were desired. Black wax was used in a two step gold-chrome etching process to define both chrome (resistive) areas and gold contacts. Typical resistors of this type are shown in the photographs of Figure 15, Section 2.4.

Tuning capacitors used in the lumped element VCO were fabricated by etching quartz in HF to a thickness of approximately 12.5 microns and then metallizing both surfaces with chrome and gold. Individual capacitors having a .015 x .030 microns, oblong shape were then photo-etched. For these chips, capacitors covering the range from 0.4 pF to 1.0 pF were obtained. R.F. by-pass capacitors were fabricated by metallizing a SiO_2 surface grown on a highly doped Si substrate. Individual capacitors having a .020 mil diameter were then photo-etched and diced in the usual manner. The thin SiO_2 layers permitted large capacitance values, about 30 pF, to be realized in relatively small size devices.

To evaluate both elements, sample resistors and capacitors were mounted in standard microwave pill packages. Similar dummy packages were fabricated with the capacitor or resistor omitted. The impedance of each device (including dummy packages) was then measured using an automatic network analyzer. These data were reduced, using the DEMBED computer program, to determine the resistor and capacitor values as a function of frequency. Excellent agreement was obtained between the low frequency (1 MHz bridge or d.c. ohmeter) measurements and those computed, based on the ANA measurements. The agreement is illustrated in Figure 9. Unfortunately, comparison of the "dummy" data and the quartz capacitor data did not allow computation of the capacitor Q because of its relatively high Q. Nevertheless, the data showed that the overall reflection

coefficient for the mounted capacitor was approximately the same as that for the dummy package, implying low capacitor loss.

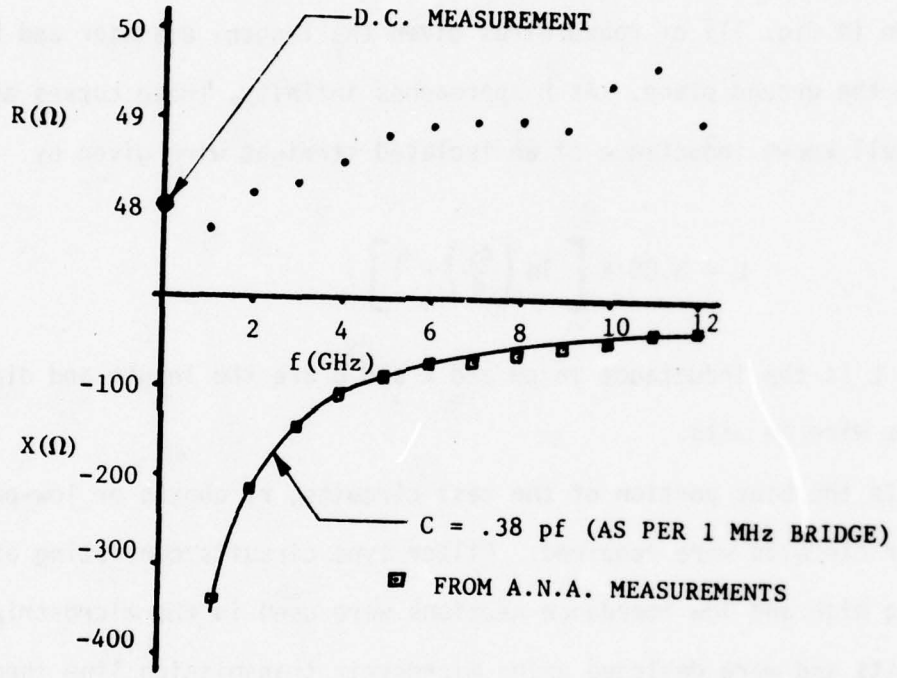


Fig. 9. Automatic Network Analyzer Data of Resistor and Capacitor Elements.

2.2.3 Inductors

In the rf portion of the test circuits, the varactor chip, the Gunn chip and the other circuit elements were connected together with various lengths of 1 mil gold wire. The inductance of each wire lead or conversely the distance between components for a desired inductance was estimated from the curves shown in Figure 10. These curves were generated using a computer program [2] which computes the inductance and loss resistance (shown in fig. 11) of round wires given the length, diameter and height above the ground plane. As h approaches infinity, these curves approach the well known inductance of an isolated straight wire given by

$$L = 5.08\,\ell\left[\ln\left(\frac{4\ell}{d}\right) - 1\right]$$

where L is the inductance in pH and ℓ and d are the length and diameter of the wire in mils.

In the bias portion of the test circuits, rf chokes or low-pass filter circuits were required. Filter type circuits consisting of alternating high and low impedance sections were used in the microstrip test circuits and were designed using microstrip transmission line theory. As the work progressed, however, the circuit elements became more lumped. An intermediate bias circuit consisted of a quarter/wavelength of high impedance line between the device to be biased and a 30 pF SiO_2 rf by-pass capacitor mounted to the ground plane. Bias supply connections were then made to the by-pass capacitors. Although the impedance shunting the rf circuit with this bias arrangement was not explicitly measured, calculations indicated it to be greater then 250 ohms from 6.0 GHz to

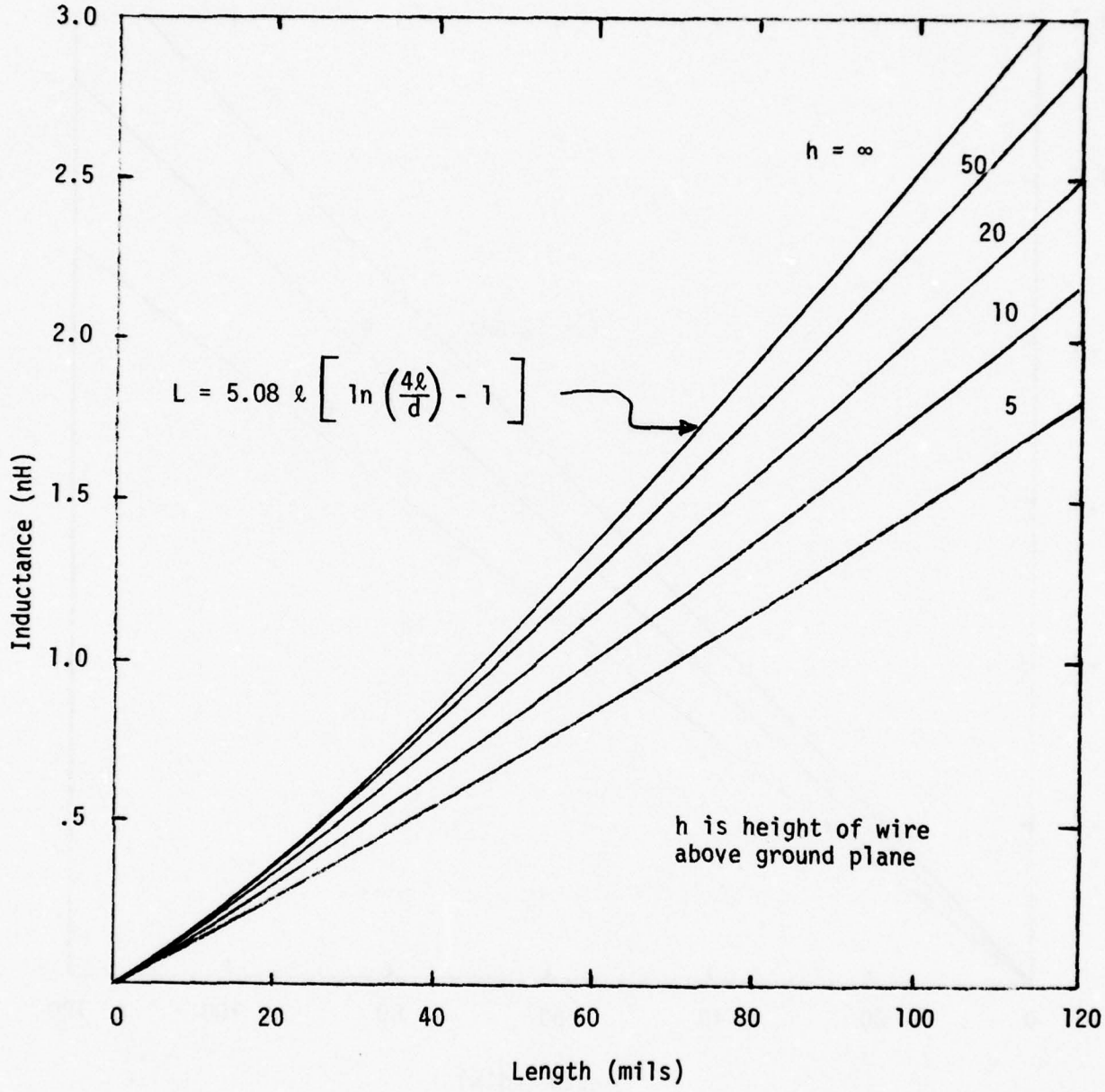


Fig. 10. Inductance of 1 mil Wire Above Ground Plane Versus Length of Wire.

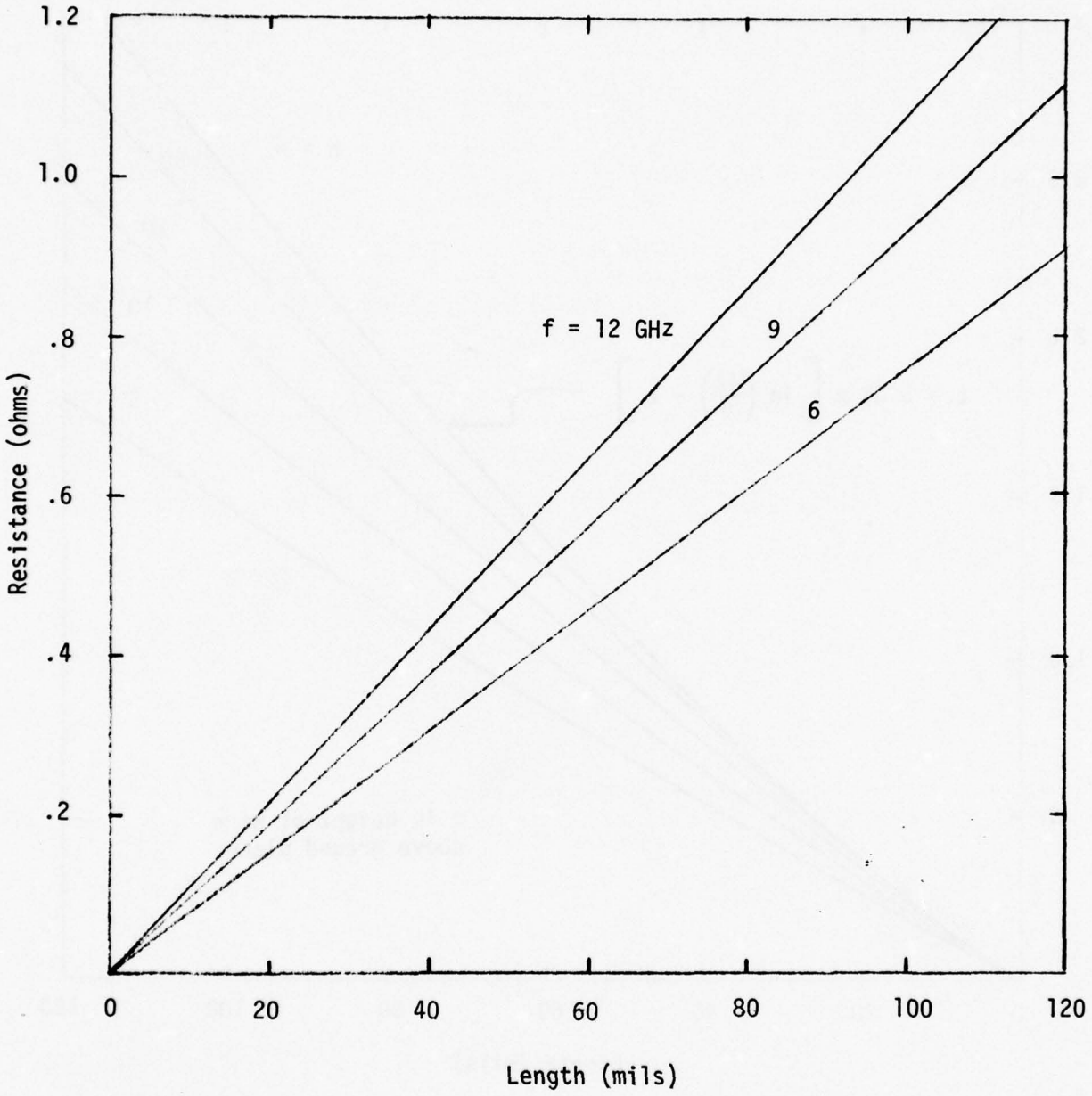


Fig. 11. Resistance of 1 mil Wire Versus Length for Selected Frequencies.

12.0 GHz. The quarter wavelength of wire was later replaced with "lumped" element inductors which were made by winding lengths of 1 mil wires into solenoids. These were wound on a 10 mil form and usually consisted of about 6 turns. These "coils" were adjusted empirically.

2.3 Coaxial Test Circuits

A number of experiments were conducted with a coaxial test circuit in which either an IMPATT or a Gunn chip was series connected to a varactor chip. Except for the additional circuit required to separately bias the two devices, this circuit had been used successfully to test both IMPATT and Gunn devices. The objectives of these experiments were to determine the frequency range over which the various IMPATT/Gunn - varactor combinations would operate and to establish matching requirements for later use. The idea here was to start with a circuit that was easily modeled, determine its overall characteristics when used as a VCO and from measured data deduce the characteristics and limitations of the various active device-varactor combinations.

The basic circuit is shown schematically in Figure 12 where discontinuity, corner and radial line capacitors and inductors are not shown for simplicity. The lumped portion of the circuit is mounted on a 30 x 30 x 20 mil diamond chip TC bonded to a 0.5 inch diameter copper slug which fits in the coaxial test structure. The active device (IMPATT or Gunn) chip and varactor chip are TC bonded to gold pads deposited on one face of the diamond and then connected electrically in series by the lead arrangement shown in Figure 13. The long lead wire (approximately a quarter wavelength long at 9 GHz) connecting the top of the chips leads around two quartz posts to an insulated bias wire which is fed through the copper slug to the outside of the coaxial test fixture.

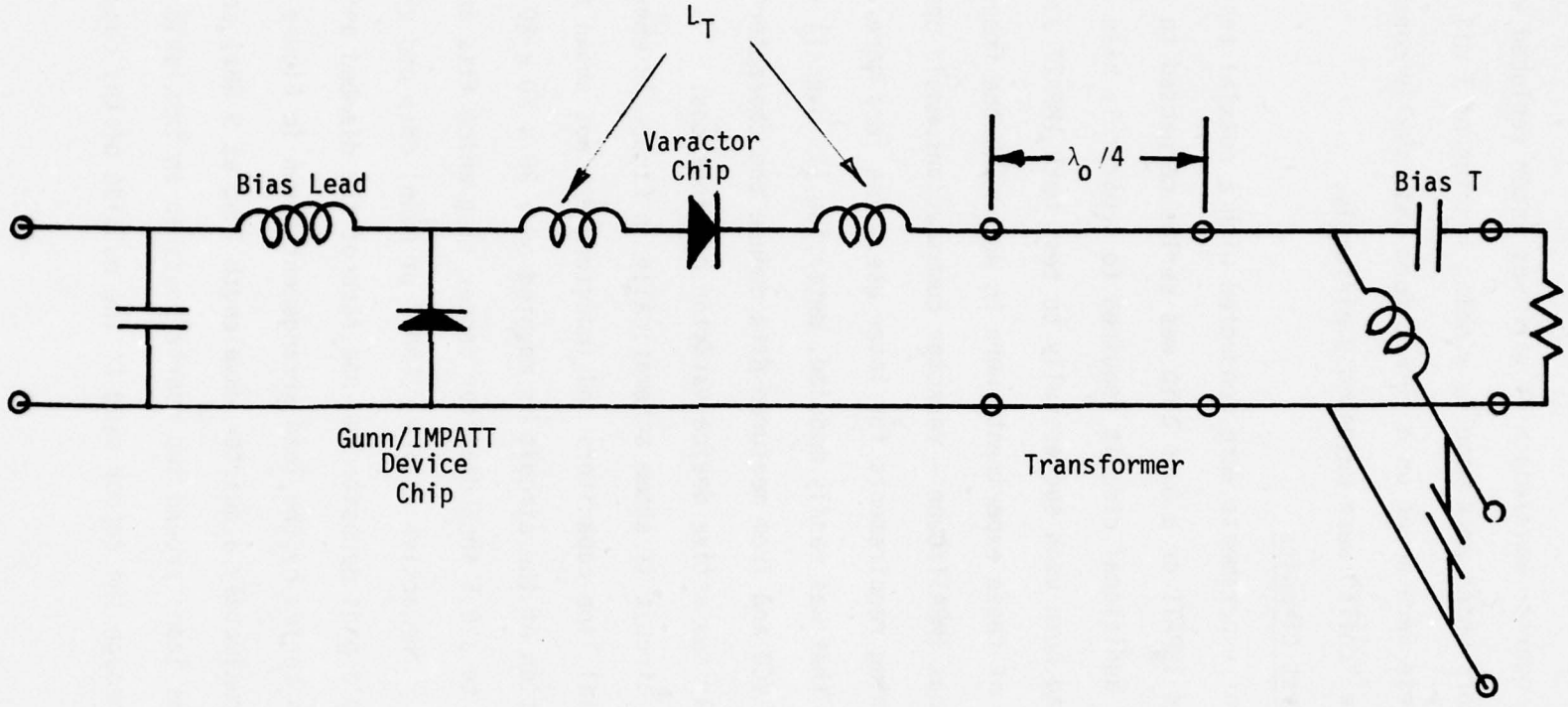


Fig. 12. Schematic of Coaxial VCO Circuit

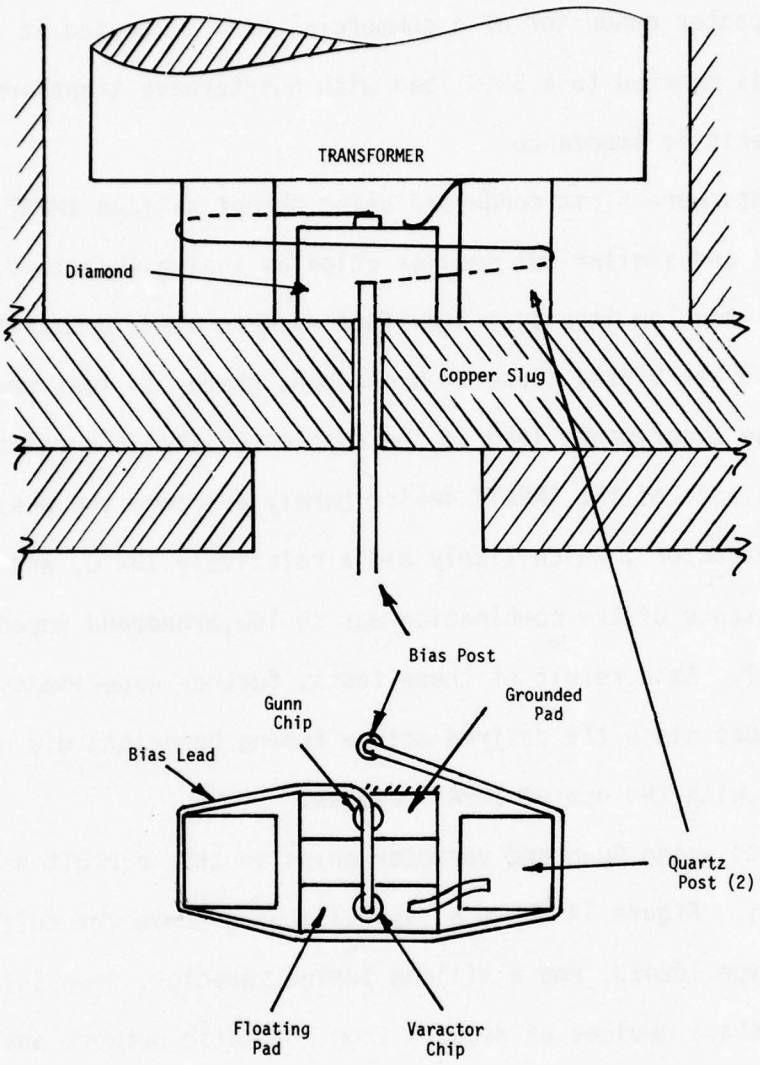


Fig. 13. Coaxial VCO Circuit

Bias is applied to the active device through the bias wire and the outside conductor of the test fixture. The varactor chip is biased through the bias wire and the center conductor of a commercial bias T located in the output line. This circuit is matched to a 50 Ω load with quarterwave transformers of appropriate characteristic impedance.

Experiments were first conducted using abrupt silicon IMPATT chips as active devices and similar but smaller chips as tuning varactors. Oscillations were obtained when low impedance transformers were used, primarily when the "varactor" chip was biased close to breakdown, where its loss resistance is minimum. These experiments lead to the conclusion that the relatively low negative resistance of the IMPATT device barely overcame the positive resistance of the "varactor", which likely had a relatively low Q, and that the net negative resistance of the combination was so low, broadband impedance matching was impractical. As a result of these tests, further experiments with IMPATTS were discontinued since the desired octave tuning bandwidth did not appear to be achieveable with the use of IMPATT diodes.

Experiments using Gunn and varactor chips in this circuit proved to be more successful. Figure 14 shows a typical tuning curve for this circuit using a Gunn chip, type 102473, and a silicon tuning varactor, type E-73-15. The impedances of these devices as deduced from automatic network analyzer data were given in Section 2.2.1. This tuning curve was obtained with the transformer having the largest characteristic impedance which was about 20 ohms. The circuit would not oscillate with a straight through section, i.e., 50 ohm load. This fact added some credibility to the measured impedance data for the

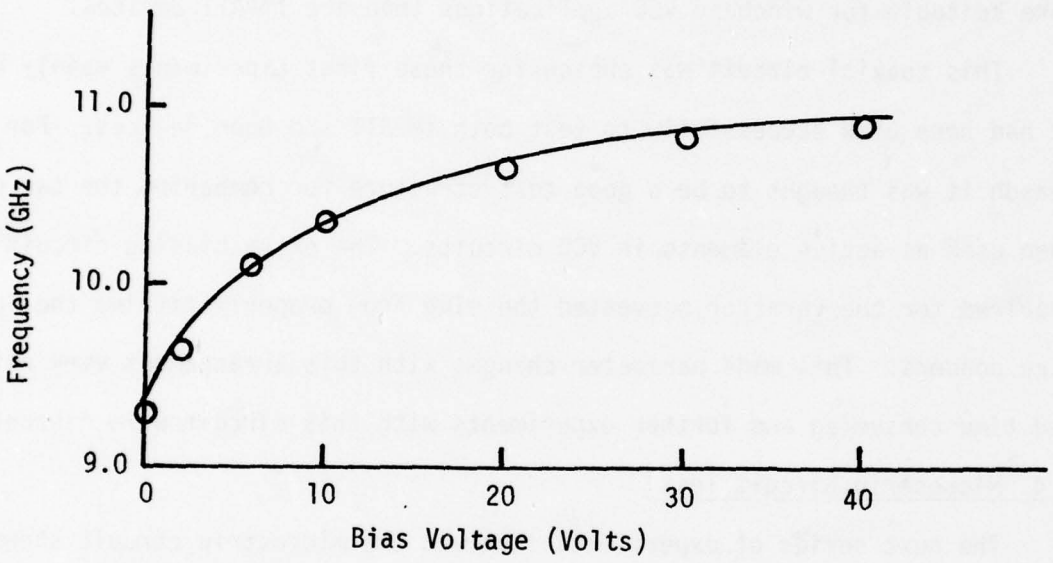


Fig. 14. Tuning Curve of Coaxial VCO Circuit

Gunn device. Although the tuning range was significantly less than expected, several factors observed with the Gunn experiment were encouraging.

- The circuit, as designed, oscillated in the frequency band of interest.
- The circuit tuned continuously with no frequency "hopping" or "glitches".

The experiment also added further to the consensus that Gunn devices are more suitable for wideband VCO applications than are IMPATT devices.

This coaxial circuit was chosen for these first experiments mainly because it had been used successfully to test both IMPATT and Gunn devices. For this reason it was thought to be a good test structure for comparing the two devices when used as active elements in VCO circuits. The extra biasing circuit required for the varactor prevented the slug from properly fitting the TC and wire bonders. This made parameter changes with this arrangement very difficult and time consuming and further experiments with this circuit were discontinued.

2.4 Microstrip Circuit Test

The next series of experiments involved the microstrip circuit shown in Figure 15. Although some of the components in this circuit are even less "lumped" than those in the circuit described in the previous section, experiments with this type circuit were thought necessary for several reasons. First, important objectives of this program were to evaluate the capabilities, advantages and limitations of lumped element VCOs and to compare their characteristics with those of distrubuted element VCOs. The vast differences in the measured small-signal impedance characteristics of the Gunn devices indicated that comparisons between circuits would be meaningful only if the same type Gunn device was used. Secondly, this circuit has been used by others[1] and would act as a

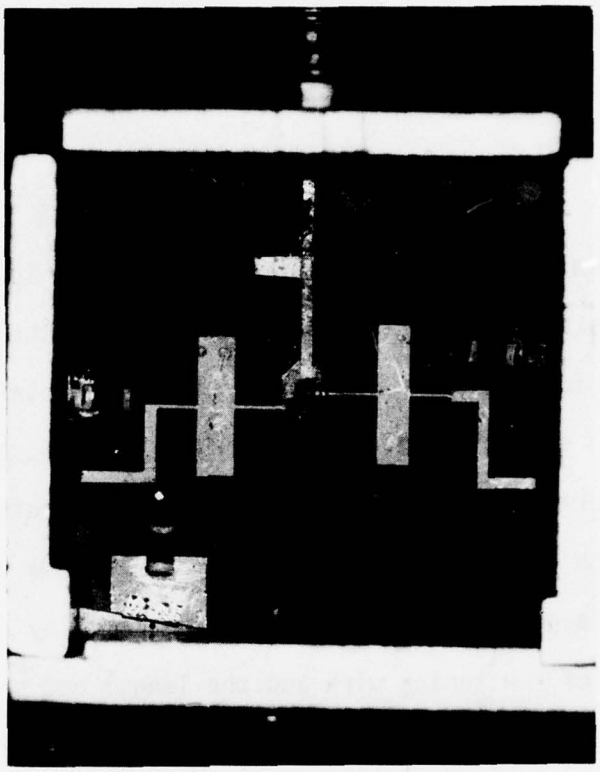


Fig. 15. Photograph of Microstrip VCO Circuit

suitable test structure for evaluating the Gunn and varactor devices.

The microstrip circuit tested initially consisted of a 20 ohm transformer (quarter wavelength at 9.0 GHz) for impedance matching, two low-pass bias filters made of alternating high and low impedance sections of quarter wavelength line, and varactor and Gunn chips connected in series. The microstrip circuit was constructed on a 26 mil thick alumina substrate. Reactive tuning was provided by an appropriate length of 1 mil wire connecting the transformer to the varactor Gunn chips.

The tuning and matching arrangement proved difficult to adjust and was replaced by an open stub which could be positioned along the output line (this arrangement is shown in Fig. 15). It was also found necessary to include series RC circuits in each bias circuit to inhibit low frequency oscillations.

A series of experiments were conducted with this circuit using Microwave Associates X-band Gunn chips and Sperry graduated multimesa varactor chips. The tuning range for a given varactor mesa was optimized by systematically adjusting the length of the tuning wire and the length and position of the open stub. The optimized tuning curve obtained with varactor mesas number 3, 4, and 5 are shown in Figure 16. The smallest of the mesas, number 3, yielded the largest tuning range, as expected from the computer simulations. The circuit tuned between 6.65 and 10.2 GHz with no frequency "hop" or "dead spots" for a total tuning range of 3.55 GHz or better than 42%.

The power, however, dropped from approximately 75 mW at zero volts varactor bias to 20 mW at 40 volts. Unfortunately, but not surprising, the wider tuning ranges are obtained at a sacrifice in power and power flatness.

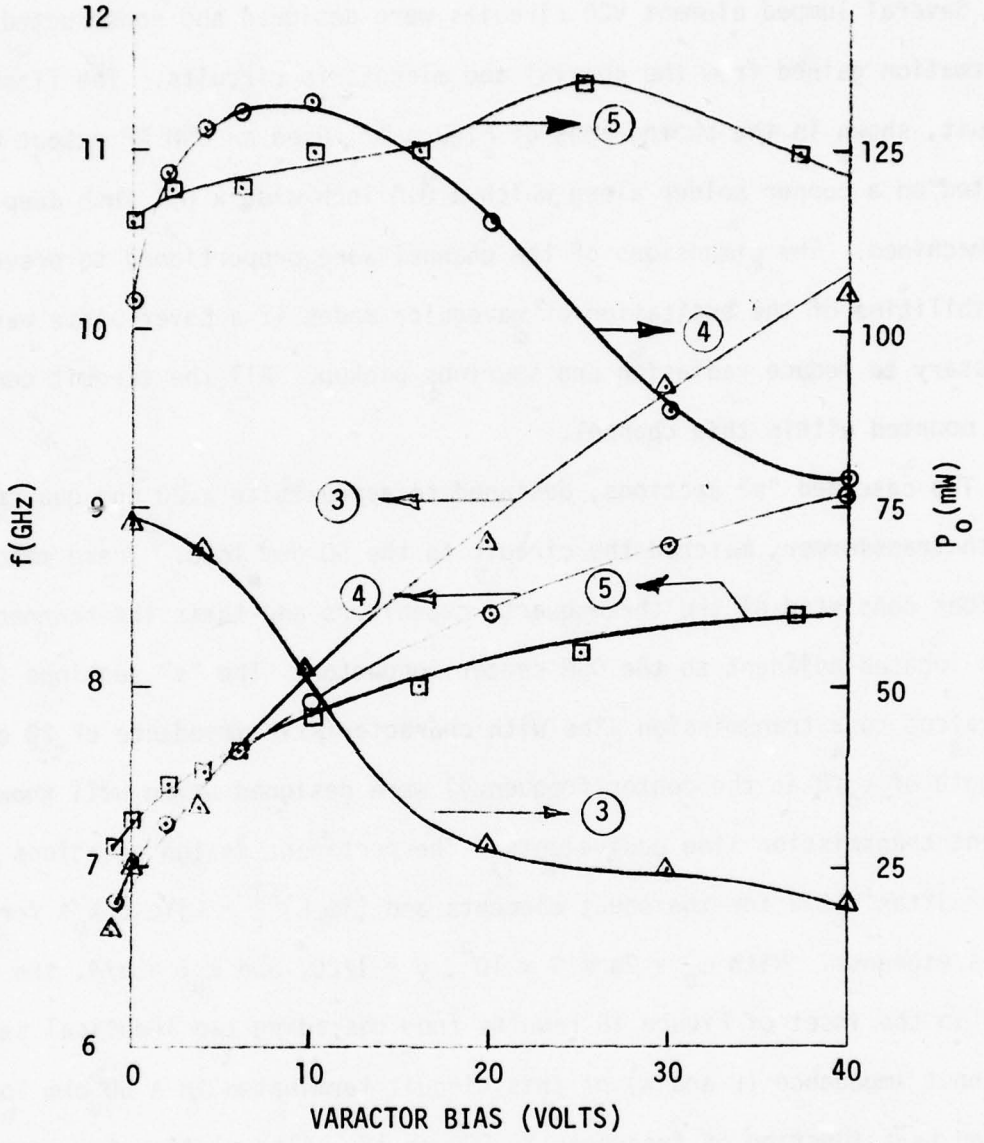
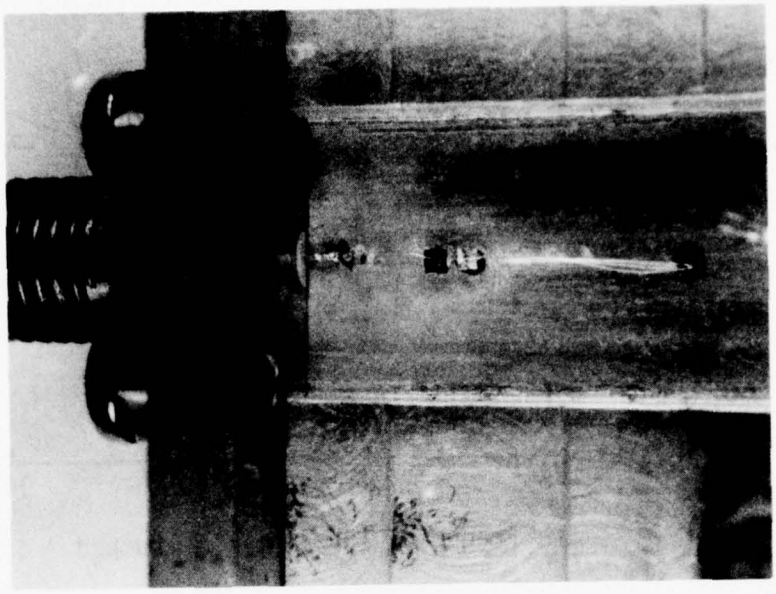


Fig. 16. Tuning Characteristics of Microstrip VCO for Different Size Varactor Mesas.

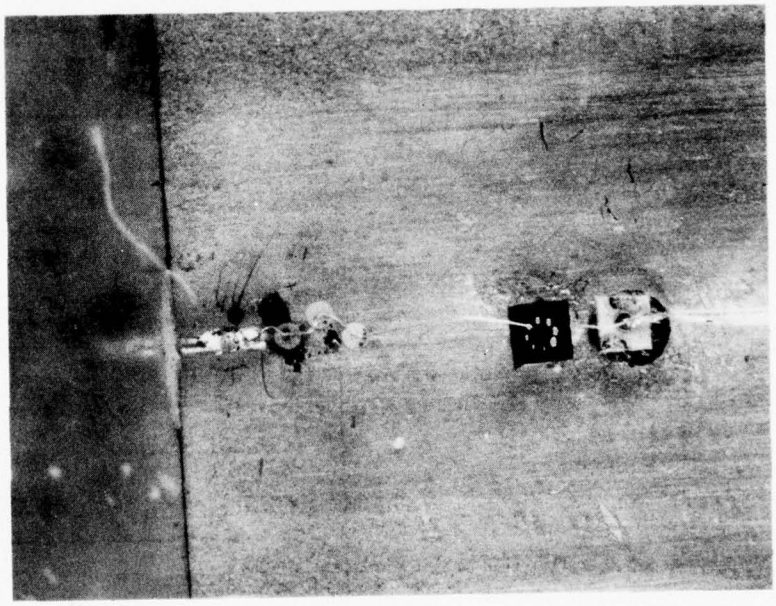
2.5 Lumped Element VCO

Several lumped element VCO circuits were designed and constructed using information gained from the coaxial and microstrip circuits. The first such circuit, shown in the photographs of Figure 17, used an OSM RF output connector mounted on a copper holder along which a 0.4 inch wide x 0.1 inch deep channel was machined. The dimensions of the channel were proportioned to prevent the possibilities of the excitation of waveguide modes if a cover plate was found necessary to reduce radiation and spurious pickup. All the circuit components were mounted within this channel.

Two cascaded "π" sections, designed to approximate a 20 ohm quarter wavelength transformer, matched the circuit to the 50 ohm load. These matching sections consisted of the three quartz capacitors and their interconnecting wires located adjacent to the OSM center conductor. The "π" sections (each equivalent to a transmission line with characteristic impedance of 20 ohms and a length of $\lambda_o/8$ at the center frequency) were designed using well known lumped element transmission line equivalents. The pertinent design equations are: $j\omega_o C = jY\tan k_o \ell/2$ for the shunt elements and $(j\omega_o L)^{-1} = -jY\csc k_o \ell$ for the series elements. With $\omega_o = 2\pi \times 9 \times 10^9$, $y = 1/20$, and $k_o \ell = \pi/4$, the circuit shown in the inset of Figure 18 results from cascading two identical sections. The input impedance (R and X) of this circuit terminated in a 50 ohm load is plotted as a function of frequency in Figure 18. Also plotted for comparison is the impedance of a 50 ohm load transformed through a 20 ohm transmission line whose length is a quarter wavelength at 9 GHz. Both circuits of course, transform the 50 ohm load to approximately 8 ohms real at the center frequency. For both circuits, the resistive parts of the impedances remain between 8 and



(a)



(b)

Fig. 17. Photographs of Lumped Element VCO.

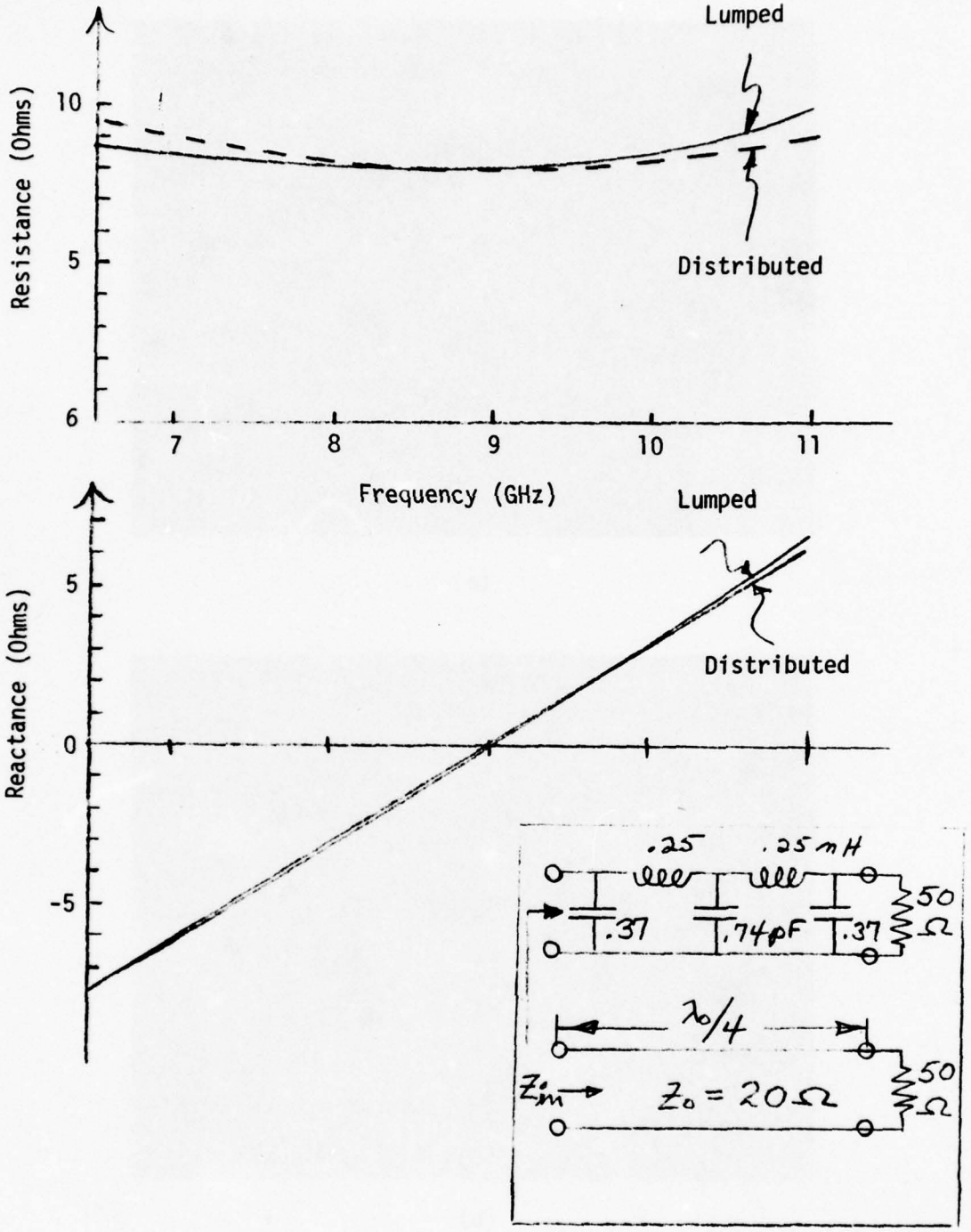


Fig. 18. Comparison of Lumped Element Matching Circuit with Quarter Wavelength Transformer (see inset).

10 ohms and the reactive parts are within a half ohm of each other at any frequency between 7 and 11 GHz.

Except for the matching and bias arrangements, the remainder of the circuit is identical to that used in the microstrip prototype, i.e., a grounded Gunn chip in series with a varactor chip insulated from ground. The Gunn-varactor combination is tuned to the center frequency by the inductance of a one mil wire of appropriate length. This wire also connects the Gunn-varactor circuit to the matching circuit.

Bias is applied to the Gunn chip via another length of wire (actually 4 one mil wires in parallel in order to carry the high Gunn currents) which leads to a SiO_2 30 pF RF bypass capacitor. Tuning voltage is applied to the varactor output via the Gunn bias lead and the output center conductor through a bias "T".

Typical frequency versus varactor voltage data using a number 3 mesa and a Microwave Associates Gunn device are shown in Figure 19. These data are plotted for three values of Gunn bias. As seen, the overall performance of the VCO circuits is somewhat dependent on Gunn bias. For a Gunn bias of 9.0 volts, the circuit tuned from 5.2 GHz at slight forward bias to 9.8 GHz at 40 volts reverse bias. This is an absolute tuning range of 4.6 GHz or better than 61%. The output power varied between 5 and 20 mw. When the Gunn bias was increased to 10.5 volts, the absolute tuning range tended to decrease and the circuit stopped oscillating for varactor voltages above 30 volts. When the Gunn was operated at 7.5 volts, the tuning slope, $\Delta f/\Delta v$, increased at the higher varactor voltages but the circuit stopped oscillating for varactor voltages below 5 volts. This behavior suggests that the circuit is optimally loaded in the sense of obtaining

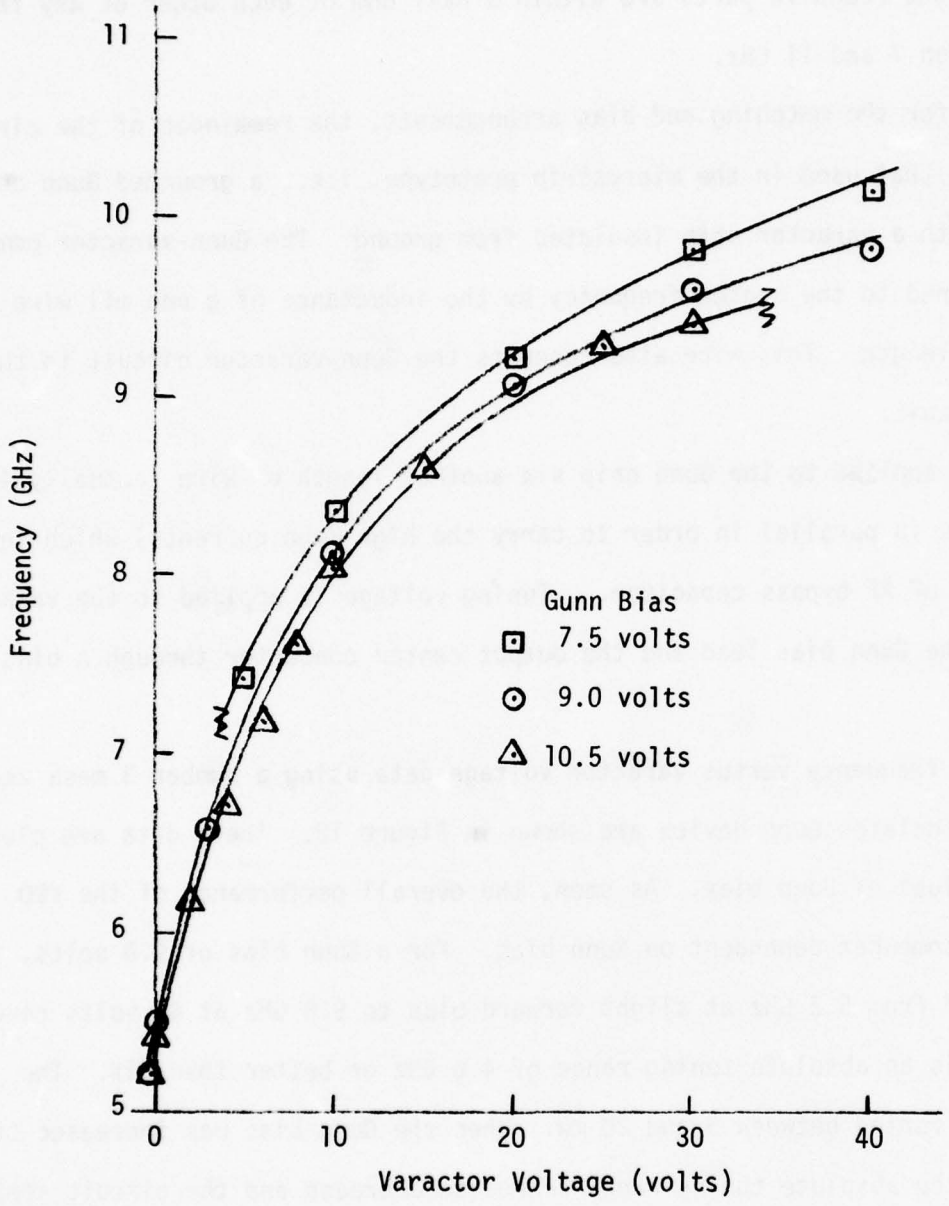


Figure 19. Tuning Curve for Lumped Element VCO.

maximum tuning for a Gunn bias of about 9.0 volts. For this condition, a tuning range of 4.0 GHz (5.5 to 9.5 GHz) was obtained for a change in varactor voltage of 30 volts (0.0 to 30.0 volts).

Computer simulations of the lumped element VCO were conducted using the circuit shown in fig. 20a as a model. The Gunn device was modeled as a -60 ohm resistor in parallel with a 0.3 pF capacitor as discussed in Section 2.2.1. Except for the varactor loss which was represented as a constant 1 ohm series resistor, the other elements were either measured or calculated using actual dimensions. The capacitance versus voltage relationship for the varactor was taken to be that measured previously for a number 3 mesa of the multimesa device. The curves of Figure 20b are the results of those evaluations and were to obtain a theoretical tuning curve. For this curve the frequency of oscillation was taken to be that frequency at which the negative of the reactance to the right of aa (see fig. 20a) was equal to the reactance to the left of aa. That is, the frequency of oscillation for a given value of varactor capacitance was determined by the intersection of the X_L curves with the $-X_R$ curve. The tuning curve thus obtained is plotted in Figure 21. The experimental data of Figure 18 are also plotted to show the correlation between experimental and theoretical results. Agreement is quite good considering the uncertainty in the model for the Gunn device.

It is well known that the parameters of the parallel equivalent Gunn model are dependent on frequency, bias voltage and load conditions. The one used represents the "best estimate" constant parameter model. The two dashed curves of fig. 20b represent calculated values of the reactance of the circuit to the left of aa for a tuning inductor of 1.6 nH and for a varactor capacitance variation between .66 and .145 pF. These lines indicate that a tuning range

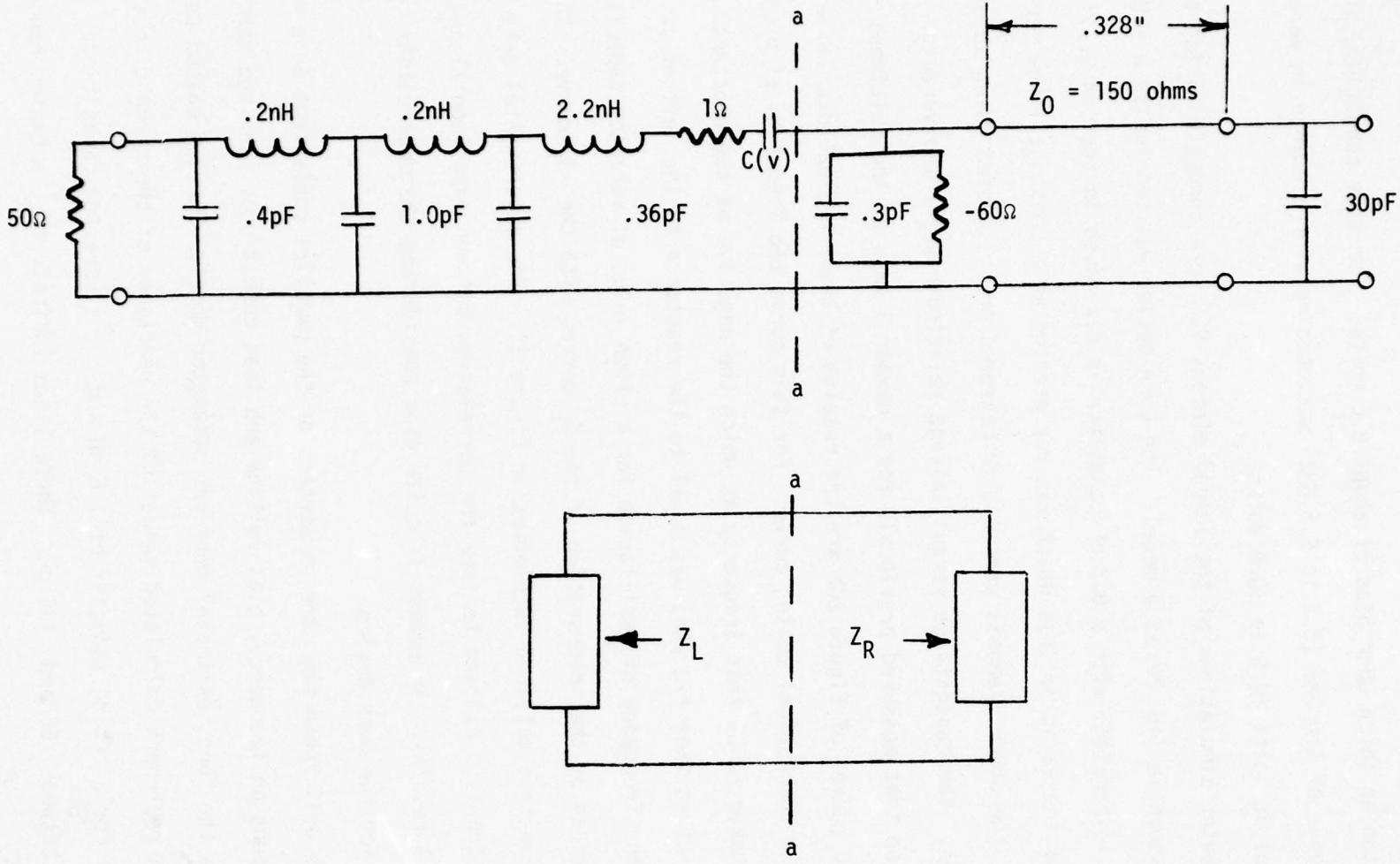


Figure 20a. Circuit Model of Lumped Element VCO.

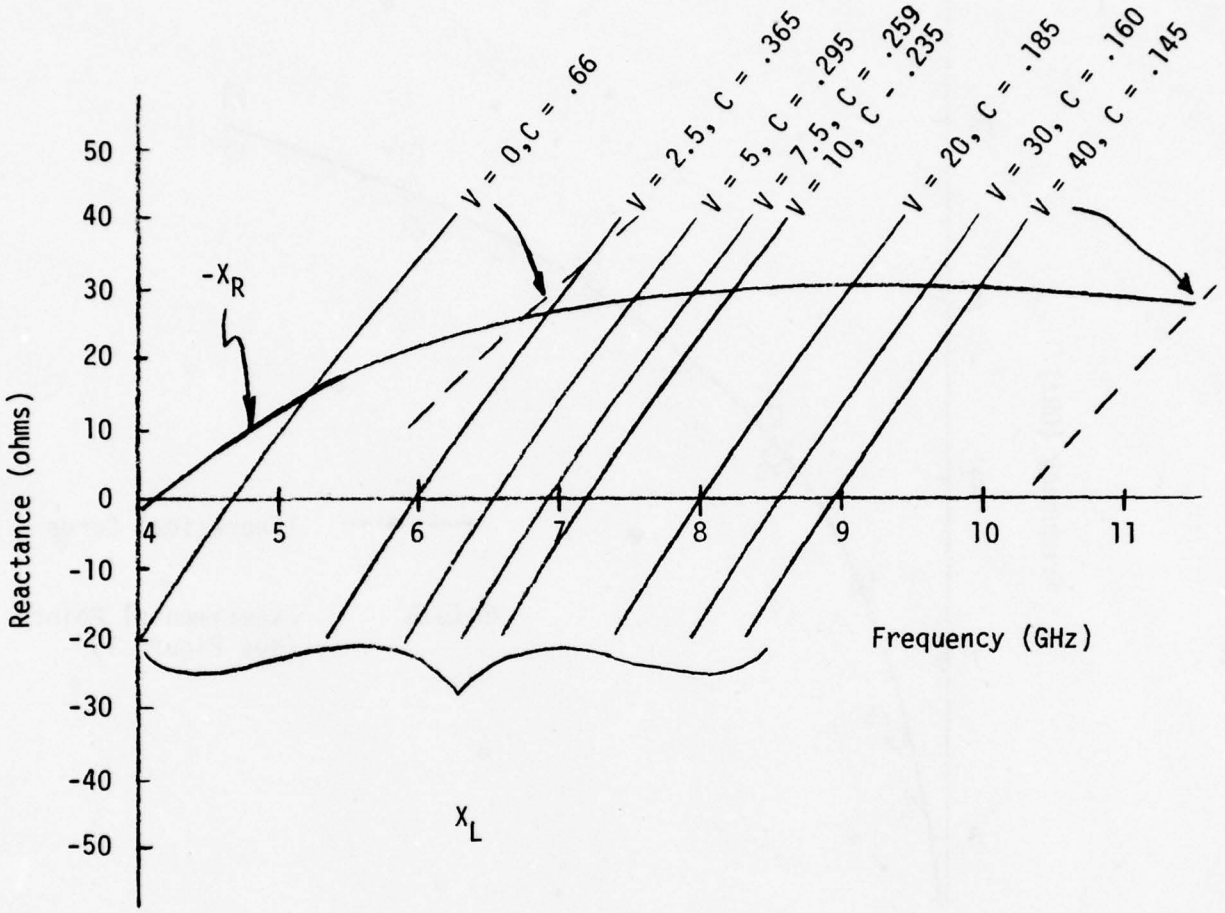


Fig. 20b. Reactance vs Frequency for Circuit of Fig. 20a

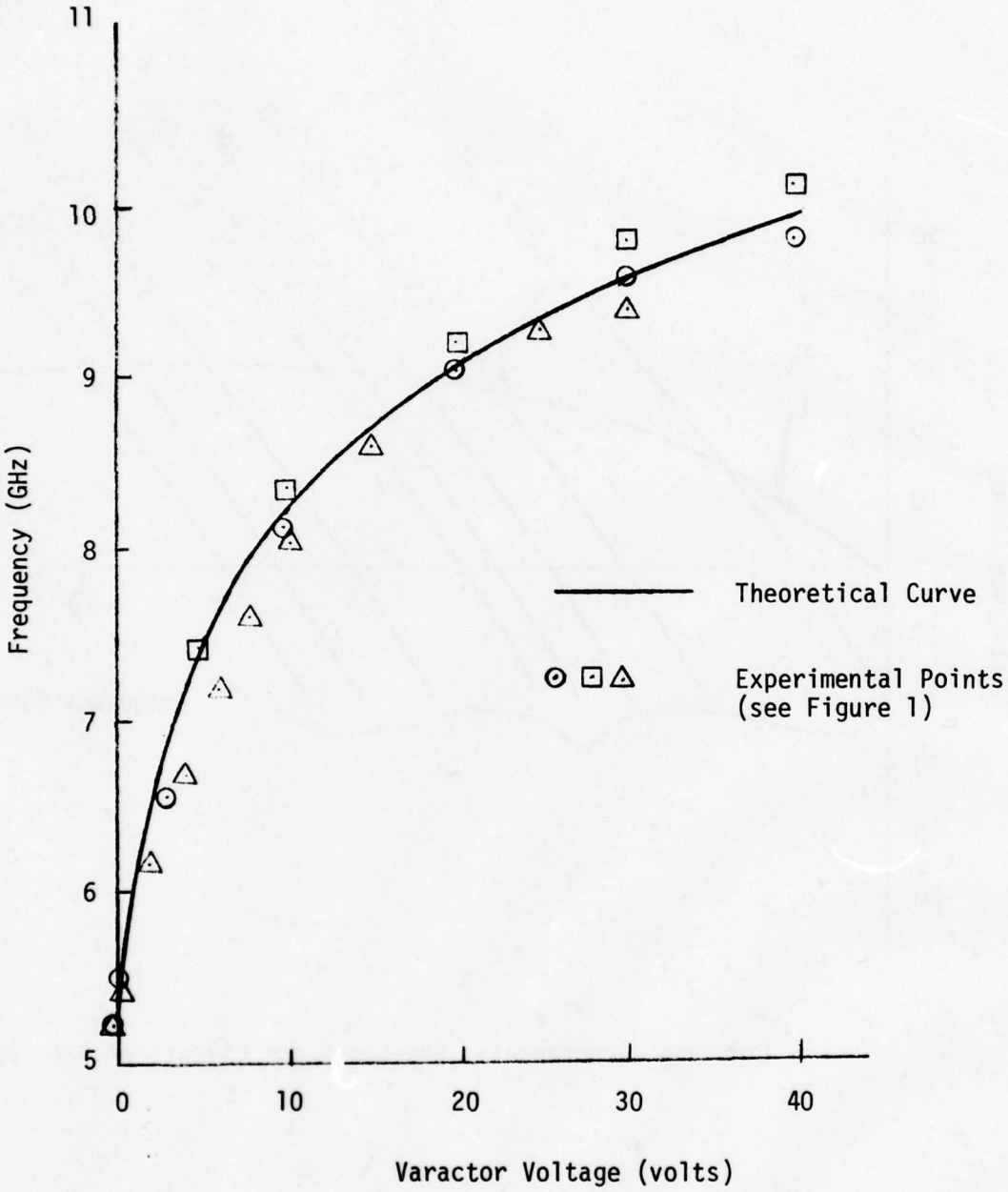


Fig. 21. Theoretical Tuning Curve for Lumped Element Circuit Shown in Fig. 20a

between 6.6 and 11.4 GHz could be obtained with slight modification of the circuit.

To check the repeatibility, another lumped element circuit was constructed and tested using new matching capacitors. A number 3 varactor mesa was again used, but the length of the inductive wire was decreased in an attempt to raise the center frequency to 9 GHz. The circuit tuned from 5.6 GHz to 10.9 GHz, a total tuning width of 5.3 GHz or 64%, with better than 10 mw across the band for tuning voltages between +.5 volts and -40 volts. Power output and tuning voltage versus frequency are shown in fig. 22 for a Gunn bias of 9 volts. As may be seen, a range of 58% is obtained for tuning voltages between 0 and -40 volts.

Varian GaAs tuning varactor chips were also tested in the lumped element VCO circuit, using Microwave Associates Gunn chips. These tuning varactors (70V breakdown) were characterized in terms of their C versus V relationship and found to be nearly abrupt junction devices with zero bias capacitance of about 1.3 pF. This was significantly larger than the 0.7 pF zero bias capacitance of the number 3 mesa used previously. Initial experiments were conducted in which unetched GaAs chips directly replaced the number 3 mesa with no other circuit changes.

As expected, the tuning bandwidth for these large capacitance chips was found to be relatively narrow (5.9 to 8.9 GHz) and the output power relatively high (~100 mW across most of the band). The spectrum was exceptionally clean across the entire tuning band. The varactor was then etched in the circuit a number of times in an effort to increase the tuning bandwidth and midband frequency. The intent here was to continue etching until the tuning range was

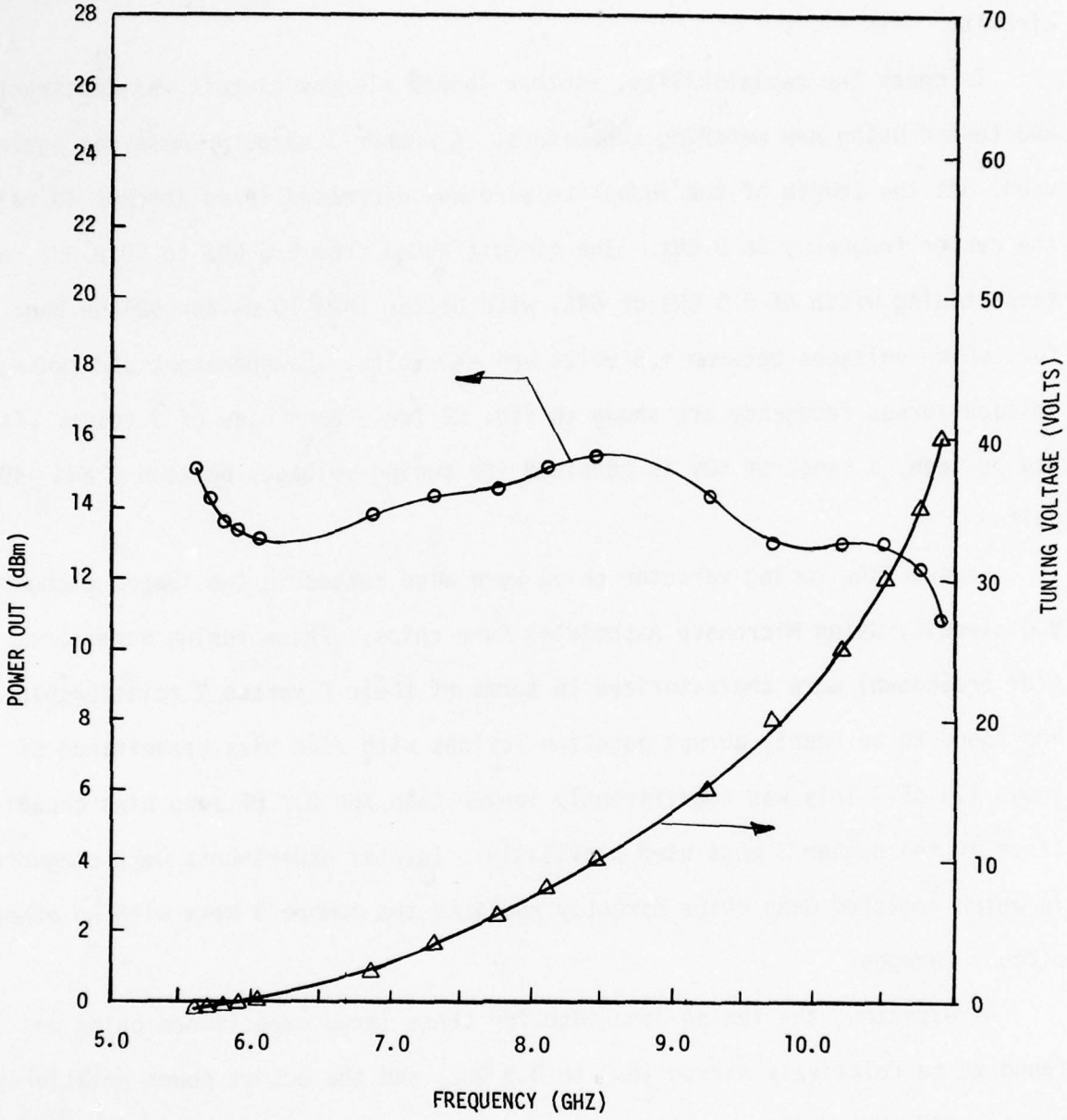


Fig. 22. Lumped Element VCO Data Using Microwave Associates Gunn and Sperry Varactor.

equal to that obtained with the number 3 silicon mesa varactor. As the tuning range approached that typically obtained with the silicon chip, the spectrum began to show noisy characteristics, especially at higher reverse varactor voltages (higher frequencies). This behavior had also been observed during initial experiments with the silicon varactor chips and was attributed to non-optimum matching of the load at the higher frequencies. It was felt, but not proved, that this was due to a rapid decrease in negative resistance of the Microwave Associate Gunn chips which was thought to occur at about 10 GHz.

The circuit was reconstructed, using an improved method of connection between the matching circuit and the OSM output connector. Prior to this change, a short 1 mil gold wire, TC bonded to the first matching capacitor, was soldered to the center conductor of the connector, as shown in Figure 17. For each circuit modification, this connection had to be first unsoldered and then resoldered. Repeated movement of the connection wires eventually resulted in damage to the matching capacitors. A 30 mil high quartz standoff metallized on opposite faces was mounted directly under the OSM center conductor. A gold foil connected to the first matching capacitor was then TC bonded to the top of the quartz post. When the OSM connector was mounted to the structure, its center conductor made pressure contact to the gold foil on the top of the quartz post, thereby eliminating the need for the solder operation. The varactor and Gunn bias circuits were also modified. The quarter wavelength bias wires were wound as coils as shown in Figure 23.

The results obtained with this circuit, using Varian Gunn and varactor chips, are shown in Figure 24. A tuning range between 7 and 11 GHz with greater than 10 mw was obtained with less than a 40 volt change in tuning voltage. For tuning voltages between +1 and -50 volts the bandwidth was 6 to 11.25 GHz or 61%.

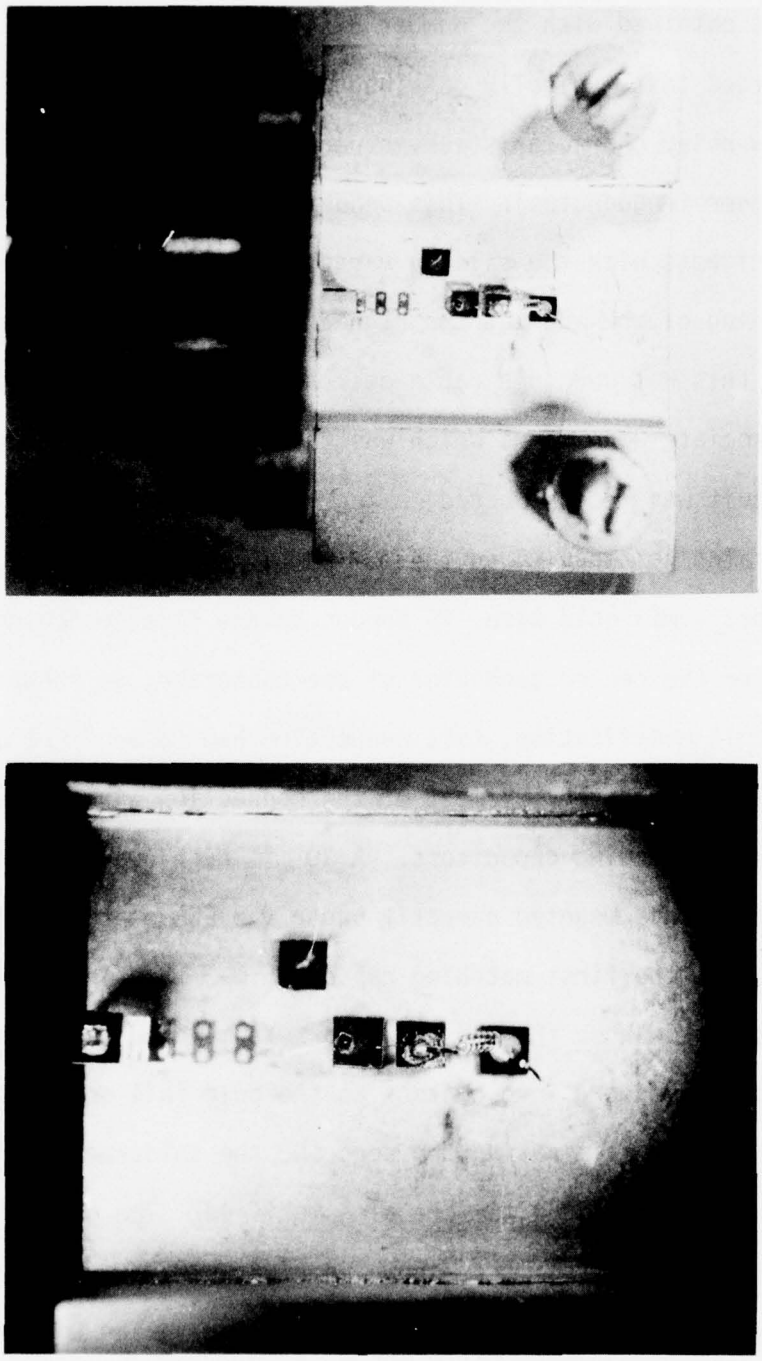


Figure 23. Photographs of Lumped Element Oscillator

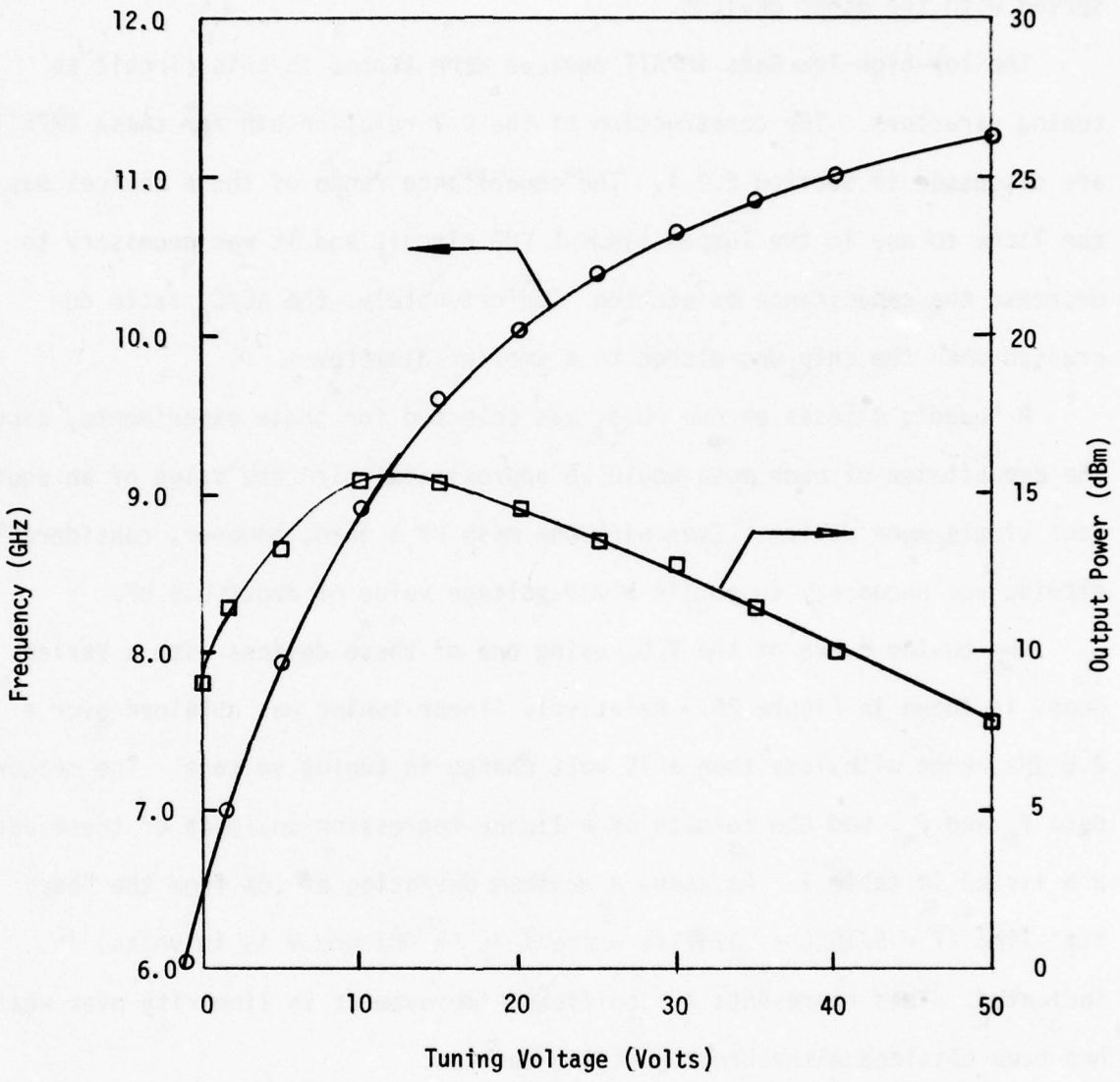


Fig. 24. Tuning curve of lumped element VCO using Varian Gunn and Varactor Chips

The spectrum over the entire tuning range was exceptionally clean and there was no evidence of the noisy region at the higher frequencies that was observed with the other devices.

The low-high-low GaAs IMPATT devices were tested in this circuit as tuning varactors. The construction of the C-V relationship for these IMPATTS are discussed in Section 2.2.1. The capacitance range of these devices was too large to use in the lumped element VCO circuit and it was necessary to decrease the capacitance by etching. Unfortunately, the $\Delta C/C_o$ ratio decreased when the chip was etched to a smaller diameter.

A "quad", 4 mesas on one chip, was selected for these experiments, since the capacitance of each mesa would be approximately 1/4 the value of an equivalent single mesa device. Even with one mesa of a quad, however, considerable etching was necessary to obtain a mid-voltage value of about 0.5 pF.

The tuning curve of the VCO, using one of these devices with a Varian Gunn, is shown in Figure 25. Relatively linear tuning was obtained over a 2.5 GHz range with less than a 15 volt change in tuning voltage. The measured data V_m and F_m, and the results of a linear regression analysis of these data are listed in table 1. As seen, a maximum deviation of .6% from the "best fit" line ($\overline{f}$ = 5/1086 + .17577V, where $\overline{f}$ is in GHz and V is in volts) is indicated. This represents a significant improvement in linearity over what has been obtained with abrupt junction devices.

Additional experiments were conducted using MA Gunns and low-high-low IMPATTS as tuning varactors. Since these Gunn chips did not operate well above approximately 9.5 GHz in the lumped element circuit, wide tuning ranges were not expected. The main objective of these experiments was to check the linearity and reproducibility of previous experiments using a different type Gunn

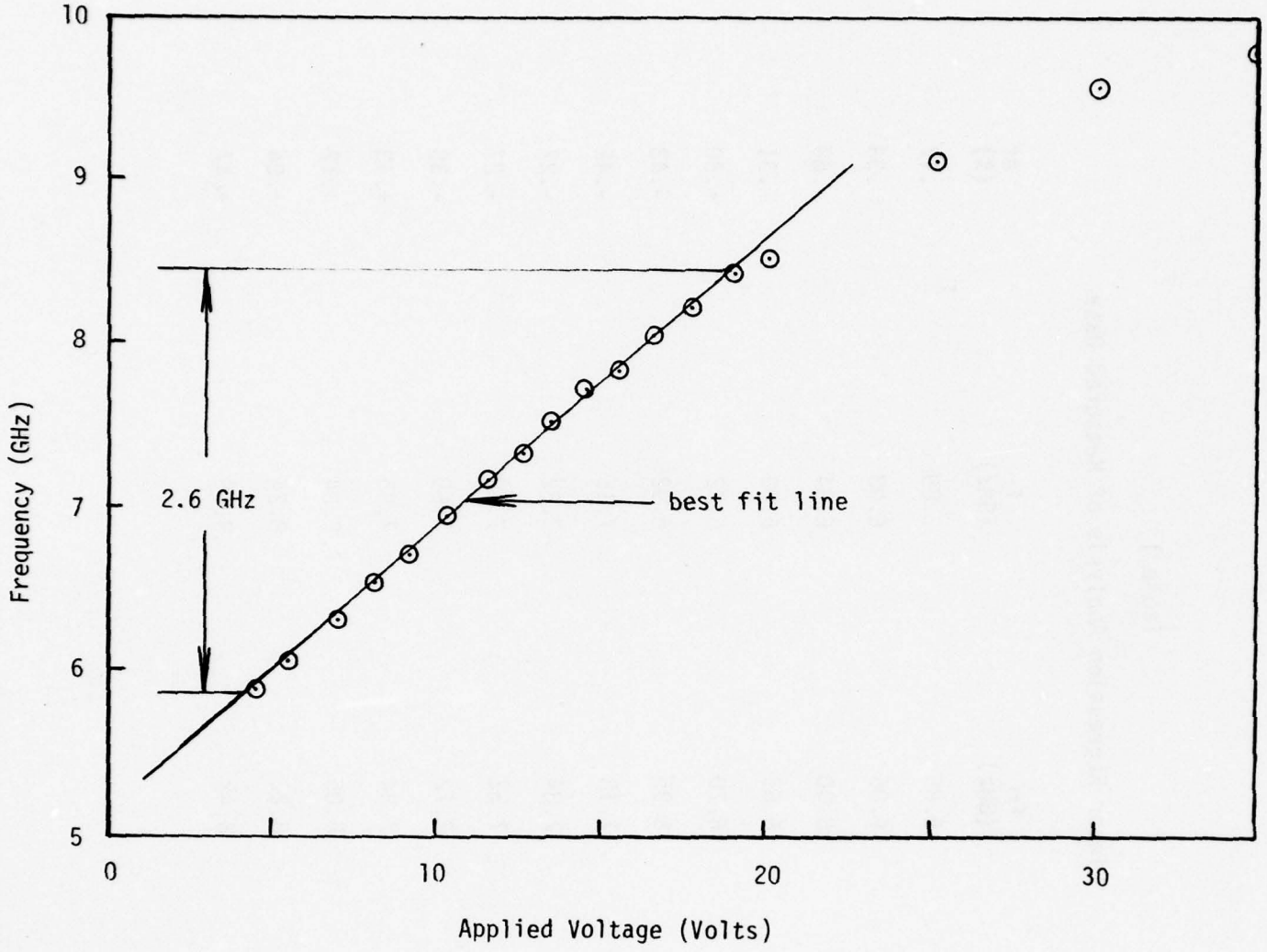


Fig. 25. Tuning Curve of VCO Using Low-High-Low GaAs IMPATT Diode as Tuning Varactor

Table 1

Linear Regression Analysis of Measured Data

Vm (volts)	Fm (GHz)	$\bar{f}$ (GHz)	Δf (%)
4.45	5.88	5.89	.17
5.50	6.06	6.08	.33
7.00	6.30	6.34	.63
8.10	6.55	6.53	.31
9.15	6.70	6.72	+.30
10.31	6.95	6.92	-.43
11.61	7.18	7.15	-.42
12.57	7.34	7.32	-.27
13.61	7.52	7.50	-.27
14.69	7.72	7.69	-.39
15.61	7.84	7.85	+.13
16.70	8.05	8.04	-.12
17.80	8.22	8.24	+.24
19.08	8.42	8.46	+.47

device and circuit. The matching portion of the circuit was modified by replacing the two "π" sections by a simple "L" section consisting of a 0.9 pF $A\ell_2O_3$ capacitor and a slightly longer lead wire to the varactor. The other portion of the circuit remained as described in previous reports.

Relatively clean oscillations were obtained from approximately 8 to 9 GHz with the spectrum showing the usual "fuzzy" characteristics at frequencies above 9 GHz. The circuit would not oscillate for tuning voltages below about 6 volts indicating that the load was improperly matched at the lower frequencies. Consequently, two additional 0.9 pF capacitors were mounted alongside the original one. With two of the matching capacitors in parallel, the circuit tuned from about 7 GHz to 9.3 GHz at which point the spectrum became noisy. A significant hop in frequency occurred for a tuning voltage between 8 and 9 volts; but between 4 and 8 volts, the circuit was well behaved and exhibited excellent tuning linearity.

Data recorded from the spectrum analyzer frequency dial and from a multi-meter used to monitor tuning voltage indicated a maximum deviation of $\pm$ 0.25% from a "best fit" line over a 1 GHz band for a 4 volt change in tuning voltage. The output power over this range was 13.8 dbm $\pm$ 0.5 db.

Since this tuning deviation was within what one would expect from measurement accuracy, a waveguide frequency meter and a digital voltmeter was incorporated in the test set up. In an attempt to eliminate the frequency hop, the other matching capacitor was connected, thereby placing three 0.9 pF capacitors in parallel across the load. It should be noted here that the physical dimensions of the three capacitors are appreciable compared to a quarter wavelength and can no longer be considered lumped.

The additional capacitor eliminated the frequency hop; however, the

spectrum showed sidebands similar to a frequency modulated signal when tuned to approximately 7.6 GHz. It was felt that this behavior was caused by a "loop" in circuit impedance and could be eliminated if this method of coupling proved otherwise successful. When data points about this instability were included, the maximum deviation was $\pm$ .5% over a 1.9 GHz range with a 7 volt change in tuning voltage. By neglecting two data points about the instability (total of eight data points) the maximum deviation from the best "fit line" determined from the remaining points was less than $\pm$ 0.2% over the 1.7 GHz range (6.9 to 8.6 GHz). This is close to that expected from the relative accuracy of the voltage readings of $\pm$ .005 volt. The overall accuracy of the frequency meter is given by the manufacturer as $\pm$ .17%. No indication of the relative accuracy is available.

Although inconclusive, these and previous tests indicate quite good tuning linearity can be obtained using low-high-low devices as tuning elements. It should be kept in mind, however, that the increased change in capacitance for a given change in voltage, which these devices exhibit, will detrimentally effect other oscillator characteristics. For example, the FM noise properties are expected to degrade as the tuning sensitivity increases.

The set of photographs of Figure 26 show the spectrum of a VCO operated at 10 GHz and modulated by a 50 MHz signal. During these experiments, Varian Gunn and varactor chips were used. Although the spectrum indicates rather good modulation characteristics, the oscillator was operating under conditions where the power-frequency curve was relatively flat and the frequency-voltage curve was relatively linear. Under other operating conditions, the modulation characteristics degraded somewhat as evidenced by the lack of symmetry and relative magnitudes of the spectral components. The main object of these

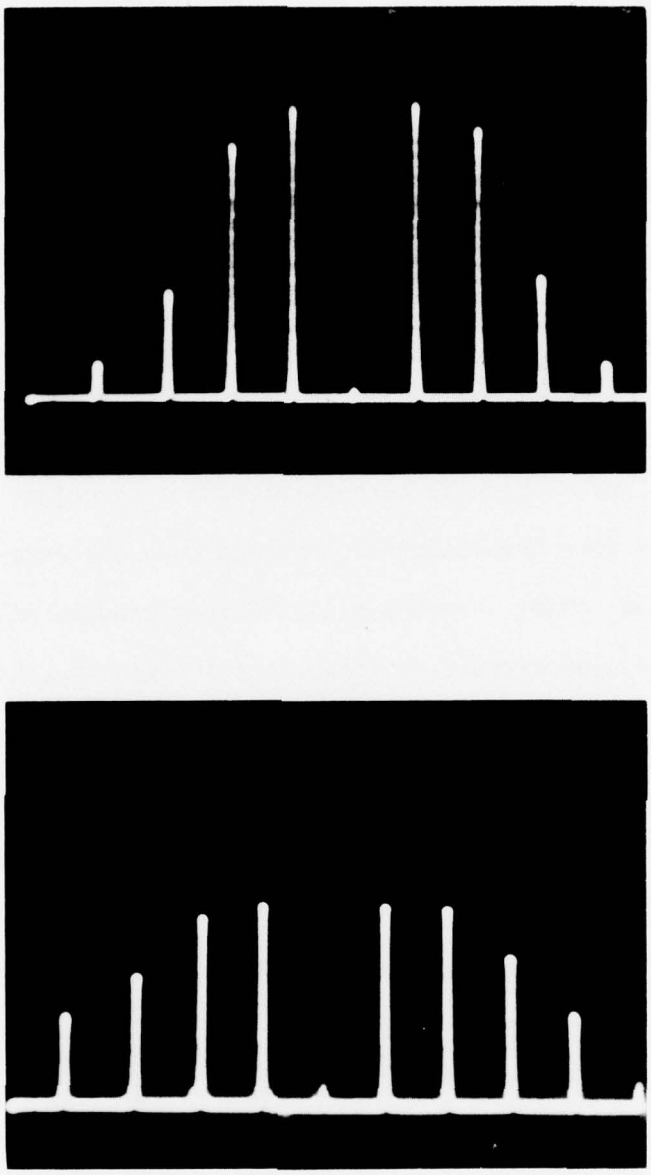


Fig. 26. Spectrum of VCO Modulated at 50 MHz rate. Horizontal scale ~ 50 MHz/cm. Vertical Scale a) linear b) log.

experiments was to demonstrate the high modulation rate capability of the VCO. The modulating source was an HP 606A signal generator capable of supplying 3V across a 50 ohm load at frequencies up to 65 MHz, but high modulation indices could not be obtained due to the sources limited output voltage. Nonetheless, these experiments and theoretical calculations indicate that the VCO is capable of being modulated at rates well in excess of 100 MHz.

2.6 PLANAR DEVICE TESTS

Planar Gunn devices, developed on this program and described in subsequent sections, were tested in various microwave circuits.

After chips were developed which showed Gunn characteristics on a curve tracer, individual chips were encapsulated in microwave pill packages and tested in a waveguide circuit designed to offer wide matching and reactive tuning capabilities. In general, the planar Gunn chips behaved similar to their conventional counterparts in that, as the bias voltage was increased, low-frequency, non-monochromatic signals occurred just past threshold current. As bias voltage was further increased, coherent oscillations would set in with the low-frequency signals disappearing. Results of these initial tests are summarized in the spectral photograph of Figure 27. Operating characteristics were obtained for various circuit tuning and Gunn bias conditions. The best results obtained with the planar devices in the waveguide circuit are tabulated below:

P_o = 5 mW
f_o = 6.8 GHz
V_G = 8.5 volts @ 110 mA

It was noted during these tests, however, that the circuit could be adjusted to yield significant output power only at certain frequencies.

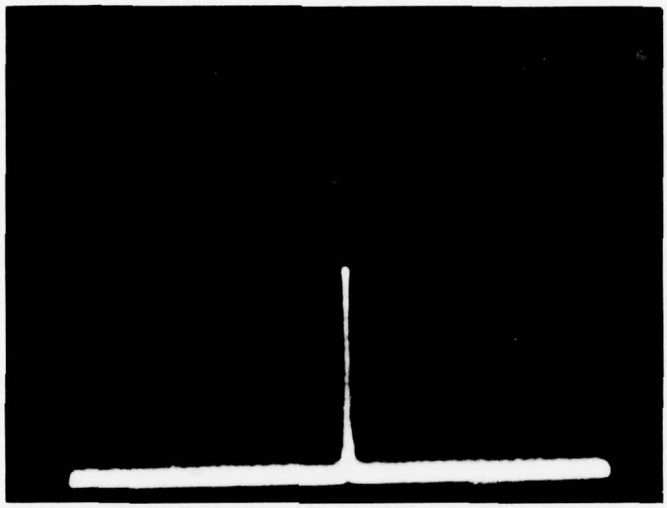


Fig. 27. Spectrum Photograph of Oscillations Obtained with Planar Gunn Devices. P_o = 1 mW, f_o = 11.8 GHz, V_G = 8.5 volts, and I_g = 110 mA.

One of the encapsulated planar Gunn chips was then tested in the coaxial test circuit described in Section 2.3. This circuit had been used successfully to test conventional Gunn chips during the first phase of the program. Since only a Gunn chip was involved in this test, the quarter wave biasing circuit shown in Figure 13 was not required. Rather a commercial bias T, placed in the output line, was used to supply Gunn bias. The circuit and the planar Gunn oscillated between 2.0 GHz and 2.5 GHz, depending upon bias voltage. Relatively strong harmonics extending into Ku-band were observed.

The low-frequency oscillations and strong harmonics observed with the coaxial circuit suggests the possibility that harmonic outputs were being observed and optimized during the waveguide tests. The fact that the waveguide results were relatively insensitive to circuit tuning lends support to this possibility.

Other r.f. tests on the planar Gunn chips were performed in lumped element circuits using Si tuning varactors. Circuits similar to those described in Section 2.5 also oscillated at significantly lower frequencies with the planar Gunn chips than with the conventional chips. Typically, lumped circuits with the planar chips oscillated between 2 GHz and 4 GHz with about 15 mW output power and could be electronically tuned with the number 3 silicon varactors over a bandwidth of about 25%. Relatively strong harmonics were also observed with these circuits. The magnitudes of the harmonics were relatively insensitive to varactor bias. Attempts to increase the operating frequency to X-band by circuit changes were unsuccessful.

A new planar Gunn-varactor (pGv) device was developed where the length of the active region of the Gunn was reduced in a further attempt to increase the operating frequency. A number of chips were obtained in which both the

Gunn and varactor looked acceptable from capacitor bridge - curve tracer measurements. A number of these chips were mounted and tested in the lumped element circuit used successfully with conventional chips. In these tests, the pGv simply replaced the individual Gunn and varactor chips. The rest of the circuit was essentially identical to that used with the conventional chips. The shorter distance between Gunn metallizations (7 microns vs 10 microns) and the smaller zero bias capacitance of the planar varactor (~ 1/3 that of the silicon varactors) was expected to increase the frequency of operation. Instead, the circuit continued to operate in the 2 GHz to 4 GHz range, but at a reduced power level (several milliwatts).

Circuit changes were attempted in hopes of increasing the frequency of operation. It was reasoned that the impedance level of the planar Gunn was higher than that of the conventional Gunn due to differences in area. This, in addition to the fact that the impedance level of the varactor increased by about a factor of three, was conceivably causing the bias circuits to be the predominant frequency determining circuit rather than the tuning inductor output, matching circuit. Considerable difficulty was experienced in rebonding to the planar devices, however, and these tests involving circuit changes could not be carried to a logical conclusion.

These initial tests on planar Gunn varactor chips were encouraging, however, in that tunable oscillations were obtained with the planar Gunn-varactor combination. These tests and the lumped-element tests using conventional chips demonstrate the realizability of lumped element monolithic VCOs.

SECTION III

PLANAR VARACTOR AND GUNN DIODE DEVELOPMENT

3.1 PROCEDURE DEVELOPMENT

In order to make planar device circuits on GaAs, technologies for ohmic contacts, implanted p-n junctions, device isolation, and planar Gunn devices had to be developed. The development of these procedures was a significant part of the early work and continued in part for the entire program. These procedures are described in the following paragraphs.

3.1.1 Ohmic Contacts

The fabrication procedure for planar varactors requires ohmic contacts for both n and p type implanted regions. For good devices the resistance of these contacts must be minimized. Therefore, the first goal in the planar diode fabrication was to establish metallization and alloying procedures that provided low resistance ohmic contacts and were compatible with the other fabrication steps.

The method described by Cox and Strack[3] was used to evaluate the various metallization procedures. The total resistance R_T of a contact to an epitaxial layer on a heavily doped substrate is given by the expression

$$R_T = \frac{\rho}{d\pi} \arctan\left(\frac{4}{d/t}\right) + \frac{R_c}{\pi(d/2)^2} + R_o$$

where ρ = resistivity of the epitaxial layer

d = contact diameter

t = epi layer thickness

R_c = specific contact resistance

R_o = residual resistance including substrate contact and measuring circuit.

The first term on the right is the spreading resistance term and can be calculated from given parameters. By using several different contact diameters, the residual resistance term can be eliminated and contact resistance obtained.

Substrate Contact

To evaluate the epitaxial layer contacts it is necessary to have a good low resistance susbtrate contact. The following procedure was used for forming the substrate contact in the ohmic contact evaluation measurements.

1. Wet sand substrate with 400 grit paper until mat surface is obtained.
2. Thin Ni electroplate (2-3 sec. sulfamate bath).
3. Au electroplate 5-10 μm.
4. Alloy 470 °C 2 min. in forming gas.

This procedure is quick and easy to perform, is very reliable and gives a specific contact resistance of 1.1×10^{-5} Ω cm^2. An additional gold electroplate after alloying is sometimes used.

An X-ray analysis of the electroplated Ni film showed a sulfur content of 2-3%. It is believed that this sulfur insures a heavily doped n-type regrowth region during alloying and thus produces a good low resistance contact.

Ohmic Contacts for N-type Epitaxy

The initial procedure that was tried for ohmic contacts to n-type epitaxial GaAs was that reported by Heime et al[4]. In this procedure 50Å of Ni, 700 Å of AuGe (88:12 wt.%) and 300 Å of Ni are evaporated sequentially and alloyed in forming gas at 460 °C. The first contacts using this procedure were very poor and this led to a rather lengthy investigation of

ohmic contacts that was not anticipated as part of the proposed program. The following sections describe the different metallization procedures that were tried in order to obtain good ohmic contacts to n-type GaAs. The experiments are described in the same time sequence as performed.

Electroplated Ni-Au contacts were very reliable for the substrate material; thus, the same procedure was tried for epi material doped to 3×10^{16} cm^3. The specific contact resistance obtained for these contacts was 4×10^{-5} Ω cm^2 and thus would have been acceptable. However, the smooth GaAs epi layer is much more difficult to electroplate than the sanded substrate surface. It is important that the initial Ni electroplate be very thin, otherwise, too much strain is introduced on alloying and the contacts pop off like fish scales when probed or during wire bonding. The thickness of this initial Ni electroplate could not be controlled, so this method was dropped for epitaxial layer contacts.

An initial AuGe evaporated layer was tried in order to make the GaAs epi layer easier to electroplate. These contacts were not uniform in resistance over the sample and even showed rectifying characteristics near the edges. A heavier NiAu plate again resulted in stress at the metal GaAs interface and mechanical failure of the contacts.

The Ni:AuGe:Ni procedure reported by Heime was tried again on both substrate material (Te doped 10^{18} cm^{-3}) and epitaxial material. The contacts made on substrate material had a specific contact resistance of 3×10^{-4} Ω cm^2, but the resistance of the contacts on the epitaxial material varied from .2 to 23 Ω across the sample. These difficulties led to questions concerning the epitaxial material surfaces. It is believed that a non-stoichiometric or contaminated surface could cause the rectifying contacts that were observed.

Therefore, several layers were analyzed, using Auger electron spectroscopy. The usual small amounts of carbon and oxygen were observed, but no other surface contamination was found. Also, the stoichiometry was the same as that reported by Uebbins and Tayloe[5] for GaAs. Nothing that would yield rectifying contacts was found on any of the six samples tested. Also, a chemical analysis was performed on the AuGe alloy that was used in the metallizations to determine if a p-type doping agent had been inadvertently added by the supplier, but none was found.

The variation in resistance of the contacts with position on the sample was believed to be due to non-uniform alloying. A new alloying system was made that would heat the sample uniformly and rapidly bring it to the desired temperature. The system is shown in Figure 28 and consists of a hot and cool metal plate enclosed in a glass tube that is purged with forming gas. The hot plate is kept at the alloying temperature and the sample is placed on a thin aluminum plate. Alloying is accomplished by moving from the cooling position to the hot plate and back. Alloying temperature is monitored by a thermocouple in a hole drilled to the center of the hot plate. The surface temperature of the samples was not measured, but the metallizations changed color and seemed to be completely alloyed in 15 seconds. The uniformity of the contacts has been much better with this alloying system.

A copper sputtering target was made and electroplated with Ni from a sulfamate bath. Films sputtered from this target were analyzed and found to contain about .3% sulfur. Using this target sputtered Ni:Au, sputtered Ni + evaporated AuGe:Ni, and sputtered Ni + evaporated AuGe:Ni + electroplated Au metallizations were evaluated. The Ni:Au contacts were not ohmic, but both of the other metallizations produced ohmic contacts with the latter showing

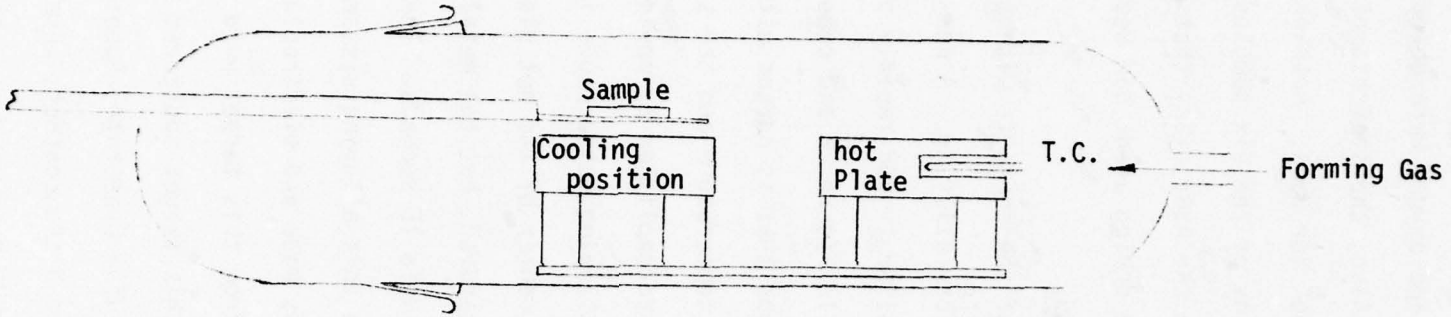


Fig. 28. Alloying System

the least resistance. The thickness of the sputtered Ni can be thin and carefully controlled; thus, little strain is introduced at the Ni:GaAs interface. Although these contacts were ohmic, no further work was done with sputtered films because of the unknown effects of sputtering on the edge of the p-n junction at the surface.

In the above attempts to achieve ohmic contacts the processes that seemed to produce the most improvement were the new alloying system (rapid heating and cooling) and the gold electroplating before alloying. When these processes were added to the Ni:AuGe:Ni metallization, the ohmic contacts were the best that have been evaluated. This procedure as outlined in Table II gave a specific contact resistance of 5.4×10^{-5} Ω cm^2 on epitaxial material with an impurity level of 1×10^{16} cm^{-3}. Selenium implanted epitaxial material was also contacted using this procedure with a resulting contact resistance of 3×10^{-4} Ω cm^2. The metallization presently being used for n-type ohmic contacts omits the initial 50Å Ni and uses 1000Å of evaporated Au instead of the electroplated Au. This method is easier to apply and is reliable if the rapid alloy cycle is used.

TABLE II

Metallization Procedure Used for Ohmic Contacts to N-type Epitaxial Layers

1. Evaporate: 50Å Ni
   700Å AuGe 88:12 wt%
   300Å Ni
2. Photomask for contact metallization
3. Electroplate 5.0 μm Au in contact areas

TABLE II (Continued)

4. Strip photomask
5. Alternating etch in cyanide Au etch and $HC\ell:HNO_3:H_2O$ 4:1:5 for isolation
6. Alloy 480 °C 2 min. in forming gas (rapid heat and cool).

Ohmic Contacts to Beryllium Implants

Ohmic contacts were made to Be implanted n-type epitaxial material on n^+ and Cr doped substrates. The material was implanted over the entire surface of the device with a flux of 5×10^{14} cm^{-2} at 100 keV. The metallization procedure developed for the Be implants is given in Table III. The specific contact resistance was not measured for this procedure, but the I-V characteristics given in Figure 29 show that the contacts are ohmic. No p-type substrate material was available for this study so most of the resistance shown in Figure 29 is due to the thin (.5 μm) implanted layer on which the contacts were made.

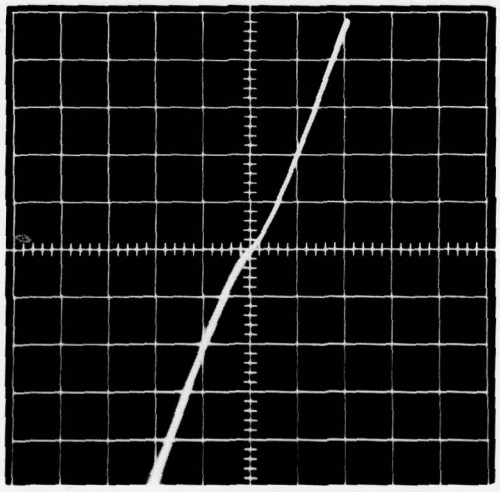


Figure 29. P-type Ohmic Contact
(1.0 ma/cm, 2V/cm)

TABLE III

P-type Ohmic Contact Metallization Procedure

1. Clean sample in HF, hot DI water and blow dry in N_2.
2. Heat sample to $\simeq$ 190 °C in vacuum better than 4×10^{-6} Torr.
3. Evaporate in sequence from dimpled W boat at a spacing of 14 cm (a) 3 mg Ni (50Å), (b) 4 mg In, 4 mg Mn, 40 mg Ag (1,000Å), (c) 40 mg Au, (1,000Å).
4. Apply photoresist to the clean metallized surface immediately after removing from evaporator.
5. Define the desired metallized areas in the top Au layer using photoresist and technistrip Au etch.
6. Remove the photoresist. Use the Au as mask and etch the remaining AuInMn:Ni in one drop of nitric acid per 10 cm^3 of concentrated sulfuric.
7. Rinse in methanol (water rinse etches surface), hot DI, and blow dry.
8. Alloy 600 °C 15 seconds in forming gas (rapid heat and cool important).

3.1.2 Implanted P-N Junction Evaluations

Mesa Diodes

Several experiments were performed to evaluate the characteristics of the Be implanted p-n junction. Part of the material that was implanted with Be for ohmic contact evaluation was used to make mesa diode structures as shown in Figure 30. After the contact metallization for these diodes was defined and alloyed, the current-voltage relation between contacts was measured and found to be ohmic. The samples were then etched to form the mesa structures and the junction characteristics of these mesa diodes are shown in Figure 31. The characteristics are good, but show a reverse breakdown of only 14 V.

Additional epitaxial material was selected for higher breakdown and implanted with Be for the fabrication of mesa diodes as described above. Typical I-V characteristics of these diodes are shown in Figure 32. Most of the devices exhibited a premature reverse bias breakdown. The voltage at which this premature breakdown occurred varied considerably from diode to diode (Figure 32a and c). Figure 32a and b show the reverse characteristics of the same diode with a different current scale. This diode has very small reverse leakage current to -47V and thus confirms a Be implanted p-n junction of sufficient quality for varactor diodes. The premature reverse breakdown exhibited by some of the mesa diodes would indicate poor device yield from this material and detracts from, but does not negate, this confirmation.

Planar Diodes

The mesa structure confirmed that implanted p-n junctions of device quality could be made, but many problems were encountered with implanted planar diodes that were not encountered with the mesa structure. The fabrication problems are discussed in detail in another section, but the identification

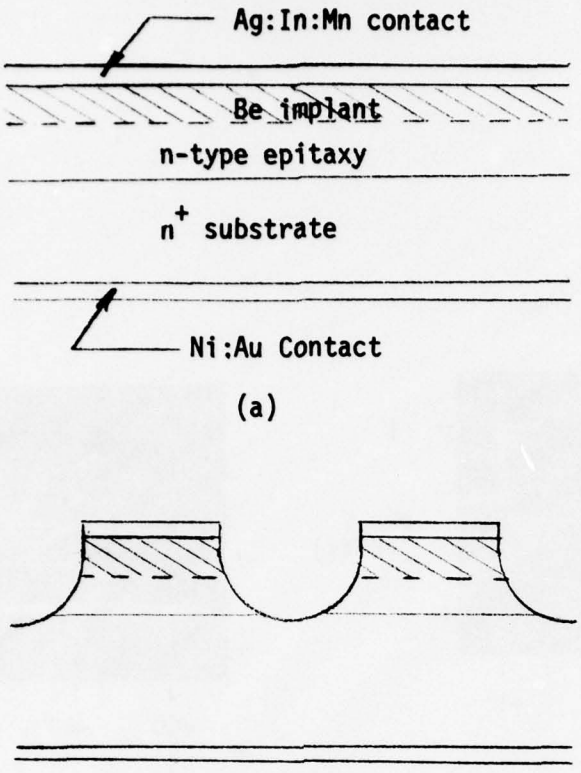


Fig. 30. Mesa Diodes With Be Implanted p-n junction

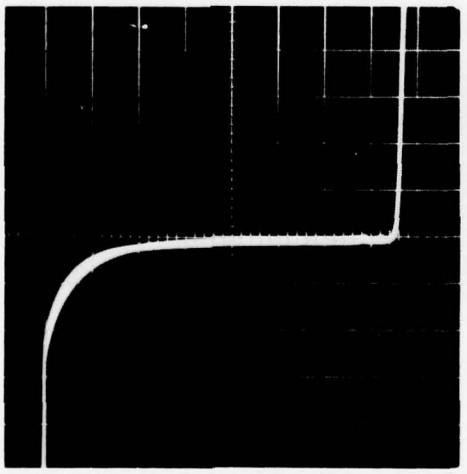


Fig. 31. I-V Characteristic of Mesa Diode With Be p^+ implant (2V/cm, .01 mA/cm).

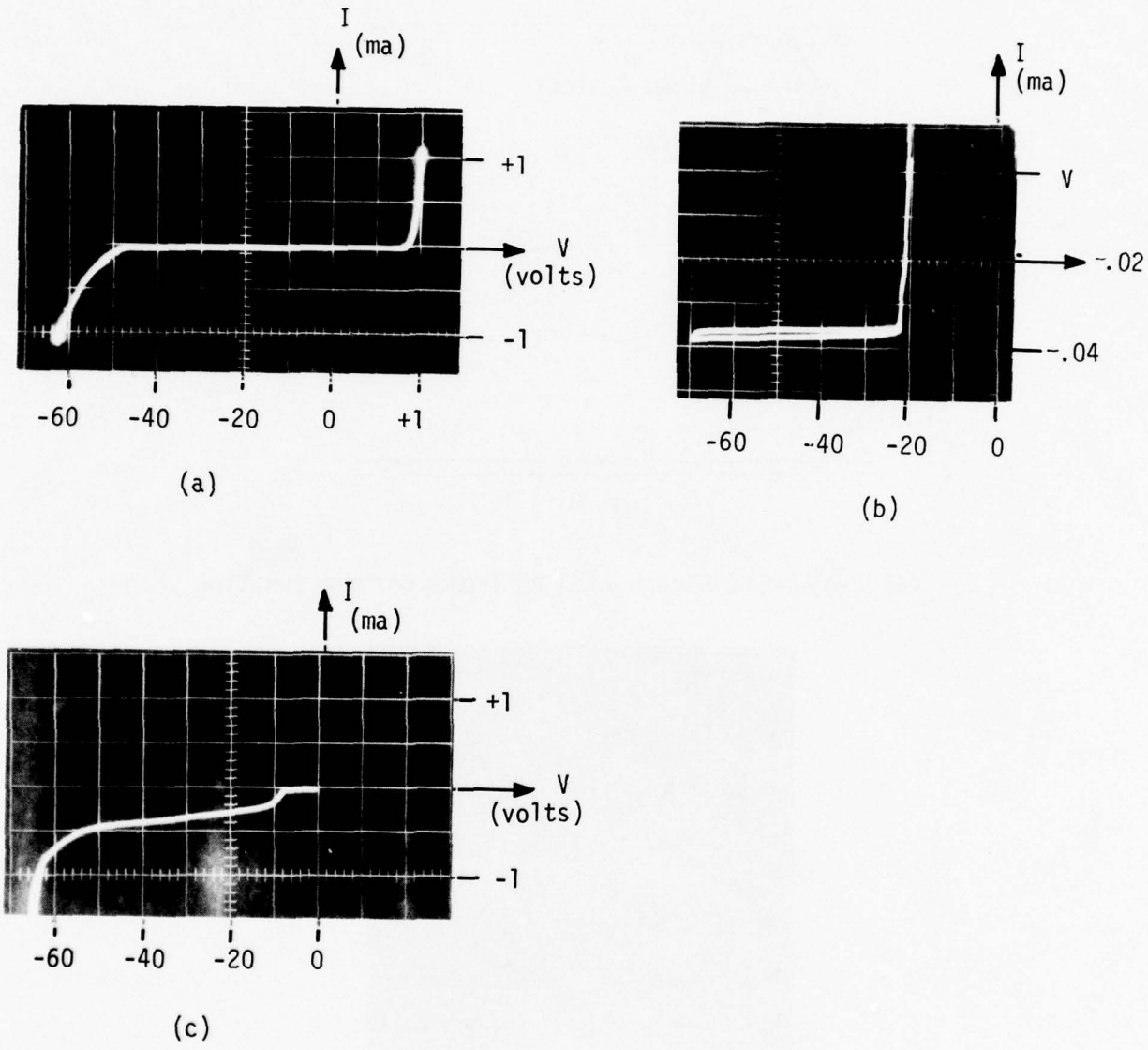


Fig. 32. I-V characteristics of Be implanted p-n junctic

of some of the problems is given here.

Figure 33 identifies the structure of the first implanted planar diodes and Figure 34 is a typical I-V characteristic. The diodes are very soft showing large reverse leakage currents. Figure 35 shows the I-V characteristics of the same diodes after several minutes etch in H_2SO_4:H_2O_2:H_2O 5:1:1. Little improvement is observed in the reverse characteristics. Thus the poor quality of these diodes is not primarily a surface problem, but seems to be associated with the material.

A complete planar diode structure with both Be implanted p^+ region and Se implanted n^+ region was also evaluated. An SEM photograph of this structure and typical I-V characteristics are shown in Figure 36. The p-n junction for this device is between the metallized areas, normal to the surface, and extends for about .5 micron into the surface. The devices are definitely rectifying, but have high reverse leakage and show very high resistance. The high series resistance is most likely due to autodoping from the Cr doped substrate during growth of the epitaxial layer.

The next two groups of planar diodes and many groups thereafter had a common problem that was identified as a highly doped surface layer. The implant areas of the second group of planar diodes are shown in Figure 37. After the encapsulant was removed, the devices were probed to measure the I-V characteristics. The probes did not make ohmic contacts to the GaAs, but are sufficient for a preliminary evaluation. When both probes are connected to the p^+ region, the characteristics are as shown in Figure 38. Almost identical characteristics were observed when the probes were attached to the p^+ and n^+ regions (Figure 38b). The third group of devices was different from the previous groups. First, the epitaxial material was part of a wafer from RCA that had been used by Ken Sleger of NRL to make FETs. It

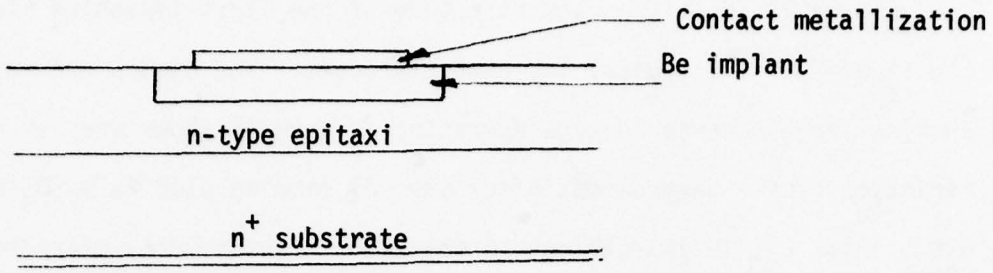


Fig. 33. Implanted Planar Diode Structure

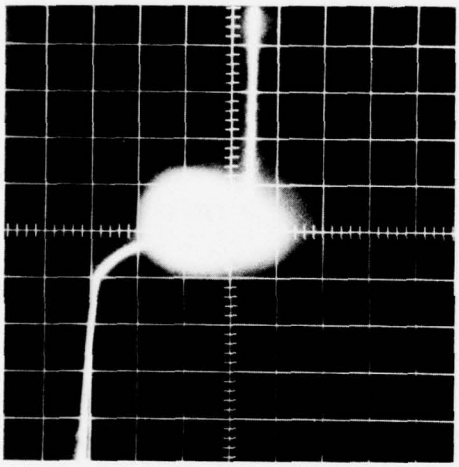


Fig. 34. I-V Characteristics of Planar Device Prior to Etching (2V/cm, 1mA/cm)

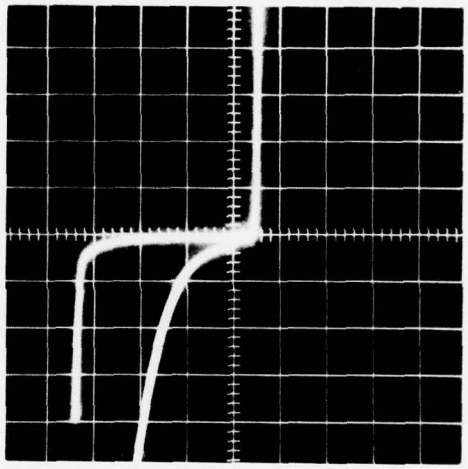
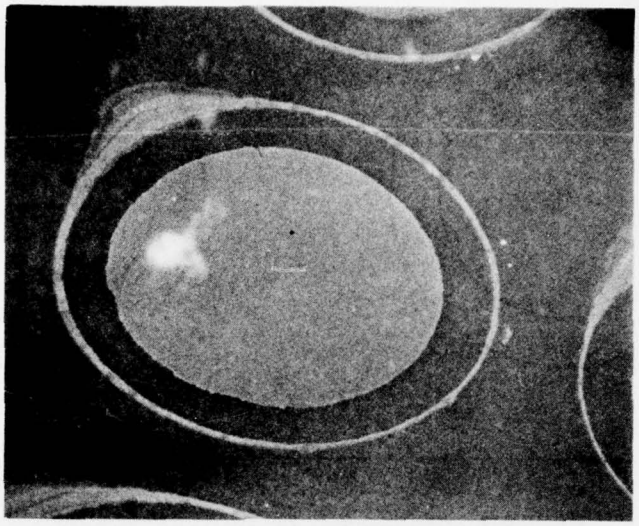


Fig. 35. I-V Characteristics of Planar Device After Etching (2V/cm, 1mA/cm and .01mA/cm)



Completed Planar Diode

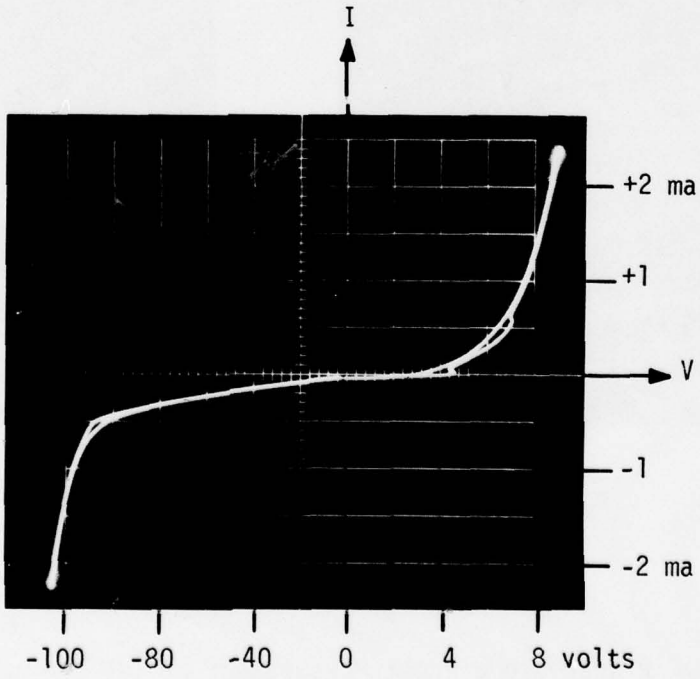


Fig. 36. Complete planar diode with p-n junction normal to the surface.

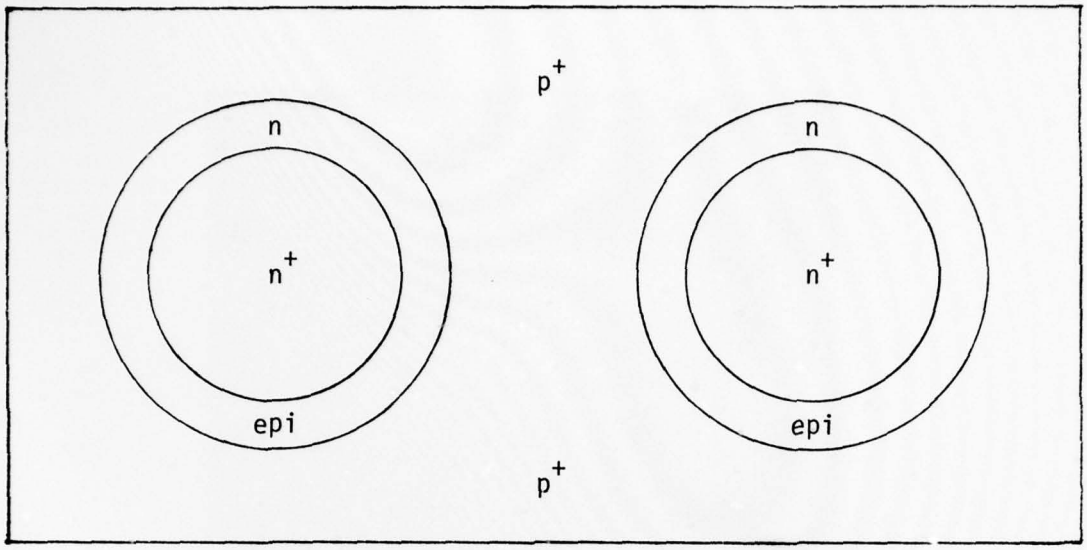
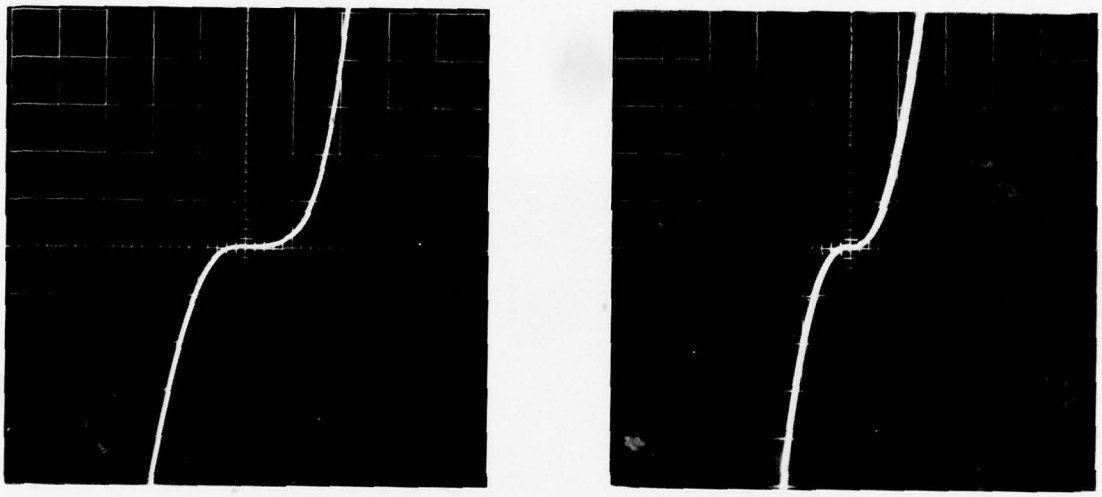


Fig. 37. Planar Diode Implant Areas



a b

Figure 38. Planar Diode Probe Measurement of I-V Characteristics a, b, and c (2 V/cm, .1 ma/cm) (Group 2)

a. Probes connected p^+ to p^+

b. Probes connected p^+ to n^+

was, therefore, firmly established as device quality material. The epitaxial layer was specified as 1.0 micron thick n-type (sulfur 1 x 10^{16} cm^{-3}) with a symetric probe to probe breakdown to 15 volts. Second, there was no n^+ implant for ohmic contacts. This step was omitted in order to simplify the process and isolate the problem area.

In spite of the above differences, probe measurements of the I-V characteristics were very much the same (Figure 39) as those of the other groups of planar diodes processed. Approximately the same characteristics are obtained regardless of where the probes are placed on the sample. Also, part of the wafer was etched in Br methanol to remove about .2 microns of the surface layer. (An interference objective and mercury vapor light source with green filter was used to determine the amount of material removed by the etch.) The electrical characteristics were not significantly changed by removing this material.

These data indicate that a highly doped surface layer which extends over both implanted and unimplanted regions has been introduced by the device processing. A great deal of work was directed toward identifying the layer and its probable source.

3.1.3 Device Isolation

A necessary part of the incorporation of a planar diode in a monolithic circuit is device isolation. An experiment was, therefore, designed to evaluate proton bombardment as the isolation process for these devices. An epitaxial layer 1.0 μm thick doped n-type to 2.4 x 10^{16} cm^{-2} was grown on a semi-insulating substrate for this experiment. Ohmic contacts were applied to the epitaxial layer using evaporated Ni:AuGe:Ni and lift-off metallization techniques. After alloying at 480 °C for two minutes the contacts were electroplated with gold. An emitter evaluation mask that was on hand was used to

define the contact geometry as shown in Figure 40. Electrical measurements show that the contacts were ohmic to very high current levels and had average resistances of 14.6 Ω and 46.4 Ω between points A and B and A and C, respectively. This material was then subjected to proton bombardment. The contact metallization provided shielding for certain areas of the epitaxial layers, but the unshielded areas were rendered semi-insulating by the bom-

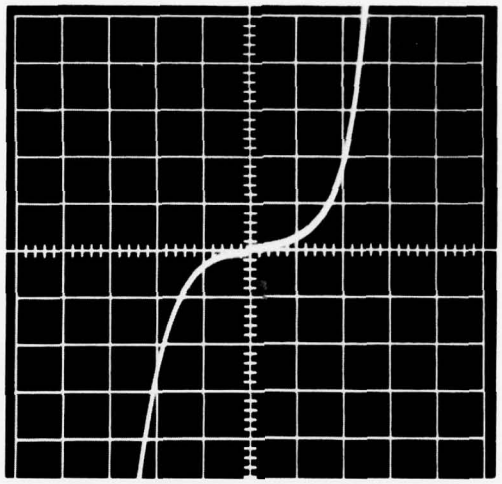


Fig. 39. Group 3 Characteristics (.01 ma/cm , 2 V/cm)

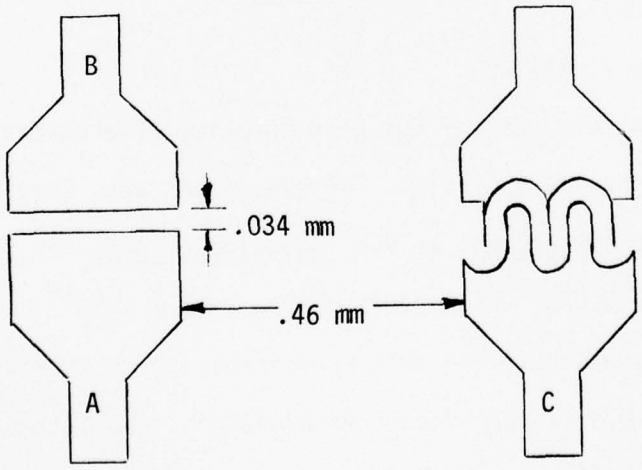


Fig. 40. Contact Areas for Isolation Experiment

The proton bombardment changed the resistance as measured between A and B, Figure 40, from 14 ohms to more than 10 megohms. This would provide adequate isolation for the planar varactor circuits and monolithic circuits needed for this program.

3.1.4 Planar Gunn Device

An approximate design for a planar Gunn device may be obtained using the relations

$$\ell(\mu m) = \frac{100}{f\ GHz} \tag{1}$$

$$n\ell > 10^{13}\ cm^{-2} \tag{2}$$

$$nd > 10^{12}\ cm^{-2} \tag{3}$$

where n is the epi layer impurity concentration and ℓ and d are as defined in Figure 41. The design parameters of primary interest are given in Table IV.

f(GHz)	$\ell(\mu m)$	d(μm)	n(cm^{-3})
20	5	.5	2×10^{16}
10	10	1	1×10^{16}
5	20	2	5×10^{15}

Table IV. Planar Gunn design parameters.

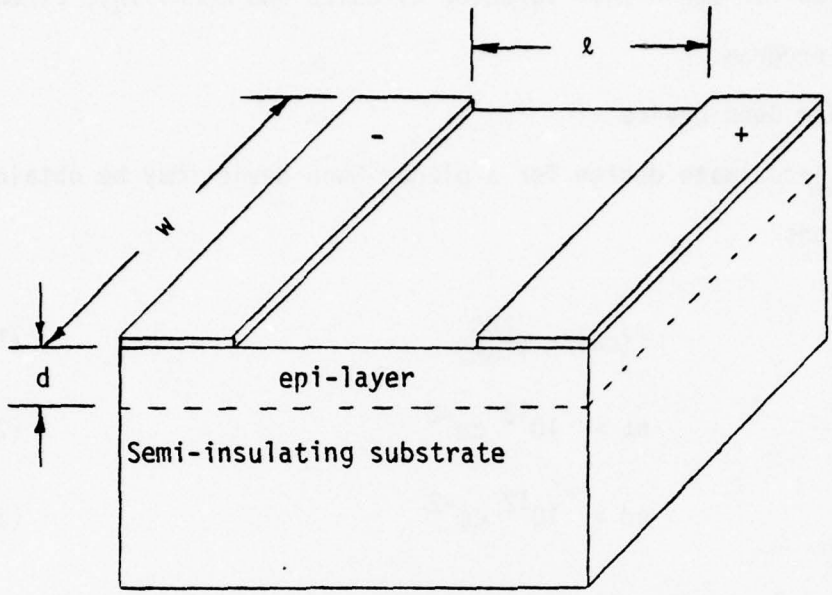


Fig. 41. Planar Gunn Device

We are restricted to using a .5 μm epi-layer in order to achieve complete penetration of the p^+ implant for the planar varactor fabrication. Since we intend eventually to make both Gunn and varactor devices on the same slice, the Gunn device suffers the same .5 μm epi-layer thickness restriction. This layer thickness is most compatible for a Gunn device at 20 GHz which is not in the frequency band of interest on this program. Therefore, some trade-off was necessary to optimize design parameters for the combined Gunn-varactor device.

As a first try, planar Gunn devices were fabricated on a 1.5 μm thick

n-type epitaxial layer doped to 2×10^{16} cm^{-3} with a 5 μm intrinsic buffer layer and Cr doped substrate. A Ni:AuGe:Ni metallization alloyed for 2.5 minutes at 480 °C in forming gas was used for ohmic contacts. Figure 42 is an optical micrograph of the top contact metallizations. The center contact (cathode) is 127 μm in diameter with a 10 μm active region between the concentric metallizations. Kodak 747 photoresist and masks made with a fly's eye camera were used to define the metallization. Typical I-V characteristics are shown in Figure 43.

3.2 FABRICATION PROBLEMS OF IMPLANTED PLANAR DEVICES

Some necessary procedures for planar GaAs circuits were developed quickly with very little expenditure of funds. However, a great deal of effort was spent in obtaining implanted planar p-n junctions. Good planar junctions were consistently achieved only at the end of the program on the last four epitaxial layers processed. Unfortunately, this left little time to investigate device isolation, to develop high quality Gunn devices, or to compare the microwave properties of planar implanted junctions with more conventional mesa junctions. The problems encountered in the fabrication of the planar devices are discussed in the following sections.

3.2.1 Growth of Thin Epitaxial Layers

As mentioned previously, the first diodes (Group 1) had a high series resistance due to autodoping of the epitaxial layer from the Cr doped substrate. Autodoping is always present at the beginning of CVD epitaxial growth. The control of this initial growth region is difficult, particularly when layers only .5 μm thick are being grown. If too much autodoping from the substrate occurs the epitaxial layer is esentially Cr doped and, therefore, its resistivity is very high. This problem was solved by growing an undoped

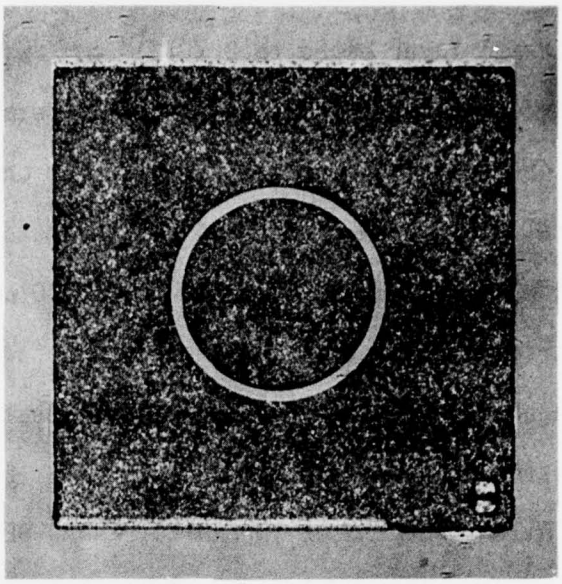


Fig. 42. Planar Gunn Contact Metallization

Fig. 43. Planar Gunn I-V Characteristics (5 V/cm, 20 ma/cm) Center Contact Negative

buffer layer to bury the effects of the Cr doped substrate before the doped active region was grown. A typical impurity profile, obtained using an uninterrupted growth sequence, is shown in Figure 44. An evaporated Au Schottky barrier and Materials Development Corporation Automatic Doping Profiler was used to obtain the profile shown in Figure 44. The impurity level of the buffer layer, as obtained with this instrument, drops below 10^{14} cm^{-3} and, therefore, adds only a very small shunt current path to the devices. Devices made from this material (Figure 45) have much better forward bias characteristics than those of the first group of planar diodes shown in Figure 36.

3.2.2 Photoresist Masks

Another problem area revealed during this work was the poor definition of the photoresist used for the first implantation masks. A series of experiments was performed on silicon wafers to determine the optimum spin, viscosity and exposure for the Waycoat resist. The optimum conditions were found to be 2:1 dilution, 5,000 rpm spin for 30 seconds, and a 2 second exposure using the K&S mask aligner. Good edge definition was obtained with these conditions. Photoresist was not an adequate implant mask and was abandoned in favor of Au masks. Good edge definition was also required for the Au masks and the conditions given above were used to obtain the required definition.

3.2.3 Highly Doped Surface Layer

As discussed previously, a highly doped surface layer that extended over both implanted and unimplanted regions was identified as an initial problem. This problem was eliminated by using thick Au implant masks, using only a Be implant to make the devices, and changing to a capless anneal. A great deal of time was spent investigating other possible causes before

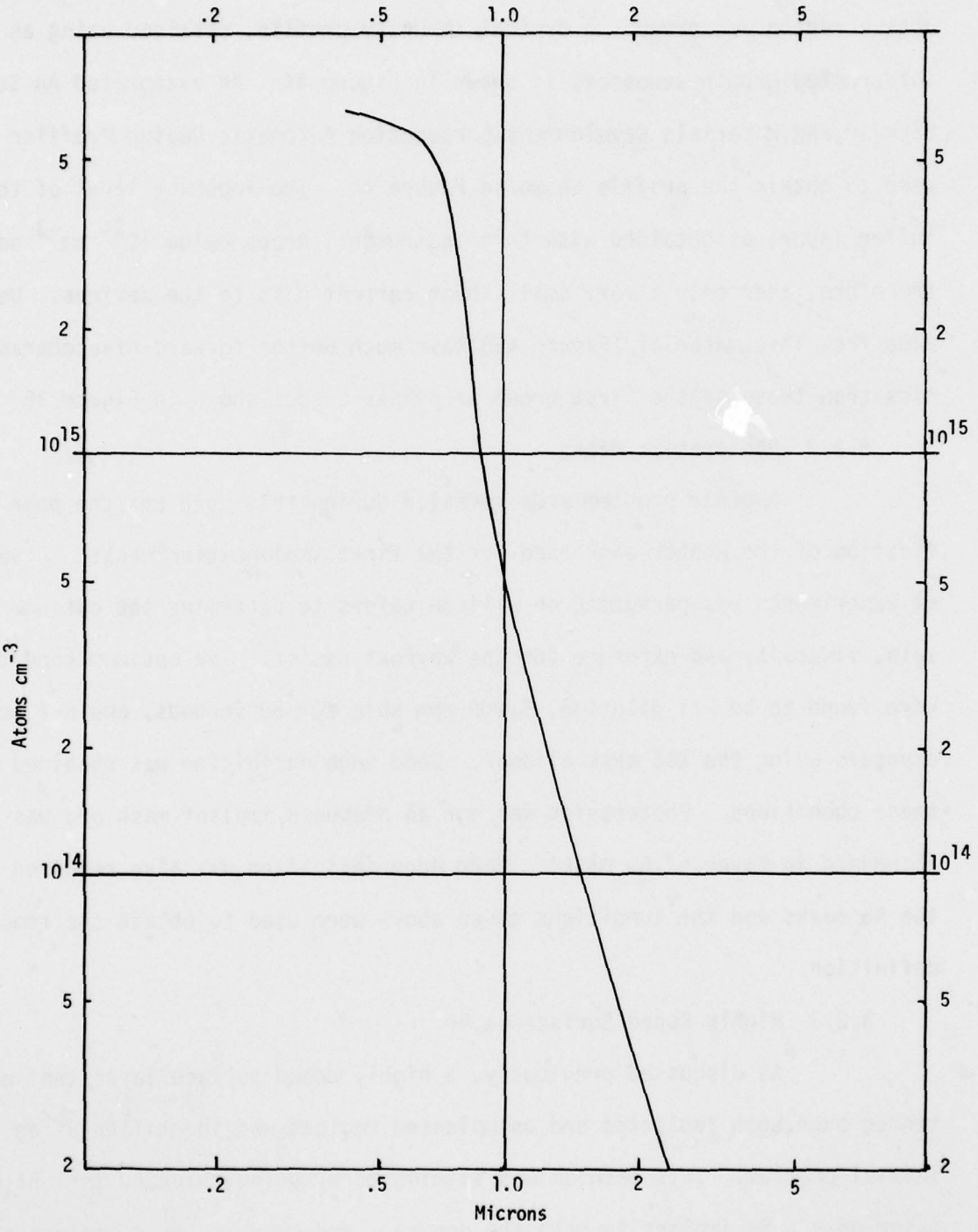
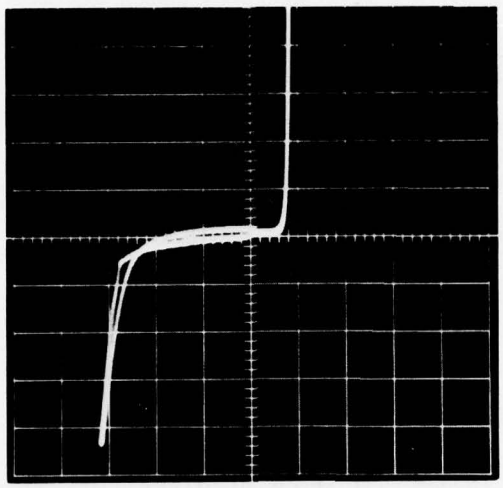


Figure 44. Impurity Profile Showing Undoped Buffer



.01 ma/cm
1 V/cm forward
20 V/cm reverse

Figure 45. Characteristics of p-n Junction Implanted in Active Region Grown on Undoped Buffer Layer.

this solution was found. These investigations and solutions represent a significant part of the work done on this program and are discussed in the following paragraphs.

Surface Contamination

One possible source of the highly doped surface layer was thought to be surface contamination. Therefore, group 2 and 3 samples were examined by Auger electron spectroscopy (AES). Sulfur was detected which could have accounted for the highly doped surface layer, if present in sufficient quantities, during encapsulation and anneal. Other experiments confirmed the presence of S in the photoresist used for implant masks. Normally, the photoresist is kept in a 25 ml glass syringe with a filter and a few drops are squeezed out as needed. It was established that the sulfur was present only in the resist stored in the syringe. However, careful application of standard stripping procedures would not leave a S residue from either AZ-111 or Waycoat resists. No other contamination was detected with AES. Thus, surface contamination was eliminated as the cause of the highly doped surface layer.

High Surface Concentration Implant

The early Be implants for planar diodes were done in one step at 100 keV 5×10^{14} cm^{-2} and annealed for 30 minutes at 800 °C with a SiO_2 encapsulation. This procedure produces a very high surface concentration[6]. An enhanced surface diffusion, caused by the high surface concentration during annealing, could have produced the observed highly doped surface. Additional samples were prepared with a multiple implant (Figure 46) to avoid the high surface concentration, but they still showed a highly doped surface after encapsulation and anneal.

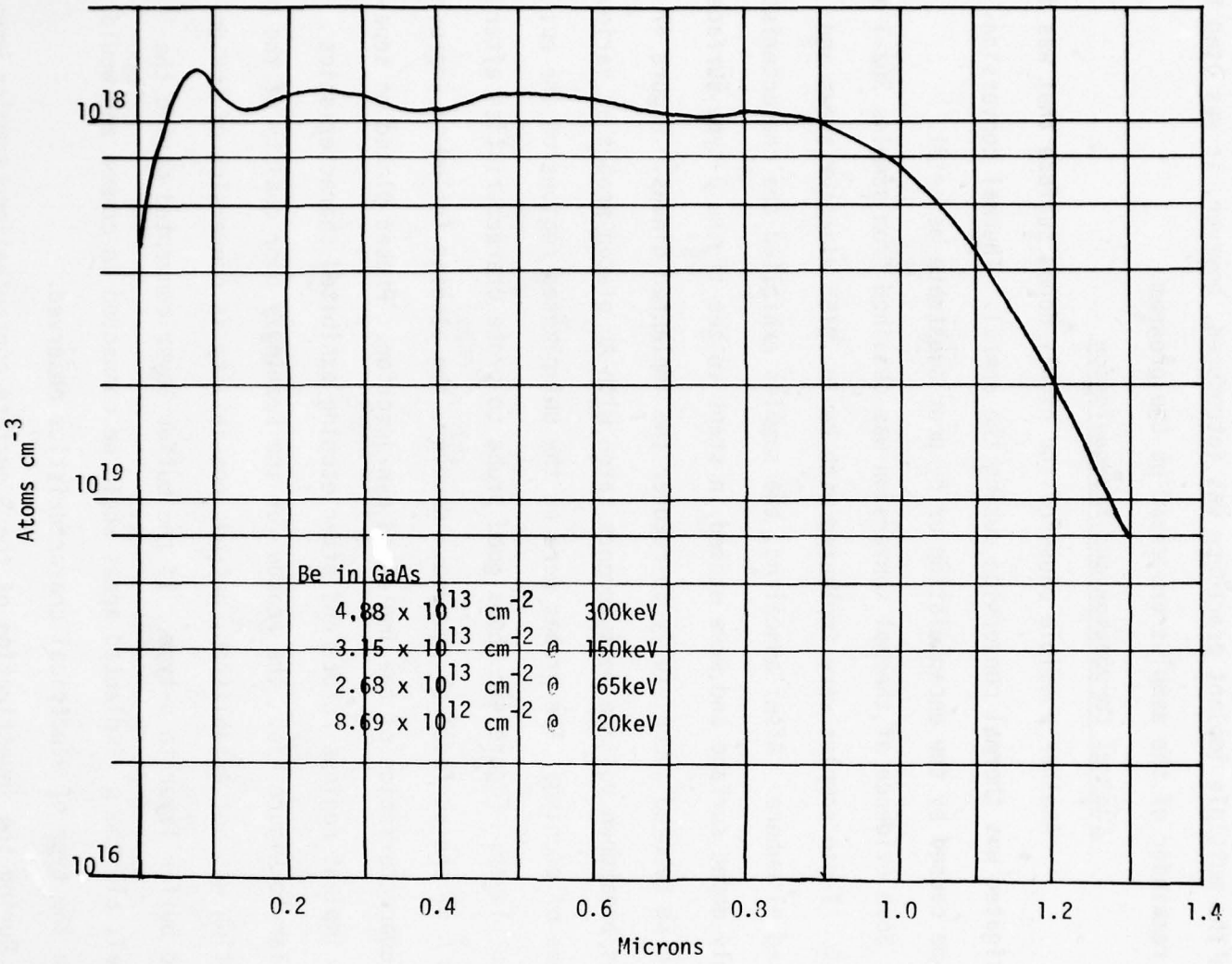


Figure 46. Berylium Implant Profile Calculated by H. Dietrich, NRL

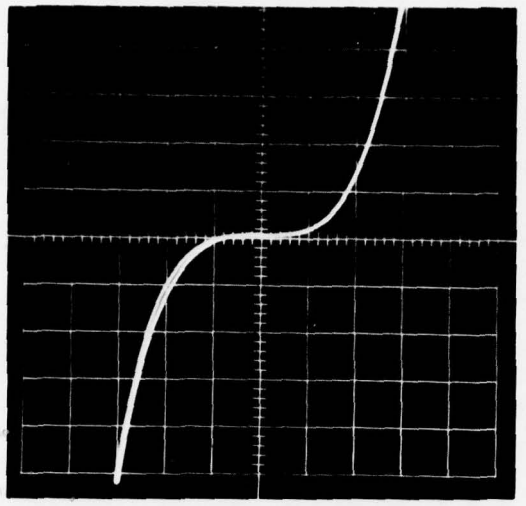
Since the multiple implant did not solve the problem of the highly doped surface, it was probably not caused by the original Be implant procedure. Once the multiple implant procedure was introduced, however, it was used for the remainder of the samples processed on the program.

Thermal Conversion and Encapsulation

Another possible cause of the highly doped surface that was investigated was thermal conversion during the anneal. Thermal conversion can be caused by the encapsulation or by poor substrate material.

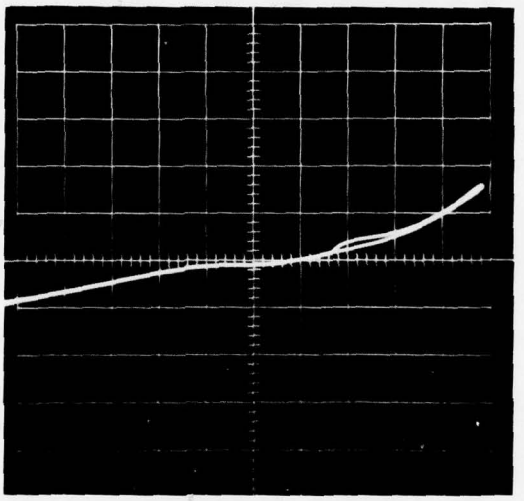
Some evidence of thermal conversion was obtained from samples 302-1 and 218-1. These samples were implanted with Be in .015" diameter areas and masked elsewhere. After annealing, the samples exhibited the characteristic highly doped surface and were etched in steps to see if the p-type surface could be removed successfully to recover the implanted diodes. Figure 47 shows breakdown voltage measurements taken with Au plated probes at various stages of etching. The probes were on the unimplanted regions of the epitaxial layer. Figure 47c shows good probe to probe characteristics after 2500 Å of the surface was removed. However, the etching failed to improve the characteristics of the implanted p-n junction. Probes placed on separate implant regions before and after etching exhibited characteristics similar to Figure 47a. The reason for the seemingly poor quality of the p-n junction was not established, but one possibility is conversion of the undoped buffer layer to p-type. If the buffer layer converted during the anneal, all the p^+ implanted areas would be connected in common and would cause the type of electrical characteristics observed.

During the investigation of the S surface contamination, samples were prepared with a 2500 Å thick evaporated Au film applied before the photoresist mask. In this way, the surface was protected from S contamination from the



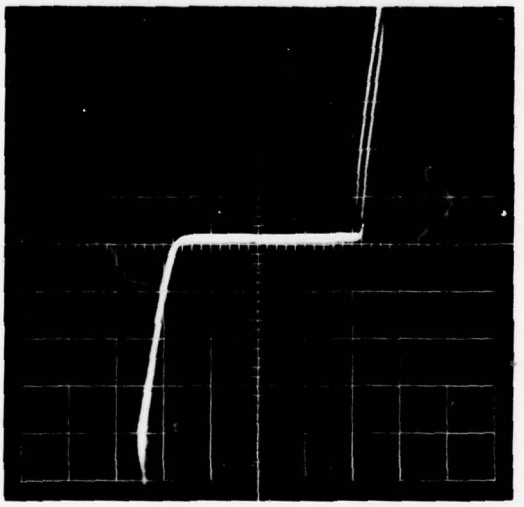
(a)

no etch
1V/cm
.1 ma/cm



(b)

1800 Å etch
1V/cm
.1 ma/cm



(c)

2500 Å etch
10V/cm
.01 ma/cm

Fig. 47. Sample 302-2 Probe to Probe Voltage Breakdown of Unimplanted Region

AD-A059 045 GEORGIA INST OF TECH ATLANTA ENGINEERING EXPERIMENT --ETC F/G 9/5
INTEGRATED VARACTOR TUNED MICROWAVE SOURCES.(U)
JAN 78 J W AMOSS, E L MEEKS, N W COX N00173-76-C-0044

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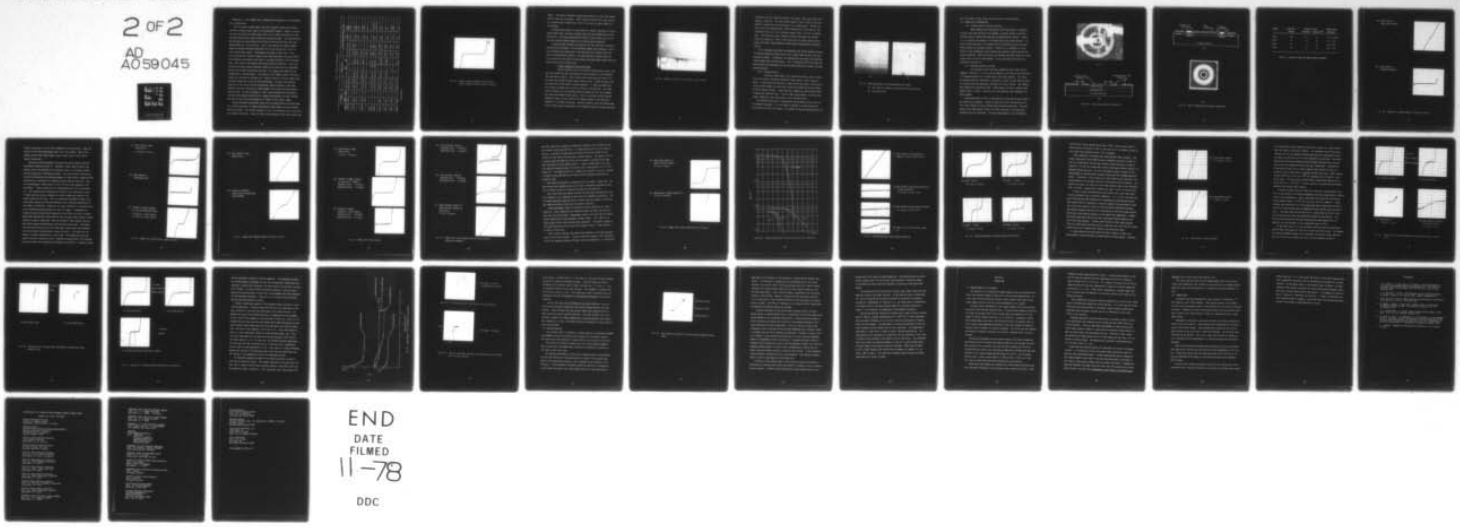

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photoresist. These samples had a combination of photoresist and evaporated Au as implant mask.

The first metal masked sample (1124-1B) resulted in good planar diodes and had no p-type surface layer on the unimplanted regions. However, the next four runs processed with metal masks (218-1, 221-1, 228-1 and 302-2) all had the same highly doped p-type surface over the entire wafer. The one good metal masked sample was encapsulated with silicon nitride and the other four were encapsulated with silicon dioxide. Table V was compiled to compare thermal probe and voltage breakdown measurements on silicon dioxide and silicon nitride encapsulated samples. Measurements were made on both side). Also, since some epitaxial material always grows around the edge of the back side of the substrate, measurements were taken at the edge and middle of the substrate side. Both sides of the samples were encapsulated for annealing. Thus, comparisons were made between implanted epitaxy on the front and the unimplanted epitaxy and Cr doped substrate on the back. All samples were masked for Be implantation in isolated areas. The surface of all samples except 1124-1B was p-type over the entire implanted side. Samples 1124-1B is the only sample that was metal masked and silicon nitride encapsulated. The back side epitaxial layer of all the silicon nitride encapsulated samples remained n-type after annealing, but was converted to p-type whenever the silicon dioxide encapsulation was used. The data presented in Table V were obtained from experiments that were not designed specifically to compare encapsulants, but does indicate that the silicon nitride encapsulation if better for the planar diodes.

Voltage breakdown measurements taken with Au plated probes were established as a routing evaluation to compare measurements taken before and after encapsulation and anneal. The voltage breakdown of the 1124-1B material was 14 volts before implant and anneal. Figure 48 shows the measurements taken after implant and

Table V. Comparison of Encapsulants

Sample	SUBSTRATE				THERMAL PROBE			VOLTAGE BREAKDOWN PROBE TO PROBE			
	crystal number	slice number	mask	cap	front	back middle	back edge	n to n	n to p^+	back middle	back edge
1124-1B	3109	9	Au + resist	Si_3N_4	0	0	n	8 - 10	8 - 10	>220	25-30 sharp
1212-B	3109	10	resist	Si_3N_4	strong P	0	weak n	soft <1 *	soft <1 *	>220	7-10 sharp
	3109	10	resist	$Si\ O_2$	strong P	0	weak P	soft <1 *	*	>220	15 sharp
106-1B	3109	12	resist	Si_3N_4	strong P	0	weak n	soft <1 *	*	>220	30-45 sharp
	3109	12	resist	$Si\ O_2$	strong P	P	P	soft*	*	soft	soft
H 351	-	-	resist	Si_3N_4	strong P	metallized		soft <2	soft <2	back	metallized
Bozler	-	-	resist	$Si\ O_2$	strong P	metallized		soft <2	soft <2	back	metallized
221-1	6393	3	Au + resist	$Si\ O_2$	strong P	0	strong P	soft <2	soft <2	>220	soft <1
218-1	6393	3	Au + resist	$Si\ O_2$	strong P	0	strong P	soft <1	soft <1	>220	soft <2
302-2	6393	4	Au + resist	$Si\ O_2$	P	0	P	soft <2	soft <2	>220	60-80 sharp
228-1	6393	4	Au + resist	$Si\ O_2$	P	0	weak P	soft <2	soft <2	>220	>220

* No index marks

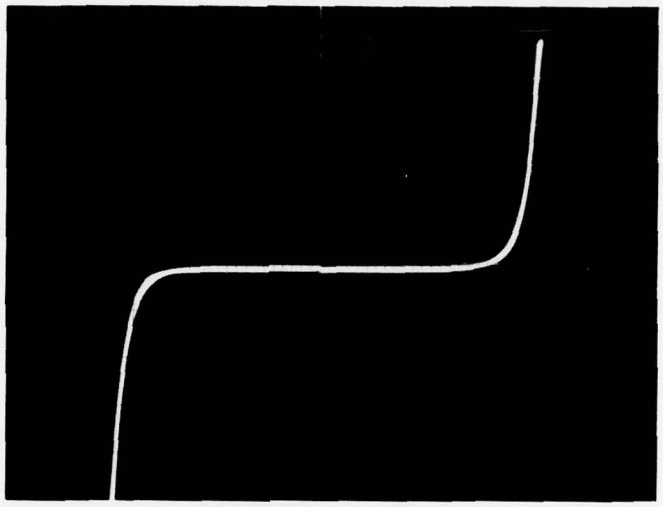


Fig. 48. Probe to Probe Breakdown Voltage After Anneal (sample 1124-1B, 2v/cm, .01 ma/cm)

anneal. The reverse breakdown voltage was decreased, but the highly doped surface layer was not present. Other samples processed with Si_3N_4 cap and at a reduced anneal temperature of 630 °C also had the highly doped surface problem.

Although some evidence is given above for thermal conversion of the undoped buffer layer, the major problems seem to be the implant mask and encapsulation. The Si_3N_4 encapsulation process is better than SiO_2, but at the time, neither seemed adequate for reliable device processing.

A capless anneal procedure was used for the last four sets of devices processed on the program. The Be implanted samples were annealed at 550 °C for 30 minutes with forming gas in the same hot plate system (Figure 28) used for alloying ohmic contacts. An electroplated Au implant mask over 1.0 μm thick was also used for these samples and good planar diodes were produced from all four of these sets.

Implant Through the Photoresist Mask

Another possible cause of the heavily doped surface layers that was investigated was that the photoresist mask allowed Be to be implanted over the entire surface. Angle lap and stain techniques were used to try to reveal the suspected highly doped surface region. Figure 49 shows a lap and stain done on the group 2 varactor material. A light unstained area can be seen to extend over the entire surface of the material. The light area is thicker over the implanted regions between the .015 inch diameter dots that were masked during implant. This is consistent with Be implant through the mask, but the stain on the lapped surface is not definitive enough for a confident conclusion. Several different stains and etches were tried to obtain better definition of the implanted region, but none were more

Fig. 49. Angle Lap and Stain of Varactor Group 2 Diodes

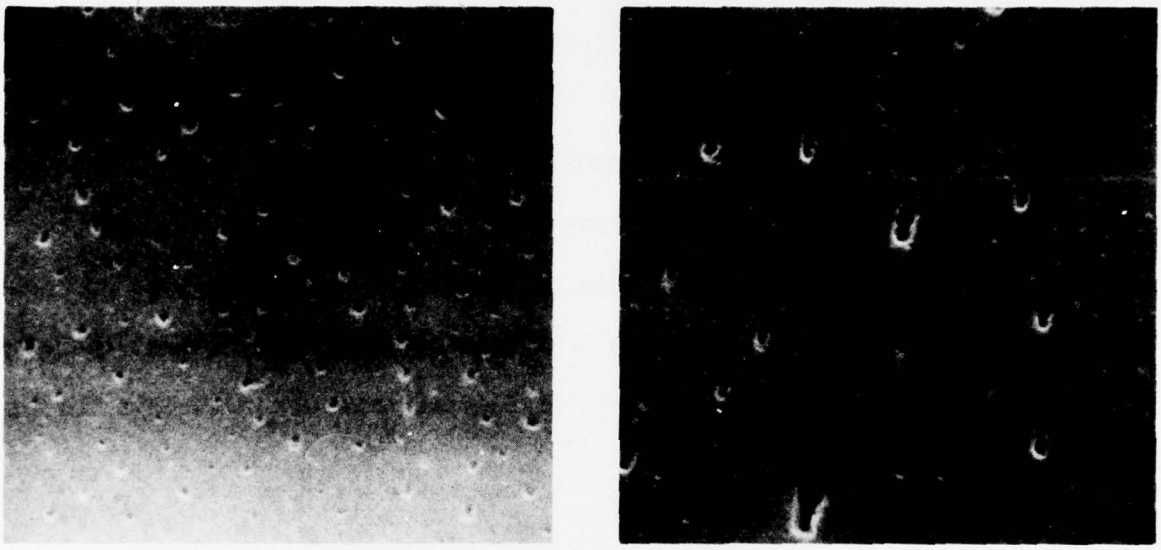
successful than the solution (10g KOH, 10g kFe_3CN, 100cc H_2O) used on the sample in Figure 49. The metal masked samples listed in Table V had only 2500 Å of evaporated Au and photoresist as an implant mask. Another epitaxial layer was prepared with a 2500 Å evaporated Au film that was electroplated with Au to a final thickness greater than 1.0 μm for an implant mask. This group was given a multiple implant and broken into several pieces for annealing. Some of these pieces had the highly doped surface layer, but others, when properly cleaned before encapsulation and anneal, did not.

It is concluded from these investigations that the Be implant was penetrating the photoresist mask and causing a highly doped surface layer over the entire sample. In addition, the encapsulation and anneal also produced highly doped p-type surface layers. This is supported by the fact that the best devices were obtained by using thick metal masks and a capless low temperature anneal.

3.2.4 Thermal Etching

The planar diode material was implanted through a mask of photoresist to achieve isolated Be implanted p-type regions in the n-type epi layer. In processing this material, a hazy surface was noted. SEM pictures of the surface showed pits which most likely were formed during the encapsulation or annealing steps. Figure 50a and b compare pits which were formed in masked and implanted areas. The pits were larger (about .9 μm being the largest dimension), but further apart in the implanted areas.

The thermal etching was an intermittent problem which did not occur on all material processed. It is no longer a problem if the desired devices can be made only with a Be implant. No thermal etching was observed with the



(a) (b)

Fig. 50. SEM Photographs of Be Implanted Material 9,000x

(a) Area that was masked by photoresist during Be implant

(b) Be implant area

550 °C 30 minute capless anneal which suffices for the Be implant.

3.3 PLANAR DEVICE COMBINATIONS

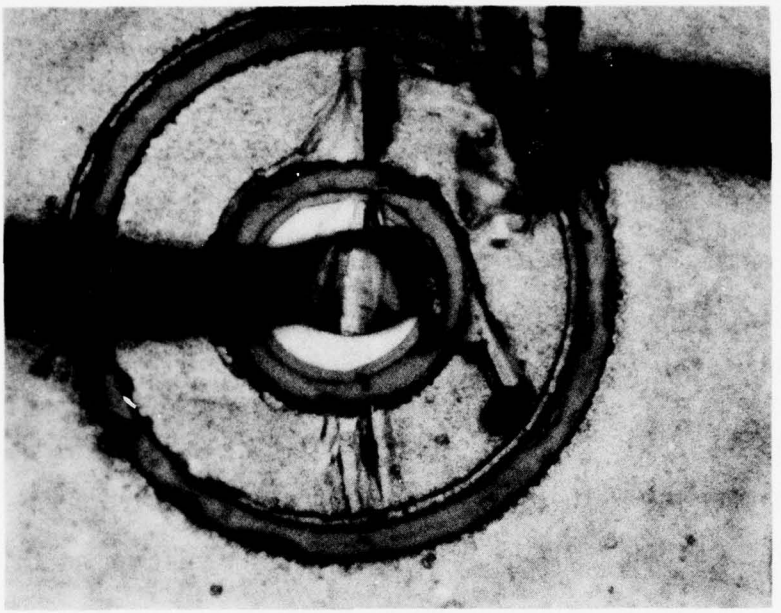
3.3.1 Schottky Barrier Varactor and Gunn

Many problems were encountered in the fabrication of implanted varactors and, near the end of the program, a parallel effort to develop a Schottky barrier varactor and Gunn device combination was started. Figure 51a is an optical micrograph of a finished device with leads attached. The central metallized area is the Schottky barrier varactor and the two outer metallizations are the Gunn contacts. Figure 51b is a drawing of a cross section of the combination device showing the concentric metallizations and series connection. Both the varactor and the Gunn have been tested with probe contacts for C-V and I-V measurements. Circuit testing on this device is described in Section 2.6.

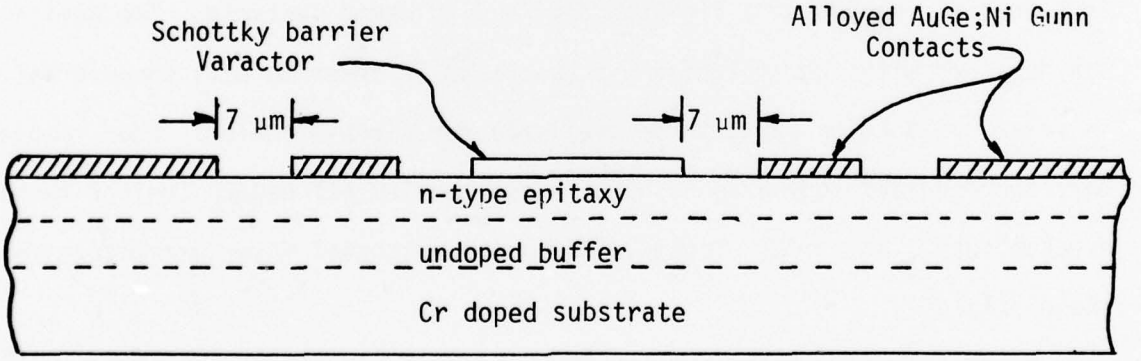
3.3.2 Implanted Varactor and Gunn

An implanted varactor and Gunn combination device was also attempted. Figure 52a is a cross section drawing of this device and Figure 52b is a photomicrograph of a finished device with ohmic contacts. The device was designed with two implanted p-n junctions in order to have some variation in varactor junction capacitance available for circuit tuning. Four samples were prepared and implanted at NRL. These samples all had Au implant masks greater than 1 μm thick. Table VI lists the epitaxial layer parameters for these samples.

Probe measurements of the I-V characteristics were made at each stage of the fabrication procedure. Figure 53 shows the initial characteristics of 714-1 after removal of the Au implant mask and before annealing. With both probes on the same implant region, very high resistance (.6 M ohm) ohmic characteristics were obtained. The probe measurements on the unimplanted

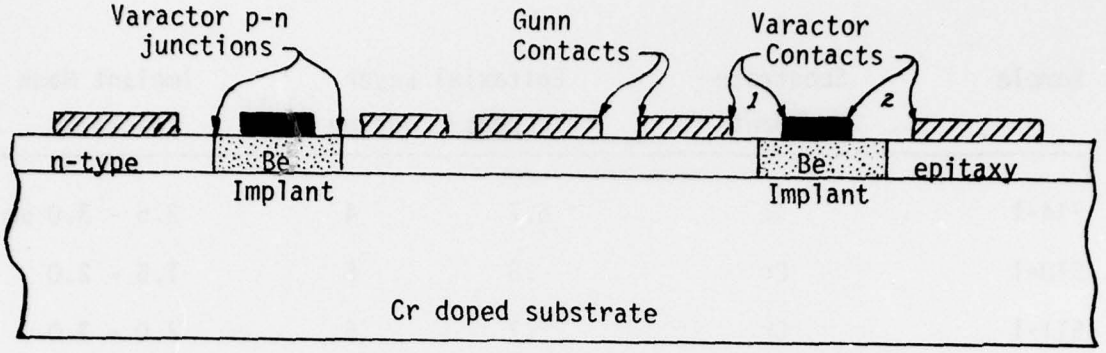


(a)

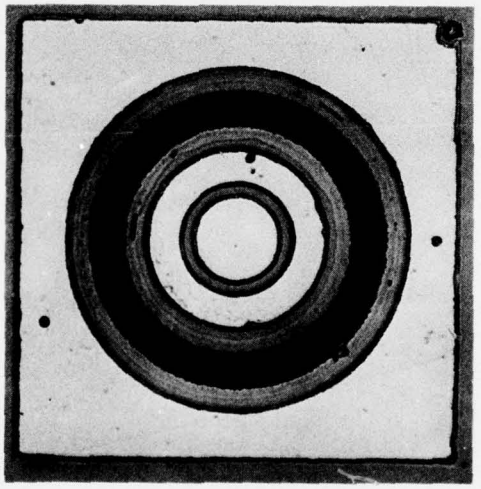


(b)

Figure 51. Planar Gunn Varactor Combination



(a)



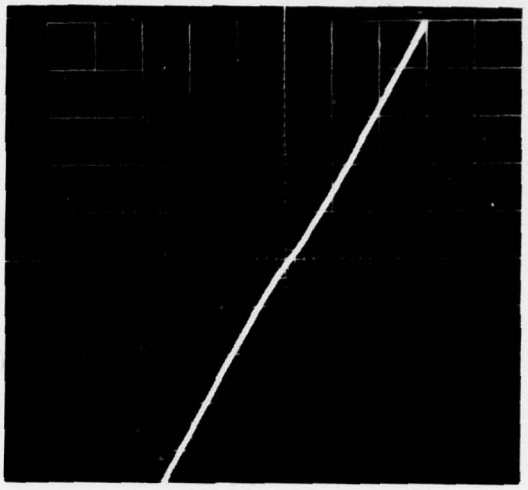
(b)

Fig. 52. Series connected Gunn varactor combination

Sample	Substrate dopant	Epitaxial Layer thickness	Epitaxial Layer doping $x10^{15}$	Implant Mask thickness
714-1	Te	5.7	4	2.5 - 3.0 μm
510-1	Cr	.8	6	1.5 - 2.0
511-1	Cr	.7	6	2.0 - 3.0
513-1	Cr	1.2	8	4.0 - 4.5

Table VI. Epitaxial Layer and Implant Mask Parameters

(a) Both Probes on
Same Implant Region



(b) Both Probes on
Unimplanted Region

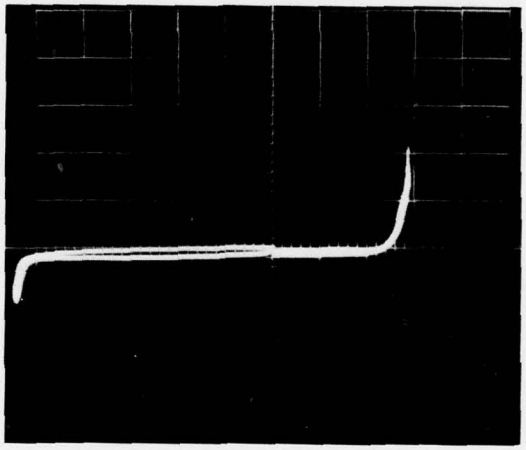


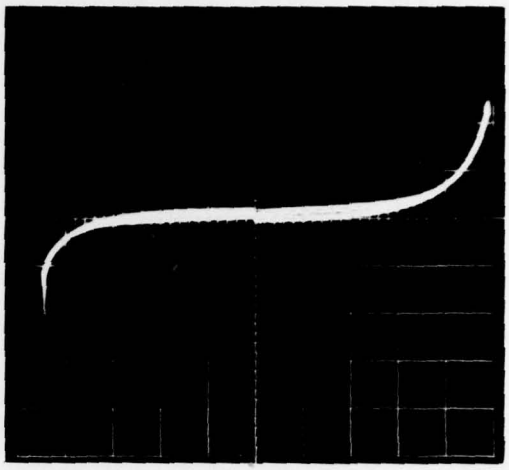
Fig. 53. Sample 714-1 Before Anneal (.01 ma/cm, 10 V/cm)

regions (n-type epi) of 714-1 show breakdowns of 20 to 50 volts. These are typical of the probe measurements made on all four samples. None of the samples had the fatal highly doped p-type surface layer at this initial stage of processing.

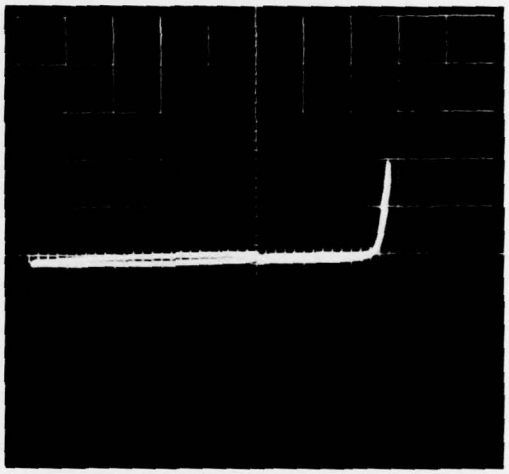
Discussions with NRL personnel revealed that the Be implant could be activated by annealing at 550 °C. Therefore, a small piece of one of the samples (513-1) was annealed for 30 minutes at 550 "C in the ohmic contact alloying system with a forming gas ambient. No p-type surface layer was observed after annealing and probe measurements of these devices showed the best characteristics observed for an implanted planar diode at that time. With this encouragement, larger pieces of 714-1 and 513-1 were annealed in the same manner. Figure 54 shows the I-V characteristics of 714-1 after annealing. This sample was not processed any further at this time since it has a Te doped substrate and was intended to be used to make mesa diodes if the planar process did not work. The 513-1 sample was processed for both n and p-type ohmic contacts to form the completed series connected combination device shown in Figure 52b. Figures 55, 56, and 57 show the I-V characteristics at the different processing steps for the 513-1 sample. A comparison of Figures 55a and 56a shows quite dramatically the effect of the 550 °C anneal. Good diode characteristics were obtained with just quasi-ohmic burned in probe contacts as seen in Figure 56b. When the alloyed p^+ ohmic contacts were added, better forward characteriwtics were obtained (Figure 56c). The processing and second alloy step for the n-type ohmic contacts were very detrimental to the forward characteristics (Figure 57a and b). The reason for the change in forward characteristics is not known. The change was quite unexpected, since the alloying for the P^+ contacts was done at 600 °C and improved the devices while the n-contacts were alloyed at only 480 °C. Figure 57c shows

(a) Both Probes on Same Implant Area

(.01 ma/cm, 10 V/cm)



(b) Both Probes on Unimplanted Area



(c) "Burned in" Ohmic Contacts to n-epi and Implanted Areas

(.01 ma/cm, 1 V/cm) forward

(.01 ma/cm, 5 V/cm) reverse

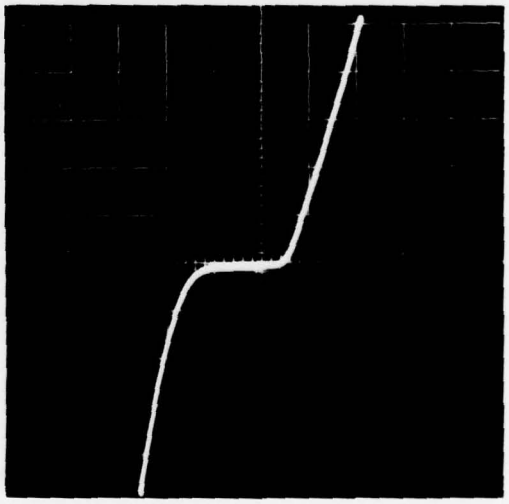
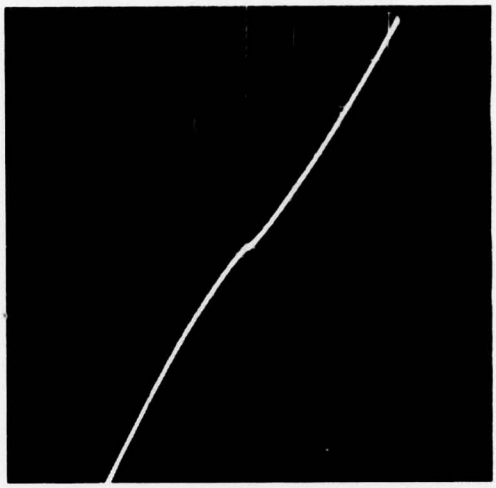


Fig. 54. Sample 714-1 After 30 Min. Anneal at 550°C

(a) Both Probes on Same Implant Area



(b) Probes on Different Implant Areas (unimplanted n-epi between)

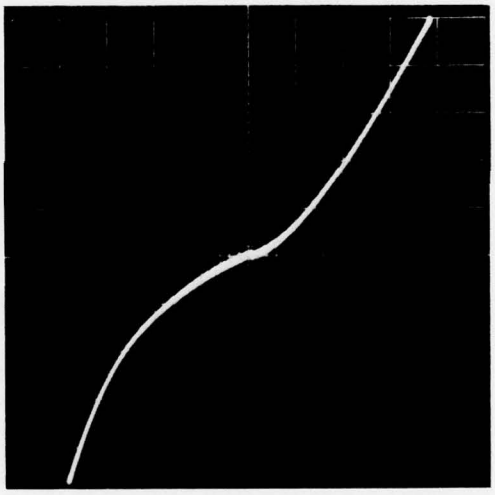
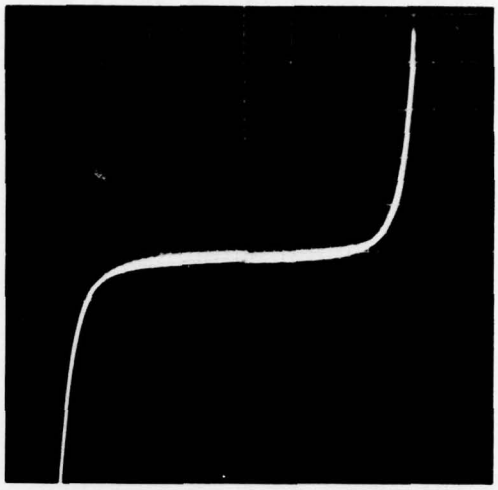
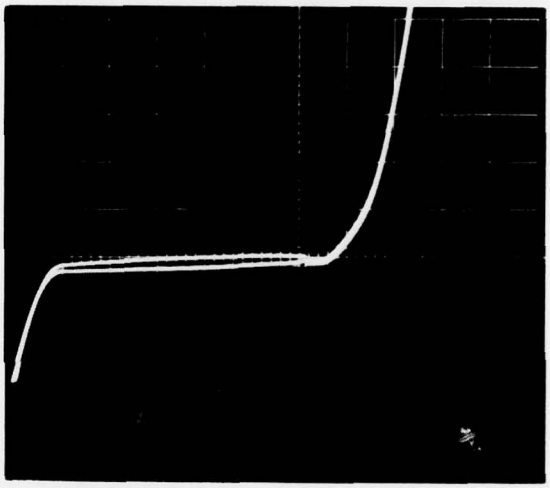


Fig. 55. Sample 513-1 Before Anneal(.01 ma/cm, 10 V/cm)

(a) Both Probes on Same
Implant Area
(10 V/cm, .01 ma/cm)



(b) "Burned in" Ohmic Contacts
to n-epi and p^+ Implant
Forward(1 V/cm , .01 ma/cm)
Reverse(20 V/cm , .02 ma/cm)



(c) Alloyed p^+ Contact
"Burned in" n-epi Contact
Forward(1 V/cm , .01 ma/cm)
Reverse(20 V/cm , .01 mc/cm)

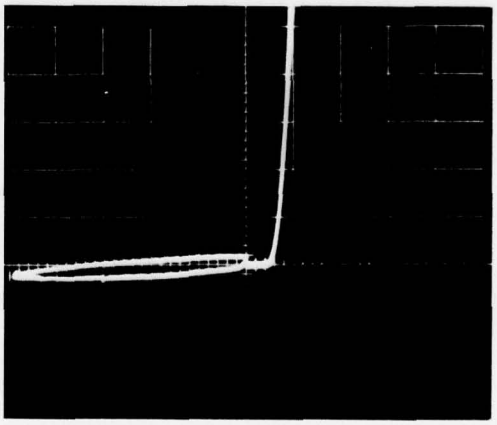
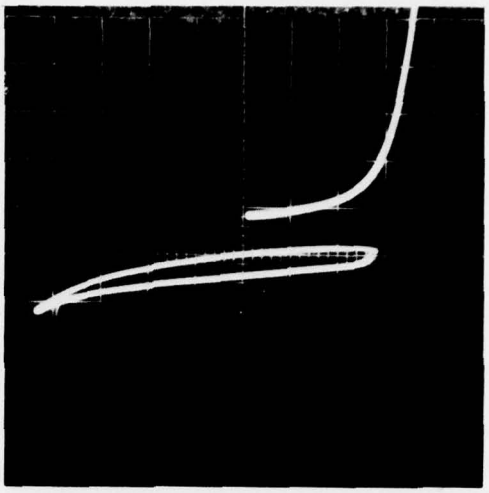
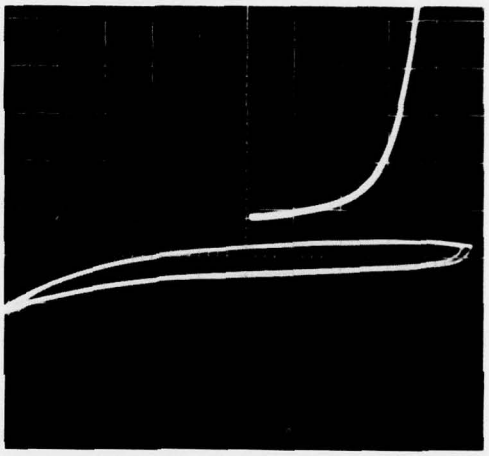


Fig. 56. Sample 513-1 After Anneal

(a) Outer Varactor Junction
Forward(2 V/cm , .01 ma/cm)
Reverse(20 V/cm , .01 ma/cm)



(b) Inner Varactor Junction
Forward(2 V/cm , .01 ma/cm)
Reverse(20 V/cm , .01 ma/cm)



(c) Outer Varactor Contact To
Outer Varactor Contact of
Next Device
(2 V/cm, 10 ma/cm)

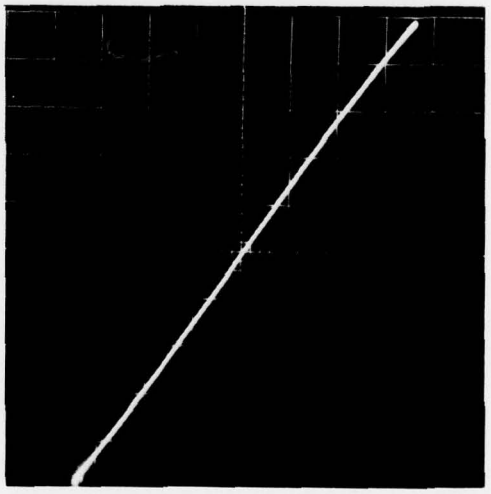


Fig. 57. Sample 513-1 After Second Alloy for Ohmic Contacts
(processing complete)

that the n-type ohmic contacts are good and, therefore, not to blame for the poor forward diode characteristics. A second problem area for this group of devices is revealed by Figure 58a which shows that the Be implant did not isolate the Gunn device from the outer varactor contact. The reason for this is obvious when the impurity profile for the sample is plotted on the same semi-log graph as the Be implant profile. Figure 59 shows that a p-n junction would be formed at about 1.44 microns and a concentration of 4.6×10^{15} atoms cm^{-3}. The impurity profile of samples 510-1 and 511-1 are also included in Figure 59 and show that the Be implant should completely penetrate the epitaxial layer.

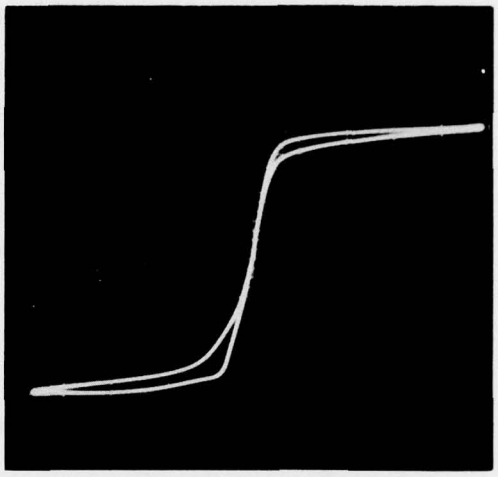
The planar Gunn device I-V characteristics are shown in Figure 58b. The Gunn devices were checked on the curve tracer to determine threshold values, but no further testing or evaluation was done for this material.

Both planar Gunn and varactor devices have been made from the 510-1 and 511-1 material, but a combination device was not completed successfully. The following paragraphs describe what was learned from the attempt to fabricate the combination device from these two groups of material.

Probe measurements taken on the material before annealing are shown in Figure 60. Probe contacts on the implanted region are ohmic and confirm a very high resistivity layer. Measurements taken on the area that was masked during implant show a high breakdown voltage (>200V). Thus, there is no highly doped surface layer present before annealing. The reverse leakage of the probe Schottky barriers on the thin epitaxial layer is light sensitive as shown in Figure 60d.

After careful cleaning, the samples were annealed in the same apparatus used to alloy ohmic contacts. Figure 61 shows the changes in the characteristics of the implanted region with anneal time and temperature. A significant

(a) Outer Gunn Contact to
Outer Varactor Contact
(5 V/cm, 2 ma/cm)



(b) Gunn Device - Center Contact (-)
(5 V/cm, 20 ma/cm)

Fig. 58. Sample 513-1 After Second Alloy for Contacts

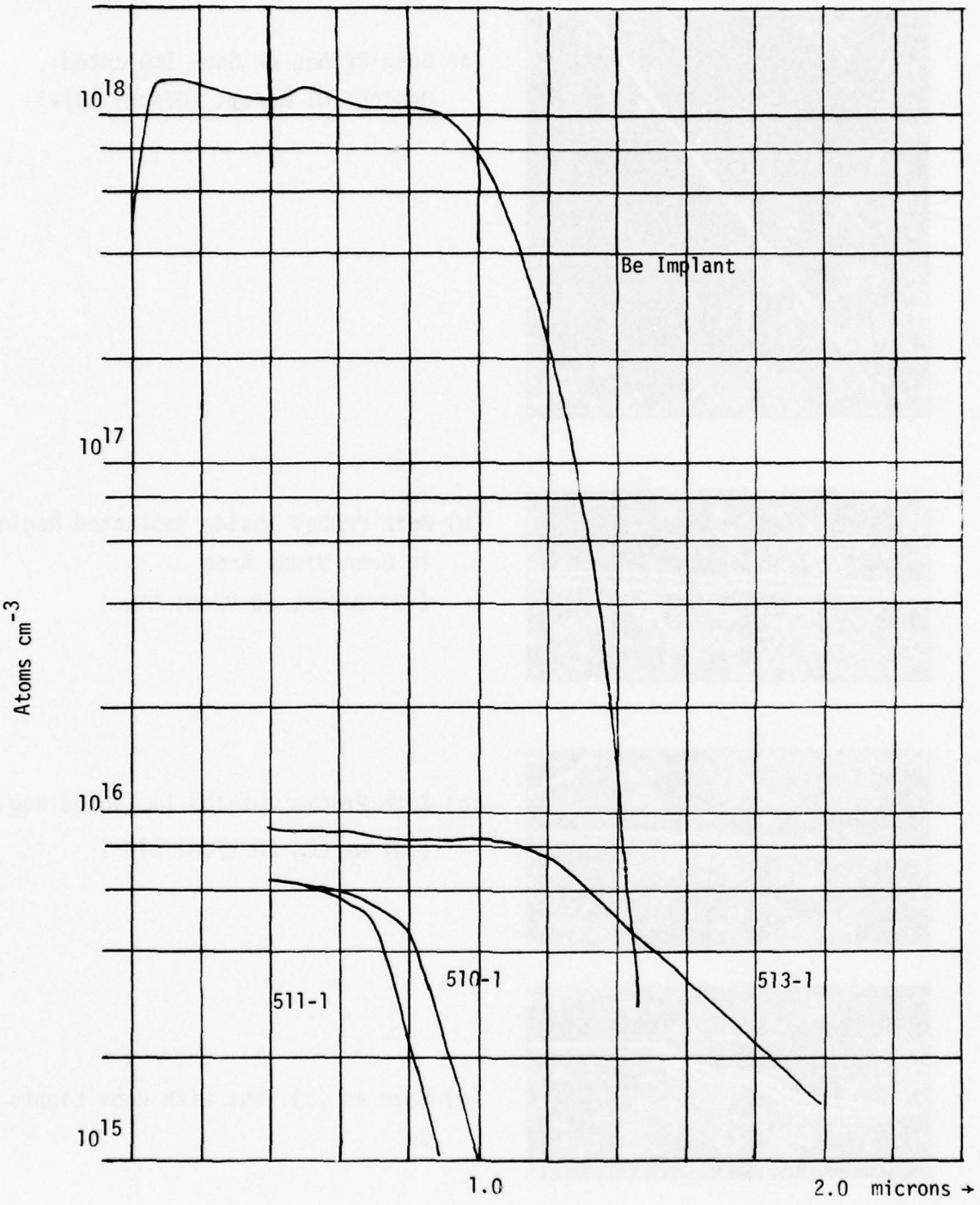
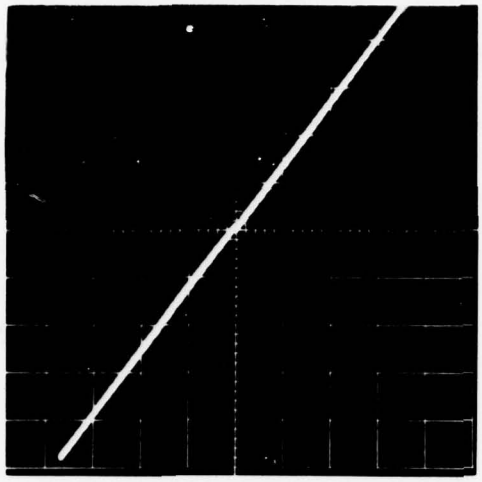
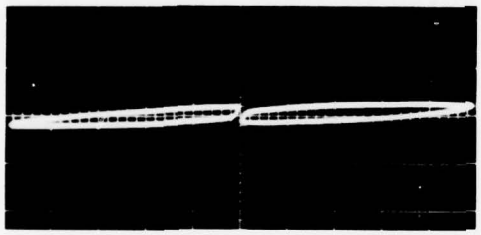


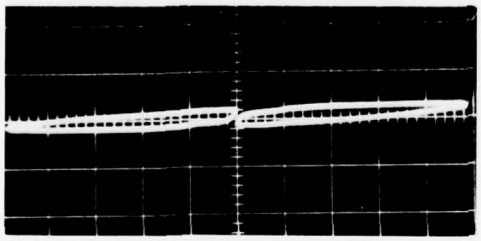
Figure 59. Implant and Impurity Profile for 510-1, 511-1 and 513-1



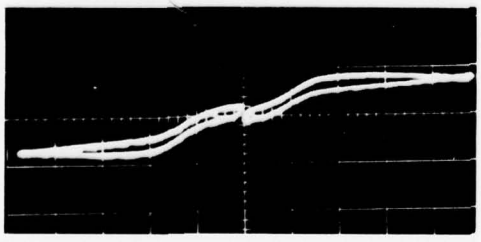
(a) Both Probes on Same Implanted Region(.01 ma/cm, 20V/cm) 511-1



(b) Both Probes Inside Implanted Region in Gunn Diode Area (.01 ma/cm, 20 V/cm) 510-1

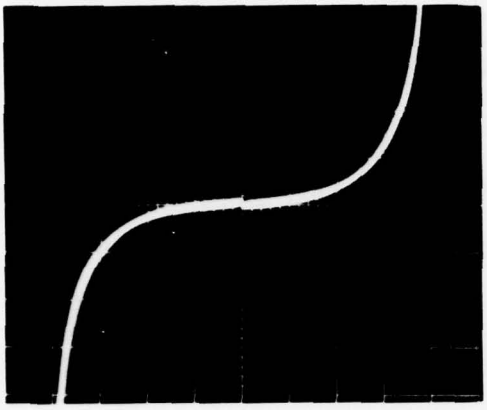


(c) Both Probes Outside Implanted Region (.01 ma/cm, 20 V/cm) 510-1

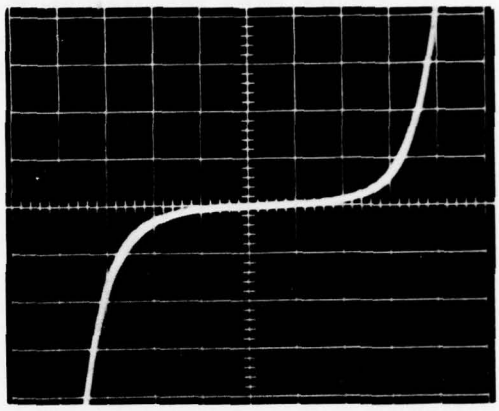


(d) Same as (c), but with Room Lights On

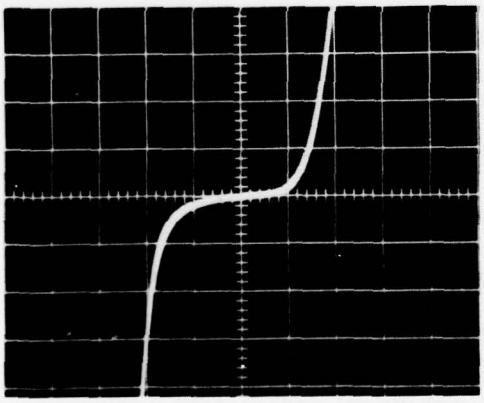
Fig. 60. Probe Measurements Taken Before Annealing



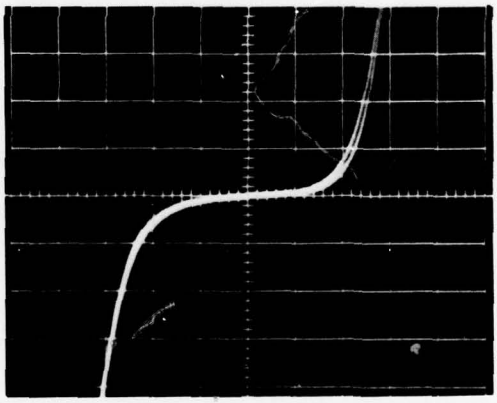
(a) 480°C 30 min.
(.01 ma/cm, 10 V/cm)



(b) 550°C 15 min.
(.01 ma/cm, 2 V/cm)



(c) 550°C 30 min.
(.01 ma/cm, 2 V/cm)



(d) 550°C 60 min.
(.01 ma/cm, 2 V/cm)

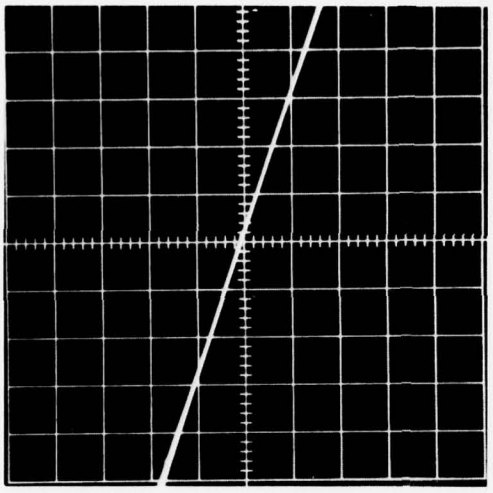
Fig. 61. Probe Measurements on Implant Region After Anneal

activation of the Be implant occurs even at 480 °C and not much change is observed after 30 minutes at 550 °C; thus the rest of the samples treated in this report were annealed at 550 °C for 30 minutes.

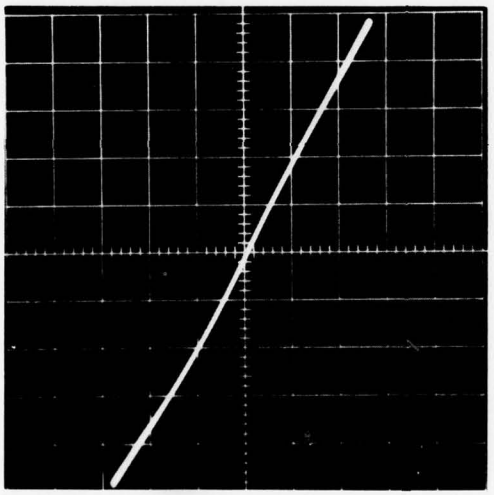
After annealing, the samples were metallized for ohmic contacts. The p and n-type ohmic contact metallization procedures are given in Tables II and III, respectively, and the ohmic nature of these contacts is shown in Figure 62. To test the n-type metallization, the outer varactor contacts for adjacent devices are used. For the p-type metallization a secton of 511-1 large enough to include several adjacent devices was left unmasked during Be implant. Therefore, in this region the p-type contacts were connected by implanted material and the ohmic nature of the contacts could be checked. The contacts are ohmic, but both the p and n-type contacts show a high resistance (800 Ω and 520 Ω, respectively), because the layer is only 0.5 micron thick.

In order to make the combination planar device the p and n-type metallization procedures must be mutually compatible. It is in this area that the most difficulty has been encountered in developing the combination devices. Over twenty slices of substrate or epitaxial material were processed in addition to the 510-1 and 511-1 runs to refine the device fabrication methods. The logical procedure that was first followed was to form the p-type contacts before the n-type contacts because of the higher alloy temperature. However, the dilute aqua regia used to etch the n-type metallization undercuts and lifts the p-type contacts. A double metallization of the p-type contacts using the n-type metallization on top as a mask was also tried, but the p-type contacts were still undercut and lifted by the dilute aqua regia.

A single metallization that would give ohmic contacts to both n and p-type material would eliminate the metallization lifting problem. Therefore,



(a) p-type Ohmic Contact
(1.0 ma/cm, 2 V/cm)



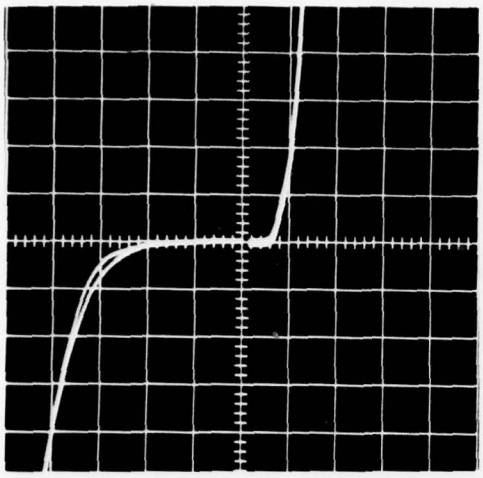
(b) n-type Ohmic Contact
(5 ma/cm, 5 V/cm)

Fig. 62. Confirmation of Ohmic Contacts

the p-type metallization (omitting the Mn) was tried on an n-type epitaxial layer and found to give ohmic contacts. The characteristics of the planar varactor part of the combination device made with the single metallization are given in Figure 63a and b for both implanted p-n junctions. The planar diodes have low reverse leakage and good forward characteristics, but the Gunn part of the combination device was poor (Figure 63c). The modified p-type metallization did not form as good an ohmic contact on the 511-1 epitaxial layer (Figure 63d) as expected from the trial runs. Ohmic contacts are more difficult at the 5-6 x 10^{15} cm^{-3} impurity level of the 511-1 epitaxial layer. The test pieces on which ohmic contacts were made had an impurity level of 1 x 10^{16} cm^{-3}. The poor quality of the Gunn device probably resulted from the poor ohmic contacts.

A fourth procedure that was tried was to form the n-type contacts first. This is the reverse of the natural procedure, since the p-type contacts require a 600 °C alloy temperature. Again, the process was successful on epitaxial layers doped at about 1 x 10^{16} cm^{-3}, but not on the 511-1 material. Figure 64 shows the characteristics of the planar Gunn device taken after the 480 °C alloy for n-type contacts and the degradation of the devices after the 600 °C alloy. The planar Gunn devices were not r.f. tested after the first alloy, but the curve tracer shows characteristics typical of Gunn devices. Thus, both planar Gunn devices and planar varactors have been made on the 511-1 material, but the procedure for the combination device failed.

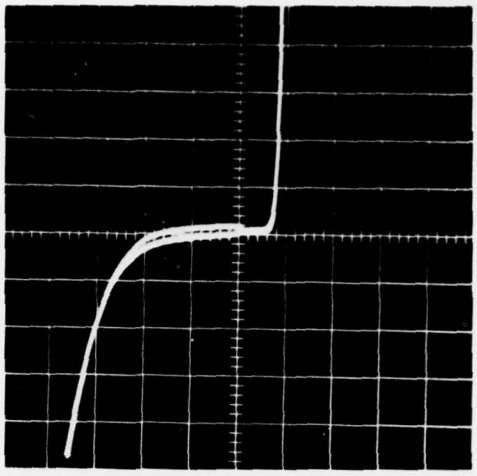
On the other hand, all of the procedures mentioned above produced good planar diodes with properties that are in some cases quite unique. For example, the reverse breakdown voltage of the individual outside and inside junctions given in Figure 65 are greater than 120V, but the breakdown voltage of



.01 ma/cm

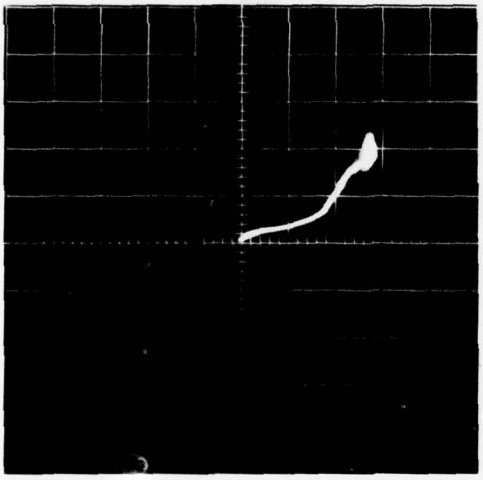
1V/cm Forward

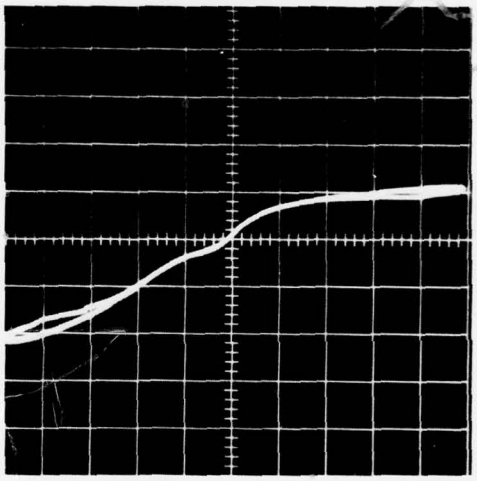
20V/cm Reverse



(a) Outside Junction

(b) Inside Junction

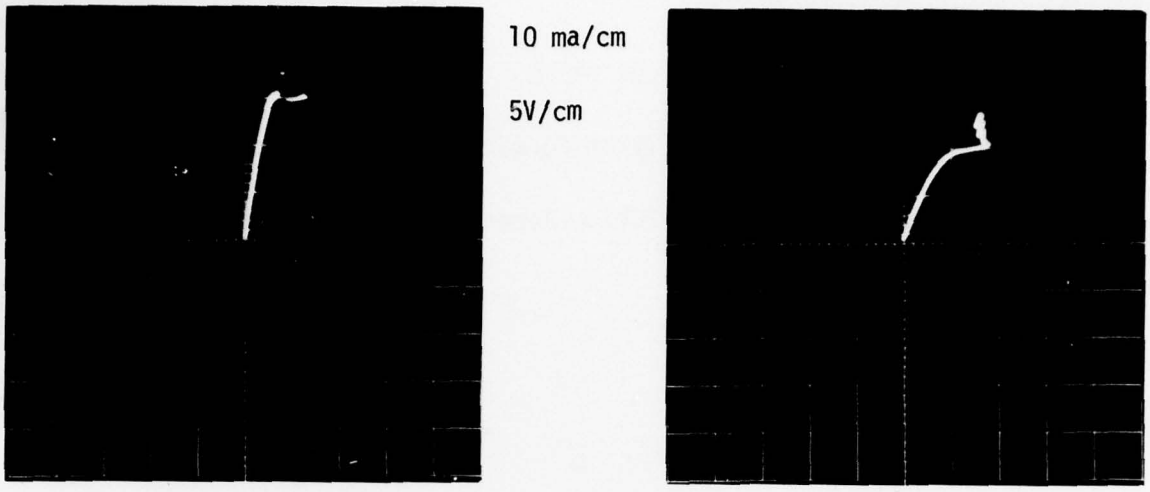




(c) Gunn Device
(2 ma/cm, 5 V/cm)

(d) Outer Varactor Contacts
of Adjacent Devices
(.5 ma/cm, 5 V/cm)

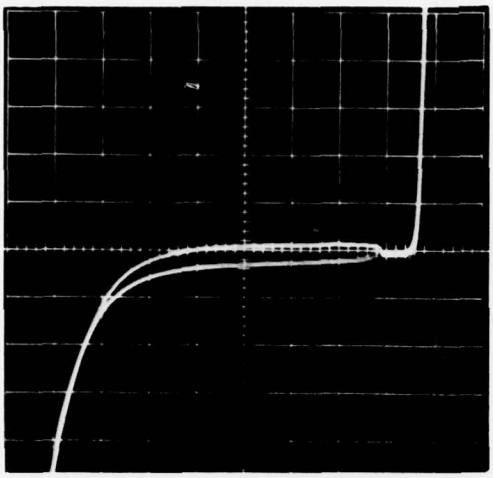
Fig. 63. Planar Varactor Gunn Combination with Ni:AgIn contacts. (Sample 511-1)



(a) After 480°C Alloy

(b) After 600°C Alloy

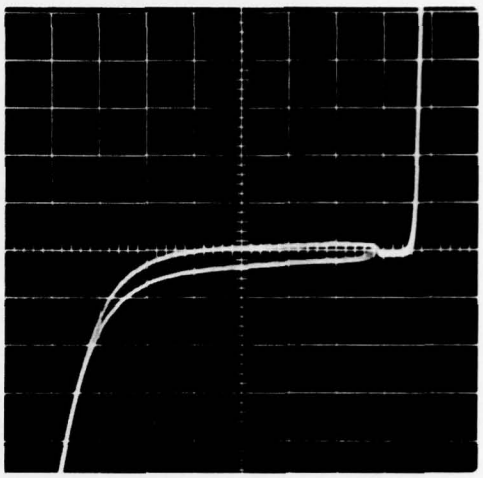
Fig. 64. Characteristics of Planar Gunn Fabricated by Forming the n-type Contacts First



.01 ma/cm

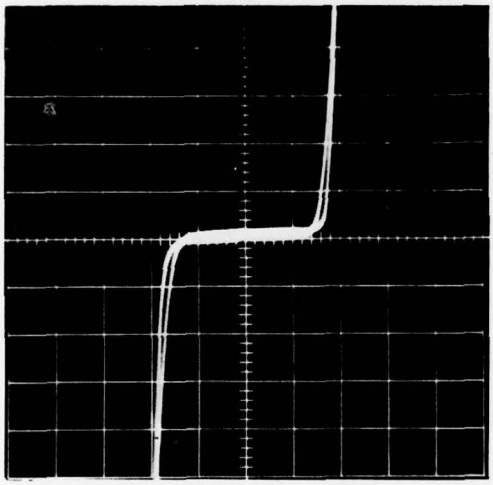
1V/cm Forward

20V/cm Reverse



(a) Outside Junction

(b) Inside Junction



.01 ma/cm

20V/cm

(c) Outside and Inside Junctions in Series

Fig. 65. Sample 511-1 Implanted Planar Diode Junction Properties

the two junctions in series is 38V and symmetric. The implantation seems to be deep enough to completely isolate the two junctions, because when one junction is over-driven to burnout, the characteristics of the outer junction do not change. A second intriguing phenomena observed is that the capacitance of the two junctions in series has a value between the values measured for the individual junctions. Figure 66 is a C-V plot of each individual junction and the junctions in series.

Another interesting property of the implanted planar junctions is their relative magnitudes. Figure 66 shows that the zero bias capacitance of the outer junction is 3.86 times the capacitance of the inner junction. The geometrical area of the implanted junction is proportional to the diameter and the ratio of the diameters of the junctions is only 1.55. Even if it is assumed that the inner junction space charge moves inward 25 microns and the outer junction space charge moves out 25 microns due to the built-in potential, the ratio of the diameters is still only 2.11. Also, from Figure 66, there is little capacitance change for either junction above 1.0V. Thus, the stray capacitance for the outer junction must be about .33 pF and for the inner junction .11 pF. At zero bias, the variable junction capacitance for the outer and inner junctions must be .16 pF and .03 pF, respectively and the ratio of these quantities is 5.33. Thus, there is a large difference between the increase in the measured value of the junction capacitance and the increase in the geometrical area of the implanted junction.

The decreased breakdown voltage for the planar junctions in series is explained by transistor action. With probes connected to the outer Gunn contact, the p^+ contact, and the outer varactor contact a transistor action can be observed as shown in Figure 67. This "transistor" has a base width of 75

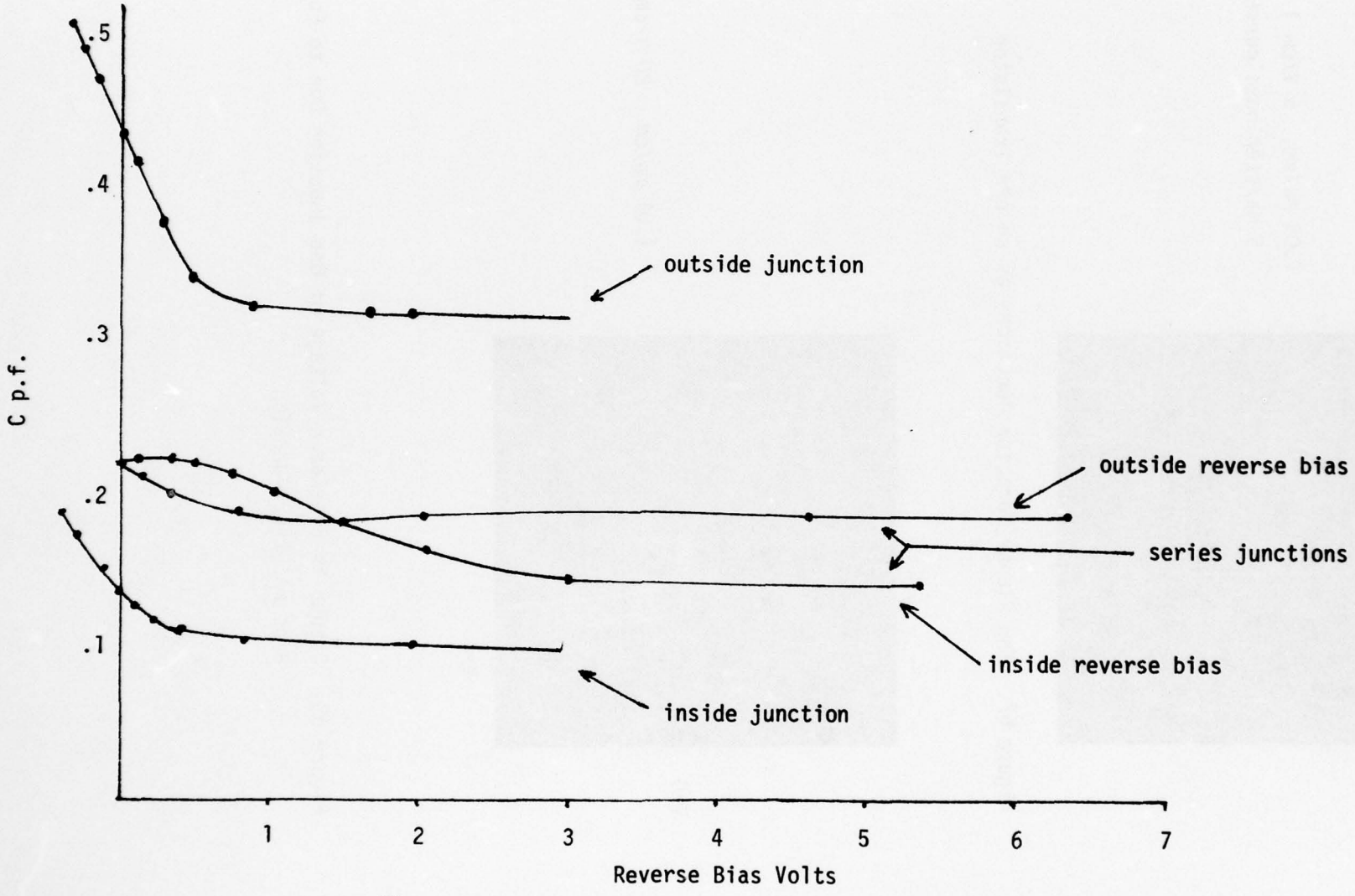
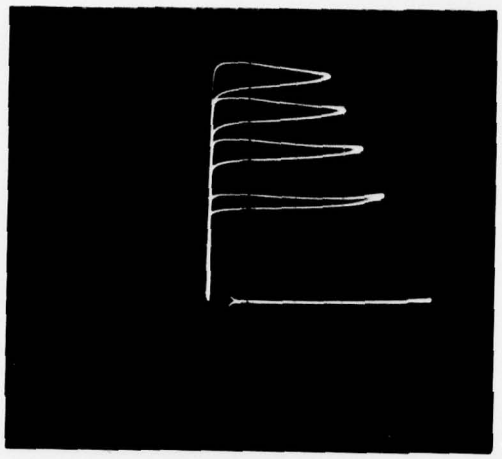
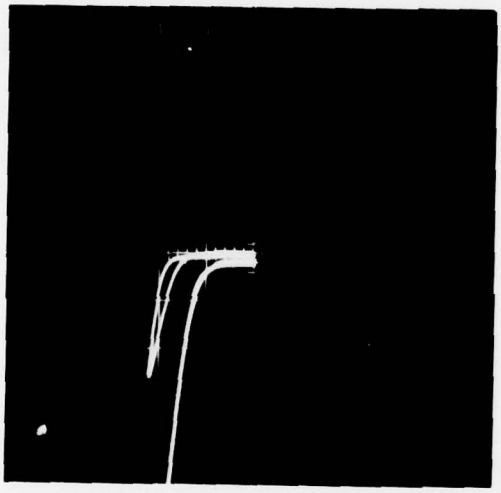


Fig. 66. Capacitance of the Implanted p-n Junctions



(.05 ma/cm, 5 V/cm)
.5 ma/step base current

Figure 67. The Planar Varactor Junctions as an nPn Transistor



V=0

V=1

(.01 ma/cm 20 V/cm)

Figure 68. Change in Breakdown Voltage of One Junction Due to Forward Bias on Other Junction

μm and hence, a current gain of .2, but there is sufficient influence between junctions to change the breakdown voltage. Figure 68 shows the reverse breakdown of one varactor junction when a forward bias V = 0 and V = 1 volt is separately applied to the outer junction. The breakdown is changed from 40 to 20V by a bias of 1 volt. This transistor action is probably also the explanation for the discrepancies in the measured capacitance of the series junctions.

In one of the many tests performed on the planar junctions it was noticed that with enough forward bias the varactor diodes behaved like Gunn devices. Figure 69 shows the high current forward bias characteristics of both inside and outside varactor junctions. At a bias of about 16V it was possible to detect the signal produced with a spectrum analyzer and identify the frequency as 2.1 GHz. No further testing or evaluation of these observations was performed.

3.5 Varactor Modeling

The principal effort in modeling a varactor whose C-V relationship depends upon geometry has been solving Poisson's Equation for the planar varactor. The solution has been obtained in closed form for the circular p-n junction.

The solution of Poisson's Equation for the circular geometry degenerates to the classic one-dimensional solution for an abrupt p-n junction as the radius R gets very large.

The junction capacitance of the circular geometry model can be obtained by using the formulas for the capacitance of a coaxial line providing the width of the space-charge region is small compared to the thickness of the epilayers. As the potential difference across the junction is increased to a point where the width of the space-charge region is of the same order of

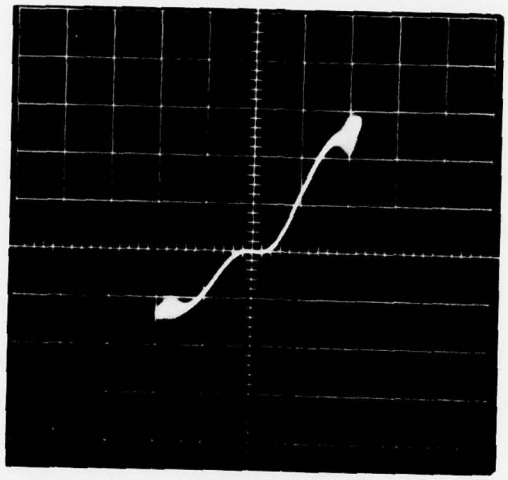


Fig. 69. Gunn Operation Observed in Forward Biased Implanted Planar Diode

magnitude as the thickness of the epilayers, fringing effects become significant. If free-space is assumed next to the exposed face of the planar varactor, the electric field in the space-charge region will tend to remain confined to the space-charge region and not significantly fringe out into the free-space region. Thus, little fringing is expected on the free-space surface on the varactor. However, fringing into the insulating substrate will be significant, since the permittivities of the two regions are approximately the same. The effect of fringing is to increase the total capacitance and decrease the percent change with voltage.

A general technique for solving Poisson's Equation within the space-charge region is required before the C-V relationship for the more complicated device geometries can be obtained analytically. Three analytical methods of either obtaining or checking the solution of free-boundary problems of the type considered here were investigated. First, an iterative solution was formulated using a technique called invariant-embedding and a computer program to implement and test this technique was developed. Secondly, a Green's Function Integral can be evaluated using the results of the invarient-imbedding method to independently verify the solution. Although the Green's Function approach could be used alone to solve the free-boundary problem, the invariant-embedding method appears to yield a more straightforward solution with the Green's Function method serving as a check of the solution. A third approach, using variational inequalities, was also considered. This approach, however, seems to offer no advantages over the former two.

The power of the computer model of the varactor diode was increased by developing an algorithm that permits the analysis of graded, as well as abrupt, planar junctions. Another program modification allows greater range in the

eccentricity for elliptical planar geometries. Both modifications are significant, because they lift restrictions that previously limited the number of configurations which could be evaluated in selecting an optimized diode design.

The solution of the circular planar varactor gives some insight into the potential value of the planar varactor. As the junction radius is made smaller, the C-V characteristics change from those of an abrupt p-n junction, to those of a hyperabrupt p-n junction (i.e., the capacitance is proportional to voltage raised to the minus one-half power for an abrupt junction for large R. As R decreases, the magnitude of the exponent increases.)

Typical calculations (neglecting fringing) for a planar circular varactor with R = 500 μm, a doping concentration of 2×10^{16} cm^{-3} in the n-type GaAs, and an epilayer thickness of 0.5 μm give a zero-bias capacitance of approximately 0.53 picofarads. The capacitance is directly proportional to the epilayer thickness and the doping level of the n-type GaAs. This magnitude of capacitance is lower than is found in typical varactor applications. The capacitance can be increased by increasing R, but the usefulness of this idea is offset by the increase in the physical size of the device. An alternative would be to alter the junction geometry so that for a given average radius, the path length of the junction would be increased. Recent work by Comas et al[6], at NRL indicates that the Be profile extends to a depth of 1.5 μm after a 900 °C anneal. This additional thickness would increase the device capacitance by a factor of three.

SECTION IV

CONCLUSIONS

4.1 MIMINUM PARASITIC VCO STUDIES

The feasibility of constructing lumped element varactor-tuned Gunn Oscillators that operate between 6.0 GHz and 11.5 GHz has been demonstrated. By using state-of-the-art Gunn and varactor chips, greater than octave tuning ranges appear possible with the circuit developed on this program.

The best overall performance of the lumped element circuit was obtained with Varian Gunn and GaAs varactor chips. A tuning range between 6.05 GHz and 11.25 GHz with greater than 15 mW of output power was obtained for 51 volt change in tuning voltage (from about +1 to -50 volts). Although no quantitative measurements were made of the AM and FM noise, the spectrum over the entire tuning range appeared exceptionally clean when viewed on a spectrun analyzer with no evidence of spurious sidebands. The circuit was well behaved and showed no evidence of spurious oscillations, frequency hops, or tuning glitches.

During the experiments with the Varian devices, the tuning voltage was kept below 50 volts to protect the matching capacitors even though the breakdown voltages of the varactor chips were typically greater than 70 volts. Extrapolating the tuning curve indicated an additional 700 MHz would have been obtained if the tuning voltage had been taken to 70 volts. Also allowing positive bias, a total tuning range of 5.9 GHz (6.05 to 11.95) or 0.1 GHz less than an octave would have been obtained with these devices.

Almost equal performance was obtained with the Microwave Associates Gunn chips and Sperry multimesa silicon varactor chips, despite the latter's lower

breakdown voltage (approximately 45 volts). A tuning range between 5.6 GHz and 10.9 GHz was obtained with this combination for 40.6 volt change in tuning voltage (+0.6 to -40 volts). This compares favorably with the tuning range obtained with the other combination in terms of an overall modulation sensitivity, i.e., $\Delta f/\Delta V$. These ratios (considering a voltage change from 0 to -40 volts) were 115 MHz/volt for the Varian devices and 122 MHz for the MA-Sperry devices.

These comparisons are made to show the repeatibility of the circuit rather than to differentiate between the various devices. It is felt that the slight difference here was due mainly to the better "match" between the Microwave Associates Gunn and Sperry varactor and not to differences in the $\Delta C/C_o$ ratios of the varactors.

Although hyperabrupt tuning varactors were not tested in these circuits, a few experiments were conducted using low-high-low GaAs IMPATT devices as tuning varactors. Previous capacitance measurements on these devices indicated rather dramatic changes in capacitance with applied voltage similar to what one would expect from hyperabrupt devices. Relatively linear tuning was obtained with these devices over a 2.5 GHz range with less than a 15 volt change in tuning voltage. The measured data indicated a maximum deviation of 1.3% from a "best fit" line.

Planar Gunn and varactor devices were developed and tested in microwave circuits. In a particular circuit, the planar Gunns operated at lower frequencies than conventional Gunns. A planar Gunn-varactor device, mounted in the lumped-element circuit used in the tests described above, oscillated in the 2 GHz to 4 GHz range at power levels of several milliwatts. Although the operating frequency and power level were lower than that obtained with conventional devices, the tests were encouraging in that tunable oscillations were

obtained with a single planar Gunn-varactor chip.

The single-chip pGv tests and the lumped-element tests using conventional chips demonstrate the relizability and desirability of lumped-element monolithic VCOs and their potential in increasing the tuning bandwidth of VCOs.

4.2 PLANAR DIODE

Procedures have been developed for ohmic contacts to substrates, n^+ (Se) implants, and p^+ (Be) implants. Some problem remains in the compatability of the two procedures done on the same material, but this can certainly be solved. Probably the single p-type metallization (omitting the Mn) would work for both p and n-type contacts if they are implanted to give a highly doped surface.

Implanted p-n junctions in both mesa and planar form were evaluated and found to be of good quality. Many problems were encountered with the fabrication of the planar diodes. These problems were solved, but only after a major portion of the second year's effort was expended. The solution found involved only Be implants. Thus, for a device that requires Se implants, a first step would be the development of a reliable encapsulation and anneal procedure.

Some of the necessary procedures were developed with very few problems. Very good device isolation was achieved with proton bombardment on the first try. Planar Gunn devices were also fabricated with little difficulty, but were not developed fully because of the effort required on the implanted planar diodes.

The good planar diodes evaluated at the end of the program had a small capacitance value, because the material was selected for maximum space charge

motion with bias. It is only within the limits of this space charge motion that a geometrical tuning of the C-V relation may be expected for a planar varactor. As the doping level in the epitaxial layer increases, the capacitance of the varactor increases, the space charge motion decreases, and a much more critical masking restriction prevails. The geometrical tuning of the C-V relation is, therefore, not practical. A planar ion implanted vertical junction diode is, however, a practical device and may have many applications in the future in GaAs monolithic circuits.

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