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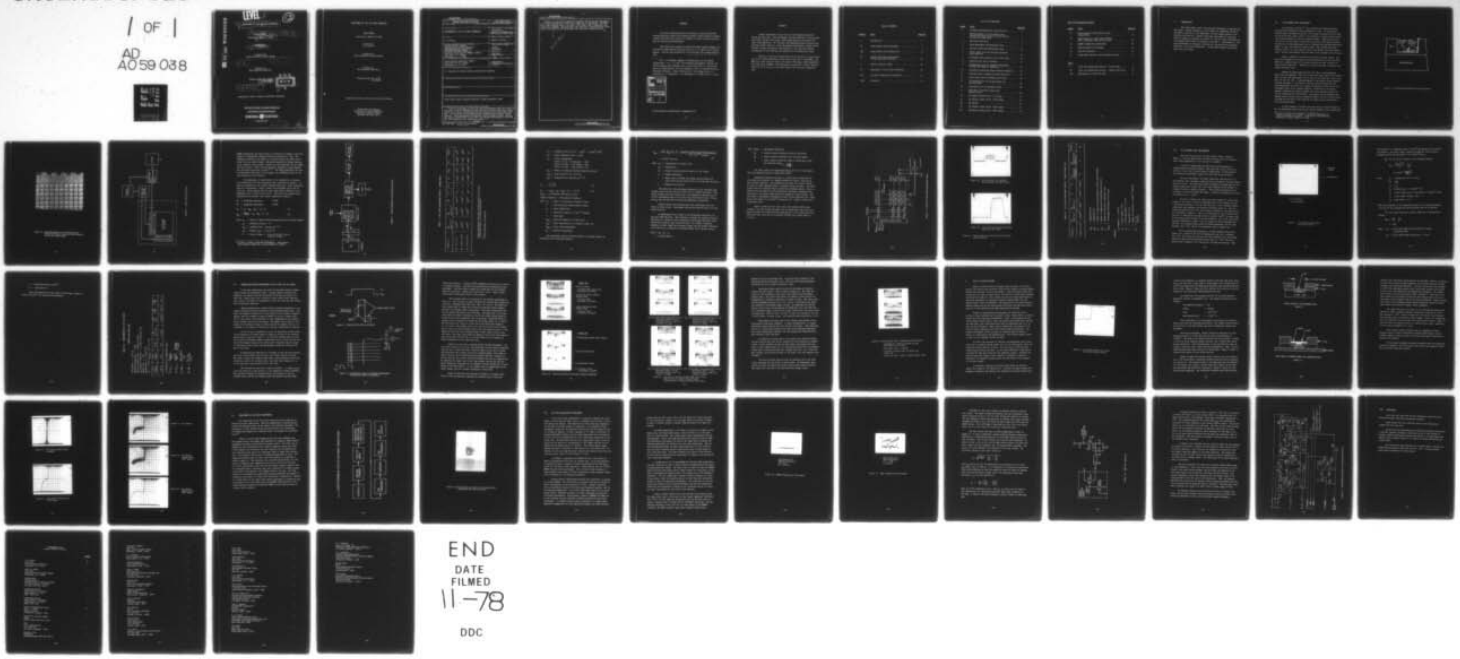

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DEVELOPMENT OF InSb CID ARRAY TECHNOLOGY.

FINAL REPORT. May 77-Feb 78,

Contract No. N00173-77-C-0241

Prepared by:
W. E. Davern

Sponsored by:
Naval Electronic Systems Command

57p.

Jul 78

Directed by:
Naval Research Laboratory

Program Project No. 62762N
XF54583004

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OPTOELECTRONIC SYSTEMS OPERATION

ELECTRONIC SYSTEMS DIVISION

GENERAL ELECTRIC

Syracuse, N.Y.

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Further improvement on both line and two-dimensional InSb CID arrays has been made. Array performance has been improved by using thinner-gate oxide, thicker field oxide, lower-doping substrate materials, and lower noise amplifier. The co-planar two-dimensional array structure also has been further improved. Array performance efficiencies, (which include transfer, quantum and readout efficiencies) of over 30%, and transfer efficiencies of over 98% have been measured on two dimensional arrays.

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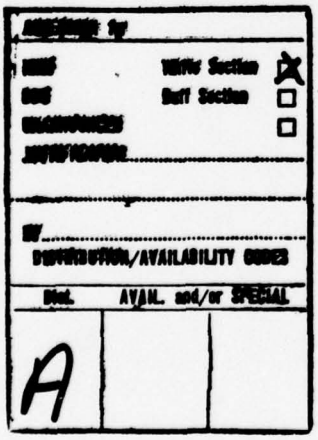
micrometers

FOREWORD

This Final Technical Report was prepared by the Optoelectronic Systems Operation of Electronic Systems Division, General Electric Company, Syracuse, New York under Contract No. N00173-77-C-0241, entitled "Development of InSb CID Array Technology".

This effort was sponsored by Naval Electronic Systems Command, and directed by Naval Research Laboratory with Dr. W. D. Baker as the Project Monitor. The work was performed for the period May 1977 through February 1978.

Mr. L. A. Branaman, Manager of Engineering, was the Program Administrator. Dr. J. C. Kim*, the Principal Investigator, directed the overall program until September 1977, after which time W. E. Davern was given the responsibility of Project Engineer, and M. D. Gibbons served as Technical Consultant. Other contributors to the program were E. M. Littebrant, J. B. MacHaffie, V. M. Meikleham, J. M. Swab, and M. L. Winn.



*Joined Rockwell International in September 1977.

ABSTRACT

Further improvement on both line and two-dimensional InSb CID arrays has been made. Array performance has been improved by using thinner-gate oxide, thicker field oxide, lower-doping substrate materials, and lower noise amplifier. The co-planar two-dimensional array structure also has been further improved. Array performance efficiencies, (which include transfer, quantum and readout efficiencies) of over 30%, and transfer efficiencies of over 98% have been measured on two dimensional arrays.

Effort on a low-noise preamplifier has been carried out and performance of the JFET preamplifier is much better than that of the MOSFET. The NETD for a line array was found to be about $0.1^{o}K$ using a JFET preamplifier and $0.5^{o}K$ using a MOSFET. The measurement was made with a narrow spectral filter of 3.6 to 4.0 μm, f/3.25 lens system, and a 500 μsec integration time.

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Table

I. INTRODUCTION

This Final Report covers the continued development of InSb MIS and CID arrays. Further progress on 16x24 element two dimensional arrays is described in Section II, and measurement of 32x32 element arrays is described in Section III. Transfer efficiency measurements on dual gate InSb CID arrays are discussed in Section IV. The work with p-diffused and ion-implanted InSb diodes is presented in Section V. Improvements in line array performance is discussed in Section VI, and Section VII discusses efforts on a low noise preamplifier. Section VIII contains conclusions drawn from this effort.

II. 16x24 ELEMENT ARRAY DEVELOPMENT

As previously reported [1], the co-planar two-dimensional array structure has exhibited the best performance to date. In the previous parallel gate overlapping structure, the top gate oxide was twice as thick as the bottom gate oxide so that it was difficult to create the deep potential wells necessary for effective charge transfer. Reducing the thickness of the top gate oxide to overcome this problem often caused shorting between the two overlapped gates, and it increased the coupling capacitance which, in turn, contributed to pattern noise. The coplanar structure, however, results in a more uniform output video signal, with less pattern noise. Further improvements have been made in the coplanar array structure.

Figure 1 shows the structure of an earlier coplanar device. The gold layer bridging the two gates provided continuity over the steep step. However, it obscured some of the infrared collection area, and thus reduced optical sensitivity. Therefore, an effort was made to eliminate the opaque gold metal layer.

Instead of using opaque gold over the step, a semitransparent metal layer was employed. This is the same metal layer used for the second gate; in fact, the metallization can be done at the same time, both on the gate and over the step. A photomicrograph of the current array structure is shown in Figure 2. The whitish lines are metallized gold bus line interconnections, and there is no opaque gold layer over the step in the overlapped region of the sensing elements. Evaluation of this array geometry indicates that charge transfer does occur properly between the row and column gates in each element. This means that the coplanar overlapping array structures can be fabricated without the use of a gold layer to bridge the two gates, thus resulting in simpler array structure and fewer processing steps.

A block diagram of the InSb array test setup is shown in Figure 3. The two dimensional InSb array and the silicon scanners, which contain the

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[1] J.C.Kim, W.E.Davern, D.Colangelo, "Continued Development of Indium Antimonide CID Arrays". Final Report, Naval Research Laboratory, Contract N00173-76-C-0128.

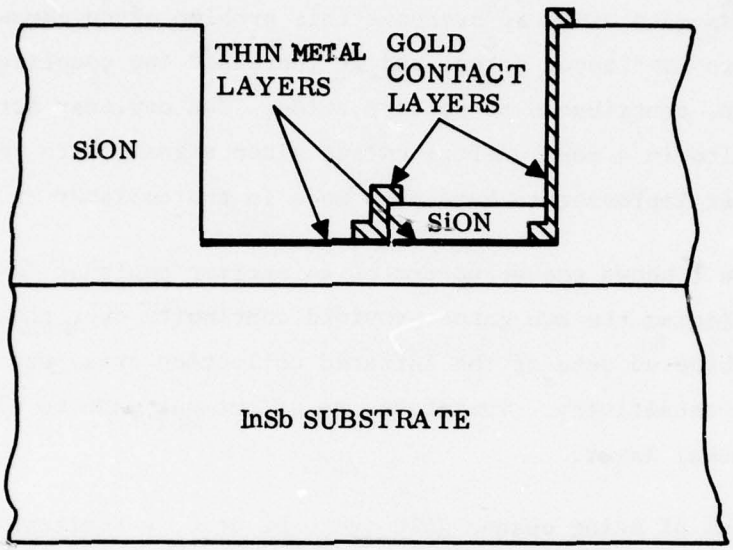

Figure 1. Co-Planar Two-Dimensional Array Structure

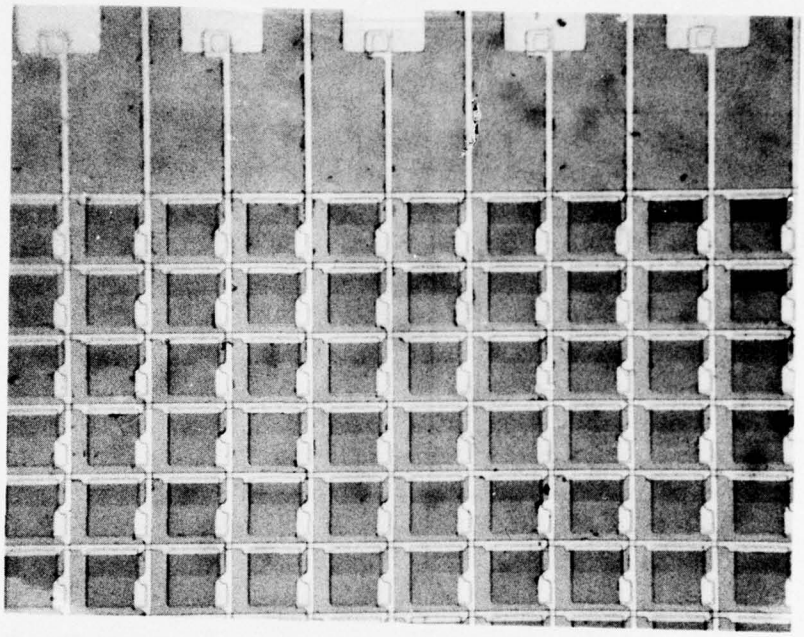

Figure 2. Photomicrograph of the Co-planar Array Fabricated Without Using Gold Layer Between the Row and Column Gates.

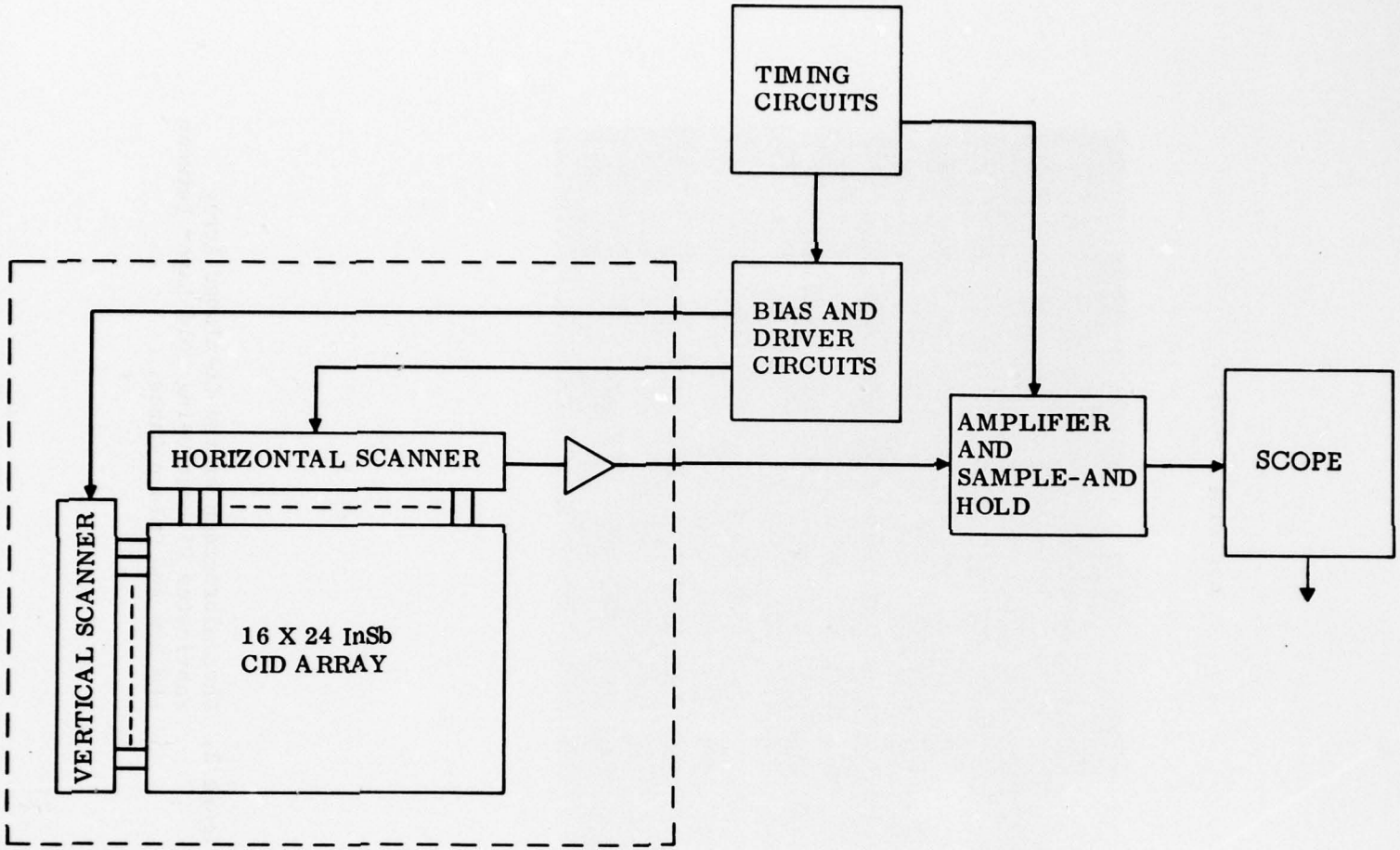

Figure 3. InSb Array Test Setup

MOSFET preamplifier and reset switch, are mounted in a header on the cold finger of a demountable cryogenic dewar and operated at ~ 77°K. The remaining electronic test circuitry is mounted outside the dewar, partitioned into two circuit boards. One board contains the timing, bias and driver circuits, and the other contains the video amplifier and the sample and hold circuits. These circuits and their associated timing diagrams were previously explained in detail[1) 2)]. The JFET preamplifier was used in measurements made later in the program, but a MOSFET was used for the data presented in this section.

One measurement of significance is the responsivity or performance efficiency of the two dimensional array (electrons per photon). An array was connected in the staring (imaging) mode with a frame integration time of 3 milliseconds. Figure 4 shows the measurement setup used for this test. Array response data was then taken using 3 different filter bandwidths, with a field of view of 30°. Important test parameters and equations are as follows, with results summarized in Table I:

BB = Blackbody temperature = 873°K

BG = Background temperature = 293°K

$$N_P = A_A \cdot P_{BB} \cdot \Omega_E/\pi \cdot T_I \cdot T_F \qquad (1)$$

$$N_{PB} = \frac{\Omega_{(FOV)}}{\pi} \cdot A_E \cdot P_{BG} \cdot T_I \cdot T_F \qquad (2)$$

where N_P = Number of signal photons/integration period (chopped signal)

A_A = Blackbody aperture - m^2

P_{BB} = Blackbody flux, photons sec^{-1} m^{-2}

A_E = Element area = 2.5×10^{-9} m^2

R = Source Distance = 0.5m for filters 1 and 2, 0.25m for filter 3

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2) J.C.Kim, J.M.Swab, "InSb MIS Development". Final Report, Naval Research Laboratory, Contract N00173-77-C-0022.

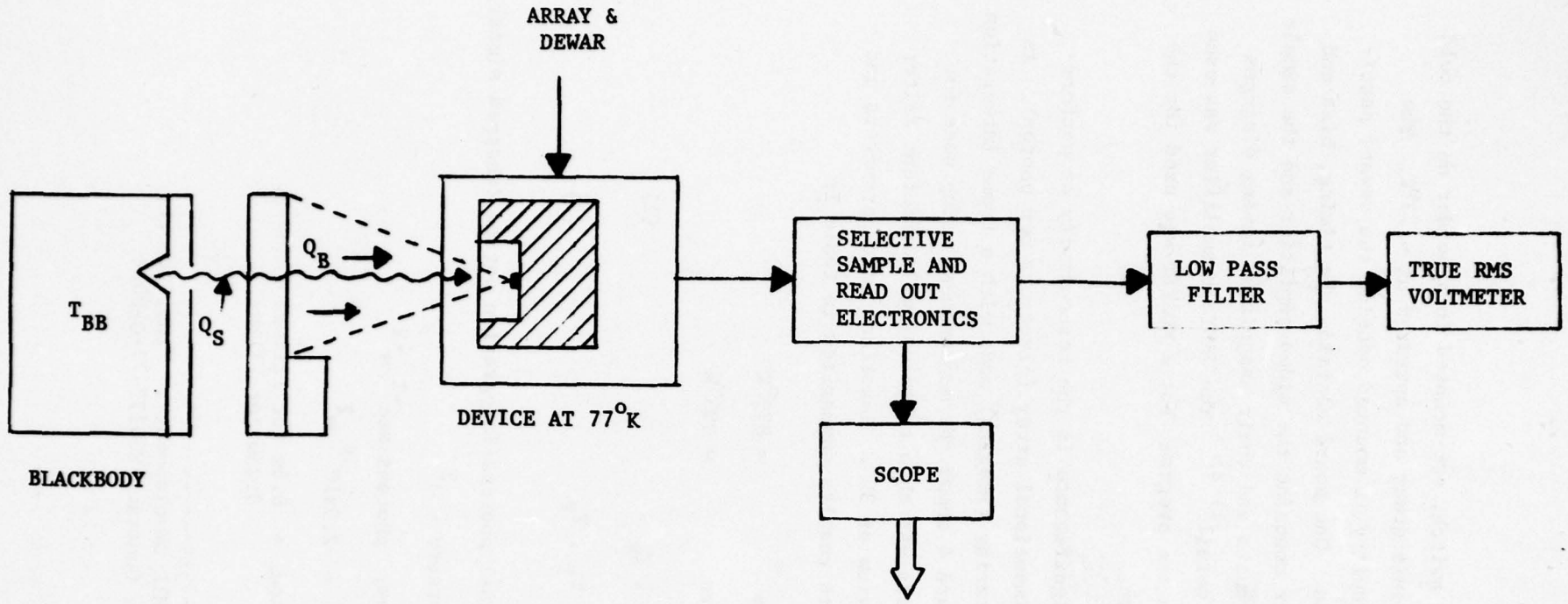


Figure 4. Array Measurement and Evaluation Setup

TABLE I. 16x24 ARRAY MEASUREMENT RESULTS - STARING MODE

Filter $\Delta\lambda$	P_{BB} $Psec^{-1}cm^{-2}$	P_{BG} $Psec^{-1}cm^{-2}$	Ω_E	R m	T_F	N_P	N_{PB}	N_e	$*N_e/N_P$
#1 3.5 to 5.6	$2.6x10^{23}$	$2.36x10^{20}$	$1x10^{-8}$	0.5	.8	$6.7x10^{7}$	$1x10^{8}$	$1.3x10^{6}$	$.02^{**}$
#2 3.68 to 4.165	$5.9x10^{22}$	$1.5x10^{19}$	$1x10^{-8}$	0.5	.8	$1.1x10^{7}$	$6.9x10^{6}$	$7.7x10^{5}$	$.086^{**}$
#3 3.63 to 3.66	$4.2x10^{21}$	$5.3x10^{17}$	$4x10^{-8}$	0.25	.35	$1.45x10^{6}$	$1.12x10^{5}$	$4.8x10^{5}$	.33

*Array performance efficiency includes Transfer Efficiency, Quantum Efficiency, and Readout Efficiency.

**Array operating in saturation.

Ω_E = Elemental field of view = A_E/R^2 = 2.5×10^{-9} m^2/R^2

T_I = Frame integration time = 3 msec

T_F = Filter Transmission

Filter 1 (3.35 - 5.60 micron) = 80%

Filter 2 (3.681 - 4.165 micron = 80%

Filter 3 (3.625 - 3.660 micron) = 35%

N_{PB} = Number of background photons/integration period

Ω_{FOV} = Array field of view = 0.25 SR

P_{BG} = Background flux, photons sec^{-1} m^{-2}

$$N_e = \frac{V \cdot C_T}{e \cdot G} \qquad (3)$$

$$C_T = C_{INJ} + C_{SH} + C_{COL} + C_A = 22.7pF \qquad (4)$$

N_e/N_p = performance efficiency at array

Chopper frequency << than sampling frequency.

where N_e = number of electrons at amplifier input

V = Peak-to-Peak AC chopped signal voltage

C_T = Total capacitcance

e = Charge per electron = 1.6×10^{-19} coulomb

G = System gain

C_{INJ} = Injection capacitor on enable line

C_{SH} = Shunt capacitance due to scanner, leads, etc.

C_{COL} = Array column capacitance.

C_A = Amplifier capacitance.

The approximate electron storage capacity of an array element is determined by the following equation:

$$N_{SAT} = \frac{C_{OX} \cdot A_E \cdot V_I \cdot n_r}{2\,e} = \frac{(3.0\times10^{-8}\ F/cm^2)(2.5\times10^{-5}cm^2)(1.6V)(0.7)}{(2)(1.6\times10^{-19}\ coulomb)} \quad (5)$$

$$= 2.59\times10^{6}\ \text{electrons}$$

where C_{OX} = Capacitance of the gate oxide

A_E = Element area

V_I' = Injection pulse amplitude applied to the element

n_r = Readout efficiency

2 = Factor used to account for charge sharing between the equal sized row and column cells in the dual gate structure.

e = Charge on an electron.

This shows that the approximate saturation for an overlapped gate transfer device with an area of 2.5×10^{-5} cm^2 is 2.59×10^{6} electrons. This charge storage limitation explains why the performance efficiency was so low for measurements made on the array using broad band filters. The N_P and N_{PB} were too high and the array was operating in saturation.

Similar results were obtained when these experiments were performed on other arrays. Performance efficiencies measured were 32 to 35%, using filter #3.

An approximation can be made of the performance efficiency of a dual gate InSb CID array. This efficiency includes the quantum collection efficiency of a discrete device (dependent on metal gate electrode transmission and perimeter edge collection area), the transfer efficiency (dependent on gate length and interface states) and the readout efficiency of the structure (a function of substrate dopant level and gate oxide):

$$N_e/N_P = Q_E \cdot T_E \cdot n_r$$

$$= (0.5)(0.98)(0.7)$$

where N_e/N_p = performance efficiency

Q_E = discrete detector quantum collection efficiency

T_E = charge transfer efficiency for 1 mil gate length

n_r = device readout efficiency based on initial gate oxide and substrate dopant $(1 - \frac{C\ MIN}{C\ MAX})$

For these arrays, the approximated N_e/N_p of 34% is in good agreement with measured results on unsaturated arrays.

Additional evaluation was done on a 16x24 array, operating with one column wired directly to a MOSFET preamplifier source, reset switch and injection capacitor. The preamplifier was used as a source follower to drive the video amplifier which is located outside the dewar. The background level was increased using an additional blackbody source. Refer to Table II for the results of this performance efficiency measurement when operating in the single column scan mode, sequential inject readout. For this array, a performance efficiency of about 38% was measured with a background flux density of 1.213×10^{15} photons/sec-cm^2. Figure 5 depicts this measurement setup.

Figure 6a shows the row video output from another 16x24 array, running in the 1x16 column scan mode, with an integration time of 64 μsec. Figure 6b shows the injection pulse being applied to the column sense line. This pulse has a rise time of 25 nanosec (10-90%) and a pulse width of .25 μsec.

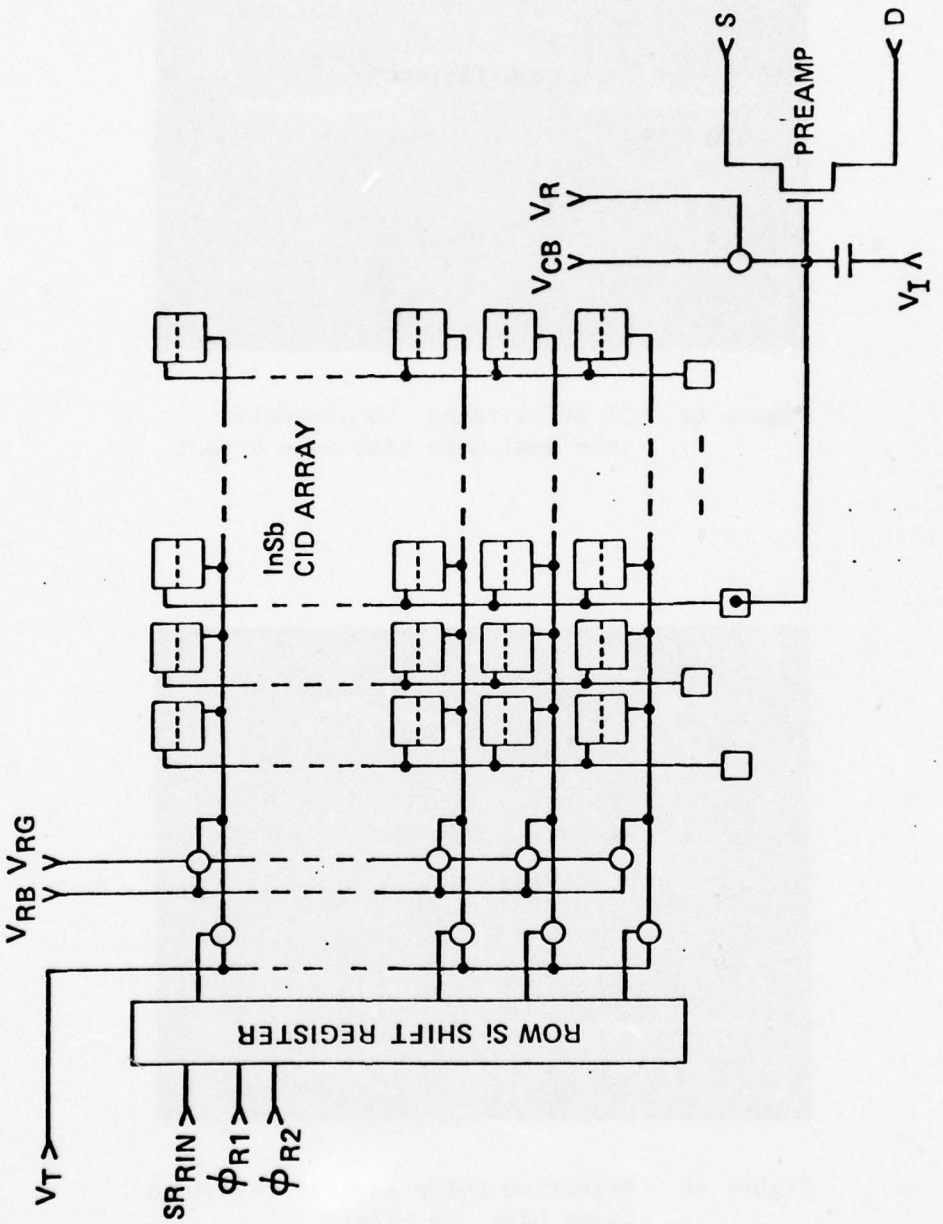


Figure 5. Discrete Column Read Measurement Setup

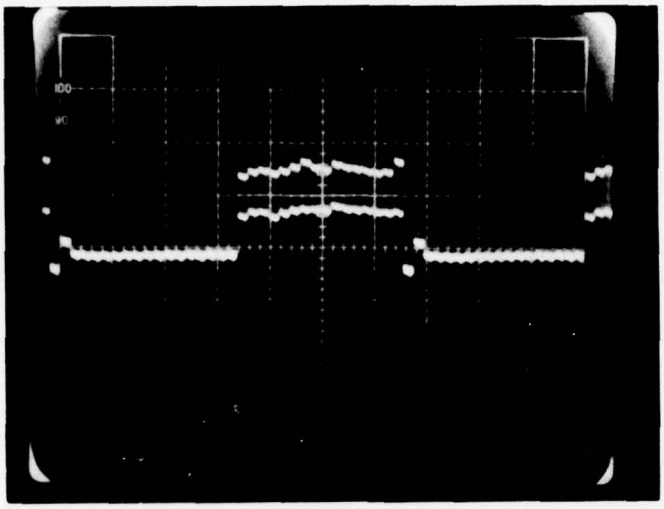


Figure 6a. 50 mv/division, 20 μsec/div
1x16 Dual Gate Line Scan Output

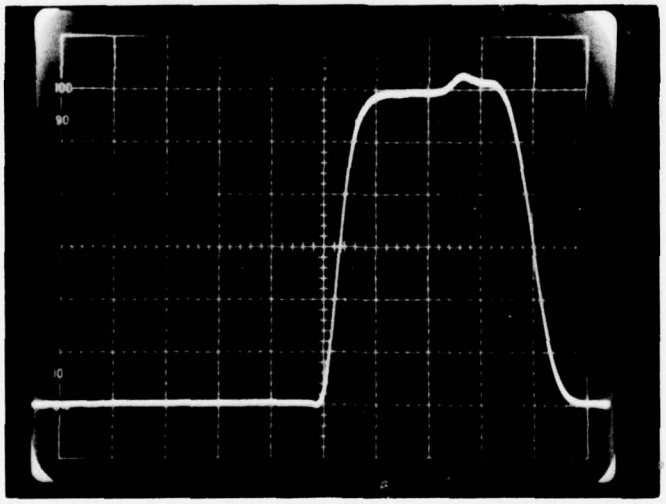


Figure 6b. Injection Pulse Applied to Column
Sense Line .05 μs/div.

Figure 6. (16x24 array) 1x16 Line Scan and Injection
Pulse Waveforms.

TABLE II. 16x24 Array Measurement Results - Single Column Scan

Filter $\Delta\lambda$	P_B $Psec^{-1}cm^{-2}$	P_{BG} $Psec^{-1}cm^{-2}$	N_P	N_e	T_I Integration time(μsec)	T_E Element Read Time (μs)	N_e/N_P
3.681 to 4.165	1.213×10^{15}	2.98×10^{14}	4.77×10^{5}	1.82×10^{5}	64	2	.38

P_{BG} = Background flux

P_{BB} = Blackbody flux

N_P = Number of signal photons/Integration period (chpped signal)

N_{PB} = Number of background photons/Integration period

N_e = Number of electrons at amplifier input

N_e/N_P = Performance efficiency of the array

Response:

N_P (chopped) = 4.77×10^{5}

V_S = Output signal = 0.2V

C_T = Total capacitance = 16.7 PF

G = System gain = 115

e = Charge of an electron = 1.6×10^{-11} coulombs

$$N_e = \frac{V_S \cdot C_T}{G \cdot e}$$

III. 32x32 ELEMENT ARRAY MEASUREMENTS

The test setup used for the 32x32 element array is shown in Figure 4. The only significant difference from the 16x24 test setup is that a JFET preamplifier is used instead of a MOSFET.

A 32x32 two dimensional CID InSb array was fabricated on a company-funded development program. This array has a pixel size of 1.8 mils by 2.2 mils, and 2.8 mils centers, respectively. In this section, the sensitivity measurement results for this 32x32 array are given.

For this measurement, the frame integration time was set at 2.3 milliseconds, which required a sampling rate of 445 KHz in the first sample and hold circuit. The JFET single ended preamplifier voltage gain and the sampled signal gain totaled 138. The output signals from 18 elements of a sampled column are shown in Figure 7. This waveform demonstrates the uniformity of this 32x32 InSb CID imager. Uniformity throughout this array was measured to be $\sim \pm$ 10%.

In order to measure the signal and noise voltages of a particular element in the array, a selective sampling circuit with a sample rate of $\sim$ 434 Hz was introduced. For the InSb CID array, the AC (chopped) signal values were then displayed and measured (reference Figure 4). The rms noise was measured with a true rms voltmeter preceded by a low-pass filter, as illustrated in Figure 4. The cut off frequency of the low pass filter was set at 1 KHz which was higher than the nyquist limit[1)], to assure that all the noise passed through to the rms voltmeter. For the D^* calculation, the noise bandwidth is equal to 434 Hz, though the filter bandwidth was 1000 Hz. The injection pulse width for these measurements was 250 nanoseconds, with a rise time of 25 nanoseconds (refer to Figure 6b).

For the systems $D^*_{\lambda o}$ measurement, a 780°K blackbody source and a cooled 4.12 μ spike filter with 55% transmission and 0.12 μ bandwidth were used. The filter and 2D array were both attached to the cold finger inside the dewar and the measurements were made at $\sim$ 77°K. The cold aperture had a diameter of 0.5 cm and was 1 cm from the detector. This

50 mv/division

5 μsec/division

Figure 7. 18 Sampled Column Outputs
from a 32x32 Array.

FOV resulted in a background flux of 3.5×10^{13} photons/sec cm^2 incident on the detector. The input signal radiation through the filter from the blackbody source was calculated to be 2.8×10^{-11} watts.

$D^*_{\lambda o}$ for this array is given by the following equation:

$$D^*_{\lambda o} = \frac{(A_E \, \Delta f)^{1/2}}{P_s} \cdot \frac{V_s}{V_N}$$

$$= 3.9 \times 10^{11} \ \frac{cm(Hz)^{1/2}}{watt}$$

where T_I = Integration time = 2.3 msec

$^{\#}\Delta_f = \frac{1}{2T_I}$

Δf = 217

A_E = Element Area = 2.55×10^{-5} cm^2

P_s = Input signal power on the detector = 2.8×10^{-11} watts

V_s = Peak signal voltage = 180 V

V_N = RMS noise = 1.2 V

$^{\#}$The noise bandwidth of the measurement system is the nyquist frequency (1/2 T_I) 217 Hz, although the filter bandwidth was set at 1000 Hz.

The total noise equivalent carriers (NEC) can be determined as follows:

$$NEC = \frac{C_T}{q} \cdot \frac{V_N}{G}$$

$$= 1576$$

where C_T = total shunt capacity across which the signal is generated 29PF

V_N = total measured RMS system noise = 1/2 mV

q = coulomb/electrons 1.6×10^{-19}

G = total gain 138

Table III summarizes the data taken on this array. Refer to previous reports[1] for detailed noise analysis.

TABLE III. MEASUREMENTS OF 32x32 CID ARRAY

CENTER DUAL GATE PIXEL

Cold Shield = $\sim 30^{o}$ FOV

Blackbody Temperature = $780^{o}K$

Watts on Detector (Pd) = 2.86×10^{-11} Watts

Q_B Incident on Detector = 3.5×10^{13} photon/cm^2 sec

System Gain = 138

Element Area = $2.55 \times 10^{-5} cm^2$

I_T = 2.3 ms, f_{sample} = 434, Δf = 217

(1) $V_{S(peak)}$	(1) $V_{N(RMS)}$	V_S/V_N	(2) $R_{\Delta \lambda_o}$ V/W	(3) $D^*_{\Delta \lambda_o}$	(4) NEP	(5) NEC
1.30 mv	8.7μv	150	4.5×10^7	3.9×10^{11}	2×10^{-13}	1576

(1) Referred to preamplifier input

(2) $R_{\Delta \lambda_o} = \frac{V_{S(peak)}}{Pd}$

(3) $D^*_{\Delta \lambda_o} = \frac{(Ad\Delta f)^{1/2}}{Pd} \cdot \frac{V_{S(peak)}}{V_{N\ (RMS)}}$

(4) $NEP = \frac{(Ad \cdot \Delta f)^{1/2}}{D^*_{\Delta \lambda_o}}$

(5) $NEC = \frac{C_T \cdot V_N}{1.6 \times 10^{-19}}$

IV. TRANSFER EFFICIENCY MEASUREMENTS ON DUAL GATE InSb CID ARRAYS

It has been demonstrated that good bi-directional charge transfer occurs in InSb two dimensional arrays. Charge transfer efficiency was measured to be greater than 98% and quantum efficiency was found to be about 50%. These results were verified on three arrays, A218, A280 and A318, and are the result of optimization of the rise times and bias levels, and by additional annealing.

These conclusions were induced from the waveform comparison of the readout waveforms from half selected and full selected sensor sites. Consider the idealized waveform of a fully selected site as shown in Figure 8. Ideally, when the transfer voltage is applied to the row, charge transfers to the column. The column well is then collapsed with the injection pulse, causing injection of the charge. The signal level at point A is a measure of the charge leaving the column pad and the signal level at B is a measure of the charge not returning to the pad, charge that is injected.

If the row pad is unselected, and is not saturated, and the column is half selected, one should observe a signal at the top of the injected pulse, point A, but not at point B. In this half selected case, the signal at point A represents charge transferring from the column into the row, and if this charge returns to the column after injection, then no signal is observed at point B since the same charge is under the column pad as when it was reset.

By observing the magnitude of the signal in both the half selected and fully selected cases, one can infer that charge transfer occurred. The signal, during full select at both point A and B, should be twice that observed at point A on the half select. The half select signals on top of the injection pulses should build up with time.

The experimental setup was as shown in Figure 9. A single column of an area array was wired directly to the preamplifier (source follower). The rows were connected in parallel via the load devices to the row transfer pulse, and the row transfer pulse was applied only after many

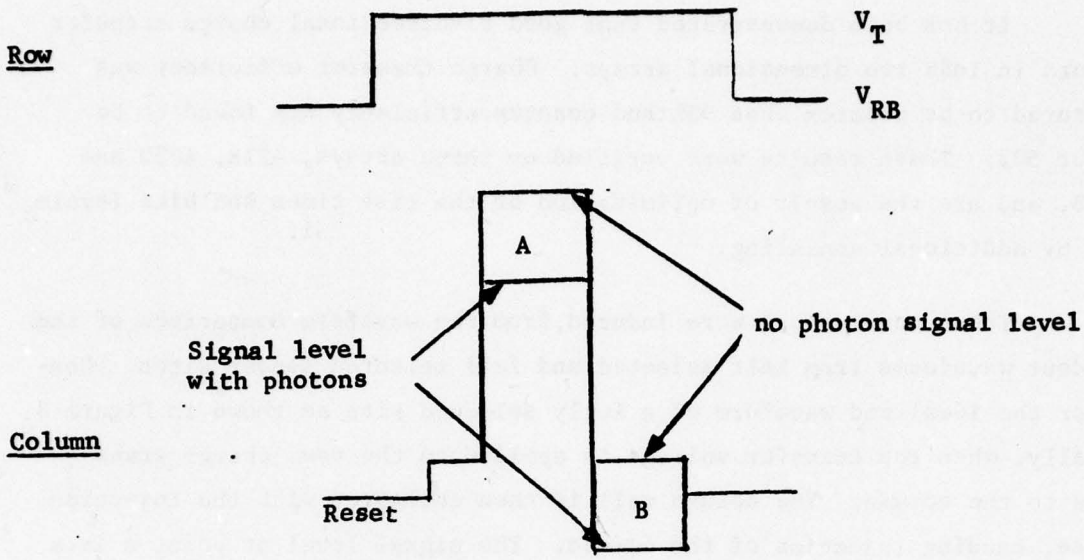


Figure 8. Idealized Full Select Waveforms

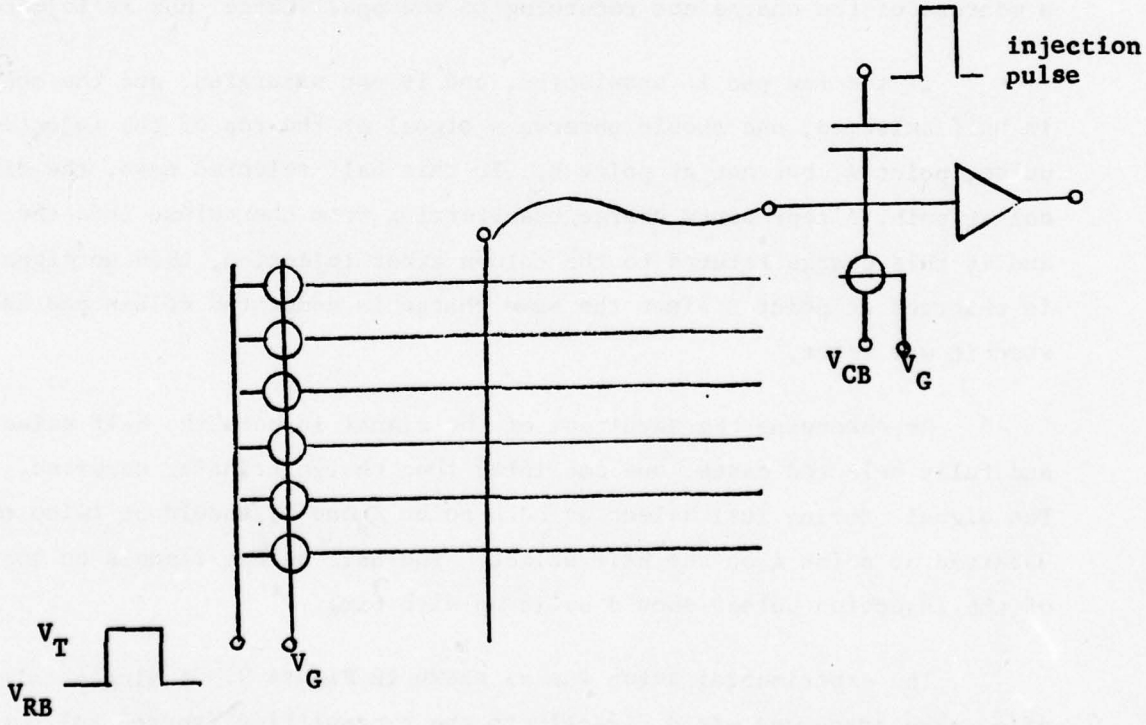


Figure 9. Experimental Setup for Transfer Measurements in Which One Column Is Connected.

column half selects. A chopped 1000°C blackbody source was used to obtain the modulated signal. The time interval was varied, depending upon the experiment. The reset switch clamped the column when the row transfer pulse was initiated. Column bias levels were 6 volts. Other voltage levels can be ascertained from the scope traces.

The procedure used is illustrated in the waveform photographs of Figure 10. The top trace of photo 10a shows the row half select where the row well is collapsed every 320 μsec, from 7 to 4 volts. The middle and lower traces show 32 column half selects for each full select without, and with, the chopped light, respectively. Full select occurs when the row and column half selects are coincident. The upper part of the lower trace shows the signal increasing on top of the inject pulses (point A) during the 320 μsec integration time, as expected. Figure 10b shows expanded traces of column half selects for the pulse numbers 32, 31 and 16. The 32nd pulse (top trace) is a full select and shows equal signal at points A and B. The middle trace is the 31st half select and has signal only at the top of the injection pulse, with zero signal at point B. The signal on top of the 31st injection pulse is about half of that on the 32nd pulse. The lower trace shows the signal on top of the 16th injection pulse to be about half of that of the 31st pulse, and is a measure of charge integration of the column pad only.

Figure 11 can be used to measure charge transfer efficiency. The top traces, Figures 11a and 11b, show identical row half selects occurring every 64 μsec. Center and lower traces of Figure 11a are the 16 column half selects/64 μsec without and with the chopped signal, while those of Figure 11b have the 15 intervening half selects inhibited. Figures 11c and 11d show the full select interval of Figures 11a and 11b, respectively. By comparing the signal read in the lower traces, one can see they are almost identical, indicating the 30 transfers occurred during the 15 intervening column half selects. If the transfer loss is proportional to the signal charge, then the transfer efficiency is about 98+%.

Using the data from the waveforms of Figure 11, a quantum efficiency of 59% is calculated, assuming the effective area is only the

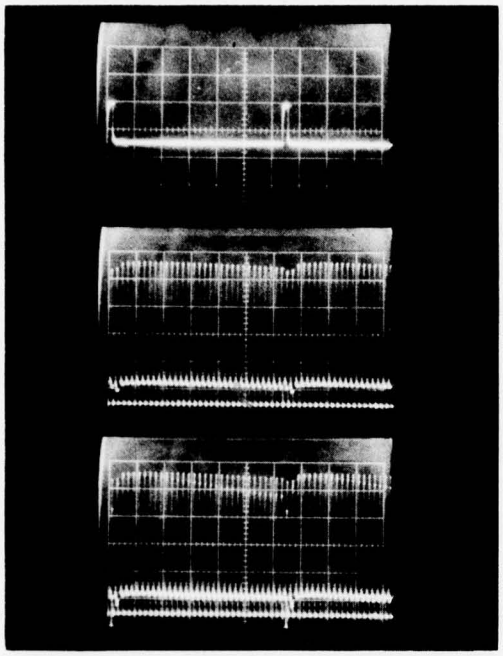


Figure 10a

Row half select

- vertical 2V/□, zero at top
- horizontal 50 μsec/□

Column half select without chopped light

- vertical .2V/□
- horizontal 50 μsec/□

Column half select with chopped light

- vertical .2V/□
- horizontal 50 μsec/□

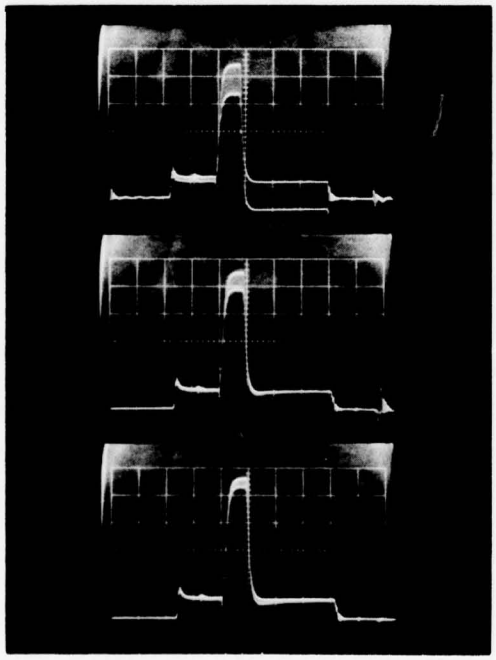


Figure 10b

32 column half select (full select)

31 column half select

16 column half select

all vertical .2V/□
horizontal 1 μsec/□

Figure 10. Waveforms Illustrating Charge Transfer Mechanism.

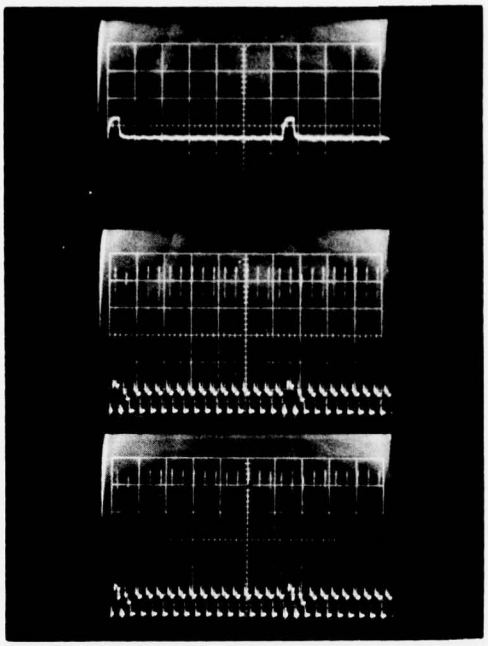


Fig. 11a -with intervening half selects
-horizontal scale 10 μsec
-vertical scale of lower two traceses is .2V/□

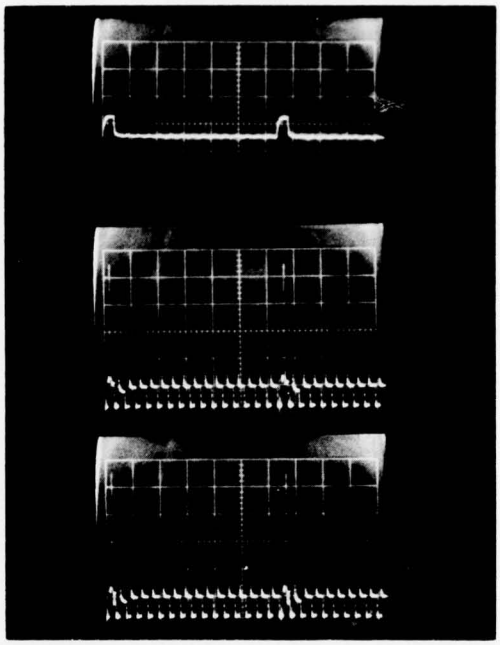


Fig. 11b -without intervening half selects
-horizontal scale 10 μsec
-vertical scale of lower two traces is .2V/□

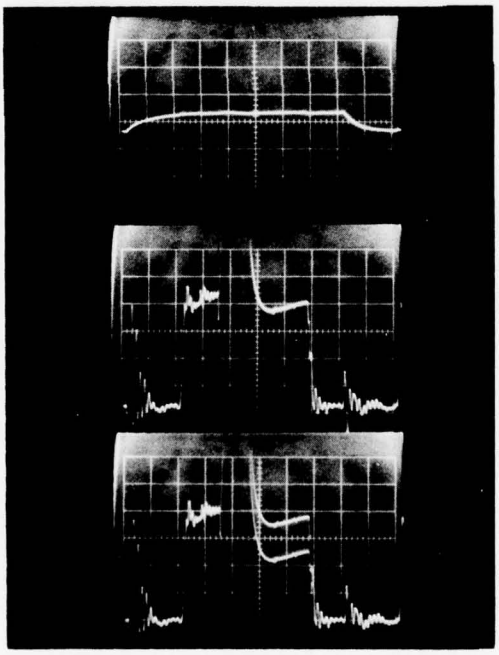


Fig. 11c -with intervening half selects
-horizontal scale .5 μsec
-vertical scale of lower two traces is .05V/□

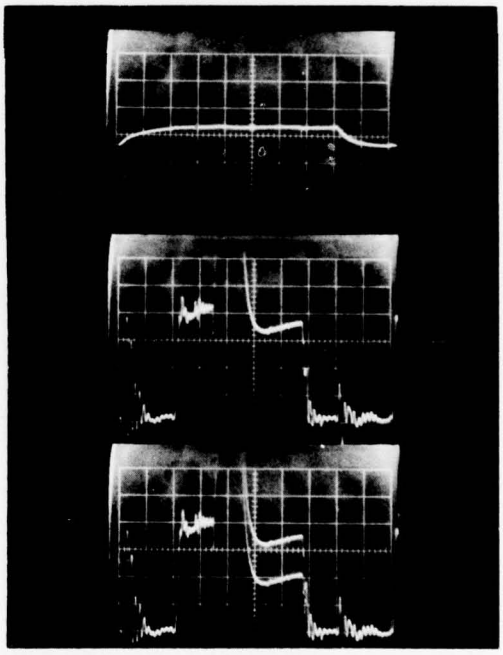


Fig. 11d -without intervening half selects
-horizontal scale .5 μsec
-vertical scale of lower two traces is .05V/□

Figure 11. Top trace is row half select 2V/□ zero at top
Center trace is without chopped signal
Waveforms Used to Measure Transfer Efficiency

geometric area of the storage site. Using the data of Figure 10, the calculated quantum efficiency is 41% under the conditions approaching saturation due to the longer integration times.

Saturation effects can be observed by extending the interval between row half selects. This is shown in Figure 12. The lower two curves are the waveforms of the column half selects with and without chopped light. The center trace shows the buildup of dark current and background flux leading to saturation in about 1.5 msec. The filter used in this experiment was the 3.7 to 4.2 μ filter. The bottom curve shows the envelope of the chopped signal buildup. By examining the relative slopes of both curves and estimating the background flux, one finds that the non-chopped signal trace has about equal contribution from dark current and background. Based on this, the time it takes for saturation, due only to dark current, is about 3 msec. The injection pulse was about 0.7 volt.

Measurements have been made of the thermal effectiveness of the experimental array-dewar assembly. In early configurations, a 6 degree difference existed between the array and the cold finger. This difference was due to differential contraction of some of the mounting components. More recent measurements indicate that the temperature differential has been reduced by more than half.

An important transfer factor is to insure that interface states are kept low and that they are not uncovered by the injection or transfer pulses. Better transfer is observed when higher bias charge levels are used, so that surface states are not emptied when either well is collapsed. Arrays tend to work better when bias voltage levels are 7 to 9 volts and when transfer and injection voltage are at least a volt more negative than threshold.

The better results reported here are partially due to the additional annealing that was given to these arrays. CV measurement taken before and after the anneal did indicate lower surface state densities. This agrees with the need to maintain good bias charge levels.

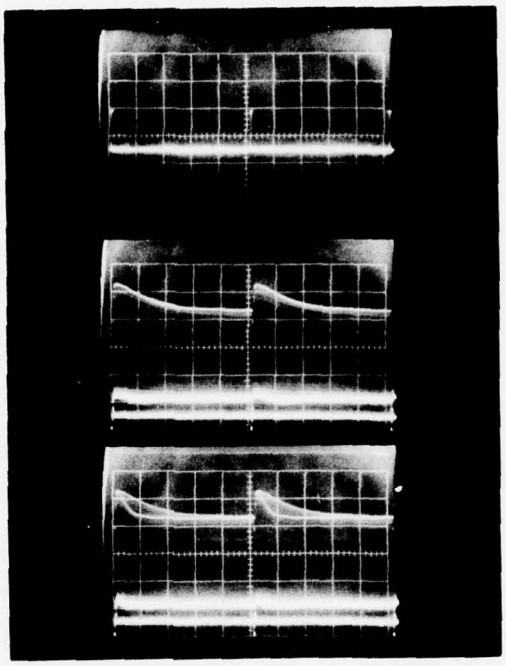


Figure 12. Scope Traces Used to Estimate Dark Current By

- extending the interval between row and half select to 2.6 msec.
- horizontal scale .5 msec/□
- top trace vertical scale is 2V/□, zero at the top
- center and lower traces, vertical scale .2V/□

V. InSb P-N JUNCTION DIODES

Based on results with the coplanar array structure, it was felt that an even better array structure could be built using a p-coupled island between the two gates in each array element. Since both gates could thus be placed on the same thin gate oxide, the ability to create deep potential wells would be expected. Also, because the row and column gates would be physically separated, the capacitive coupling between them, and thus pattern noise, should be minimized. The operation of this array should be simpler because the row and column gates would have the same oxide thickness and so they could have the same operating bias voltage.

Because of these potential advantages, an effort was made to develop a planar p-diffused p-n junction on InSb. Planar InSb p-n junction diodes have been fabricated successfully. First, p-type doping was diffused through selected areas. Then the surface was cleaned after removing the mask oxide, and a SiON dielectric layer was deposited just as it is done for MIS structures. Small contact windows were then opened on the diffused areas, and a metal layer for contact leads was deposited. The typical performance of such a planar p-n junction diode is shown in Figure 13, exhibiting an I-V characteristic. The reverse leakage current is low, but the breakdown voltage is small.

An effort has been made to fabricate two-dimensional array structures with a p-coupled island between the row and column gates, using the diffusion process referred to above. For this work, a 1x16 dual gate linear array structure was used. It has proven difficult to fabricate a p-coupled CID dual gate array with the diffusion process. Diffusion was made through small windows, which resulted in problems of selective diffusion; the diffusion occurred under the mask oxide on the periphery of the open windows.

An alternate technique for forming InSb Planar P-N Junction diodes is by means of ion implantation. An effort was begun during this program to fabricate and evaluate ion implanted P-N junction devices and

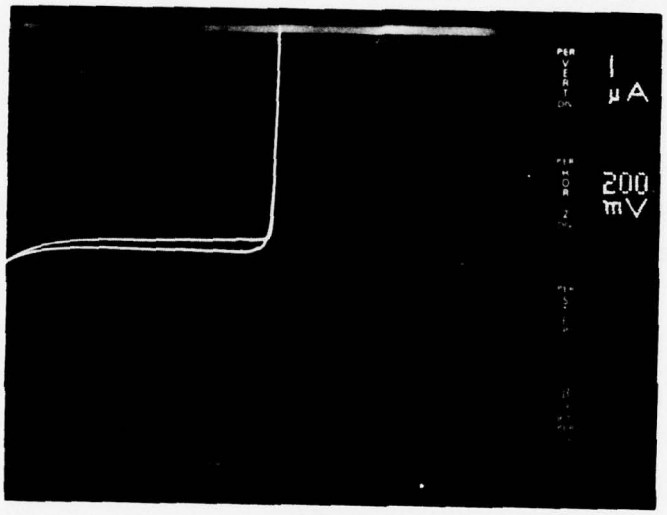


Figure 13. I-V Characteristic of an InSb Planar P-N Junction Diode.

to apply this technique to p-coupled islands in the dual gate array structure. For this work, N type InSb 111 plane wafers with a dopant level of $7x10^{14}$ were masked with low temperature deposited SiO_2 and patterned with 20 mil dots. Figure 14 shows the cross section of the pattern to be ion implanted, with appropriate masking against ion beam.

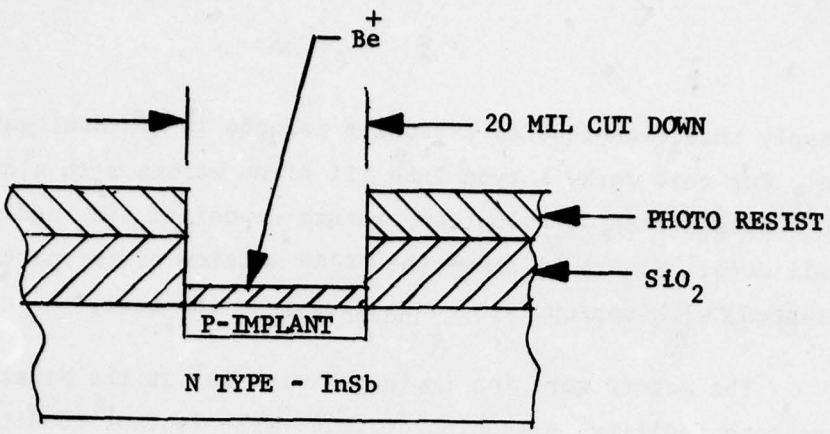
The wafers were ion implanted with Be^+ at the Naval Research Laboratory facility in Washington, D.C. The implant conditions were as follows:

Ion Implanted Acceptor	=	Be^+
Energy	=	100 Kev
Dose	=	$3x10^{13}$ cm^{-2}
Peak Concentration	=	$7.5x10^{17}$ cc

After implantation, the photoresist was stripped, and selected wafers were diced for annealing experiments. The original oxide passivation was left on the InSb surface and various temperature anneals were performed.

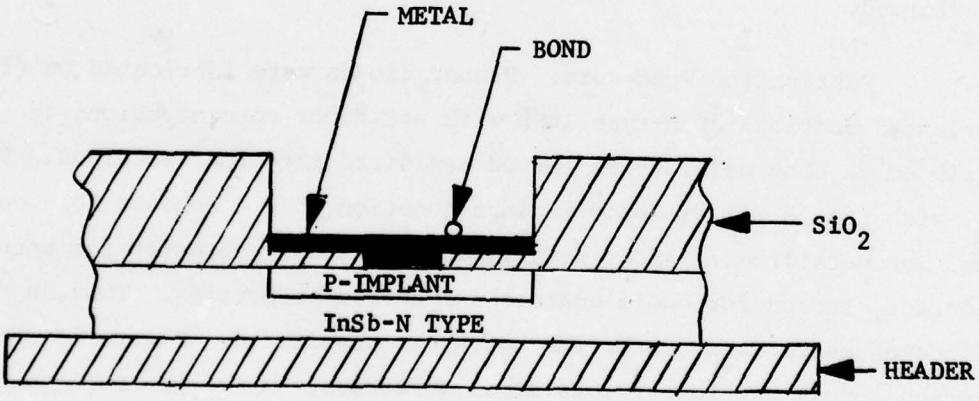
Fabrication Procedure: Planar diodes were fabricated on (111) oriented sections of n-type InSb with net donor concentrations of $7x10^4 cm^{-3}$. The wafer to be tested was diced into four sections. Section 1, with its 20 mil diameter implant junction, had a contact hole opened and was metallized. After metallization, it was patterned for bond pad contact, tested for ohmic contact and device properties. Thus, a device diode characteristic base line could be established. Figure 15 shows the typical cross section of this diode structure.

Figure 16 shows the expected (I-V) resistive trace for section 1, due to the non-annealed, crystalline disorder created by the ion implant on a 20 mil dot. The second section of the same wafer was then annealed at 195°C (oxide still intact), contact holes were opened, and the dots were metallized and mounted for evaluation. Figure 17 shows the (I-V) results after annealing. The crystalline disorders have been partially



CROSS SECTION OF ION IMPLANTED DIODE

Figure 14



SIDE VIEW OF A MOUNTED PLANAR InSb IMPLANTED DIODE

Figure 15

annealed away, and diode characteristics are observed. However, the device is leaky and has soft reverse breakdown, due to surface inversion during annealing and crystalline disorders. The third section was then annealed at 250°C with passivation glass intact, after which contact holes opened, and the device was metallized and packaged for evaluation. The results were similar to the previous device shown in Figure 17. This device was then stripped of its original oxide (the ohmic contact metal acts as an etch mask), given a slight clean up etch and re-evaluated. Figure 18 shows the results of this etching process, which reduced the surface inversion layer effect and resulted in higher reverse breakdown.

The fourth section of the wafer in this experimental sequence was annealed at 300°C, processed through metallization (oxide still intact) and evaluated at 77°K. Figure 19 shows that this device has an improved diode characteristic and reduced surface leakage. There is an indication that the crystalline disorders have been significantly reduced. Figure 20 shows the same ion implanted diode at a higher current scale, exhibiting a soft reverse breakdown of 2.5 volts.

These initial results indicate that ion implanted p-coupled channels could be formed, crystalline disorders annealed away, surface leakage reduced by clean up etches, and planar oxide gates deposited for dual gate CID devices.

No functional p-coupled dual gated structures have been fabricated during this program. The effort under this contract was completed before that development stage was reached.

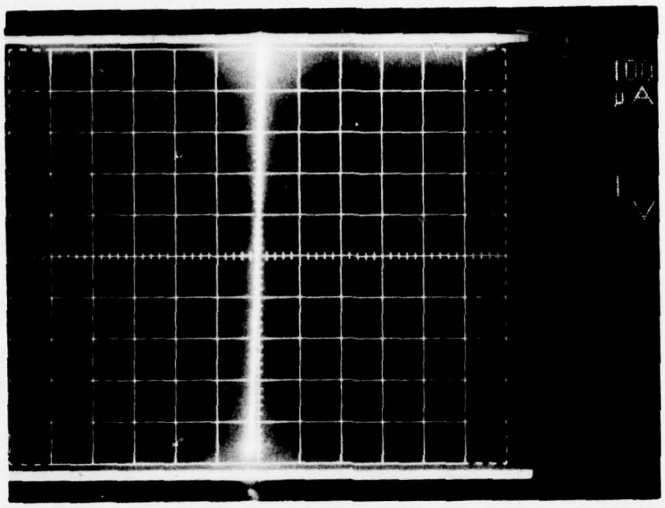


Figure 16. Ion Implant Planar Device
No Anneal.

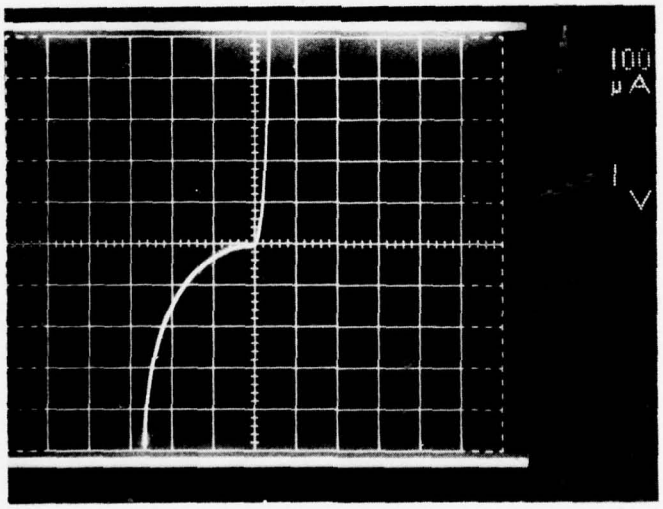


Figure 17. Ion Implant Planar Device
195°C Anneal

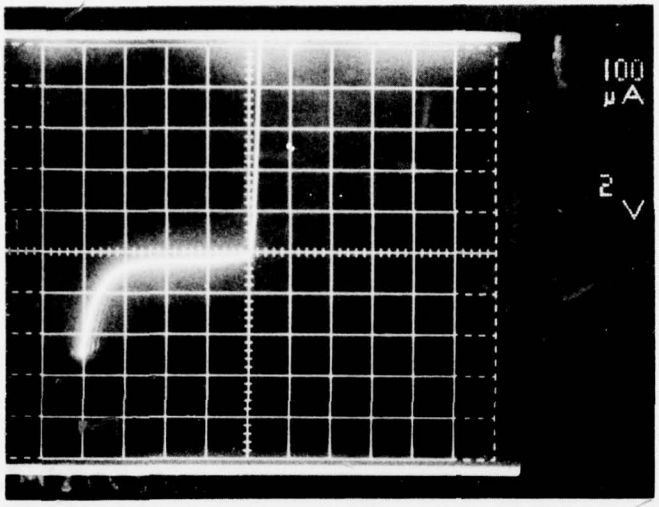


Figure 18. Ion Implant

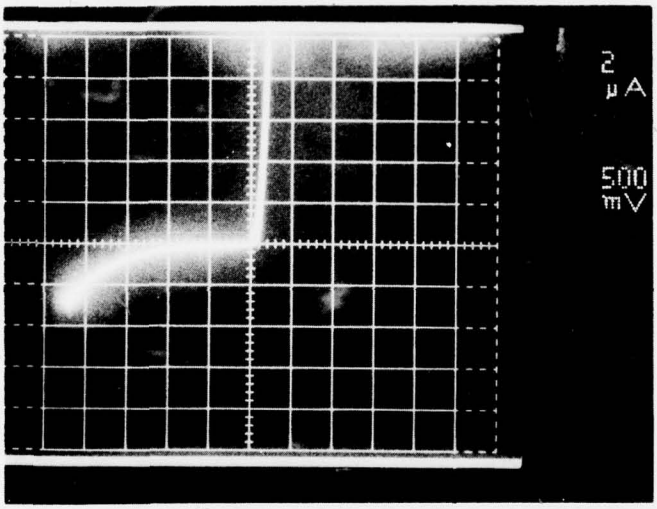


Figure 19. Ion Implant
Planar Device
300°C Anneal.

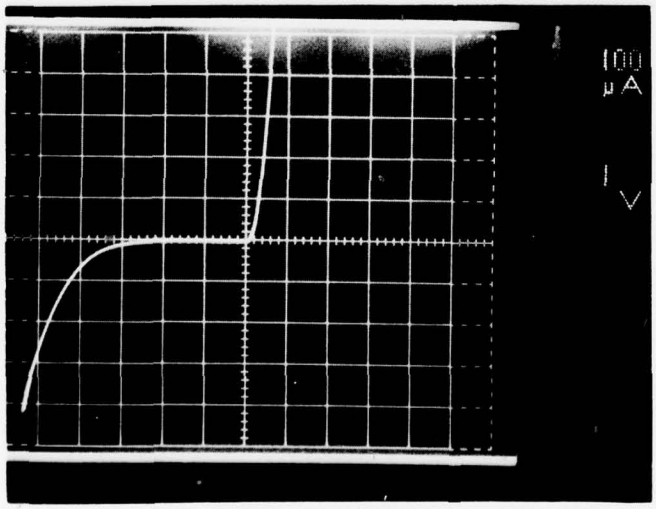


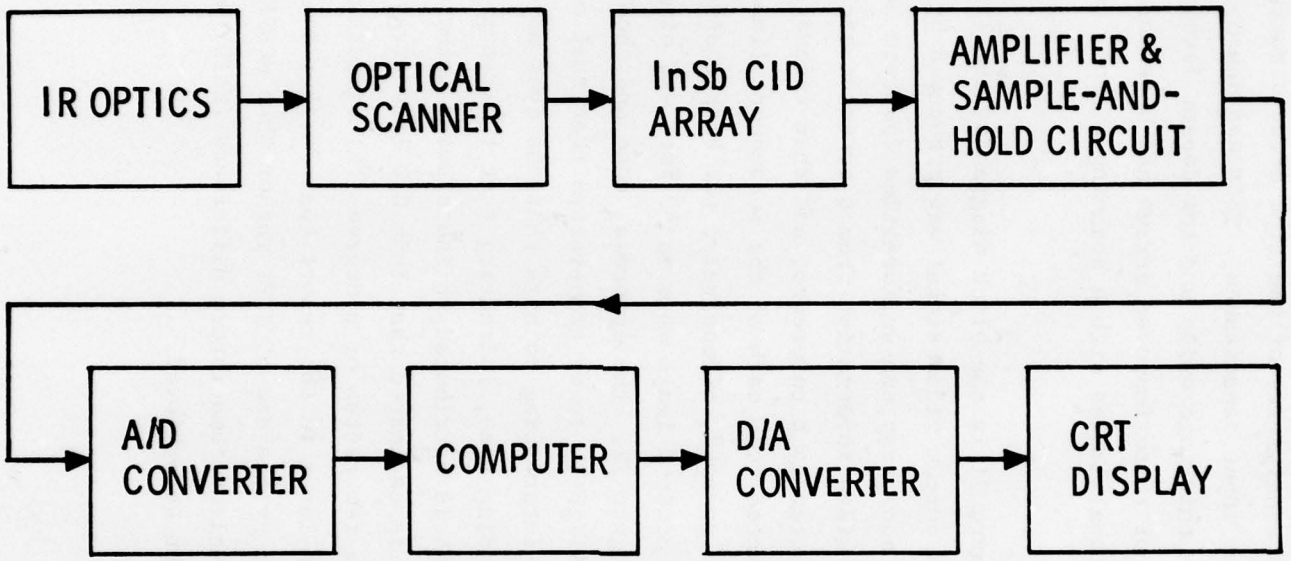
Figure 20. Ion Implant
Planar Device
300°C Anneal.

VI. IMPROVEMENT IN LINE ARRAY PERFORMANCE

The sensitivity of the line array structure has been improved by reducing the input capacitance. This was accomplished by fabricating the arrays with thin-gate oxide and low dopant level substrate materials. The evaluation of these improved arrays has been carried out by generating two-dimensional images with a scanning mirror, as discussed in a previous report[1].

Figure 21 is the block diagram of the line array imaging setup. The sampled output video signal was processed by a computer, which removed background and array non-uniformities (pattern noise). The first line of background video information from a constant background scene was stored in the computer as a reference, and that reference line information was then subtracted from each of the subsequent lines of image video information. This removed, effectively, the background-generated dc level. The computer-processed image of a man's face was displayed on a CRT and is shown in Figure 22. The eyebrows, nose and cheeks appear darker, an indication of slightly lower temperature than that of the rest of the face. It is also interesting to note that the eyes appear slightly brighter than the surrounding face, indicating that their temperature is slightly warmer, a fact which is attributed to the exposed veins in the eyes. For these results it is estimated that InSb CID line arrays presently are capable of resolving a few tenths of a degree (^{o}K) difference in temperature. However, it is shown later in the report that further improvement in sensitivity can be expected by the use of JFET rather than MOSFET preamplifiers so that a noise equivalent temperature difference (NETD) of less than one tenth of a degree can be achieved.

Fig. 21. BLOCK DIAGRAM OF InSb CID LINE ARRAY IMAGING SETUP



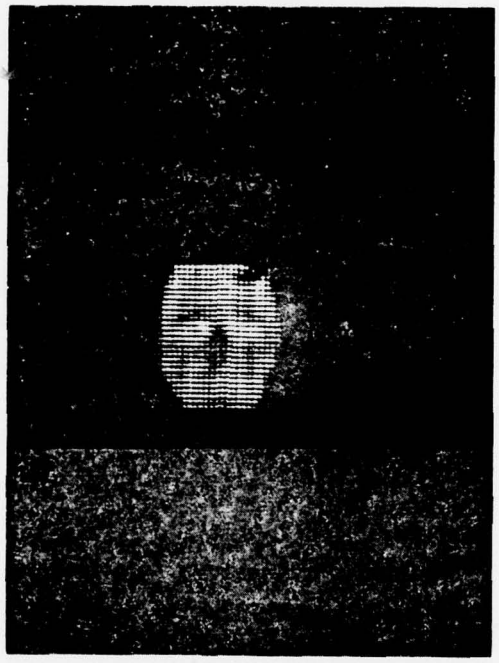


Figure 22. Image Display of a Man's Face Produced With a 32-Element InSb CID Line Array.

VII. LOW NOISE PREAMPLIFIER DEVELOPMENT

A low noise linear preamplifier is required to amplify the video signal directly from the enable line to a suitable level so that it can be DC restored and sampled. This amplifier must have high input impedance so that when the stored charge is transferred to the amplifier input, a reasonable voltage will be generated and will not leak off before the output voltage is sampled. An input impedance of 10^7 ohms is sufficient to prevent appreciable leakage, but the input capacitance must be minimized so that it will not add appreciably to the total shunt capacitance of the enable line. The amplifier also must have high dynamic range, since the noise level is expected to be equivalent to 10^2 charge carriers and the maximum stored charge can be 10^7 carriers. This 100 dB dynamic range extends from about 1 microvolt to 100 millivolts on the enable line. In addition to this, the amplifier must tolerate and rapidly recover from the injection pulse, which is on the order of 2 volts.

A p-channel, enhancement mode MOSFET has been used inside the dewar as an amplifier built onto the scanner chip. An on-chip amplifier is desirable, since it reduces the shunt capacitance and the FET works better at $77^{\circ}K$ than at room temperature. Unfortunately, even at $77^{\circ}K$ the MOSFET has poor noise performance. The 1/f noise corner frequency is about 100 KHz, which makes 1/f noise significant at high sampling frequencies and dominant at low sampling frequencies.

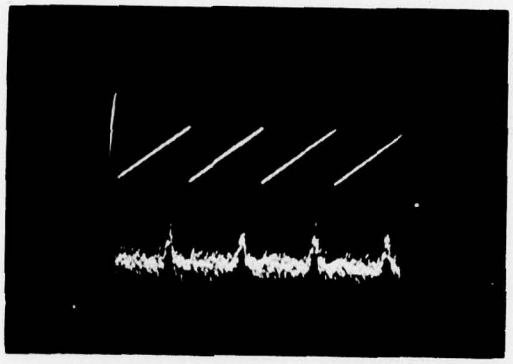
Several discrete semiconductor devices were considered to replace the on-chip MOSFET. The device was to be mounted off-chip but within the dewar, and operated at low temperature ($> 77^{\circ}K$). Bipolar transistors were not considered because of the high input impedance required, and the low operating temperature. An rf type of FET would seem to be the appropriate device, combining low noise, low input capacitance and good low temperature performance. Unfortunately, common rf MOSFETs and JFETs are of the n-channel type and available p-channel devices have poor noise performance. A p-channel device would be preferred in a common source amplifier configuration for this application because the large positive-

going injection pulse would tend to cut the device off rather than drive it into saturation. However, the increased noise is too great a penalty to pay so a "garden variety" n-channel JFET was mounted in a dewar for testing.

The JFET preamplifier in the dewar can be used in a number of configurations, including common source, source follower, or as the input part of a cascode stage. The normal common source configuration has two disadvantages: first, the large injection pulse tends to drive the JFET into saturation; and second, the gain of the stage tends to amplify the feedback capacitance and increase the total input capacitance. The cascode configuration keeps the input capacitance down, but the injection pulse is still a problem unless a differential input is used, which in turn, adds more noise. The source follower has a gain of less than one, but the effective gate-to-source capacitance is reduced, thus reducing the input capacitance somewhat.

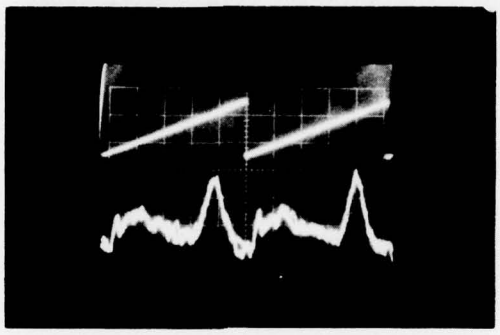
A comparison of the on-chip MOSFET and off-chip JFET preamplifier was made using both of them in source follower configurations with similar following amplifier stages. The lower trace of Figure 23 shows the MOSFET sample-and-hold video output from a single element of a line array, as the array is mechanically scanned across a test target with a $3^{o}K$ temperature difference. The test target was 3 two-watt resistors mounted on a large circuit board. Both the resistors and the circuit board had thermistors mounted on them for temperature measurement. The resistance of the thermistors was measured with a digital multimeter and then the temperature difference was determined by looking up the resistance values in a table. The upper trace shows the scan mirror drive waveform.

Figure 24 shows similar video from the same array element using the JFET, except that in this case the test target temperature difference was $1.75^{o}K$. In both cases the integration time was 500 μsec, which requires a sampling rate of 68 KHz for the 33-element line array. The low sampling frequency is well into the 1/f noise region of the MOSFET; therefore, the JFET provides a much better signal-to-noise ratio.



A266 Element #24
MOSFET Preamplifier
$\Delta T = 3^{o}K$
10 m Sec/Div

Figure 23. MOSFET Preamplifier Performance



A266 Element #24
JFET Preamplifier
$\Delta T = 1.75^{o}K$
5 m Sec/Div

Figure 24. JFET Preamplifier Performance.

The NETD for this array element was measured using the resistor test target. The signal voltage was measured from the oscilloscope trace shown in Figures 23 and 24, and the noise voltage was measured by turning off the mechanical scanner and measuring the voltage with an rms voltmeter. The NETD was found to be $0.11^{o}K$ using the JFET preamp and $0.5^{o}K$ using the MOSFET preamp. The $0.11^{o}K$ NETD is near BLIP for this f/3.25 lens system with a 3.6 to 4.0 μm filter and a 500 μsec integration time.

The test circuit used with the JFET preamplifier is shown in Figure 25. It can be considered a source follower driving a common gate amplifier or a differential amplifier, with one JFET inside and one outside the dewar. This circuit handles the injection pulse gracefully, by simply letting it cut Q3 off, and the JFET sources present the cable with both a source and load impedance near its characteristic impedance. The penalty for these features is an increase in the noise voltage. The equivalent amplifier input noise voltage is

$$V_N = \sqrt{\frac{8K\,\Delta f}{3}\left(\frac{T_1}{g_{m1}} + \frac{T_2}{g_{m2}}\right)}$$

where g_{m1} and T_1 are the transconductance and temperature of Q1, while g_{m2} and T_2 refer to JFET Q2. It is convenient to determine the equivalent noise input resistance so that the amplifier noise can easily be compared with the selection switch thermal noise. The equivalent noise input resistance, R_n, for this amplifier is

$$R_n = \frac{2}{3T_r}\left(\frac{T_1}{g_{m1}} + \frac{T_2}{g_{m2}}\right)$$

where T_r is the temperature of R_n. When T_r, T_1 and T_2 are all equal to room temperature, the calculated equivalent noise input resistance is 400 ohms. A value of 550 ohms was measure, using a 50 KHz to 1 MHz bandpass.

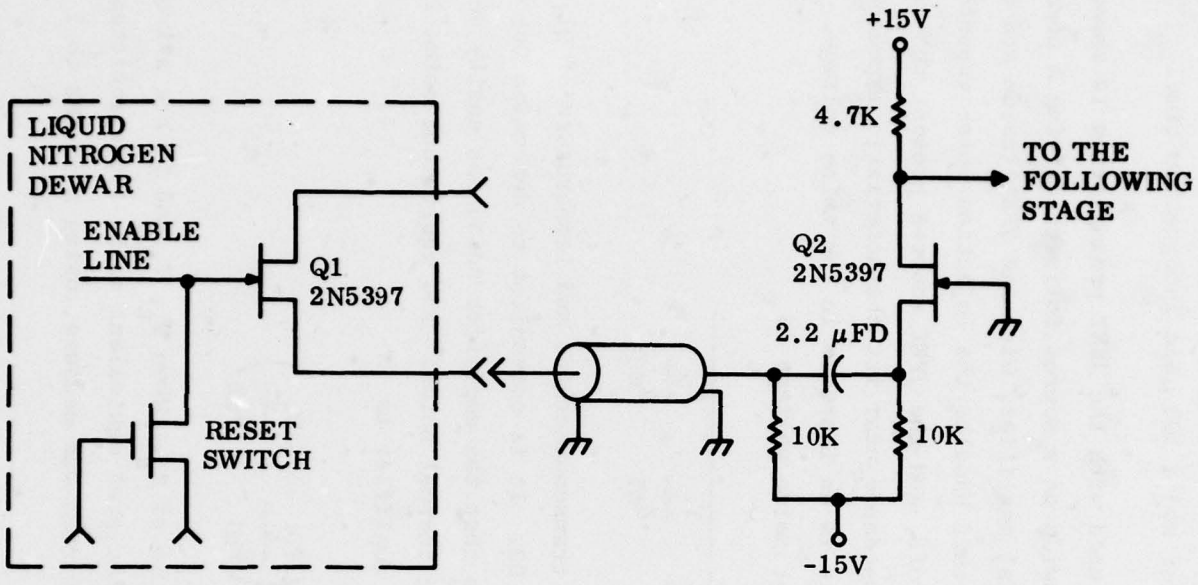


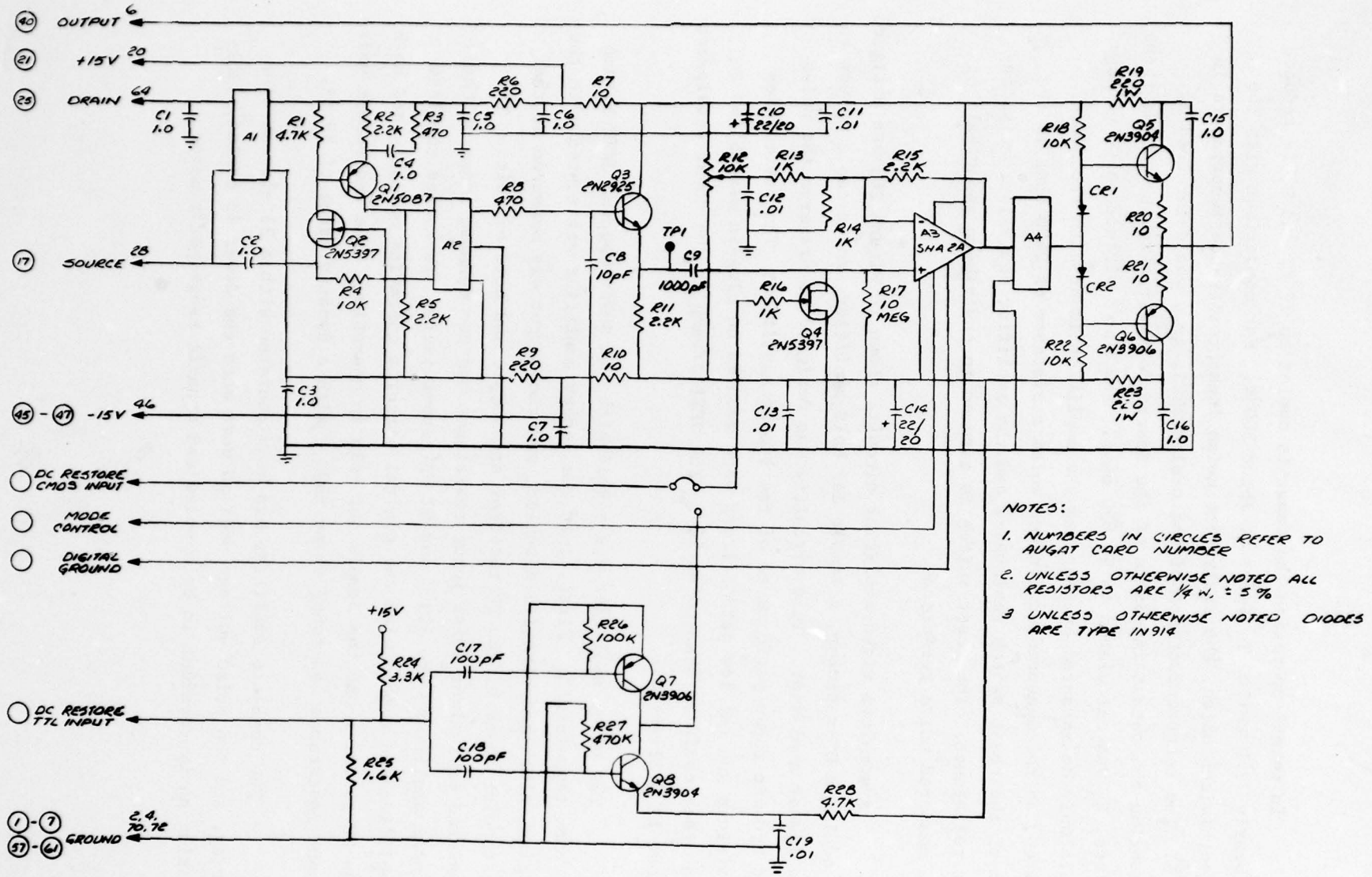
Figure 25. JFET Test Amplifier

In normal operation the dewar is cooled to 77°K, and T_1 is reduced to nearly 77°K while T_2 stays at about 300°K. For comparison with the select switch noise, the equivalent noise input resistance temperature is 77°K. The transconductance of the cooled JFET, g_{m1}, was determined by measuring the output impedance of the source follower circuit. Using these values, R_n was calculated to be 890 ohms. The short circuit noise voltage could only be measured by shorting the amplifier input with the reset switch, so the measured equivalent noise resistance of 2400 ohms is the sum of the reset switch resistance and the amplifier equivalent noise input resistance. The reset switch is assumed to contribute about half of the measured noise resistance.

A complete video amplifier circuit, shown in Figure 26, was designed by adding a DC restorer, a sample and hold amplifier, and a cable driver to the linear amplifier. This circuitry was designed to preserve the noise and dynamic range performance of the linear amplifier. The preamp bias resistors and the low pass filters were mounted on plug-in assemblies so that they could be changed easily. The JFET preamp in the dewar dissipated about 12 milliwatts.

The video amplifier was tested with the dewar mounted JFET preamp at room temperature. First, just the linear amplifier was tested with the digital clock and circuits disabled, and the output was measured at the test point ahead of the DC restorer and sample and hold circuits. The measured equivalent noise input resistance and the dynamic range of the linear amplifier were 700 Ω and 91 dB respectively. Then, the complete amplifier was tested with the digital circuits operating normally and both the DC restorer and the sample and hold in operation. The equivalent noise input resistance was found to be 2300 Ω with a dynamic range of 89 dB.

The complete amplifier has been operated with a 33 element line array, and the noise voltage does go down when the dewar is cooled, indicating an improvement in both noise and dynamic range performance.



NOTES:

1. NUMBERS IN CIRCLES REFER TO AUGAT CARD NUMBER
2. UNLESS OTHERWISE NOTED ALL RESISTORS ARE ¼ W, ± 5%
3. UNLESS OTHERWISE NOTED DIODES ARE TYPE IN914

Figure 26. Single-Ended Amplifier and Sample/Hold Circuit

VIII. CONCLUSION

Both 16x24 and 32x32 InSb CID two dimensional arrays have been fabricated using a multilayer processing technique.

These arrays have been evaluated, both in the staring array (imager) and line scan mode.

Arrays have been characterized and exhibit performance efficiencies > than 30%, observed uniformity variation of $\pm$ 10% or less (column to column), transfer efficiencies greater than 98% for 1 mil gate length and high $D^*_{\lambda o}$ which presently appears to be limited by signal processing electronics noise.

Line arrays have been fabricated on a routine basis, evaluated and a NETD has been measured which was less than .11^{o}C. Previous reports confirm BLIP performance on linear arrays.

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