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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The objective of this research program is to develop MSI circuits using GaAs transferred-electron logic devices for gigabit-rate signal processing applications. The test vehicles used for technology development are exclusive-OR, Carry, and Full Adder circuits.

In the previous phase of this program, it was shown that an integrated TELD-FET structure with a capacitive-output electrode

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has many advantages over simple 3-terminal TELDs with linear loads for realizing multigigabit-rate signal processing. This integrated structure uses an FET input section with a 2-terminal TELD output section with a capacitive-pickoff electrode. This structure has higher trigger sensitivity, higher voltage gain (and hence fan-out), and has compatible input/output characteristic allowing direct cascading of logic gates without level-shifting. As a result of this study, the major effort of this program phase was devoted to developing logic circuits and associated fabrication technology using the integrated TELD-FET combination as the basic building block.

The major accomplishments of this phase of the program are:

(i) A hybrid two-stage cascaded circuit using discrete TELDs with capacitive-output electrodes was evaluated. The capacitive output showed both positive and negative peaks and the output of one device was sufficient to trigger the other. This established the basic feasibility of our capacitive-output technology.

(ii) The design of an integral TELD-FET device using a uniformly doped n-layer was completed.

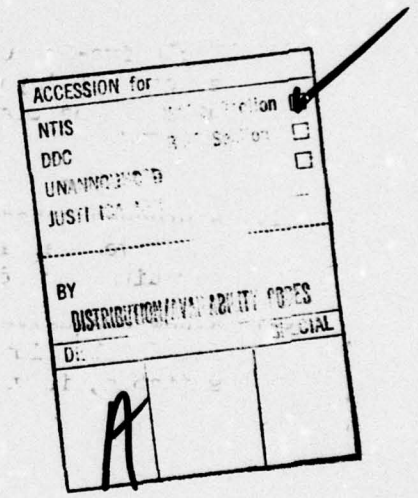
(iii) Exclusive-Or, Carry generator, and Full Adder circuits were designed. A layout for the adder circuit was generated. This uses 200 ps transit-time TELDs and is expected to operate at 2-3 Gb/s-rates with 300-400-mW power dissipation for one bit of the adder.

(iv) A process schedule for the fabrication of GaAs MSI circuits was developed and is being debugged. Monolithic full adder circuits were fabricated, and are currently being evaluated.

(v) A new exclusive-Or circuit configuration is being evaluated for further improving the performance. If this circuit is found suitable, it will be incorporated in the adder circuit.

## PREFACE

This Annual Report describes research done in the Microwave Technology Center of RCA Laboratories under Contract No. N00014-75-C-0100 during the period of 15 December 1976 to 14 March 1978. F. Sterzer is the Center's Director; S. Y. Narayan is the Project Supervisor, and L. C. Upadhyayula the Project Scientist. Others who participated in the research are R. E. Smith, J. F. Wilhelm, S. T. Jolly, J. P. Paczkowski, and J. E. Brown. The draft of this report was originally submitted in April, 1978.



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## INTRODUCTION

The objective of this research program is to develop MSI circuits using GaAs transferred-electron logic devices (TELDs) for gigabit-rate signal-processing applications. The test vehicles used for technology development are exclusive-OR, CARRY, and Full ADDER circuits.

In the previous phase of this program, it was shown that an integrated TELD-FET structure with a capacitive-output electrode has many advantages over simple 3-terminal TELDS with linear loads for realizing multigigabit-rate signal processing. This integrated structure uses an FET input section with a 2-terminal TELD output section with a capacitive-pickoff electrode. This structure has higher trigger sensitivity, higher voltage gain (and, hence fan-out), and has compatible input/output characteristic allowing direct cascading of logic gates without level-shifting. As a result of this study, the major effort in this program phase was devoted to developing logic circuits and associated fabrication technology using the integrated TELD-FET combination device as the basic building block. The major accomplishments of this phase of the program are summarized below:

(1) Breadboard two-stage cascaded circuits using TELDS with capacitive-output electrodes were evaluated. The capacitive output showed both positive and negative peaks and the output of one device was sufficient to trigger the other. This established the basic feasibility of our capacitive-output technology.

(2) The design of an integral TELD-FET device using a uniformly doped n-layer was completed.

(3) Exclusive-OR, CARRY generator and Full ADDER circuits were designed. A layout of the ADDER circuit was generated. This design uses 200-ps transit-time TELD and is expected to operate at 2-3 gigabits/s rates with 300-400-mW power dissipation for 1 bit of the adder.

(4) A process schedule for the fabrication of GaAs MSI circuits was developed and is being debugged. Monolithic full adder circuits were fabricated and are currently being evaluated.

The effort in all these areas is described in the following sections.

## SECTION II

## DEVICE AND CIRCUIT DESIGN

### A. INTRODUCTION

For logic applications the switching device should have (a) good trigger sensitivity, (b) fan-out capability, (c) input-output compatibility, and (d) stability. In addition to this, gigabit-rate MSI circuits require devices with low power dissipation and switching speed in the 100-ps range. Transferred-electron logic devices (TELDs) have been designed, fabricated, and evaluated as single gates [2-4] and rudimentary integrated circuits [1,5,6]. Early theoretical calculations projected that logic gates with fan-out capability of between 6 and 10 are feasible [7]. Experimental results have not yet borne out these theoretical predictions. Voltage gains (hence, fan-out capability) of 0.5 for split-gate devices and 1 for single-gate devices have been demonstrated. The device dc-dissipation in these experimental studies was at best, *200-300 mW, and approximately an equal amount of dc power was dissipated in the load resistor*. This performance is clearly unacceptable for MSI logic circuits. Our initial experimental results with discrete TELD-FET combination circuits are very encouraging. Instead of developing the output signal across

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1. K. Mause, A. Schlachetzki, E. Hesse, and H. Salow, "Monolithic Integration of Gallium Arsenide-Gunn Devices for Digital Circuits," Proc. Fourth Biennial Cornell Electrical Eng. Conf. Microwave Devices, Circuits and Applications, Vol. 4, p. 211, 1973.
2. T. Sugeta, H. Yanai, and K. Sekido, "Schottky-Gate Bulk Effect Digital Devices," Proc. IEEE 59, 1629 (1971).
3. L. C. Upadhyayula, R. E. Smith, J. F. Wilhelm, S. T. Jolly, and J. P. Paczkowski, "Transferred Electron Logic Devices for Gigabit-Rate Signal Processing," IEEE Trans. Microwave Theory Tech. MTT-24(12), pp. 920-926 (1976).
4. T. Sugeta et al., "Characteristics and Applications of a Schottky-Barrier-Gate Gunn-Effect Digital Device," IEEE Trans. Electron Devices ED-21, 504-515 (Aug. 1974).
5. N. Hashizume and S. Kataoka, "Integration of GaAs MESFETS and Gunn Elements in a 4-Bit-Gate Device," Electron. Lett. 12(15), 370-372 (1976).
6. S. Yanagisawa, O. Wada, and H. Takahashi, "Gigabit-Rate Gunn-Effect Shift Register," Tech. Digest, Int. Electron Device Meeting, Washington, D.C. 1975, p. 317.
7. H. Yanai and T. Sugeta, "Some Features and Characteristics of Gunn-Effect Digital Device," Jap. IECE Natl. Conv. Rec. No. 717. p. 808, Sept. 1969.

a linear or nonlinear load resistor and capacitively coupling it to the succeeding stages, a capacitive-pickoff electrode on the TELD itself can be used to provide the output.

An integrated TELD-FET device with capacitive output is used as a building block for our logic circuits. Two-input exclusive-OR and three-output MAJORITY gates have been designed with the TELD-FET combination devices. A monolithic full ADDER layout has been prepared consisting of two exclusive-OR circuits and one MAJORITY gate. The following pages describe briefly some of the design considerations.

## B. DEVICE DESIGN

A detailed discussion on the design of a TELD-FET device with capacitive-output electrode was given in our previous annual report [8]. A brief summary is included here for completeness. Figure 1 shows schematically a TELD-FET device.

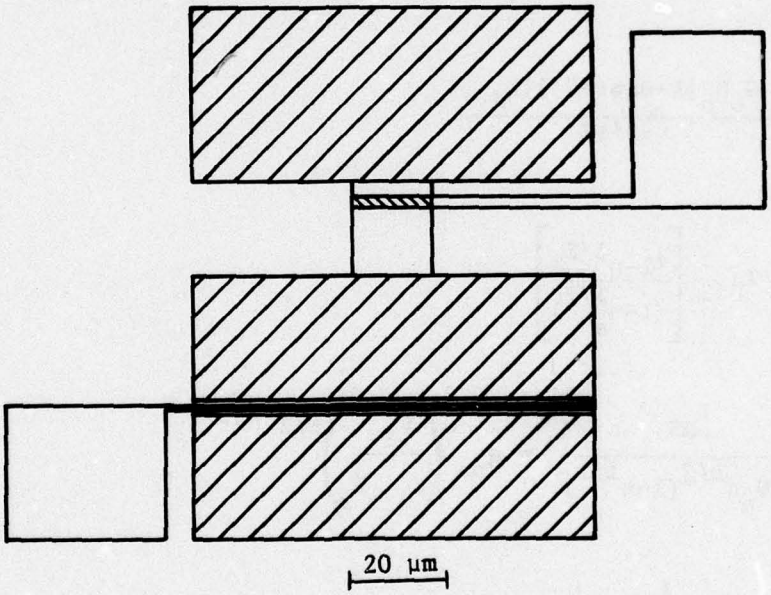



Figure 1. Schematic of an integrated TELD-FET with a capacitive-pickoff electrode.

8. L. C. Upadhyayula, R. E. Smith, and J. F. Wilhelm, *Transferred-Electron Logic Device (TELD) Development*, Annual Report, Office of Naval Research Contract No. N00014-75-C-0100 and ONR Contract Authority Nos. NR 251-023 and NR 251-024, April 1977.

The current in the FET and TELD sections are matched by a proper choice of the device width and channel thickness. The optimum material parameters generally used for GaAs FETs are 8-10 x $10^{16}$ $cm^{-3}$ doping density with 5 to 8-V pinch-off voltage whereas the optimum doping density for TELDs is 4-8 x $10^{15}$ $cm^{-3}$ with a pinch-off voltage of about 30 V. Therefore, a compromise has to be made in both doping density as well as pinch-off voltage when both these devices have to be fabricated in an integral fashion. A doping density of 1-2 x $10^{16}$ $cm^{-3}$ with a pinch-off voltage of about 15 V was selected for our design. Further decrease in pinch-off voltage for FET sections can be realized by selective chemical etching.

1. FET Section Design

Graphical design procedures discussed by R. B. Fair [9] are used in the FET design. The FET saturation current ($I_{DSS}$), transconductance ($g_m$) and input gate capacitance ($C_g$) are related to the material parameters by the following relations:

$$I_{DSS} = \frac{G_o U_o [1-\exp(-\Gamma')] Z_d}{(\Gamma')2} \tag{1}$$

$$I_{DS} = I_{DSS} \left[ \frac{(1-\eta^{1/2})}{(1-\eta_s^{1/2})} \right] \tag{2}$$

$$g_m = \frac{I_{DS}}{2U_o \eta^{1/2} (1-\eta^{1/2})} = g_{ms} \left( \frac{V_B}{V_G + V_B} \right)^{1/2} \tag{3}$$

$$g_{ms} = \frac{I_{DSS}}{2U_o \eta_s^{1/2} (1-\eta_s^{1/2})} \tag{4}$$

9. R. B. Fair, "Graphical Design and Iterative Analysis of the DC Parameters of GaAs FETs," IEEE Trans. Electron Devices ED-21(6), 357 (June 1974).

$$C_g = \sqrt{\frac{\varepsilon en}{2(V_B+V_G)}}\ \ell_g W_g \tag{5}$$

$$G_o = ne\mu W_g a/\ell_g \tag{6}$$

where $\mu$ = low-field electron mobility;

$E_c$ = critical field at which electron velocity reaches a maximum ($\sim$3.9 kV/cm for GaAs);

$V_B$ = built-in diffusion potential for the Schottky barrier;

$V_G$ = external gate bias;

$W_g$ = gate width;

$\ell_g$ = gate length;

and $a$ = channel thickness.

$$\eta = \left(\frac{V_B + V_G}{U_o}\right);\ \eta_s = \left(\frac{V_B}{U_o}\right) \tag{7}$$

$$\Gamma' = \left(\frac{U_o}{\ell_g E_c}\right)\ \mu_m \tag{8}$$

and $Z_d = h_D/a$ = normalized channel height at the drain end. (9)

FET parameters have been calculated for two different doping densities and the results are summarized in Table 1. As expected, the transconductance is higher for heavily doped devices.

## 2. TELD Section Design

TELD sections were designed so that the threshold current ($I_{th}$) is smaller than the FET section drain saturation current ($I_{DSS}$). The FET quiescent drain current ($I_{DS}$) was chosen to lie between the TELD peak ($I_{th}$) and the valley ($I_v$) currents. The TELD cathode-anode spacing was chosen to provide substantial output voltage at the capacitive electrode and yet operate at the desired repetition rate. The dimensions of the capacitive-pickoff electrode were chosen so that

TABLE 1. FET PARAMETERS CALCULATED AS A FUNCTION OF DOPING DENSITY

| Doping Density $n(cm^{-3})$ | Pinch-Off Voltage $V_o$ | From Fair's Curves [9] for $l_g$ = 1.0 μm $W_g$ = 500 μm | | For our Proposed Geometry with $l_g$ = 1.0 μm W = 90 μm | | | |
|---|---|---|---|---|---|---|---|
| | | $I_{DS}$(mA) | $g_{ms}$(ms) | $V_G$(V) | $I_{DS}$(mA) | $g_m$(ms) | $C_g$(pF) |
| $2.0 \times 10^{16}$ | 5.0 | 55 | 22 | -2.0 | 7.0 | 2.0 | 0.023 |
| $1.0 \times 10^{16}$ | 5.0 | 48.0 | 19 | -1.5 | 4.6 | 1.92 | 0.0180 |

a large fraction of the domain voltage could be coupled to the input of the following logic gates.

The amplitude of the output voltage is given by:

$$\Delta V_o = \alpha K V_{th}$$

where $\alpha$ = coupling coefficient

$K$ = percentage current drop

$V_{th} = \ell E_{th}$ = threshold voltage

and $E_{th}$ = threshold field for TE effect

The transit length $\ell$ of the TELD is fixed by the maximum operating frequency and power dissipation considerations. A transit length of 20 μm was chosen for our devices resulting in a threshold voltage of about 8.0 V. For the material under consideration, the K values range from 0.3 to 0.4. The coupling coefficient $\alpha$ can be expressed in terms of the domain capacitance ($C_d$), gate input capacitance ($C_g$) and fan-out factor Z as

$$\alpha = \frac{Cd}{Cd + ZC_g} \tag{10}$$

The threshold current $I_{th}$ is given by

$$I_{th} = nev_{th}Wd$$

TELD threshold current has been selected to be compatible with that of FETs shown in Table 2. Low field mobility values of 6000 and 5500 $cm^2/V^{-1}s^{-1}$ have assumed for $1 \times 10^{16}$ and $2 \times 10^{16} cm^{-3}$ GaAs, respectively. For a device width of 15 μm, the TELD parameters are given in Table 2.

3. Integral TELD-FET Device

The integral TELD-FET characteristics are then summarized in Table 3. This table indicates that a positive input signal ΔV, produces a current increase ΔI in the TELD. Consequently, the TELD thresholds and produces an output voltage ΔV (same as the input) under the maximum fan-out (Z) requirement envisioned in our applications (e.g., Z = 1.33 in the full ADDER).

TABLE 2. TELD PARAMETERS CALCULATED AS A FUNCTION OF DOPING

| Doping Density | Channel Thickness d(μm) | Peak Velocity up (cm/s) | Fractional Current Drop K | Domain Capacitance Cd(pF) |
|---|---|---|---|---|
| $2.0 \times 10^{16}$ | 1.0 | $1.6 \times 10^{7}$ | 0.35 | 0.00518 |
| $1.0 \times 10^{16}$ | 1.5 | $1.74 \times 10^{7}$ | 0.40 | 0.0059 |

TABLE 3. INTEGRAL TELD-FET CHARACTERISTICS

| Doping Density $n(cm^{-3})$ | α | ΔV (V) | ΔI (mA) |
|---|---|---|---|
| $2.0 \times 10^{16}$ | 0.145 | 0.4 | 1.6 |
| $1.0 \times 10^{16}$ | 0.197 | 0.63 | 1.2 |

C. MSI TEST VEHICLE

A full ADDER has been chosen as a test vehicle for TELD MSI technology development. In a full ADDER, the sum ($S_n$) and carry ($C_n$) for the $n^{th}$ bit are generated from the data inputs $X_n$ and $Y_n$ and the carry from the previous bit $C_{n-1}$. The expressions used in generating $S_n$ and $C_n$ are:

$$S_n = (X_n \oplus Y_n) \oplus C_{n-1} \tag{11}$$

$$C_n = X_n Y_n + X_n C_{n-1} + Y_n C_{n-1} \quad (12)$$

Therefore, $S_n$ can be realized with a two-stage, two-input exclusive-OR and $C_n$ can be realized with a two-out-of-three MAJORITY gate. The design of the exclusive-OR and MAJORITY gates and the implementation of the full ADDER are discussed below.

1. Exclusive-OR Circuit

Figure 2(a) is an exclusive-OR circuit conceived at the beginning of the program. The two-input FET section and the TELD output section form a two-input OR. The second two-input FET section along with the current limiter form the inhibit circuit.

In the quiescent state, the FET sections are biased so that the TELD current is below the threshold current ($I_{th}$) and the FET current limiter is in the linear part of its I-V characteristic. When a single (positive) input is applied, TELD current reaches the threshold value. Domains are nucleated and an output appears at the capacitive electrode. When both the inputs (positive) are present, the total current exceeds the limiter current and a substantial part of the voltage is dropped across the limiter and TELD domain formation is inhibited. The currents in various sections of the circuit are adjusted by a judicious selection of the channel widths.

A modified exclusive-OR circuit which was designed toward the end of the present program phase is shown in Fig. 2(b). This circuit utilizes a positive signal at the FET input for triggering and a negative pulse for inhibition. The required positive and negative signals are obtained at the capacitive output and at the FET drain electrode, respectively, in a TELD-FET combination device. This circuit also has one gate delay. This modified exclusive-OR circuit, if used in the full adder, reduces the fan-out requirement of the drive circuits from 1.33 to 0.63 and also reduces the dc dissipation from 400 mW to 250 mW. As a result of these important advantages, we will try to incorporate this circuit in our efforts during the next program phase.

2. MAJORITY Gate

Figure 3 shows a three-input MAJORITY gate. The three FETs serve as input sections and the TELD with the capacitive electrode provides the output. The

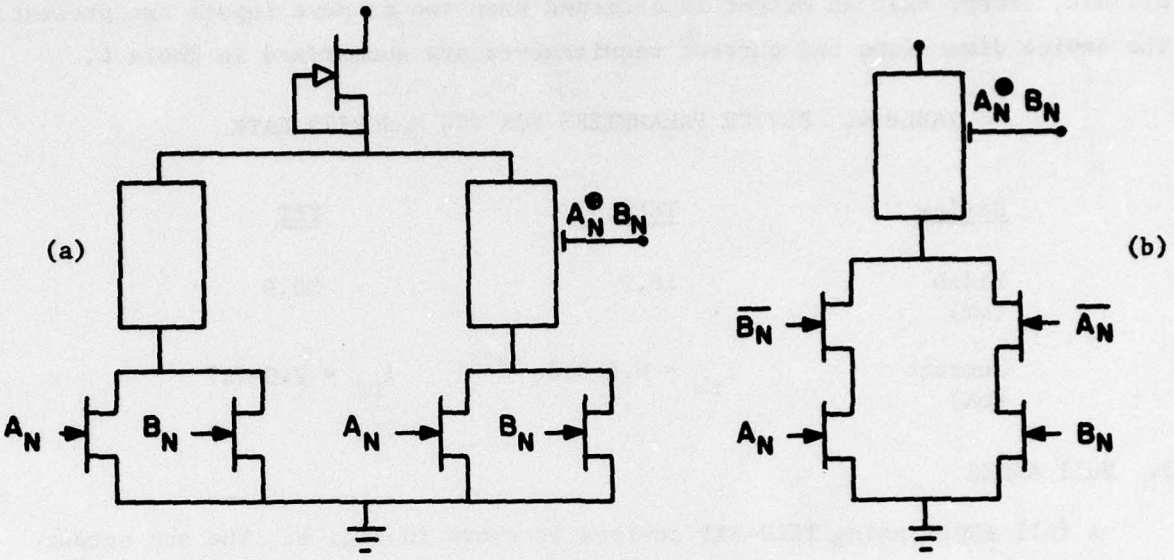



Figure 2. Exclusive-OR circuits. (a) A two-input exclusive-Or circuit with TELD-FET devices. (b) Modified circuit for exclusive-OR.

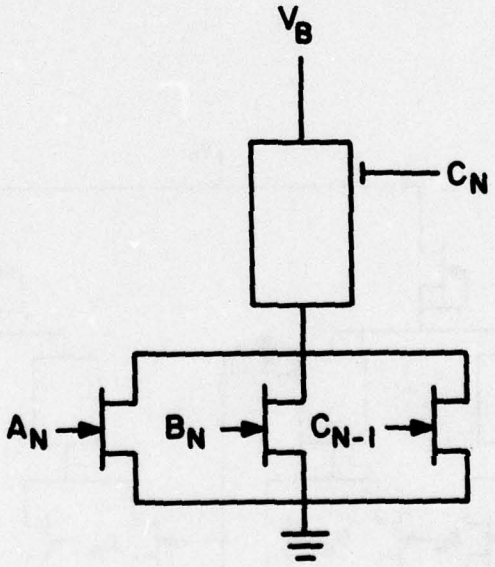



Figure 3. A TELD-FET 2/3 MAJORITY gate.

biasing and operation of the TELD-FET are similar to that of the exclusive-OR circuit, except that an output is obtained when two or more inputs are present. The device dimensions and current requirements are summarized in Table 4.

TABLE 4. DEVICE PARAMETERS FOR THE MAJORITY GATE

| Device | TELD | FET |
|---|---|---|
| Width (μm) | 16.5 | 30.0 |
| Current (mA) | $I_{th}$ = 6.6-8.8 | $I_{DS}$ = 2.0-2.7 |

3. Full ADDER

A full ADDER using TELD-FET devices is shown in Fig. 4. The sum output is generated in a two-stage, two-input exclusive-OR circuit and the carry output is generated in a two-out-of-three MAJORITY gate. Figure 5 shows the layout of the monolithic adder. The transit time for TELDs is about 200 ps and therefore, the circuit is expected to work at 2-3 gigabit-rates.

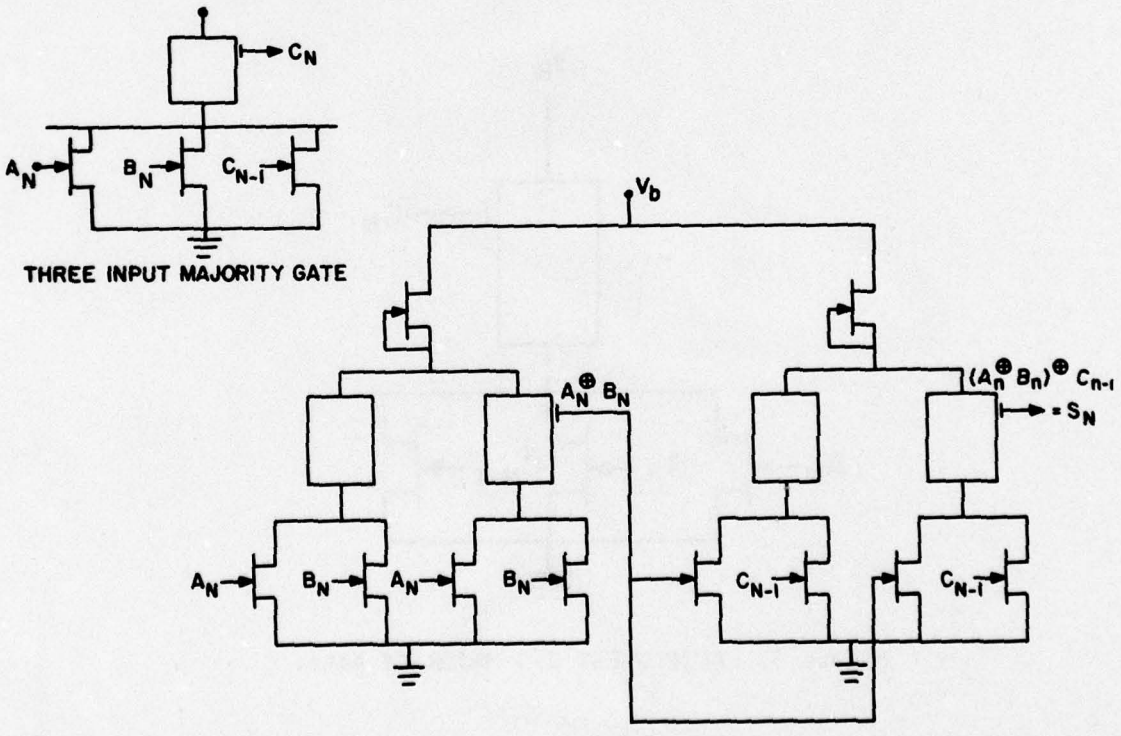



Figure 4. Schematic of the TELD-FET full ADDER.

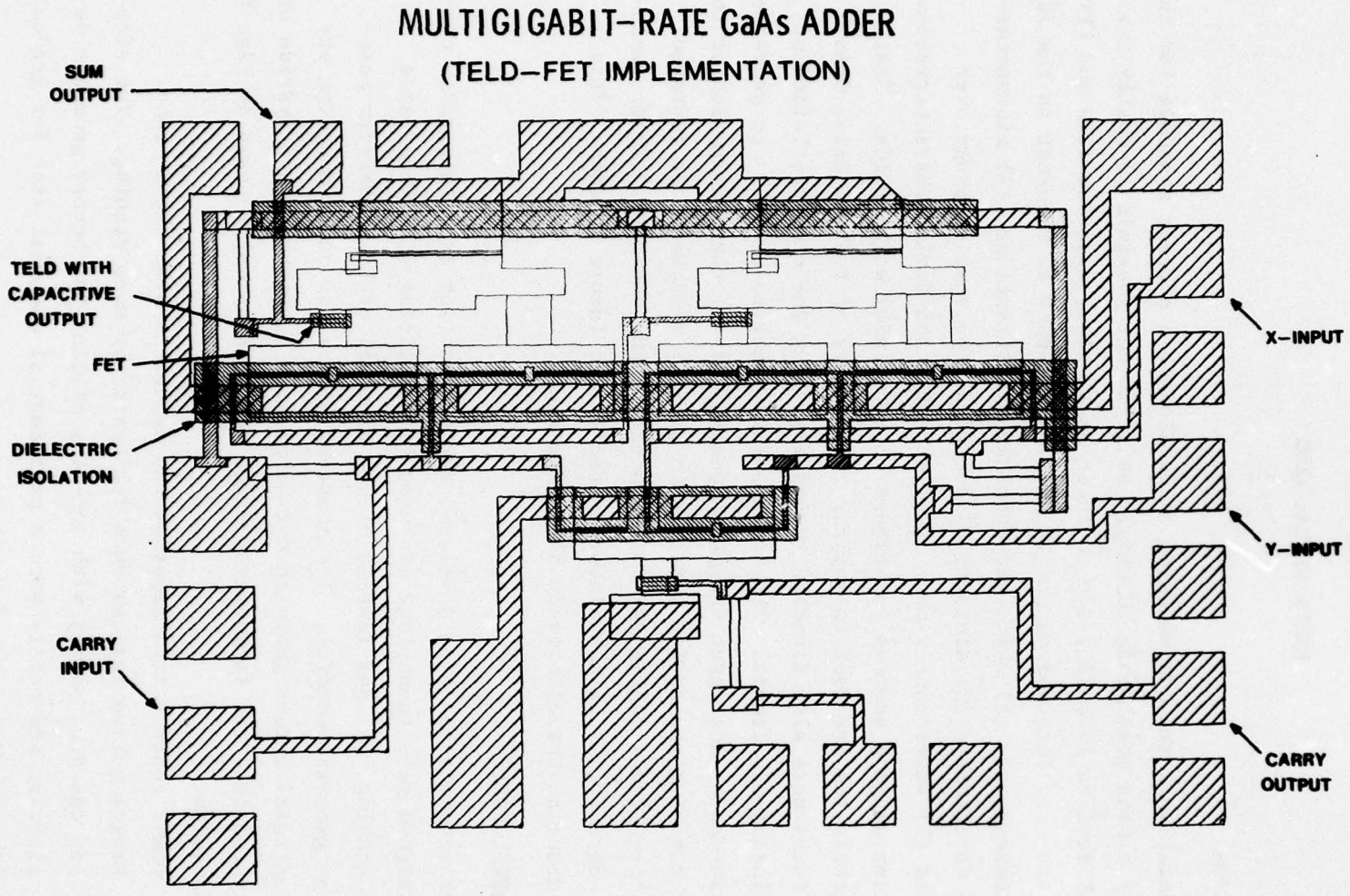



Figure 5. Multigigabit-rate GaAs ADDER (TELD-FET implementation).

## SECTION III

## EXPERIMENTAL WORK

### A. INTRODUCTION

Experimental work was concentrated on developing a process schedule for the fabrication of a GaAs monolithic IC chip. As it is not possible to easily test the individual devices in an IC, due to their small size, discrete TELD and FET test devices are also included on the IC chip. The areas of interest in the IC process development are: (1) ohmic and Schottky metallizations, (2) micrometer-size geometry definition, (3) dielectric isolation, (4) step coverage over mesa edges, and (5) interconnections. Good material and device characteristics are as important as good process techniques for obtaining working ICs. Test device characteristics are used to monitor the quality of the epitaxial GaAs material. Efforts were also directed toward improving the characteristics of the basic exclusive-OR circuit. The improvements required are: (a) to decrease the load or fan-out on the input trigger signals, and (b) the elimination of the necessity for matching the device currents in so many branches. An improved exclusive-OR circuit was configured with discrete TELDs and FETs. After evaluation of this circuit, it will be incorporated in the future IC chip. This section will describe the efforts in all these areas.

### B. PROCESS DEVELOPMENT

A process schedule has been developed for fabricating GaAs integrated circuits. Self-aligned gate technology was used for realizing micrometer-size gates and dry etching was used instead of wet chemical etching wherever possible for better geometry control. The starting wafers for our processing are $n^+$-n-SI GaAs epitaxal wafers grown in our laboratory by either vapor hydride or trichloride synthesis. The fabrication steps are schematically shown in Fig. 6, and summarized below.

1. Ohmic contact metallization was deposited over the $n^+$ face.
2. Device active regions were delineated by mesa etching. The etching was done partly with ion-beam milling for better geometry definition and partly with a preferential chemical etch for gradual sloping mesa edges for gates.

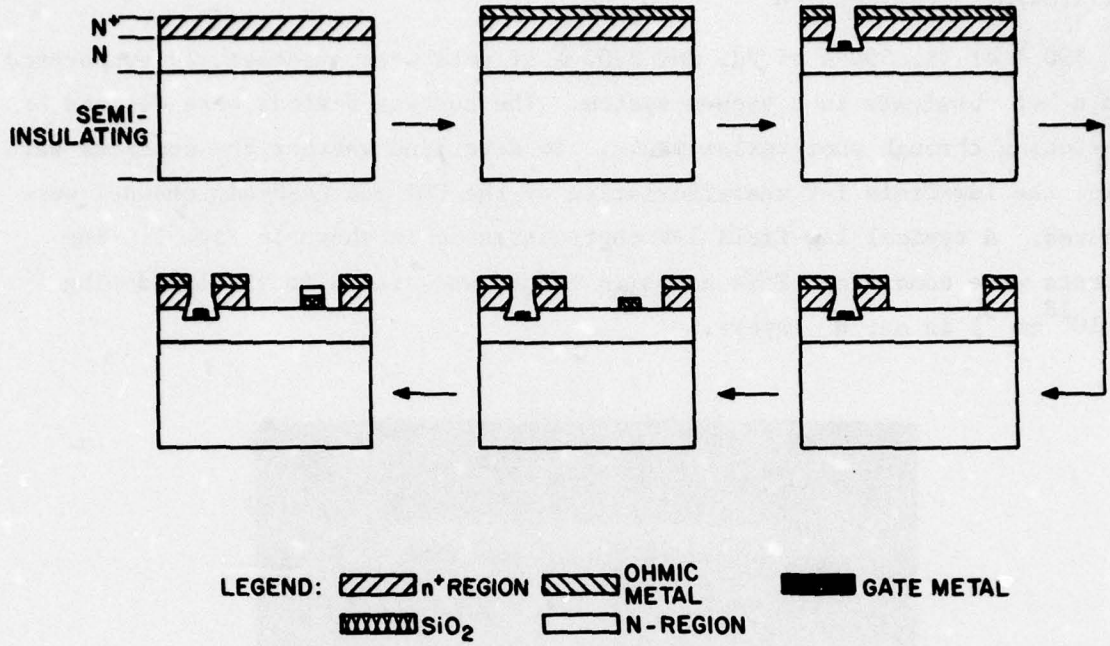



Figure 6. Process schedule for the fabrication of self-aligned gate TELD-FET devices.

3. FET channels were opened with ion-beam etching (IBE). A chemical touch-up etch was used to undercut the source-drain regions and provide overhangs for self-registration of gates.
4. Ti/Pd/Au metallization was deposited to form FET gates and some of the interconnections.
5. TELD active regions are opened using IBE and the channel thickness adjusted so that the TELD and FET currents are compatible.
6. $SiO_2$ and/or $Si_3N_4$ dielectric layers were deposited either by CVD or by plasma deposition.
7. Capacitive pickoff and interconnect regions were defined.
8. Ti/Pd/Au second-level interconnections and bonding pads were formed.

## C. OHMIC METALLIZATION

Ti/Pd/Au and Au:Ge/Ni systems were evaluated to form ohmic contacts in the IC fabrication.

1. Ti/Pd/Au Metallization

300 Å of Ti, 500 Å of Pd, and 2200 Å of gold were successively evaporated onto a hot substrate in a vacuum system. The contact regions were defined by ion-etching through photoresist masks. To determine whether the contacts were ohmic, the low-field I-V characteristics of the FET source-drain channel were measured. A typical low-field I-V characteristic is shown in Fig. 7. The contacts were nonohmic. This nonohmic nature was traced to the low doping ($<3\times10^{18}$ $cm^{-3}$) in our $n^+$ layers.

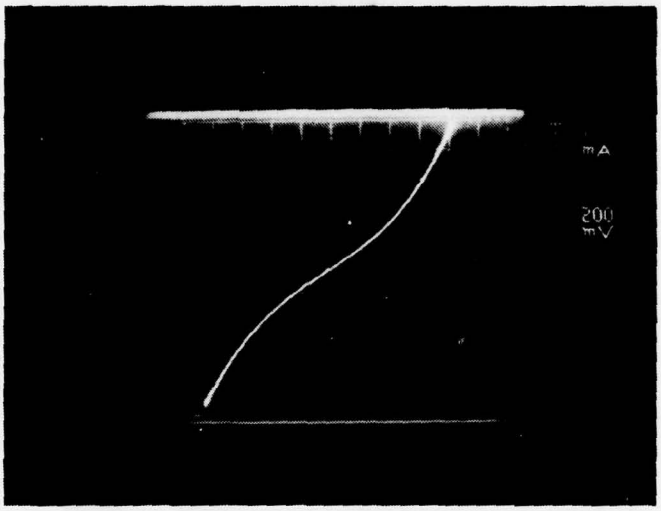
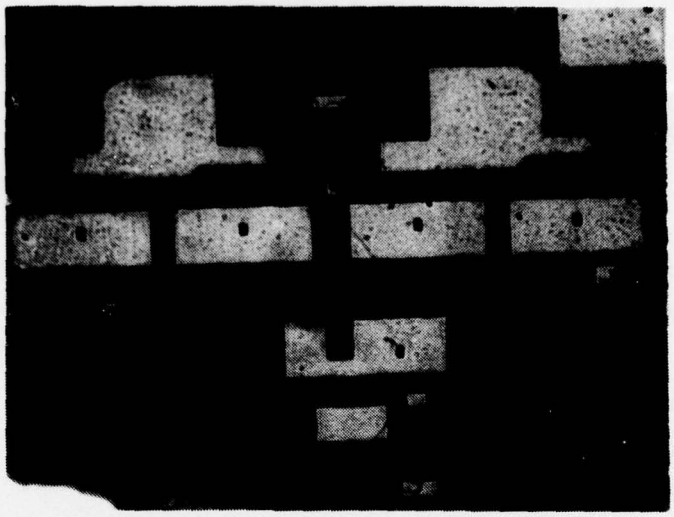


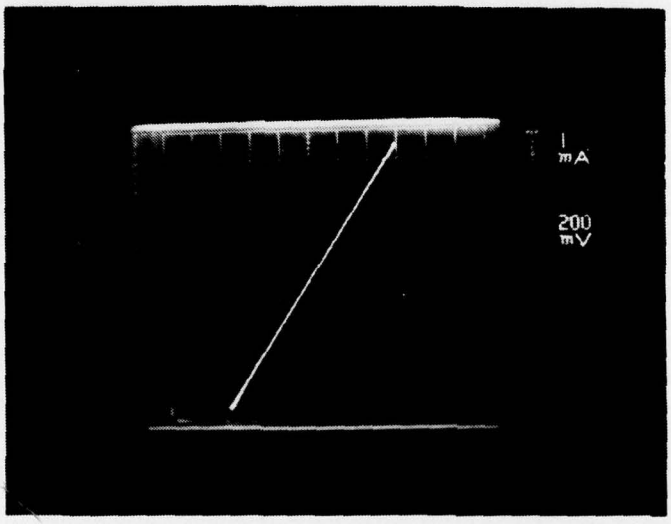

Figure 7. Low-field I-V characteristic of Ti/Pd/Au contacts to $n^+$ GaAs.

2. AuGe Contacts

Earlier in the TELD development program, Au-Ge (12%)/Au-Ni(18%) metallization was used to make ohmic contacts to n or $n^+$ regions. These contacts were ohmic, however, considerable balling occurred, which made it unsuitable for defining the micrometer-size gates required for the FET sections. The contact balling is probably due to the smaller amount of Ni present in the evaporated films. The Ni content was then increased by evaporating a thin film of Ni. We found that 1500 Å of Au-Ge, 250 Å of Ni and 2200 Å of Au-Ni result in good ohmic contacts without any balling. Figure 8 shows the surface quality of these films and the ohmic nature of these contacts.



(a)




(b)

Figure 8. Au:Ge/Ni/Au:Ni contacts on GaAs. (a) Surface of the sintered contacts. (b) Low-field I-V characteristic showing the ohmic nature of the contact.

## D. SCHOTTKY-BARRIER GATES

Titanium and aluminum are widely used for gates in GaAs power FETs. However, IC fabrication requires that dielectric isolation layers be deposited subsequent to Schottky-gate fabrication. These dielectric layers are generally deposited at temperatures well over 300°C. Therefore, the gate metallization must withstand this temperature without increasing the gate leakage current substantially.

### 1. Al Gates

About 3000-Å-thick Al was vacuum-deposited onto GaAs substrates and then heat-treated at 350°C for 5 min in a hydrogen atmosphere. The barrier potential increased from 0.5 to 0.8 V and the leakage current decreased from 20 μA to 5 μA for 250-μm-diameter Schottky diodes.

These Schottky diodes did not show any observable changes in their characteristics when they were subjected to a 370°C-temperature cycle during the CVD-$SiO_2$ deposition.

Gold interconnections are desirable because of their higher conductivity and better bondability. Gold, however, interacts with aluminum and forms a highly resistive intermetallic compound. Ti/Pd and Cr/Pd have been suggested [10] as buffer layers to prevent intermetallic diffusion. We have incorporated 500 Å of Ti or Cr and 1000 Å of Pd as buffer layers between Al and Au. After the gold evaporation, the barrier potential decreased from 0.8 to 0.5 V indicating that the buffer layers were not effective and intermetallic diffusion did indeed take place. This problem requires further study.

### 2. Ti/Pd/Au Gates

Titanium adheres well to GaAs and forms reasonably good Schottky barriers. Pd serves as a barrier between Ti and Au. This metallization scheme yielded good Schottky barriers but the barrier potential is only about 0.5 V. This metallization scheme also withstood the 350-370°C temperature cycling required in the subsequent process steps.

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## E. MICROMETER GEOMETRIES

The smallest dimension in our device is the gate length which is about 1.0-1.25 μm. This is routinely achieved by using RCA's self-aligned gate technology for power FETs. Therefore, self-aligned gate technology was used in the fabrication of FET sections and standard alignment and delineation techniques were used in the fabrication of TELD sections and interconnections.

## F. DIELECTRIC LAYERS

In our IC processing, dielectric layers are required for the capacitive-pickoff electrode and for crossovers in two-level metal interconnections. For capacitive-pickoff electrodes, the thickness of the dielectric layer should be small ($\sim$0.1-0.2 μm) and the relative dielectric constant should be high ($\varepsilon_r \sim 8$-12). For the metal crossovers, on the other hand, the thickness of the dielectric layers should be as large as possible (1-2 μm) and the relative dielectric constant should be as small as possible ($\varepsilon_r \sim 1$-4). In view of these conflicting requirements, we intended to use $Si_3N_4$ for capacitive pickoff and phosphorus-doped $SiO_2$ for crossovers. $Si_3N_4$ and P-$SiO_2$ have different etch rates both in chemical and plasma etchings. This property can be used to advantage in chip processing.

Undoped or doped $SiO_2$ was deposited by CVD technique at the substrate temperature of 350-370°C. $Si_3N_4$ was deposited in a plasma deposition system at a substrate temperature of 300°C.

## G. STEP COVERAGE AND INTERCONNECTIONS

The regions of concern for step coverage in our chip processing are located at: (1) the active device mesa edges at the FET gate and TELD output electrode, and (2) the interconnections through etched holes in dielectric isolation layers for crossovers.

### 1. Step Coverage at the Active Device Mesa Edge

The n-layer thicknesses for the FET and TELD sections are 0.7-1.0 μm and 1.0-1.5 μm, respectively. The mesa etching was carried out partly by ion-beam milling for better geometry definition and partly by preferential chemical etch ($1H_2SO_4:8H_2O_2:1H_2O$) to obtain gradual sloping edges. The thickness of the metallization used is about 3000-4000 Å.

2. Step Coverage in $SiO_2$

7.5-μm-wide lines were used for input and output signal connections and 10-15 μm-wide lines were used for bias connections. The bias connections were made through etched holes in the dielectric. The mesa step is about 0.7-1.2 μm. Experiments were carried out to determine the suitability of wet chemical and dry plasma etching. Figure 9 shows a picture of the 7.5-10 μm Ti/Pd/Au metal lines across a 0.7-μm mesa step chemically etched in $SiO_2$. The thickness of the metal is 5000-6000 Å. The metal lines were continuous but the sheet resistivity of the metal was a factor of 2 higher than expected. This increase in sheet resistivity is due to the poor step coverage.

Figure 9. 7.5 to 10-μm Cr/Au-metal lines across a 0.75-μm-thick $SiO_2$ mesa step. (Magnification = 800).

1-μm-thick phosphorus-doped (2-7.5%) $SiO_2$ films were plasma-etched in $CF_4$ plasma using 100 W of power level. Figure 10 shows the etch rate as a function of phosphorus content. The etch rate increased with the increase in the phosphorus content. The mesa edges had almost a 45° slope which is very desirable for interconnections.

## H. INTEGRATED-CIRCUIT FABRICATION

The technology developed under this program is directed toward IC chip processing. Self-aligned gate technology, ion-beam etching, and plasma etching

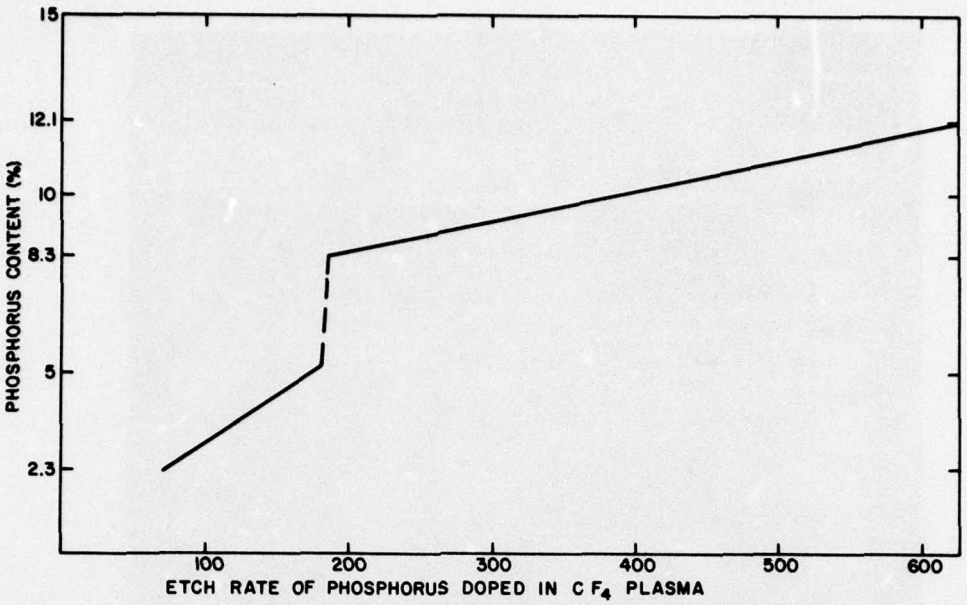



Figure 10. Etch rate of phosphorus-doped $SiO_2$ in $CF_4$ plasma.

are crucial steps in IC fabrication. This technology has been successfully used in the fabrication of a GaAs monolithic full ADDER. Figure 11 shows a fabricated IC chip.

## I. EVALUATION

A device test pattern was interlaced with an IC chip pattern to allow evaluation. Test device characteristics were used to determine the quality of the GaAs epitaxial layers to estimate their adequacy for proper IC operation.

### 1. FET Section

The transfer characteristics of a typical split-gate FET is shown in Fig. 12. The total channel width is 90 μm, the width of each gate is 45 μm, the drain saturation current ($I_{DSS}$) is 7.0 mA, and the dc transconductance for each gate is 1.0 mS. The doping density in the n-channel is about $2x10^{16} cm^{-3}$ and channel thickness is 1.0 μm.

The measured FET parameters are in reasonable agreement with those calculated. The FET channel thickness used is somewhat higher than that used in the calculations. This might indicate slightly lower mobilities in the epitaxial layers.

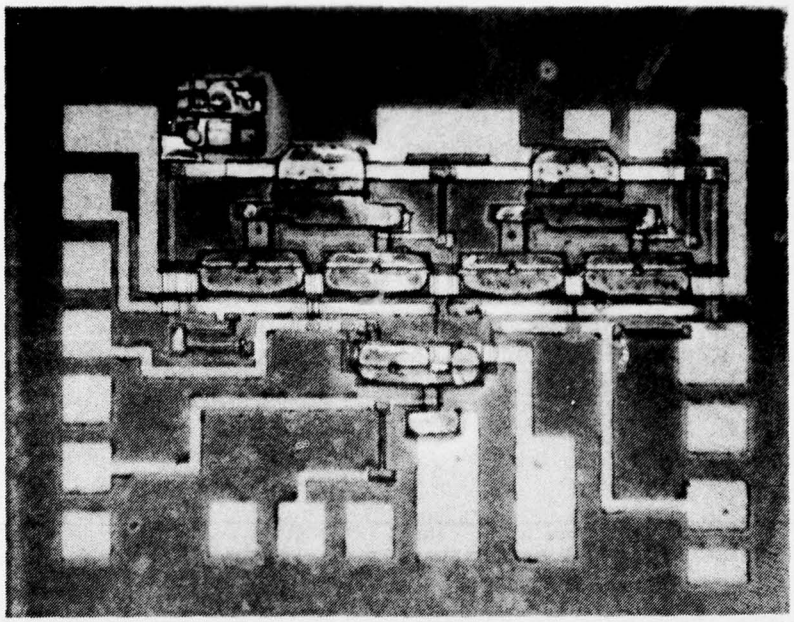


Figure 11. Photomicrograph of a fabricated GaAs full ADDER.

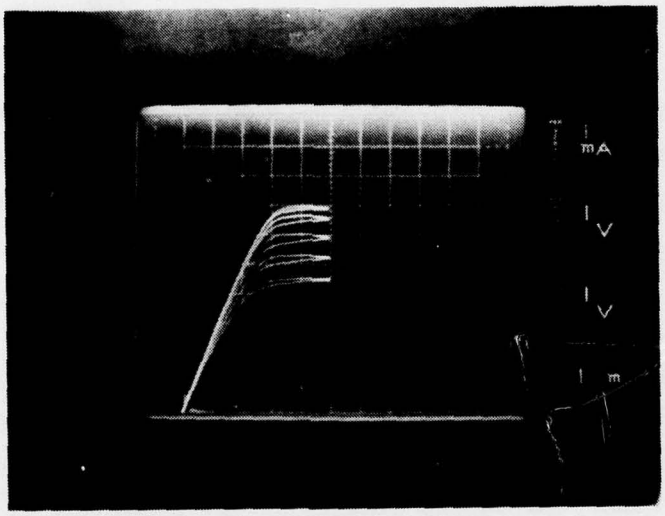



Figure 12. DC transfer characteristics of FET.

2. TELD Section

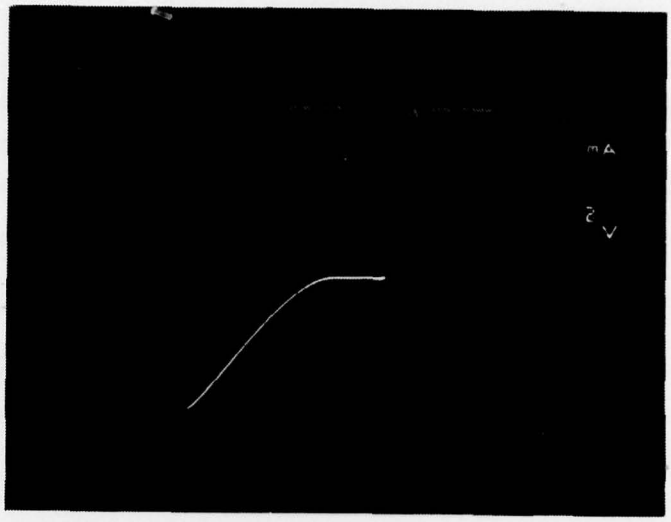
Figure 13(a) shows the typical I-V characteristics of a TELD. The I-V characteristic does not show any thresholding and the current saturation occured at 11 V. This is not clearly understood at this time. However, TELDs fabricated from a recent wafer grown by trichloride synthesis showed a 15-20% current drop with 6-mA threshold current and 8.5-V threshold voltage (Fig. 13(b)). Threshold current and voltage are closer to the design values, but a current drop of 30% is desirable for the operation of the IC chip.

3. Integrated Circuit

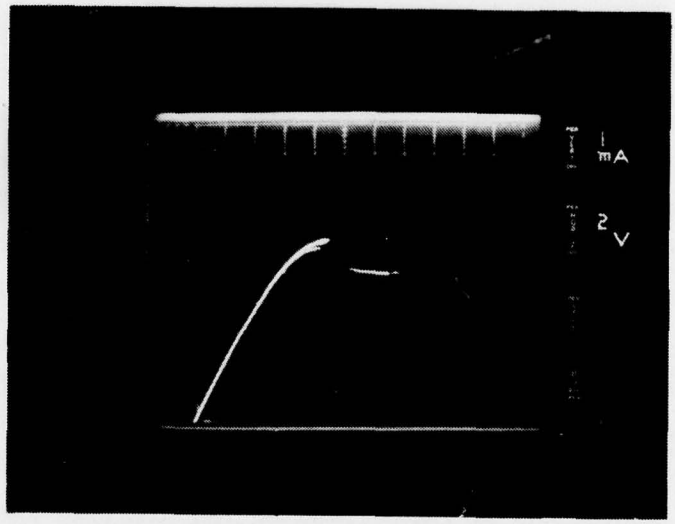
The integrated circuit has not been evaluated. It is, however, necessary that both TELDs and FETs should operate satisfactorily before the integrated circuit can be evaluated. Improvements in the quality of GaAs epitaxial layers grown in our arsenic-trichloride reactor have been reported recently. With the availability of such wafers for this program, full ADDER IC chips will be fabricated and electrical performance evaluated.

4. Evaluation of TELDs with Capacitive Output

Discrete TELDs with capacitive-output electrodes were fabricated at the end of the previous program phase. In the early part of the current program, a few of these devices were evaluated in circuits. The cathode-anode spacing for this device is 20 μm and the capacitive probe is located 5.0 μm from the anode. An integral cathode resistor is also included in the device. In order to study the switching characteristics of these devices, the two-stage cascaded circuit shown in Fig. 14 was fabricated. The two TELDs were biased just below threshold value and the first device was triggered by a negative pulse from a charge line pulser. The capacitive output of the first device was used to trigger the second device. The output at the capacitive electrode and the cathode of the second device were monitored on the sampling scope. Figure 15 shows the output waveforms of the second device. The capacitive output shows both positive and negative peaks and the cathode output shows only negative peaks, as expected from theory. This also confirms that the capacitive output provides enough signal voltage to trigger at least one similar device.




(a)




(b)

Figure 13. I-V characteristics of TELDs. (a) Typical characteristics of a device fabricated from a wafer grown by vapor hydride synthesis. (b) Typical characteristics of a device fabricated from a wafer recently grown by trichloride synthesis.

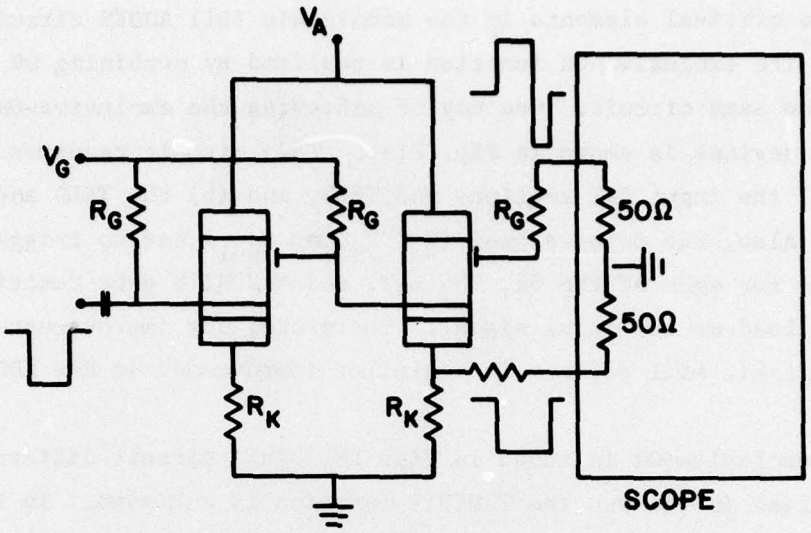



Figure 14. Cascaded circuit with capacitive-output TELDs.

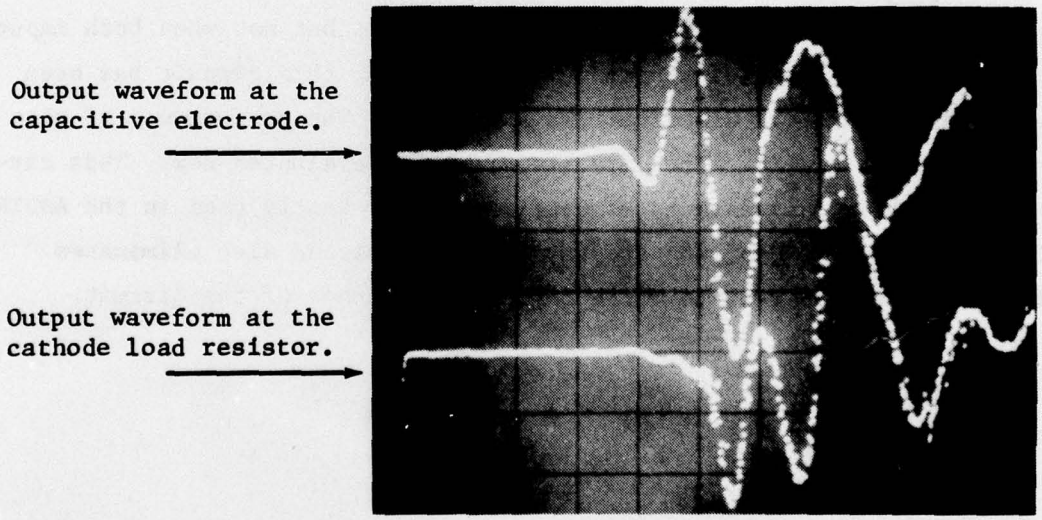



Figure 15. Performance of cascaded TELDs with capacitive-output electrodes.

## 5. Modified Exclusive-OR

One of the critical elements in the monolithic full ADDER circuit is the exclusive-OR. The exclusive-OR function is realized by combining OR and INHIBIT functions in the same circuit. One way of achieving the exclusive-OR function using TELD-FET devices is shown in Fig. 2(a). This circuit requires current matching in (a) the input FET sections and TELD, and (b) the TELD and FET current limiter. Also, the input signal ($X_n$, $Y_n$, or $C_{n-1}$) has to trigger three FET gates - one for each of the OR, INHIBIT, and MAJORITY gate functions which puts excessive load on the input signal. Therefore, any improvements in the exclusive-OR circuit will reflect in a similar improvement in the ADDER circuit.

Modified exclusive-OR is shown in Fig. 16. This circuit differs from that shown in Fig. 2(a) in the way the INHIBIT function is achieved. In the modified exclusive-OR, the INHIBIT function is achieved by utilizing the negative output pulse present at the drain of the TELD-FET combination device. The INHIBIT circuit is schematically shown in Fig. 17. FET-1, FET-2, and TELD-1 form the INHIBIT circuit, and FET-3, FET-4, and TELD-2 form the switching circuit. TELD-2 provides an output when the input B is present, but not when both inputs A and B are present. In order to study its operation, this circuit has been fabricated in MIC form with discrete FETs and TELDs. The performance of this circuit is shown in Fig. 18. The circuit is further evaluated now. This circuit appears to offer many advantages over the one presently used in the ADDER chip. It reduces the load on the trigger input signal and also eliminates the need to match the current in three different branches of the circuit.

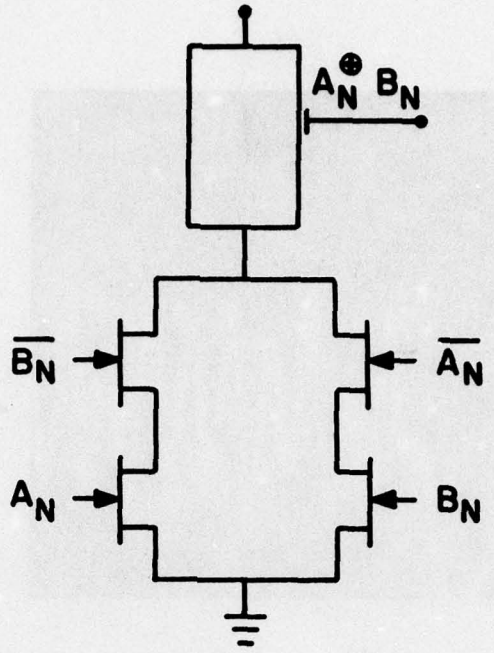



Figure 16. Modified circuit for exclusive-OR. (Also shown as Fig. 2(b).)

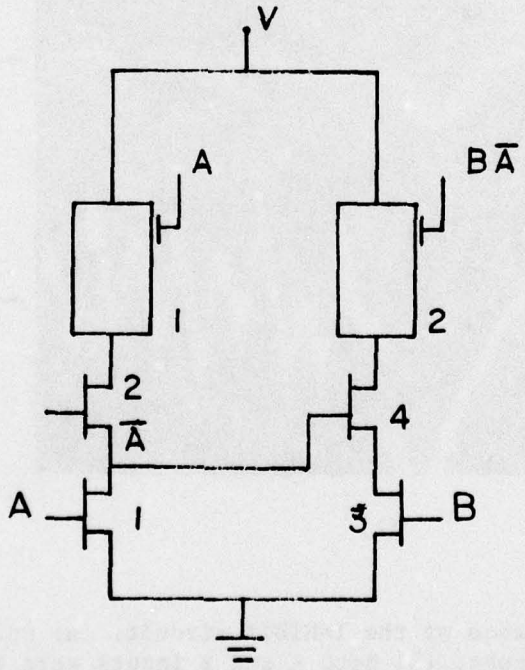
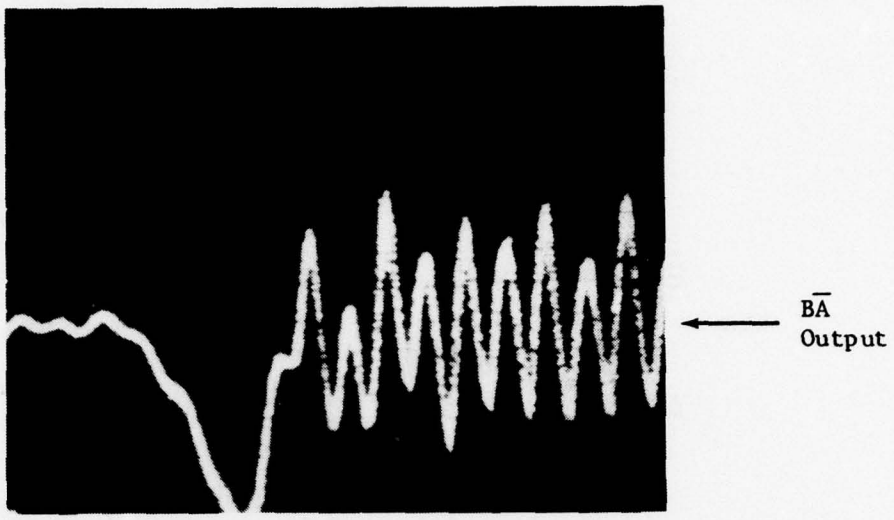
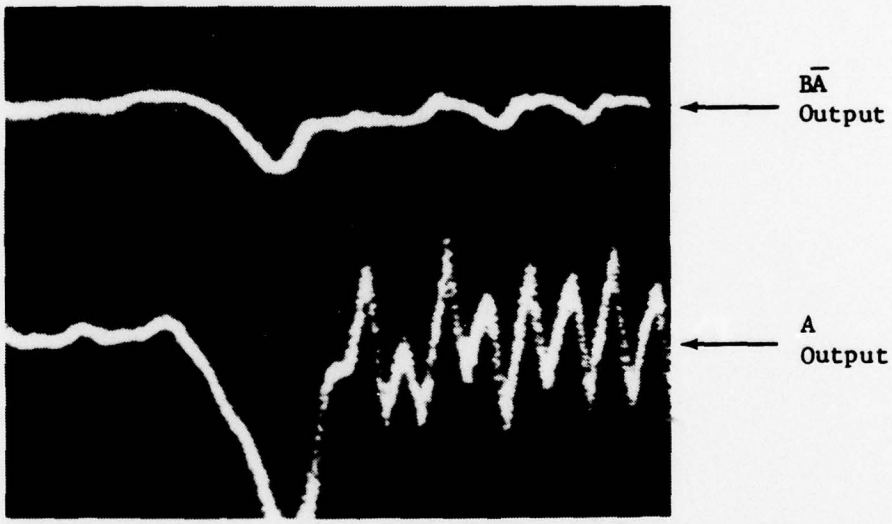



Figure 17. Schematic of the INHIBIT circuit.




(a)




(b)

Figure 18. Performance of the INHIBIT circuit. (a) Only B input was present. (b) Both A and B inputs were present. Vertical scale: 20 mV/div. Horizontal scale: 200 ps/div.

## SECTION IV

## CONCLUSIONS AND RECOMMENDATIONS

The progress made during this program period has been described in the previous sections. GaAs MSI circuits have been fabricated and are being evaluated. It is necessary to demonstrate operation of the simple logic circuits before the MSI circuits can be evaluated. This section summarizes the results achieved so far and makes recommendations for further work.

### A. CONCLUSIONS

TELD-FET devices with capacitive output were designed. Exclusive-OR, CARRY, and full ADDER circuits were designed with TELD-FET devices. A process schedule has been developed for the fabrication of GaAs MSI circuits.

One bit of the ADDER is 0.65 mm x 0.45 mm in size. It is expected to operate at 2-3-gigabit clock rates and dissipate 300-400 mW of dc power. Discrete test FETs fabricated on the IC chip showed drain saturation current ($I_{DSS}$) and transconductance which are in agreement with the calculated values. Recently, fabricated discrete TELDs on the IC chip showed 15-20% current drop. A current drop of 30% is desirable for the ADDER IC chip to function satisfactorily.

### B. RECOMMENDATIONS

Exclusive-OR, and CARRY circuits must be fully evaluated before testing the MSI ADDER. The parameters of interest are: (1) trigger sensitivity, (2) power dissipation, and (3) propagation delay and fan-out. If the fan-out is not adequate in the present circuit configuration, an improved exclusive-OR circuit, presently under investigation, must be incorporated in the ADDER circuit.

GaAs epitaxial layers grown by trichloride synthesis are promising. Efforts should be made to grow high-resistivity buffer layers to improve the epitaxial material quality to further improve device characteristics. The gate length of the FET input section in our present IC fabrication is about 1.25 μm. The gate length should be reduced to 1.0 μm which will result in a 25% decrease in the required fan-out. Selective doping for TELD and FET channels using ion implantation should be investigated.

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