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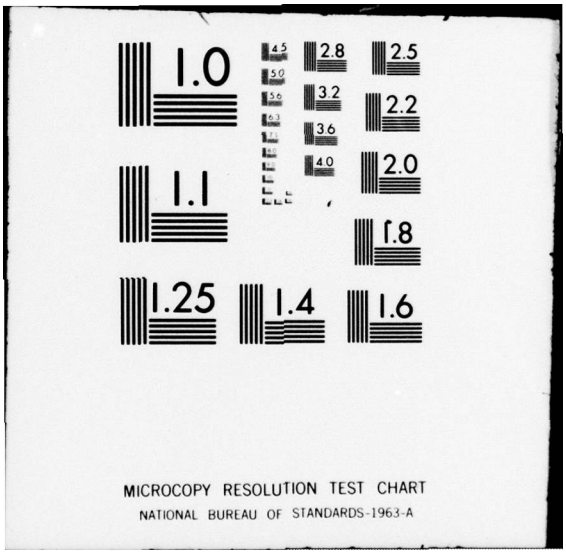
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JOSEPHSON A/D CONVERTER DEVELOPMENT

Annual Technical Report
to
Office of Naval Research, Code 427
Arlington, VA 22217

May 1, 1977 to April 30, 1978
Contract Number N00014-77-F-0048
Contract Authority NR 383-040

by

C. A. Hamilton, R. E. Harris, R. L. Kautz,
R. L. Peterson, and D. B. Sullivan

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This report describes the first year of an effort to demonstrate an ultra-high-speed analog-to-digital converter using superconducting electronics. Fabrication methods capable of producing a complete eleven layer circuit have been developed. Testing techniques enable 70 ps risetime signals to be sent onto or off of a chip. Experimental and theoretical characterizations of superconducting striplines are in good agreement.

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A.1. "Photolithographic Fabrication of Lead Alloy Josephson Junctions," R. H. Havemann, C. A. Hamilton, and R. E. Harris, J. Vac. Sci. Technol. 15, 392 (1978).

A.2. "Fast Superconducting Instruments," by R. E. Harris and C. A. Hamilton, Future Trends in Superconductive Electronics, ed. by B. S. Deaver, Jr., C. M. Falco, J. H. Harris, and S. A. Wolf (American Institute of Physics, New York, 1978), pp. 448-458.

A.3. "Automatic 300 - 4 K Temperature Cycling Apparatus," C. A. Hamilton, Rev. Sci. Instrum. 49, 674 (1978).

A.4. "Picosecond Pulses on Superconducting Striplines," R. L. Kautz, J. Appl. Phys. 49, 308 (1978).

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JOSEPHSON A/D CONVERTER DEVELOPMENT

Electromagnetic Technology Division
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I. INTRODUCTION

This report describes results from the first year of a three-year program directed toward the demonstration of a 4-bit Josephson A/D Converter which will operate to frequencies of 300 MHz or higher. A subsequent goal would then be to use the experience gained in this effort along with some improved fabrication methods to push the concept into the microwave region (above 1 GHz).

The approach of this program has been to concentrate on fabrication methods during the early phases and to build gradually from simple, well-characterized circuits towards the final goal. There is, as yet, no firm commitment to a particular converter design. Two circuit designs are being studied, but any selection will probably await further experience with the simple circuits. Factors, such as reproducibility of critical current on a given chip, will certainly influence the design decisions. The selection of design will probably occur during this next (second) year of development.

Outside of the computer efforts at IBM and Bell Laboratories, little effort has been expended on fabrication methods which are highly reliable and reproducible. Some information from these laboratories has appeared in the literature and this has provided the basis for the fabrication methods described in this report. Our use of alloy films and the sputter-oxidation scheme for tunnel junction barriers are just two examples of fabrication methods which have been generated in the industrial research laboratories. The Josephson computer effort at IBM is quite large and we expect it to have continuing influence on the field in general and our effort in particular. Thus, while we have specific ideas about the directions of our effort, we expect that outside developments which occur along the way will to some extent affect the outcome of the program.

It should be noted that the junction switching measurements described in section V.3 are supported by ONR under contract N00014-78-0018. The results, which are complimentary to this program, are included in this report for completeness.

II. FABRICATION

During the period of this contract, nearly all of the processes required for fabricating superconducting integrated circuits have been developed. We have fabricated ground planes, insulating layers, Josephson junctions, and resistors. In fact, test circuits containing all of these items, in seven layers of material, have been fabricated.

Success in developing these processes now permits us to begin to construct circuits. Initial attempts to fabricate a complete, eleven layer, circuit are under way, and early success is expected.

In the following, we first list the various layers required in a complete circuit along with their functions. The process for fabricating each layer is described briefly. Then some of the special equipment developed for carrying out these processes is introduced. Finally we conclude with a discussion of some of the work which remains incomplete, some of the efforts which were unsuccessful, and speculation on the future course of the project.

To place these fabrication efforts in the proper perspective, it is useful to describe the expected nature of a complete circuit. Eleven layers will be present as shown in Table 1. The numbered items in Fig. 1 correspond to the seven layers already fabricated in one of our test circuits.

Forming each layer involves two distinct procedures: forming the material which comprises the layer, and patterning that material. Below we will describe how each layer is formed, but because patterning most of the layers is done by the same process, that process will be described here. (Layers 1 and 2 are patterned differently as will be described in the detailed discussion for those layers).

Table I

Layer	Material	Function
1	Niobium	Ground plane. Defines magnetic field configuration near junctions and forms striplines from conductors above it.
2	Nb_2O_5	Insulator above ground plane.
3	SiO	Additional insulator above ground plane. Low dielectric constant and readily variable thickness permit good control of stripline impendance.
4	$AuIn_2$	Resistors for terminating striplines, voltage dividers, etc.
5	Pb alloy Pb (88%) In (8%) Au (4%)	Junction base electrode and stripline conductor.
6	SiO	Forms window through which barrier is formed. Minimizes anomalous effects at junction edges.
7	Pb_xO_y In_xO_y	Insulating tunneling barrier formed by oxidizing base electrode.
8	Pb alloy Pb (98%) Au (2%)	Junction upper electrode.
9	SiO	Insulator between junctions and control leads.
10	Pb alloy same as layer 5	Control leads for junctions and additional stripline conductors.
11	SiO	Protective layer for entire circuit.

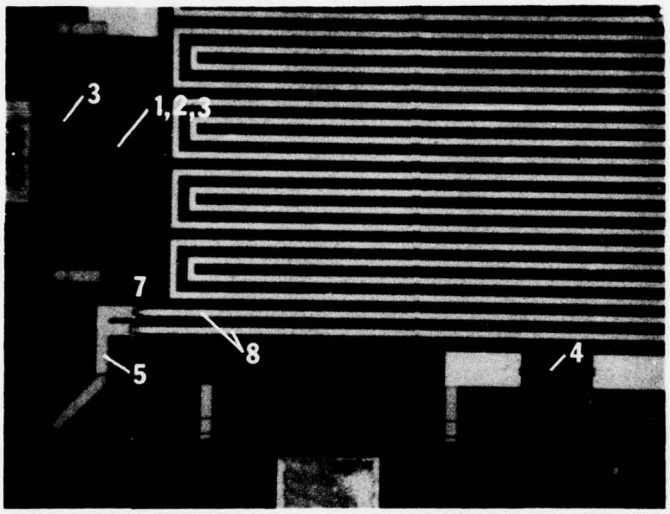


Figure 1

Corner of chip used for observation of junction switching. The numbers refer to layers described in Table I: 1, 2, and 3 are the Nb, Nb_2O_5 and SiO (the ground plane and insulators); 4 is a resistor; 5 is the Pb alloy base electrode; 7 is the tunnel barrier (lead oxide--at the overlap of layers 5 and 8); 8 is the upper electrode for the tunnel junction. This latter electrode connects to a stripline which is used to delay the junction transition in a measurement of switching speed.

II.1 Patterning with the Lift-Off Process

Layers 3 through 11 are patterned using a lift-off process. While this process is described briefly here, detailed discussions are in two of the attached papers and in interim reports for this contract.

In a lift-off process, the entire substrate is covered with photoresist. The resist is exposed and developed to remove it in areas where the substrate is to be coated with metal or insulator. Then the metal or insulator is deposited onto the entire substrate. Finally the substrate is immersed into a solvent. The photoresist dissolves, causing the material above it to flake off. The material which was not on top of resist adheres to the substrate producing the desired pattern.

One difficulty commonly occurs if material is unavoidably deposited onto the edges of the resist layer. Thus when the resist is dissolved, edges of the material which remain may protrude upward leading to undesirable results in subsequent steps of the process. This problem is eliminated by producing photoresist layers which are undercut; that is, the top of the resist protrudes beyond the bottom. Materials deposited on such a layer are thus discontinuous at the resist edge. This process is illustrated by the scanning electron micrographs (Fig. 1 and 2) found in the attached paper by Havemann, Hamilton and Harris.

A further difficulty is with adequate adherence of the resist. So far these difficulties have been successfully eliminated by applying an adhesion promoter to the substrate just before coating it with resist. The promoter is hexamethyldisilazane (HMDS) mixed 1:1 with xylene. A few drops are applied to a substrate and spun off. The resist is then applied immediately.

II.2 Considerations for All Layers

With a large number of films present in a given circuit, it is important that films be continuous over the edges of previously deposited films. This can be assured through the careful shaping of film edges to produce smooth inclines for later films to cover. However, a much more straightforward method is simply to have each film be thicker than all of those deposited before it. This is the approach which we have adopted.

Prior to the deposition of each of layers 3 through 11, the substrate is rf sputter cleaned in argon. The sputtering is done at 25 watts rf power for 3 minutes.

II.3 Substrates

The substrates are silicon wafers which are insulated with SiO_2. These wafers have a 2 in. diameter and 0.010 in. thickness. They are purchased from an outside vendor with the SiO_2 already formed.

II.4 Layer 1 - Niobium Ground Plane

Niobium is deposited onto the ground plane by e-beam evaporation in an ultra-high vacuum system. It is subsequently patterned by selective etching. The parts which are not to be etched are protected by a patterned layer of Shipley AZ-1350J photoresist. The etchant is a mixture of 1 part hydrofluoric acid, 9 parts nitric acid, and 20 parts water, all measured by volume. The etching is done at room temperature and requires about 5 minutes.

II.5 Layer 2 - Nb_2O_5 Ground Plane Insulator

The Nb_2O_5 insulation is formed by anodizing the Nb ground plane. Some areas of the ground plane must remain uninsulated, however, to permit electrical contact to it. One might think of using Shipley 1350 series resist to protect these regions from anodization. However, the anodizing solution is a solvent for this resist. Therefore, the areas of niobium which are to be uninsulated are coated with 1000 Å of aluminum patterned using the lift-off process. The anodization is carried out in a solution (Hickmott and Hiatt, 1970) of 18 g of ammonium pentaborate in 200 ml of ethylene glycol. The thickness of the Nb_2O_5 is approximately proportional to the anodization voltage, the ratio being in the range 22 to 24 Å/volt. Layers of 1000 to 2000 Å thickness have been made. The protective aluminum layer is then removed in 50% H_3PO_4 at 60°C.

II.6 Layers 3, 6, 9, and 11 - SiO

Silicon monoxide is evaporated in a high vacuum system, with a pressure during evaporation of about 1×10^{-6} mm Hg. The material used is a powder which is evaporated from a baffled source designed especially for SiO. Both powder and source are commercially available. The SiO is evaporated at a rate of about 10 Å/s. Junctions are often made through windows, or holes, in layer 6. When junctions are formed more simply by directly overlapping the electrodes layer 6 is omitted.

II.7 $AuIn_2$ Resistors

The material used is $AuIn_2$, an intermetallic which is present in the base electrode of the junction. We have made such resistors consisting of 46 wt. percent Au and 54 wt. percent In. With total film thickness of 2870 Å the resistance was 0.03 ohms per square. Thinning the films to 1435 Å raised the resistivity to 0.1 ohms per square. No difficulties whatsoever have yet been experienced with these resistors. Further thinning of the films should increase the resistivity to a goal of 1 ohm per square. These resistors have shown negligible resistance change with up to 20 thermal cycles and room temperature storage for one month.

II.8 Layer 5 - Pb-In-Au Base Electrode

The base electrode is formed by a sequential evaporation of 500 Å of In, 100 Å of Au, and 3500 Å of Pb. During the baking of photoresist for the next layer, these films intermix to form a homogeneous alloy. The heat treatment is at 70°C for 25 minutes.

II.9 Layer 7 - Tunneling Barrier

The tunneling barrier is formed by oxidizing the base electrode through openings in the photoresist pattern for layer 8 and the SiO of layer 6. The oxidation process is described in two of the attached papers and other references therein. It involves using rf sputtering in oxygen to remove the surface of layer 5. Since the surface continually reoxidizes, an equilibrium between the rate of removal of material and the rate of reoxidation occurs. The equilibrium takes place at a specific oxide thickness essentially independent of the time taken (beyond a few minutes). The oxygen pressure and the cathode self-bias voltage are carefully controlled to produce the desired thickness.

II.10 Layer 8 - Upper Electrode

The upper junction electrode is formed through a sequential deposition of 3000 Å of Pb, 50 Å of Au, and 2000 Å of Pb. This deposition immediately follows the formation of the oxide tunneling barrier (without opening the vacuum system). Homogenization of the alloy is promoted through baking of the photoresist in subsequent steps. In our work we have always provided baking at 70°C for at least 50 minutes, the equivalent of two more layers.

II.11 Layer 10 Pb-In-Au Control Electrodes (incomplete)

It is anticipated that this electrode will be made from the same alloy as the base electrode. However, it will be thicker to provide for good edge coverage over the intervening layers. The presence of indium in this electrode will also promote its connection to other lead layers. If indium were not present, connections to other layers might often be Josephson junctions, rather than the superconducting shorts which are desired.

III. EQUIPMENT DEVELOPED FOR FABRICATION

III.1 Computer Aided Design of Photomasks

Photomask patterns are made at ten times final dimensions using a Gyrex 1001-4 digitally controlled pattern generator at the NBS Boulder Laboratories. This machine exposes rectangles on a photographic plate. The position and size of the rectangles are digitally controlled. As part of this contract we have developed computer programs to aid in the use of this machine.

The input to the machine is provided on punched paper tapes containing code in a language analogous to machine language for a minicomputer. The first program we have developed provides an English-like language for specifying the location and size of the rectangles to be exposed. It also provides the ability to define subpatterns and to repeat them at arbitrary locations with variable size and rotation. The output of the program is the machine language code which can be interpreted directly by the pattern generator.

The second program enables the computer to read the machine code and plot the rectangles on a cathode ray tube terminal. Thus, the person coding a pattern can quickly see errors and correct them.

III.2 Combined Sputtering and Evaporation System

A combined sputtering and evaporation system has been assembled for depositing resistors and lead alloys. The system has a number of special features which are important for fabricating superconducting integrated circuits.

III.2.1 Sputtering System: A commercially available rf sputtering system was modified so that it could be used to form the oxide tunneling barrier. The modifications included reducing the capacity of the rf power supply in order to increase its controllability at low power levels, and changing the rf power sensor and cathode self-bias meter to obtain greater accuracy at low levels.

III.2.2 Pressure Control System: A commercially available system is used to control the pressure during sputtering oxidation. This control is important because the oxide thickness is a sensitive function of oxygen pressure. The system can achieve pressure control of about $\pm$0.005 microns at the 10 micron level. Routinely, it achieves $\pm$0.02 microns.

III.2.3 Moving Sources: Since the alloys are evaporated sequentially, it is important that each component be evaporated from the same point. Otherwise, shadowing at the edges of undercut resist layers might lead to different chemical composition at the edges of the films. The evaporation filaments are therefore on a movable carriage. The position is controlled through a rotary vacuum feedthrough.

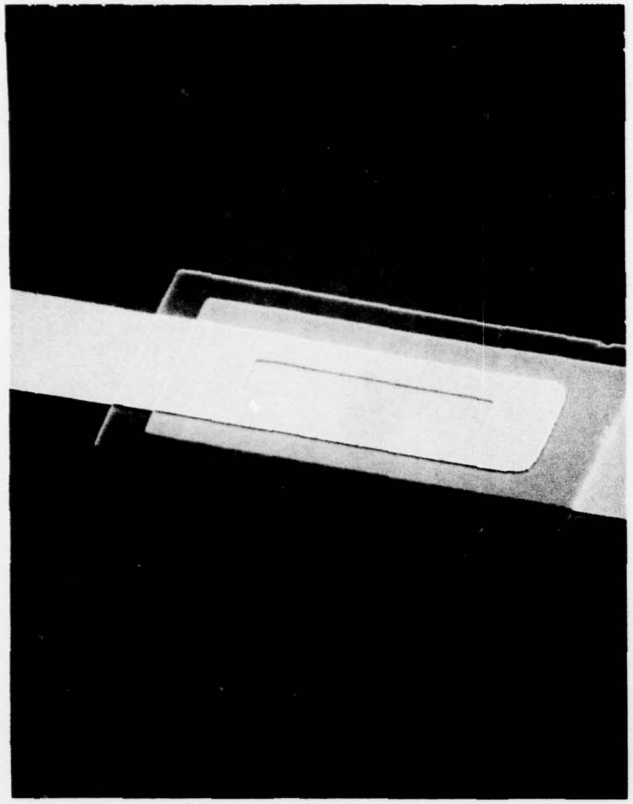
III.2.4 Film Thickness Monitor and Shutter Control: A commercial quartz crystal film thickness monitor is used to determine the film thickness on the substrate. The monitor can be programmed to operate a shutter when the film thickness reaches a predetermined value. Since the monitor has a one second response time, exceedingly fast evaporations lead to substantial thickness errors. Because rapid evaporations are important in achieving high density indium films, it is anticipated that the monitor will be replaced by a faster one. At that time the evaporation part of this system may be totally automated to eliminate human error during the many steps in depositing these alloy films.

IV. FUTURE FABRICATION IMPROVEMENTS

Further effort is required to improve the process for making Josephson junctions. Present yield is variable. During some periods, it is nearly 100%, but at other times, it is close to zero, even though there is no apparent difference in the process. Some improvement in this situation is obtained by using junctions made through SiO windows (See Fig. 2). Also a correlation has been noted between the use of new masks and good yield. As a result we are beginning to use hard surface masks, rather than photographic ones, so that they may be cleaned between uses. While this problem with yield does not prevent us from beginning to work on complete circuits, it does need a solution. Otherwise detailed design work in the future will not proceed efficiently because of the difficulty of making Josephson junctions whose properties closely match design values.

Possibly related to these difficulties in fabricating Josephson junctions is our lack of success during a brief attempt at making junctions having thinner electrodes. Such junctions should exhibit increased resistance to degradation during thermal cycling. Furthermore layers placed on top of them could also be thinner and still have adequate edge coverage. Further efforts with thinner junction electrodes are anticipated.

Several other minor improvements in the processes may be possible. First, the use of an aluminum protective layer during ground plane anodization is time consuming. It could possibly be replaced with a type of resist which does not dissolve in the anodizing solution. The resistivity of the resistors is not yet conveniently high. Efforts will be made to decrease their thickness to solve this problem. Finally, control lines have not yet been fabricated. No significant difficulties are anticipated with them, except possibly ones related to edge coverage. Solution of the above problems will allow full attention to be devoted to circuit design and testing.



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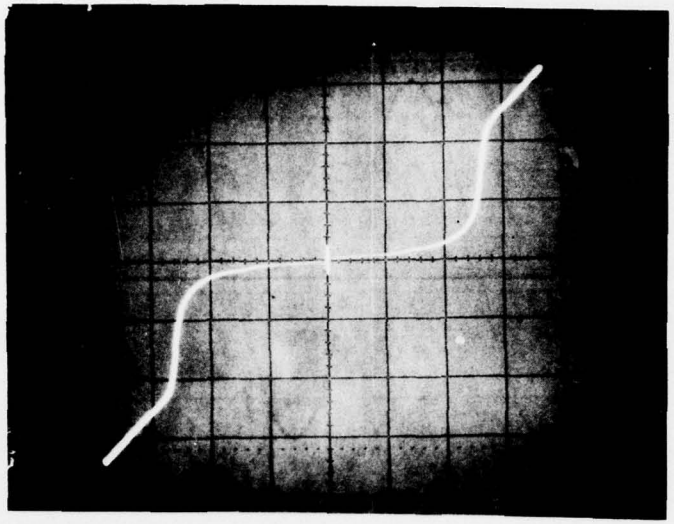


(b)

Figure 2

(a) Silicon monoxide window for a tunnel junction. The SiO layer prevents tunneling at the edges of either electrode. This type of junction has exhibited the lowest excess current we have observed.
(b) I-V curve for an SiO windowed junction. The excess current below 1 mV is about the amount predicted for thermally excited quasiparticle tunneling on the basis of the BCS theory.

V. CIRCUIT CHARACTERIZATION

V.1 Storage and Cycle Testing

Two important requirements for Josephson integrated circuits are (1) the ability to remain unchanged during extended storage periods and (2) the ability to withstand a number of cycles between room temperature and 4 K. We have fabricated a large number of test junctions specifically to test these properties. Cycle testing was facilitated by using the device described in the attached paper, "Automatic 300-4 K Temperature Cycling Apparatus." The results of these tests on ten different junctions are plotted in Fig. 3. The curve shows normalized junction resistance at 4 K as a function of the number of thermal cycles. In all cases, the junctions remained essentially unchanged up to about 10 thermal cycles and degraded rather rapidly thereafter. The number of cycles survived was roughly inversely proportional to junction area suggesting that random hillock growth is the destructive mechanism.

Periodic resistance measurements were also made on junctions stored at room temperature and at -15°C (in the freezer compartment of an ordinary refrigerator). The results are shown in Fig. 4. In general, the devices stored at room temperature showed large and erratic resistance changes while those stored at -15°C remained virtually unchanged over the duration of the test period (3 months).

V.2 Gain Curve Measurement

One of the most important parameters of a Josephson switching device is its critical current as a function applied magnetic field. This is often called the gain or diffraction curve. This curve must be measured by sweeping through the I-V curve at each value of magnetic field and recording the maximum value of the supercurrent (critical current). An instrument has been designed to perform the sweep operation and to automatically sample the bias current at the instant of switching thus providing a direct measure of the critical current. Using the instrument, gain curves can be traced out automatically on an X-Y recorder. A block diagram for the setup is shown in Fig. 5. The junction I-V curve is swept at about 20 Hz and displayed on a scope. At the instant that the junction switches to the voltage state, the current is sampled and stored. When the sample current is plotted vs. a slowly varying applied field, the gain is traced out. A circuit diagram for

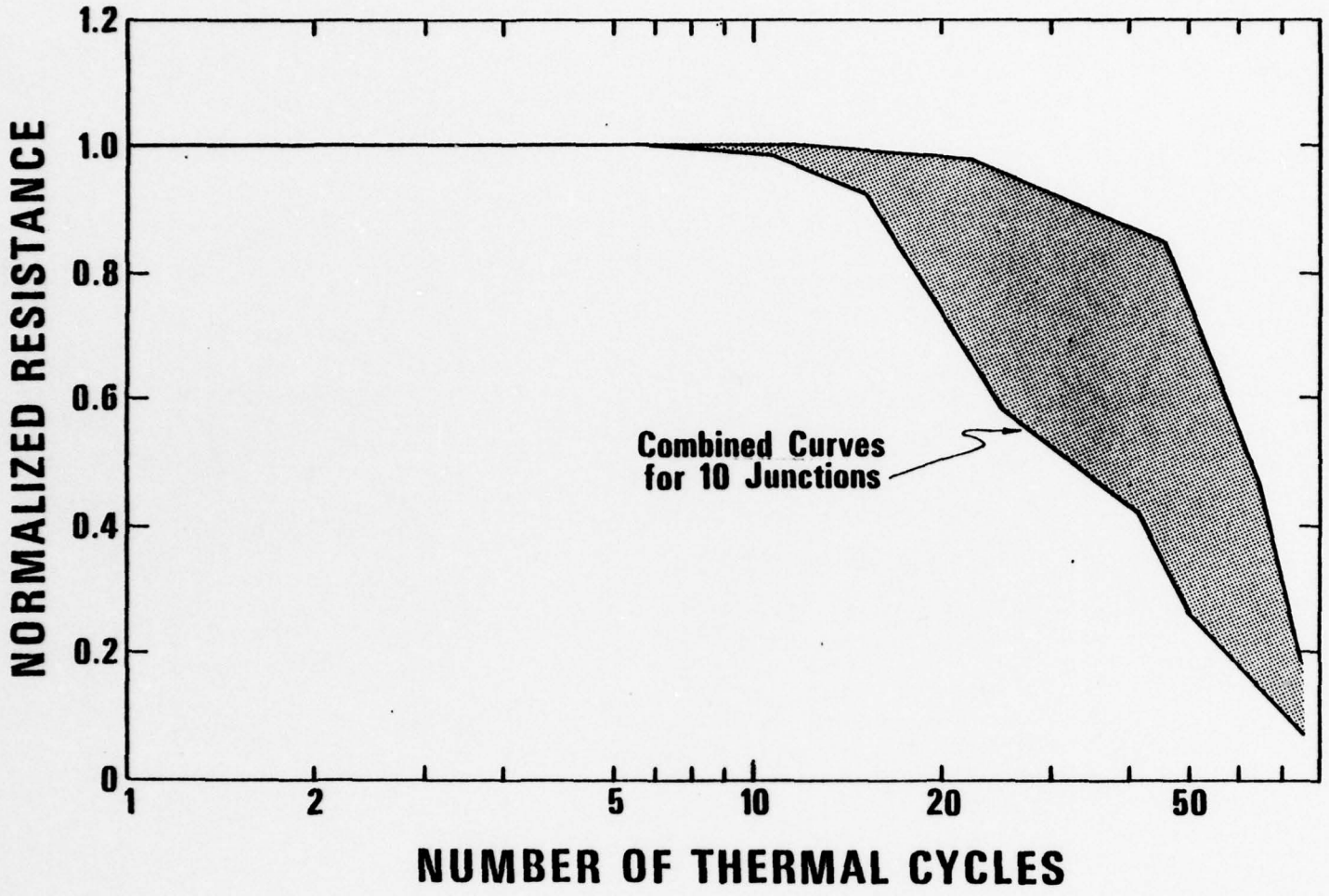


Figure 3

Normalized resistance as a function of number of thermal cycles. The resistance provides a good measure of the stability of the junction.

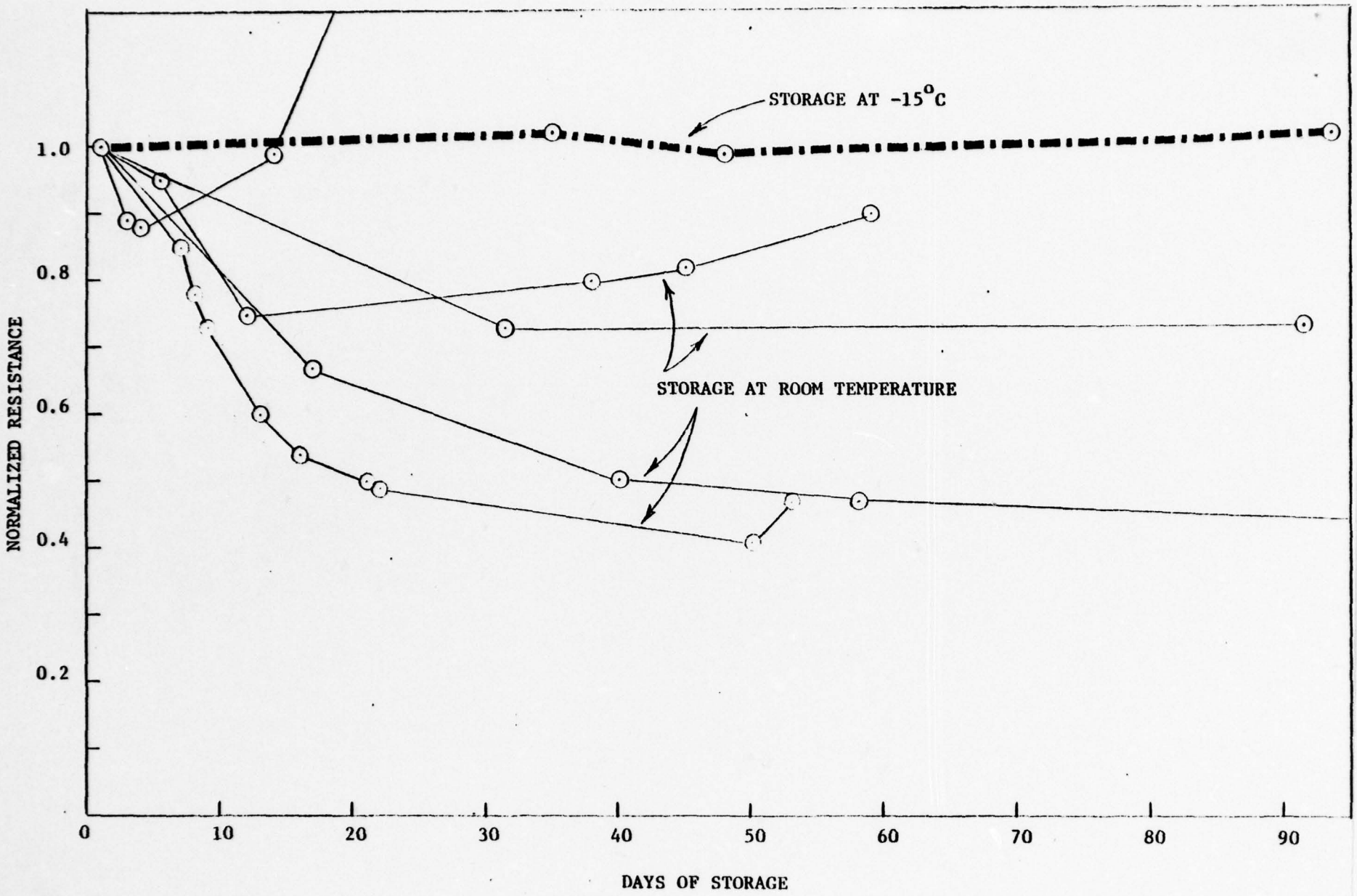


Figure 4

Normalized resistance as a function of storage time. Storage at -15 °C is seen to result in little or no change.

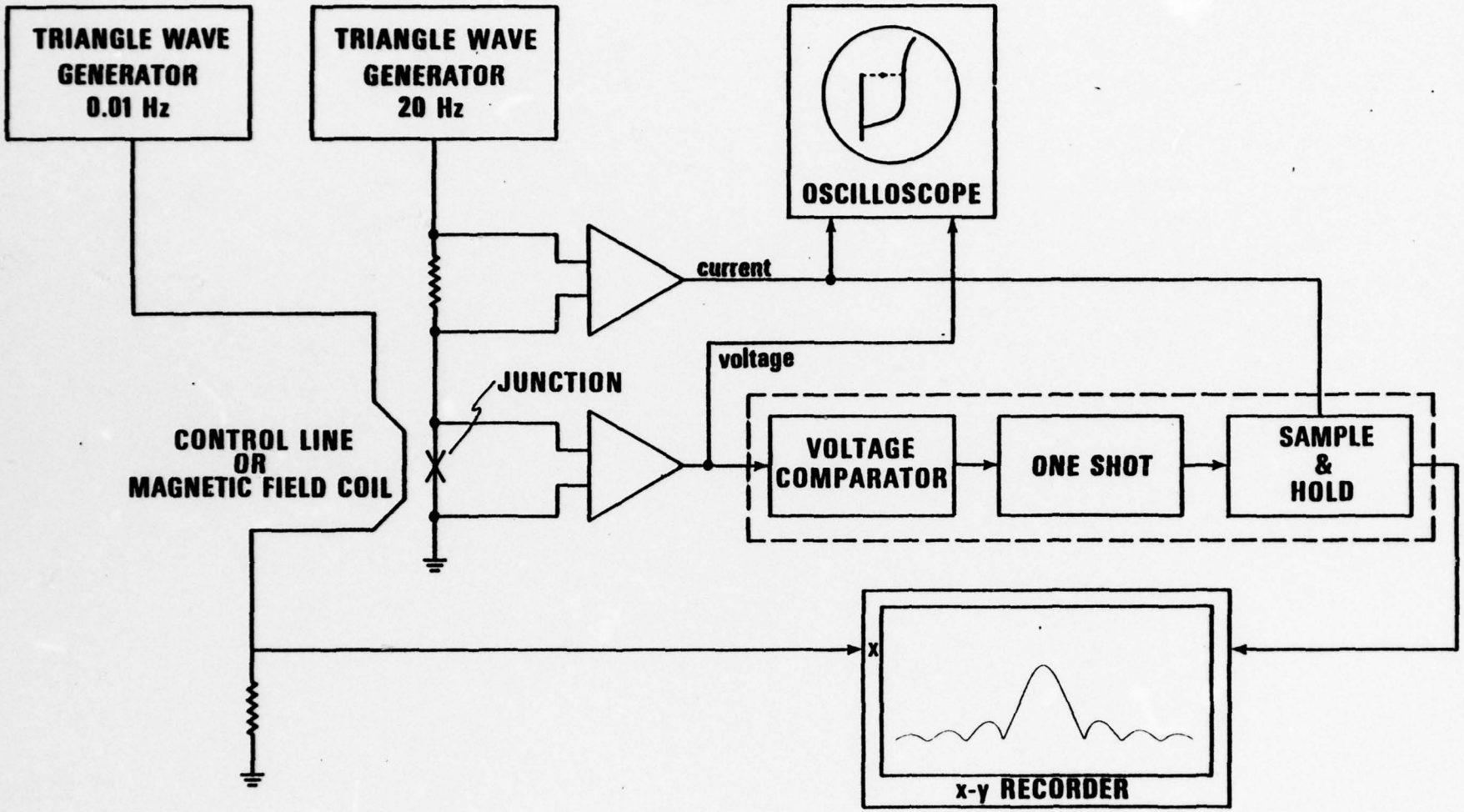


Figure 5

Block diagram of the instrument for gain curve measurement. See the text for description of operation.

the elements in the dashed box is shown in Fig. 6. Fig. 7 is an actual curve produced with this set up. Since the junction used for Fig. 7 is short relative to λ_j (the Josephson penetration depth), the curve has the familiar (sin X)/X shape.

In "long" junctions or multi-junction interferometers which are fabricated over a ground plane, the field produced by the lead current is a significant part of the total field. The result is a skewed gain curve wich can be tailored to achieve a gain substantially greater than one--a requirement for junctions used in multilevel logic circuits.

V.3 High Frequency Chip Mount

In order to take advantage of the high speed of Josephson integrated circuits it is necessary to have a chip mount capable of transmitting signals to and from the chip with very broad bandwidth. Conventional wire bonded integrated circuit headers are unsuitable because the inductance of the bonded wires severely limits bandwidth. The Kovar leads used in almost every IC header available are also unsuitable because they are magnetic. For these reasons we have fabricated chip mounts specifically designed to obtain broad bandwidth on a large number of leads. A cross section of the mount is shown in Fig. 8. A photograph of the assembled and disassembled mount is shown in Fig. 9. The mount makes 24 pressure contacts to a 6 x 6 mm chip. The chip is accurately aligned and pressed against 24 gold plated copper tabs which contact 24 pads on the chip. The copper tabs are the ends of 50 Ω striplines etched on a standard 0.4 mm pc board. The last 0.5 mm of each stripline tab is peeled from the pc board in order to achieve a small amount of individual spring pressure on each contact. The other end of each stripline is connected to 50 Ω, RG-83 coax cables which bring the signals out to room temperature. Since microstriplines on the chip have impedances on the order of 1 Ω, it is desirable to fabricate impedance matching networks on the chip.

The performance of the chip mount was tested using a chip with a single long (6 cm) microstripline shorted at one end. A schematic diagram of the experiment is shown in Fig. 10a. A very fast (< 30 ps) voltage step is produced by the tunnel diode generator and transmitted onto the chip. Because of the large impedance mismatch at the input to

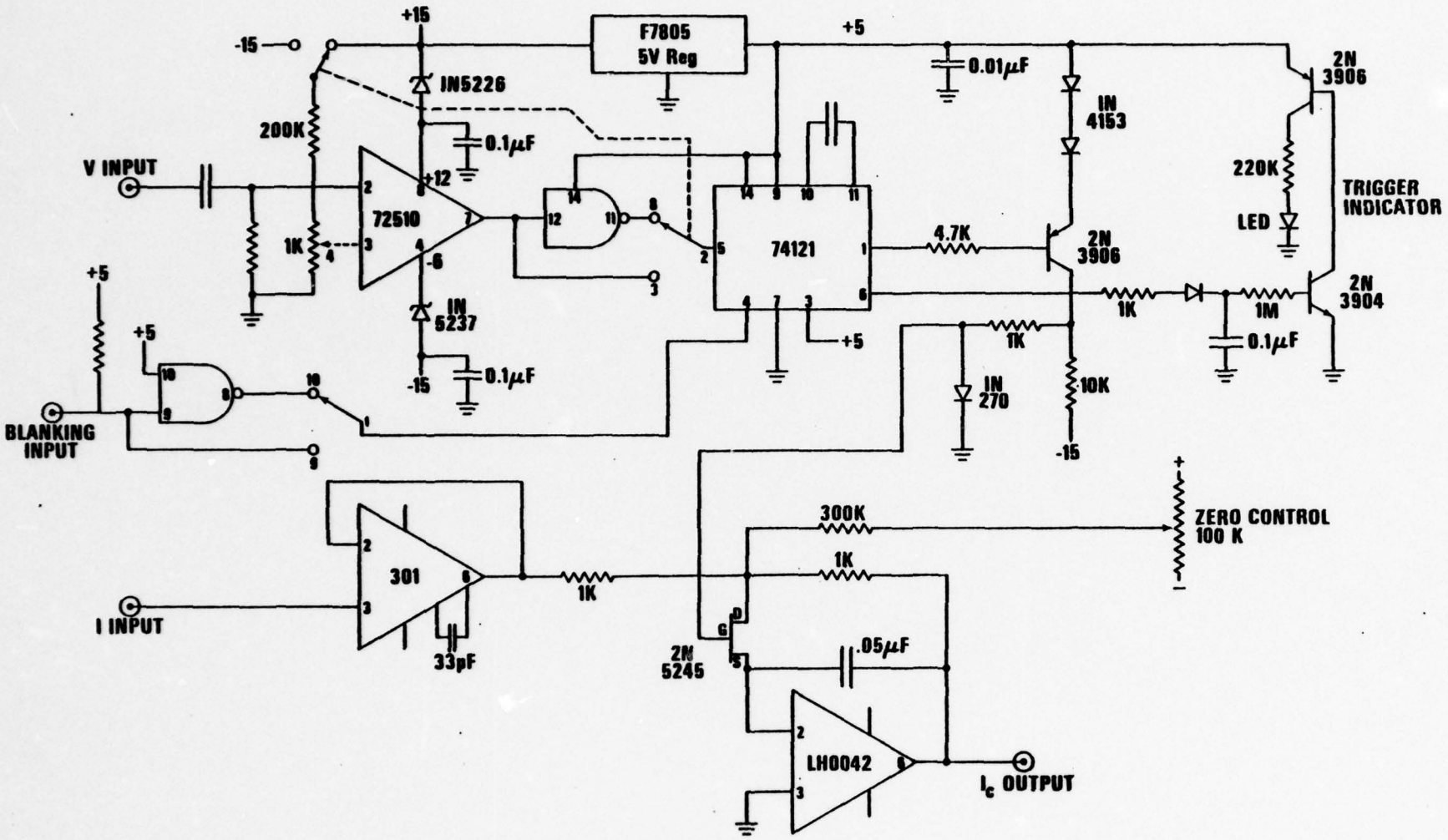


Figure 6

Circuit diagram for the components within the dashed box of Figure 5.

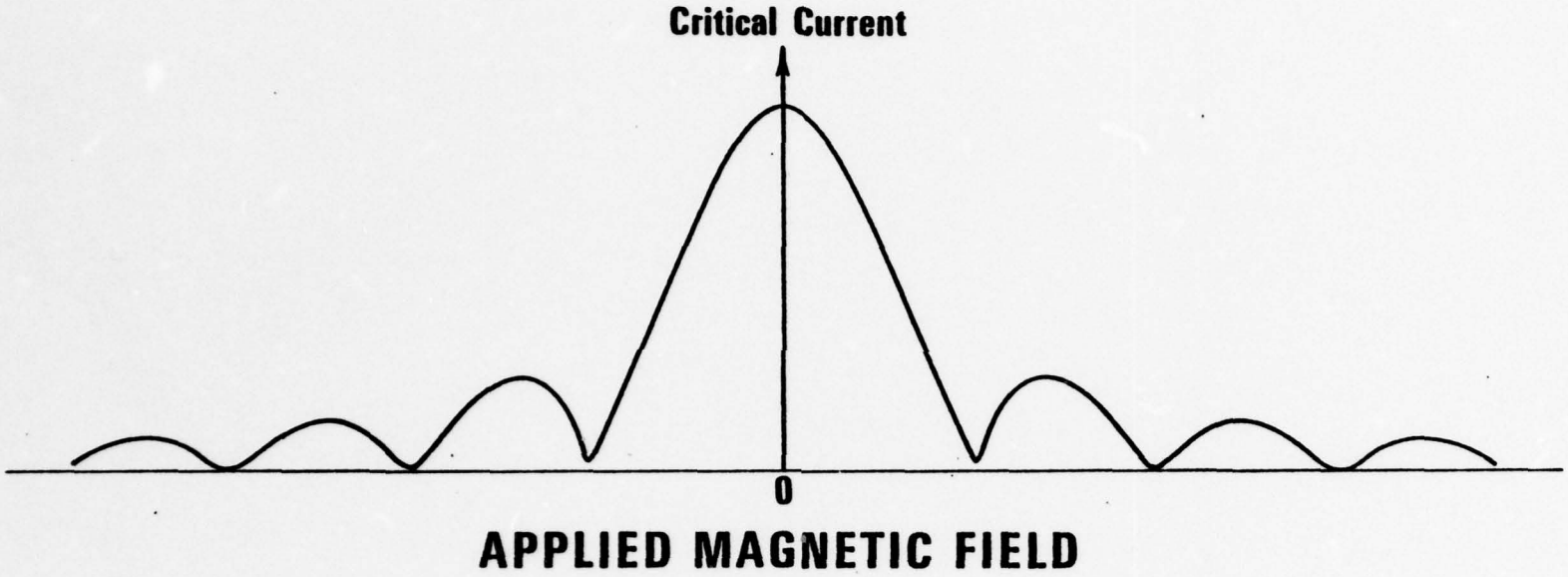


Figure 7

Gain curve for a 'short' junction (short relative to λ_J).

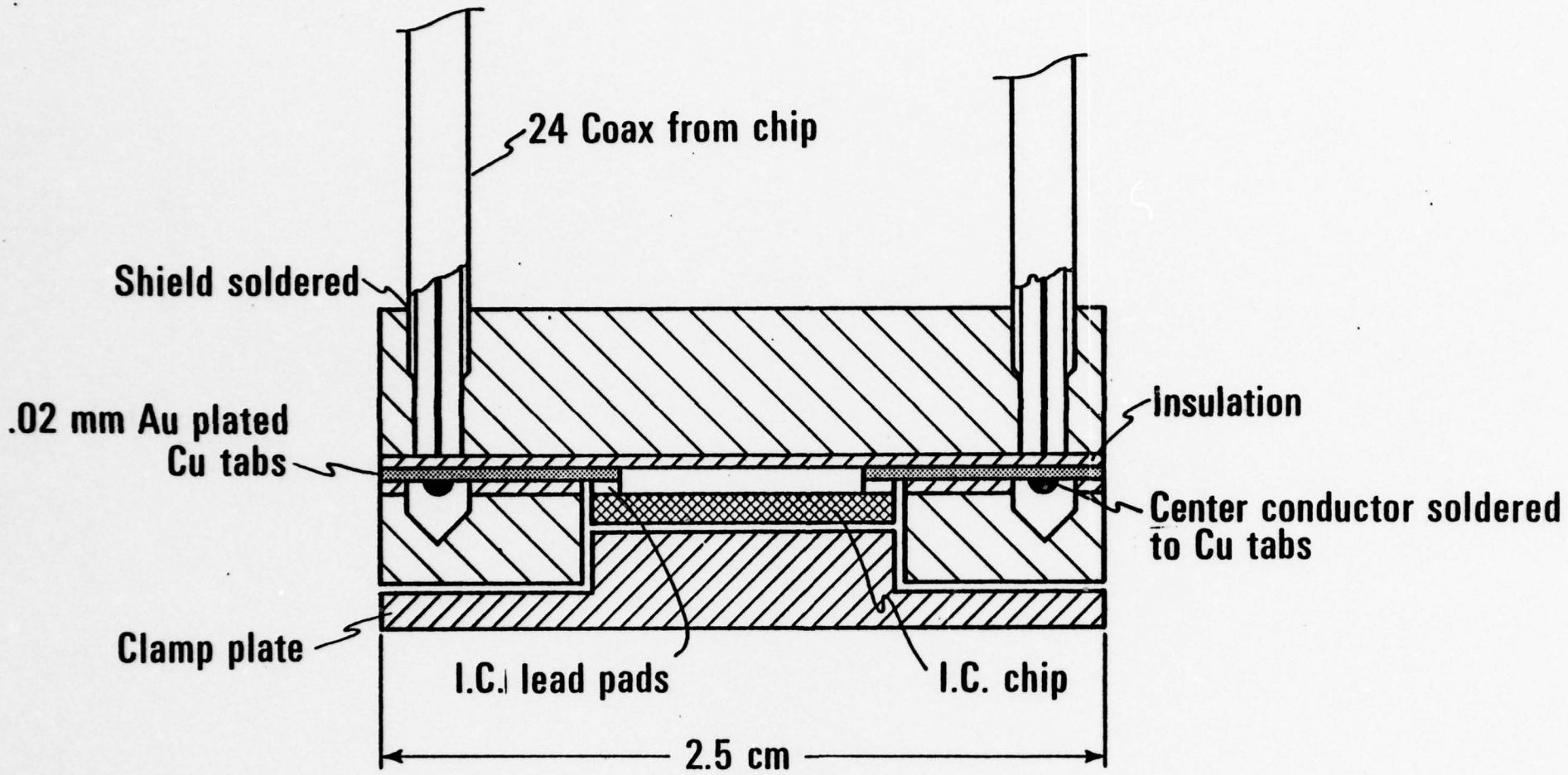


Figure 8

Cross section of the high frequency chip mount. The transitions from coaxial lines to the chip are striplines on a standard pc board.

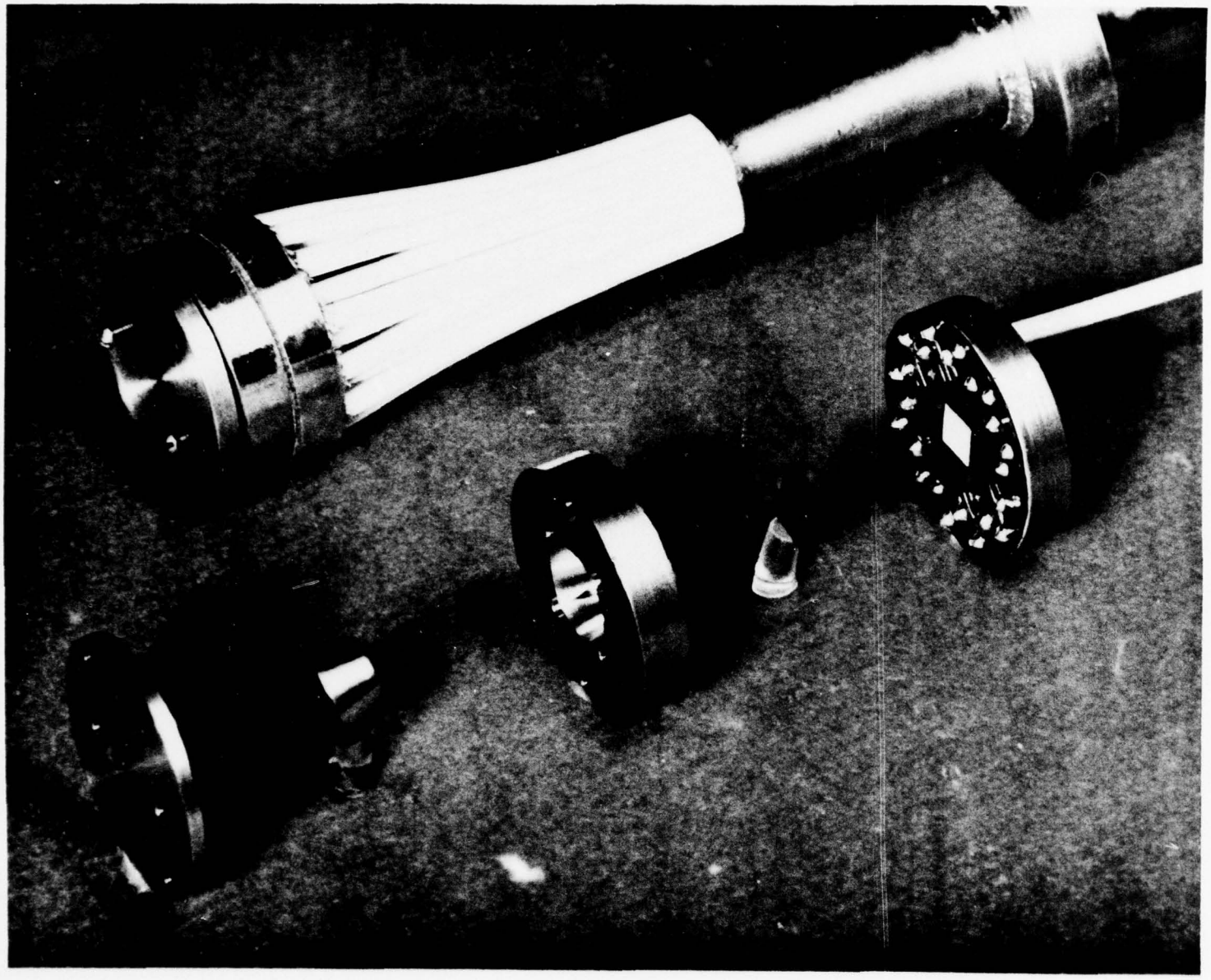
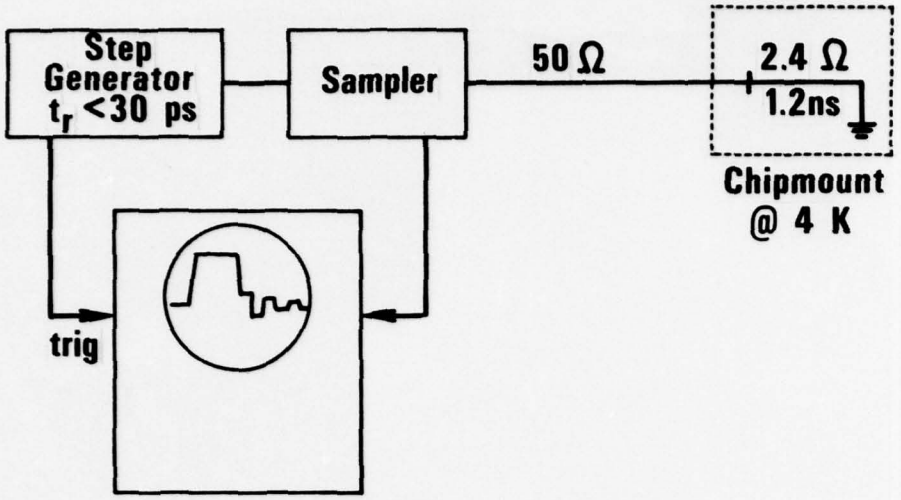


Figure 9

Photo of the high frequency chip mount. The upper portion shows the assembled device. The disassembled mount is shown below.



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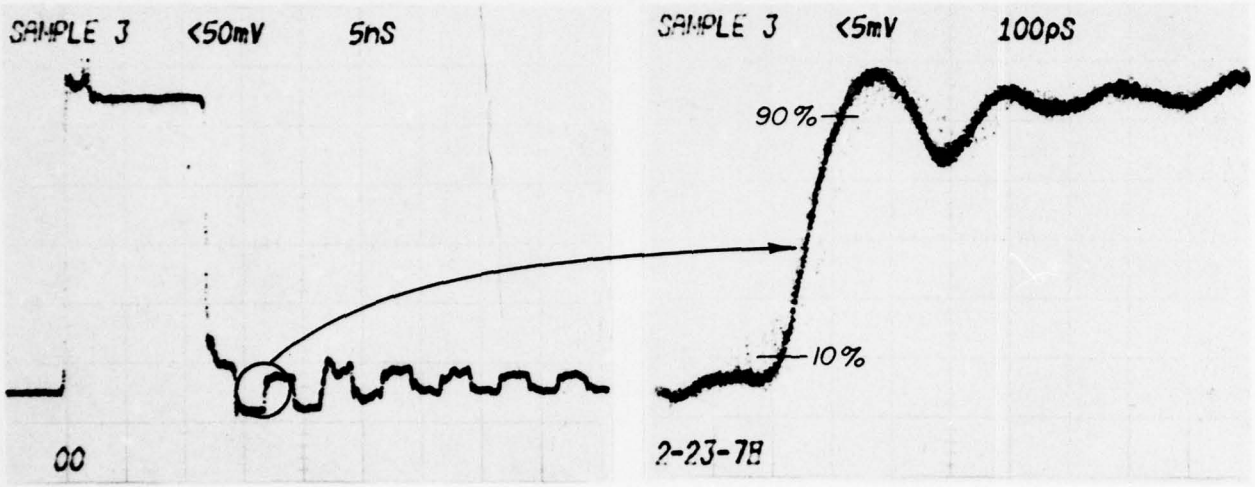


(b)

Figure 10

(a) Schematic diagram of the test of the high frequency chip mount.

(b) Typical test data for the mount evaluation.

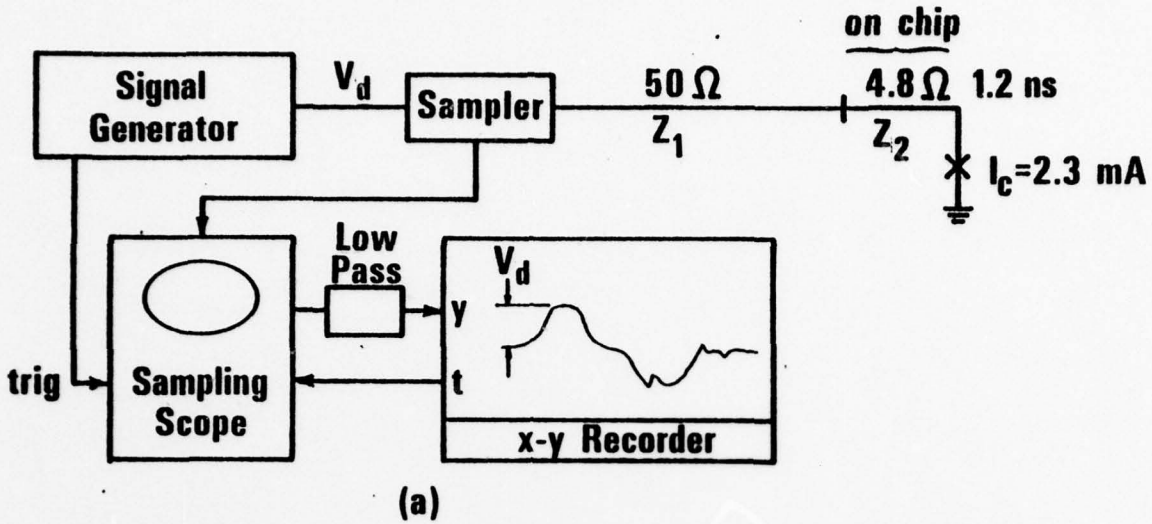
the microstripline, the signal on the chip undergoes multiple reflections. The rise time of the signal transmitted to the 50 Ω line at each of the reflections is a measure of the rise time achievable with the chip mount. The amplitude of these signals can also be used to determine the impedance of the superconducting microstripline (see section VI). Typical data shown in Fig. 10 b indicate a rise time of about 100 ps. Since this is for a signal transmitted onto the chip and back off again, the actual contact rise time is about $100/\sqrt{2}$ = 70 ps. This corresponds to a bandwidth of 5 GHz.

A second version of this chip mount has been made in which the brass chip holder can be unplugged from the 24 coax cables. These devices are very convenient for storing mounted chips and making simple room temperature measurements. The extra connector in each line increases the rise time to about 140 ps.

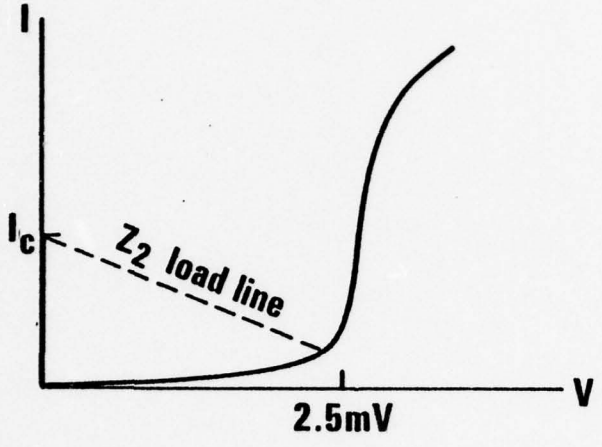
With a relatively high speed mount available it is possible to consider measurements of junction switching time. A simple way of doing this is to attach a junction to the end of a long microstripline. The delay in the long line separates reflections in time so that it is not necessary to fabricate an impedance matching network at the chip edge. A slow-rise-time pulse launched into the microstripline will cause the junction to switch producing a fast transition on the returning signal. Since the amplitude of this fast transition is only a few millivolts it is necessary to do signal averaging on the sampling scope output. A block diagram of the experiment is shown in Fig. 11a. The signal averaging is accomplished by using a y vs. t recorder to control the sampling time base and feeding the sampler output through a low pass filter to the recorder y axis.

There are two design considerations in this very simple circuit. First, as shown in Fig. 11b, the junction will switch along a load line defined by the characteristic impedance (Z_2) of the microstrip line. Thus, the junction critical current must be greater than V_{gap}/Z_2. If this is not the case, the junction will not switch to the full gap voltage. The second requirement is that the drive voltage be large enough to switch the junction. Taking into account the reflection at the chip mount, the required voltage is

$$V_d > I_c Z_2 \left\{ \frac{2Z_2}{Z_1+Z_2} \right\}$$



(a)



(b)

Figure 11

(a) Schematic diagram of junction switching experiment.

(b) Load line for switching. This load line is defined by the characteristic impedance (Z_2) of the microstripline.

Finally we should note that the amplitude of the observed transition should be

$$V_s \left\{ \frac{2Z_1}{Z_1+Z_2} \right\}$$

The amplifying factor is also a result of the impedance mismatch at the chip mount.

Fig. 1 is a photograph of a corner of the chip used in this experiment. The two striplines (8) are 25 μ wide and are terminated in junctions which are shorted to the ground plane in the lower left corner. The actual parameters used were Z_2 = 4.8 Ω, I_c = 2.3 mA. Figure 12 shows the data obtained. The first pulse is produced by the signal generator and has a rise time of 5 ns. The reflected pulse has the junction transition riding on it. The observed rise time is 70 ps. Since we expect a junction of this current density (300 A/cm^2) to have a rise time on the order of 10 ps, the experiment simply confirms the known rise time of the chip mount. The observed amplitude is somewhat less than expected. This is a result of low frequency dispersion caused by skin effect losses in the cable leading to the chip mount. From this data it is clear that meaningful measurements of junction switching times will require on-chip techniques.

VI. SUPERCONDUCTING STRIPLINES

Accurate characterization of the superconducting striplines which interconnect active devices on a microcircuit is essential to the construction of high-speed Josephson-junction logic. In particular, the stripline propagation velocity is required in estimating the time delay of a logic stage and the stripline impedance must be matched to device impedances in order to minimize signal reflections. Characterization of striplines has proceeded along both theoretical and experimental lines.

In a theoretical study, the BCS theory of superconductivity was used to calculate attenuation and dispersion of striplines at high frequencies. This study shows that superconducting striplines are nearly ideal at frequencies below the superconducting energy-gap frequency but have high attenuation and dispersion about the gap frequency.

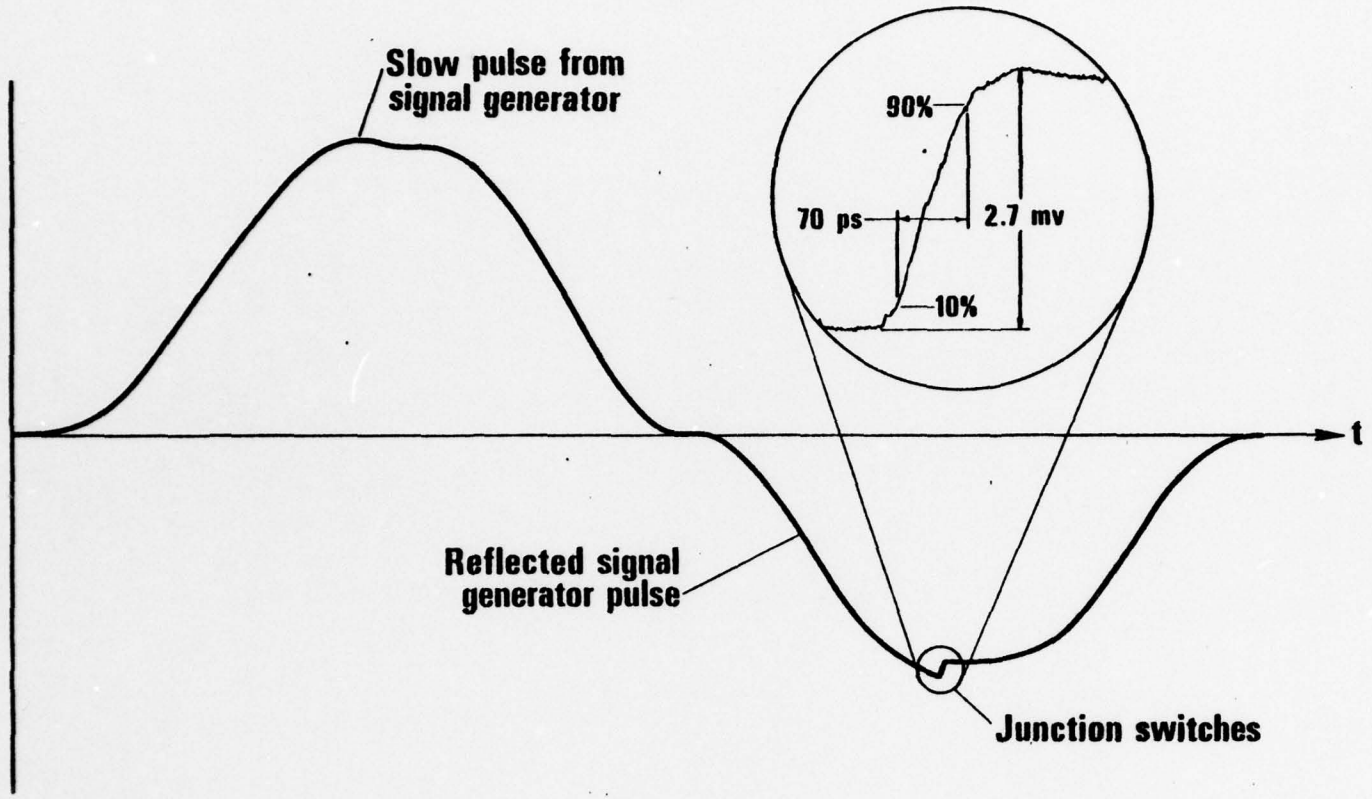


Figure 12

Results of junction switching experiment. The junction transition (inside the circle) rides on the reflected pulse.

For Pb striplines this departure from ideal behavior at high frequencies means that it will be difficult to transmit pulses shorter than about a picosecond across a microcircuit. A detailed account of this study entitled "Picosecond Pulses on Superconducting Striplines" appeared in the January 1978 issue of the Journal of Applied Physics and a copy is included in this report.

Experimental study has centered on the stripline circuit shown in Fig. 13. The circuit consists of a Nb groundplane, a layer of anodic Nb_2O_5 and two 50 μm wide, 70 cm long strips of Pb-Au alloy which meander back and forth over the oxide. The properties of such striplines were studied using the circuit of Fig. 14 in which the stripline, located in a dewar, is connected to a signal generator and an oscilloscope via 50 Ω coaxial lines. Two basic experiments can be performed using this circuit configuration, a time-domain reflectometer (TDR) experiment and a resonant cavity experiment.

In the TDR experiment the signal generator produces a step function and the voltage V_I is monitored as a function of time. A typical TDR trace is shown in Fig. 15. The step produced by the voltage generator appears here as a sudden increase in V_I from 0 to 250 mV. About 15 nS after this rise V_I falls to about 10 mV. The fall in V_I is due to the arrival of a reflection from the discontinuity in impedance between the 50 Ω coax and the stripline. The magnitude of the voltage reflected from the discontinuity in impedance allows one to calculate the characteristic impedance of the stripline, in this case about 1 Ω. The staircase rise in voltage appearing after the initial fall results as the signal bounces back and forth between the ends of the stripline, and the 36 nS interval between the arrival of steps is the time required to traverse the 70 cm stripline. Thus the propagation velocity of the stripline is 3.9×10^7 m/s. In general, TDR allows one to measure the characteristic impedance to better than an ohm and the propagation velocity to within a few percent.

In the resonance experiment the voltage generator is a frequency sweep oscillator and an oscilloscope is used to monitor V_o. Because of the discontinuities in impedance between the stripline and the 50 Ω coax at each end, the stripline acts as a resonant cavity and the voltage V_o reaches a maximum whenever the frequency of V_G hits a cavity resonance.

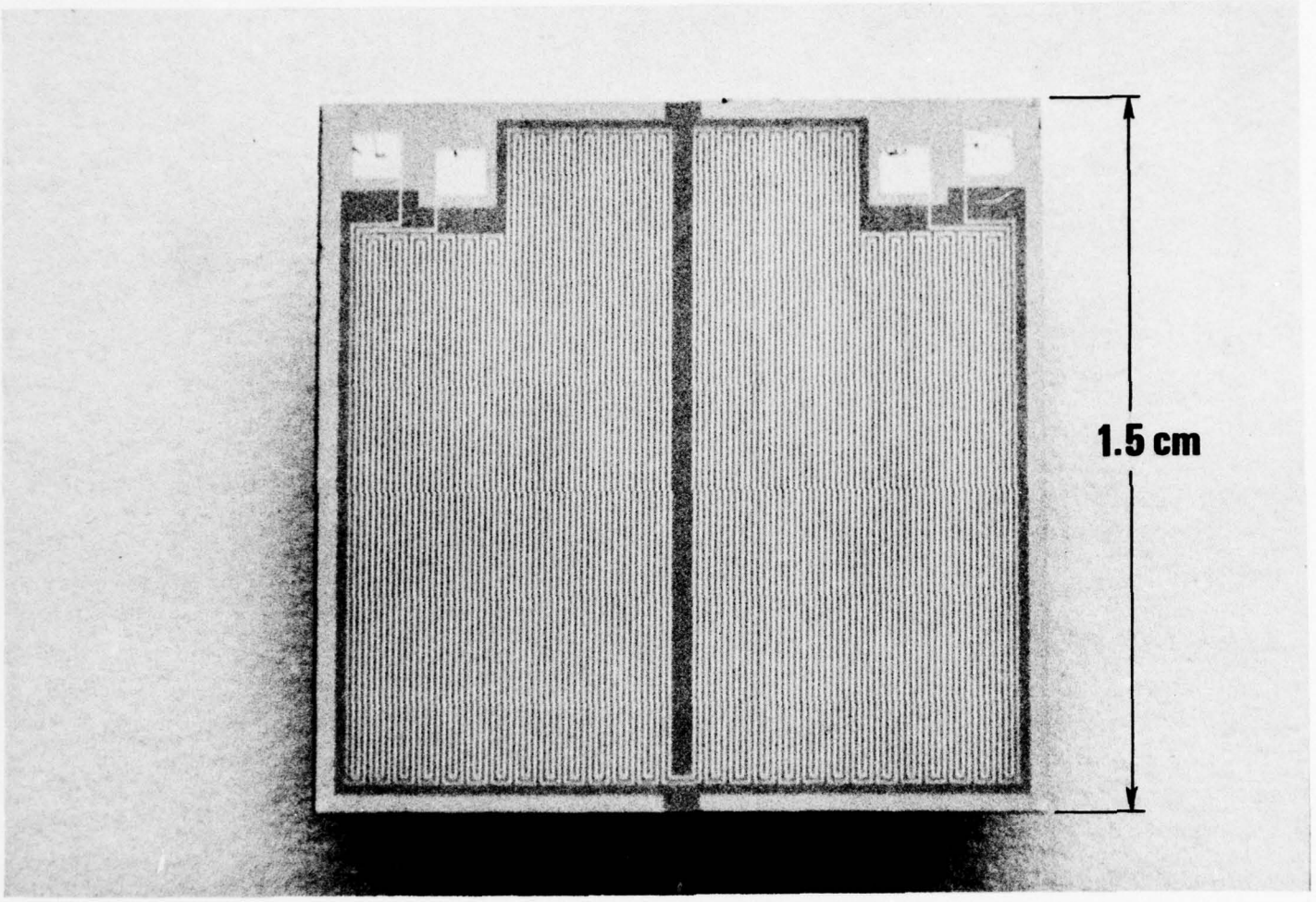


Figure 13

Superconducting striplines. The chip has two parallel striplines which are each 50 μm wide and 70 cm long.

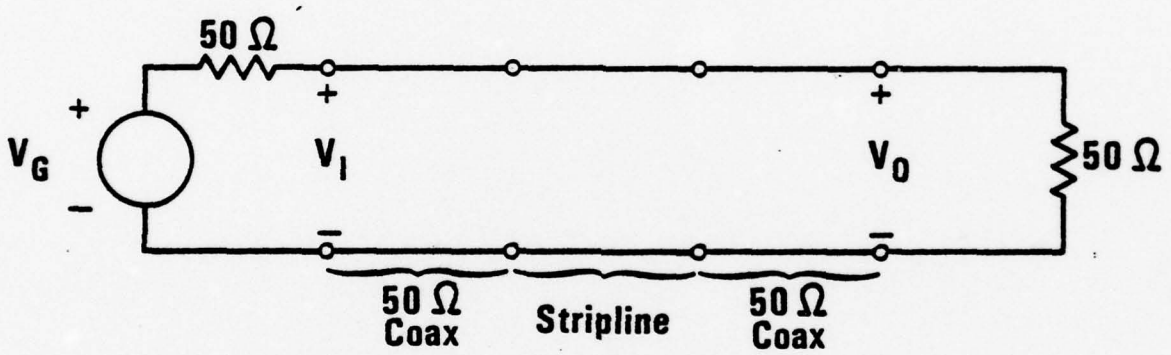


Figure 14

Circuit for study of superconducting striplines.

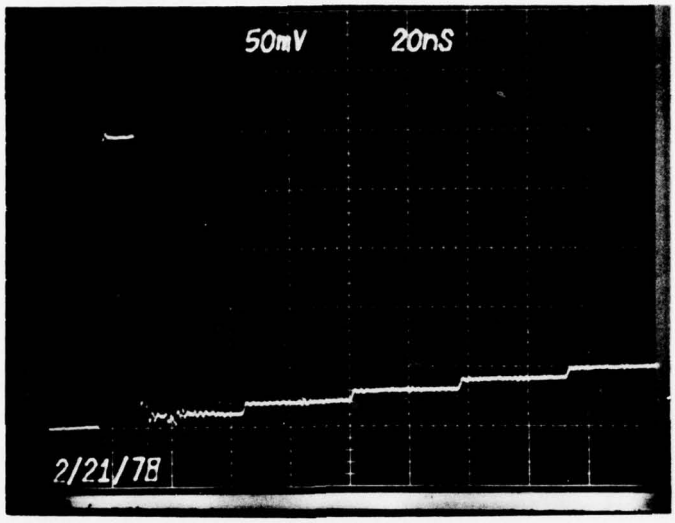


Figure 15

Time-domain reflectometer experiment. The steps result from reflections from the discontinuities in impedance between the 50 Ω coax and the stripline.

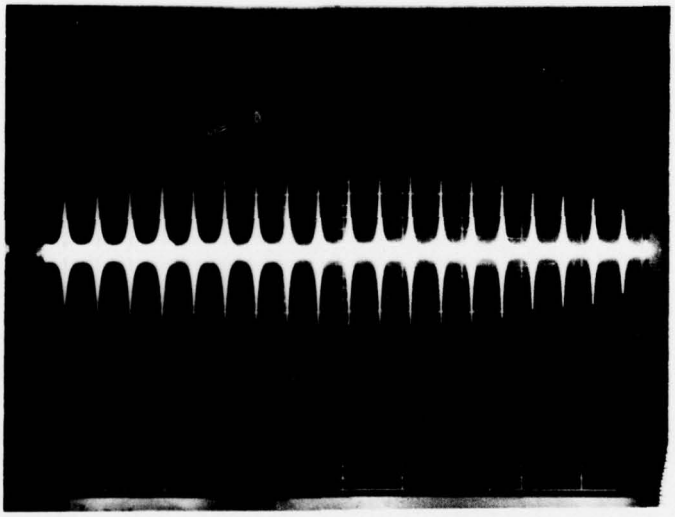


Figure 16

Resonant cavity experiment. Here the stripline acts as a resonant cavity. The horizontal axis is proportional to the exciting frequency. Resonance occurs when an integer multiple of the wavelength of radiation on the stripline equals twice the length of the line.

The condition for resonance is simply that an integer multiple of the wavelength of radiation on the stripline equal twice the length of the stripline. Fig. 16 shows an oscilloscope trace of V_o as a function of the frequency of V_G. The spikes mark the frequency at which the resonance condition is met. Measurement of the resonant frequency and stripline length yield the propagation velocity to one part in a thousand.

While it is not necessary to know the propagation velocity to such high accuracy to design logic circuits, this information is of scientific interest in that it provides perhaps the only direct measurement of the penetration depth of a superconductor. For a stripline in which the strip and groundplane are of the same material, the propagation velocity is given by

$$v = c\sqrt{\frac{s/\varepsilon}{s + 2\lambda}}$$

where c is the velocity of light in free space, s is the dielectric thickness, ε is the relative dielectric constant, and λ is the penetration depth. Because s/ε can be determined by a capacitance measurement and v is known from the resonance experiment, the quantity $s + 2\lambda$ can be obtained to high accuracy. Thus, only an accurate measurement of s is required to determine λ, a fundamental superconducting parameter. It is hoped that such measurements will be an important by-product of stripline analysis.

Finally, the resonance experiment has been used to measure the attenuation of superconducting striplines. Information about losses is contained in the width of the resonance spikes shown in Fig. 16 and this information has been used to generate the attenuation data shown in Fig. 17. At 4 K it is seen that the attenuation is proportional to frequency. The way in which the 4 K losses scale with dielectric thickness indicates that they are dielectric rather than superconductor losses. Uncorrelated hopping conduction, previously observed in anodic Nb_2O_5 at room temperature (Fuschillo, Lalevic, and Annamalai, 1976), would explain an attenuation proportional to frequency. At 6.7 K the attenuation above 400 MHz is proportional to frequency squared, as expected for superconducting losses.

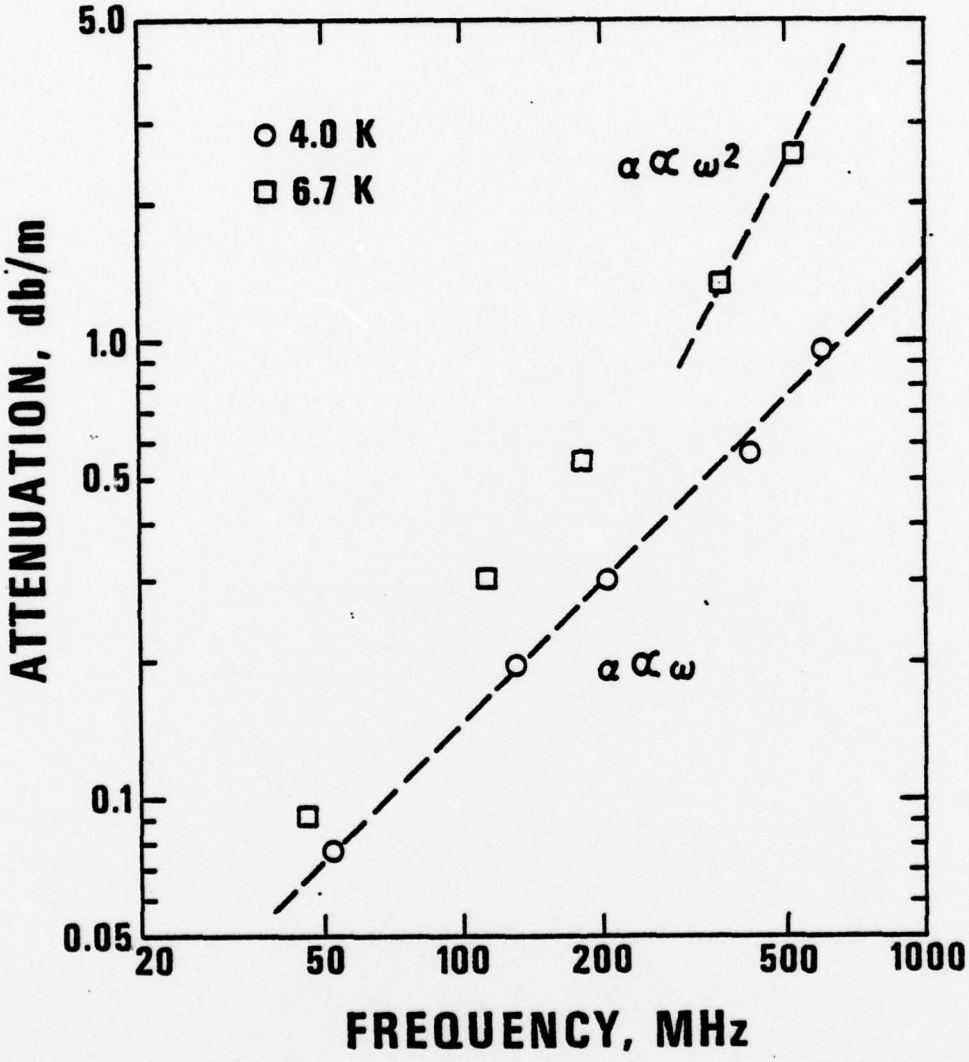


Figure 17

Attenuation of a superconducting stripline as a function of frequency. This data is generated from the width of the resonances shown in Figure 16.

Measurements of stripline impedance and propagation velocity are in quantitative agreement with theory. We further believe that the attenuation measurements can now be modelled semi-quantitatively by theory. Thus, it is now possible to construct striplines with the predetermined characteristics necessary for a given logic circuit.

VIII. CIRCUIT MODELLING

Computer software packages for the analysis and design of large electrical circuits have been available for many years, and widely used in semiconductor technology. The packages are specifically designed to incorporate models of semiconducting devices, and are of varying degrees of sophistication.

We have investigated about twenty of these software packages for their applicability to large electrical circuits containing superconducting elements especially Josephson junctions. This investigation has consisted of studying the literature, consulting with people familiar with such programs, and experimenting with various programs made available to us at universities and commercially (the latter via remote batch methods).

Only one such program (SCEPTRE, and its variants) has been found to be powerful enough to handle Josephson junctions directly, without a modelling of the junction itself by means of an equivalent circuit. IBM's ASTAP program can also handle Josephson junctions, but they must be modelled. Further, we would have had to pay a monthly charge to IBM in excess of $1300, whereas SCEPTRE is free to us.

We originally attempted to obtain SCEPTRE from the Kirtland Air Force Base Weapons Laboratory (AFWL), the listed supplier of SCEPTRE. Unfortunately for us, Kirtland has in the past year or two reassigned its military people responsible for SCEPTRE. This resulted in long delays in sending us the SCEPTRE tapes, then sending us the wrong tapes, and finally sending a version of Extended SCEPTRE which has bugs in it. We, together with our computer systems people, identified and eliminated two such errors, and verified that the modified version worked for simple circuits. However, we had little confidence in this particular package and decided not to use it.

Subsequently, we located a supporter of SCEPTRE (Picatinny Arsenal). They sent us the tapes for SUPER*SCEPTRE, which is now installed and working on our system (CDC 6600). This version presumably is correct, having been sent to some 50 other groups without serious complaint, according to Picatinny. We have compared this version of SUPER*SCEPTRE with alternative direct calculational techniques, on several simple circuits, and are satisfied with its accuracy. We have found the people with whom we have dealt at Picatinny to be knowledgeable and cooperative.

The version of SUPER*SCEPTRE sent us had limited plotting options. We have modified the program so as to produce a file containing all computed points, which we then use in our own plotting package. This package makes use of DISSPLA, a powerful commercial plotting program also installed on the CDC 6600. Plots are being made on our new Tektronics 4014 CRT and hard copy unit, which operates at transmission rates up to 9600 BAUD.

We consider the entire package (modified SUPER*SCEPTRE plus DISSPLA) to be quite suitable for our purposes. Although we have not yet stretched SUPER*SCEPTRE to its limits, the many circuits analyzed thus far have shown no intractable difficulties. SUPER*SCEPTRE is not expected to be a perfect solution to our analysis problems, but we are hopeful and anticipate that it will be a very valuable tool.

The circuit in Fig. 18 is used to provide an example of the output of the SUPER*SCEPTRE-DISSPLA package. It contains two Josephson junctions in parallel, separated by an inductance, and driven with a sinusoidal current. This combination is one manifestation of a double-junction SQUID. Fig. 19 shows the driving current, the voltage response at the second junction and the current in the inductance, each as a function of time. The total cost to obtain this result, including computer time, line printer, and plotting, was about $6.

We anticipate using the program for simulating superconducting and normal transmission lines, large-area Josephson junctions, multi-junction SQUIDs or interferometers, and circuits with many Josephson junctions.

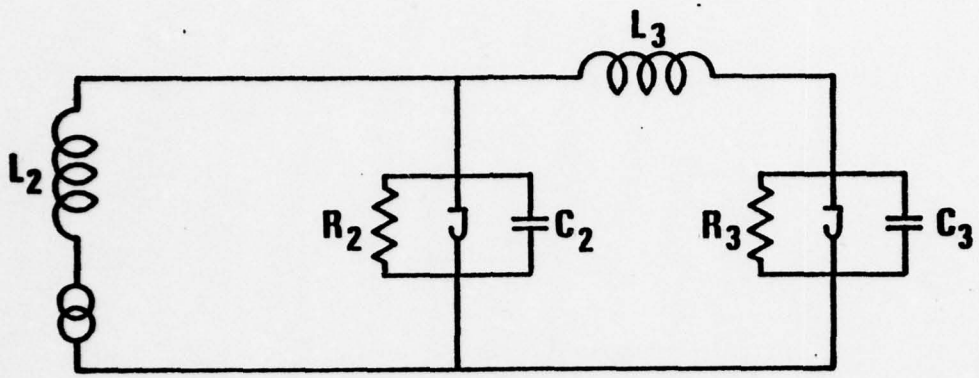


Figure 18

Simple two-junction circuit for test of SUPER*SCEPTRE. The driving current which is sinusoidal is shown at the top of Figure 19.

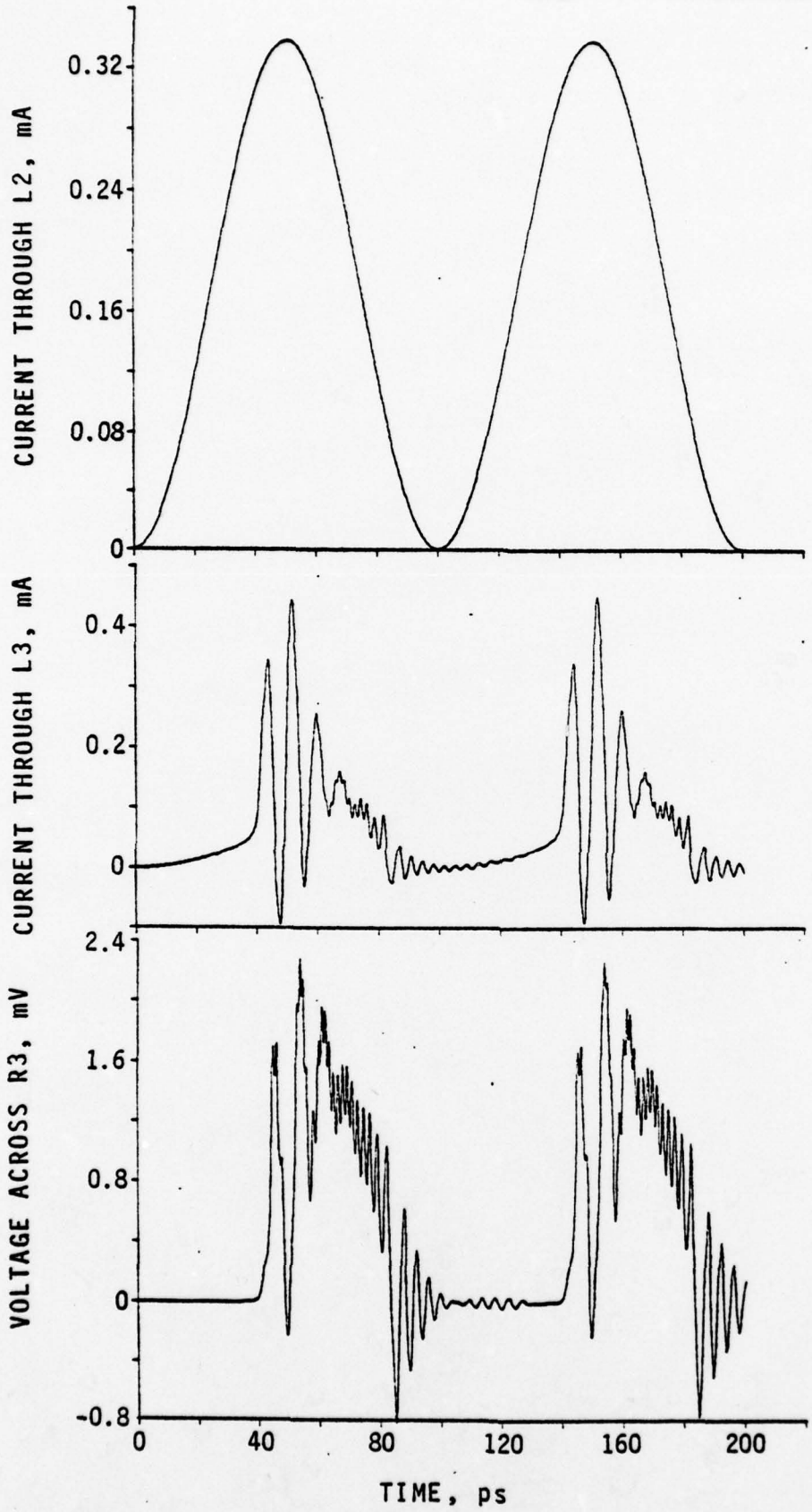


Figure 19

Solutons for two-junction circuit shown in Figure 18. The circuit elements R3, L3 and L2 refer to Figure 18.

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Fuschillo, N., Lalevic, B., and Annamalai, N. K., J. Non-Crystalline Solids, 21, 85 (1976).

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Photolithographic fabrication of lead alloy Josephson junctions[a)]

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Techniques for the photolithographic fabrication of thin-film Josephson junctions are presented in detail, including metal liftoff processes, lead alloy composition, and formation of tunneling junction barriers using plasma oxidation in an rf discharge. A comparison with earlier rf plasma oxidation studies on Pb(In)–oxide–Pb junctions shows the tunneling resistance of Pb(In,Au)–oxide–Pb(Au) junctions to be nearly two decades lower for a given oxygen pressure in the rf discharge; this difference was attributed to the use of different alloys and sputtering parameter measurement techniques in the respective studies. Typically, tunneling resistance decreased by only 2% after ten thermal cycles, but decreased at an accelerated rate with subsequent cycling. Room-temperature storage often induced downward resistance changes on the order of 30% per month. Junctions stored at −15°C generally showed little change after a period of three months.

PACS numbers: 85.25.+k

I. INTRODUCTION

Many attempts have been made to fabricate reliable Josephson devices which will survive repeated thermal cycling to 4.2 K. These efforts have been stimulated by the growing list of Josephson junction applications[1]: high-frequency detectors and mixers, voltage and other standards, SQUID magnetometers, and computer switching elements. More recently, ultrahigh speed Josephson junction electronic circuits such as analog-to-digital converters, sampling circuits, and counters have been proposed or constructed.[2] Until recently, progress with all of these applications has been impeded because of the lack of adequately reliable and reproducible devices.

This paper specifically addresses improved fabrication processes for thin-film lead alloy Josephson junctions, including lift-off techniques, alloy composition, and tunneling barrier oxidation parameters. Although identical or very similar processes have appeared in the literature,[3–7] a detailed overview of the fabrication process is presented for completeness. In addition, process parameters and device test results are given for Pb(In,Au)–oxide–Pb(Au) Josephson junctions. These alloy junctions are particularly important from the standpoint of an improved thermal cycling capability.

II. LIFT-OFF TECHNIQUES

An important consideration in the fabrication of thin-film Josephson junction circuits is to avoid damaging electrode surfaces in processing. Consequently, the lift-off method[4] was used in preference to alternative methods of chemical etching and sputter etching. However, a reverse bevel profile for the photoresist edge is generally required to provide separation between the desired pattern and portions to be "lifted off"; otherwise, tearing will occur and lead to jagged electrode edges. Two methods were employed to obtain the required reverse bevel: (1) forming an aluminum–photoresist composite[4] and (2) profiling the photoresist by treating it after exposure with chlorobenzene.[7] In both methods, Shipley AZ-1350J[8] photoresist was used.

The first method involved a sequence of steps which is described elsewhere,[4] and yielded an aluminum shadow mask (approximately 300 nm thick) supported by a photoresist layer approximately 1.5 μm thick. A lead alloy film evaporated onto this mask is shown in Fig. 1. Note particularly the "penumbra" effect at the edge of the alloy film. This problem has been corrected by using movable sources so that each component of the sequentially deposited alloy can be evaporated from the same point. Although a dramatic reverse bevel is obtained using this method, several tedious steps are involved, the aluminum layer is subject to tearing, and resolution is limited.

Consequently, a new single-step method of photoresist profiling[7] was adopted which produces a somewhat less dramatic, but quite adequate, reverse bevel in the photoresist itself. The new technique involves prebaking the photoresist at a reduced temperature (70°C, instead of 90°C, for 25 min), increasing the exposure to uv by a factor of 2, soaking the wafer for 10 min in chlorobenzene following exposure, and finally, overdeveloping the pattern (2 min in Shipley AZ developer[8] diluted 1:1 with water). A profiled photoresist layer with overlaid lead alloy film is shown in Fig. 2. Note that the undercut in the photoresist suffices to separate the electrode from the layer to be "lifted off"; the edge of the electrode maintains a smooth profile after lift off if the evaporation source is near the substrate normal.

III. ALLOY COMPOSITION

Alloy films of lead with indium and/or gold were used primarily for their reported resistance to hillock formation induced by thermal cycling.[9,10] During warming, thermal expansion leads to compressive stresses in the plane of the film

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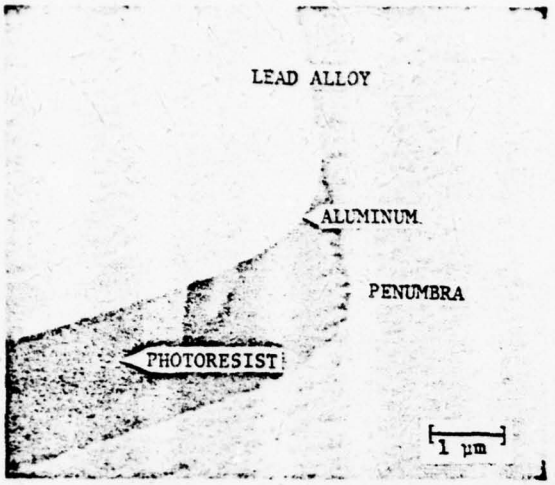

FIG. 1. Lead alloy film evaporated onto an aluminum shadow mask. The photoresist layer supporting the mask is approximately 2 μm thick.

which can cause hillock growth.[11] Hillock growth can be extremely detrimental to Josephson junction devices, since penetration of the oxide tunneling barrier by a hillock will probably result in an electrical short.

The first electrode was formed by sequential evaporation of 50 nm of In, 10 nm of Au, and 350 nm of Pb.[12,13] The alloy is formed during the photoresist prebake cycle (70°C for 25 min) which precedes exposure of the second electrode pattern. One might expect subsequent oxidation of the alloy surface to produce a homogeneous mixture[14] of In_2O_3 and PbO in similar proportions to the elemental content of In and Pb. However, Auger studies[15] have shown that indium in the alloy is preferentially oxidized; oxides of Pb(In) alloy thin films are indium enriched in concentrations which depend on specific alloy composition and film thickness. For Pb(In) alloys containing more than 30 at. % In, the surface layer of the oxide has been found[15] to be pure In_2O_3. The preferential oxidation of indium has been attributed[12] to the higher free energy of In_2O_3 formation compared with PbO.

Since the potential barrier height of In_2O_3 is lower than that of PbO, similar tunneling currents can be obtained with a thicker layer of In_2O_3 than PbO—an apparent advantage in terms of tunnel junction reliability.[10]

The second electrode consists of a sequential evaporation of 300 nm of Pb, 5 nm of Au, and 200 nm of Pb.[12] Since In has a higher free energy of oxide formation than Pb, it must be excluded from the second electrode to avoid the tendency for oxygen in the barrier to diffuse into the second electrode where it could form stable oxides. Although the Pb(Au) alloy exhibits a greater tendency for hillock formation than the Pb(In,Au) alloy,[9] junctions typically survive many thermal cycles as discussed in Sec. V. The second electrode is heat treated for 50 min at 70°C during subsequent photoresist baking.

IV. OXIDATION

A crucial step in the fabrication of thin-film Josephson junctions is the formation of an oxide tunneling barrier which is typically only a few nanometers thick. Junction properties are strongly dependent upon oxide layer integrity and thickness; indeed, the tunneling resistance of Pb–oxide–Pb junctions changes by more than a decade for each 0.4-nm change in oxide thickness.[16] Thus, oxide layer formation must be controlled in a repeatable fashion if Josephson junction circuits are to be reliably made.

Both predictable and consistent oxide tunneling barriers can be fabricated by low-power rf sputter etching in an oxygen plasma.[5,6] The process involves a continuous sputter etching and reoxidation of the electrode surface. Substrate temperature, oxygen pressure, rf power (or cathode self-bias), and time are variables which must be controlled, although evidence[5,6] indicates that the sputter etching and oxidation process for pure Pb eventually approaches an equilibrium state and thereafter barrier thickness is constant, independent of time.

For purposes of this study, oxidation time and cathode self-bias (CSB) were held constant while oxygen pressure was varied from run to run. Although no attempt was made to measure substrate temperature, the substrates were provided with thermal backing[17] and pressed against the water-cooled cathode. Immediately prior to oxidation, substrates were cleaned by sputter etching in an argon atmosphere of 0.8 Pa (6×10^{-3} Torr) for 2 min at 0.082 W/cm^2 or 70 V of CSB. Subsequent oxidation was in pure oxygen at pressures indicated in Fig. 3, maintained for 10 min with a CSB of 45 V, corresponding to an rf power density of approximately 0.055 W/cm^2. Sustaining a constant CSB may require small adjustments in rf power or matching conditions during oxidation, and further adjustments may be required for different oxygen pressures. It should be noted that the values of CSB given are system dependent since measurement of CSB is known to load the discharge.[18]

As seen from Fig. 3, the measured tunneling conductance per unit area (and critical current density calculated therefrom as discussed in Sec. V) is inversely proportional to approximately the fourth power of oxygen pressure. This result differs from earlier work on Pb(In)–oxide–Pb junctions,[5]

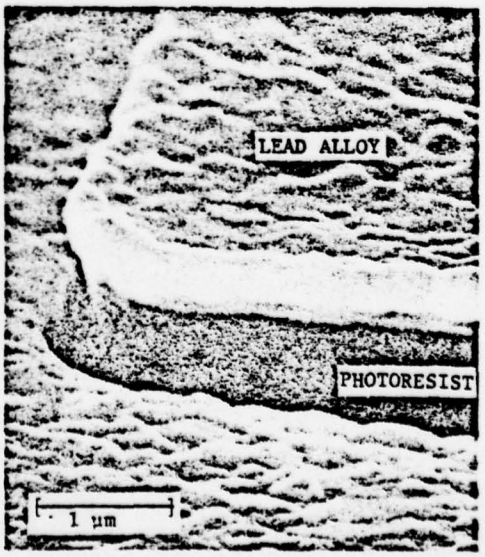

FIG. 2. Lead alloy film evaporated onto a profiled 1-μm-thick photoresist layer.

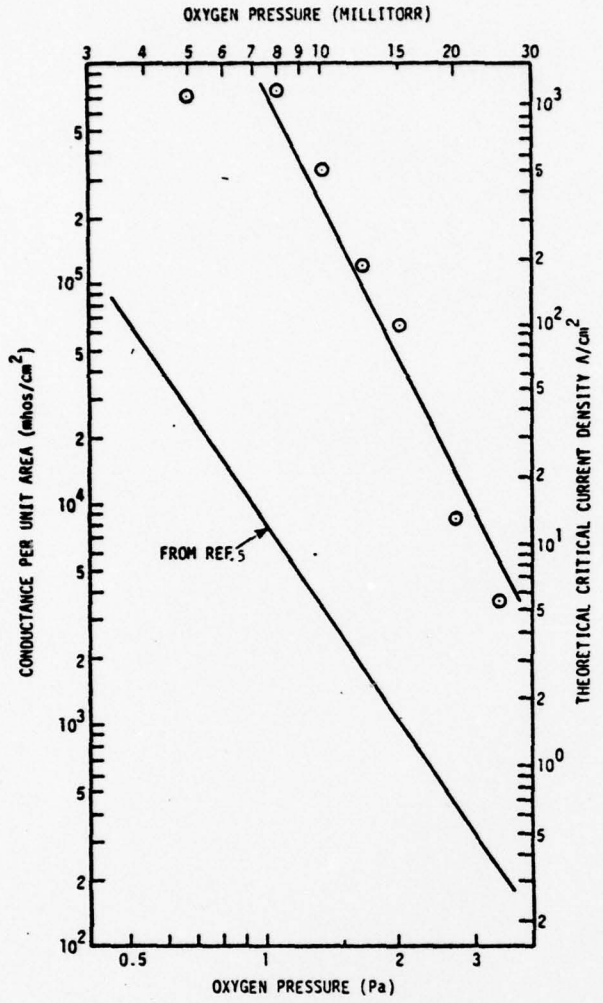

FIG. 3. Conductance per unit area of rf-sputter-oxidized tunnel junctions as a function of oxygen pressure. Cathode self-bias was regulated at 45 V and rf power was approximately 10 W during oxidation. The line drawn through the points is proportional to the fourth power of oxygen pressure. The lower line shows similar results from Ref. 5 and illustrates the great sensitivity of the process to alloy composition and measurement of the oxidation parameters. The scale on the right gives the theoretical critical current density as calculated in Sec. V using $R_3/R_2 = 0.2$.

where tunneling conductance is lower by approximately two orders of magnitude and is found to be inversely proportional to the cube of oxygen pressure. This may be due to the use of different alloys and sputtering conditions (or differences in measuring them) in the respective studies.

V. *I–V* CHARACTERISTICS

The current–voltage characteristic of a typical Pb(In,Au)–oxide–Pb(Au) junction is shown in Fig. 4. The supercurrent at zero voltage and jump in current at the energy gap (about 2.5 mV) are typical of tunnel junctions made of pure lead. Well-known Fiske modes are revealed by structures around 0.7 mV. In contrast to pure lead junctions, the alloy junctions exhibit a current jump at about 1.3 mV and significant current (usually referred to as excess current) is observed below the gap. This current is probably due to intrinsic properties of alloy junctions.

To discuss this structure it is helpful to introduce a small number of parameters (chosen for convenience of measurement) by which the I–V curve can be characterized. The current through the junction is measured at 2 and at 3 mV; that is, just below the gap and just above it. Each of these currents is divided into the corresponding voltage to give resistances R_2 and R_3, respectively. The ratio of R_3 to R_2 provides a measure of the excess current; the ratio is small for small excess current and large for large excess current. For a typical "good" junction, R_3/R_2 falls in the range 0.15–0.25.

Since external magnetic fields often suppressed the measured critical current, the critical current scale of Fig. 3 was calculated theoretically. In the absence of a theory for lead alloy junctions, a model was chosen in which the current through the junction is the sum of the current that would be observed in a pure lead junction and the current through a parallel resistance (corresponding to the observed excess current). The ratio of the critical current I_c to the jump in quasiparticle current at the gap has been calculated[19] to be 0.755. Using extrapolations to the gap from the R_2 and R_3 values, we find $I_c = 1.925 \times 10^{-3}\,(1/R_3 - 1/R_2)$. From the I–V curve in Fig. 4, $R_2 = 1\ \Omega$, and $R_3 = 0.22\ \Omega$. Based on the formula above, the theoretical value of I_c is 6.8 mA, which is only slightly greater than the 6 mA observed.

The origin of the bump at 1.3 mV is unclear. However, similar structure has been observed[20] in junctions having Pb(Au) alloy electrodes and has been attributed to tunneling from pure lead into the intermetallic $AuPb_3$, combined with the usual tunneling from Pb to Pb. A similar explanation may be possible for the present alloys. It has also been shown[9] that the Pb(In,Au) alloy consists of Pb–In solid solution and the intermetallic $AuIn_2$. Thus one can speculate that the structure in Fig. 4 is due to tunneling from a combination of Pb–In solid solution and $AuIn_2$ in the lower electrode into a combination of Pb and $AuPb_3$ in the upper electrode. Measurements as a function of temperature, which have been made[20] to determine the gap of $AuPb_3$, would further clarify the origin of this structure.

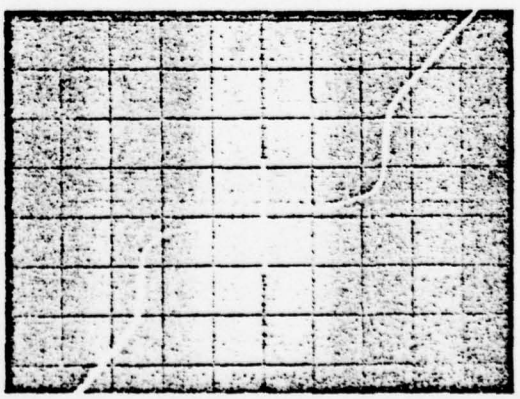

FIG. 4. Current–voltage characteristic of a lead alloy Josephson junction. Since the junction was not magnetically shielded, the critical current may not exhibit maximum value. The junction had a critical current density of 1×10^3 A/cm² and was in its 16th thermal cycle when this curve was obtained. Vertical axis 5 mA/div; horizontal axis 1 mV/div.

VI. THERMAL CYCLING AND STORAGE

The "ideal" Josephson junction could be stored indefinitely at room temperature and cycled to 4 K at will—without noticeable changes in device performance or characteristics. Although no such ideal performance has been reported, the Pb(In,Au) alloy films offer considerable improvement in thermal cycling capability over earlier pure lead and Pb(In) alloy films.[9]

Three samples having five junctions each (with areas of 180 to 1800 μm^2) were cycled extensively. I–V characteristics changed by less than 2% during approximately the first ten thermal cycles. Thereafter, both R_3 and R_2 decreased more rapidly and R_2 was typically down by a factor of 2 after about 50 thermal cycles. Furthermore, the ratio R_3/R_2 began increasing after about ten cycles, indicative of larger excess current. Not all of the junctions exhibited changed I–V characteristics or junction failure after the same number of cycles. The resistance ratio R_3/R_2 remained less than 0.75 for a minimum of 15 and a maximum of 76 thermal cycles. Generally, the larger the junction, the earlier changes in junction characteristics occurred during thermal cycling.

These observations are consistent with the hypothesis that changes in junction characteristics are caused by hillocks puncturing the oxide barrier and inducing microshorts. It has been observed that hillock growth in films of these alloys is initiated after a certain number of thermal cycles, and is followed by an accelerated growth on subsequent cycles.[9] A similar pattern of hillock growth in junctions tested here could explain the observed increasing rate of change in R_2 and R_3 after about the tenth thermal cycle.

In addition to the problem of thermal cycling, junction resistance gradually changes during room temperature storage. It was found that annealing junctions at 70°C for 50 min substantially accelerated this aging process and thereafter yielded more stable devices. However, even these devices, when stored at room temperature, often showed downward resistance changes on the order of 30% per month. Recently fabricated junctions have been stored at −15°C. These devices have shown little or no degradation over a storage period of 3 months.

VII. CONCLUSIONS

While some of the work described in this paper is preliminary, the junctions were produced by controllable processes and had substantially improved thermal cycling and storage properties when compared to those fabricated from pure lead by more conventional techniques. In addition, barriers have been formed by an oxidation process which permits critical current densities to be obtained over a three-decade range. It is expected that further experience with these processes will produce additional improvement.

ACKNOWLEDGEMENT

For helpful conversations we wish to thank W. Anacker, M. Hatzakis, C. Kircher, J. Matisoo, T. VanDuzer, and H. Zappe. D. Larson and G. Wallace provided invaluable technical assistance. Research is partially supported by the Office of Naval Research under contract numbers N00014-77-F-0048 and N00014-77-F-0019.

[a] Contributions of the National Bureau of Standards, not subject to copyright.

[b] NRC postdoctoral fellow.

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[13] A quartz crystal film thickness monitor was assumed to obey the relation $\Delta f = \rho t/2$ where Δf is the frequency shift, ρ is the density of the film, and t is the film thickness.

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A.2. "Fast Superconducting Instruments," by R. E. Harris and C. A. Hamilton, Future Trends in Superconductive Electronics, ed. by B. S. Deaver, Jr., C. M. Falco, J. H. Harris, and S. A. Wolf (American Institute of Physics, New York, 1978), pp. 448-458.

FAST SUPERCONDUCTING INSTRUMENTS*†

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ABSTRACT

The emerging technology for fabricating superconducting integrated circuits offers the possibility of remarkable new instruments. The advantages of this form of electronics are high device speed and low dissipation, combined with lossless, dispersionless, properly terminated transmission lines. A number of possible new instruments are presented. It is shown that a small group can successfully fabricate the superconducting integrated circuits required for these new instruments.

INTRODUCTION

Scientific experimentation, military devices, and the potential arrival of very fast computers all require new fast measurement capabilities. Josephson tunneling logic is a compelling candidate for this new class of instruments. Its known high speed and low power dissipation, its past successes in this field (some Josephson instruments are now available commercially), and its newly developed fabrication technology make it most attractive. In the following we shall discuss some of the requirements of fast instruments, indicate how superconducting electronics meets those requirements, and give a few examples of the kind of instruments that might result. Finally, we discuss progress toward such instruments at the National Bureau of Standards, as an example of what can be accomplished by a small group.

I. REQUIREMENTS

Speed

The speed of a Josephson junction is at least as great as the fastest semiconductor devices. Its intrinsic response time [1] has been shown to be determined by the superconducting energy gap 2Δ as

$$\tau_J = \hbar/2\Delta \quad .$$

For lead, which has an energy gap of 2.5×10^{-3} mV, $\tau_J = 0.27$ ps.

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†Supported in part by the Office of Naval Research under contracts N00014-77-F-0048 and N00014-77-F-0019.

A more serious limitation is due to the intrinsic capacitance C of a typical Josephson device which consists of two planar electrodes separated by an exceptionally thin insulating layer. An $R_N C$ time constant (R_N is the junction normal state resistance) provides a measure of the response time of the device [2]. Although data on this time constant are scarce for the alloys from which junctions are usually made, R_N can be estimated from a patent [3] for an alloy of Pb with 6.5% In. The capacitance C can be approximated from other data. The resulting dependence of $R_N C$ on the current density j_c and the barrier thickness is shown by the solid line in Fig. 1. The left ordinate gives $R_N C$ normalized to the intrinsic response time. The right ordinate gives the time in ps for a lead alloy junction. The numbers along the curve give the oxide thickness in Angstroms. The x's are actual values from several papers. The figure is probably correct to half an order of magnitude. Reliable junctions have been commonly fabricated with critical current densities up to at least 2×10^3 A/cm^2. This corresponds to $R_N C/\tau_J$ = 13. Thus for lead, $R_N C$ = 3.5 ps, an extremely low value when compared to conventional electronic devices.

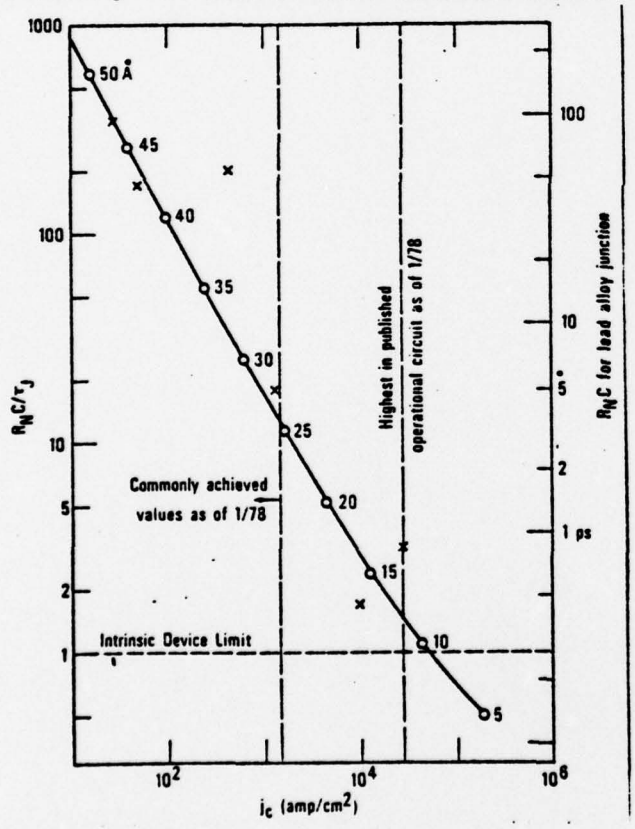

Fig. 1. Response time of a Josephson tunnel junction, when limited by $R_N C$, as a function of critical current density j.

The fastest junction reported in an operational logic device had j_c = 2.8×10^4 A/cm^2 ($R_N C$ = 0.87 ps). It may also be possible to fabricate reliable devices having higher critical current densities. Thus $R_N C$ times approaching the intrinsic device limit may be possible. Other parameters serve to make it difficult to achieve this performance in a circuit, but at least one calculation [4] suggests switching times shorter than 1 ps will be possible.

Dissipation

High speed devices necessarily require small size. Recall that signals propagating at the speed of light travel at most 0.3 mm (0.012 in.) in 1 ps. If an instrument consists of many interconnected elements which must interact with each other within the response time of the instrument, then its maximum size will be determined by the desired speed of operation. We must thus consider the possibility of 1 ps instruments which have a maximum dimension of only a few tenths of a mm.

If the elements in a circuit are located close together, the total dissipation must be sufficiently small that the operating temperature can be maintained. The heat produced by very fast conventional devices already places a severe limit on the number which can be located on the same integrated circuit chip.

Heat dissipation has been shown to be of fundamental origin by Keyes [5]. It varies as the square of the operating temperature. Thus cryogenic devices should offer significant reductions in dissipation.

In particular, Josephson junctions offer 1000 to 10,000 times lower dissipation than semiconductor devices. Thus while the density of fast semiconductor devices is seriously limited, it should be possible to fabricate rather complex superconducting integrated circuits without serious dissipation problems. For this reason, low dissipation is probably a more significant advantage of superconducting electronics than the high speed of the Josephson junction. For example, the Transferred Electron Device (TED) exhibits a response time which is comparable to that of a Josephson junction, but the heat dissipation is much greater.

Terminated Superconducting Transmission Lines

Superconducting technology offers not only a remarkably fast, low-dissipation active element, but also makes possible the use of nearly lossless, dispersionless microstrip lines [6]. These lines are composed of a superconducting ground plane, covered by an insulator, with a narrow superconducting strip on top. Their high quality persists from dc up to frequencies approaching that of the superconducting energy gap, about 700 GHz [7]. In contrast, the miniaturization of normal state lines for use in integrated circuits produces excessive dispersion and loss.

The usual technique in superconducting circuits is to transmit signals from one logic level to the next via overlaid control lines. These lines can be accurately terminated with a resistor [6]. This is another important advantage since it reduces interference from reflections and maintains the highest possible speed.

II. EXAMPLES OF POSSIBLE SUPERCONDUCTING INSTRUMENTS

The use of new lithographic techniques for fabricating superconducting circuits makes possible not only fast new instruments, but also improvements in superconducting instruments of existing design.

Extensions of Existing Techniques

The ac Josephson effect now provides a reference voltage with which the U. S. legal volt is maintained. This reference is of the order of 5 to 10 mV. As we shall see below, lithographic thin film fabrication techniques may make possible a substantial increase in this reference level.

The use of arrays of Josephson junctions as microwave detectors offers promise. Such arrays would have higher impedance and lower saturation levels than single junctions. Their fabrication is carried out conveniently only by using lithographic techniques. Additionally, the use of the quasiparticle curve as the nonlinear element in a detector [8] may be a significant competitor for existing devices.

Present SQUIDs are rf biased primarily because of the difficulty of fabricating more than one junction in a device. Dc biased SQUIDs, consisting of at least two Josephson junctions fabricated lithographically, would not require the complicated room temperature rf biasing circuitry, but would still provide the same or better sensitivity and signal-to-noise ratio. The new fabrication techniques might also allow a low noise superconducting amplifier to be placed on the same chip as the SQUID.

Finally another paper at this conference suggests the replacement of the whisker-type contacts normally applied to frequency synthesis with a Josephson thin film device [9].

Important Elements of New Instruments

There are a variety of possible new instruments. Those to be discussed here make use of two simple components, a current comparator and a sample-and-hold circuit. Some instruments may also make use of digital logic.

Current Comparator

A Josephson gate is essentially a current comparator. In digital circuits it must determine only whether a signal represents a "0" or a "1". However, it can also be used in an analog sense [10]. If the gate is biased in the zero voltage state with some current flowing through it, then the gate will switch at some well-defined current flowing through the control line over the gate. One can vary the switching point by providing a bias current through a second control line over the gate. Thus an adjustable current

comparator results. It should operate as fast as any Josephson gate -- that is, ultimately in less than 1 ps.

Sample-and-Hold

Sample-and-hold circuits are used to sample a signal in a very short time, and maintain it until it can be characterized by a slower device. One possible kind of superconducting sample-and-hold device would store a persistent current in a superconducting loop. The current would be switched in and out of the loop using a Josephson junction. Since the maximum flux in the loop, LI_o, is quantized in units of the flux quantum, 2.07×10^{-15} Wb, the inductance of the loop would have to be large enough to permit the loop to contain enough flux quanta to achieve the desired resolution. The speed of response of such a simple circuit would be determined by the time required for the Josephson junction to go from the normal state to the superconducting state. Times as short as 1 ps might be achieved.

Logic Circuits

Logic operations may also be essential in some instruments. A counter for example must perform logical operations. Such elements of an instrument might be quite similar to those in superconducting computers.

A Few Possible Josephson Instruments

Analog Sampling Device

Published [10] and unpublished reports of sampling devices suggest that such instruments have already been constructed having a time resolution of a few ps. Such sampling devices are constructed from current comparators of the type described above. Present conventional sampling oscilloscopes have a time resolution of about 25 ps.

Fast Counters

It should be possible to construct fast counters using superconducting technology. The speed of response would be determined by the speed of the circuitry for the least significant bit. More significant bits would change state more slowly and would therefore not be as important. Careful engineering of the first stage might bring the response time down to a few picoseconds, corresponding to a counting rate of order 500 GHz. Present maximum counting rates are about 500 MHz.

A/D Converters

In conventional electronics the fastest analog-to-digital converters are of the parallel type. That is, the converter contains

one current (or voltage) comparator for every possible level of the input analog signal. Thus, a 4-bit converter might have 16 comparators. Subsequent circuitry then condenses the 16 bits of level information into a 4-bit binary word. A similar design in superconducting technology would also provide the highest possible speed.

A/D conversion is subject to limitations. One cannot accurately digitize a signal which is changing faster than the resolution of the converter. Thus, sample-and-hold circuits are used to maintain a signal until it can be digitized. The aperture time t_{ap} of a sample-and-hold circuit may determine the fastest signal which can be digitized. During this period the signal is allowed to change no more than one part in 2^n for an n-bit converter. Assuming a sine wave at frequency f, one finds

$$f_{max} = (\pi 2^n t_{ap})^{-1} .$$

Thus the achievement of the minimum aperture time represents a high priority task if extremely high-speed A/D converters are to be realized. For example, sampling with 4-bit accuracy at a rate of about 10 GHz would be possible with aperture times below about 15 ps. Present A/D converters having this accuracy operate in the range of hundreds of MHz. A long range goal might be to reduce t_{ap} below a few ps.

Digital Instruments for Real-Time Signal Processing

Given a high-speed digital technology, it becomes possible to conceive of real-time applications of computational techniques which previously were done off-line, or which could be applied only to very slow signals. One such example involves Fourier analysis of signals. Such signals might pass through a superconducting A/D converter of the type discussed above, and then be digitally analyzed using a special-purpose fast Fourier transform processor designed to perform these calculations at the highest possible speed. Such an FFT processor could produce a variety of instruments. Digital filters could be produced which might have rapidly tunable frequency, lineshape, etc., possibly controlled by the incoming signal. In addition a multi-channel spectrum analyzer having high speed and a large number of channels should be feasible. Such analyzers are now being developed, using conventional technology. This device could also be coupled with processing, possibly using special purpose pattern recognition circuits, to examine the data in real time.

III. PROGRESS TOWARD SUPERCONDUCTING THIN FILM INSTRUMENTS AT THE NATIONAL BUREAU OF STANDARDS

While the preceeding discussion suggests a number of possible areas in which superconducting electronics can make significant contributions, there remains the question of the difficulty of fabricating them. Our experience shows that considerable success can be achieved by a group of three people. The following discussion of our problems

and successes is offered for the consideration of others who might enter the field or attempt to assess its future impact.

The effort is about two years old. The first year was largely concerned with the procurement and assembly of the required equipment. This includes a complete mask-making facility, three vacuum evaporators, and the equipment required to do photoresist lift-off processing. The work to date has been largely directed towards reproducing techniques reported in the literature.

Considerable time was devoted to the production of photoresist layers with sufficient undercutting so that tearing would not occur in the lift-off process. If the deposited metal layer is connected where it crosses the edge of the photoresist, it will tear during lift-off and ragged edges result. The method finally adopted involves soaking the photoresist in chlorobenzene [11] prior to development. Figure 2 shows such a photoresist layer with 4000 Å of lead alloy deposited on top. The chlorobenzene treatment results in an undercut of about 2000 Å which is sufficient to make the deposited film discontinuous at the edge.

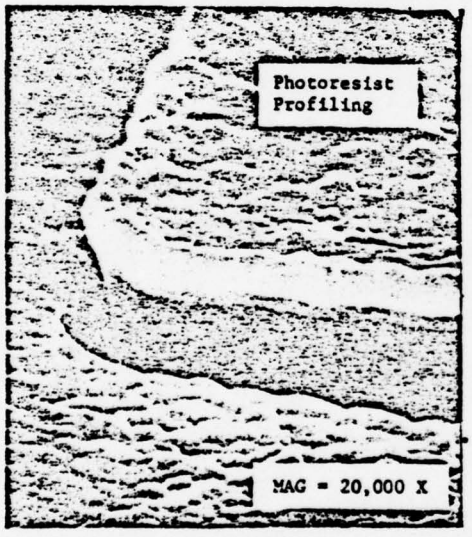

Fig. 2. Lead alloy film evaporated on a 2 μm thick photoresist layer. The photoresist is undercut due to treatment with chlorobenzene.

Control of edges is essential for the production of junctions with good I-V curves and predictable critical currents. Our measure of the quality of a junction is the ratio of the instantaneous resistance at 2 mV to that at 3 mV (i.e., 2 mV/I(2mV) and 3 mV/I(3mV)). Typical values of this ratio for our good junctions are five to six. While it is possible to fabricate good junctions by simply overlapping the electrodes, we have found that junctions made through windows in a layer of silicon monoxide are more consistently of high quality.

The oxide barriers are formed by rf sputter oxidation [12]. Figure 3 gives an indication of the reproducibility and transferability of the process. The figure plots the critical current density as a function of oxygen pressure for fixed rf power and an oxidation time of ten minutes. The bottom curve is derived from the paper which first reported this technique [12]. We do not

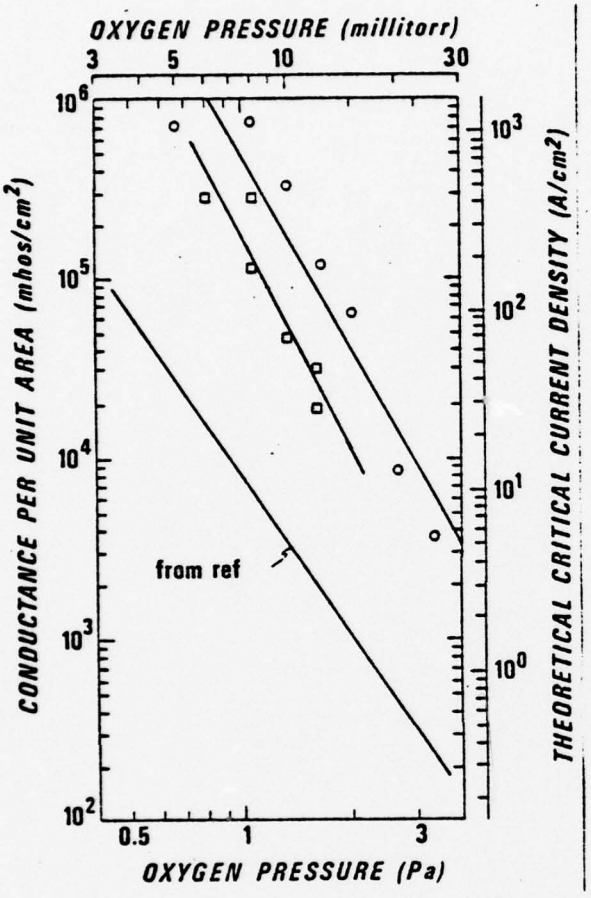

Fig. 3. Conductance per unit area of rf sputter oxidized tunnel junctions as a function of oxygen pressure. Cathode self bias was regulated at 45 volts and rf power was approximately 10 W during oxidation. The lower line is from reference 12. The square and circle points represent our data taken under somewhat different conditions. See text.

characterize our rf conditions in the same way, but a comparison of this curve with ours illustrates the great sensitivity of the process to the rf conditions. The top curve has been reported previously by us [13]. Since then we have made slight changes in the vacuum system and have begun the use of SiO windowed junctions. We are now obtaining the results indicated by the middle curve. The difference suggests that there are some parameters which are not sufficiently well understood and therefore not adequately controlled.

Another important property of these junctions is their ability to cycle repeatedly between room temperature and helium temperature. We have performed automated cycling tests using a low-helium-consumption apparatus [14]. Figure 4 is a plot of normalized junction resistance versus the number of thermal cycles. Most of the devices tested changed very little for the first 10 to 15 cycles and degraded rapidly after that. Lahiri and Basavaiah [15] have recently reported that the use of thinner films can substantially improve cyclability. Nevertheless the junctions we have already made are sufficiently stable to demonstrate prototype instruments.

Storage of these devices is also an important consideration. Data thus far indicate that storage at room temperature can produce significant changes in a period of a few days while junctions stored at -15°C remain essentially unchanged for up to eight months.

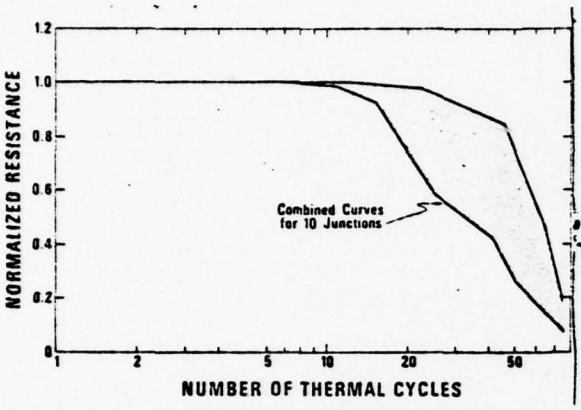

Fig. 4. Normalized junction resistance as a function of the number of thermal cycles.

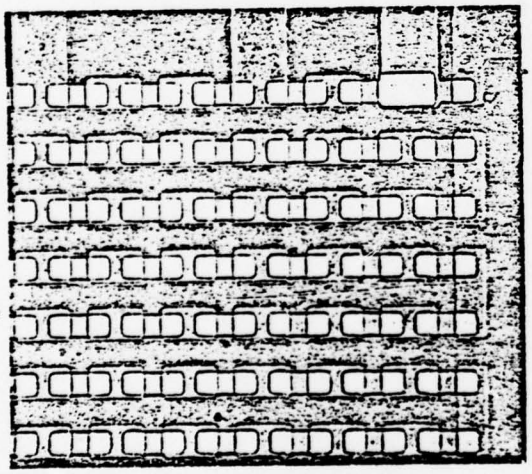

Fig. 5. Photograph of a portion of a series array of 5276 junctions.

The most complex device which we have fabricated thus far is a series array of 5276 junctions, each with dimensions of about 15 μm x 15 μm. A portion of this array is shown in Figure 5. The array is being studied as a potential candidate for a voltage standard at the one volt level. The operation of such a standard would make use of zero-crossing steps as discussed by Levinson, et. al [16].

Observation of the I-V curve of this array provides a convenient way to measure the reproducibility of a large number of nominally identical junctions. Figure 6 shows the I-V curve for our first successful array. Although these junctions had considerable excess current, the energy gap is clearly visible at 12.5 V. The transition from the dc supercurrent to the energy gap is smeared out by the variation of critical current from one junction to the next. Viewed with higher sensitivity, this portion of the curve is actually a staircase (nominally 5276 steps). Assumming that each junction switches to the energy gap voltage, a plot of (dV/dI) versus I yields a probability density function for the critical current. For the example shown in the Fig., the mean critical current is 0.9 mA with a standard deviation of ± 12%. In this example, trapped flux is certainly responsible for a large part of the spread.

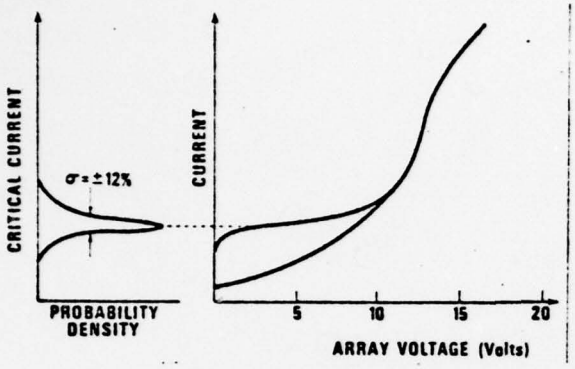

Fig. 6. The I-V curve for a series array of 5276 junctions. The slope of the upper branch of the curve gives a probability density function for the critical current of individual junctions.

Our effort is currently moving toward the incorporation of junctions in high speed circuits. This requires a mounting which is capable of transmission of high speed signals to and from the chip [17]. Figure 7 is a cross-sectional view of our approach to signal coupling. Twenty-four 50 Ω coax lines are terminated at a 2.5 cm diameter printed circuit board. Striplines (50 Ω) on the printed circuit board are laid out so as to contact the lead pads of a chip pressed against the board. By fabricating a long superconducting stripline on the chip, a time domain reflectometer can be used to measure the risetime achievable with the chip mount. These measurements indicate that the risetime for transmission of a signal at room temperature to a superconducting stripline on the chip is less than 70 ps. Through use of both niobium oxide and silicon monoxide as the dielectric we have managed to fabricate superconducting striplines with predictable impedances in the range of 0.1 to 10 Ω. This is a useful range for matching to Josephson junctions.

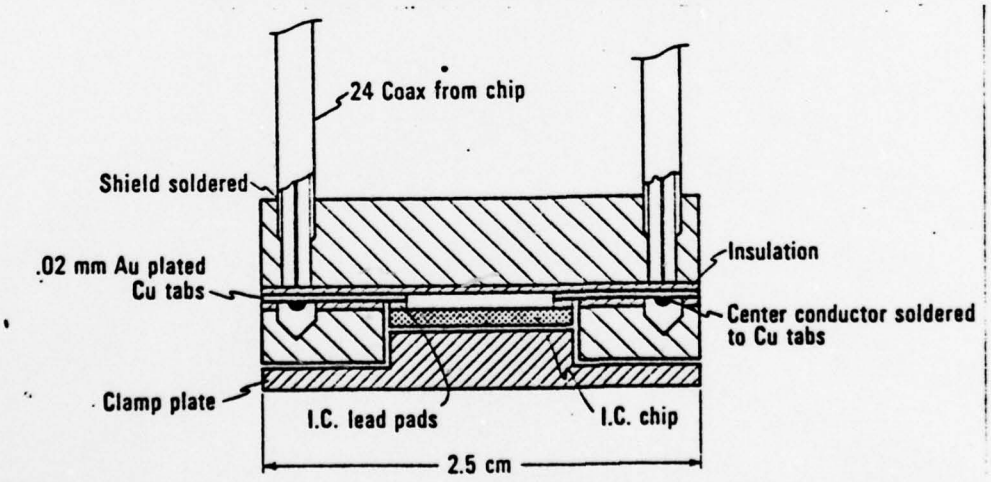

Fig. 7. Cross-sectional view of a chip mount for making 24 high frequency contacts. Signals can be transmitted from room temperature onto the chip with a bandwidth of about 5 GHz.

CONCLUSION

Superconducting integrated circuits utilizing Josephson devices and lossless, dispersionless transmission lines make possible the construction of a variety of useful new instruments. The fabrication technology required is becoming sufficiently well-known that even a small group can use it. Success in constructing portable refrigerators for these instruments would make them even more attractive [18]. Over the next few decades such instruments may find widespread use in areas where the highest possible speeds are required.

ACKNOWLEDGEMENTS

We are grateful to a number of people for stimulating and useful discussions: L. H. Holdeman, W. Henkels, R. L. Kautz, C. Kircher, F. L. Lloyd, D. G. McDonald, D. B. Sullivan, and H. H. Zappe.

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A.3 "Automatic 300 - 4 K Temperature Cycling Apparatus," C. A. Hamilton, Rev. Sci. Instrum. 49, 674 (1978).

Automatic 300–4 K temperature cycling apparatus[a)]

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The apparatus described here automatically cycles small samples between 300 and 4 K by alternately raising and lowering the sample through the neck of a commerical liquid helium storage Dewar. A bellows, which is pressurized by the helium boil-off gas, provides all of the required mechanical motion. By utilizing the cooling available from the boil-off gas, liquid helium helium consumption is limited to 0.03 l/cyc for a 12-g sample. Cycle times can be as short as 5 min.

There is presently a rapidly expanding interest in the development and application of superconducting devices utilizing the Josephson effect. Such devices include SQUIDS and voltage standards, as well as ultrafast logic circuits, samplers, and A/D converters. The ability to withstand repeated cycling between room temperature and 4 K is an essential requirement for the practical utilization of all of these devices. In most cases, considerable development and testing is necessary to meet this requirement.[1]

This paper describes an apparatus for automatically temperature cycling samples between 300 and 4 K. The

apparatus is relatively easy to build and operate. For small samples (12 g) the liquid helium consumption is 0.03 l/cyc with a cycle time of as little as 5 min.

Three methods of making an automatic temperature cycler will be considered. In the first, the sample is placed in a container above the helium bath. Cooling is achieved by transferring a small amount of liquid helium into the sample container. An electrical heater is used to bring the sample back to room temperature. In the second method, the sample container is placed in the helium bath but separated from it by a vacuum space. Cooling is achieved by increasing the pressure (and consequently the heat leak) of the vacuum space. When the vacuum space is pumped out, the sample can be electrically heated back to room temperature.[2,3] The third method involves slowly lowering the sample through the neck of the Dewar. As radiation from the sample reaches the helium bath, the boil-off rate increases. The resulting cold gas flows around the sample providing most of the cooling. Thus the sample is cooled to nearly 4 K before being immersed into the liquid.

The first two methods require considerable automatic valving and pressure control. Furthermore, in the second method, cooling is provided almost exclusively by vaporizing the liquid helium rather than from the cold boil-off gas. The cooling available from the helium gas is about 3000 J/mol, whereas the heat of vaporization is only about 81 J/mol. Thus this method makes very inefficient use of the liquid helium.

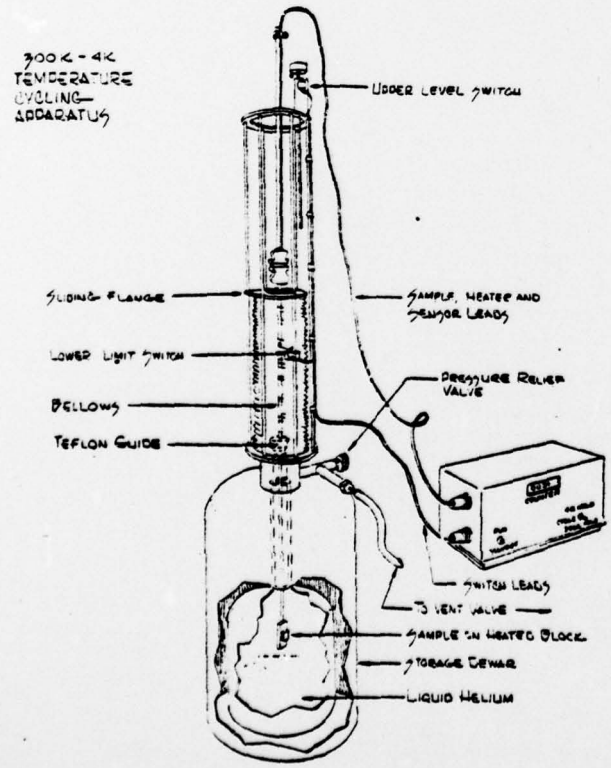

FIG. 1. Functional drawing of temperature cycling apparatus. The sliding flange and the attached sample probe is shown about in the center of its total travel.

The third method was chosen for our apparatus because it makes efficient use of the helium and can be simply implemented. The mechanical apparatus for accomplishing this is shown in Fig. 1. The Dewar used is a commercial superinsulated storage Dewar with a 3.8-cm neck diameter. The sample is mounted at the end of a 100-cm-long stainless steel tube. The sample probe is in turn attached to a sliding flange. A bellows between the sliding flange and the top of the Dewar provides an air tight seal. The 10-cm-diam bellows needs to have an expansion ratio of about 4:1. A very suitable bellows can be made from an ordinary plastic wrapped spiral wire hose such as is used for venting clothes dryers. When the electrically operated vent valve is opened, the sliding flange will slowly lower the sample into the helium. The lowering rate is controlled by pressure from the helium boil-off and thus makes efficient use of the helium gas for cooling. When the sliding flange reaches the lower limit switch the vent valve is closed and a heater at the sample is turned on. In a few seconds this heater produces enough gas to raise the sample well into the neck of the Dewar.

The boil-off rate then returns to the background level of the Dewar and the sample remains relatively stationary as it continues warming. A thermistor sensor detects when the sample reaches 300 K (or any preset temperature) and reverses the operation.

The control circuitry for performing these operations automatically is shown in Fig. 2. This circuitry is also designed to put the system into a safe standby mode if any of a variety of failures occur. In the standby mode the vent valve is closed and the heater off. The sample probe will therefore rise slowly to its upper limit after which helium gas will be vented through the pressure relief valve which is set at 1400 Pa (0.2 psi). The most important part of the fail-safe circuitry is a timer which requires that the sample reach the upper level switch within 20 s after the heater turns on. This prevents loss of the entire He reservoir should a bellows leak develop and will also shut down the system if there is a failure in the heater or its supply. Overheating of the sample due to a failure of the thermistor circuit is prevented by attaching one heater lead under tension with a low melting point solder. Should the temperature sensor erroneously indicate that the sample is at 300 K and the upper level switch is not activated, the system will also switch to the standby mode. This feature, together with the overheating protection, switches the system to standby mode if the temperature sensor becomes either open or short circuited. A three-position switch is used to make the system cycle or hold in either the 300 or 4 K positions.

The Boolean algebra expressions which describe these functions and from which Fig. 2 is derived are

$$H = R\,\bar{V}\,\bar{A}\,\bar{T},$$
$$V = R\,\bar{H}\,\bar{B}\,(\bar{D} + A),$$
$$R = \bar{S} + R_1,$$
$$S = \bar{R} + S_1 + \bar{M}\,\bar{U}\,H + C\,\bar{U},$$

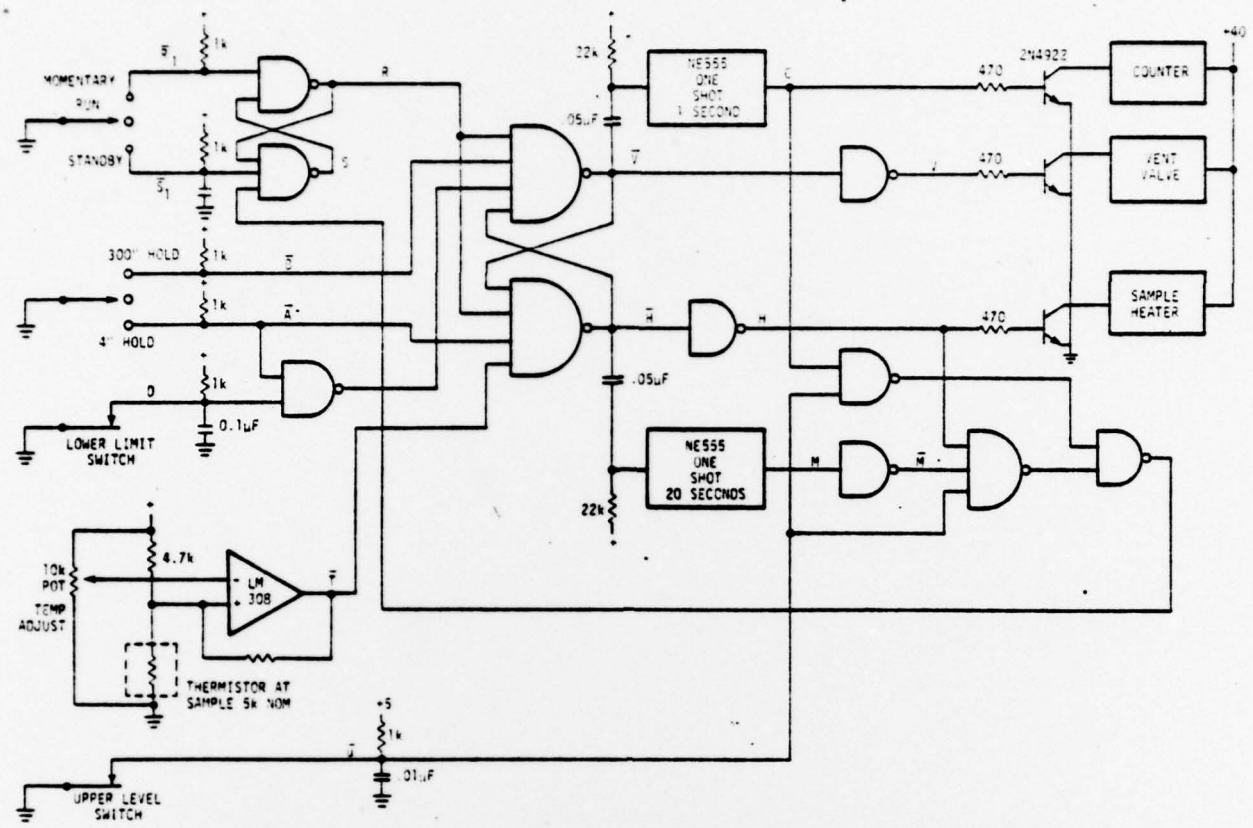

FIG. 2. Logic circuit controls the heater and vent valve to produce automatic cycling or to hold the sample in either the 4 or 300 K positions. Several failure modes are detected, causing the system to switch into a safe standby mode. The logic could be TTL, DTL, CMOS, or, best of all, HTL for noisy environments.

where the inputs are

R_1 = 1 when the system is directed into the run mode by the front panel switch,
S_1 = 1 when the system is directed into the standby mode by the front panel switch,
A = 1 when the system is directed to keep the sample at 4 K,
B = 1 when the system is directed to keep the sample at 300 K,
D = 1 when the probe is at the lower limit switch,
U = 1 when the probe is above the upper level switch, and
T = 1 when the sample temperature is 300 K or greater.

Intermediate logic parameters are

R = 1 when the system is in the run mode,
S = 1 when the system is in the standby mode, and
M = 1 during the first 20 s after the heater turns on,

and outputs are

H = 1 turns on the heater,
V = 1 opens the vent valve, and
C = 1 for 1 s after V goes to 1 and increments the cycle counter.

This control circuitry represents a fairly minimal solution for a safe operating system. Although Fig. 2 looks complicated, it can be built with integrated circuits costing a total of about $5. The entire circuit fits on a 5 by 8 cm printed circuit board. Expanded capability such as direct control of the temperature versus time profile may be a desirable addition. This system has cycled hundreds of times using numerous sample configurations and has never failed in such a way as to waste the helium reservoir or create a dangerous situation.

The helium consumption per cycle consists of the helium required to inflate the bellows (5 l of gas or 0.22 mol) plus the helium required to cool the sample probe from 300 K to 4 K. The total enthalpy change of helium from liquid at 4 K to gas at 300 K is about 6100 J/mol. However, if the sample is cooled to 4 K, even with perfect heat exchange, only about half of the enthalpy change or 3000 J/mol is available for cooling.[4] Typical materials such as metal, ceramic, and plastic give up approximately 100 J/g in cooling from 300 to 4 K. The total material to be cooled in our test probe weighed about 12 g, thus requiring about 1200 J of cooling. The helium consumption with ideal heat exchange would therefore be 0.4 + 0.22 = 0.62 mol. This corresponds to 14 l of helium gas or 0.02 l of helium liquid. The actual measured consumption was 0.03 l of liquid helium/cyc. The energy required to warm the sample from 4 to 300 K was 7.2 W × 175 s or 1260 J. Thus, for this particular sample configuration the system operated at about 60% efficiency relative to ideal utilization of the liquid helium. It is interesting to note that if only the heat of vaporization of the helium were

utilized, the consumption per cycle would be 0.51 l of liquid helium.

The author gratefully acknowledges helpful discussions with Ray Radebaugh and the technical assistance of Donald R. Larson.

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A.4. "Picosecond Pulses on Superconducting Striplines," R. L. Kautz, J. Appl. Phys. 49, 308 (1978).

Picosecond pulses on superconducting striplines[a)]

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The attenuation and phase velocity of a superconducting thin-film stripline are calculated at high frequencies using the theory of Mattis and Bardeen. These results are used to study the propagation of picosecond pulses which have frequency components approaching the superconducting energy-gap frequency.

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I. INTRODUCTION

Recently Peterson and McDonald[1] have shown how picosecond voltage pulses might be generated with a Josephson-junction microcircuit. Such pulses would contain frequency components approaching the superconducting energy-gap frequency. In this paper we use the theory of Mattis and Bardeen[2] for the complex conductivity of a BCS superconductor to study the propagation of picosecond pulses on a superconducting stripline. Several authors,[3–5] considering superconducting striplines at low frequencies, have used the two-fluid model to characterize the superconductors. The BCS model has previously been applied to the superconducting stripline by Mason and Gould[6] and to the coaxial line by McCaa and Nahman.[7] As will be shown, it is essential to use the Mattis-Bardeen theory at frequencies approaching the energy-gap frequency.

To be specific, we consider a thin-film stripline whose characteristics have been measured by Henkels and Kircher.[8] This stripline, of the geometry shown in Fig. 1, consists of a strip of Pb-In-Au alloy separated from a Nb groundplane by a Nb_2O_5 dielectric. Henkels and Kircher estimate the mean free path of normal electrons in the Pb alloy and Nb to be 12 nm and 11 nm, lengths much smaller than the penetration depths which they measure for these materials, namely, 137 nm and 86 nm. This fact allows us to assume a local relationship between the current density J and the electric field E within the superconductors and greatly simplifies the mathematical analysis. Nonlocal theories have been applied to superconducting transmission lines by Mason and Gould[6] and McCaa and Nahman.[7]

In Sec. II we develop expressions for the propagation constant of a superconducting stripline in the limit of local electrodynamics. In Sec. III we compare results for the attenuation and phase velocity obtained using the two-fluid model and the Mattis-Bardeen theory. The propagation of picosecond pulses is discussed in Sec. IV.

II. THEORY

The propagation of a sinusoidal voltage $V(x,\omega)\times\exp(i\omega t)$ on a transmission line is governed by the differential equation

$$\frac{d^2V}{dx^2}=\gamma^2V, \tag{2.1}$$

where γ is the propagation constant. To a good approximation γ is given by[9]

$$\gamma=(ZY)^{1/2}, \tag{2.2}$$

where Z and Y are the series impedance and shunt admittance per unit length of the line.

In analyzing the superconducting stripline we assume that its width W is much greater than the dielectric thickness s and, hence, that fringing fields can be neglected. Assuming a lossless dielectric, Y reduces to the capacitive admittance of a unit length of line, namely,

$$Y=i\omega(W/s)\epsilon\epsilon_0, \tag{2.3}$$

where ϵ is the relative dielectric constant and ϵ_0 is the permittivity of free space. The series impedance is given by

$$Z=i\omega(s/W)\mu_0+(1/W)(Z_{sa}+Z_{sb}), \tag{2.4}$$

where the relative permeability of the dielectric is assumed to be unity, μ_0 is the permeability of free space, and Z_{sa} and Z_{sb} are the surface impedances of the strip and groundplane. The first term of the right-hand side of Eq. (2.4) is the inductance associated with magnetic fields in the dielectric region, and the second term accounts for fields penetrating into the conductors.

The surface impedance used here is defined for an infinite conducting slab of thickness d. Taking one surface of the conductor as the x-y plane and the second

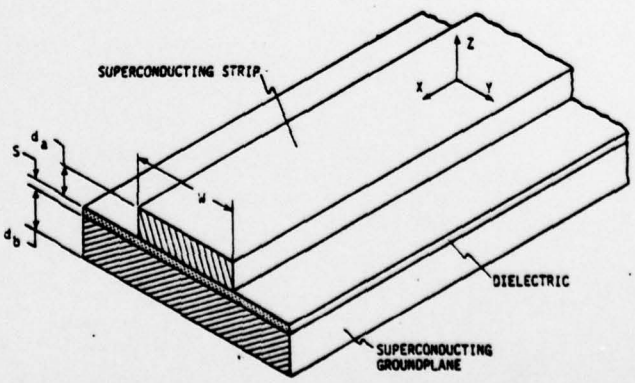

FIG. 1. Stripline geometry. It is assumed that $W \gg s$.

[a)]Contribution of the National Bureau of Standards. Research partially supported by the Office of Naval Research, Contract Number N00014-77-F-0048, dated 1 May 1977.

surface at $z=d$, the surface impedance is defined for sinusoidal fields $E_x(z,\omega)\exp(i\omega t)$ and $J_x(z,\omega)\exp(i\omega t)$ by

$$Z_s(\omega)=\frac{E_x(0,\omega)}{\int_0^d dz\, J_x(z,\omega)}, \tag{2.5}$$

with the boundary condition that the magnetic field be zero at $z=d$ as is appropriate for a stripline with $W \gg s$. Given that $\mathbf{J}$ and $\mathbf{E}$ are related by a complex conductivity $\sigma(\omega)$ and neglecting displacement currents in the conductor, Maxwell's equations can be solved to obtain the surface impedance.[10]

$$Z_s(\omega)=(i\omega\mu_0/\sigma)^{1/2}\coth[(i\omega\mu_0\sigma)^{1/2}d]. \tag{2.6}$$

Thus, given the conductivity of the two superconductors we can obtain the propagation constant of the stripline.

In the two-fluid model the complex conductivity $\sigma=\sigma_1-i\sigma_2$ is given by

$$\sigma_1=\sigma_n\tilde{T}^4, \tag{2.7}$$

$$\sigma_2=(1-\tilde{T}^4)/\omega\mu_0\lambda^2(0), \tag{2.8}$$

where σ_n is the normal-state conductivity at the critical temperature T_c, $\tilde{T}=T/T_c$ is the reduced temperature, and $\lambda(0)$ is the penetration depth at $T=0$. The real and imaginary components of σ translate directly into the normal-electron and superfluid components of the two-fluid model.

Mattis and Bardeen[2] derived a more realistic result for the conductivity using the BCS weak-coupling theory, namely,

$$\frac{\sigma_1}{\sigma_n}=\frac{2}{\hbar\omega}\int_\Delta^\infty d\epsilon\,[f(\epsilon)-f(\epsilon+\hbar\omega)]\frac{\epsilon^2+\Delta^2+\hbar\omega\epsilon}{(\epsilon^2-\Delta^2)^{1/2}[(\epsilon+\hbar\omega)^2-\Delta^2]^{1/2}}$$

$$+\frac{1}{\hbar\omega}\int_\Delta^{\hbar\omega-\Delta}d\epsilon\,[1-2f(\hbar\omega-\epsilon)]$$

$$\times\frac{\hbar\omega\epsilon-\epsilon^2-\Delta^2}{(\epsilon^2-\Delta^2)^{1/2}[(\hbar\omega-\epsilon)^2-\Delta^2]^{1/2}}, \tag{2.9}$$

$$\frac{\sigma_2}{\sigma_n}=\frac{1}{\hbar\omega}\int_{\Delta-\hbar\omega,-\Delta}^{\Delta}d\epsilon\,[1-2f(\epsilon+\hbar\omega)]$$

$$\times\frac{\epsilon^2+\Delta^2+\hbar\omega\epsilon}{(\epsilon^2-\Delta^2)^{1/2}[(\epsilon+\hbar\omega)^2-\Delta^2]^{1/2}}, \tag{2.10}$$

where $\Delta=\Delta(T)$ is the energy-gap parameter and $f(\epsilon)=[1+\exp(\epsilon/kT)]^{-1}$ is the Fermi function. The first integral of σ_1 represents conduction by thermally excited normal electrons, while the second integral, which is zero for $\hbar\omega<2\Delta$, represents the generation of quasiparticles by high-frequency fields. As in the two-fluid model, σ_2 describes the superconducting electrons. The lower limit on the integral for σ_2 becomes $-\Delta$ when $\hbar\omega>2\Delta$. To complete the Mattis-Bardeen picture we note that the reduced gap $\tilde{\Delta}=\Delta(T)/\Delta(0)$ is related to the reduced temperature by the integral equation[11]

$$\ln(\tilde{\Delta})=-2\int_0^\infty d\epsilon\,(\epsilon^2+\tilde{\Delta}^2)^{-1/2}\{1+\exp[(\pi/\gamma_E\tilde{T})(\epsilon^2+\tilde{\Delta}^2)^{1/2}]\}^{-1}, \tag{2.11}$$

where $\gamma_E=1.781$ is Euler's constant.

Above T_c we take $\sigma_1=\sigma_n$ and $\sigma_2=0$ for both models, with σ_n assumed independent of temperature and frequency.

At this point the conductivity can be evaluated at a given T and ω provided we know the material parameters T_c, σ_n, and $\lambda(0)$ for the two-fluid model or T_c, σ_n, and $\Delta(0)$ for the Mattis-Bardeen theory. In order to relate the two theories we use the fact that in the limit of local electrodynamics[12]

$$\lambda=\lim_{\omega\to 0}(i\omega\mu_0\sigma)^{-1/2}, \tag{2.12}$$

to obtain from the Mattis-Bardeen theory

$$\lambda(0)=[\hbar/\pi\mu_0\sigma_n\Delta(0)]^{1/2}. \tag{2.13}$$

A comparison of the two-fluid model and the Mattis-Bardeen theory can thus be made if $\lambda(0)$, $\Delta(0)$, and σ_n are chosen to obey Eq. (13).

The above analysis is subject to the following restrictions. In calculating the shunt capacitance and series inductance it was assumed that the fields are uniform across the thickness of the dielectric, or that[13]

$$v_\phi/\omega \gg s, \tag{2.14}$$

where v_ϕ is the phase velocity and $2\pi v_\phi/\omega$ is the line wavelength. In calculating the surface impedance it was assumed that the depth which fields penetrate into the conductors is small compared to the line wavelength.[14] For superconductors at frequencies below the energy-gap frequency $\omega_g=2\Delta/\hbar$ this assumption is justified only if

$$v_\phi/\omega \gg \lambda. \tag{2.15}$$

For normal conductors and superconductors above the gap frequency the condition becomes

$$v_\phi/\omega \gg \delta, \tag{2.16}$$

where $\delta=(2/\omega\mu_0\sigma_n)^{1/2}$ is the classical skin depth. Because v_ϕ is less than the speed of light, Eqs. (2.15) and (2.16) are sufficient to assure that displacement currents can be neglected in the conductors.[14] The analysis also ignores the possibility of modes of higher order than the transmission-line mode. Such modes will be absent provided

$$v_\phi/\omega > W/\pi. \tag{2.17}$$

Finally, in order to assure a local electrodynamics in the normal state the skin depth must be much greater than the mean free path l[15]

$$\delta \gg l. \tag{2.18}$$

For the example stripline considered in Secs. III and IV all of the above conditions are met for frequencies less than about 10^{13} Hz. For frequencies somewhat higher than this, Eqs. (2.14), (2.17), and (2.18) are all violated.

III. ATTENUATION AND PHASE VELOCITY

The parameters of the example stripline considered in the remainder of this paper are listed in Table I. The values of T_c and $\Delta(0)$ chosen for the Pb-In-Au strip and the Nb groundplane are the bulk values for Pb and Nb.

TABLE I. Parameters of the example stripline.

	Strip	Groundplane	Dielectric
Material	Pb-In-Au	Nb	Nb_2O_5
T_c (K)	7.2	9.2	
$2\Delta(0)$ (meV)	2.73	3.05	
σ_n (Ω^{-1} m^{-1})	7.56×10^6	1.57×10^7	
$\lambda(0)$ (nm)	127	83.4	
ϵ			29
Thickness (nm)	400	400	100

Values for $\lambda(0)$ were obtained from the measured $\lambda(4.2\ \mathrm{K})$ given by Henkels and Kircher,[8] assuming the Mattis-Bardeen temperature dependence. The normal-state conductivities σ_n were obtained from Eq. (2.13) using the assumed $\lambda(0)$ and $\Delta(0)$. These values for σ_n are to be compared with the measured values of Henkels and Kircher, namely, $1.37\times10^7\ \Omega^{-1}\,m^{-1}$ for the Pb alloy and $1.59\times10^7\ \Omega^{-1}\,m^{-1}$ for Nb. While agreement is very good in the case of Nb, it is relatively poor for the Pb alloy, perhaps due to strong-coupling effects. The dielectric constant of Nb_2O_5 is that measured by Henkels and Kircher. Thicknesses of the various layers were chosen to be typical of those used in Josephson-junction microcircuits. Because the propagation constant is independent of the stripline width, it is sufficient to note that $W \gg s$ as is required in order to apply the theory used here.

The power attenuation in decibels per length α_{dB} and the phase velocity v_ϕ can be obtained directly from the real and imaginary parts of the propagation constant. If $\gamma = \alpha + i\beta$, then

$$\alpha_{dB} = (20\log_{10}e)\alpha, \tag{3.1}$$

$$v_\phi = \omega/\beta, \tag{3.2}$$

where e is the base of the natural logarithm. For the example stripline we show in Figs. 2 and 3 the attenuation as a function of frequency and temperature. Solid lines indicate the Mattis-Bardeen results and dashed lines the two-fluid model. At frequencies small compared to the energy-gap frequencies of the superconductors (660 GHz for Pb-In-Au and 740 GHz for Nb at $T=0$) the two models are in reasonable agreement. In the limit of small ω we can derive an approximate expression for the attenuation valid for both models.

$$\alpha_{dB} = (20\log_{10}e)\frac{\mu_0^{3/2}\epsilon^{1/2}\epsilon_0^{1/2}}{4s}\omega^2 \times\left[1+\frac{\lambda_a}{s}\coth\left(\frac{d_a}{\lambda_a}\right)+\frac{\lambda_b}{s}\coth\left(\frac{d_b}{\lambda_b}\right)\right]^{-1/2} \times\left\{\sigma_{1a}\lambda_a^3\left[\coth\left(\frac{d_a}{\lambda_a}\right)+\frac{d_a/\lambda_a}{\sinh^2(d_a/\lambda_a)}\right] +\sigma_{1b}\lambda_b^3\left[\coth\left(\frac{d_b}{\lambda_b}\right)+\frac{d_b/\lambda_b}{\sinh^2(d_b/\lambda_b)}\right]\right\},\quad \omega\ll\frac{2\Delta_a}{\hbar},\ \frac{2\Delta_b}{\hbar}. \tag{3.3}$$

Here subscripts a and b are used to distinguish parameters of the strip and groundplane superconductors, respectively. In the two-fluid model σ_1 is independent of

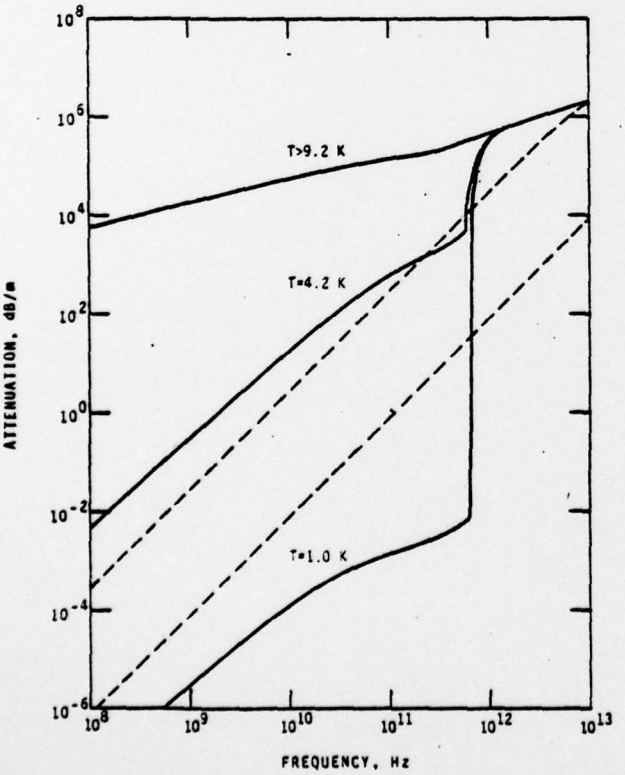

FIG. 2. Attenuation as a function of frequency for the example stripline. Solid lines are for the Mattis-Bardeen theory and dashed lines for the two-fluid model. For $T>9.2$ K both conductors are normal and the two theories give the same result.

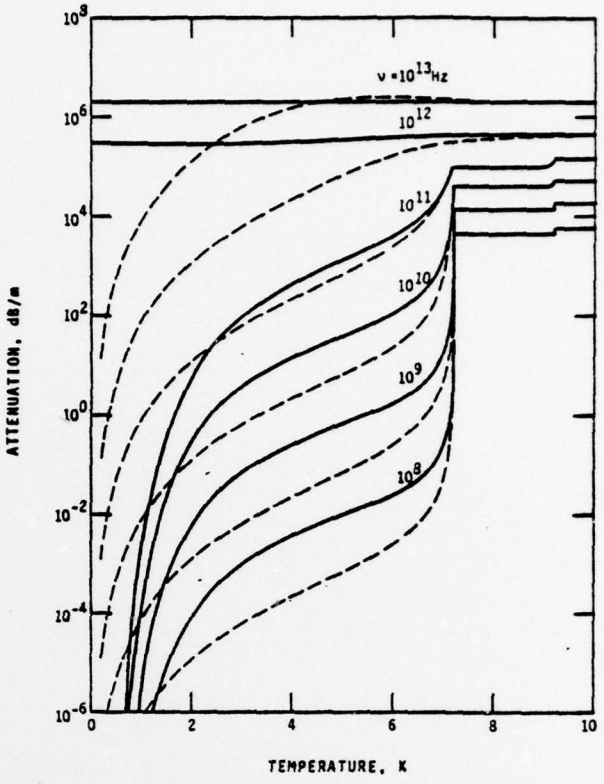

FIG. 3. Attenuation as a function of temperature for the example stripline. Solid lines are for the Mattis-Bardeen theory and dashed lines for the two-fluid model.

ω and α_{dB} is proportional to ω^2. In the Mattis-Bardeen theory

$$\frac{\sigma_1}{\sigma_n} = \frac{2\Delta}{kT} \frac{\exp(\Delta/kT)}{[1+\exp(\Delta/kT)]^2} \ln(\Delta/\hbar\omega), \quad \omega \ll \frac{2\Delta}{\hbar}, \quad (3.4)$$

so that the attenuation deviates from a strict ω^2 dependence by a factor of $\ln(\Delta/\hbar\omega)$. The temperature depen- of the attenuation at low frequencies is also different for the two theories, being T^4 for the two-fluid model while the Mattis-Bardeen theory predicts an $\exp(-\Delta/kT)$ dependence at low temperatures. Thus, the attenuation is expected to fall much more rapidly at low temperatures than the two-fluid model would predict. At high temperatures the two theories gradually approach one another, becoming identical above 9.2 K where both conductors are normal. Between 7.2 and 9.2 K, where Nb is superconducting and the Pb alloy is normal, attenuation is dominated by losses in the normal material and it makes little difference which theory is applied to the superconductor.

The principle difference between the two theories occurs at the energy-gap frequency. As the gap frequencies of Pb-In-Au and Nb are exceeded, the Mattis-Bardeen attenuation increases by several orders of magnitude and rapidly approaches that of the normal stripline. The two-fluid model fails to predict this behavior.

The phase velocity of the example stripline is shown as a function of frequency and temperature in Figs. 4 and 5. At frequencies much less than the gap frequency the phase velocity is given for both models by

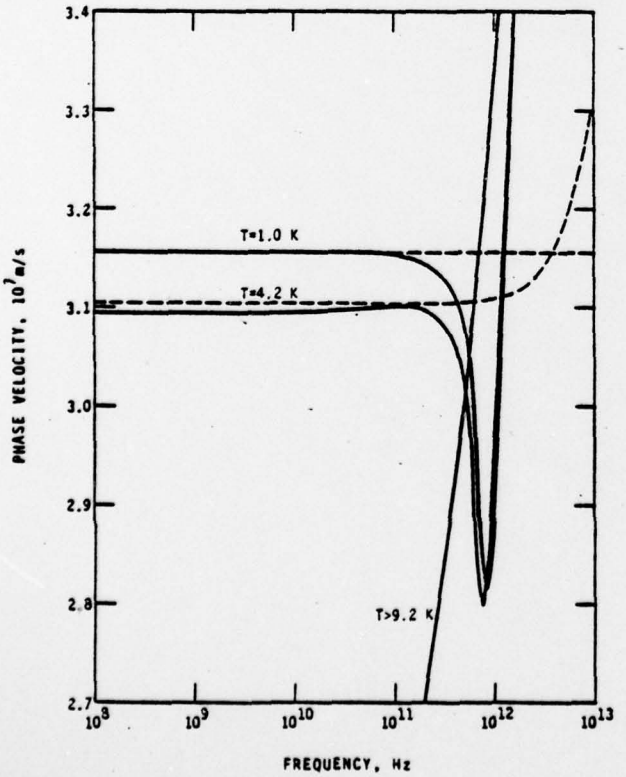

FIG. 4. Phase velocity as a function of frequency for the example stripline. Solid lines are for the Mattis-Bardeen theory and dashed lines for the two-fluid model.

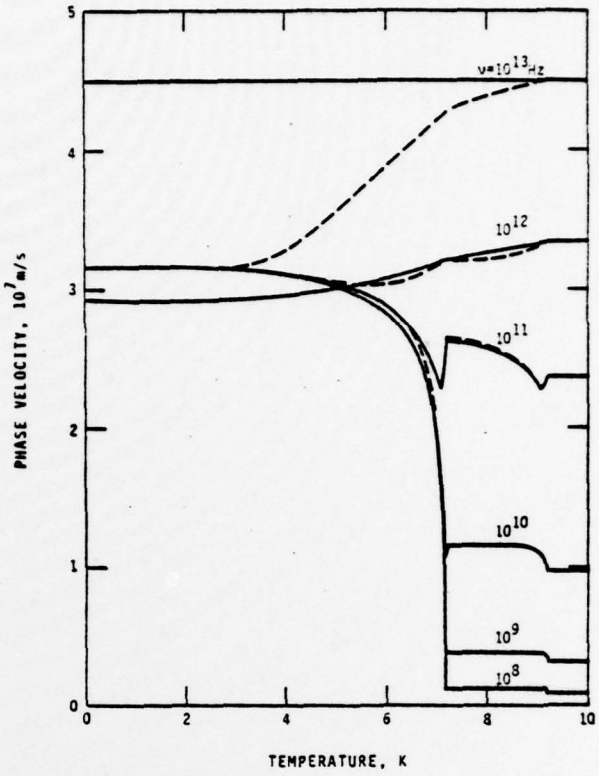

FIG. 5. Phase velocity as a function of temperature for the example stripline. Solid lines are for the Mattis-Bardden theory and dashed lines for the two-fluid model.

$$\nu_\bullet = \frac{1}{(\epsilon\epsilon_0\mu_0)^{1/2}} \left[1 + \frac{\lambda_a}{s}\coth\left(\frac{d_a}{\lambda_a}\right) + \frac{\lambda_b}{s}\coth\left(\frac{d_b}{\lambda_b}\right)\right]^{-1/2},$$

$$\omega \ll \frac{2\Delta_a}{\hbar}, \frac{2\Delta_b}{\hbar}. \quad (3.5)$$

Because the temperature dependence of λ is nearly the same in the two-fluid model and the Mattis-Bardeen theory, the predicted phase velocities are of almost the same magnitude. More importantly, at low frequencies both theories predict a $\nu_\bullet$ which is independent of frequency, making the superconducting stripline dispersionless and suitable for the transmission of information. In the normal state ($T > 9.2$ K); on the other hand, the phase velocity of the sample stripline is highly frequency dependent.

The dispersive nature of the normal-state stripline found here contrasts with the usual dispersionless behavior of macroscopic striplines. In general, a normal transmission line is dispersionless at frequencies sufficiently high that the skin depth δ is small compared to the dielectric thickness s, and the fields are essentially confined to the dielectric region. If the conductor thickness is comparable to or larger than the dielectric thickness, then the line becomes dispersive at frequencies low enough that $\delta \gtrsim s$, in which case field penetration into the conductors is both significant and frequency dependent. For macroscopic lines such dispersion is usually limited to frequencies below about 10^3 Hz, but with the very thin dielectric of the example line dispersion exists even up to 10^{13} Hz.

The dispersionless behavior of the superconducting stripline is remarkable in that it occurs in spite of significant field penetration into the conductors. The frequency independence of ν_ϕ occurs because at frequencies much less than the gap $\sigma_1 \ll \sigma_2$ and $\sigma_2 \propto 1/\omega$. These conditions make the depth of field penetration frequency independent.

As with attenuation, the phase velocity predicted by the two theories differs markedly near the gap frequency. In the Mattis-Bardeen theory the line becomes dispersive for frequencies somewhat below the gap. In this frequency range the phase velocity at temperatures low enough that $\sigma_1 \ll \sigma_2$ is given by

$$\nu_\phi = \frac{1}{(\epsilon\epsilon_0\mu_0)^{1/2}}\left(1+\frac{\coth[d_a(\mu_0\omega\sigma_{2a})^{1/2}]}{s(\mu_0\omega\sigma_{2a})^{1/2}} + \frac{\coth[d_b(\mu_0\omega\sigma_{2b})^{1/2}]}{s(\mu_0\omega\sigma_{2b})^{1/2}}\right)^{-1/2},$$

$$T \ll T_c, \quad \omega \leq \frac{2\Delta_a}{\hbar}, \frac{2\Delta_b}{\hbar}. \tag{3.6}$$

In practice Eq. (3.6) is accurate even for a reduced temperature of 0.5. From this equation we see that the line is dispersionless as long as $\sigma_2 \propto 1/\omega$. However, at frequencies just below the gap frequency σ_2 begins to deviate from a $1/\omega$ dependence and the line becomes dispersive. At frequencies above the gap σ_1 becomes larger than σ_2 and the phase velocity rapidly approaches that of a normal line. In contrast, the two-fluid model predicts a dispersionless line at frequencies considerably higher than the gap. At sufficiently high frequencies, however, σ_1 and σ_2 become comparable and the two-fluid model also predicts dispersion.

IV. PICOSECOND PULSES

To study the propagation of picosecond pulses we consider a Gaussian pulse of the form

$$V(0,t) = V_0 \exp(-t^2/2\tau^2), \tag{4.1}$$

where τ is the standard deviation and the full width at half-maximum is 2.35τ. Taking the Fourier transform obtains

$$V(0,\omega) = (2\pi)^{1/2}\tau V_0 \exp(-\tfrac{1}{2}\omega^2\tau^2), \tag{4.2}$$

so that the frequency spectrum is also Gaussian. To characterize the bandwidth of the pulse we define ν_{99} such that 99% of the pulse energy is contained in frequencies less than ν_{99}.

$$\nu_{99} = 0.29/\tau. \tag{4.3}$$

Solving Eq. (2.1) for the voltage at a distance L along the line we obtain

$$V(L,\omega) = \exp(-\gamma L)V(0,\omega),$$

$$V(L,t) = (2/\pi)^{1/2}\tau V_0 \int_0^\infty d\omega \exp[-(\alpha L + \tfrac{1}{2}\omega^2\tau^2)] \times \cos(\omega t - \beta L). \tag{4.5}$$

In Figs. 6 and 7 we show the result of numerical evaluation of the above integral using the Mattis-Bardeen result for α and β. Each frame is a superposition of simulated oscilloscope traces recording the computed shape of a pulse at several distances L along the stripline. For each trace the time origin has been shifted by an amount.

$$t_L = L/v_\phi(\omega = 0), \tag{4.6}$$

so that a pulse composed entirely of low frequencies would be centered at the time origin. Each trace is labeled by the energy of the pulse E relative to its original energy.

$$E = (1/\pi^{1/2}\tau V_0^2)\int_{-\infty}^{\infty} V^2(L,t)\,dt. \tag{4.7}$$

The three frames of Fig. 6 show the history of pulses with $\tau = 1.0$, 0.5, and 0.2 ps for the example stripline at 1.0 K. For the 1.0- and 0.5-ps pulses ν_{99} is below the energy-gap frequency so that the severe attenuation expected for frequencies above the gap is not

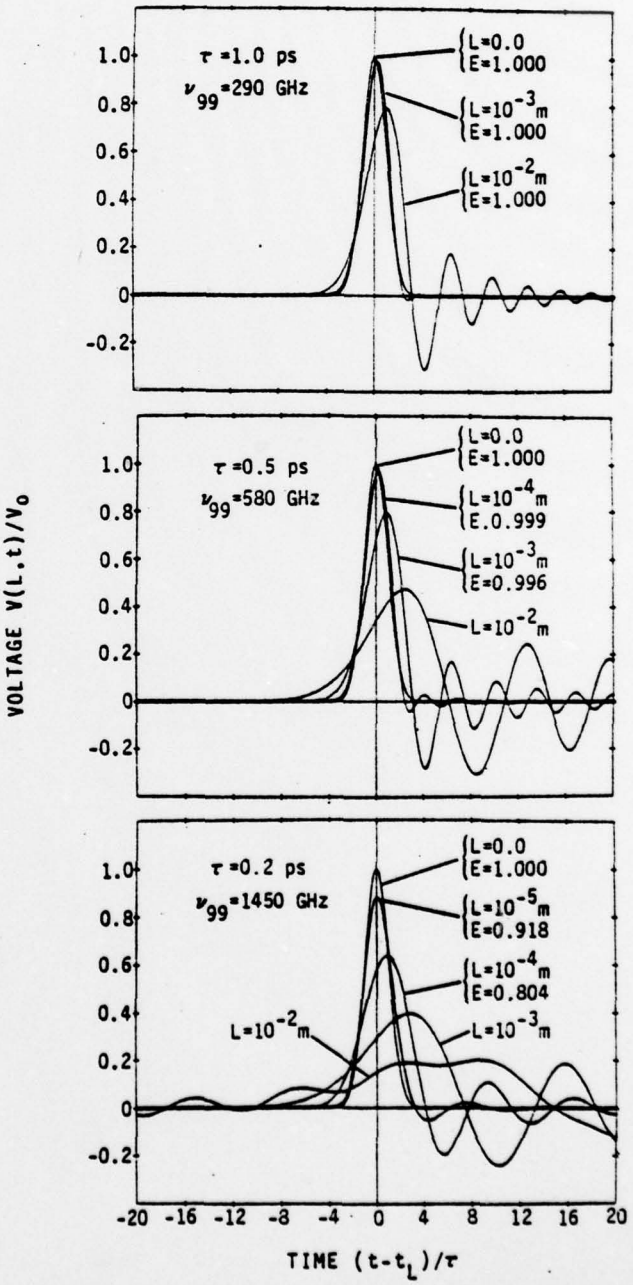

FIG. 6. Propagation of Gaussian pulses for the example line at 1.0 K. The low-frequency phase velocity is 3.16×10^7 m/s so that the delay time t_L is 317 ps for $L = 10^{-2}$ m.

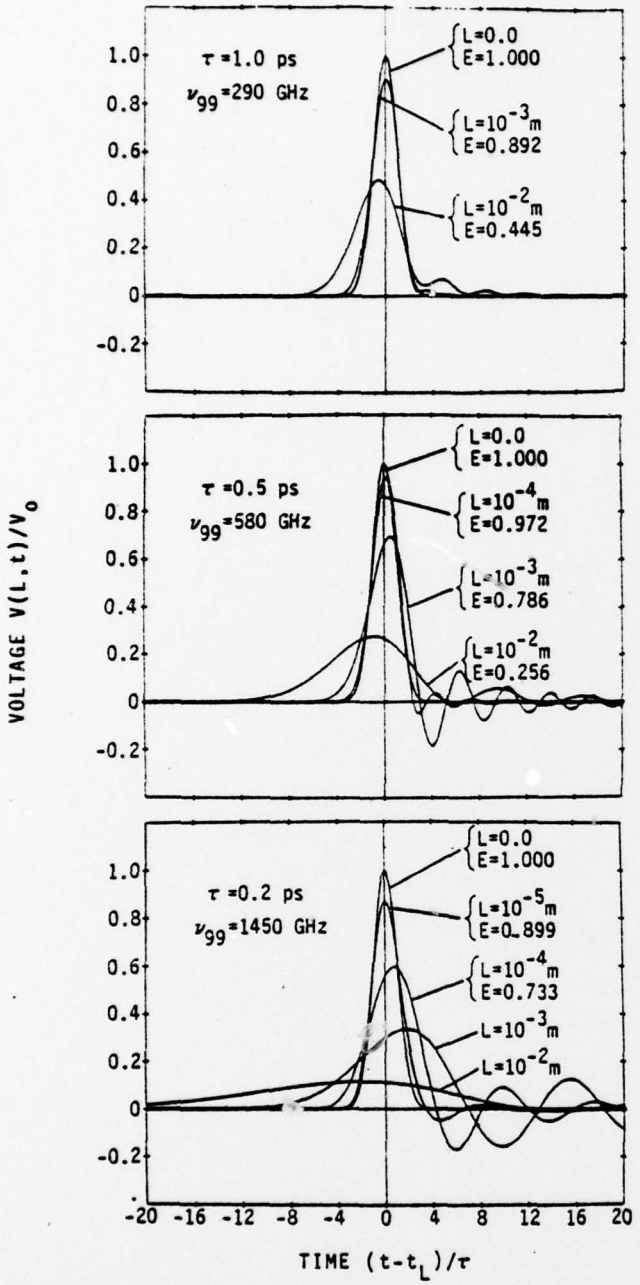

FIG. 7. Propagation of Gaussian pulses for the example line at 4.2 K. The low-frequency phase velocity is 3.09×10^7 m/s so that t_L is 323 ps for $L=10^{-2}$ m.

important. After propagating 1 mm the 0.5-ps pulse still includes 99.6% of its original energy. In spite of this low attenuation the pulses become distorted after propagating relatively short distances. This distortion can be traced to the dispersion evident in Fig. 4. The sharp drop in ν_ϕ for frequencies approaching the gap frequency accounts for the long oscillatory tails developed by the pulses. Considering the 0.5-ps pulse after it has traveled 1 mm, we see that the oscillatory tail has a frequency of about 500 GHz. From Fig. 4 we can calculate that after traveling 1 mm the 500-GHz component has fallen behind the low frequencies by 0.9 ps or about a half-cycle, making it especially evident in the tail.

For the 0.2-ps pulse $\nu_{99}=1450$ GHz and about one-fourth of the pulse energy falls above the energy gap. Here we see that attenuation has become significant, the pulse retaining only about 80% of its original energy after propagating 0.1 mm. This attenuation also contributes to distortion of the pulse since all frequencies are not equally attenuated. A long section of line acts like a low-pass filter with a sharp cutoff at the gap frequency of the Pb alloy. Thus, after propagating 1 cm the 0.2-ps pulses shows oscillations at about 660 GHz, the cutoff frequency.

In Fig. 7 we show results similar to those of Fig. 6 but for a temperature of 4.2 K. At 4.2 K, attenuation at frequencies below the gap becomes significant. Strangely enough, the presence of this attenuation tends to produce the degradation in shape of the 1.0- and 0.5-ps pulses, making their oscillatory tails smaller than at 1.0 K. The reason is that at 4.2 K the high-frequency components which travel at a smaller velocity and cause the tails are more strongly attenuated than the lower frequencies.

For the 0.2-ps pulse a sufficient fraction of the energy falls above the gap frequency where attenuation and dispersion do not depend on temperature, making the difference between the 1.0- and 4.2-K striplines less distinct. However, because the 4.2-K does not act as a filter with a sharp cutoff frequency we do not see oscillations at the Pb-alloy gap frequency as at 1.0 K.

For the example line considered here one concludes that pulses with full widths of 2.35 and 1.18 ps can propagate without significant distortion for distances of 1000 and 100 μm, respectively. Because such distances are relatively long on a microcircuit, propagation will not be a limiting factor in creating and detecting picosecond pulses using Josephson-junction microcircuits. A pulse with a full width of 0.47 ps, however, can propagate no more than about 10 μm without severe distortion, making such pulses difficult to utilize.

So far we have restricted attention to a specific example line. One might question whether the high-frequency limitations of this line might be significantly altered by using different materials or dimensions. In principle, the easiest way to increase the frequency range over which the line is dispersionless would be to use superconductors with larger energy gaps. Once the superconductors are specified, however, one might hope to reduce the dispersion at frequencies just below the gap. In this frequency range Eq. (3.6) is valid and we see from it that the dispersive terms can be made small by choosing the dielectric and superconductor thicknesses, s and d, to be large. For the example line the superconductors are thick enough that the coth factors are nearly unity and further increasing their thickness has little effect. However, if the dielectric thickness of the example line is increased by a factor of 10, the 0.5-ps pulse travels about 10 times farther without severe distortion. Thus, while the energy gap represents an upper frequency limit, the dispersive behavior of the line at lower frequencies can be partially eliminated by choosing large conductor and dielectric thicknesses.

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