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Final Technical Report
July 1978

SYSTEM TIMING AND SYNCHRONIZATION

Peter Alexander
James W. Graham
David J. Miller

CNR, Inc.

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In the planned DCS digital network, the ability to coordinate clocks placed at geographically separated nodes will be of critical importance. Aside from the characteristics of the clocks themselves, medium and link equipment parameters play dominant roles in determining performance for the system. The emphasis in this report is on troposcatter and line of sight link parameters and their relationship to network clock synchronization. This report includes analysis and discussion of the important physical effects in troposcatter —> next page (Cont'd)

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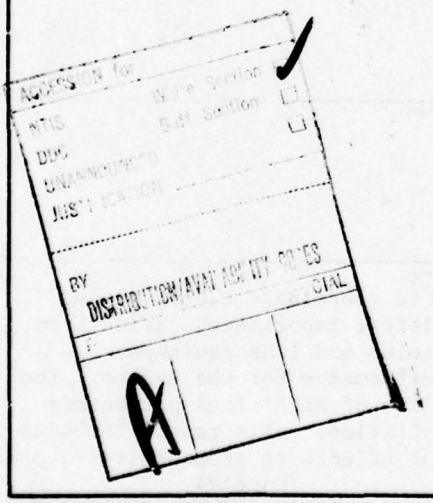
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propagation, and a description of experiments and data acquired during a recent measurement program designed to establish a better understanding of the relevant troposcatter and line of sight medium and equipment effects.



PREFACE

This final report, covering the period July 1976 to January 1978, was prepared by CNR, Inc., of Needham, Mass., under Contract No. F30602-76-C-0347 with Rome Air Development Center, Griffiss Air Force Base, New York.

The experiment concept formulation, clock control design and data analysis aspects were carried out by Dr. P. Alexander, who was also responsible for overall project management. Mr. J. W. Graham, who performed the difficult tasks of field engineering and data reduction, can be credited with the success of the experimental program, while Mr. D. J. Miller designed and developed all of the special purpose microprocessor and clock control instrumentation circuits.

The authors wish to acknowledge the enthusiastic support and assistance given by the RADC Project Engineer, Mr. W. Cote. Invaluable assistance was also given by the RADC Site Supervisory Engineers, Messrs. W. Schneider and D. Mangold. Many other RADC personnel, including Messrs. W. Voss, J. Pritchard, J. Krause, L. Sues, and E. Miceli also made substantial contributions to the successful operation of field equipment, and the authors thank them for their support.

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EVALUATION

Contract F30602-76-C-0347 - Final Report - System Timing and Synchronization, CNR, Inc.

This report represents the completion of the first major goal of Task 215704 to develop the timing subsystem for the future, synchronous digital DCS. This report documents the experimental field measurement program results which were established to measure time transfer functions over troposcatter and line-of-sight transmission media.

The data reported herein was obtained to verify theoretical assumptions made in various timing technique studies and to provide the necessary design criteria to continue the development of experimental timing subsystems. Considerable resources and effort were expended to obtain highly accurate geodetic surveys and unique absolute path delay information and statistics. This data should be valuable to other researchers in various technology areas, such as propagation modelling, surveying, communication equipment design and range determination at the frequencies involved. The clock control experiments and other data analyses provided herein provide the necessary design criteria to approach the experimental timing subsystem development phases with confidence.

Walter E. Cote'

WALTER E. COTE'
Project Engineer

SECTION 1

INTRODUCTION

This report is intended to support the long-term objective of digital signal synchronization within the Defense Communications System (DCS). The work described in this document covers an 18-month program consisting of analysis, experimentation, and data reduction. In concert with the results derived in earlier and parallel studies, this effort should provide the fundamental design base for future development of a DCS timing subsystem which will distribute coordinated timing signals at each node.

The planned DCS digital transmission network can be visualized in its most elementary form as a collection of nodes interconnected by radio links or cascades of links. Bit streams originating from geographically-separated sources enter the node and typically require multiplexing for retransmission to a common destination node. While incoming data signals may be conveniently buffered to smooth out the path length variations, drift between originating node clocks, if unchecked, will eventually result in buffer depletion or overflow.

In the past few years, various methods of avoiding or minimizing these undesirable phenomena have been proposed, including independent highly stable atomic clocks [1.1], mutual frequency averaging [1.2], hierarchical master/slave [1.3], and self-organizing master/slave [1.4]. More recently, consideration has been given to the use of network facilities for system-wide transfer of a time reference [1.5], and theoretical models have been used to predict relationships between time transfer accuracy and link parameters. To satisfy normal communication requirements, relative time synchronization of the nodes is sufficient, i.e., the node clocks need not be phased identically as long as their mutual average frequency offsets are zero. On the other hand, transfer of a time reference throughout a network is equivalent to the requirement that node clocks be synchronized with zero phase offset. However, the additional hardware required for time reference transfer does not appear to be significant for a production timing subsystem model, and

the benefits of a systemwide time reference certainly seem to justify further examination in terms of performance and feasibility.

The DCS network involves a large number of links and nodes with various categories of transmission media, including line-of-sight microwave (LOS), troposcatter (TROPO), satellite, and cable. The variety of transmission equipment that is available now, or planned as part of the all-digital network, makes a complete and comprehensive evaluation of system performance difficult; therefore, an emphasis in the experimental work reported on here has been toward a separation of propagation and equipment effects. Furthermore, the scope of the effort was limited to measurement of TROPO and LOS links because of equipment and site availability. Of these two classes of transmission medium, troposcatter involves a greater degree of variability in its parameters, making its characterization and measurement substantially more difficult. Accordingly, a more complete treatment has been given in this report on the subject of time transfer via TROPO links, as compared with the more widely understood LOS application.

The organization of the report is as follows. In order to gain an understanding of the overall network synchronization problems and alternatives, we review in Section 2 network timing techniques, the interaction of different network functions, such as time transfer and communications, and finally address the survivability and security questions.

Sections 3 and 4 are concerned more with the experimental program carried out to determine the range of variation of certain parameters. The first of these, Section 3, gives details concerning the experimental configurations and objectives, while Section 4 presents the results obtained in these tests. Included are measurements of one-way path delay for troposcatter and line-of-sight links, modem and radio static delay as a function of various conditions, and clock alignment for a master/slave clock control experiment.

The experimental data contained in Section 4, along with analyses of equipment characteristics (Appendices A and B) provide a firm base for the design of the node timing subsystem. In Section 5 we have run through the exercise of designing a timing subsystem. Some of this material is conceptual in nature, whereas other portions correspond to the clock control

servo that was implemented in the field tests. The subject of interfacing with other DCS network subsystems is also examined in detail in Section 5.

Section 6 contains a summary and recommendations for the timing subsystem design. Appendix C is a very concise tabulation of survey data acquired during the test program, while Appendix D is a summary of the equipment layout for the Youngstown and Verona sites, including cable and waveguide lengths and interconnection details. Finally, Appendix E contains some sample delay power spectra measured on the Youngstown-Verona troposcatter link.

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SECTION 2

SYNCHRONIZATION OF TIMING NETWORKS

Certain aspects of the timing subsystem design must be addressed within the context of the complete network, whereas for others the design issues do not extend beyond the links terminating at a given node. We first examine the network synchronization concepts and then, in Section 5, follow this up with a discussion of link synchronization and control.

2.1 Network Timing Considerations

A digital transmission network can be visualized in its most elementary form as a collection of nodes interconnected by radio links or cascades of links. Bit streams originating from geographically-separated sources enter the node and typically require multiplexing for retransmission to a common destination node. While incoming data signals may be conveniently buffered to smooth out the path length variations, drift between originating node clocks, if unchecked, will eventually result in buffer depletion or overflow.

A division can be made between two types of network synchronization – asynchronous and synchronous. Generally speaking, each node in the system will have its own clock which is used for data transmission out of the node, while the incoming data timing may be associated with the originating node. The node clocks can also be slaved to some other timing source, for example, by means of network time dissemination; or by averaging all of the incoming data rates to produce a frequency control voltage for the node clock. Alternatively, the node clock may be free-running with phase unrelated to other nodal clocks.

In the asynchronous network, each node clock is assumed free-running and not of particularly high stability. At individual nodes, the receivers lock onto incoming data to produce a set of incoming clock signals. The reconstituted bit stream to be transmitted is clocked out at a rate high enough above the incoming rates, so that differences in the incoming/outgoing rates can be accommodated by bit stuffing or spilling (i.e., padding of the outgoing bit stream as required).

In a synchronous configuration, the incoming data enters an elastic store at a rate determined by the receiver tracking loop output, but is clocked out of the store at a rate determined by the local node clock. Differences are accommodated as long as the buffer capacity is not exceeded, and data is transmitted out of the node without the need for pulse stuffing. Although not classified as synchronous, the independent clock approach follows this methodology, and accommodates the inevitable buffer overflows by means of periodic buffer resets.

2.1.1 Interaction of Timing and Communications Functions

The input/output node components for a synchronous network node are shown in Figure 2.1. For the output case indicated in Figure 2.1, the node clock is synchronous with the transmitted data, and it is simply a matter of multiplexing the bit streams together with the appropriate control and framing overhead bits. Incoming data is extracted from the analog receiver output by the modem, passed through the decryption device, and entered into the elastic store at a rate determined by the bit tracking loop. With correct frame synchronization and sufficient buffer capacity, the data bits can be clocked out of the store by the local clock and demultiplexed to the digroup level. The link control processor is responsible for the anticipation and correction of difficulties which may arise in the operations shown, such as loss of bit count integrity (BCI) resulting from buffer overflow/underflow, or loss of frame sync.

It should be evident from this discussion that, as far as maintaining the network data communications capability is concerned, the objective is simply to avoid buffer overflow or depletion for all of the terminated links at any given node. This can be achieved by periodic adjustment of network clock frequencies in a prearranged manner. Moreover, the incremental cost of buffer capacity is quite low, and buffer lengths of 1024 and 2048 bits are quite economical once the basic design has been accomplished. With the availability of low cost buffers, the network synchronization problem is simplified as far as the data communications requirements are concerned.

However, the availability of a world-wide high-speed digital network provides potential for other services less directly associated with the communications functions described above. In particular, network time transfers would be a valuable asset on a world-wide scale, and would also provide

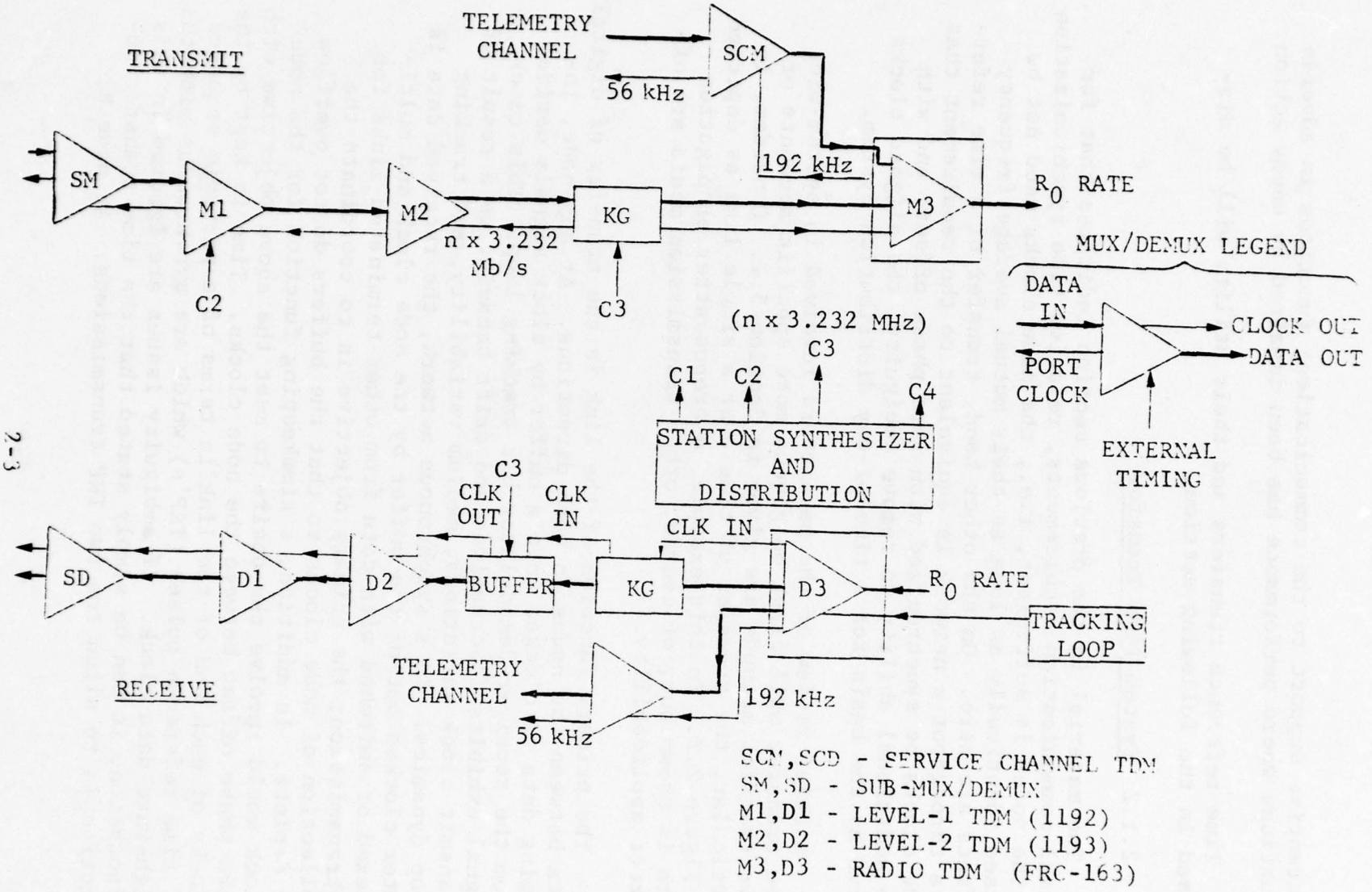


Figure 2.1 Illustration of Station Timing Distribution for Synchronous Network

substantive support to the communications functions in adverse situations where performance has been impaired by enemy action.

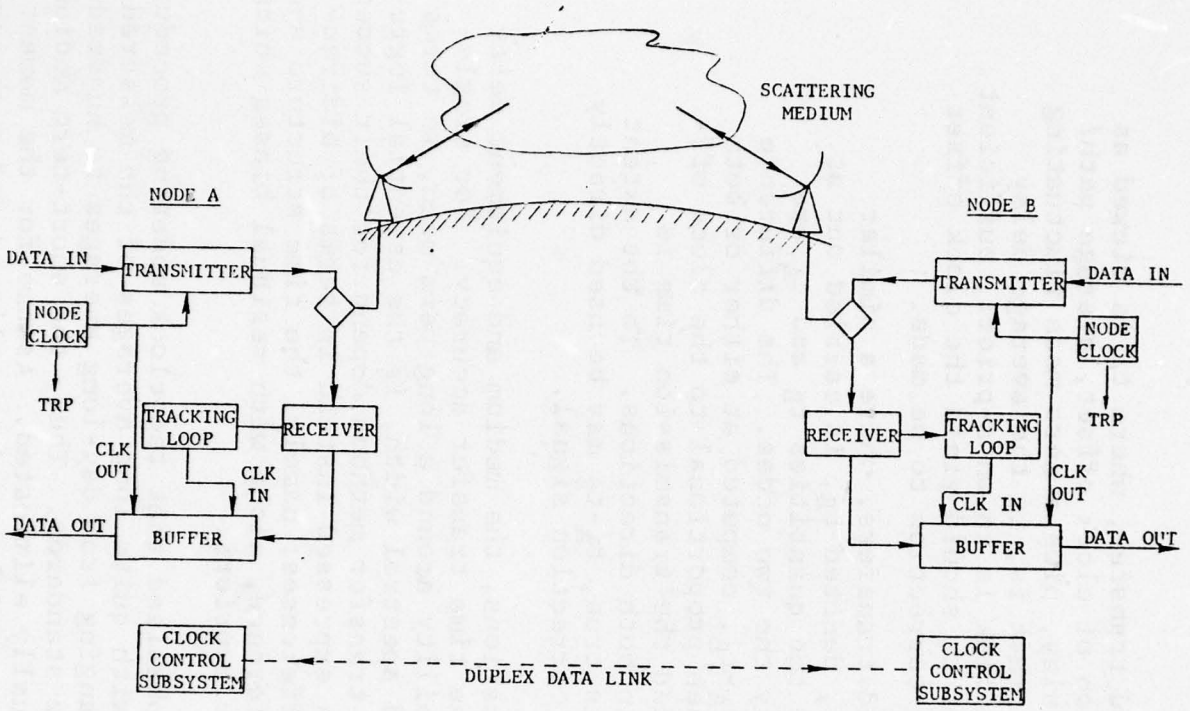
Time reference transfers and their utility will be discussed in the following section.

2.1.2 System Time Transfer

The material in the previous section indicates that for normal communication requirements, relative time synchronization of the nodes is sufficient, i.e., the node clocks need not be phased identically as long as their mutual average frequency offsets are zero. On the other hand, transfer of a time reference throughout a network is equivalent to the requirement that node clocks be synchronized with zero phase offset; and with the additional ability to remove ambiguity, the aligned clocks serve as the basis for a time-of-day distribution system.

A brief review of the parameters involved in system-wide time transfer will first be given; more specific accounts of time transfer methods are given in Section 5.1. Consider, in particular, the transfer of time over a single link as depicted in Figure 2.2. In this example, a troposcatter propagation path is shown but, of course, other transmission media are of direct applicability.

The primary function of the link is the transfer of digital data between the nodes in both directions. At any node, incoming data is clocked into a buffer by clock signals derived from the receiver-demodulator bit tracking loop. This clock signal exhibits fluctuations and drift behavior as a result of transmit clock variations, medium variability, and tracking loop dynamics. In a synchronous network, the received data is later clocked out of the buffer by the node clock and multiplexed or switched with data from other terminated links for retransmission; the primary objective is to coordinate the collection of node clocks so that the buffers do not overflow or deplete. In addition, a timekeeping function for the node clock would involve the desire to meet the above objective with zero phase offset between the node clocks. Time is kept by the clocks at each end of the link in terms of a periodic sequence of time reference pulses (TRP's) which are synchronous with the high-rate data clock. If ambiguity issues are ignored in this discussion, it can be simply stated that the time transfer objective is to align the two TRP transmissions. At node B,



TRP = CONCEPTUAL TIME REFERENCE PULSE

Figure 2.2 Block Diagram of a Digital Troposcatter Link

this is achieved by comparing the arrival time of a pulse transmitted from node A with the locally-generated pulse time, i.e., the node B clock pulse. Time transfer from A to B can then be implemented using this measurement, denoted t_A, in one of two ways:

(1) Single-ended transfer, where t_A is viewed as a combination of clock offset, average path/equipment delay, plus a zero mean fluctuating component. That is, if the average delay through the link is known a-priori, sufficient averaging of t_A should yield the clock offset and allow a correction to be made.

(2) Double-ended transfers, where a similar measurement, denoted t_B, is carried out at node A, and the quantities t_B and t_A are exchanged by the two nodes. The difference parameter t_A-t_B, computed at either or both ends, is then proportional to the clock offset, provided the transmission time is identical in both directions. To the extent that this is true, t_A-t_B may be used directly as a clock correction signal.

In both of these situations, the medium and equipment delay variations control the time transfer accuracy. For single-ended systems, variability around a long-term mean, in terms of both magnitude and spectral width, is the essential ingredient. Double-ended transfer methods depend for their success on similar parameters expressed instead in terms of bidirectional path delay differences; namely, the time structure and magnitude of the difference, along with residual biases which are not accounted for a-priori.

It should be emphasized that the clock updating procedure will be carried out with quite long averages of the measured arrival time data, ranging from day-long averages to hundreds of seconds for quartz standards. Thus, the short-term medium effects will be virtually eliminated. Assume for the moment, then, that the clocks at either end are aligned and much more stable than the incoming TRP signal which is perturbed on an instantaneous basis by the medium fluctuations. With this situation, the path delay itself can be established and, if variable, tracked in time. In the event of link disruptions,

the demultiplexers and decryption units may lose sync, and the availability of a network time reference at the node provides valuable support for the reframing operation.

2.2 Network Synchronization Techniques

Many of the system and link control techniques proposed have common features. It is our intention in this section to summarize the important parameters and issues for a representative number of the suggested candidates.

It will be assumed that the reader is reasonably conversant with each method, thereby allowing our presentation to be more concise. References to the many relevant synchronization studies that have been funded in the past are provided for the reader who needs more background. For a direct comparison of the alternative network timing and synchronization technique, the reader is referred to [2.23]. Despite the abundance of information available on the various network synchronization techniques, a formal classification scheme does not seem to have evolved. In Section 2.2.1 we therefore present a time/frequency hierarchy which serves to illustrate and distinguish between the different levels of network synchronization.

2.2.1 Time/Frequency Synchronization Hierarchy

The classification scheme outlined here serves the purpose of defining the various synchronization conditions under which a system may operate.

In Table 2-1, we have classified five levels of network synchronization, beginning with the lowest level of independent uncoordinated clocks and progressing through to the highest level, which involves universal time dissemination. There are two main groups: one collection lumped under "relative time synchronization", and a second called "precise time dissemination". The former group represents techniques which are sufficient to satisfy network synchronization for communications purposes, while the latter techniques offer the enhancement of a precise time reference at every node. Further subdivisions are possible depending on the detailed node and link distribution scheme.

In Figure 2.3 we have attempted to further refine the generic time and frequency synchronization technique categorization. The distinction between precise time and relative time

TABLE 2-1

TIME/FREQUENCY SYNCHRONIZATION HIERARCHY

Level 1:	Independent Node Clocks No coordination	Relative Time Synchronization
Level 2:	Frequency Synchronization All clocks at same average frequency; system insensitive to phase steps	
Level 3:	Relative Time Synchronization Coordination of time reference at each node with incoming time reference events	
Level 4:	Network Time Reference Sync All clocks in network synchronized to internal network time	Precise Time Dissemination
Level 5:	Time Synchronization with an External Reference (e.g., Universal Time)	

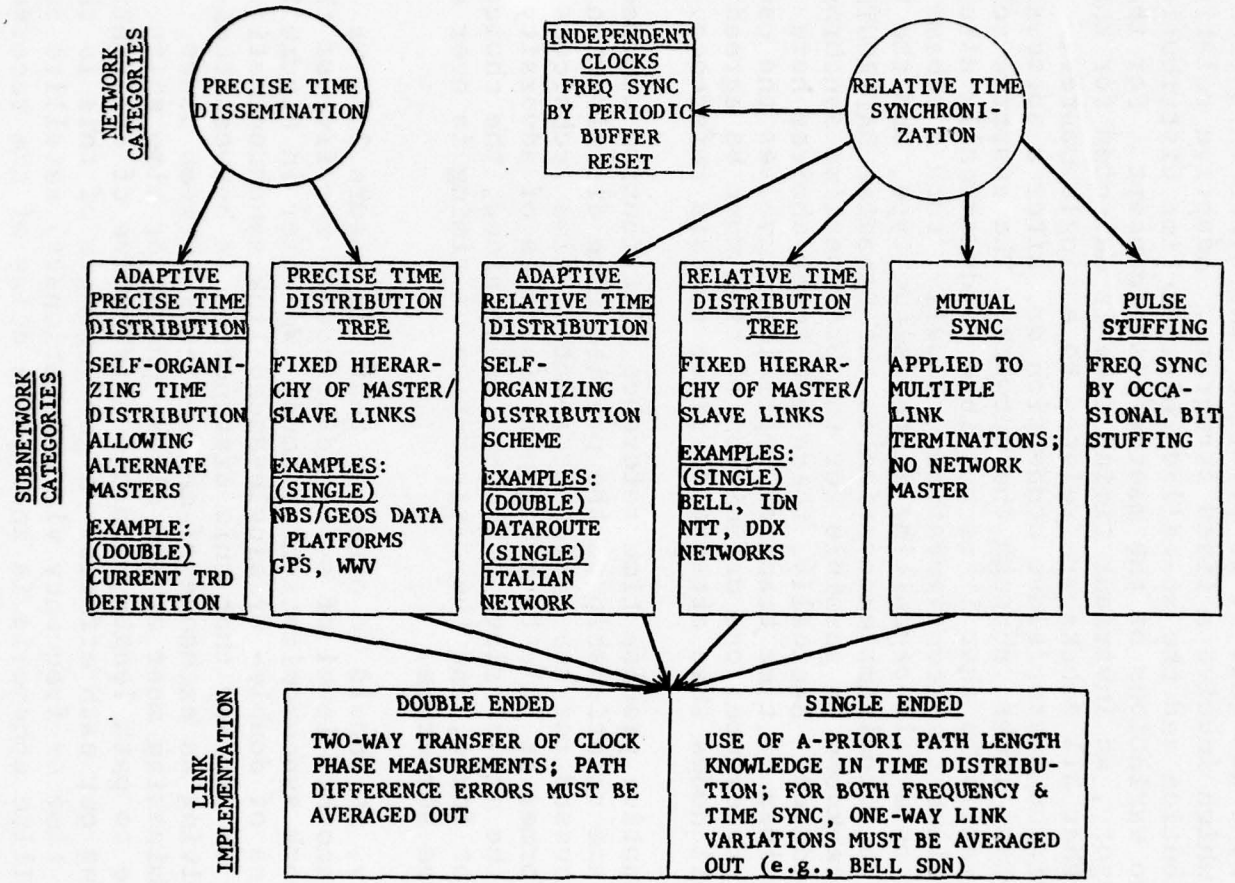


Figure 2.3 Categorization of Network Synchronization Techniques

is in the sense previously discussed; the relative time signals are lacking in ambiguity to the resolution desired, e.g., years, days, seconds, or cycles. Independent clocks, pulse stuffing, and mutual sync all qualify as relative time synchronization techniques which involve a fixed structure. Adaptive relative time distribution and the so-called relative time distribution tree are two variations of the master/slave concept. For the latter category, an invariant timing tree is selected for the network so that all clocks are related to a single master, either by direct master/slave connection or, after a succession of master/slave links, through the network. The adaptive scheme differs primarily in that it is possible to dynamically alter the master/slave tree configuration. Usually, such a scheme is categorized as a self-organizing master/slave type, and the best example of an actual implementation is the Canadian DATAROUTE. A similar breakdown is possible for the precise time synchronization candidates. Basically, there are fewer choices here because the idea of time transfer implicitly involves the use of a master reference; one definition of time must be agreed upon, and all nodes then attempt to slave to this reference.

The adaptive precise time reference distribution approach bears the same relationship to the precise time distribution tree as discussed for the analogous relative time techniques, i.e., the former is able to reorganize in times of adversity so that while the master/slave structure is retained, the choice of master is not fixed, and the distribution of timing is over a variable tree structure.

Finally, it should be observed that, in Figure 2.3, we have shown another level of system distinction for five of the listed network synchronization schemes. We refer in Figure 2.3 to the choice of double- or single-ended link synchronization. In summary, we can say that this distinction is between techniques involving an exchange of measurements between nodes, thereby eliminating most of the clock, phase, or time shift attributable to path length, and the alternative of calibrating and averaging out path effects. A good example of this is the transfer of time or frequency via a (stationary) satellite path. If the satellite ephemeris is known, the delay of the received signal relative to the system reference clock can be computed and subtracted out to form a clock error. With two-way transmissions and exchange of clock error signals via a data link, path length changes can be accounted for without such detailed calculations.

We now proceed to describe the four synchronization schemes of primary interest. Figure 2.4 illustrates a simple five-node network which will be used as specific reference in the discussion.

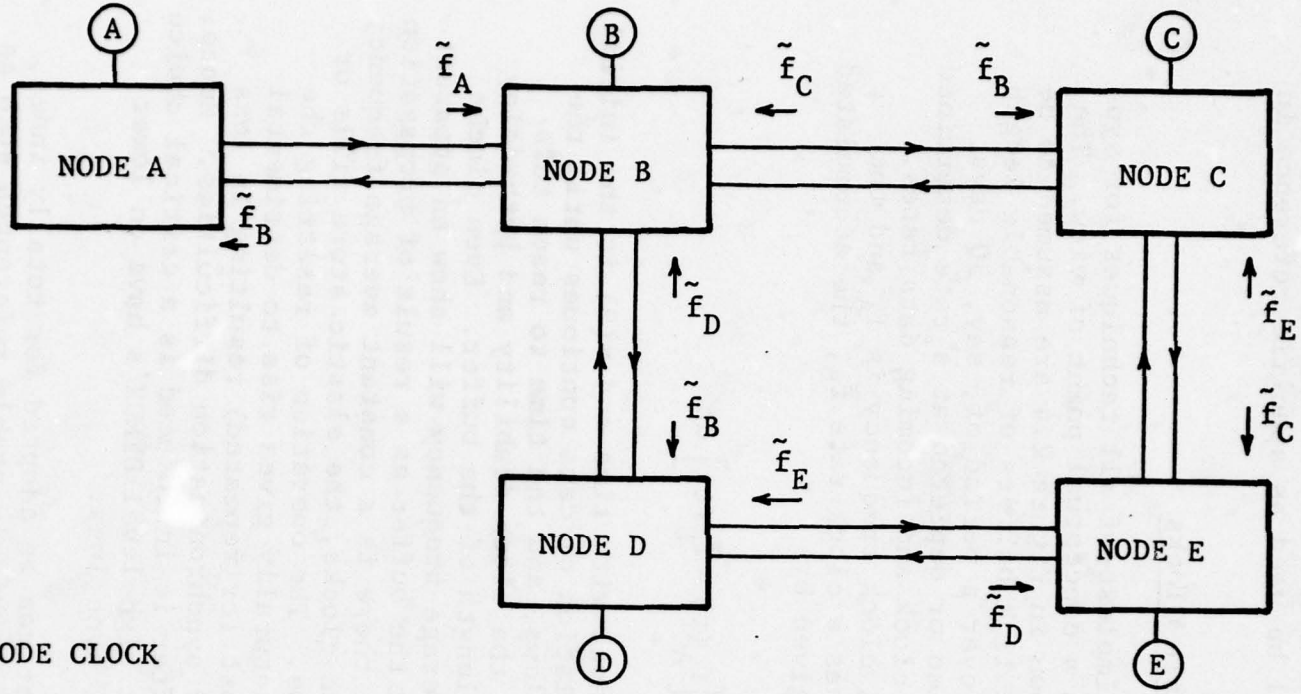
2.2.2 Independent Stable Clocks

This constitutes the simplest of all techniques for synchronization, at least from a conceptual point of view. The individual nodal clocks shown in Figure 2.4 are assumed to be sufficiently stable so that link buffers of reasonable length can maintain bit integrity over a period of, say, 50 days. Clearly, the buffer is filled or depleted at a rate determined by the difference in nodal clock and incoming data rates. Specifically, if the node A clock frequency is f_A and the incoming data from node B has a clock rate $\tilde{f}_B$, the accumulated buffer level (in bits) is given by:

$$x(t) = x(0) + \int_0^t \left[f_A(t) - \tilde{f}_B(t) \right] dt$$

where x(t) is the buffer level with time and x(0) is the initial value of x(t). The accumulation of data continues until the buffer overflows or underflows, and the time to reach this condition is determined by the clock stability and path delay variation, as well as the length of the buffer. Even clocks with the same long-term average frequency will show an apparent instantaneous difference at the buffer as a result of propagation delay variations, and when there is a constant average frequency offset between the two node clocks, the elastic store fills or depletes linearly with time. The operation of resetting the buffer when it overflows naturally gives rise to detrimental system effects; data is lost (or repeated) resulting in loss of bit integrity (BCI) and synchronization difficulties. Hence, the level at which the buffer is introduced is a critical choice given the BCI effects that high-level DEMUX's have on lower level units at the time of sync loss.

The best approach that can be adopted for totally independent node clocks is to use highly stable references such as atomic clocks, with a large enough buffer to maintain BCI over a predetermined period. After loss of BCI, the system must be reinitialized. An overview of this method of system synchronization can be found in [2.1].



A NODE CLOCK

A NETWORK NODE

DUPLEX LINKS (E.G., MULTIPLE LOS/TROPO HOPS)

$\tilde{f}_A$, $\tilde{f}_B$, etc., DENOTE DERIVED CLOCK SIGNALS FROM ANOTHER NODE

Figure 2.4 Reference Multinode Network

There are several types of frequency standards in common use today, including the cesium atomic beam resonator, the rubidium gas cell resonator, and the quartz crystal oscillator. The first of these is a primary standard giving good long-term stability without requiring any other reference for calibration. The last two are designated secondary standards, meaning that calibration of some kind is necessary at intervals depending on the desired accuracy. The two mentioned above have the advantage of compactness and portability in contrast to cesium standard. The three types of frequency standards are compared in Table 2-2 (from [2.2]).

2.2.3 Mutual Synchronization by Frequency Averaging

The technique of mutual synchronization is one in which each node has a clock that may be adjusted in frequency so as to reduce the timing error between itself and some average of the rest of the network. The general approach calls for a weighted sum of phase errors for all incoming data clocks to be used as a control signal to pull the node clock frequency. The network therefore attempts to reach a stable frequency of operation using the notions of feedback control. The method has the advantage that removal of any one node from the network still leaves the system in synchronism, although in this situation and others, a transient disturbance will propagate around the network until a stable equilibrium frequency has been reached.

Earlier studies of this type of network synchronization favored an analog type of implementation, at least for the purposes of analysis. These include, for example, [2.1], [2.3], and [2.4] as well as earlier work at Bell Labs [2.5] - [2.7] and Nippon Telegraph and Telephone [2.8], [2.9].

The essence of these studies was that each node estimated the phase error between all incoming data streams and its own clock, and combined these estimates to form a (VCO) clock control signal. In terms of Figure 2.4, for example, node B would compute

$$x_{BA} = \varphi_B - \tilde{\varphi}_A$$

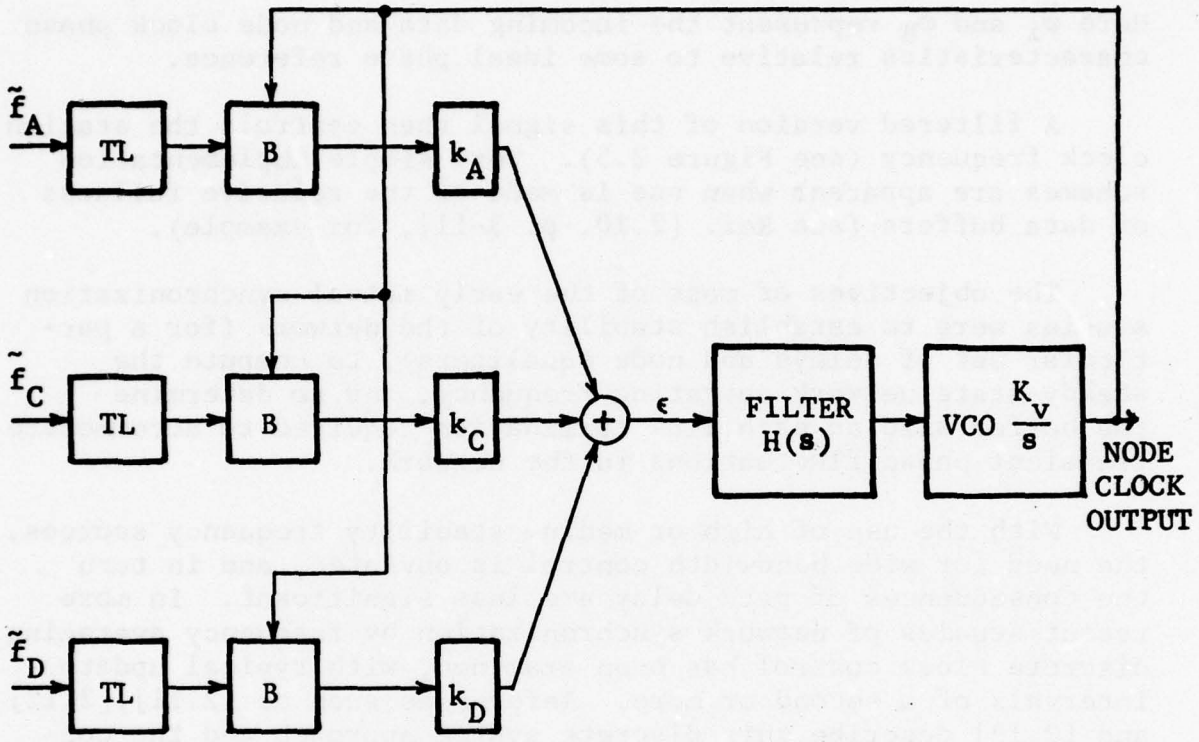
$$x_{BC} = \varphi_B - \tilde{\varphi}_C$$

$$x_{BD} = \varphi_B - \tilde{\varphi}_D$$

TABLE 2-2

COMPARISON OF FREQUENCY STANDARDS

Standard	Short-Term Stability		Long-Term Stability		
	1 sec	100 sec	Accuracy	Adjustment	Drift Rate
Cesium Atomic Beam Resonator	5×10^{-12}	10^{-12}	1×10^{-11}	7×10^{-13}	None
Rubidium Gas Cell Resonator	5×10^{-12}	5×10^{-13}	5×10^{-11}	2×10^{-12}	1×10^{-11} per month
Quartz Crystal Oscillator	10^{-11}	10^{-11}	--	--	5×10^{-10} per day



B = INPUT BUFFER PHASE DETECTOR

VCO = VOLTAGE CONTROLLED OSCILLATOR

TL = LINK TRACKING LOOP

Figure 2.5 Mutual Synchronization
(Node B of Figure 2.4)

and a composite error signal

$$\epsilon = k_A x_{BA} + k_C x_{BC} + k_D x_{BD}$$

Here $\tilde{\varphi}_i$ and φ_B represent the incoming data and node clock phase characteristics relative to some ideal phase reference.

A filtered version of this signal then controls the station clock frequency (see Figure 2.5). Very simple implementation schemes are apparent when use is made of the relative fullness of data buffers (see Ref. [2.10, p. 3-11], for example).

The objectives of most of the early mutual synchronization studies were to establish stability of the network (for a particular set of delays and node equalizers), to compute the steady-state network operating frequency, and to determine the buffer size at each link termination required to accommodate transient phase fluctuations in the network.

With the use of high or medium stability frequency sources, the need for wide bandwidth control is obviated, and in turn the consequences of path delay are less significant. In more recent studies of network synchronization by frequency averaging, discrete clock control has been examined, with typical update intervals of a second or more. References such as [2.11],[2.12], and [2.13] describe this discrete system approach and the conditions for stability. Most of the concepts embodied by the analog control system design carry over to the discrete system formulation, and once the linear discrete system equations are formulated, the considerable body of theory and computational methods for discrete systems can be called upon. Once again the important issues are final operating frequency, stability, and buffer lengths to accommodate transients.

2.2.4 Master/Slave Systems

Other methods of network synchronization that have been proposed which, like the frequency averaging approach, are not as demanding in terms of clock stability as the independent clock method, include fixed hierarchy master/slave and self-organizing master/slave techniques. The simple master/slave arrangement [2.14],[2.15] used, for example, in the Bell System and originally proposed for the DATRAN network, are examples of networks embracing the fixed master/slave timing distribution philosophy.

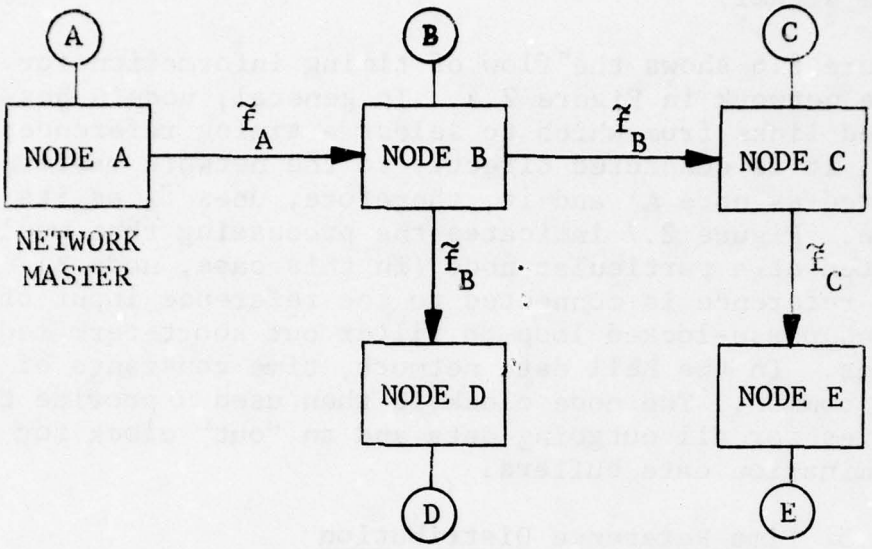
The key idea is that individual nodes take their timing from only one of the terminated links at that node in a prearranged way. The choice is made so that timing signals originating at the master clock are disseminated through the network via the most reliable links and handed on at each node in such a way that every node eventually receives a suitable reference signal.

Figure 2.6 shows the flow of timing information for the five-node network in Figure 2.4. In general, node B has three terminated links from which to select a timing reference; but, as shown, it is connected directly to the network master clock (designated as node A) and it, therefore, uses $\tilde{f}_A$ as its reference. Figure 2.7 indicates the processing that would be implemented at a particular node (in this case, node B). The selected reference is connected to the reference input of a narrowband phase-locked loop to filter out short-term medium variations. In the Bell data network, time constants of several days are common. The node clock is then used to provide transmit frequencies for all outgoing data and an "out" clock for the link termination data buffers.

2.2.5 Time Reference Distribution

In the Time Reference Distribution approach to network timing, individual node clocks are subjected to occasional correction using timing information being continually passed around the network from node to node [2.16]. In this regard, there are some similarities with the double-ended frequency averaging method touched on in Section 2.2.3, where linked nodes exchanged timing data via a service channel. However, the Time Reference Distribution system goes well beyond this concept. Because all of the node clocks are ranked in an order of increasing importance, the network has the capability of locking itself totally to the highest ranked clock currently in operation. This technique has been discussed for synchronization of the Western Union digital network [2.17] and the DATRAN network.

A similar and closely-related concept has been implemented in the Canadian DATAROUTE digital transmission scheme [2.18], [2.19] where it is referred to as the "Hierarchical Master/Slave Slave" method of synchronization. This approach to network synchronization will be outlined first, and the additional features embraced by the Time Reference Distribution concept will then be covered.



(A) NODE CLOCK

$\tilde{f}_i$ INCOMING TIMING REFERENCE
(SELECTED FROM THOSE AVAILABLE)

Figure 2.6 Master/Slave Network showing Flow of Timing References

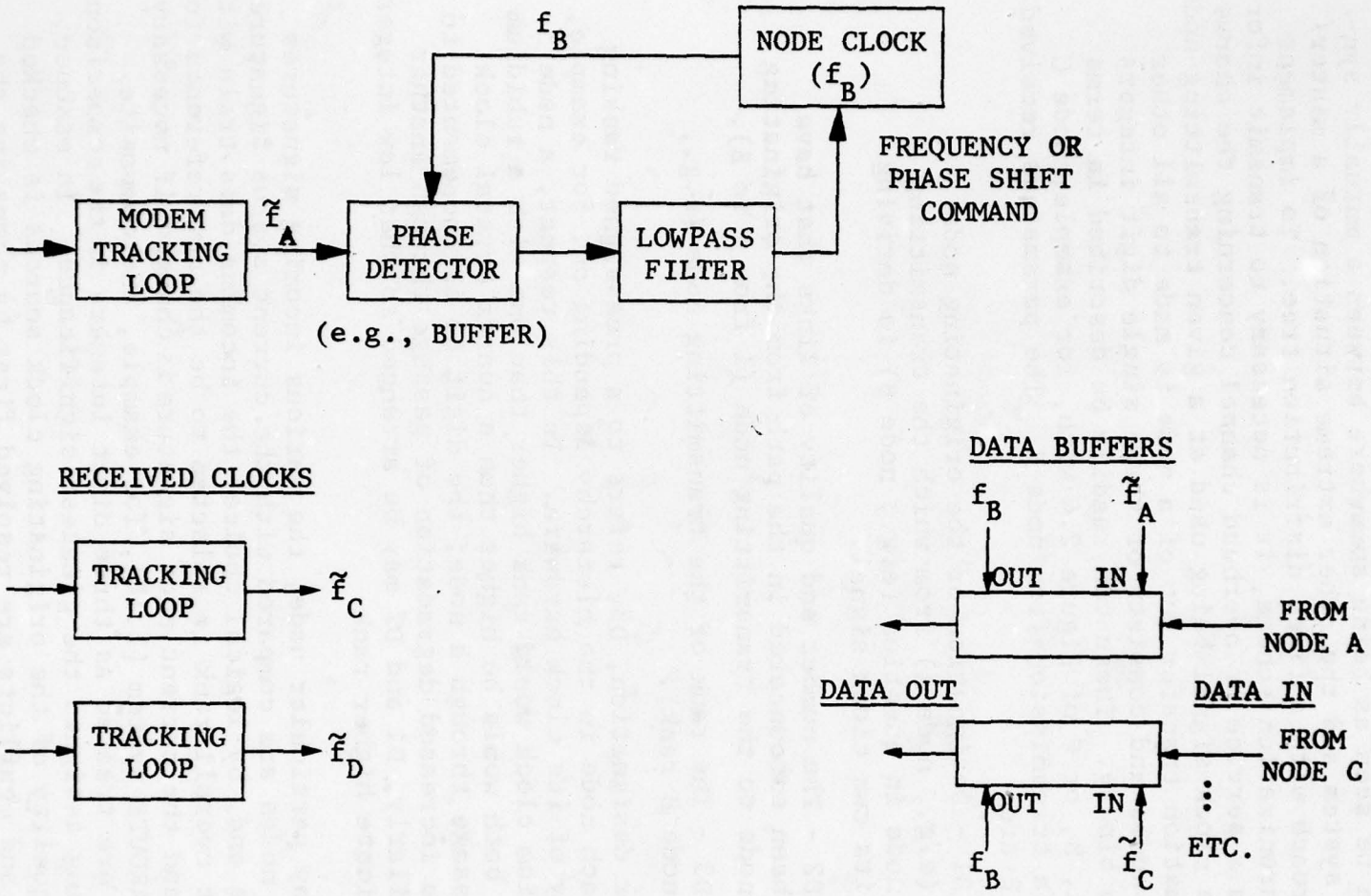


Figure 2.7 Node Signal Processing for Master/Slave Network Timing
(Example: Node B of Figure 2.4)

From a general viewpoint, the hierarchical master/slave system can be seen as being somewhere between a mutually synchronized system and the other extreme situation of a master/slave approach with a fixed distribution tree. To implement this synchronization scheme, it is necessary to transmit information via a service or overhead channel concerning the character of the clock signal being used at a given transmitting node. The information transfer out of a node is made to all other connected nodes and consists of three single digit integers coded into binary. These can readily be described in terms of nodes A, B, or C of Figure 2.4 with, for example, node C receiving a transmission from node B. The parameters received at C from B are:

(1) D1 - Designation of the originating node (e.g., node A) from which the transmitting node in question (e.g., node B) is deriving its own clock signal.

(2) D2 - The number and quality of links that have been encountered in the path from the originating node to the transmitting node (1 from A to B).

(3) D3 - The rank of the transmitting node (e.g., node B rank).

This latter designation, D3, refers to a preassigned ranking given to each node in the hierarchy depending on, for example, the quality of its clock hardware. In this respect, a node with a cesium clock would rank higher than one with a rubidium clock, and both would be higher than a quartz crystal clock. At each passage through a node, the digit D2 is incremented to reflect the increased degradation of passage through another link. Similarly, D1 and D2 may be arranged so that low integer values indicate higher rank.

For any particular node, the various incoming signatures from other nodes are compared with the current status signature of the node and, by logical choice, the incoming data train with the highest overall rank is selected to be the new reference for the node, and the current node signature is changed if necessary. In the DATAROUTE system [2.18], for example, the composite signatures are treated as three digit integers in the comparison, with D1 being assigned the greatest significance. In essence, then, the quality of the originating clock sources is checked initially, and conflicts are resolved first by comparing the quality of links encountered, and second by the rank of the

transmitting node. The incoming signal finally selected therefore represents the best quality timing data available to a given node, and the local node clock is locked to it alone until such time as conditions change in the system. Note that eventually the complete system is clocked by a single master node. If this clock fails, however, the network automatically reorganizes itself to lock onto the next best clock source.

The node outgoing data is clocked from the local clock which is slaved to the chosen incoming timing signal by means of a narrowband phase-locked loop to help eliminate the effects of medium jitter.

The hierarchical master/slave (and time reference distribution) scheme offers superior advantage in network control as far as survivability is concerned.

The distinctive feature of Time Reference Distribution (TRD) is that a network with reasonably stable clocks at each node is forced to take corrective action at these nodes on the basis of network time references that are continually passed around the system. As in the previous discussion, all nodal clocks are rank-ordered, and the timing of an incoming line is compared with the local clock in the derivation of a timing error for the corresponding link. This error signal is transmitted back to the originating node which is likewise computing its own nodal clock error for the link. With the ensuing exchange of clock error signals between both ends of the link, each of the two nodes has the capability of computing the true nodal clock time difference with virtually no dependence on path delay. This can be expressed more precisely in the following way.

Mathematically, the situation can best be described by considering the transmission from two nodes, A and B of a time reference pulse (TRP), as discussed in Section 2.1.2. Node B measures the elapsed time of the incoming TRP from node A relative to its own clock, resulting in a quantity t_A. Similarly, at node A the TRP from node B is measured relative to the local clock producing t_B. Defining the clock TRP emission times on a reference time scale to be T_A and T_B, and the path delay from A to B as τ_{AB}, it can be shown that

$$t_A = T_A + \tau_{AB} - T_B$$

and

$$t_B = T_B + \tau_{BA} - T_A$$

Hence, the clock difference $T_A - T_B$ can be computed as:

$$T_A - T_B = \frac{1}{2}\left[(t_A - t_B) + (\tau_{BA} - \tau_{AB})\right]$$

When the path delay in both directions is identical, it is apparent that

$$T_A - T_B = \frac{1}{2}(t_A - t_B)$$

and once the measurements t_A and t_B are available at both nodes, the clock offset can be calculated.

Apart from the requirement of timing error exchange, the Time Reference Distribution technique functions in a manner which is very similar to that of hierarchical master/slave. The control signals, which must be transferred around a time reference distribution controlled network, may be summarized as follows for a single node:

(1) The local time measurement (t_A) for a particular incoming link (returned to the originating node).

(2) The rank of the node being used as a master timing node for the local node (D1).

(3) A measure of the path quality for the master node supplying the local clock (D2).

(4) The rank of the local node clock (D3).

The three latter items are used with a set of prearranged selection rules* in the manner described earlier. The network then locks onto the timing data of highest rank.

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*Selection rules are discussed in [2.20] and Section 5.3.2.

We conclude this section by noting that several refinements have been built into the Time Reference Distribution technique over the last few years [2.20]-[2.22], and these features will be discussed in Section 5.

2.3 Network Survivability and Security

2.3.1 General Issues

The DCS network must be designed for satisfactory operation under conditions of hostility. There is an underlying premise, therefore, that no single node should be critical to the functioning of the remainder of the network. When one or more nodes are eliminated, the surviving nodes should be capable of continued operation.

In the next few subsections we shall examine the issues of survivability and security by comparing the different clock control techniques in stress situations requiring reorganization of the timing distribution scheme. Then we cover the subject of backup modes, where it is envisioned that normal operation with, say, master/slave, mutual sync, or TRD, is ruled out for the complete network, or at least for large portions of it. Finally, we examine the related areas of jamming and spoofing. Enemy action of this nature may, in fact, be the mechanism by which the network is disrupted.

We begin by dividing the disruption scenarios into several types. In Table 2-3 we have listed three prime categories, denoted "Stand-Alone", "Black-Out", and "Uncoordinated". Obviously, even finer distinctions can be made, particularly if only portions of the network are under stress. The reader may conveniently think of these scenarios as applying to a complete segment of the total network that has been isolated. The remaining network nodes are assumed to be functioning normally, once the temporary reorganization phase has passed.

Now let us elaborate on the categories in Table 2-3.

(1) Stand-Alone: This signifies the loss of normal clock data communications facilities. It might occur in a jamming situation which is severe enough to throw the service channel multiplexer out-of-sync. We do, however, assume that some form of high-speed communications link is functioning; e.g., the digital radios might have a

TABLE 2-3

SCENARIOS FOR NETWORK DISRUPTION

Scenario	Description
Stand-Alone	Loss of service channel and, hence, ability to data link clock control information. TRP time markers assumed available.
Black-Out	Loss of radio bit stream, i.e., no TRP frame pulses available. Telemetry orderwire disabled; hence, no clock data. Occurs after long period of normal operation.
Uncoordinated	Same as Black-Out except that the period of disruption has extended over a long period, and the prior performance history is no longer of value.

very high error rate because of jamming, but still be capable of maintaining frame sync. This is expected to be true for many situations since the radio, being basically unprotected, must have robust frame sync behavior. In such cases, the frame sync pattern is available as the TRP, but the associated clock data, including time-of-arrival measurements, are not exchanged between nodes. When this situation is encountered, the most appealing option available is the employment of some form of single-ended clock control; the choices would, of course, be master/slave, mutual sync, and a subset of the TRD technique equivalent to the self-organizing master/slave strategy. The lack of clock data forces us to resort to a relative time synchronization mode for the network. Moreover, the possibility of delay jumps (and, hence, error jumps) exists, particularly when equipment is taken in and out of service. Over extended periods, the lack of a clock data link would compromise the system time reference distribution performance somewhat, although nominal communications synchronization would be maintained for all techniques (including TRD).

(2) Black-Out: Without either the TRP time marker or the service channel clock data, the node clocks become virtually isolated. Then, one of the backup modes, independent clock or external reference, is called for in the hope of keeping the frequency of buffer resets as low as possible while the blackout conditions persist. In this scenario, recourse to independent clock operation, for example, is taken with the understanding that a known history of normal synchronization performance for the network already exists. The theme is the following. If the frequency offset and drift characteristics of every station standard are

known exactly at the time of the blackout, buffer resets should not be necessary at all. That is, station standards with accuracies of $1:10^{11}$ may be compensated for their drift and offset characteristics to provide one or two orders of magnitude better accuracy (relative to the last network master). It is shown in Section 5.4.1 that the required parameters, local standard drift and offset, can be found as variables in the control loop processing algorithm. The reader is referred to Section 5.3.5 to learn more about the "coast" mode of loop operation; clearly, that is the desired mode for the blackout scenario provided the drift and offset variables are accurate enough. With the more stable standards and a long preceding period of quiescent operation, there is no doubt that coasting through a blackout period, in the manner described in Section 5.3.5, will result in substantial improvement over the performance with completely uncontrolled independent clocks.

(3) Uncoordinated: This final scenario is intended to represent total chaos in the realm of network timing distribution. It is virtually identical to the blackout scenario except that there is no past history of satisfactory quiescent operation. Therefore, drift and offset for individual station standards will not be known. The backup alternatives are reduced to completely independent clock operation, or use of an external reference such as LORAN-C.

In concluding this section, it should be remarked that, apart from shear physical destruction of network transmission equipment, the main stress-inducing element will probably be in the nature of electronic jamming. While the jamming may be effective enough to disable the normal time transfer capabilities, it should be realized that other more rugged communications options, such as spread spectrum transmissions, will often be available. With the maintenance of precise time at both ends of a link, even in periods of disruption, some modest level of communication will be feasible. This points out the importance of establishing backup clock synchronization strategies to support such emergency communications systems if they exist on a link.

2.3.2 Self-Organizing Features

When segments of the network are in a condition of stress, it is likely that the timing distribution tree for the remainder of the network will have to be reorganized. This is the essence of survivability, and its importance for a military network is patently clear. Of course, there are more mundane reasons for implementing automatic time distribution recovery; clock and transmission equipment failures in the network are inevitable and contingency plans must be formulated to cover these events.

Of the synchronization techniques, the TRD approach is superb in the survivability features it offers. The behavior of the TRD scheme under stress conditions was covered in Section 2.2.5. It is sufficient to say here that the capacity to automatically reorganize is the feature of TRD that sets it apart from the others; namely, master/slave, mutual sync, and independent clocks. This self-organizing capability should be recognized as a characteristic that does not necessarily have to be associated with TRD; that is, the time distribution functions and the reorganization functions are essentially separate. We can contemplate the development of a relative time synchronization scheme which has these self-structuring features; it would be equivalent then to a master/slave scheme with an adaptively reorganized distribution tree. Definitions covering such an approach were presented in Section 2.2.1.

It can be safely concluded that the self-organizing aspects of the currently formulated TRD technique are of great benefit, and bring to the overall network a level of resilience that cannot be matched by other approaches. Of the remaining choices, the independent clock method is in a class of its own and need not be discussed. Then, the mutual synchronization technique should be considered as having reasonable survivability characteristics. Despite the potential for operation without the need for a clock control data link, there are however questions of stability which arise when the structure of the network is undergoing change. Finally, it is recognized that the master/slave technique, at least in its classical form, is not well-suited to coping with network stress.

There is a temptation to treat these candidate techniques in isolation, as separate and unalterable methodologies. But, as we pointed out above, certain features of one may be applicable to others. The self-organizing features of TRD should

not be associated with TRD exclusively, for example. Another important point is that reorganization without control data linking is a very desirable goal; that is, it may be feasible to formulate reference selection rules on the basis of the received TRP signals alone. Clearly, there will be a sacrifice in terms of selection optimality. On the other hand, the physical structure of the DCS network is likely to remain relatively invariant, and preplanned timing recovery strategies, including reference selection, should be easy to test by means of simulation. Furthermore, with a reliable enough backup mode of operation, the reference selection process could be undertaken at a fairly leisurely pace to minimize the possibility of network instability.

2.3.3 Backup Modes of Operation

When one considers the topic of survivability, the idea of a backup mode is immediately brought to mind. Here we will be concentrating on two particular backup configurations. It should not be concluded that these are the only two, but they are generally considered as likely candidates.

These backup concepts involve:

- Use of AN/GSQ-183 timing terminal; i.e., a LORAN-C based external frequency source.
- Network operation with highly stable independent standards.

Both modes will be considered subsequently.

First we outline the functional properties of the AN/GSQ-183 Frequency Control Set, which is intended for use as an interim timing subsystem in DCS.

2.3.3.1 Description of the AN/GSQ-183 Frequency Control Set

The AN/GSQ-183 frequency control set uses the worldwide LORAN-C transmissions to obtain high-resolution frequency references and calibration at a network node. The system generates a 1-MHz output signal which may be phase-locked to either a 1-MHz local reference or to the incoming LORAN-C signal.

The principal components are shown in Figure 2.8. The CV-3094 frequency multiplier consists of a combiner to supply a 1-MHz reference to the LORAN receiver. This signal is derived from either the primary or secondary RF oscillators (O - 1632) using an automatic selection procedure in the event of oscillator failure. The CV-3094 also ensures that the system output (1 MHz) is slaved to the best reference choice, i.e., either the LORAN-C groundwave or the alternate local reference. When neither of these signals is available, each RF oscillator is put into a coast mode using digital control signals as shown. This unit and the oscillators can function independently of the LORAN receiver using alternative 1-MHz frequency sources (sine or square wave).

The R-1776 receiver is a solid-state unit designed to track the LORAN-C signals. It features an all-electronic phase-tracking servo system, with 20-ns resolution.

The O - 1632 oscillators consist of a voltage-controlled crystal oscillator with digital control signals and provision for manual slewing of frequency to assist in acquisition. The digital servo memory retains the crystal aging rate when the loop is opened. Finally, the CV-3093 frequency multiplier consists of three identical modules, each of which synthesizes 96 kHz and 1.2288 MHz from a 1-MHz input signal.

2.3.3.2 AN/GSQ-183 as a Backup Frequency Source

The AN/GSQ-183 output may be visualized as a frequency reference with excellent long-term stability traceable back to an atomic standard via the LORAN-C path. However, quite severe path length variations are evidenced, and this is equated with unwanted phase and frequency jitter on the output signal.

There are at least two ways of integrating the AN/GSQ-183 signals into the timing subsystem. In discussing two obvious possibilities, we shall also touch on the subject of independent clock operation as a backup mode.

The two figures which follow, Figures 2.9 and 2.10, provide a pictorial statement of the two integration choices alluded to above. Some explanation of the symbols and notation shown is first required. (See Sections 5.3.1 and 5.3.4 for a more comprehensive control loop description.) Without getting into the subtleties of the complete loop design, it can be said that

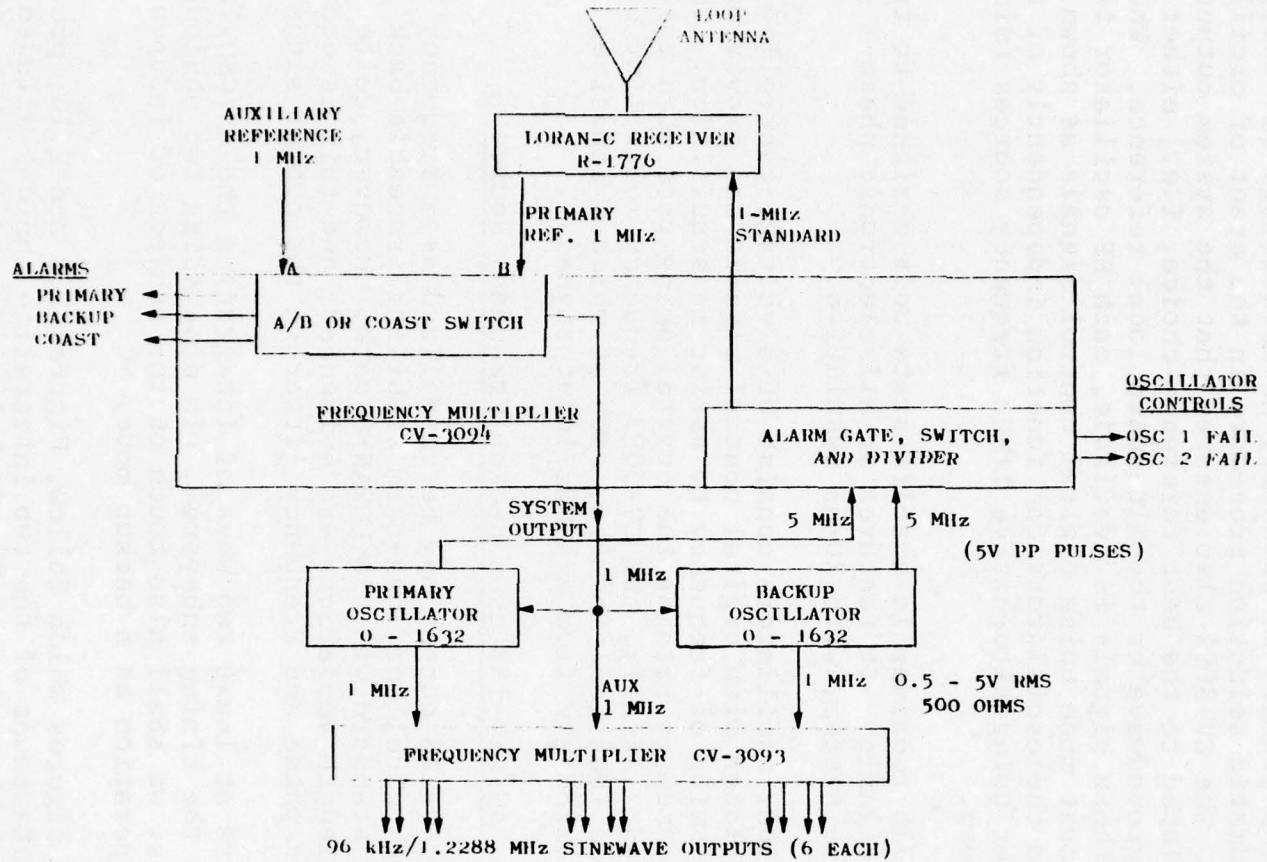


Figure 2.8 AN/GSQ-183 Frequency Control Set

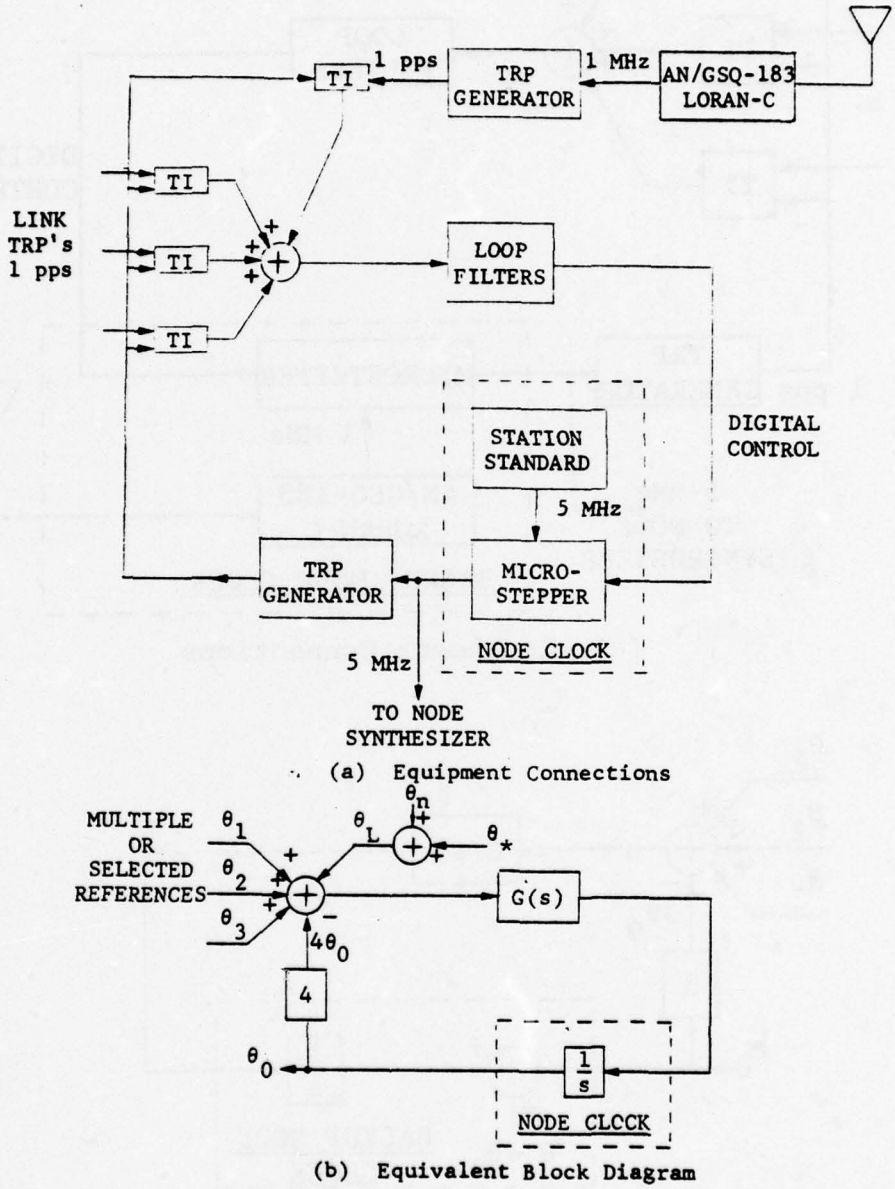
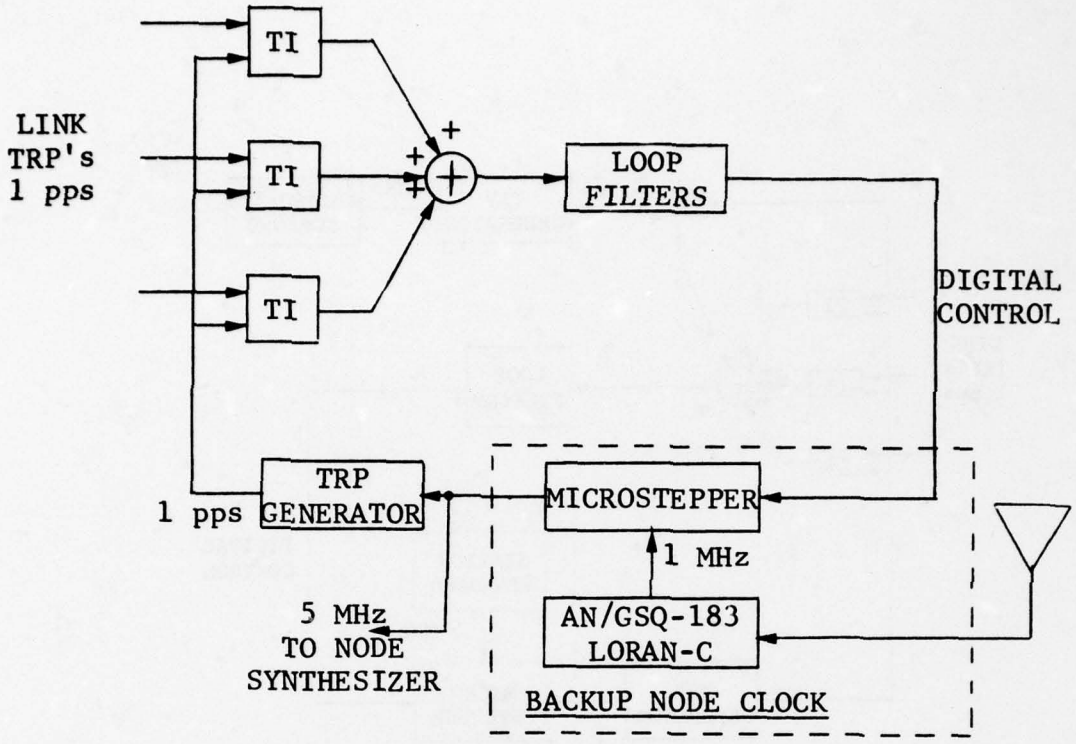
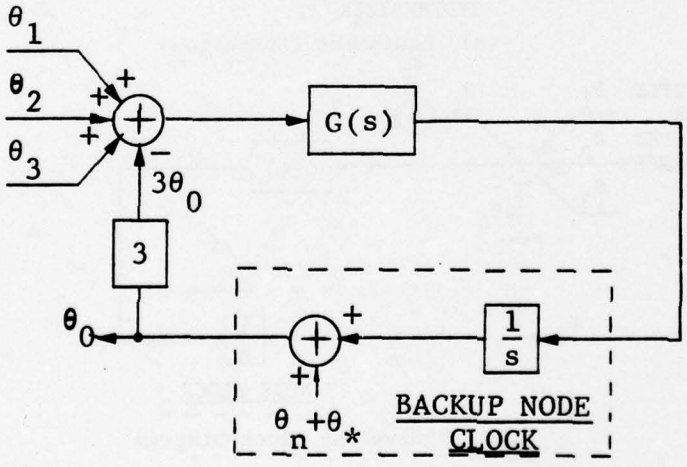


Figure 2.9 Integration of the Interim Subsystem as an Alternative Reference



(a) Equipment Connections



(b) Equivalent Block Diagram

Figure 2.10 Integration of the Interim Subsystem as a Backup Node Clock

one or more arrival time measurements from terminated links will be processed and combined to produce a clock correction signal. In its simplest form, this is a clock phase error. Figure 2.9(a), for example, has three terminated links, and, for each, a time of arrival or phase measurement is made relative to the local node clock. In Figure 2.9(b), we have the transfer function block diagram equivalent of (a). The inputs are represented as phase variables θ_1, θ_2, θ_3, and, after being compared with the node clock phase θ_0, the differences are passed to the control loop filter.

The LORAN-C external reference is represented in terms of the phase of the originating standard θ_*, and a propagation induced phase perturbation (i.e., noise) θ_n. The total is designated θ_L. The method suggested in Figure 2.9 is to simply treat the external LORAN signal as another equivalent reference. This is implemented by generating a standard TRP with repetition rate of 1 per second. This derived timing event is compared with the local TRP, and the resulting time interval measurement is used in the clock updating. For time reference distribution, the LORAN TRP would not be used explicitly since it is incapable of providing precise time data; its role is limited to stable relative time transfer. Consider, then, the situation where none of the links can provide a reliable time transfer path. Then, backup operation would consist of maintenance of the node clock phase so that the relative time between the local TRP and the LORAN TRP was preserved. The loop would serve to lowpass filter the LORAN time variation; thus, the loop time constants would be chosen to smooth out θ_n in Figure 2.9 and hold the node clock output to a constant relative time with respect to the LORAN standard. With this form of backup, there is no stringent stability requirement for the local standard since it is effectively locked to the LORAN atomic standard.

The important aspect of this mode is that the LORAN-C TRP signal can be subjected to a set of consistency and rejection rules in the same way that link termination TRP's will be (see Section 5.4.2). Hence, loss of the LORAN reference because of transmission or medium disruptions should be detectable. Then, the local station standard resorts to stand-alone operation as an independent clock. This safety mechanism represents a second level of backup for the node.

The other approach, depicted in Figure 2.10, is more straightforward, and perhaps more representative of circumstances where the station standard had failed. As shown, the

LORAN 1 MHz is used as a direct substitute for the station standard. While link references remain valid and reliable, the servo loop can operate with them as shown. The output signal phase, marked by the symbol θ_0, is not the same as the direct LORAN phase. The loop provides highpass filtering of the LORAN phase (see Section 5.3.1). This means that any low frequency fluctuations in θ_L cause the loop to produce a counteracting phase stepper control voltage; thus, as far as θ_0 is concerned, there is no effect. The node, therefore, depends on the long-term stability of the incoming link reference rather than the LORAN-C signal.

When the node must operate completely without the link references, it would make sense to open the loop to obtain the LORAN-C long-term stability at the node. This is done quite simply by clamping the phase stepper control voltage at zero. Then the microstepper output is used directly by the node synthesizer. If we compare this open loop operation of the configuration in Figure 2.10 with that shown in Figure 2.9, it is seen that while they are basically both locked to the LORAN signal, the latter lowpass filters the incoming LORAN signal and, in addition, allows the node to revert to independent clock operation without reconfiguration.

Our recommendation for backup node operation would, therefore, be to use the "pseudo link" configuration of Figure 2.9 except when the station standard has failed completely, in which case the configuration in Figure 2.10 must be utilized, either open loop or closed loop.

2.3.4 Anti-Jam Precautions

With the timing subsystem designs to be discussed, we are dependent on the quality of both radio TDM frame synchronization and service channel data. At times when the link is being jammed, both of these signals may be unreliable (e.g., high error rate) or, indeed, unusable. The anti-jam design issues are mainly associated with the radio design, since we are concerned primarily with the processing of digital waveforms in the subsystem.

The radio DEMUX frame markers constitute the most viable form of TRP transmission, provided the radio circuitry is sufficiently accessible and amenable to modification (see Section 5.1.2). These sync codes are interpretable correctly only if:

- The frame synchronizer is giving out a correct frame clock.
- The bit error rate is low enough so that the TRP sync code matching circuitry can still get reliable detection performance.

This problem is very closely related to the determination of detection/false alarm thresholds for demultiplexer synchronizers. The requirements are similar, but to proceed with a full analysis we need definitive information concerning the proposed FRC-163 design.

As a response to the jamming threat, we recommend that specific analyses be carried out. They should involve an examination of the following issues:

- The error rate for different types and levels of jamming must be established. This has already been pursued for some types of existing radios.
- Frame and bit synchronization performance for the FRC-163 and existing radios must be analyzed, since the recommended clock synchronization schemes depend, in one way or another, on radio bit and frame sync.
- Time transfer sync code detection and false alarm statistics can be computed as a function of jammer level. This applies to the frame sync bits identified as being the 1-per-second time markers. Interaction of the required detection circuitry with the radio frame sync circuitry must be critically examined to determine the best overall combination from an anti-jam point of view.
- Synchronization performance for the service channel TDM must be determined. We expect that a unit such as the 1192 will be quite vulnerable in high error-rate environments such as those occurring with jamming. The capacity of the DEMUX to hold synchronization during these periods must be investigated.

- Vulnerability of the clock control subsystem to jamming or spoofing of the clock exchange data. The ability of the clock control processor to eliminate poor quality data must be confirmed by thorough analysis and design for situations involving high error rates or spoofing.

The overall network resistance to jamming and spoofing will depend on the clock synchronization technique employed; with the candidate timing subsystem approaches outlined in Section 5, performance in every case can be related back to radio error rate, which impacts the subsystem design and demodulator bit tracking loop loss-of-sync threshold (specified independently of timing subsystem requirements).

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SECTION 3

LINK PARAMETER EVALUATION EXPERIMENTAL PROGRAM

3.1 Summary of Objectives

In Section 2, some of the candidate network synchronization techniques were discussed. The most important equipment and medium effects as far as performance is concerned can be classified in the following way:

- Link equipment and medium delay, both fixed and variable
- Bi-directional link delay differences, fixed and variable
- Short-term timing jitter
- Error rates and distributions and their effect on clock data transmissions

The last item was not considered a primary data acquisition target because of the copious quantities of such data available from other programs. Our concern was more for the one-way and bi-directional path length biases and time variation.

The geographical relationships of the sites can be seen in Figure 3.1. A more detailed diagram of the Verona and Youngstown path and site configurations can be found in Appendix D.

3.2 TROPO Equipment Configuration

Here we examine the general TROPO equipment characteristics with emphasis on Government-furnished items. Much of the custom built hardware provided by CNR, Inc. will not be fully described until Section 3.4, since a real understanding of its operation requires an appreciation of the test procedure involved.

The radio paths available on the Youngstown/Verona link are summarized in Figure 3.2. The dotted connecting lines indicate the paths selected for use in the TROPO tests. Generally, the 912-MHz path from Youngstown to Verona was included in all tests as a controlled reference. The special TRC-132 beam,

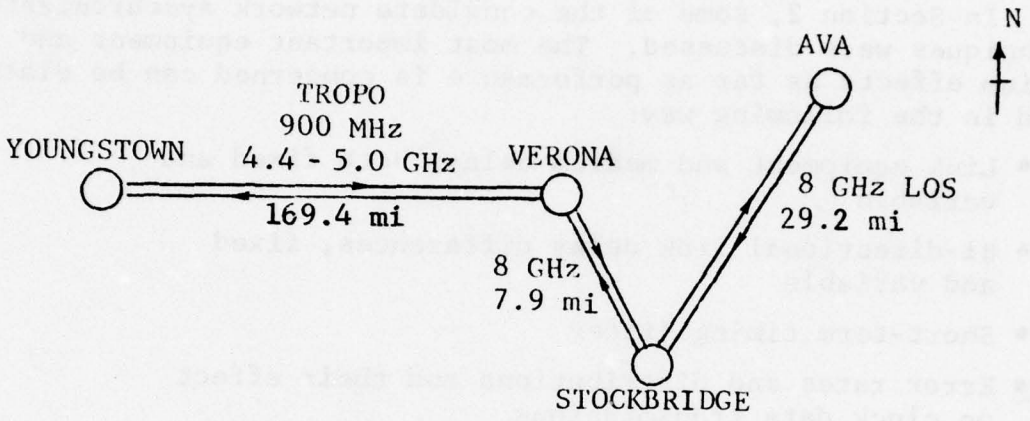


Figure 3.1 Geographical Site Layout

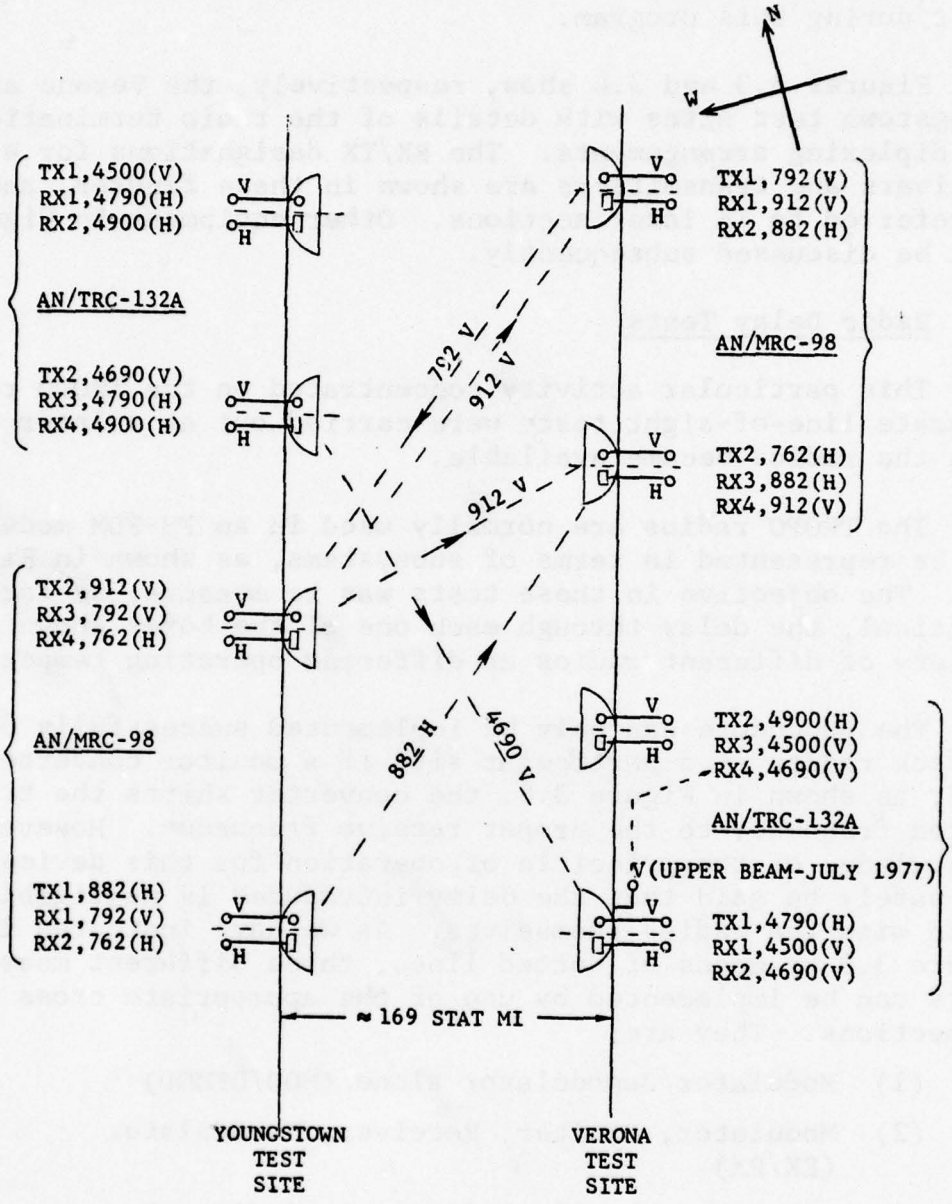


Figure 3.2 TROPO Link Configuration

marked as "UPPER BEAM- JULY 1977", was a nonstandard feed horn installed for angle diversity purposes as part of another contract during this program.

Figures 3.3 and 3.4 show, respectively, the Verona and Youngstown test sites with details of the radio terminations and diplexing arrangements. The RX/TX designations for all receivers and transmitters are shown in these figures, and will be referred to in later sections. Other equipment in Figure 3.4 will be discussed subsequently.

3.3 Radio Delay Tests

This particular activity concentrated on the TROPO radios. Separate line-of-sight tests were carried out at a later date when the radios became available.

The TROPO radios are normally used in an FM-FDM mode. They can be represented in terms of subsystems, as shown in Figure 3.5. The objective in these tests was to measure, as far as practical, the delay through each one of the boxes shown for a variety of different radios at different operating temperatures.

The procedure can only be implemented successfully on back-to-back radios at a particular site if a monitor converter is used; as shown in Figure 3.6, the converter shifts the transmitted frequency to the proper receive frequency. However, from a knowledge of the principle of operation for this device, it can safely be said that the delay introduced is negligible compared with the radios themselves. As we have indicated in Figure 3.6 by means of dotted lines, three different measurements can be implemented by use of the appropriate cross connections. They are:

(1) Modulator/Demodulator alone (MOD/DEMOD)

(2) Modulator, Exciter, Receiver, Demodulator (EX/RX)

(3) Loop through all equipment including the Power Amplifier (PA) and Receiver (PA/RX)

The common thread for all these measurements is that they are carried out using the modulator and demodulator baseband interfaces. This is necessary to allow baseband tones to be fed to the radios for delay tests. In Figure 3.7, the simplified delay measurement setup is illustrated. A tone in the

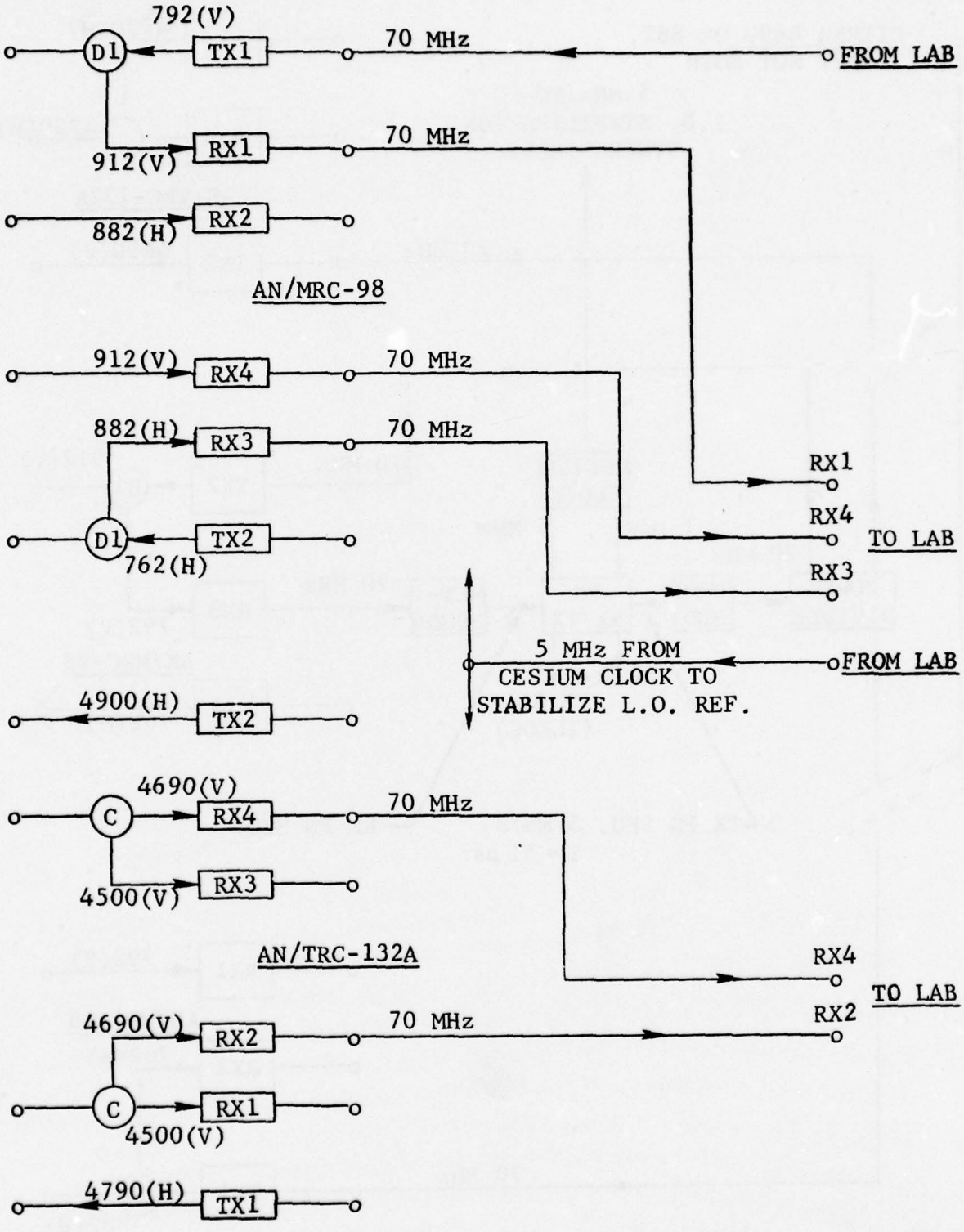


Figure 3.3 Verona Test Site Configuration

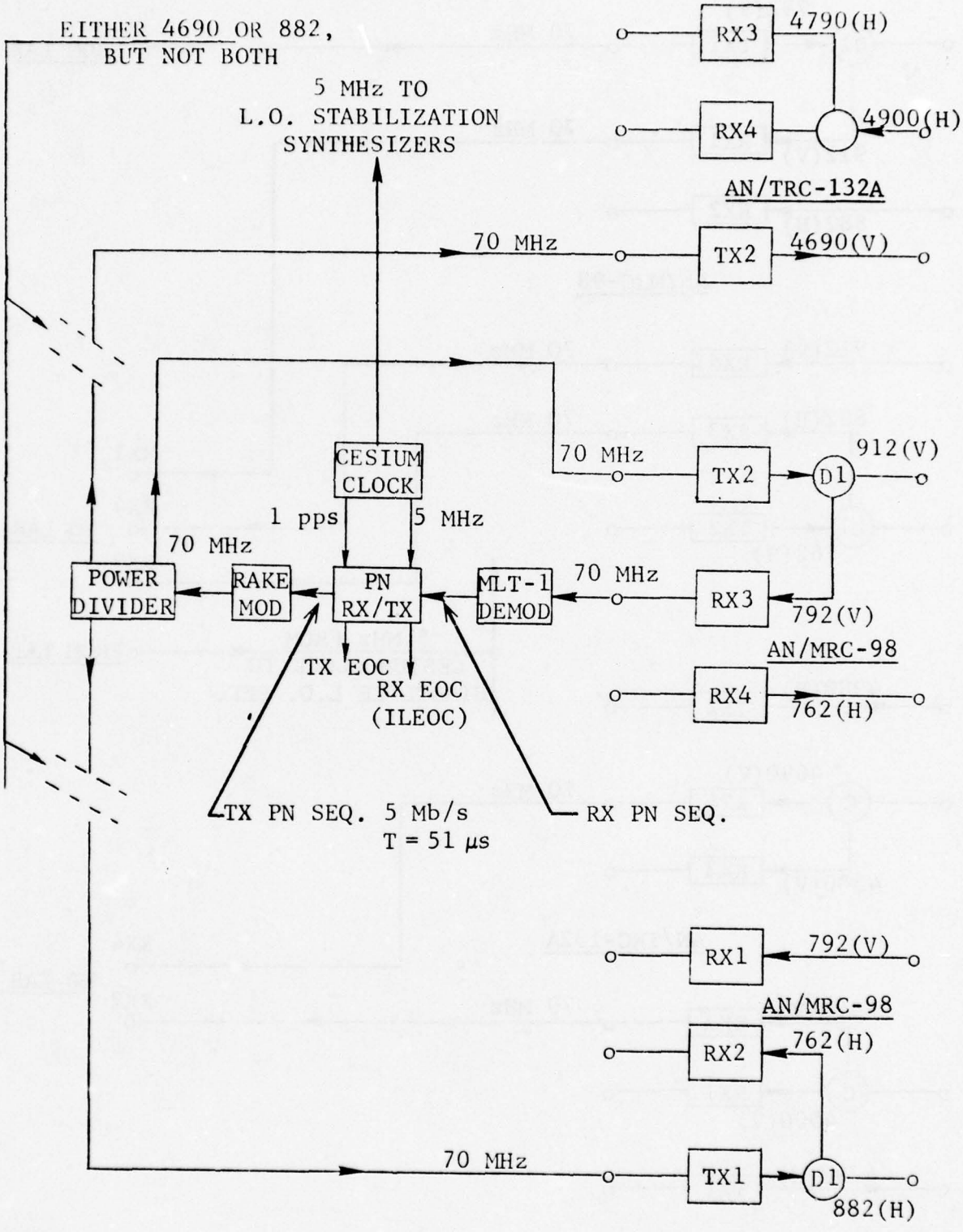
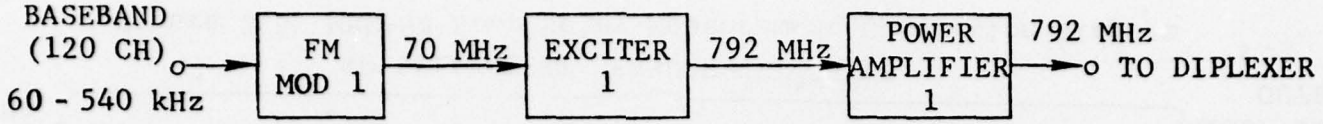
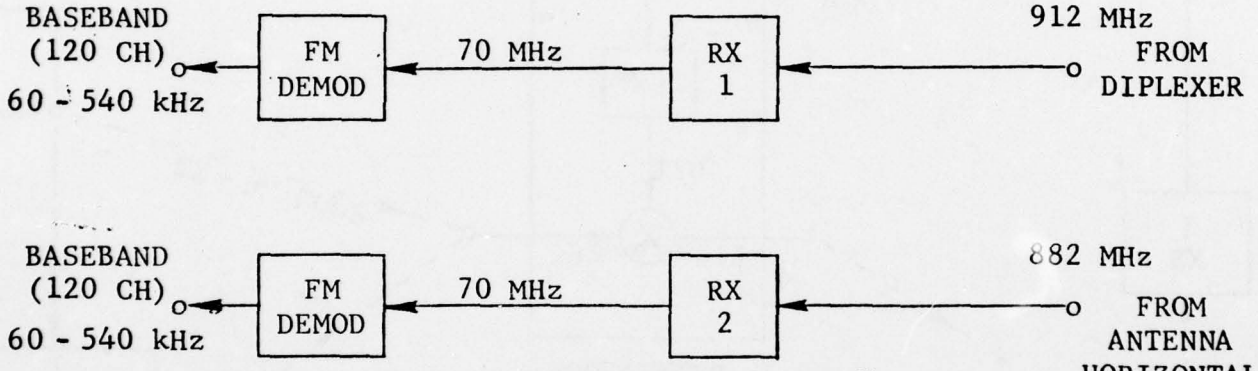


Figure 3.4 Youngstown Test Site Configuration



(a) Typical Transmitter (L-Band)



(b) Typical Receiver (L-Band)

Figure 3.5 FM-FDM Radio Block Diagram

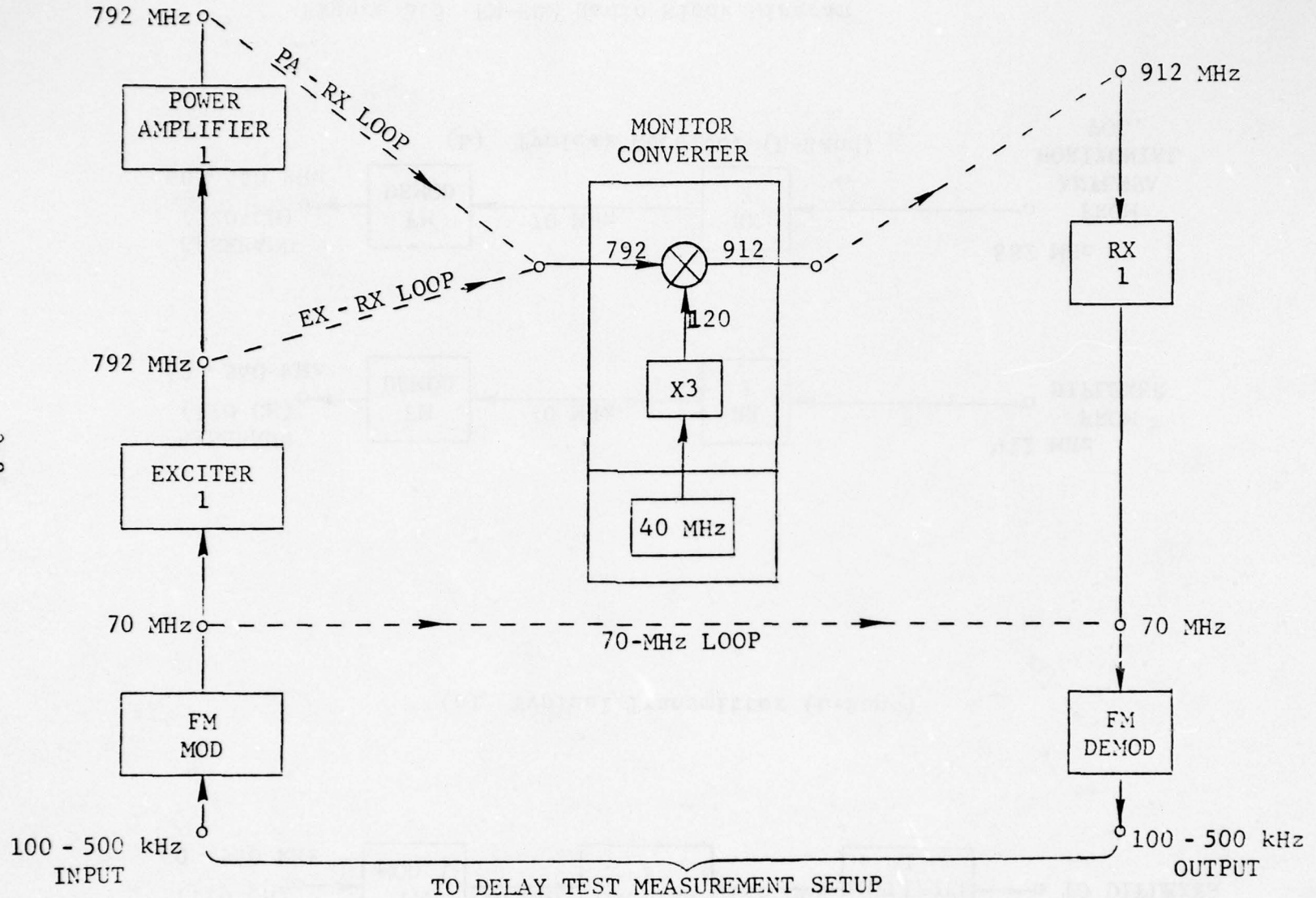


Figure 3.6 MRC-98 Loop Delay Measurement Connection Diagram

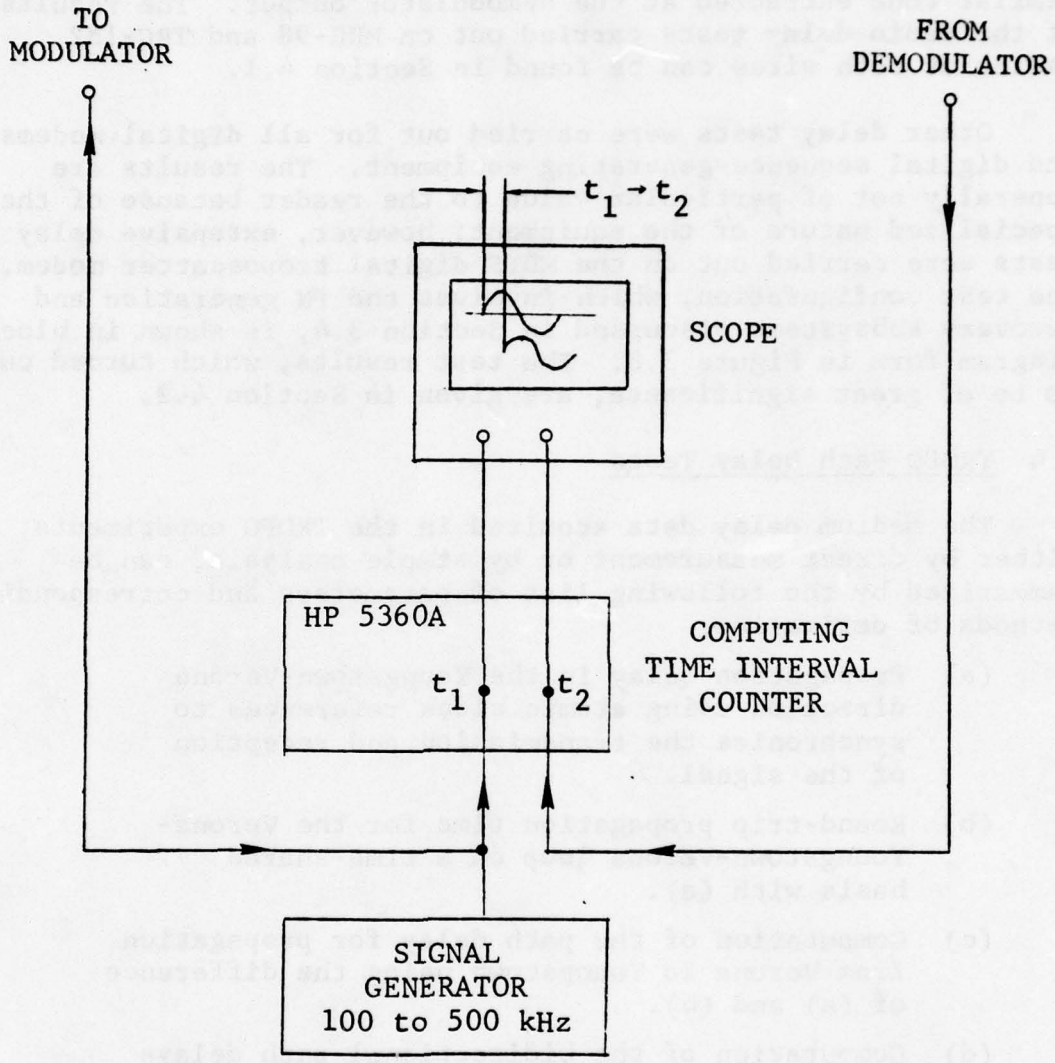


Figure 3.7 Baseband Delay Measurement Test Setup (Simplified)

range 100 kHz to 500 kHz is applied to the radio equipment and a counter, and compared with the zero crossing time for a similar tone extracted at the demodulator output. The results of the radio delay tests carried out on MRC-98 and TRC-132 radios at both sites can be found in Section 4.1.

Other delay tests were carried out for all digital modems and digital sequence-generating equipment. The results are generally not of particular value to the reader because of the specialized nature of the equipment; however, extensive delay tests were carried out on the MDTS digital troposcatter modem. The test configuration, which involves the PN generation and recovery subsystems discussed in Section 3.4, is shown in block diagram form in Figure 3.8. The test results, which turned out to be of great significance, are given in Section 4.2.

3.4 TROPO Path Delay Tests

The medium delay data acquired in the TROPO experiments, either by direct measurement or by simple analysis, can be summarized by the following list of parameters and corresponding methods of derivation:

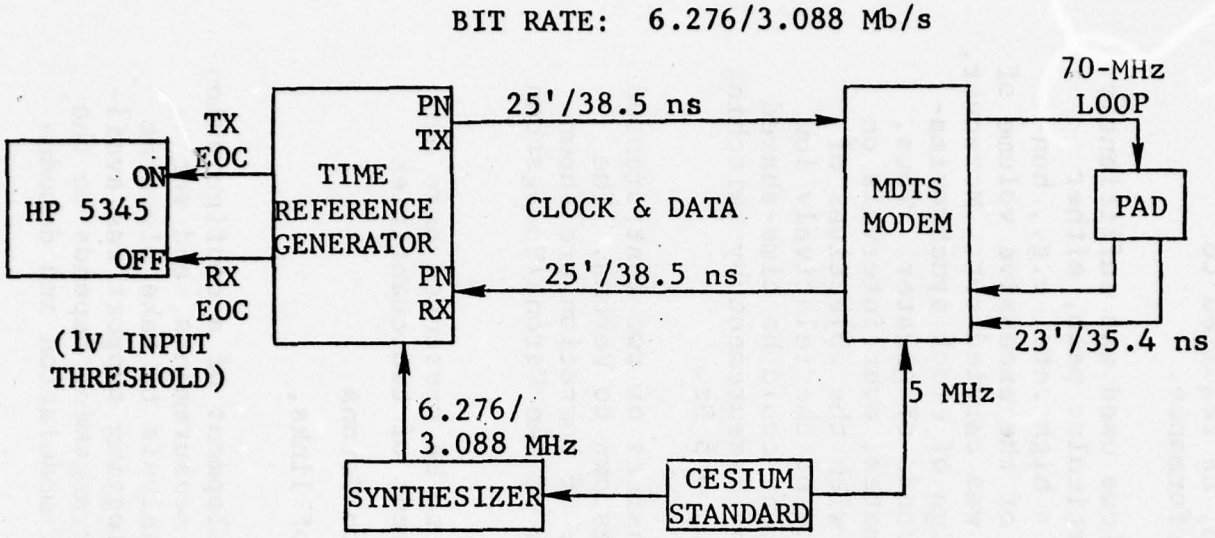
(a) Propagation delay in the Youngstown-Verona direction using atomic clock references to synchronize the transmission and reception of the signal.

(b) Round-trip propagation time for the Verona-Youngstown-Verona loop on a time-shared basis with (a).

(c) Computation of the path delay for propagation from Verona to Youngstown using the difference of (a) and (b).

(d) Computation of the bidirectional path delays Verona to Youngstown and vice versa, using (a) and (b).

(e) Absolute and relative delay measurements as above using different receiving antennas (space diversity paths), different frequencies in the same band (frequency diversity paths), and different frequency bands.



TOTAL CABLE DELAY = 38.5 x 2 + 35.4

= 112.4 ns

TIME REFERENCE GENERATOR DELAY

RX EOC - TX EOC = { 1.4691 μs @ 6.276 Mb/s
1.3764 μs @ 3.088 Mb/s

MDTS MODEM DELAY = Measurement - Cable Delay - TRG Delay

where Measurement = RX EOC - TX EOC for the composite cable and modem loop

Figure 3.8 Measurement Configuration for MDTS Static Delay Tests

(f) Differential path delay for two signals transmitted from Youngstown to Verona on different space or diversity paths.

(g) Multipath spread, received signal level statistics, fade rate and duration, as required to determine overall system performance.

The time delay measurement technique used was sufficiently responsive so that the delay for a particular path, either direct or looped, could be sampled at a high rate, e.g., hundreds of samples per second. Because of the excessive volume of data produced, on-line data reduction was carried out. Moreover, the time scale of interest in the design of clock synchronization subsystems is on the order of seconds or greater. Thus, the averaging of time-of-arrival estimates, over intervals on the order of a second, was consistent with the objectives of the experiments. A further consequence of the relatively low data rate requirements was that equipment could be time-shared between, say, a loop and a direct delay measurement by switching input signals at a suitable rate, e.g., 0.5 Hz.

The configuration of interest consists of two instrumented links: Verona to Youngstown and Youngstown to Verona. The primary choices of radios or frequency of operation are shown in Figure 3.9 which is a block diagram of the Verona/Youngstown link and associated test equipment.

The important equipment features to be presented here are associated with the efficient measurement of two quantities:

(1) Path delay from Youngstown to Verona

(2) Loop delay for the cascade of links, Verona-Youngstown-Verona

Substantial thought went into the development of a configuration which would allow bidirectional delay measurements, and yet allow all critical data logging and analysis to take place at the Verona site where extensive data logging support was available. The method of achieving this arrangement depends on the time-multiplexing of certain pieces of modulation and demodulation equipment shown in Figure 3.10.

It is apparent that the measurement of TROPO path delay cannot be readily measured to tens of nanoseconds without first measuring the channel impulse response which forms the basis for

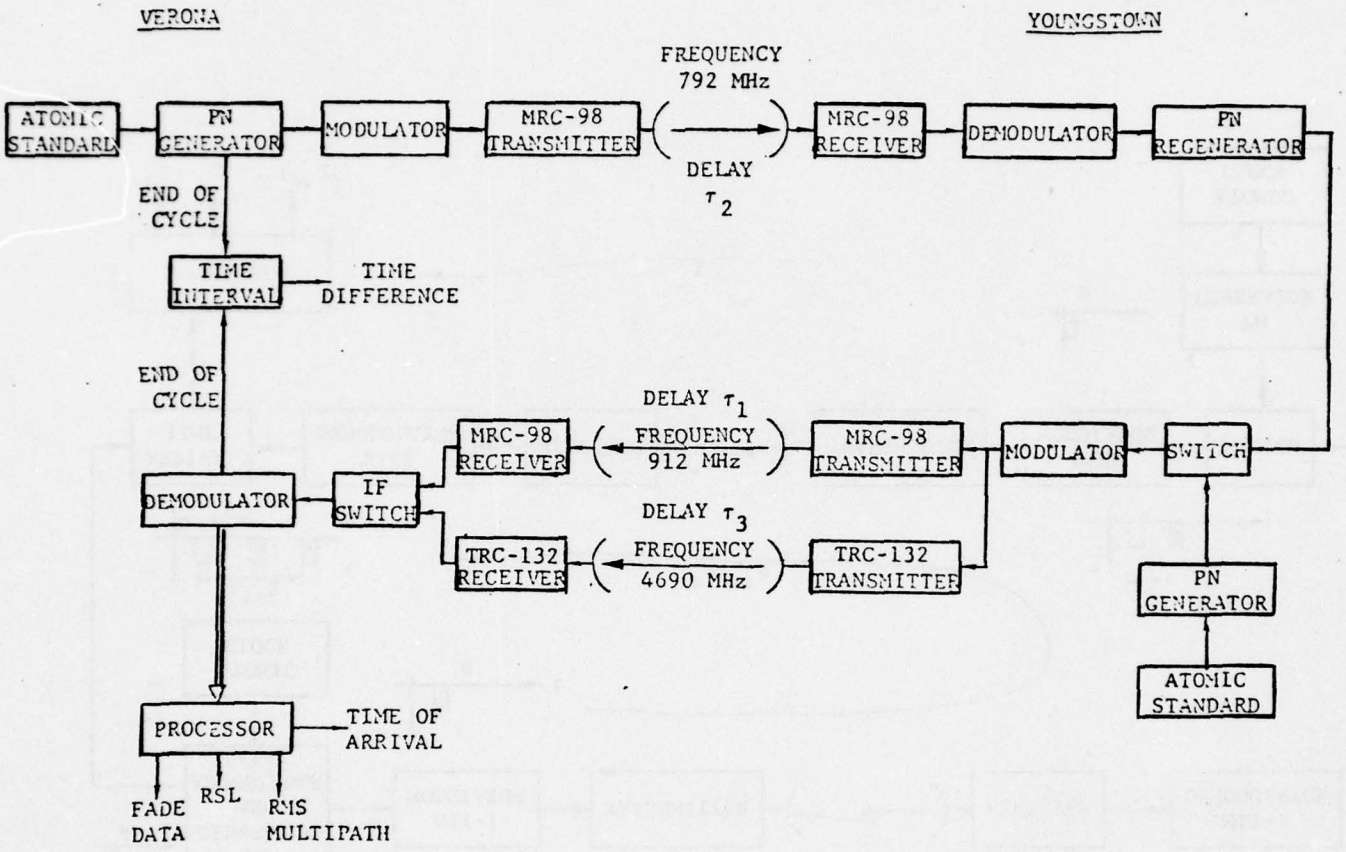


Figure 3.9 Differential and Absolute Delay Measurement Configuration

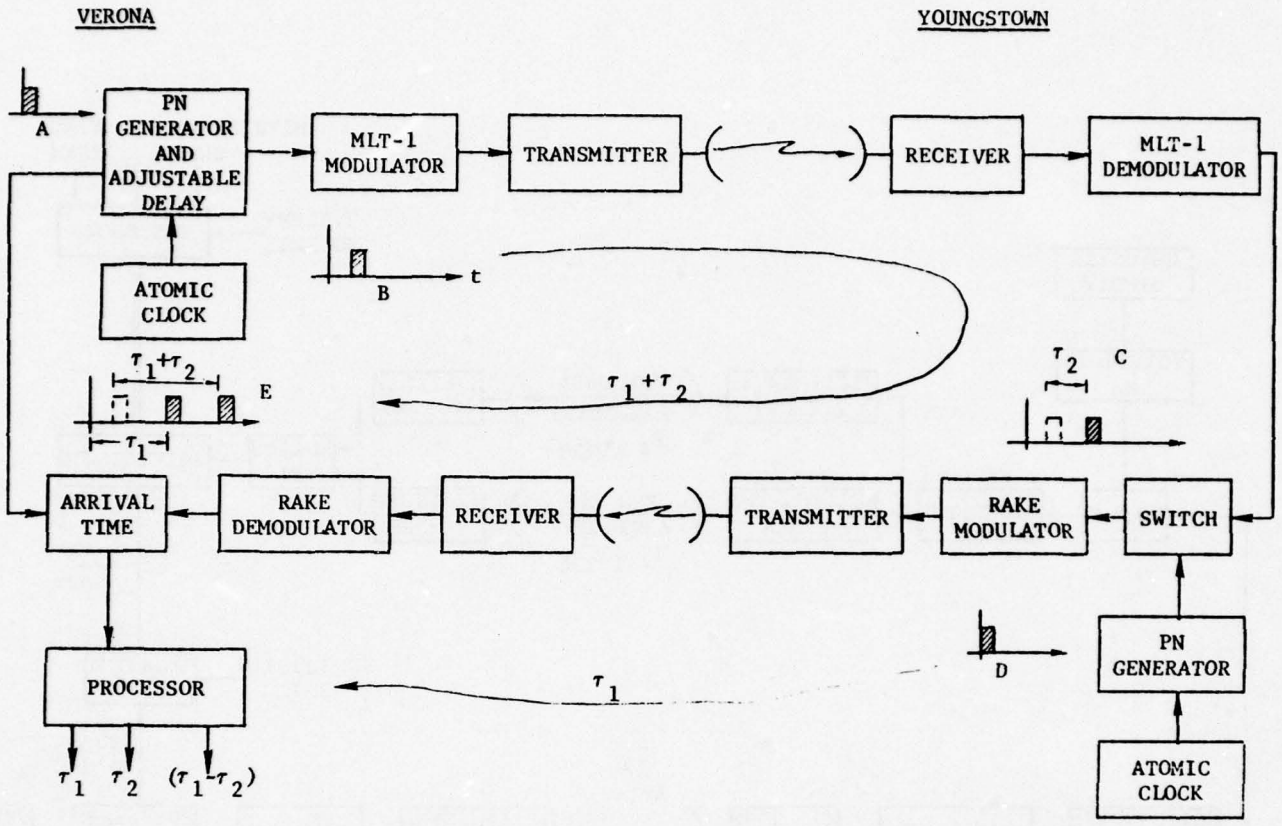


Figure 3.10 Verona-Youngstown Timing Measurement Principles

an instantaneous arrival time estimate. Averaging of this quantity may then be carried out over a desired time interval to produce a smoothed arrival time. Both forward and return Verona-Youngstown links were instrumented with channel impulse response probing equipment. For the Verona to Youngstown link, the MLT-1 modem, built by CNR, Inc., was set up to transmit data and probing signals from the Verona end. At Youngstown, the demodulator stripped off the response to the probing signal and formed an estimate of the instantaneous impulse response. The bit tracking loop followed the time variation of this impulse response by forming an estimate of the arrival time of the energy maximum for the demodulator window. Various choices of different loop filter bandwidths in the tracking loop allowed the arrival time estimate to be smoothed. For the experiments carried out, the transmitted data bit rate was 5 Mb/s in all cases.

The Youngstown-Verona link was measured using the Sylvania RAKE probing equipment which has been employed in a variety of programs in the past. It was set up to run at either 5 Mb/s or 1.25 Mb/s, and was modified slightly to accept bits from an external PN generator rather than from its own internal modulator PN generator. However, it was subsequently discovered that the RAKE was not operational at 1.25 Mb/s and, as a result, all tests were carried out at 5 Mb/s.

Figure 3.10 illustrates the general nature of the experimental setup without being too specific. With the aid of this block diagram, we now proceed to explain the method of operation; more detailed equipment block diagrams will follow. The principle involved is that of synchronized PN sequence transmission from two ends of the link. The atomic clocks shown allow the two sequence generators, one at Verona and one at Youngstown, to be reset to the same starting point at a given instant, e.g., at a particular hour, minute, and second. The atomic clocks were not precisely time-synchronized, but their offset was established to within certain limits by carrying portable atomic clocks between the two sites. A one-second event and a 5-MHz timing signal were both available. The one-second pulse was divided down to give a minute clock. Then, at a predetermined instant of time, the PN generators were reset and began clocking at a 5-Mb/s rate. Because the behavior of a PN sequence from a time transfer point of view is conceptually similar to a pulse transmission, we choose to explain the measurement method in terms of pulses. For example,

in Figure 3.10 at the point marked by A, a pulse is shown to start at time zero when the PN generator is reset. Similarly, a transmission is initiated from Youngstown.

For reasons which will later become more obvious, arrangements were made to delay the PN sequence generated at Verona by a fixed number of bits using a manual control. Since this delay is known, its effect can be accounted for in the final data analysis. The delayed PN sequence under discussion is thus shown conceptually by the delayed pulse at point B in Figure 3.10. The sequence is transmitted over the medium using the data input to the MLT-1 modem, and after passage through sequence regeneration circuitry at the output of the MLT-1 demodulator (not shown in Figure 3.10), it becomes available to the RAKE modulator. The path delay in the direction of Verona-Youngstown is represented by the symbol τ_2, as shown in the equivalent pulse diagram at point C.

The local Youngstown clock also initiates a PN sequence transmission with zero delay relative to the initial Verona sequence, and the timing is indicated at point D. Timing offsets between the Youngstown and Verona clocks should be explicitly indicated as an offset between the pulses and A and D but, for simplicity of presentation, we have chosen not to do so in Figure 3.10.

The RAKE modulator is switched between the two available modulating sequences as shown; either the regenerated PN sequence from Verona or the local PN sequence from Youngstown. The sequences were made identical in length and pattern by implementing sequence generators with the same feedback taps as the RAKE demodulator throughout the system. The difference between signals at D and C is simply one of sequence phasing. The path delay τ_2 causes the Verona-originated sequence to appear with a time-varying delay relative to the local Youngstown sequence.

The switching between inputs is not a critical function and was controlled by the Youngstown clock to alternate inputs every four seconds. In either switch position, the modulation sequence was transmitted back to Verona where it was processed by the RAKE system. The RAKE demodulator has an internal sequence generator which can be manually shifted in time, forward or backward, relative to the incoming signal. By comparing the original sequence available at point A and the received energy in the bank of tap correlators, the total round-trip propagation

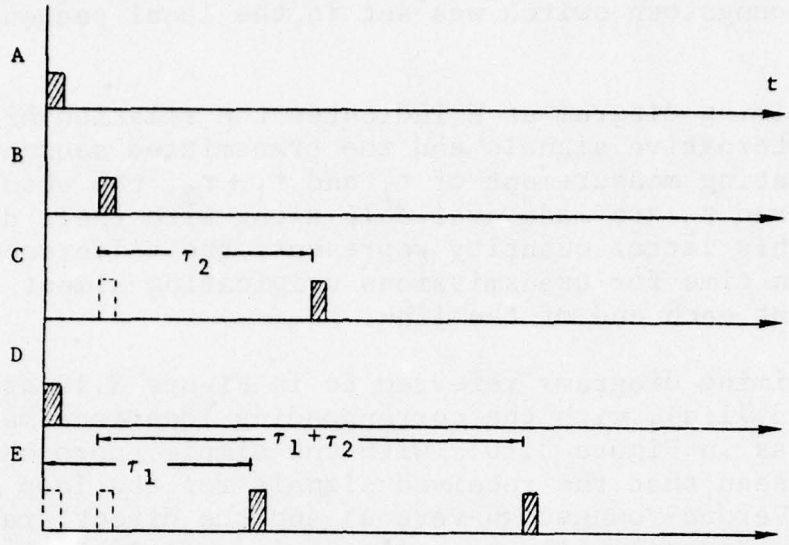
time was obtained, i.e., $\tau_1 + \tau_2$. Alternatively, τ_1 was measured when the Youngstown switch was set in the local sequence position.

The timing diagram at E indicates the relationship between the two alternative signals and the transmitted sequence. From the alternating measurement of τ_1 and $\tau_1 + \tau_2$, the absolute path delays τ_1 and τ_2 are made available along with their difference $\tau_1 - \tau_2$. This latter quantity represents the difference in propagation time for transmissions originating almost simultaneously at each end of the link.

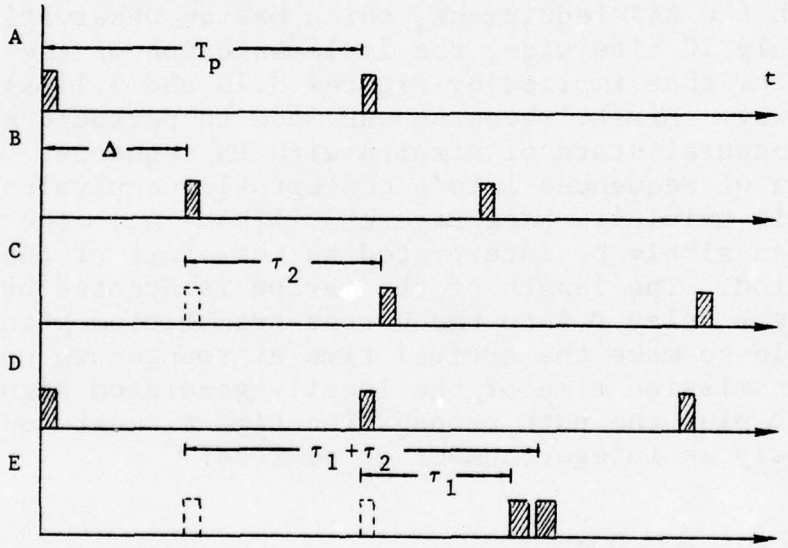
The timing diagrams referred to in Figure 3.10 are repeated in Figure 3.11(a), with the corresponding locations marked A, B, C, ... as in Figure 3.10. With the simple approach outlined, it can be seen that the received signals for the loop transmissions (Verona-Youngstown-Verona) and the direct transmission (Youngstown-Verona) will generally arrive at widely-separated points in time. To alleviate difficulties in following the signal with the RAKE equipment, which has an observation "window" only 10 bits wide, the implementation of the experiment deviated from that implied by Figures 3.10 and 3.11(a) in the following way. First, recourse was made to periodic signals. This is a natural state of affairs with PN sequences, and the translation of sequences into a conceptually equivalent train of pulses is trivial. [See Figure 3.11(b) - A.] The pulse position can simply be interpreted as the start of the PN sequence period. The length of the period is denoted by T_p. By introducing a delay Δ into the Verona-transmitted signal, it was possible to make the arrival time at Youngstown correspond to the transmission time of the locally-generated signal. Then, the delay Δ plus the path propagation time τ_2 must add up to approximately an integer number of periods:

$$\tau_2 + \Delta \approx n T_p$$

With synchronized transmissions, as depicted by A and D of Figure 3.10 [or Figure 3.11(a)], the artificially-introduced delay element Δ results in signals at points C and D approximately in synchronism (again refer to Figure 3.10). In Figure 3.11(b), such a situation is illustrated; the delayed transmission depicted by B arrives at Youngstown at time $\tau_2 + \Delta$, as shown in C, at approximately the right time to be closely synchronized with the local signal shown in D. After transmission of either the looped or direct signal on the Youngstown



(a) Simplified Single-Pulse Timing Transfer Diagram



(b) Periodic Pulse Timing Transfer Diagram

Figure 3.11 Timing Diagrams for One-Way and Loop Propagation Time Measurement

to Verona leg, the signals arrive loosely synchronized at Verona, as indicated in E. With this arrangement, the demodulator window need not be altered in its delay position except if τ_1 and τ_2 deviate by tens of bits. Provided the arrival time processor knows which signal is currently being transmitted, it can compute τ_1 or $\tau_1+\tau_2$ as appropriate.

The use of periodic transmissions does introduce the problem of ambiguity when the period T_p is smaller than the propagation times τ_1 or τ_2. The RAKE system was limited to a particular PN sequence of length 255 bits, with the bit rate ranging from 1.25 Mb/s to 10 Mb/s. For compatibility with the MLT-1 modem, we chose a maximum bit rate of 5 Mb/s, resulting in a period of 51 μs. For the Verona-Youngstown path, the free space path delay is on the order of 900 μs with additional delay attributable to the equipment itself. Therefore, the delay τ_1 (or τ_2) is on the order of 20 periods. To reduce the ambiguity, an alternative transmission rate of 1.25 Mb/s was originally contemplated, but later abandoned. Ambiguity resolution was achieved using baseband pulse signals fed directly to the FM modulator radio interface prior to setting up the more precise PN measurement equipment. A resolution of about 1 μs was realized with this approach.

Note that, once the ambiguities are eliminated, the delay variations, $\tau_1(t)$ and $\tau_2(t)$, can be tracked as a function of time by the high-speed probe without the need for repeated ambiguity checks. That is, the delays, τ_1 and τ_2, may vary over several periods of the high-rate sequence provided the variation is smooth and sampled sufficiently rapidly to avoid large jumps.

The full equipment configuration is illustrated in block diagram form in Figure 3.12, and we briefly review the measurement strategy the outlining the sequence of events involved. Assuming that τ_1 and τ_2 are known to be within 10 μs by square wave modulation experiments, the equipment is prepared for operation, and at an instant determined by the 1-pps signal from the atomic clock and the time-select circuitry, the PN sequence generators are started at both ends of the link. The MLT-1 demodulator output is cleared of errors by injection loading into a generator which is switched to load the modem data stream into its register or, alternatively, the feedback generated bit stream, if a satisfactory match between the two is being obtained. The Youngstown switch controls the input to the RAKE demodulator, and alternates between the two PN

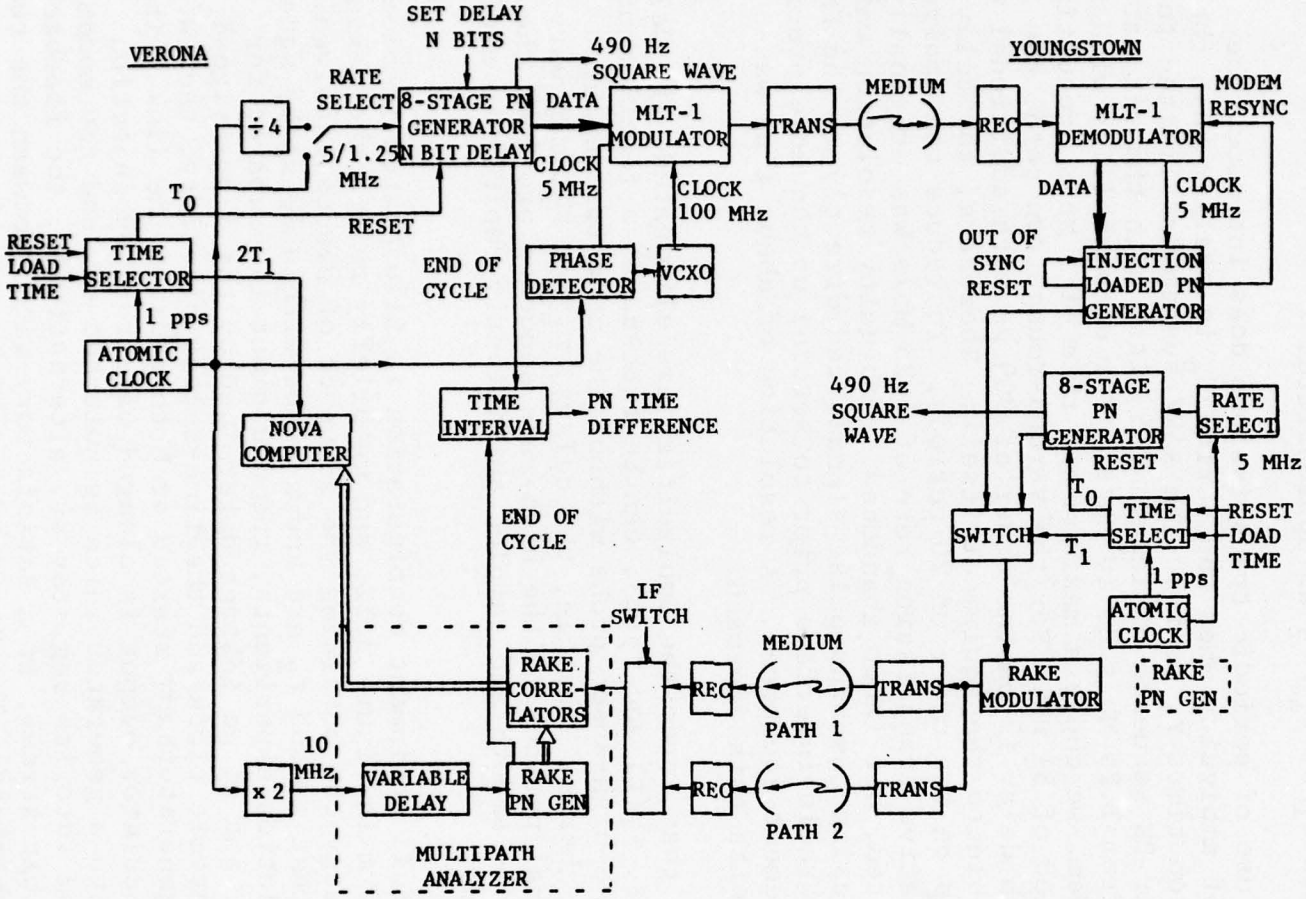


Figure 3.12 Equipment Configuration for Link Delay and Delay Difference Measurements

sequences every two seconds. At the RAKE demodulator, the correlator outputs are observed when the Youngstown PN sequence is being transmitted; the RAKE controls allow the internally-generated PN reference to be delayed in steps of 20 ns, with the stepping rate determined by the setting of front panel controls. The range of sweep rates varies from one 20-ns increment per two seconds to 250 increments per second or, equivalently, 10 ns per second to 5 μs per second. Eventually, sufficient delay will be introduced in the local sequence so that all of the significant received energy is contained within the 10-tap RAKE window. At this point, the manual search can be discontinued. Recall that this synchronization is carried out for the Youngstown-originated PN sequence only. The next step is to adjust the delay in the Verona-originated PN sequence so that it too is received within the same RAKE window. At the point when both signals are captured by the window, a time delay estimate relative to the window is implemented in software for each signal and combined with the known delay Δ. A further time difference measurement must be made, as shown in Figure 3.12. The quantity of interest is equivalent to a fixed delay offset between the Verona transmit PN and the RAKE internal PN sequences. The necessity for its measurement is a consequence of the lack of calibration available in the manual RAKE synchronization procedure. An end of PN cycle signal must be extracted from the internal generator and compared with the end of cycle signal from the node clock PN generator.

With changes in τ_1 and τ_2 over a period of time (e.g., one day), adjustments in both the Verona PN sequence delay and the internal RAKE reference PN are required. The node clocks also drift apart with time because of minute frequency differentials, and this effect alone necessitates infrequent delay corrections. Clock offset of one part in 10^{11}, for example, gives rise to a relative shift in the timing signals amounting to about 35 ns per hour in the worst case. With a RAKE window of 10 taps and bit rate of 5 Mb/s, the temporal width of the window is 2000 ns, while the impulse response is hundreds of ns wide; hence, adjustments because of clock drift are required at most a few times a day.

A detailed block diagram for the Verona site is shown in Figure 3.13.

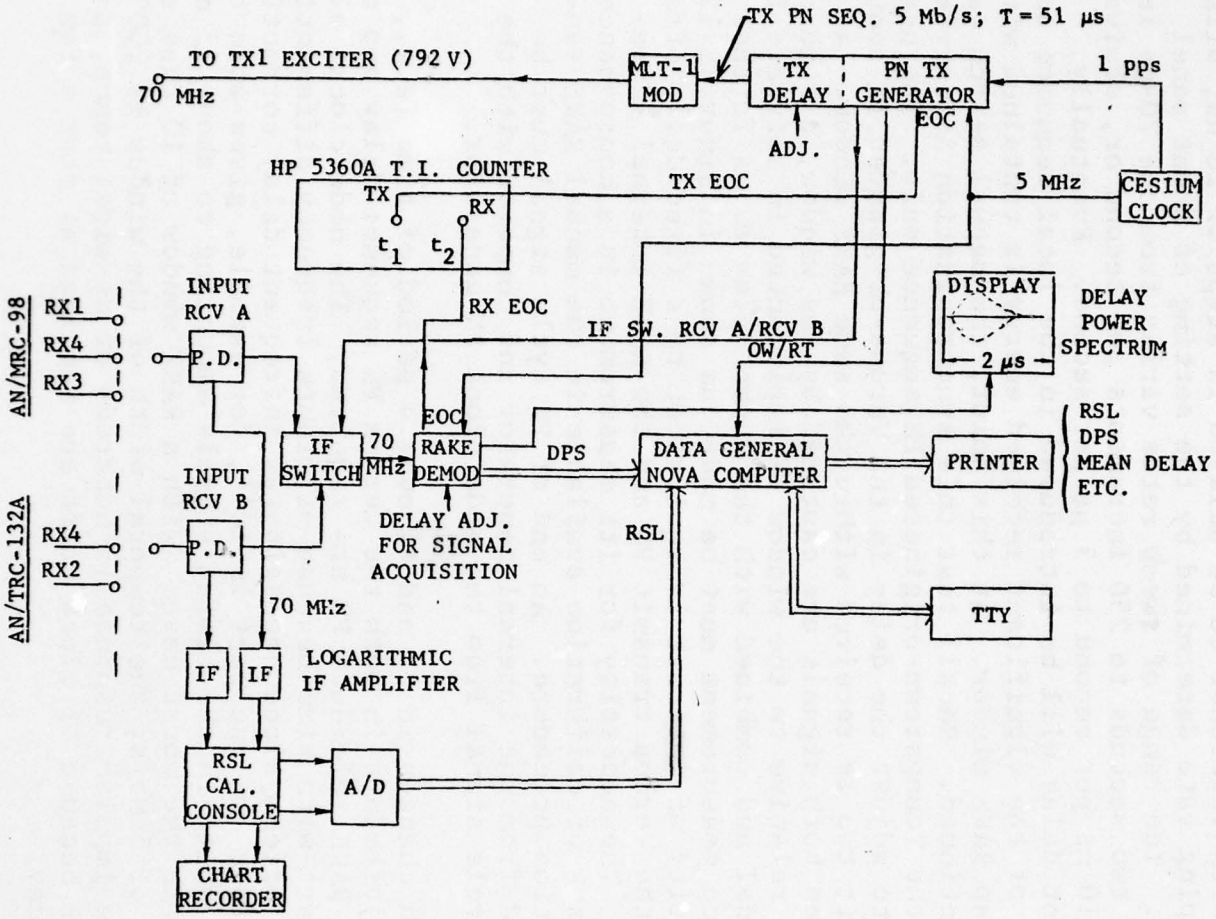


Figure 3.13 Laboratory Setup at Verona Test Site

3.5 Clock Synchronization Experiments

In the final series of tests, the equipment described in Section 3.4 was reconfigured for closed loop clock control experiments.

The link configurations consisted of a tandem master/slave arrangement using a 75-mile line-of-sight loop and a 338-mile troposcatter loop. Figure 3.14 shows the interaction of clock control equipment with the site radio equipment. It can be seen that all network "nodes" were at the Verona site, which allowed easy access to signals required in the evaluation of performance. The Verona node C clock was used to generate a PN sequence for transmission through the LOS loop (via Stockbridge, Ava, and return). At the node B equipment, the incoming PN sequence was regenerated and the end-of-cycle signal applied to the counter, which was an HP 5360 programmed to average 1000 time interval events. This averaging was controlled by means of an external 1-kHz gate signal so that the availability of data from the counter at 1-second intervals provided a periodic 1-pps interrupt request signal for the node processor. The time interval output, representing the difference between a local PN end of cycle and an incoming PN end of cycle, is passed to the microprocessor shown where it is filtered by the clock control algorithm and used to generate a local clock correction signal. This is sent as a frequency control signal to the microstepper which then slews the clock phase in the appropriate direction. The structure and details of the clock control algorithm are discussed in Section 5.3, and will not be pursued any further here.

The second link shown in Figure 3.14 is between Verona nodes B and A; it constitutes a master/slave clock synchronization scheme. The complete LOS/TROPO double link cascade was used for some experiments but, more typically, the LOS and TROPO links were studied separately; in the latter case, by manually setting the microstepper phase control to zero at node B so that the clock there became a master clock for node A.

The objectives of the tests were as follows:

- Investigation of control loop acquisition performance for TROPO and LOS.
- Optimization of steady-state tracking loop parameters to suit the medium characteristics.

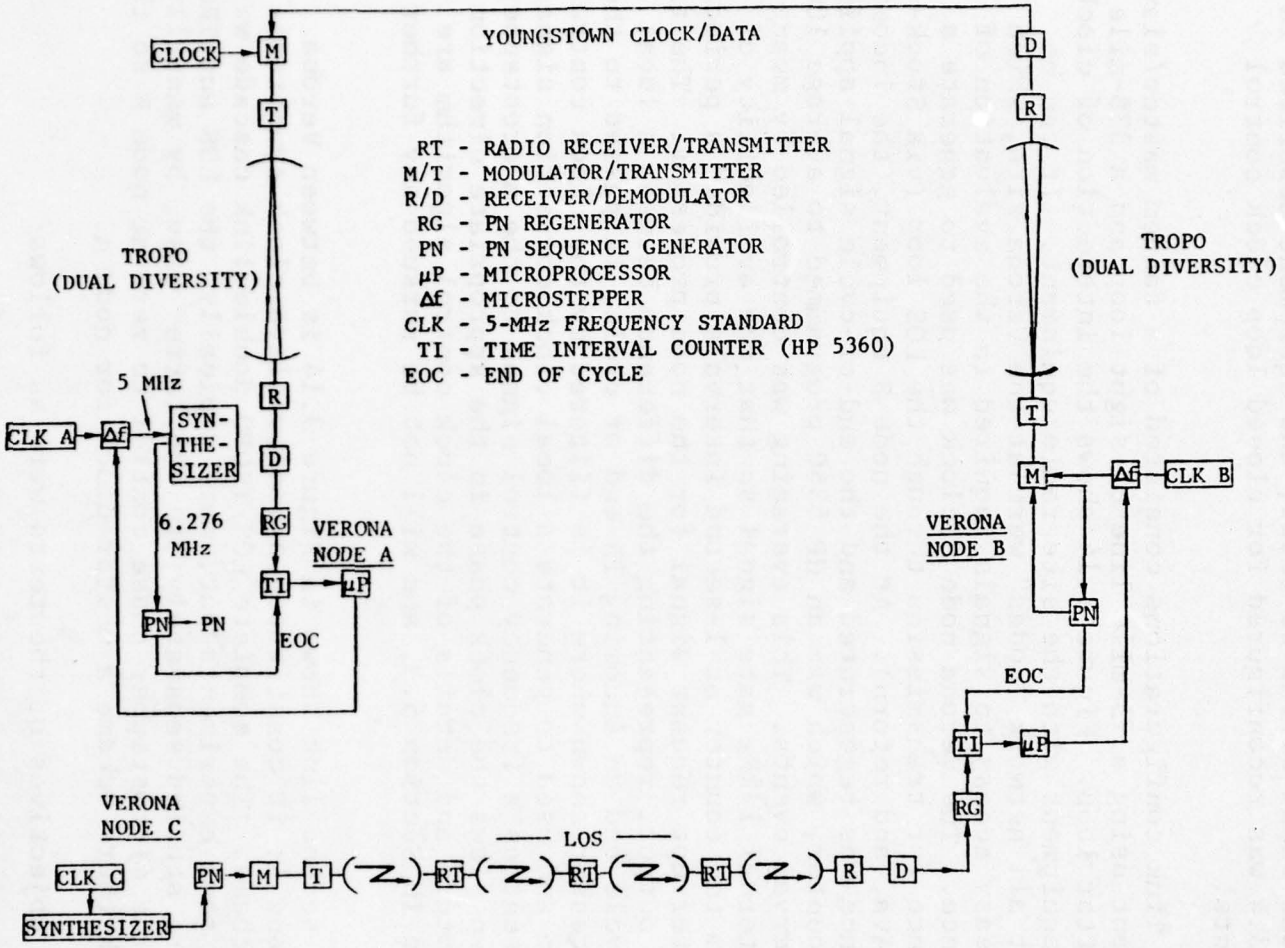


Figure 3.14 Interaction of Timing Subsystem and Radio Equipment

- Evaluation of long-term and short-term path length fluctuations.
- Investigation of the viability of quartz clocks slaved to higher quality master standards, and the transient behavior for switching of incoming timing references.

Most of the results of these tests are presented in Section 5.3 in the form of subsystem design recommendations.

The other equipment aspect of these tests is the performance monitoring issue. While Figure 3.14 shows the radio equipment and interfaces to the clock control components (thereby representing the required timing subsystem portions), additional equipment was required at the Verona site to gauge the relative success of different clock control strategies. Thus, in Figure 3.15, we have shown the interaction of the timing subsystem and a performance assessment subsystem; the latter consisted of external measuring equipment which played no role in the clock correction procedures. The HP5345 time interval counter was connected to two PN end-of-cycle signals for comparison, and the resulting measurement was displayed, printed, and plotted as required.

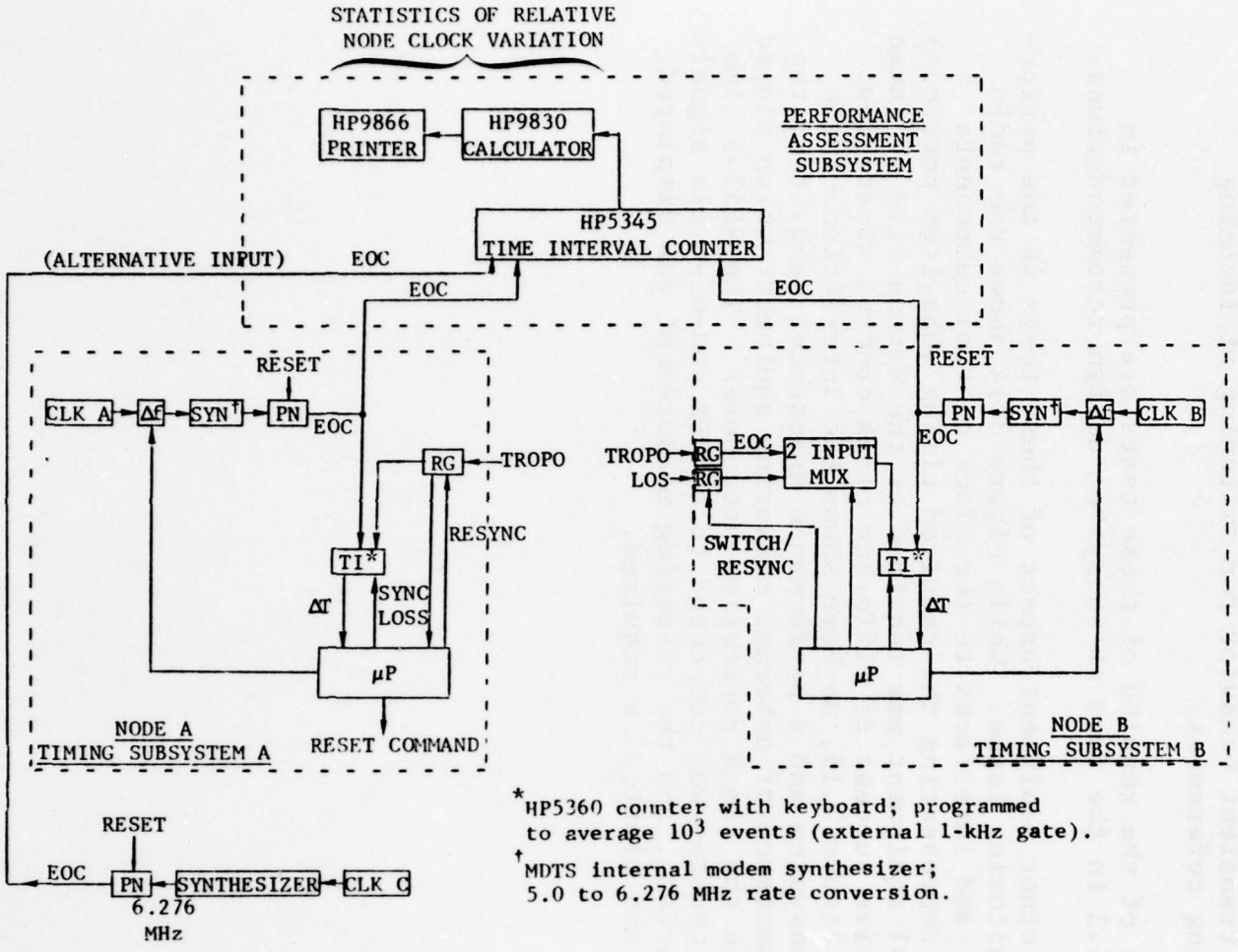


Figure 3.15 Interaction of Timing Subsystem and Performance Assessment Subsystem

SECTION 4

PRESENTATION AND INTERPRETATION OF DATA

The results of the experimental program will now be presented. Where possible, we shall attempt to augment the data with our interpretation of the physical mechanisms that are of importance. The static radio and modem delay tests are discussed first, followed by data on the short-term and long-term medium variability. Finally, we show some of the results of the clock control tests carried out in the last series of experiments.

4.1 TROPO Radio Delay

In an effort to obtain a better understanding of the delay variability occurring in the receiver and transmitter components of the system, a comprehensive set of tests was undertaken with the method described in Section 3.3. The use of a variable frequency tone probing technique was dictated by the desire to obtain preliminary equipment delay data prior to the availability of the digital pseudo-noise (PN) phase-encoded probing system. Furthermore, this approach allows measurement of the FM modulator and demodulator portions of the radio which have a low frequency cutoff at around 100 kHz, thereby ruling out interfaces with the PN equipment.

The main objective was to isolate the various delay components in the transmitter and receiver as far as possible, and to establish the delay sensitivity to carrier offset, temperature and probing tone frequency. Moreover, it was expected that differences in radios of the same family would also be observed.

4.1.1 Delay Tests on the Verona MRC-98 Radios

The first set of equipment delay curves, given in Figure 4.1, shows the results from a series of measurements carried out on the radio pair TX1/RX1 (see Section 3.2 for site layout). Similarly, Figure 4.2 applies to the pair TX2/RX3. In both cases, there are three sets of curves plotted corresponding to the modulator/demodulator loop, the exciter/receiver output loop, and the power amplifier (PA)/ receiver output loop. One curve is plotted for each test

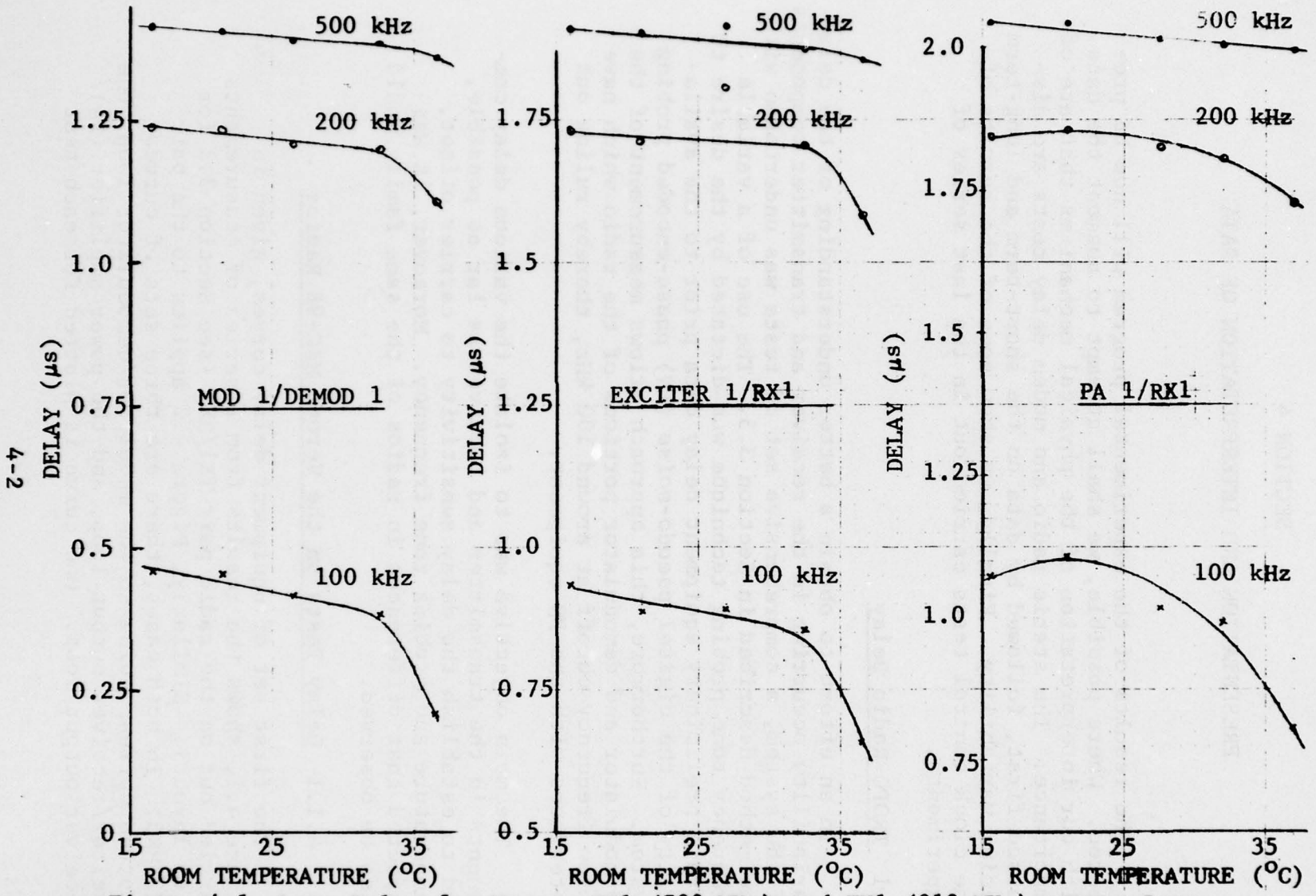


Figure 4.1 Loop Delay for Verona TX1 (792 MHz) and TX1 (912 MHz) versus Room Temperature and Tone Frequency (Run 012)

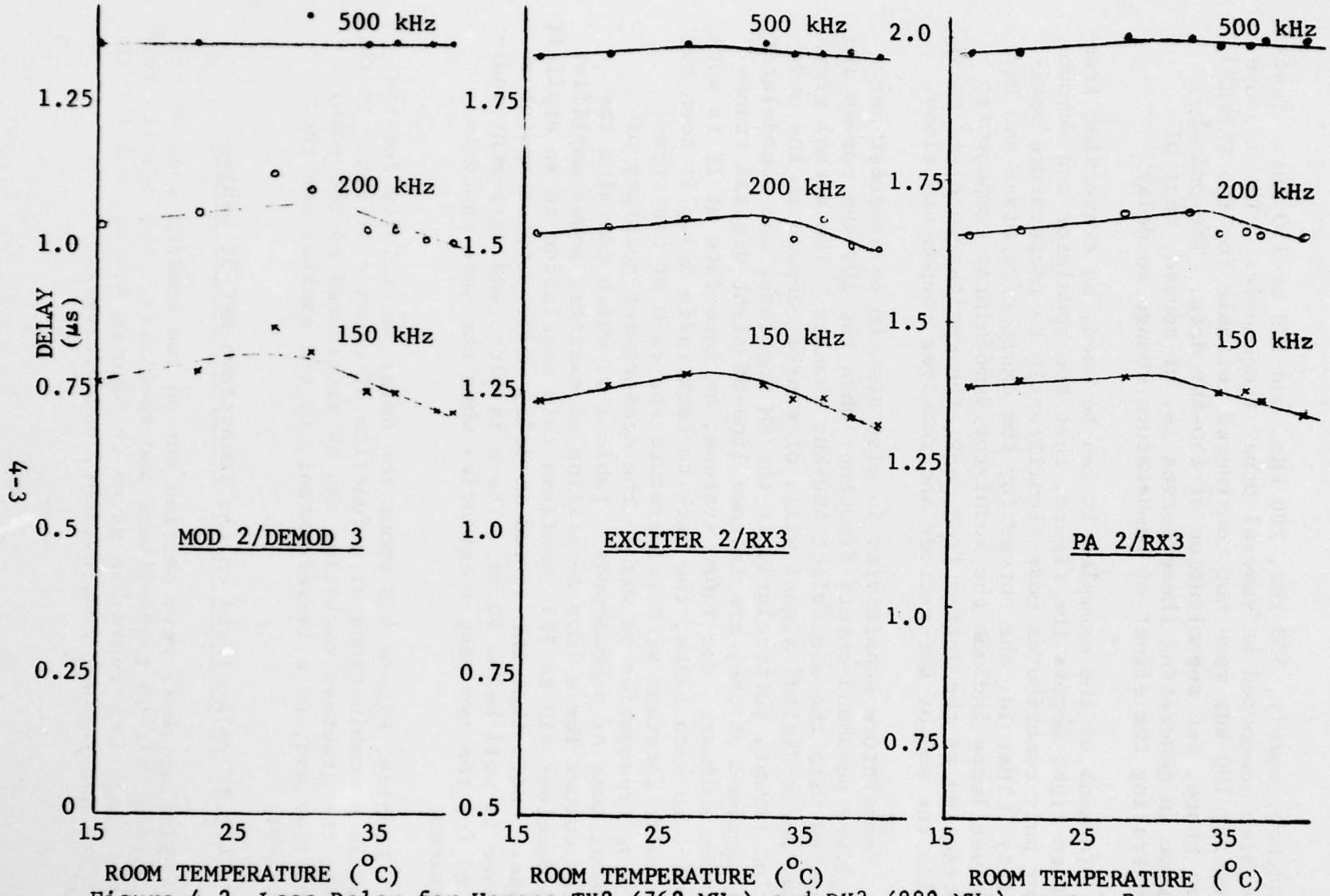


Figure 4.2 Loop Delay for Verona TX2 (762 MHz) and RX3 (882 MHz) versus Room Temperature and Tone Frequency (Run 010)

frequency; namely, 500 kHz, 200 kHz, and 100 or 150 kHz. Tests were also conducted at several other frequencies. The measurements for 100 kHz were not considered reliable for the TX2/RX3 pair; hence, the substitution of 150-kHz data. The primary purpose in generating these curves is, of course, that of illustrating the effect of temperature change on delay.

In most of the examples it can be seen, by traversing from left to right across the figure, that the modulator and demodulator pair contributes most significantly to temperature variability. That is, the curves for the exciter/receiver and PA/receiver loops include the modulator/demodulator components; subtraction of the latter from, say, the exciter/receiver curve yields the sum of the exciter and receiver components alone.

Temperature sensitivity is also seen to be greatest near the lower passband cutoff frequency when the 100-kHz curves are compared with the equivalent 500-kHz results. The actual group delay for a digital signal will, of course, depend on the modulation format, particularly if the FM modulator and demodulator are retained as they are in some line-of-sight digital transmission schemes. For TROPO systems, an interface at IF is more likely; in such cases, the back-to-back radio delay is seen to be almost constant with temperature for each of the three probing frequencies to within the measurement accuracy of several tens of nanoseconds. Table 4-1, which contains the delay values for a loop consisting of exciter, power amplifier and receiver (IF to IF), confirms this conclusion in an explicit manner. Note that the spread in delay values with temperature change is well below 50 ns. There is also good agreement indicated for the two test frequencies when the same radio is compared.

Finally, Figure 4.3 shows the delay sensitivity for the same loop combinations as a function of carrier offset. In this case, the greatest variation can be attributed to the power amplifier and, to a lesser extent, to the exciter and the receiver.

4.1.2 Delay Tests on the Youngstown MRC-98 Radios

Similar tests were carried out on two combinations of the Youngstown MRC-98 transmitters and receivers. The results for the various loop tests are given in Figures 4.4 and 4.5 for the TX2/RX3 and TX1/RX2 combinations, respectively.

TABLE 4-1

LOOP DELAY IN MICROSECONDS FOR VERONA MRC-98 RADIOS REFERENCED TO THE IF INTERFACES

Temperature (°C)	500 kHz		200 kHz	
	TX2/RX3	TX1/RX1	TX2/RX3	TX1/RX1
16	0.618	0.626	0.622	0.601
22	0.615	0.636	0.608	0.622
30	0.645	0.625	-	-
32	0.654	0.620	0.655	0.608
38	0.648	0.634	0.650	0.620
40	0.642	0.594	-	-

Note: Delay includes receiver, exciter, and power amplifier components.

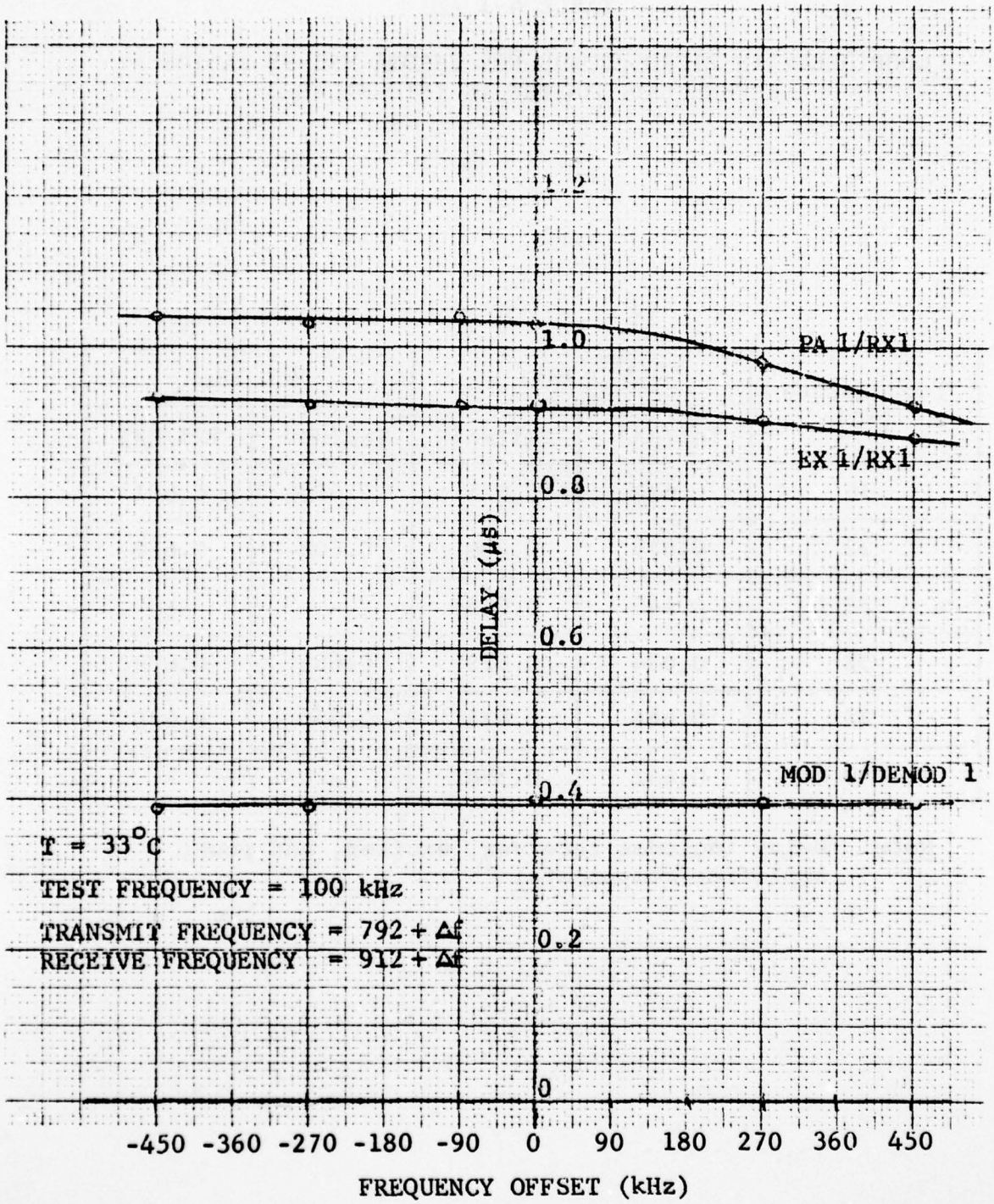


Figure 4.3 Loop Delay for Verona TX1 (792 MHz) and TX1 (912 MHz) versus Carrier Frequency Offset (Run 007)

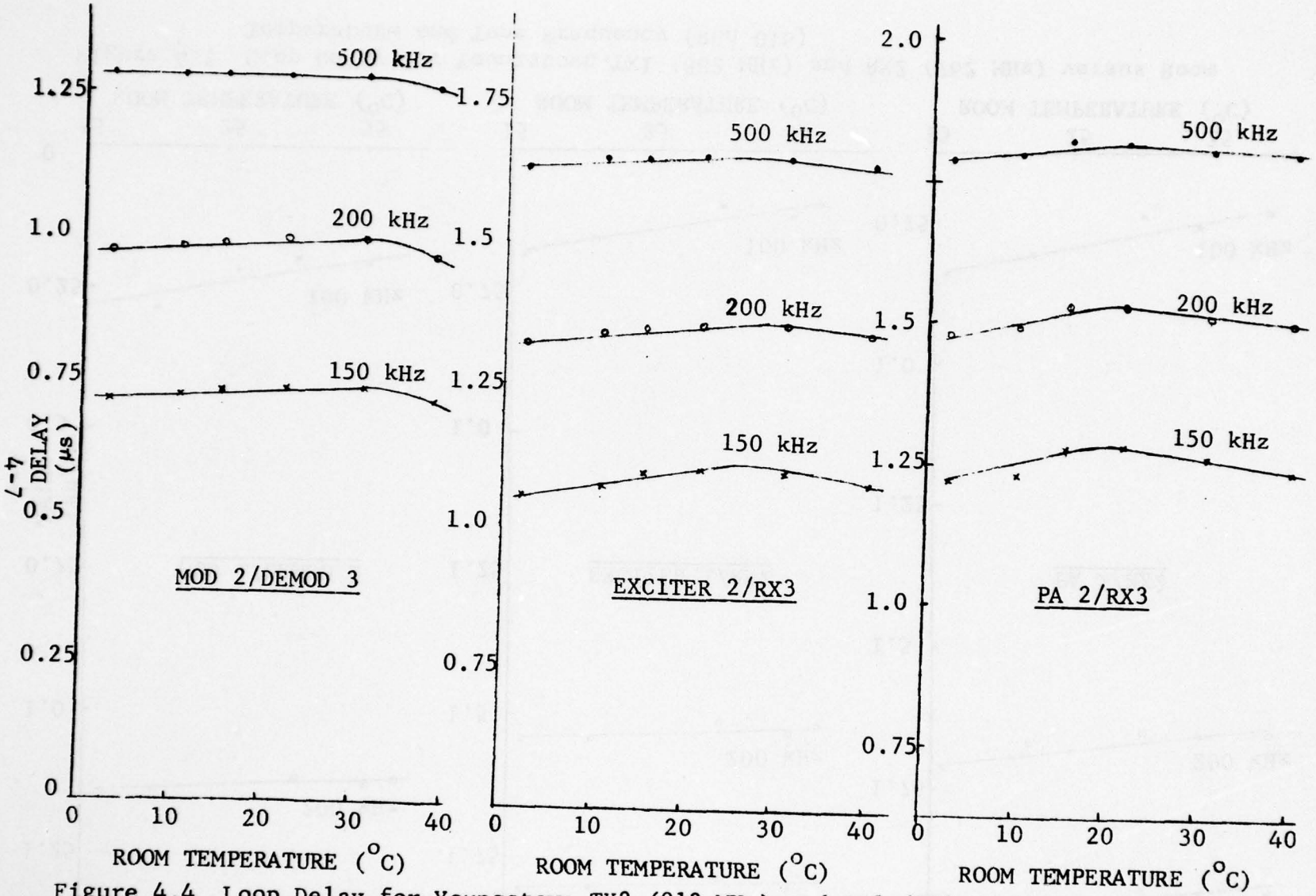


Figure 4.4 Loop Delay for Youngstown TX2 (912 MHz) and RX3 (792 MHz) versus Room Temperature and Tone Frequency (Run 014)

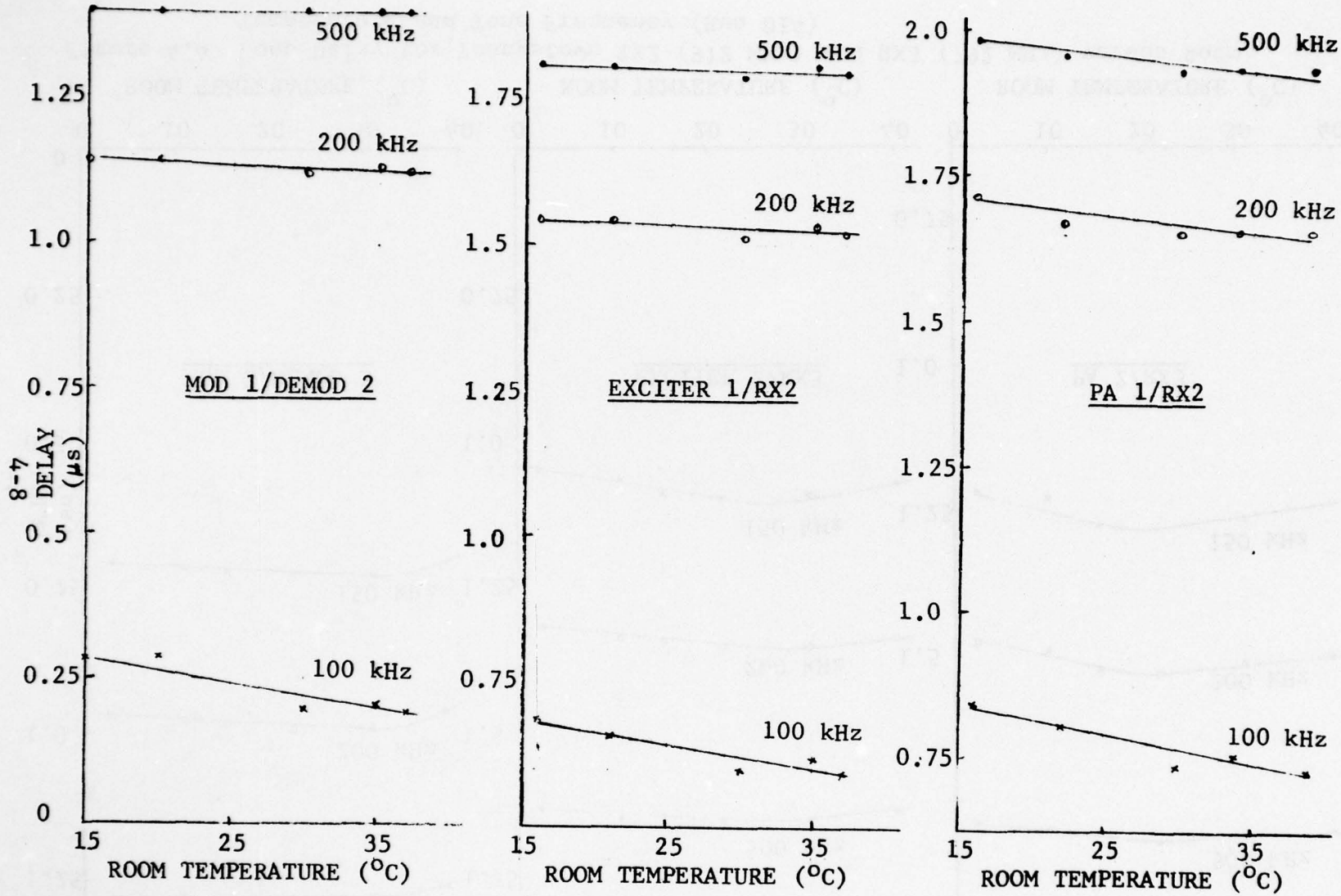


Figure 4.5 Loop Delay for Youngstown TX1 (882 MHz) and RX2 (762 MHz) versus Room Temperature and Tone Frequency (Run 016)

The loop delay at the radio IF interfaces is again summarized in tabular form for 500- and 200-kHz measurement frequencies. Table 4-2 shows the difference between the modulator/demodulator loop and the PA/receiver loop and, as expected from earlier results, the spread is small, generally less than 50 ns. Also, the delays at the two measurement frequencies are close, in almost every case differing by less than 10 ns. This confirms that both temperature and probing frequency sensitivity are confined to the modulator and demodulator units.

When compared with the MRC-98 delays found at Verona, the Youngstown values seem consistently lower by roughly 100 ns for both radios. It is suspected that the difference is attributable to power amplifier tuning variations.

4.1.3 Delay Characteristics of the TRC-132A Radios

The delay measurements carried out on the TRC-132 radios are summarized in Table 4-3, where the back-to-back radio delay is shown as a function of unit, carrier frequency, and tone frequency. All of these measurements were obtained with the narrowband TRC-132 exciter filters in place. Table 4-4 illustrates the delay difference between the narrowband and wideband configurations for a later set of measurements.

4.2 Modem Static Delay Tests

Here we are concerned with the delay through digital modems placed in a back-to-back configuration. It should be appreciated that the digital nature of these devices is likely to result in significant delay effects, both fixed in nature and variable. For the latter category, we refer particularly to the delay uncertainty that arises for certain pieces of equipment as they are switched in and out of service. This is generally a result of buffer and synthesizer initialization variations, and we refer the reader to Appendix A for a full discussion of the subject.

4.2.1 Measured MBS Delay Characteristics for the MDTS Modem

In the final series of tests carried out at RADC, the delay characteristics of two different MDTS modems in back-to-back configurations were evaluated. Particular emphasis was placed on the objective of confirming the delay uncertainties of 1-baud predicted theoretically in Section A3.3 of Appendix A.

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TABLE 4-2

LOOP DELAY IN MICROSECONDS FOR YOUNGSTOWN MRC-98 RADIOS REFERENCED TO THE IF INTERFACES

Temperature (°C)	500 kHz		200 kHz	
	TX2/RX3	TX1/RX2	TX2/RX3	TX1/RX2
2	0.513	-	0.511	-
10	0.519	-	0.518	-
15	0.544	0.582	0.550	0.572
22	0.543	0.555	0.547	0.527
30	0.533	0.536	0.535	0.535
40	0.544	0.540	0.541	0.534

Note: Delay includes receiver, exciter, and power amplifier components.

TABLE 4-3

TRC-132A DELAY MEASUREMENTS AT VERONA AND YOUNGSTOWN
(DELAY IN MICROSECONDS)

		Carrier Frequency (MHz)	400 kHz		500 kHz	
			With Mod/ Demod	Alone	With Mod/ Demod	Alone
Youngstown (20°C)	EX1, PA1 RX2	4500 4900	1.424	0.280	1.440	0.280
Youngstown (20°C)	EX2, PA2 RX1	4690 4790	1.437	0.293		
Verona (25°C)	EX2, PA2 RX1	4900 4500	1.409	0.262	1.421	0.254
Verona (25°C)	EX2, PA2 RX3	4900 4500	1.414	0.267	1.421	0.254

TABLE 4-4

COMPARISON OF NARROWBAND AND WIDEBAND TRC-132 DELAY*

	Frequency (kHz)	Narrowband (With 5-MHz Filter) (μs)	Wideband (Without 5-MHz Filter) (μs)	Change (μs)
EX1, RX2	400	1.359	1.337	0.022
EX1, RX4	400	1.363	1.330	0.033
EX1, RX2	500	1.373	1.345	0.028
EX1, RX4	500	1.373	1.347	0.026

*These delay measurements include arbitrary (but constant) delay components such as connecting cables. The values shown are, therefore, useful only for comparisons of relative delay for the wideband and narrowband configurations.

The transmit and receive times for PN sequences clocked into the two modems at 6.276 and 3.088 Mb/s, respectively, were applied to a time interval measurement setup; with adjustments for cable lengths, etc., the input/output delay was found. The results are tabulated in Table 4-5 for the 6.276-Mb/s modem and in Table 4-6 for the 3.088-Mb/s modem. Note that this represents the delay through the MBS ports. Total delay and delay differentials (for individual runs) are itemized in the above tables.

The various trials consisted of power off/on, station clock (5 MHz) removal and replacement, and simulated loss of sync by severing the IF connection between modulator and demodulator units. In general, the full 1-baud spread in transit times was observed when reinitialization of the MDTS was performed. During loss-of-sync conditions, the stability of clocks in the system was such that no loss of BCI was experienced for reasonable disconnection periods and, as a consequence, the DEMUX frame and output data clocks retained their original relationship when tracking loop sync was regained, resulting in no delay change.

4.2.2 Measured Delay Characteristics of the MLT-1 Modem

A limited amount of testing was carried out in the early stages of the field program to establish delay through the CNR MLT-1 modem. Because of the nature of the synthesizer circuits and the way in which it was provided clock in the field tests, this piece of equipment does not exhibit the delay uncertainty which was found with the MDTS modem. This is primarily because of the absence of an internal radio multiplexer in the MLT-1.

Back-to-back delay tests were carried out at two rates, 5 Mb/s and 1.25 Mb/s. However, the arrangement was such that the modem functioned independently of the user-selected bit rate; data at 1.25 Mb/s was simply repeated to make up the 5 Mb/s modem output rate. Hence, we expect the delay data to be the same for both rates, and this was confirmed experimentally. The results are shown in Table 4-7 for the 5-Mb/s rate tests. The delay values represent 10-second averages. No sync and clock interruption tests were tried since, at that time, we were not aware of the potential delay variations which can result from such action. One column indicates the overall back-to-back delay including the PN generator and synchronizer components. The second column shows the corrected modem back-to-back delay.

TABLE 4-5

MDTS MODEM DELAY AT 6.276 Mb/s
(MDTS UNIT NO. 008)

Run ID	Run Length (mins)	Total Loop Time RXEOC - TXEOC (μs)	Measurement Standard Deviation (ns)	Corrected MDTS Delay (μs)	Deviation from Minimum (ns)	Configuration
A	1	8.1876	1.26	6.606	370	Clock loss
B	1	7.8171	1.25	6.236	0	Clock loss
C	1	8.0414	1.31	6.460	224	Clock loss
D	1	7.9142	1.40	6.333	97	Clock loss
E	1	8.0834	1.41	6.502	266	Clock loss
1	1	8.0478	1.30	6.466	230	Clock loss
2	1	8.0406	1.25	6.459	223	Clock loss
3	1	8.1216	1.41	6.540	304	Clock loss
4	1	8.1122	1.27	6.531	295	Clock loss
5	10	8.1758	0.08	6.594	358	Clock loss
6	5	8.1185	0.11	6.537	301	Loss of Signal Only
7	1	8.1187	1.41	6.537	301	
8	1	7.9524	1.42	6.371	135	Loss of IF Signal Only
9	1	7.9524	1.34	6.371	135	
10	1	8.0214	1.50	6.439	204	Clock loss
11	1	7.9468	1.41	6.365	129	Clock loss
12	1	8.0866	1.44	6.505	269	Clock loss

Corrected MDTS Delay = Total Loop Time - (Cable + TRG Delay)
Cable + TRG Delay = 1.5815 μs
Baud Duration = 319 ns

TABLE 4-6

MDTS MODEM DELAY AT 3.088 Mb/s
(MDTS UNIT NO. 004)

Run ID	Run Length (mins)	Total Loop Time RXEOC - TXEOC (μs)	Measurement Standard Deviation (ns)	Corrected MDTS Delay (μs)	Deviation from Minimum (ns)	Configuration
14	1	11.8223	1.62	10.333	605	Clock loss
15	1	11.5648	1.54	10.076	347	Clock loss
16	1	11.7545	1.52	10.265	537	Clock loss
17	1	11.3121	1.55	9.823	94	Clock loss
18	1	11.2173	1.48	9.728	0	Clock loss
19	1	11.8246	1.50	10.335	607	Clock loss
20	1	11.3754	1.47	9.886	158	Clock loss

Corrected MDTS Delay = Total Loop Time - (Cable + TRG Delay)

Cable + TRG Delay = 1.4888 μs

Baud Duration = 647 ns

TABLE 4-7

BACK-TO-BACK MLT-1 TROPO MODEM DELAY
(IN MICROSECONDS)

Data Rate = 5 Mb/s

Trial	Measured Delay	Net Modem Back-to-Back Delay
1	32.7767	25.908
2	32.7762	25.907
3	32.7775	25.909
4	32.7748	25.906
5	32.7765	25.908
6	32.7761	25.907
7	32.7761	25.907
8	32.7770	25.908

Modem Delay = Measured Delay - PN Generator Delay
= Measured Delay - 6.869 μs

4.3 TROPO Modem/Medium Jitter

The troposcatter medium can be thought of in terms of two different time scales. The first is related to meteorological effects occurring over time periods of 10 minutes or more, while the second time scale is associated with the short-term fading occurring at rates as high as several fades per second. We are concerned here with the latter. Long-term path length variations are covered in Section 4.4.

Bit synchronization circuits are provided in digital modems to accommodate the timing variations caused by the propagation medium and the timing clock at the transmitter. The function of the sync circuit is generally to smooth out short-term timing jitter present on the received signal so that only the long-term effects are tracked. For TROPO channels, residual jitter occurs as a result of the multipath propagation as well as receiver noise, whereas for LOS channels, the main concern is with receiver noise and data-induced noise. Our discussion here is concerned primarily with TROPO timing jitter, and we first review the bit tracking loops which are likely candidates for use in digital TROPO links.

The elements of a bit sync tracking loop include a time discriminator, a VCO, and a loop filter. The time discriminator provides an error signal indicating the size and polarity of the timing difference between the input data signal and the VCO output. This error signal filtered by the loop filter is used to control the VCO so that the error signal is minimized.

The various bit sync systems differ primarily in the nature of the time discriminator. The time discriminator can, for example, be based upon the explicit calculations of the different kinds listed below:

(a) Centroid calculation of the combined diversity or individual impulse response energy distributions.

(b) Split gate or median discriminator using impulse response energy distribution.

(c) Curve fit maximum picker, with the smoothed impulse response energy distribution.

These techniques assume that a channel measurement process is taking place continuously. This may be done by transmission

of a low-level PN (pseudo-noise) probing signal and cross correlation at the receiver with delayed replicas of the PN sequence, or by means of decision-directed operations. A channel measurement subsystem, such as discussed above, must be available as part of a TROPO link modem to provide a measurement of samples of the impulse response for each diversity channel. Since the channel is randomly time-varying, its distribution of energy vs. path delay may bunch up at early delays (or later delays) resulting in a slow change in group delay which can be several bits for the longer troposcatter links.

The nature of the processing in currently-available high-speed TROPO modems is such that quite wide timing excursions are legitimate in order to accommodate the time-varying nature of the impulse response. Consider, for example, the measured MDTS modem tracking loop jitter shown in Figures 4.6 through 4.11. The first three curves apply to the 6.276-Mb/s MDTS modem, while Figures 4.9 - 4.11 are for an MDTS running at 3.088 Mb/s. At the lower bit rate, a narrower bandwidth is used with corresponding improvement in signal-to-noise.

The timing jitter shown in Figure 4.6 is for the master/slave TROPO portion of Figure 3.14. A cesium standard at node B was used as a reference for the cesium clock at node A after passage through the MRC-98 Verona/Youngstown/Verona cascade. Although this was a clock control experiment, the short time constant used ensures that most of the medium/modem interaction is unaffected. At about 330 seconds into the run, the modem sync loss light came on, and the tracking loop apparently started searching for a new stable operating point. During this period, the error rate reached 10^{-1}, whereas the error rate was in the vicinity of 10^{-3} at the start and end of the run.

Similar effects are seen in Figure 4.7 which is set up with the same loop parameters. It should be noted that two modems are involved in these experiments, one at Youngstown and the second at Verona. Timing variations in the first will be reflected in the output of the second. Variations depicted in Figure 4.7 are on the order of a complete baud (319 ns) from the nominal time difference of 1000 ns. In this run, the error rate went to its maximum value (10^{o} on the meter; interpreted as $\frac{1}{2}$ in practice) during most of the peak and valley excursions, after being at the 10^{-3} level at the start of the run.

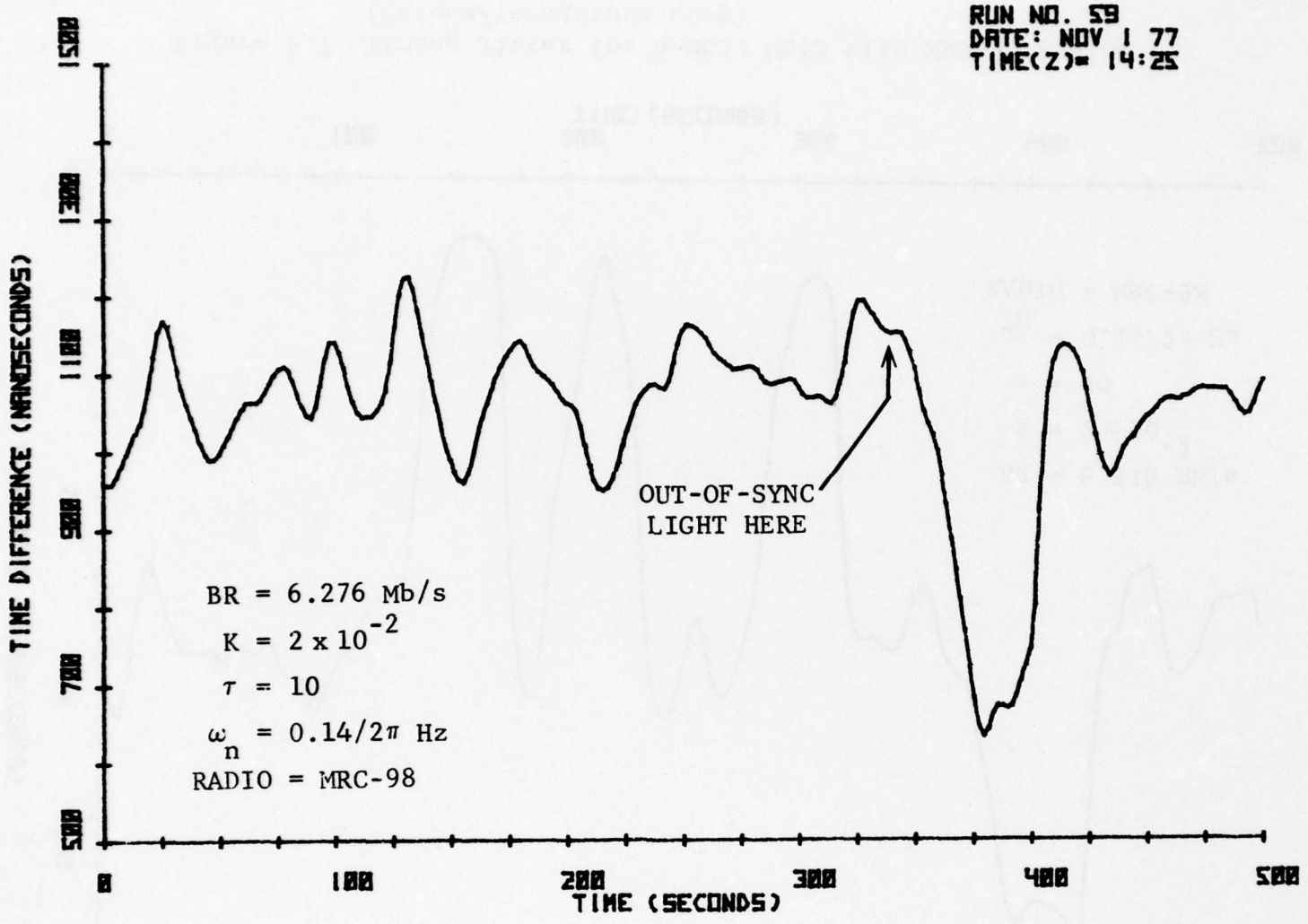


Figure 4.6 Timing Jitter for 6-Mb/s MDTS with MRC-98 Radios (Verona/Youngstown Loop)

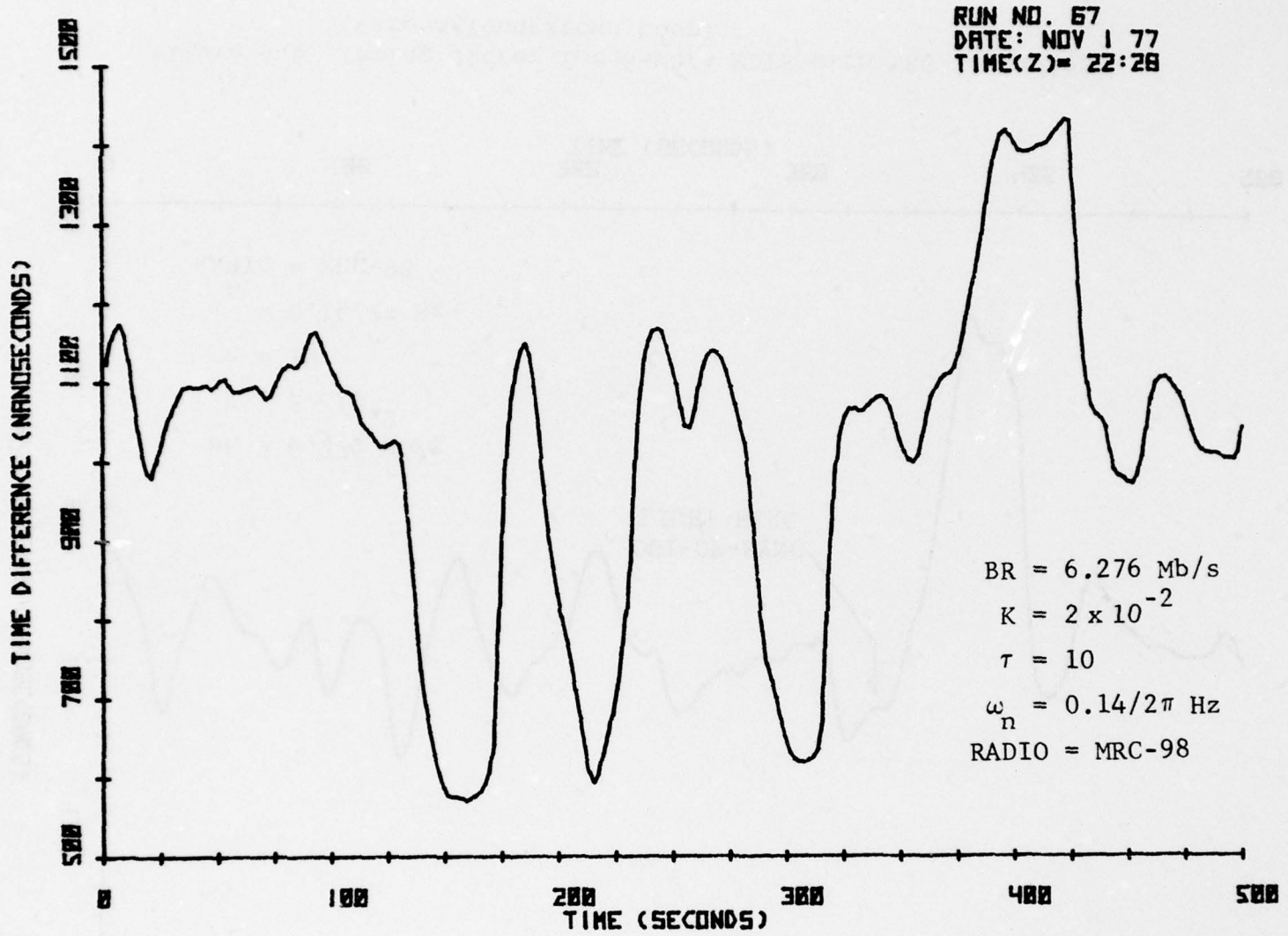


Figure 4.7 Timing Jitter for 6-Mb/s MDTS with MRC-98 Radios (Verona/Youngstown Loop)

Figure 4.8 differs from the previous two figures in that it represents the open loop timing jitter. By this we mean that at node A of Figure 3.14 the microprocessor phase control was locked at zero manually, and the variable incoming PN timing was compared with the stable PN sequence generated locally. Thus, Figure 4.8 shows the pure medium and modem effects; there is no additional averaging as a result of the clock control loop. It can be seen that the timing fluctuations are a little more rapid than in Figures 4.6 and 4.7, indicating some effective smoothing for the closed loop results. Once again we also see a 1-baud jump effect in the timing jitter which corresponded to the loss-of-sync indication after about 160 seconds. The error rate was between 10^{-3} and 10^{-4} at the start of the run.

Now we present results for the other MDTS modem which was run at 3.088 Mb/s. This modem was set up on the TRC-132 radios for these tests. At the C-band frequencies, a higher signal strength can be realized, while the lower bit rate allows signal-to-noise ratio enhancement by virtue of the lower bandwidth requirements. In Figure 4.9, for example, the received signal level was about -87 dBm, while earlier MRC-98 runs were with RSL values of between -92 and -98 dBm. This figure indicates open loop jitter for the modem amounting to $\pm$ 20 ns peak-to-peak. The measured error rate was 10^{-4}. Soon after this run was completed, a 20-minute run was executed to establish the statistical properties of the jitter process. The recorded 20-minute mean and standard deviation were:

20-minute mean = 55.984 μs

20-minute standard deviation = 25.99 ns

However, the minute-by-minute standard deviations showed quite significant variability, as indicated in Table 4-8. The notes made at the time included the comment that, while error rates were normally 10^{-4}, there was a period of about 10 minutes into the run when an error rate of 10^{-6} was in effect.

Figure 4.10 is another example of the open loop medium/modem jitter at 3.088 Mb/s. The scale has been expanded to give a more detailed view of the jitter behavior, but the plot is basically the same as the one in Figure 4.9 with a peak-to-peak variation of around 20 ns.

Finally, in Figure 4.11 we show one of the few examples available of a large timing excursion for the 3-Mb/s tests. This run was closed loop so the variability is smoother and

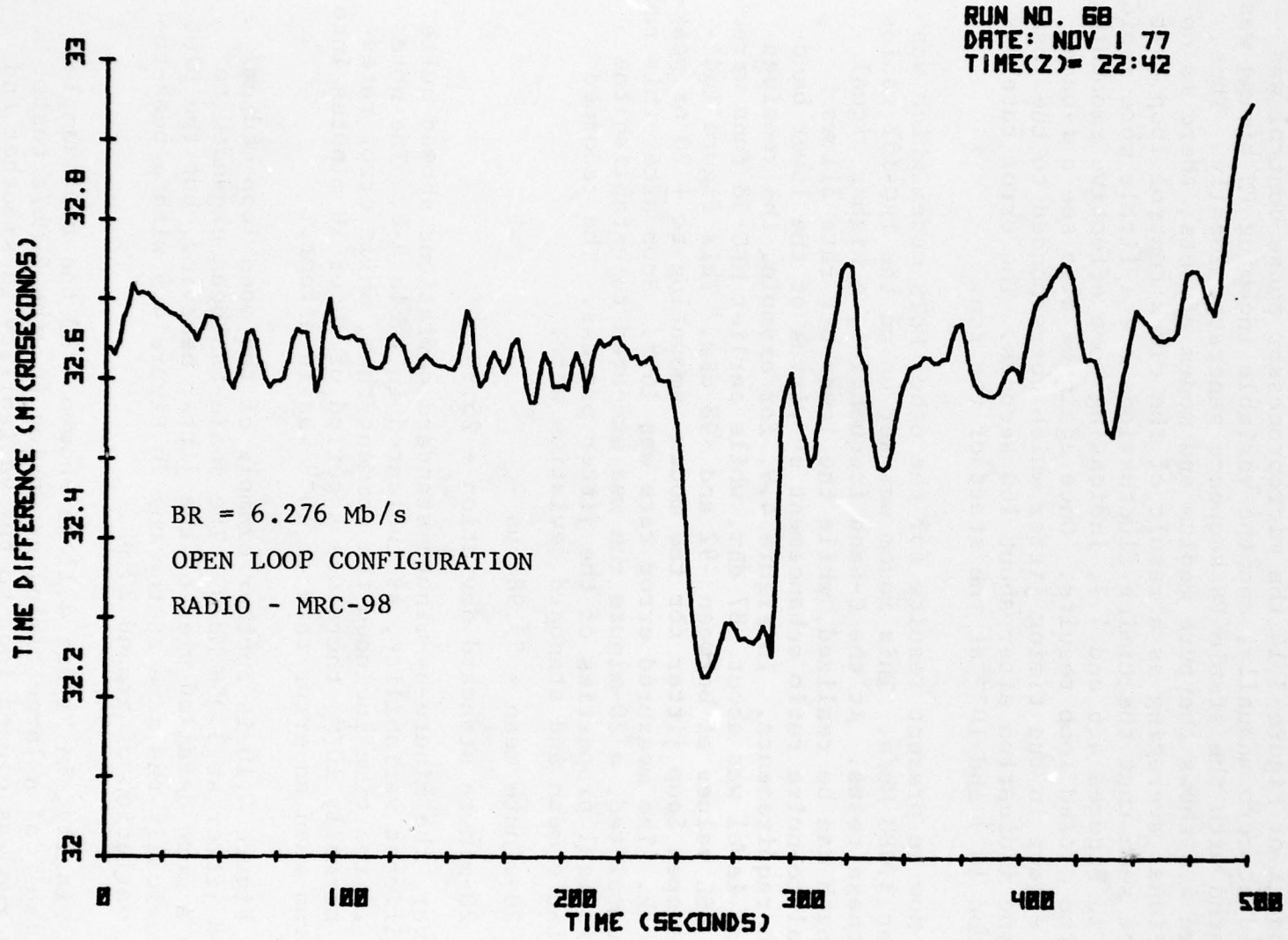


Figure 4.8 Open Loop 6.276-Mb/s MDTS Timing Jitter with MRC-98 Radios (Verona/Youngstown Loop)

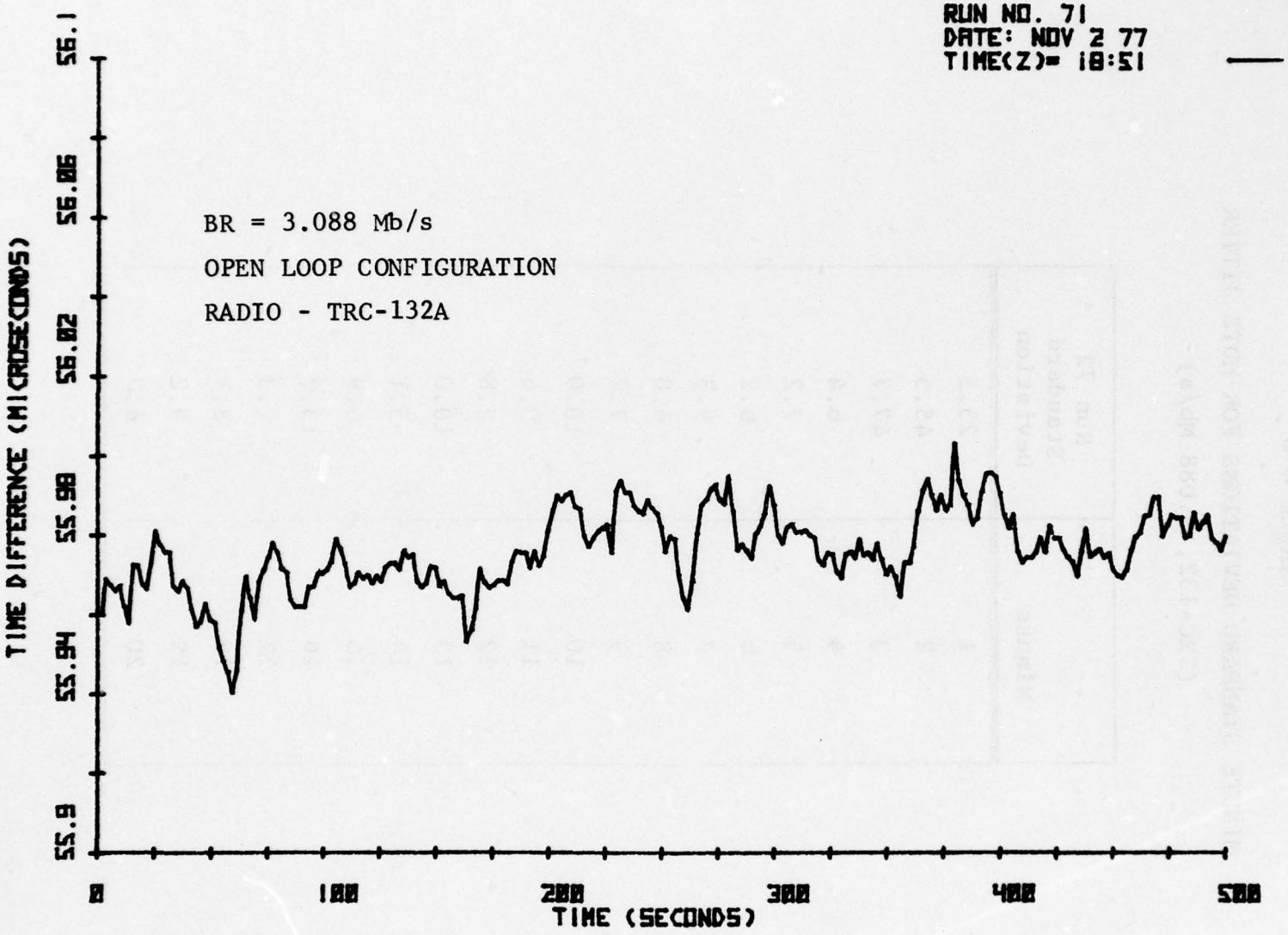


Figure 4.9 Open Loop 3.088-Mb/s MDTS Timing Jitter with TRC-132A Radios (Verona/Youngstown Loop)

TABLE 4-8

MINUTE STANDARD DEVIATIONS FOR MDTS JITTER

(TRC-132, 3.088 Mb/s)

Minute	Run 72 Standard Deviation
1	25.5
2	45.5
3	47.7
4	6.4
5	7.2
6	6.2
7	9.3
8	6.0
9	7.2
10	10.0
11	9.6
12	5.8
13	10.0
14	5.1
15	6.9
16	13.6
17	7.3
18	8.1
19	9.2
20	6.7

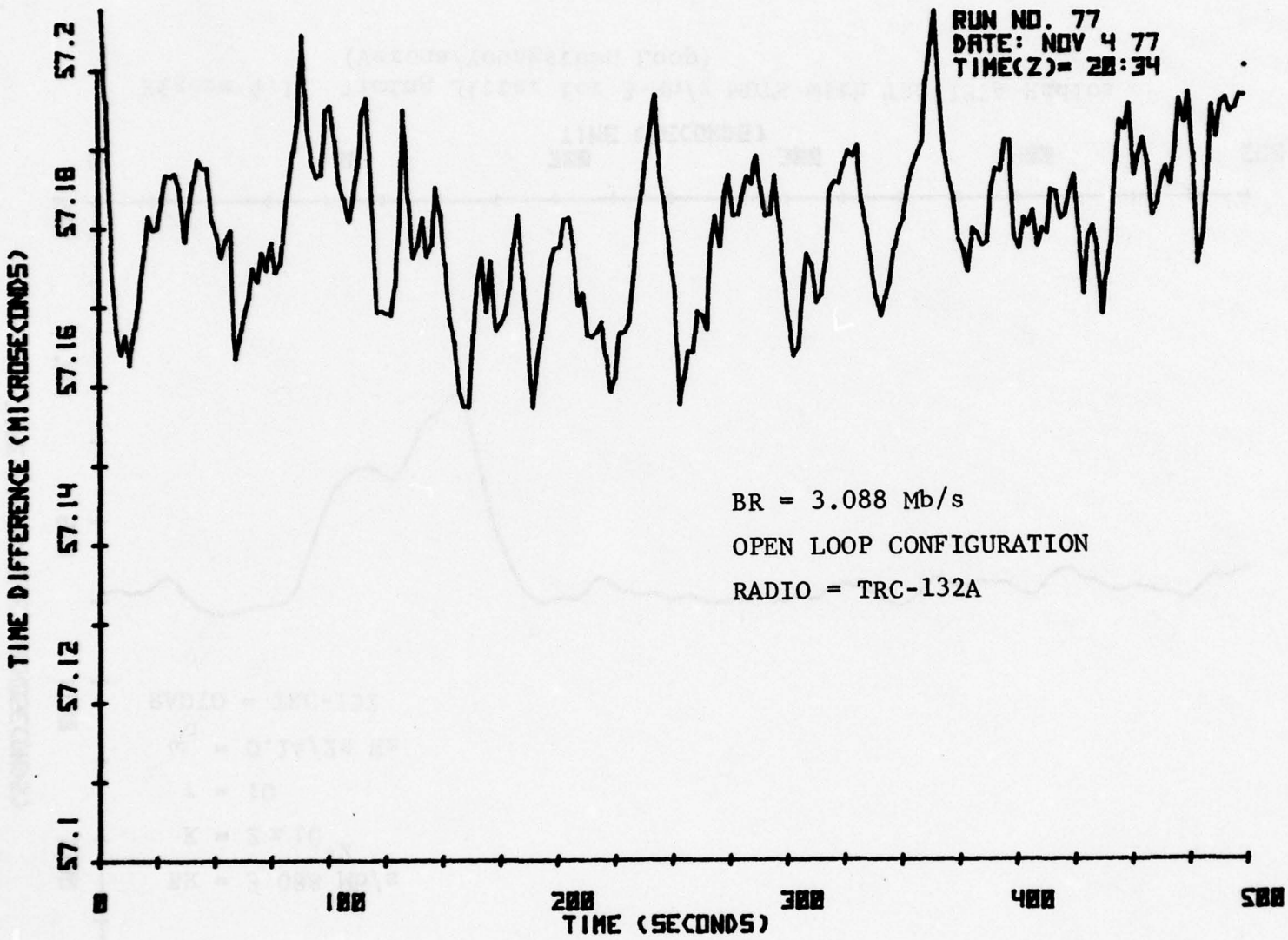


Figure 4.10 Open Loop 3.088-Mb/s MDTS Timing Jitter with TRC-132A Radios (Verona/Youngstown Loop)

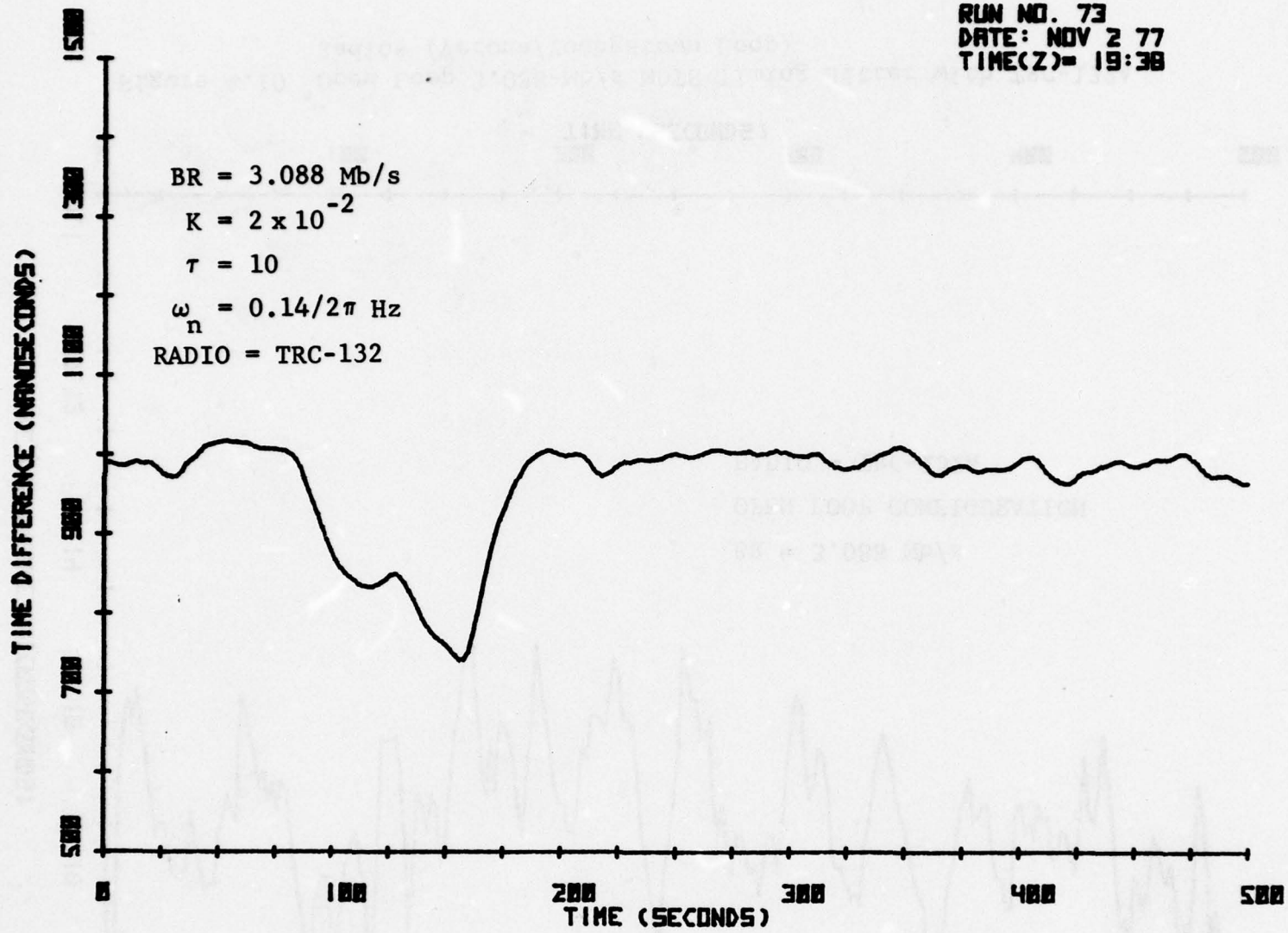


Figure 4.11 Timing Jitter for 3-Mb/s MDTS with TRC-132A Radios (Verona/Youngstown Loop)

not as pronounced as in the open loop examples. The modem error rate was between 10^{-5} and 10^{-6} during the run. For a subsequent run of about 10 minutes duration, the jitter showed no further excursion tendencies, but was confined to a narrow ripple range of about $\pm$ 10 ns, as in the later portions of Figure 4.11.

4.4 TROPO Path Delay

For the network synchronization techniques discussed in Section 2, it was established that medium and equipment delay variations control the system performance. For single-ended systems, variability around a long-term mean, in terms of both magnitude and spectral width, is the essential ingredient. However, the concept of a known long-term mean will be suspect in most operational systems, and the magnitude of residual biases must also be estimated. Double-ended transfer methods depend for their success on similar parameters expressed instead in terms of bidirectional path delay differences; namely, the time structure and magnitude of the difference, along with residual biases which are not accounted for a-priori.

One-way and bidirectional delay parameters have been investigated for TROPO links at the RADC test facilities over a period of a year, with measurements carried out over a range of conditions encompassing seasonal, temperature, operating frequency, signal level, and diversity angle effects. The temporal behavior of various links has been studied with averaging times ranging from seconds up to 20 minutes, and data records often extending over 3- or 4-day periods.

Before presenting the results of these tests, we should make some general comments about the troposcatter propagation mechanism.

4.4.1 General TROPO Propagation Considerations

The usual assumptions invoked when deriving theoretical models for troposcatter paths include a linear inhomogeneous weak-scattering medium, separating two antennas which are not within line-of-sight to one another. As a result of the weak-scattering assumption, a single scattering model is normally used, with the refractivity inhomogeneities causing the scattering attributed to temperature, pressure, and water vapor variations in the atmosphere. The linearity assumptions allow the link to be characterized in terms of its (time-varying)

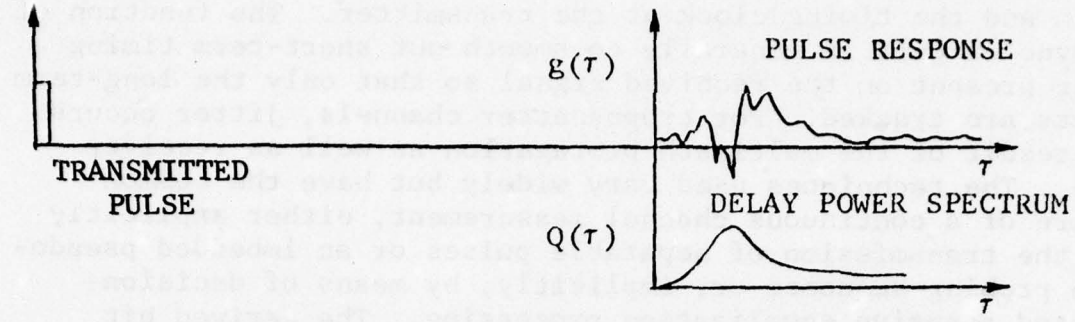
pulse response $g(\tau)$ and, with some further very weak assumptions of the scattering mechanism, the process $g(\tau)$ can be described as a stationary Gaussian process with zero mean and second-order characteristic:

$$E\left\{|g(\tau)|^2\right\} \propto Q(\tau)$$

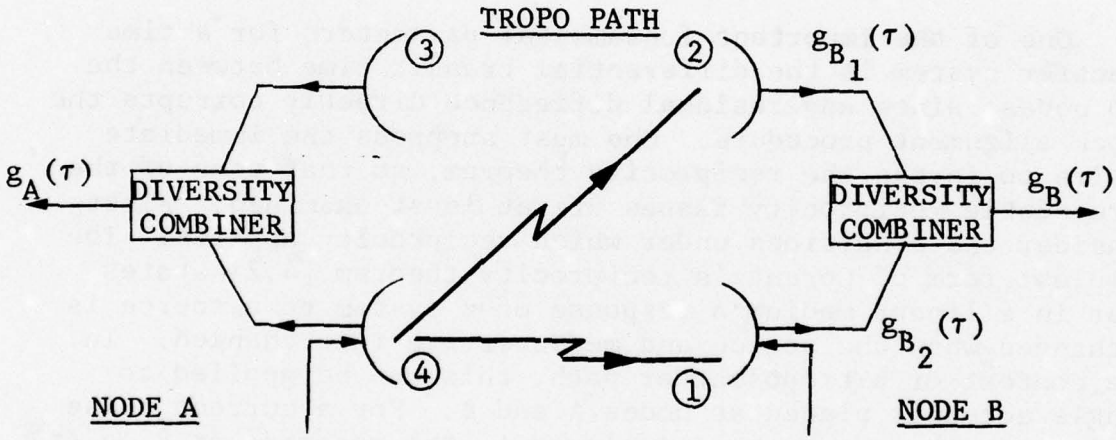
where E denotes statistical expectation and Q is the power density versus delay [4.1]. The functions $g(\tau)$ and $Q(\tau)$, which are depicted in Figure 4.12(a), typically extend over several hundred nanoseconds. A more complete statistical description of the received TROPO signal can be formulated, but is not required here.

As discussed earlier, it is convenient to associate two different time scales with the quantities g and Q. Typically, the pulse response $g(\tau)$ varies rapidly over a period of seconds, depending on wind conditions, link geometry, and frequency of operation. A second time variation is, in effect, a deviation from the stationarity condition normally claimed. Large-scale meteorological influences, typically seasonal or diurnal in nature, give rise to changes in the shape of average characteristics such as $Q(\tau)$. A precise time-scale delineation of the two medium variation classes is not possible, but for measurement purposes the medium is usually considered to be stationary over nominal intervals of 20 minutes.

Even when the time-varying pulse response and its second-order statistic $Q(\tau)$ provide an adequate characterization of the troposcatter medium, there is clearly some difficulty in defining time of arrival for a hypothetical transmitted time reference pulse. An instantaneous arrival time parameter can be defined, for example, in terms of the response leading edge, energy centroid, energy median (early/late), or function maximum; and in sympathy with $g(\tau)$, the parameter will exhibit fluctuations of a short-term nature. Furthermore, while two similar paths (e.g., forward and return) might have the same profile $Q(\tau)$, their instantaneous arrival time parameters could be quite different. Fortunately, in digital network applications one is normally relieved of the philosophical burden of defining transit time for multipath transmissions by the presence at every link termination of a bit synchronization tracking loop.



(a) Troposcatter Link Response Characteristics



(b) Dual Diversity Link Example

Figure 4.12 Troposcatter Link Reciprocity Considerations

Bit synchronization circuits are provided in digital modems to accommodate the timing variations caused by the propagation medium and the timing clock at the transmitter. The function of the sync circuit is generally to smooth out short-term timing jitter present on the received signal so that only the long-term effects are tracked. For troposcatter channels, jitter occurs as a result of the multipath propagation as well as receiver noise. The techniques used vary widely but have the common feature of a continuous channel measurement, either explicitly with the transmission of separable pulses or an imbedded pseudo-noise probing sequence or, implicitly, by means of decision-directed adaptive equalization processing. The derived bit clock, therefore, responds to both short-term and long-term path length changes. An equivalent of the time transfer configuration is obtained when marked bits in the data stream, such as multiplexer frame patterns, are used as time-of-arrival events.

One of the important fundamental parameters for a time transfer system is the differential transit time between the two nodes, since any residual difference directly corrupts the clock alignment procedure. One must suppress the immediate desire to invoke the reciprocity theorem, so that some of the more subtle reciprocity issues are at least examined. First consider the conditions under which reciprocity applies. The simplest form of Lorentz's reciprocity theorem [4.2] states that in a linear medium a response of a system to a source is unchanged when the source and measurer are interchanged. In the context of a troposcatter path, this can be applied to single antennas placed at nodes A and B. For a current pulse applied to the antenna terminals at A, the response at B, $g_B(\tau)$, will be identical to the response at A, $g_A(\tau)$, for a pulse originating at B. This will not necessarily be true, however, if the antennas are interchanged along with the source. Other factors of interest in a search for potential nonreciprocal effects can be listed as follows:

(1) Transmissions in opposite link directions will generally be on different (albeit close) carrier frequencies.

(2) Space diversity transmission configurations violate the assumptions necessary for application of the reciprocity theorem. Consider the example of Figure 4.12(b) where we use a single current source at node A to generate two port outputs, $g_{B_1}(\tau)$ and $g_{B_2}(\tau)$, at node B.

A composite signal, $g_B(\tau)$, is then formed in the diversity combiner. Transmission in the reverse direction (from B to A) normally uses only one of the B node antennas, with reception on two antennas at node A. Generally, there will not be correspondence between the two diversity combined responses $g_A(\tau)$ and $g_B(\tau)$ for the same current pulse transmission. A simple physical demonstration of this would involve rotating antenna ① 90° so that antennas ③ and ④ receive very little signal. In the other direction, g_{B_2} will also be greatly diminished but the composite output g_B will be nonzero because of the path from ④ to ②.

(3) Even with radios from the same family, differences in tuning and temperature will result in some path delay asymmetry. For example, if receivers are more sensitive to temperature than transmitters, complementary delay/temperature effects will not be exhibited for the two path directions.

With favorable geometry and recourse to some mild assumptions, it is often possible to demonstrate that the paths from A to B, and vice versa, will have the same delay power profile $Q(\tau)$ if not the same instantaneous pulse response $g(\tau)$. In the experimental program to be described next, the emphasis was on long-term one-way link delay and bidirectional delay asymmetries.

4.4.2 Troposcatter Path Delay Data

We consider now the one-way and round-trip delay measurements taken with the time-multiplexed configuration illustrated in Figure 3.12. The emphasis here is on longer averaging periods, typically 20 minutes, to eliminate the short-term fluctuations, such as those shown in Section 4.3. Furthermore, all of the equipment delay components have been edited out of the data so that pure path delay is obtained.

The results for a three-day acquisition period are presented in Figures 4.13 through 4.16. Each point plotted represents a 20-minute average of transmit time. A direct comparison between the forward path at 792 MHz and the return path at 912 MHz is shown. The forward path is indicated on the graphs

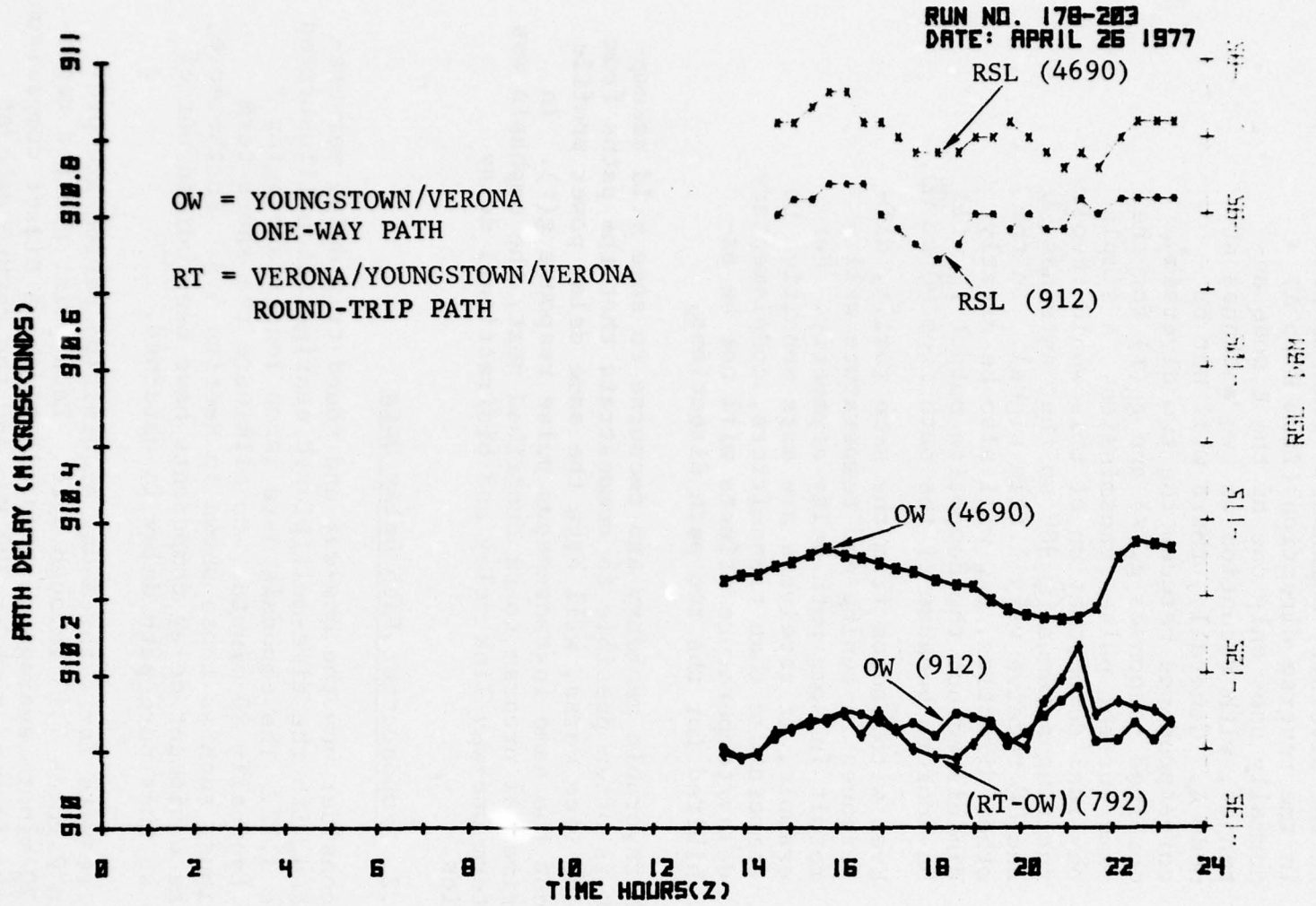


Figure 4.13 1-GHz/4-GHz TROPO Path Delay and RSL Data (April 26)

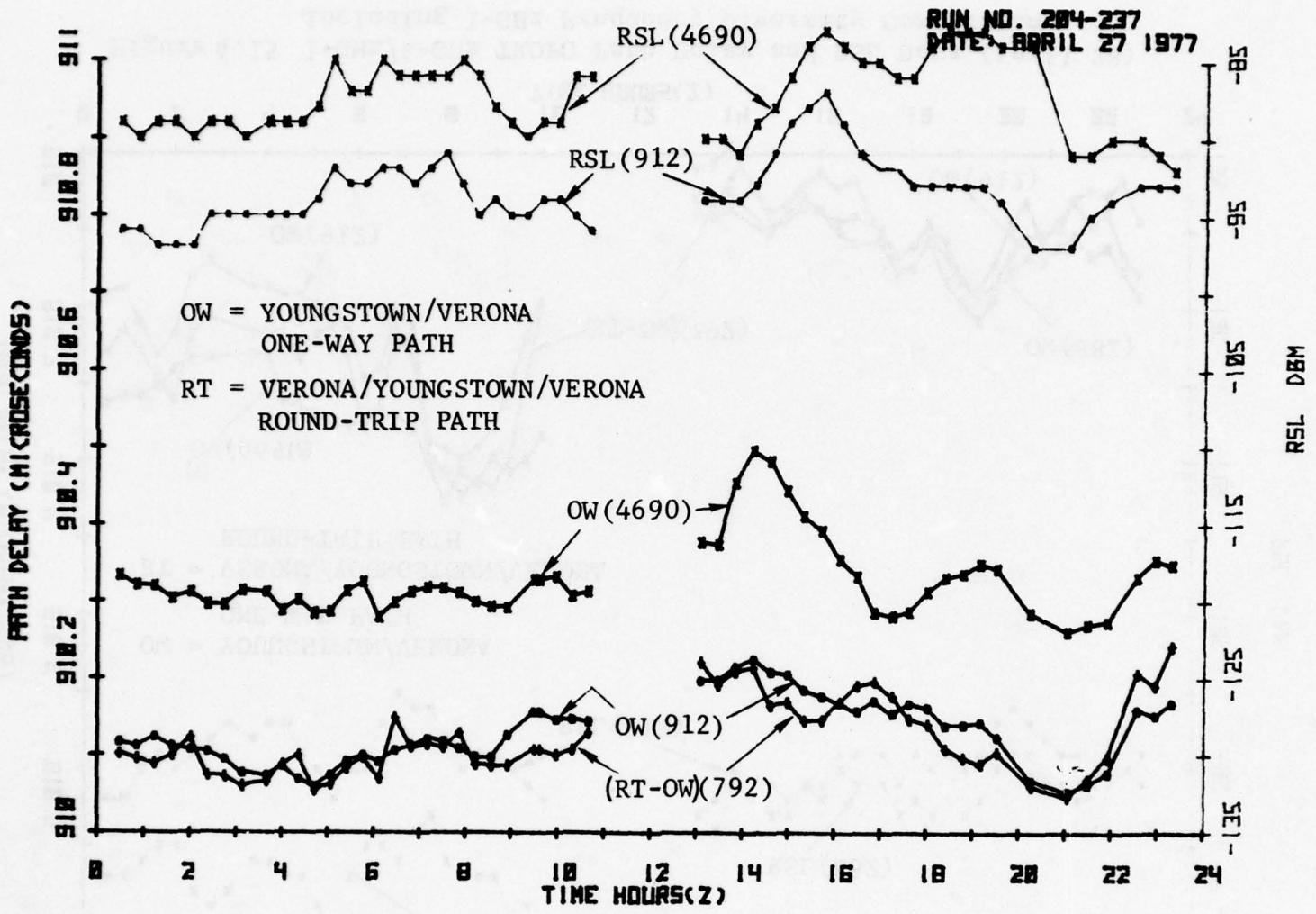


Figure 4.14 1-GHz/4-GHz TROPO Path Delay and RSL Data (April 27)

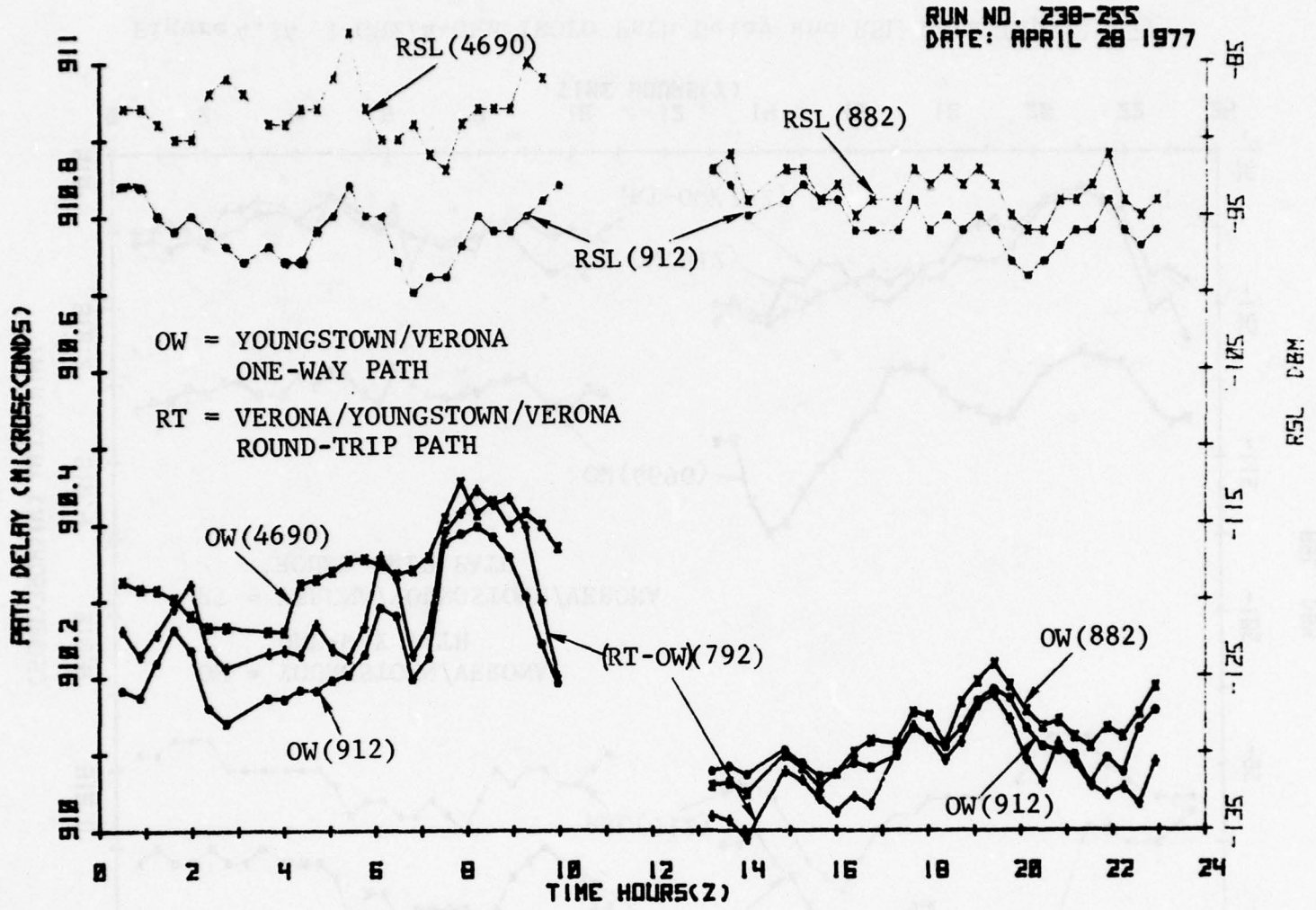


Figure 4.15 1-GHz/4-GHz TROPO Path Delay and RSL Data (April 28) including 1-GHz Frequency Diversity Comparison

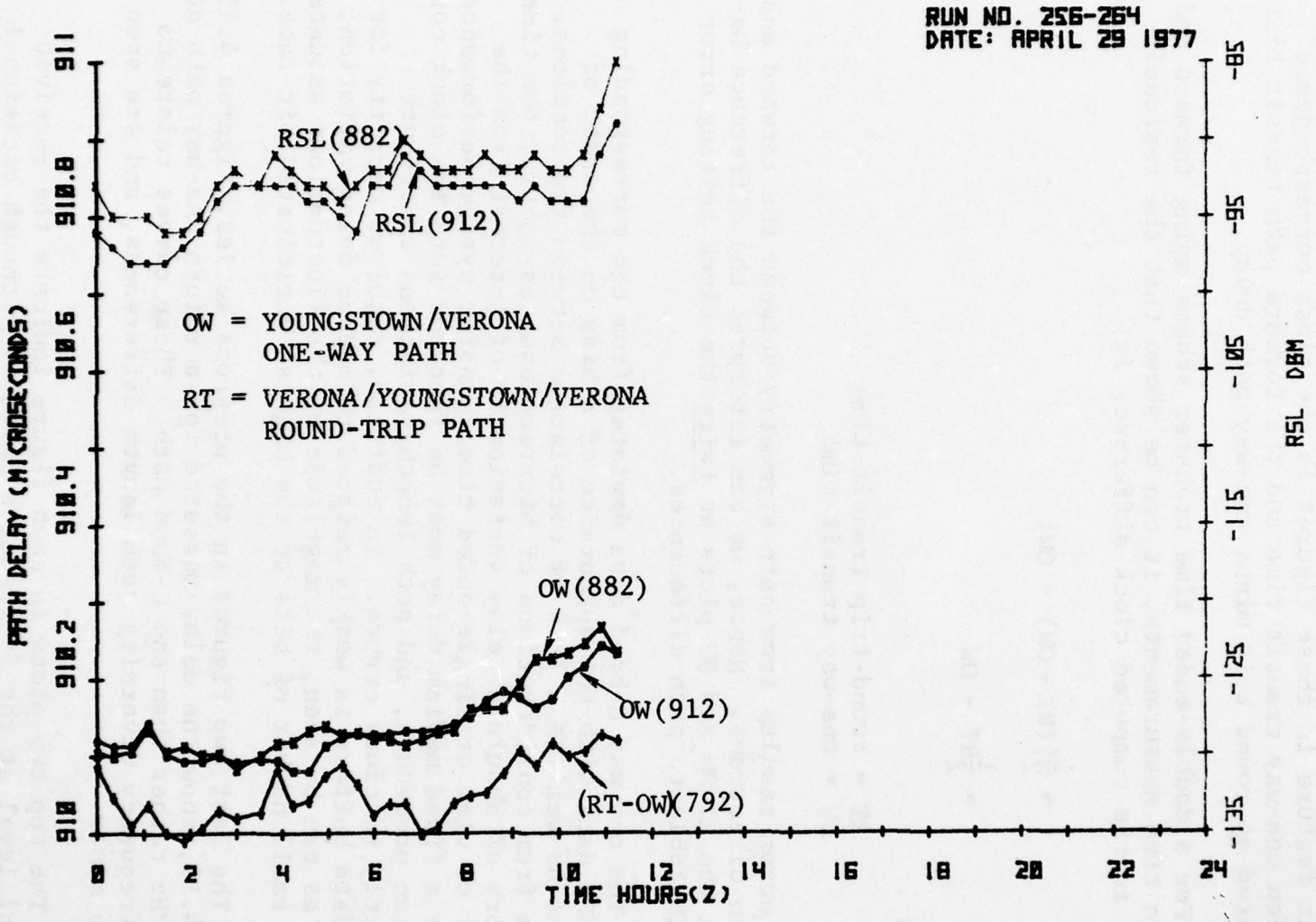


Figure 4.16 1-GHz TROPO Path Delay and RSL Data (April 29) with Frequency Diversity Comparison

with the notation (RT-OW). Also indicated is the delay variation for one-way transmission on the C-band link. The significant feature in these figures is the close correspondence between one-way transit time and the forward path transit time computed as round trip minus one-way path delay.

For a double-ended time transfer scheme using forward and return time measurements, it can be shown that the residual error in the computed clock difference is:

$$\epsilon = \frac{1}{2}[(RT - OW) - OW]$$

$$= \frac{1}{2}RT - OW$$

where

RT = round-trip transit time
OW = one-way transit time

This error results from path asymmetry between the forward and return directions. Hence, we can interpret the difference between the RT-OW and OW plots as <u>twice</u> the clock setting error attributable to path differences.

The one-way C-band data deviates from the corresponding 900-MHz data with the appearance of a bias on the order of 200 ns as well as a lack of correlation between fluctuations. Aside from considerations of bidirectional asymmetry, the time history of absolute delay variation is of interest from the point of view of single-ended time transfer system performance, where a fixed medium delay must be factored into the clock correction procedure, and path length variations contribute directly to clock errors. In addition, required capacity for the data buffers is weakly related to medium delay variation, but, as can be seen, the magnitude of the fluctuations amounts to a small number of bits at the highest anticipated bit rate.

The last two figures in the previous series, Figures 4.15 and 4.16, show the delay measured for a return one-way path at 882 MHz rather than the C-band path. These curves relate to the frequency diversity path length differences, and are seen to be minor.

The top two plots in each figure indicate the received signal level at the frequencies marked. Although occasional correlation with the delay plots may be observed, there is no consistent or strong coupling between the two sets of data.

Figures 4.17 through 4.20 provide a statistical summary of the delay during the complete measurement period. Figures 4.17 and 4.18 are histograms of the 20-minute one-way delay samples for 912 MHz and 4690 MHz, respectively. Then, in Figure 4.19, we have the histogram for (RT/2)-OW delay corresponding to the 792-MHz forward path and the 912-MHz return path. Recall that this quantity is the clock setting error that results when double-ended time transfer is attempted. For these two frequencies, a standard deviation of 27 ns was computed using the 165 20-minute samples. Finally, in Figure 4.20 we have a distribution for the one-way differences corresponding to path delays in the return direction at 882 MHz and 912 MHz. The standard deviation in this case is 22 ns, with a bias of 13 ns.

The next series of graphs, Figures 4.21 through 4.27, was extracted from the July data.

The first few days of data, as represented by Figures 4.21, 4.22, and 4.23, provide a comparison of the one-way path delay at the two frequencies, 912 MHz and 4690 MHz. The presence of a duct can be observed in Figure 4.23 where the RSL went higher than -70 dBm. At the same time, the path delay became smaller; that is, ducting propagation corresponds to a more direct path, with shorter transit time. Note that, at the beginning of the test period, the 4690-MHz link was running with an RSL greater than -70 dBm, but there was no corresponding shortening of the path. In Figure 4.22, good evidence may be found of correlation between RSL and path delay, however. Between 200Z and 1000Z, the RSL curves climb upward while the delay gets progressively smaller. Similarly, between 1200Z and 2000Z, there is a milder variation in the reverse sense; RSL decreases while delay increases. This period corresponds to mid-day and early afternoon. Then, at 2100Z, corresponding to late afternoon, the RSL is seen to increase rapidly, going all the way into the ducting condition shown in Figure 4.23. Meanwhile, the path delay decreases at an accelerated rate.

Overall, the path length at 4690 MHz and 912 MHz varied less than $\pm$ 200 ns for this sequence of test runs.

In the late July series, shown as Figures 4.24 through 4.27, we have a mixture of different operational conditions. Beginning with Figure 4.24, the one-way Youngstown/Verona tests involved 4690-MHz and 912-MHz transmissions, and with the continuation on Figure 4.25, we see that there was not such a striking correlation between RSL and delay, especially at C-band.

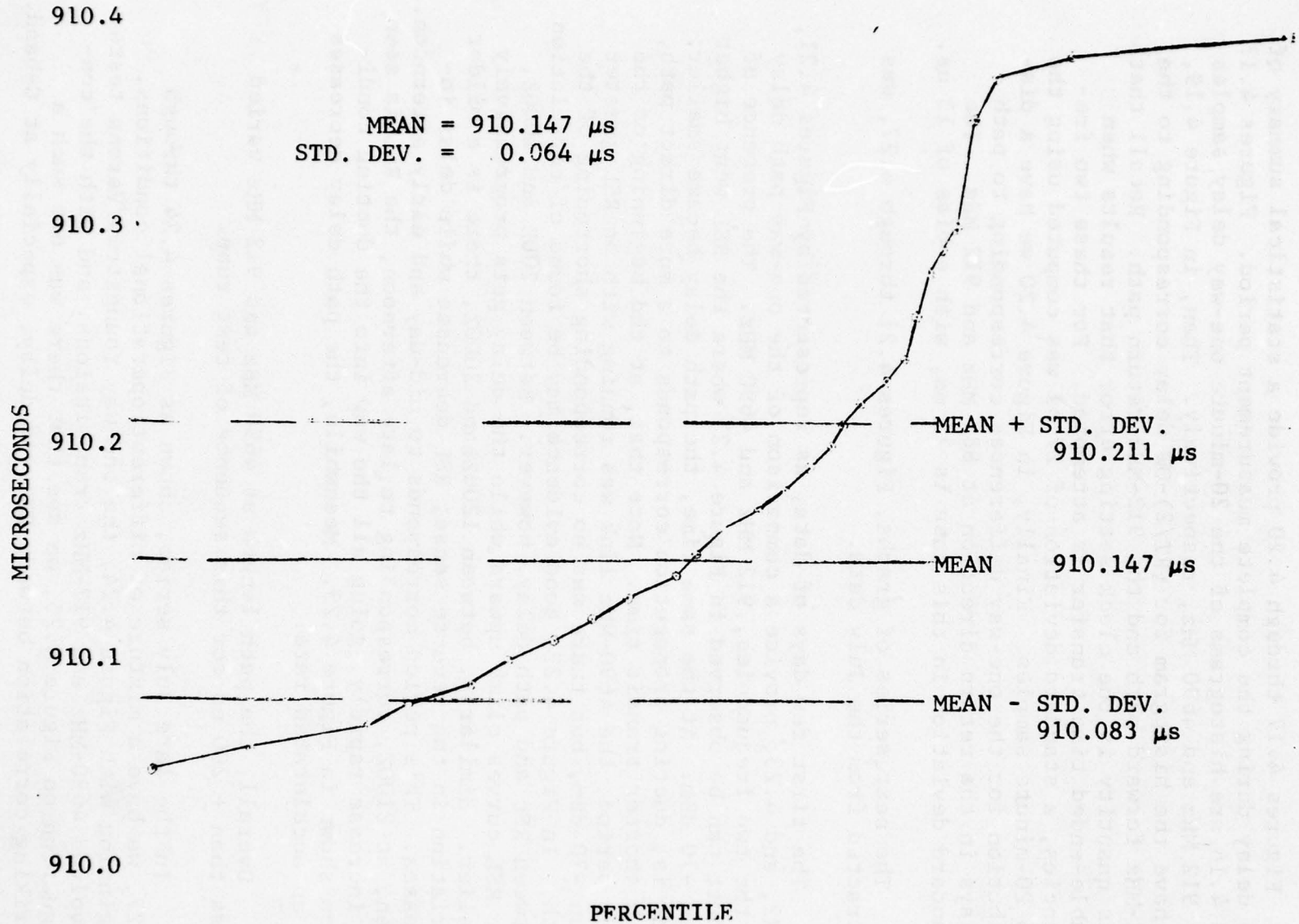


Figure 4.17 Distribution of One-Way Delay, 26 - 29 April 1977 (20-minute Averages, 912 MHz, 165 Samples)

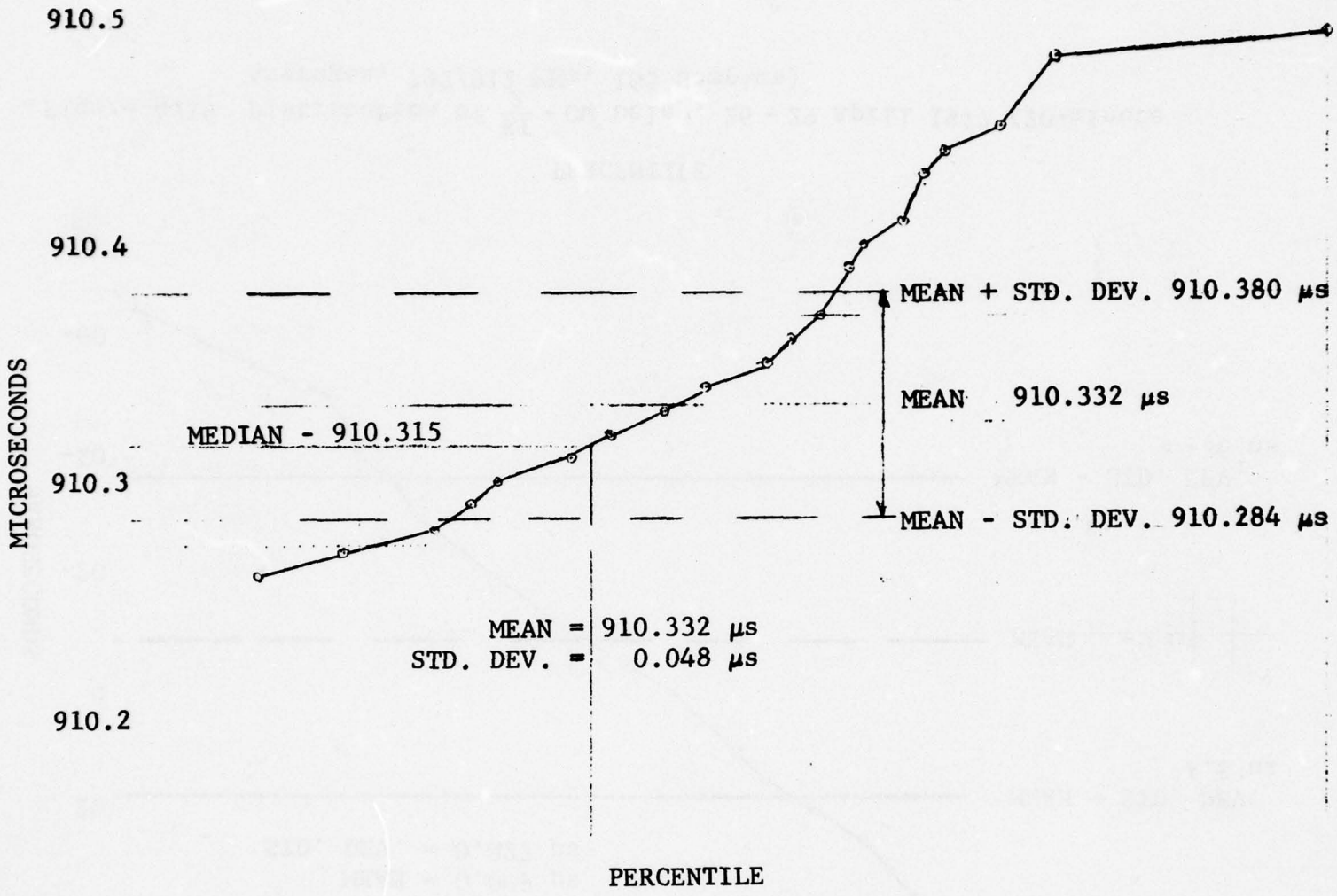


Figure 4.18 Cumulative Distribution of 20-Minute One-Way Delay Averages, 26 - 27 April 1977 (4690 MHz, 107 Samples)

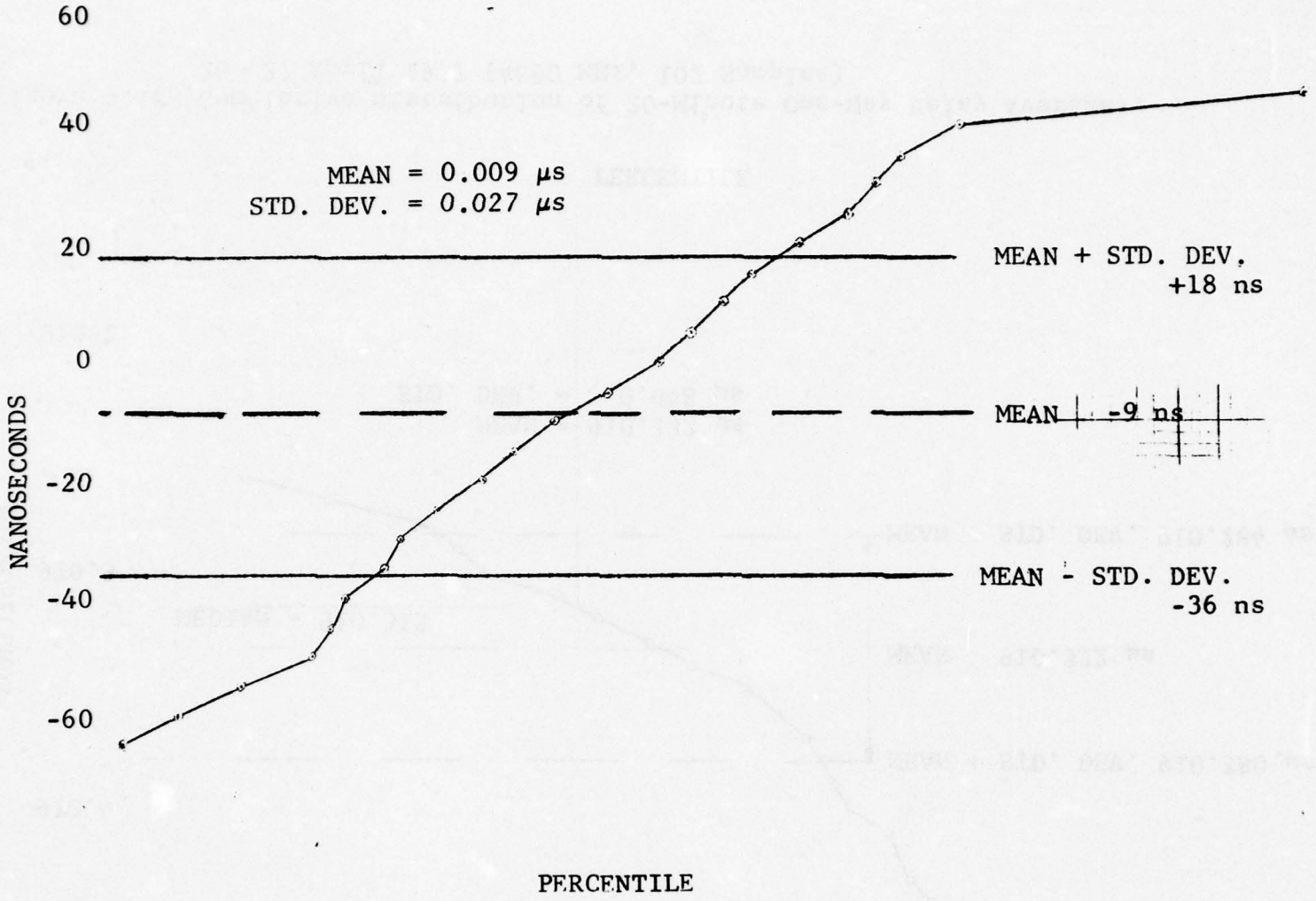


Figure 4.19 Distribution of $\frac{RT}{2}$ - OW Delay, 26 - 29 April 1977 (20-minute Averages, 792/912 MHz, 165 Samples)

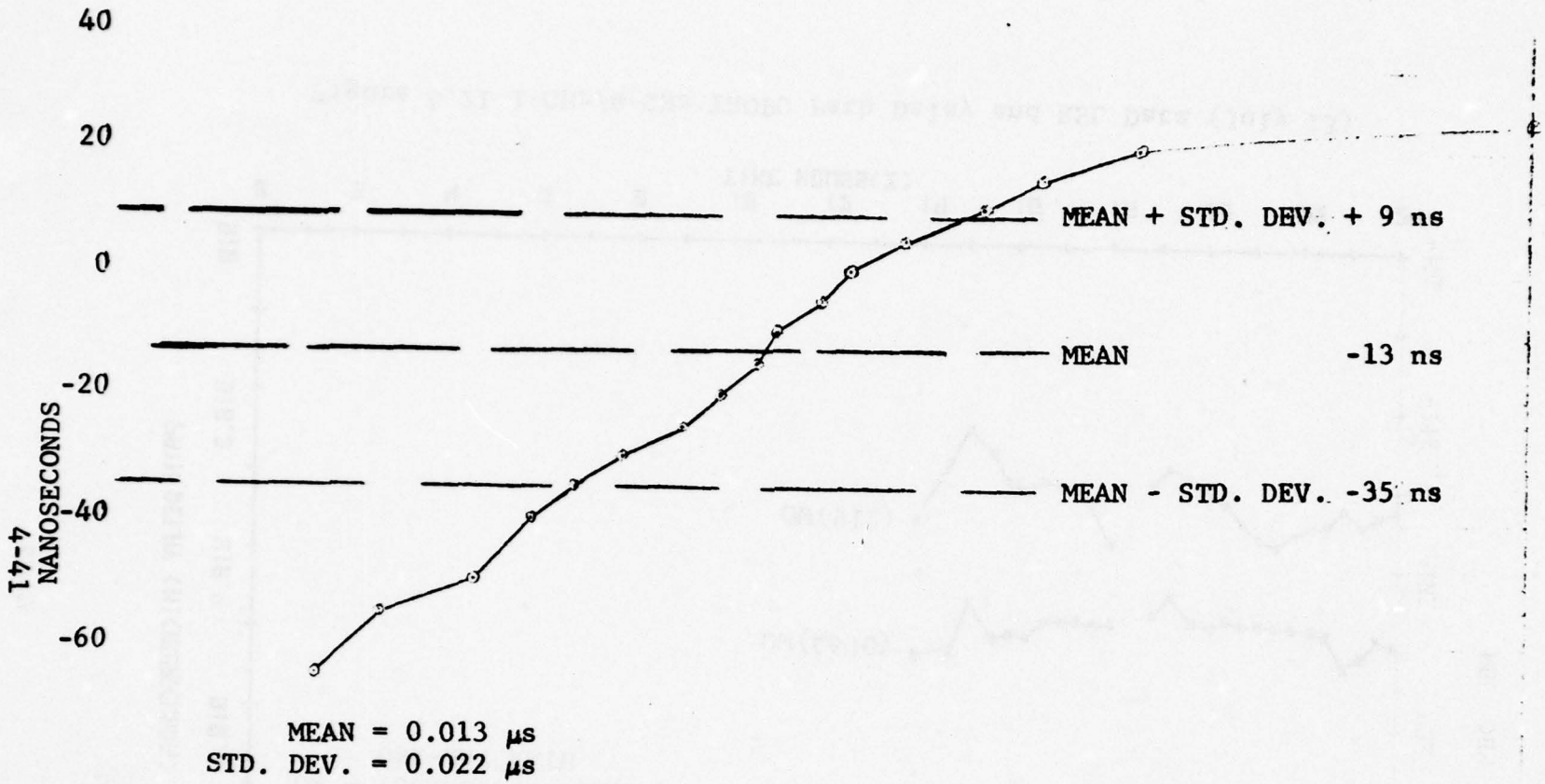


Figure 4.20 Distribution of (One-Way 912 - One-Way 882) Delay, 28 - 29 April 1977 (20-minute Average, Frequency Diversity 912/882, 58 Samples)

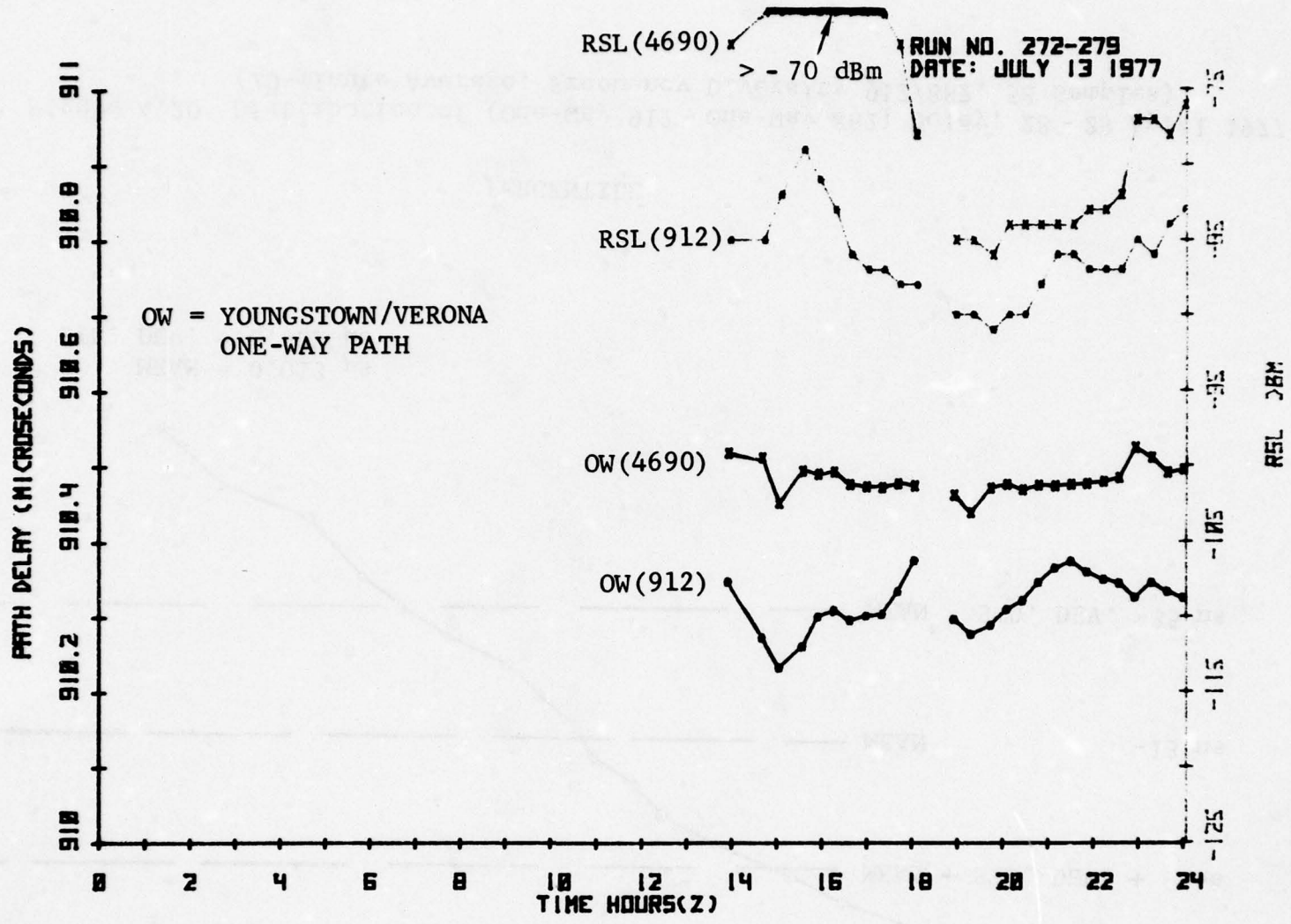


Figure 4.21 1-GHz/4-GHz TROPO Path Delay and RSL Data (July 13)

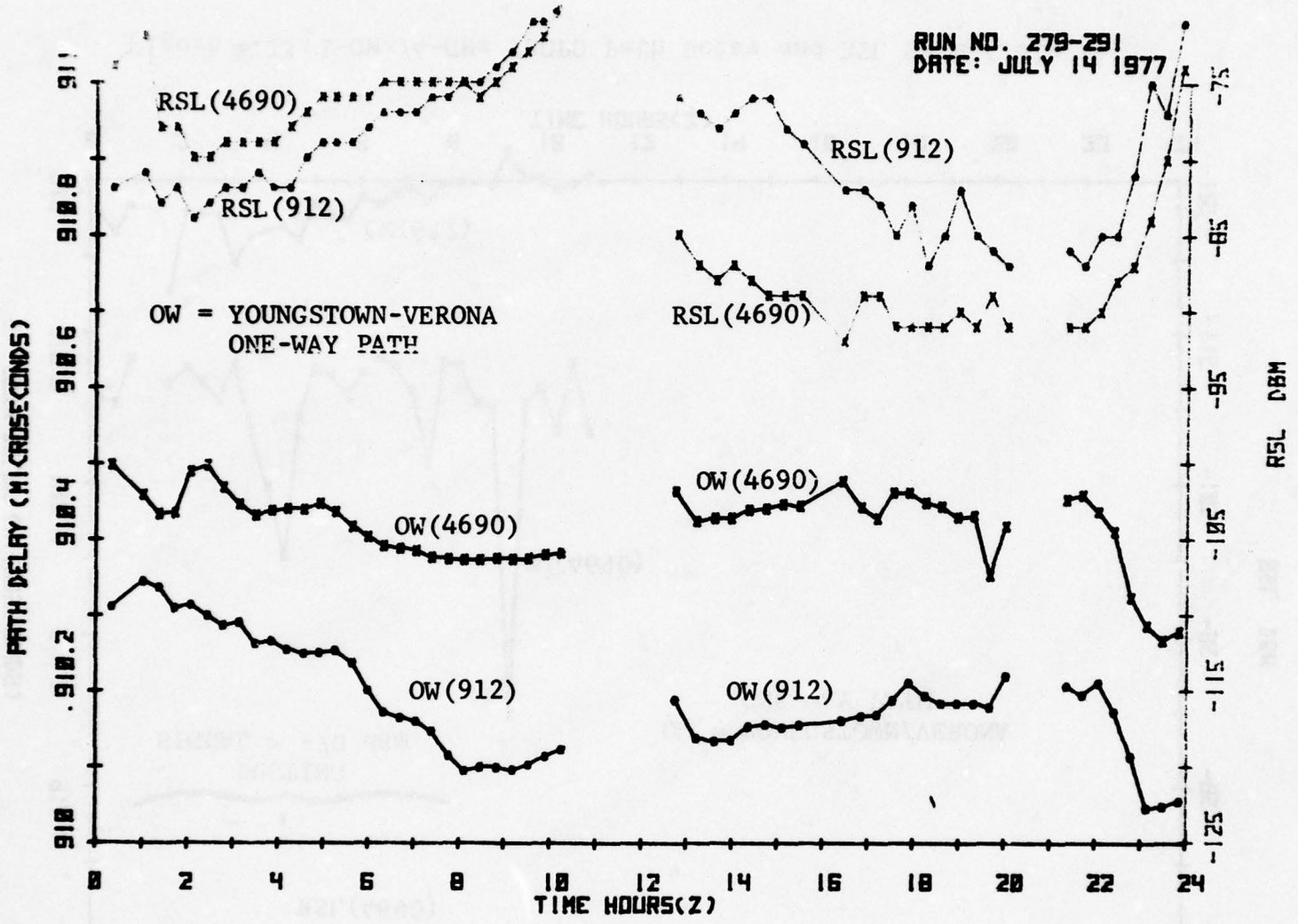


Figure 4.22 1-GHz/4-GHz TROPO Path Delay and RSL Data (July 14)

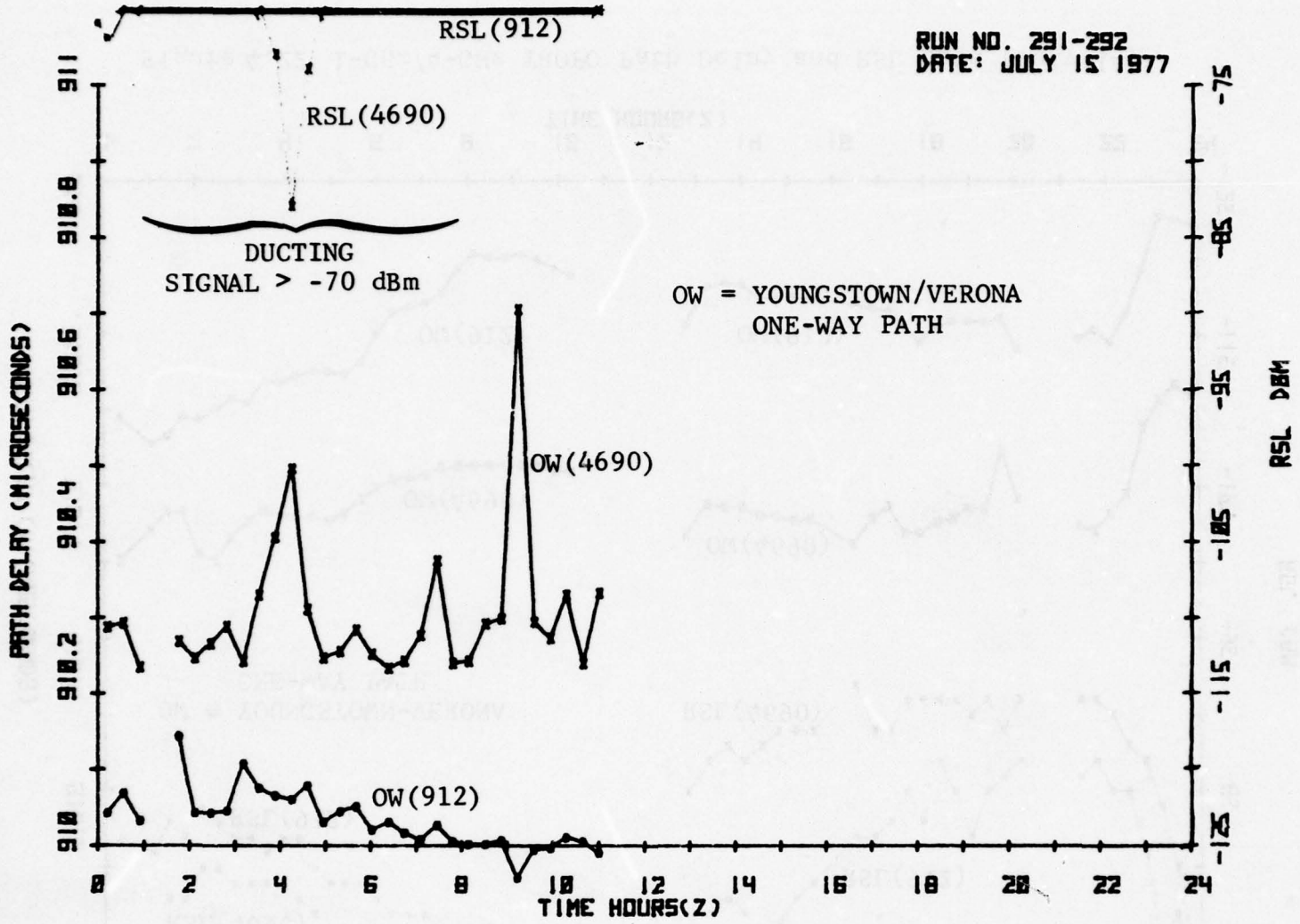


Figure 4.23 1-GHz/4-GHz TROPO Path Delay and RSL Data (July 15)

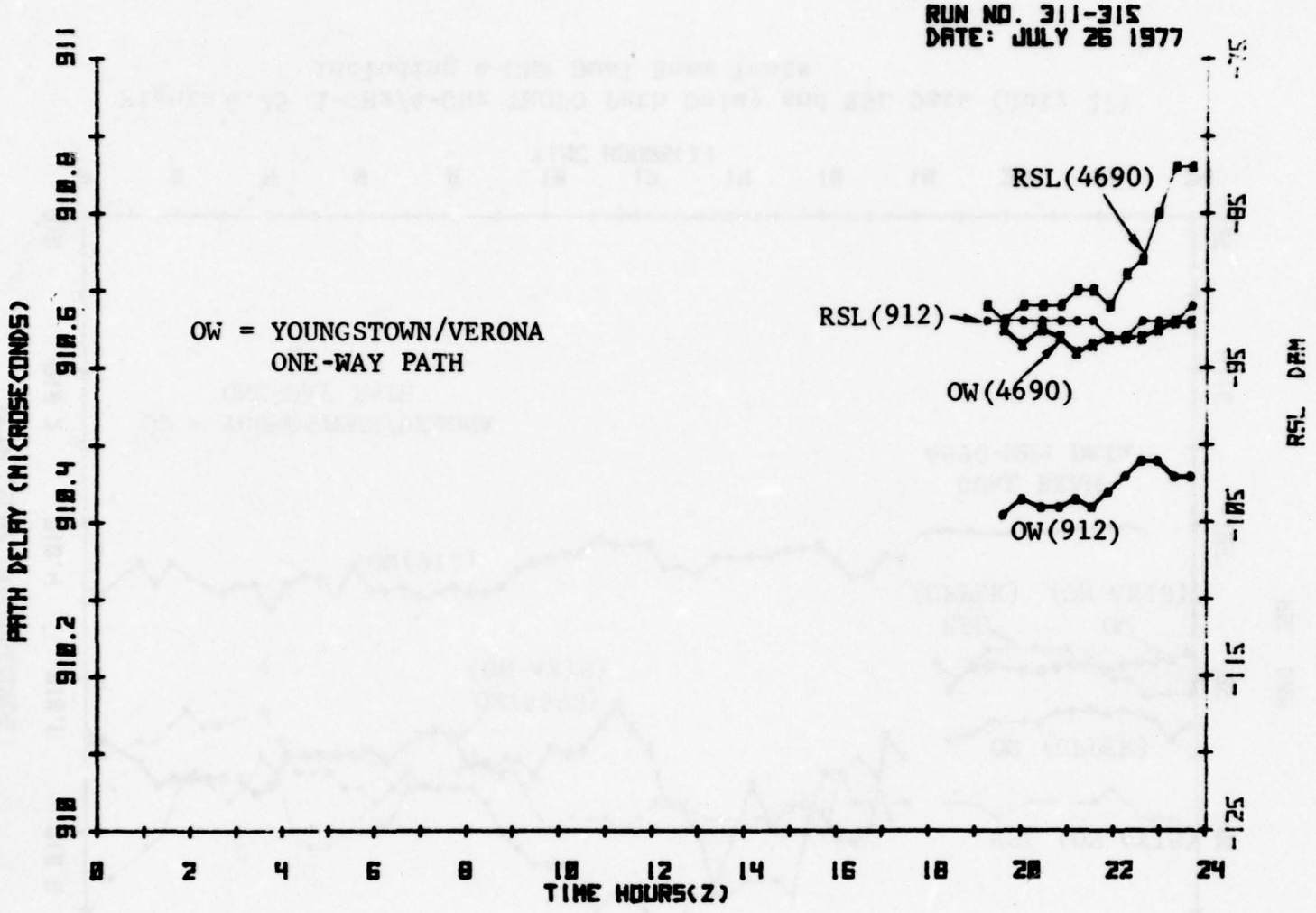


Figure 4.24 1-GHz/4-GHz TROPO Path Delay and RSL Data (July 26)

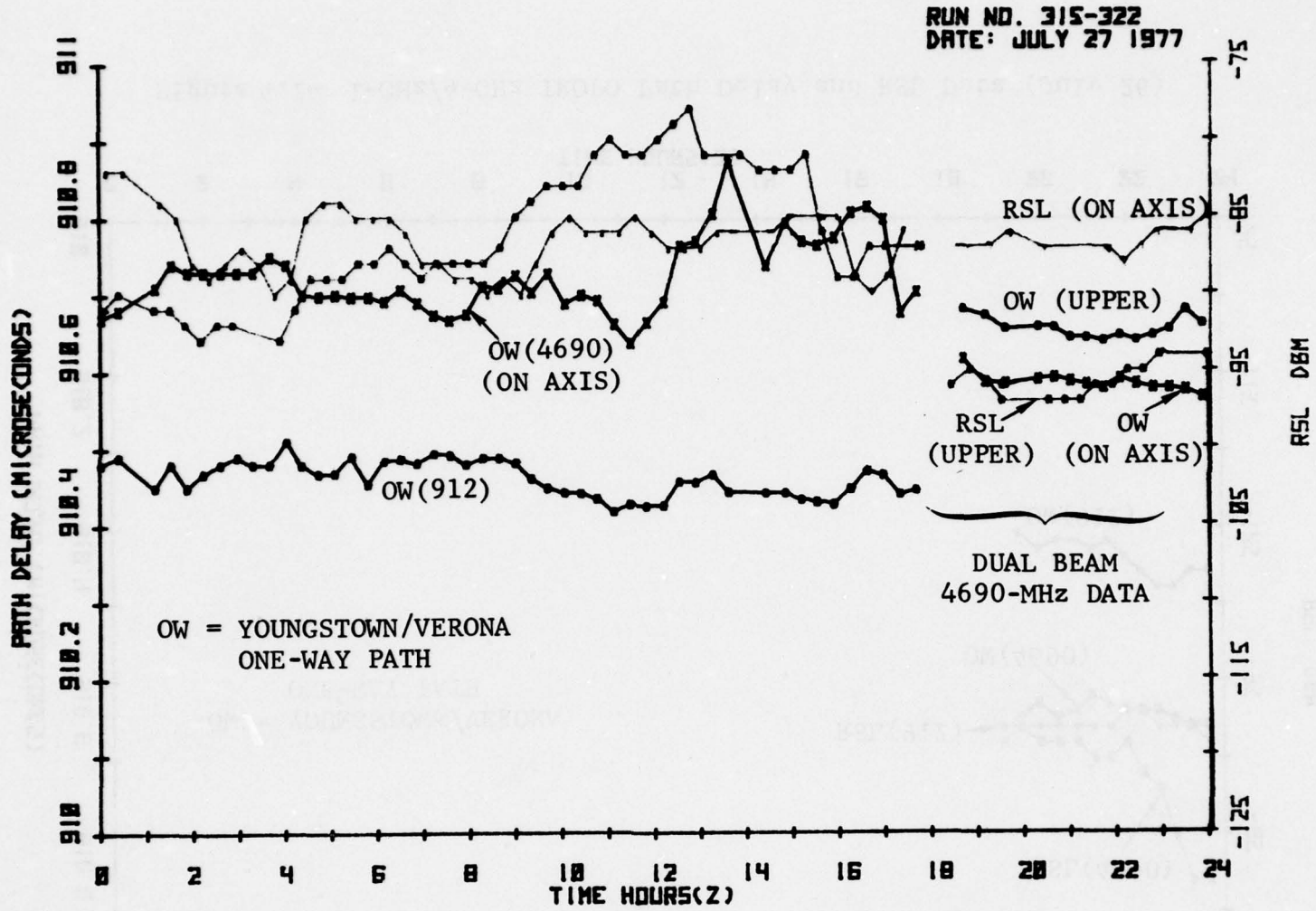


Figure 4.25 1-GHz/4-GHz TROPO Path Delay and RSL Data (July 27) including 4-GHz Dual Beam Tests

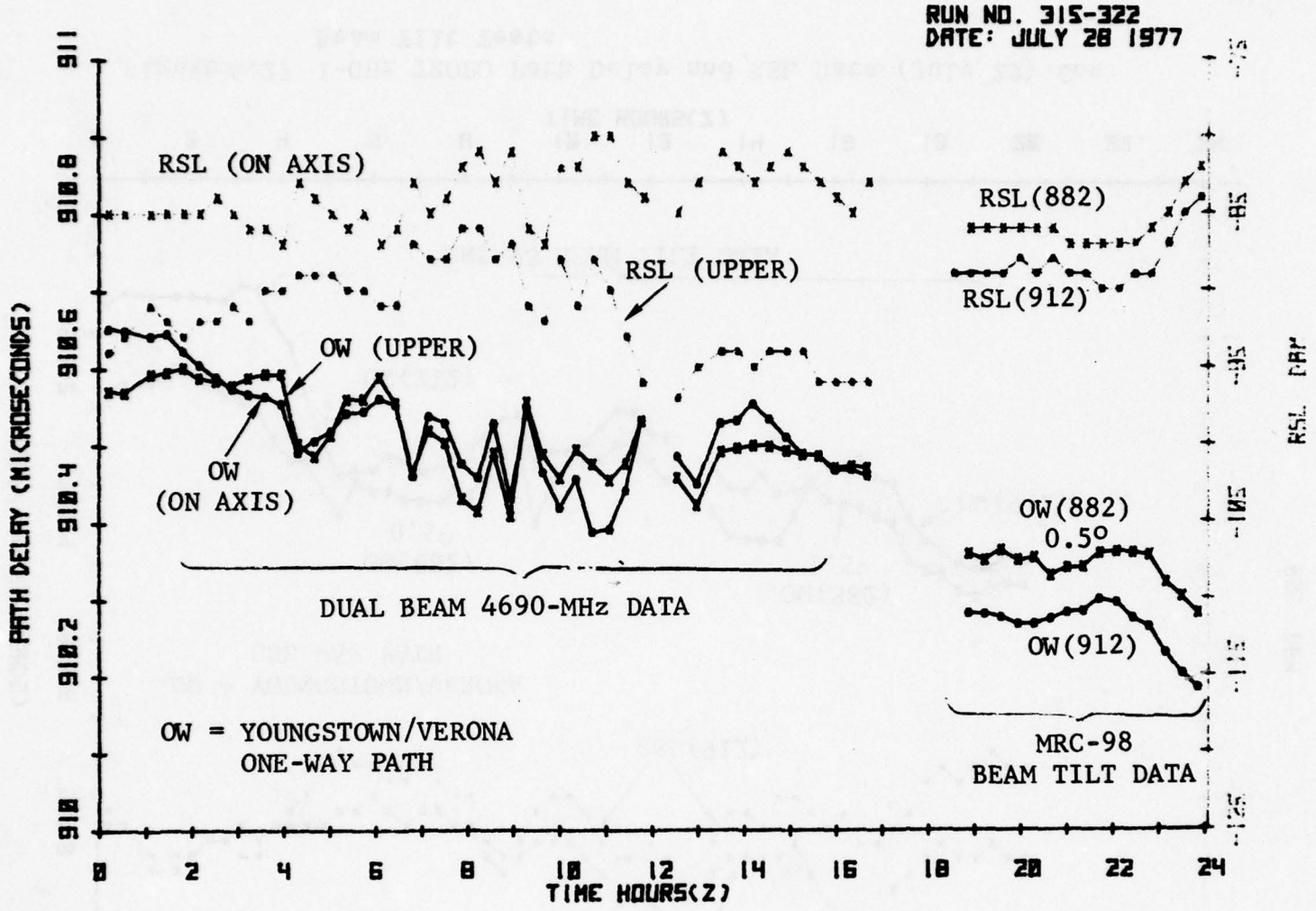


Figure 4.26 1-GHz/4-GHz TROPO Path Delay and RSL Data (July 28) including 4-GHz Dual Beam and 1-GHz Beam Tilt Tests

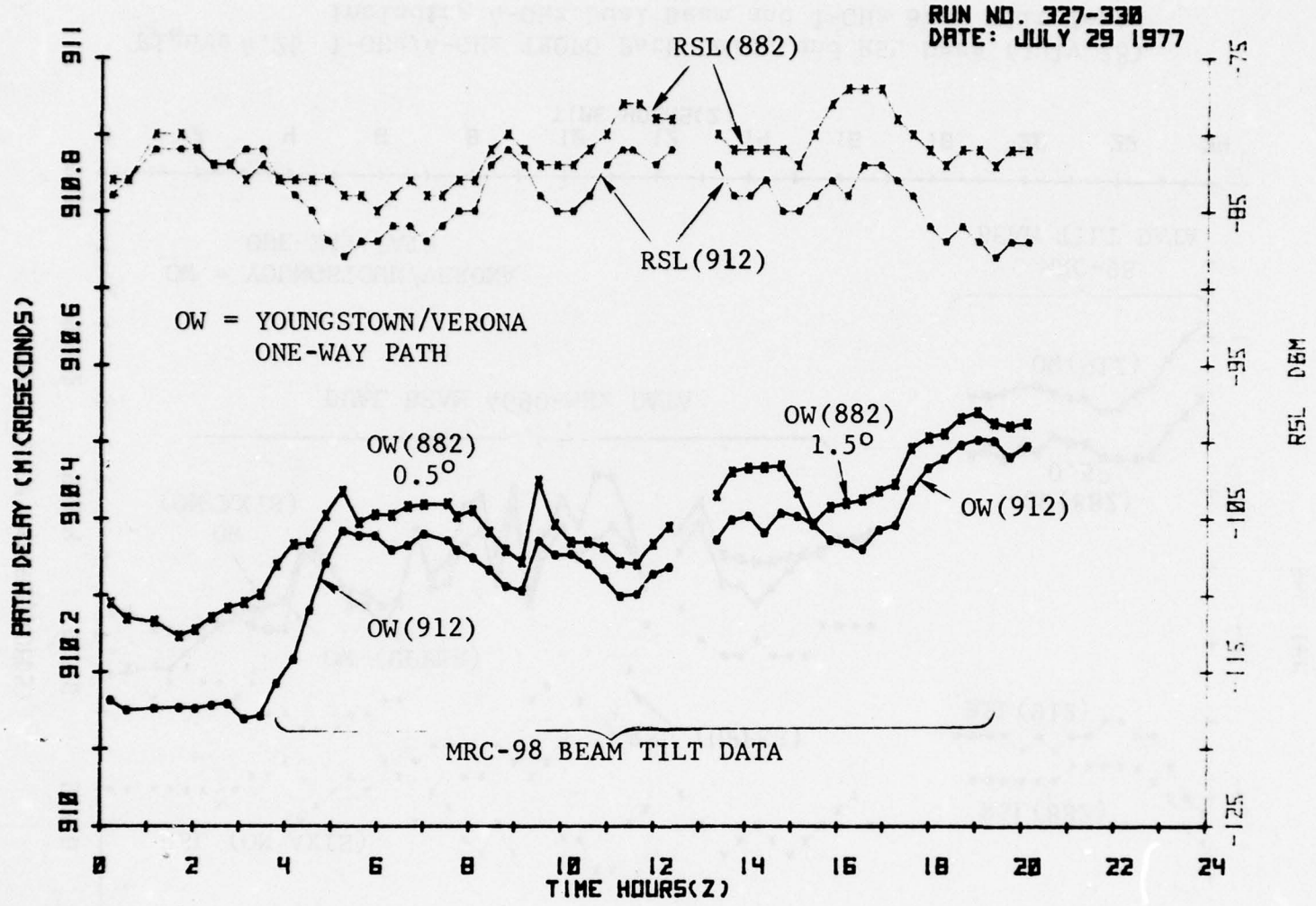


Figure 4.27 1-GHz TROPO Path Delay and RSL Data (July 29) for Beam Tilt Tests

From 0800Z to 1800Z, the 912-MHz data does show the anticipated trends, but the 4690-MHz data does not.

Beginning at 1800Z on the 27th of July, the dual beam 4690-MHz tests were run. The on-axis beam corresponds to the normal TRC-132 feed horn (at Verona) while the upper axis beam is a special feed horn installed in the Verona dish to allow angle diversity tests. The beam inclination from boresite is understood to be on the order of 1^{o} (the beams cross at the 4-dB level). We see from Figure 4.25 that there is a marked disparity between the two RSL's, approximately 10 dB, and at the start of the run, an 80-ns delay differential. In the later portions of the test (Figure 4.26), the on-axis RSL is considerably better and the delay for both beams decreases progressively throughout the day. Because the two path delays are so close, it can be inferred that the lower portions of the scattering region contribute most significantly to the received signal for both beams; i.e., the upper beam is receiving most of its signal at the edge of the beam pattern mainlobe, and the RSL is down by an amount corresponding to the beam power pattern at that angle.

For the test sequence starting at 1900Z on 28 July (Figure 4.26), the MRC-98's were used in elevated angle configurations. First, the 882-MHz dish at Youngstown was raised 0.5^{o} from the normal pointing angle, and data was acquired for this arrangement until 1200Z on 29 July. Note the strong correlation between delay and RSL for the last few hours of Figure 4.26, as well as the complete 20 hours shown on Figure 4.27. Again, as in the C-band tests just described, high RSL gives rise to a convergence effect for the two beam path delays; i.e., high RSL corresponds to low altitude scattering or reflection which dominates the received signal for both beams.

Interestingly enough, when the 882-MHz MRC-98 dish at Youngstown was raised to 1.5^{o} at 1300Z on 29 July, the transit time difference between the 882- and 912-MHz beams was <u>less</u> than what it had been earlier for an elevation of 0.5^{o}. The RSL did remain relatively high for the last hours of Figure 4.27, and the overall conclusion is the same as before. Raising the beam elevation has very little effect on delay when the basic RSL is high. Of course, the RSL for the raised beam decreases at a rate determined by the beam pattern.

The last two figures in this subsection, Figures 4.28 and 4.29, are repeated from data presented earlier, but include surface refractivity estimates. Although many other similar plots are available, the lack of any obvious correlation effects dictates the inclusion of only two plots in this report. A cursory examination of Figure 4.29 seems to indicate that refractivity increased when path delay decreased, but several other similar examples do not confirm this trend in general. Figure 4.28, for example, shows the same kind of rise in refractivity during the night, but very little change in delay.

4.4.3 Propagation Mechanisms Inducing Delay Fluctuations

We refer here to the long-term variations which are a function of the power profile $Q(\tau)$, rather than the short-term interference effects.

For troposcatter paths, we can attribute path length variation to three principal theoretical mechanisms. They are:

- Changes in the bulk troposphere refractivity and, hence, the speed of propagation.
- Beam motion or misalignment resulting, for example, from refractive index gradient variations.
- Distortion of the delay power profile $Q(\tau)$ which occurs as a result of variable medium characteristics and distributions, e.g., ducting, turbulence, or tropospheric stratification.

Consider the first of these, bulk refractivity changes. The path length is on the order of 1000 μs. Therefore, with each N unit of refractivity, there is an additional delay of

$$\Delta\tau = (1 \times 10^{-6}) \times 10^{-3} \text{ seconds}$$

$$= 1 \text{ nanosecond}$$

Day-to-day changes in refractivity on the order of $\pm$ 10 N units are readily observed, while seasonal cycles may amount to considerably more. But we are concerned primarily with the hourly path delay changes here, and can see from earlier figures that they amount to hundreds of nanoseconds;

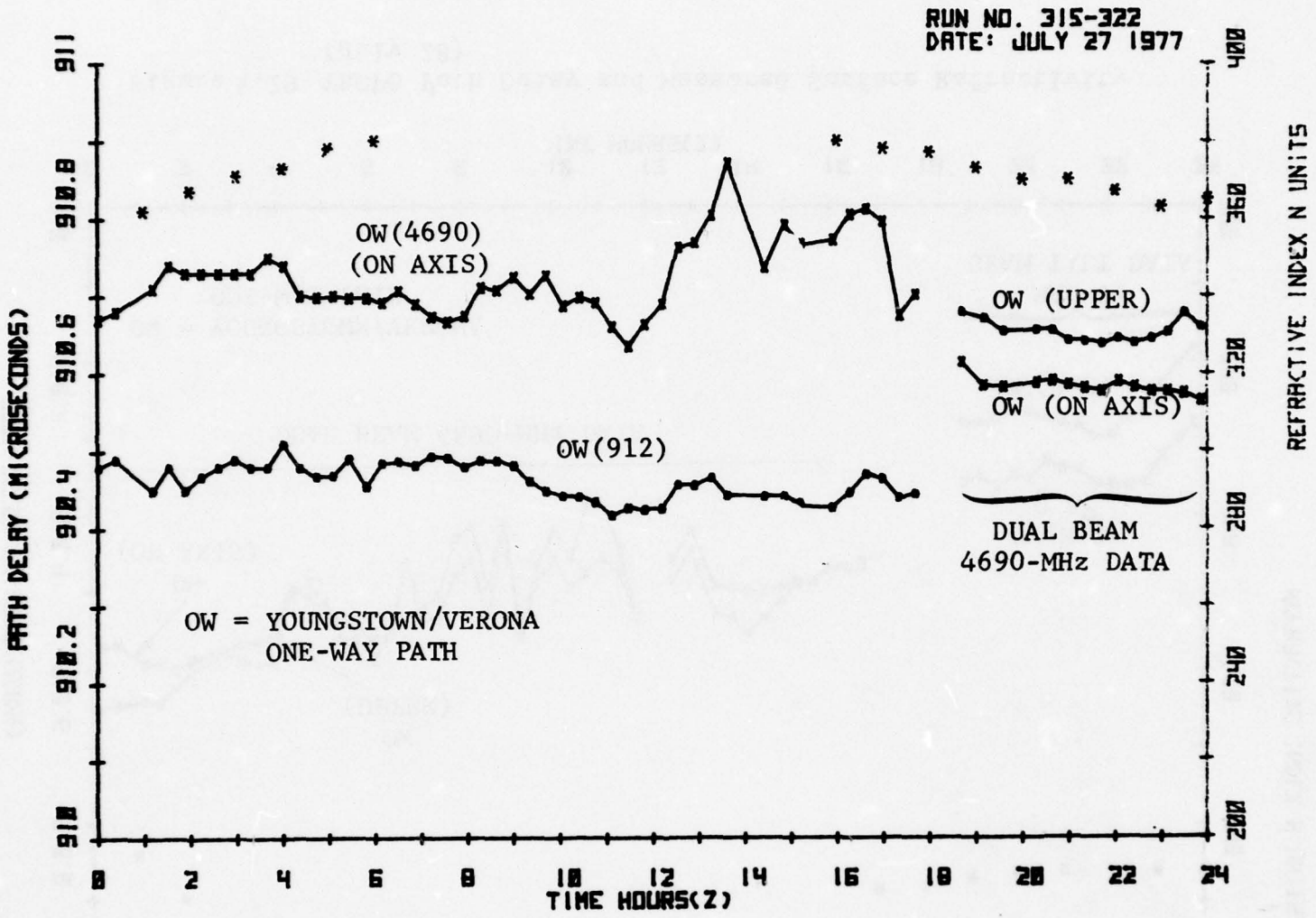


Figure 4.28 TROPO Path Delay and Measured Surface Refractivity (July 27)

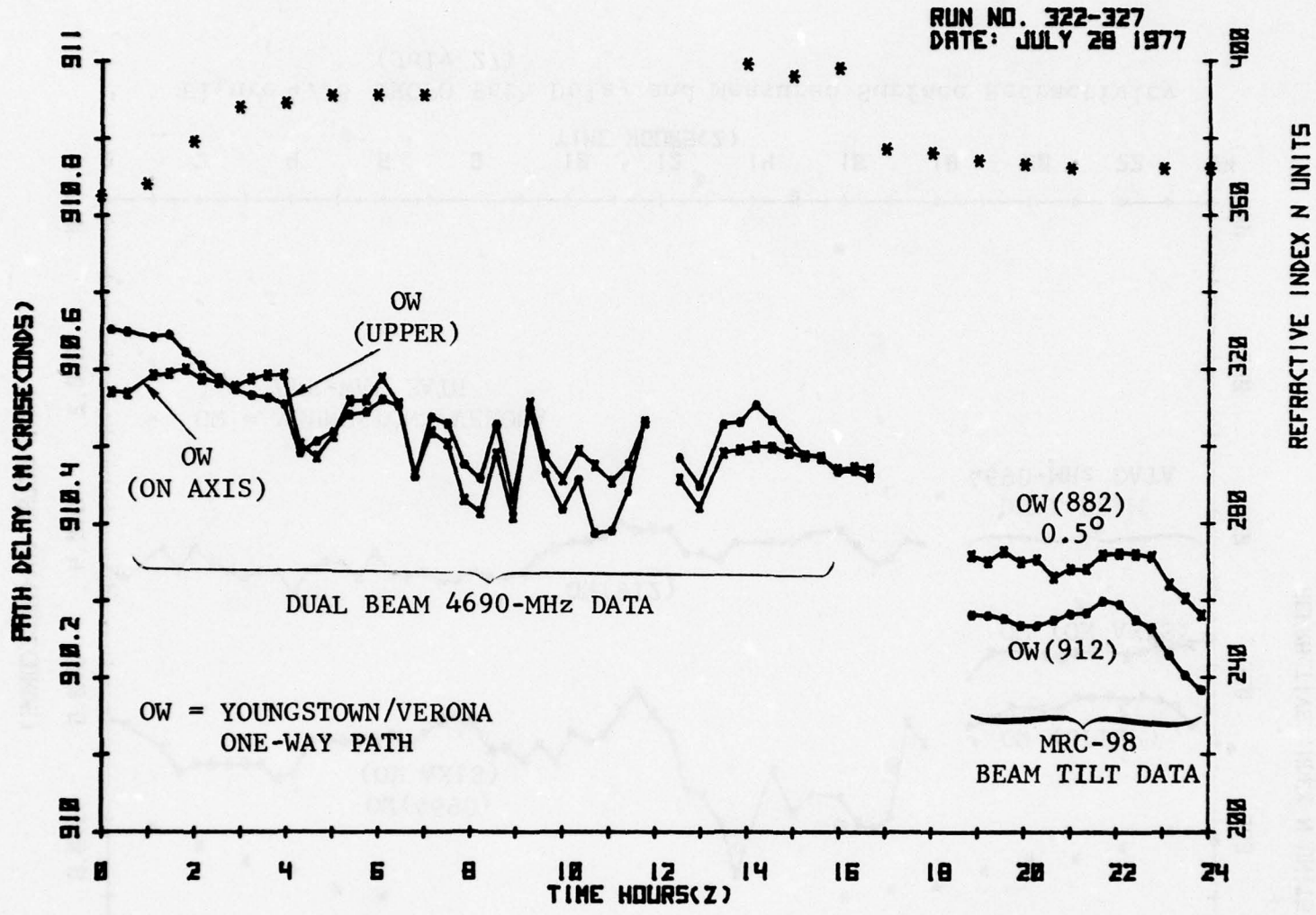


Figure 4.29 TROPO Path Delay and Measured Surface Refractivity (July 28)

we are forced to conclude that bulk changes in refractivity account for only a portion of the observed path length fluctuations.

Beam movement as a result of refractivity gradient variability is more promising. To gain some insight into this effect, we have run a troposcatter computer model through a range of parameter values corresponding to the MRC-98 and TRC-132 configurations.

The nominal operating point for these links was assumed to be with a 4/3 equivalent earth radius, which is a refractivity gradient of -40 N units/km. The relationship in question is:

$$\frac{1}{R_e} = (g_e + 156)\, 10^{-6}$$

where g_e is the gradient in N units per km, and R_e is the equivalent earth radius. With $g_e < -156$, we have ducting.

In Table 4-9 we show the computer model delay estimates. The program computes the link delay power spectrum and then evaluates the mean of this function; we have in this case used the mean as the path length attribute. The minimum delay is the delay of the leading edge of the response characteristic relative to the chord joining receiver and transmitter sites. Then, relative to this leading edge we have an average delay representing the mean of the delay power spectrum. Total path delay variation is found using the sum of the two. In the net change column, we have shown the change in mean of the power spectrum relative to the nominal 4/3 earth value of path delay.

For the range of gradients used, we see a path length range of +108 to -92 ns relative to the nominal 4/3 earth model for the MRC-98 link. The values for the TRC-132 link are considerably smaller as a result of the narrower beamwidth. This can be seen by comparing the "average delay" columns. Furthermore, the amount of change vs. refractivity gradient is roughly proportional to beamwidth, so the variability is not as great for the C-band link. Note carefully the final column for the TRC-132 which expresses the change relative to the MRC-98 nominal 4/3 earth delay. There is 130-ns difference at the 4/3 earth point; yet, in the field tests, the C-band path length was found to be consistently larger than the 1-GHz path by about 200 ns. It is felt that this is a consequence of antenna alignment differences.

TABLE 4-9

THEORETICAL DELAY VARIATIONS RESULTING FROM REFRACTIVE INDEX GRADIENT CHANGES

(IN NANOSECONDS)

Gradient N units/km	MRC-98			TRC-132		
	Minimum	Average	Net	Minimum	Average	Net
- 9	157	239	108			
-12	150	234	96	150	70	- 68
-20	135	221	68	135	67	- 86
-29	116	205	33			
-40	99	189	0	99	59	-130
-51	78	168	- 42	78	55	-155
-68	55	140	- 93			

The next question to be addressed concerns the frequency of occurrence of these refractivity gradients. In [4.3], several months of refractivity gradient data are presented as a probability distribution. This analysis was carried out on radiosonde data from the Buffalo area. Referring to the curves for winter, we find that gradients are steeper than -44 N units/km ($a/R_0 = 1.4$) about 10% of the time, while gradients are shallower than -20 N units/km ($a/R_0 \simeq 1.2$) approximately 10% of the time. Gradients more negative than -51 N units/km are only present 2% of the time. We would therefore expect most of the gradient variation in the -50 to -20 N units/km range with a corresponding path delay time variation of -42 to 68 ns. Reference [4.3] also indicates that the spread is likely to be greater in the summer months compared with the winter, and biased slightly toward a longer path length.

The effects of troposcatter stratification and other phenomena that cause a deviation in scatter distributions are perhaps the most important and yet the most difficult to characterize. The intensity of scatterers in the troposphere is normally represented in computer models by rather idealistic smooth functions of altitude; but, of course, there are wide variations in practice with corresponding influence on the delay power profile and, hence, the signal time of arrival. The only definitive statement that can be made is that ducting situations will give rise to near minimum path delay and high signal strengths. This mode of propagation was observed a few times during the tests. The reader is referred to Appendix E for a sample of the delay power spectra measured at the Verona site during the tests.

Finally, we present some of the results obtained by exercising the computer model through a beam swinging sequence. In this study, the effective earth radius was held constant while one of the beams was moved vertically by 1^o and then 2^o. The narrower beamwidth of the C-band antennas plays a different role here. The important consideration to keep in mind is that the dominant scattering contributions correspond to the lower spatial tropospheric regions, as defined by the antenna beam and shadowing effects. For the MRC-98 with 3^o beamwidths, this bright spot is only mildly affected when the beam is moved up 1^o. However, for the TRC-132, the beamwidth is less than a degree, so the volume of contributing scatterers is at a higher altitude. Although portions of July beam tilt data agree very well with the theoretical predictions of Table 4-10, we can see also that, at other times, the elevated and normal beams gave path delays much closer than predicted by the model.

TABLE 4-10

THEORETICAL MISALIGNMENT DELAY SENSITIVITY ANALYSIS

Angular Elevation* (deg)	Gradient N units/km	MRC-98		TRC-132	
		Average Delay	Net Change	Average Delay	Net Change
0	-40	189	0	59	0
1	-40	221	32	145	86
2	-40	279	90	296	237

*The beam moved vertically.

We conclude this section by tabulating the path delay components that were derived from a knowledge of the geographical coordinates combined with a theoretical scattering model. Because of conflicting coordinate data originally available, the RADC sites were resurveyed in July 1977 to establish geometric path lengths. As a guide, the following delay budget indicates the relative importance of different components in a transit time calculation:

Estimated Great Circle Path Verona-Youngstown (912-MHz path)	272695 ± 3 meters
Uncorrected Transit Time (using speed of light in a vacuum)	909.610 μs
Correction for Refractivity with n = 320 N units	0.291 μs
Correction for Path Length corresponding to Delay Power Spectrum Centroid (1 GHz)	0.219 μs
Total Path Delay	910.120 μs

This value agrees very well with the experimental data for the 1-GHz path. In the April data, for which the distribution of Figure 4.17 applies, the average path delay was found to be 910.147 μs.

4.5 Line-of-Sight Equipment Delay

4.5.1 LOS Radio Delay

Delay measurements were carried out on the LOS radios at the Verona and Stockbridge sites. Additional measurements were begun on the Ava equipment but, as a result of failure in the converter, this activity was abandoned.

The measurement configuration for these radios was basically the same as for the TROPO FM radios; the block diagrams of Figures 3.6 and 3.7 are equivalent to the setup utilized.

However, only two different loops were possible: one at the RF output level, the other at the 70-MHz modulator/demodulator interfaces. Baseband tones ranging from 50 kHz to 1500 kHz were applied to the modulator. The results of the tests are presented in Tables 4-11 and 4-12 for both A and B units at the Verona and Stockbridge sites.

4.5.2 LOS Modem Delay

Back-to-back delay tests were carried out for the Philco-Ford Quaternary Baseband modems and interfaces. There are clock phasing controls on the front panel of the equipment, implying that the measured data must be used with caution. It is known that tens of nanoseconds timing variation can be effected with these controls within the range of satisfactory modem performance and, overall, a whole bit of variation is possible.

The measurements for the Verona equipment are shown in Table 4-13. The PN generator/synchronizer delay component was measured separately and subtracted from back-to-back tests with loops at the NRZ interfaces as well as at the modem output. The resulting delay values are shown in Table 4-13.

No delay uncertainty was anticipated for this equipment because it does not include an internal multiplexer.

4.6 Line-of-Sight Path Delay

Several long data acquisition runs were made on the LOS portion of the network shown in Figure 3.14. The most comprehensive of these runs were in the October series when a quartz clock was set up to track a master cesium clock at the other end of a 75-mile loop. The clock controller at the slave end was run with a relatively short time constant on the order of 100 seconds. With single-ended master/slave synchronization of this form, the slave clock attempts to follow long-term variations of the incoming time reference; i.e., relative time synchronization. As the medium "breathes" during the day, the controller adjusts the local clock to follow the reference variations. In other words, path length variation on a time scale exceeding 100 seconds is directly reflected in the relative phase for the transmit and receive clocks, while shorter term fluctuations are averaged out in the servo loop. Earlier LOS delay tests carried out in July resulted in several days of raw arrival time data recorded manually at 15-minute intervals. The graphical nature of the October data allows for easier

TABLE 4-11

VERONA LOS LC-8D RADIO DELAY MEASURED AT BASEBAND INTERFACE

Baseband Frequency (kHz)	RF Back-to-Back Delay (ns)	70-MHz Back-to-Back Delay (ns)
A Side: TX - 8.075 GHz; RX - 8.390 GHz		
50	463	255
100	455	244
200	449	237
300	446	234
400	448	236
500	447	234
1000	445	232
1500	445	231
B Side: TX - 8.075 GHz; RX - 8.390 GHz		
50	518	299
100	506	282
200	495	272
300	490	267
400	490	266
500	487	263
1000	483	258
1500	481	256

TABLE 4-12

STOCKBRIDGE LOS LC-8D RADIO DELAY MEASURED AT BASEBAND INTERFACE

Baseband Frequency (kHz)	RF Back-to-Back Delay (ns)	70-MHz Back-to-Back Delay (ns)
A Side: TX - 7.965 GHz; RX - 8.290 GHz		
50	342.5	186.3
100	392.8	232.4
200	414.8	251.5
300	421.0	255.6
400	428.3	262.4
500	430.1	265.1
1000	434.3	271.6
1500	437.4	273.6
B Side: TX - 8.390 GHz; RX - 8.075 GHz		
50	352.2	188.5
100	395.2	230.7
200	413.8	247.0
300	418.3	251.4
400	422.8	256.5
500	425.6	258.8
1000	429.9	261.7
1500	431.0	264.9

TABLE 4-13

DELAY MEASUREMENTS FOR PHILCO-FORD BASEBAND MODEM

Rate 5.0 Mb/s
Scrambler out.
Test mode off.

PN generator/synchronizer Back-to-back	8.4330 μs
T^2L to NRZ and NRZ to T^2L Interfaces (one each)	0.0805 μs
Philco-Ford Modem Back-to-back	2.409 μs

interpretation so we begin there and complete this section with a comparison of the two data sets.

Figure 4.30 shows a portion of a 4-day run in which a quartz clock was tracking a cesium reference through the 75-mile LOS loop. The plotted variable is the slave clock relative to the master clock expressed in nanoseconds. Once again there is an offset of 1 μs which was programmed into the controller to avoid measurements near zero time difference. The controller was also given a nominal path delay parameter which it used to advance the slaved clock; i.e., using single-ended master/slave operational principles. Thus, the plotted output is directly related to path length, although it is evident that the choice of nominal path length was too large, resulting in a bias of the plot down from the 1-μs objective. Ideally, the graphed time difference function would have fluctuated around 1 μs indicating a correct choice of nominal path length.

It should be apparent from Figure 4.30 that LOS links have relatively mild delay characteristics compared with TROPO paths. Transit time fluctuations appear to be confined to a ± 10-ns region. We note also that there is strong evidence of diurnal delay variations. For example, the valleys in Figure 4.30, corresponding to shortened path length, occur in the early afternoon (the plot is in local time to help the reader identify diurnal effects). During the night, the path length is greatest.

The medium portion of the radio path corresponds roughly to a propagation time of 375 μs. Hence, with refractivity variations on the order of ± 10 N units daily, the anticipated path length variation is:

$$\Delta\tau = \pm (10 \times 10^{-6})(375 \times 10^{3}) \text{ ns}$$

$$= \pm 3.75 \text{ ns}$$

The normal diurnal fluctuations shown in Figure 4.30 amount to roughly ± 6 ns, so it is likely that the bulk refractivity variations are the principal mechanism at work in this case.

During the 4-day run being discussed, the weather was typically mild with temperatures in the 10^{o} - 15^{o}C range. Notes in the operator's log indicate the presence of early morning

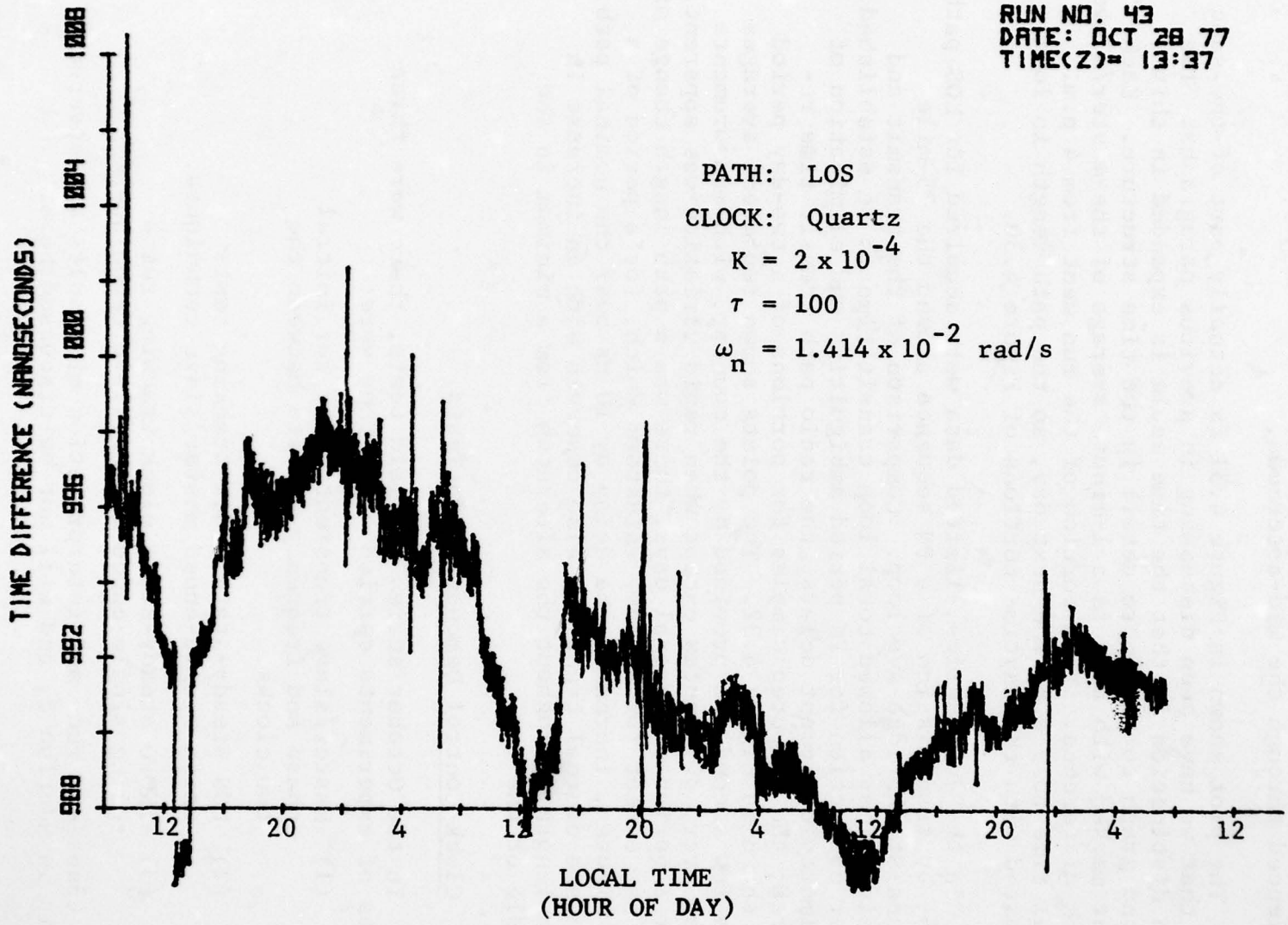


Figure 4.30 Path Delay Variations for 75-Mile Line-of-Sight Loop

fog on several of the days. During the late morning, the sun burned this fog off and bright sunny skies were generally experienced through the mid-afternoon.

The plot shown in Figure 4.31 is actually part of the same run that we have been discussing in previous paragraphs. The main distinction is that the time scale is expanded in this second graph to show more detail in the time structure. Each point marked with an x is a 1-minute average of the master/slave clock difference. This portion of the run went from 4 p.m. local time to 9 a.m. the next day, so the path length is long compared with the daytime portions of Figure 4.30.

In the July series, limited data were acquired for LOS path delay by transmission of a PN sequence around the 75-mile Verona-Stockbridge-Ava loop. Comparison of the transmit and receive times allowed total loop transit time to be established. After correction for PN period ambiguities and elimination of estimated equipment delays, the radio path transit time resulted; the computed samples for portions of a two-day period are shown in Figure 4.32. The points shown represent averages of a few seconds as provided by the counter, with measurements taken every 30 minutes except when rapid variation was apparent. Over a period of several days, there was a path length change of $\pm$ 4 ns, except for a heavy rainstorm which, for a period of a few minutes, increased the delay by 10 ns over the nominal path. The same diurnal trend was also observed with an increase in path length throughout the afternoon from a minimum in the middle of the day.

4.7 Clock Control Demonstration Tests

In the October series of field tests, there were three types of experiments carried out. They were:

(1) Master/slave transient tests for initial phase and frequency offsets between the two clocks.

(2) LOS steady-state clock tracking tests using single-ended master/slave techniques.

(3) TROPO steady-state clock tracking tests using single-ended master/slave techniques.

The transient runs and interpretation of results are covered fully in Section 5, and will not be discussed here.

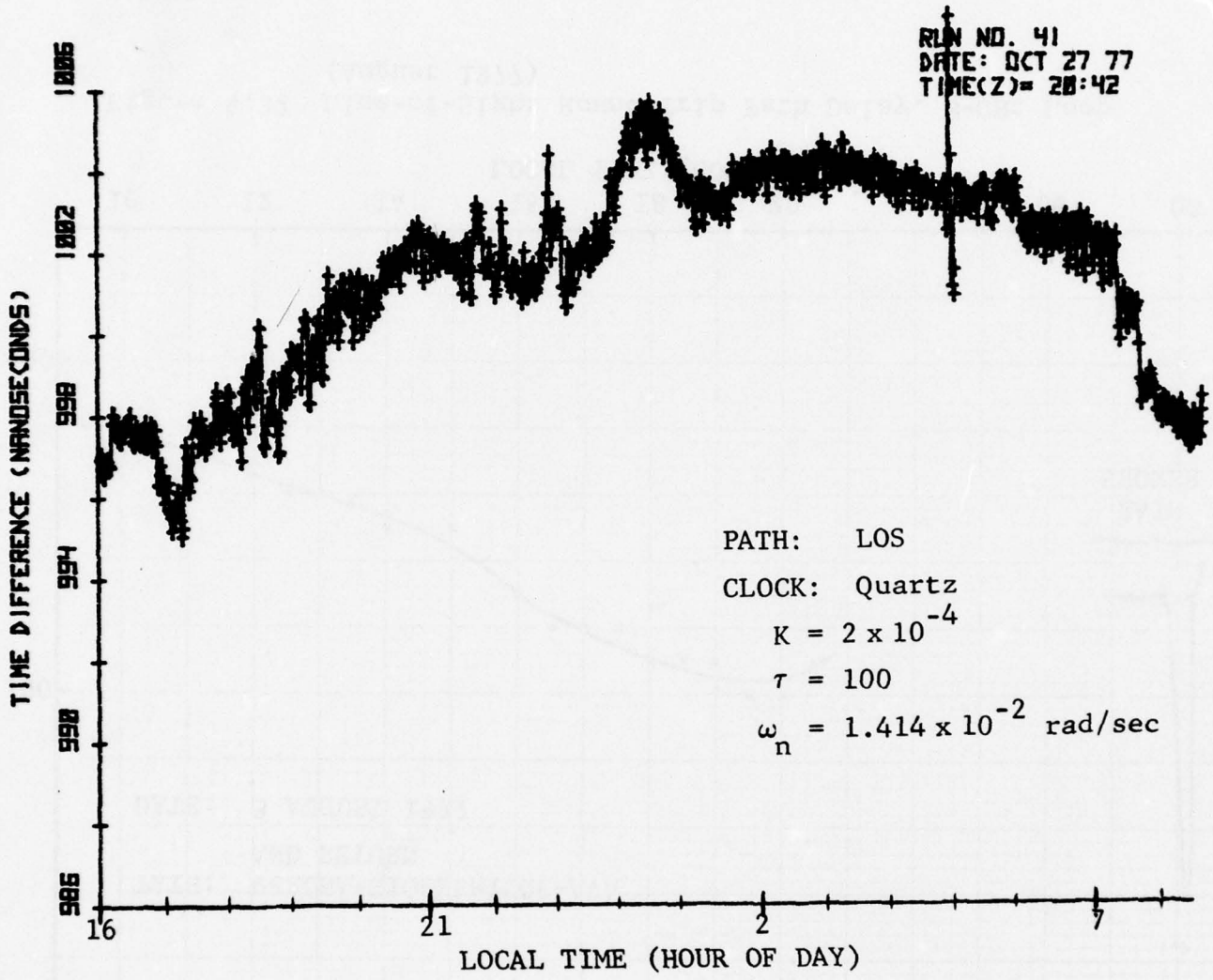


Figure 4.31 LOS Path Delay Variation on Expanded Time Scale

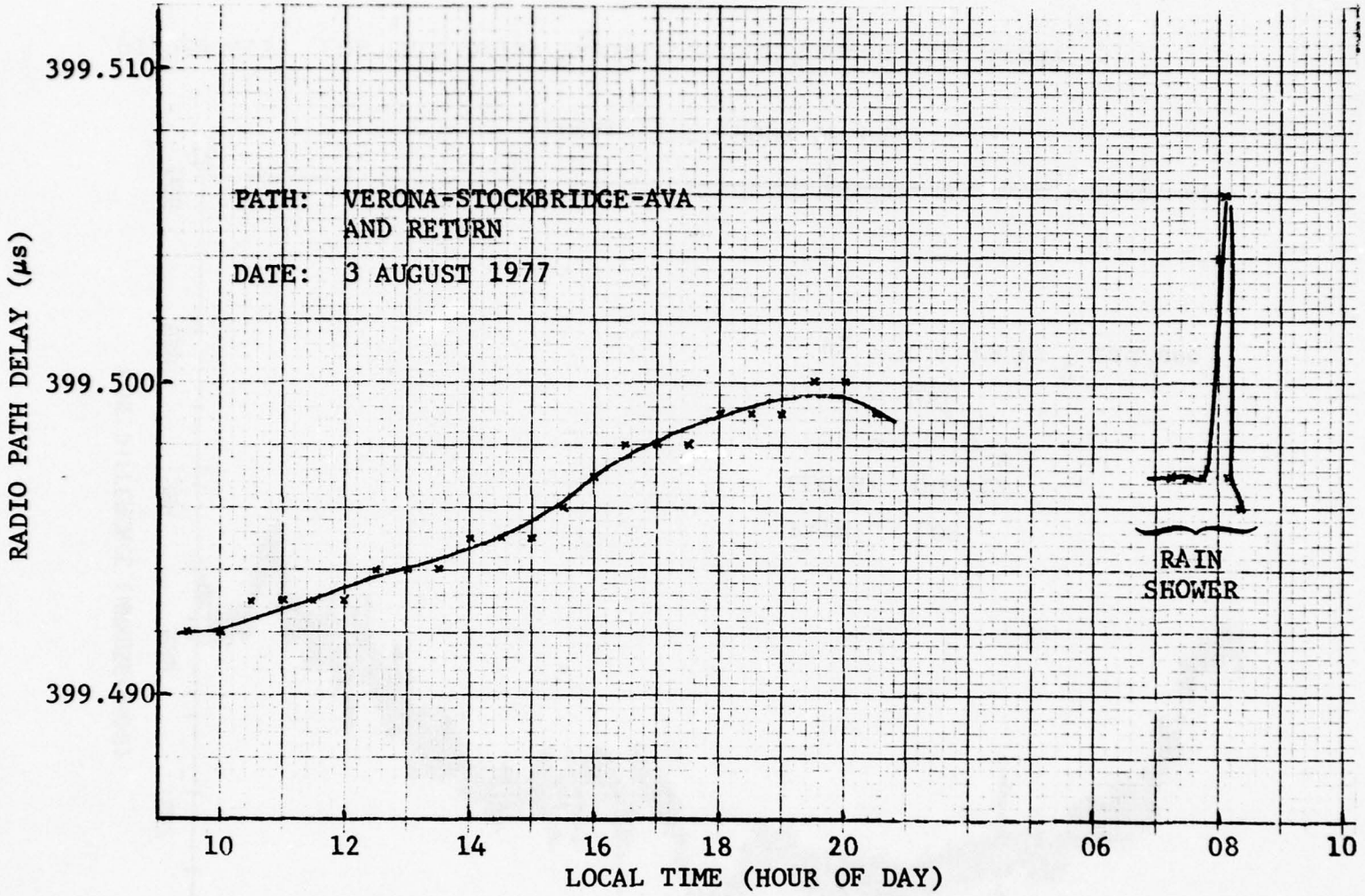


Figure 4.32 Line-of-Sight Round-Trip Path Delay, 8-GHz Loop (August 1977)

The LOS clock synchronization tests were described in Section 4.6, where the medium variability was being considered (see Figures 4.30 and 4.31). Briefly, the objective was to align a quartz slave clock to the master cesium clock via a 75-mile LOS transmission loop. The slaved quartz clock was extracted from one of the HP standards running open loop. Initially, the standard control voltage was set to be close to zero, so that the quartz was on frequency. Period measurements for the open loop quartz were taken over a 4-day interval; the results are reported in Table 4-14. The values shown in the right-hand column represent the change in period from the nominal of 200 ns. Thus, the first measured period was 199.999 999 86. Throughout the 4-day run, the period increased gradually. Unfortunately, the middle two days correspond to a weekend and, since the sites were unattended during this time, no period measurements were made. As a result, these data look a little sketchy when plotted as a time function, and we have chosen not to do so here. However, it is interesting to compute the total accumulated phase drift that occurs between the uncorrected quartz clock and the master cesium.* This will be done now assuming a linear frequency vs. time drift characteristic for the quartz clock.

First we use the period measurements at 1105 on 10/28 and 0900 on 10/31 to find the drift rate:

$$\text{Period at start } (t = 0) \quad T_0 = 200.000\,000\,00 \text{ ns}$$

$$\text{Period at end } (t = t_3) \quad T_3 = 200.000\,000\,43 \text{ ns}$$

Therefore, the frequency drift rate

$$\dot{\Delta f} = \frac{\left(\frac{1}{T_0} - \frac{1}{T_3}\right)}{t_3} \quad \text{Hz}$$

The quantity $\dot{\Delta f}$ is the effective change in frequency vs. time. For the 3-day interval above, we get an accumulated phase shift of:

*Recall that the master/slave demonstrations used a microstepper to phase shift the output of the quartz clock in order to remain in synchronism with the reference.

TABLE 4-14

PERIOD MEASUREMENTS FOR THE QUARTZ CLOCK USED IN LOS MASTER/SLAVE TESTS

Date	Time of Day	Elapsed Time	Period Deviation $\Delta\tau$ from Nominal ns x 10^{-6}
10/27	0900	0000	- 0.14
	1200	0300	- 0.14
	1430	0530	- 0.20
10/28	0900	2400	- 0.06
	1105	2605	0
	1245	2745	+ 0.03
	1450	2950	+ 0.05
	1645	3145	+ 0.09
10/31	0910	9600	+ 0.43

$$\text{Period} = 200.000 + (\Delta\tau \times 10^{-6}) \text{ ns}$$

$$x(t_3) = \int_0^{t_3} (\dot{\Delta f})t \, dt$$

$$= \frac{t_3^2}{2} \dot{\Delta f}$$

$$= \left(\frac{t_3}{2}\right)\left(\frac{1}{T_0} - \frac{1}{T_3}\right) \quad \text{cycles}$$

$$\simeq \left(\frac{t_3}{2}\right)\left(\frac{0.43 \times 10^{-6}}{T_0}\right) \quad \text{nanoseconds}$$

Substituting for $\frac{1}{T_0} = 5 \times 10^6$ and $t_3 = 3$ days, we have

$$x(t_3) = 278.64 \ \mu s$$

Given the enormity of this number relative to the clock differences plotted in Figure 4.30, there is certainly no doubt that the servo loop was functioning correctly. It is also interesting to compute the phase offset required at the servo loop input to support the quoted frequency drift. In Section 5 the steady-state loop characteristics are studied in more detail. It suffices to say here that, for a constant rate of frequency drift $\dot{\Delta f}$, the steady-state clock error is:

$$\epsilon = \frac{\dot{\Delta f}}{K}$$

The units of K are $(\text{sec})^{-2}$. Expressing $\dot{\Delta f}$ in ns/s, we get an error

$$\epsilon = \left(\frac{\dot{\Delta f} \times T_0 \times 10^9}{K}\right) \text{ ns} \qquad \text{for } T_0 \text{ in seconds}$$

This reduces to

$$\epsilon = \left(\frac{\Delta T}{t_3 T_0^2}\right)\left(\frac{T_0}{K}\right) 10^9$$

$$= \left(\frac{0.43 \times 10^{-6}}{200}\right)\left(\frac{1}{2 \times 10^{-4}}\right)\left(\frac{10^9}{3600 \times 24 \times 3}\right)$$

$$= 0.04 \text{ ns}$$

A bias of this magnitude is therefore introduced into the clock difference measurement (Figures 4.30 and 4.31), but it is so small that it can safely be ignored.

The final clock control experiments attempted involved a single-ended master/slave time transfer between the Verona and Youngstown sites via a troposcatter link. Unfortunately, problems with the 6-Mb/s MDTS modem left very little time for demonstration of TROPO time transfer.

The configuration consisted of a cesium clock slaved to a second cesium clock acting as master. The path was the Verona/Youngstown/Verona loop shown in Figure 3.14 with MDTS TROPO modems at both ends. The two cesium standards were quite closely aligned when disconnected from the control loop, so the real objective of the tests was to demonstrate that, with a sufficiently long loop time constant, the path length fluctuations could be averaged out. When one examines the TROPO path length data in Section 4.4, it becomes apparent that averaging times of a day or so are desirable. This, in turn, means that the experiment must be run continuously over a period of several days just to allow transient effects to die out. Our schedule allowed only about two days of continuous TROPO operation, so the results of the testing are not very enlightening. However, some of the difficulties of single-ended time transfer via TROPO paths are certainly brought out.

In Figure 4.33 we show a preliminary run of about 4-hours duration beginning around noon. This configuration involved the 1-GHz MRC-98 path and a loop time constant of about 10 minutes. The variation between the master and slave clocks is

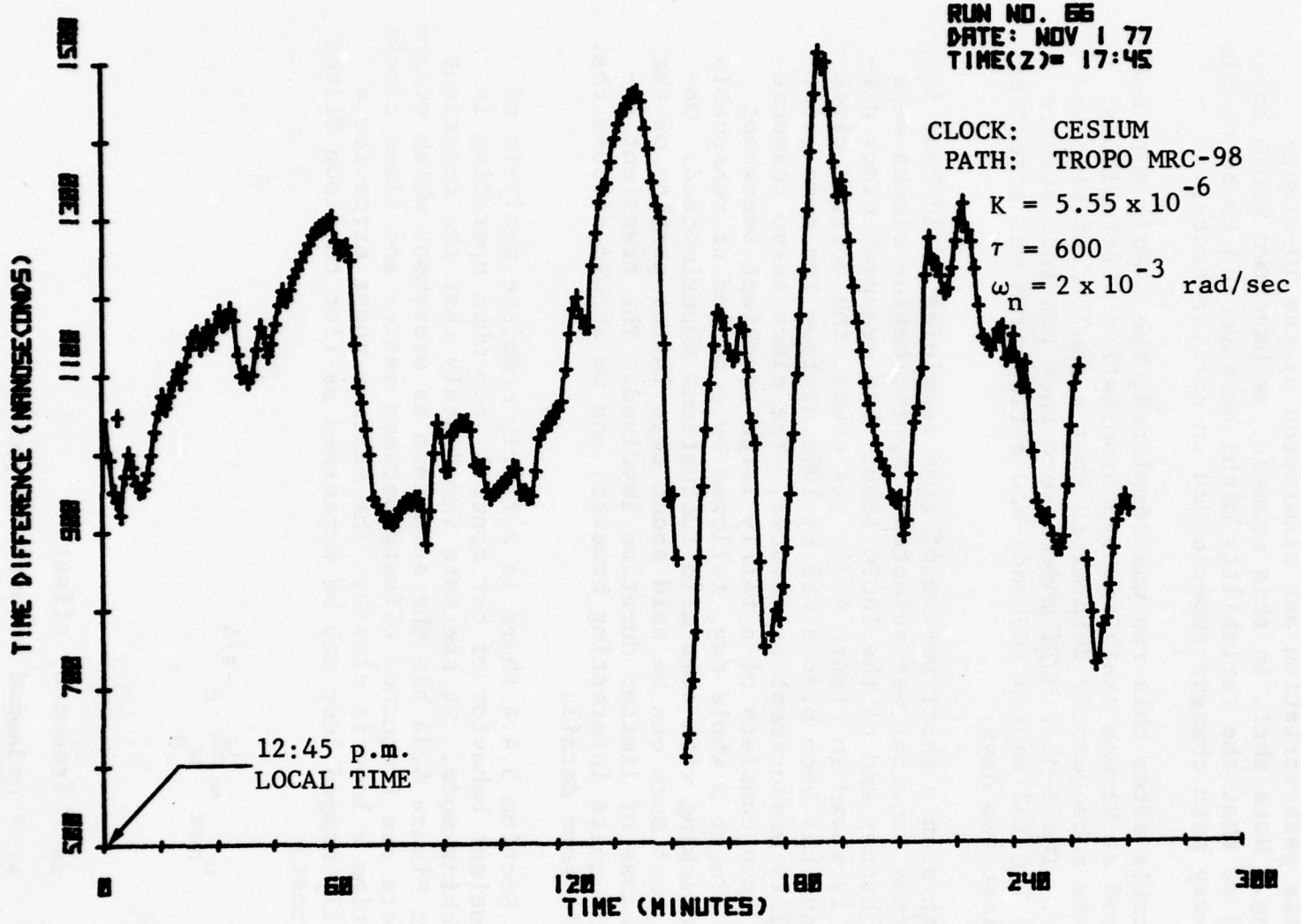


Figure 4.33 Master/Slave TROPO Time Transfer Experiment with 10-Minute Loop Filter Time Constant

plotted and, as expected, has about the same character as the earlier path length data. That is, the plot of Figure 4.33 represents path variation not eliminated by the 10-minute averaging. Note that, in this example, we have two TROPO hops tandemed so that the variability might be expected to be double the one-way path changes experienced in earlier tests.

Shortly after this run was completed, the 6-Mb/s MDTS modem being used at Verona exhibited synchronization difficulties, and it was subsequently determined that a fault condition had occurred. The 3-Mb/s MDTS modems were then put into service with the TRC-132 radios (C-band) and a final run was attempted in the last two days.

With such a short period of time remaining, a 10-hour loop filter time constant was selected. Again, cesium clocks were used at either end of the TROPO loop. The measured clock difference is shown in Figure 4.34. As usual, the desired clock difference has been biased off by 1000 ns from the zero point to simplify measurement procedures. The clock servo response in this case consists of a fairly large transient overshoot lasting almost a whole day, followed by a period of reasonably stable tracking with some mild fuctuations superimposed. Obviously, not much can be said about this latter portion of the plot because of limited duration involved. The transient response is quite interesting however, and we should discuss that aspect in more detail.

In Section 5.4.4 there is a fairly complete analysis of the transient behavior of our control loop when operating in the tracking mode. We can note immediately that the transient shown in Figure 4.34 has the same form as overshoot which occurs when there are frequency offsets between master and slave clocks at the time a loop is closed. The maximum phase error for a critically damped loop may be expressed as (for the loop filter of interest):

$$u_{max} = \frac{\Delta f}{\omega_n} e^{-\pi/4}$$

where

Δf = frequency offset

ω_n = undamped natural frequency
$= \sqrt{K}$

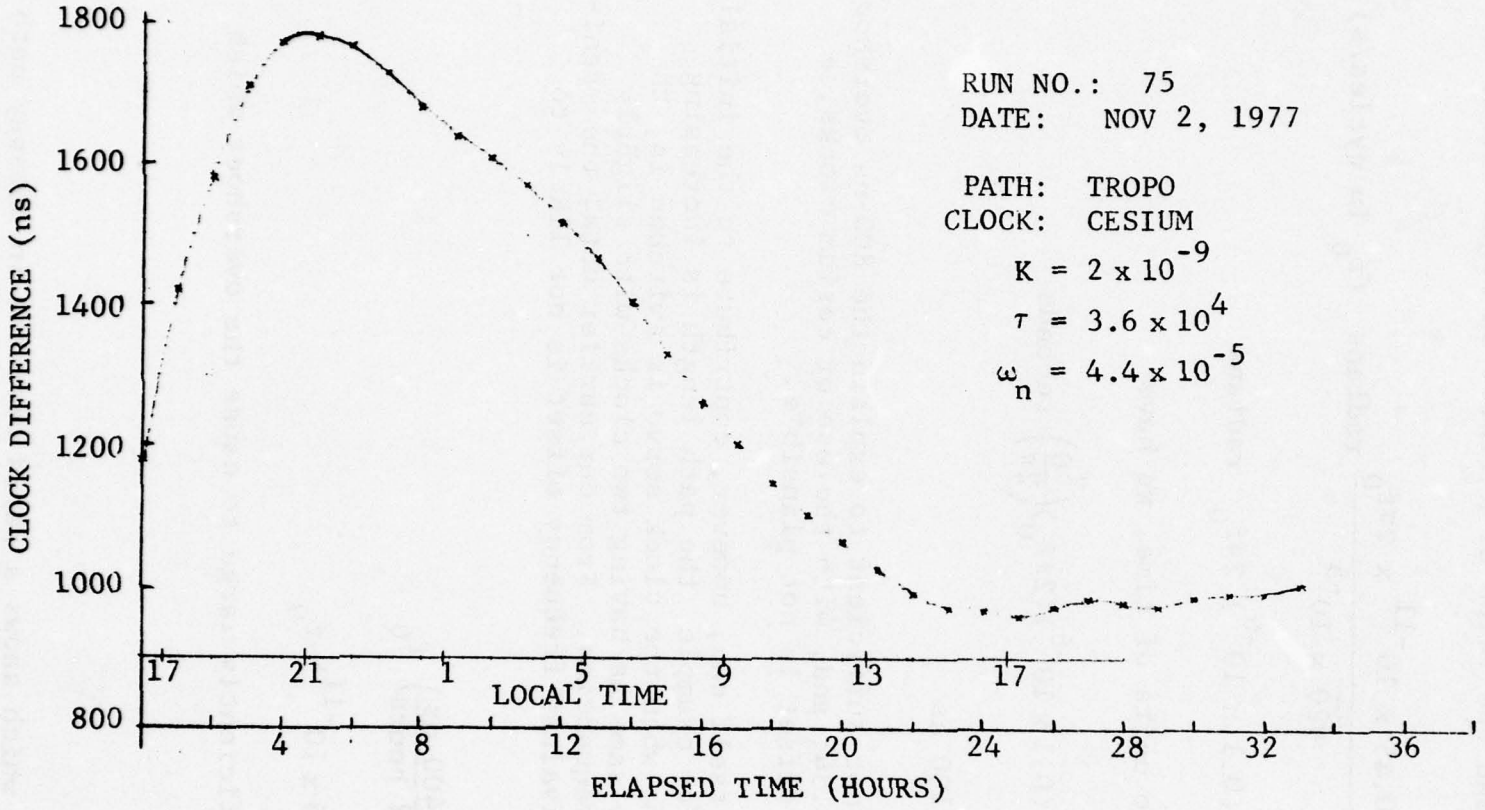


Figure 4.34 Master/Slave Clock Control Response

Thus, if we consider a worst-case offset of 1×10^{-11} for the cesium standards and the value of K listed on Figure 4.34, we get:

$$u_{max} = \frac{0.45 \times 10^{-11} \times 2\pi f_0}{\sqrt{20} \times 10^{-5}} \text{ radians} \quad (f_0 \text{ in cycles/s})$$

$$= (0.1 \times 10^{-6})\ 2\pi f_0 \text{ radians}$$

Converting this to units of time, we have

$$u_{max} = (0.1 \times 10^{-6})(2\pi f_0)\left(\frac{T_0}{2\pi}\right) \text{ seconds}$$

$$= 100 \text{ ns}$$

Clearly, this is not sufficient to explain the 800-ns overshoot shown in Figure 4.34; and, with the use of cesium clocks, a larger frequency offset is not plausible.

The medium itself can, however, contribute to the initial transient. If, for example, the path length is increasing steadily with time when the clock servo is switched in, the net effect is the same as having two clocks with slightly different rest frequencies. From our earlier data, the magnitude of this equivalent frequency offset is not likely to exceed*

$$\Delta f = \left(\frac{400 \text{ ns}}{2 \text{ hours}}\right) f_0$$

$$\simeq (5 \times 10^{-11})\ f_0$$

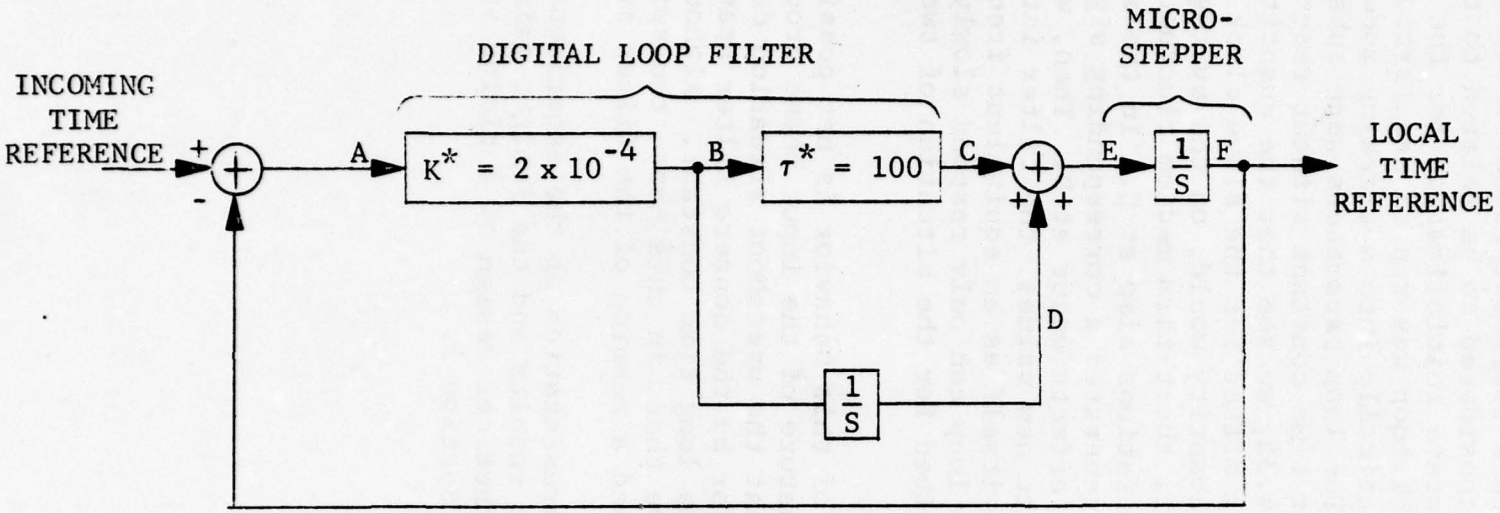
which is not sufficiently large to cause the overshoot which was measured.

*See Figure 4.22 which shows a rapid decrease in one-way path length on the 4690-GHz path during the later afternoon hours.

Although the cause of this overshoot is not known definitively at this time, it is considered to be related to the problem of acquisition and state initialization for the servo system. Initially, the clock loop was run in acquisition after which it was switched automatically into a tracking mode with a 100-second time constant. The loop parameters were subsequently changed to provide a 10-hour time constant without resetting the loop. Referring to Figure 4.35, we see that the quantity at E represents a rate command or offset for the slave clock. With a 10^{-11} clock offset, this quantity would, on the average, have a value 10^{-2} ns/s^2. However, short-term medium fluctuations appearing at A result in variations also at C. In the situation shown, a 100-ns error at A generates a corresponding signal of magnitude 2 ns/s^2. Similar effects occur at D. Then, when the gains K and τ are switched to new values, the filter integrator starting state (D) reflects itself as an equivalent frequency offset command to which the loop can only respond slowly and in the manner previously described for the situation of two clocks offset in frequency.

The detailed analysis of this behavior is not possible because of the stochastic nature of the input phase process. It is apparent, however, that the overshoot situation described could easily be accounted for by the nonzero filter state at the time of switching to the long time constant. Although it is not always so, we believe that, in this case, the switching strategy should have involved a zeroing of the filter state.

Having completed our presentation of the experimental data, we now proceed to apply the results and the insight gained from the field work to the hypothetical design of a timing subsystem. This subject is covered in Section 5.



*INITIAL TRACKING PARAMETERS.
AFTER SWITCHING, $K = 2 \times 10^{-9}$
$\tau = 3.6 \times 10^{4}$

Figure 4.35 Clock Servo Block Diagram

REFERENCES

[4.1] P. A. Bello, "A Study of the Relationship Between Multipath Distortion and Wavenumber Spectrum of Refractive Index in Radio Links," Proc. IEEE, January 1971, pp. 47 - 75.

[4.2] R. F. Harrington, Time Harmonic Electromagnetic Fields, McGraw-Hill, New York, 1961, pp. 116 - 120.

[4.3] A. Sherwood and L. Suyemoto, "Multipath Measurements over Troposcatter Paths," MITRE Technical Report MTP-170, April 1976, pp. 102 - 103.

SECTION 5

TIMING SUBSYSTEM DESIGN CONSIDERATIONS

5.1 Timing Subsystem Integration with DCS Equipment

It is clear that a timing subsystem and time or frequency synchronization technique should be developed so as to be compatible with other specified DCS components. Since equipment modifications and retrofits are inclined to be expensive for operational units, the interfacing in question should be as simple as possible. This section describes the general characteristics of the DCS transmission system, and the recommended method of implementing a time transfer scheme.

5.1.1 DCS System Elements

The existing DCS network is based almost exclusively on analog circuits, with digital transmission capabilities being provided by *quasi-analog methods*, such as the use of a data modem within a single analog voice channel. Dedicated command and control networks also exist, with a heavy reliance being placed on voice and tone signaling. As progress is made toward implementation of an all-digital network, some new problems arise, particularly concerning systemwide timing and synchronization.

Performance of the individual digital links ultimately determines overall network performance. The most important performance characteristics for a link are:

(1) Bit error rate
(2) Timing jitter and delay
(3) Time to loss of bit count integrity

Other characteristics, such as error-free run length distributions and block error distributions, also have a bearing on performance of certain equipment.

Table 5-1 summarizes the performance objectives for a line-of-sight digital link consisting of a cascade of LOS hops [5.1]. Also shown is the total for a reference 12,000-nm circuit consisting of a 3000-mile satellite link, a 3000-mile submarine cable, and many LOS links. Table 5-2 indicates error

TABLE 5-1*

LOS DIGITAL TRANSMISSION PERFORMANCE OBJECTIVES

Performance Parameter	Allocation Per LOS Hop	Allocation Per Digital Link	Total (Subsystem)	Total (12,000 nmi Circuit)
1. Availability	0.99995	$0.99995^{N(1)}$	$0.99995^{Nn(2)}$	0.99
2. Bit Error Rate	5×10^{-9}	5×10^{-9} N	5×10^{-9} Nn	5×10^{-6}
3. Error Free Seconds				99.99% (4)
4. Bit Count Integrity (mean time to loss of		24 n hours	24 hours	
5. Jitter				
(a) Maximum Departure (3)	1/4 bit interval			
(b) Short-term Stability of Bit Timing Rate	$\frac{1 \times 10^{-2}}{N}$	1×10^{-2}		
6. Noise (equivalent PCM noise)		316 pWp^0	316 pWp^0	3160 pWp^0

*From [5.1]

(1) N is the number of LOS hops in the digital link.
(2) n is the number of digital links in the subsystem.
(3) Maximum departure from nominal transition time at the timing recovery and regeneration point.
(4) Being considered for digital data services.

TABLE 5-2*

MEGABIT DIGITAL TROPOSCATTER SUBSYSTEM OBJECTIVES

1. Bit Rates: 12.6 Mb/s for path length up to 150 nmi
   6.3 Mb/s for path length up to 250 nmi

2. Ber:

% of All Hours of the Year	Path Length (nmi)		
	Up to 100	100 to 200	200 to 250
99.00	10^{-8}	10^{-7}	5×10^{-7}
99.90	10^{-7}	10^{-6}	5×10^{-6}
99.99	10^{-6}	10^{-5}	5×10^{-5}

*From [5.1]

rate objectives for troposcatter systems which will be included eventually in the digital network.

The DCS network will be configured from a variety of interconnected elements including multiplexers, clocks, modems, codecs, and radios. In addition, certain network control functions must be provided, such as timing synchronization and performance monitoring for switching to standby subsystems.

Figure 5.1 shows some of the basic elements of a single node, and indicates explicitly the service channel which would normally be used to provide monitoring and control data transfers. In Figure 5.1, dark lines indicate data connections while fine lines are used to show clock and control signal transfers. The main data stream is typically two to eight medium-speed lines (1.544 Mb/s) multiplexed together to give a total data rate of up to 12.9 Mb/s at the output of level-2 MUX. Multiplexed into this bit stream is an overhead channel containing framing, control, and bit stuffing information.

The multiplexer hierarchy for the DCS network consists of three distinct levels. It suffices to say here that the sub-MUX combines bit streams with rates n x 1.2 kb/s or n x 8 kb/s into one or more 64-kb/s PCM equivalent bit streams, while the level-1 MUX combines 24 64-kb/s digital input lines to give an output at 1.544 Mb/s. This output will be referred to as a digital group (digroup); the second level MUX then combines two or more digroups for transmission over the medium.

Overall network synchronization and control depends on the interaction between individual node subsystems and a master control subsystem. Each node may, of course, provide a termination for several links, each with its own link control subsystem, while the node itself will have certain components which are common to all links attached to the node, e.g., the node clock and clock control subsystem.

The control and timing features of a node are shown more explicitly in Figure 5.2. These subsystems then provide data to the system control center, and control directives are returned. The node subsystems can be listed as follows:

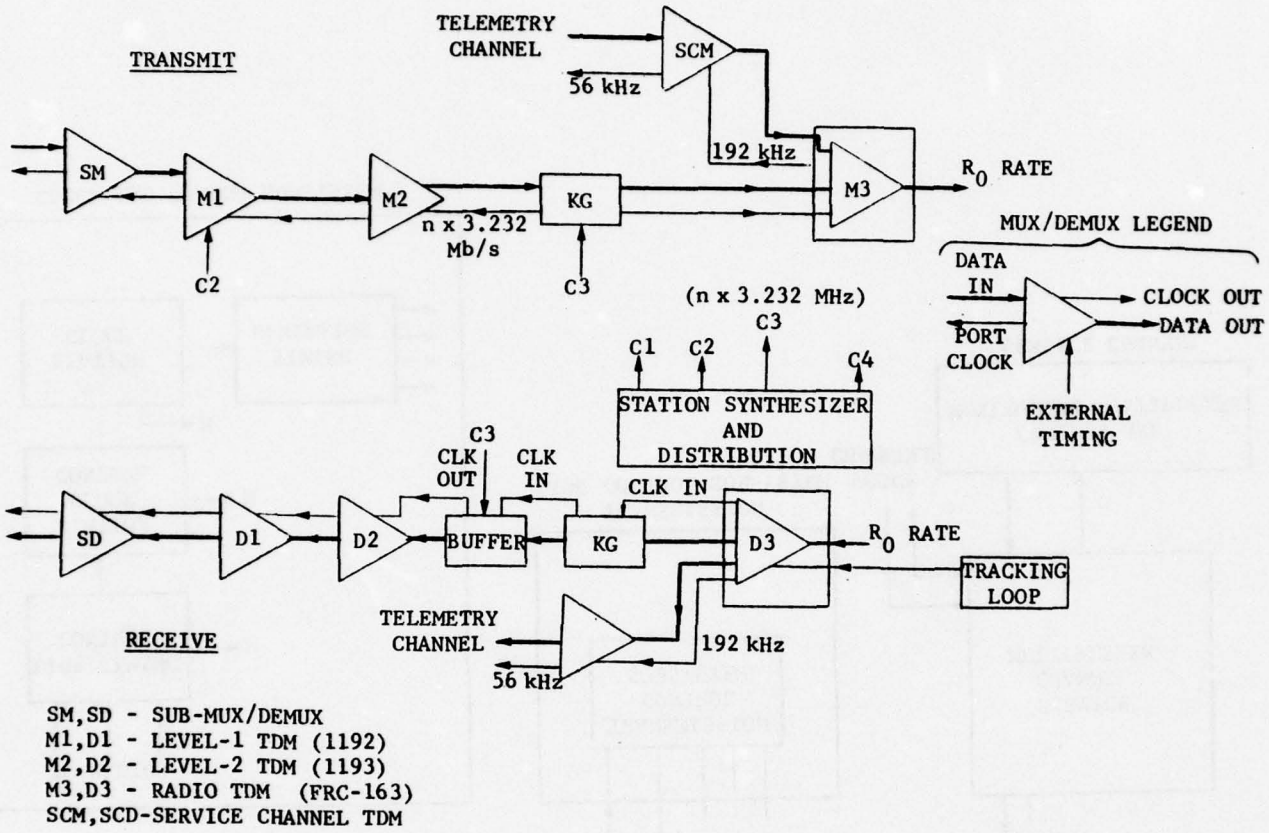


Figure 5.1 Illustration of Station Timing Distribution for Synchronous Network

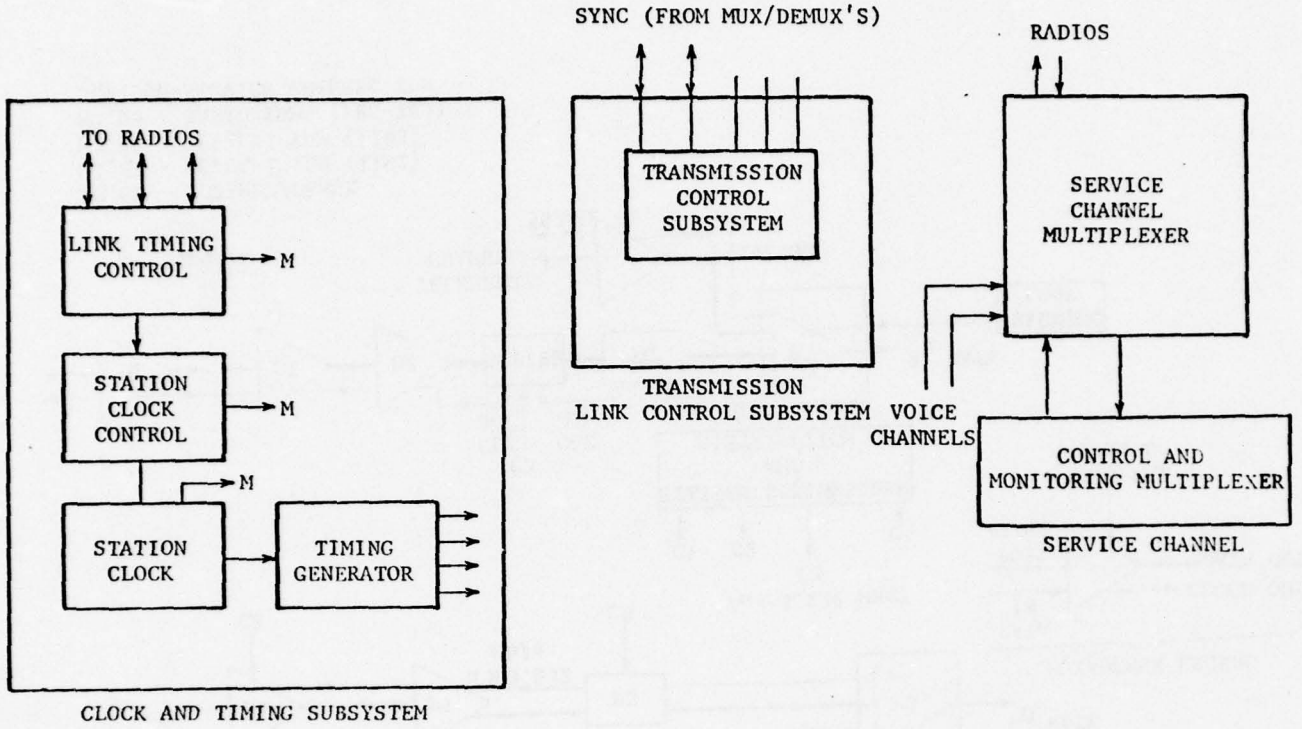


Figure 5.2 Control and Timing Subsystems at a Node

(1) Link Timing and Clock Control Subsystem
In this unit the measured incoming bit rates are sensed for each terminating link, and combined according to some control algorithm to provide a station clock correction and synthesized clocks for use internal to the station.

(2) Transmission Link Control Subsystem
This equipment is concerned with the maintenance of synchronization on the individual links, and accordingly, monitors the status of node multiplexers. It attempts to minimize the frequency and duration of resynchronization attempts.

(3) Service Channel Multiplexer
The transfer of control and monitored data from node to node is implemented by means of a system service channel, multiplexed into the outgoing signals.

The service channel plays an important role in system coordination. It will be implemented as a digital channel multiplexed at the radio. Note that, with the all-digital approach, a strong framing pattern must be provided for the service channel to hold synchronization under worst-case conditions. The current specifications for the DCS digital network [5.2] indicate that the telemetry channel will be either 50 kb/s asynchronous or 56 kb/s synchronous. It will be combined with two voice service channels to give a total service channel data rate of 192 kb/s, and will be multiplexed with the mission bit stream at the radio. However, each node must have access to this telemetry channel, requiring the development and exercise of a line protocol by the system control center. The current specifications [5.2] call for a minimum data insertion capability of 600 b/s at each transmitting site. The service channel allows system maintenance and control functions to be achieved, as well as the synchronization of all network nodes by exchange of timing information.

The function of system maintenance and control is to assure that the system performance objectives are met. In this regard, critical parameters must be measured throughout the system and transferred back to the nearest system control center. Maintenance and control will be facilitated by the availability of

standby equipment, built-in diagnostics and fault isolation, and performance assessment capabilities. Various techiques have been proposed for estimating the performance margin of an operational system, including pilot signals and loop back measurement of out-of-service units. Performance data along with node equipment fault indications can be acted on by the system control center in such a way as to increase the performance margin.

Network timing information can be relayed over the telemetry service channel. It would include, for example, buffer status and node clock phase relative to the receiving node clock. However, before discussing such details, we need to examine the various DCS time transfer options that are available, and this is done below.

5.1.2 Transfer of Timing Events in DCS

The distribution of time throughout the DCS network can most readily be superimposed onto the normal network communications functions by taking advantage of available overhead and monitoring signals built into the specified transmission rates. Some candidate signals include:

(1) Level-1 or level-2 MUX/DEMUX frame sync patterns

(2) Radio (i.e., level-3) MUX/DEMUX frame sync patterns

(3) The system service channel (i.e., burst or pulse types of reference signals)

While these particular signals have received a great deal of attention as candidate time reference signals (i.e., the TRP's of Section 2.1.2), the choice is not clear-cut by any means, and it is only after a very thorough examination of DCS equipment characteristics that a suitable selection can be made.

In Figure 5.1 we indicated the equipment modules which would be present for each link termination, and in Figure 5.3 we give a preview of the timing subsystem elements and the DCS equipment interfaces required. Most of the specified equipment is sufficiently flexible to allow the use of alternative station reference signals instead of the data/clock cascade scheme shown, e.g., the service channel MUX can be supplied with a 192-kHz clock from the station synthesizer.

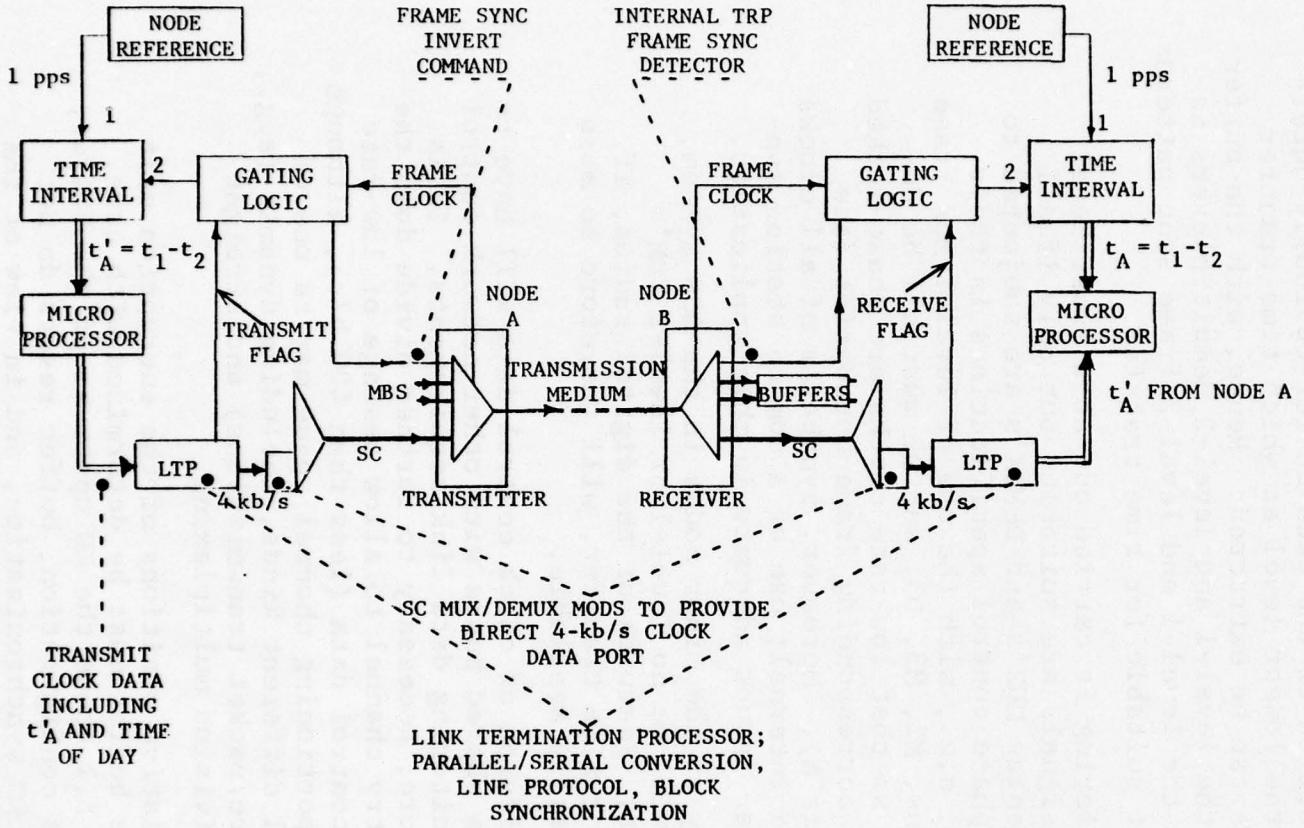


Figure 5.3 Block Diagram of Timing Subsystem and DCS Interfaces

The following brief points can be made concerning the signals listed above and the equivalent hardware components shown earlier in this section on Figure 5.1.

- The position of the data buffer obviously determines the lowest level at which time transfer signals can be extracted. Hence, with the buffer above the level-1 and level-2 demultiplexers as shown, the level-1 and level-2 frame sync patterns are not suitable for time transfer.
- If buffering is carried out at a lower level, these signals are suitable, but only if all intervening MUX's and DEMUX's are subjected to rigid phase control specifications in their design, e.g., with the use of level-1 MUX frame patterns, M2, M3, D3, and D2 must all be designed so that low-rate clocks are phase-locked to the corresponding frame boundaries (see Appendix A). Moreover, synthesis of all clocks must be internal; use of a common station synthesizer is not adequate in this application.
- At many of the minor nodes in the DCS system, there will be no level-1 or level-2 TDM's present. Features of the digital radios, if used for time transfer, will therefore be more universally available.
- Transmission of clock control data will have to be on a shared basis with other network control and monitoring data link requirements. It is, therefore, necessary to further divide down the telemetry channel to allow passage of low-rate clock control data (less than 400 b/s), although the apportioning channel space may be one of several different kinds, including dynamic (e.g., software/packet transmissions) and straight time-division multiplexing.
- The relative positions of the encryption unit and the buffer must be determined with care. Figure 5.1 shows the KG upstream of the buffer; in this configuration, buffer resets do not affect KG synchronization, and in view of the high resynchronization overheads, this is considered desirable. Note that, although it is not shown explicitly, separate encryption of the

telemetry channel (Figure 5.1) may also be a requirement, in which case the delay characteristics of the selected device must be considered carefully.

The stated accuracy requirement for the complete system is 2 μs. Working backward from this figure to an individual link error budget, it is inferred that 100 ns or better time transfer accuracy is required on a per-link basis. The difficulty with the level-1/level-2 TDM or service channel approaches is that there will generally be equipment delay uncertainties present which are independent for the forward and return link directions. With the level-2 DEMUX frame, for example, there will be a time-of-arrival uncertainty of one bit at the mission bit stream rates, which may amount to 300-ns differential delay at the low rates. Appendix A provides a full discussion of this difficulty, and the theoretical treatment of the subject given there is supported by delay measurements carried out on a candidate DCS TROPO modem (MDTS) to confirm the prior analysis. For the service channel, accuracy is even more severely impaired if stringent precautions are not taken to maintain timing integrity. With the use of an 8-kb/s subchannel multiplexed into the service channel, for example, the delay uncertainty may very easily exceed 125 μs, depending on the method of implementation (e.g., use of internal FIFO data buffers). Again, the reader is referred to Appendix A for more details, and to Appendix B for a more specific treatment of the 1192 TDM properties relevant to its use as a service channel TDM.

Table 5-3 provides a summary of the delay components for various DCS transmission components, and includes estimates of both the fixed (permanent) delay as well as delay uncertainties (variations exhibited as equipment is taken out and put back into service, for example). This data was tabulated from earlier analyses carried out (Appendices A and B) and, in many cases, the entries were inferred from specifications and quite sketchy descriptions of circuit operation currently available. In some cases, definite conclusions cannot be drawn without additional information (e.g., FRC-163 synthesizer details) and the estimates may be pessimistic.

The radio (level-3) sync pattern option listed previously does not suffer from these serious drawbacks, which are a consequence of passage through multiplexers and demultiplexers subjected to arbitrary synthesizer phase initialization. Moreover, the radio framing patterns are, of necessity, quite robust

TABLE 5-3

SUMMARY OF WORST-CASE DCS EQUIPMENT DELAY COMPONENTS

Equipment	Function	Constant Delay (μs)	Delay Uncertainty Limits (μs)
1192 as a Service Channel MUX	56-kHz derived clock (arbitrary phasing)	0	± 9.0
	56-kHz clock jitter (pulse deletion)	0	+ 0.25
	56-kb/s FIFO's half-full (4 bits at 56 kHz)	72	±18.0
	Serial 56 kb/s / Serial 1.544 Mb/s waiting time	120	0
	Serial/parallel waiting time	4.2	0
	192-kHz clock jitter (pulse deletion)	0	+ 0.04
	NRZ receiver/driver (1 each)	?	?
1192 as a Service Channel DEMUX	192-kHz derived clock jitter	0	+ 0.04
	192-kb/s FIFO's half-full (4 bits at 192 kb/s)	20	± 5.0
	Serial/parallel waiting time	35	0
	56-kHz clock jitter (pulse deletion)	0	+ 0.25
	56-kHz derived clock (arbitrary clock phasing)	0	± 9.0
	NRZ receiver/driver (1 each)	?	?
FRC-163 Service Channel Back/Back	192-kHz synthesized clock (arbitrary phasing)	0	± 5.0
	Transmit and receive FIFO's (half-full, 32 bits each)	320	0
	NRZ receiver/driver (1 each)	?	?

TABLE 5-3 (Continued)

Equipment	Function	Constant Delay (μs)	Delay Uncertainty Limits (μs)
FRC-163 MBS Ports Back/Back (Worst-Case Data Rate 3.232 Mb/s)	Level-3 MUX/DEMUX (arbitrary clock phasing)	0	+ 0.3
	Transmit and receive FIFO buffers (half-full, 32 bits each)	19.2	0
	NRZ receiver/driver (1 each)	?	?
MDTS TROPO Modem Back/Back MBS Ports	Measured delay characteristics		
	at 6.276 Mb/s	6.4	± 0.18
	at 3.088 Mb/s	10.0	± 0.3

in terms of their protection from channel fades and jamming, and therefore provide a solid design base for the timing subsyste..

The elimination of all level-1 and level-2 multiplexer-based time reference schemes leaves three prime subsystem candidates. With a detailed examination of these in the following three subsections, a comprehensive view of the equipment and timing distribution problems will be presented to the reader.

Three figures, 5.4, 5.5, and 5.6, summarize the time transfer methodology in block diagram form in each case, as well as the timing relationships throughout the node equipment. For simplicity, a single simplex link is shown, with one set of transmitting equipment (node A) and one set of receiving equipment (node B). In general, a full duplex arrangement is more appropriate for individual links, and certain node equipment (such as the time interval and microprocessor units) will be time-shared for use on several link terminations.

To keep the diagrams and explanations concise, liberal use of abbreviations has been made, and Table 5-4 contains a glossary of the terminology.

5.1.2.1 Radio Sync Pattern Detection (Option A)

We first describe the operations illustrated in Figure 5.4. Direct access to the frame sync pattern at the transmit level-3 multiplexer is assumed. The technique involves modification or encoding of these sync bits (of which there are 16 placed contiguously at the start of each 250-μs frame); one very simple approach, as shown, is to simply invert them. Thus, when the node reference 1-pps pulse appears (at ① on the timing chart), a frame sync code inversion command is issued by the gate generator ③. The next frame sync burst, produced by the radio MUX, is inverted and a coincident frame clock pulse is brought out of the radio to be presented to the counter TI. The gate generator only allows a single clock pulse from the 4-kHz frame clock to pass. This particular frame pulse is referred to as the designated TRP, and the event is recognizable at the receiver because of the inverted sync pattern.

The receiver hardware is a little more complicated. The demodulator output must be tapped off for use by the external circuitry denoted "sync detector". This digital logic is meant to recognize the inverted frame sync pattern and, if it finds a

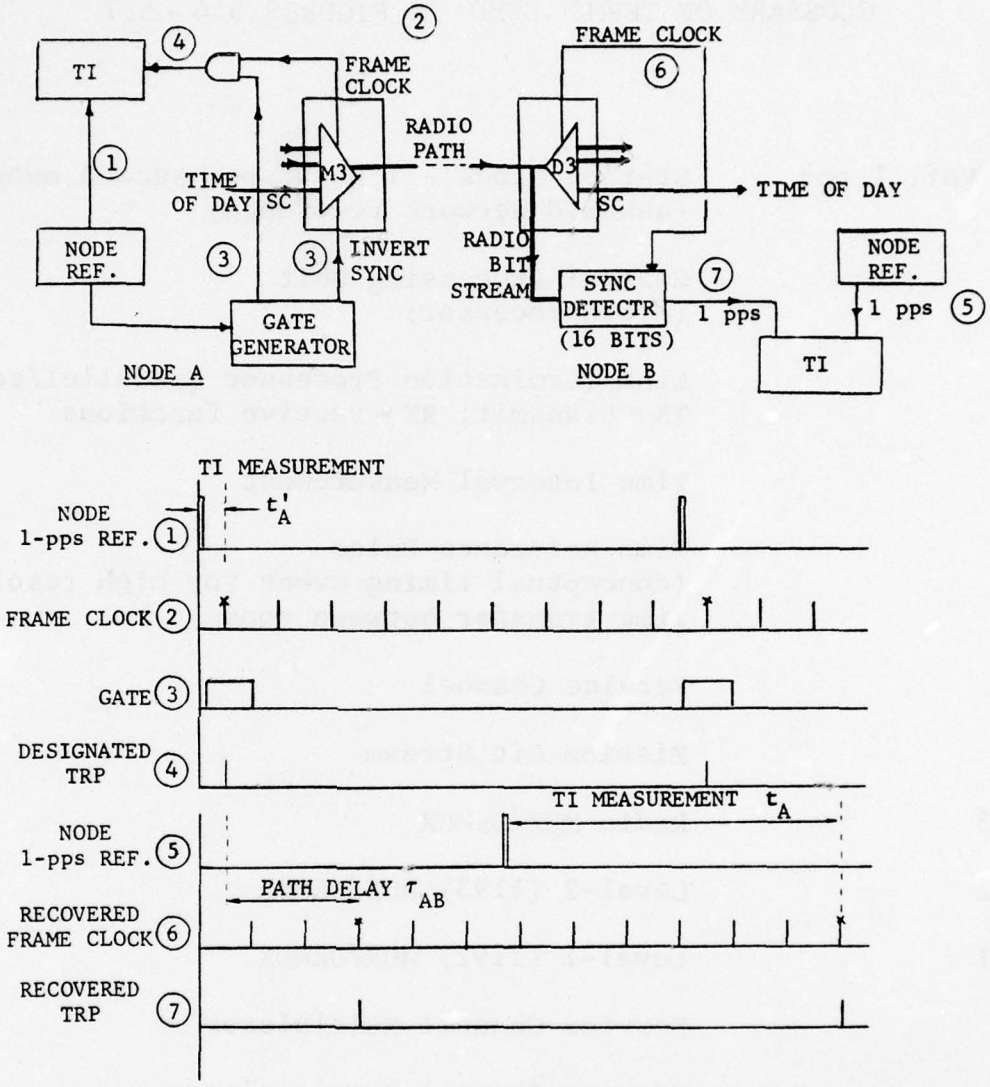


Figure 5.4 DCS Timing Transfer: Option A - Radio Sync Pattern Inversion/Detection

TABLE 5-4

GLOSSARY OF TERMS USED IN FIGURES 5.4 - 5.7

Node Ref. 1 pps	Station Clock - 1 pulse per second output (assumed network reference)
CPU	Central Processing Unit (Microprocessor)
LTP	Link Termination Processor (parallel/serial) TX = transmit; RX = receive functions
TI	Time Interval Measurement
TRP	Time Reference Pulse (conceptual timing event for high resolution time transfer between nodes)
SC	Service Channel
MBS	Mission Bit Stream
M3/D3	Radio MUX/DEMUX
M2/D2	Level-2 (1193) MUX/DEMUX
M1/D1	Level-1 (1192) MUX/DEMUX
SCM	Service Channel Multiplexer
SCD	Service Channel Demultiplexer
——→	Denotes serial data line
——→	Denotes clock or control signal lines

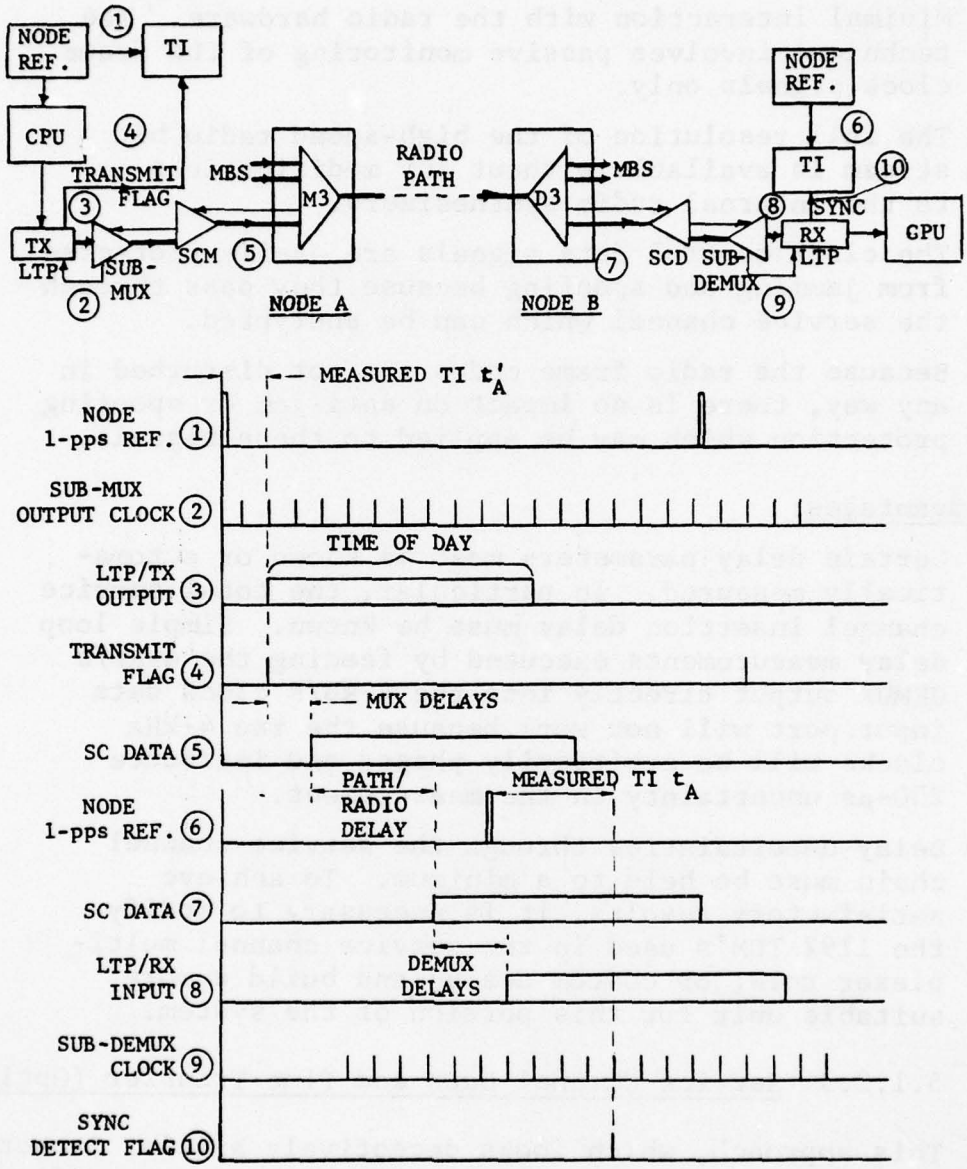


Figure 5.6 DCS Timing Transfer: Option C - Service Channel Data and Time Transfer

Advantages and disadvantages for option B are listed as follows:

Advantages:

- Minimal interaction with the radio hardware. The technique involves passive monitoring of the frame clock signals only.
- The full resolution of the high-speed radio bit stream is available without any modifications to the internal radio synthesizers.
- The clock control data signals are easily protected from jamming and spoofing because they pass through the service channel which can be encrypted.
- Because the radio frame codes are not disturbed in any way, there is no impact on anti-jam or spoofing protection which may be applied to these signals.

Disadvantages:

- Certain delay parameters must be known or automatically measured. In particular, the total service channel insertion delay must be known. Simple loop delay measurements executed by feeding the 4-kb/s DEMUX output directly into the 4-kb/s clock data input port will not work because the two 4-kHz clocks will be arbitrarily phased and introduce 250-μs uncertainty in the measurement.
- Delay uncertainties through the service channel chain must be held to a minimum. To achieve satisfactory results, it is necessary to modify the 1192 TDM's used in the service channel multiplexer role, or custom design and build a more suitable unit for this portion of the system.

5.1.2.3 Service Channel Data and Time Transfer (Option C)

This approach, which looks deceptively simple, is actually doomed to failure without quite massive equipment modifications. In particular, it would seem that the 1192 TDM must be rejected outright as a candidate for the service channel multiplexing tasks, mainly because of unsuitable clock synthesis techniques and serious FIFO buffer reset uncertainties (see Appendix B). At the very least, the service channel multiplexer would need to be custom-designed to meet the time transfer requirements, and

marked in the output bit stream except for the understanding that it corresponds to a particular point in the level-3 frame. It is the purpose of the service channel data transmission to resolve the ambiguity in frame choice and, to do so, requires controlled (albeit, relatively loose) delay through this channel.

At the receiving node, the arrival of data through the service channel is indicated by the LTP-RX sync flag (9). A gate is generated (10) from this flag to allow the next frame pulse to be extracted from the radio and sent to the TI unit (11) for comparison with the node reference. Unfortunately, this is not the frame marker designated as the TRP because of excess delay imposed by the service channel chain. With the aid of tabulated equipment delays, correction by a whole number of frame periods can be made to the measured quantity t_A.

As we have shown in Figure 5.5, there may be time delay uncertainty associated with the arrival of data transmitted through the telemetry portion of the service channel. Table 5-4 listed some of the potential uncertainties, and while these particular values are barely tolerable, our need for another level of service channel multiplexing down to 8 kb/s introduces far worse delay uncertainty, perhaps in excess of one bit interval (125 μs) above that shown in Table 5-4. Obviously, delay uncertainty in the data link should be much less than one radio frame interval (250 μs) if an unambiguous TRP transmission is to be made.

Fortunately, the service channel access can be designed with existing equipment modified to hold down the delay uncertainties to an acceptable level. One suitable approach is described in Section 3 of Appendix B; stated briefly, it suggests a modification to the 1192 TDM to allow direct 4-kb/s clock data access via bit 8 of the telemetry channel byte, thereby locking the 4-kHz timing signals to the 1192 frame boundary and eliminating the potential delay uncertainty alluded to above. Of course, the error budget implied by Table 5-4 still applies, but overall the delay uncertainty is a small fraction of the 250-μs radio frame.

In conclusion, it should be mentioned that the data packet transmitted from node A to node B will contain the measured parameters t_A' and t_B from the previous 1-second interval, along with the time-of-day data.

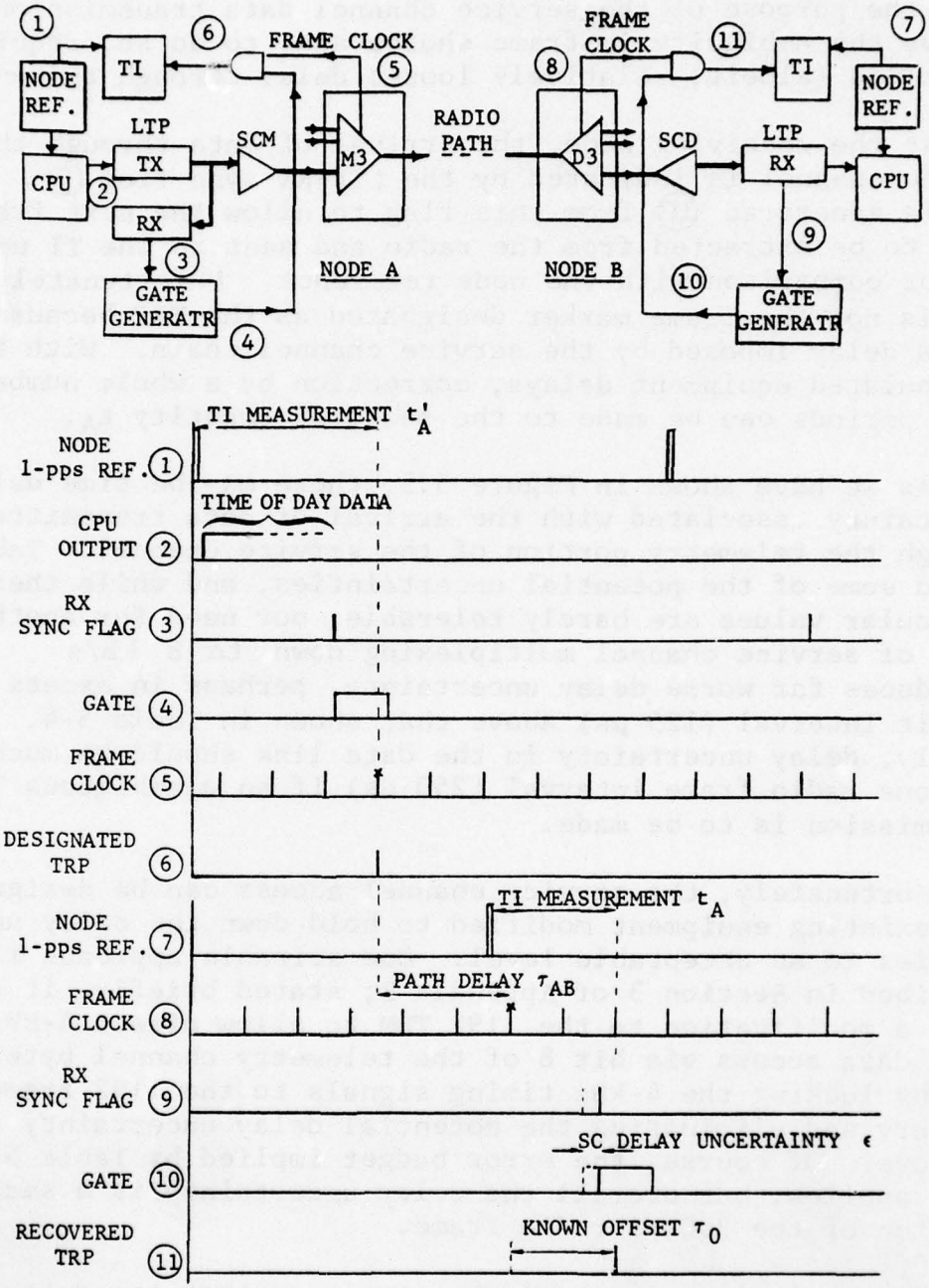


Figure 5.5 DCS Timing Transfer: Option B - Radio Sync Pattern with Service Channel Ambiguity Resolution

- When several transmitters are serviced by one TI using a time-shared approach, additional processing must be set up at the transmit end to sequence the invert sync commands and avoid coincident TRP's on different links with the attendant TI measurement difficulties. The hardware to meet this requirement is embodied in the block diagram pertaining to the next section, Figure 5.5; despite appearances, the additional complexity is not really significant. The transmit CPU, LTP, and SCM hardware are implicitly required by option A in any case, since they provide the data link interface for internode exchange of measured time parameters and other data, inluding time of day.

5.1.2.2 Radio Sync Pattern with Service Channel Ambiguity Resolution (Option B)

Although it is probably not glaringly obvious to the reader, the time transfer systems described in Figures 5.4 and 5.5 are, in fact, very similar. The principal differences are those of emphasis in the block diagram presentations. In Figure 5.4, the data link interfaces have been suppressed but, as a matter of necessity, the LTP and CPU components shown in Figure 5.5 must also be present in the former system. Hence, although option B seems to entail more hardware than option A, the reverse is true. Option A requires the frame sync detector hardware not required by option B.

The detailed operation of the scheme depicted in Figure 5.5 is as follows. Immediately after the transmit node 1-pps pulse occurs ①, the CPU is interrupted and initiates the transmission of a data packet over the service channel ②. The LTP-TX generates a sync word as a header to the packet, and this word will be recognized by any LTP-RX units which receive the data string. Upon recognition, a sync flag is raised. The loopback operation to LTP-RX at node A therefore provides a flag at the same position in the data string as will be present at the receiving end (node B). This mechanism simply removes a large fixed delay component from consideration. When the sync flag ③ is raised, the next frame clock pulse from the radio is gated to the counter ⑥, and a measurement of its event time relative to the node reference is completed (i.e., t_A'). Thus, we have one particular frame boundary representing the TRP (marked with a cross in our conceptual diagram ⑤). The difference from option A is that this event is no longer uniquely

16-bit code match, it then puts out a pulse ⑦ for TI measurement relative to the local 1-pps reference ⑤ (denoted t_A). Note that the reference sync code of interest is marked with a cross in the timing diagram, and it is delayed by τ_{AB} due to passage through the radios and propagation medium. The composite time interval $(t_A - t_A')$ is then made available at both nodes by exchanging t_A and t_A' as well as the time of day in hours, minutes, and seconds over the service channel. In this configuration, service channel timing and delays are not critical and can be ignored.

We now highlight some of the advantages and disadvantages of this approach.

Advantages:

- Conceptual simplicity. This option is easy to comprehend because of the simple structure involved.
- Resolution. The full bandwidth of the radio is being utilized, since the frame clock is derived directly from the high-speed transmit/receive clocks; i.e., there are no synthesizer ambiguities or delay uncertainties to contend with (see Appendix A).
- There are no timing constraints on the service channel.

Disadvantages:

- Interference with normal frame sync performance. The arrival of an inverted frame sync pattern is counted as an error in the DEMUX frame sync loss up/down counter. However, it only slightly dilutes the synchronization performance, and the inverted code alone will never cause loss of sync. The 1:4000 ratio of inverted frame codes to total frames should ensure an insignificant overall effect.
- The MUX must be examined in detail to ascertain how difficult the inversion implementation would be. Any alternative encoding scheme can be considered but would probably be even more costly to implement.

the digital radio synthesizers and FIFO's would have to be subjected to stringent specifications (see Appendix A).

The above statements might seem puzzling to the reader following as they do our optimism in the preceding section regarding fairly straightforward modifications to the 1192 TDM. The difference is that, in option C, we must attempt to remove all delay uncertainties in the service channel chain down to a net level of about 10 ns. We, therefore, need to introduce most of the design requirements specified and discussed in Appendices A and B.

The delay budget given in Table 5-4 introduces the reader to the difficulty of such an undertaking. Furthermore, if submultiplexing is implemented to segment the 50-kb/s telemetry channel, as shown in Figure 5.6, additional delays not listed in Table 5-4 must be considered.

Option C does have the redeeming advantage of conceptual simplicity. In Figure 5.6, the CPU initiates a transmission in response to the 1-pps clock pulse and, after a short delay, the LTP transmit flag is raised (alternatively, a loop connection to an RX unit could be included, as in Figure 5.5). At the receiving end, node B, the data packets arrival is signaled by the RX sync flag. These flags are measured for arrival relative to the 1-pps local standard at the respective nodes. The data packet would include the previous measurement values and time of day.

The delay components, marked on the timing diagram of Figure 5.6, are, of course, the bane of this technique; total delay in each link direction must be matched to the desired clock setting accuracy; alternatively, biases, if they exist, must be known to the same precision.

The advantages and disadvantages for option C should be obvious, and will not be labored. For the reader who desires a better understanding of the delay mechanisms introducing uncertainty, a thorough reading of Appendices A and B is recommended.

5.1.3 Data Buffer Placement

We are concerned here with the buffering capability which must be provided in the DCS timing subsystem. The buffers in question are primarily of use for protection against timing transients which may occur in a system with coordinated clocks or, more likely, to take up the differences in data transmitted between nodes when independent clocks are set up in the network.

The size of such a buffer, often called an elastic store or a first-in first-out buffer (FIFO), is determined by the data rate, expected worst-case frequency offset, and required time before over- or underflow starting with the buffer half-full. This can be expressed as

$$B = 4 R E_f T_R$$

where

B is the buffer capacity in bits (equal to twice the difference in number of input and output bits before over- or underflow starting from half-full)

R is the data rate (bits/second)

E_f is the fractional frequency error of one clock

T_R is the time required before reset

The factor of 4 results from assuming that the two clocks each have errors of E_f of opposite sense and from the fact that only half the buffer capacity is available before over- or underflow if started half-full. The table below shows the minimum buffer size required for $E_f = 10^{-11}$ and $T_R = 1200$ hours* for a number of data rates. (Size is rounded upward to nearest integer.)

Data Rate	Buffer Size Required (bits)
8 kb/s	2
16	3
32	6
64	12
192	34
1.544 Mb/s	277
3.232	559
6.464	1117
9.696	1676
12.928	2234

Buffers can be placed at a number of possible locations in the demultiplexer hierarchy. The choice of location depends

*Equivalent to 50 days continuous operation.

upon a number of considerations, one of which is the topology of the network. For example, if a drop-and-insert capability is required at the T1 level, where one or more level-2 demultiplexer output ports feed level-2 multiplexers for retransmission, while data from other ports are further demultiplexed, there must be a buffer either between the radio and the level-2 demultiplexer or buffers at the T1 level.

To avoid confusion in the discussion of other placement issues presented below, we should first define some terms. Level-2 buffering will refer to buffers placed in the MBS lines between the level-2 MUX's or DEMUX's and the radios. Level-1 buffering will imply buffers placed in all lines on the output side of the level-2 DEMUX or, equivalently, the input side of level-2 MUX's, i.e., between level-1 and level-2 equipment. Buffers at lower levels, e.g., in 16-kb/s lines, will simply be identified in terms of their data rates.

A few general comments about cost will help to orient the reader before more specific recommendations are put forward. Present technology allows buffers for level 2 (up to 13 Mb/s) to be built at only a marginally higher cost than buffers for level 1 or below. Above about 1K bits of storage there is virtually no cost differential and, more important, the incremental cost of adding storage beyond this value is quite small compared with the initial cost of control circuitry.

Given that there are no significant cost constraints, we can therefore explore other issues that may influence the placement decision:

- When buffering is carried out at one of the lower levels, all upstream equipment must be clocked from the recovered modem clock which will exhibit jitter and other medium effects (e.g., frequency offset for satellites). To avoid the presence of this jitter in equipment, it must be placed on the downstream side of the buffer.
- At some stations, switching and combining of data streams from several remote sources must be achieved. This can only be done with synchronously clocked data, implying that the data must have already passed through a buffer by the time it is presented for combining. For example, if digroups (1.544 Mb/s) with different geographical origins are to be combined at a level-2 MUX, they must have been subjected to buffering either at level 2 or at level 1.

- At the output of the radio, we have an opportunity to buffer data in such a way that resets correspond to the deletion or insertion of an integer number of level-1 and level-2 frames. We dismiss the possibility of extending this concept to lower level submultiplexers because of the increased storage requirements. However, the possible avoidance of level-1/level-2 TDM resynchronization is in itself appealing enough, particularly when a major portion of the traffic is voice. In terms of the effects on voice channels, the objective is to reduce the resetting operation to the loss of signal for a few milliseconds or less.

- To successfully attempt such a strategy, it is necessary to know the TDM frame format, and to examine the consequences of implementing multiple frame resets with buffers at different levels, e.g., at level 2. A jump by a whole level-2 TDM frame may not throw that DEMUX out-of-sync, but still not safeguard the level-1 DEMUX's. Alternatively, if the buffers are at level 1, such resets do not affect the level-2 DEMUX's in any way.

- The level-2 TDM rate specifications allow for input port strapping (i.e., output ports at the DEMUX); hence, the buffer design must accommodate various rates if it is to be used at level 1. This is rather awkward when one considers that the total number of bits of storage required at a level-2 DEMUX output is invariant regardless of the division of the total MBS bit rate into various port rates, strapped or otherwise. Obviously, the designer is forced to develop an 8-port flexible buffer unit with programmable rate structure (and movable storage boundaries), or he must design for the worst-case rate (i.e., maximum) and develop eight identical buffers to satisfy the worst-case number of ports. These design issues give added weight to the selection of a level-2 buffer design.

- Other considerations mainly involve cost and reliability of a few large fast buffers vs. a larger number of smaller slower buffers of comparable total capacity. A large buffer is probably cheaper than a number of smaller ones of similar total capacity, unless reliability requirements (MTBF is probably a function of size) or the high data rate

required dictate a more expensive approach (either a different technology or more expensive components). The consequences of a failure of a large buffer are more serious than those of a failure in one of a number of smaller buffers which might be used instead.

It can be concluded from the above discussion that placement of the buffers between the radio demultiplexer and the level-2 demultiplexer is favored. The only disadvantage of its insertion at that level is one of reliability.

5.2 General Synchronization and Clock Control Requirements

This section reviews the nature of the node subsystem design problem and leads to an elaboration of features which must be built into the timing subsystems. The equipment shown in block diagram form in Figure 5.7 is representative of the components needed for one (full duplex) link termination at a node. For most situations, several links will be terminated, in which case all of the transmission equipment shown above the dotted line would be replicated and interfaced to the common timing subsystem grouped below the line.

5.2.1 General Principles of Clock Information Exchange

To fully understand the operational characteristics of the node timing subsystem shown in Figure 5.7, one needs to visualize the internode timing and data relationships depicted in Figure 5.8. Here we have shown four interconnected nodes. Node B has been amplified to indicate the basic functions performed there and at all other nodes. On each connecting link, there is the transfer of timing events (via radio frame sync) and control data. In Figure 5.8 this has been indicated conceptually by means of an arrow (for the timing event) attached to a packet of data (enclosing such things as node status, time measurements, and time of day). Although we have emphasized the use of these time reference information packets (TRIP's) on the link connecting node A and node B, they would of course be present on <u>all</u> links in general. Typically, these TRIP's would emanate from every node at a 1-per-second rate, and the time-of-arrival resolution for each would be on the order of 10 ns. The data rate for packet parameters would be roughly 4 kb/s via the service channel.

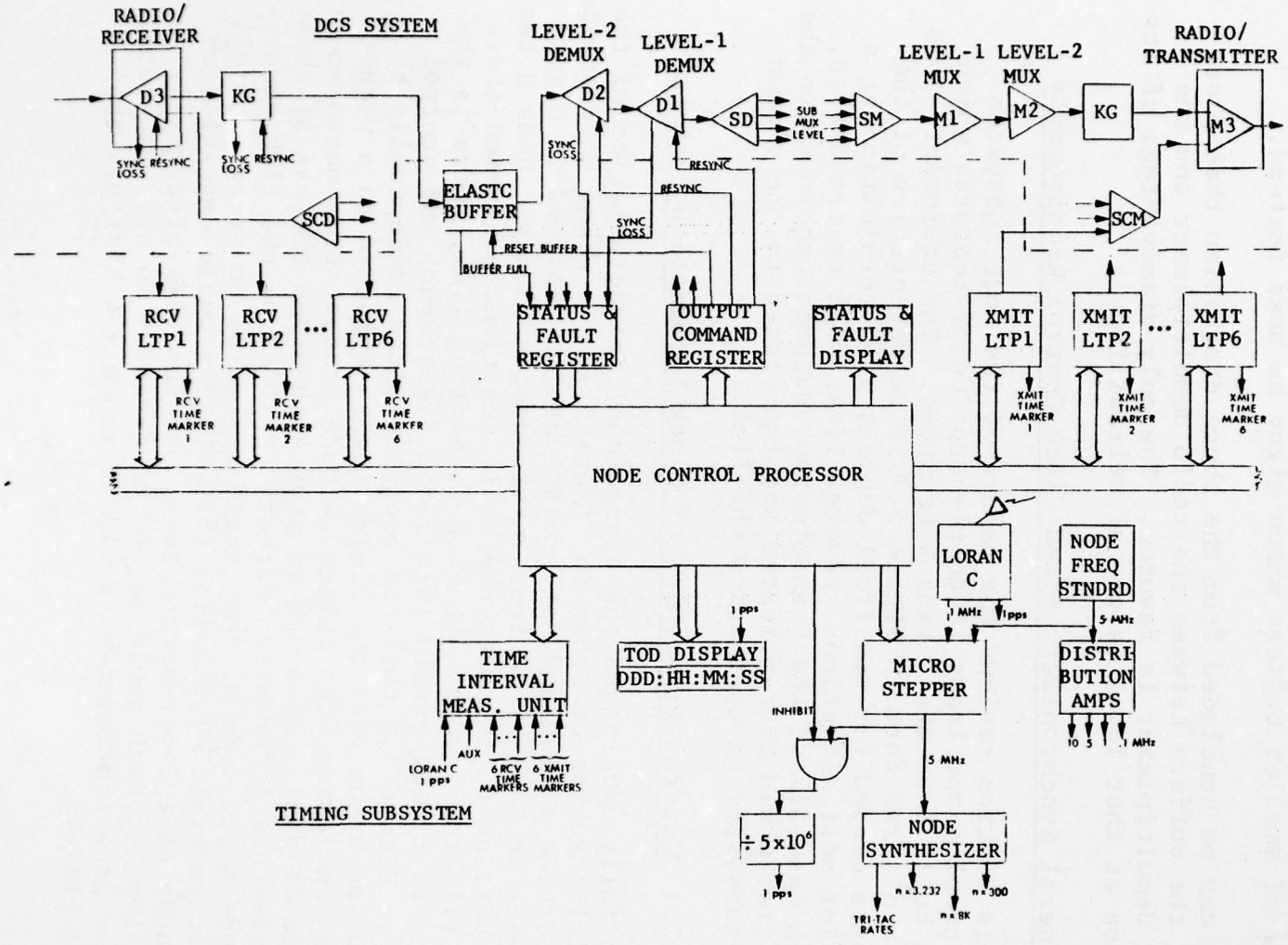


Figure 5.7 Block Diagram of Timing Subsystem showing Interfaces with Link Multiplexers

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SYSTEM TIMING AND SYNCHRONIZATION.(U)
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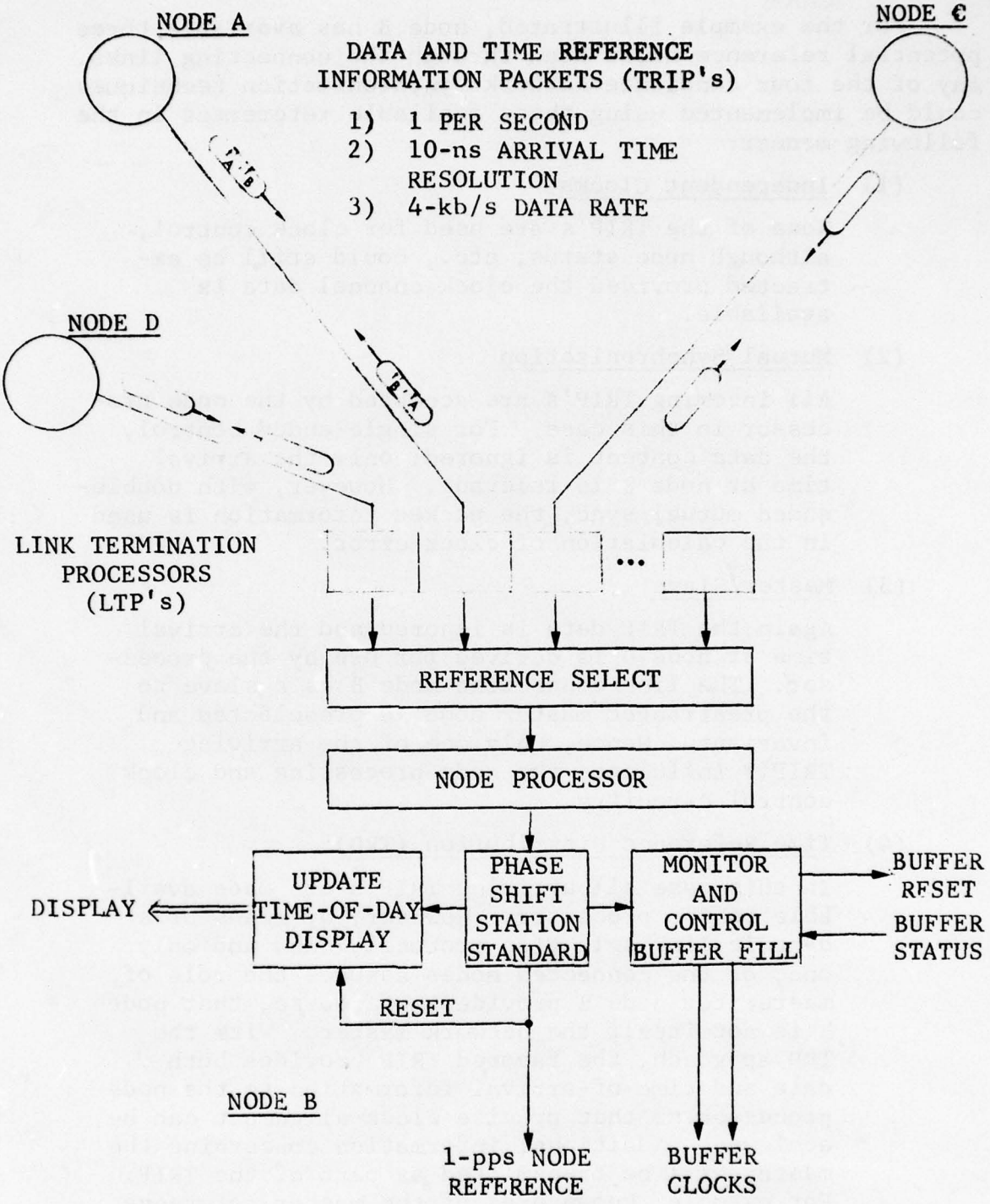


Figure 5.8 Simplified View of Link Termination and Node Processing Arrangements

For the example illustrated, node B has available three potential reference nodes seen through the connecting links. Any of the four candidate network synchronization techniques could be implemented using these available references in the following manner:

(1) Independent Clocks

None of the TRIP's are used for clock control, although node status, etc., could still be extracted provided the clock channel data is available.

(2) Mutual Synchronization

All incoming TRIP's are accepted by the node processor in this case. For single-ended control, the data content is ignored; only the arrival time at node B is relevant. However, with double-ended mutual sync, the packet information is used in the calculation of clock error.

(3) Master/Slave

Again the TRIP data is ignored and the arrival time at node B is derived for use by the processor. The link connecting node B as a slave to the prearranged master node is preselected and invariant. Hence, only one of the arriving TRIP's influences the node processing and clock control circuitry.

(4) Time Reference Distribution (TRD)

In this case all arriving TRIP's are made available to the processor. However, by means of a dynamic link selection protocol, one, and only one, of the connected nodes assumes the role of master for node B provided, of course, that node B is not itself the network master. With the TRD approach, the favored TRIP provides both data and time-of-arrival information to the node processor so that precise clock alignment can be achieved. Additional information concerning the master will be transmitted as part of the TRIP. For example, known bias of the master reference relative to some higher-order reference can be used by the slave node to compensate for this offset in the correction of its own clock [5.3].

Implementation of these different techniques within this data exchange framework varies only in the way references are selected or combined. The processor software differences are not too significant and, in each case, the result is a clock phase or frequency shift command to alter the node reference 1-pps phasing. Similarly, the phase control indirectly affects the buffer clocks causing the rate of buffer fill or depletion to change. With independent clock operation, the phase shift control is zeroed.

The ultimate node reference signal is the 1 pps derived from the phase-shifted frequency standard. At the risk of being repetitious, the reader is reminded that the network time synchronization objective is the alignment of all such 1-pps references throughout the system. In master/slave and mutual sync approaches, the relative variation of the 1 pps after buffer reset is the important consideration. That is, absolute phase or time relationships are unimportant throughout the network, but accumulated phase variations in the 1-pps signal are indicative of buffer fullness variations, and controlling one will control the other if the station clock frequencies all originate from the corrected station standard.

The data required in the clock control loop processor will depend on the synchronization technique selected, but, as a general rule, it will consist of time measurements from the other end of the link (t'_A and t_B) as well as time measurements made locally (t_A and t'_B). For double-ended time reference distribution, the block error calculation is therefore (see Figure 5.9):

$$u = \frac{1}{2}\left[(t'_A + t_B) - (t'_B + t_A)\right]$$

$$= \text{Node Ref. A - Node Ref. B.} \qquad (5.1)$$

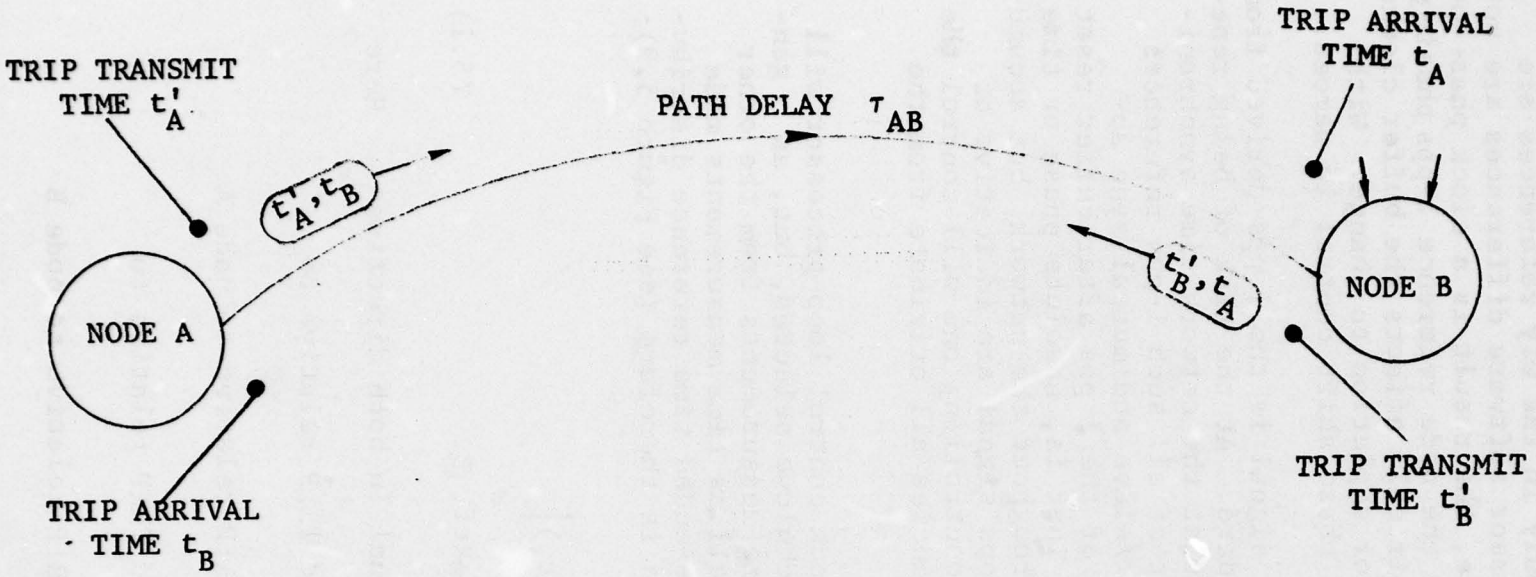
(provided the path delays are equal in both directions). Here

t'_A = node A transmitted TRIP relative to node A reference

t_B = received node B TRIP relative to node A reference

t'_B = node B transmitted TRIP relative to node B reference

t_A = received node A TRIP relative to node B reference



TRIP ARRIVAL TIME AT B (RELATIVE TO A) = $t'_A - t_A + \tau_{AB}$

TRIP ARRIVAL TIME AT A (RELATIVE TO B) = $t'_B - t_B + \tau_{BA}$

CLOCK ERROR (EQUAL DELAYS) $u = \frac{1}{2}(t'_A - t_A - t'_B + t_B)$

= CLOCK A - CLOCK B (START TO STOP TIME)

PATH DELAY $\tau_{AB} = \frac{1}{2}\left[(t_A + t_B) - (t'_A + t'_B)\right]$ ASSUMING $\tau_{AB} = \tau_{BA}$

Figure 5.9 Clock Error and Path Delay Calculations for Time Reference Distribution

All parameters listed are to be interpreted as elapsed time measurements. Similarly, for a single-ended time reference transfer, a nominal path delay must be known. If this quantity is denoted τ_{AB}, the measured quantities t'_A and t_A can then be used to calculate clock offset:

$$u = t'_A - t_A + \tau_{AB}$$

$$= \text{Node A clock} - \text{Node B clock} \qquad (5.2)$$

The same principles are used in the master/slave and mutual sync techniques except that only relative variations in the arrival time of the incoming TRP's need be considered. Hence, with master slave:

$$u = -(t_A - t_{A0}) \qquad (5.3)$$

where t_{A0} is the value of t_A when the system is reset (i.e., buffers are set to half-full). Then, for single-ended mutual synchronization, we need:

$$u = \sum u_i$$

$$= \sum_i k_i (t_i - t_{i0}) \qquad (5.4)$$

where $u_i = k_i(t_i - t_{i0})$ is the error for the i^{th} terminated link. That is,

$t_i = t_A, t_B, t_C$, etc.

k_i = gain constant for each

t_{i0} = initial value of t_i at reset

In other words, it is the relative variation of TRIP's that concerns us; for example, $t_A - t_{A0}$. Note that the TRIP transmit times t'_A, t'_B, etc., are not of interest for a single-ended scheme (computed clock errors of the form (5.1) are used to generalize Eq. (5.4) for double-ended mutual sync).

At the originating node, e.g., node A, the TRIP (and frame bits) are basically locked to the node A 1-pps reference, although their phase relationship will be arbitrary and subject to change each time the radio is taken out of service. An event of that nature would, of course, be highly visible at the receive end in any case. Demultiplexers would signal loss-of-sync and the radio would alarm. Use of that particular link as a reference would therefore be inhibited by the node processors until such time as the link was available again, and then the corresponding buffer would be reinitialized and a new value of t_{i0} established (for the i^{th} link only).

It can be seen that there are many similarities between the four candidate synchronization techniques from the point of view of signal processing. To simplify the presentation in subsequent sections, we will orient our discussion toward the time reference distribution processing requirements, since the other three can be satisfied from within the TRD framework.

A closing comment on timing jitter and measurement noise is also relevant here. The clock error computed in Eq. (5.1), for example, is ideal in the sense that it assumes equal path delays in opposite link directions. This is almost never true for TROPO links on an instantaneous basis (see Section 4.4.1). While the path differential does tend to average out over several minutes, its variability does influence the clock control servo design in certain ways.

5.2.2 Operational Modes

We are mainly concerned here with the status and functional behavior of the clock control loop in different operational circumstances. This contrasts with the synchronization technique considerations highlighted in Section 5.2.1.

Four principal modes of operation can be defined:

(1) Startup. When the network is first initialized for time synchronization of clocks, a special step-by-step startup phase will probably be required (similarly, for addition of new nodes to the network). For two nodes, A and B, we would classify operation as "startup" if the difference between the node clocks is in excess of 5 μs.

(2) Acquisition. This category applies when the clock errors are large enough so that normal control loop servo design principles would not give fast enough convergence speed, and yet the more disruptive "startup" response is neither necessary nor desirable. In terms of clock error between the reference and the slave clocks, the dividing line has been set at 5 μs for a maximum error (beyond which the startup mode is entered) and 60 ns as the smallest error. For errors less than this value, the tracking mode is entered.

(3) Tracking. This is the normal mode of operation, and involves use of standard servo design methods to keep the steady-state clock phase close to the selected reference.

(4) Coast Mode. This applies only when no suitable reference is available and arrangements must be made to extrapolate future clock controls from the past history.

The interaction between these operational modes is shown as a logical flowchart in Figure 5.10. The startup phase can be completed in a matter of seconds if the master node is stable; then the acquisition phase begins and could take up to 50 seconds to complete. Finally, there will be a small transient associated with entry into the tracking mode, the duration of which depends on the selected loop constants.

5.3 Analysis of the Clock Control Loop

This section concentrates on design issues surrounding the clock control portion of the subsystem. In particular, we are concerned with the time lock control loop, including phase shifters, digital update algorithms, time measurement, and clock error computation.

5.3.1 General Structure of the Loop

The clock control components are presented in block diagram form in Figure 5.11. It is shown as a digital system; the low bandwidths of interest here rule out the possibility of an analog implementation because of drift and offset problems that would arise.

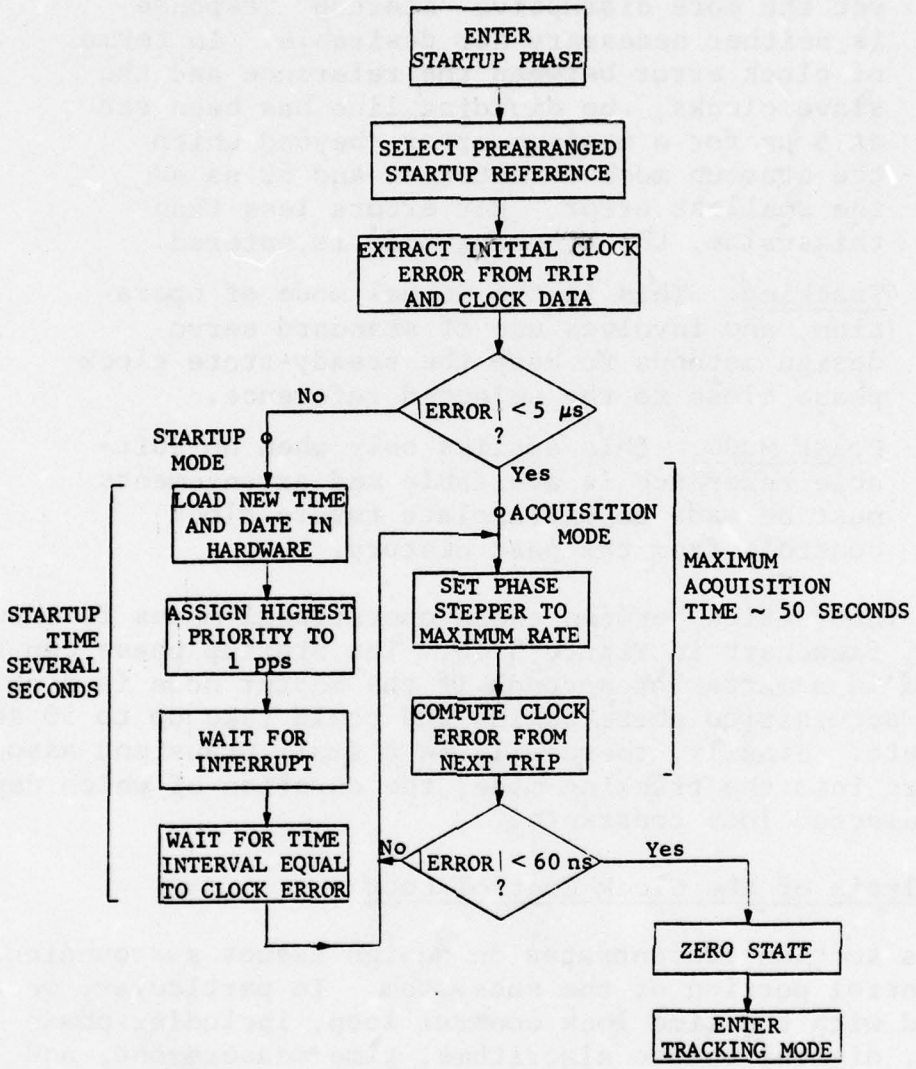


Figure 5.10 Logical Progression through Operational Modes

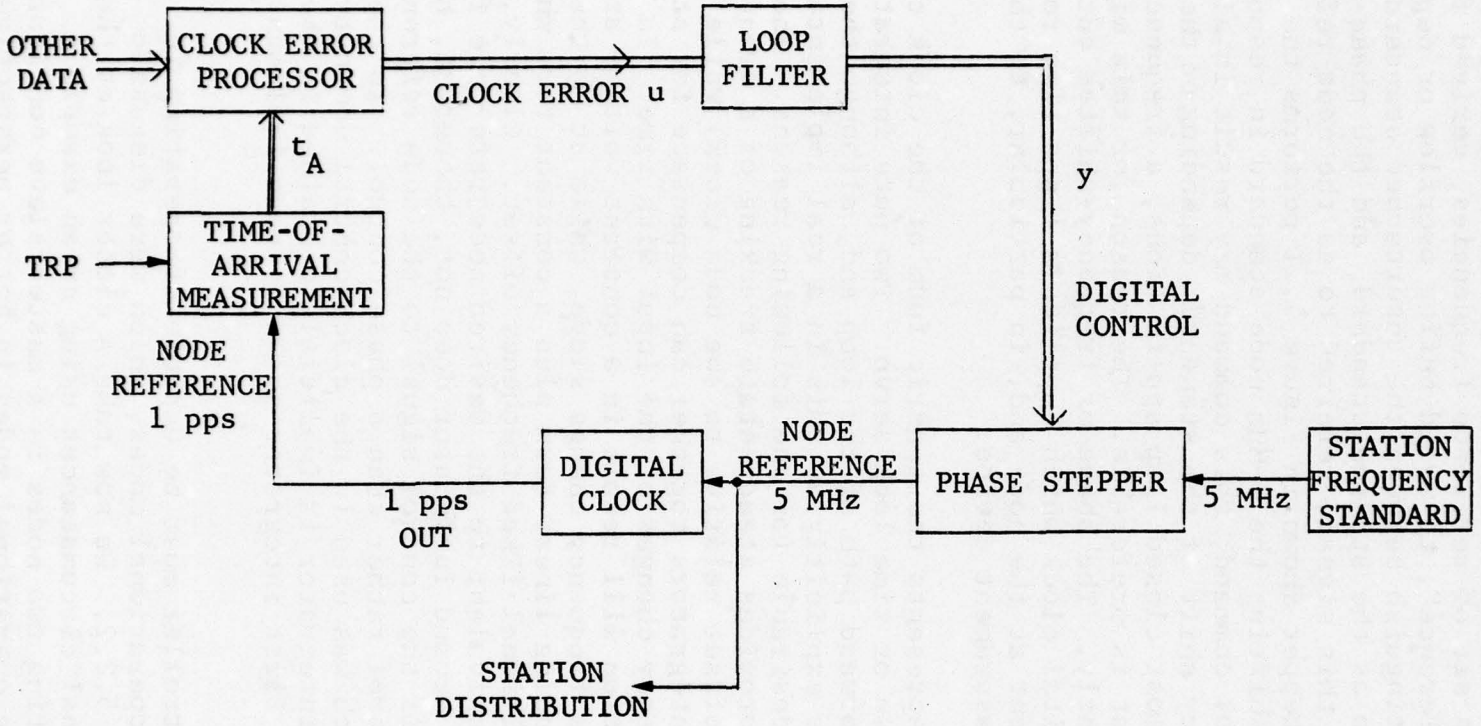


Figure 5.11 Basic Time Reference Control Loop

The fundamental function performed by the control loop is the generation of a set of reference frequencies, derived from the 5-MHz "node reference", to avoid buffer overflow or depletion. We will distinguish between the unperturbed standard output, referred to as the station standard, and the phase-shifted version of this signal, referred to as the node reference. The phase stepper shown in Figure 5.11 performs the function of phase shifting the 5-MHz node standard in response to a digital control command; this command may result in either a phase or frequency shift of the standard, depending on the mode setting; but, for most closed loop applications, a frequency shift command format is preferable. The reason for this will be explained subsequently. The phase of frequency-shifted output then goes to a digital clock which supplies a 1-pps time reference to all equipment at the node and, in particular, to the time-of-arrival measurement device.

Figure 5.12 represents the generic form of the clock control loop as a phase or time lock servo. Two pure integrators are shown in the forward path of the loop and, although they may not appear quite as explicitly as this in a real implementation, their presence is desirable for the following reasons. The second integrator provides steady-state tracking of a frequency offset reference (offset relative to the node clock) while the first and second integrators together can compensate for steady-state linear frequency changes of the input with time. In fact, steady-state operation will result in a constant voltage at ② proportional to the frequency change slope, while at ③ there will be a corresponding linear term plus a constant term which provide for an additional fixed frequency offset. Clearly, the voltage at ③ is equivalent to the desired node reference frequency offset; the second integrator does not, therefore, have to be implemented if the control signal to the node reference is a <u>frequency</u> control rather than a phase control. In the former choice, which was used in the clock control demonstrations, the second integrator is implicitly contained in the phase stepper; the first integrator shown is then implemented in software.

The clock controller must be capable of operating in several different operational modes, which were discussed briefly in Section 5.2.2. We now take a closer look at these different operational circumstances using as an example a single link connecting two nodes in a master/slave configuration. To place the operational modes in better perspective, we treat them in the order in which they would occur for a link that is initially out-of-sync.

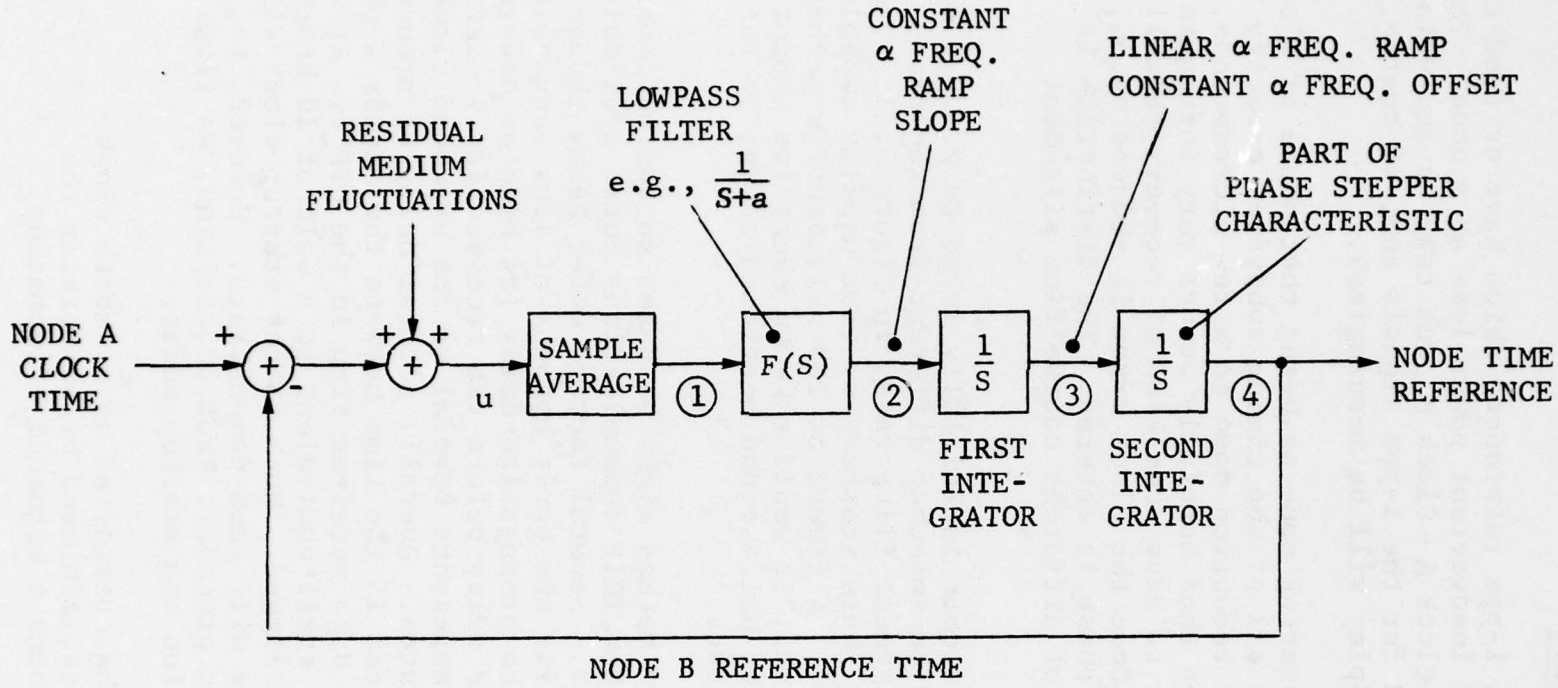


Figure 5.12 Generic Form of Clock Control Loop

5.3.2 Startup Phase

Consider two node 1-pps references which have drifted apart perhaps as a result of inadvertent power loss at a node. The relative clock error, Clock A - Clock B, can take on any value between 0 and 1 second for the 1-pps signals and, of course, the digital output display will be meaningless.

We refer to the startup mode as being that phase of clock alignment during which all of the timing subsystem capacity is devoted to clock error reduction down to a few microseconds, i.e., it is a situation that hopefully occurs very infrequently; however, it is prudent to have some kind of recovery capability in such a situation. Once the clock error is reduced below, say, 5 μs, the acquisition phase is entered. The distinction is primarily as a result of different coarse/fine alignment implementation.

If the clock difference is initially large (e.g., 0.5 s), the approach used must be somewhat different from the phase stepping kind of arrangement illustrated in Figure 5.11. The reason is that precise phase steppers are not usually capable of fast stepping action. A figure of 100 ns/second is perhaps typical and, at that rate, it would take an excessive amount of time to step through the half-second mentioned above; in fact, on the order of 1000 hours.

A more appropriate method might be based on the uncompensated arrival time of the TRIP communications burst available via the service channel. Several factors enter here, though: the delay in transmitting the burst because of link sequencing at the transmit end, the propagation delay (as high as several ms), and the 8-bit baud delay before the receive flag is set. This latter quantity represents several ms for expected clock control channel data rates. Overall, a total delay of around 5 ms could be experienced in the time between the master 1 pps and the raising of the data received flag in the LTP's. At 100 ns/second, this is still equivalent to a wait of 10 hours before the clocks are aligned. Much faster startup clock alignment is possible, as we will soon demonstrate. However, to distinguish the startup procedure from acquisition, we first delineate the acquisition and startup modes.

- Acquisition will be considered as a smooth clock realignment process, achieved by exercising the phase stepper through a sequence of commands.

All outgoing radio and TDM clocks will be slewed, and all buffers at the slave node will empty or fill by the amount of the realignment.

- The startup alignment phase would be carried out by stepping the node 1-pps reference only once, with a resulting alignment accuracy of around 5 μs. This operation will not affect the buffers or output radio clocks in any way.

It should be understood that startup operation would be used infrequently and by design, so that abrupt time-of-day changes may be anticipated throughout the network. Moreover, the buffers are not affected, so that it represents a satisfactory method of passing from independent clock network operation to full synchronization.

One form of implementation is shown as a block diagram in Figure 5.13. The node processor is required to compute the clock error based on available time-of-arrival measurement data, and to use the result to correct the 1-pps node reference. The local 1-pps signal is made available to the processor at an interrupt request line for internal time-of-day updating. After receipt of the request for startup, a clock delay routine is entered, and a wait loop executed to delay the local 1 pps by the amount of the clock error. During this programmed delay, the 5-MHz input signal to the 1-pps divide chain is inhibited, and the next 1-pps output will have been shifted by some large number of 5-MHz clock periods to fairly close alignment with the master clock. The corresponding time/date variables are also loaded into the time/date counter. This information must be obtained from the master node using TRIP's arriving via the service channel.

The alignment of clocks cannot be done exactly by this method since we are dependent on software-generated delays. This shortcoming is of no real consequence since the acquisition algorithms outlined in the next section provide rapid convergence for errors of a few microseconds.

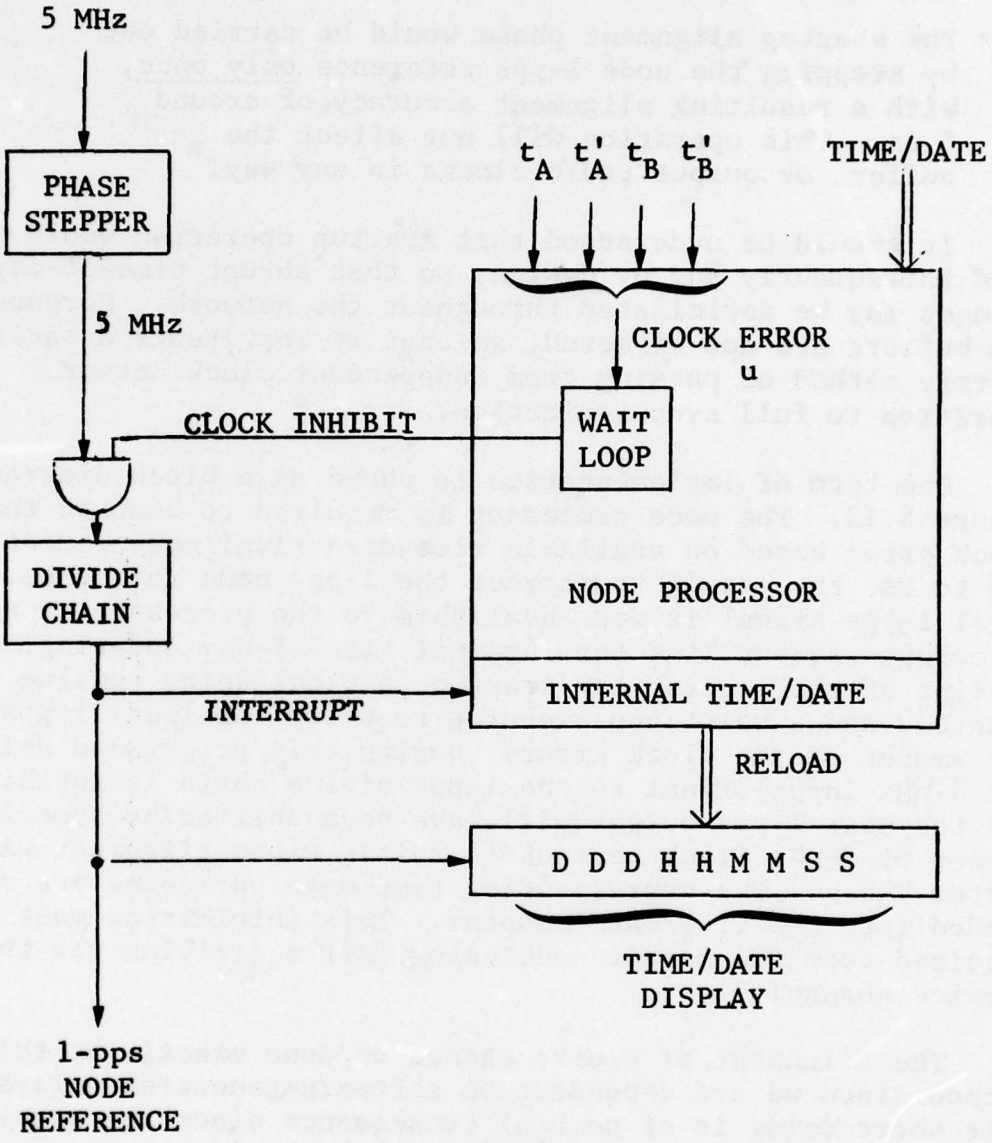


Figure 5.13 Startup Phase Clock/Reference Reset Operation

5.3.3 Acquisition Considerations

The reference to acquisition in this context concerns the strategy used to rapidly reduce any moderate phase or time errors between the master and slave clocks. Once acquisition has been completed, the tracking algorithm is initiated, and normal closed loop servo action proceeds (as described in Section 5.3.4) until such time as the clock phase error becomes excessive and the acquisition mode is again reentered. This might occur when a new time reference is selected, for example, or when a node clock is being brought back into service.

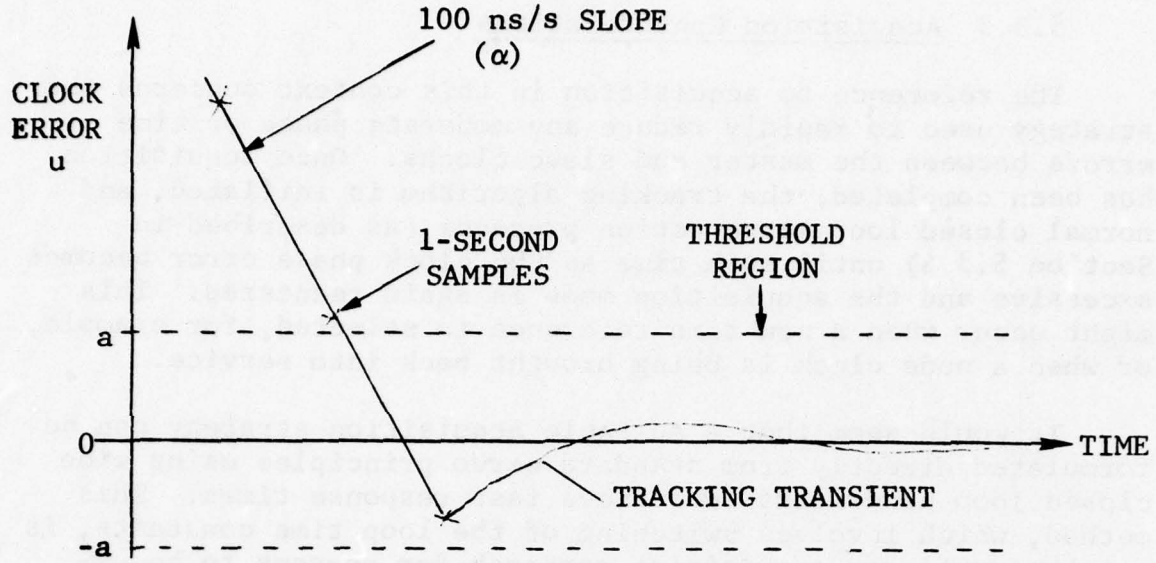
It would seem that a suitable acquisition strategy can be formulated directly from standard servo principles using wide closed loop bandwidths to achieve fast response times. This method, which involves switching of the loop time constants, is not the preferred acquisition approach for reasons to be explained. In summary, we can state the following:

- Switching of loop parameters to give a larger resultant bandwidth does not provide the most rapid reduction of clock error.
- If the switched parameter approach is used, special precautions must be taken to initialize the control loop state at the switching point in order to avoid severe overshoot problems in the tracking mode.
- Coordination between several node clock controllers, all attempting acquisition, is complicated by this approach.

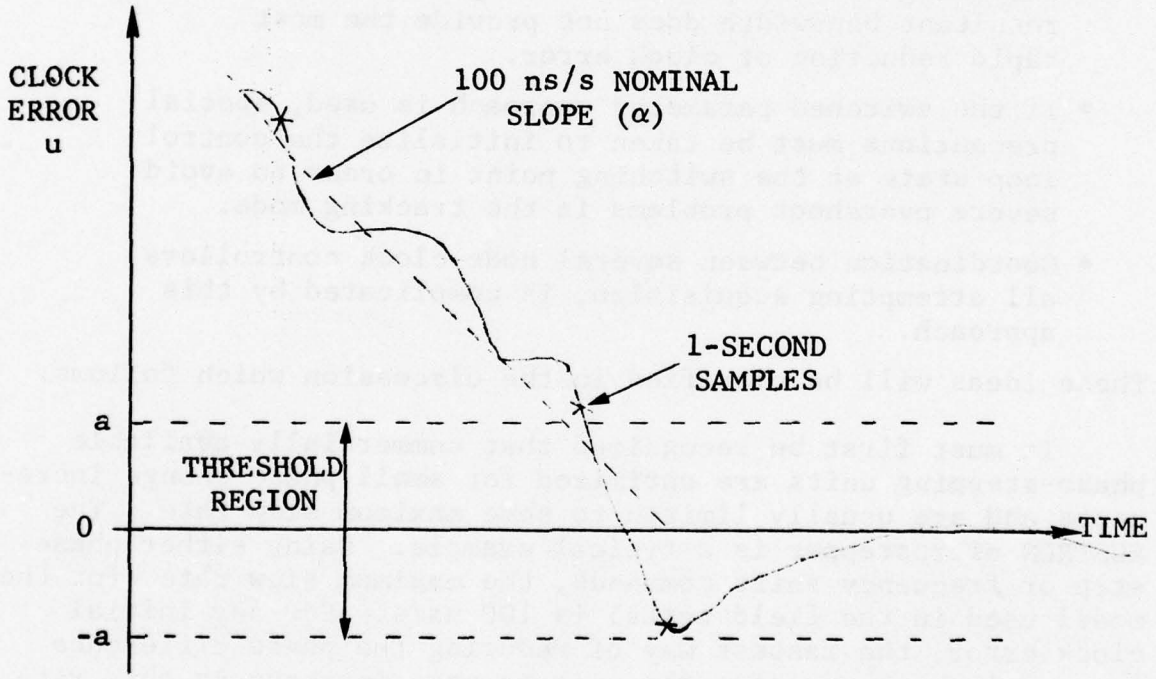
These ideas will be clarified in the discussion which follows.

It must first be recognized that commercially-available phase-stepping units are optimized for small phase change increments and are usually limited to some maximum slew rate. The AUSTRON microstepper is a typical example. Using either phase step or frequency shift commands, the maximum slew rate (for the model used in the field tests) is 100 ns/s. For any initial clock error, the fastest way of reducing the phase difference to zero is by commanding the unit to step in-phase at this rate. This results in a linear reduction in error with time, as shown in Figure 5.14. In (a), the clock error is reduced uniformly at a rate of 100 ns/s until the threshold region is reached. When

$$|u| < a$$



(a) Noise-Free Acquisition Behavior



(b) Acquisition Behavior with Superimposed Medium Jitter

Figure 5.14 Convergence Trajectories for the Acquisition Algorithm

a switch to tracking mode is made. The following observations are important, however:

- The update repetition rate will influence the maximum size of the threshold region, i.e., the maximum value of a. With 1-second measurement updates and a slew rate of 100 ns/s, 2a must be less than 100 ns; otherwise, it is possible for the trajectory to pass completely through the transition region without switching to tracking mode. Of course, the trajectory would reverse direction on the next update, but undesirable hunting behavior would be experienced with excessive error fluctuations.

- The threshold band should be made as narrow as possible to minimize the transient which inevitably occurs in the tracking mode. The ideal clock error at the time of switching is zero, although switching at that point may not, in itself, be enough to completely eliminate the transient because of differences between the master and slave rest frequencies (see Section 5.3.4).

- Noisy measurements or, equivalently, timing jitter compound the difficulties. Obviously, when the system is in the acquisition mode and slewing the clock at 100 ns/s, no averaging of any significance can be carried out on the measured clock error data. With TROPO links, the short-term jitter can be significant (see Section 4) and certainly comparable with otherwise reasonable choices of threshold size. Figure 5.14(b) illustrates this situation. The one-second samples include a random component and the switching to tracking mode takes on a stochastic nature. Clearly, large enough rms jitter will, on occasion, cause a jump between samples larger than the threshold, resulting in a missed switching point. It therefore becomes necessary to choose a threshold value large enough to accommodate the rms jitter component.

The outcome is that convergence time is not easily predicted when jitter is present and discrete time measurements are being processed. The best that can be done is to match

the slew rate, update rate, and threshold selection to the rms jitter. Figure 5.15 illustrates the equivalent combined acquisition/tracking loop block diagram.

Some of the results of test runs carried out in the October series of tests at RADC will now be presented to further demonstrate the advantages of the acquisition algorithm used. The parameters selected were 100 ns/s phase step slew rate, 1-per-second update rate, and a threshold region of $\pm$ 60 ns.

Figures 5.16 and 5.17 are plots of clock error for two different tracking loop time constants. The constants listed on the diagrams will be explained in the next subsection. In both cases, a quartz clock (with virtually zero frequency offset) was being slaved to a cesium standard via a 75-mile LOS link cascade. The servo error was biased off by 1000 ns to avoid measurement difficulties peculiar to the counters available in the region near zero time differential. The clock error was initially in excess of 1 μs, but only the last 400-ns portion of the acquisition trajectory was plotted. The convergence rate is 100 ns/s in this phase, so that rapid reduction in clock error was experienced. The primary difference between these two curves is the shape of the transient which appeared after changeover to the tracking mode. The switching point was roughly the same in each case, presumably because both runs were initialized to the same clock offset.

The plot in Figure 5.18 is of a similar nature except that a 336-mile TROPO loop was the supporting link. Once again, a quartz clock was slaved to a cesium reference, and rapid acquisition was achieved. For this link the medium jitter was not too significant (20 - 30 ns rms) judging by the smoothness of the acquisition trajectory. A certain amount of ripple can be seen in the tracking mode response however, and it would appear that a narrower loop bandwidth would be beneficial in this case.

5.3.4 Steady-State or Tracking Mode Loop Operation

The servo loop block diagrams of Figure 5.19 apply here. The important considerations for steady-state operation are simply the following:

- Noise reduction by selection of suitable loop filter gains and time constants to give a narrow closed loop bandwidth.

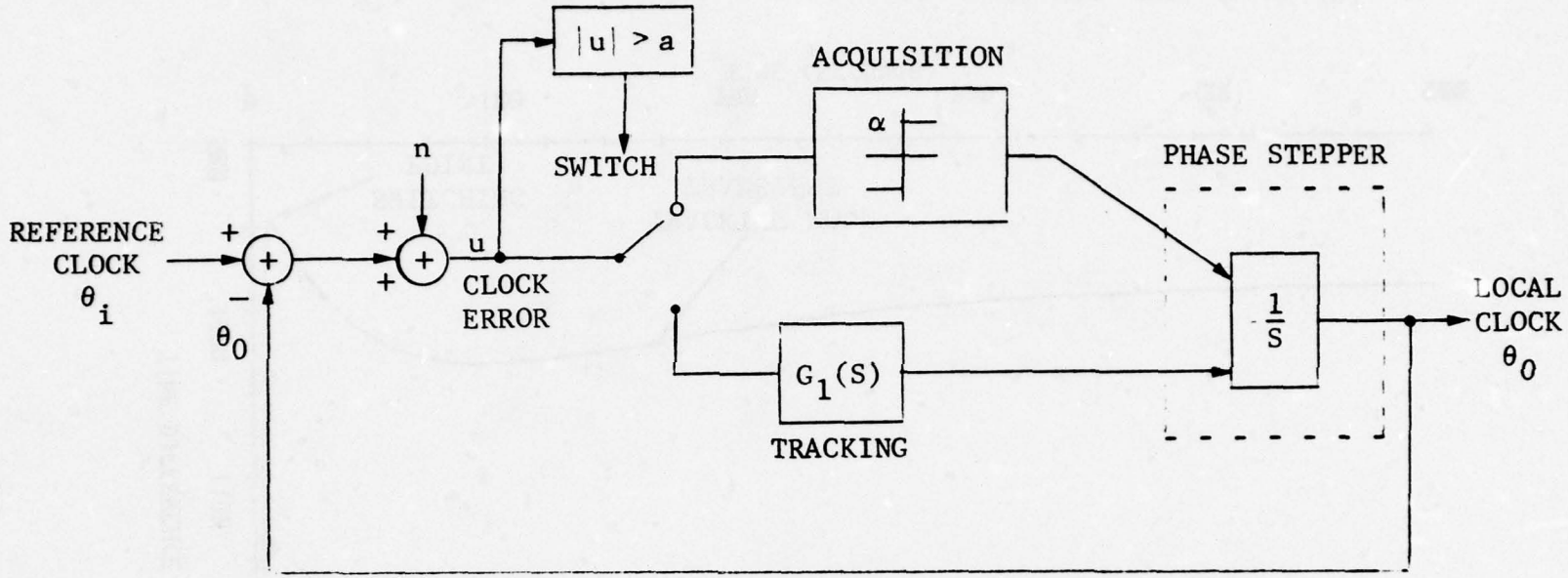


Figure 5.15 Block Diagram of Clock Control Servo with Acquisition Switching

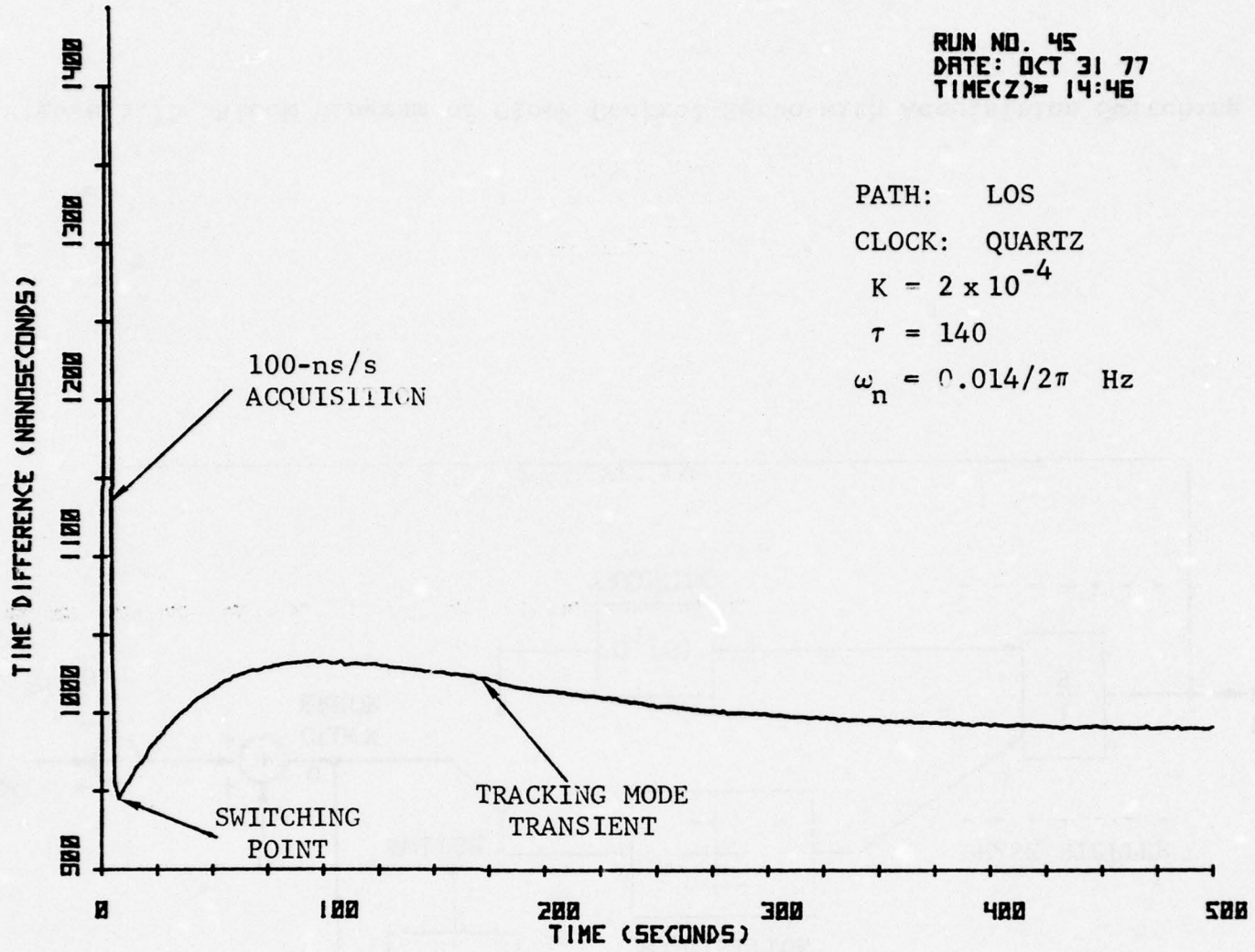


Figure 5.16 Acquisition and Transient Behavior for a 75-Mile LOS Master/Slave Time Transfer Experiment (Closed Loop Bandwidth = 0.014 rad/s)

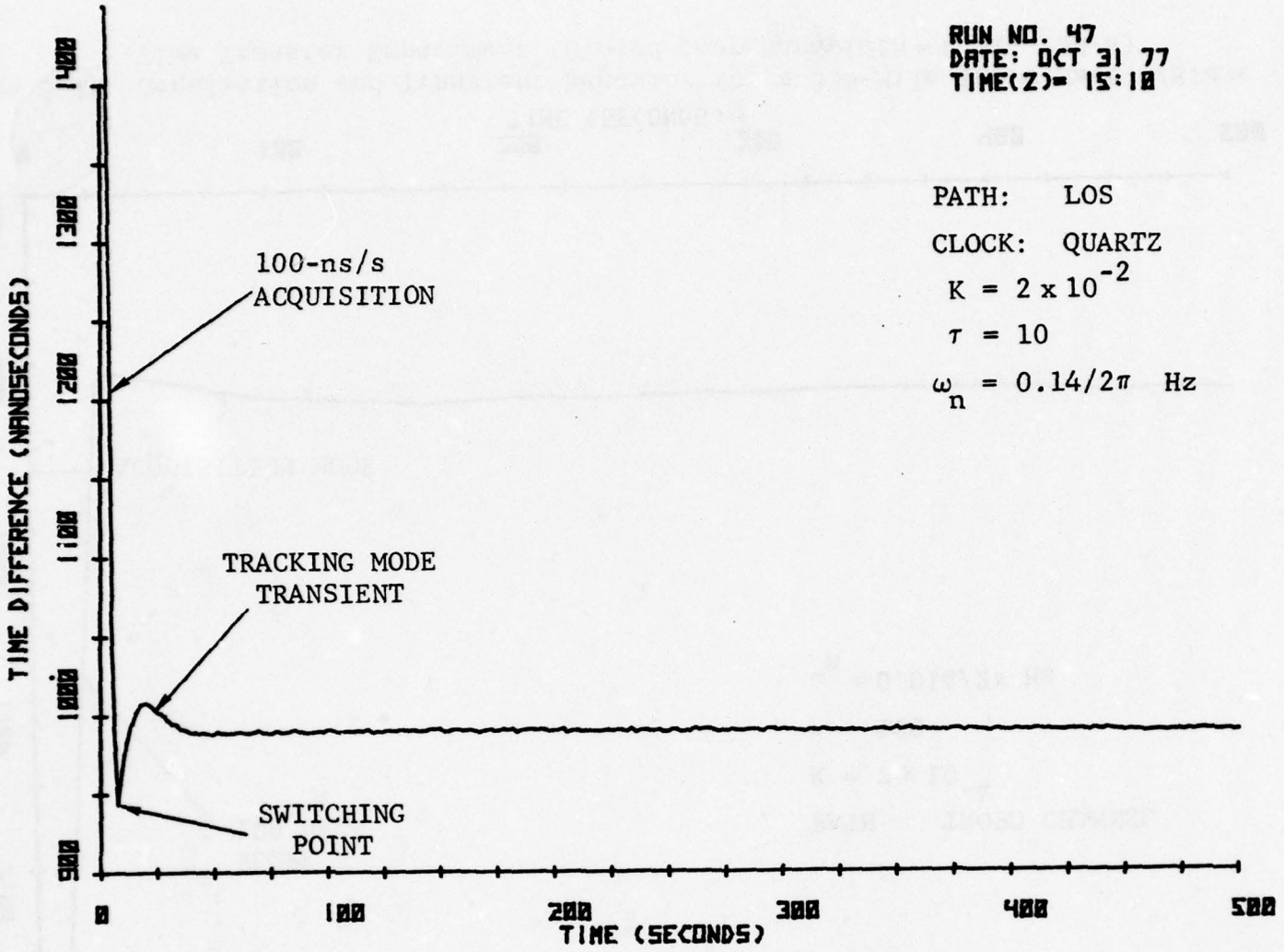


Figure 5.17 Acquisition and Transient Behavior for a 75-Mile LOS Master/Slave Time Transfer Experiment (Closed Loop Bandwidth = 0.14 rad/s)

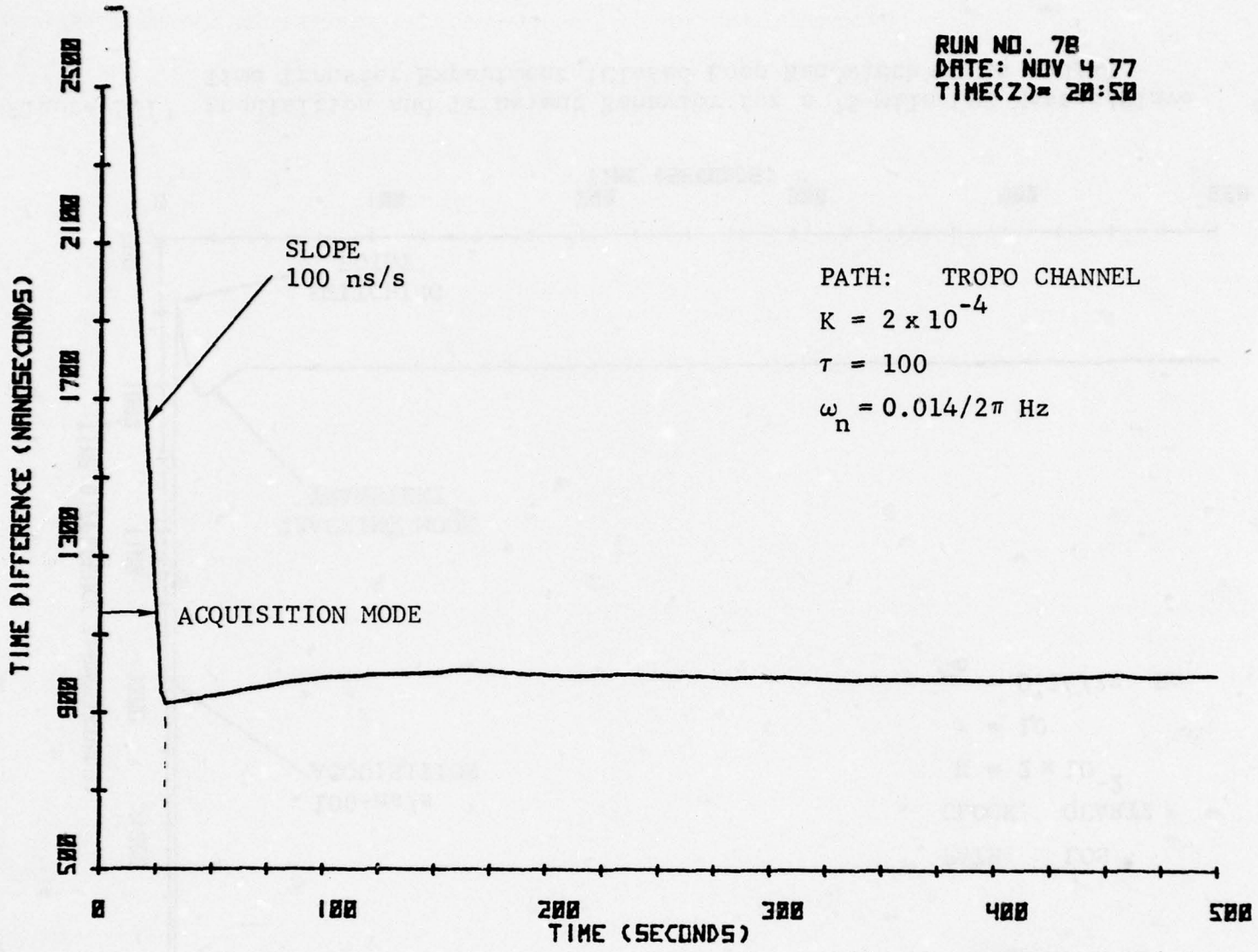


Figure 5.18 Acquisition and Transient Behavior for a 336-Mile TROPO Master/Slave Time Transfer Experiment (Closed Loop Bandwidth = 0.014 rad/s)

- Selection of parameters to optimize rise times and overshoots resulting from minor transient effects.
- Steady-state tracking of fixed frequency offsets and frequency trends relative to the station standard characteristics to allow for an operational switch to the open loop coast mode described in Section 5.3.5.

The last item dictates the number of perfect integrators in the open loop transfer function. For example, it is easily shown that an input reference phase (or time) function θ_i* with the temporal behavior

$$\theta_i = t^n$$

can be tracked by a system with open loop transfer function

$$F(s) = \begin{cases} F'(s)\left(\frac{1}{s}\right)^{n+1} & \text{for zero steady-state error} \\ \text{or} & \\ F'(s)\left(\frac{1}{s}\right)^{n} & \text{for finite steady-state error} \end{cases}$$

Conversely, a local reference with the same open loop phase characteristics can be locked to a quiescent input reference. In the above expressions, F' is defined so that it does not contain any factors of (1/s), i.e., it does not contain a pure integrator. As an example, consider a ramp in frequency which is equivalent to a quadratic phase variation with time,

$$\theta_i = t^2$$

Then the output phase θ_0 follows θ_i only if the open loop transfer function has a factor $(1/s)^2$. Even then, there is a finite steady-state error, but it can be made small by choice of a high open loop gain.

*To avoid confusion of time variables and time functions, the clock characteristics will be represented in terms of their phase variable θ. Thus, θ_i is the phase of a 1-pps periodic event in radians, relative to a hypothetical ideal reference. In practice, of course, one can only measure differences between clocks, e.g., $\theta_i - \theta_0$, where θ_0 is the phase of the slaved node clock.

This situation is germane to the case of quartz crystal oscillators. If the input to the loop is the phase of an atomic clock, and the station standard is a quartz clock, the relative phase characteristic is a ramp as a result of constant frequency offset, and a quadratic as a result of frequency drift in the quartz unit, i.e.,

$$\theta_i - \theta_0 = at + bt^2$$

Generally speaking, it is advisable to have a type-2 servo system (i.e., two integrators) when quartz clocks are to be used in the network. Higher numbers of integrators jeopardize the stability of the loop and usually are not justified.

Fortunately, one of the integrators needed can be obtained from within the phase stepper when it is configured as a frequency stepping device. The second would be implemented in software.

One popular method of avoiding instabilities in the closed loop configuration is to select a first-order loop filter with feed forward around an integrator. In system function terms, this amounts to a loop filter

$$F(s) = K_f\left(\frac{1}{s} + \tau\right) \tag{5.5}$$

where K_f is a gain constant to be selected, and τ is the feed forward gain. The complete open loop transfer function is, therefore,

$$G(s) = K_f\left(\frac{1}{s} + \tau\right)\ \frac{K_v}{s} \tag{5.6}$$

Rearranging (5.6), we have

$$G(s) = K_f K_v (1 + s\tau)\ \left(\frac{1}{s}\right)^2 \tag{5.7}$$

i.e., it will give rise to a type-2 system.

Various other choices are available. However, the above transfer function is well-understood and has been widely used in servo loops. In the clock control tests carried out at RADC,

this characteristic was programmed into the control software and performed well. In particular, it was used to slave a quartz oscillator ($1:10^8$) to a cesium standard, and with the design implemented, any frequency drift was accounted for by the servo loop.

Figure 5.19(b) indicates the component blocks for this control loop. As noted under the block diagram, the closed loop transfer function can be computed as:

$$H(s) = \frac{K(s\tau + 1)}{s^2 + K(s\tau + 1)} \tag{5.8}$$

with

$K = K_d K_f K_v$

K_d = phase detector (time interval processor) gain

K_f = selectable filter gain

K_v = phase stepper gain

τ = selectable feed forward constant

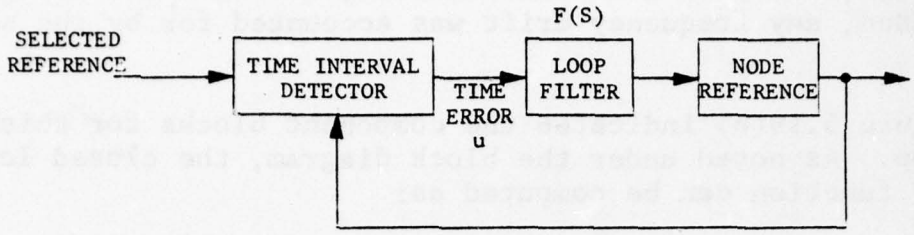
The free parameters K_f and τ can now be chosen to satisfy the bandwidth and transient behavior of the closed loop system. For good transient performance, we require close to critical damping of the loop.

By computing the damping ratio ξ and undamped natural frequency ω_n,

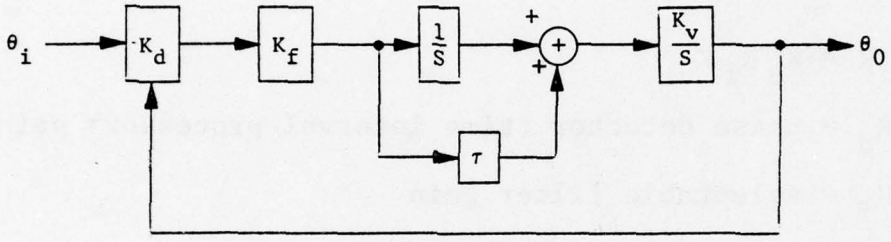
$$\xi = \frac{\tau}{2}\sqrt{K} \tag{5.9}$$

$$\omega_n^2 = K \tag{5.10}$$

we can set $\xi = 1/\sqrt{2}$ for good transient performance. Thus, we establish a constraint relationship between τ and K:



(a) General Time Servo Structure



LOOP FILTER TRANSFER FUNCTION:

$$F(S) = \frac{K_f(S\tau + 1)}{S}$$

CLOSED LOOP TRANSFER FUNCTION:

$$H(S) = \frac{K(S\tau + 1)}{S^2 + K(S\tau + 1)} \qquad K = K_d K_f K_v$$

AND

$$\omega_n^2 = K$$

$$\xi = \frac{\tau}{2}\sqrt{K}$$

(b) Detailed System Function Block Diagram

Figure 5.19 Transfer Function Specifications for the Clock Control Loop in Tracking Mode

$$\frac{1}{\sqrt{2}} = \frac{\tau}{2}\sqrt{K} \tag{5.11}$$

Then, for any desired choice of ω_n we must choose K to satisfy

$$K = \omega_n^2 \tag{5.12}$$

with

$$\tau = \sqrt{\frac{2}{K}} \tag{5.13}$$

Now, for the transfer function H(s) above, the undamped natural frequency ω_n is not necessarily the same as the noise bandwidth. A close relationship exists however. Defining the two-sided noise bandwidth as

$$B_n = \int_{-\infty}^{\infty} |H(j\,2\pi\,f)|^2\,df \tag{5.14}$$

and substituting H of Eq. (5.8), B_n can be computed as [5.4]:

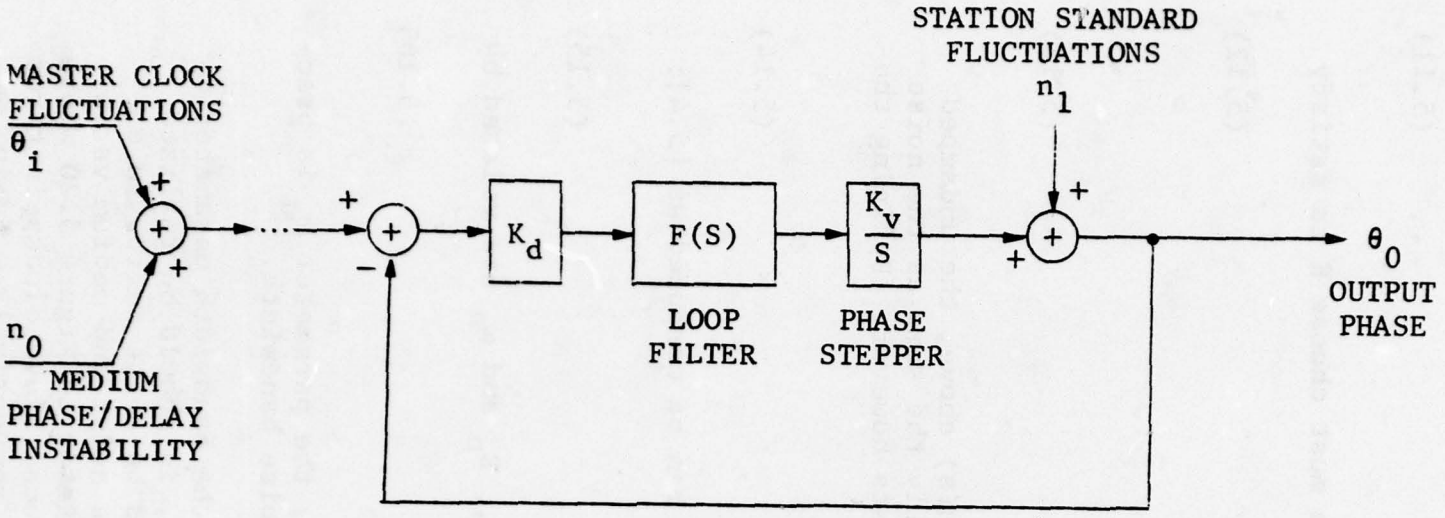
$$B_n = \frac{K\tau^2 + 1}{2\tau} \quad \text{rad/s} \tag{5.15}$$

i.e., for the selected damping ratio, B_n and ω_n are related by

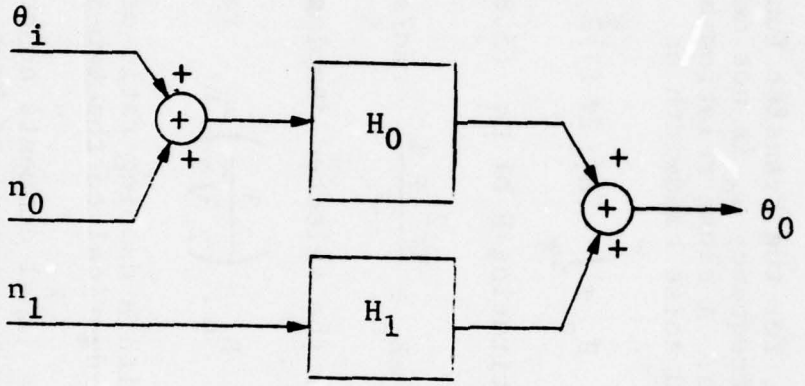
$$B_n = \left(\frac{3}{2\sqrt{2}}\right)\omega_n \quad \text{rad/s} \tag{5.16}$$

Hence, with a damping ratio of 0.707, the parameter ω_n is practically identical to the two-sided noise bandwidth.

Some final comments concerning the bandwidth parameter ω_n (or B_n) are appropriate here. First, is should be realized that the closed loop bandwidth should be quite narrow in a normal tracking mode to eliminate the noise and medium variations imposed on the input signal. Refer to Figure 5.20 where we have represented the master and local slave clocks in terms of their phase variations θ_i and θ_0, respectively. Again, we intend these quantities to be interpreted as phase shifts relative to some hypothetical ideal reference. Similarly, n_0 is



(a) Complete Block Diagram



$$H_0 = \frac{K(S\tau + 1)}{S^2 + K\tau S + 1}$$

$$H_1 = \frac{S^2}{S^2 + K\tau S + 1}$$

(b) Compressed Transfer Function Representation

Figure 5.20 Phase Noise Transfer Function for the Clock Control Loop

the phase instability resulting from transmission medium variations, while n_1 is an undesirable local clock phase noise. As far as the output phase is concerned, we would like to eliminate as much as possible of n_0 and n_1, and yet track the master phase reference θ_i. For n_0, this clearly involves a compromise, since n_0 and θ_i are indistinguishable without recourse to a-priori information about the nature and time scale of the fluctuations. In any case, the loop filter can be adjusted to smooth out as much of the n_0 variations as possible without degrading the tracking of θ_i significantly. With a quartz master reference, this would mean inverse bandwidths higher than, say, 100 seconds, whereas for atomic standards, much longer time constants (narrower bandwidths) would be appropriate.

The phase noise component generated by the local station standard (n_1) is considered undesirable, but it is not easily removed. The transfer function relating an input n_1 to the output phase has been denoted H_1 on Figure 5.20, whereas the transfer function for n_0 and θ_i is shown as H_0. The former represents a highpass filter characteristic. Hence, a narrower loop bandwidth (ω_n) results in a greater level of local standard phase noise in the output. Clearly, there is an optimum choice of bandwidth to be made, depending on the specific phase noise characteristics of the local standard.

The final selection of loop parameters is determined as much by transient behavior as by noise bandwidth requirements. We have already seen in Figures 5.16, 5.17, and 5.18 the transient response of a loop designed in the fashion described. With only one free parameter to select (K), the response rise time in those figures was seen to vary directly with the closed loop bandwidth when a phase step was introduced at the point of switching from acquisition to tracking. Note that, in the earlier examples, there was no frequency offset between the input reference and local node reference, so the plots referred to are for a pure phase step.

When attempts are made to lock together two clocks having a frequency offset, transient responses of the form shown in Figures 5.21 and 5.22 are generated. Once again, these results were obtained on a 75-mile LOS link cascade at RADC using the tracking loop design previously described and a quartz clock slaved to a cesium clock.

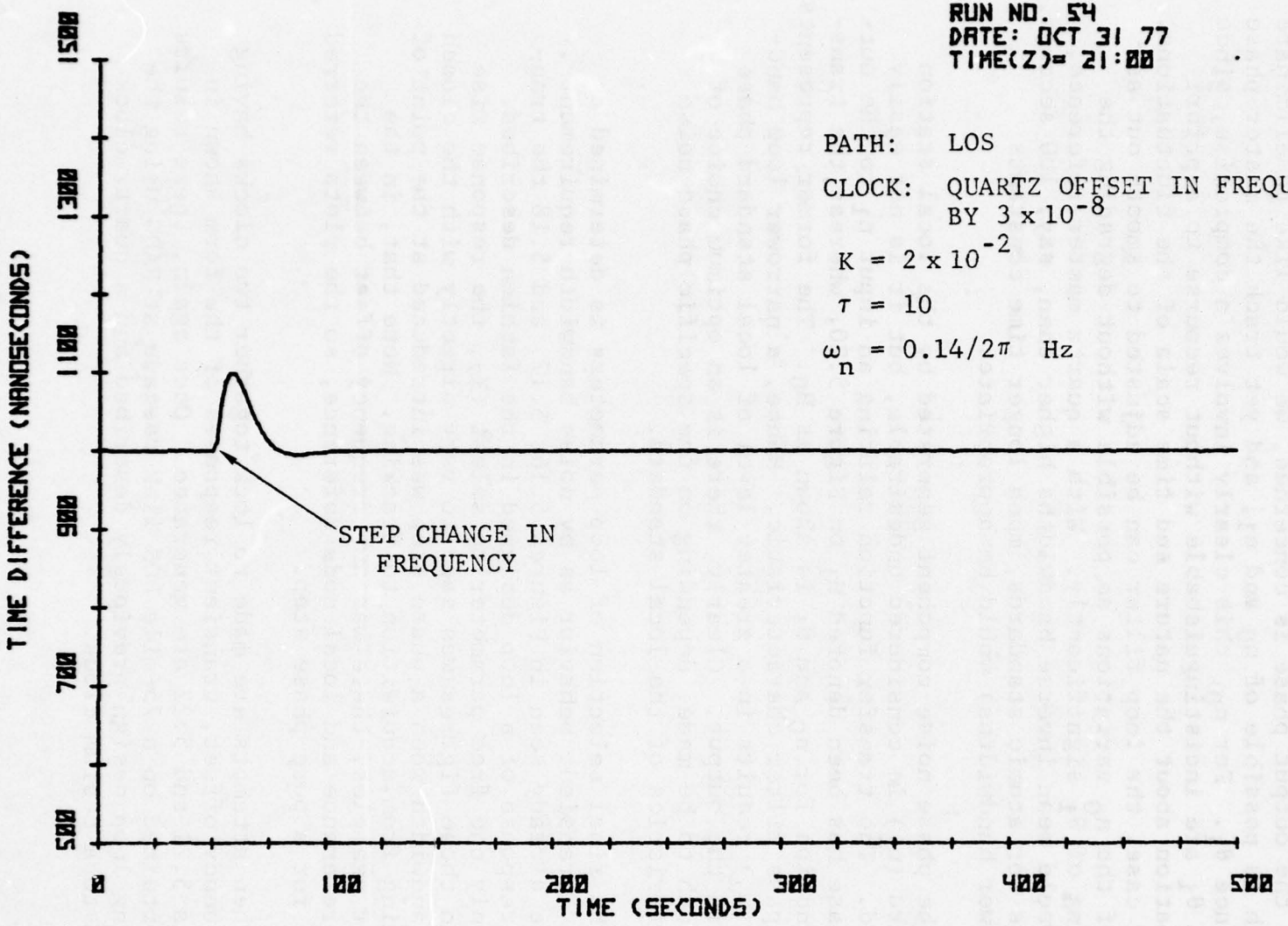


Figure 5.21 Transient Response of Clock Control Loop to a Frequency Offset of 3×10^{-8} ($\omega_n = 0.14$ rad/s)

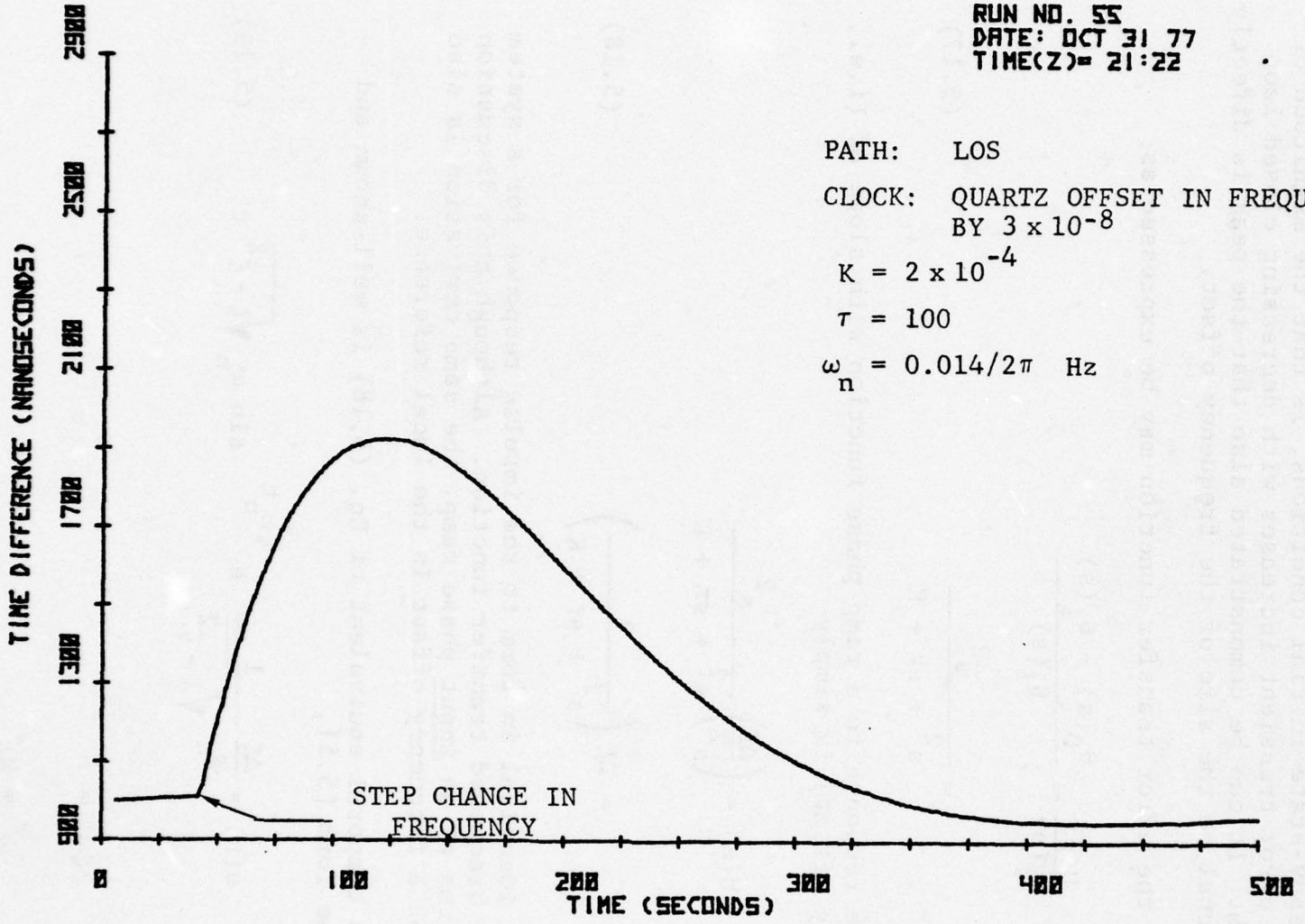


Figure 5.22 Transient Response of Clock Control Loop to a Frequency Offset of 3×10^{-8} ($\omega_n = 0.014$ rad/s)

The most interesting aspect of these curves, which were the result of quartz oscillator control voltage step changes made under steady-state initial conditions, is that the magnitude of the peak error transient increases with decreasing closed loop bandwidth. It can be demonstrated also that the peak is directly proportional to the size of the frequency offset.

Now the error transfer function may be expressed as:

$$\frac{U(s)}{\theta_i(s)} = \frac{\theta_0(s) - \theta_i(s)}{\theta_i(s)}$$

$$= \frac{s^2}{s^2 + s\tau + K} \qquad (5.17)$$

Thus, the response to a ramp phase function with slope Δf (i.e., frequency offset) is simply

$$U(s) = \left(\frac{\Delta f}{s^2}\right) \frac{s^2}{s^2 + s\tau + K}$$

$$= \Delta f \left(\frac{1}{s^2 + s\tau + K}\right) \qquad (5.18)$$

which is identical in form to the impulse response for a system with the bracketed transfer function. Although this discussion is in terms of an <u>input</u> phase ramp, the same derivation is also valid for a frequency offset in the local reference.

The temporal equivalent of Eq. (5.18) is well-known and takes the form [5.5],

$$u(t) = \frac{\Delta f}{\omega_n} \frac{1}{\sqrt{1 - \zeta^2}} \; e^{-\zeta\omega_n t} \; \sin \omega_n \sqrt{1 - \zeta^2}\; t \qquad (5.19)$$

where

$$2\zeta\omega_n = \tau$$

$$\omega_n^2 = K$$

The maximum of this time function can readily be found by differentiating. Specialized for a damping ratio of $1/\sqrt{2}$, the result can be stated as follows:

$$u_{max} = \frac{\Delta f}{\omega_n} e^{-\pi/4}$$

is the maximum error, and it occurs at a time

$$t_{max} = \frac{\sqrt{2}\ \pi}{4\ \omega_n}$$

The error peak is, therefore, inversely proportional to the parameter ω_n, as is seen on Figures 5.21 and 5.22, while the time of the peak is also inversely related. The consequences of selecting very narrow loop bandwidths are therefore manifest as excessive error peaks when locking up to a clock offset in frequency.

Generally, the transition from acquisition to tracking will involve a master and slave clock that are offset in both time and frequency. The transient behavior will then be a combination of the effects demonstrated because of the system linearity and recourse to superposition principles.

Conversion of the loop filter to a discrete time (digital) filter equivalent is quite straightforward. For example, using the impulse invariant method of transformation, the discrete time transfer function G(z) is found from

$$G(z) = F(s)\Big|_{s+a = (1-e^{-aT_z-1})} \qquad (T = \text{sample interval}) \tag{5.20}$$

Hence, with

$$F(s) = \frac{K_f(s\tau + 1)}{s}$$

$$G(z) = K_f\tau + \frac{K_f}{1 - z^{-1}} \tag{5.21}$$

Equivalently, defining x as a state variable and u as the input process (to the loop filter), the output y is written as

$$y_n = x_n + K_f \tau u_n \tag{5.22}$$

with state equation

$$x_n = K_f u_n + x_{n-1} \tag{5.23}$$

where y_n is the n^{th} sample output to the phase stepper. The composite discrete time system block diagram is shown in Figure 5.23.

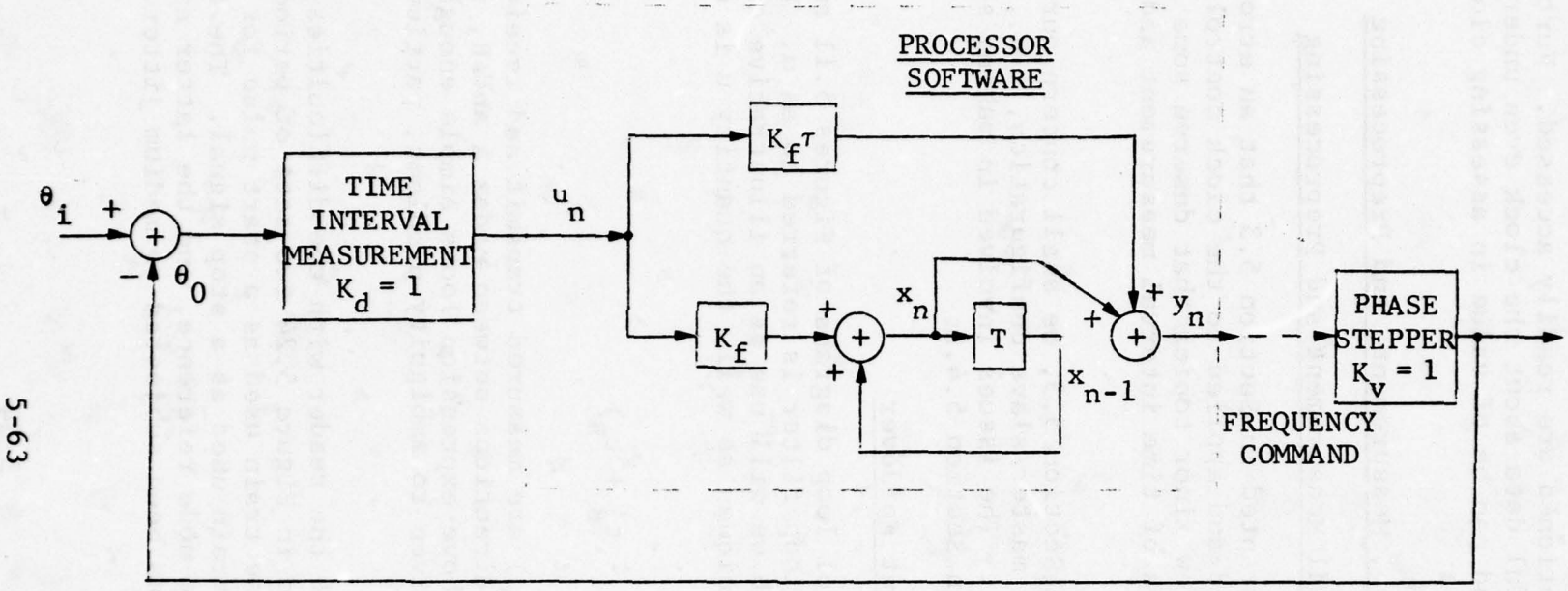
5.3.5 Coast Behavior

There will be circumstances when no reference is available to a node because of link or clock outages. Furthermore, there are times when a node is required to reference itself, e.g., while reference selection information is propagating through a network, and a node may have to coast for a period of time rather than immediately selecting a new reference.

Provided the accumulated clock control information is used correctly, this should be a satisfactory mode of operation even with lower quality quartz clocks. The assumption must of course be made that the network was previously stable and that the information in question is valid.

Earlier, in Section 5.3.1, we discussed the advantages of including pure integrators in the open loop transfer function. The relevant information is also contained in Figure 5.12 where the integrator inputs are equivalent to relative frequency offset and rate of change of frequency for the master and slave clocks.

It can be inferred from this earlier material that the clock controller "learns" these steady-state offsets over a period of time, and it follows that when no references are available to the node, an excellent strategy is to clamp the integrator inputs at their existing values to compensate for local clock offset and drift relative to the node's perception of the network time reference.



T = UNIT DELAY (1 SECOND)

Figure 5.23 Discrete Time System Function Representation of the Clock Control Loop

The parameters mentioned are readily accessed. Furthermore, they provide useful data about the clock even under normal tracking conditions, and can be of value in assessing clock degradation.

5.4 Reference Selection, Measurement, and Preprocessing

5.4.1 Time Interval Measurement and Preprocessing

It was taken for granted in Section 5.3 that an error signal could be measured and applied to the clock control loop. There are, however, a few minor topics that deserve some comment in the general area of time interval measurement and preprocessing.

As was the case in Section 5.3, we shall concern ourselves primarily with a single master/slave configuration, i.e., the selected reference link. The issues involved in making such a selection are covered in Section 5.4.2.

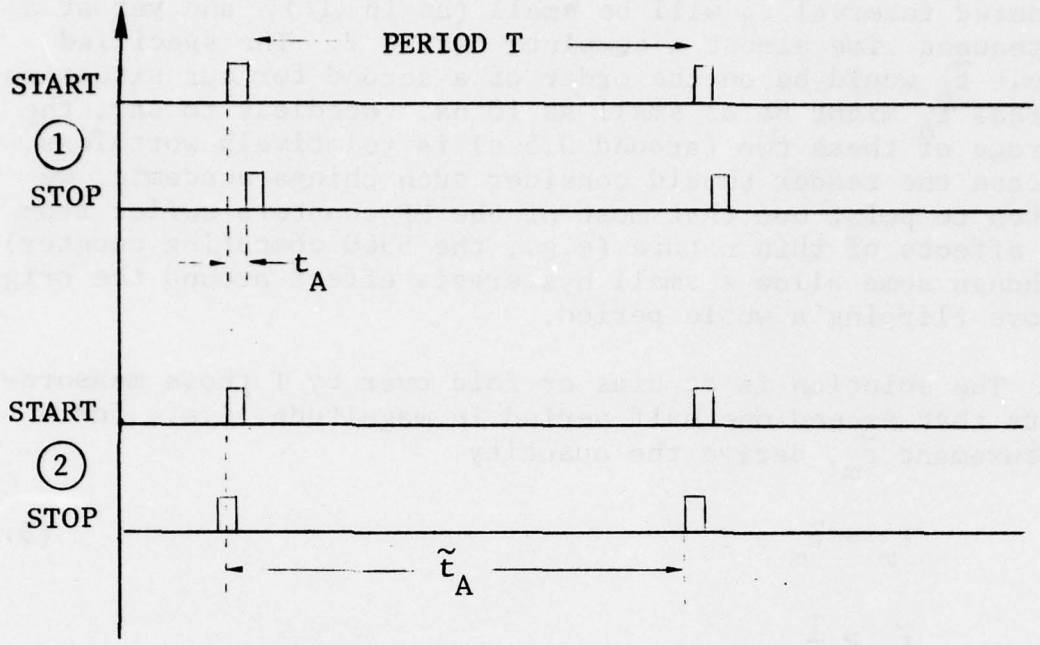
5.4.1.1 Measurement Foldover

In the basic control loop diagrams of Figures 5.11 and 5.12, the input to the loop filter is referred to as u. For the TRD technique, which we will use as an illustrative example to cover all other techniques as well, the quantity u is computed as

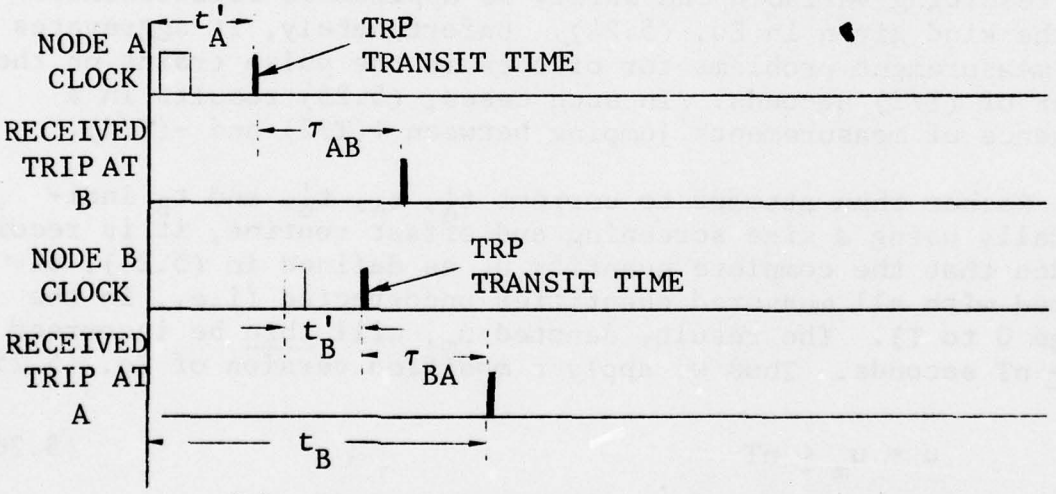
$$u = \frac{1}{2}(t'_A - t_A - t'_B + t_B) \tag{5.24}$$

where (t'_A, t_A) and (t'_B, t_B) are measured transmit and receive times for the two link directions between nodes A and B, respectively. While the above expression looks simple enough, some thought has to be given to ambiguity problems, particularly if u is to be averaged.

To quickly acquaint the reader with the difficulties that arise, we have presented in Figure 5.24 two sets of periodic pulses with the top pulse train used as a start pulse for a counter, and the lower train used as a stop signal. The former might represent a stable node reference, and the latter an incoming signal which has been subjected to medium jitter.



(a) Start/Stop Measurement Difficulties for Two Periodic Pulse Trains



(b) Timing Diagram for Delay Measurement

Figure 5.24 TRP Timing Diagrams

In certain situations of the variety illustrated, the measured interval t_A will be small (as in ①), and yet at a subsequent time almost a complete period T. The specified result $\tilde{t}_A$ would be on the order of a second for our situation, whereas t_A might be as small as 10 ns. Needless to say, the average of these two (around 0.5 s) is relatively worthless. In case the reader should consider such things academic, we hasten to point out that most of the HP counters suffer from ill effects of this nature (e.g., the 5360 computing counter) although some allow a small hysteresis effect around the origin before flipping a whole period.

The solution is to bias or fold over by T those measurements that exceed one half period in magnitude, i.e., for a measurement $\tilde{t}_m$, derive the quantity

$$t_m = \tilde{t}_m - T \tag{5.25}$$

if $$\tilde{t}_m > \frac{T}{2}$$

That removes the problems for a pulse train whose time of arrival is almost coincident with the counter reference, and the resulting variable can safely be applied to relationships of the kind given in Eq. (5.24). Unfortunately, it aggravates the measurement problems for offsets in the pulse trains on the order of (T/2) seconds. In such cases, (5.25) results in a sequence of measurements jumping between +(T/2) and -(T/2).

Rather than attempt to correct t_A', t_A, t_B', and t_B individually using a size screening and offset routine, it is recommended that the complete quantity u, as defined in (5.24), be formed with all measured quantities uncorrected (i.e., in the range 0 to T). The result, denoted u_m, will then be incorrect by $\pm$ nT seconds. Thus we apply a modified version of Eq. (5.25):

$$u = u_m \pm nT \tag{5.26}$$

with n chosen to give the result u in the range [-T/2,T/2]. Mathematically this is expressed as

$$u = (u_m) \bmod T \tag{5.27}$$

When the value of u_m is too close to $\pm(T/2)$, this strategy must be modified by simply replacing the step called for in Eqs. (5.25) or (5.26) above with a positive biasing of u_m by nT to make u fall in the range [0,T]. Fortunately, this situation will occur only rarely since it corresponds to the startup mode of operation.

The same ideas must also be applied to the corresponding error signals for mutual sync and master/slave techniques, but the extension of the above approach to these cases is trivial and will not be discussed.

5.4.1.2 Data Averaging

For quiescent network operation and well-behaved links, the time data available could easily be subjected to preliminary averaging. There are three choices:

(1) Explicit averaging of the raw measurement data, t_A, t'_A, t_B, t'_B.

(2) Explicit averaging of the derived variables such as u of Eq. (5.24).

(3) Implicit averaging by means of the clock control loop action.

Although not exactly equivalent, the similarities for these choices are more notable than the differences.

The first option can be rejected on the grounds that immediate exchange of parameters, such as t_A and t'_A, between nodes is desirable from the point of view of increased awareness of potential trouble. Consequently, there is no sense in averaging them individually at their respective measurement point and, from the discussion in Section 5.4.1.1, individual averaging would also be more complicated because of the need to fold over each variable rather than the composite produced by means of an expression such as Eq. (5.24). Furthermore, the instantaneous path delay can be computed from the raw measurements; averaging times and presentation of such data will be subjected to a different set of requirements than the clock control variables.

Our conclusion, therefore, is that separate averaging of t_A, t'_A, t_B, and t'_B is not desirable, so we now consider the possible advantages in averaging derived quantities such as u in Eq. (5.24).

It should first be recognized that any averaging of u is, of necessity, done within the loop; that is, it must be implemented on a signal which is itself affected by the result of the averaging. Functionally, then, it belongs in the loop block diagram cascaded with the loop filter, as shown in Figure 5.12. While the question of separation of the averaging and loop filtering function is important in designing the reference selection and acquisition switchover capabilities for the clock servo, it can be seen that averaging and filtering functions are virtually indistinguishable under steady-state tracking conditions with a single reference. In other words, the averaging can be carried out by means of a block (box-car) or recursive averaging form of implementation; the latter is identical to a lowpass filter, and can thus be built into the loop filter.

This subject will be taken up again in Section 5.4.2 where reference selection strategies are discussed.

5.4.1.3 Path Delay Calculations

The requirement for path delay measurement can easily be satisfied once the four relevant time measurements are available at one end of the link. Thus, if t_A', t_A, t_B', and t_B have the same significance as before, the path delay is obtained from:

$$\tau = \frac{1}{2}(t_A - t_A' + t_B - t_B') \tag{5.28}$$

provided the delays τ_{AB} and τ_{BA}, shown in Figure 5.24(b), are identical. This will not be the case on an instantaneous basis for TROPO paths where τ_{AB} and τ_{BA} may differ by several hundred nanoseconds. In reality, Eq. (5.28) is simply

$$\tau = \frac{\tau_{AB} + \tau_{BA}}{2} \tag{5.29}$$

The clock error and path delay can only be separated with two measurement equations and the assumption of equal delays in the two directions. In some cases, the clock error may be smaller than the path difference. If this is the case, the delays can obviously be approximated by:

$$\hat{\tau}_{AB} = t_A - t_A' \tag{5.30}$$

and

$$\hat{\tau}_{BA} = t_B - t'_B \tag{5.31}$$

[Refer to Figure 5.24(b).] The use of either Eq. (5.29) or (5.30) and (5.31) for delay calculation will be dependent on the circumstances, e.g., TROPO vs. LOS link, and confidence in the accuracy of the local reference.

5.4.2 Reference Selection Issues

We are mainly concerned here with the censoring of bad or unreliable timing data to assist the timing reference distribution (TRD) selection process. To a lesser extent though, these same link monitoring functions are of value in the master/slave and mutual sync techniques where, rather than forcing an alternative reference selection, a poor reference is dropped completely from the error signal formulation.

5.4.2.1 Link Quality Assessment

Reference selection will be based on various items of information available to the clock control processor. Some of these are derived naturally from other clock control parameters, and the remainder are accessed via the fault and status register, shown in Figure 5.7, which monitors equipment alarms.

The quality assessment parameter flags are divided into two tiers. "Switch" flags (level 2) are considered fatal and force the processor to choose an alternative reference. "Time-out" (level 1) flags are indicative of difficulties which may be temporary in nature. Persistent level-1 flags will be promoted to level 2 after a period of time (e.g., 1 minute). In the interim, the control loop will proceed in the coast mode, and measurement data, which must be considered unreliable, will be ignored.

The quality assessment parameters of interest are itemized in Table 5-5 and, with the comments included, this table should be self-explanatory.

5.4.2.2 Reference Monitoring and Selection

This subsection concerns the TRD reference selection process. Suitable rules for automated and distributed selection

TABLE 5-5

LINK QUALITY ASSESSMENT PARAMETERS

Time-Out Parameters	Indicator	Comments
Radio DEMUX Sync Loss	Equipment alarm	Usually caused by loss of BCI or temporary link outage
Service Channel DEMUX Sync Loss	Equipment alarm	Usually caused by loss of BCI or temporary link outage
Buffer Status	Full/empty flag	Does not affect reference selection normally
Magnitude of Computed Clock Error	$u_n = \frac{1}{2}(t'_A - t_A + t_B - t'_B)$	Test on individual sample basis
Measurement Error	Time interval flag	Radio sync TRP omitted because of errors; time measurement exceeds 1 second

Switch Parameters	Indicator	Comments
Magnitude of Averaged Clock Error	u_2 of Figure 4.20	Test output of averaging filter
Rate of Change of Reference Clock	y of Figure 4.20	Local and reference clocks may be offset in frequency even though clock error is bounded
Excess Path Delay	$\tau_{AB} = t_A - t'_A$ $\tau_{BA} = t_B - t'_B$	Test on an averaged sample basis; compare with nominal delay
Change in Ultimate Reference Rank Parameters	N_1, N_2, N_3	Discussed in Section 5.4.2.2

of a reference by individual nodes in the network have been discussed at length in several references [5.3] and [5.7]. They can be briefly summarized as follows.

Each node in the network is assigned a unique rank according to the quality of its clock. Then, all nodes are required to transmit out to connecting nodes the rank of the ultimate master N_1 being used by that node, the ranking of the total transmission path between it and its ultimate master N_2, and the rank of its own currently available clock N_3. The basic selection rules for a set of available* references are, then:

> Rules 1, 2, and 3: A node must reference itself temporarily at the time of network startup, loss of link to the immediate reference node, or when the ultimate reference rank is lowered.
>
> Rules 4, 5, and 6: For all available connected nodes (including the node in question), the choice of reference is made successively on the basis of the best N_1, N_2, and then N_3.
>
> Rule 7 states that if no links are available, a node references itself.

These rules were found to be sufficient to produce a unique and optimum timing distribution on each occasion that the network was started up. That is, automatic selection of the highest ranking node in the network as the ultimate master by each node, and transfer of timing to this node from the network master by a path of minimum demerit. Problems have been uncovered for fault situations where obsolete data can propagate through the system and disrupt the decision processes. The time required to purge this misleading data is, of course, related to the size of the network and the rate at which reference selection can be updated. This indicates the desirability of a high TRIP transmission rate.

One possible method of overcoming the obsolete data problem is by giving each node an update counter N_4 [5.7]. If the node count is low enough relative to update counters associated with available incoming references, the node is forced to reference itself temporarily. However, with the implementation of a

*"Available" here is intended to mean that none of the alarm flags in Table 5-5 are active.

suitable counter decrement strategy (for each node), the self-referencing outcome will usually just be temporary.

The previous rules are used to choose a tentative best reference; then a final decision is made based on the "decision" rules which are applied sequentially to the tentative best reference. They are as follows:

Rule D1: When the tentative best reference is the node itself, the update counter is decremented by 1 (to a minimum of 0).

Rule D2: If the received update count from the tentative choice is smaller than the local update count, the tentative reference selection is confirmed and the received update count is incremented by 1, and thereafter used at that node.

Rule D3: Otherwise, the node uses itself for a reference and increments its own update counter by 1.

A detailed study of the software implementation of this algorithm was published recently [5.8]. Other solutions to the obsolete data problem have been suggested [5.3], and an alternative set of TRD decision rules involving multiple path, rather than single path selection, have been described in [5.6].

5.4.3 Switching Transients

At the time of switching between alternative references, transient behavior will be experienced. A reasonably smooth transition is possible, however, if all of the potential reference signals are monitored and individually filtered. Since this filtering is carried out in software, the only possible objection is the additional software computational burden. Such a philosophy results in switching of alternate links near the phase shifter interface and, although transient effects are still not completely eliminated, they are definitely reduced in comparison with any approach that involves switching at the loop input. This issue is particularly important for TROPO links where momentary fluctuations in path length will appear in the clock error signal u. For such links, short-term jitter (which can be several hundred nanoseconds) is not cancelled in the computation for u.

To illustrate the link switching alternatives, consider the block diagram in Figure 5.25. After averaging the available

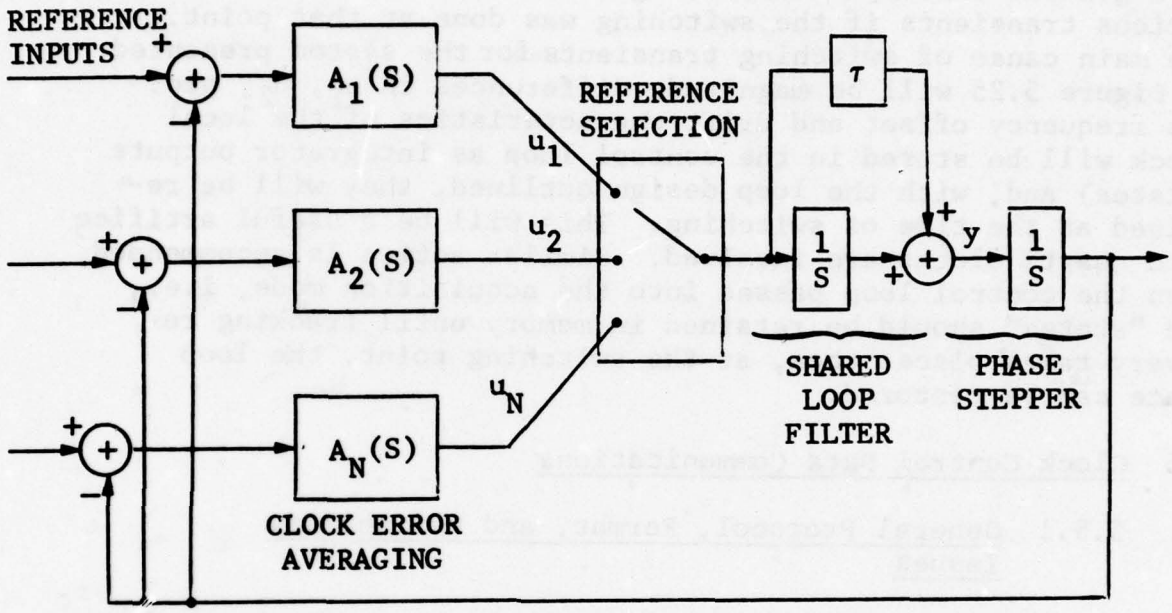


Figure 5.25 Reference Selection and Control Loop Block Diagram for Transient Minimization

references with the filters marked as A_1, A_2, ..., A_N, the residual jitter in the references will be relatively small. Ideally, all of the smoothed clock error estimates, u_1, u_2, u_3, etc., will be identical and close to zero. One of these signals is then selected for use by the remainder of the loop. The approach recommended here uses a shared loop filter to avoid a possible integration of nonzero error estimates. If separate integrators are used with A_1, A_2, etc., there could be a gradual buildup at the integrator outputs which would cause serious transients if the switching was done at that point. The main cause of switching transients for the system presented in Figure 5.25 will be magnitude differences in u_1, u_2, etc. The frequency offset and drift characteristics of the local clock will be stored in the control loop as integrator outputs (states) and, with the loop design outlined, they will be retained at the time of switching. This will be a useful artifice when quartz clocks are involved. Similar action is recommended when the control loop passes into the acquisition mode, i.e., the "states" should be retained in memory until tracking recovery takes place; then, at the switching point, the loop state can be restored.

5.5 Clock Control Data Communications

5.5.1 General Protocol, Format, and Reliability Issues

The transfer of clock data throughout the network requires some thought, particularly with regard to error control and centralized network control.

Reliability for the clock control data link is paramount. It is quite obvious that the data being transferred between nodes is highly intolerant of errors; the adaptive reorganization merit and ranking parameters, for example, must be carefully protected to eliminate the possibility of inadvertent network reconfiguration.

The task of designing the data link is complicated even further by the following considerations:

- Error patterns observed on the links will tend to be burst-like as a result of channel fading, particularly for TROPO and LOS systems.

- Although the DCS specifications call for quite low error rates (e.g., 5×10^{-9} for LOS, 5×10^{-5} for TROPO, 99.99% of the time), data link integrity is even more important during periods of jamming when the error rates will be much higher. Therefore, a high tolerance to errors is necessary.

From these statements we can glean some important guidelines which apply to our data link design. Briefly, there are certain data items that must be delivered with virtually zero error probability or, as an alternative, not at all; i.e., gaps in the clock updating procedure are preferable to the use of invalid data. Then it must be accepted that, during times of stress, the raw bit error rate may be quite high (e.g., approaching 0.5). These two facets of the data communications design task are rather ominous considering the narrow range of options they leave open.

The necessity of achieving close to zero error probability strongly suggests that a dependable error detection scheme is mandatory; error correction is of limited value, although it may be useful in bolstering the effective data transfer rate. The use of several data modes is also advocated. We can exploit the fact that in a heavy jamming situation only the more essential data need be conveyed between nodes. Thus, we should contemplate a backup low data rate mode of operation. The unused capacity would then serve to enhance the reliability of the remaining data bits by allowing additional redundancy.

5.5.1.1 Data Format

The data to be transmitted between nodes come in several different forms, including ASCII time-of-day characters, single bit flags for condition and fault indication, integer counts for TRD merit and ranking, and 4-byte floating point format variables. All of this information could be converted to 8-bit ASCII bytes, but there is a penalty in terms of data transmission efficiency as well as the additional processor burden to carry out the code conversions; i.e., with every four bits of straight binary, we need to allocate seven bits for the ASCII code (assuming a 4-bit hexadecimal format) plus an additional parity bit. Most of the relevant data here takes the form of floating point numbers, so the overall efficiency is seriously affected by the use of ASCII. Such a scheme can be referred to as byte-oriented, whereas a bit-oriented scheme would use the data in its original form without the need for

conversion to a byte structure. The final selection has an impact on the form of line protocol that can be used. With byte-oriented protocol [5.9], certain byte patterns are reserved for use as line control characters and are, therefore, not available to the user. For bit-oriented protocol [5.10], we have the other problem; any bit pattern is considered valid, and full transparency can then only be achieved if the line controller modifies the data (bit stuffing) at transmission and corrects for that action at the receiver (bit deletion) so that a few control patterns are kept sacred. Bi-sync is an example of a byte-oriented protocol, while SDLC (i.e., ADCCP) is a bit-oriented protocol.

5.5.1.2 Error Control

Error will occur in the transmission of data from one point to another and, if the information content is highly critical as it is in the case of clock control, plans must be laid for dealing with the errors. There are two fundamental categories for improving the reliability of a data link. The first, commonly called ARQ (automatic repeat request), involves transmission by blocks. Each block has a number of parity bits appended. At the receiving end, the parity bits are recomputed from the data and compared with the received parity bits. If there are no discrepancies, the block is accepted; otherwise, the sending station is notified and the complete block must be transmitted. This is referred to as an error detection scheme. We rely on the decoder to detect the presence of most errors, while correction may be carried out by retransmission.

Forward error control (FEC), on the other hand, is more complicated and involves attempts by the decoder to determine the location of the errors from the pattern of discrepancies between received and recalculated parity bits. With FEC there is an error correction mechanism. Depending on the nature of the error patterns, FEC systems may be able to correct a maximum number (say, t) random errors or, alternatively, a burst of errors having a span of B bits. Composite error detection/error correction schemes using both ARQ and FEC can also be devised.

In most situations, particularly TROPO, the errors will not be independent random events, primarily because of channel fades and we must evaluate and compare the performance of ARQ and FEC techniques carefully to see how they perform in a burst error environment.

While ARQ errors may be corrected by retransmission of a block, the FEC must attempt correction on the fly. Thus we see that, although FEC may not be able to achieve such low overall error rates as ARQ, the latter has a variable and possibly low transmission efficiency. There is no doubt that a combination of both has merit [5.11],[5.12].

There are several ARQ variants. By far, the most common is the stop and wait system, whereby the transmitter waits after each block for a positive acknowledgement before sending the next block. Then there are two versions of the so-called continuous ARQ approach. With sequential numbering of the outgoing blocks, the receiver is able to request retransmission of a particular block. This can be done in a pull-back manner; the transmitter discounts any higher numbered blocks it may have sent in the interim, and retransmits a complete sequence of blocks, starting at the block found to be in error. This keeps the blocks in sequence. Alternatively, the transmitter can retransmit only the block found to be in error, in which case the blocks would be received out of order.

FEC performance is more sensitive to the distributional nature of the errors, e.g., burst or random. The easiest way of achieving protection against both kinds is to use interleaved codes; with a relatively low cost approach, modest improvements can be achieved with this method. The FEC schemes available are successful to one degree or another in reducing the bit error rate. But the fact remains that errors must be virtually eliminated for some of the more sensitive clock data. Consequently, a high level of error detection performance is still required.

5.5.1.3 Line Protocol and Error Control Recommendations

The preceding paragraph suggests that the principle of operation for the data link should be based on ARQ with a very low residual undetected error rate by judicious choice of parity check code. However, it is apparent that additional FEC capabilities will be required between the SDLC line controller and the service channel multiplexer to maintain good performance during periods of jamming when the error rate will be quite high.

A full investigation of the requirements for such an FEC unit appears necessary. However, three key topics can be itemized at this point:

- Delay through the FEC must be carefully controlled if the clock data channel is being used to convey node time, as in option B of Section 5.1.2.
- With the channel data rate tentatively selected as 4 kb/s, and an information rate that is on the order of 300 b/s, there is significant redundant channel capacity available for use by the coding scheme.
- Contingency plans can be formulated for minimizing the data transfer requirements during jamming situations. Such a reduction will allow the use of even lower rate codes in the FEC application.

Finally, we note that the burst nature of the error distributions existing on TROPO links creates additional difficulties which can only be solved with specialized coding and decoding equipment.

5.5.2 Compatibility with DCS Signaling Formats

In earlier sections we investigated the relationships between different time transfer implementations and the accessibility of the required signals within the DCS transmission equipment. For all of the three options discussed at length in Section 5.1.2, the demands on the network service channel gravitated toward a dedicated 4-kb/s subchannel. The reasons for this are the following:

- The full system digital telemetry channel data rate is not needed by the clock control system and is shared with other network control functions on the basis of time-division multiple access or synchronous time-division multiplexing. The latter has been selected.
- Although a high data rate is not necessary, equipment delay uncertainties can be a problem if a simple sub-MUX approach is used.
- With the TRP transmission interface, option B, the clock data link must be fully synchronized with the service channel MUX/DEMUX. This requirement narrows the choice in such a way that 4 kb/s is the most obvious choice of clock data rate (see Appendix B). With the service channel modifications suggested, the full 56-kb/s system

telemetry channel is preserved, and the additional 4-kb/s clock data channel is derived from what would have been wasted capacity.

The objective in subsequent sections will be to verify that the 4-kb/s rate budgeted is adequate for the data involved.

5.5.3 Clock Data Format and Rate Requirements

We are now at the point where the data rate burden must be estimated. This will be done for a hypothetical SDLC [5.10] packet transmission between nodes.

The basic data format in our example is illustrated in Figure 5.26. Because the TRIP transmission rate is once per second, we can refresh parameters at opposite ends of the link at the same rate. Thus, the TRIP shown in Figure 5.26 will contain all of the clock update parameters required for the cooperative node. These include the following:

Node Status - sync and overflow condition flags for radios and buffers; also, loop mode, e.g., acquisition and tracking.

Transmit Time (t'_A) - measured time of previous outgoing TRP signal relative to 1 pps.

Receive Time (t_B) - measured time of previous incoming TRP signal relative to 1 pps.

Clock Error (u_A) - current estimate of clock error.

TRD Rank and Merit Parameters - TRD decision parameters N_1, N_2, N_3, N_4.

Second Count - time in seconds at last 1-pps tic at transmit node.

The number of bits allowed for each of these parameter fields is seen near the top of Figure 5.26. The standard SDLC control address, flag, and frame check fields are included also. Except for the controller message area which will be described shortly, the total count comes to 214 bits.

The remaining packet capacity is allocated to exchange of network level commands and performance parameters. In addition, provision has been made for transmission of date and time

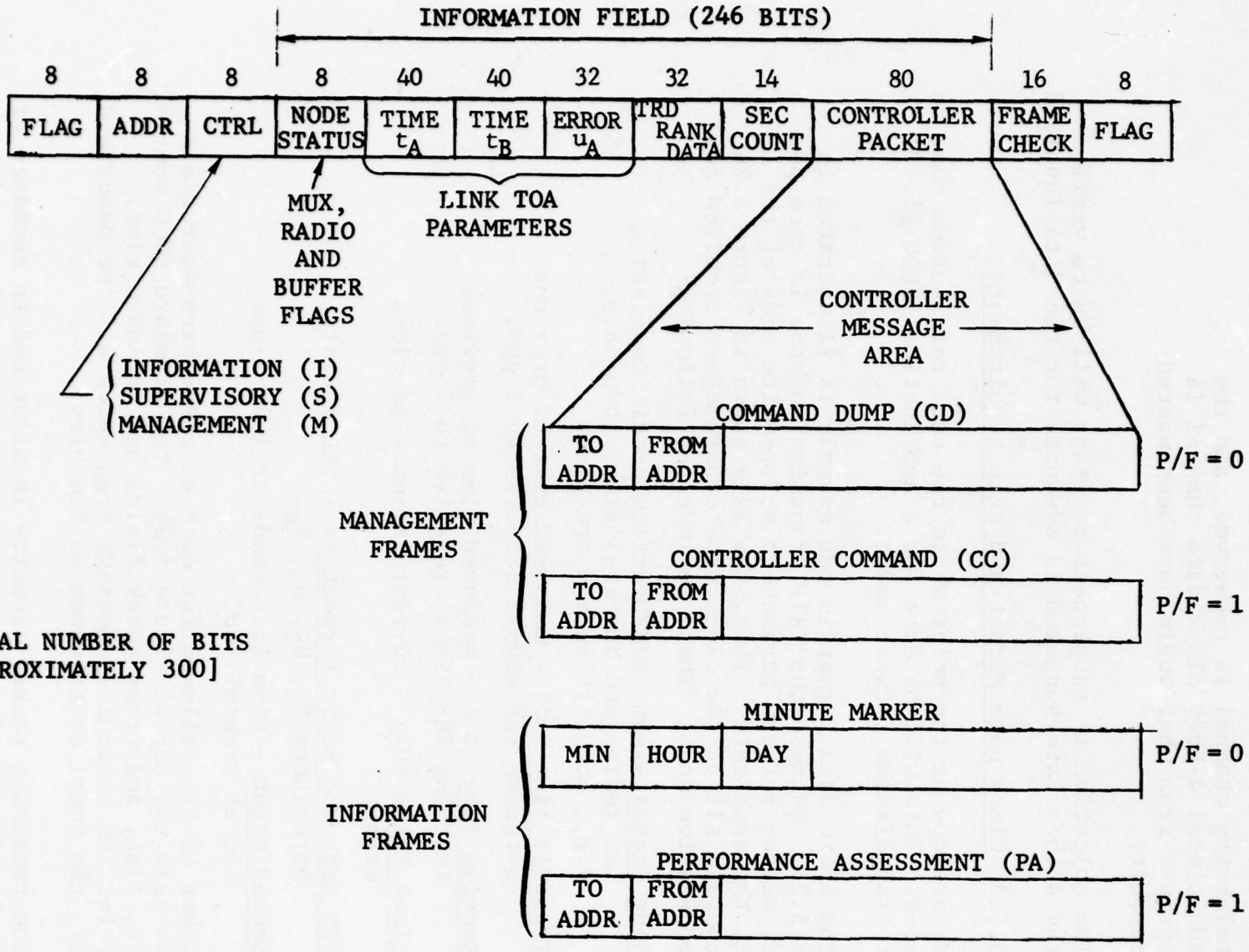


Figure 5.26 Clock Data TRIP Format

of day resolved down to 1 minute; this would be transmitted only on the minute boundaries in order to conserve space in the 1-second data transmissions.

There are four different controller message formats, as shown in Figure 5.26. The normal SDLC control field is used to signal the transmission of an information, supervisory, or management frame (i.e., TRIP). The poll/final bit in this field can be used to give two choices for each of these frame types. For example, management frames, which will be subjected to error checking and retransmission if necessary, might be used to convey network control commands to the outlying timing subsystems or, alternatively, to send back the command responses.

Those frames designated as information frames are considered less critical. If an error condition is found, the complete frame can be rejected and a retransmission requested or the clock processor can simply wait for the next 1-second data burst.

With the allowance of 80 bits for the general control message area, the total bit count is about 300 bits.

Finally, it should be mentioned that all time/date variables would probably be transmitted as 7-bit ASCII (for a total of 63 bits) when the minute marker message is transmitted (once per minute). Other parameters will be single bit flags, addresses (8-bit bytes), or floating point variables (32 bits plus 8-bit mantissa extension).

With a TRIP length of 300 bits and data rate of 4 kb/s, the total transmission time would be on the order of 75 ms.

5.5.4 Data Link Performance

Performance for ARQ is dependent on the block error rate, i.e., probability of one or more errors in a block, the time delay for retransmission of a block, and the undetected error rate [5.13]. For stop-and-wait ARQ, the time to send a message will be approximately a multiple m of the time to receive a block, check for errors, and request a retransmission. Hence, the transmission time T is given by

$$T(m) = m(2T_p + T_b + T_r) + T_p + T_b$$

where

T_p = propagation time (one-way)

T_b = information block duration (300 bits)

T_r = repeat request block duration (48 bits)

m = number of repeats required for successful data transfer

Here we have assumed a short block format (supervisory) for the retransmission request. The total transmission time for a single block repeated m times is, therefore,

$$T(m) \simeq m\,87 + 75 \quad \text{(in milliseconds)}$$

and the probability that it will take m or more repeats is:

$$P(m) = p_b^m$$

where

p_b = block error probability

Propagation delays have been neglected in the above expressions; for LOS and TROPO paths, they are small compared with the duration of a block. For other media, inclusion of path delay may be warranted.

Evidently, up to about ten retransmission attempts will be permitted every second for blocks of data containing 300 bits.

The length of data block transmitted and link error rate will both be influential factors as far as clock control performance is concerned. The principal error effects we are faced with are as follows:

- Probability that at least one bit in a block is in error (block error rate).
- Probability that the OPEN FLAG sequence is received in error.
- Probability that the OPEN FLAG is in error and a data sequence is received as a FLAG.

The first of these results in rejection of the frame data, although certain attributes, such as arrival time, may still be considered valid and useful. The second situation applies to the incorrect reception of the true OPEN FLAG bits. This results in an arrival time miss. The receiving station, which is monitoring the line for the arrival of a FLAG sequence, will therefore not register the start of a TRIP; however, subsequent data in the TRIP (including the CLOSE FLAG) will be scanned for a FLAG. This leads to the third kind of error situation, where not only is the true OPEN FLAG missed but, because of line errors, a portion of the data is converted to a FLAG and assumed to be the start of a TRIP. It is evident that the processor will easily recognize the occurrence of such events. It need only examine a few of the bytes following the registration of a FLAG and, if the extracted address and control bits are not consistent with previous TRIP's, a false alarm FLAG is assumed. In any case, the frame error checking procedure will show that an indiscretion occurred, and the data itself must certainly be used with caution.

Error detectability is also an important performance criterion. This is a specification of the probability that an error will occur in a block and not be detected, so that the block is accepted without a request for retransmission. The probability of an undetected error is inversely related to the number of check bits. This can be easily illustrated by means of a high error situation corresponding, for example, to a deep signal fade. If the raw error rate approaches 0.5, there will be many code sequences received that are accepted as being valid despite an abundance of errors. With a block length of n containing k information bits and n-k check sum bits, there will be 2^n possible equi-likely received sequences when the error rate is 1/2. Of these, 2^k correspond to acceptable information sequences with associated check bits. Consequently, the fraction of error patterns that are passed as valid is $2^k/2^n$, which is equivalent to an undetected error rate,

$$P_u = 2^{k-n}$$

$$= 2^{-\ell}$$

where ℓ is the number of parity bits. Note that the result is independent of the block length.

The above relationship holds only for an error rate of 1/2. To make a fair appraisal of overall undetected error rates, we need a much more sophisticated analysis which relates the undetected error rate to the raw error rate. Suitable codes exist which allow correction and detection of errors down to very low undetected error rates [5.19]. The application of these codes to jamming situations requires further study to determine the overall performance benefits.

5.5.5 Network Timing Control

The packet data communications approach outlined is quite versatile and could be extended in the future to allow for the implementation of a network timing control center which we dicuss briefly.

An adaptive timing distribution technique, such as TRD, results in the formation of a timing tree, as depicted in Figure 5.27 by means of dotted lines between nodes. The tree may change in structure if the network is stressed, but eventually one clock in the network assumes the role of master (unless the network is severed into separate entities, of course).

It is certainly desirable to have a centralized facility which is capable of monitoring and perhaps interrogating the network timing distribution system. We have shown this facility in Figure 5.27 as the Network Controller. There is an equivalent "tree" for data transfers to this node, as shown by the heavy lines joining nodes in Figure 5.27. Design of a suitable communications networking scheme to satisfy this requirement is similar in nature to the design of commercial packet switching networks. In fact, the thrust toward packet switching has been motivated by the same issues that appear here: high reliability despite the failure of individual nodes, backup control centers, and traffic flow management. We refer the reader to some papers on the subject [5.14] - [5.18] which, although primarily for commercial applications, are certainly relevant here.

The packets we refer to are to be interpreted as the controller information data area depicted in Figure 5.26. This unit of information, which is distributed at a network level by means of a switching procedure at each node, should not be confused with the complete TRIP or SDLC frame. The TRIP is a vehicle for conveyance of the controller packet between one node and the next. Some information in the TRIP goes no further.

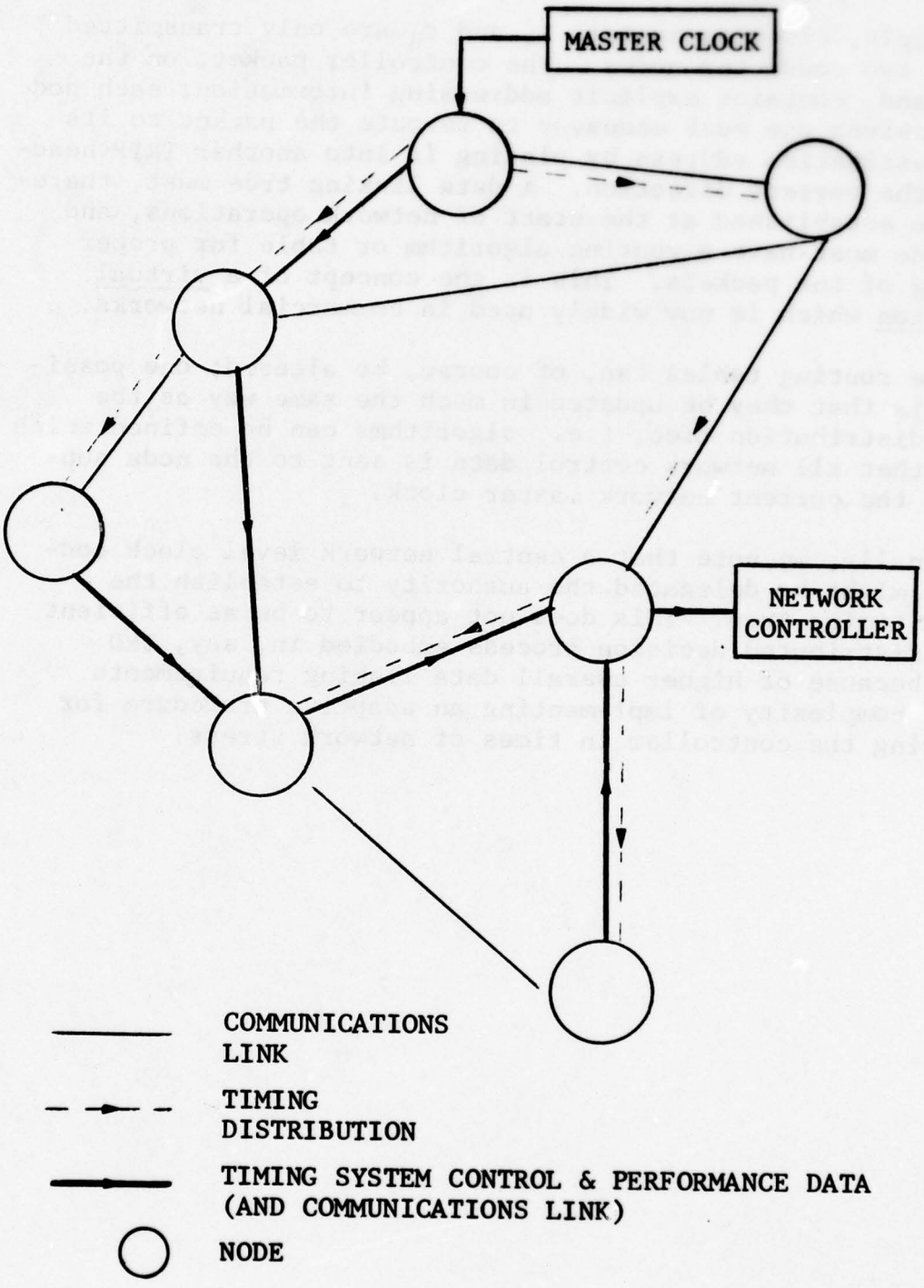


Figure 5.27 Timing and Timing System Control Data Flow in a Network

For example, clock parameters t'_A and t_B are only transmitted between two connected nodes. The controller packet, on the other hand, contains explicit addressing information; each node that receives one must endeavor to reroute the packet to its final destination address by placing it into another TRIP heading in the correct direction. A data linking tree must, therefore, be established at the start of network operations, and each node must have a routing algorithm or table for proper handling of the packets. This is the concept of a virtual connection which is now widely used in commercial networks.

The routing tables can, of course, be altered; one possibility is that they be updated in much the same way as the timing distribution tree, i.e., algorithms can be defined which ensure that all network control data is sent to the node supporting the current network master clock.

Finally, we note that a central network level clock controller might be delegated the authority to establish the network timing tree. This does not appear to be as efficient as the distributed decision process embodied in, say, TRD mainly because of higher overall data linking requirements and the complexity of implementing an adaptive procedure for relocating the controller in times of network stress.

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SECTION 6

CONCLUSIONS AND RECOMMENDATIONS

In this final section we summarize our conclusions and recommendations for future development of the DCS timing subsystem based on the analysis and experimentation carried out in this program.

It should be stated at this point that many of the important system decisions must be made by examining the behavior of a large-scale model of the network. For example, we are in a position to discuss the relative merits of different techniques, such as master/slave, TRD, and mutual synchronization, but the comparison must be carried out primarily at the link level. In the material which follows, we assume that any of the above synchronization techniques might be used in one form or another as part of the final network synchronization scheme. However, where appropriate, we attempt to highlight their differences in terms of cost, performance, or implementation difficulty.

6.1 Network Synchronization Candidates

We first define what we consider to be the four candidate techniques.

(1) Time Reference Distribution (TRD)

In this case we mean the accepted DCA definition of TRD, which includes precise time coordination of clocks, adaptive reorganization of the network timing tree, and use of a clock control data link to provide a means of resolving ambiguities and transferring clock parameters.

(2) Self-Organizing Relative Time Transfer (SORTT)

This concept is equivalent to master/slave with the added feature that the network is capable of reorganizing itself. The level of network synchronization is equivalent to relative time transfer only; hence, nodes do not exchange precise time-of-day data.

A control data link must be provided though to allow clock rank parameter transfers between nodes.

(3) Mutual Synchroni.ation (MSYNC)

With this technique all valid timing references at a node are weighted together to form the clock control signal. To allow for double-ended control, a data link must be available. Once again we are interested in relative time synchronization between nodes.

(4) Independent Clocks (IC)

The independent clock technique does not require the control data channel that is necessary for the other three. Its basic simplicity is balanced by the higher cost associated with the stable frequency standard which is needed.

In the above form, all of the synchronization candidates have the common attribute of survivability. This is recognizable as a critical feature for a military network, and one that is lacking in the usual concept of master/slave synchronization. By adding the self-organizing features to the master/slave approach, we are able to make a fairer comparison.

With the above definitions we can make the following brief comments:

- TRD and SORTT differ only in that one provides precise time coordination while the other allows only relative time synchronization. TRD incurs additional costs in equipment design modifications to control delay variations. These costs must be traded off against the universal time distribution advantages it offers.
- The MSYNC approach offers very little over the SORTT technique, against which it can be compared directly because it offers the same operational features of relative time synchronization and survivability. MSYNC does have the distinction of allowing clock coordination without the use of a clock data channel. However, this apparent advantage must be qualified; the final steady-state network operating frequency will be dependent on link delays for a

single-ended system unless a single node clock in the system acts as master. This is achieved by eliminating its mutual coupling with neighboring nodes. Thus, to ensure operation of the network clocks at a predetermined frequency, it is necessary to provide a master, and survivability requirements may then dictate the ability to select one of several network clocks as a master via a telemetry channel. Alternatively, a double-ended system must be implemented which also requires data link facilities. The potential cost savings over SORTT for a single-ended implementation of MSYNC (which does not use a clock data channel) must therefore be weighed against the problems of network instability and frequency uncertainty which arise.

- The independent clock technique appears to have been relegated to candidate of last resort because of the undesirable buffer resetting requirements. Therefore, it is not seriously considered as a candidate in this discussion.

It would be very satisfying if an endorsement could be given at this point to one or other of the candidates above. However, it is not realistic to do so; the best we can offer is Table 6-1 which summarizes the main cost and performance attributes of the different choices. The reason we can go no further is that certain key cost elements require more complete design information concerning the FRC-163 radio than is available at this point. Also, the cost of retrofit or redesign of the service channel multiplexer can only be determined from the circuit schematics. These areas pertain to the choice between TRD and SORTT. The remaining factor is the cost of the time interval measurement device which must be significantly more complicated when precise time transfers are involved. We have estimated the incremental cost of this device as being around $3 - 5K in production quantities of less than 100; obviously, the cost variability for the choice of station standard is more significant. In our comparison of the three primary choices (TRD, SORTT, and MS), we can see very few differential cost factors except the frequency standard and time interval counter (or phase detector); note, however, that we assume research and development costs are not relevant. This viewpoint follows from the realization that funds have already been committed for

TABLE 6-1

NETWORK SYNCHRONIZATION TECHNIQUE COMPARISON

	Time Reference Distribution TRD	Self-Organizing Relative Time Transfer SORTT	Single-Ended Mutual Sync MSYNC	Independent Clock IC
Candidate Comparisons	Cost vs. universal time dissemination			
		Cost of data link vs. stability		
		IC compared with both relative time techniques		
Cost Factors	Retrofit or redesign of service channel MUX Precision time interval counter In-service link calibration and alignment			Cost of atomic standards
Positive Performance Factors	Distribution of a universal time reference		May not require clock control data channel	No data channel required
Negative Performance Factors			Instability and lack of operational frequency control	Buffer resets are necessary

timing subsystem R&D activities, thereby covering most of the development costs for all four candidate techniques. The exception, albeit an important one, is the cost of including design changes into existing DCS equipment. This cost component is of particular significance for the TRD technique, but virtually negligible for the relative time synchronization candidates.

Table 6-1 summarizes the points that we have made in this subsection. For the purposes of comparison, we have implicitly used the SORTT as a reference concept for the cost and performance base. The entries in the table are therefore considered to be advantages and disadvantages relative to this technique.

We now proceed to give an overview of the more specific findings resulting from this program.

6.2 General Timing Subsystem Design Constraints

Consider first the general structure of the time distribution scheme we have described in the body of this report.

We have taken as the designated node reference signal the 1 pps derived from a phase-shifted frequency standard, and the reader is reminded that the network time synchronization objective is the alignment of all such 1-pps references throughout the system. In master/slave and mutual sync approaches, the relative variation of the 1 pps after buffer reset is the important consideration. That is, absolute phase or time relationships are unimportant throughout the network, but accumulated phase variations in the 1-pps signal are indicative of buffer fullness variations, and controlling one will control the other if the station clock frequencies all originate from the corrected station standard.

The data required in the clock control loop processor will depend on the synchronization techniques selected but, as a general rule, it will consist of time measurements from the other end of the link (t_A' and t_B) as well as time measurements made locally (t_A and t_B'). The parameters in question are:

t'_A = node A transmitted TRIP* relative to node A reference

t_B = received node B TRIP relative to node A reference

t'_B = node B transmitted TRIP relative to node B reference

t_A = received node A TRIP relative to node B reference

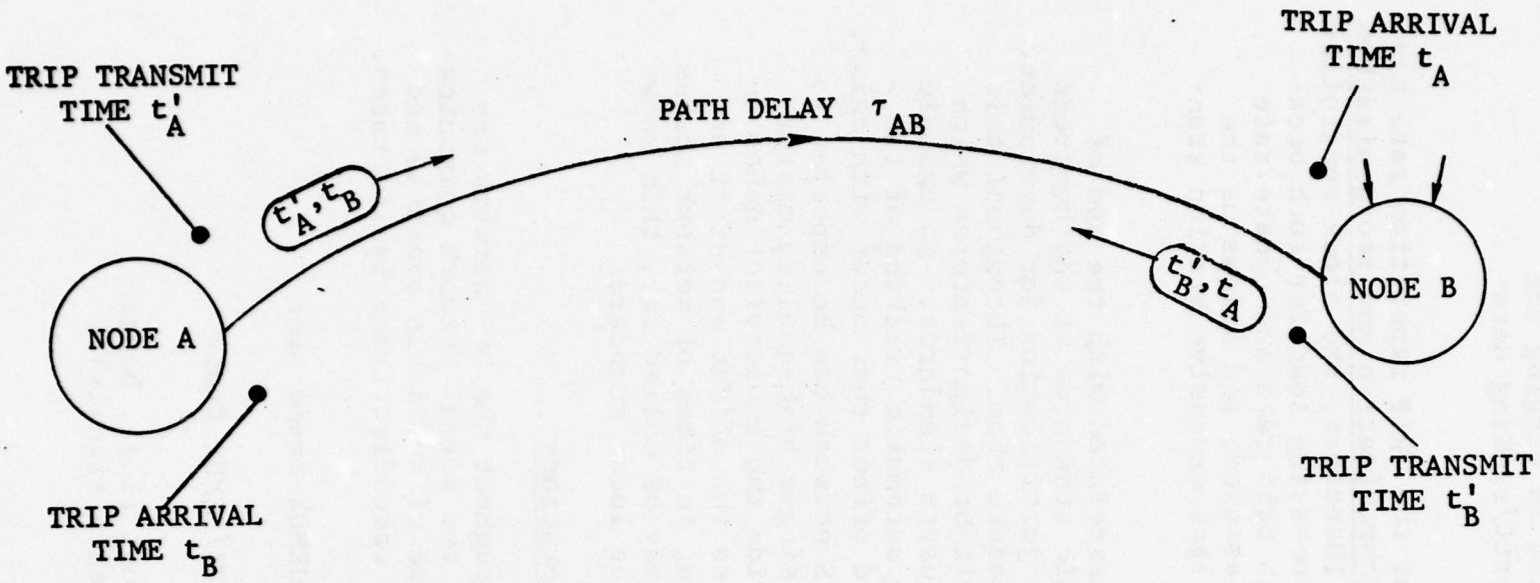
All parameters listed are to be interpreted as elapsed time measurements. Figure 6.1 attempts to depict the relationships between the TRIP data packets and the actual elapsed time measurements above.

The rationale behind our selection of the 1-per-second TRIP repetition rate is not easily stated. The choice is one of convenience tempered by the desired to keep the overall processing as simple as possible. We do note, however, that there are definite disadvantages to the use of slower repetition rates. The main issues can be summarized as follows:

- With the requirement for time-of-day transfers between nodes, a 1-per-second TRIP transmission on the second is convenient.
- The chosen TRIP rate will be suitable for all classes of clocks envisaged for use in the DCS network, i.e., clock update rates as high as 1 per second are feasible.
- Once a design has been established for 1-per-second TRIP's, there is no valid reason for updating the node clocks at a slower rate provided the node processor can handle the computation burden. Long-time constants can still be implemented even if the update rate remains at 1 per second.
- Fast TRIP repetition and clock update times are essential for rapid acquisition convergence and satisfactory tracking transient response.

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*TRIP (Time Reference Information Pulse), a conceptual pulse burst having one of several forms, which is used to convey timing and data between nodes.



TRIP ARRIVAL TIME AT B (RELATIVE TO A) $= t'_A - t_A + \tau_{AB}$

TRIP ARRIVAL TIME AT A (RELATIVE TO B) $= t'_B - t_B + \tau_{BA}$

CLOCK ERROR (EQUAL DELAYS) $u = \frac{1}{2}(t'_A - t_A - t'_B + t_B)$

$=$ CLOCK A - CLOCK B (START TO STOP TIME)

PATH DELAY $\tau_{AB} = \frac{1}{2}\left[(t_A + t_B) - (t'_A + t'_B)\right]$ ASSUMING $\tau_{AB} = \tau_{BA}$

Figure 6.1 Clock Error and Path Delay Calculations for Time Reference Distribution

- Fast TRIP times are of benefit in purging the network of unwanted clock merit/ranking data in the adaptive techniques.

In short, it can be seen that the TRIP repetition rate has a strong influence on network synchronization and reorganization performance in times of stress. Therefore, the clock controller must be designed to handle the processing load for such occasions. Operation at the same high data rate and update rate during quiescent periods is then assured, and allows us the option of using lower stability, less expensive station standards at minor nodes.

The potential cost savings associated with the use of quartz standards in place of atomic standards at the hundreds of less significant nodes provide justification for development of the timing subsystem to accommodate them. Throughout this report we have endeavored to highlight design features which will enhance the performance of quartz standards. An example is the attention we have given to automatic tracking of the local standard frequency drift and offset that occur with aging. It should be realized that the DCS network can be expected to run for very long periods with a single high-quality master standard, and such intervals provide the subservient nodes an opportunity to qualitatively assess the offset and drift of their own station standards. Then, in times of network stress when independent clock operation may be called for, this knowledge can be used to compensate the local standard.

6.3 Equipment Interfacing Considerations

The distribution of time throughout the DCS network can most readily be superimposed onto the normal network communications functions by taking advantage of available overhead and monitoring signals built into the specified transmission rates. Some candidate signals include:

(1) Level-1 or level-2 MUX/DEMUX frame sync patterns

(2) Radio (i.e., level-3) MUX/DEMUX frame sync patterns

(3) The system service channel (i.e., burst or pulse types of reference signals)

While these particular signals have received a great deal of attention as candidate time reference signals, the choice is not clear-cut by any means, and it is only after a very thorough examination of DCS equipment characteristics that a suitable selection can be made.

We shall refer frequently to a hypothetical timing reference pulse (TRP) which, in general, will be transmitted out of a node via all connecting links. Its precise form will be specified after a complete review of the alternatives, some of which are listed above. Note that we wish to retain a distinction between TRIP's and the TRP's; in most cases, the TRIP's alone will not provide enough accuracy for our application. This will become clearer as we proceed.

We should first state some general guiding principles and conclusions:

- For precise unambiguous transfers, the maximum possible bandwidth should be utilized. With digital systems, this implies that particular bits should be tagged in the highest rate accessible bit stream. The reasons for this are subtle but well-documented in this report (see Section 5.1.2 and Appendices A and B).
- Lower level bit streams may be used to carry the TRP's, e.g., level-1 and level-2 TDM frame markers. However, extensive design precautions must be taken in the development of these units and the radio level TDM to achieve this capability. Such precautions are not normal design practice as evidenced by the 600-ns delay uncertainty measured recently for the MDTS troposcatter digital modem (see Appendix A).
- It is not feasible to transfer time markers through the service channel alone. Even with the full telemetry bit rate of 56 kb/s (available from the 1192 as a service channel TDM), delay uncertainties of tens of microseconds are experienced (see Appendix B).
- If the periodic TRP transmissions are implemented by means of unmodified TDM frame markers, ambiguities result. These ambiguities cannot be resolved by simultaneous service channel transmissions unless loose time delay specifications

are met for the service channel. We do not believe that the present service channel concept will satisfy this requirement without extensive modifications.

- The level at which TRP signals are extracted also influences the data buffer placement level. That is, the buffer must be at a lower level than the TRP level (e.g., buffers at the level-1 1192 DEMUX outputs when the 1192 frame pattern is used for a TRP).

These equipment delay anomalies are attributable to the internal synthesizer and data buffer arrangements. Normal design techniques do not guard against the possibility of delay uncertainties finer than a single bit. However, in our case we require delay uncertainties to be below the 100-ns level. Unfortunately, these delay variations are not readily averaged out; the multiplexer delay is variable with a new constant value established each time the equipment is taken out and put back into service.

We have concluded that TRP transfers via the level-1 or level-2 TDM frame sync patterns seriously compromise the link time distribution accuracy and make the systemwide goal of 2 μs virtually impossible to meet without extensive TDM circuit modifications. Three other alternatives have been studied in detail (see Section 5.1.2). The options are:

Option A: Radio Sync Pattern Detection (Section 5.1.2.1)

Option B: Radio Sync Pattern with Service Channel Ambiguity Resolution (Section 5.1.2.2)

Option C: Service Channel Data and Time Transfer (Section 5.1.2.3)

Figure 6.2 represents the block diagram of a simplex link showing interfaces of DCS radios and service channel TDM with the timing subsystem. We will attempt to clarify the complex interaction shown by explaining the philosophy behind each of the three options above.

For option A, direct access to the frame sync pattern at the transmit level-3 multiplexer is assumed. The technique involves modification or encoding of these sync bits (of which there are 16 placed contiguously at the start of each 250-μs frame); one very simple approach is to simply invert them.

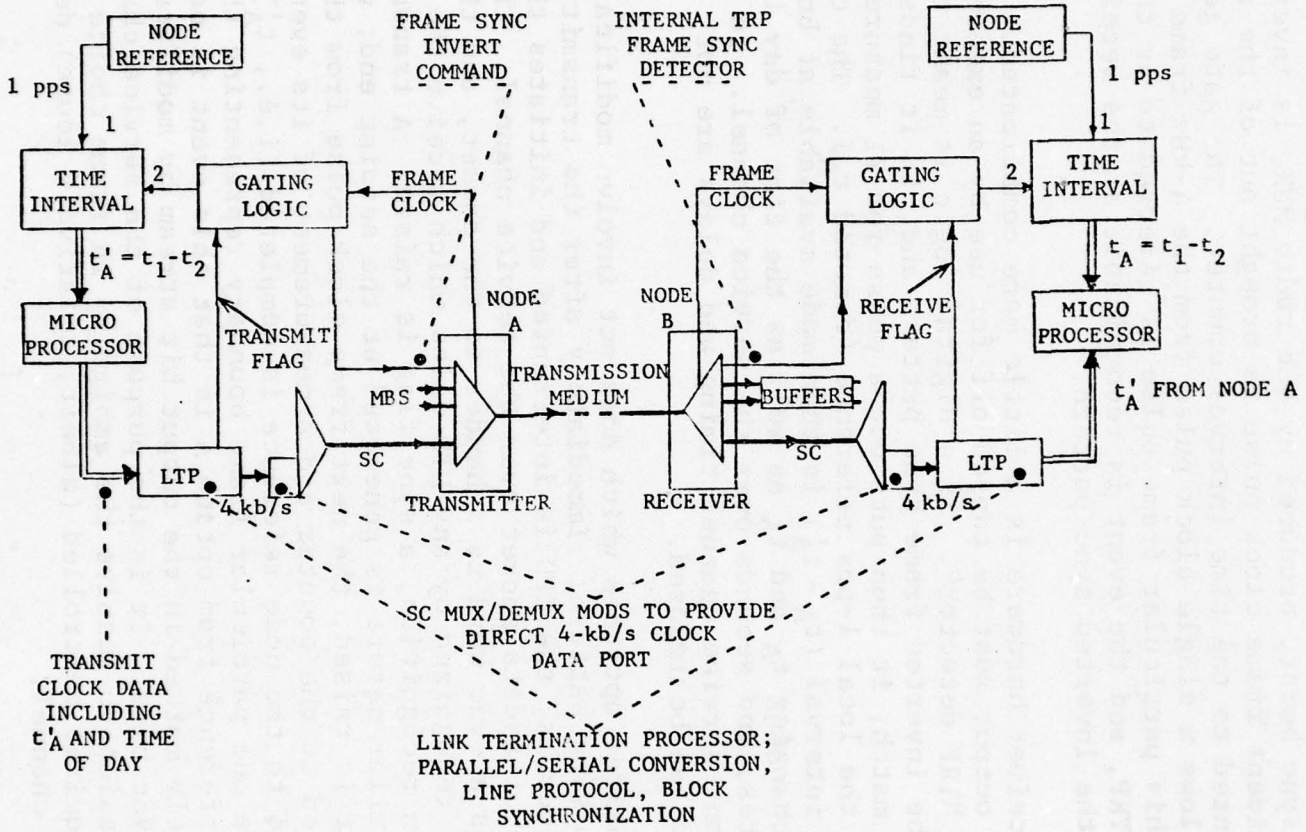


Figure 6.2 Block Diagram of Timing Subsystem and DCS Interfaces

Thus, when the node reference 1-pps pulse appears, a frame sync code inversion command is issued by the gate generator. The next frame sync burst, produced by the radio MUX, is inverted and a coincident frame clock pulse is brought out of the radio to be presented to the time interval counter. The gate generator only allows a single clock pulse from the 4-kHz frame clock to pass. This particular frame pulse is referred to as the designated TRP, and the event is recognizable at the receiver because of the inverted sync pattern.

The receiver hardware is a little more complicated. The demodulator output must be tapped off for use by an external or internal "TRP detector". This digital logic is meant to recognize the inverted frame sync pattern and, if it finds a 16-bit code match, it then puts out a pulse for TI measurement relative to the local 1-pps reference (denoted t_A). The composite time interval ($t_A - t_A'$) is then made available at both nodes by exchanging t_A and t_A' as well as the time of day in hours, minutes, and seconds over the service channel. In this configuration, service channel timing and delays are not critical and can be ignored.

Now consider option B which does not involve modification of the radio sync pattern. Immediately after the transmit node 1-pps pulse occurs, the CPU is interrupted and initiates the transmission of a data packet over the service channel. The LTP generates a sync word as a header to the packet, and this word will be recognized by any LTP units which receive the data string. Upon recognition, a sync flag is raised. A transmit flag of a similar nature is generated at the sending end; when the sync flag is raised, the next frame clock pulse from the radio is gated to the counter and a measurement of its event time relative to the node reference is completed (i.e., t_A'). Thus, we have one particular frame boundary representing the TRP. The difference from option A is that this event is no longer uniquely marked in the output bit stream by modification of level-3 sync bits. It is the purpose of the service channel data transmission to resolve the ambiguity in frame choice and, to do so, requires controlled (albeit, relatively loose) delay through this channel.

At the receiving node, the arrival of data through the service channel is indicated by the LTP sync flag. A gate is generated from this flag to allow the next frame pulse to be extracted from the radio and sent to the TI unit for comparison with the node reference. Unfortunately, this will not be the

frame marker designated as the TRP because of excess delay imposed by the service channel chain. With the aid of tabulated equipment delays, correction by a whole number of frame periods can be made to the measured quantity t_A.

There will, however, be time delay uncertainty associated with the arrival of data transmitted through the telemetry portion of the service channel. In Section 5.1.2, we have listed some of the potential uncertainties, and while these particular values are barely tolerable, our need for another level of service channel multiplexing down to, say 8 kb/s, introduces far worse delay uncertainty, perhaps in excess of one bit interval (125 μs). Obviously, delay uncertainty in the data link should be much less than one radio frame interval (250 μs) if an unambiguous TRP transmission is to be made.

Fortunately, the service channel access can be designed with existing equipment modified to hold down the delay uncertainties to an acceptable level. The proposed method is described in Section 3 of Appendix B. Stated briefly, it suggests a modification to the 1192 TDM to allow direct 4-kb/s clock data access via bit 8 of the telemetry channel byte, thereby locking the 4-kHz timing signals to the 1192 frame boundary and eliminating the potential delay uncertainty alluded to above. Of course, the delay budget given in Section 5.1.2 still applies, but overall the delay uncertainty is a small fraction of the 250-μs radio frame.

In conclusion, it should be mentioned that the data packet transmitted from node A to node B will contain the measured parameters t_A' and t_A from the previous 1-second interval, along with the time-of-day data.

Option C, which looks deceptively simple, is actually doomed to failure without quite massive equipment modifications. For precise time transfer, it would seen that the 1192 TDM must be rejected outright as a candidate for the service channel multiplexing tasks, mainly because of unsuitable clock synthesis techniques and serious FIFO buffer reset uncertainties (see Appendix B). At the very least, the service channel multiplexer would need to be custom-designed to meet the time transfer requirements, and the digital radio synthesizers and FIFO's would have to be subjected to stringent specifications (see Appendix A).

Based on the discussion presented in Section 5 and Appendices A and B, we are in a position to offer specific subsystem design recommendations.

The important conclusions reached may be summarized as follows:

- For precise time transfer, the subsystem architecture and interfacing presented as option A is the most straightforward, although it requires access to several signal lines within the radios. Depending on the D3 sync monitoring circuit design however, the interfacing could be trivial; specifically, internal sync circuitry may be amenable to changes which would encompass the inverted sync detection functions. Similarly, the difficulty of frame sync code inversion at the transmitter must be examined when detailed M3 schematics become available.
- If the radio interfaces for option A prove to be too difficult, the approach outlined under option B is available. Since options A and B differ in their external hardware in only minor ways, a decision between the two can be deferred until more is known about the radio design. With option B processing, service channel delay characteristics must be controlled within certain limits. If the 1192 TDM is used in the service channel MUX application, it must be modified or adapted for use as outlined in Section 3 of Appendix B. This modification is necessary to satisfy the low data rate budgeted for clock control while keeping the total delay uncertainties to within a few microseconds, thereby allowing ambiguity resolution of the higher resolution timing events.
- Partitioning of the telemetry channel has been tentatively fixed such that clock control data transmissions are apportioned a dedicated 4-kb/s slice of the total capacity (< 64 kb/s). The actual data rate requirements are considerably less. For option B, the important concern is that of delay uncertainty, and it is this aspect that has dictated the above data rate rather than the volume of traffic. With option A, division of the telemetry channel is of less concern, and the allocated clock control capacity could be as low as 400 b/s.

- If it becomes evident that radio interfacing for option A is not trivial and that the 1192 cannot be modified in the way described in Appendix B to suit option B requirements, then a custom design for the service channel TDM will be necessary.

The timing subsystem interfacing arrangements shown in block diagram form in Figure 6.2 indicate quite explicitly the optional radio and TDM interfaces which may be used (to implement either option A or option B). A final choice can only be made after discussions with the radio vendor.

6.4 Data Buffer Design and Placement

We are concerned here with the buffering capability to be provided by the timing subsystem prototype. The buffers in question are primarily of use for protection against timing transients which may occur in a system with coordinated clocks or, more likely, to take up the differences in data transmitted between nodes when independent clocks are set up in the network.

Present technology allows buffers for level 2 (up to 13 Mb/s) to be built at only a marginally higher cost than buffers for level 1 or below. Above about 1K bits of storage, there is virtually no cost differential and, more important, the incremental cost of adding storage beyond this value is quite small compared with the initial cost of control circuitry.

Given that there are no significant cost constraints, we can therefore explore other issues that may influence the placement decision.

- When buffering is carried out at one of the lower levels, all upstream equipment must be clocked from the recovered modem clock which will exhibit jitter and other medium effects (e.g., frequency offset for satellites). To avoid the presence of this jitter in equipment, it must be placed on the downstream side of the buffer.
- At some stations, switching and combining of data streams from several remote sources must be achieved. This can only be done with synchronously clocked data, implying that the data must have already passed through a buffer by the time it is presented for combining. For example, if digroups (1.544 Mb/s) with different geographical origins

are to be combined at a level-2 MUX, they must have been subjected to buffering either at level 2 or at level 1.

- At the output of the radio, we have an opportunity to buffer data in such a way that resets correspond to the deletion or insertion of an integer number of level-1 and level-2 frames. We dismiss the possibility of extending this concept to lower level submultiplexers because of the increased storage requirements. However, the possible avoidance of level-1/level-2 TDM resynchronization is in itself appealing enough, particularly when a major portion of the traffic is PCM voice. In terms of the effects on voice channels, the objective is to reduce the resetting operation to the loss of, at most, two PCM samples for each voice channel passing through the buffer.
- To successfully attempt such a strategy, it is necessary to know the TDM frame format, and to examine the consequences of implementing multiple frame resets with buffers at different levels. For example, at level 2, a jump by a whole level-2 TDM frame may not throw that DEMUX out-of-sync, but still not safeguard the level-1 DEMUX's. Alternatively, if the buffers are at level 1, such resets do not affect the level-2 DEMUX's in any way.
- The level-2 TDM rate specifications allow for input port strapping (i.e., output ports at the DEMUX); hence, the buffer design must accommodate various rates if it is to be used at level 1. This is rather awkward when one considers that the total number of bits of storage required at a level-2 DEMUX output is invariant regardless of the division of the total MBS bit rate into various ports rates, strapped or otherwise. Obviously, the designer is forced to develop an 8-port flexible buffer unit with programmable rate structure (and movable storage boundaries), or he must design for the worst-case rate (i.e., maximum) and develop eight identical buffers to satisfy the worst-case number of ports. These design issues give added weight to the selection of a level-2 buffer design.
- Other considerations mainly involve cost and reliability of a few large fast buffers vs. a larger

number of smaller slower buffers of comparable total capacity. A large buffer is probably cheaper than a number of smaller ones of similar total capacity, unless reliability requirements (MTBF is probably a function of size) or the high data rate required dictate a more expensive approach (either a different technology or more expensive components). The consequences of a failure of a large buffer are more serious than those of a failure in one of a number of smaller buffers which might be used instead.

A suggested buffer size of 2048 bits was determined on the basis of a minimum size requirement (see Section 5.1.3) for independent clock operation without reset over a period of 50 days.* Beyond that, the size may be easily increased; but, if the buffers become too large, reliability becomes an issue.

An attractive possible application for relatively large buffers is the preservation of multiplexer synchronization during buffer reset. If buffer capacity exceeds the length of the framing pattern (e.g., superframe or super-superframe), when it gets nearly full, its fullness can be decreased in one jump by a number of bits equal to the framing pattern length. We have examined a buffer design to include this feature. If the TDM 1193 superframe needs to be preserved, the total buffer size must be in excess of 25 Kbits, and the step resets must be a corresponding magnitude. It would appear, however, that the 1193 superframe carries only pulse stuffing information, which will not be relevant in a synchronous network. Obviously, it is necessary to have additional information concerning the 1193 frame format to pursue the design further.

6.5 Clock Control Algorithms

We are mainly concerned here with the status and functional behavior of the clock control loop in different operational circumstances.

Four principal modes of operation can be defined:

(1) Startup. When the network is first initialized for time synchronization of clocks, a special step-by-step startup phase will probably be required (similarly, for addition of new nodes

*Assuming a relative clock offset of 2×10^{-11}. With an offset of 10^{-8}, this becomes 2.2 hours.

to the network). For two nodes, A and B, we would classify operation as "startup" if the difference between the node clocks in in excess of 5 μs.

(2) Acquisition. This category applies when the clock errors are large enough so that normal control loop servo design principles would not give fast enough convergence speed, and yet the more disruptive "startup" response is neither necessary nor desirable. In terms of clock error between the reference and the slave clocks, the dividing line has been set at 5 μs for a maximum error (beyond which the startup mode is entered) and 60 ns as the smallest error. For errors less than this value, the tracking mode is entered.

(3) Tracking. This is the normal mode of operation, and involves use of standard servo design methods to keep the steady-state clock phase close to the selected reference.

(4) Coast Mode. This applies only when no suitable reference is available and arrangements must be made to extrapolate future clock controls from past history.

The startup phase can be completed in a matter of seconds if the master node is stable; then the acquisition phase begins and could take up to 50 seconds to complete. Finally, there will be a small transient associated with entry into the tracking mode, the duration of which depends on the selected loop constants.

The clock control components are presented in block diagram form in Figure 6.3. It is shown as a digital system; the low bandwidths of interest here rule out the possibility of an analog implementation because of drift and offset problems that would arise.

The fundamental function performed by the control loop is the generation of a set of reference frequencies, derived from the 5-MHz "node reference", to avoid buffer overflow or depletion. We will distinguish between the unperturbed standard output, referred to as the station standard, and the phase-shifted version of this signal, referred to as the node reference. The phase stepper shown in Figure 6.3 performs the

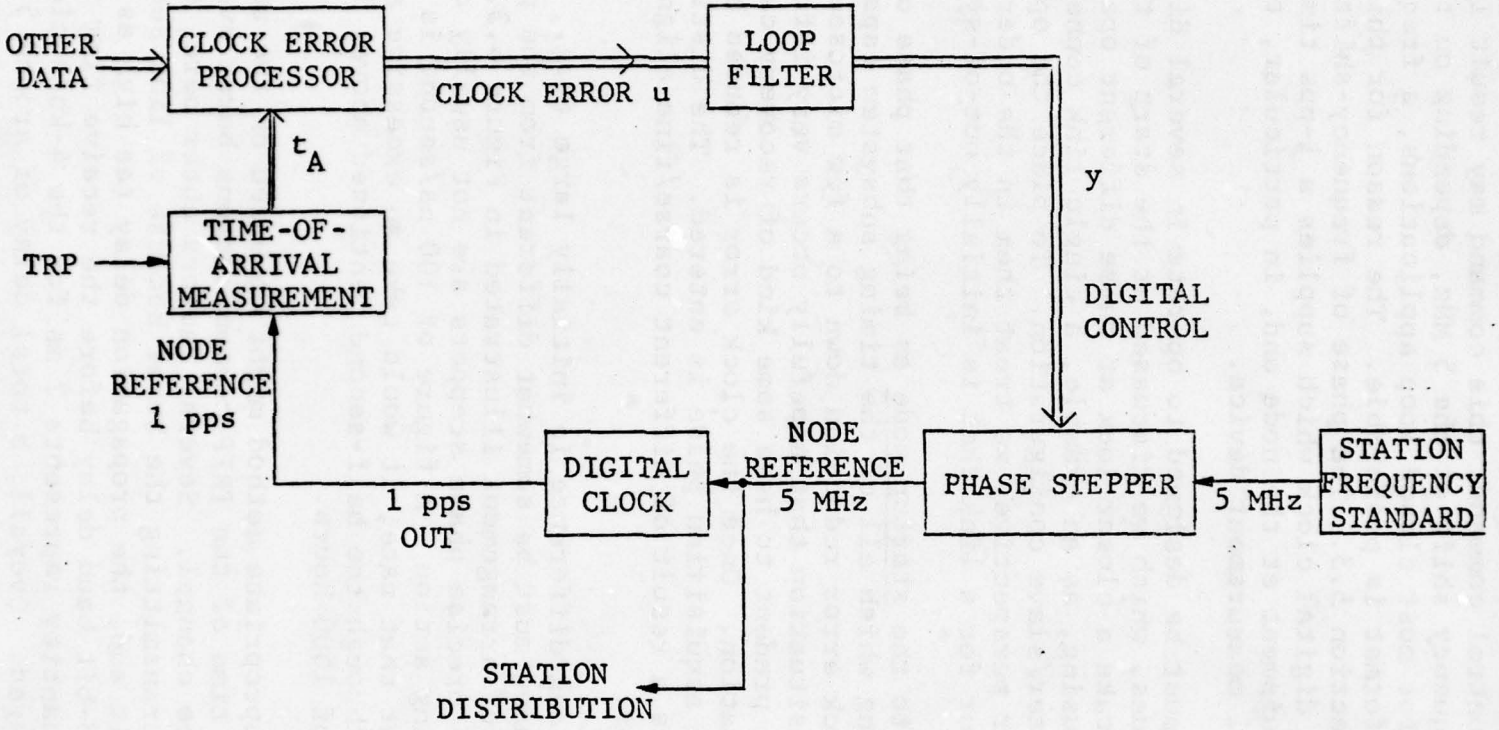


Figure 6.3 Basic Time Reference Control Loop

function of phase shifting the 5-MHz node standard in response to a digital control command; this command may result in either a phase or frequency shift of the 5 MHz, depending on the mode setting; but, for most closed loop applications, a frequency shift command format is preferable. The reason for this is explained in Section 5.3. The phase of frequency-shifted output then goes to a digital clock which supplies a 1-pps time reference to all equipment at the node and, in particular, to the time-of-arrival measurement device.

The loop must be designed to operate in several different operational modes, which we discussed at the start of this section. We now take a closer look at these different operational circumstances using, as an example, a single link connecting two nodes in a master/slave configuration. To place the operational modes in better perspective, we treat them in the order in which they would occur for a link that is initially out-of-sync.

We refer to the startup mode as being that phase of clock alignment during which all of the timing subsystem capacity is devoted to clock error reduction down to a few microseconds, i.e., it is a situation that hopefully occurs very infrequently; however, it is prudent to have some kind of recovery capability in such a situation. Once the clock error is reduced below, say, 5 μs, the acquisition phase is entered. The distinction is primarily as a result of different coarse/fine alignment implementations.

If the clock difference is initially large (e.g., 0.5 s), the approach used must be somewhat different from the phase stepping kind of arrangement illustrated in Figure 6.3. The reason is that precise phase steppers are not usually capable of fast stepping action. A figure of 100 ns/second is perhaps typical and, at that rate, it would take an excessive amount of time to step through the half-second mentioned above; in fact, on the order of 1000 hours.

A more appropriate method might be based on the uncompensated arrival time of the TRIP communications burst available via the service channel. Several factors enter here, though: the delay in transmitting the burst because of link sequencing at the transmit end, the propagation delay (as high as several ms), and the 8-bit baud delay before the receive flag is set. This latter quantity represents 2 ms for the 4-kb/s clock data channel envisaged. Overall, a total delay of around 5 ms could be experienced in the time between the master 1 pps and the raising of the data received flag in the LTP's. At 100 ns/s,

this is still equivalent to a wait of 10 hours before the clocks are aligned. Much faster startup clock alignment is possible, as we have demonstrated in Section 5.3.2.

The reference to acquisition in this context concerns the strategy used to rapidly reduce any moderate phase or time errors between the master and slave clocks. Once acquisition has been completed, the tracking algorithm is initiated, and normal closed loop servo action proceeds (as described in Section 5.3.4) until such time as the clock phase error becomes excessive and the acquisition mode is again reentered. This might occur when a new time reference is selected, for example, or when a node clock is being brought back into service.

It would seem that a suitable acquisition strategy can be formulated directly from standard servo principles using wide closed loop bandwidths to achieve fast response times. This method, which involves switching of the loop time constants, is not the preferred acquisition approach for reasons to be explained. In summary, we can state the following:

- Switching of loop parameters to give a larger resultant bandwidth does not provide the most rapid reduction in clock error.
- If the switched parameter approach is used, special precautions must be taken to initialize the control loop state at the switching point in order to avoid severe overshoot problems in the tracking mode.
- Coordination between several node clock controllers, all attempting acquisition, is complicated by this approach.

These ideas will be clarified in the discussion which follows.

It must first be recognized that commercially-available phase-stepping units are optimized for small phase change increments and are usually limited to some maximum slew rate. For any initial clock error, the fastest way of reducing the phase different to zero is by commanding the unit to step in-phase at this rate. This results in a linear reduction in error with time, as shown in Figure 6.4, where the clock error u is reduced uniformly until the threshold region is reached.* When

*Figure 6.4 is a plot of clock error measured in the clock control demonstration field tests. The maximum microstepper rate was 100 ns/s.

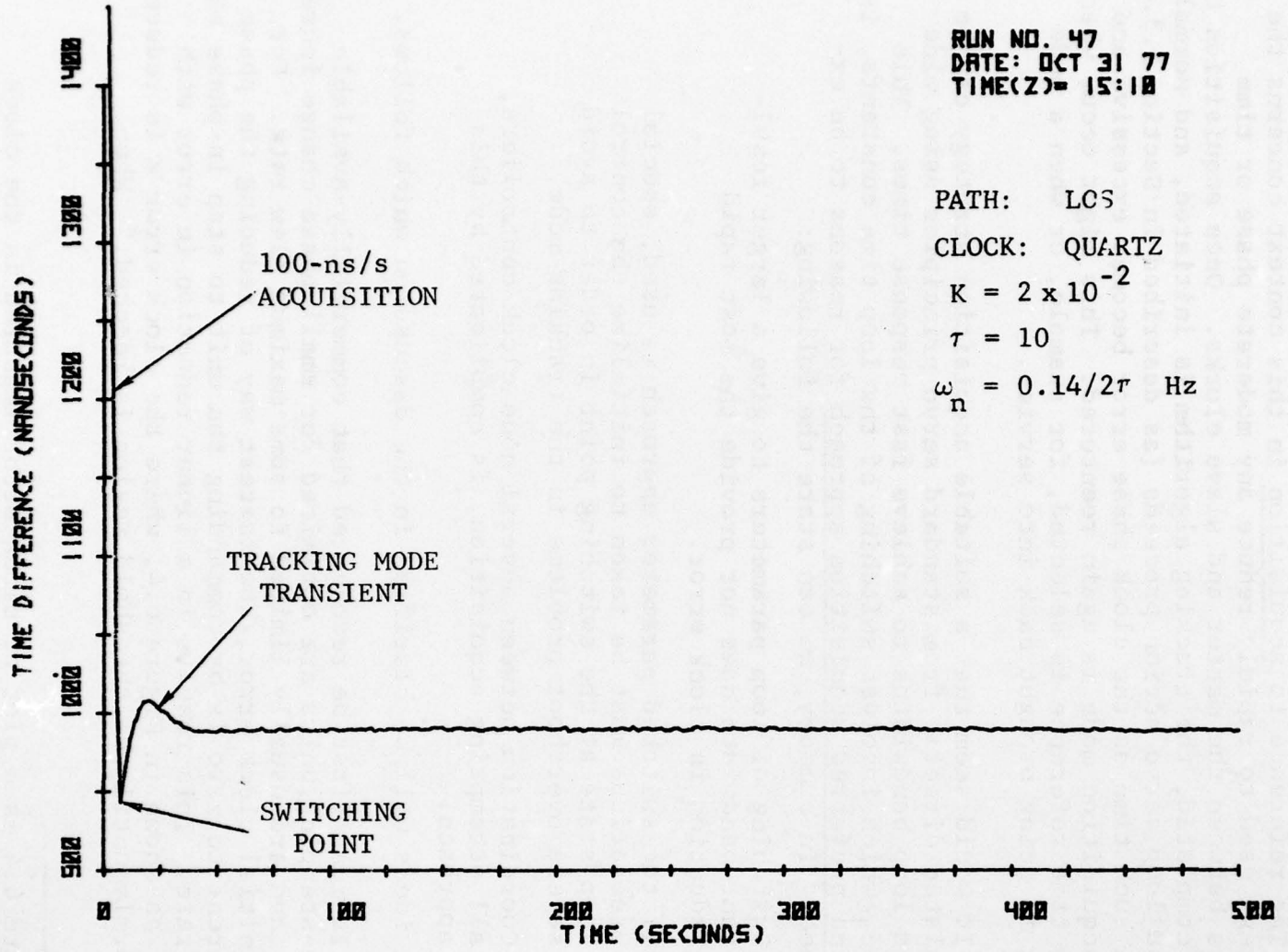


Figure 6.4 Acquisition and Transient Behavior for a 75-Mile LOS Master/Slave Time Transfer Experiment (Closed Loop Bandwidth = 0.14 rad/s)

$$|u| < a$$

a switch to tracking mode is made. The following observations are important however:

- The update repetition rate will influence the maximum size of the threshold region, i.e., the maximum value of a. With 1-second measurement updates as proposed, and a slew rate of 100 ns/s, 2a must be less than 100 ns; otherwise, it is possible for the trajectory to pass completely through the transition region without switching to acquisition. Of course, the trajectory would reverse direction on the next update, but undesirable hunting behavior would be experienced with excessive error fluctuations.
- The threshold band should be made as narrow as possible to minimize the transient which inevitably occurs in the tracking mode. The ideal clock error at the time of switching is zero, although switching at <u>that</u> point may not, in itself, be enough to completely eliminate the transient because of differences between the master and slave rest frequencies (see Section 5.3.4).
- Noisy measurements or, equivalently, timing jitter compound the difficulties. Obviously, when the system is in the acquisition mode and slewing the clock at, say, 100 ns/s, no averaging of any significance can be carried out on the measured clock error data. With TROPO links, the short-term jitter can be significant and certainly comparable with otherwise reasonable choices of threshold size.

The outcome is that convergence time is not easily predicted when jitter is present and discrete time measurements are being processed. The best that can be done is to match the slew rate, update rate, and threshold selection to the rms jitter.

Figure 6.4 shows the plot of clock error for a quartz clock (with virtually zero frequency offset) slaved to a cesium standard via a 75-mile LOS link cascade. The servo error was biased off by 1000 ns to avoid measurement difficulties peculiar to the counters available in the region near zero time differential. The clock error was initially in excess of 1 μs, but only the last 400-ns portion of the acquisition trajectory was plotted. The convergence rate is 100 ns/s in this phase, so that rapid reduction in clock error was experienced.

The important considerations for the tracking mode of operation are simply the following:

- Noise reduction by selection of suitable loop filter gains and time constants to give a narrow closed loop bandwidth.
- Selection of parameters to optimize rise times and overshoots resulting from minor transient effects.
- Steady-state tracking of fixed frequency offsets and frequency trends relative to the station standard characteristics.

The last item dictates the number of perfect integrators in the open loop transfer function. For example, it is easily shown that quartz standards, which exhibit both a frequency offset and a drift in frequency, require two perfect integrators in the servo open loop transfer function.

Our field experience at RADC has convinced us that the most significant tracking mode design issue is the rise time optimization, particularly for situations where frequency offset reference signals are switched into the loop. As we show in Section 5.3.4, the magnitude of the transient phase overshoot is proportional to the amount of the frequency offset and inversely proportional to the closed loop bandwidth.

When attempts are made to lock together two clocks having a frequency offset, transient responses of the form shown in Figure 5.17 are generated. Note that even with a frequency offset of 3×10^{-8}, reasonable transient performance was obtained. The consequences of selecting narrower loop bandwidths are, however, manifest as increasing error peaks when locking up to a clock offset in frequency.

Generally, the transition from acquisition to tracking will involve a master and slave clock that are offset in both time and frequency. The transient behavior will then be a combination of the effects demonstrated because of the system linearity and recourse to superposition principles.

The coast mode applies when no reference is available to a node because of link or clock outages. Furthermore, there are times when a node is required to reference itself, e.g., while reference selection information is propagating through a network for the TRD technique. To avoid the so-called "obsolete data

problem", a node may have to coast for a period of time rather than immediately selecting a new reference.

Provided the accumulated clock control information is used correctly, this should be a satisfactory mode of operation even with lower quality quartz clocks. The assumption must of course be made that the network was previously stable and that the drift and offset data available are valid.

6.6 Clock Data Design

Reliability for the clock control data link is paramount. It is quite obvious that the data being transferred between nodes is highly intolerant of errors; the adaptive reorganization merit and ranking parameters, for example, must be carefully protected to eliminate the possibility of inadvertent network reconfiguration.

The task of designing the data link is complicated even further by the following considerations:

- Error patterns observed on the links will tend to be burst-like as a result of channel fading, particularly for TROPO and LOS systems.
- Although the DCS specifications call for quite low error rates (e.g., 5×10^{-9} for LOS, 5×10^{-5} for TROPO, 99.99% of the time), data link integrity is even more important during periods of jamming when the error rates will be much higher. Therefore, a high tolerance to errors is necessary.

From these statements we can glean some important guidelines which apply to our data link design. Briefly, there are certain data items that must be delivered with virtually zero error probability or, as an alternative, not at all; i.e., gaps in the clock updating procedure are preferable to the use of invalid data. Then it must be accepted that, during times of stress, the raw bit error rate may be quite high (e.g., approaching 0.5). These two facets of the data communications design task are rather ominous considering the narrow range of options they leave open.

The necessity of achieving close to zero error probability strongly suggests that a dependable error detection scheme is mandatory; error correction is of limited value, although it may be useful in bolstering the effective data transfer rate. The

use of several data modes is also advocated. We can exploit the fact that in a heavy jamming situation only the more essential data need be conveyed between nodes. Thus, we should contemplate a backup low data rate mode of operation. The unused capacity would then serve to enhance the reliability of the remaining data bits by allowing additional redundancy.

The preceding paragraph suggests that the principle of operation for the data link should be based on automatic repeat request procedures (ARQ), with a very low residual undetected error rate by judicious choice of parity check code.

In this program we examined the use of the bit-oriented Synchronous Data Link Control (SDLC) protocol for the clock data link, which includes a 16-bit (CCITT) cyclic redundancy check. This will give more than adequate performance for all links satisfying the DCS specifications. However, it is apparent that additional forward error correction (FEC) capabilities will be required between the SDLC line controller and the service channel multiplexer to maintain good performance during periods of jamming when the error rate will be quite high.

A full investigation of the requirements for such a unit must be made during the timing subsystem design phases. Three key topics can be itemized at this point:

- Delay through the FEC must be carefully controlled if the clock data channel is being used to convey node time, as in option B of Section 5.1.2.2.
- With the channel data rate tentatively selected as 4 kb/s, and an information rate that is on the order of 300 b/s, there is significant redundant channel capacity available for use by the coding scheme.
- Contingency plans can be formulated for minimizing the data transfer requirements during jamming situations. Such a reduction will allow the use of even lower rate codes in the FEC application.

For all of the three options discussed at length in Section 5.1, the demands on the network service channel gravitated toward a dedicated 4-kb/s subchannel. The reasons for this are the following:

- The full system digital telemetry channel data rate is not needed by the clock control system and is shared with other network control functions on the basis of time-division multiple access or synchronous time-division multiplexing. The latter is recommended.
- Although a high data rate is not necessary, equipment delay uncertainties can be a problem if a simple sub-MUX approach is used.
- With option B, the clock data link must be fully synchronized with the service channel MUX/DEMUX. This requirement narrows the choice in such a way that 4 kb/s is the most obvious choice of clock data rate (see Appendix B). For the service channel modifications suggested, the full 56-kb/s system telemetry channel is preserved, and the additional 4-kb/s clock data channel is derived from what would have been wasted capacity.

The basic data transferred between nodes can be summarized as follows:

Node Status - sync and overflow condition flags for radios and buffers; also, loop mode, e.g., acquisition and tracking.

Transmit Time (t_A') - measured time of previous outgoing TRP signal relative to 1 pps.

Receive Time (t_B) - measured time of previous incoming TRP signal relative to 1 pps.

Clock Error (u_A) - current estimate of clock error.

TRD Rank and Merit Parameters - TRD decision parameters N_1, N_2, N_3, N_4.

Second Count - time in seconds at last 1-pps tic at transmit mode.

The number of bits allowed for each of these parameter fields is given in Section 5.5.3. The standard SDLC control address, flag, and frame check fields are included also. Except for the controller message area which will be described shortly, the total count comes to 214 bits.

The remaining packet capacity is allocated to exchange of network level commands and performance parameters. In addition, provision has been made for transmission of date and time of day resolved down to 1 minute; this would be transmitted only on the minute boundaries in order to conserve space in the 1-second data transmissions.

Finally, we mention that all time/date variables should be transmitted as 7-bit ASCII. Other parameters will consist of single bit flags, addresses (8-bit bytes), or floating point variables (32 bits plus 8-bit mantissa extension). With a TRIP length of 300 bits and data rate of 4 kb/s, the total transmission time will be on the order of 75 ms.

6.7 Medium Path Length Considerations

Substantial effort went into the measurement of medium delay variability for TROPO and LOS links. Although there were not too many surprises in the resulting data, it should be emphasized that many other important issues were examined and analyzed in the support of these experiments; the critical evaluation of equipment characteristics has brought forward some particularly valuable results, and, overall, the major role of the field program has been one of developing keenness of insight into time transfer problems. We have reported in this document many facets of the time transfer and system integration tasks that would not have been uncovered without the stimulus of a field testing effort.

Addressing ourselves more directly now to the results of the medium parameter tests, we can present the following conclusions:

- Path length variation for LOS links is relatively unimportant; according to our rather modest data set, it is limited to about $\pm 10^{-5}$ variation around the nominal path length. The principal effect is considered to be refractivity changes with corresponding variations in the speed of propagation. A single-ended time transfer system with a time constant of a few minutes would suffice. Data buffering requirements amount to less than 1 bit over normal length links.

- For TROPO links, there is considerable timing jitter in the recovered clock. This has an influence on acquisition performance. When the timing reference is averaged over periods of 10 minutes or more, the long-term path length variations are left. This latter category exhibits swings of $\pm$ 200 ns over periods of several hours.
- Reciprocity of the TROPO paths is not likely on an instantaneous basis. However, with the short-term fluctuations averaged out, forward and return links are expected to have the same delay down to the 20-ns level. This was confirmed by the results of our TROPO path length measurements, at least for a nondiversity configuration.
- Single-ended time transfer is not viable for TROPO links unless long time constants are used (e.g., several days) and stable frequency standards are available at both ends of the link. With very long time constants, the tracking loop transient behavior becomes more severe in terms of overshoots, particularly when two clocks offset in frequency are being synchronized.

Finally, we should comment on the merits of different types of frequency standards and their performance when used with TROPO and LOS links. Although time constants of several hours or more are normally recommended for atomic standards, there appears to be no particular advantage to such long averaging times for LOS links. In fact, there appears to be no fundamental argument against the use of quartz standards on most, or all, of the LOS links during normal operational periods. If node clocks must run in the independent clock mode, then the long-term stability does become important, but this appears to be the only real factor against quartz standards. For TROPO links, longer time constants are necessary to smooth out medium variability. A time constant of an hour or so is quite adequate for double-ended systems, and quartz clocks would be expected to function satisfactorily. However, for a single-ended TROPO path, a time constant of a day or two is necessary; this, in turn, necessitates the use of atomic standards at the connected nodes.

APPENDIX A

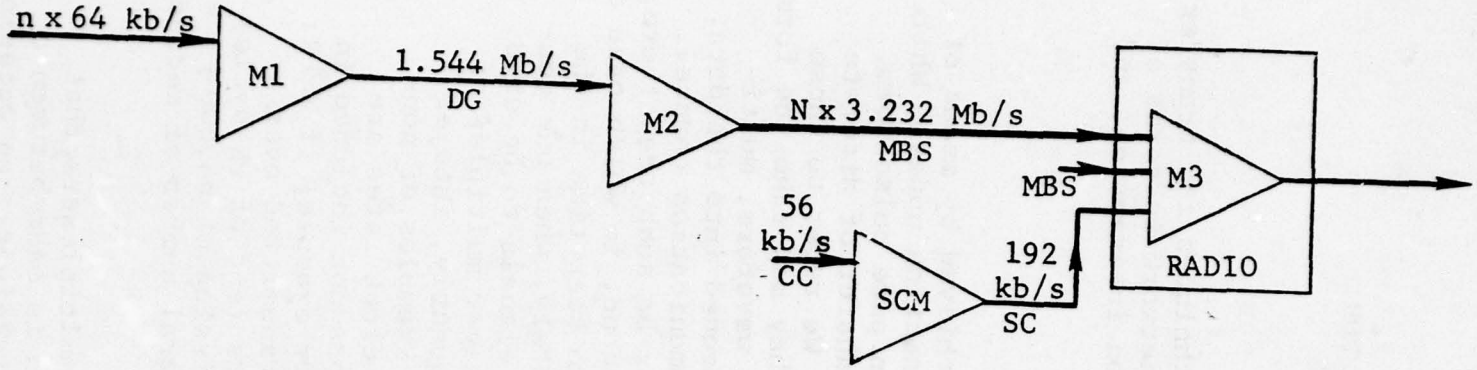
ANALYSIS OF DELAY UNCERTAINTY FOR DCS RADIOS AND MULTIPLEXERS

Here we examine several alternative techniques for transfer of time between different nodes in the DCS network in terms of time transfer accuracy, TDM resynchronization interaction, and implementation difficulty.

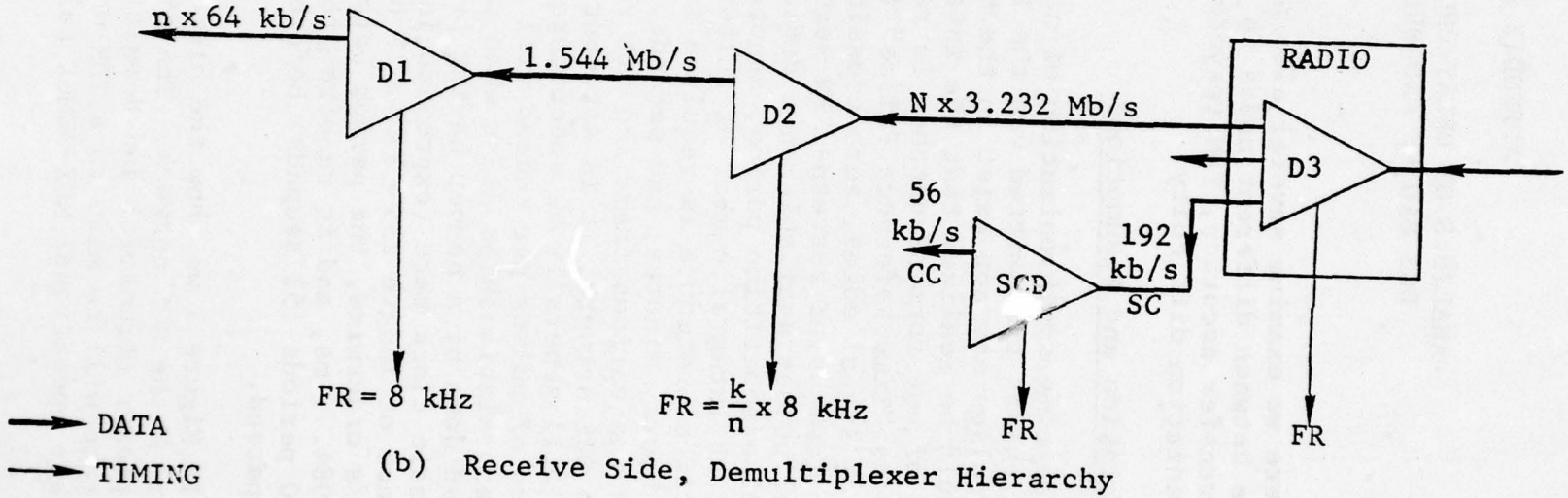
A1. Notation and Assumptions

The time synchronization of nodes is achieved by means of timing pulses transmitted via the links connecting nodes. While these pulses may not exist in the network in pure pulse form, it should be realized that the internode transfer of discrete events of one form or another is required. We refer to these pulses as "Time Reference Pulses" (TRP). They may take the form of clock signal edges, zero crossings for a waveform, multiplexer frame sync patterns, PN sequences encoded into the data, or real pulses available on a dedicated communication channel. The pulse repetition period, denoted T_p, may be such that there is not an integral number of pulses in a second, in which case a conversion procedure is required in order to keep time in the usual hours, minutes, and seconds. Fortunately, when one considers the various frame and bit rates for signals to be used in the DCS network, it is apparent that integer multiples of 8 kHz will generally be encountered; consequently, integer numbers of pulses per second will result. Examples of non-integer relationships arise when the basic clock rates are divided down by a number having prime factors not included in the basic clock rate (expressed in Hz). For example, if a PN sequence of length $255 = 3 \times 5 \times 17$ bits is transmitted over a 64-kb/s orderwire, the period between events (end of PN cycle) is 3.984... ms, and it requires the transmission of $64{,}000 \div 5 = 12{,}800$ periods (51 seconds) before an integral number of seconds have passed.

In Figure 1 we show the hierarchy of multiplexers that appears in the DCS network. The distinction is made between a multiplexer (transmit) and demultiplexer (receiver); on occasion, reference will be made to a TDM which is intended to mean a complete operational MUX-DEMUX pair. The various bit rates



(a) Transmit Side, Multiplexer Hierarchy



(b) Receive Side, Demultiplexer Hierarchy

Figure 1 DCS Multiplexer Hierarchy Showing Frame Rates

shown in Figure 1 are derived from DCS standards published to date. However, certain rates (in particular, the radio transmit/receive rate) and the level-2, level-3, and service channel frame rates have not been finalized at this time. Table 1 summarizes the nomenclature which will be used throughout this discussion.

A2. Time Reference Transfer: DCS Equipment Considerations

The purpose of a time reference transmission is to provide a comparison between the transmit clock at the remote end of a link and the local or node clock. In its most basic form, the TRP transmission must be structured as in Figure 2, with an event triggered by the remote clock, transmission over the link, and comparison at the local node. Because the TRP transmission will be periodic, some variation of the pulse format might be implemented to remove the ambiguity; e.g., hours, minutes, seconds markers could be included in some way. For the moment we pass over this consideration and examine ways of transmitting the elementary pulses.

There are three possible approaches that come to mind:

(1) Use of the TDM frame markers.

(2) Transmission of a time reference signal via the control channel.

(3) Implementation of an auxiliary analog channel dedicated to the transfer of timing pulses, e.g., subcarrier modulation.

Of these, the third does not appear feasible within the current state of DCS network development, so we limit our attention to the other two.

A2.1 Time Transfer via TDM Frame Sync

It can be seen from Figure 1 that at least four different multiplexer frame rates will exist in the system. Some of these will be more accessible and useful than others, however. After we have presented some of the salient features for a scheme involving the level-3 or radio multiplexing, the remaining choices can be handled with little further elaboration.

A few general comments are in order regarding the use of frame sync bits for time reference transfer between nodes. First, it should be stated that the timing event, which we have

TABLE 1

GLOSSARY OF NETWORK TERMS

SC	Digital Service Channel	192 kb/s
RBS	Radio Bit Stream	(2 x MBS + OH) Mb/s
MBS	Level-2 Bit Stream	n x 3.232 Mb/s
FR	Frame Rate	
CC	Control Channel	56 kb/s
NTD	Node Clock Timing Distribution	
RTD	Receive Clock Timing Distribution	
DG	Digital Group	1.544 Mb/s
TRP	Time Reference Pulse	
TASS	Timing and Sync Subsystem	
FIFO	First-in First-out Data Buffer	
SYN	Frame Synchronizer	
SCM	Service Channel Multiplexer	
SCD	Service Channel Demultiplixer	
M3	Level-3 (Radio) Multiplexer	
D3	Level-3 (Radio) Demultiplexer	
M2	Level-2 Multiplexer	
D2	Level-2 Demultiplexer	
M1	Level-1 Multiplexer	
D1	Level-1 Demultiplexer	
SM	Subrate Multiplexer	
SD	Subrate Demultiplexer	
OW	Orderwire	
TDM	Time-Division Multiplexer (MUX/DEMUX)	
OH	Overhead Bit Stream (e.g., service channel pulse framing bits)	

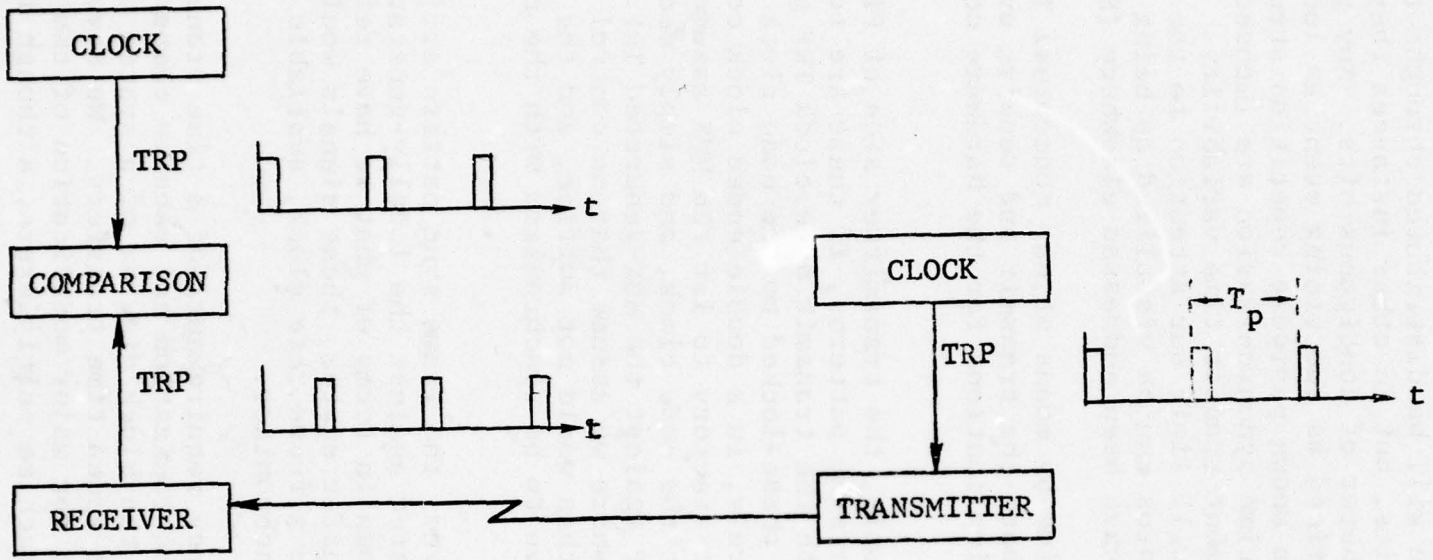


Figure 2 Basic Elements of a Time Reference Transmission

generally referred to in terms of the conceptual time reference pulse (TRP) must be associated with the transmission and reception of one edge of a single bit in the frame sync sequence. Often the sync sequence will be distributed throughout hundreds or thousands of data bits, but in other instances they will be bunched together in a burst of contiguous bits. Any point in the sequence can be defined as the timing event as long as it is measurable and has a known periodic repetition structure. Fundamental limits on time synchronization are imposed by both medium and radio equipment transit time variability. However, in this discussion we will limit our attention to the equipment effects so that the radios can be visualized as being back-to-back. Medium effects have been addressed elsewhere (Section 4).

The transfer of time by means of our conceptual TRP's requires knowledge of both the transmit and receive events, and in turn there are implications for the hardware configuration complexity.

Consider, for example, the transmitter side of Figure 2. The generation of frame sync patterns, if these are to be used, must be coordinated with the transmit node clock TRP generation, e.g., the MUX could be phase-locked to the node clock at the frame rate. Alternatively, in a double-ended clock control system, it would be satisfactory to let the MUX assume an arbitrary phase relative to the node clock, and simply measure the transmit node clock TRP against the MUX-generated TRP. With single-ended systems, where we assume that no control data link exists between nodes, this would not suffice, and the MUX-generated TRP would have to be synchronized with the node time reference.

At the receiving end, the frame sync pattern arrival must be registered and compared against the locally-generated event. In Figure 2 this is shown in terms of what we have referred to as TRP's; in a TDM transfer system, these signals would be basically equivalent to a frame rate clock, available from the demultiplexer frame synchronizer.

To summarize the key requirements of a time transfer system, i.e., transmit synchronization and receive comparison, we have shown in Figure 3 the block diagram of a system capable of single-ended and double-ended time transfers. We have purposely avoided any requirement for major modification of the standard equipment components, such as multiplexers, although it is clear

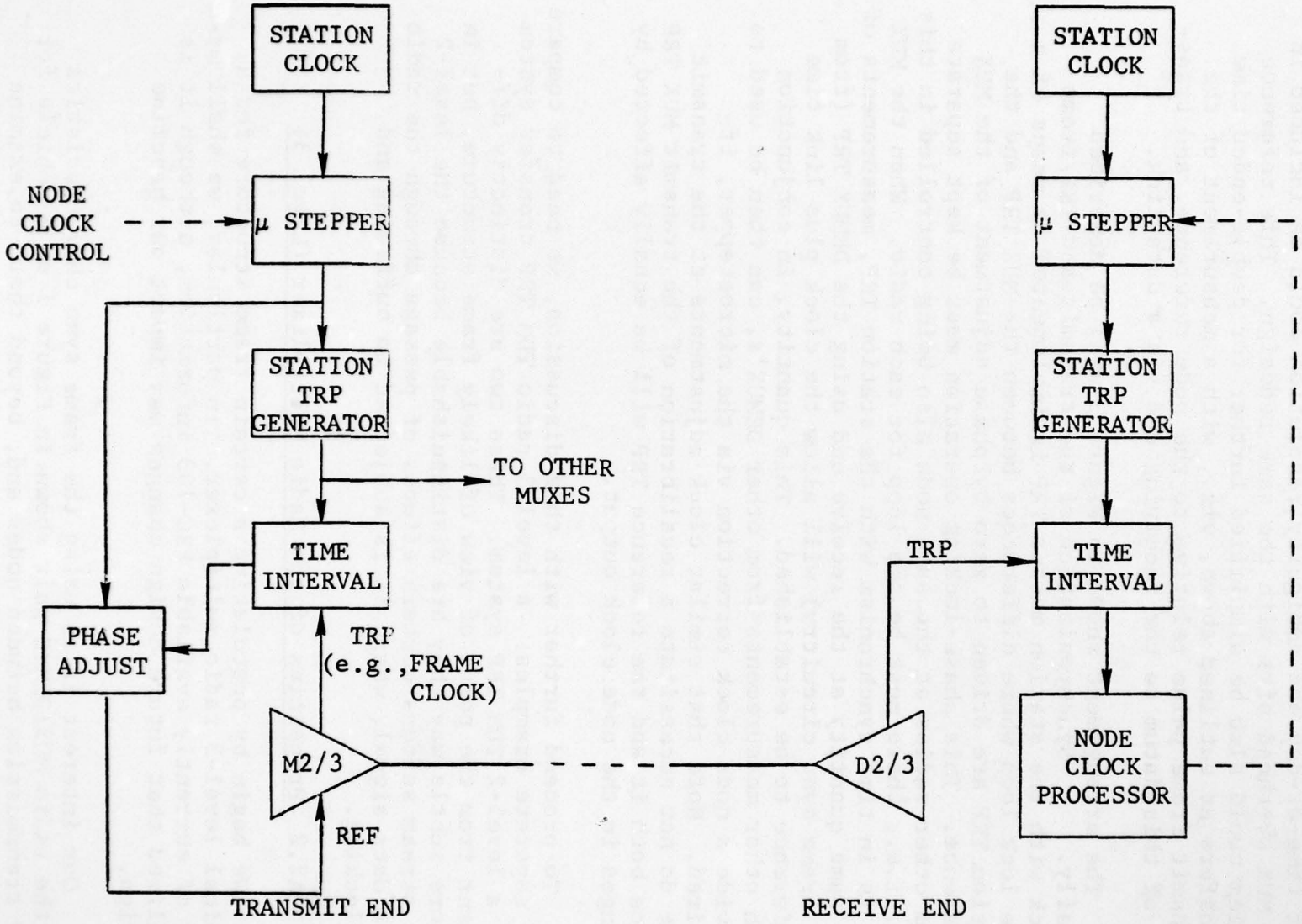


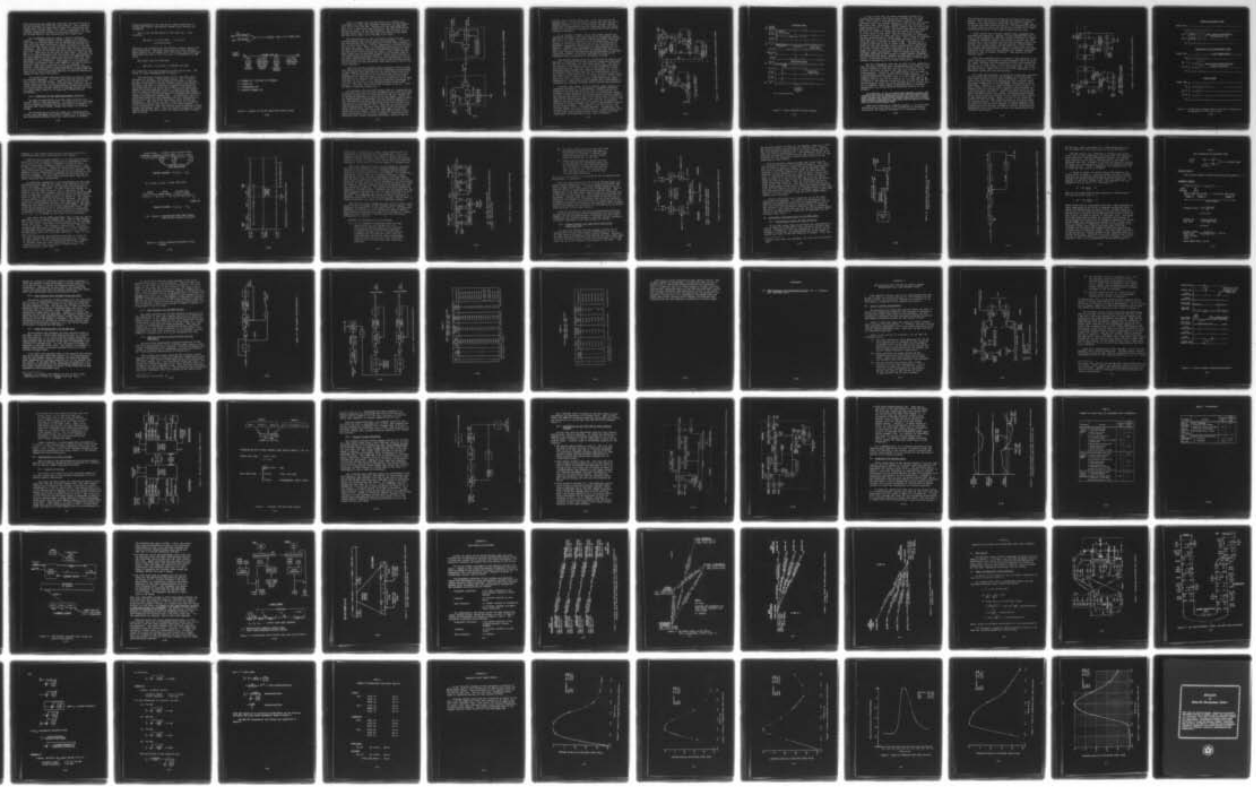
Figure 3 TDM Frame Sync Timing Transfer Block Diagram

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SYSTEM TIMING AND SYNCHRONIZATION.(U)
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that time-of-day and ambiguity resolution could be included in the MUX overhead bits with the same redesign. This reference system could also be simplified further for double-ended time transfers as outlined above, viz., with a measurement of the transmit frame pulse relative to the node reference, and transfer of this datum to the receiving end via a data link.

The arrangement shown in Figure 3 will be described briefly. Synchronization of the transmit and TRP/frame clock with the station master TRP is implemented by means of a time lock loop where differences between the MUX TRP and the station TRP are driven to zero by phase adjustment of the MUX reference. This phase-locking operation must be kept separate from other radios at the same node also being controlled in this way, i.e., there must be one loop for each radio. When the MUX TRP is in time synchronism with the station TRP, measurements of the same quantity at the receive end using the DEMUX TRP (from its frame sync circuitry) will allow the clock plus link time difference to be established. This quantity, in conjunction with other measurements from other DEMUX's, can then be used to provide a node clock correction via the microstepper, if desired. Note that similar clock adjustments at the transmit node do not necessitate a recalibration of the transmit MUX TRP since both it and the reference TRP will be equally affected by changes in the node clock output.

To proceed further with this discussion, we need to compare two separate examples: a level-3 radio TDM TRP transfer system and a level-2 TDM TRP system. These two are distinctly different from the point of view of likely frame structure, but in a more subtle way they are distinguishable because the level-2 bit stream suffers certain effects of passage through the radio as a data signal, where it is subjected to buffering and reclocking.

A2.2 Properties of the Radio Multiplexer (Level 3)

We begin by postulating a certain frame structure for a typical level-3 radio multiplexer. In particular, we shall make use of currently available FRC-163 information, although it is realized that future design changes may impact our baseline design.

Our interest is in using the frame sync characteristics of the radio MUX/DEMUX pair shown in Figure 1 as a vehicle for TRP transmission between nodes and, beyond that, to examine

certain properties of the MBS and SC outputs which are of concern when level-2 and service channel time transfer are considered.

Each of the two MBS inputs to the radio has a rate structure:

$$\text{MBS rate} = n \times 3.232 \text{ Mb/s} \qquad n = 1,2,3,4$$
$$= 2n \times 202 \times 8 \text{ kb/s}$$

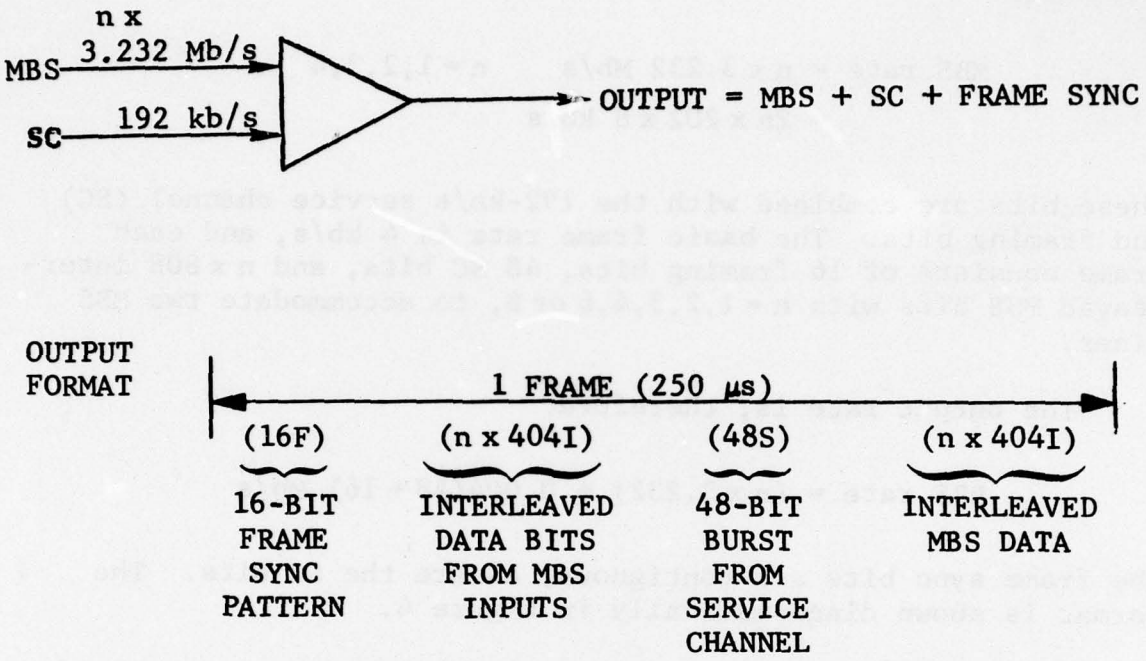
These bits are combined with the 192-kb/s service channel (SC) and framing bits. The basic frame rate is 4 kb/s, and each frame consists of 16 framing bits, 48 SC bits, and $n \times 808$ interleaved MBS bits with $n = 1,2,3,4,6$ or 8, to accommodate two MBS lines.

The output rate is, therefore:

$$\text{RBS rate} = (n \times 3.232) + 0.004(48 + 16) \text{ Mb/s}$$

The frame sync bits are contiguous, as are the SC bits. The format is shown diagramatically in Figure 4.

The functional characteristics of the radio MUX can be described as follows. Three data buffers, each of length 64 bits, are available for the MBS and SC inputs to the MUX. Because of the burst of service channel data in the middle of the frame, MBS data is subjected to timing fluctuations approaching ± 24 bits, so these FIFO buffers do not leave much margin for other buffering services. Because of the requirement for high availability, every radio has duplicate backup units, including a second MUX which is available with elaborate standby and switchover capabilities. In particular, the corresponding buffers in each redundant unit are synchronized to maintain the same fill level and, hence, delay through the transmitter. The buffers are set to half-full at a predetermined initialization time relative to the frame boundary. It is also necessary to align the transmit frame boundaries in both primary and standby units. This is achieved by means of control signals between the two to reset the frame countdown circuitry when necessary.



n = NUMBER OF 3.232-Mb/s BIT STREAMS

F = FRAME BIT

I = INFORMATION BIT

S = SERVICE CHANNEL BIT

Figure 4 Example of FRC-163 Radio MUX Output Format

Data is clocked into the MBS FIFO's at a uniform rate according to a clock rate generated internally or from another unit such as the 1193 MUX. Readout onto the high-speed RBS line is at a nonuniform rate provided by the RBS clock and the MBS output gates. At the demultiplexer, this activity is reversed; output FIFO's (64 bits each) are filled at the gated RBS rate and clocked out at the MBS or SC rates.

The demultiplexer is also required to search for the framing pattern, and acquire frame synchronization. To do this, the received RBS data is clocked into a 16-bit shift register and, at each clock time, a 16-bit comparison is carried out with the true sync word. When two successive frame words are found to match up perfectly, the sync confirmation flip-flop is set, and the master frame counters are reset. After frame acquisition, frame sync is monitored by means of an up-down count of incorrect-correct frame word matches. Frame count circuitry is not reset immediately after a loss of sync declaration, but is deferred until at least the first resync trial has been carried out to provide for the possibility that there was no loss of bit count integrity.

There are certain problems which may beset a level-2 frame sync timing system associated with the buffering and reclocking of data signals that take place in the third level radio multiplexer. For the purposes of illustrating this point, we have represented the radio in Figure 5 as it is seen by the data. Both MBS and SC data bits are subjected to buffering, as we have indicated by the FIFO's, to cover the variations in passage of data bits into and out of the transmitted bit stream (rate R_0 b/s). The input rate for the MBS is shown as R_1 b/s. (Only one MBS is shown for simplicity.)

Our interest lies with the transit time of a single MBS bit at the radio MUX input to reach the DEMUX output; this bit would represent perhaps one bit of the level-2 frame sync pattern and is therefore equivalent to one form of TRP signal. Timing for the demultiplexer is available from the incoming signal by means of a demodulator tracking loop, and some form of synthesizer must be used to develop the MBS output rate clock R_1' and a corresponding service channel clock. Note that in a back-to-back radio configuration the input data clock R_1 and the desired output data clock R_1' will be at the same rate, but may not necessarily be in phase. Moreover, they may not bear a fixed phase relationship for all time, although no change would be perceived under normal operating conditions, which we take to

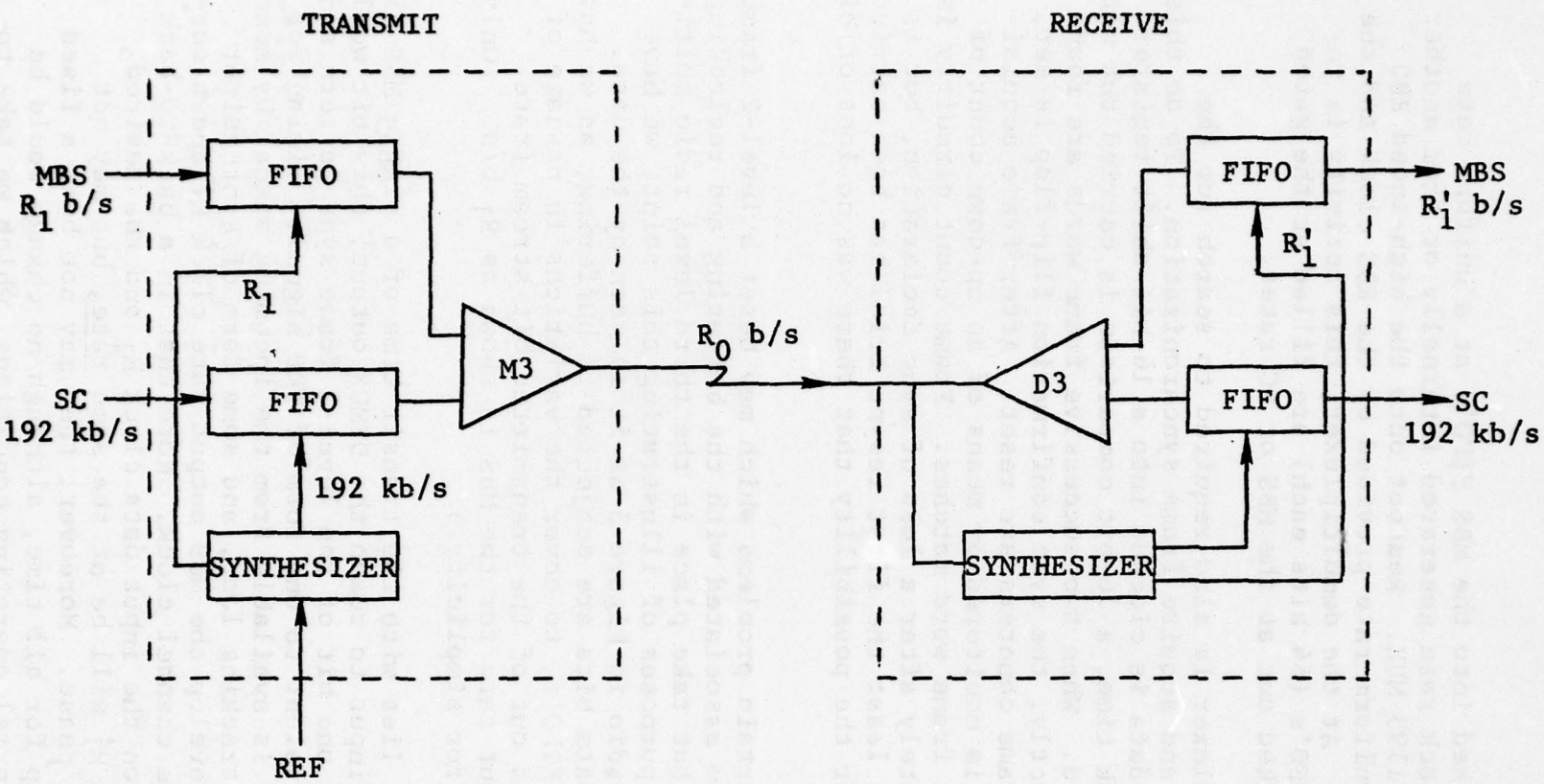


Figure 5 Buffer Organization in the Radio Level-3 MUX/DEMUX

exclude loss of level-3 frame sync or bit sync loss at the tracking loop. It is very easy to accept the fact that R_1' is delayed relative to R_1 by a fixed amount; however, greater difficulty is encountered with the conjecture that the delay could vary according to equipment initialization and synchronization conditions.

It is possible to show, albeit with rather lengthy and cumbersome arguments, that some choices of synthesizer design give rise to a delay uncertainty through the DEMUX amounting to one bit or one baud, depending on the configuration. We now attempt to illustrate this with the aid of the hypothetical MUX/DEMUX synthesizer scheme shown in block diagram form in Figure 6. Whether this arrangement is representative of the FRC-163 cannot be determined with information made public at this time. However, the approach <u>is</u> representative of the MDTS troposcatter modem, as has been confirmed by study of the schematics and a comprehensive measurement program.

The external timing signal at the MUX will be rate R_1, the MBS rate. From this clock, the transmit synthesizer generates the SC clock (192 kHz) and the output clock (R_0). The latter is produced by dividing R_1 down to 32 kHz and phase-locking a VCO running at R_0. This RBS clock is then passed to a gate generator which consists of a series of counters and decoders. It produces gates for the MBS, SC, and frame pattern bursts. The result, in the case of the MBS gate, is that a gated series of stable pulses, designated $\bar{R}_0$, is made available to the data FIFO, and used to clock in a burst of MBS data stored there temporarily. Frame reset at the transmit end is equivalent to resetting the counters contained within the MBS gate generator.

To assist the reader, an illustrative timing diagram is presented in Figure 7. It represents a somewhat simplified version of the real situation for ease of illustration, by assuming a frame length of only 19 bits into which are packed 11 bits of data and 8 bits of framing (service channel omitted). The external MUX clock at rate R_1 is divided down to 32 kb/s as shown by the second timing line, and from the VCO locked to this signal, the phase-locked loop (PLL) output R_0 is generated. Note that the figure assumes PLL counter initialization exactly at the frame boundary. This appears to be the case for the FRC-163 design, and is a logical approach. Furthermore, the transmit FIFO's are reset to half-full at a predetermined point in the frame upon initializing the radio, another necessary requirement for minimizing transit time uncertainty.

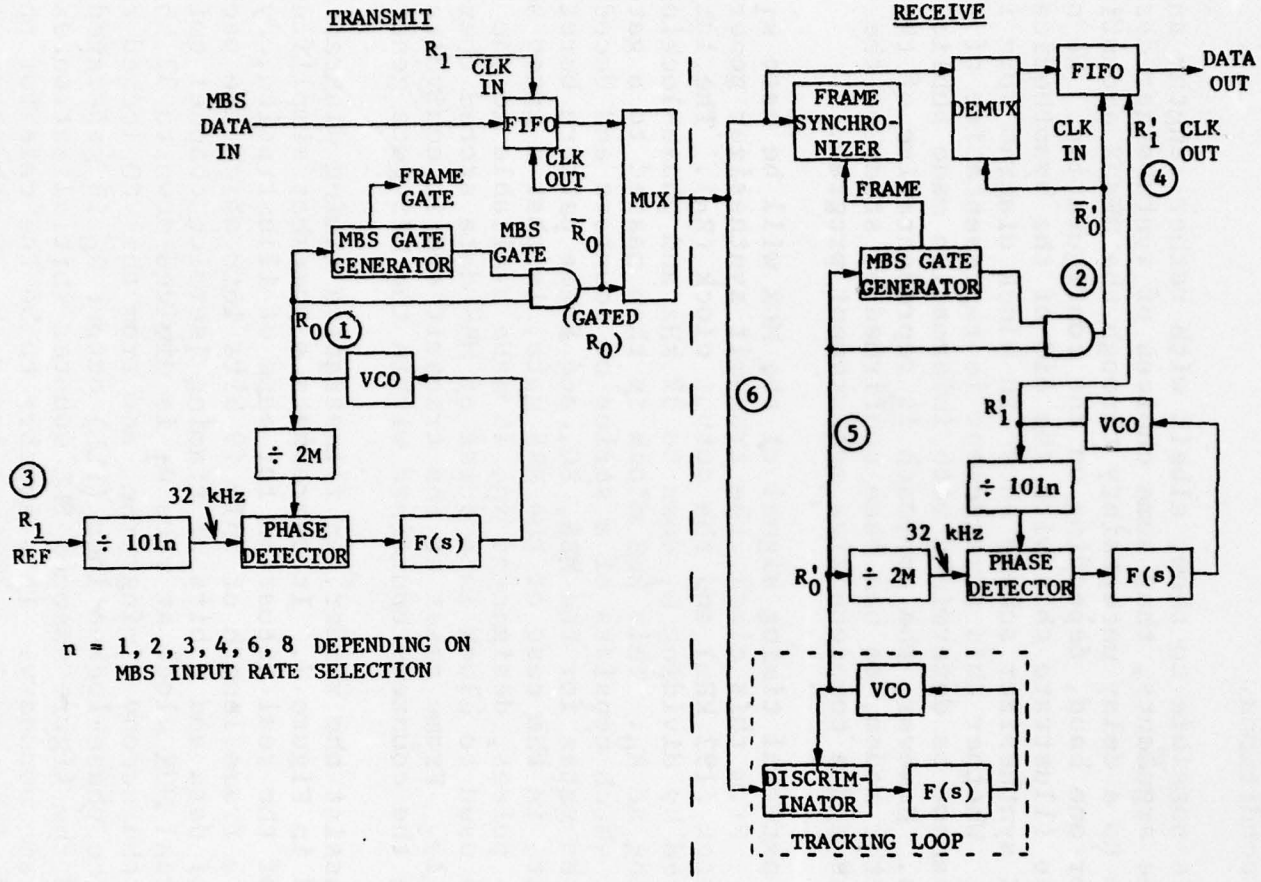
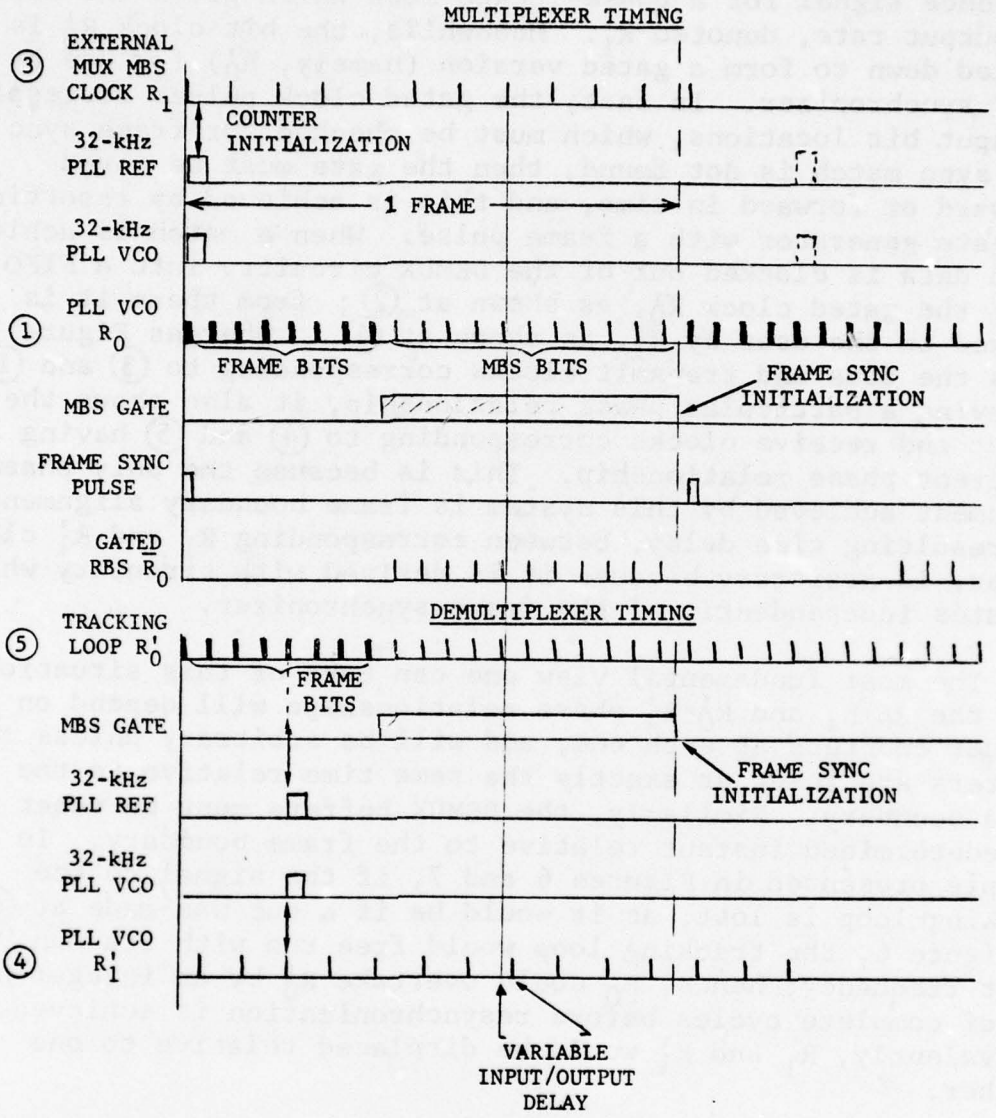


Figure 6 FRC-163 Radio Level-3 MUX/DEMUX Clock Synthesis Scheme



PLL = PHASE-LOCKED LOOP

Figure 7 Radio MUX/DEMUX Timing Diagram

At the receive end, the modem processing results in a tracking loop output clock R_0' at the transmit bit (or baud) rate. This clock is then divided down to produce a 32-kHz reference signal for a phase-locked loop which gives the correct MBS output rate, denoted R_1'. Meanwhile, the bit clock R_0' is counted down to form a gated version (namely, $\overline{R}_0'$) for use by the DEMUX synchronizer. In fact, the gated clock pulses correspond to input bit locations, which must be checked for frame sync. If a sync match is not found, then the gate must be moved backward or forward in time, and this is achieved by resetting the gate generator with a frame pulse. When a match is achieved, valid data is clocked out of the DEMUX circuitry into a FIFO using the gated clock $\overline{R}_0'$, as shown at ②; from there it is clocked to the user by R_1', as shown at ④. Whereas Figure 7 shows the data and transmit clocks corresponding to ③ and ① as having a particular phase relationship, it also shows the output and receive clocks corresponding to ④ and ⑤ having a different phase relationship. This is because the only phase alignment achieved by this system is frame boundary alignment. The resulting time delay, between corresponding R_1 and R_1' clock pulses, is arbitrary because it is derived with circuitry which operates independently of the frame synchronizer.

The most fundamental view one can take of this situation is that the R_0-R_1 and R_0'-R_1' phase relationships will depend on the divider counters at each end, and will be arbitrary unless these counters are reset at exactly the same time relative to the frame boundary. Similarly, the DEMUX buffers must be reset at a predetermined instant relative to the frame boundary. In the example presented in Figures 6 and 7, if the signal to the tracking loop is lost, as it would be if a cut was made at ⑥ of Figure 6, the tracking loop would free run with its own VCO reset frequency; hence, R_0 could overtake R_0' by an integer number of complete cycles before resynchronization is achieved. Equivalently, R_1 and R_1' would be displaced relative to one another.

To summarize, it can be stated that complete transit time integrity can only be maintained if both MUX and DEMUX synthesizer circuits and input/output buffers are reset in a coordinated fashion; specifically, they must both be reset at a fixed point in the multiplexing frame.

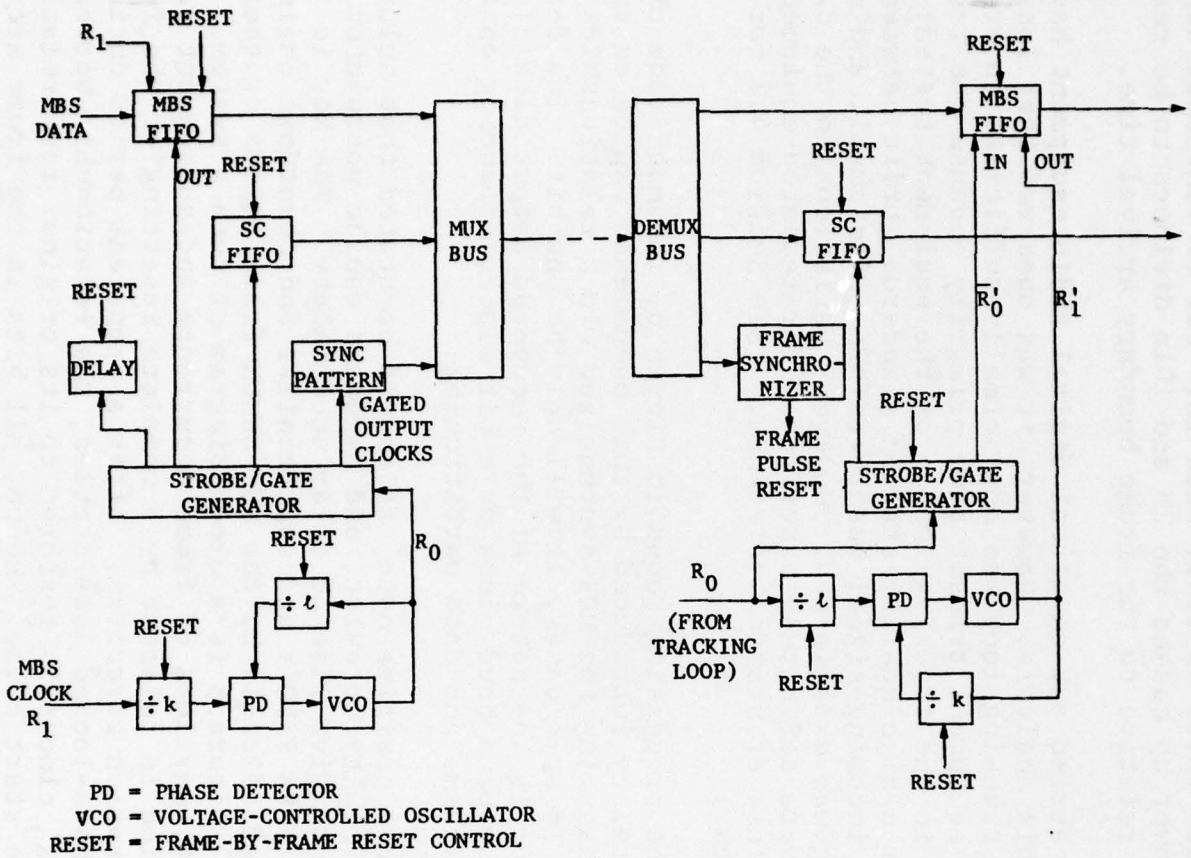
When this situation is examined further, it is found that difficulties are not likely to be introduced by synthesizer circuits at the transmit end where it is customary to reset

the synthesizer dividers and frame gate dividers with the same signal. It is the receive processing that creates problems. Moreover, the complications arise when equipment is taken out of service and later switched back in. For conventional designs at least, power up causes the 2M and 10ln dividers to be reset arbitrarily relative to the frame boundary arrival time.

Tests carried out on actual digital radio equipment have confirmed this analysis. However, it was observed that loss of sync by the tracking loop was not normally sufficient to create a change in equipment transit time primarily because the free-running VCO in the tracking loop (for the equipment tested) was derived from a high quality station standard. Drift between the VCO and incoming signal was therefore quite small, and no bit skipping was experienced. However, variations in the delay properties were definitely experienced for repeated equipment startup or loss of station reference. (See Section 4.2 for measured data.)

With the processing shown in Figure 6, the magnitude of the delay uncertainty introduced by this phenomenon can be as great as 1 baud, assuming the MUX-synthesized clock relationships are all fixed. In some cases, it will only be one bit. The determining factor is the nature of the recovered output data clock R_1', which may be a baud clock or a bit clock, depending on the modulation scheme and data partitioning.

On a more positive note, it should be stated that solutions to this difficulty do exist, and hardware can be postulated which does not give rise to delay uncertainty. The key is to ensure that both FIFO's and synchronizer and countdown chains are reset periodically by the MUX/DEMUX frame pulses or their equivalent. Figure 8 is a block diagram of such a system. In this concept, any loss of frame occurrence and subsequent reframing action is followed by a complete resetting of the frequency generation circuitry. After a transient period during which the phase-locked loop settles, the relationship between the R_1' and R_0' clocks is restored to its original form relative to the frame start pulse. Hence, all bits in the frame are clocked out with the same relative timing as they were before the reframing event. The three sets of timing diagrams shown in Figure 9 illustrate this sequence of events beginning with timing before the reframe, followed by similar characteristics immediately after the reframe and after the phase-locked loop transient has settled.



PD = PHASE DETECTOR
VCO = VOLTAGE-CONTROLLED OSCILLATOR
RESET = FRAME-BY-FRAME RESET CONTROL

Figure 8 Ideal Radio MUX/DEMUX Timing Synthesis

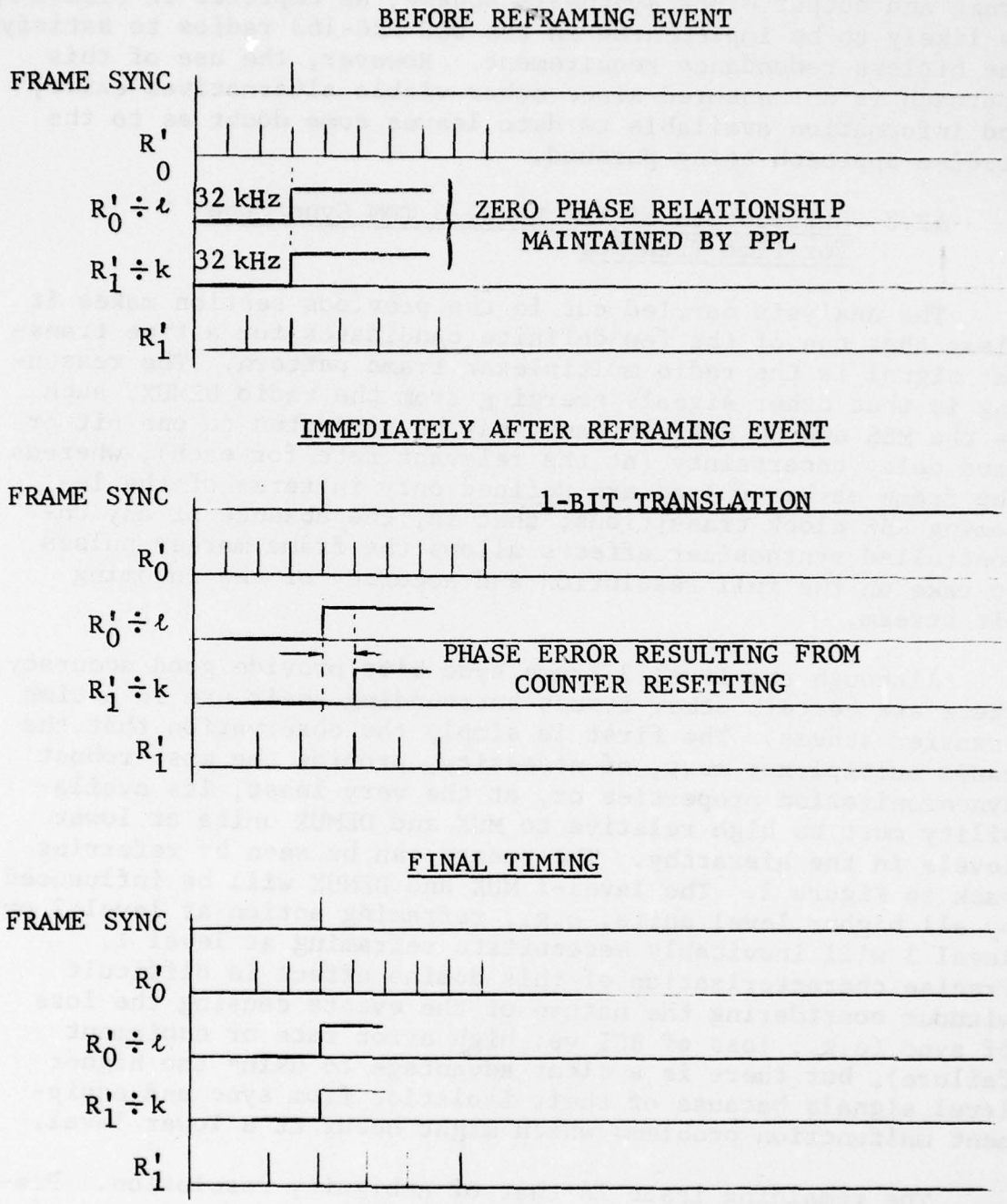


Figure 9 Timing Relationships Before and After Reframing to Accommodate a 1-Bit Loss of BCI

In conclusion, it can be stated that a fully synchronized frame and output clock synthesis scheme, as depicted in Figure 8, is likely to be implemented in the DCS FRC-163 radios to satisfy the hitless redundancy requirement. However, the use of this approach is not assured since other viable alternatives exist, and information available to date leaves some doubt as to the precise approach being pursued.

A2.3 Utilization of the Level-3 TDM Sync Code for Time Transfer

The analysis carried out in the previous section makes it clear that one of the few definite candidates for a time transfer signal is the radio multiplexer frame pattern. The reasoning is that other signals emerging from the radio DEMUX, such as the MBS and SC data streams, may be subjected to one bit or baud delay uncertainty (at the relevant rate for each), whereas the frame marker pulses are defined only in terms of the incoming RBS clock transitions; that is, the absence of any uncontrolled synthesizer effects allows the frame marker pulses to take on the full resolution and accuracy of the incoming bit stream.

Although the level-3 frame sync bits provide good accuracy, there are certain other issues surrounding their use in a time transfer scheme. The first is simply the observation that the radio multiplexer must, of necessity, provide the most robust synchronization properties or, at the very least, its availability must be high relative to MUX and DEMUX units at lower levels in the hierarchy. The reason can be seen by referring back to Figure 1. The level-1 MUX and DEMUX will be influenced by all higher level units, e.g., reframing action at level 2 or level 3 will inevitably mecessitate reframing at level 1. Precise characterization of this domino effect is difficult without considering the nature of the events causing the loss of sync (e.g., loss of BCI vs. high error rate or equipment failure), but there is a clear advantage to using the higher level signals because of their isolation from sync and equipment malfunction problems which might occur at a lower level.

The remaining issue is that of ambiguity resolution. Preliminary information on the FRC-163 indicates a frame rate of 4 kHz; therefore, a frame start indicator pulse at this rate should be easy to extract from the equipment. While such a signal offers good accuracy, the ambiguity arising out of a

periodic transmission must be taken care of for precise time-of-day distribution throughout the network. One method involves the simultaneous transmission of an encoded data sequence in such a way that its arrival time uncertainties, while much greater than the frame rate pulses, are bounded sufficiently so that a particular frame pulse can be identified, e.g., as a 1-second marker. The encoded data would, in addition, reveal the second, minute, hour, and day count. To carry this off successfully, the time code arrival time uncertainty must be less than half the period of the frame pulses, i.e., less than $\pm$ 125 μs. The actual transmission can conveniently be carried out over the service channel, so it remains only to establish whether the above accuracy goal can be met. Certainly, if the service channel clock synthesizer in the level-3 DEMUX does not synchronize with the frame boundary, at least one bit of uncertainty is introduced. At 192 kb/s, this amounts to about 5 μs.

In Section A2.4, this topic will be examined from the point of view of time transfer via the service channel itself.

A2.4 Transmission of Time Reference Signals via the Service Channel

Our emphasis thus far has been on the utilization of internal time markers which will exist for other reasons inside the various radios and TDM's. An alternative philosophy is to attempt transfer of timing events via one of the data interfaces available to the user. There would clearly be reluctance to devote one of the high-rate digital channels exclusively to time synchronization, so we concentrate our attention on a more obvious candidate — the service channel. It can be seen, by reference to Figure 1, that the digital portion of the service channel (referred to as the telemetry channel) amounts to a full duplex line between nodes with data rate on the order of 56 kb/s. The actual rate will depend on the structure of the service channel MUX, but present indications are that a modified 1192 would be used in this role. The inputs to the MUX correspond to two 64-kb/s PCM voice channels and a digital input. With an output rate of 3 x 64 kb/s, the required overhead for SCM framing must be extracted from either the voice inputs or the digital input. We can surmise that the structure will be one of two types. Either occasional framing bits will be "stolen" from the least significant bit of one or more of the input

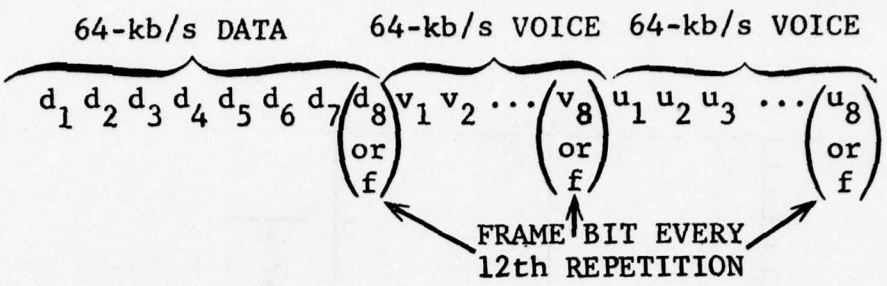
channels, or the digital input will be restricted to 56 kb/s synchronous with 8 kb/s then available for framing.*

With PCM voice signals present, it is anticipated that the usual 8-bit byte interlacing scheme will be implemented; that is, 8 bits of voice channel 1 followed by 8 bits of voice channel 2 and 8 bits of digital data or, alternatively, 7 bits of data plus 1 frame bit. Figure 10 illustrates the two format types with format A representing the current 1192 approach. The emphasis on byte interleaving is related to the structure of the PCM voice signals. The most significant bit position must be known at the DEMUX for correct D/A reconstruction, and this is simply done with byte interleaving.

An important consequence of byte interleaving is the delay experienced by the data at the input to the MUX and at the output of the DEMUX. This delay is introduced intentionally by FIFO's in a practical design. All MUX clocks are assumed synchronous so that there is no net fill or depletion of the buffers; but, for time transfer systems, the total input/output delay is important. Figure 11 shows the output clock relationships for the SCD, assuming format B of Figure 10. The notation used is similar to that used in previous sections. The symbol r_0 denotes a high-speed (192-kb/s) clock signal at the MUX end, while r_0' is the equivalent derived clock generated by the radio DEMUX for data hand-on to the service channel DEMUX. Similarly, $\overline{r}_0$ and $\overline{r}_0'$ are gated versions of these high-speed clocks. The clock signal specified as r_0 at the MUX (and r_0' at the DEMUX) represents the digital data clock for transfer of control data (i.e., CC). It is assumed to be 56 kHz in this discussion.

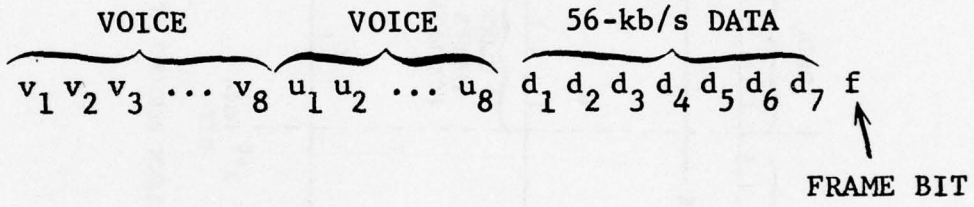
Data comes off the DEMUX high-speed line at rate r_0', and is gated for use by a digital channel FIFO. Data is then clocked out of this device at a more leisurely pace by r_1', the smoothed output rate clock. Note that a 14 clock period delay (in terms of r_0') is incurred. This amounts to about 80 μs! The bits experiencing less delay at the SCD must, of course, experience an equivalent delay increase at the SCM, e.g., bit 1 must be delayed almost until bit 8 has been clocked in. Hence, we can

*The 1192 multiplexer specifications allow for 3, 6, 12, or 24 input channel formats with an output rate of n x 64 kb/s in the case of 3, 6, or 12 channel configurations. Framing is achieved using the least significant bit of all 8-bit channel bytes at every 12th group of channel bytes, i.e., every 12n bytes, or 96n bits.



FRAMING SEQUENCE $f_1\ f_2\ f_3\ \ldots\ f_{12}$

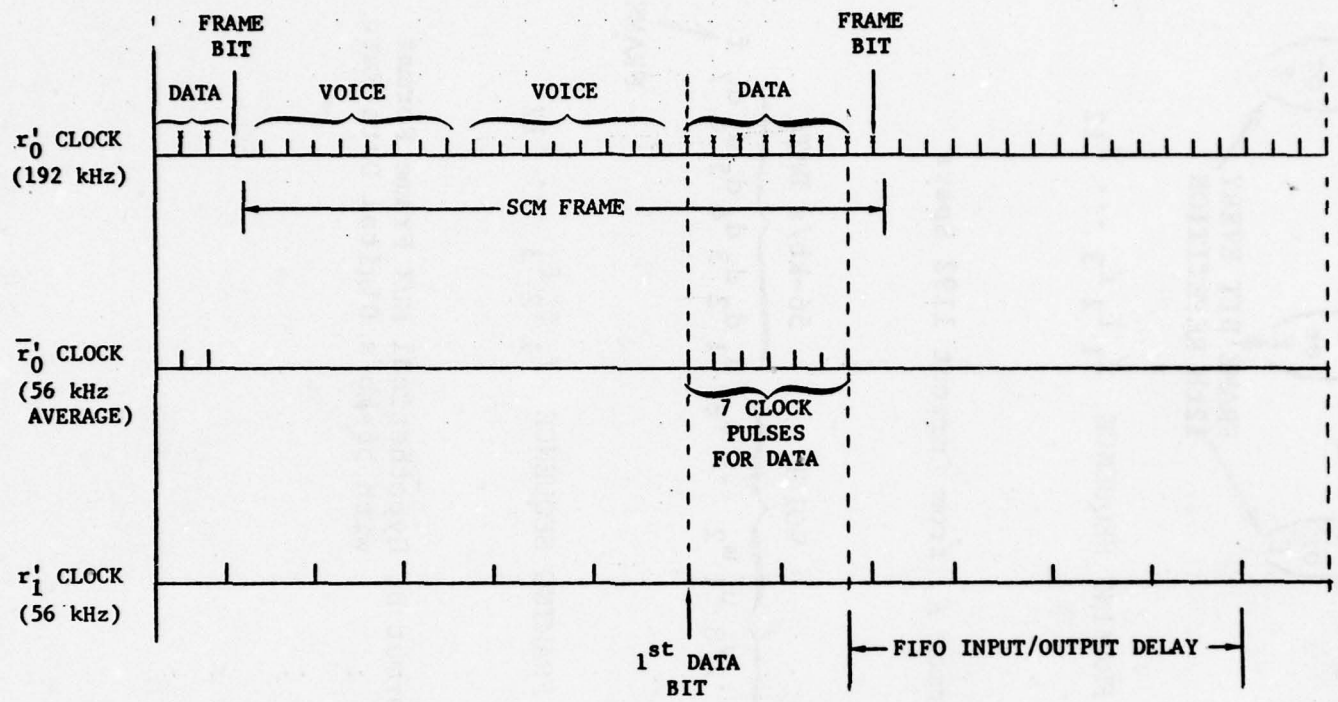
(a) Format A, from Current 1192 Specs



FRAMING SEQUENCE $f_1\ f_2\ f_3\ \ldots\ f_{12}$

(b) Format B, Hypothetical MUX Frame Format with 56-kb/s Digital Data Rate

Figure 10 Service Channel Multiplexer Frame Formats



MAXIMUM DELAY (FOR BIT 7) ≈ 14 CLOCK PERIODS AT 192 kHz

Figure 11 Service Channel Demultiplexer Timing Relationships

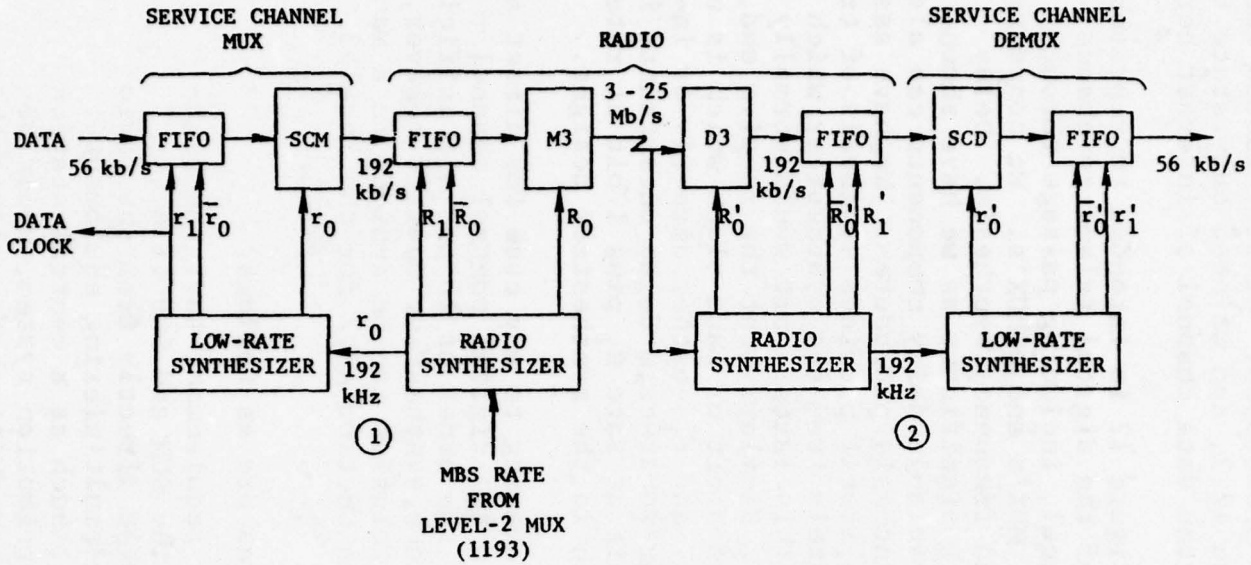
infer that a fixed delay of rather large magnitude will be introduced by passage through the SCM/SCD pair. Even more important is the variable delay which may be present as a result of typical synthesis procedures. Similar issues were covered at length in Section A2.2, and we need only state the equivalent conclusions for the data channel of interest here.

The block diagram of Figure 12 is intended to represent the end-to-end processing of the digital telemetry channel portion of the service channel, including passage through level 3 and service channel MUX's and DEMUX's. We concentrate once again on FIFO delay and frequency synthesis. Delay through the FIFO's, although significant as we have shown, will be mostly fixed, but variable delay components can also occur with certain clock synthesis procedures. We have assumed in Figure 12 that the radio itself provides synthesis of transmit clocks R_1 and R_0 separately from the synthesizer which we show producing r_1 and r_0. This latter unit would normally be included in the MUX itself. Similarly, at the receive end, the radio tracking loop provides a bit or baud clock which is used for synthesis of R_0', R_1', r_0', and r_1', either directly or indirectly. The potential for worst-case delay uncertainty is therefore equivalent to 1 bit at rate R_1 plus 1 bit at rate r_1, unless precautions are taken in the synthesizer designs.

The result is rather damaging to any case for direct application of the TRP signals to the digital control channel — the equipment uncertainty is of the order of 16 μs. If sufficient attention is paid to the clock synthesizer designs however, these potential delay uncertainties can be avoided in a manner similar to that described in Section A2.2 for the level-3 multiplexing operations.

Briefly, the precautions are as follows:

(1) It is a mandatory requirement that the high-speed clocks for the SCM and SCD (i.e., 192 kb/s) be derived directly from the radio multiplexing and demultiplexing equipment. A separate source, such as a central station synthesis and distribution system, would be unsatisfactory because its phase relationship with the clocks in and out of the radio MUX/DEMUX FIFO's is uncontrolled and, therefore, arbitrary.



$r_0\ R_0$ MUX OUTPUT CLOCKS AT TRANSMIT END

$r'_0\ R_0$ DEMUX INPUT CLOCKS AT RECEIVE END DERIVED FROM INCOMING DATA

$\bar{r}_0\ \bar{r}'_0\ \bar{R}_0\ \bar{R}'_0$ GATED CLOCKS AS ABOVE

Figure 12 Digital Control Channel Processing

(2) The radio synthesizers must have the frame synchronized reset features described in Section A2.2 to maintain a constant phase relationship between the service channel clocks at either end of the link.

(3) Similar design features must be included in the SCM and SCD synthesizer units, viz., the synthesizer counters and FIFO buffers must be reset at a predetermined point in time relative to the start of frame, and this must be carried out at least after each reframing operation.

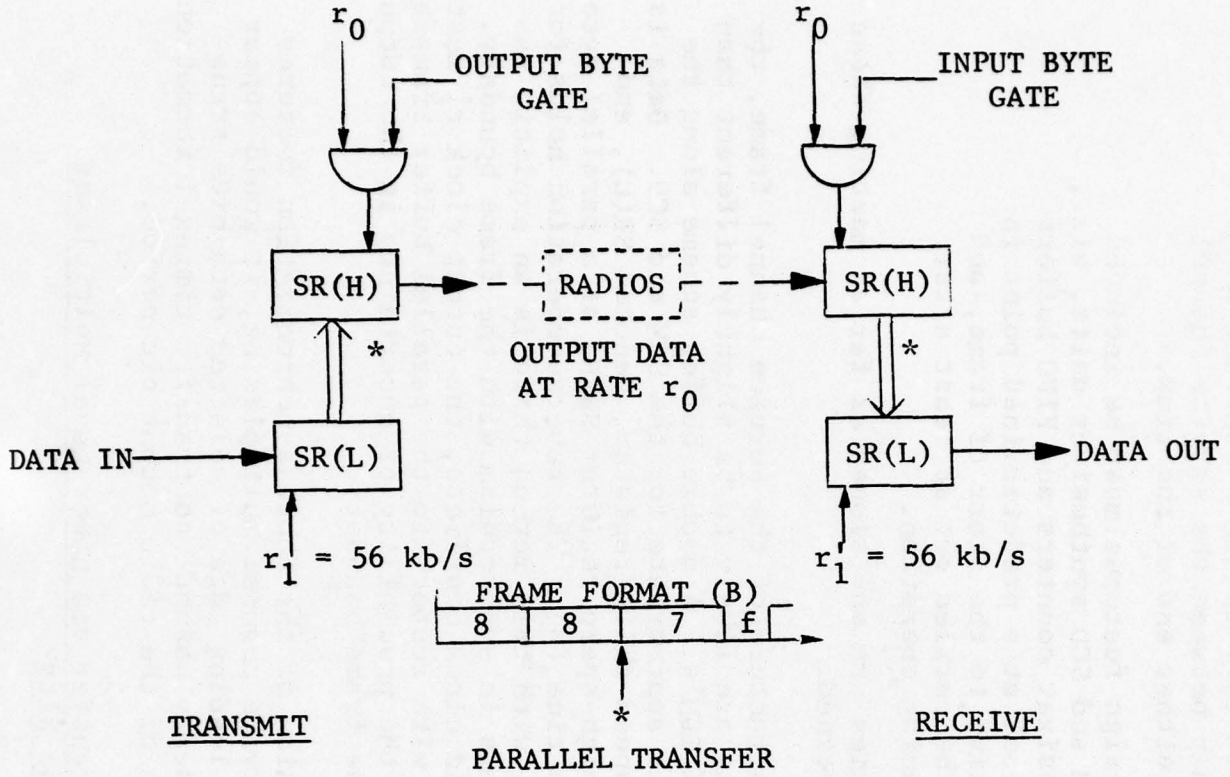
No serious difficulties are envisioned as far as meeting these requirements is concerned.

With the byte structure of the service channel frame, the buffer design details are likely to be slightly different than for the higher level TDM's. A double buffer scheme along the lines of Figure 13 is appropriate for the SCM and SCD. Data is clocked into a low-speed shift register, denoted SR(L), and transferred to the high-speed register SR(H) as a parallel byte at the start of byte time (*). The reverse operation holds for the DEMUX. Clearly, with this method there is an explicit resetting of the buffers in synchronism with the frame boundary. Furthermore, to avoid clock conflicts, the output clock r_1' must be phased correctly with respect to the parallel buffer transfer, thereby eliminating the possibility of uncertainty in the output clock relative to the frame boundary.

With the inclusion of the above synchronization features in the radio and service channel multiplexing, it would appear feasible to use the leading edge of selected data bits transmitted via the telemetry channel to transfer timing information to within a fraction of the radio output bit period.

A2.5 Timing Transfer via Lower-Level Multiplexer Frame Sync Bits

It should be evident from the analysis carried out in Sections A2.2 and A2.4 that similar difficulties can occur in lower-level multiplexer timing transfer schemes. Obviously, the data feeding a DEMUX must pass through the radio DEMUX where it may be subjected to the 1-baud delay uncertainty at the MBS rate; but it is not limited to this amount by any means. Take



SR(H) - HIGH-SPEED SHIFT REGISTER
SR(L) - LOW-SPEED SHIFT REGISTER

Figure 13 Service Channel MUX/DEMUX Buffering

the situation shown in Figure 14, for example. Here the level-1 TDM frame boundaries are utilized for time transfer. However, the corresponding 1.544-Mb/s signal must pass through both the radio and level-2 demultiplexers. The synthesizer shown can be internal or external to these devices, but it will exist in some form and will not generally be phase-locked directly to the beginning of frame markers.

With the explicit reference shown, MBS clocks from the radio would pass directly into synthesis circuits. This situation is shown in detail in Figure 15, where the modem-derived bit clock is divided down to 8 kHz (with an arbitrary phase relative to the frame repetition clock), and then used as a reference for the generation of 1.544 MHz with a phase-locked loop. A synthesizer of the form shown in Figure 15 will normally be built-in to the level-2 TDM, and it is the timing output at this level that we must be concerned with for level-1 frame sync timing transfer. With the divide-down operation shown at (1), the 8 kHz and 1.544 MHz will again have an arbitrary relationship to the level-2 frame sync pattern unless the $\div 193$ and $\div 2n$ counters are reset at a precise point in the frame. The resulting delay uncertainty can therefore reach a worst-case limit of 1 bit at 1.544 Mb/s (plus the level-3 DEMUX delay) without such precautions.

Similar conclusions can be drawn for any of the other lower-level multiplexers. It should also be observed that external data buffering, which must be implemented to take up node clock differences, must be inserted after the point of TRP recovery in the multiplexer hierarchy; hence, buffering must be at a lower level than the TRP, and all timing at higher points in the demultiplexer chain must be generated from the original modem clock.

A3. Multiplexer Characteristics of the MDTS Modem

A3.1 Multiplexing Format and Rate Structure

In the MDTS modem, there is provision for multiplexing of data at rates $2n \times 1.5690$ Mb/s* with a 64-kb/s orderwire data stream. Although the rates are nonstandard as far as the DCS network is concerned, the relationships are close enough to justify our study of the MDTS modem as an example. Note that

*Certain other rates are available, but need not be discussed here.

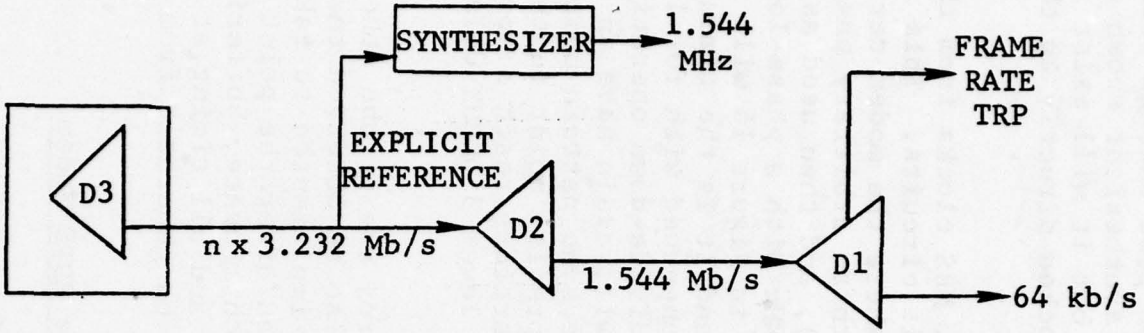


Figure 14 Demultiplexer Hierarchy for Time Transfer Using the Level-1 TDM Frame

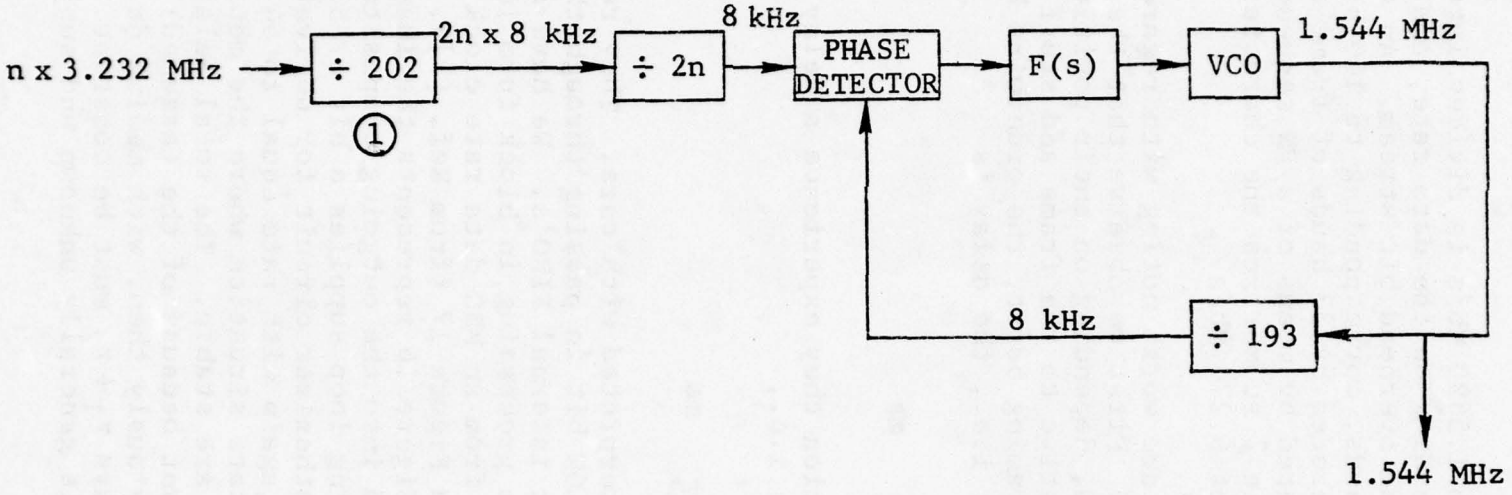


Figure 15 Synthesis of Level-2 DEMUX Frequencies for Level-1 Timing Transfer

the MBS rate, which corresponds to a VICOM multiplexer rate, is a multiple of 2 kb/s (not 8 kb/s as in the DCS specs).

The MBS data at $2n \times 1.5690$ Mb/s is divided into groups of 80, 120, or 160, depending on the data rate, and interlaced with single bits from the overhead bit stream. An overhead frame consists of 193 bauds, corresponding to 160 bauds of orderwire data (OW), preceded by 33 bauds of frame sync pattern. The frame sync is generated by means of a PN sequence generator of length 63 bits. Table 2 summarizes the characteristics for an input MBS data rate of 6.276 Mb/s.

A couple of points are worth noting with regard to the format shown in Table 2. First we observe that the orderwire data bits may be delayed, depending on their position in the overhead bit stream relative to the frame and stuff bits. For example, at the first framing burst, the orderwire bits are delayed by 66 sync bits; i.e., the delay is

$$\Delta\tau = 66 \frac{1}{78.45} \quad \text{ms}$$

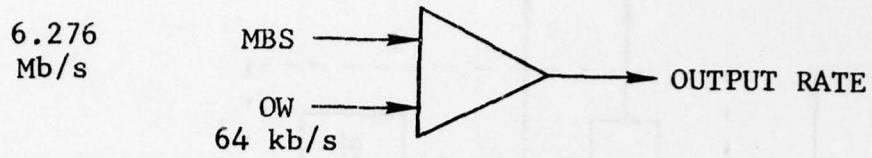
while at the stuff position they experience a delay equal to 116 bits at the OH rate, i.e.,

$$\Delta\tau = 116 \frac{1}{78.45} \quad \text{ms}$$

These delays must be interpreted with care. They represent the delay experienced by an OW bit in passing through the multiplexer and demultiplexer internal FIFO's. We have shown the MUX portion of the modem processing in block form in Figure 16. The OW clock is derived from an MBS data rate clock or from the data itself, as shown in Figure 17 (from Ref. [1]). The gated bit clock indicated on Figure 16 represents the instants at which OW data is clocked into the outgoing composite bit stream. At the DEMUX, the tracking loop supplies a bit or baud clock which is passed to a synthesizer circuit for derivation of an orderwire output clock, again with rate equal to 64 kHz. Consider now a steady-state situation where the medium delay is fixed and all clocks are stable. The total delay from OW-in to OW-out must be constant because of the (assumed) identical 64-kHz clock rates. Obviously then, with medium delay τ_0 fixed, the sum of the FIFO delays $\tau_1 + \tau_2$ must be constant. The only problem is that $\tau_1 + \tau_2$ is generally unknown and subject to

TABLE 2

MDTS ORDERWIRE MULTIPLEXING DATA



OUTPUT FORMAT:

$$(80I)\,O_1\,(80I)\,O_2\,(80I)\,O_3\,(80I)\,O_4\,(80I)\,O_5\,(80I)\,O_6\,(80I)\,O_7\,\ldots\ldots$$

OVERHEAD FORMAT:

$$O_1\,O_2\,O_3\,O_4\,O_5\,O_6\,\ldots\,O_{1569}\,O_1\,O_2\,\ldots\ldots$$

SYNC PATTERN — OW DATA

(66f)(320d) (66f)(320d) ... (50 stuff) (66f)(320d)

FRAME 1 FRAME 2 FRAME 8

MAJOR FRAME

$$\text{OVERHEAD RATE} = \frac{4 \times 1.569 \text{ Mb/s}}{80}$$

$$= 78.45 \text{ kb/s}$$

$$\text{AVERAGE OW DATA RATE} = \frac{78.45 \times (320 \times 8)}{[(8 \times 386) + 50]}$$

$$= 64 \text{ kb/s}$$

$$\text{AVERAGE MINOR FRAME RATE (SYNC PATTERN RATE)} = \frac{78.45 \times 8}{[(8 \times 386) + 50]} = 200 \text{ Hz}$$

MAJOR FRAME RATE = 25 Hz

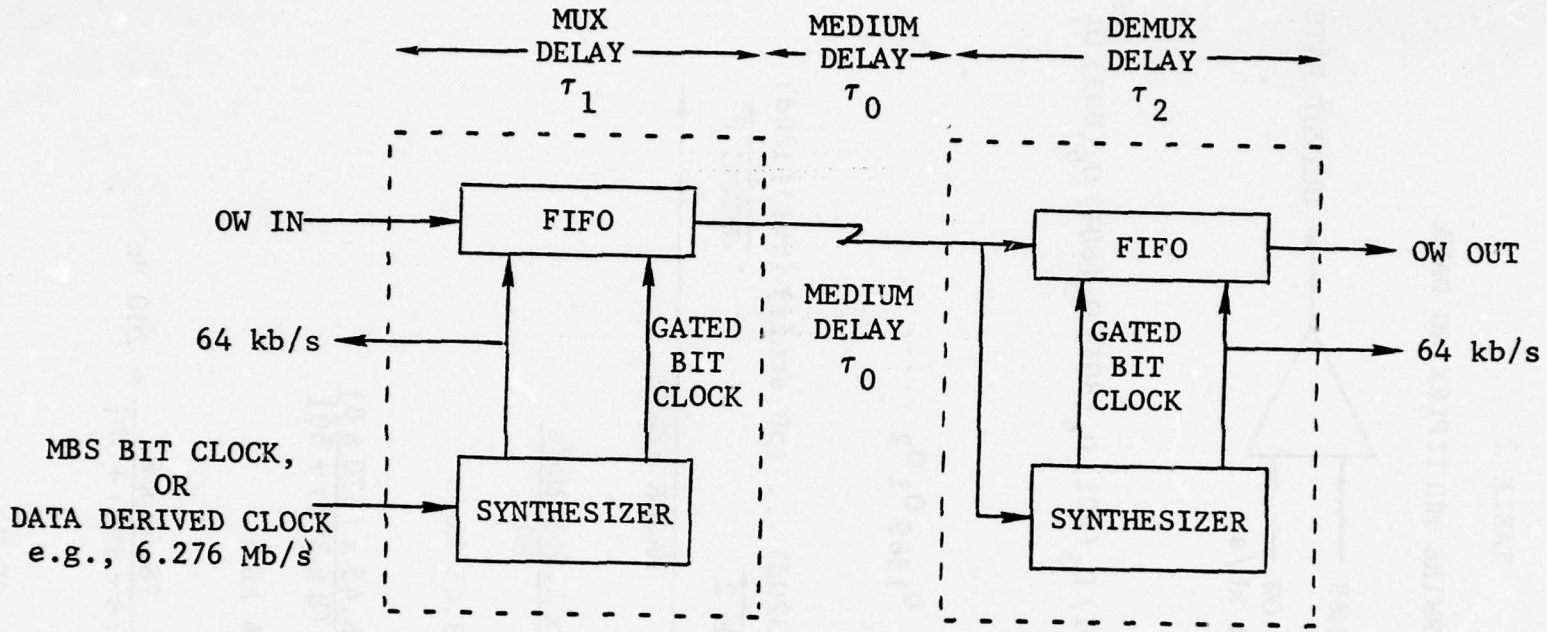


Figure 16 Orderwire Data Processing

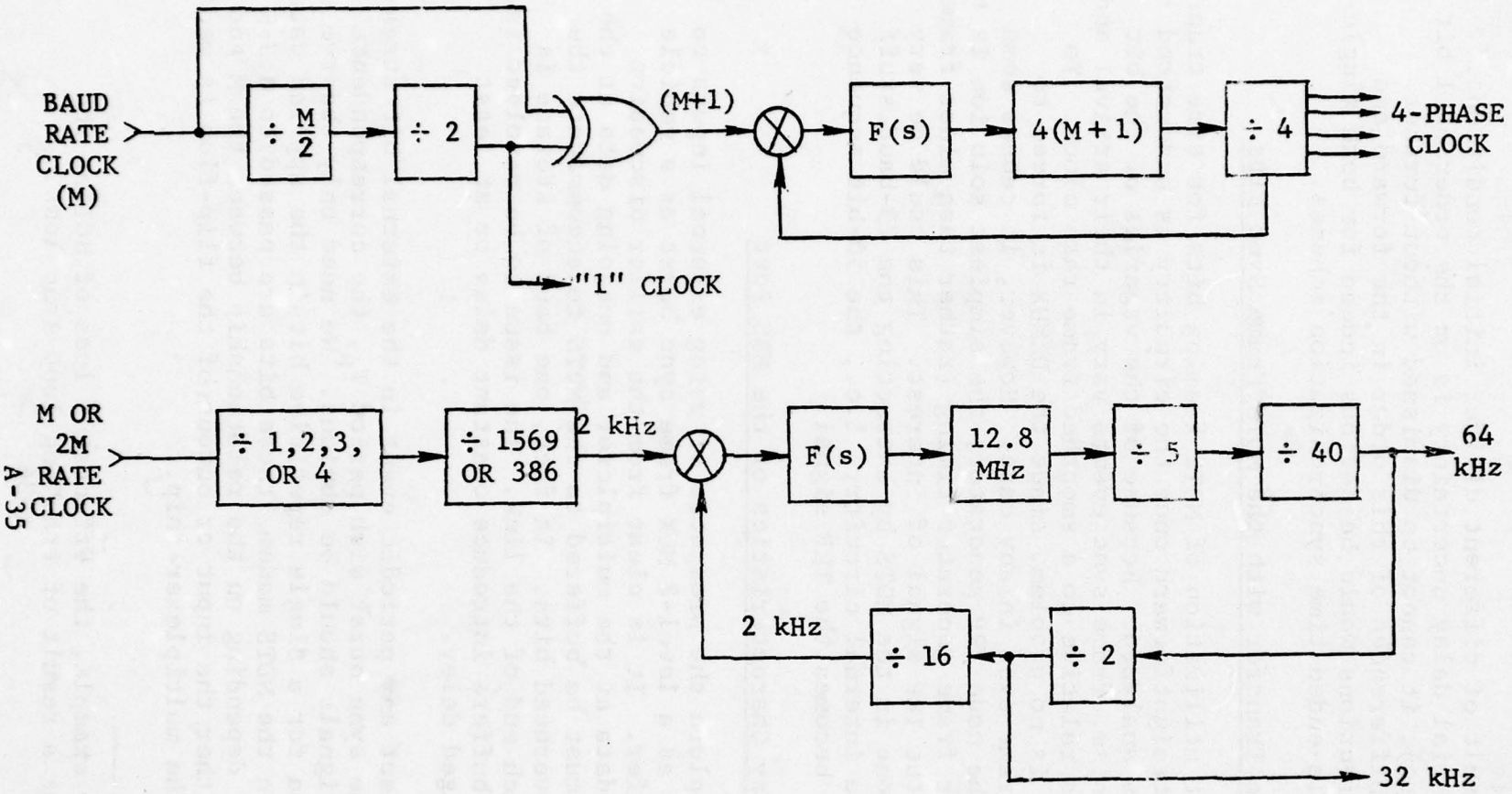


Figure 17 Block Diagram of Transmit Rate Generator (TRG)

change as a result of different divider initial conditions.* Since the potential delay uncertainty is on the order of 1 bit at 64 kHz (16 μs), it cannot be dismissed without further examination. Differences of this order in the forward and return link directions would be serious indeed for both single-ended and double-ended time synchronization schemes.

A3.2 Time Transfer with the MDTS Frame Sync Bits

The direct utilization of MDTS framing bits for time transfer is quite straightforward once the circuitry is understood and the options analyzed. Because of the vagaries of the bit stuffing mechanism, frame sync events vary in their arrival and departure times relative to a smoothed frame rate clock. To the modem this is no problem, since the DEMUX is forced to attain major frame sync in any case. However, it causes some problems for the node TRP generator; the simplest solution is to adopt the major frame generator timing (rather than minor frame generator) as the TRP signal of interest. This could be very conveniently done in the MDTS by extracting the 25-baud stuff signal from the internal circuitry, i.e., the 50-bit sequence of stuffed 1's becomes the TRP signal.

A3.3 Delay Characteristics of the MBS Port

We now explore the prospects of using external inputs to the MDTS, such as a level-2 MUX frame sync burst as a vehicle for time transfer. It is clear from the earlier discussion that incoming data at the multiplexer and outgoing data at the demultiplexer must be buffered to the MDTS to accommodate the injection of overhead bits. In fact, one baud of storage is required at each end of the link. The issue to be resolved is whether these buffers introduce constant delay or at least constant averaged delay.

If we select any periodic event in the external bit stream, such as a frame sync burst with period T_p, the correspondence with our TRP signals should be obvious. We need only observe delay phenomena for a single repetitive bit in the applied data bit stream. In the MDTS modem, these bits are passed to a J-K flip-flop and, depending on the relationship between the M and M+1 clocks, either the input or output of the flip-flop is made available to the multiplexer chip.

---

*Consider, for example, the effects of loss of BCI at the demodulator as a result of tracking loop sync loss.

In Figure 18 we show the clock portions of the clock generation circuitry at the transmitter. The true data baud clock, or "M" clock, is divided down to generate a "1" clock pulse for every 80, 120, or 160 M pulses. The extra pulse is added to the M clock and filtered by means of a phase-locked loop. With the existing loop design, offsets in frequency from the VCO rest frequency can be accommodated with zero steady-state average phase error, i.e., the quantity φ will average to zero. Similar circuitry exists in the DEMUX, as indicated in Figure 19. The most interesting feature of this block diagram is that the RRG and OTG baud clocks can have an arbitrary relationship* and, as a consequence, transit time through the DEMUX is subject to fixed biases of up to 1 baud.

A3.4 Time Transfer via the MDTS OW Port

The broad conclusion we are led toward as a result of earlier discussion is that time transfer via the OW is limited by the uncertainty in bit timing relationships for the input and output clocks. At the DEMUX, OW bits are clocked into the FIFO in accordance with their position in the OH frame; i.e., their arrival is coordinated with frame boundaries. Bits are then clocked out of the FIFO by a synthesized 64-kHz clock whose relationship to the frame boundaries is not controlled. Consequently, at least 1-bit uncertainty is anticipated, and this amounts to approximately 16 μs at the designated bit rate.

A3.5 Measured MBS Delay Characteristics for the MDTS Modem

As part of the experimental program carried out by CNR, the delay characteristics of two different MDTS modems in back-to-back configurations were evaluated. Particular emphasis was placed on the objective of confirming the delay uncertainties of 1 baud predicted theoretically in Section A3.3.

The transmit and receive times for PN sequences clocked into the two modems at 6.276 and 3.088 Mb/s, respectively, were applied to a time interval measurement setup; with adjustments for cable lengths, etc., the input/output delay was found. The results are tabulated in Table 3 for the 6.276-Mb/s modem and in Table 4 for the 3.088-Mb/s modem. Note that this represents the delay through the MBS ports. Total delay and delay differentials (for individual runs) are itemized in the above tables.

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*See also p. 4-53 of Ref. [1].

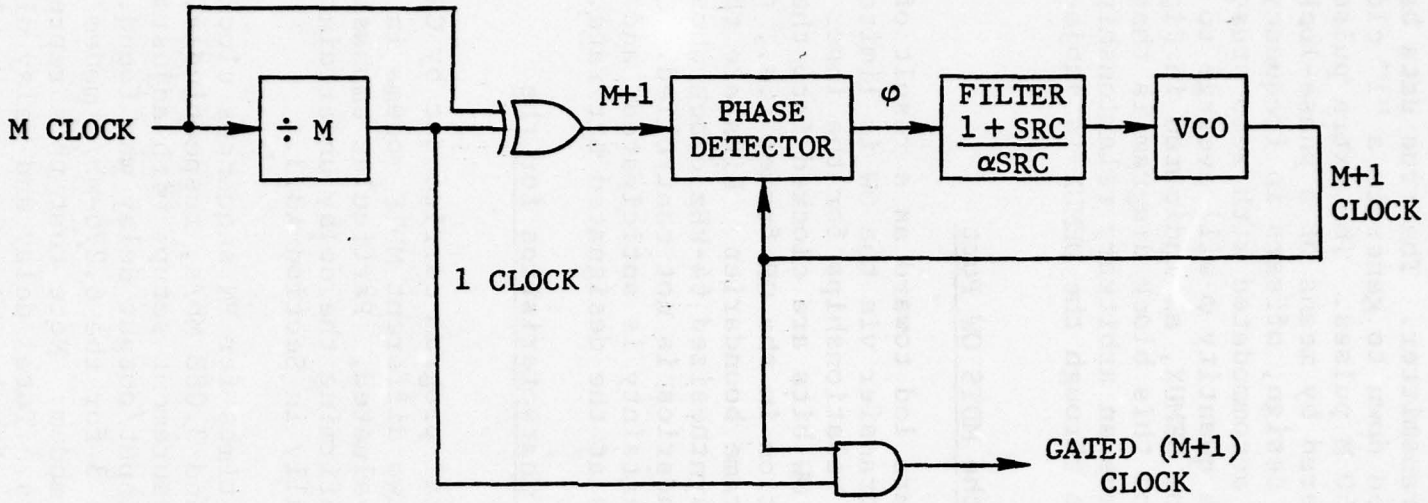


Figure 18 MDTS Transmit Timing Generation

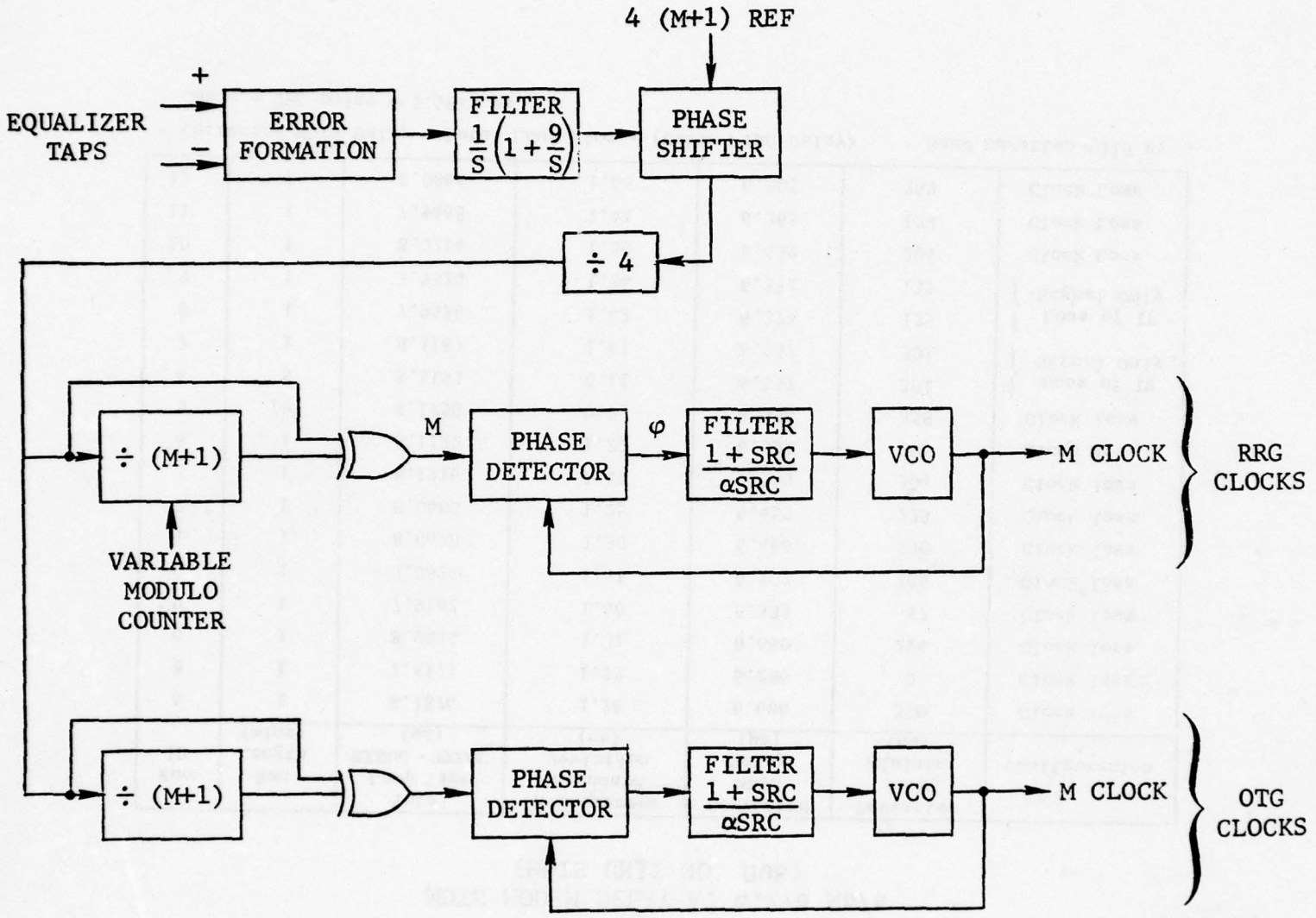


Figure 19 MDTS Receive Timing Generation

TABLE 3

MDTS MODEM DELAY AT 6.276 Mb/s
(MDTS UNIT NO. 008)

Run ID	Run Length (mins)	Total Loop Time RXEOC - TXEOC (μs)	Measurement Standard Deviation (ns)	Corrected MDTS Delay (μs)	Deviation from Minimum (ns)	Configuration
A	1	8.1876	1.26	6.606	370	Clock loss
B	1	7.8171	1.25	6.236	0	Clock loss
C	1	8.0414	1.31	6.460	224	Clock loss
D	1	7.9142	1.40	6.333	97	Clock loss
E	1	8.0834	1.41	6.502	266	Clock loss
1	1	8.0478	1.30	6.466	230	Clock loss
2	1	8.0406	1.25	6.459	223	Clock loss
3	1	8.1216	1.41	6.540	304	Clock loss
4	1	8.1122	1.27	6.531	295	Clock loss
5	10	8.1758	0.08	6.594	358	Clock loss
6	5	8.1185	0.11	6.537	301	Loss of IF Signal Only
7	1	8.1187	1.41	6.537	301	
8	1	7.9524	1.42	6.371	135	Loss of IF Signal Only
9	1	7.9524	1.34	6.371	135	
10	1	8.0214	1.50	6.439	204	Clock Loss
11	1	7.9468	1.41	6.365	129	Clock Loss
12	1	8.0866	1.44	6.505	269	Clock Loss

Corrected MDTS Delay = Total Loop Time - (Cable + TRG Delay) Baud Duration = 319 ns

Cable + TRG Delay = 1.5815 μs

TABLE 4

MDTS MODEM DELAY AT 3.088 Mb/s
(MDTS UNIT NO. 004)

Run ID	Run Length (mins)	Total Loop Time RXEOC - TXEOC (μs)	Measurement Standard Deviation (ns)	Corrected MDTS Delay (μs)	Deviation from Minimum (ns)	Configuration
14	1	11.8223	1.62	10.333	605	Clock Loss
15	1	11.5648	1.54	10.076	347	Clock Loss
16	1	11.7545	1.52	10.265	537	Clock Loss
17	1	11.3121	1.55	9.823	94	Clock Loss
18	1	11.2173	1.48	9.728	0	Clock Loss
19	1	11.8246	1.50	10.335	607	Clock Loss
20	1	11.3754	1.47	9.886	158	Clock Loss

Corrected MDTS Delay = Total Loop Time - (Cable + TRG Delay) Baud Duration = 647 ns

Cable + TRG Delay = 1.4488 μs

The various trials consisted of power off/on, station clock (5 MHz) removal and replacement, and simulated loss of sync by severing the IF connection between modulator and demodulator units. In general, the full 1-baud spread in transit times was observed when reinitialization of the MDTS was performed. During loss-of-sync conditions, the stability of clocks in the system was such that no loss of BCI was experienced for reasonable disconnection periods and, as a consequence, the DEMUX frame and output data clocks retained their original relationship when tracking loop sync was regained, resulting in no delay change.

REFERENCES

[1] MDTS Operation and Maintenance Manual, Vol. 1, Sylvania ESD, September 1976.

APPENDIX B

APPLICATION OF THE 1192 TDM TO SERVICE CHANNEL MULTIPLEXING IN A TIME TRANSFER SYSTEM

This appendix outlines some of the requirements that must be met in order to provide satisfactory time transfer via the service channel with particular emphasis on properties of the 1192 TDM as a potential service channel multiplexer.

B1. Service Channel Requirements

The potential time delay uncertainties which can exist in various DCS transmission elements were analyzed in Appendix A. We now extend these ideas down to, and including, the user interface to determine the most desirable equipment properties and timing distribution scheme for the service channel.

Figure 1 shows once again the radio and service channel TDM's and their interconnection. In addition, the user-provided link termination processors (LTP's) are shown interfaced to the service channel MUX/DEMUX units. Note that the NRZ interfaces are indicated explicitly.

Based on the analysis in Appendix A, we can make the following points:

(1) The radio synthesizer which generates the 192-kHz clock signals must be designed so that resetting of divider chains occurs after every reframing operation, i.e., the 192 kHz for the SCM and SCD must be phase-synchronized with the transmit and receive frame boundaries, respectively.

(2) Delay variation for paths through the NRZ interface drivers and receivers must be minimized. This is not easy because these devices are purposely made with inherently low bandwidth.

(3) The SCM and SCD must receive their timing directly from the radio synthesizer. The alternative of using C4 (indicated on Figure 1) from the station synthesizer is unacceptable because the phase of the 192-kHz C4 output is not locked to the M3 frame boundary.

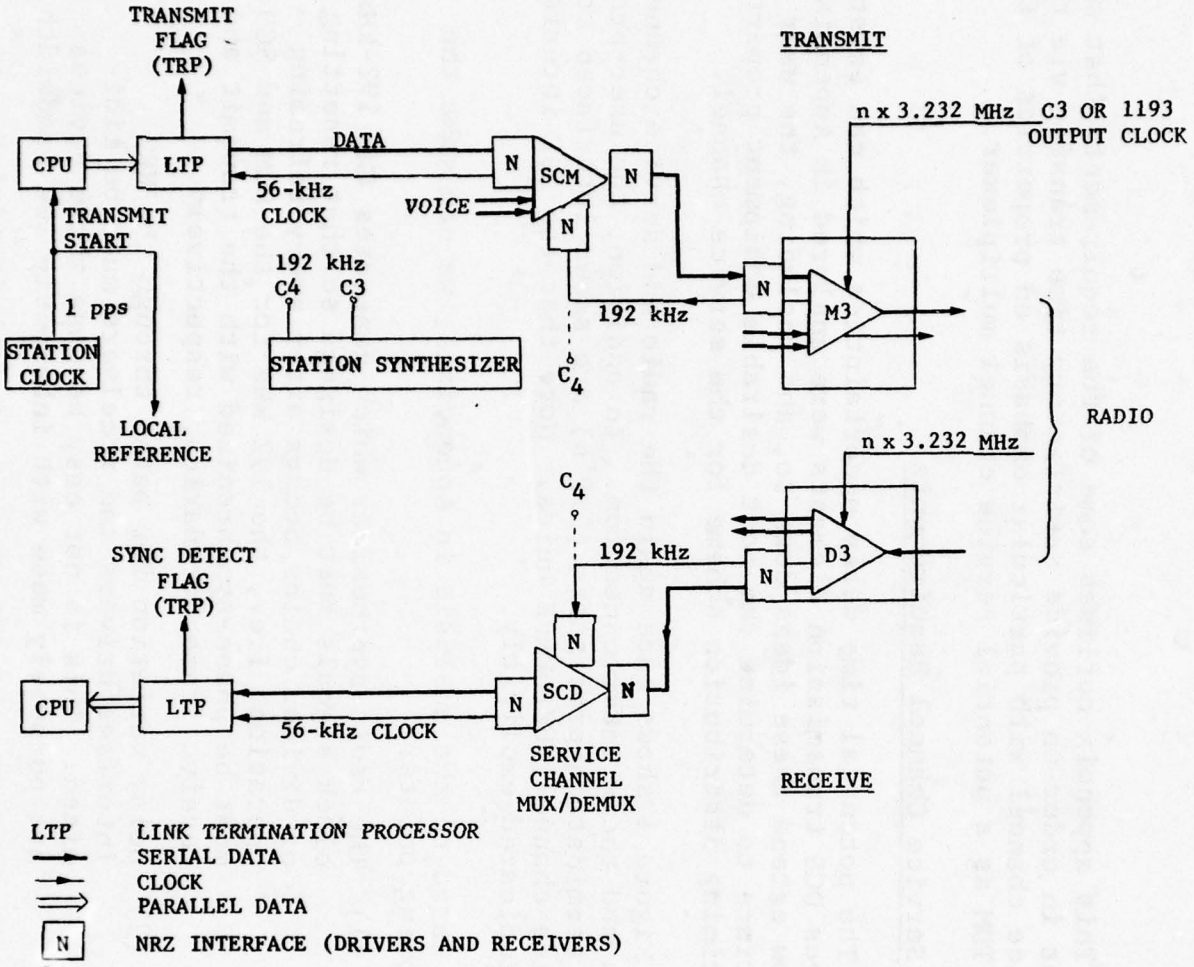


Figure 1 Service Channel Timing and Data Distribution

(4) All synthesis circuitry contained in the SCM and SCD units must be designed so that a deterministic phase relationship is obtained for the 56-kHz* clock relative to the 192-kHz clock. Again, this necessitates more sophisticated synthesizer circuitry than is normally envisaged by the TDM designer.

(5) The LTP processors must be clocked from the SCM/SCD output clocks; i.e., a synchronous communications scheme is necessary.

If implemented, these clock synchronization features would result in timing relationships of the form shown in Figure 2 which will be discussed in detail subsequently. Let us assume, for the moment, that all of the above conditions can be met, and examine the other features of the system in Figure 1.

The transfer of time in this particular approach begins with an interrupt from the station clock at the time of the 1-pps pulse, which we consider here to be the standard time reference at all nodes throughout the network. With the implementation shown in Figure 1, the result is a request for data transfer over the service channel and, at one of the 56-kHz clock transitions, the transmission begins and a coincident flag (transmit flag) is set. There will generally be uncertainty in the time at which this event occurs as a result of variable software delays; hence, a measurement of the time between the station 1 pps and LTP transmit flag is necessary (see t'_A in Figure 2). Similarly, for the receive functions, the data burst, which will have a sync code prefix byte, passes through the LTP and sets the sync detect flag on arrival with fixed delay relative to the 56-kHz receive clock. This pulse must be measured for its arrival time compared with the local 1-pps reference.

There is an alternative to this approach, but it has some drawbacks which require elaboration. Consider Figure 3 which illustrates a central node (node A) transmitting time references (designated TRP's) to four connected nodes (B, C, D, E). It is

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*The input data rate for the SCM has been chosen arbitrarily to be 56 kb/s. Other choices are possible; some of them are much more desirable. However, the 1192 TDM discussed in the next section can be readily configured for 56 kb/s synchronous or 50 kb/s asynchronous.

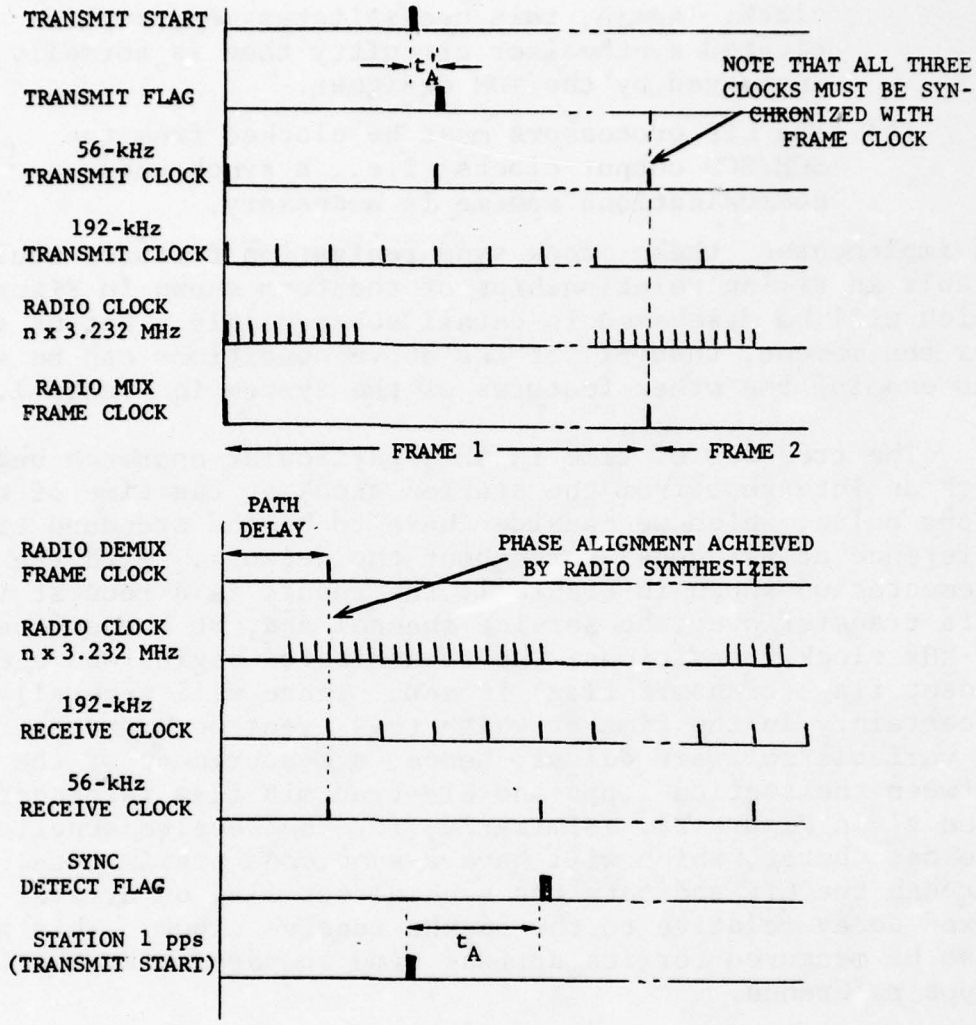


Figure 2 Service Channel Timing Relationships

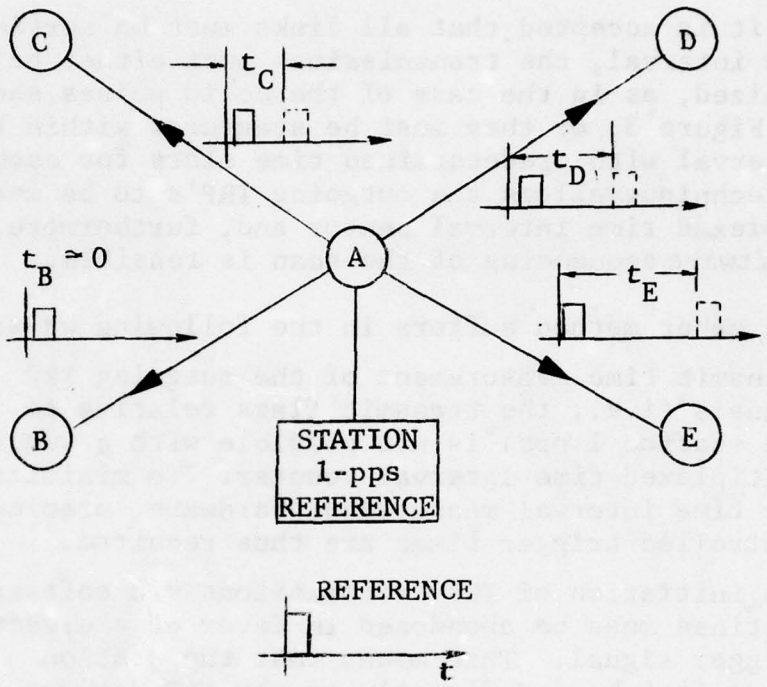


Figure 3 TRP Transmissions from Central Node A to Four Connected Nodes

desirable that each node in the system transmit such a signal through all terminated links at a fixed repetition rate; otherwise the complications of scan cycles and their coordination must be introduced. For example, with a sequential triggering of TRP transmissions for the four links at one per second, there would be a 4-second cycle, and node D may have to wait four seconds to receive an event on its link to A.

If it is accepted that all links must be serviced in the 1-second interval, the transmissions must either be totally synchronized, as in the case of the solid pulses shown for each link in Figure 3, or they must be staggered within the 1-second time interval with predetermined time slots for each. The latter technique allows the outgoing TRP's to be measured by a multiplexed time interval sensor and, furthermore, loosely timed software sequencing of the scan is feasible.

The other method suffers in the following ways:

- Transmit time measurement of the outgoing TRP signals (i.e., the transmit flags relative to the station 1 pps) is not possible with a single multiplexed time interval counter. To minimize the time interval measurement hardware, precisely-controlled trigger times are thus required.
- The initiation of TRP transmissions via software routines must be abandoned in favor of a direct trigger signal. This means that the station 1 pps must be fed directly to the TRP devices to start the signal transmissions.
- It is not sufficient that the LTP's all have a common 1-pps trigger; there is now the mandatory requirement that the 56-kHz clock fed to the LTP have a known and repeatable phase relationship with the 1 pps, i.e., the time difference t'_A (shown in Figure 2), which is not measured in this approach, must be constant for all possible equipment initialization sequences. Moreover, all service channel MUX's must have the same timing relationship between their 56-kHz clock and the 1 pps on a network-wide basis. If this condition is not satisfied, as much as one cycle of 56-kHz clock time uncertainty could be experienced (18 μs).

- To achieve the above phasing for the 1-pps and 56-kHz clocks, it is necessary that the n x 3.232-MHz clock to the radio be derived from a common source for all radios at a node, and that it be phased with the 1 pps in the same manner as all other nodes. Then, as an additional requirement, the radio MUX and SCM must both coordinate their frame and synthesizer resets at a predetermined time relative to the 1-pps station clock. This is necessitated by the stated 56-kHz and 1-pps clock phasing requirement, as well as the usual need to preserve delays through the radio.

Stated concisely, it would appear that the method of simultaneous TRP transmission is feasible only if all 56-kHz clocks at SCM inputs are phased identically with the 1-pps clock. This, in turn, places quite stringent demands on the resetting of synthesizers and frame counters at the service channel and radio multiplexers.

B2. Characteristics of the 1192 TDM

Here we look at the specifications and available design data on the 1192 TDM, which has been considered as a candidate for the service channel MUX/DEMUX functions.

B2.1 General Properties

We restrict our attention to the 3-channel version of this TDM, since that is the assumed configuration for the service channel application.

The clock and data inputs are indicated in Figure 4 which shows the 1192 TDM in block diagram form. The data channel modules may be selected from a range of devices to provide interfaces at 0 - 20, 50, and 56 kb/s. The timing modules set up the channel select signals for each byte of data being multiplexed and provide a 1.544-MHz clock to the channel modules for a high-speed serial transfer burst of 8 bits. The output bit rate is 192 kb/s and the frame format is specified in Figure 5. In the 3-channel mode, a frame consists of three interleaved 8-bit bytes, one from each channel, making a total frame length of 24 bits. Since there is no direct overhead allocation for frame bits, a bit stealing approach is used. At every 12th frame, the 8th bit of each channel byte is set alternately to

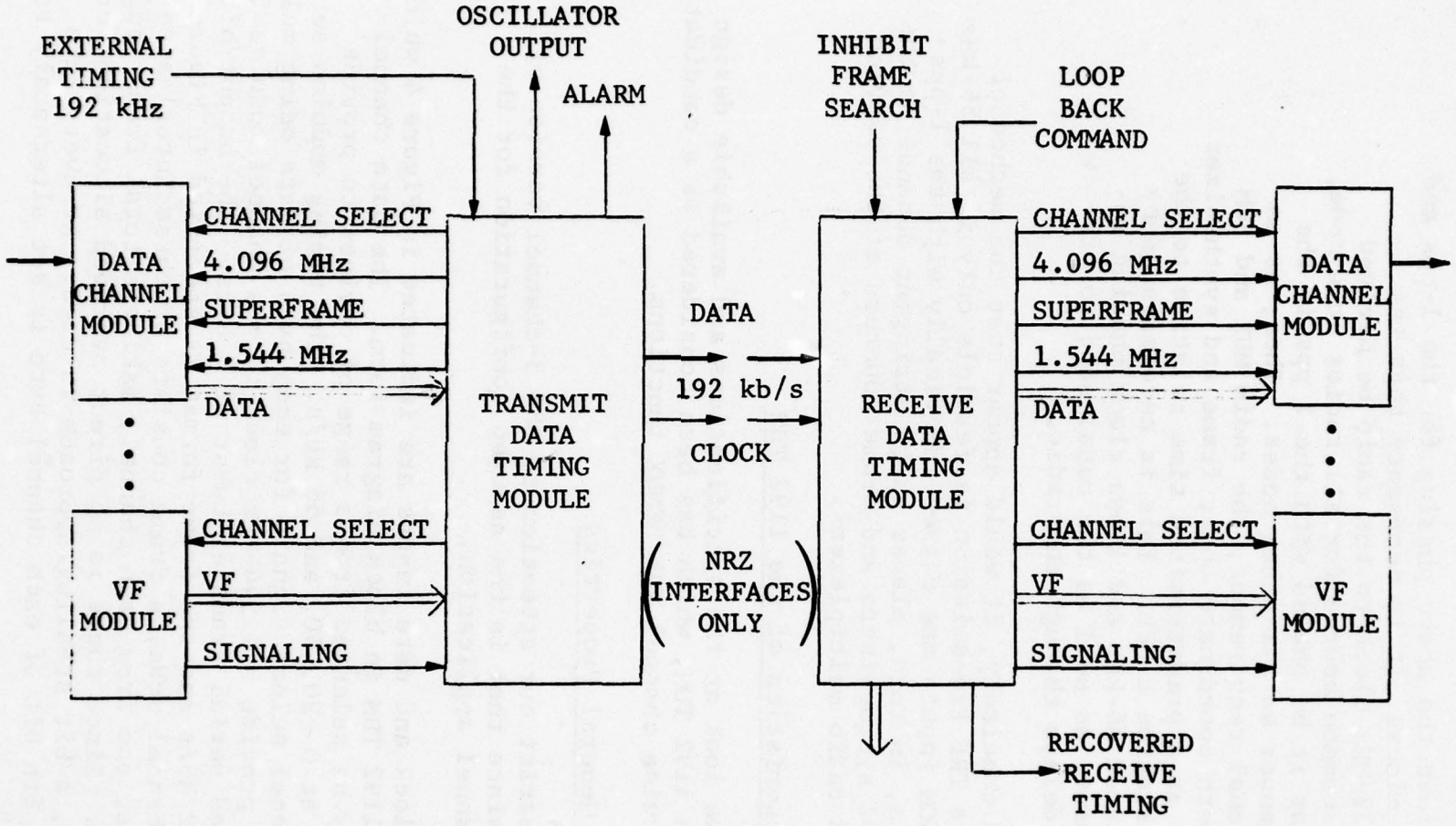
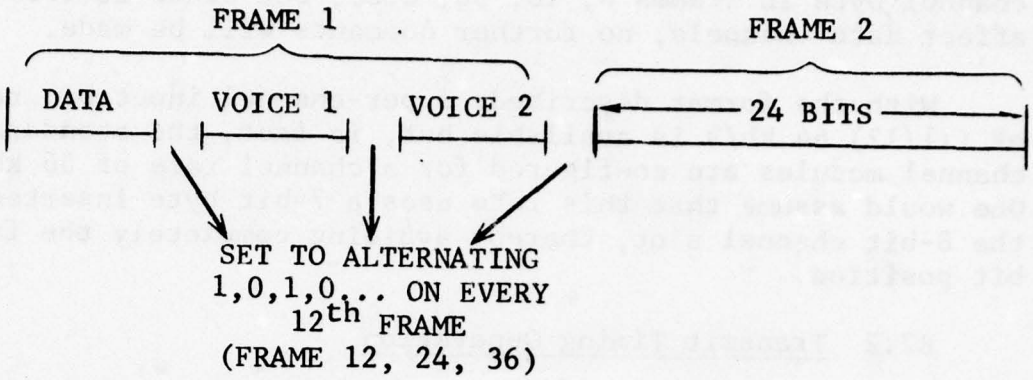


Figure 4 1192 Block Diagram and Signal Interfaces



SIGNALING ON BIT 8 VOICE CHANNELS ONLY DURING FRAMES 6, 18, 30 ...

OUTPUT DATA RATE: $8 \times 8 \times 3$ kb/s

$= 192$ kb/s

DATA INPUT RATE =

$\left(\frac{11}{12}\right)$ 64 kb/s	MAX
56 kb/s	WITH 7-BIT BYTE
50 kb/s	ASYNCHRONOUS (PULSE STUFF)

Figure 5 3-Channel 1192 TDM Frame Format

a 1, 0, 1, 0, 1 .... Interleaved with this sequence is a channel signaling bit, stolen from the 8th bit of each voice channel byte in frames 6, 18, 30, etc., but since it does not affect data channels, no further comments will be made.

With the format described, a per-channel input bit rate of (11/12) 64 kb/s is available but, in fact, the standard data channel modules are configured for a channel rate of 56 kb/s. One would assume that this rate uses a 7-bit byte inserted into the 8-bit channel slot, thereby avoiding completely the framing bit position.

B2.2 Transmit Timing Generation

The standard internal timing signals consist of 1.544 MHz, as a basic data timing source, and 4.096 MHz, which is an even integral multiple of all synchronous data rates except 56 kb/s. The 4.096-MHz clock is locked to the TDM external clock input (in this case, 192 kHz) using a phase-locked loop of the form shown in Figure 6. The output clock (192 kHz) is derived by dividing down the VCO frequency after elimination of every 193rd VCO pulse. The 4.096-MHz clock is obtained in a similar manner, while the 1.544-MHz clock is derived by directly counting down the VCO output. About 40 ns of jitter is introduced in both the 192-kHz and 4.096-MHz clocks with this approach. For a periodic 1-per-second transmission, this would manifest itself as a fixed delay offset rather than jitter and, without resetting the ÷193 counter at a fixed time in the frame, an uncertainty of 80 ns would be introduced.

The 1.544-MHz and 4.096-MHz signals are distributed to all data modules; from available information, it would appear that the individual data modules (only one in the case of the SCM) derive the 56-kHz clock from the 4.096-MHz clock by inhibiting pulses and counting down the result. For example, the ratio between the two rates is 73-1/7. If the 4.096-MHz clock is divided by 73 on six out of seven occasions and then by 74 on the seventh, a jittered version of 56 MHz is generated. The time variation is one period at the high rate, i.e., approximately 250 ns. Again, it should be pointed out that all divider circuitry in this synthesis circuit must be locked to some timing event available at both ends of the link, such as the frame boundary; otherwise, delay uncertainties of up to one period (18 μs) will occur.

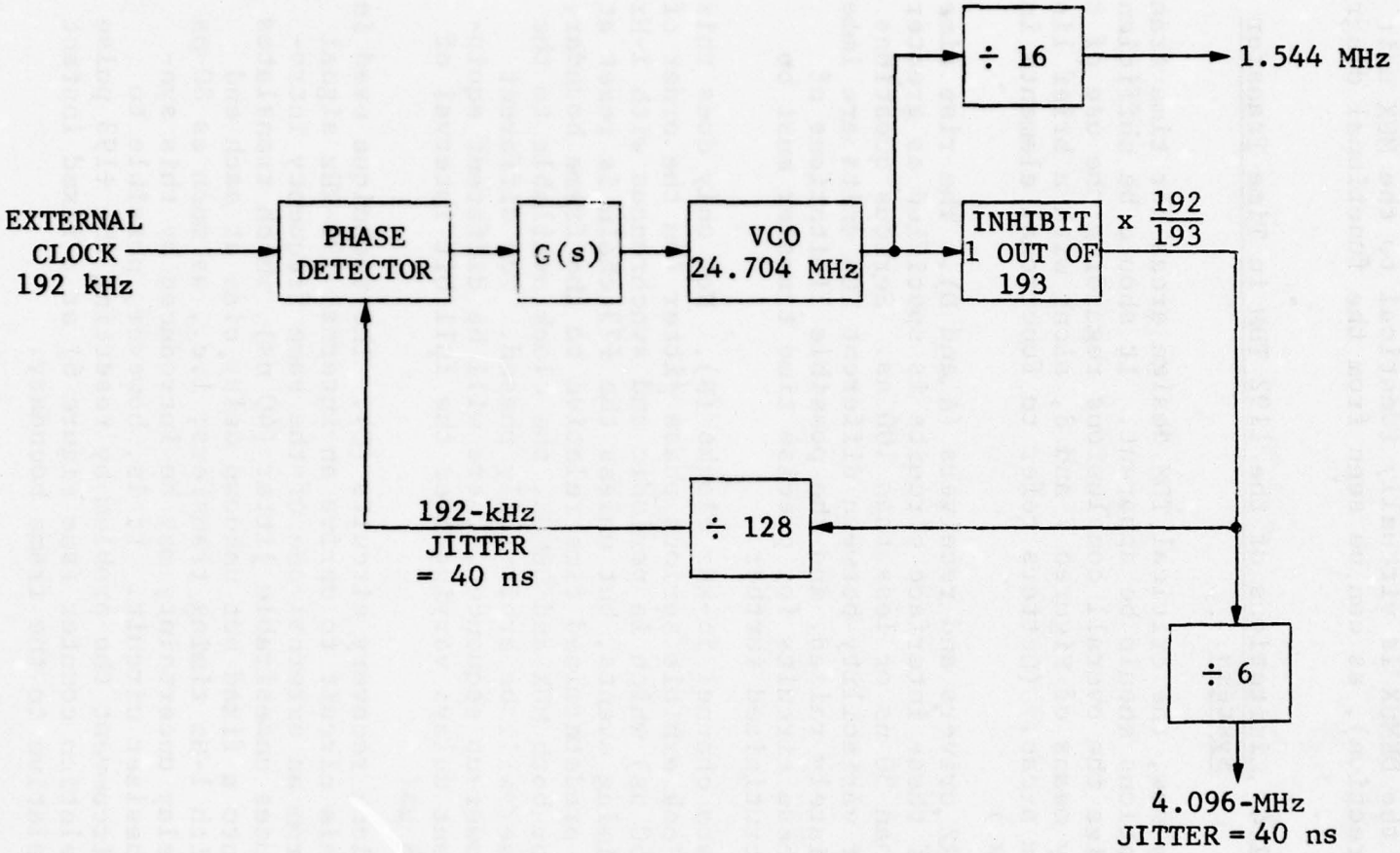


Figure 6 Transmit Frequency Generation for 1192

The 4.096-MHz clock is passed to the data channel module synthesizer for generation of a 56-kHz clock. Data transfer within the DEMUX is virtually identical to the MUX unit (except for direction), as can be seen from the functional diagram, Figure 7.

B2.4 Limitations of the 1192 TDM in Time Transfer Systems

By now, the critical TDM design areas for time transfer applications should be apparent. It should be sufficient to summarize the overall conclusions regarding the use of the 1192 by means of Figures 7 and 8, along with a brief list of problem areas. (Letters refer to functional elements in the figures.)

- NRZ drivers and receivers (A and D). The rise time of these interface circuits is specified as greater than 30 ns or less than 100 ns. Serious questions of variability between different TDM units are immediately raised, and the possible limitations of these circuits for precise time transfer must be scrutinized further.
- Data channel 56-kHz clocks (B). Not only does this clock exhibit serious phase jitter (on the order of 250 ns) which is periodic and synchronous with 1-Hz timing events, but unless the ÷73 chain is reset at a predetermined time relative to the frame boundary for both MUX and DEMUX, the clock available to the user will be arbitrarily phased. For different power-up sequences, there will be different equipment delays varying over the full bit interval of 18 μs!
- Clock recovery circuits (C). The technique used in this circuit to derive an internal 192-kHz signal from an external one of the same frequency introduces undesirable jitter (40 ns), which translates into a fixed but unknown delay bias at each end with 1-Hz timing transfers; i.e., as much as 80-ns delay uncertainty may be introduced by this synthesizer circuit. It is, however, possible to circumvent the problem by resetting the ÷193 pulse deletion counter (see Figure 6) at a fixed instant relative to the frame boundary.

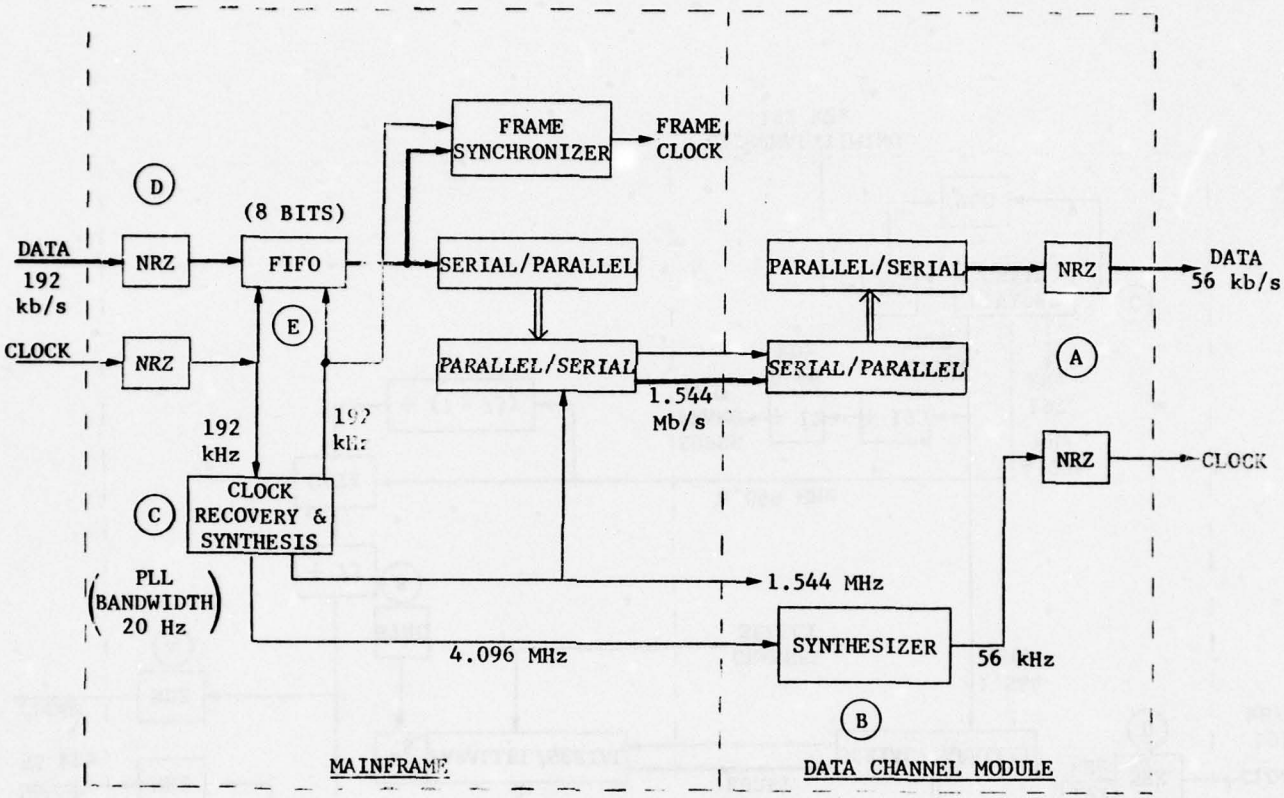


Figure 7 Functional Representation of 1192 DEMUX Functions for Time Transfer Purposes

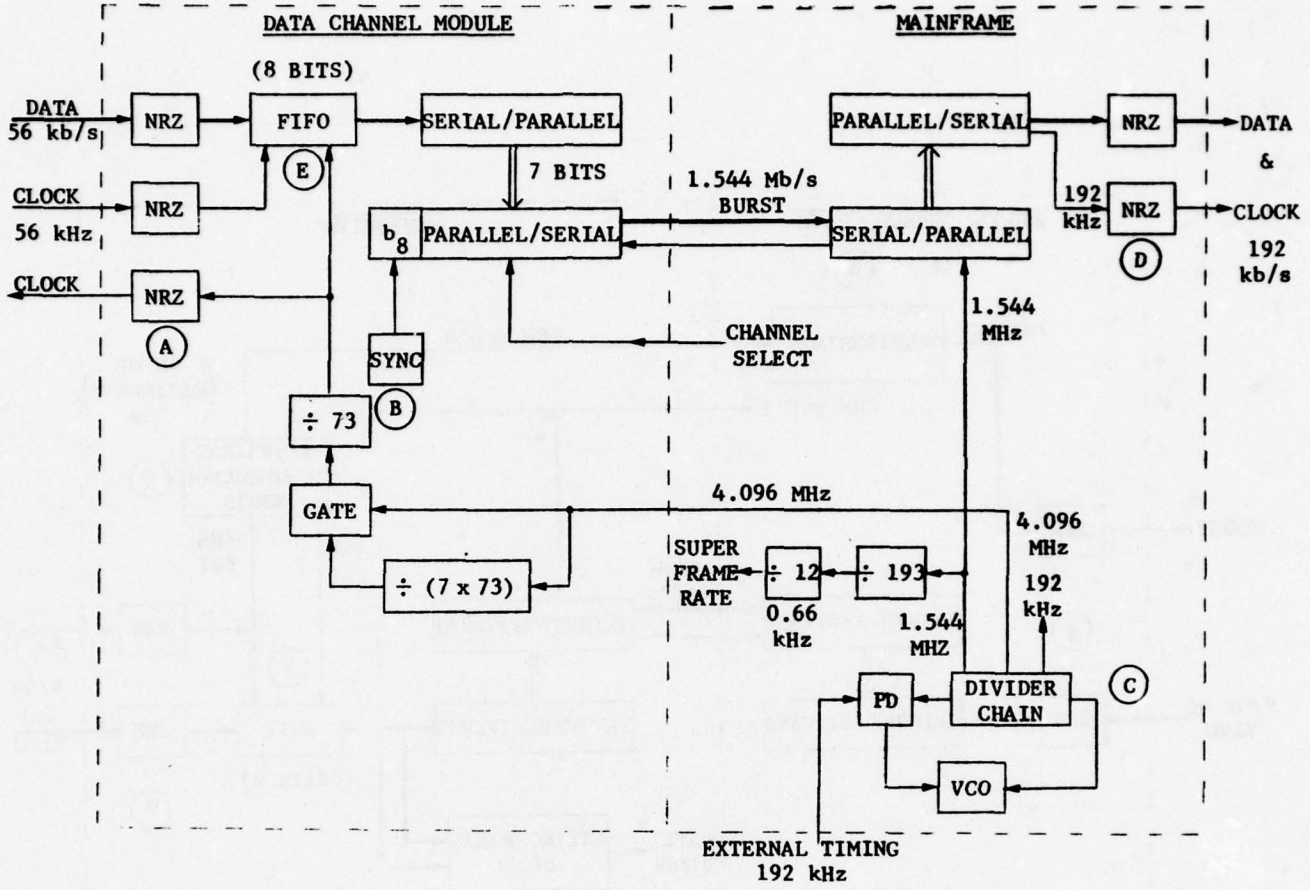


Figure 8 Functional Representation of 1192 MUX Functions for Time Transfer Purposes

- FIFO delay characteristics (E). Some care is necessary in the initialization of the low-speed MUX data FIFO (Figure 8) and, more particularly, of the higher-speed DEMUX FIFO (Figure 7). In the latter case, the recovered 192-kHz clock represents a smoothed version of the external 192-kHz clock, so that the phase difference between these two signals is a time-varying random process. Therefore, if phase slewing in excess of 1 bit is permissible on the external clock, the FIFO reset, which must be implemented at some point in the power-up sequence, may occur at a time when the differential phase momentarily exceeds 1 bit. As a result, an initialization bias will be set into the device (see Figure 9). In general, delay biases corresponding to integer bit intervals could occur in such situations.

It is apparent from the discussion presented in this appendix that significant redesign is needed to adapt the basic 1192 TDM unit to the service channel functions when precise time transfer is to be carried out via the digital portion of the service channel.

B3. Suggested 1192 Modifications

Direct application of the service channel to precise time transfer does not appear to be feasible when the present 1192 TDM design forms part of the channel. The estimated delay components for various pieces of DCS equipment are itemized in Table 1. The clear indication is that the service channel multiplexer must be custom-designed to meet the stringent delay uncertainty requirements in this application. Instead of addressing that topic in full, we assume instead that one of the alternative time transfer methods is more likely; therefore, the tolerances on delay through the service channel may be relaxed, and we will concentrate in this section on modifications to reduce the uncertainty to a few microseconds.

It should be stated first that part of the design problem is to reduce the clock control data link bit rate to a level more appropriate for the volume of data to be transferred. In addition, this strategy will ease the link processing burden which is increasingly present at higher data rates. The task then is to supply the clock controller with a data link port having a

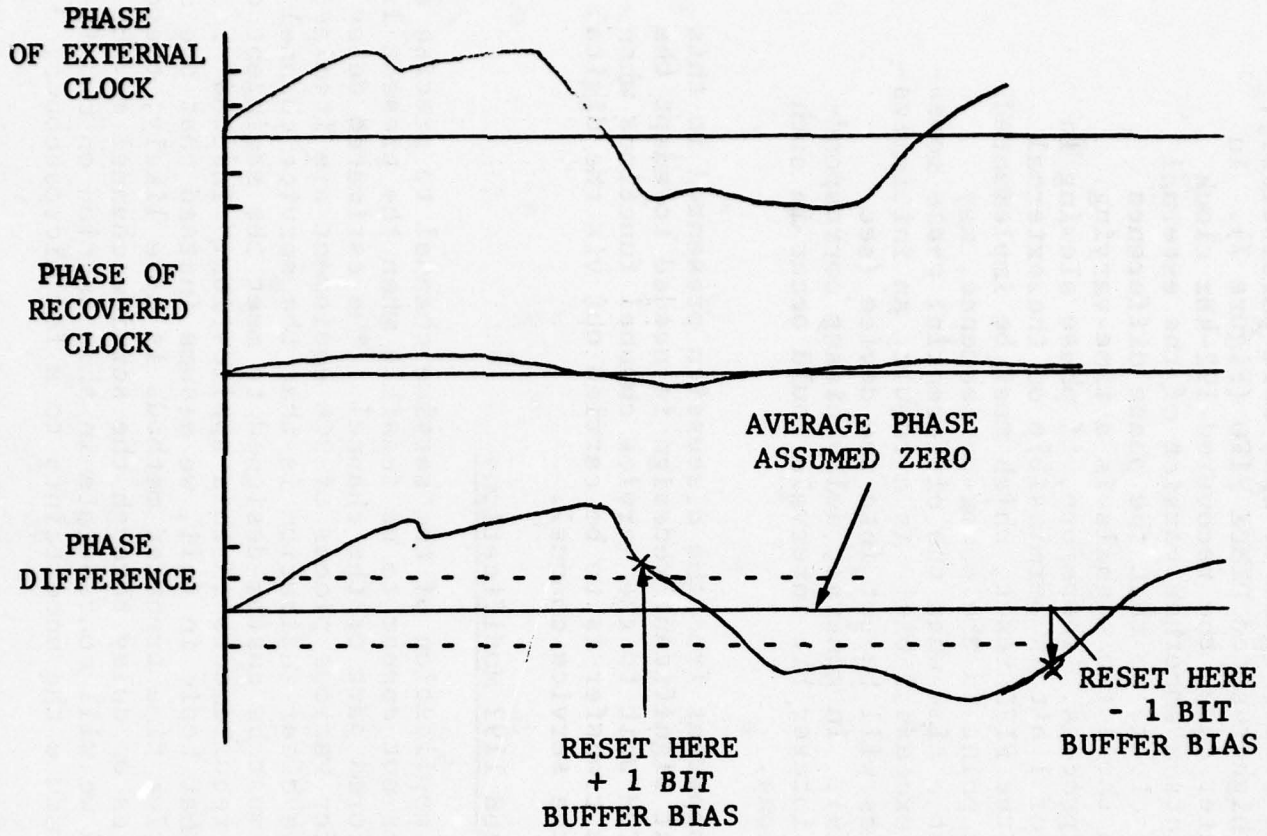


Figure 9 Clock Phase Relative to Perfect Reference and Phase Difference; Influence of Buffer Reset Time and Delay Bias

TABLE 1

SUMMARY OF WORST-CASE DCS EQUIPMENT DELAY COMPONENTS

Equipment	Function	Constant Delay (μs)	Delay Uncertainty Limits (μs)
1192 as a Service Channel MUX	56-kHz derived clock (arbitrary phasing)	0	± 9.0
	56-kHz clock jitter (pulse deletion)	0	+ 0.25
	56-kb/s FIFO's half-full (4 bits at 56 kHz)	72	±18.0
	Serial 56 kb/s / Serial 1.544 Mb/s waiting time	120	0
	Serial/parallel waiting time	4.2	0
	192-kHz clock jitter (pulse deletion)	0	+ 0.04
	NRZ receiver/driver (1 each)	?	?
1192 as a Service Channel DEMUX	192-kHz derived clock jitter	0	+ 0.04
	192-kb/s FIFO's half-full (4 bits at 192 kb/s)	20	± 5.0
	Serial/parallel waiting time	35	0
	56-kHz clock jitter (pulse deletion)	0	+ 0.25
	56-kHz derived clock (arbitrary clock phasing)	0	± 9.0
	NRZ receiver/driver (1 each)	?	?
FRC-163 Service Channel Back/Back	192-kHz synthesized clock (arbitrary phasing)	0	± 5.0
	Transmit and receive FIFO's (half-full, 32 bits each)	320	0
	NRZ receiver/driver (1 each)	?	?

TABLE 1 (Continued)

Equipment	Function	Constant Delay (μs)	Delay Uncertainty Limits (μs)
FRC-163 MBS Ports Back/Back (Worst-Case Data Rate 3.232 Mb/s)	Level-3 MUX/DEMUX (arbitrary clock phasing)	0	+ 0.3
	Transmit and receive FIFO buffers (half-full, 32 bits each)	19.2	0
	NRZ receiver/driver (1 each)	?	?
MDTS TROPO Modem Back/Back MBS Ports	Measured delay characteristics		
	at 6.276 Mb/s	6.4	$\pm$ 0.18
	at 3.088 Mb/s	10.0	$\pm$ 0.3

bit rate much less than the maximum of 64 kb/s available at the telemetry channel, and yet not compromise delay uncertainty requirements. This becomes more difficult as the data rate is reduced, as we shall now indicate.

In Figure 10, the 1192 is shown in the service channel TDM role. Then, a sub-MUX is piggy-backed onto this unit to give a lower data rate. The example used is 1200 b/s. This data stream originates at Ⓐ and must be multiplexed onto the 56-kb/s line at Ⓑ, assuming 1192 56-kb/s data interface modules are employed. This is not the best way of proceeding by any means, and under normal circumstances would introduce a $\frac{1}{2}$ bit of delay uncertainty at Ⓐ, i.e., 400 μs, and at least a $\frac{1}{2}$ bit of delay uncertainty at Ⓑ, amounting to 9 μs. With similar effects at Ⓒ and Ⓓ, the net result is a severe delay variation of at least 818 μs, which is clearly excessive. For the system described as Option B in Section 3.3, delay uncertainty must be limited to a fraction of the radio frame interval (250 μs).

The response to this dilemma must be the implementation of a tighter timing relationship between the 1192 and the sub-MUX shown in Figure 10. One approach, which assumes retention of the 1192 as the primary service channel TDM, will now be described.

Recall that the 1192 consists of a standard mainframe which accepts data from 3-, 6-, 12-, or 24-channel interface modules. The transfer is in the nature of frame-synchronized serial bursts at a 1.544-MHz rate. While the 56-kb/s synchronous interface module only sends seven valid data bits in this burst, it is clear that eight bit slots must be provided to accommodate a mixture of different module types (see Figure 11). Inside the mainframe there will be a circuit to set the frame sync bit on every 12th frame. The frame rate is 8 kHz ÷ 12, i.e., 0.66 kHz. The suggested approach is to feed serial data into corresponding unused bits (bit 8 for each byte) with similar circuitry. Some care must be exercised with regard to rate selection, however. Briefly:

- An 8-kb/s rate would annihilate the frame sync bit in the 12th data byte and necessitate DEMUX sync circuit modifications.
- With one of the unused bits out of every superframe (e.g., the unused bit in frames 6, 18, 30, etc. corresponding to the voice channel signaling bit),

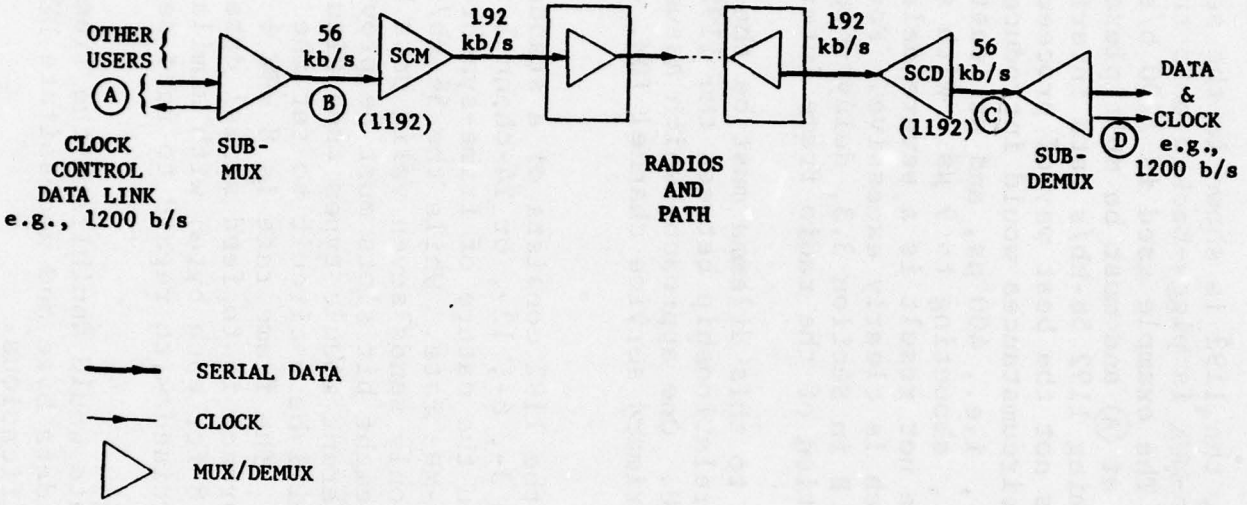


Figure 10 Sub-MUX Approach to Service Channel Partitioning

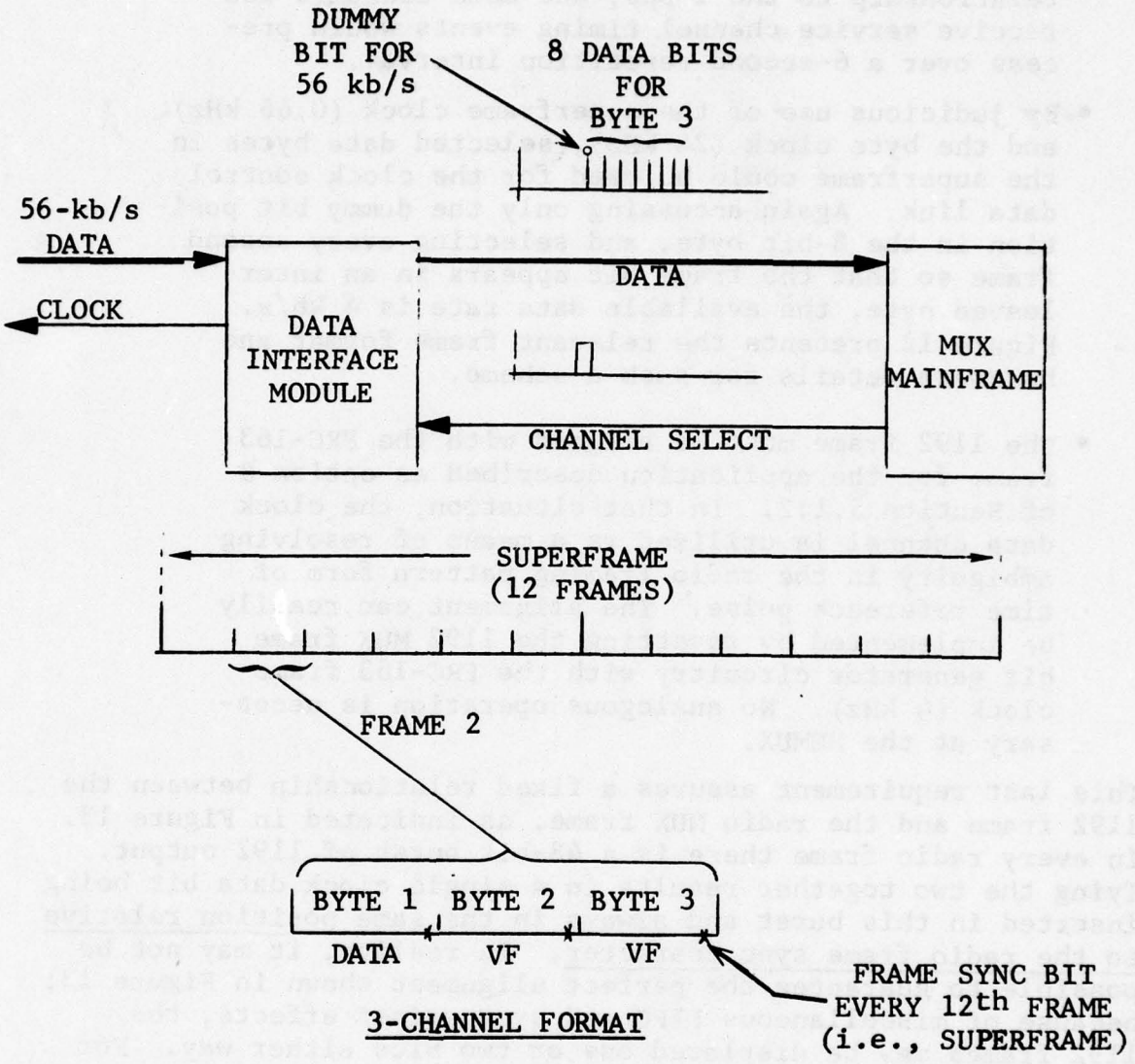


Figure 11 1192 Channel Interface Data Format and Output Frame Mapping

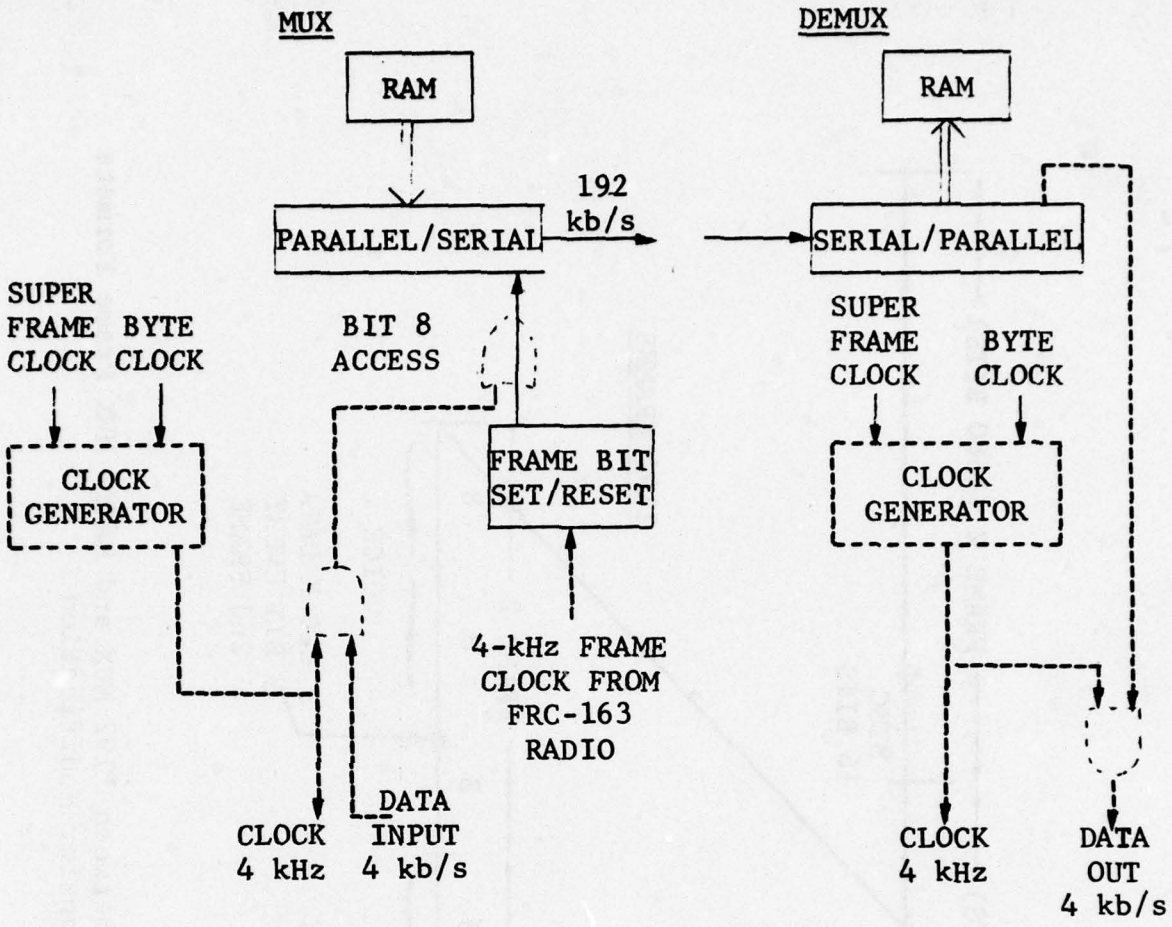
the resultant bit rate is 0.666... kb/s; this would cause some consternation because of its noninteger relationship to the 1 pps, and both transmit and receive service channel timing events would precess over a 6-second repetition interval.

- By judicious use of the superframe clock (0.66 kHz) and the byte clock (24 kHz), selected data bytes in the superframe could be used for the clock control data link. Again accessing only the dummy bit position in the 8-bit byte, and selecting every second frame so that the frame bit appears in an interleaved byte, the available data rate is 4 kb/s. Figure 12 presents the relevant frame format and hardware details for such a scheme.

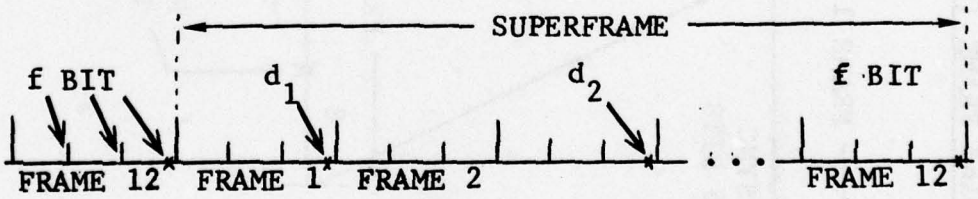
- The 1192 frame must be aligned with the FRC-163 frame for the application described as option B of Section 5.1.2. In that situation, the clock data channel is utilized as a means of resolving ambiguity in the radio framing pattern form of time reference pulse. The alignment can readily be implemented by resetting the 1192 MUX frame bit generator circuitry with the FRC-163 frame clock (4 kHz). No analogous operation is necessary at the DEMUX.

This last requirement assures a fixed relationship between the 1192 frame and the radio MUX frame, as indicated in Figure 13. In every radio frame there is a 48-bit burst of 1192 output. Tying the two together results in a single clock data bit being inserted in this burst and always in the same position relative to the radio frame sync character. In reality, it may not be possible to guarantee the perfect alignment shown in Figure 13; because of miscellaneous FIFO and synthesizer effects, the 1192 frames may be displaced one or two bits either way. For the application in question, this is more than adequate.

With the direct bit access approach described, a 4-kb/s clock control data link is established which allows full use of the 56-kb/s port for other network supervisory and control transmissions. The 4-kb/s channel will also have less delay uncertainty than the 56-kb/s port. Finally, it is clear that avoiding a further level of multiplexing (e.g., sub-MUX of Figure 10) to get the desired low rate results in a higher level of reliability and availability for the clock control data link because it does not introduce another layer of DEMUX synchronization problems.



FRAME FORMAT



d_1, d_2, d_3, ... 4-kb/s CLOCK DATA SEQUENCE

---- MODIFICATIONS SHOWN BY DOTTED LINES
—— SOLID LINES REPRESENT EXISTING DESIGN

Figure 12 Recommended Clock Control Data Link Access Method

FRC-163 FRAME (n = 2)

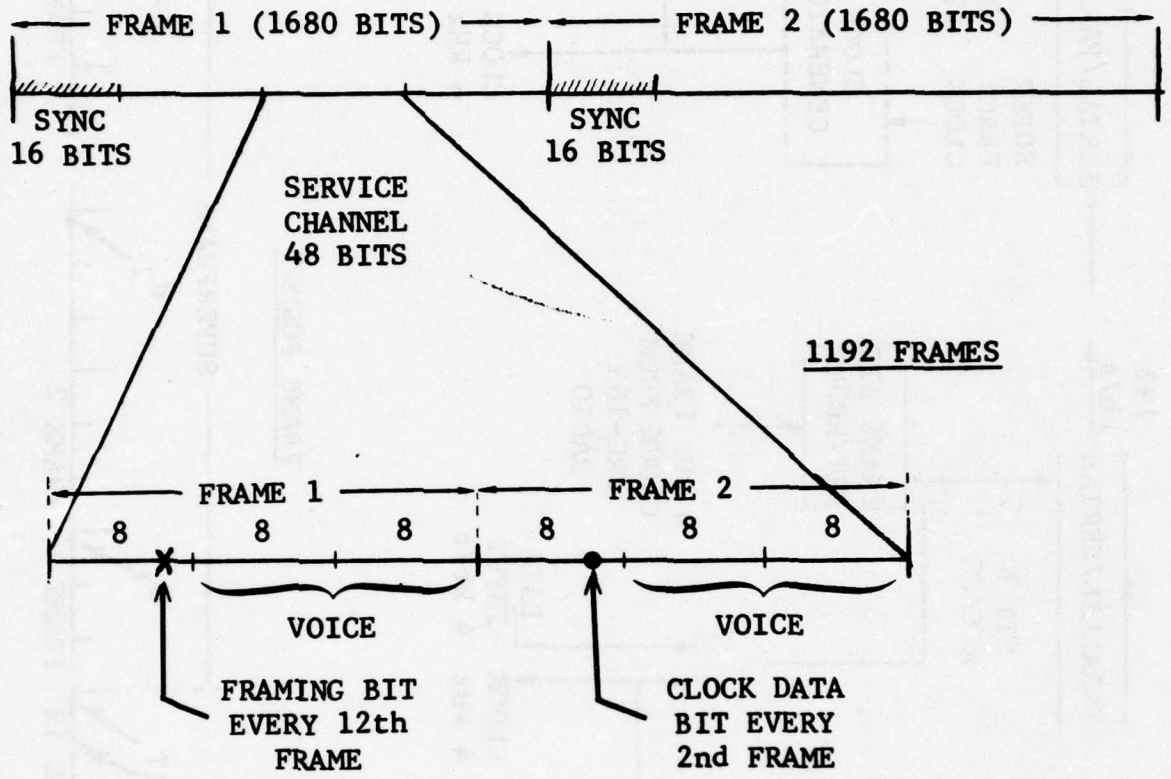


Figure 13 Relationship between 1192 MUX and Radio MUX Frame Formats after Time Transfer Modification

APPENDIX C

PATH LENGTH CALCULATIONS

During the course of the field testing, there was some confusion as to the precise location and distance between sites. A survey was carried out to provide up-to-date information; for historical purposes, we present here the results of the survey.

All survey points correspond to the physical antenna locations. Figures 1 and 2 show the geodetic parameters associated with the AN/MRC-98 and AN/TRC-132 antennas located at Verona and Youngstown sites, and microwave tower locations at Bldg. 3, Stockbridge, Verona, and Ava sites.

The geographic positions of the antennas and microwave towers were determined by field measurements extended from local primary geodetic control stations. Path distances and azimuths between these locations were then determined by computation. The estimated accuracies are as follows:

Geographic positions:	$\pm$ 0.5 meter relative to the local primary geodetic control network
Azimuths:	$\pm$ 6 seconds relative to true north
Path distances:	$\pm$ 3 meters (Verona to Youngstown)
	$\pm$ 0.5 meter (between microwave tower locations)

For completeness, the survey points and path lengths for points between Ontario Center and Verona, as well as Ontario Center and Youngstown, are given in Figures 3 and 4. The estimated accuracies are as follows:

Geographic positions:	$\pm$ 0.2 meter relative to the primary geodetic control network
Azimuths:	$\pm$ 3 seconds relative to true north
Path distances:	$\pm$ 2 meters

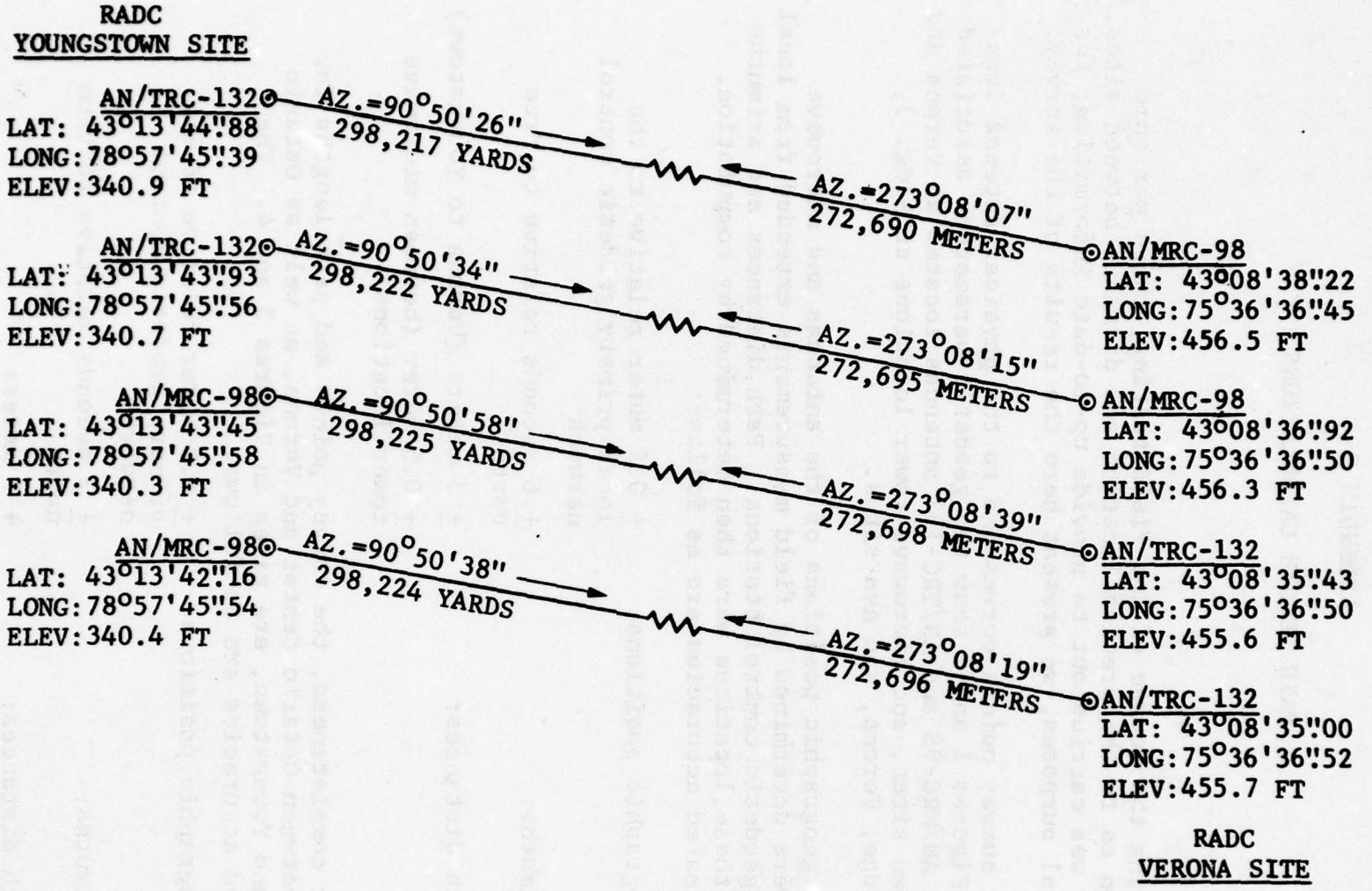
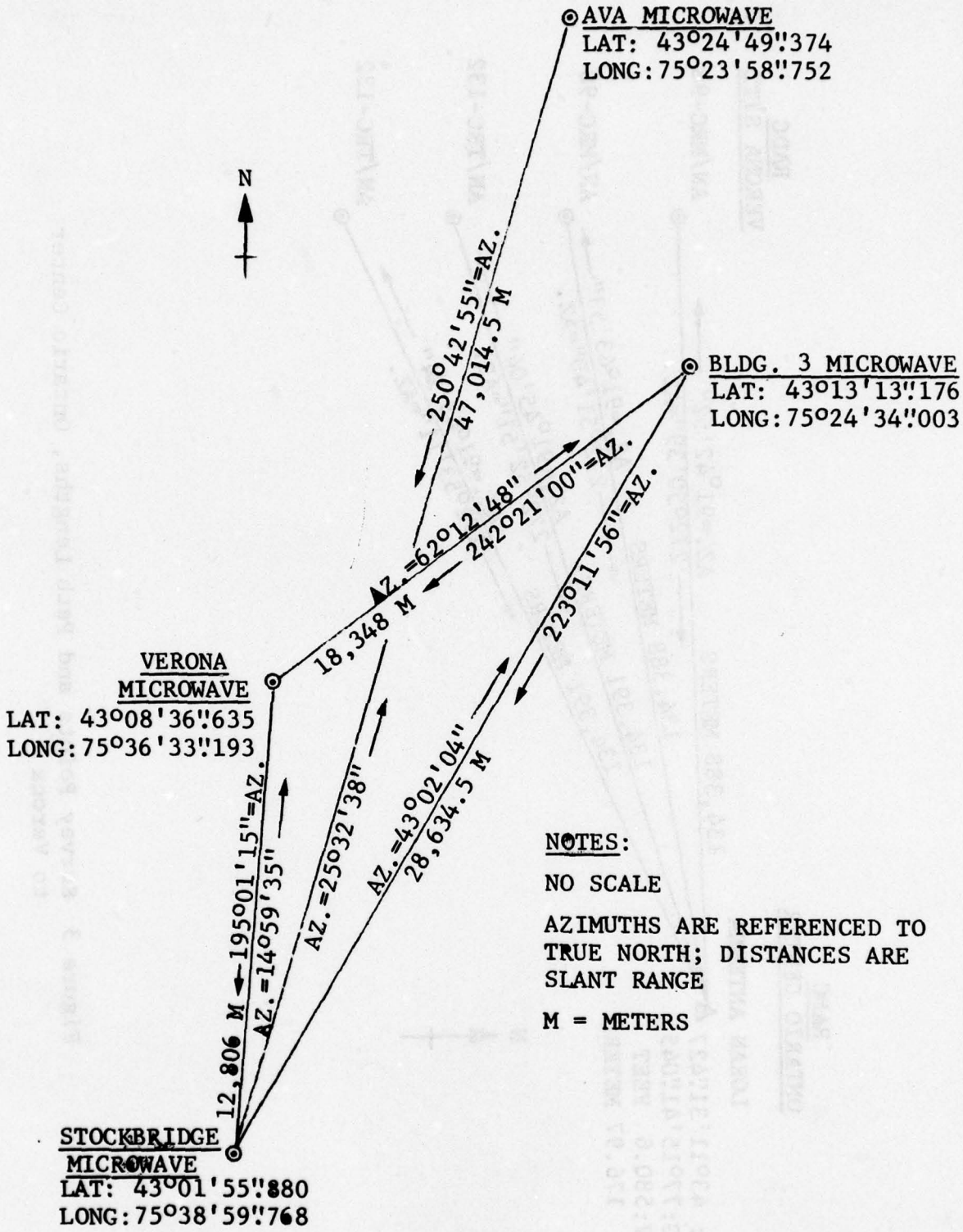


Figure 1 Location and Range Determination Plot for AN/MRC-98 and AN/TRC-132 Antennas, RADC Verona and Youngstown Sites (September 1977)



NOTES:

NO SCALE

AZIMUTHS ARE REFERENCED TO TRUE NORTH; DISTANCES ARE SLANT RANGE

M = METERS

Figure 2 Microwave Tower Survey Points
(Ava, Stockbridge, Verona, Bldg. 3)

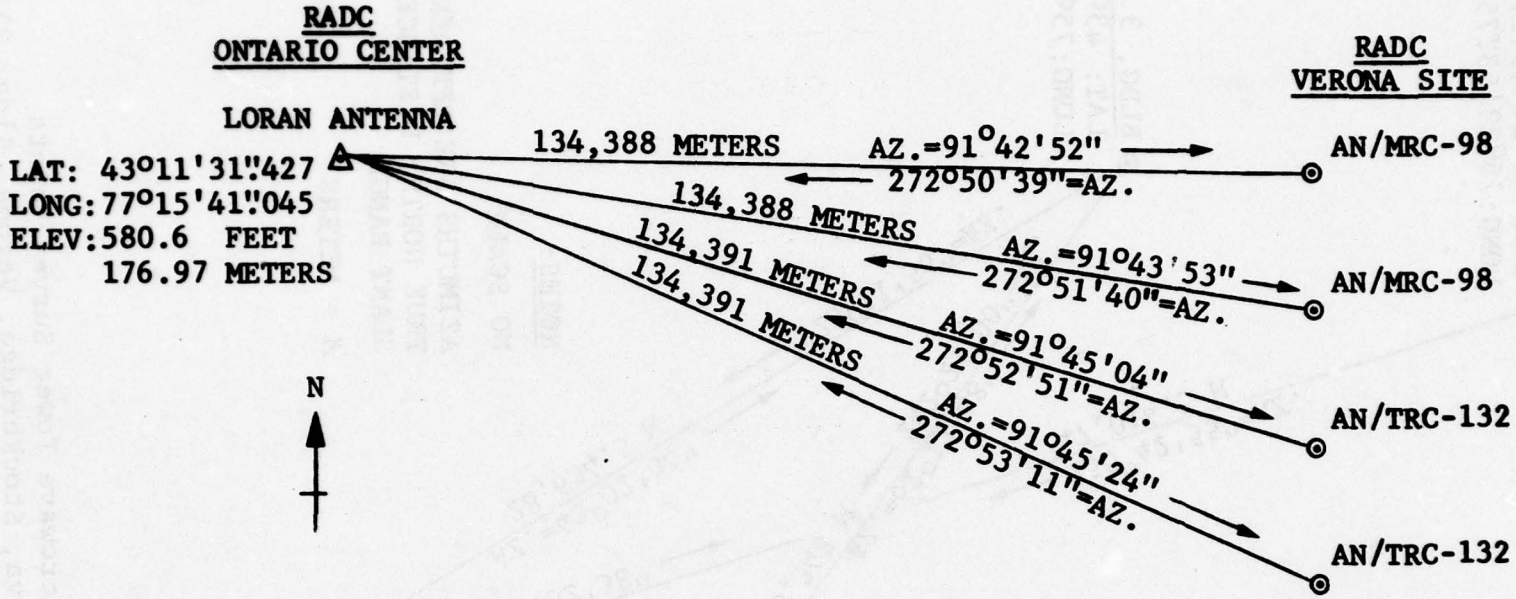


Figure 3 Survey Points and Path Lengths, Ontario Center to Verona

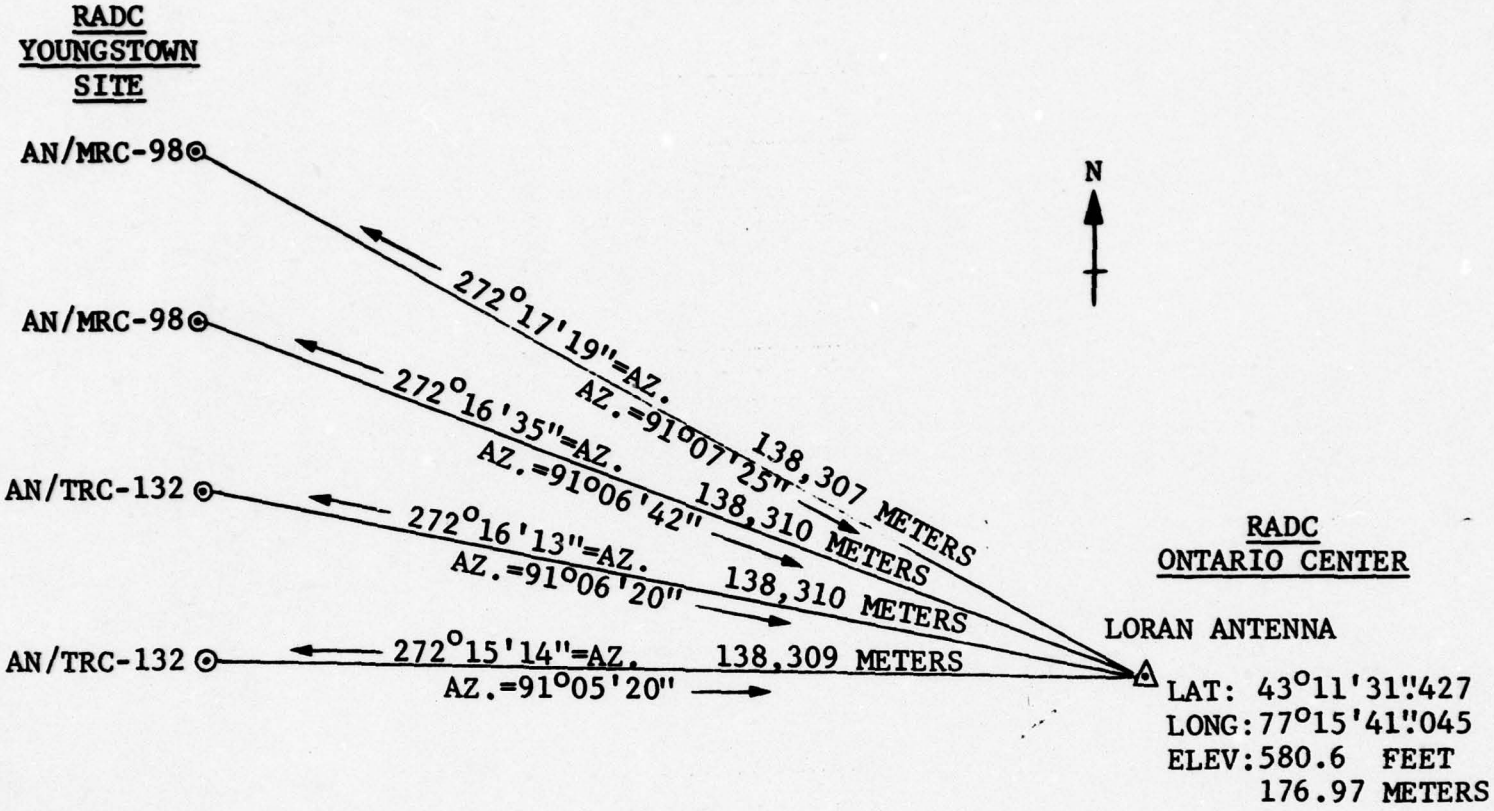


Figure 4 Survey Points and Path Lengths, Youngstown to Ontario Center

APPENDIX D

DETAILED SITE LAYOUT AND TRANSMISSION LINE DELAY ESTIMATES

D1. Site Layout

The detailed layout of both Youngstown and Verona sites is shown in Figure 1. In Figure 2 we show the equipment path and transmission line layout for the Verona-Stockbridge-Ava LOS loop. Every piece of transmission equipment and connection transmission line has been shown in order to properly account for the delay components introduced into the system.

D2. Cable and Waveguide Delay Estimates

A summary of the parameters used to compute waveguide and coax delay is given in Table 1.

For coaxial cable with a polyethylene dielectric, the following equations apply (RG-214 and RG-58):

$$\epsilon_r = 2.3 \text{ for polyethylene}$$

$$\frac{v}{c} = \frac{1}{\sqrt{\epsilon_r}} = \frac{1}{\sqrt{2.3}} = 0.66$$

T = time delay in seconds/unit length

$$= \frac{1.016 \times 10^{-3}}{\frac{v}{c}} = 1.016 \times 10^{-3} \sqrt{\epsilon_r} \quad \text{microseconds/ft}$$

$$= 1.016 \sqrt{\epsilon_r} \quad \text{nanoseconds/ft}$$

$$= 1.016 \times \sqrt{2.3} = 1.54 \text{ nanoseconds/ft}$$

Hence, delay for RG-58C/U and RG-214/U is 1.54 nanoseconds/ft.

For rectangular waveguide with dimensions x_0 and y_0, we have the following parametric relationships:

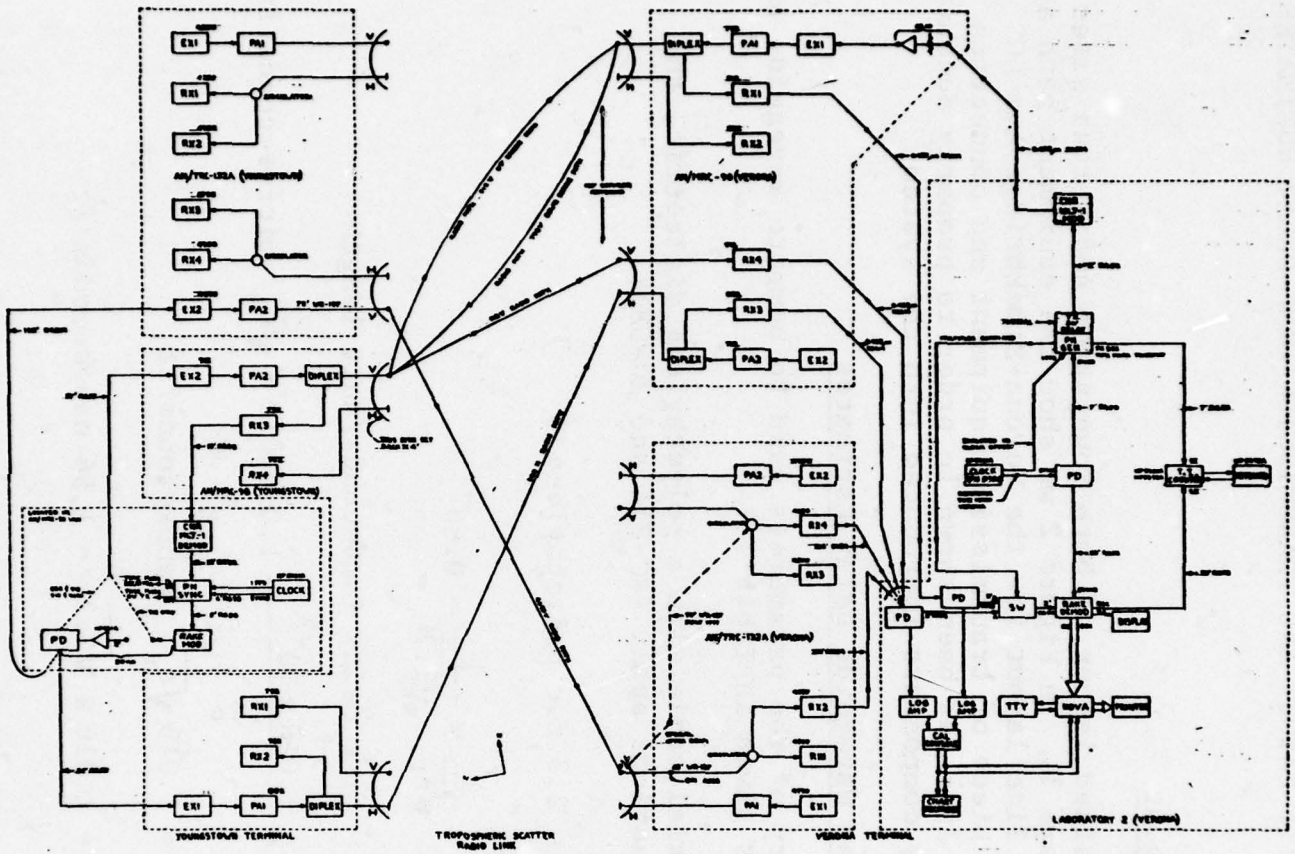


Figure 1 Youngstown and Verona Site Layouts

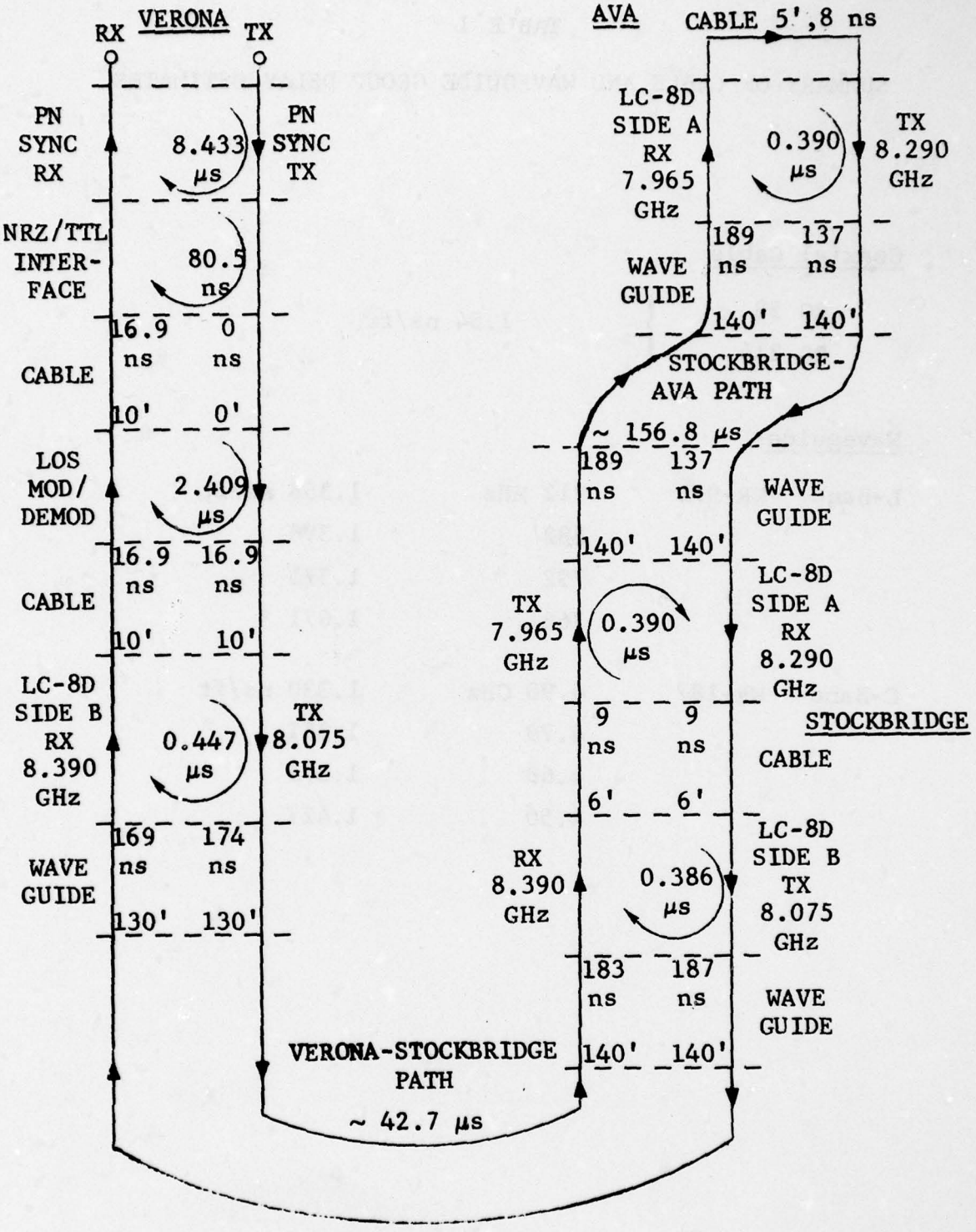


Figure 2 LOS Loop Equipment, Cable, and Path Delay Estimates

TABLE 1

SUMMARY OF CABLE AND WAVEGUIDE GROUP DELAY ESTIMATES

Coaxial Cable

RG 58 RG 214	1.54 ns/ft

Waveguide

L-Band	WR-975	912 MHz	1.358 ns/ft
		882	1.396
		792	1.575
		762	1.671
C-Band	WR-187	4.90 GHz	1.330 ns/ft
		4.79	1.351
		4.69	1.375
		4.50	1.427

$$\left(\frac{\lambda_2}{\lambda}\right)^2 = \left(\frac{\text{Guide Wavelength}}{\text{Free Space Wavelength}}\right)^2$$

$$\left(\frac{\lambda_g}{\lambda}\right)^2 = \frac{1}{\left[1 - \left(\frac{\lambda}{\lambda_c}\right)^2\right]}$$

where

$$\left(\frac{1}{\lambda_c}\right)^2 = \left(\frac{1}{\text{Cutoff Wavelength}}\right)^2$$

$$= \left(\frac{m}{2x_0}\right)^2 + \left(\frac{n}{2y_0}\right)^2$$

For TE_{10} mode, $m = 1$, $n = 0$:

$$\left(\frac{1}{\lambda_c}\right)^2 = \left(\frac{1}{2x_0}\right)^2$$

$$\boxed{\lambda_c = 2x_0}$$

Group velocity

$$u = \frac{c^2}{v}$$

When phase velocity $v = c\frac{\lambda_g}{\lambda}$,

$$u = c^2 \frac{\lambda}{c\,\lambda_g} = c\left(\frac{\lambda}{\lambda_g}\right)$$

but

$$\frac{\lambda_g}{\lambda} = \frac{1}{\sqrt{1 - \left(\frac{\lambda}{\lambda_c}\right)^2}}$$

$$u = c\sqrt{1 - \left(\frac{\lambda}{\lambda_c}\right)^2}$$

$$\boxed{u = c\sqrt{1 - \left(\frac{f_c}{f}\right)^2}} \quad \text{when } f_c = \text{cutoff frequency}$$

$$= c\sqrt{1 - \left(\frac{\lambda}{2x_0}\right)^2}$$

$$\left(\frac{u}{c}\right) = \sqrt{1 - \left(\frac{f_c}{f}\right)^2}$$

In TE_{10} rectangular waveguide mode:

$$\frac{u}{c} = \frac{\text{Group Velocity}}{\text{Velocity Free Space}}$$

$$= \sqrt{1 - \left(\frac{\text{Cutoff Frequency}}{\text{Operating Frequency}}\right)^2}$$

Example 1:

C-Band: RG-49/U; TE_{10} Mode; WR-187 (2" x 1")

Frequency Range: 3.95 to 5.85 GHz
Cutoff Frequency: 3.16 GHz

At 4.69 GHz,

$$\frac{u}{c} = \sqrt{1 - \left(\frac{3.16}{4.69}\right)^2} = 0.73894$$

Example 2:

L-Band: RG-204/U; WR-975

Frequency Range: 0.75 - 1.12 GHz
Cutoff Frequency: 0.605 GHz

For the frequencies of interest, we have:

(1) 912 MHz

$$\frac{u}{c} = \sqrt{1 - \left(\frac{605}{912}\right)^2} = 0.748$$

(2) 882 MHz

$$\frac{u}{c} = \sqrt{1 - \left(\frac{605}{882}\right)^2} = 0.728$$

(3) 792 MHz

$$\frac{u}{c} = \sqrt{1 - \left(\frac{605}{792}\right)^2} = 0.645$$

(4) 762 MHz

$$\frac{u}{c} = \sqrt{1 - \left(\frac{605}{762}\right)^2} = 0.608$$

The group delay is now computed from:

$$T_g = \frac{L \text{ meters}}{u \text{ m/s}} = \frac{L}{c\sqrt{1 - \left(\frac{f_c}{f}\right)^2}}$$

Let L = 1 foot; then,

$$\frac{L}{c} = 12 \times \frac{.1}{39.37} \times \frac{\text{sec}}{3 \times 10^8}$$

$$= \frac{12}{39.37 \times 3} \times 10^{-8} = 1.016 \text{ nanoseconds/foot}$$

$$T_g = \frac{1.016}{\sqrt{1 - \left(\frac{f_c}{f}\right)^2}} \quad \text{nanoseconds/foot}$$

$$= \frac{1.016}{\frac{u}{c}} \quad \text{nanoseconds/foot}$$

With the values of u/c previously established, we can directly calculate the group delay parameters shown in Table 1.

The MRC-98 transmission line delays are summarized in Table 2.

TABLE 2

SUMMARY OF TRANSMISSION LINE DELAYS (MRC-98)

Verona		
VAN 1	TX792 (V)	128 ns
	RX912 (V)	138 ns
	RX882 (H)	116 ns
VAN 2	TX762 (H)	134 ns
	RX882 (H)	140 ns
	RX912 (V)	116 ns
Youngstown		
VAN 1	TX912 (V)	112 ns
	RX792 (V)	158 ns
	RX762 (H)	121 ns
VAN 2	TX882 (H)	114 ns
	RX762 (H)	166 ns
	RX792 (V)	119 ns

Down Range:

792 (V) 128 + 158 = 286 ns

Up Range:

912 (V) 112 + 138 = 250 ns

Total Loop Delay = 536 ns

APPENDIX E

MEASURED DELAY POWER SPECTRA

In the following figures we have presented a selection of delay power spectra, all measured at the Verona site during the March/April series. They are typical of the complete data set for the 912 MHz link. Data for the other Youngstown/Verona links is available but has not been plotted to date.

Although similar plots have been presented by others in the past, very few RAKE tests have been carried out at Verona with the 5 Mb/s signaling rate. This choice allows the RAKE window to cover a full 2 μs, thereby giving a more complete indication of spectra tail behavior. The delay coordinates shown in the figures indicate delay relative to the first RAKE tap.

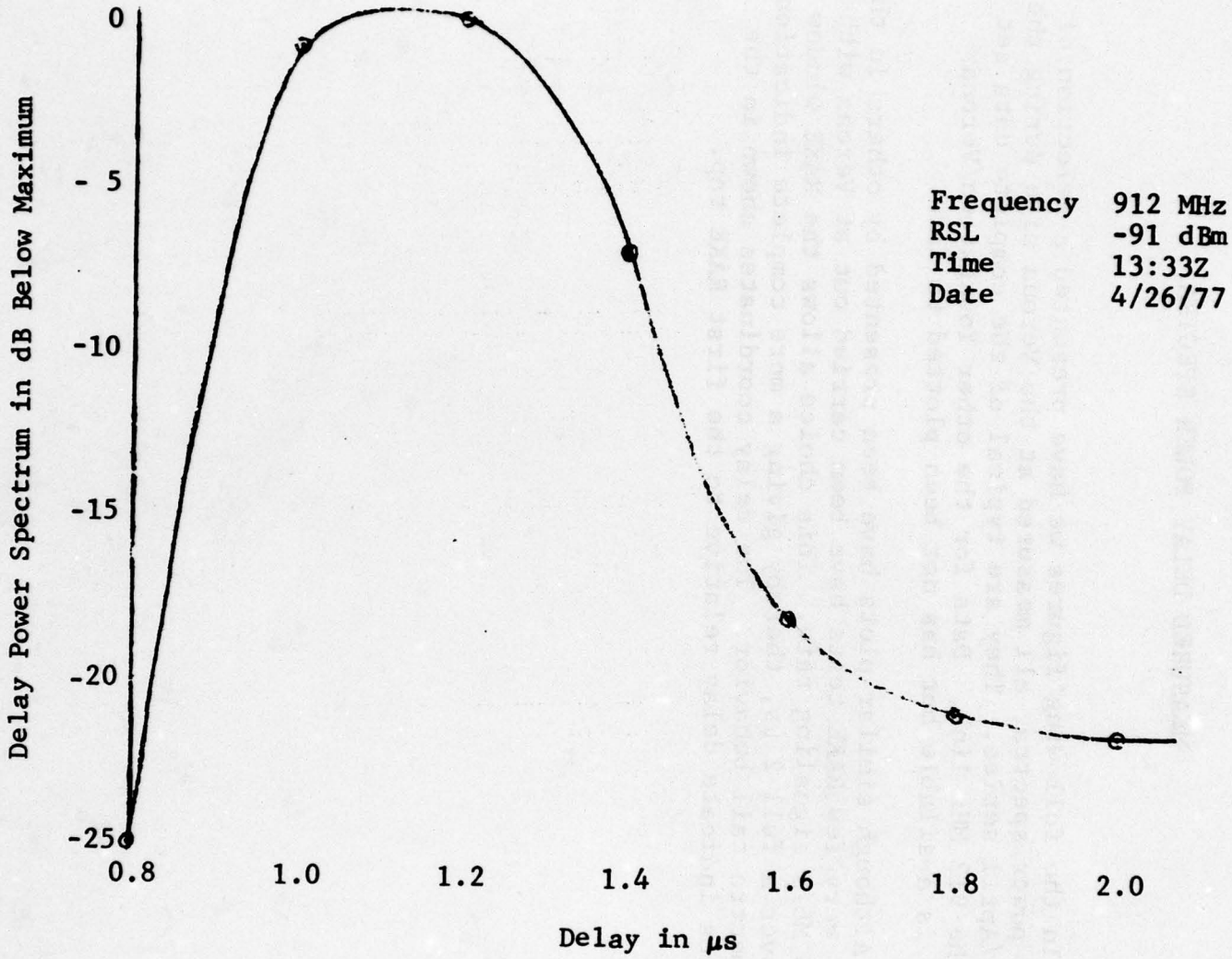


Figure 1 Verona to Youngstown Delay Power Spectrum

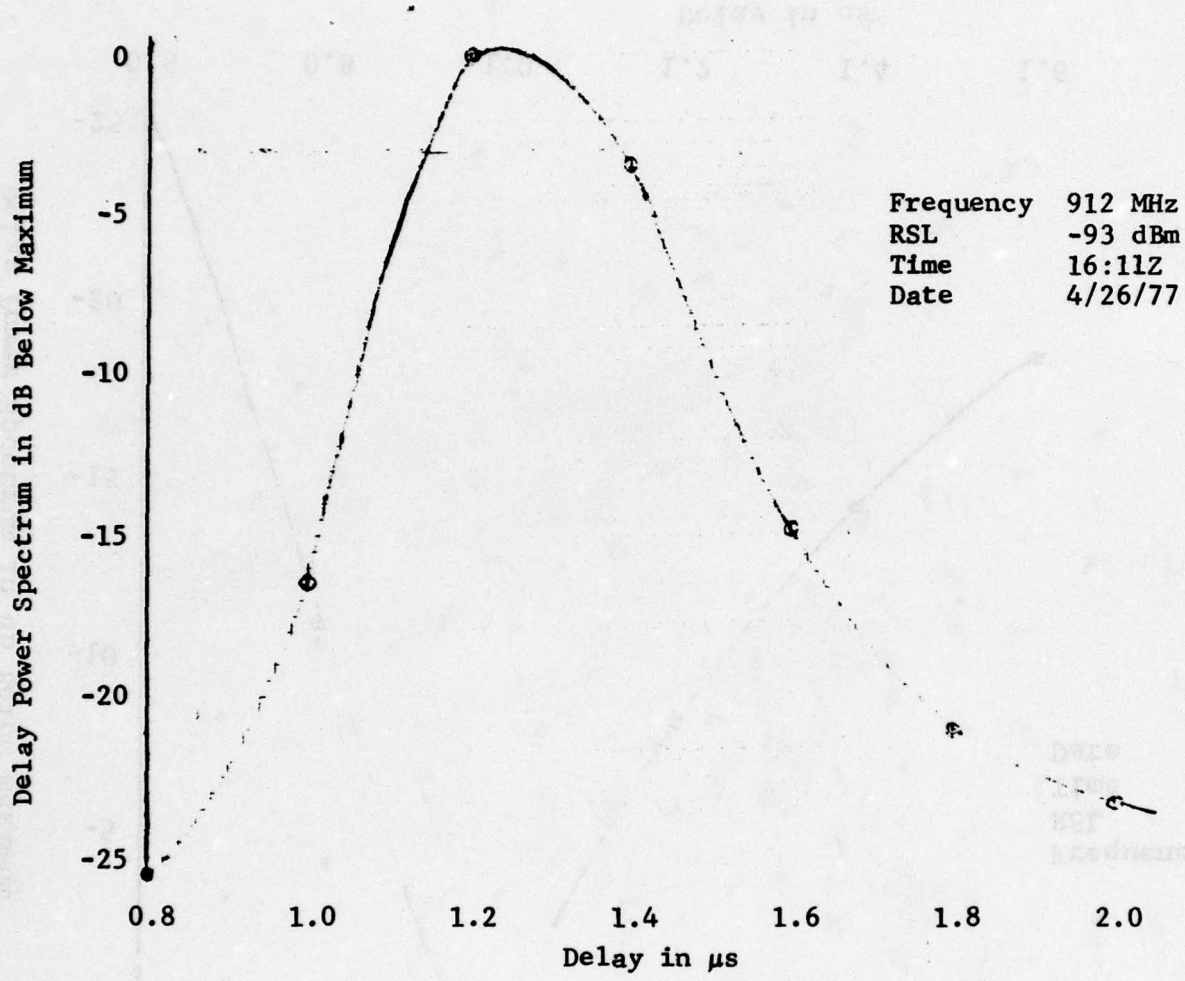


Figure 2 Verona to Youngstown Delay Power Spectrum

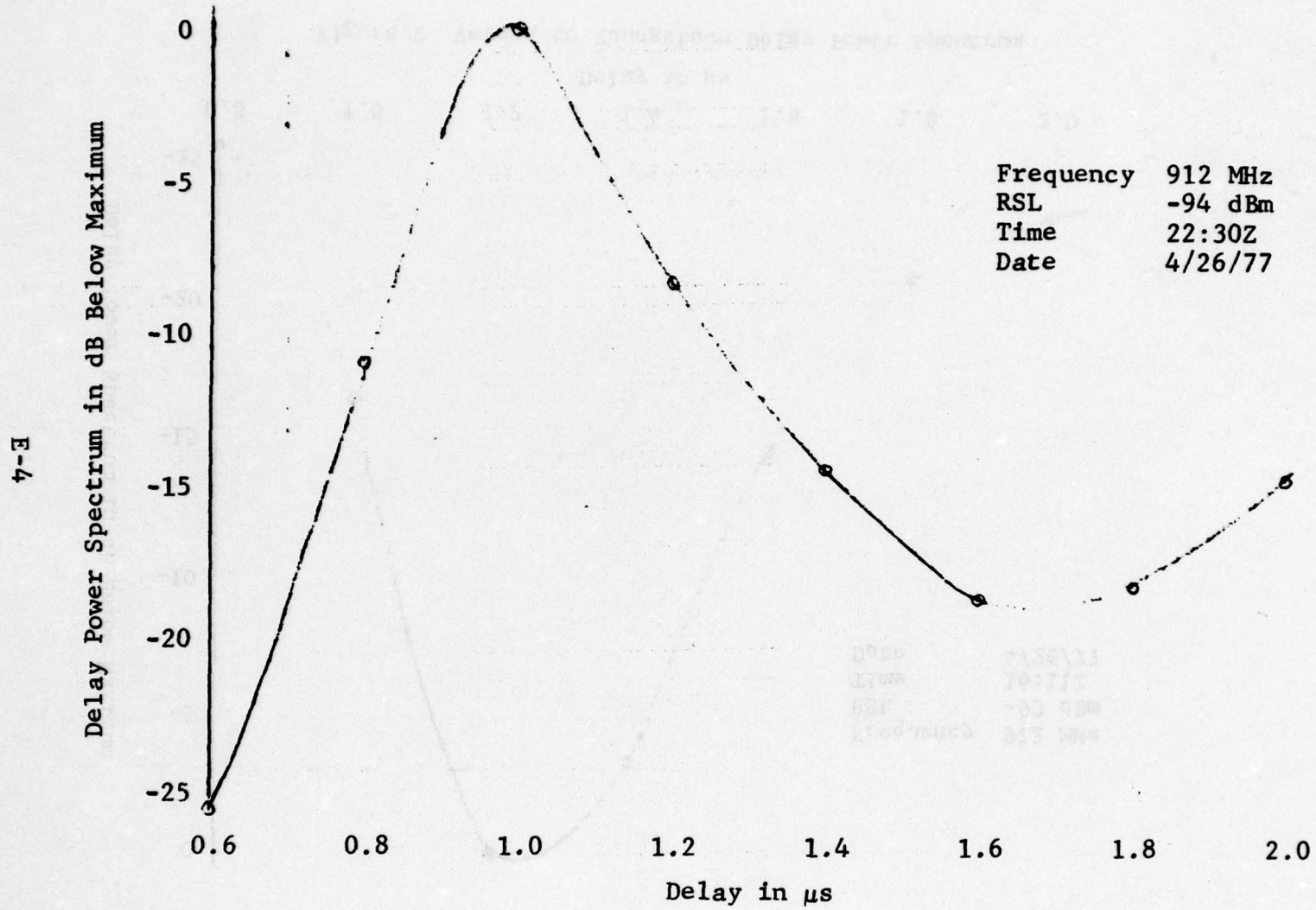


Figure 3 Verona to Youngstown Delay Power Spectrum

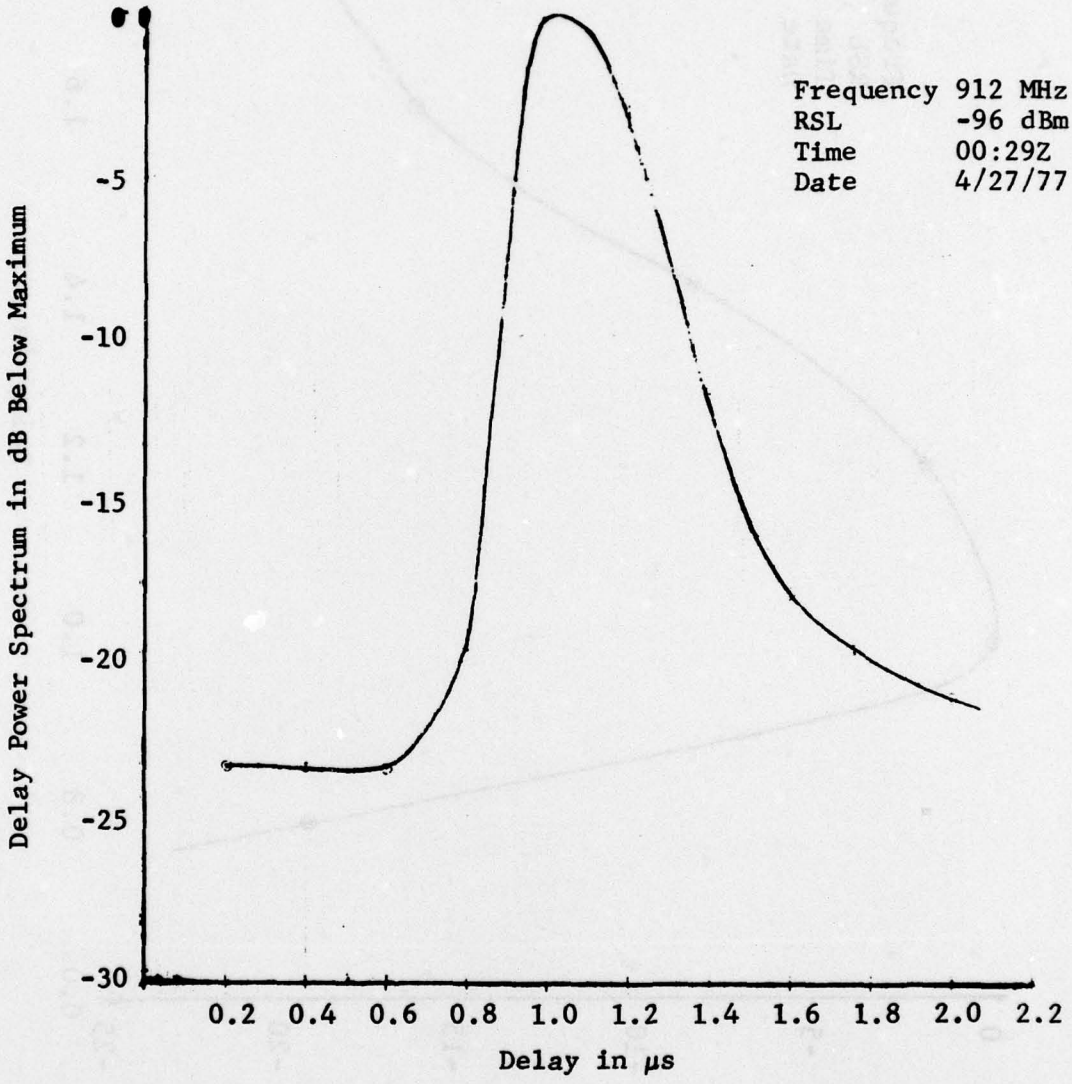


Figure 4 Verona to Youngstown Delay Power Spectrum

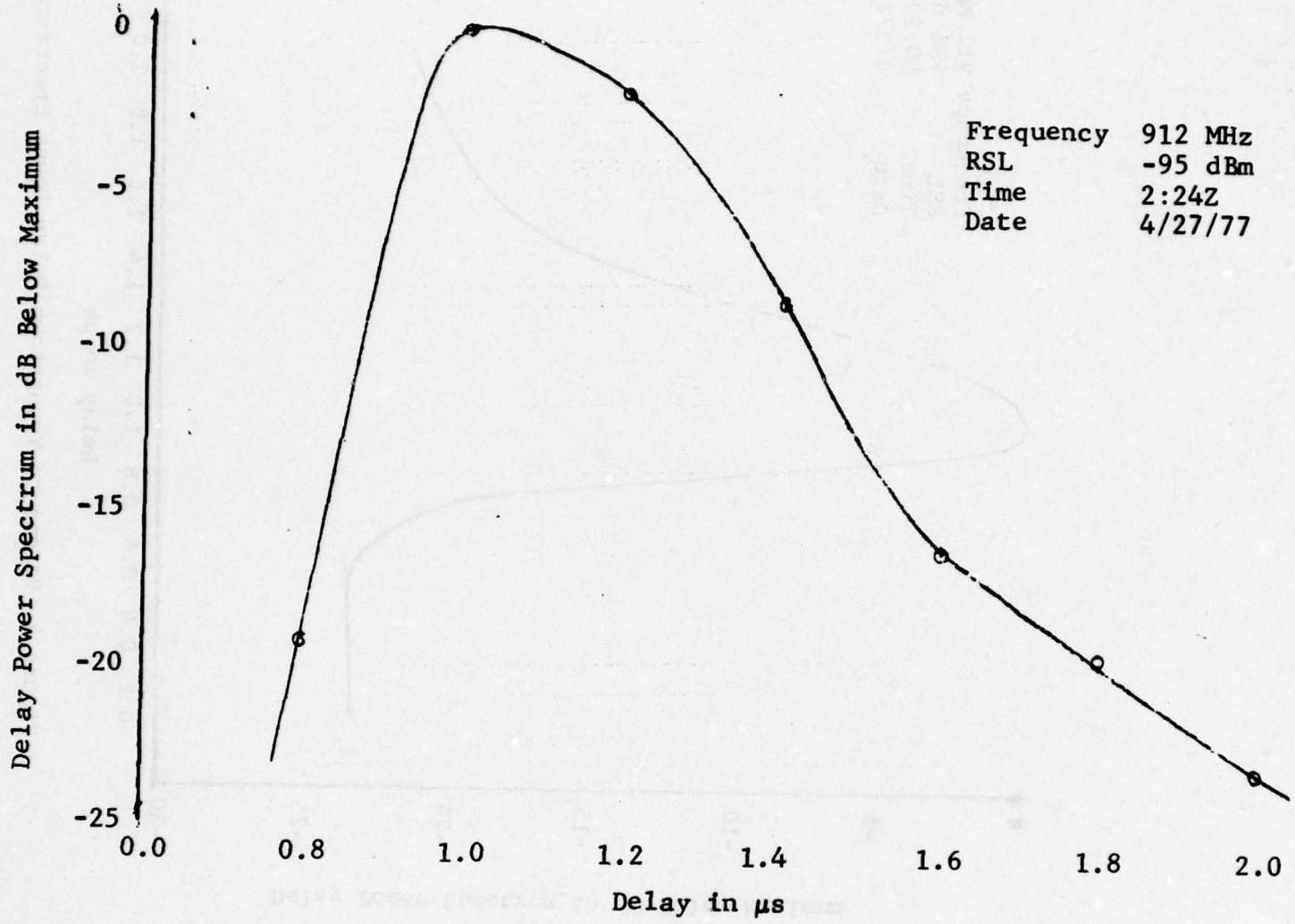


Figure 5 Verona to Youngstown Delay Power Spectrum

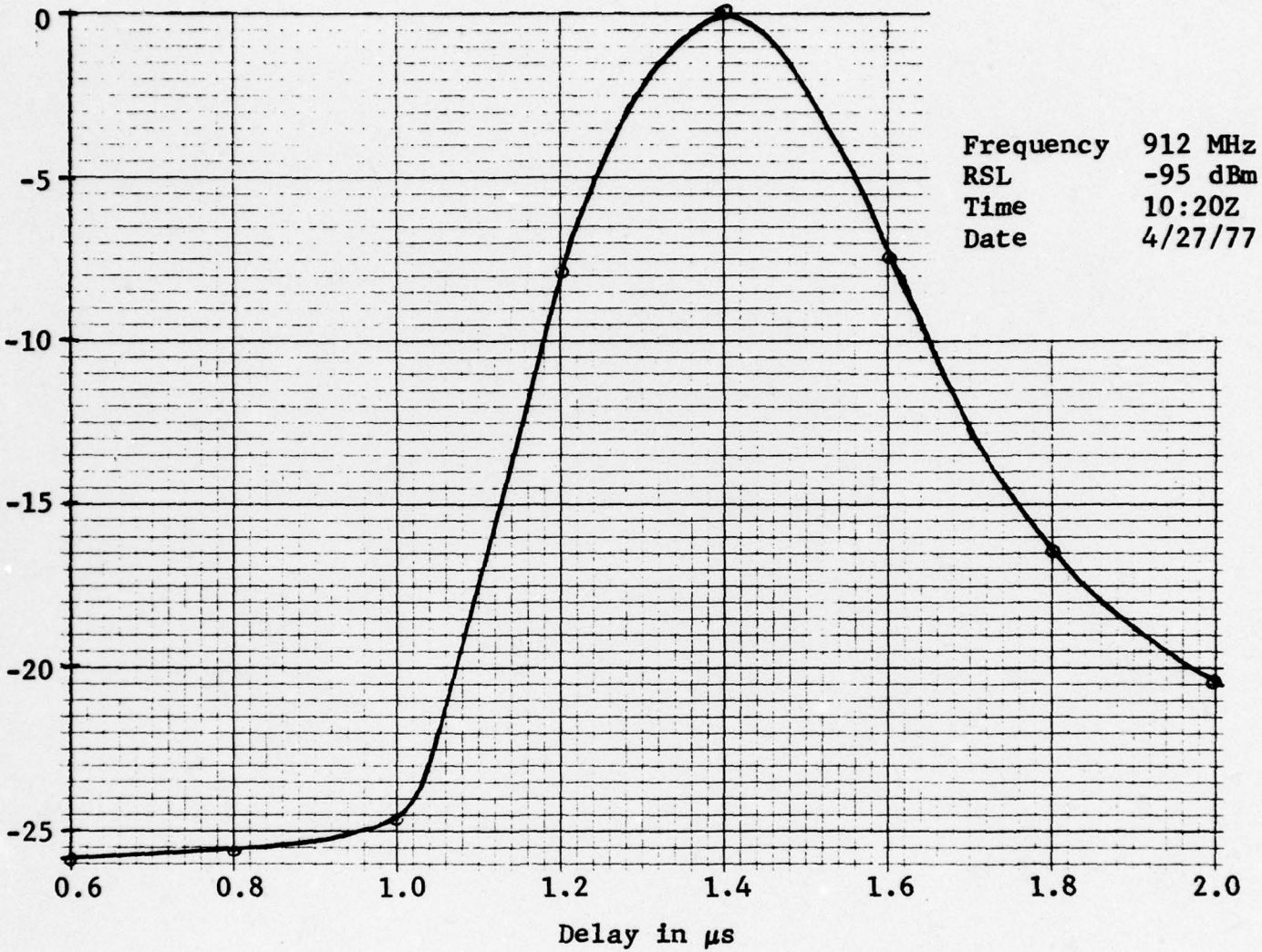


Figure 6 Verona to Youngstown Delay Power Spectrum

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