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SHIPBOARD DATA MULTIPLEXING SYSTEM, ENGINEERING DEVELOPMENT MOD--ETC(U)
JUN 78 W M GREGORY N00024-78-C-7129

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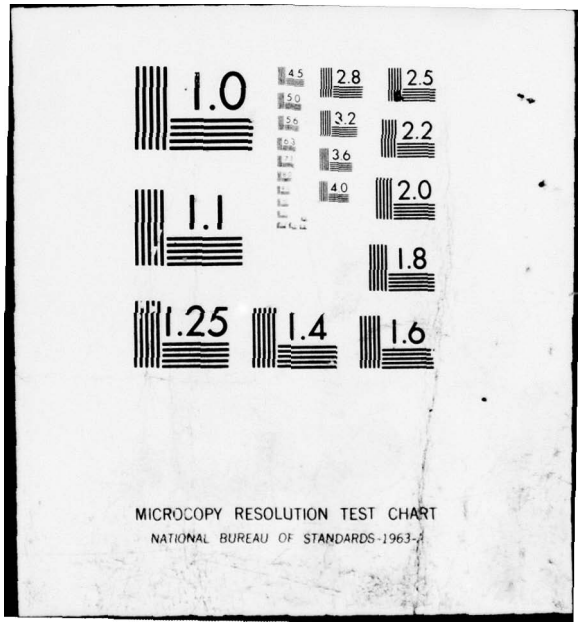
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LEVEL II

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(14) C78-500.2/301

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(6) Shipboard Data Multiplexing System, Engineering Development Models (SDMS-EDM).

LEVEL

SDMS-EDM

REPORT, TECHNICAL (9) INTERIM PROGRESS rept. no. 2,

PREPARED UNDER CON (15) N00024-78-C-7129

for

THE DEPARTMENT OF THE NAVY
NAVAL SEA SYSTEMS COMMAND

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CONTENTS

ILLUSTRATIONS

TABLES

1.0 SUMMARY

This is the second monthly progress report submitted under Contract N00024-78-C-7129 for the development, test and delivery to the U.S. Navy, Naval Sea Systems Command, of two (2) Engineering Development Models (EDM) of a Shipboard Data Multiplexing System (SDMS). Activity during this reporting period is reflected in the program overview chart of Figure 1 with in process or completed efforts indicated by darkened triangles.

Technical progress on the program during this report period was slowed, somewhat, due to the following EDM related items:

a) Priority placed on getting the ADM system at NOSC up to par for their design baseline tests.

b) Unscheduled task requests from NAVSEC (data terminal turn-around, common MPUs, etc.).

c) Rescheduling due to FY78 funding constraints.

While the above described task assignments are conflicting with some of our internal plans and schedules, they do not at this time represent any changes to the major program objectives (i.e., CDR, hardware ship, etc.).

During the regularly scheduled program review, held on 24 and 25 May, we were able to reach an accord with the Navy on a technical baseline for the EDM program. This, of course, is a necessary prelude to contract definitization.

Other continuing efforts during this report period include:

a) Basic Hardware Definition

b) Basic Hardware Design

c) Software Definition and Design

d) Prepartion of Detail Schedules for all EDM Program Activities

e) D^3 Preparation

f) Establishment of Firm Technical Baseline

As indicated in item d) above, preparation of detail schedules is in process and will be included in subsequent reports as they become available.

Also, it is to be noted that in addition to the technical progress, which is CDRL Sequence No. A02V, this report covers the progress and/or status of the following EDM activities:

a) Reliability Status (A005)

b) Maintainability Status (A012)

c) LOR Status (A02H)

d) Technical Manual Status (A00F)

2.0 TECHNICAL PROGRESS

2.1 General

Per mutual agreement of the Navy and Rockwell's Program Office, top priority was assigned to resolving technical problems on the design baseline system at NOSC, San Diego. The motivation behind this request is to minimize carry over problems from ADM and SA-SDMS equipment into the EDM design. This effort included the following tasks:

1. Correct all problems on the system as installed.
2. Integrate the AM Loader and Cable Loader into the system and verify proper operation.
3. Reconfigure the ADM system (by adding sink/source PROMS) to test system load characteristics per an NOSC test plan.

The first task was initiated in April and, in combination with task 2, was successfully completed during this reporting period. In addition, the MU operational integrity was verified. The detected error rate was observed to be within the acceptable range.

After reconfiguration (task 3), a significant and unacceptably high detected error rate was observed. This condition is still being investigated.

2.2 Prime Mission Equipment

2.2.1 Traffic Controller (TC)

The technical proposal depicts a TC configuration that is externally controllable via the test connector. Investigation into

2.2.1 (Continued)

the requirements for mechanizing this feature indicated that 16 additional wires would have to be added to the TC wire harness. The addition of these connections exceeds the pin availability on the test connector. Since this capability is not a specification requirement, and is considered by Rockwell to be in the "desired" category, the added cost for its implementation is considered not warranted. Hence, we plan to discuss the possibility of not incorporating this feature at the next program review meeting. The TC operational configuration will be established by a pre wire strap installed on the TC logic module.

Preliminary design of the TC logic module has been started. The TC/Cable Loader interface is being mechanized to eliminate the need for a special adapter which interfaced with the logic module test point connector. This will be accomplished by incorporating two buffer ICs and four resistors on the TC logic module and using the originally specified test connector.

2.2.2 Area Multiplexer (AM)

Preliminary logic design of the cable controller module has been completed and the parts are now being ordered for breadboard fabrication.

Preliminary concepts have been developed for mechanizing the AM configuration monitor and RM Address (RMID) compare functions.

2.2.3 Remote Multiplexer (RM)

1. The RM functional requirements to meet the unique "smart users" requirements and Remote PROM Control were discussed and agreed to during the 5/10/78 program review at Autonetics.
2. Customer comments on the EDM technical proposal were revised, discussed and are being incorporated in D^3.
3. Changes to the EDM spec (pp. 16, 17, 17A, 18, 18A and 18B, dated 5/18/78) were received and are being reviewed by Autonetics Engineering for consistency with prior technical agreements and for potential cost impact.
4. The RM Controller Unit (CU) design is presently being reviewed to expand its memory size from 4K to 6 or 8K. Anticipate this decision to be made during the next report period.
5. Preliminary concepts for implementing an intra-RM data transfer capability were developed and presented to the Navy. Refinement of these concepts and customer coordination continues.

2.2.4 Input/Output Unit (IOU)

Preliminary design of the IOM logic for the IOM/TIB interface indicates that a single file design is preferred over the dual file design. The same functional TIB interface is provided with simpler overall logic (less complex and less hardware required). The first cut detail design of the dual redundant IOM EMR logic is complete.

2.2.5 Maintenance Unit (MU) and Peripherals

Nothing to report.

2.2.6 System

2.2.6.1 RF Transceivers

The FM detector zero-crossing test described in last month's report was incorporated in the RF Transceiver test procedure. An additional test to measure the "xen" (enable transmit) turnoff delay has also been added to the procedure. Four ADM modules have been successfully tested to the new requirements.

Continuing operation of the ADM hardware at NOSC has demonstrated significant improvement in system operation with the implementation of the RF Transceiver and RF Cable fixes.

The EDM Local Oscillator (L.O.) driver stage was redesigned to provide a more consistant RF drive level over the operating bandwidth. An interactive computer program was written to facilitate tolerance analysis of the network. A breadboard unit was built to verify the computed response; with acceptable results. This driver stage is being incorporated into the EDM Transceiver breadboard for interface tests.

Work is underway to generate the RF power budget as requested by NOSC. Initial emphasis will be placed on obtaining a statistical model of the FM detection process to assess the false alarm characteristics.

2.2.6.2 Cables and Miscellaneous Bus Hardware

Nothing to report.

2.2.6.3 Battery Pack Assembly

Nothing to report.

2.2.6.4 Power Supplies

Nothing to report.

2.2.6.5 Mechanical and Environmental Considerations

A study of airborne/structureborne noise, as applicable to our EDM packaging requirements and design solutions, continues with two primary outputs during this report period as follows:

1. An internal report was prepared which summarizes the airborne/structureborne noise requirements for the SDMS-EDM throughout its evolution (this includes data taken at NOSC on the SA-SDMS-RM).
2. A preliminary specification was generated for the EDM fan. RFQ's were sent out to potential suppliers and we are awaiting their response.

A thermal analysis was completed and will be summarized in a report scheduled for completion early next month.

Design layout of the RM and the 16-module IOU continues with developmental analysis supporting the design effort.

An analysis is currently underway to determine IOU cooling requirements for an ambient temperature of 65°C. Feasibility of meeting this ambient condition without drastic changes to the planned configuration will be included in the analysis.

2.2.7 Input/Output Modules

New requirements for eleven IOMs were described in last month's report. The remaining eight IOM requirements were reviewed during this period for feasibility, cost and potential problem areas. No significant problems were identified. A summary of old and new requirements for the aforementioned eight IOMs is provided in Table 1.

The high input impedance requirement for the DC Analog input module, which was discussed in last month's progress report, was found to be based on a yet undefined, but potentially existent application. The problem of implementing this tight tolerance requirement is primarily cost (i.e., the technical risks do not appear to be excessive). With this in mind, Rockwell plans to proceed with the implementation of this requirement. Should the need for this input impedance value fail to materialize, the change to a more practical value could be easily implemented.

2.2.8 Design-to-Cost (DTC)

A contractural baseline is being established in preparation for generation of the DTC Plan, CDRL Seq. #A034. Other related issues such as production WBS, establishment of DTC targets and requirements of CDRL A035 (DTC Report) are being examined to determine their influence on the DTC Plan.

The computer program used to support DTC efforts on the SA-SDMS program is being reviewed for applicability to CDRL A035 requirements.

Activity expected during the next status reporting period will include the drafting of the DTC Plan.

TABLE I - IOM REQUIREMENT COMPARISON

O L D	N E W
Synchro Input, Dual/Single Speed 1. Accuracy ± 1/2 LSB ± 0.25 degree	Synchro Input, Dual/Single Speed 1. Accuracy is defined for each type of operation and gear ratio - requires significant data processing to perform, but low technical risk
Synchro Output, Dual/Single Speed 1. Waveform distortion, total harmonies (maximum) is 5%	Synchro Output, Dual/Single Speed 1. Waveform distortion, total harmonies (maximum) is 10%
NRZ Serial Data Input/Output (NATO)	NRZ Serial Data Input/Output (NATO) No changes.
High Speed Serial Data Input (NATO) 1. RAM buffer size is 1024 bits 2. EMR timer: 100-5000 μs ± 20%	High Speed Serial Data Input (NATO) 1. RAM buffer size if 4096 bits 2. EMR time: 100-1000 μs ± 50 μs ± 20%

TABLE I (Continued)

O L D	N E W
3. Subaddress Coding:	3. Subaddress Coding:
Code — Function	Code — Function
0 — MRC word supplied to RM	0-7 — Next word in sector identified by code supplied to RM
1 — Next word in buffer supplied to RM	8 — Word at bottom of FIFO supplied to RM
	15 — Header word supplied to RM
4. Maximum response time allowable	4. Maximum response time allowable
a. SOS to SIS — 1.0 microsecond	a. SOS to SIS — 1.0 microsecond
b. IF to SIS — 1.0 microsecond	b. Message IF to SIS — 1.0 microsecond
	c. Header IF to SIS — 20 microseconds
	d. Module Control Frame to SIS — 20 microseconds
	e. Forced C/I Frame to SIS — 50 microseconds
	5. Two modes of operation
	6. RAM sectors; programmable for eight starting addresses and sector lengths.

TABLE I. (Continued)

O L D	N E W
High Speed Serial Data Output (NATO) 1. RAM buffer size is 1024 bits	High Speed Serial Data Output (NATO) 1. RAM buffer size is 4096 bits 2. Subaddress coding: Code — Function 0-7 — Data words stored in RAM sector identified by code. 8 — C/I word stored in RAM sector zero 9, 10, 11 — C/I word stored in RAM sectors 5, 6 or 7 12 — Data words stored in FIFO 13 — C/I words stored in FIFO 14 — Forced readout header word 15 — C/I header word 3. Programmable for frame length of 8-63 bits and for eight starting addresses and RAM sector lengths.
Parallel Data Output, NTDS Fast/Slow 1. Word length: 16 or 32 bits	Parallel Data Output, NTDS Fast/Slow 1. Word length programmable for any length from 8 to 32 bits

TABLE I. (Continued)

O L D	N E W
	2. Subaddress coding: Code — Function 0 - 7 — Data words stored in RAM sector identified by code. 8 — EF/EI words stored in RAM sector zero 9,10,11 — EF/EI word stored in RAM sectors 5, 6 or 12 — Data words stored in FIFO 13 — EF/EI words stored in FIFO 14 — Forced readout header word 15 — EF/EI header word 3. EDM timer: 100 - 2000 us ± 100 us ± 20%
Switchboard Control 1. Number of messages controllable (maximum): 32	Switchboard Control 1. Number of messages controllable (maximum): 128 2. Subaddress coding: Code — Function 0 — Used for switchboard data acquisition review request commands 1 — Used to transfer switchboard data 2 — Used to transfer remote enable commands

2.3 Test Equipment

2.3.1 Peculiar Support Equipment

Nothing to report.

2.3.2 Factory Test Equipment

Nothing to report.

2.4 Software Development

2.4.1 Simulation Program

Two key simulation engineers (Bob Doyle and Milt Allione) attended a five day course, "Simulation, Model Building and SIMSCRIPT II.5", presented by CACI, the firm which maintains and markets the SIMSCRIPT II.5 computer. Additional effort during this period has been primarily to become familiar with the SIMSCRIPT language. Acquisition of the SIMSCRIPT computer from CACI and implementation within our computational environment is scheduled for early June.

2.4.2 Operational Programs and Firmware

Work continues on generating the MU PPS. The first partial rough draft is nearing completion and will be incorporated in D^3 in June.

A definition of RM firmware anticipated memory requirements, IOM related functional requirements and desired CPU characteristics are in work.

3.0 RELIABILITY

3.1 General

Reliability/safety activities for the period 30 April 1978 through 27 May 1978 are summarized below. Primary efforts during this reporting period were associated with parts control plan preparation, updating the MTBF prediction for the TC to support a tradeoff decision, and preparation of reliability design criteria (guidelines).

3.2 Reliability Management Summary

An overview of SDMS reliability/safety task milestones showing work in progress is presented in Figure 2. Specific tasks conducted during this initial reporting period and activities planned for the next reporting period are indicated below.

3.2.1. Reliability/Safety Management

Preparation of SDMS reliability design criteria (guidelines) is in progress. The design criteria will be issued to responsible design personnel. The criteria contain information related to EDM reliability requirements, parts selection and approval procedures, derating policy, stress and thermal analysis requirements, design review checklist and electrostatic discharge protection measures. The guidelines will be issued to designers by 20 June 1978.

Submittal of the reliability and safety program plans have been rescheduled due to FY78 funding limitations. Final drafts of the Reliability Program Plan (DSN A00N) and System Safety Program Plan (DSN A03Q) will be submitted in mid-September.

3.2.2 Reliability/Safety Analysis

Computer reliability files for the latest RF transceiver (XCVR) design are currently being compiled and edited. Initial reliability prediction activity will consist of generating two computerized MIL-HDBK-2178 predictions for the TC RF XCVR to evaluate the effect on the TC MTBF of operating with and without a cooling fan. Results of these initial predictions will be completed during the first week in June and will be used to support a TC cooling design tradeoff (fan vs. dissipators) decision. Results of this study and tradeoff recommendations are

3.2.2 (Continued)

scheduled to be discussed with the Navy at our next regularly scheduled program review.

3.2.3 Parts Reliability

The SDMS EDM Parts Control Program Plan (DSN A02Q) was completed and submitted during this report period. The plan describes policies and procedures for EDM parts selection, control and approval.

3.2.4 Data Items

DSN A02Q - SDMS EDM Parts Control Program Plan, dated 15 May 1978 was submitted on schedule.

3.3 $\overline{R}$ Schedule Problem Narrative

A revised scheduling of $\overline{R}$ task milestones and CDRLs have been made to reflect rescoping of the FY 1978-9 reliability effort. Revised task milestones are shown in Figure 2.

3.4 Reliability Trend Summary

Nothing to report.

4.0 INTEGRATED LOGISTICS SUPPORT

4.1 General

Completion of sections 1 through 4 of the ILS plan was accomplished during this report period. Effort continues on the remaining sections of the plan. Anticipate the completed plan, revised to include Navy comments, will be completed as scheduled in November.

4.2 Maintainability ($\overline{M}$) Status

Current maintainability activities being performed include the following:

4.2 (Continued)

1. Development of $\overline{M}$ guidelines.
2. Preparation of the preliminary $\overline{M}$ program plan.
3. Incorporation of $\overline{M}$ features into the TC-power supply sub-contractor specifications.
4. Study of PROM identification.
5. Development of an approach to BITE evaluation.

The $\overline{M}$ guidelines and a rough draft program plan are scheduled for the end of June.

4.2.1 $\overline{M}$ Problem Summary

Nothing to report.

4.2.2 GFE $\overline{M}$ Problems

Nothing to report.

4.2.3 $\overline{M}$ Trend Summary

Nothing to report.

4.3 Level of Repair (LOR)

Activity on this task is being deferred until FY79 due to funding constraints.

4.4 Life Cycle Cost (LCC)

Activity on this task is being deferred until FY79 due to funding constraints.

4.5 Training

Activity on this task is being deferred until FY79 due to funding constraints.

4.6 Technical Manuals

Activity on this task is being deferred until FY79 due to funding constraints.

5.0 TECHNICAL STUDIES AND ANALYSES

The following is a listing of studies and analyses accomplished during this reporting period:

RM controller requirements and design concepts.

Development of a common IOM logic design for the IOM/TIB interface (in progress).

TC temperature evaluation with and without fan (reliability tradeoff).

6.0 MEETINGS

The following SDMS-EDM related meetings were held at the Rockwell Anaheim facility.

1. SDMS-EDM Program Review 10 May 1978
2. SDMS-EDM Program Review 24 and 25 May 1978

7.0 PENDING, UNRESOLVED PROBLEMS

7.1 Engineering

No new problems were identified during this reporting period. Effort toward resolving the problems indicated in the last report continues, namely:

A. TC Cooling

B. Excessive Airborne Noise

C. CPU Size Limit of 4K

7.2 Logistics

Nothing to report.

7.3 Operations

Nothing to report.

7.4 Other

Nothing to report.

8.0 DOCUMENTS TRANSMITTED

The following SDMS-EDM related documents were transmitted to the Navy during this report period.

a) Minutes of Program Review Mtg. of 10 May (C78-380.5/301) (A030)

b) Minutes of Program Review Mtg of 24 & 25 May (C78-380.6/301)(A030)

c) Cost Performance Report for May 1978 (C78-461.2/301) (A031)

d) EDM Management Proposal (Vol. I) - Final (T77-894/301)

e) EDM Technical Proposal (Vol II) - Final T77-894/301)

f) EDM Cost Proposal (Vol III) - Final (T77-894/301)

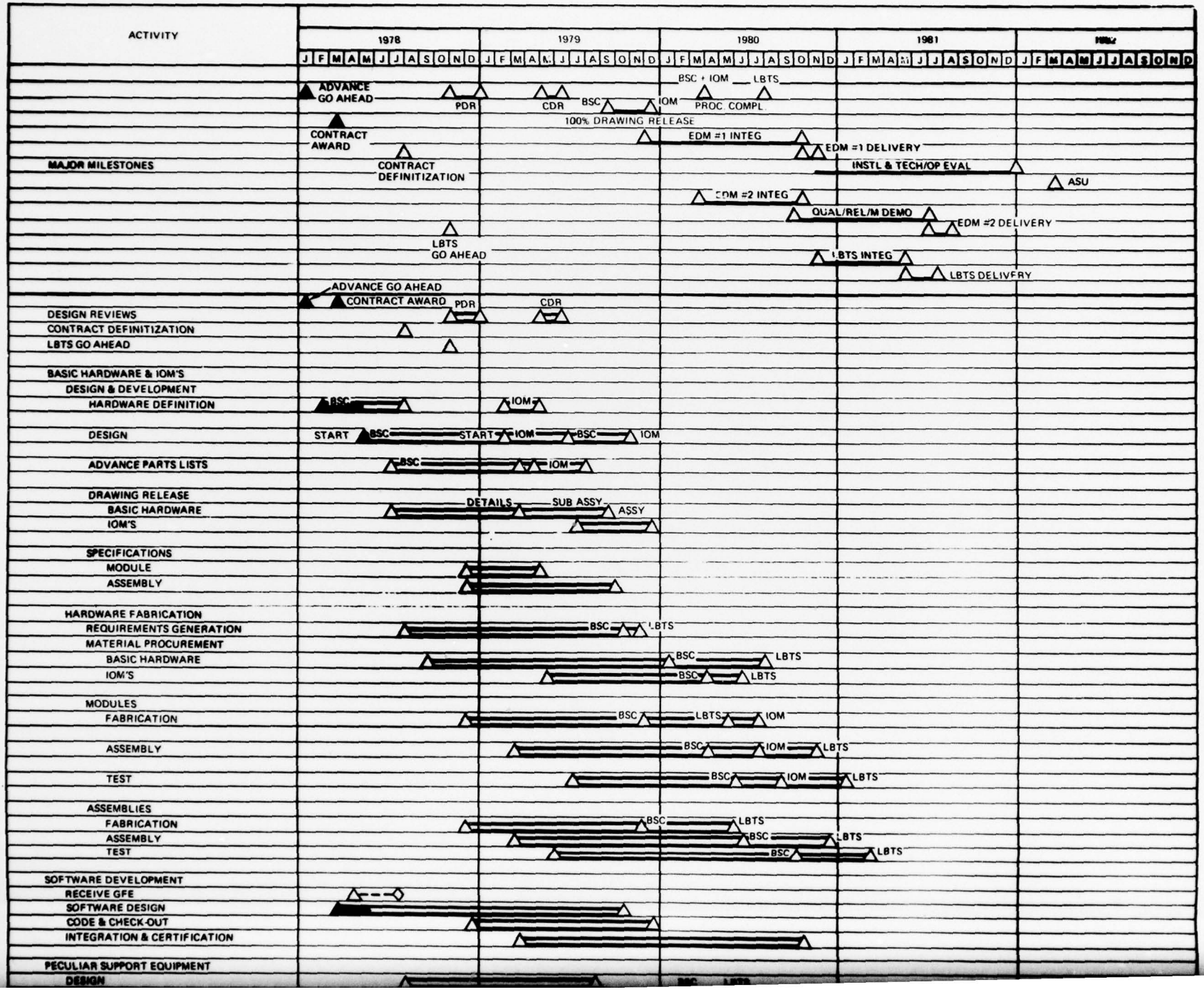
1) Interim Technical Report for April (C78-500.1/301) (A02V)

h) Part Control Program Plan (C78-577/301) (A02Q)

9.0 DOCUMENTS RECEIVED

None.

Data as of 5/31/78



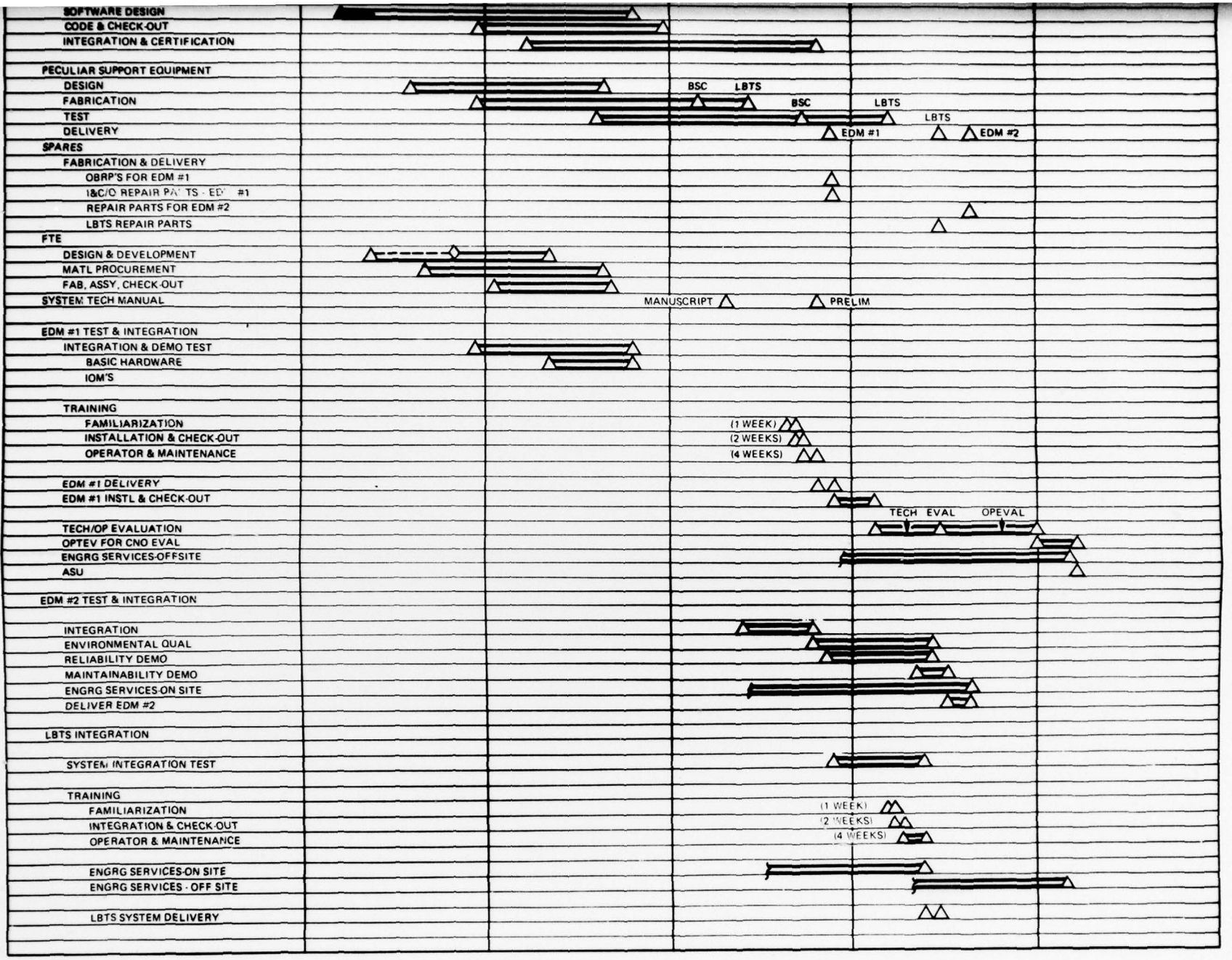


FIGURE 1. SDMS-EDM PROGRAM OVERVIEW

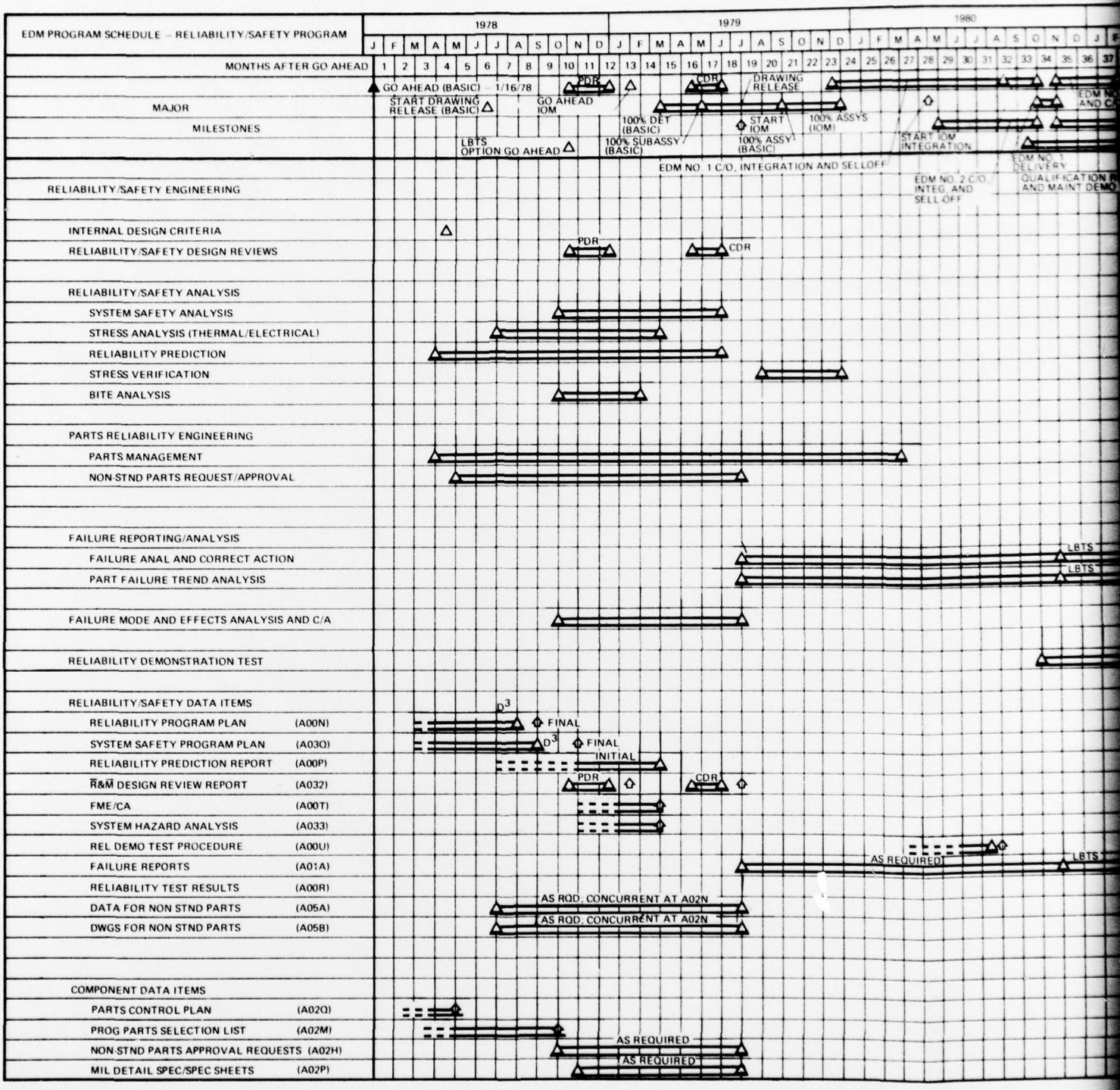
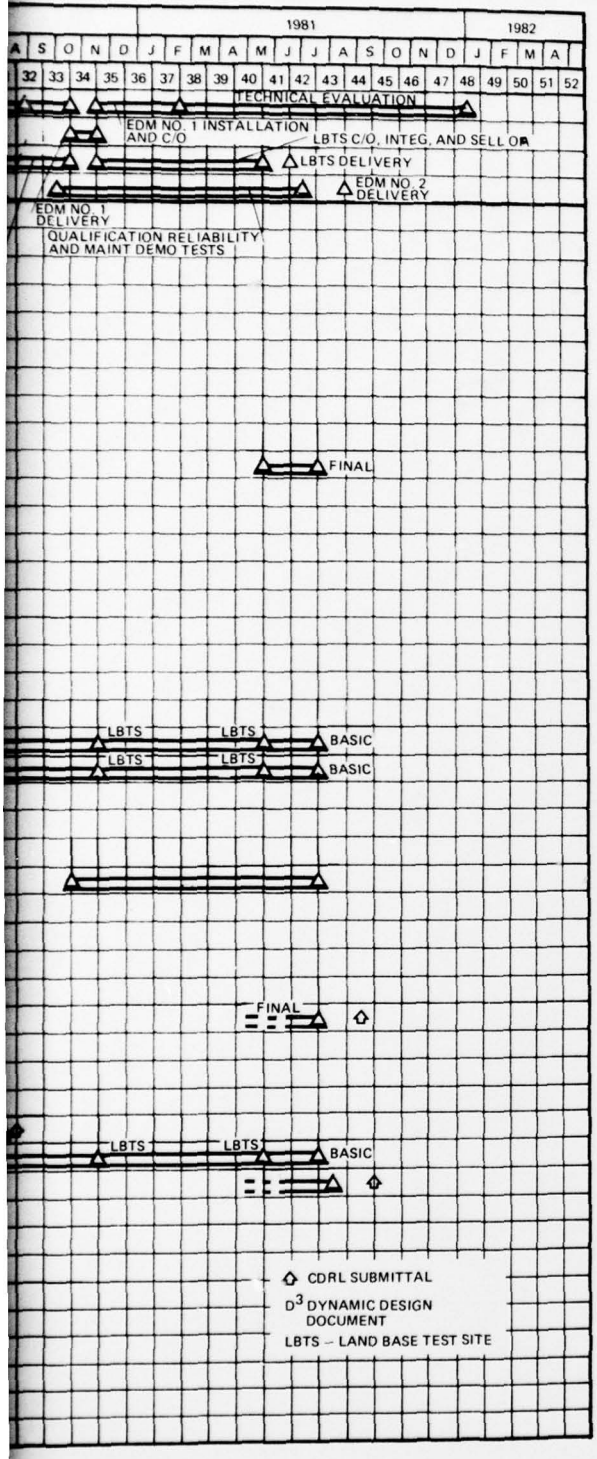


Figure 2. Reliability/Safety Program Schedule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LBTS DELIVERY
EDM NO. 2 DELIVERY
EDM NO. 1 DELIVERY
QUALIFICATION RELIABILITY AND MAINT DEMO TESTS
FINAL
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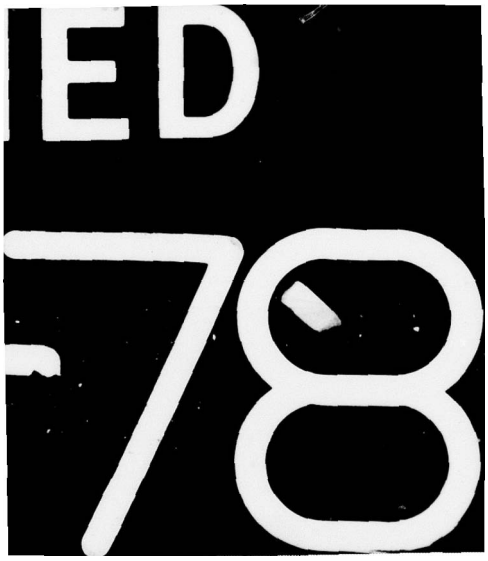
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