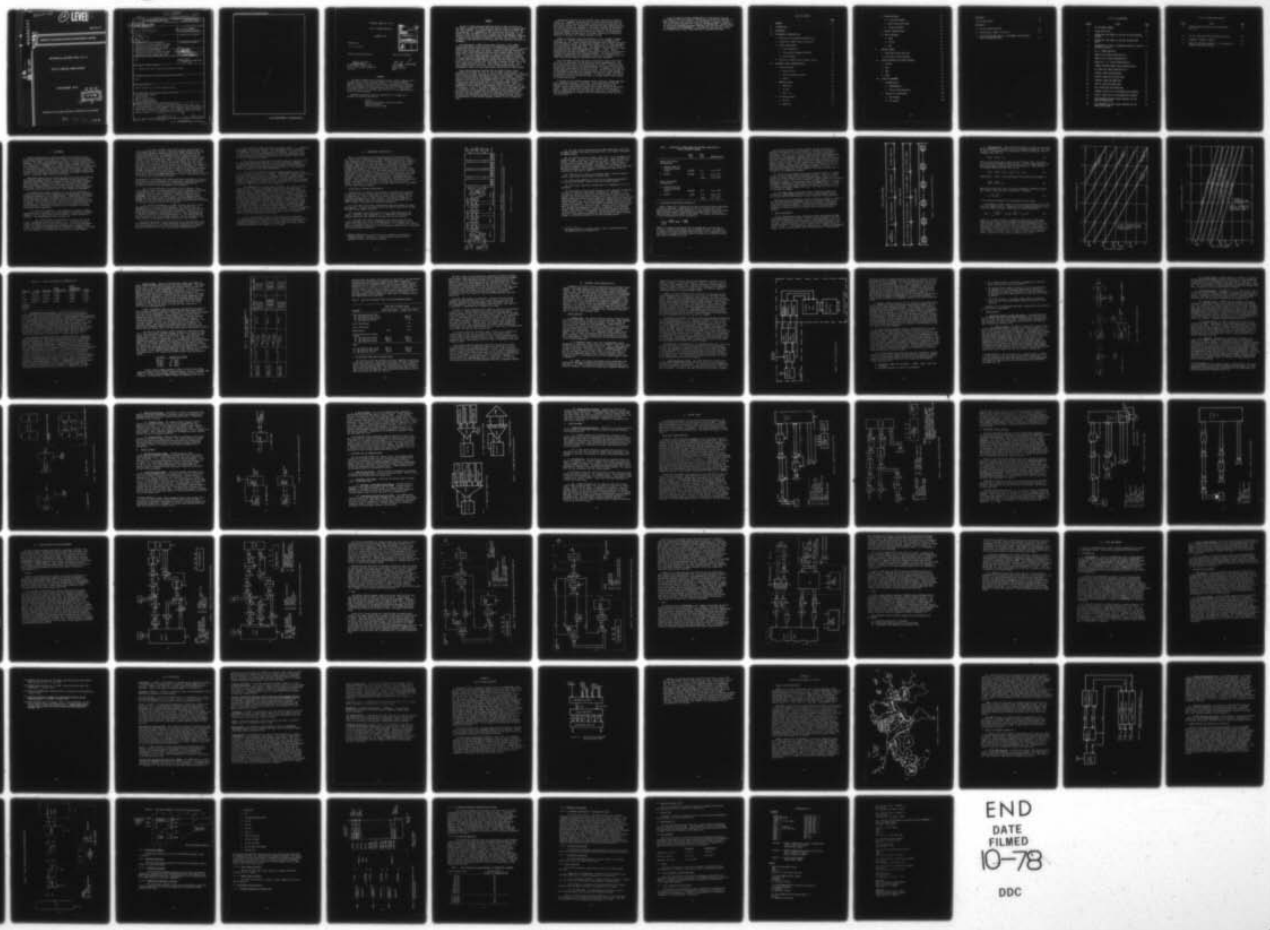
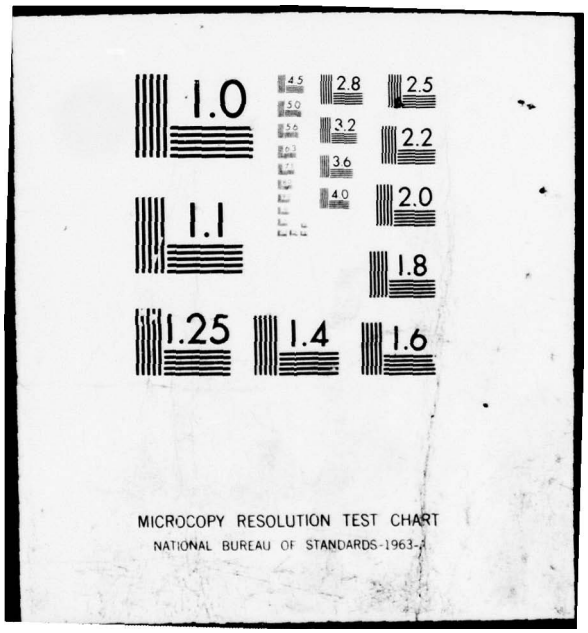
AD-A058 261 DEFENSE COMMUNICATIONS ENGINEERING CENTER RESTON VA F/G 17/2
DCS II TIMING SUBSYSTEM.(U)
DEC 77 D R SMITH

UNCLASSIFIED DCEC-TR-23-77 SBIE-AD-E100 089 NL

| OF |
AD
A058261



END
DATE
FILMED
10-78
DDC


1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
4.5
5.0
5.6
6.3
7.1
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

TR 23-77

DEFENSE COMMUNICATIONS ENGINEERING CENTER

TECHNICAL REPORT NO. 23-77

DCS II TIMING SUBSYSTEM

DECEMBER 1977

APPROVED FOR PUBLIC RELEASE; DISTRIBUTION UNLIMITED

(18) SBIE

(19) AD-E100 089

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

(14) 1. REPORT NUMBER: DCEC-TR-23-77	2. GOVT ACCESSION NO. / 3. RECIPIENT'S CATALOG NUMBER
(6) 4. TITLE (and Subtitle): DCS II Timing Subsystem,	(9) 5. TYPE OF REPORT & PERIOD COVERED: Technical Report, / 6. PERFORMING ORG. REPORT NUMBER
(10) 7. AUTHOR(s): D. R. Smith Arid	8. CONTRACT OR GRANT NUMBER(s)
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Defense Communications Engineering Center, Transmission Engineering Division, R220, 1860 Wiehle Avenue, Reston, VA 22090	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: N/A
11. CONTROLLING OFFICE NAME AND ADDRESS: Defense Communications Engineering Center, Transmission Engineering Division, R220, 1860 Wiehle Avenue, Reston, VA 22090	(11) 12. REPORT DATE: December 1977 / 13. NUMBER OF PAGES: 91 (12) 92p.
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): N/A	15. SECURITY CLASS. (of this report): Unclassified / 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE: N/A

16. DISTRIBUTION STATEMENT (of this Report)

A. Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

N/A

18. SUPPLEMENTARY NOTES

Review relevance 5 years from submission date.

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

DCS Synchronous Network
Timing Systems
Digital Transmission
DCS II Timing Subsystem
Future Timing Subsystem

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

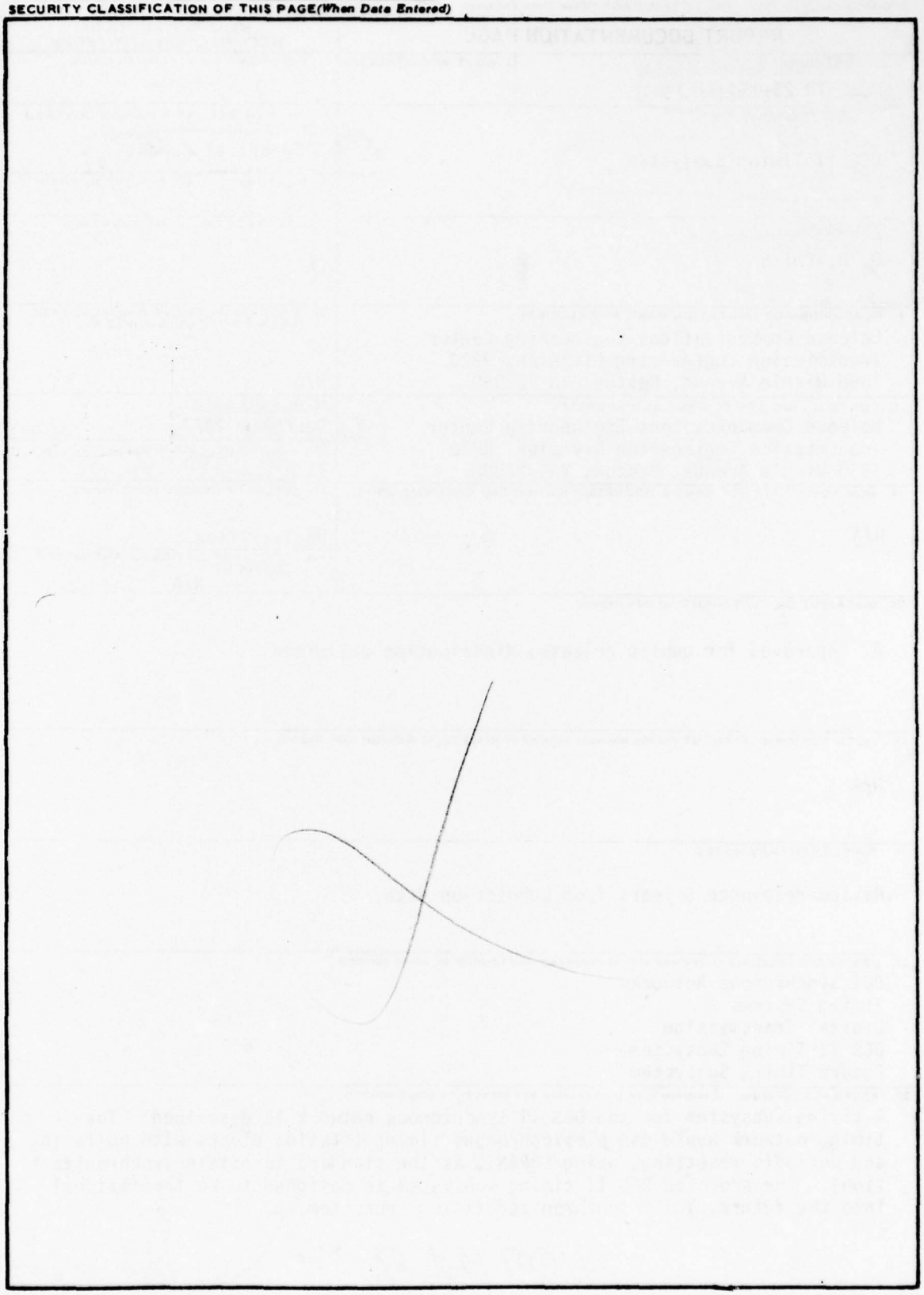
A timing subsystem for the DCS II synchronous network is described. The timing network would use plesiochronous timing (station clocks with buffering and periodic resetting, using LORAN C as the standard to obtain synchronization). The proposed DCS II timing subsystem is designed to be transitional into the future, fully synchronized timing subsystem.

407519

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

Unclassified

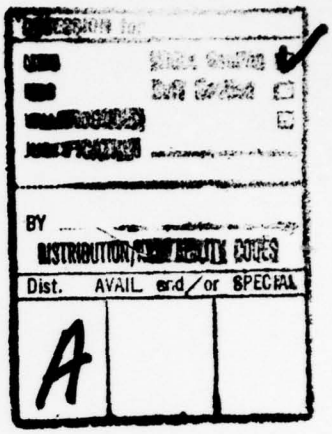
SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)



TECHNICAL REPORT NO. 23-77

DCS II TIMING SUBSYSTEM

DECEMBER 1977



Prepared by:

- D. R. Smith

Technical Content Approved:

A. J. TALLET, Captain, USN
Chief, Transmission Engineering
Division

Approved for Release:

R. H. LEVINE
Deputy Director
DCEC

FOREWORD

The Defense Communications Engineering Center Technical Reports (TR's) are published to inform interested members of the defense community regarding technical activities of the Center, completed and in progress. They are intended to stimulate thinking, encourage information exchange, and provide guidance for related planning and research. They are not an integral part of the DoD PPBS cycle and should not be interpreted as a source of program guidance.

Comments or technical inquiries concerning this document are welcome, and should be directed to:

Director
Defense Communications Engineering Center
1860 Wiehle Avenue
Reston, Virginia 22090

SUMMARY

The DCS II timing subsystem described herein is based on the use of the LORAN C navigational system which can provide timing and synchronization over long distances. An existing LORAN C receiver system, the AN/GSQ-183, (or equivalent), is recommended as the timing source for the DCS II. The AN/GSQ-183 uses the LORAN C signal to phase-lock two independent, highly accurate crystal oscillators and to generate three 1 MHz frequency standards. A separate clock distribution system will interface with the three 1 MHz standards to then generate and distribute each rate required by transmission equipments.

The advantage of a LORAN C based timing subsystem is that LORAN C stations have atomic sources which are all synchronized to Universal Coordinated Time (UTC) such that there is no further requirement to externally control these clocks within the system. However, buffers are required to absorb small timing differences which may arise between LORAN C chains, and losses of bit count integrity (BCI) will result due to occasional buffer spill. Yet for any timing subsystem, synchronous or otherwise, buffering is always required to compensate for transmission path delay variation and to provide phase adjustment between outgoing clock and incoming data. Also, losses in BCI due to timing slips can be made infrequent (at most once a day for a global end-to-end circuit). Other sources of loss of BCI, such as pulse stuffing control word error, loss of frame synchronization, and cryptographic rekey, will add a much greater contribution to total outages.

Under normal operating conditions for the LORAN C system, timing accuracies on the order of 1 part in 10^{12} or better can be expected. For such accuracies, buffer underflow or overflow can be expected only infrequently and will have negligible contribution to total circuit outages. However, there are certain failure and degraded conditions which will worsen timing accuracies and shorten the time between buffer slips. With failed atomic clocks or with scheduled maintenance at a particular LORAN C station, a LORAN-based timing subsystem, such as the AN/GSQ-183, will revert to an independent clock system by using redundant crystal oscillators (1 part in 10^9 accuracy). Also, if the LORAN C receiver fails or if the LORAN C signal is corrupted by noise or jamming, the LORAN-based timing subsystem again would use only its internal crystal oscillators with no external source. The mean time between buffer slip for the attendent crystal oscillator accuracies are considered acceptable for short periods of time, but would be unacceptable if such periods exceeded a nominal 1% of all operating time.

Performance objectives for the proposed timing subsystem are stated in chapter III. Equipment characteristics discussed include timing subsystem reliability, buffer location and length, clock accuracy and stability, and mean time to timing slip. Reliability objectives are made commensurate with like digital transmission equipments. Two buffer locations are considered, the first directly at the radio mission bit stream, and the second at the lowest synchronous interface in the multiplex hierarchy. Clock parameters and buffer lengths are specified so as to meet a mean time to timing slip objective of 24 hours for a global reference circuit.

Chapter IV describes timing characteristics of (1) the DCS II timing subsystem, (2) digital transmission equipments including DRAMA and FKV configurations, (3) digital transmission equipments which operate over analog plant including VF, group, and troposcatter modems, and (4) other equipment including the ULS, TTC-39, and KG-81. Two candidates are discussed for use as a timing source, independent clocks and LORAN C. The pros and cons of each candidate are given and a recommendation of LORAN C is made. Timing characteristics are then described as they currently exist or are planned for transmission, encryption, and switching equipment. The data/timing line interface, internal oscillator parameters, provision for external clock, and buffer location and length are characterized for each equipment.

The fifth chapter defines two types of transmission node, called major and minor, for the purpose of describing two timing implementations. The major node typically has a heavy concentration of traffic, several incoming and outgoing links, perhaps switching equipment, and perhaps interface with another major system such as the DSCS or TRI-TAC. A separate, self-contained timing subsystem is proposed for the major node. The minor node has none of the attributes of the major node and typically might be a simple repeater or a terminating site off the major backbone. For the minor node, loop timing may be used to provide the required clock, or in some special cases internal oscillators may be used.

In chapter VI the interface between the DCS synchronous network and other major synchronous networks is discussed. Timing interface with TRI-TAC requires the DCS timing subsystem to provide clocked frequencies for external timing of the digital multiplex family (DGM) and the TTC-39 digital switch. Timing interface with the DSCS will require a satellite delay buffer to compensate for satellite path delay variations. Interface with AT&T and NATO systems will require only that already provided by the DCS II timing subsystem.

Plans for R&D and ultimate implementation of a DCS timing subsystem are treated in the final chapter. For the near term (DCS II) subsystem, no R&D is required, since state-of-the-art technology is proposed. However, the future timing subsystem still requires considerable R&D. Implementation of the interim subsystem has been scheduled in the 1980 Five Year Plan (FYP) in conjunction with AUTOSEVOCOM II. The 1980 FYP also contains a project for implementing a future timing subsystem in the 1985 time frame.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (CONT'D)

LIST OF TABLES

I. INTRODUCTION

This technical report describes the timing subsystem for implementation in support of near-term synchronous subnetworks in the Defense Communications System. Consideration is given to the requirements of near-term synchronous subnets, performance characteristics of timing subsystem components, integration of a timing subsystem into the digital transmission system, and interface of the DCS synchronous network with other synchronous networks. An acceptable choice for a DCS II timing subsystem is shown to be a plesiochronous system using LORAN C as a primary frequency standard and buffers to absorb timing differences between nodal clocks.

This report makes no attempt to exhaustively compare all potential candidates for a DCS II timing subsystem. A fundamental requirement for this timing subsystem is off-the-shelf availability and proven performance which thereby eliminates a number of candidate techniques. Of the systems which can or will provide worldwide dissemination of precise time and frequency, including HF (WWV), LF (LORAN C), VLF (OMEGA) and Global Position Satellites (GPS), only LORAN C meets all the requirements of a DCS II timing subsystem. Likewise, of the timing and synchronization concepts which do not depend on outside sources, the independent atomic clock approach most closely meets DCS needs. Therefore, only LORAN C and independent atomic clocks are considered here. However, even in comparing these two techniques, no detailed cost comparison has been attempted here, as such an effort is beyond the scope of this report.

II. BACKGROUND

Initial implementations of digital transmission in the DCS, such as the Frankfurt-Koenigstuhl-Vaihingen (FKV) Project and the Digital European Backbone (DEB) Stage I, are using pulse stuffing as the basic synchronization technique. The existing AUTOSEVOCOM network, which is largely based on 50 kb/s KY-3 operation, is accommodated via a pulse stuffing interface with first level multiplexers. Likewise, the 1.544 Mb/s output of first level multiplexers is interfaced via pulse stuffing with second level multiplexers. Provision for this pulse stuffing interface made it possible to use medium grade clocks internal to the individual transmission equipments and thereby eliminated the need for a separate, highly accurate timing source.

Synchronous subnets now exist within the DCS which already are configured with separate timing subsystems. Both AUTODIN and Channel Packing are configured with LORAN C timing subsystems to provide synchronous interface within the subnet. However, these subnets are presently interfaced with digital transmission equipment via a VF modem operating into a 64 kb/s PCM channel. Because of this analog interface, adequate timing performance is provided by using the internal clocks of the transmission equipments.

In considering the timing characteristics for the next generation of digital transmission, one must account for the characteristics of near-term synchronous subnetworks, such as AUTOSEVOCOM II. Additionally, the schedule for implementation of these synchronous subnets and the availability of timing subsystem components to support these near-term requirements must be recognized. Finally, the choice of a near-term timing subsystem must allow for expansion of synchronous services and for the evolution to a future timing subsystem. Three basic alternatives are considered for providing the required timing capability:

(1) The first alternative is the continued use of pulse stuffing. This alternative is available in the next generation transmission equipment (DRAMA) and will be used initially until the DCS II timing subsystem is available. The disadvantages of this approach are:

(a) Losses of BCI associated with stuff code errors can be a major contribution to short term outages [1,2]. Operation of a pulse stuffing multiplexer over a bursty error channel, such as with tropospheric scatter, can result in unsatisfactory performance due to frequent losses of BCI. This particular problem could be alleviated by attempting to increase the system margin on all troposcatter links but only at great expense.

(b) Pulse stuffing jitter, which results from the inability of the smoothing loop to provide a perfectly averaged destuffed clock, can cause timing problems in equipments which must extract timing from the jittered destuffed clock. A narrowband filter, as found with most bit synchronizors, may not be able to track the high frequency (slewing) jitter inherent in most destuffed clock signals. For example, when using a pulse stuffing second level multiplexer, the bit synchronizer in a first level multiplexer must be able to extract and maintain timing from the jittered destuffed clock associated with the second level multiplexer. Bit synchronization problems have been experienced for this type of interface [3]. Such problems led to an R&D contract [4] which studied pulse stuffing multiplexers and made recommendations for specifying a standard interface between pulse stuffing multiplexers and bit synchronizers. Results of this R&D contract were used as input to the DRAMA specifications and will provide future guidance in the planning of pulse stuffing networks.

This approach is satisfactory for limited synchronous requirements but becomes costly and sacrifices performance for a large-scale synchronous subnetwork. In view of the objective to evolve to an all-digital integrated DCS, synchronous digital transmission appears to be mandatory.

(2) A second alternative, the subject of this technical report, is to provide a separate timing subsystem to support synchronous requirements in the near-term DCS. Such an approach would utilize state-of-the-art technology to provide initial capability. Potential candidates are an independent clock system, as presently used in TRI-TAC, and the LORAN C navigational and timing system, as presently used with AUTODIN and Channel Packing. At some later date, the near-term timing subsystem would be upgraded or replaced to become the future timing subsystem.

(3) The third alternative is to apply directly the desired final configuration of the future timing subsystem. This approach calls for implementation of a processor-based timing subsystem, such as master/slave, mutual synchronization, or time reference distribution. However, such a system would be premature and potentially costly in that considerable R&D is required to define the required characteristics. The required R&D has been initiated with Air Force and DCA contracts, and will culminate in the field testing of a developmental model scheduled for the mid 1980's.

The overall conclusion is that state-of-the-art timing subsystem is the only alternative which will provide synchronous capability with reasonable cost and performance and still meet a near-term implementation schedule. Required characteristics of this interim timing subsystem include:

(1) Ability to support near-term synchronous subnets, i.e., AUTODIN II, AUTOSEVOCOM II and Channel Packing. This requirement is met by providing two families of bit rates: 8000N b/s, up to 12,928 Mb/s, and 75 x 2^N b/s, up to 9.6 kb/s. These clocked frequencies will provide synchronous timing to end instruments, such as the digital secure voice terminal (DSVT), and to digital transmission equipments.

(2) Provision for expansion from initial operational capability (IOC) to final operational capability (FOC) of a given synchronous subnetwork. The timing subsystem will include a clock distribution system with built-in modularity to allow a thinly populated system to grow to a fully populated system, as required for the final configuration.

(3) Ease of integration of timing subsystem components into transmission equipments and other major networks. Requirements imposed on transmission equipments should be met with existing design and require no modification. Provisions for internal buffering and external clocking capability, which already exist, should not need modification. Interface with other synchronous systems, including TRI-TAC, NATO, DSCS, and AT&T, should also require minimal additional capability for the DCS timing subsystem.

(4) Adaptability to future timing subsystem. The choice of interim capability must reflect the requirement to provide an enhanced timing capability later. Certainly, a desired result would be to have the interim capability become a backup mode to the future timing subsystem. Either the independent clock system or LORAN C could serve as an interim capability as well as a backup to this future timing subsystem. In fact, the AN/GSQ-183 LORAN receiver system used with AUTODIN and Channel Packing has provision for two frequency standards, primary and secondary. LORAN C would be used as the primary standard in a DCS II timing subsystem, and could well become the secondary standard in a future timing subsystem; alternatively, LORAN C could remain the primary standard and another source, such as independent atomic clocks, could be used as the secondary standard. The other consideration is that of buffer compatibility between DCS II and future timing subsystems. Again, no problems exist in using the same buffers, both with respect to their location and operating characteristics.

(5) A desired characteristic of the interim timing subsystem is its commonality with existing subsystems used in AUTODIN and Channel Packing. If the same timing source (LORAN C) were selected for the interim timing subsystem, advantage could be taken of previous experience gained, previous technology development, and common logistics support.

III. PERFORMANCE CHARACTERISTICS

Here, the performance of the timing subsystem will be characterized by stating a set of objectives for timing subsystem availability, station clock performance, and buffer performance. To derive availability objectives, a DCS reference channel is first defined to include provision for a timing subsystem. Objectives for Mean Time Between Outage*(MTBO) and Mean Time to Repair (MTTR) are made consistent with previous choices for other transmission equipment. Two alternative buffer locations in the multiplex hierarchy are analyzed here: (1) The higher level buffer location provides synchronization of the entire mission bit stream (MBS), while (2) the lower level buffer location provides synchronization at only low-speed synchronous interfaces. Buffer lengths are specified to meet performance objectives for Mean Time to Timing Slip (MTTS) allocated over a DCS global reference channel. Clock parameters (accuracy and stability), time varying propagation delays, and choice of MTTS are seen to influence the choice of buffer length. Allocations are also shown for the mean time to recover timing (MTRT) over the same reference channel.

1. ALLOCATION OF EQUIPMENT UNAVAILABILITY

Unavailability calculations have been made of the DCS timing subsystem using the DCS reference channel shown in Figure 1 and previously defined in reference [2]. Table I summarizes the unavailability analysis for two different configurations of buffer location. Allocations of Mean Time Between Outage (MTBO), Mean Time to Repair (MTTR), and Unavailability (U) shown in Table I are based on the following assumptions:

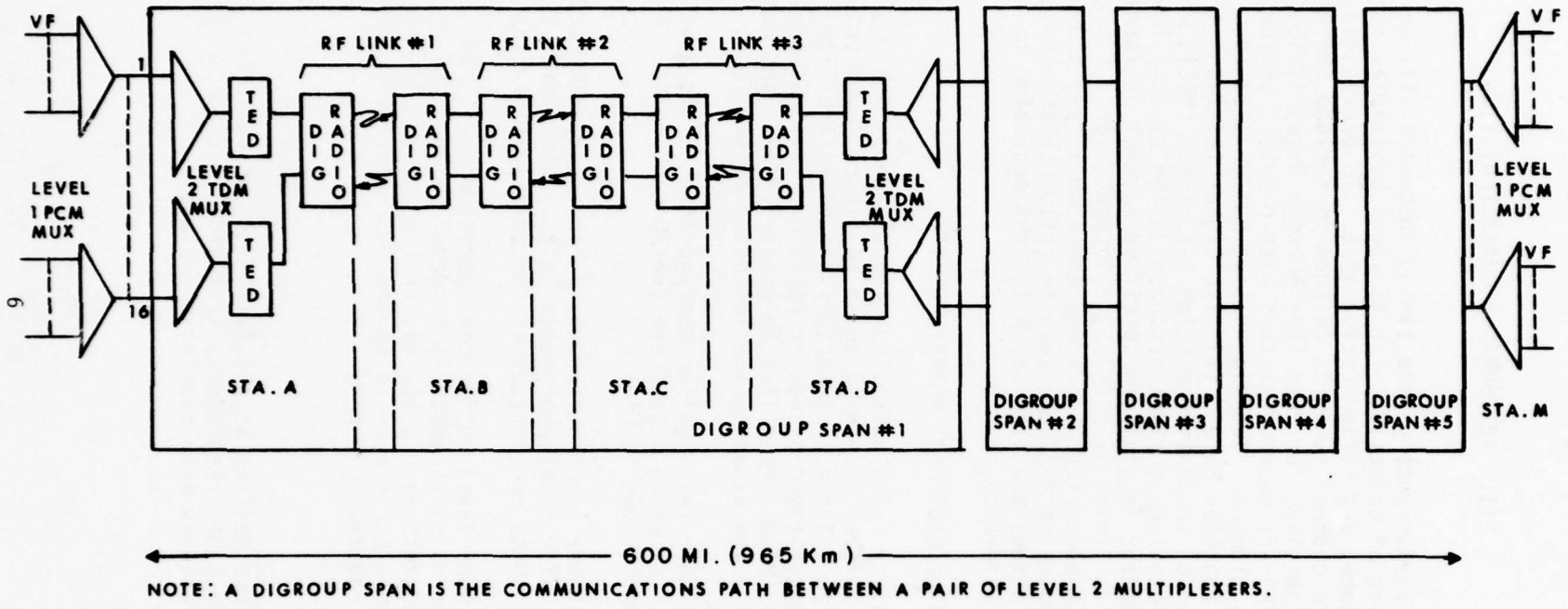
(1) The higher level buffer configuration would have buffers for every MBS breakout, in which case there are 20 such buffers required for the DCS reference channel shown in Figure 1.

(2) The higher level buffer would require an MTBO commensurate with choices of MTBO for other equipments (e.g., DRAMA Level 2 multiplex and digital radio) which are located at the same level in the hierarchy.

(3) The lower level buffer configuration would have buffers for the lowest synchronous rate, which is tandemed between the uncombined sides of Level 1 multiplexers (e.g., 16, 56, or 128 kb/s). It is assumed that initially 10% of all channels represented by the DCS reference channel would be synchronous and therefore require buffering.

---

* Outage is here defined as the failure of an equipment to perform its intended function. Redundancy is typically used to prevent single equipment failures from causing an outage.



NOTE: A DIGROUP SPAN IS THE COMMUNICATIONS PATH BETWEEN A PAIR OF LEVEL 2 MULTIPLEXERS.

Figure 1. DCS Reference Channel

(4) The lower level buffer would have an MTBO commensurate with other equipments located at the same hierarchical level (e.g., Level 1 multiplexer or submultiplexer).

(5) The station clock will supply a clock signal to all equipments of a synchronous node. Station clock failure would cause outages on some or all channels traversing that node. Therefore, a highly reliable station clock is desired with attendent high MTBO. The MTBO figures shown in Table I for station clock plus distribution system are considered feasible with appropriate (probably triple) level of redundancy. Similar timing subsystems have been described in the literature as having MTBO's close to [5] or exceeding [6] that shown in Table I.

(6) There exist five pairs of synchronous nodes in the DCS reference channel, each of which would require a station clock.

(7) Only timing components intrinsic to the transmission equipments are required for repeater stations of the DCS reference channel.

(8) MTTR figures have been allocated which are commensurate with link equipments.

The unavailability calculations* indicate a timing subsystem availability in excess of 0.9999 for either buffer configuration. Reference [2] had allocated an availability objective of 0.999 for the DCS reference channel. However, that allocation did not include provision for station timing, but rather assumed that required timing signals were generated by the transmission equipments themselves. It can be assumed that a station clock will provide higher reliability than would timing components located directly within the transmission equipments. Hence, the overall availability of a timing source would be improved by use of station clock. However, use of timing buffers will introduce some degradation in overall availability of the reference channel, which would effectively negate any availability gain anticipated by use of station clock. To summarize, conservative objectives have been given for timing subsystem availability, and the impact of timing subsystem outages is considered acceptable for the DCS reference channel.

---

* The unavailability calculations shown in Table I were derived using the method outlined in reference [2].

TABLE I. ALLOCATION OF TIMING SUBSYSTEM EQUIPMENT UNAVAILABILITY FOR DCS REFERENCE CHANNEL

	MTBO (hrs)	MTTR (hrs)	UNAVAILABILITY
1. Higher Level Buffer Configuration			
a. Station Clock and Clock Distribution System	200,000	0.5	1.25×10^{-5}
b. Buffers	200,000	0.5	2.5×10^{-5}
		TOTAL	3.75×10^{-5}
2. Lower Level Buffer Configuration			
a. Station Clock and Clock Distribution System	200,000	0.5	1.25×10^{-5}
b. Buffers	4,000	0.33	1.65×10^{-5}
		TOTAL	2.9×10^{-5}

2. ALLOCATION OF MEAN TIME TO TIMING SLIP

Here a timing slip is defined as the loss of BCI which results from buffer overflow or underflow. (Other causes of BCI loss, such as loss of bit synchronization or frame synchronization, are not included in this definition). This particular outage is characterized by the Mean Time to Timing Slip (MTTS) and Mean Time to Recover Timing (MTRT). If desired, the contribution to total unavailability can be calculated as

$$U_{\substack{\text{TIMING} \\ \text{SLIPS}}} = \frac{\text{MTRT}}{\text{MTTS} + \text{MTRT}} \cong \frac{\text{MTRT}}{\text{MTTS}}$$

However, it should be pointed out that the outage due to timing slips is distinctly different from outages due to equipment failure. The former is a transient effect which typically would not cause a call termination, while the latter is a longer term effect (several minutes up to a few hours) which would cause termination of a call.

The procedure utilized to allocate the MTTS has been to assign an objective of 24 hours MTTS for the DCS global reference circuit defined in references [2] and [7]. The choice of 24 hours is based on previously stated DCA design objectives [7] and on operational practice of updating the key variable in cryptographic equipments every 24 hours. Additionally, the buffer lengths required to meet this MTTS turn out to be quite reasonable. Figure 2 shows an allocation of this 24-hour MTTS among the sections of the global reference circuit. Further suballocation is shown for the four DCS reference channels comprising the overseas terrestrial section and the major nodes comprising each individual DCS reference channel. The choice of particular MTTS allocations for each segment of the global reference circuit is based on the following assumptions:

(1) Both satellite segments and each DCS reference channel are assumed to have a buffer located at each synchronous interface. Since the overseas terrestrial segment comprises four DCS reference channels, there are four buffers per circuit in the overseas terrestrial segment compared to one buffer in the satellite segment. If we further assume that each buffer is clocked by independent timing sources (worst case, since the LORAN C system coordinates its clocks to UTC under normal operating conditions), then timing slips in the overseas terrestrial segment should occur four times as often as slips in the satellite segment.

(2) The CONUS common carrier and overseas terrestrial segments are assumed to be approximately equivalent in total length (channel mileage) and to have similar characteristics in their respective timing subsystems.

Based on the above assumptions, an MTTS allocation of 60 hours is given to both the CONUS and overseas segments, while an allocation of 240 hours is given to each satellite segment. As indicated in Figure 2, the overseas terrestrial allocation results in a 240 hour MTTS for each DCS reference channel and a 1200 hour MTTS per each major node of the DCS reference channel.

3. BUFFER REQUIREMENTS

A given length buffer can be selected to provide synchronism over some time period specified by the MTTS. The MTTS gives an estimate of the time before buffer underflow or overflow occurs, a condition which results in a bit slip. The objective here is to derive buffer lengths necessary to meet the MTTS allocations previously given. Factors which influence choice of buffer include (1) clock accuracy and stability, (2) time-varying propagation delays, and (3) choice of MTTR. Each of these effects is discussed below.

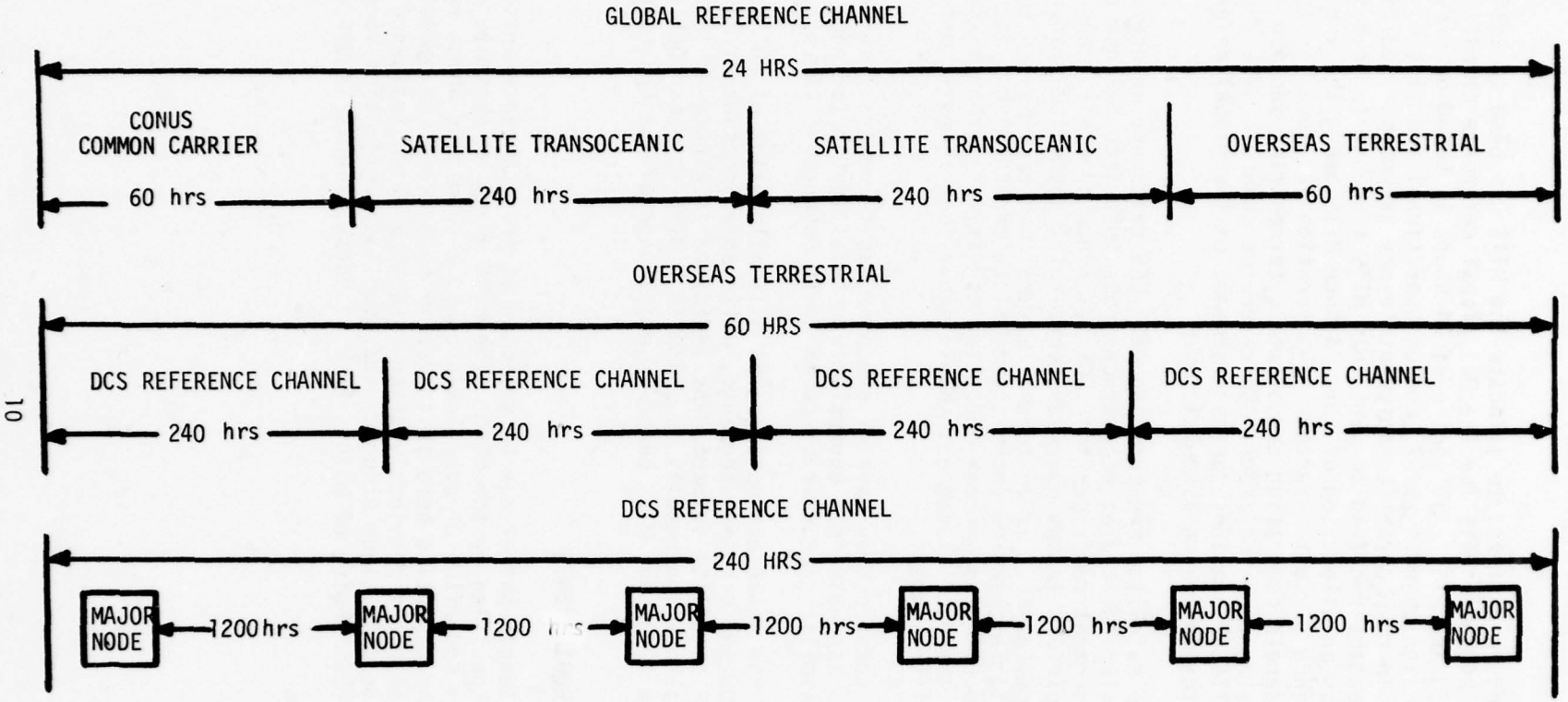


Figure 2. Allocation of Mean Time to Timing Slip

a. Clock parameters. Phase difference between two clocks can accumulate due to differences in frequency accuracy and stability between the two clocks. If $f_i(o)$ is the frequency of a clock at the i^{th} node at time zero, then the frequency after time t is

$$f_i(t) = f_i(o) + \alpha_i t \tag{1}$$

where α_i is the drift rate in Hz/sec of the i^{th} nodal clock. The factor α_i is actually a function of time, but here α_i will be assumed constant and equal to the worst resulting offset due to instability. The difference in frequency between any two clocks is then

$$f_i(t) - f_j(t) = f_i(o) - f_j(o) + (\alpha_i - \alpha_j)t. \tag{2}$$

Letting $f_i(t) - f_j(t) = \Delta f$ and dividing by the nominal clock frequency f,

$$\frac{\Delta f(t)}{f} = \frac{\Delta f(o)}{f} + at \tag{3}$$

where $\Delta f(o)/f$ and $\Delta f(t)/f$ are the relative difference frequencies between two clocks at times zero and t, respectively, and where

$$a = \frac{(\alpha_i - \alpha_j)}{f} \tag{4}$$

is the relative difference drift rate between the two clocks.

The parameter of most interest is the accumulated phase error over some arbitrary length of time T. Integration of the frequency difference, given in Eq. (3), over some time T yields the total phase accumulation:

$$\phi(T) = \int_o^T \left[\frac{\Delta f(o)}{f} + at\right] dt = \frac{\Delta f(o)}{f} T + \frac{1}{2} aT^2. \tag{5}$$

Figure 3 is a series of plots of accumulated phase error in time versus total time for various initial frequency accuracies between two clocks. Figure 4 shows a similar series of plots of accumulated phase error versus total time for selected long term (per day) drift rates. Total phase accumulation, given by Eq. (5), is then determined by summing contributions from frequency inaccuracy (Figure 3) and from frequency drift (Figure 4). Figure 5 gives accumulated errors in numbers of bits versus accumulated error in absolute time for a number of applicable bit rates.

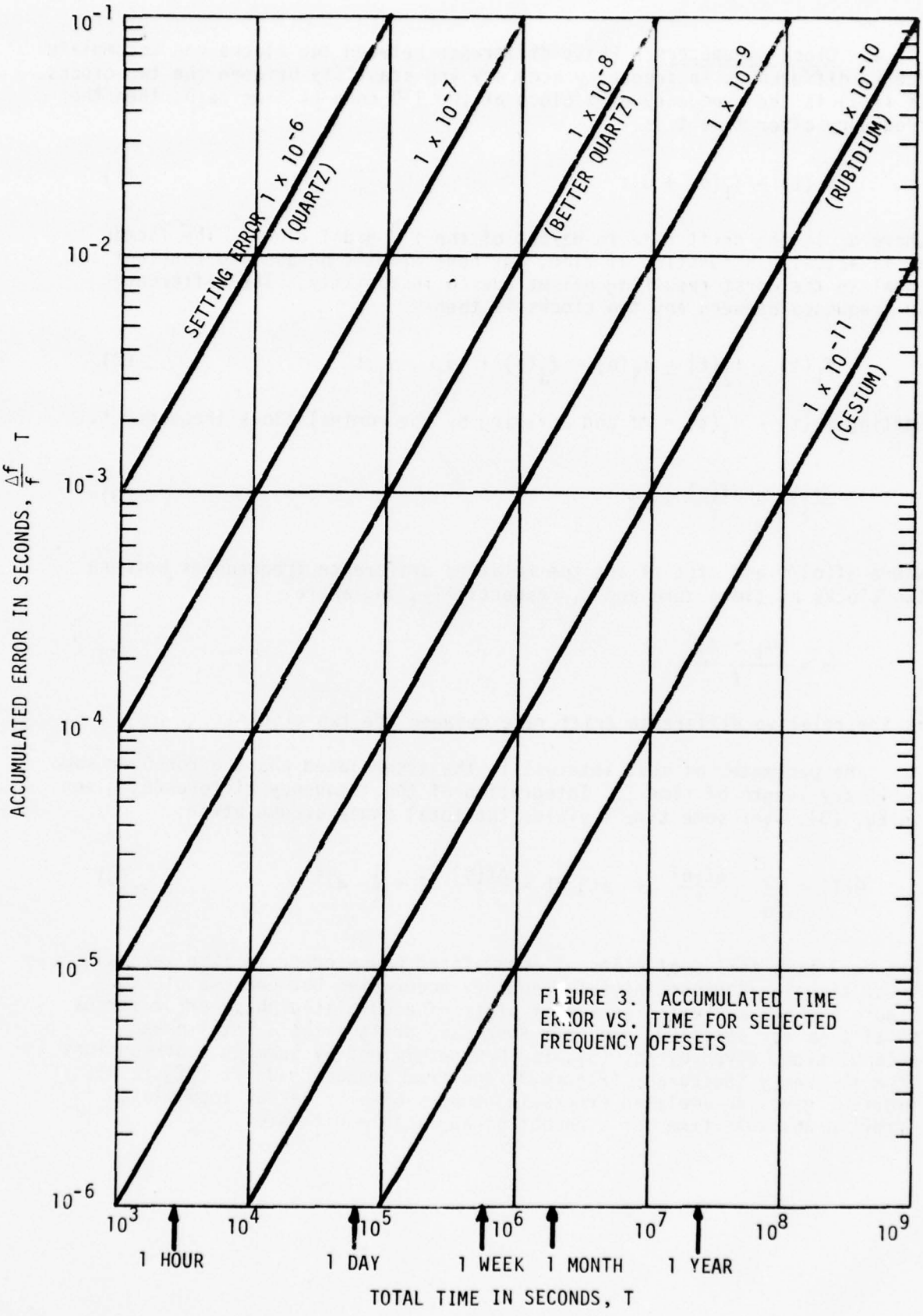


FIGURE 3. ACCUMULATED TIME ERROR VS. TIME FOR SELECTED FREQUENCY OFFSETS

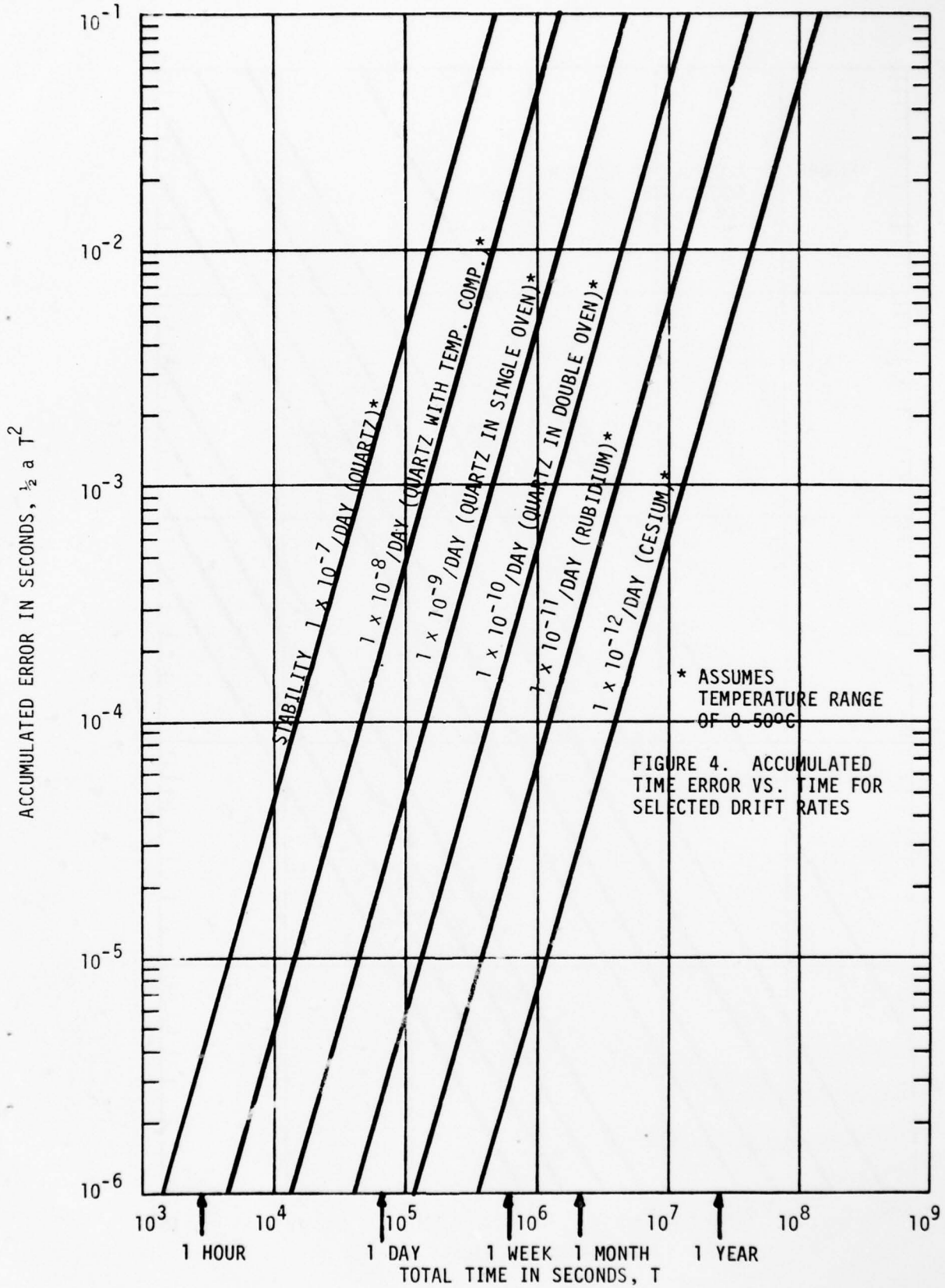


FIGURE 4. ACCUMULATED TIME ERROR VS. TIME FOR SELECTED DRIFT RATES

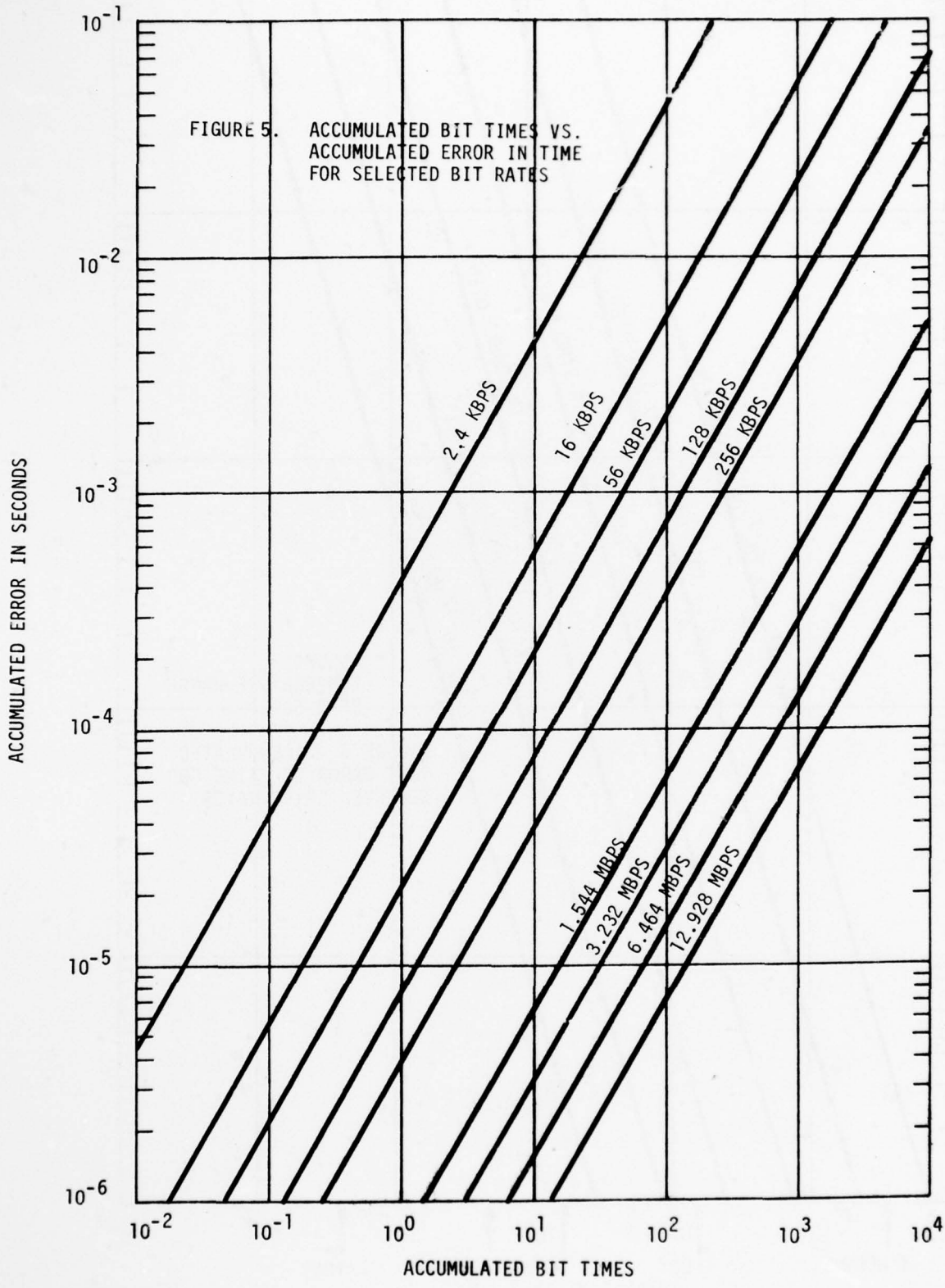


FIGURE 5. ACCUMULATED BIT TIMES VS. ACCUMULATED ERROR IN TIME FOR SELECTED BIT RATES

To determine buffer lengths required to compensate for accumulated phase error, one first selects the time period T over which the buffer is to provide synchronous operation. For a given T, Figures 3 and 4 give contributions to accumulated error in time from frequency inaccuracy and drift between two clocks. From Figure 5 the accumulated error in bit times yields the required buffer length. Since frequency inaccuracy and drift can be either positive or negative in direction, the buffer length must be doubled from that shown in Figure 5. Buffer length selected in this manner represents the worst case that arises from clock perturbations. The underlying assumption is that both frequency inaccuracy and drift are biased in opposite directions between the two clocks. For example, if two clocks are settable within $\pm$ 1 parts in 10^{11}, then the maximum frequency offset is 2×10^{-11}; likewise, if two clocks have long term stability of $\pm$ 1 parts in 10^{12}, then the maximum difference drift rate is 2×10^{-12}. In practice, frequency and drift differences between two clocks are not always biased in opposite directions, but rather are different from one pair of clocks to another. Two characteristics of interest, clock accuracy and stability, are described below.

(1) Clock Accuracy. A specified clock accuracy determines the tolerance of the clock's output frequency relative to the accepted primary standard. Typical accuracies for a variety of timing sources are indicated in Figure 3. These accuracy figures also determine the degree to which any two clocks can be set to the same frequency (called settability or reproducibility). Manufacturers' data indicate positive and negative values to the accuracy. The usual practice in estimating frequency difference between two clocks is to assume opposite direction of offset, i.e., one positive and one negative, since this results in a worse case difference.

(2) Clock Stability. Clock stability specifies the rate at which a clock will drift from nominal frequency over a selected period of time. Table II shows a sampling of manufacturers' stability specifications for a variety of clock types. Contributions to clock instability stem from two sources:

(a) Random fluctuations which dominate for periods up to one day. Note from Table II that deviations from nominal frequency become smaller for longer averaging times for the atomic clocks. Hence, the phase error accumulated due to clock instability will tend to average out to a value smaller than the phase error accumulated due to initial frequency offset.

(b) Systematic variations, which are those changes in frequency that, over a long period of time, tend to be in one direction. Cesium standards do not have any measurable systematic drift, while rubiduim specifications indicate a systematic drift of less than $\pm$ 5 parts in 10^{11} per year. Systematic variations may tend to reverse in sign occasionally; additionally, the direction of drift is peculiar to each particular clock. However, in determining the effect of systematic drift on buffer length, it is assumed that the clock at Node 1 has maximum positive drift and the clock at Node 2 has maximum negative drift, (or vice versa) and that no reversals of sign occur.

TABLE II. TYPICAL CLOCK STABILITY CHARACTERISTICS

STABILITY	CESIUM	RUBIDIUM	QUARTZ (SINGLE OVEN)	QUARTZ (TEMPERATURE COMPENSATED)	QUARTZ
1 sec	$\pm 8 \times 10^{-12}$	$\pm 1 \times 10^{-11}$	$\pm 1 \times 10^{-10}$	$\pm 1 \times 10^{-9}$	$\pm 1 \times 10^{-9}$
1 hr	$\pm 1 \times 10^{-12}$	$\pm 5 \times 10^{-12}$	$\pm 1 \times 10^{-9}$	$\pm 2 \times 10^{-8}$	$\pm 1 \times 10^{-7}$
24 hrs	$\pm 5 \times 10^{-13}$	$\pm 1 \times 10^{-12}$	$\pm 1 \times 10^{-9}$	$\pm 2 \times 10^{-3}$	$\pm 2 \times 10^{-7}$
1 year (includes systematic drift)	$\pm 2 \times 10^{-13}$	$\pm 5 \times 10^{-11}$	$\pm 5 \times 10^{-7}$	$\pm 5 \times 10^{-7}$	$\pm 3 \times 10^{-6}$

b. Time-Varying Propagation Delays. Variations in the delay over a transmission path can cause frequency wander in received timing derived by a radio. Time varying delays are caused by changing meterorologic conditions, such as atmospheric pressure, wind velocity, relative humidity, and temperature. For line-of-sight transmission, long-term (per day) delay variations of 0.1 to 0.2 nanosecond per kilometer have been reported as typical [8]. Thus, typical length LOS paths will experience total delay variations of several nanoseconds. Troposcatter paths experience daily variations which are several orders of magnitude larger than variations observed in line-of-sight. This delay variation is described by the delay power spectrum, which plots average path gain as a function of multipath delay. Typical rms delay values are a few tenths of microseconds for troposcatter paths [9].

Satellite paths experience path delay variation due to (1) satellite orbit inclination, (2) satellite orbit eccentricity, and (3) atmospheric/ ionospheric variations. The orbital plane of the satellite changes slowly over the lifetime of the satellite. To compensate for this effect, the satellite is injected initially with a maximum plane tilt in one direction and is allowed to drift through 0^{o} to a maximum in the opposite direction. The magnitude of plane tilt is maximum at the beginning and end of the satellite lifetime. The path delay varies over its range daily, and has magnitude of a few milliseconds (1-4 ms) for DSCS II satellites. The second factor contributing to daily variations is the orbit eccentricity, or lack of a perfectly circular orbit. With the present DSCS limit on allowed eccentricity of 0.01, the maximum variation in delay is 5.6 ms. There are also the usual atmospheric and ionospheric mechanisms that cause change in the index of refraction. Resulting changes in delay are independent of orbital parameters and are smaller in magnitude, with 1 millisecond being an upper bound. Assuming each of the above described phenomena is independent, the delay variations add to yield a worst case prediction of roughly 10.4 ms [10].

c. Buffer Lengths. Table III provides buffer length requirements in number of bits for both terrestrial and satellite applications. The length of the buffer is set so that the phase error which accumulates during the buffer reset period is exactly absorbed by the buffer. For each of a number of bit rates, buffer lengths were calculated as a sum of accumulated phase differences due to clock differences (found from Figure 5) and propagation delay variations. Since the bias of any two clocks is unknown and to allow any combination of initial satellite orbital parameters, each buffer length is specified as plus and minus the maximum length required. In this way, the buffer can initially be set at mid position and allowed to move in either direction to its specified maximum. Also, the timing subsystem is assumed to use LORAN C or equivalent with accuracy of $\pm$ 1 x 10^{+11} and with negligible drift.

Buffer requirements shown for terrestrial applications are based on the allocation of MTTS for the DCS reference channel, which comprises 14 LOS links and one troposcatter link. From Table III it can be seen that phase error due to clock differences is much greater than phase error due to propagation delay variations in LOS and troposcatter. Also note that the buffer reset period, derived from MTTS allocation given in Figure 2, is influenced by where the buffer is located in the multiplex hierarchy. For low level placement, buffers would be located only at the ends of the reference channel, where there are low-speed synchronous interfaces. For higher level placement, buffers would be located at the receive side for each mission bit stream, that is, at every major node of the reference channel.

For satellite applications, buffer placement is specified as lower level, since synchronous interfaces between terrestrial and satellite transmission facilities will always be at low speed rates. The required buffer lengths shwon in Table III are a result of the large delay variation encountered in satellite transmission. It is assumed that since satellite transmission nodes are in general collated with terrestrial transmission nodes, LORAN C (or equivalent) clocks will be available and utilized to provide the required 1 x 10^{-11} clock accuracy. Otherwise, timing would be provided by internal DSCS standards which are accurate to only approximately 1 x 10^{-7}. Use of this internal standard would reduce the buffer reset period considerably. For example, if the 2048 bit satellite buffer (see p.24) were used in conjunction with 1 x 10^{-7} clocks, the following buffer reset periods would result:

BIT RATE	BUFFER RESET PERIOD
128 kb/s	7.7 hours
56 kb/s	36 hours
32 kb/s	74 hours
16 kb/s	163 hours

Finally, buffer lengths provided in Table III will allow the DCS reference channel to meet its MTTS allocation given in Figure 2, assuming that LORAN C is available and provides frequency accuracies of 1 part in 10^{11} or better. During periods of LORAN C outage, the AN/GSQ-183 will use its

TABLE III. BUFFER LENGTH REQUIREMENTS FOR DCS REFERENCE CHANNEL

BUFFER LOCATION	CLOCK ACCURACY	PROPAGATION DELAY VARIATIONS	BUFFER RESET PERIOD	BUFFER LENGTH REQUIREMENTS IN BITS	
				BIT RATE	BUFFER LENGTH
Lower Level (terrestrial)	$\pm 1 \times 10^{-11}$	LOS, 30 mi: 10 nsec TROPO, 180 mi: 0.4 μsec	240 hrs	512 kb/s 256 kb/s 128 kb/s 56 kb/s	± 8 bits ± 4 bits ± 2 bits ± 1 bits
Higher Level (terrestrial)	$\pm 1 \times 10^{-11}$	LOS, 30 mi: 10 nsec TROPO, 180 mi: 0.4 μsec	1200 hrs	12.928 Mb/s 9.696 Mb/s 6.464 Mb/s 3.232 Mb/s	±1120 bits ± 840 bits ± 560 bits ± 280 bits
Lower Level (satellite)	$\pm 1 \times 10^{-11}$	Satellite, 10.4 ms	240 hrs	128 kb/s 56 kb/s 32 kb/s 16 kb/s	±1332 bits ± 583 bits ± 333 bits ± 167 bits

internal quartz oscillators, with accuracy of 1 part in 10^9. For such periods, the buffer reset period would be reduced by two orders of magnitude, corresponding to the difference between 10^{-9} and 10^{-11} frequency accuracies. Looking at Figure 2, the MTTS per DCS reference channel would be reduced from 240 hours to 2.4 hours and the overseas terrestrial segment would have its MTTS reduced from 60 hours to 0.6 hours, so that this 24 hour MTTS objective for the global reference channel would be reduced to approximately 0.6 hours. Considering the average call duration (5-10 minutes), a 0.6 hour MTTS appears to be satisfactory for those short and infrequent periods when LORAN C would not be available.

TABLE IV. MEAN TIME TO RECOVER TIMING FOR BUFFER UNDERFLOW/OVERFLOW

	MEAN TIME TO RECOVER TIMING	
EQUIPMENT	LOWER LEVEL BUFFER	HIGHER LEVEL BUFFER
Trunk Encryption Device (TED)		
(a) Two Satellite Hop Circuit		2005 ms
(b) One Satellite Hop Circuit	-	1005 ms
(c) Non-Satellite Circuit	-	5 ms
Level 2 Multiplexer	-	5 ms
Level 1 Multiplexer	-	10 ms
Submultiplexer	50 ms	50 ms
Digital Secure Voice Terminal (DSVT)		
(a) Two Satellite Circuit	2500 ms	2500 ms
(b) One Satellite Circuit	1500 ms	1500 ms
(c) Non-Satellite Circuit	500 ms	500 ms
TOTAL		
(a) Two Satellite Hop Circuit	2550 ms	4570 ms
(b) One Satellite Hop Circuit	1550 ms	2570 ms
(c) Non-Satellite Circuit	550 ms	570 ms

4. ALLOCATION OF MEAN TIME TO RECOVER TIMING

For each loss of BCI due to buffer overflow or underflow, a short term outage occurs which has a length equal to the MTRT. The MTRT is determined by the time required to resynchronize the multiplexers, trunk encryption device, and end instrument (DSVT) which experience loss of synchronization due to buffer overflow/underflow. This resynchronization time is shown in Table IV for both the higher and lower level buffer configurations, and for both satellite and non-satellite circuits.

The MTRT's shown for each multiplexer equipment are based on the mean time to acquire frame synchronization as given in each particular equipment specification. Each multiplexer provides in-band synchronization (i.e., framing bits are sent continuously such that resynchronization does not require a cooperative effort between the two ends of the TDM link.) However, the encryption technique employed in the TED and DSVT both require a cooperative cycle (handshake) to perform resynchronization. The resultant transmission delay (two round trips are required) for the TED and DSVT is negligible for non-satellite circuits but becomes the dominant contributer to MTRT for satellite circuits (assuming 500ms per satellite round trip).

The total time required to recover BCI is given as the sum of each equipment resynchronization time, since a given level of the multiplex hierarchy much achieve resynchronization before subordinate levels can also resynchronize. The time to actually reset the buffer, upon overflow or underflow, is negligible and is therefore not shown.

The MTRT is largely dominated by the number of satellite hops traversed by the circuit. The two satellite hop circuit represents the global reference channel and has a MTRT of approximately 2.5 seconds for the lower level buffer and 4.5 seconds for the higher level buffer. The non-satellite circuit is representative of the DCS reference channel and has a MTRT of approximately .5 seconds regardless of buffer location. Use of the lower level buffer indicates a somewhat shorter recovery time when compared to the higher level buffer. With the lower level buffer, only the DSVT and submultiplexer will lose synchronization upon buffer overflow/underflow, while higher level buffer overflow/underflow will cause loss of synchronization in the DSVT, TED, and all levels of multiplex.

It should be noted that the MTRT's shown in Table IV are actually the recovery times for any loss of synchronization, due to loss of bit synchronization, frame synchronization, or pulse stuffing synchronization, as well as due to loss of buffer synchronization. Unavailability due to a particular kind of synchronization loss can then be calculated as the ratio of MTRT to MTTS.

Under normal operating conditions unavailability due to all losses of synchronization will be negligible compared to unavailability due to equipment failures and propagation outages. However, in the event that LORAN C becomes unavailable, the MTTS due to loss of buffer synchronization will be reduced by two orders of magnitude, while the MTRT is unaffected by whether or not LORAN C is available. The corresponding unavailability will then be degraded for periods when LORAN C is unavailable. However, a calculation of this degraded unavailability shows that it is still less than unavailability due to either equipment failures or propagation outages.

IV. EQUIPMENT TIMING CHARACTERISTICS

Components of the DCS II timing subsystem will be described in this chapter, to include station clock, the clock distribution system, and buffers. The timing subsystem is plesiochronous, derived from LORAN C station clocks, and will use buffers to maintain synchronization between major timing nodes. The desirability and acceptability of a LORAN-based timing subsystem is reviewed and comparisons are given with the independent clock concept. By convention, buffers are built directly into the uncombined side of each appropriate transmission equipment. Timing characteristics of each transmission and perpherial equipment are also described. For transmit timing, each equipment is specified to accept external clock (from the clock distribution system) and to provide a synchronous interface on its uncombined side. Receive timing is derived from the incoming signal (RF or baseband) and is provided, along with data, to the next lower equipment level.

1. TIMING SUBSYSTEM

a. Station Clock. The station clock will supply a highly accurate and stable timing source for major DCS transmission nodes. When combined with a clock distribution system, the station clock will provide all required clocked frequencies to DCS equipments. Characteristics of alternative clock sources are discussed in chapter III. It is desirable that an atomic source be utilized to provide the accuracy and stability desired for DCS applications. Two choices for the DCS II Timing Subsystem are considered here: (1) independent atomic clocks, and (2) LORAN C. Each of these two candidates could be utilized with off-the-shelf technology, a necessary condition for application to a near-term DCS timing subsystem. These two candidates are discussed qualitatively in the following paragraphs.

(1) Independent atomic clocks have the advantage of being independent of an outside timing source (as in LORAN C); individual timing sources are provided to each major timing node. Such a timing subsystem is highly survivable, since there is complete independence between all sources in the system. A significant drawback to this approach is the cost for providing individual atomic sources to each site. However, TRI-TAC uses independent atomic clocks, primarily because of the survivability aspect. A description of the TRI-TAC timing system is given in Appendix A.

(2) LORAN C is a pulsed low-frequency radio navigational and timing system operated throughout the Northern hemisphere by the U.S. Coast Guard. All LORAN C transmitting stations are equipped with cesium frequency standards. Synchronization among these frequency standards is

maintained by monitoring and updating each standard in comparison to UTC. LORAN C coverage is currently available to nearly all DCS sites, and full coverage is anticipated by 1985. Appendix B provides a detailed description of the LORAN C system; also a description is given of the AN/GSQ-183 Frequency Control Set which is currently used in DCS Networks (Channel Packing and AUTODIN) to receive LORAN C timing.

LORAN C has been selected as the clock source for the near term DCS timing subsystem primarily because of its low cost, off-the-shelf availability, commonality with existing DCS timing standards, and proven performance. Cost of the existing AN/GSQ-183 is known to be less than the planned TRI-TAC cesium frequency standard (Hewlett Packard 5062C). Additionally, the GSQ-183 provides a complete timing subsystem including antenna, LORAN C receiver, two crystal oscillators, and power supply, whereas the cesium frequency standard requires additional equipment including power supply and some alternate clock source. Considerable experience has been gained with the GSQ-183 as a result of AUTODIN and Channel Packing applications. Continued use of the GSQ-183 would thus take advantage of field experience and provide commonality with existing logistics support.

Performance of the LORAN C system for timing and frequency dissemination has been well documented [11, 12]. Frequency accuracy of 1 part in 10^{12} is easily attainable and accuracy of a few parts in 10^{14} is in fact typical. Such performance cannot be achieved with independent atomic clocks. Also, if a given transmission node experiences loss of LORAN C due to equipment failure or signal loss, the AN/GSQ-183 provides automatic switchover to doubly redundant, temperature compensated crystal oscillators, with clock accuracy of 1 part in 10^{9}. Buffer reset periods are of course shortened with this degraded clock accuracy, but as indicated in Chapter III, the degradation would certainly be tolerable if confined to a small percentage of total operating time. In summary, the AN/GSQ-183 timing subsystem provides superior performance under normal LORAN C coverage and can also provide acceptable performance in the absence of LORAN C coverage.

The AN/GSQ-183 (or equivalent) is the intended timing source, to be used in conjunction with a clock distribution system to provide synchronous timing to DCS equipments. The block diagram of Figure 6 shows the LORAN C receiver, the frequency multiplier, and two quartz oscillators which make up the AN/GSQ-183. It is also worth noting that an alternate reference can be supplied to the frequency multiplier and used as either the primary or secondary source. This feature will allow the integration of a future timing subsystem directly into the AN/GSQ-183.

b. Clock Distribution System. The clock distribution system interfaces with the station clock to generate and distribute timing signals to transmission and switching equipments. For application with the AN/GSQ-183, the clock distribution system must interface with each of three 1 MHz frequency standards. In order to meet DCS availability objectives, redundant

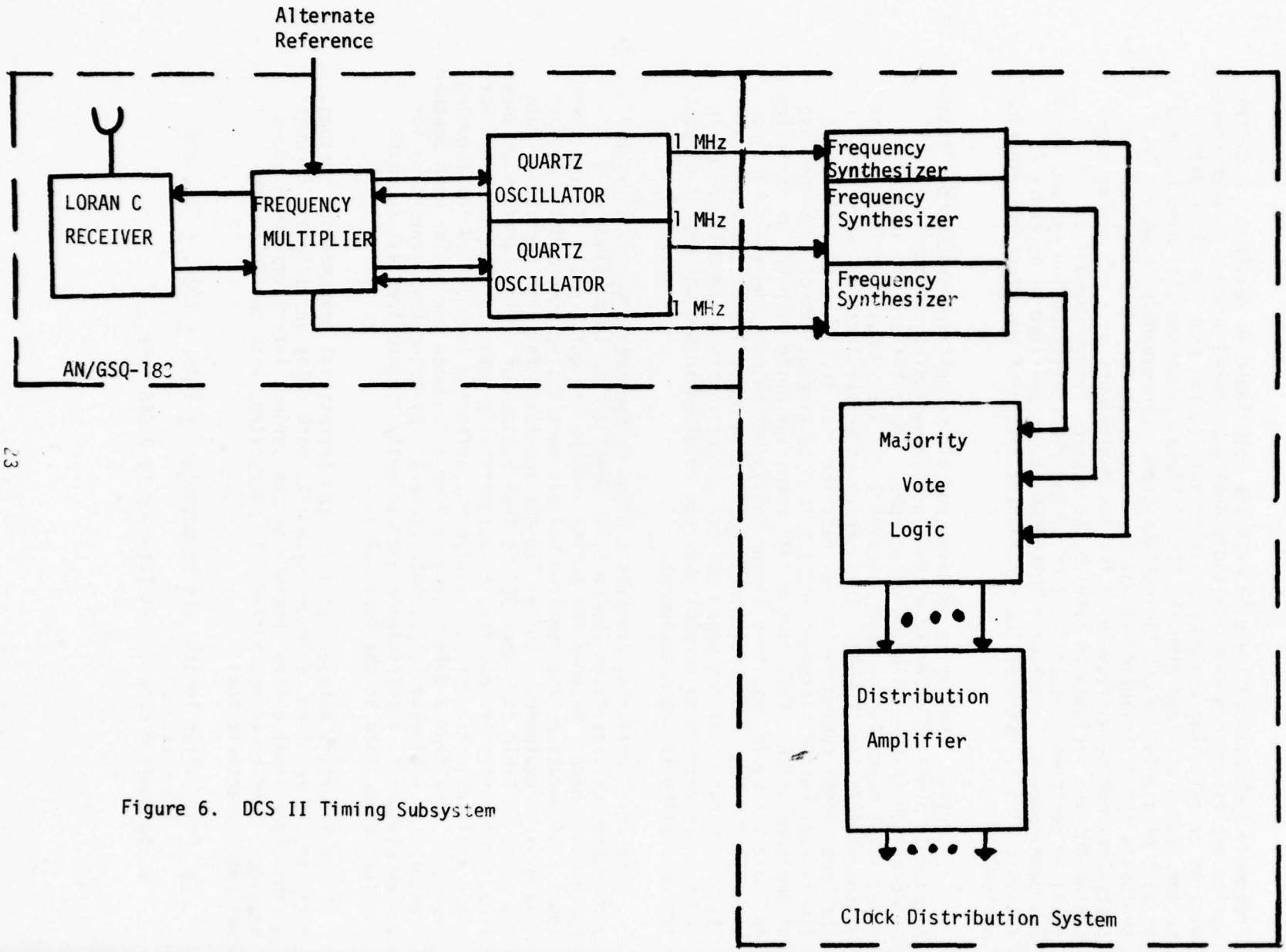


Figure 6. DCS II Timing Subsystem

frequency synthesis followed by majority vote logic is required. A distribution amplifier then provides individually buffered outputs to each transmission or switching equipment. It is anticipated that the clock distribuiton system utilized with the DCS II Timing Subsystem will also be used as part of any future DCS timing subsystem. Consequently, some of the synthesis and distribution capability built into the clock distribution system may not be applicable to initial deployments of a DCS timing subsystem but are included to provide the desired future capability. A detailed performance specification of the clock distribution system, which was developed in support of AUTOSEVOCOM II, is provided as Appendix C. Figure 6 also illustrates the fundamental design of the clock distribution system.

c. Buffer. Buffering required for all terrestrial synchronous transmission is provided directly within each transmission equipment, as will be described in the following paragraphs. These buffers are located in lower-level multiplex equipment (Level 1 mux and submux) and in switching equipment (DAX and TTC-39). This choice of buffer location corresponds to the lower level configuration, as described earlier. The selection of a lower-level buffer placement results from considerations of cost and ease of implementation. Buffering at MBS rates for buffer lengths as indicated in Table III would result in longer delays per channel and would require higher technology and hence higher costs than buffering at low speed rates. The incorporation of low speed buffers directly within transmission equipments has already been accomplished and resulted in minimal impact on cost and complexity for each equipment.

Low level buffering provides a means of synchronizing all low-speed plesiochronous interfaces (below 1.544 Mb/s) to the local clock at a synchronous node. Because the buffer lengths are quite small for the lower level configuration, the required buffers were easily accommodated in each transmission equipment. Buffer lengths specified for each particular rate are given in Table IV. When BCI is lost because of buffer overflow or underflow, each buffer is specified to automatically reset to mid position. For every applicable transmission equipment, buffering is provided for incoming (receive) data from a data source or from a tandemed connection with another transmission equipment (e.g., multiplexer). By using this convention for buffer placement, a multiplexer automatically synchronizes all incoming plesiochronous data to the local clock.

For interface between satellite and terrestrial transmission systems, buffering is required to remove satellite path delay variations. Because of the significant buffer lengths and the various interfaces required, a separate, self-contained buffer will be utilized with the following salient characteristics:

- Four buffer lengths are selectable: $\pm$ 2048, $\pm$ 1024, $\pm$ 512, and $\pm$ 256 bits.
- The buffer operates at rates up to 2.048 Mb/s.

- The ± 2048 bit buffer is sufficient to compensate for satellite delay variations for rates up to 128 kb/s.

- The shortest buffer length, ± 256 bits, is more than sufficient to compensate for clock frequency differences in terrestrial applications for rates up to 2.048 Mb/s, so that this buffer can be used for terrestrial applications at any rate up to the maximum (2.048 Mb/s).

- The buffer includes a local reset, manual reset, and automatic reset, any one of which provides for reset of the buffer to mid-position.

Reference [13] provides additional detail regarding the characteristics of this satellite delay buffer.

2. DRAMA EQUIPMENT

a. AN/FCC-98 (Formerly TD-1192) Multiplexer. The DRAMA AN/FCC-98 is a 24-channel PCM, Level 1 multiplexer with provision for synchronous data at 56, 64, 128, 256, and 512 kb/s. AN/FCC-98 timing characteristics are illustrated in Figure 7 and briefly described herein (for detailed specifications see reference [14]).

(1) Transmit Timing.* As shown in Figure 7(a), transmit timing can be provided by an internal oscillator (with initial accuracy of ± 3 parts in 10^5) or from an external timing source. The transmit source is then used to generate clock rates as required for synchronous data channels. Each synchronous data card provides a timing signal to clock data out of the data terminal equipment (DTE), as shown in Figure 7(a), and also provides for phase adjustment between the clock out and data in. Each synchronous card also buffers data received from the data source or tandemed from another Level 1 multiplexer, as indicated in Figure 7(c). These buffers are clocked in by receive timing associated with the DTE or adjacent multiplexer and are clocked out by transmit timing internal to the FCC-98. Buffer lengths of 8, 16, 32, and 64 bits are provided with synchronous rates of 56/64, 128, 256, and 512 kb/s, respectively.

* For the purposes of this technical report, transmit timing is defined as timing associated with the transmit direction of transmission, i.e., from the uncombined side toward the combined side, from the unmodulated side toward the modulated side, from the unencrypted side toward the encrypted side, etc.

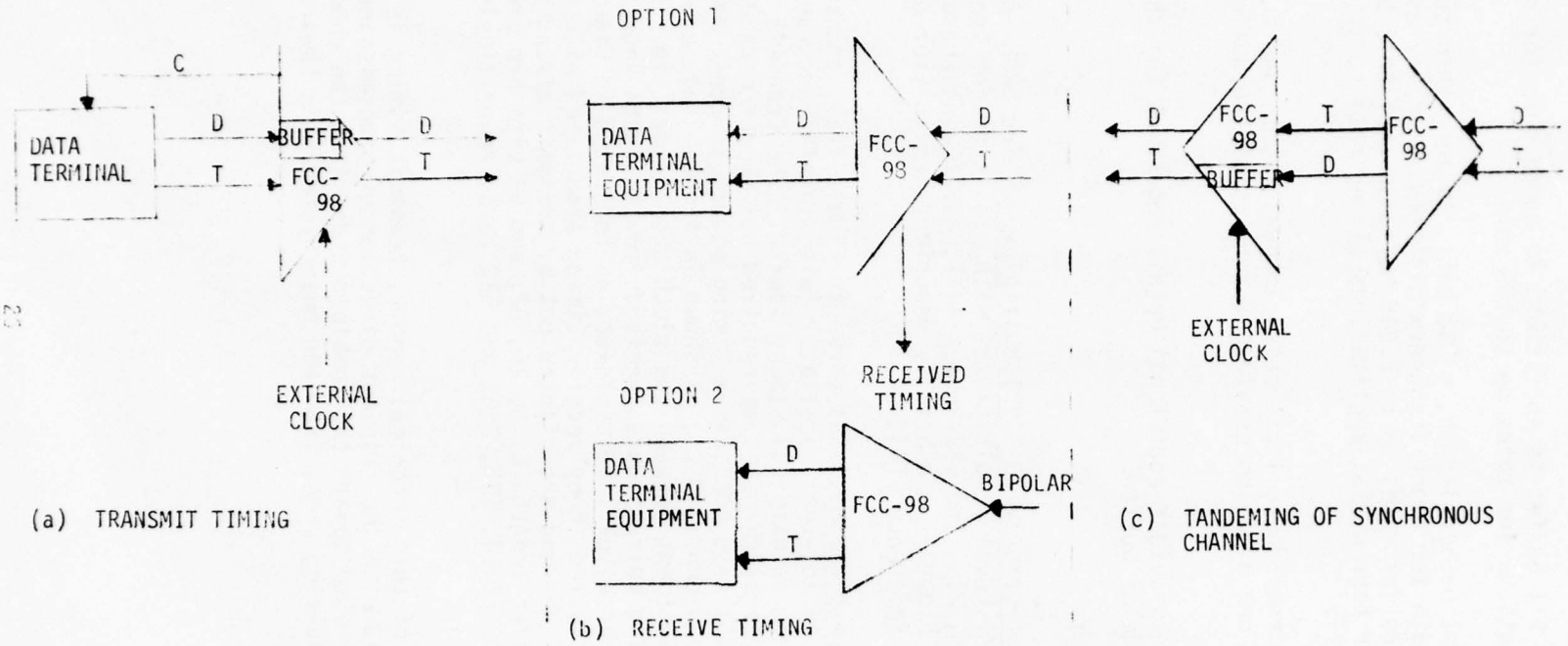


Figure 7. DRAMA FCC-98 Timing Characteristics

(2) Receive Timing.* Receive timing at 1.544 Mb/s is recovered at the combined side of the multiplexer from either (a) received NRZ data and timing or (b) recieved bipolar signal, as shown in Figure 7(b). Recovered receive timing is provided as an output available through a connector. This received timing is then divided down to individual channel rates and is provided as receive timing directly to the DTE.

b. TD-1193 Multiplexer. The DRAMA TD-1193 is a 2/4/6/8 port Level 2 multiplexer with provision for asynchronous or synchronous interface and for port strapping of 1.544 Mb/s to create 3.088 and 6.176 Mb/s input ports. Figure 8 illustrates TD-1193 timing characteristics, which are further described below (for additional information, see reference [15]):

(1) Transmit Timing. Transmit timing is normally provided by an external source (e.g., radio) but can also be provided by an internal oscillator (with initial accuracy of ± 5 parts in 10^5), as shown in Figure 8(a). Any input port rate (1.544, 3.088, or 6.176 Mb/s) can be interfaced synchronously or asynchronously, as illustrated in Figure 8(a). For the synchronous option, the TD-1193 provides source timing to the data terminal equipment (Level 1 multiplexer). A one bit buffer also allows adjustment of the phasing between lock out and data in. For the asynchronous option, the TD-1193 accepts the DTE data and timing and uses pulse stuffing to account for frequency differences between the DTE and TD-1193.

(2) Receive Timing. As shown in Figure 8(b), recieve timing, along with NRZ data, is provided to the TD-1193 demultiplexer at the MBS rate from the radio. The TD-1193 provides that received timing as an output available through a connector. Receive timing for each port is then derived from this received MBS timing. For synchronous ports, receive timing is derived using a fixed rate conversion from the MBS timing. For asynchronous ports, a smoothing loop is used to derive received timing from the destuffed data rate.

(3) Tandeming. Tandeming of a synchronous 1.544 Mb/s (also 3.088 and 6.176 Mb/s) channel is accomplished via one of two options. Option one provides a separate, self-contained buffer (no internal buffering is provided in the TD-1193), as indicated in Figure 8(c). Data is clocked into the buffer by receive timing of the first TD-1193 demultiplexer and clocked out by transmit timing of the second TD-1193 multiplexer. Option 2 utilizes the pulse stuffing interface of the TD-1193 multiplexer to accept the independently timed data from another TD-1193 demultiplexer. Use of this interface will introduce slewing jitter and occasional loss of BCI due to stuff word errors at the far end demultiplexer; however, timing accuracy inherent in the 1.544 Mb/s channel is otherwise left unperturbed by the pulse stuffing operation.

* For the purposes of this technical report, receive timing is defined as timing associated with the receive direction of transmission, i.e., from combined to the uncombined side, from modulated to the unmodulated side, and from encrypted to unencrypted side, etc.

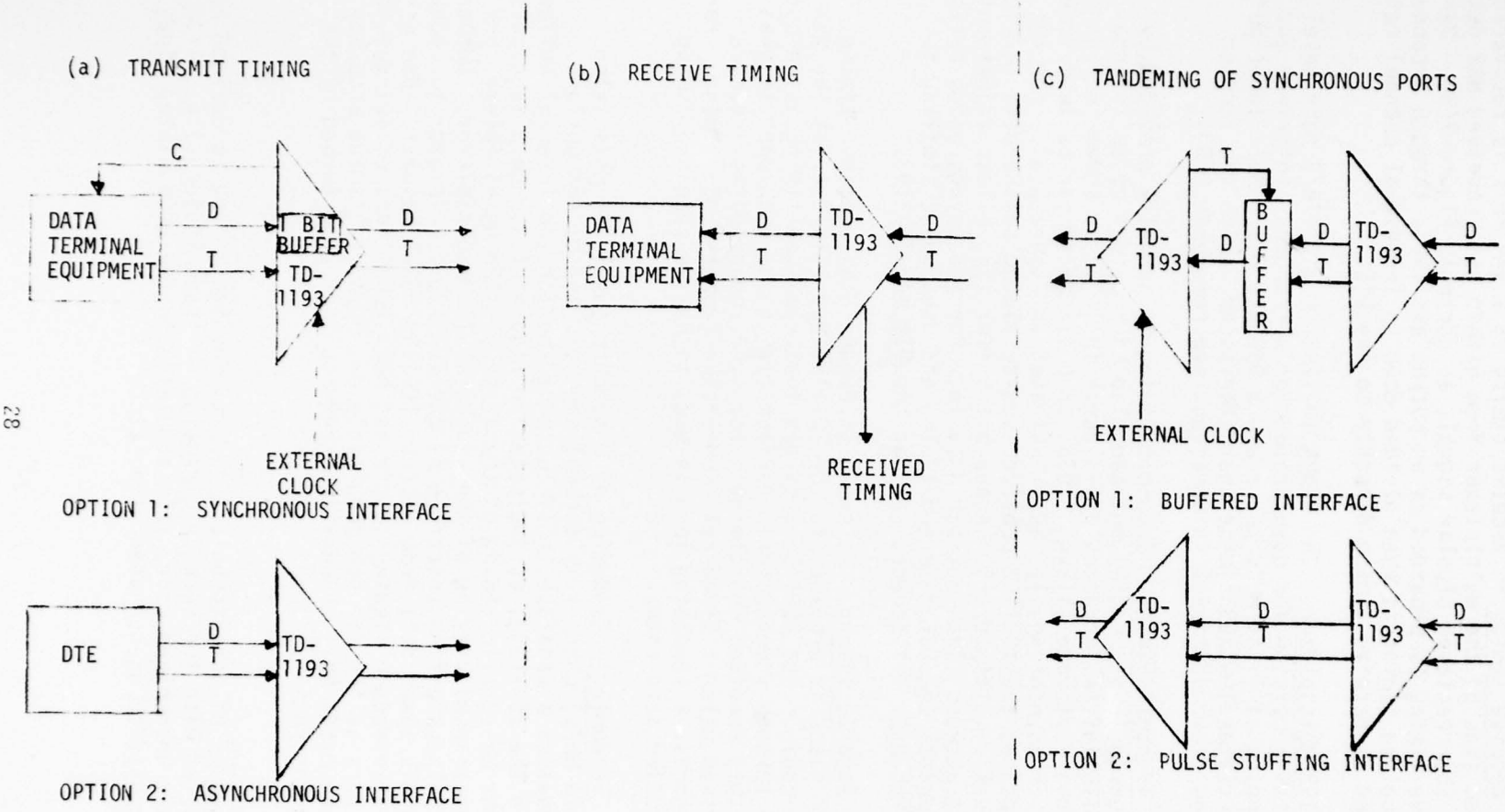


Figure 8. DRAMA TD-1193 Timing Characteristics

c. FRC- ( ) ( ) Digital Radio. The DRAMA FRC-( ) ( ) digital radio provides synchronous transmission up to 25.856 Mb/s for microwave line-of-sight links. Timing characteristics of the FRC-( ) ( ) are illustrated in Figure 9 and are briefly described below (for details, see reference [16]).

(1) Transmit Timing. Transmit timing is provided by an internal oscillator with initial accuracy of + 3 parts in 10^6, or from an external clock source. The radio is also specified to switch from the external clock source to its internal oscillator if either the external source is lost or a command level is applied to a connector on the radio. As shown in Figure 9(a), the FRC-( ) ( ) provides source timing to the TD-1193 and also provides phase adjustment on the incoming MBS data.

(2) Receive Side. Receive timing is recovered from the incoming RF signal and is provided as an output available through a connector as well as an output to the TD-1193 multiplexer.

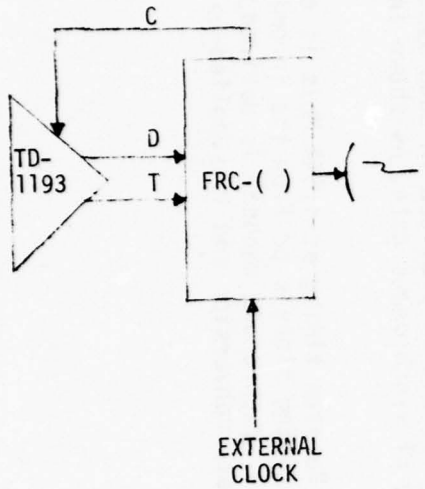
(3) Tandeming. Simple straight-through repeating at MBS rates is accomplished by clocking the transmit direction of one radio with receive timing from the other radio, as shown in Figure 9(c). One MBS can be tandemed while a second, parallel MBS is demultiplexed and remultiplexed via the TD-1193 by using receive timing from one radio to clock transmit timing in both the second radio and its associated TD-1193, as shown in Figure 9(d).

3. FKV CONFIGURATION

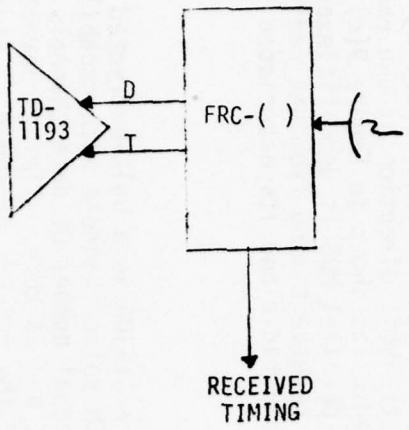
a. CY-104 Multiplexer. The CY-104 is a bulk-encrypted Level 1 multiplexer which provides 24 PCM voice channels with capability to replace up to 5 voice channels with an equal number of data channels including synchronous rates of 32, 48, 56, and 64 kb/s. Timing characteristics are essentially the same as those of the FCC-98, as shown in Figure 7 and described below.

(1) Transmit Timing. Transmit timing is provided by an oscillator internal to the HN-74 Interface Unit or from an external source. Synchronous data channels provide a timing signal to clock data out of the DTE. Buffering of $\pm$ 1/2 bit is provided in each synchronous data channel to allow tandeming of synchronous data, as shown in Figure 7 (c).

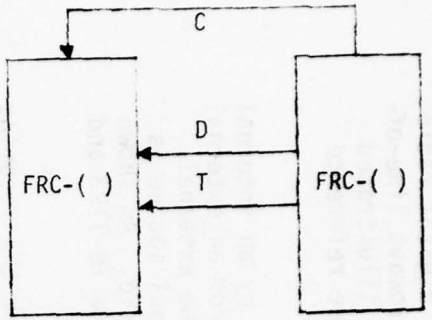
(2) Receive Timing. Receive timing at 1.544 Mb/s is derived from the incoming NRZ data and timing signals or from the incoming bipolar signal. Receive timing for each synchronous channel is derived then from 1.544 Mb/s receive timing by simple rate conversion and is supplied to the DTE along with NRZ data.



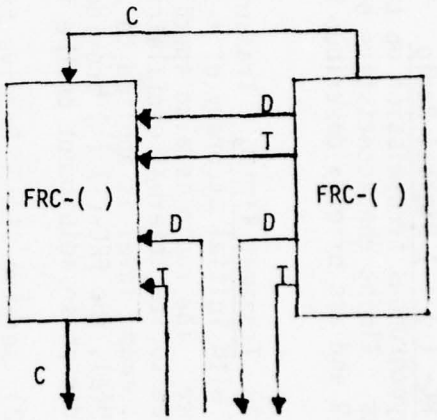
(a) TRANSMIT TIMING



(b) RECEIVE TIMING



(c) TANDEMING OF MBS WITH NO CHANNEL BREAKOUT



(d) TANDEMING OF MBS WITH CHANNEL BREAKOUT

Figure 9. DRAMA FRC-( ) Timing Characteristics

b. AN/FCC-97 Multiplexer. The FCC-97 is a Level 2 multiplexer which combines up to eight asynchronous 1.544 Mb/s signals and provides partial response modulation for direct interface with an FM radio. Timing characteristics are as follows.

(1) Transmit Timing. The transmit partial response signal is timed by an internal oscillator, but can also be synchronized to an external clock source.* For each input port (1.544 Mb/s), the incoming transmit signal from a DTE is in bipolar format without timing. There is no provision for providing true synchronous transmission since all channels are pulse stuffed. Thus, 1.544 Mb/s channels are trandemed via pulse stuffing without the use of synchronous buffering.

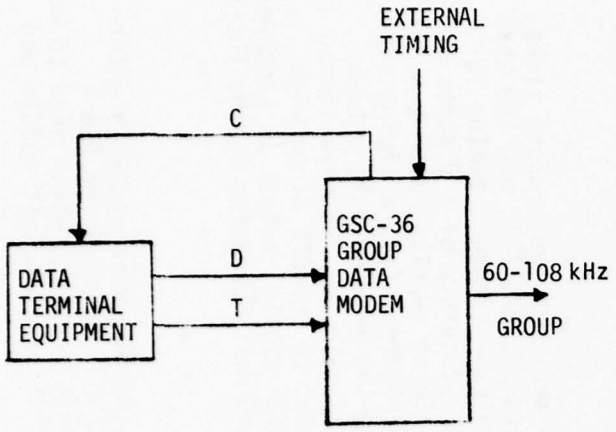
(2) Receive Timing. Receive timing is extracted as part of the decoding of the partial response signal. This receive timing at the MBS rate is then used in deriving timing associated with each receive port. The receive data and timing signals for each port are then transformed into bipolar format for routing to a data terminal equipment (Level 1 multiplexer).

4. MODEM EQUIPMENTS

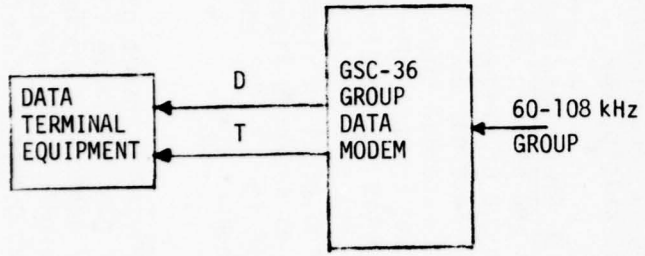
a. MD-918 Troposcatter Modem. The MD-918 digital troposcatter modem will provide synchronous transmission of up to 12.928 Mb/s over troposcatter links. Timing characteristics are nearly identical to those of the FRC- ( ) ( ) digital LOS radio, as shown in Figure 9. Transmit timing will be provided by external clock at a standard frequency (1 or 5 MHz). The troposcatter modem will provide source timing to the TD-1193 and also provide phase adjustment on the incoming MBS data. Receive timing is recovered from the incoming RF signal and is an output to the TD-1193 multiplexer.

b. GSC-36 Group Data Modem. The GSC-36 provides synchronous transmission of 56 and 64 kb/s over a half-group and 56, 64, 112, and 128 kb/s over a full group of Frequency Division Multiplex. Transmit timing is provided by an internal oscillator with initial accuracy of $\pm$ 3 parts in 10^5, or by an external timing source, or by timing supplied with the data source. For the transmit direction, shown in Figure 10(a), a timing signal is supplied to the DTE to clock out data. Phasing between this output timing signal and data input to the modem is adjustable. Receive timing is derived from the received signal and is provided to the DTE along with receive data, as shown in Figure 10(b). The GDM digital output is tandemed with the FCC-98 (or CY-104) data channel by internal buffering in the FCC-98 (or CY-104) channel card.

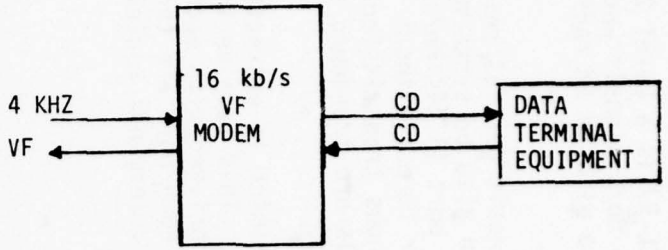
* A newly developed transmit common equipment module, which accepts external timing, is now available in the FCC-97 and will be used for DEB I. Present FCC-97 equipments implemented with the FKV Project would need to be retrofitted (simple card replacement) to add this new transmit module and thus allow timing from an external source.



(a) GDM TRANSMIT TIMING



(b) GDM RECEIVE TIMING



(c) VF MODEM TIMING

Figure 10. Channel and Group Modem Timing Characteristics

c. 16 Kb/s VF Modem. The 16 kb/s VF Modem provides synchronous transmission of 16 kb/s data over a 4 kHz VF channel. Timing characteristics of the modem are illustrated in Figure 10(c). In the transmit direction, on the digital side, the modem locks its internal oscillator to the incoming signal which is in conditioned diphase (CD) format. The VF modulated signal, transmit direction, is then timed from this slaved internal oscillator. Receive timing is derived directly from the demodulated signal. This receive timing is then directly input to the DTE. Thus, the modem is slaved to external timing for both direction of transmission such that external (and presumably) accurate timing is propagated in both transmit and receive directions. Additionally, no buffering is required to interface the modem with a DTE.

An alternative timing configuration may be required for those cases where poor quality timing is extracted from the conditioned diphase signal. If the DSVT is far removed from the modem or if the VF circuit is of poor quality, timing extracted from the incoming signal may not be accurate or stable enough to provide satisfactory performance. For these cases, the VF modem could use its own internal clock. However, the need then arises to provide a more accurate internal oscillator and a buffer to allow synchronization of the incoming conditioned diphase signal.

5. LOW SPEED TDM (OR SUBMULTIPLEXER)

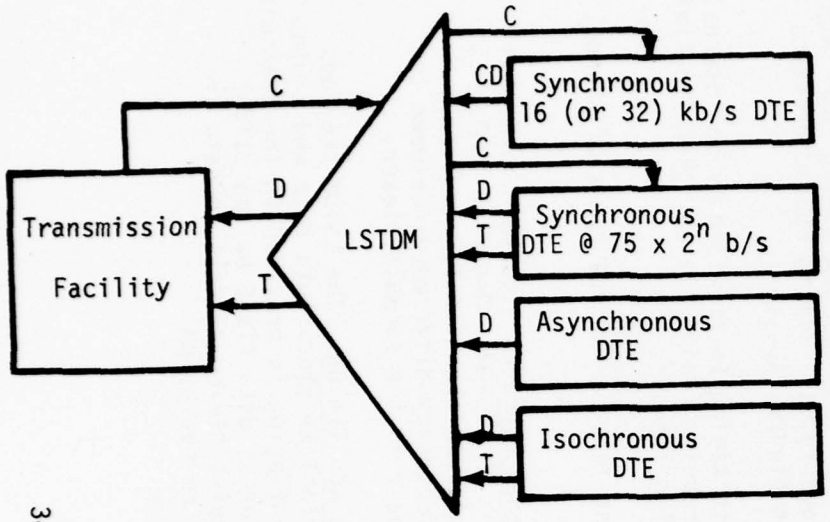
The low speed TDM (LSTDM) will combine several low and medium speed channels into a higher output rate for transmission over either digital (via Level 1 multiplexer) or analog (VF or group modem) facilities. Channel rates will include synchronous 8000N b/s with NRZ or conditioned diphase interface, synchronous 75×2^N b/s with NRZ and timing interface, and various asynchronous and isochronous rates. Timing characteristics are described below and illustrated in Figure 11.

a. Combined Side Timing. Transmit timing is provided by an internal oscillator, by external clock, or by receive (loop) timing. Receive timing is derived from incoming data and timing lines.

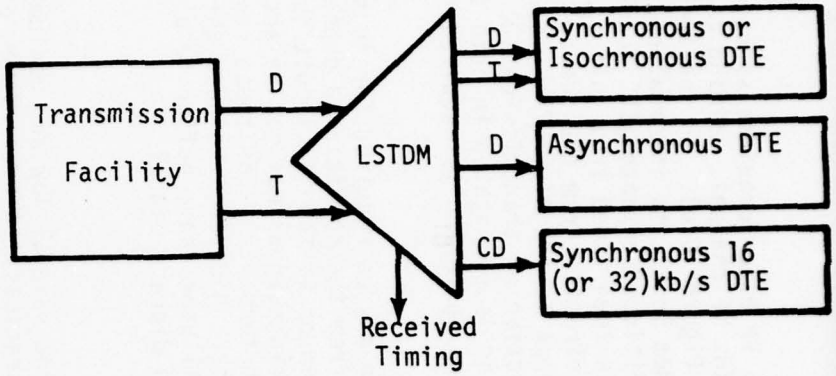
b. Uncombined Side Timing. Timing for the various types of channel inputs is described below.

(1) Synchronous with Conditioned Diphase. Transmit timing is provided to the synchronous terminal by the LSTDM. Received timing is imbedded in the outgoing diphase signal. As shown in Figure 11(c), buffering is provided to account for frequency differences between the incoming diphase signal and the time base in the submultiplexer.

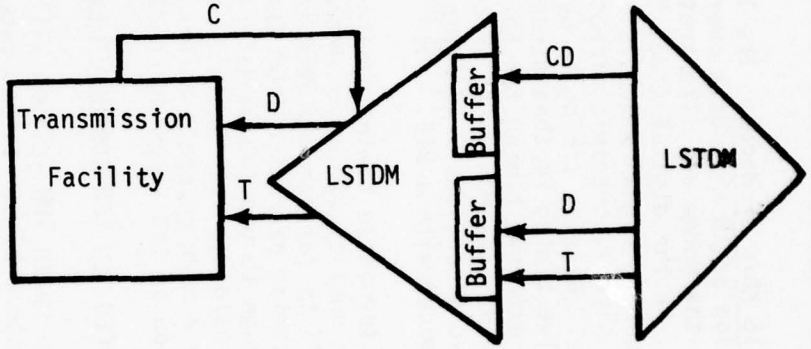
(2) Synchronous with NRZ Data and Timing. The LSTDM provides transmit clock to the synchronous terminal to clock both data and timing into the multiplexer. Additionally, buffering is provided in the transmit direction to allow tandeming of synchronous data timed by two different sources as shown in Figure 11(c). Receive timing as well as data are provided to the synchronous terminal from the LSTDM.



(a) Submultiplexer Transmit Timing



(b) Submultiplexer Receive Timing



(c) Tandeming of Synchronous Data

Figure 11. Low Speed TDM Timing Characteristics

(3) Asynchronous/Isochronous. Asynchronous terminals are characterized as having only a data input/output, without a timing line, for both transmit and receive. Isochronous terminals provide both data and timing lines, but cannot be slaved to an external timing source. For both types of terminals, the LSTDM must provide a special interface (e.g., pulse stuffing, buffering). Tandeming is provided by this same special interface.

6. OTHER EQUIPMENT

a. KG-81 Trunk Encryption Device. The KG-81 is an encryption device which operates at rates from 10 kb/s to 20 Mb/s and has the following timing characteristics.

(1) Transmit timing must be supplied by an external, black timing source; the KG-81 has no provision for internal timing nor can the KG-81 accept timing from its subordinate, red (unencrypted) multiplexer. This external timing source is used by the KG-81 to clock data out of the subordinate multiplexer. After encrypting the incoming data, both data and timing signals are transmitted to the next level within the transmission hierarchy.

(2) In the receive direction, encrypted data and timing are provided to the KG-81 from the radio or higher level multiplexer. After decryption, data and timing signals are output to the subordinate multiplexer.

b. TTC-39 Switch. The TTC-39 switch derives transmit timing from one of two sources: (1) external timing from a station clock which provides a standard frequency (e.g., 5 MHz), or (2) timing recovered from an incoming transmission group. A frequency synthesizer within the TTC-39 generates all required clock rates from the timing standard. All transmit data are then synchronous with the timing standard.

In the receive direction, the TTC-39 switch extracts timing from the conditioned diphase format of each incoming signal. This extracted timing is used to clock received data into a 256 bit buffer. Each buffer is then clocked out by internal transmit timing, thus providing synchronism of transmit and receive data.

c. ULS. Timing characteristics for the unit level switch (ULS), both for the SB 3865 and AN/TTC-42, are similar to those of the TTC-39 switch. The ULS will be capable of operating as a master or slave for transmit timing. In the master mode timing is provided by an internal oscillator which can also be locked to an external source. In the slaved mode the internal oscillator is locked to timing derived from an incoming TDM group; a loss of incoming data results in automatic switchover to the master mode. Received timing is derived from each TDM group. Buffering is then applied to these incoming digital streams for synchronization to the local oscillator.

V. STATION TIMING

Two timing configurations will be described which correspond to two types of transmission nodes, designated major and minor nodes. The major node timing subsystem incorporates a highly accurate station clock with a clock distribution system. The minor node timing subsystem uses timing derived from the transmission equipments. For typical applications of the minor node, received timing derived from a radio would be used as a station master.

1. MAJOR NODE TIMING SUBSYSTEM

Figures 12 and 13 show the arrangement of the intrastation routing of timing lines to each transmission equipment for the major node. The distribution of clock lines for the transmit direction (Figure 12) requires synthesis of the transmission rates from the station clock, distribution to the radio and all levels of multiplexer, and phase adjustment within each transmission equipment to insure correct phasing of clock and data. Note that each transmission equipment, including the KG-81, accepts external clock and each provides phase adjustment on incoming timing lines. In the receive direction, as shown in Figure 13, received data are buffered in order to synchronize the incoming data with local timing. Two alternative locations are shown for these buffers: first, at a lower level with interface at the Level 2 multiplexer, Level 1 multiplexer or submultiplexer; and second, directly at the radio output at mission bit stream rates. In either case, data are clocked into the buffer by received timing derived in the radio or multiplexer, and clocked out by the local clock. Note that the requirement for the generation and distribution of clock rates by the timing subsystem can be minimized by using the timing generation and distribution capability inherent in most digital transmission equipments (e.g., DRAMA).

Buffering at the higher level requires two high speed buffers, one for each of two parallel MBS's, while buffering at the lower level requires a buffer at every interface between two independently timed signals, as shown in Figure 13. All interfaces shown are synchronous, although the interface between Level 1 and Level 2 multiplexers could be asynchronous, since pulse stuffing is available as an option in the DRAMA TD-1193. The use of pulse stuffing at any given interface does not appreciably alter the frequency accuracy of the transmitted or received signal. However, two deleterious effects occur: (1) the received 'destuffed' signal suffers from slewing jitter due to the imperfect smoothing action required in removing stuff bits, and (2) BCI can be lost at the receiver due to channel induced errors in stuff control words. Because of these effects, it is recommended that the synchronous option of the Level 1/2 interface be used wherever practical. For those cases where the Level 1 multiplexer directly interfaces

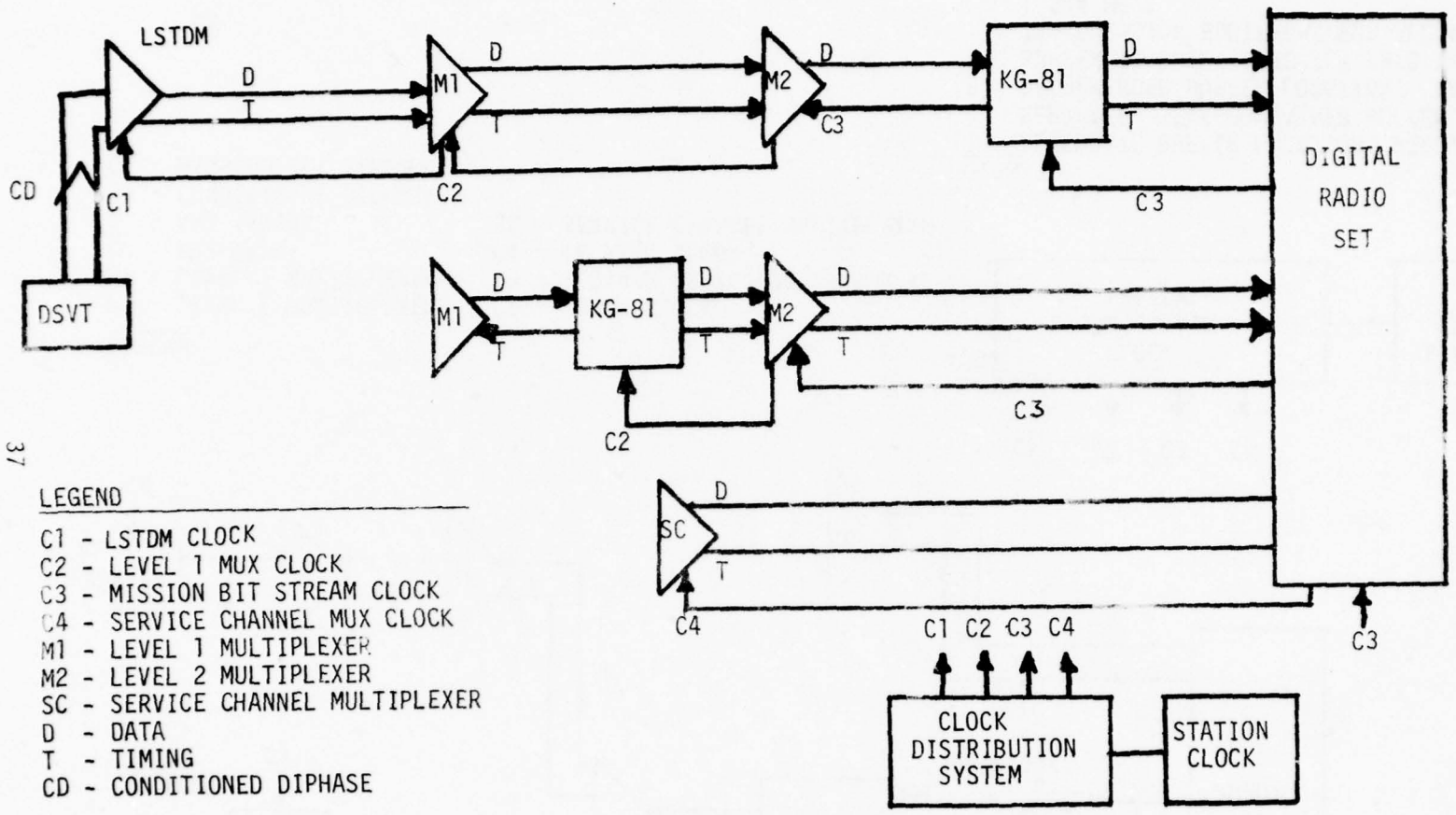
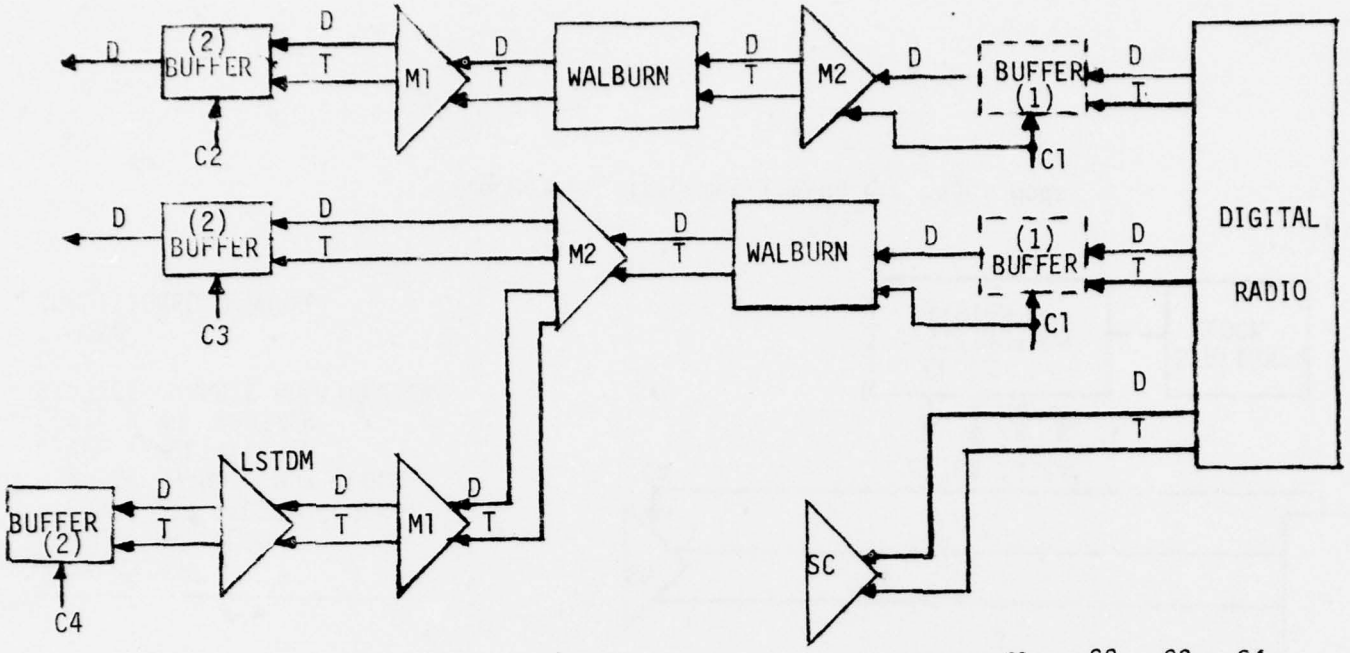
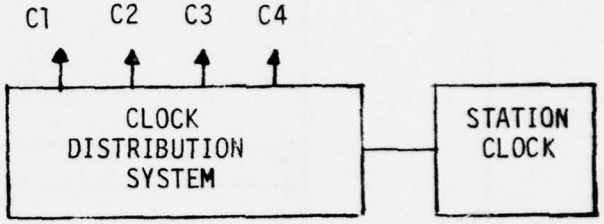


Figure 12. Transmit Timing For Major Node





LEGEND

M2 - LEVEL 2 MULTIPLEXER
M1 - LEVEL 1 MULTIPLEXER
D - NRZ DATA
T - NRZ TIMING
CD - CONDITIONED DIPHASE
C1 - MISSION BIT STREAM
C2 - LSTDM CLOCK
C3 - 1.544/3.088/6.176 MB/S RATE
C4 - 16 KB/S CLOCK
SC - SERVICE CHANNEL MULTIPLEXER

NOTES:

(1) ALTERNATE BUFFER LOCATION. REQUIRES SEPARATE, SELF-CONTAINED BUFFER.
(2) RECOMMENDED BUFFER LOCATION. EACH BUFFER IS BUILT DIRECTLY INTO THE TRANSMISSION EQUIPMENT FOR ALL RATES BEL 1.544 MB/S.

Figure 13. Receive Timing For DCS Major Node

with the Level 2 multiplexer, the synchronous option would always be used. However, when tandeming between two Level 2 multiplexers, a separate, self-contained buffer would be required to allow a synchronous interface, as shown in Figure 8(c). Because of the expected cost and added complexity of this separate buffer, the pulse stuffing interface could normally be used when tandeming between two Level 2 multiplexers. A synchronous interface, with separate buffer required should be used only in those cases (e.g., in a troposcatter channel) where a significant penalty may result from using pulse stuffing.

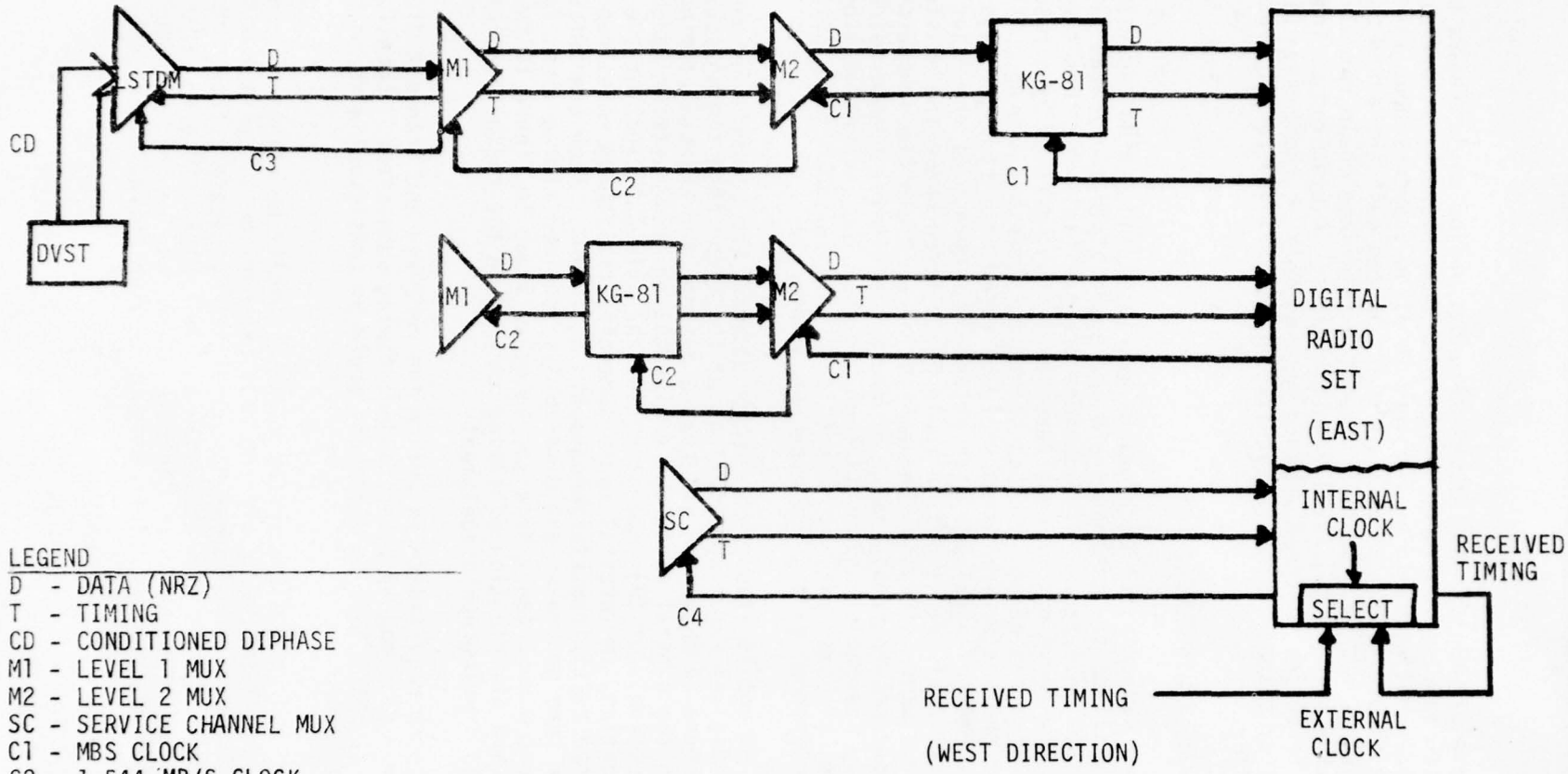
2. MINOR NODE TIMING SUBSYSTEM

The minor transmission node has no free-standing timing subsystem, but rather utilizes the timing generation and distribution capability inherent in transmission equipments. Two options are available for this timing subsystem. The first option uses received timing, derived by a master equipment (e.g., radio), as a clock source for transmit timing. Timing derived from the master equipment would be based on a timing subsystem located at a remote major node with attendent accuracy of the major node station clock. This first option would be utilized where the existence of synchronous users dictates the need for an accurate timing source. The second option uses internal timing of the highest level transmission equipment (usually the radio) as the station master. The internal timing source of the radio, with accuracy of 1 part in 10^6, is suitable for applications where no requirement exists for synchronous users.

Figures 14 and 15 illustrate station layouts for transmit and receive timing for digital radio applications of the minor node timing subsystem. Note that Figure 14 shows two selectable options for transmit timing: (1) slaving the digital radio to receive timing from a master radio (east or west direction), or (2) operating off the internal clock of the radio. For either option, the digital radio generates the timing rates required for the associated multiplexers/cryptographic equipment. Each transmission equipment in turn generates and distributes required timing lines for the next equipment downstream. Receive timing as shown in Figure 15 is the straightforward distribution of timing derived in the radio to associated multiplex and cryptographic equipment.

Buffering is required to interface the received and transmit direction since the two are timed from independent timing subsystems. Location of buffers is not specified but placement would be consistent with that shown for the major node.

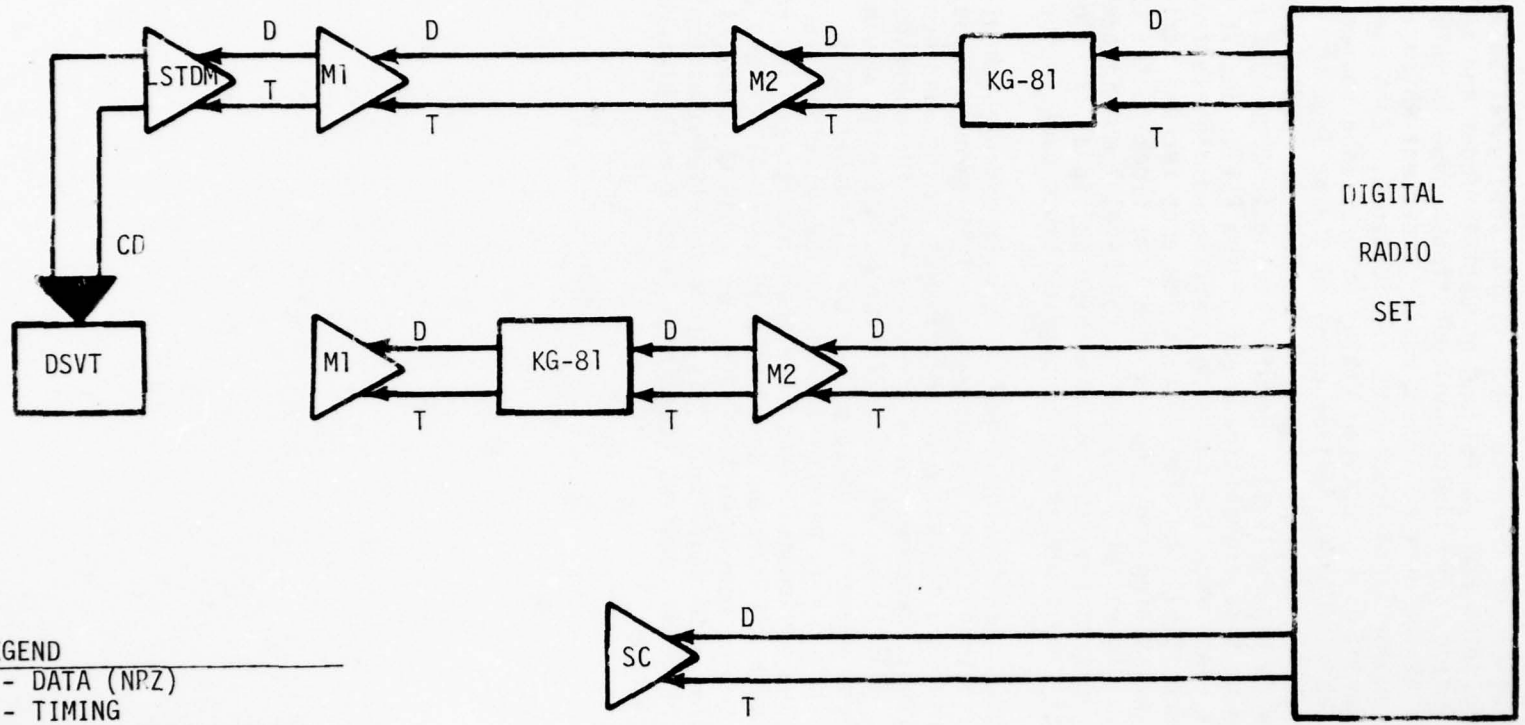
The minor node timing subsystem would typically be either a terminating site at the end of some spur off the main backbone or a repeater with no VF breakout. This type of node has no capability to generate transmission rates other than those inherent in the radio and multiplex, since no separate timing subsystem would exist to generate other required rates. Additionally, this option presupposes no requirement to provide timing to any other equipments (e.g., DAX).



LEGEND

D - DATA (NRZ)
T - TIMING
CD - CONDITIONED DIPHASE
M1 - LEVEL 1 MUX
M2 - LEVEL 2 MUX
SC - SERVICE CHANNEL MUX
C1 - MBS CLOCK
C2 - 1.544 MB/S CLOCK
C3 - LSTDM CLOCK
C4 - SERVICE CHANNEL MUX

Figure 14. Transmit Timing For Minor Node



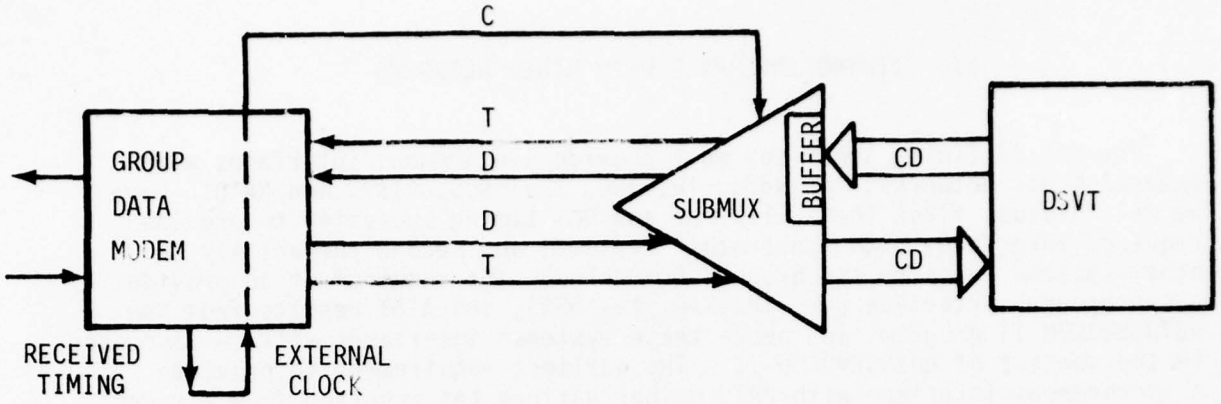
LEGEND

D - DATA (NRZ)
T - TIMING
CD- CONDITIONED DIPHASE
M1- LEVEL 1 MUX
M2- LEVEL 2 MUX
SC- SERVICE CHANNEL MUX

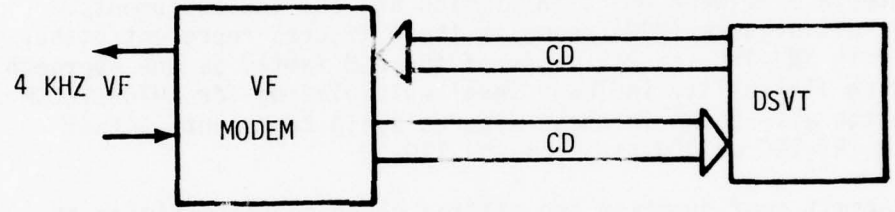
FIGURE 15. RECEIVE TIMING FOR MINOR NODE

Other applications of the minor node timing configuration are shown in Figure 16, including FDM channel and group interfaces and first level multiplexer interface. The timing configurations shown in this figure utilize received timing derived from a master equipment which is the recommended option for synchronous user applications. Each such interface provides loop timing; i.e., received timing is used as a source for transmit timing. The 16 kb/s VF modem derives received timing from the VF signal and passes the received digital signal to the DSVT in conditioned diphase format, as shown in Figure 16(a). Receive timing is then derived by the DSVT and is used to time transmit data out of the DSVT. The VF modem then derives transmit clock from the incoming conditioned diphase transmit signal. As shown in Figure 16(b), the Group Data Modem uses receive timing as a source for transmit timing and supplies this same clock to the LSTDM for transmit timing. Figure 16(c) shows that the Level 1 multiplexer uses receive timing, derived from the incoming bipolar signal, to clock transmit data in the Level 1 multiplexer and to provide clock back to the LSTDM.

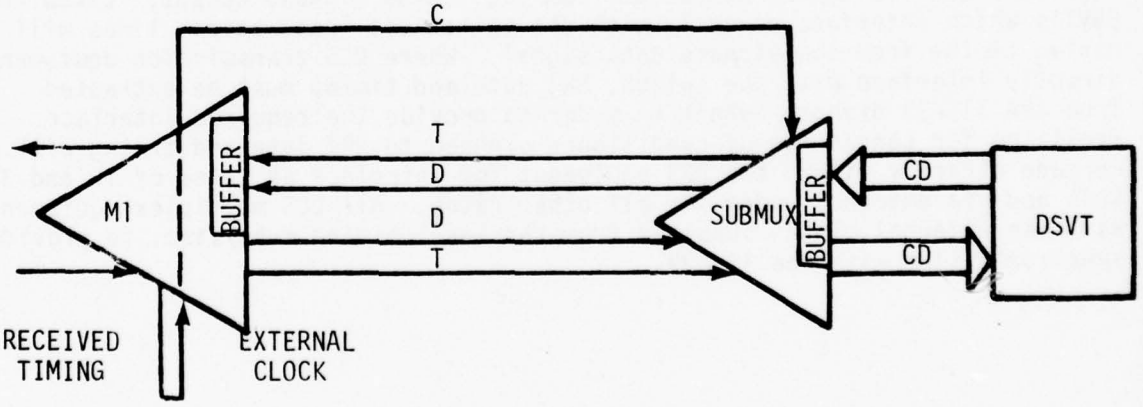
Finally, certain repeater configurations will arise which will require special timing considerations. A two-way straight-through repeater is timed by using received timing to clock transmit timing, and hence requires no special handling. However, for a three-way repeater where each received MBS is routed to a different radio, buffering at MBS rates would be required to allow one MBS to act as a timing master for all other MBS's. However, such a buffer is not included as part of the timing subsystem nor is it contained in any transmission equipment. Thus, for these relatively few repeater configurations, each MBS must be demultiplexed by TD-1193's and either (1) interfaced synchronously with a buffer at 1.544 Mb/s or (2) interfaced asynchronously via pulse stuffing. This approach eliminates the need for high speed buffering but requires additional Level 2 multiplexers at these special repeater sites.



(b) GROUP DATA MODEM TIMING



(a) VF MODEM TIMING



(c) LEVEL 1 MULTIPLEXER TIMING

FIGURE 16. LOOP TIMING USED WITH MINOR NODE

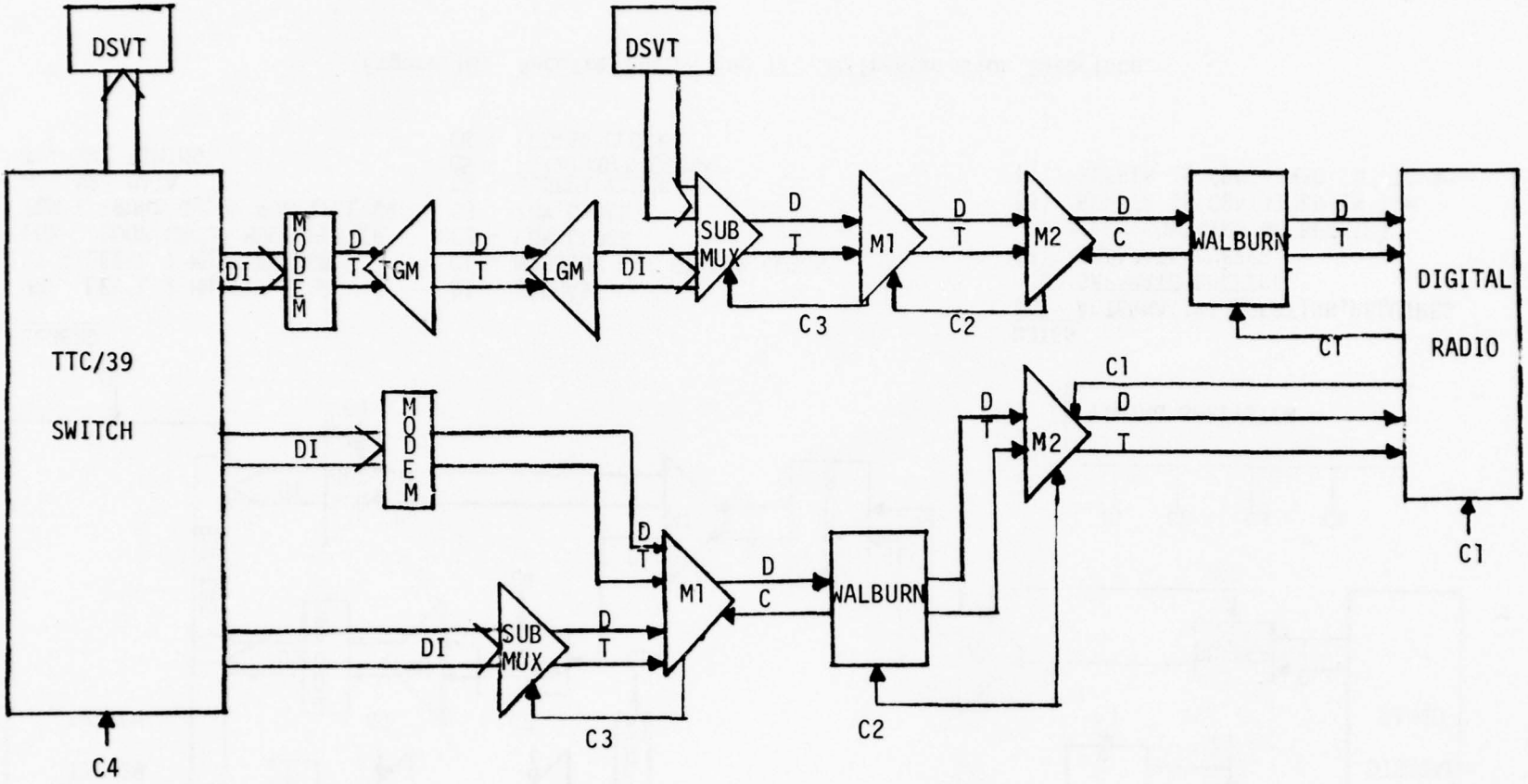
VI. TIMING INTERFACE WITH OTHER NETWORKS

The DCS II Timing Subsystem must provide synchronous interfaces with several other networks, including TRI-TAC, the DSCS, AT&T, and NATO. Here we will discuss first the ability of the DCS timing subsystem to provide required interfaces with these other systems, and second the ability of other systems to carry synchronous DCS rates. The requirement to provide a synchronous interface with TRI-TAC, the DSCS, and AT&T results from the AUTOSEVOCOM II program, and hence these systems' interfaces will be discussed in the context of AUTOSEVOCOM II. The earliest requirement to provide a synchronous interface with NATO member nations has resulted from a recent draft standardization agreement which describes digital transmission interconnection [17].

1. TRI-TAC

Figures 17 and 18 present the transmit and receive configurations of the timing interface between DCS transmission and TRI-TAC equipments. Digital Group Multiplexers (DGM) shown in these figures represent either an interface with TRI-TAC, or DCS usage of the DGM family as one approach toward providing flexibility in lower level multiplexing for AUTOSEVOCOM II. The TTC-39 switch also shown in these figures again represents actual interface with TRI-TAC or DCS usage of the TTC-39.

In the transmit configuration the station clock supplies timing to the TTC-39 switch and to each transmitting DCS transmission equipment. The TTC-39 switch will accept station clock at a standard frequency and will derive required clock rates internally. The Trunk Group Multiplexer (TGM) and Loop Group Multiplexer (LGM), both from the DGM family, utilize NRZ timing and data on their combined outputs and therefore require an external modem to interface with the conditioned diphase format of the TTC-39. The demultiplexer sides of the LGM and TGM are then slaved to the station clock via timing extracted from the TTC-39 diphase output. Likewise, DSVT's which interface directly with the switch via local access lines will derive timing from the diphase data signal. Where DCS transmission equipments directly interface with the switch, NRZ data and timing must be extracted from the TTC-39 diphase output in order to provide the required interface. Provision for conversion of conditioned diphase to NRZ data and timing will be made directly within the DCS equipment for interface at rates of 16 and 32 kb/s and via external modem for all other rates. All DCS multiplex equipments will use external clock, supplied from the local timing subsystem, to provide synchronization with the TTC-39.



LEGEND

M2 - LEVEL 2 MULTIPLEXER
M1 - LEVEL 1 MULTIPLEXER
LGM - LOOP GROUP MULTIPLEXER
TGM - TRUNK GROUP MULTIPLEXER
D - NRZ DATA
T - NRZ TIMING

D1 - DIPHASE
C1 - MISSION BIT STREAM CLOCK
C2 - 1.544 Mb/s CLOCK
C3 - SUBMUX CLOCK
C4 - TTC/39 CLOCK

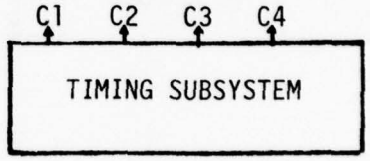
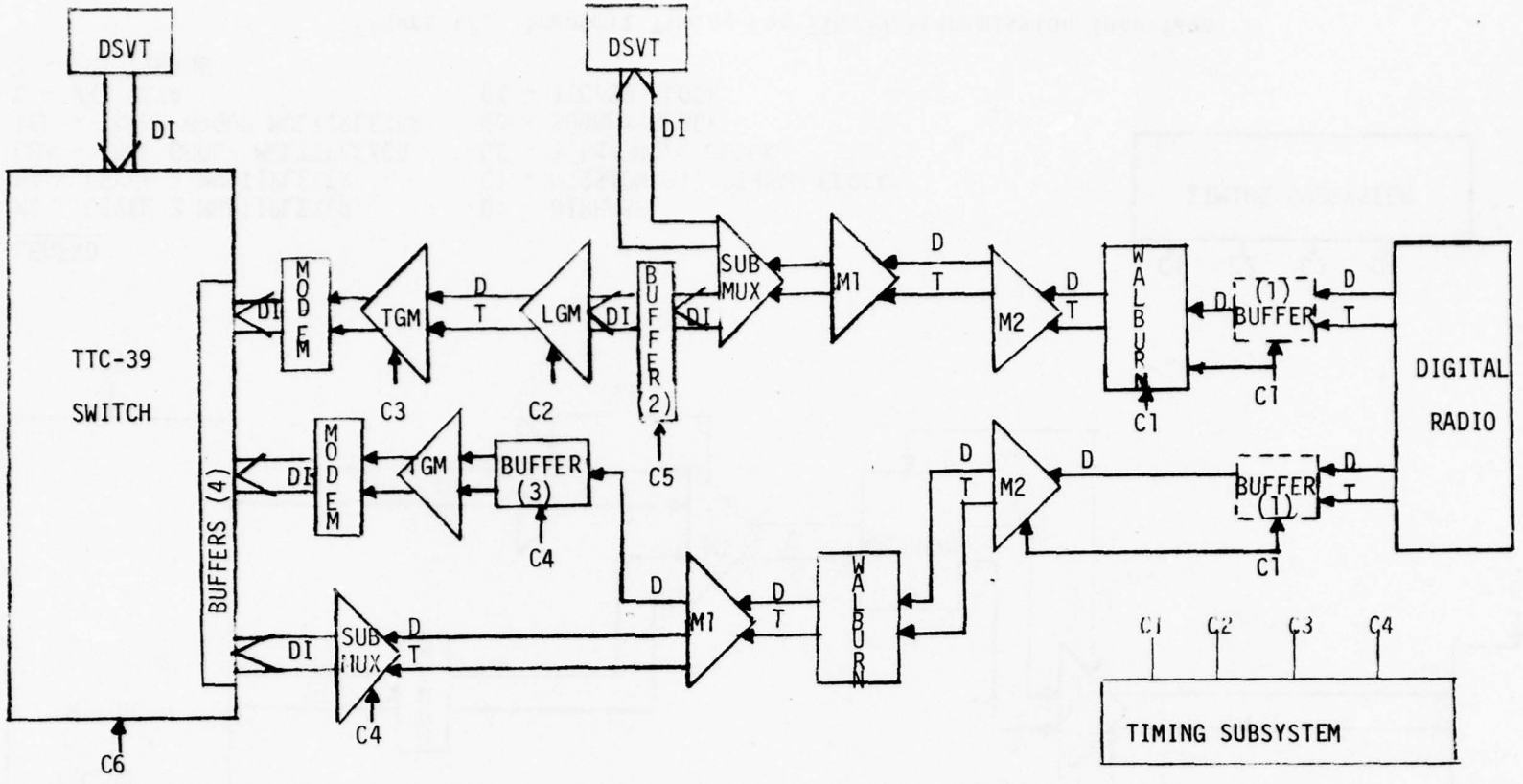


Figure 17. Transmit Timing For TTC-39/Transmission Interface



LEGEND

M2 - LEVEL 2 MULTIPLEXER
M1 - LEVEL 1 MULTIPLEXER
LGM - LOOP GROUP MULTIPLEXER
TGM - TRUNK GROUP MULTIPLEXER
D - NRZ DATA
T - NRZ TIMING

DI - DIPHASE
C1 - MISSION BIT STREAM CLOCK
C2 - LGM CLOCK
C3 - TGM CLOCK
C4 - SUBMUX CLOCK
C5 - 16/32 KB/S CLOCK
C6 - TTC-39 CLOCK

NOTES
(1) ALTERNATIVE LOCATION;REQUIRES SEPARATE BUFFERS
(2) SEPARATE BUFFER (LGM CONTAINS NO BUFFER)
(3) BUFFER IS CONTAINED IN TGM
(4) BUFFER IS CONTAINED IN TTC-39

Figure 18. Receive Timing For TTC-39/Transmission Interface

The receive configuration of Figure 18 shows the local station timing subsystem used to clock out received data from buffers located at (1) synchronous channel outputs of lower level multiplexers, or (2) at the radio mission bit stream output. Both data and timing are transferred downstream in the multiplex hierarchy to the lowest level multiplexer (Level 1 or submux) where interface occurs with DGM equipment or the TTC-39. For direct interface between DCS lower level multiplexers and the switch, provision for conditioned diphase format will be made directly within the transmission equipment for interface at 16 and 32 kb/s and via external modem for all other rates. TGM and LGM equipments will accept station timing at their group rates and require an external modem to interface with the switch in a conditioned diphase format.

Buffering at the lower level is provided according to where the receive-to-transmit interface occurs, as can be seen in Figure 18. This buffering is done internal to the multiplexer or by means of an external, separate buffer, depending on the application. The LGM has no built-in buffer capability on its channel side and therefore a separate buffer is required when interfacing with an LGM channel, as shown in Figure 18. The TGM, however, does include a 256-bit buffer, which allows direct interface on the channel side. Buffering is also provided in the TTC-39 for all incoming trunk groups to allow synchronization with the local clock. Each TTC-39 buffer has at least 256 bits allocated to compensating for frequency differences between transmit and receive clocks. As noted in earlier equipment descriptions, buffering required with any lower level DCS multiplexer (e.g., DRAMA) is done directly within the multiplexer.

2. DSCS

The timing interface between a DSCS tech control facility (TCF) and a DCS transmission node is shown in Figures 19 and 20. These figures show both GSC-24 and FCC-98 satellite transmission equipments interfacing with DCS transmission equipment on a low speed channel basis. Although these interfaces are typical, low speed channels (e.g., 16 kb/s) can also directly interface with the AN/USC-28 spread-spectrum modem, the MD-921 or MD-1002 PSK modem, or the MD-920 ICF modem. The following discussion of DSCS timing characteristics applies to any of the above listed interfaces.

Figure 19 is a block diagram of a satellite down link with buffers placed at the lowest channel level provided by DSCS associated multiplexers or modems. Here the satellite delay buffer, as described in chapter IV, is used to remove the satellite doppler and provide synchronization with the local clock of the transmission node. Since the maximum requirement is 128 kb/s for synchronous data transmission via satellite, this buffer is provided with sufficient length to meet MTTS requirements up to 128 kb/s. Each buffer would have data clocked in by DSCS demultiplexer or modem timing and clocked out by the local timing subsystem within the transmission node. The buffer is located within and is considered part of the DCS transmission node.

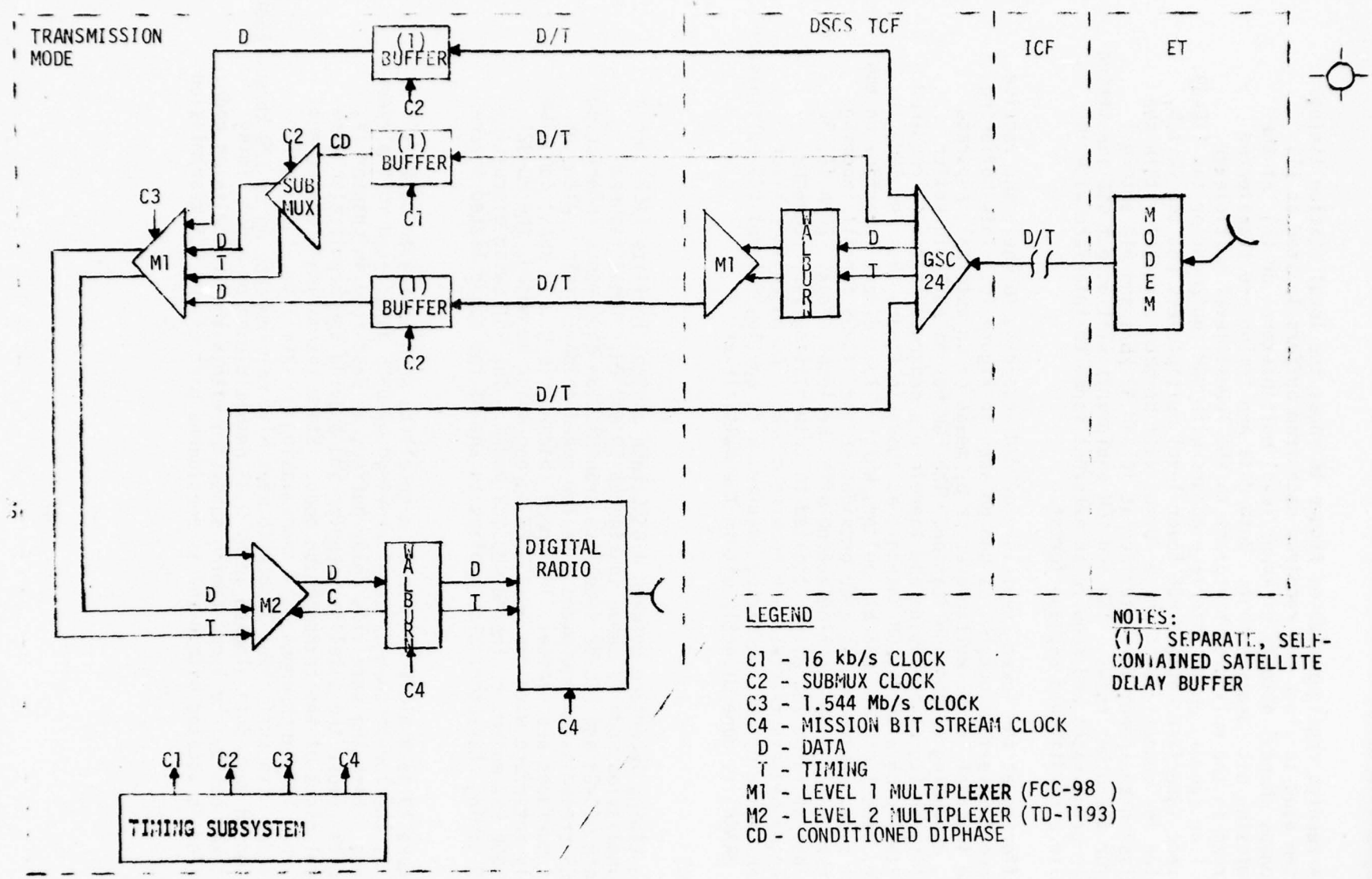


Figure 19. DSCS/Transmission Node Timing Interface For The Satellite Down Link

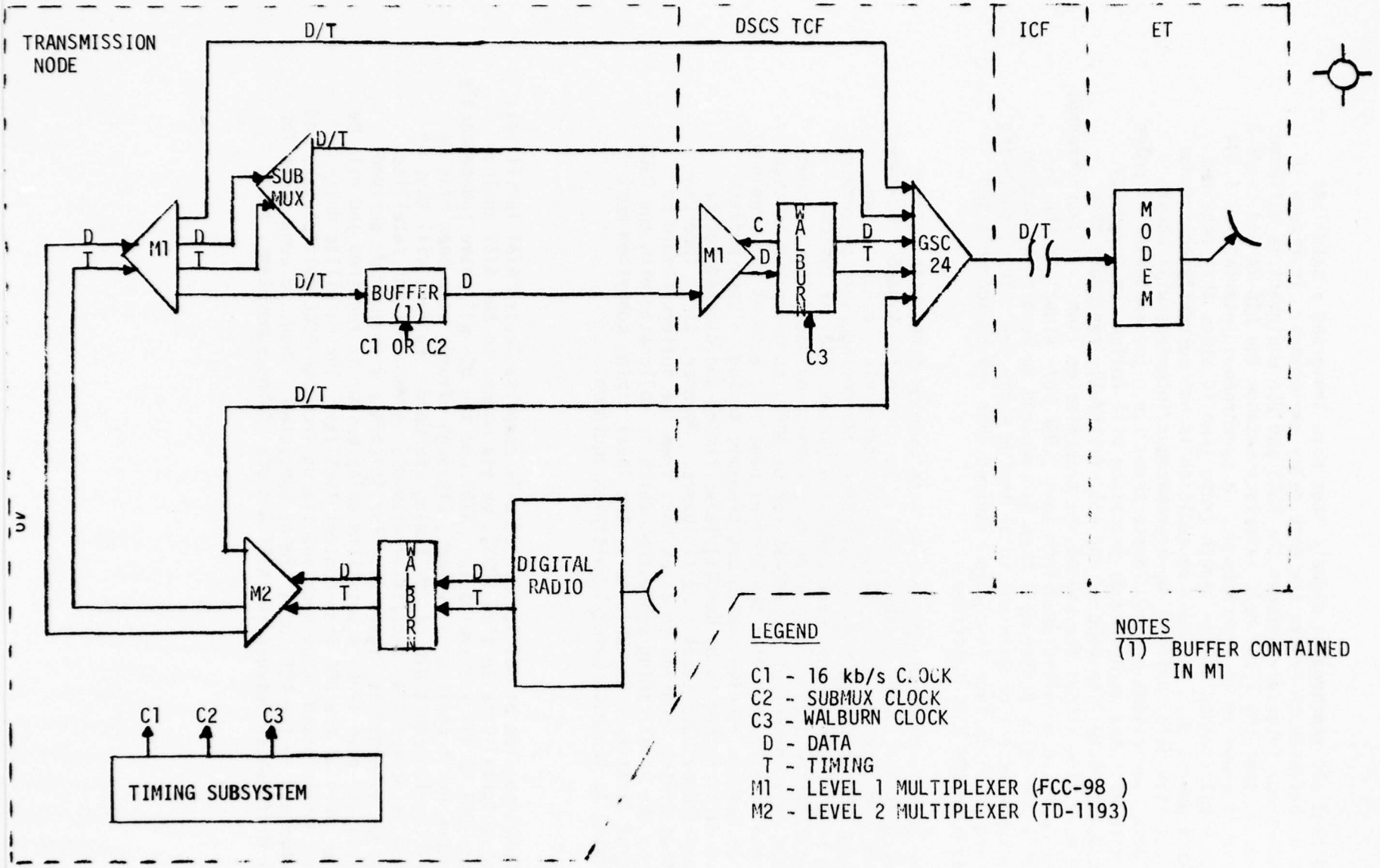


Figure 20. DSCS/Transmission Node Timing Interface for the Satellite Up Link

Noted that all synchronous signals that have traversed a satellite link must be buffered to remove the path delay variations. In Figure 19 every synchronous interface between the DSCS and DCS equipment is buffered. Note, however, that the 1.544 Mb/s interface between the GSC-24 and Level 2 multiplexer is shown to be asynchronous. A synchronous interface at 1.544 Mb/s would require added buffer length (more than 10 times that required for 128 kb/s operation), and such an addition is not currently envisioned for the satellite delay buffer. An asynchronous interface will absorb the path delay variations but not remove them; i.e., the mechanism of pulse stuffing used with the asynchronous interface will follow the frequency variation due to satellite doppler and will faithfully reproduce this frequency variation at the far end of the transmission link. If a synchronous subchannel is to be demultiplexed from this 1.544 Mb/s signal at the far end, a satellite delay buffer will then be required to remove the doppler and allow synchronization with the local timing subsystem. Thus, buffering of a synchronous interface is always required, but may be accomplished downstream from the DSCS interface.

Figure 20 is a block diagram of the satellite up link, with buffers again placed at the lowest channel level. As currently planned, low-speed data channels within the DSCS will be accommodated via the GSC-24, an asynchronous TDM which requires no buffering. Buffering would be required only if a synchronous channel were used in a DSCS FCC-98 (or CY-104). If such an application arises, buffering is already provided as part of each synchronous data channel of the FCC-98 (or CY-104), as described in chapter IV. For the satellite up link the buffers need only account for frequency differences between receive timing and transmit timing. These buffers would have data clocked in by demultiplexer timing and clocked out by timing supplied by DSCS Level 1 multiplexers. However, it is important to note that timing required to clock data from the buffers should be supplied by the local timing subsystem, which is collocated with the DSCS tech control facility. For this case, the local timing subsystem must supply timing to the DSCS Level 1 multiplex equipment.

3. AT&T

The CONUS portion of AUTOSEVOCOM II will comprise leased AT&T facilities, through the Digital Data Service (DDS), or via modems in the AT&T analog plant where DDS is not yet available. AT&T and the DCS will have independently timed synchronous transmission systems, although efforts have been made to force AT&T to also adopt UTC as its timing standard. Buffers will thus be required to interface AT&T facilities with DCS terrestrial and satellite transmission, as shown in Figure 21. For interface with channels derived from a satellite down link, a satellite delay buffer is required and will be provided as part of the DCS tech control facility. The satellite delay buffer has data clocked in by received timing from the DSCS multiplexers and data clocked out by the DCS local timing subsystem. Then, to compensate for frequency differences between the AT&T and DCS timing subsystems, each

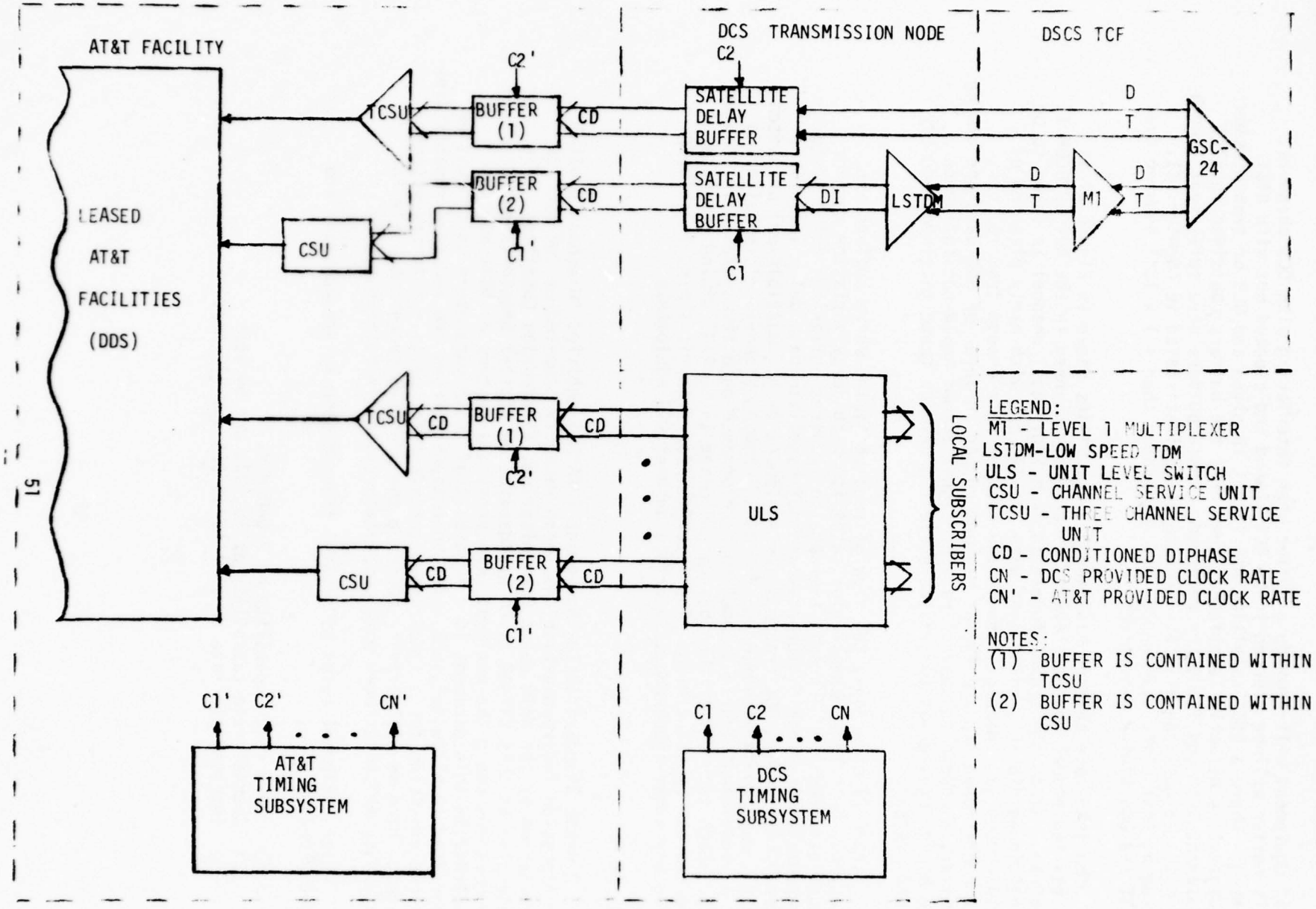


Figure 21. Timing Interface Between DCS and Leased AT&T Facilities

AT&T equipment will provide a buffer when interfacing with DCS channels. This buffer will be clocked in by DCS timing and clocked out with AT&T timing. Where a DSCS satellite hop is not involved and ULS or transmission equipment is directly interfaced, then only the buffers contained in AT&T equipment (CSU and TCSU) are required. These buffers have sufficient length (4 bits) to meet the MTTS performance objectives stated in chapter III, assuming that clock differences are no greater than $\pm$ 1 x 10^{-9} between the AT&T and DCS timing subsystems.

The interface between AT&T and DCS facilities shown in Figure 21 is at the individual channel level, as currently planned in the AUTOSEVOCOM II program. Also, the signal format on each individual channel is shown to be conditioned diphase, consistent with TRI-TAC and with early planning of AUTOSEVOCOM II. However, should the channel rate change from 16 kb/s, the conditioned diphase format may be dropped in favor of NRZ data and timing. However, a change in channel rate or signal format would not influence the basic requirement to provide buffering between these two independently timed systems.

Figure 21 shows only the flow of receive timing where buffers are required, both to compensate for satellite path delay variation and for clock differences. Transmit timing also requires buffering, but only to compensate for clock differences and not satellite path delay variations. Specifically, each DCS transmission equipment (e.g., multiplexer) or switch (e.g., ULS) contains buffering for each incoming channel. This buffering is of sufficient length to meet the performance objectives stated in chapter III. Each such buffer then has data clocked in by AT&T timing and data clocked out by DCS timing. The interface for transmit timing thus looks like any other synchronous interface between DCS equipments.

4. NATO

A draft Standardization Agreement (STANAG) entitled "Wideband Digital Transmission Interconnection" has been recently prepared by the U.S. on invitation by the NATO Joint Communications-Electronics Committee. The objective of this STANAG is to standardize on digital transmission interconnections among the national communications systems of NATO members. Included in this document is a treatment of those parameters which must be specified to allow for such interconnections. Among the required capabilities is the provision for a synchronous interface for certain interconnecting rates. Here we will briefly describe the proposed synchronous timing interface which has been more completely stated in reference [17].

Three different rates of digital transmission interconnection are considered:

(1) Group rate capability at 2.048 Mb/s
(2) Channel rate capability at 16, 32, and 64 kb/s
(3) Intermediate rate capability at 256 and 512 kb/s.

The group rate capability is specified to have an asynchronous interface, since (1) both the 1.544 Mb/s and 2.048 Mb/s second level multiplexers recommended by the CCITT are specified to be asynchronous, and (2) a synchronous interface would impose a requirement for synchronization among the networks of all member nations. Both channel and intermediate rate capabilities are specified to have synchronous interfaces, meaning that the data source must accept bit timing from the carrier system.

In specifying characteristics of the synchronous interface, no specific synchronization requirements were imposed, but rather design goals were stated which were to be subject to negotiation between participating nations for specific synchronous interface needs. The synchronous interface in general is based on the use of a station clock in conjunction with buffering to provide some objective MTTS. The station clock accuracy has a stated design goal of 1×10^{-9} and a worst case allowance of 1×10^{-7}. Also as a design goal, the mean time between loss of bit count integrity at any rate is stated to be at least 24 hours.

It is immediately obvious that clocks internal to DCS transmission equipments will not meet the stated design goal of 1×10^{-9} accuracy of the station clock and therefore would also not meet the BCI requirement. However, the station clock specified as part of the DCS timing subsystem will most certainly meet the STANAG design goal on clock accuracy. Also, with the buffers now located in DCS transmission equipments and using the station clock specified in the DCS timing subsystem, the BCI design goal would be easily met. It is further anticipated that the DCS timing subsystem would meet any additional timing requirements imposed by a NATO nation.

VII. PLANS AND PROGRAMS

Plans for implementation of a DCS II timing subsystem and for research and development toward a future timing subsystem are described below.

1. IMPLEMENTATION

a. AUTOSEVOCOM II. Plans for implementing a DCS II timing subsystem will be included in a future Five Year Plan (FYP) under AUTOSEVOCOM II Transmission. This FYP input will provide the necessary timing subsystem components to satisfy the AUTOSEVOCOM II requirement for synchronous operation. This implementation plan will be based on engineering guidance documented in this technical report. Potential changes in the choice of voice coding rate (16 kb/s vs. 8/32 kb/s) for AUTOSEVOCOM II will not change the requirements on the timing subsystem, but will of course, delay the implementation.

In support of the AUTOSEVOCOM II Program, several timing subsystem equipments will be procured and implemented, including the AN/GSQ-183 Frequency Control Set, clock distribution system, and satellite delay buffer. The GSQ-183 has previously been procured by DCA through an NSA contract and also by the Army, both procurements made in support of AUTODIN and Channel Packing. A reprocurement of the GSQ-183 is required, although there is no need to procure the additional frequency generation and distribution equipment, as was done for AUTODIN and Channel Packing. The configuration of the GSQ-183 as required for AUTOSEVOCOM II is described in Appendix B. Performance specifications have been developed for the clock distribution system and satellite delay buffer, as shown in Appendix C, and reference [13]. Procurement specifications for these two equipments are now being developed by the Army (USACEEIA) in support of AUTOSEVOCOM II Transmission requirements.

Prior to the fielding of a timing subsystem, a system integration test will be conducted to verify performance characteristics with various transmission configurations. Among those characteristics are: (1) the minor node configuration using loop timing in the radio, (2) reliability and stability of the AN/GSQ-183, (3) effect of troposcatter and satellite delay variation on buffer performance, and (4) stability of system after buffer reset(s). It is expected that tests of items (1), (2), and (4) can be accomplished in conjunction with AUTOSEVOCOM II system tests at USACEEIA, Ft. Huachuca; a test of item (3) will require the services of RADC, Griffiss AFB, or SATCOMA/ECOM, Ft. Monmouth.

b. Future Timing Subsystem. Provision for the future timing subsystem has also been included in the FYP 80. A two-phase implementation is proposed: Phase I provides test and evaluation within a representative subnet, and Phase II applies the future timing subsystem to the Worldwide DCS. The number, location, and cost of required equipments have been identified for Phase I; this same equipment information for Phase II is to be specified in a latter FYP.

This FYP project will provide for the upgrading of the AUTOSEVOCOM II timing subsystem, which is based on LORAN C, to a future timing subsystem which will not necessarily depend on external timing sources (e.g., LORAN). This upgrading will replace or augment LORAN C with a synchronization system based on additional processing capability (master/slave, mutual synchronization, or time reference distribution).

2. RESEARCH AND DEVELOPMENT

a. DCA Program. A DCA sponsored R&D study with Harris Corporation is currently developing information useful in the selection, definition, and implementation of the timing subsystem for the future digital DCS. The first phase of this study has been completed and a report has been published [18]. Four timing and synchronization approaches are now under investigation: master/slave, independent clocks, time reference distribution, and mutual synchronization. The prime baseline of this study is the utilization of the TRI-TAC timing approach and equipment to provide the functions required by the DCS, while an alternative baseline considers modifications and additions to the TRI-TAC equipment. Results from this program will be integrated into the Air Force program to aid in the selection, definition, and development of a future timing subsystem.

b. Air Force Program. A long-term RADC program to select and develop timing and synchronization techniques for the future DCS is ongoing. Experimental models of the future timing subsystem are to be evaluated, and the DCS II timing subsystem will be evaluated for its use as a fallback system. Test and evaluation of these models will be accomplished in a meshed communications network composed of RADC troposcatter, LOS, and satellite transmission facilities. Each experimental model will generate and distribute various required frequencies and will also provide buffering at some multiplex hierarchical level to be determined by performance and cost evaluation. Each model will include processing capability to accomplish required control and computation functions. Time reference distribution and master/slave techniques will be implemented. Also, the AN/GSQ-183 will be studied and evaluated for its use as a backup to the future timing subsystems.

A second RADC program, currently under contract with CNR, Inc., is investigating the effects of channel and equipment parameters on the ability to coordinate clocks placed at geographically separate nodes. This study has analysized and conducted tests on troposcatter and line-of-sight channel and equipment effects. Relationships have been developed between link and equipment parameters and network clock synchronization parameters. Results to date indicate that a lack of channel reciprocity, due to different carrier frequencies, different space diversity configurations, and different equipment delay characteristics between two nodes, must be accounted for when synchronizing clocks via time transfer [19].

Results from the RADC programs will provide input to the planning and procurement of equipment for implementation of the future timing subsystem as called out in the FYP 80.

REFERENCES

[1] D.R. Smith and J.L. Osterholz, "The Effects of Digital Tropo Error Statistics on Asynchronous Digital System Design", 1975 National Telecommunications Conference, December 1975.

[2] DCEC TR 12-76, "DCS Digital Transmission System Performance", November 1976.

[3] Various RADC and Martin Marietta Tests of GSC-24 with CV-3034, USC-26, and CY-104; 1973-1975.

[4] "Analysis of Jitter Characteristics in a Pulse Stuffing TDM Network", Final Report of DCA Contract 100-76-C-0076, June 1977.

[5] "Reliability and Maintainability Report for the CDS-1 Clock Distribution System", Versitron, Inc., March 1976.

[6] F.T. Chan, et. al., "Timing Synchronization of the DATRAN Digital Data Network", 1975 National Telecommunications Conference, December 1975.

[7] DCEC TR 3-74, "Digital Transmission System Design", March 1974.

[8] M.C. Thompson, Jr. and H. B. Jones, NBS Technical Note No. 219, "Radio Path Length Stability of Ground-to-Ground Microwave Links", November 1964.

[9] RADC TR 72-350, "Digital Troposcatter Experiments", January 1973.

[10] DCEC R400 Contracted Study, "Design of Buffers for Satellite and Terrestrial Communications", September 1976.

[11] L. Dennis Shapiro, "Time Synchronization from LORAN C", IEEE Spectrum, August 1968.

[12] R.H. Doherty, et. al., "Timing Potentials of LORAN C", Proc. IRE, November 1961.

[13] DCEC Specification R220-77-5, "Performance Specification, Satellite Delay Buffer", July 1977.

[14] USACEEIA Specification No. CCC-74047, "Specification for Multiplexer/ Demultiplexer TD-1192", 20 August 1975.

[15] USACEEIA Specification No. CCC-74048, "Specification for Multiplexer/ Demultiplexer TD-1193", 16 July 1976.

[16] USACEEIA Specification No. CCC-74049, "Specification for Radio Set AN/FRC-163( )", 16 July 1976.

[17] NATO Draft STANAG 5043, "Wideband Digital Transmission Interconnection", 13 April 1976.

[18] Study of Alternate Techniques for Communication Network Timing/ Synchronization, Final Report, 23 March 1977.

[19] Peter Alexander and J.W. Graham, "Time Transfer Experiments for DCS Digital Network Timing and Synchronization", Eighth Annual Precise Time and Time Interval (PTTI) Applications and Planning Meeting, December 1976.

LIST OF DEFINITIONS

Asynchronous - A signal is asynchronous if between any two significant instants in the same block or character there is always an integral number of unit intervals. Between two significant instants located in different blocks of characters, there is not always an integral number of unit intervals.

Asynchronous Network - A network in which the clocks of interconnected stations need not be synchronous or plesiochronous.

Bit Count Integrity - Given two enumerable bits in a transmitted bit stream that are separated by n bits, bit count integrity is maintained when the same two bits are separated by n bit intervals in the received bit stream.

Buffer - A buffer is a device which automatically synchronizes incoming data to a local clock. Synchronization is provided by elastic storage which compensates for inaccuracy and drift between a remote and local clock. The buffer has data clocked in (or written) by the remote clock and has data clocked out (or read) by the local clock. If the frequency of the remote clock is greater than the frequency of the local clock, the buffer will eventually fill and a data bit will be skipped (buffer overflow). If the frequency of the remote clock is less than the frequency of the local clock, the buffer will eventually deplete and a data bit will be read twice (buffer underflow). For either buffer overflow or underflow, a buffer typically resets to mid-position.

DCS Channel Packing Subsystem - This subsystem consists of thirteen high speed data circuits, eight trans-Pacific and five trans-Atlantic, and leased terminal equipment designed to combine existing parallel routed traffic. A channel packing trunk system consists of a high speed (9600 bps) trunk which combines low speed (1200 or 2400 bps) multiplexer trunks and 2400 bps tail circuits. A high speed trunk terminal contains a 9600 bps modem and a high speed time division multiplexer. On a low speed trunk, synchronous, asynchronous and isochronous subscribers are combined in 15 or 30 channel groups by a low speed time division multiplexer which interfaces with a 1200 or 2400 bps input port in the high speed time division multiplexer.

DCS II - The DCS II denotes a future configuration of the DCS which will include a predominantly digital transmission plant and second generation networks such as AUTOSEVOCOM II and AUTODIN II. The time frame for implementation of the various programs associated with the DCS II is approximately 1980 to 1990. Total implementation of the DCS II architecture is not expected before 1990.

Digital Radio and Multiplex Acquisition (DRAMA) - The DRAMA family of digital transmission equipments consists of (1) the FCC-98 Level 1 multiplexer which provides up to 24 data and/or voice channels and operates at a combined rate of 1.544 Mb/s; (2) the TD-1193 Level 2 multiplexer which provides up to 8

synchronous or asynchronous data channels at rates of 1.544, 3.088, or 6.176 Mb/s and operates at combined rates of 3.232, 6.464, 9.696, and 12.928 Mb/s; and (3) the FRC-( )( ) digital radio which transmits/receives synchronous data at selected rates up to 26 Mb/s, provides a choice 1 bps/Hz or 2 bps/Hz spectral efficiency, and operates in the 4 and 8 GHz bands.

Frame Synchronization - Frame synchronization provides a means for a time dividion demultiplexer to correctly recognize incoming data bits and distribute each data bit to its proper channel. Framing bits are added to a transmitted bit stream to indicate the beginning or end of a predetermined group (or frame) of bits. The demultiplexer then uses these framing bits to acquire and maintain synchronization.

Frankfurt-Koenigstuhl-Vaihingen (FKV)-Transmission System Upgrade Project - The FKV project has provided the initial introduction of PCM/TDM capability into the DCS. Equipments used in this project were the CY-104 bulk encrypted PCM channel bank, the T1WB1 asynchronous data multiplexer, the FCC-97 pulse stuffing, second level multiplexer, and the DCS Standard FM Radio. Links within this project provide up to 192 VF channels in a 12.6 Mbps transmitted bit stream.

Isochronous - A signal is isochronous if the time interval separating any two baud sampling instants is theoretically equal to the unit interval or to a multiple of the unit interval. (Note: In practice, variations in the time intervals are constrained with specified limits.)

Jitter - Short term variations of the baud sampling instants of a digital signal from their intended positions in time.

Plesiochronous - Two signals are plesiochronous if their corresponding significant instants occur at nominally the same rate, any variations being constrained within a specified limit.

Pulse Stuffing - A technique used in time division multiplexing to combine independently timed isochronous input signals. Each input is converted to a rate which is then synchronous with the TDM internal clock. This rate conversion is accomplished by writing the data input into a buffer using the source clock, reading the contents of the buffer out using the TDM clock, and monitoring the buffer fill in order to add dummy (stuff) bits periodically to account for differences between source and TDM clock. Each stuff bit location must be coded by the transmit TDM such that the receive TDM can correctly locate and remove the stuff bits. Transmission errors can cause errors in the locating of stuff bits which will cause subsequent loss of BCI in the data sink. For this reason each stuff bit location is signalled with an n bit code word (n = 3, 5, 7, 9,...), where typically an all 1's pattern would indicate a stuff bit and an all 0's pattern would indicate a data bit. Majority logic is applied to each stuff bit location at the receiver to identify actual stuff bits. A smoothing loop then is used to compensate for removal of stuff bits and provide an averaged clock frequency.

Pulse Stuffing Jitter - A pulse stuffing demultiplexer generates a jitter component during reconstruction of the original isochronous data stream. This jitter results from the insertion or deletion of bits as part of the destuffing process. The unfiltered clock is then input to a smoothing loop to filter out pulse stuffing jitter. However, this loop will not completely remove the jitter. The residual jitter found on the isochronous data stream is known as pulse stuffing jitter and, if not properly controlled, can cause loss of synchronization in the bit synchronizer of the asynchronous data sink.

Reference Circuit - A hypothetical circuit broken down into discrete segments used in designing transmission circuits and systems.

Synchronous - A signal is synchronous, if between any two significant instants in the overall bit stream, there is always an integal number of unit intervals.

Synchronous Network - A network in which the clocks of interconnected stations are controlled so as to run, ideally, at identical rates, or at the same mean rate with limited relative phase displacement. (Note: Ideally the clocks are synchronous, but they may be pleisiochronous in practice).

Universal Coordinated Time (UTC) - UTC is an international time reference maintained by the Bureau International de l'Heure, Paris, France and used by various time service organizations throughout the world. Cesium beam frequency standards are used in maintaining UTC. There atomic standards are adjusted approximately once a year in order to maintain UTC within one second of Mean Solar Time, which is based on the period of rotation of the earth about its axis. The U.S. Naval Observatory uses UTC to provide standard time throughout the U.S. LORAN C, OMEGA, WWV and other systems which distribute precise time and frequency utilize UTC as furnished by the Naval Observatory.

APPENDIX A

TRI-TAC TIMING SUBSYSTEM

The TRI-TAC timing subsystem is based on the use of independent clocks plus buffers to provide synchronous operation over finite (but long) periods of time. Within the Tactical Communications Control Facilities (TCCF), the Communications Nodal Control Element (CNCE) contains three levels of timing, which in order of precedence are: (1) cesium standard accurate to 1 part in 10^{11}, (2) timing derived from selected trunk groups, and (3) two quartz oscillators. Specifically, the first level of timing consists of a nonredundant cesium clock (HP 5062C) which acts independently from any other clock in the system. Upon failure of the atomic standard, the timing subsystem of the CNCE will switch to the second level, a timing source derived from selected incoming trunk groups (i.e., slaved to the cesium clock of an adjacent node). Two such trunks are specified as primary and secondary sources. The primary trunk group timing is first switched in line; upon its failure, the secondary trunk group timing is switched in line. Upon failure of both primary and secondary trunk group timing lines, the third level of timing is utilized. Here two quartz oscillators are provided each with accuracy of 1 part in 10^7 and long-term drift rate of 2×10^{-9}/day. One quartz oscillator is assigned as primary, the other is assigned as secondary. Failure in the primary oscillator causes automatic switchover to the secondary. For all levels of switching described above, no loss of BCI occurs.

Within the TTC-39 switch, a medium-grade quartz oscillator is provided which is phase locked to its companion timing source in the CNCE. Should a failure occur in the timing line from the CNCE to the TTC-39, the TTC-39 will automatically switch to its internal oscillator.

The CNCE timing subsystem is pictured in Figure A-1. The reference selector is locked to the highest precedence time base that is available. Rates at 576 kHz and 4.608 MHz are generated by the reference selector and are input to the clock synthesizer. Several rates are then synthesized and fed to an amplifier for distribution within the CNCE. In addition to the inherent three levels of timing source, there exists a TRI-TAC specification requirement of a 48-hour mean-time-to-loss of BCI for 1×10^{-10} clock accuracies. This specification is easily met by the choice of triply redundant timing sources and sufficient buffer lengths.

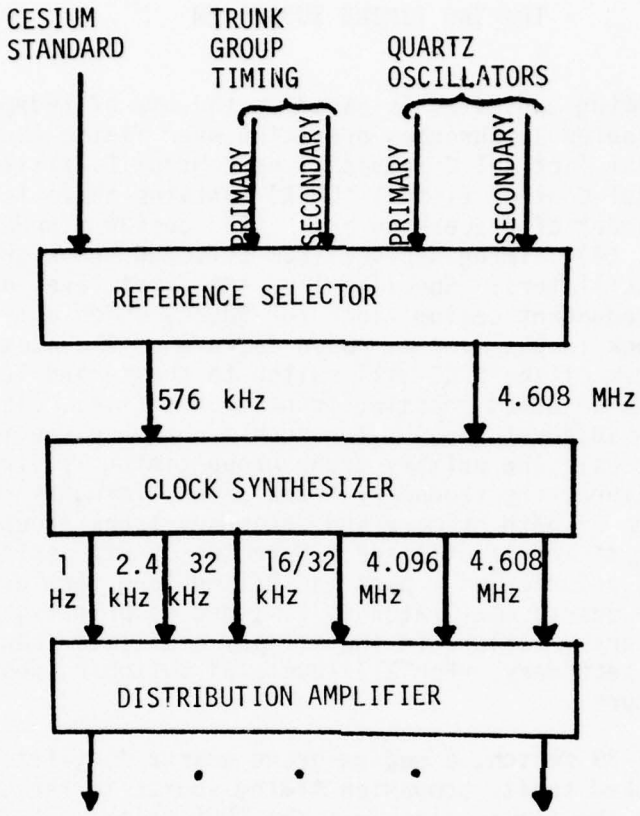


Figure A-1. TRI-TAC Timing Subsystem Contained Within CNCE

Buffers are provided with each individual trunk group as part of the channel reassignment function (CRF) within the CNCE. These buffers perform two functions: (1) to aid in frame alignment of each trunk group, and (2) to account for differences in frequencies between the independent clocks. Each incoming trunk group is first aligned on a subframe basis. Each frame contains eight subframes, and buffers delay each trunk up to one subframe. Once subframe alignment is achieved via buffer delay, the CRF rotates individual subframes to provide total frame alignment. Approximately 100 bits of the buffer are allocated for this subframe alignment function. To provide the additional function of absorbing phase accumulation due to frequency differences, buffer length was increased by an additional 256 bits. The choice of 256 bits resulted from consideration of the highest rate trunk group (4.608 MHz = 144 channels x 32 kb/s/channel) and the requirement of a 48 hour MTTS.

APPENDIX B

APPLICATION OF LORAN C TO THE DCS

1. LORAN C SYSTEM DESCRIPTION

LORAN C is a pulsed, low-frequency (LF), radio navigational system operated by the U.S. Coast Guard. Use of LF provides propagation stability and low attenuation of the groundwave with distance. Thus, highly stable, long-range transmission is possible. LORAN C is widely disseminated in the Northern Hemisphere and hence is a candidate for use with the DCS timing subsystem. Existing LORAN C chains are located in the Norwegian Sea, North Atlantic, Mediterranean Sea, Northwest Pacific, North Pacific, Central Pacific, U.S. East Coast, U.S. West Coast, and Southeast Asia.

The LORAN C system consists of many networks of stations, called chains, all of which broadcast at a low-frequency of 100 kHz. Each chain transmits a unique pulse repetition rate (PRR) by which it is distinguished from neighboring chains. A chain is composed of a master station and a few slave stations, all located within the groundwave transmission of the master station (usually within several hundred miles). All stations within a chain transmit at the same frequency and PRR, but each slave is delayed by some unique code such that the master is always received first at any receiver site. Phase coding is applied to alternate groups of pulses. Each group consists of eight modulated pulses (100 kHz carrier frequency) spaced 1 millisecond (ms) apart, and the master station transmits a ninth pulse 2 ms after the eight pulses for identification purposes. The phase modulation of each pulse in a group is binary ($\pm$ 180°) and is identical for all slaves stations. The inherent delay in receiving a slave is then propagation delay between master and slave stations plus the coding delay. This combined delay is always large enough that no two groups overlap within receiving distance of the station.

LORAN C reception of the groundwave is limited to distances of about 800 to 1200 nautical miles, where attenuation of the 100 kHz groundwave plus interference from the skywave make recovery of the LORAN C signal difficult. The range of LORAN C is, of course, dependent on transmitter power, receiver sensitivity, and losses over the signal path. Figure B-1 shows groundwave coverage of LORAN C based on a conservative estimate of a 800 nm range per transmitter. Within the groundwave range of the station, the highly stable groundwave signal can be used for precise timing and frequency dissemination. The stability of the groundwave is unaffected by diurnal variations or ionospheric perturbations which plague skywave transmission.

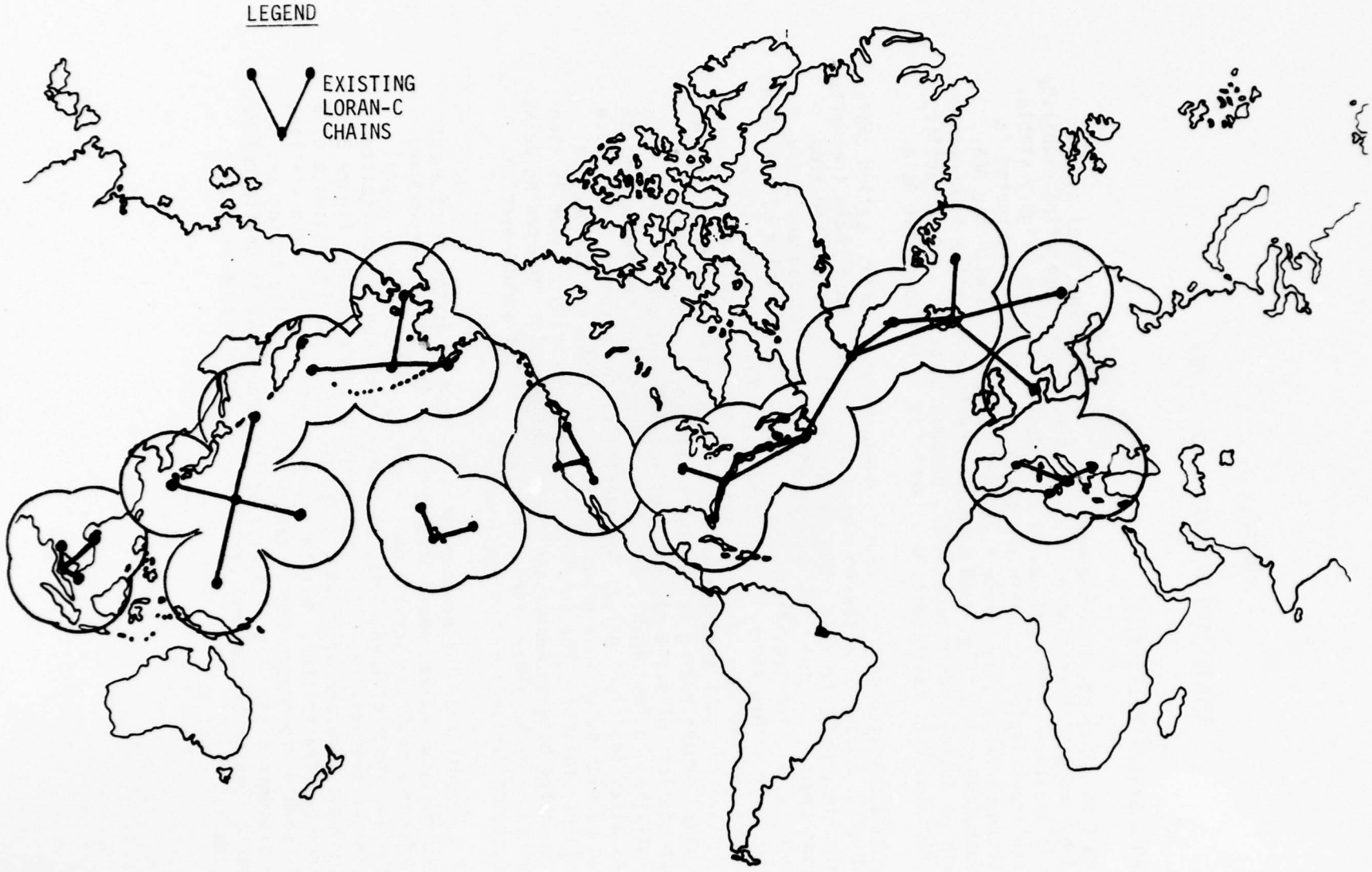


Figure B-1. Groundwave Coverage of LORAN C

All transmitting stations are equipped with cesium frequency standards. Typically, for reliability, master stations have two or three standards, while slave stations have one or two standards. Each LORAN C chain attempts to maintain a constant time difference of each master-slave pair throughout the coverage area. Frequency offsets in the cesium clocks and changes in propagation conditions can cause the observed time difference to vary. When the observed time difference exceeds the allowed time difference, a change in the timing of the slave stations is made to remove the error. Moreover, LORAN C stations provide precise time and frequency by synchronizing their cesium standards to Universal Coordinated Time (UTC) as determined by the U.S. Naval Observatory. The Naval Observatory periodically publishes a table of time differences for each LORAN C chain which has been synchronized to UTC. LORAN C cesium standards can then be periodically updated to conform with UTC.

LORAN C signals are received by an automatic tracking receiver which phase locks a local oscillator to the incoming LORAN C signal. When used within the groundwave reception range, the phase-locked frequency output will exhibit the long-term stability of the LORAN cesium standard. The long-term frequency will be within a few parts in 10^{12} per day; however, short-term stability may be affected by receiver noise and signal interference.

The LORAN C system as it operates today has demonstrated a 99.7% availability, excluding scheduled off-the-air maintenance which reduces that figure to about 99%. The U.S. Coast Guard has new equipment under development which will permit on-the-air maintenance, and also improve the system availability, with a goal of better than 99.7% including all interruptions of service.

2. AN/GSQ-183 FREQUENCY CONTROL SET

The AN/GSQ-183 provides frequency calibration via utilization of LORAN C. This system generates three 1 MHz frequency standards which are phase locked to LORAN C. Additionally, the system can lock to an external 1 MHz reference, should the primary reference (LORAN C) become unavailable. If both the LORAN C and external reference disappear, the system will lock to the last known frequency set by the servo memory action. The AN/GSQ-183 consists of several individually packaged equipments which are interconnected as shown in Figure B-2, and which are briefly described below.

a. R-1776 LORAN Receiver. In the R-1776 receiver, the received 100 kHz signal is amplified, filtered, and then phase decoded. Phase decoding is accomplished by generating the pulse generating rate from a 1 MHz standard. The 1 MHz standard is supplied by the frequency multiplier.

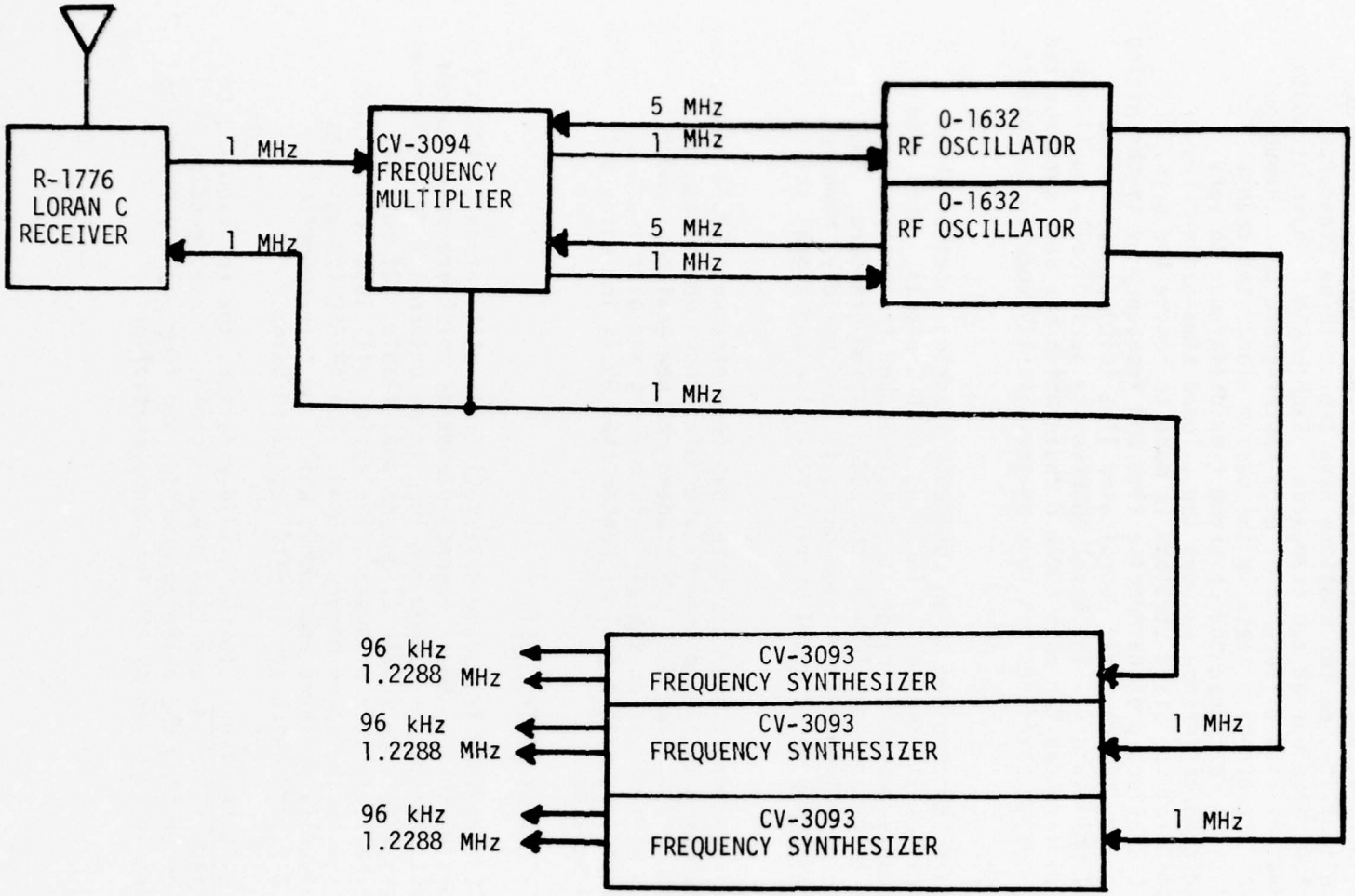


Figure B-2. AN/GSQ-183 Frequency Control Set As Configured For Current AUTODIN Applications

b. CV-3094 Frequency Multiplier. The CV-3094 performs as a frequency combiner, frequency synthesizer, and distribution amplifier. First, the CV-3094 phase locks the secondary reference (if provided) to the primary (LORAN C carrier for DCA applications). A 1 MHz synthesizer provides two 1 MHz outputs derived from either the LORAN C signal (primary source) or from the phase-locked external reference (secondary source). These two 1 MHz signals are fed to separate 5 MHz oscillators (O-1632 RF oscillator) where phase locking to the incoming 1 MHz is achieved via servo control. Failure of one of the 5 MHz oscillators results in switchover to the remaining operative standard without loss of BCI. A combiner then obtains the sum frequency of the two 5 MHz signals. A divide-by-10 circuit then produces a phase averaged 1 MHz signal which is input to the LORAN C receiver (R-1776). This same signal also is provided as the master clock to a separate frequency synthesizer (CV-3093).

c. O-1632 RF Oscillator. The O-1632 is a high stability, dual-oven crystal oscillator controlled by a third-order servo loop. Two O-1632 oscillators are provided for increased reliability within the GSQ-183. Each is disciplined to LORAN C (or external source), and each is provided as a 1 MHz frequency standard to the synthesizer.

d. CV-3093 Frequency Synthesizer. The CV-3093 is a triplicated frequency synthesizer. Each syntehsizer accepts one of the three 1 MHz standards and generates 96 kHz and 1.2288 MHz rates, as required by AUTODIN switches.

3. CHANNEL PACKING AND AUTODIN USE OF AN/GSQ-183

Currently, there are two DCS subsystems-Channel Packing and AUTODIN-which utilize the AN/GSQ-183 to provide synchronous timing via LORAN C. The Channel Packing system provides low- and medium-speed synchronous digital submultiplexing, with the maximum output rate of 9.6 kb/s, for transmission over 4 kHz analog channels. Most Channel Packing stations are configured with one AN/GSQ-183 and a companion frequency synthesizer, the AN/FSQ-44A. The AN/FSQ-44A utilizes triple redundancy in generating a number of low-rate frequencies, including those required for Channel Packing equipments. At AUTODIN switch locations, the CV-3093 synthesizer, described above as part of the AN/GSQ-183, develops a 1.2288 MHz standard. Each AUTODIN switch then develops its required rates from this 1.2288 MHz standard. There are approximately a dozen DCS stations which utilize the AN/GSQ-183 for Channel Packing and/or AUTODIN applications. Experience to date has indicated an excellent service record for the AN/GSQ-183 and the LORAN C system.

4. DCS II TIMING SUBSYSTEM USE OF AN/GSQ-183

The existing AN/GSQ-183 can be used as the timing source for the DCS II timing subsystem. Of those individual equipments which comprise the AN/GSQ-183, only the CV-3093 frequency synthesizer would not be required. In its place, the clock distribution system (Appendix C) would provide the clocked frequencies required for AUTOSEVOCOM II.

Before applying the LORAN C based timing subsystem to a particular upgrade, site surveys are recommended to determine the availability and stability of LORAN C groundwave reception. Some sites may not provide adequate groundwave reception, so that it may be necessary to use either skywave reception, provide a LORAN C receiver with increased sensitivity, or utilize a separate atomic clock.

APPENDIX C

DCEC SPECIFICATION R220-77-2

PERFORMANCE SPECIFICATION

CLOCK DISTRIBUTION SYSTEM

1.0 Scope

This specification establishes performance requirements for a clock distribution system to be used in conjunction with the AN/GSQ-183 Frequency Control Set to provide synchronous timing in support of AUTOSEVOCOM II.

2.0 Applicable Documents

DCEC Memo - AUTOSEVOCOM II Transmission Interface Description, 27 May 1977.

3.0 Requirements

3.1 Item Definition

3.1.1 Item Description

The clock distribution system shall operate in conjunction with the AN/GSQ-183 Frequency Control Set to provide synchronous rates to transmission and switching equipments from which AUTOSEVOCOM II circuits are derived. The functions of the clock distribution system shall include:

a. Accepting the three independent 1 MHz outputs of the AN/GSQ-183.

b. Providing triple redundancy in generating clocked frequencies for several required rates.

c. Distributing these clocked frequencies to individual transmission and switching equipments.

d. Providing alarms for failures which do not cause system outage and failures which do cause system outage.

3.1.2 Typical Network Configuration

The clock distribution system and its associated AN/GSQ-183 will provide synchronous timing to all transmission and switching equipments of an AUTOSEVOCOM II node. Figure 1 displays the layout of station timing for a typical synchronous node employing a DAX and DRAMA transmission equipments.

FIGURE 1. TYPICAL APPLICATION OF CLOCK DISTRIBUTION SYSTEM

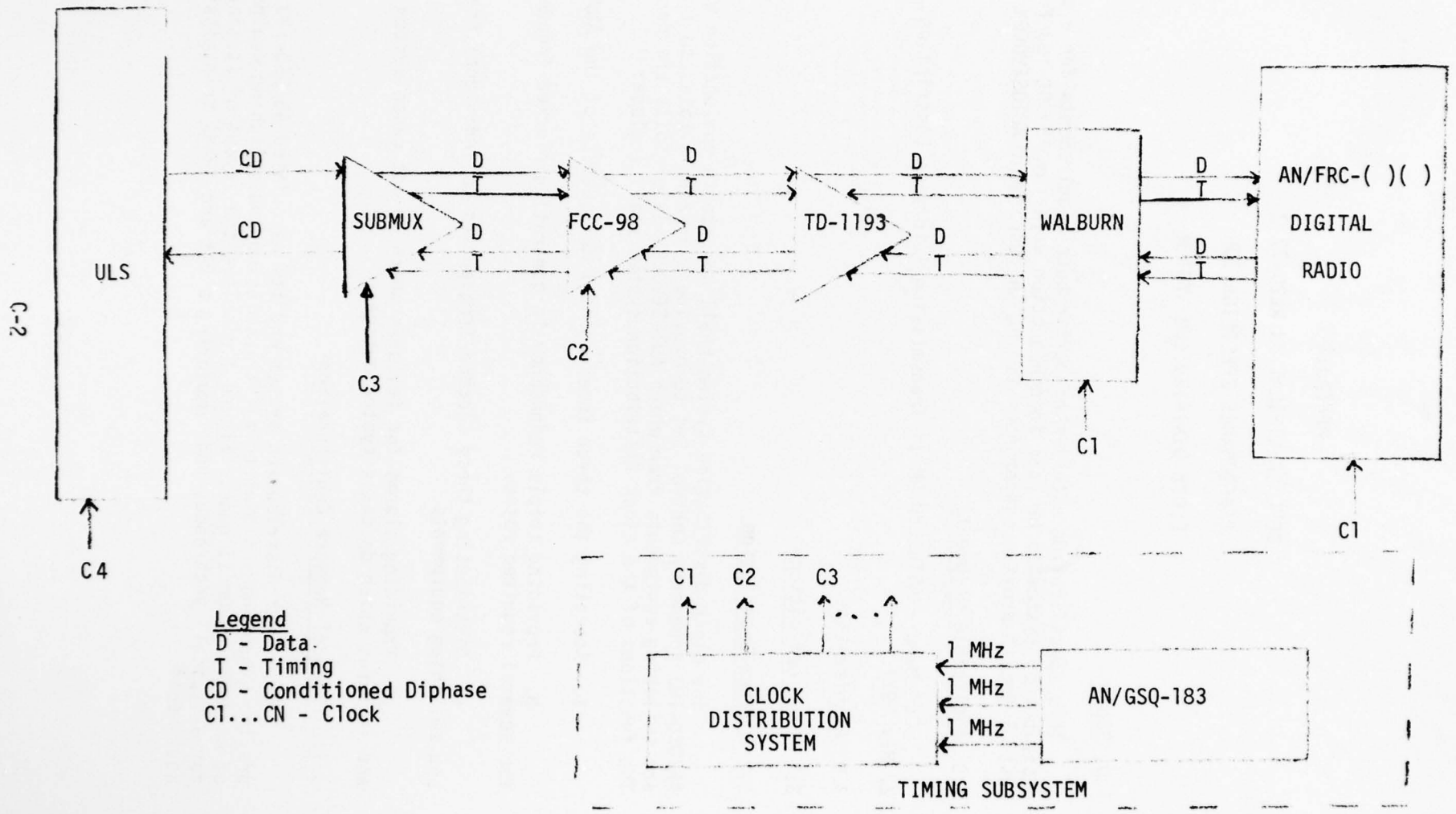
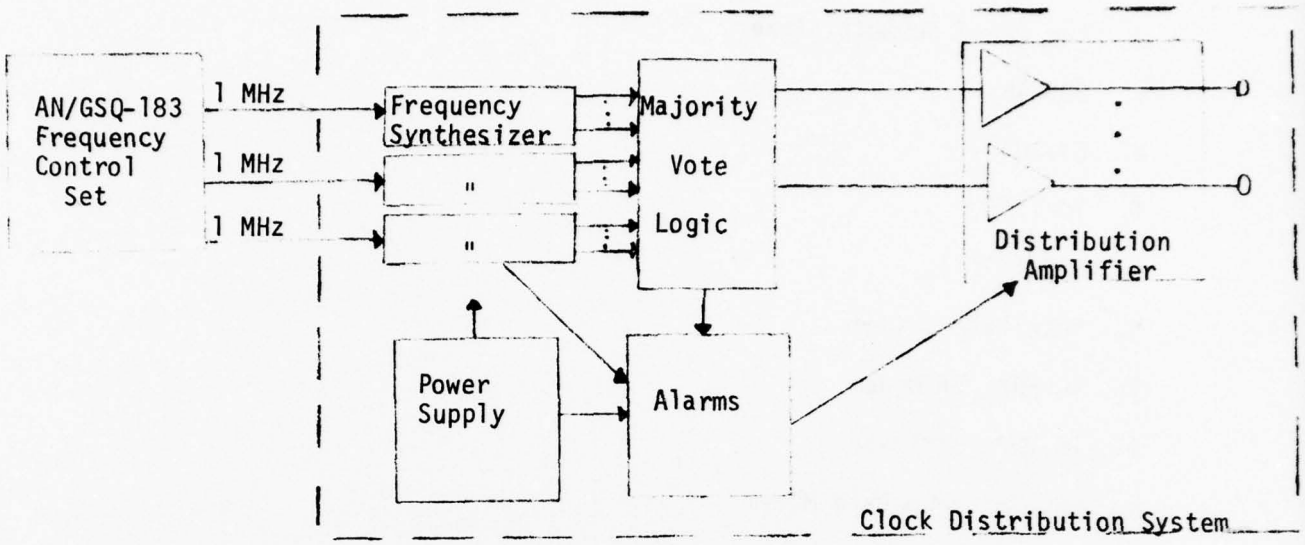


Figure 2. Functional Schematic of Clock Distribution System



3.1.3 Functional Schematic

A functional schematic of the clock distribution system is shown in Figure 2.

3.1.4 Interface Definition

The clock distribution system shall provide the interfaces shown in Figure 2 and specified below:

3.1.4.1 AN/GSQ-183 Interface

The triplicated frequency synthesizer of the clock distribution system shall interface with the three phase coherent 1 MHz outputs of the AN/GSQ-183 Frequency Control Set. Characteristics of this interface shall be as specified in U.S. Army TM 11-5895-822-14.

3.1.4.2 Communication Equipment Interface

The distribution amplifier of the clock distribution system shall interface with any of the following communication equipments at their external clock input:

a. AN/TTC-39

b. ULS

c. Low Speed Submultiplexer

d. FCC-98

e. CY-104

f. TD-1193

g. FRC-( )( )

h. Satellite Buffer

i. 16 Kb/s VF Modem

j. 16 Kb/s Biplexer

k. GSC-36 Group Data Modem

l. TRI-TAC TGM

The distribution amplifier outputs may be at any arbitrary phase but must be frequency locked to the incoming 1 MHz frequency standards. For outputs at 2.048 Mb/s and below the interface characteristics specified for timing signals of the TD-1192 shall be met. For output rates above 2.048 Mb/s, the interface characteristics specified for timing signals at rates above 2 MHz of the TD-1193 shall be met.

3.1.4.3 Power Supply Interface

Provide optional power supply modules to operate from either 115 VAC, 60 Hz or -48 VDC.

3.1.4.4 Remote Alarm Interface

All remote alarms shall be contact closures capable of carrying 250 milliamperes.

3.2 Performance Characteristics

3.2.1 Frequency Generation Characteristics

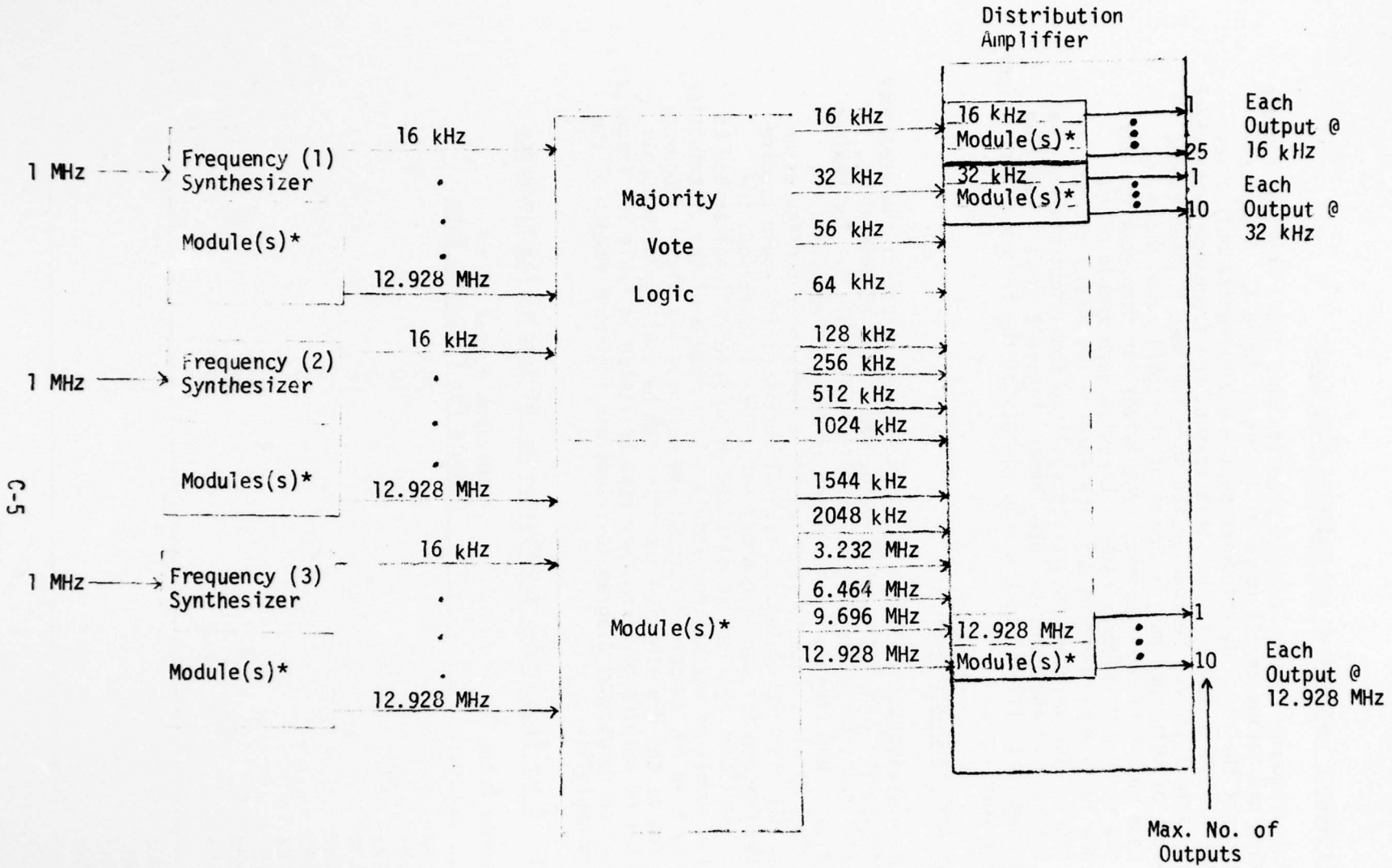


Figure 3. Detailed Functional Diagram of Clock Distribution System

* Number of Modules is Unspecified

3.2.1.1 Frequency Synthesizer and Majority Vote Logic

The frequency synthesizer and majority vote logic shall be capable of generating and voting on all rates as listed in Table 1. A typical configuration of the clock distribution system would require only a few of the rates listed in Table 1. For this reason, the frequency synthesizer and majority vote logic may be modularized in which case a given module would generate or vote upon only a subset of the total rates shown in Table 1. Each module of the frequency synthesizer may then generate any number of the required frequency rates. Likewise each module of the majority vote logic would perform majority vote on any number of the frequency rates. The selected modularity shall be consistent between the frequency synthesizer and majority vote logic. Figure 3 gives a detailed functional diagram to illustrate the requirements of the frequency synthesizer and majority vote logic.

3.2.1.2 Distribution Amplifier

The distribution amplifier shall accept the output of the frequency synthesizer/majority vote logic and have the capability of generating, for each frequency rate, the number of outputs listed in Table 1. The maximum number of outputs per frequency rate listed in Table 1 represents the maximum density of clock outputs required for a particular configuration of the clock distribution system. A typical configuration would require less than the maximum for each frequency rate. For this reason, the distribution amplifier shall be modularized using some rational method to arrive at the number of outputs per module. Each module of the distribution amplifier may have any number of outputs and may have any mix of frequency rates, so long as the distribution amplifier can be configured to supply the maximum number of outputs per frequency rate as listed in Table 1. Figure 3 gives a detailed functional diagram to illustrate the requirements of the distribution amplifier.

Table 1. Clock Frequencies and Maximum No. of Outputs Per Frequency

Clock Frequency Rates	Maximum Number of Outputs Per Frequency Rate
16 kHz	25
32 kHz	10
56 kHz	15
64 kHz	10
128 kHz	15
256 kHz	15
512 kHz	10
1024 kHz	10
1544 kHz	60
2048 kHz	10
3.232 MHz	10
6.464 MHz	10
9.696 MHz	10
12.928 MHz	10

3.2.2 Redundancy Performance

3.2.2.1 Frequency Synthesizer and Majority Vote Logic

The clock distribution system shall provide three frequency synthesizers followed by majority vote logic, as shown in Figure 2. Each frequency synthesizer shall accept one of the three phase coherent 1 MHz outputs of the AN/GSQ-183 and generate the required rates. For each required frequency rate the triply redundant frequency synthesizer shall provide three outputs to the majority vote logic. The majority vote logic shall then select one of these three outputs and provide the selected frequency rate to the distribution amplifier. The majority vote logic shall determine which (if any) of the three frequency synthesizers disagrees with the other two. If one frequency synthesizer is found to be in disagreement with the other two, its output shall be removed from the input to the distribution amplifier. If all three frequency synthesizers are found to disagree, the majority vote logic shall lock to one of the frequency synthesizers. If two or more of the frequency synthesizers are found to agree, the majority vote logic shall select any one of the agreed frequency synthesizers for output to the distribution amplifier.

3.2.2.2 Distribution Amplifier

The distribution amplifier shall accept the output of the majority vote logic and provide individually buffered outputs as specified in Table 1.

3.2.2.3 Functional Reliability

The mean time between the loss of usable signal of each output signal shall be not less than 200,000 hours.

3.2.3 Alarm Functions

The clock distribution system shall provide the following alarm functions.

a. Majority vote disagreement. An alarm shall be provided if one frequency synthesizer is found to disagree with the other two.

b. Loss of Frequency Standard. An alarm shall be provided to indicate loss of one (or more) of the three 1 MHz frequency standard inputs.

c. Loss of Output. An alarm shall be provided with each buffered output of the distribution amplifier to indicate loss of signal.

d. Loss of Input Power. An alarm shall be provided to indicate loss of primary power input to the clock distribution system.

Each of the above alarms shall be represented by a red front panel light (except the loss of power alarm which shall have a white light when not alarmed) and shall be remotable as specified in 3.1.4.4.

3.3 Physical Characteristics

The clock distribution system shall mount in a standard 19-inch rack with mounting provisions as specified in MIL-STD-189.

3.4 Reliability

The clock distribution system shall have a specified mean-time-between-failure (MTBF) of not less than 500 hours.

3.5 Maintainability

The clock distribution system shall have a mean corrective maintenance time of no greater than 20 minutes. The construction of the clock distribution system shall be modular with sufficient fault indicators and test points to support rapid fault isolation to the module level.

3.6 Environmental

The clock distribution system shall operate continuously and meet all performance requirements of this specification when subjected to environmental conditions within the operating ranges specified below. After storage in the environmental nonoperating ranges specified below, the terminal shall meet the performance requirements of this specification.

	Operating	Nonoperating
Temperature, degrees C	0 to 49	-40 to 68
Relative humidity	Up to 95%	Up to 95%
Altitude, feet, MSL	Up to 15,000	

3.7 Power

The clock distribution system shall be capable of operating from a station battery of -48 VDC or from 115 VAC, 60 Hz, using optional modules.

3.8 Electromagnetic Interference (EMI)

The clock distribution system shall be designed, constructed, and tested for compliance to the requirements of MIL-STD-461, Notice 4, Table VI, Ground C-E Equipment and Component Items of equipment for multiplexers, 4.2.6 Commercial Equipment.

3.9 Parts, Materials, and Processes

The selection and application of parts, materials, and processes for and during fabrication of the equipment shall be based on an analysis of the specified requirements of reliability, maintainability, environmental, ruggedness, and electromagnetic interference.

DISTRIBUTION LIST

STANDARD:

R100 - 2
R102/R103/R103R - 1
R102M - 1
R102T - 9 (8 for stock)
R104 - 1
R110 - 1
R123 - 1 (Library)
R124A - 1 (for Archives)
R200 - 1
R300 - 1
R400 - 1
R500 - 1
R700 - 1
R800 - 1

DCA Code 101A - 1
DCA Code 101C - 1
DCA Code 400 - 1
DCA Code 410 - 1
DCA Code 440 - 1
DCA Code 470 - 1
DCA Code 480 - 1
DCA Code 500 - 1
DCA Code 800 - 1
DCA Code 1100 - 1
931 - 1
NCS-TS - 1
205 - 20

DCA-EUR - 1 (Defense Communications Agency European Area
ATTN: Technical Director
APO New York 09131)

DCA-PAC - 1 (Defense Communications Agency Pacific Area
ATTN: Technical Director
APO San Francisco 96515)

USDCFO - 2 (Chief, USDCFO/US NATO
APO New York 09667)

SPECIAL:

Rome Air Development Center
DCC - 2
DCLD - 1
Griffiss Air Force Base, New York

U.S. Army Communications Command
CC-OPS-ST - 1
CC-OPS-SM - 1
Ft. Huachuca, Arizona

U.S. Army Communications Electronics Engineering
Installation Agency
CCC-XEM-CED - 2
Ft. Huachuca, Arizona

U.S. Army Communications Systems Agency - 2
CCC-RD
Ft. Monmouth, New Jersey

U.S. Army Electronics Command - 1
DRSEL-NL-RM
Ft. Monmouth, New Jersey 07703

U.S. Army Electronics Command - 2
DRSEL-NL-RM3
Ft. Monmouth, New Jersey 07703

U.S. Research and Development Coordination Office (USRADCO) - 2
SHAPE TECHNICAL CENTER
The Hague, Netherlands

National Security Agency
S254 - 2
S121 - 2
S411 - 1
Ft. George G. Meade, Maryland

U.S. Air Force Systems Command
Electronics System Division
DCF - 3
L. G. Hanscom Field
Waltham, Mass. 0215

U.S. Air Force Communications Service
EPPB - 1
EPEG - 2
Scott Air Force Base, Illinois

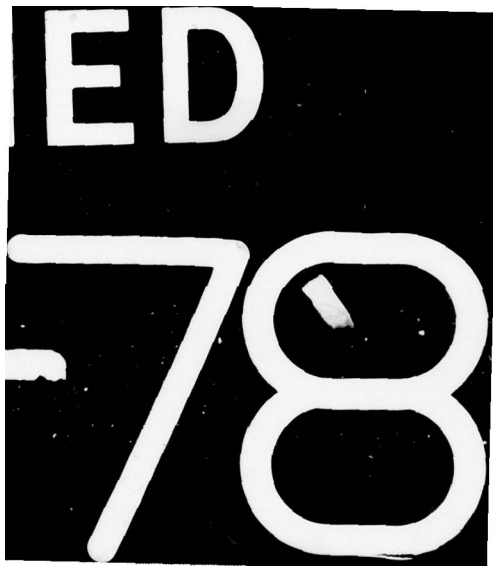
U. S. Army Satellite Communications Agency
DRCPM-SC-5G
Fort Monmouth, New Jersey 07703

U.S. Army Satellite Communications Agency
DRCPM-SC-5G
Ft. Monmouth, New Jersey 07703

Commander General
TRI-TAC Office
Ft. Monmouth, New Jersey 07703

Commander
Naval Electronics System Command
4401 Massachusettes Avenue
Washington, D.C. 20390

Commander
Naval Telecommunications Command
4401 Massachusetts Avenue, N.W.
Washington, D.C. 20390


ED
78