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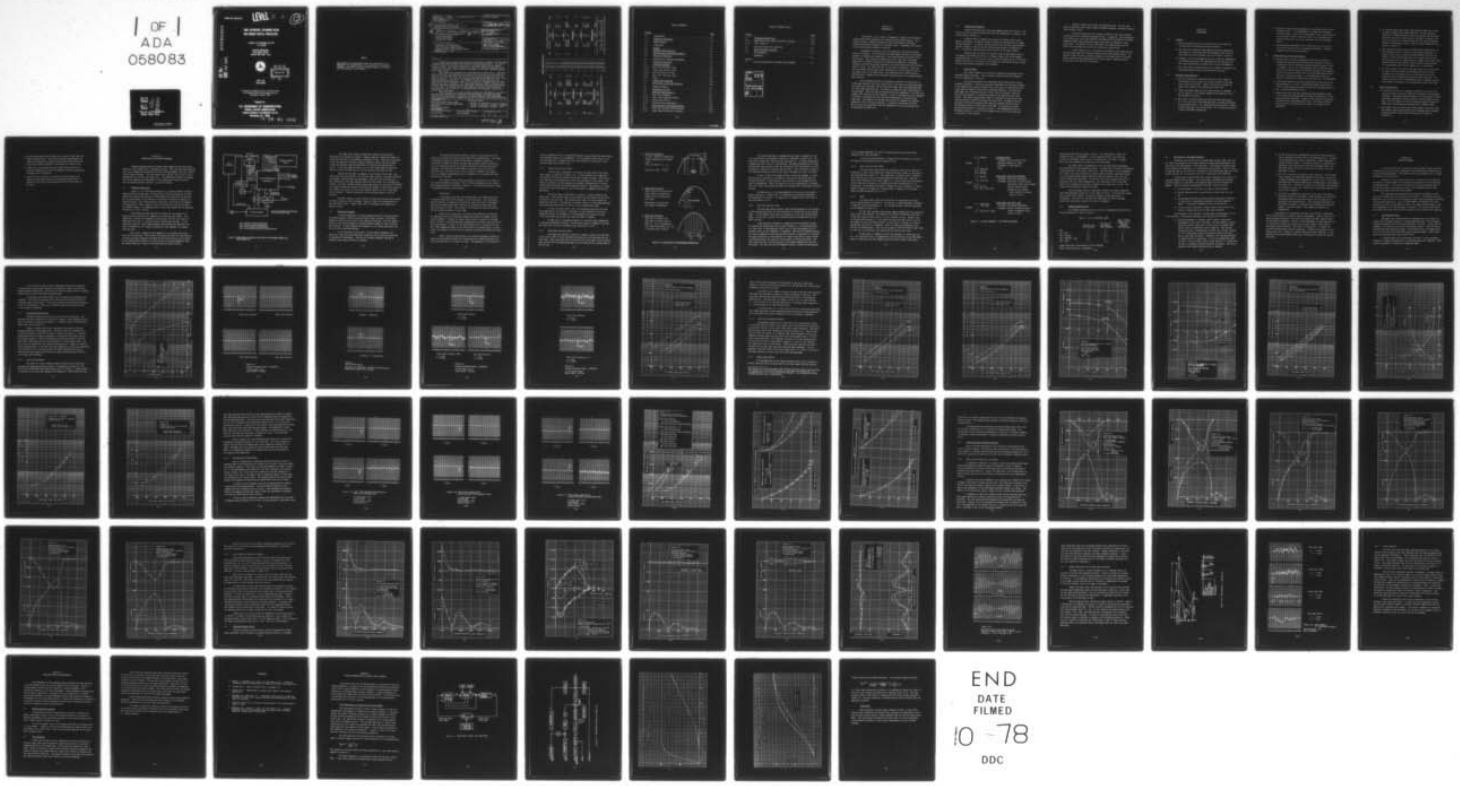

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TIME REFERENCE SCANNING BEAM MULTIMODE DIGITAL PROCESSOR

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FINAL REPORT

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16. Abstract

Landing system simulations have been carried out in support of the Microwave Landing System (MLS) program of the Federal Aviation Administration. The results of these simulations have been published in an interim report and in Calspan Technical Notes. This report contains the results of extensive simulation evaluations of a multimode digital processor developed for the time reference scanning beam (TRSB) system.

Four processing algorithms were developed for the TRSB system. Simulation tests showed that the algorithms developed for the dwell gate processor were less sensitive to multipath errors and had less processing noise than the flight test phase 3 receivers. The split gate processor had smaller multipath and noise errors than the dwell gate processor. Two asymmetrical processing algorithms were implemented that had multipath errors of less than half the magnitude of the dwell gate or split gate techniques. The single edge processor (SEP) is effective for reducing elevation multipath errors from hangar reflections and ground reflections in flare data. An adaptive SEP was developed that can be used for azimuth or elevation data and is effective in reducing errors from multipath that occurs on either edge of the beam.

The algorithms for the four processing modes were implemented in an LSI-11 microprocessor packaged for convenient field and flight tests. The multimode features permit processing an elevation or azimuth function in all four modes. This feature permits direct comparisons between the different processing techniques during any test.

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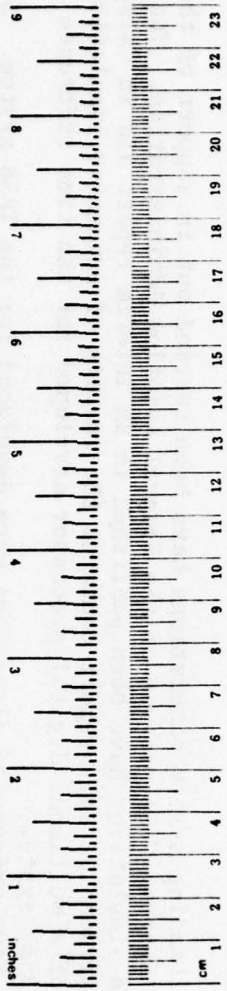
METRIC CONVERSION FACTORS

Approximate Conversions to Metric Measures

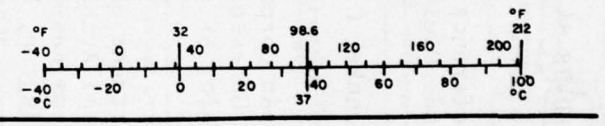
Symbol	When You Know	Multiply by	To Find	Symbol
		LENGTH		
in	inches	*2.5	centimeters	cm
ft	feet	30	centimeters	cm
yd	yards	0.9	meters	m
mi	miles	1.6	kilometers	km
		AREA		
in^2	square inches	6.5	square centimeters	cm^2
ft^2	square feet	0.09	square meters	m^2
yd^2	square yards	0.8	square meters	m^2
mi^2	square miles	2.6	square kilometers	km^2
	acres	0.4	hectares	ha
		MASS (weight)		
oz	ounces	28	grams	g
lb	pounds	0.45	kilograms	kg
	short tons (2000 lb)	0.9	tonnes	t
		VOLUME		
tsp	teaspoons	5	milliliters	ml
Tbsp	tablespoons	15	milliliters	ml
fl oz	fluid ounces	30	milliliters	ml
c	cups	0.24	liters	l
pt	pints	0.47	liters	l
qt	quarts	0.95	liters	l
gal	gallons	3.8	liters	l
ft^3	cubic feet	0.03	cubic meters	m^3
yd^3	cubic yards	0.76	cubic meters	m^3
		TEMPERATURE (exact)		
°F	Fahrenheit temperature	5/9 (after subtracting 32)	Celsius temperature	°C

*1 in = 2.54 (exactly). For other exact conversions and more detailed tables, see NBS Misc. Publ. 286, Units of Weights and Measures, Price $2.25, SD Catalog No. C13.10:286.



Approximate Conversions from Metric Measures

Symbol	When You Know	Multiply by	To Find	Symbol
		LENGTH		
mm	millimeters	0.04	inches	in
cm	centimeters	0.4	inches	in
m	meters	3.3	feet	ft
m	meters	1.1	yards	yd
km	kilometers	0.6	miles	mi
		AREA		
cm^2	square centimeters	0.16	square inches	in^2
m^2	square meters	1.2	square yards	yd^2
km^2	square kilometers	0.4	square miles	mi^2
ha	hectares (10,000 m^2)	2.5	acres	
		MASS (weight)		
g	grams	0.035	ounces	oz
kg	kilograms	2.2	pounds	lb
t	tonnes (1000 kg)	1.1	short tons	
		VOLUME		
ml	milliliters	0.03	fluid ounces	fl oz
l	liters	2.1	pints	pt
l	liters	1.06	quarts	qt
l	liters	0.26	gallons	gal
m^3	cubic meters	35	cubic feet	ft^3
m^3	cubic meters	1.3	cubic yards	yd^3
		TEMPERATURE (exact)		
°C	Celsius temperature	9/5 (then add 32)	Fahrenheit temperature	°F



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Section 1.0
INTRODUCTION

The material in this report is prepared in support of the Microwave Landing System (MLS) program for the Federal Aviation Administration. This report describes a digital multimode processor developed for evaluating different processing techniques for the TRSB system. Performance test results of four processing algorithms are included.

Performance evaluation tests were conducted on the MLS simulation facility at Calspan. In this facility the TRSB signal received by an airborne receiver is simulated and translated to the C-band frequency required in the MLS receiver. This simulation includes the direct signal and a multipath signal that is computer controlled to represent any amplitude, scalloping frequency and beam coding angle required by the reflecting surface and aircraft velocity vector. The TRSB simulator, as described in Reference 1, has been used to evaluate the multipath error characteristics of the receivers used in the flight tests of the TRSB system. The large data base on TRSB receivers has been used in comparing the performance characteristics of the digital multimode processor.

The multimode processor was developed to explore the feasibility of a dual mode processor that uses a dwell gate or split gate processing algorithm for azimuth and long range elevation data and single edge processing algorithms for short range elevation data. In addition an adaptive single edge processor was developed. These four processing algorithms were implemented in the PDP-11/10 computer that controls the MLS simulator. An LSI-11 microprocessor was configured to provide a convenient test unit for field evaluations of the processing algorithms. The software for the PDP-11/10 and LSI-11 computers are program compatible with a few minor exceptions. It should be noted that the dwell gate or split gate algorithms could be implemented in an 8-bit processor for an operational airborne unit.

1.1 Background Information

Fourteen technical notes have been prepared under this contract. The data in the first twelve technical notes has been summarized or included in the interim report, Reference 1.

Technical Note 13 contains the results of simulator tests on two phase 3 receivers to be used by the UK in flight test evaluations of the TRSB system, Reference 2. Frequency responses were run on the angle analog outputs and were similar to those run on the digital angle outputs, as reported in TN-5. In addition, autocorrelation tests were run on the angle outputs.

Technical Note 14 reports the results of field measurements made on the Doppler scan format during the J.F. Kennedy flight tests of the Doppler system, Reference 3. The 6 x 6 (six scans in one direction and six in the other) azimuth scans and 20 x 20 elevation scan format were recorded by using a C-band receiver with suitable laboratory test equipment.

1.2 Scope of Report

This report summarizes the results of simulation evaluations of the multimode digital processor. The conclusions resulting from the simulation tests are summarized in Section 2.

Four processing modes were implemented and evaluated under various multipath situations. These four processing algorithms were done with software in the computer and included the dwell gate, split gate or centroid processor, single edge and adaptive single edge processing techniques. The dwell gate algorithms were an improved version of those used in the phase 3 receiver. The centroid processor is a digitized version of the Australian split gate tracker. The single edge processor (SEP) is a digitized version of the early analog processors tested for elevation and flare data. An adaptive SEP was developed to minimize multipath errors under all possible situations when the multipath occurs on either edge of the beam. A description of these processing algorithms is included in Section 3. The implementation of the multimode processor in an LSI-11 microcomputer for use in field evaluations is described in this section.

Section 4 reports the results of simulation tests. The test data show the processor errors under various multipath situations, multipath scenarios and low signal levels.

Field test objectives are outlined in Section 5 that should provide verification of the simulator performance tests. In addition, the susceptibility of the dwell gate, split gate processor and adaptive SEP algorithms to aircraft shadowing effects when processing azimuth data would be evaluated in these field tests. The schedule for the ICAO flight test demonstrations did not permit time for completing field tests within this report period.

A brief analysis of the aircraft path following filter approximations was made using some early elevation channel closed loop simulation data. The results of this study are included in Appendix A and showed that the selected filter provided closer approximations to aircraft error responses than the filter used in the ICAO data evaluations.

Section 2.0
CONCLUSIONS

2.1 General

- The MLS Simulation Facility has proven to be very useful for developing and evaluating processing techniques.
- The split gate processor algorithms provide better performance with respect to processing noise and multipath errors than the dwell gate processing technique used in the phase 3 receivers.
- Although a 16-bit microcomputer (LSI-11) is used for implementing the multimode processor, the algorithms for the split gate and dwell gate processors are suitable for an 8-bit microcomputer.
- The single edge or adaptive SEP are very effective techniques for reducing multipath errors in elevation and flare data.

2.2 Processor Characteristics

- An 8-bit resolution in quantizing the log IF video output is satisfactory and only results in a small increase in processor noise relative to 12-bits. Going to 8-bits does increase the signal level required for acquisition by about 2 dB.
- Eight microsecond sampling of the video waveform is adequate. It was not possible to try reduced sampling rates because of time and equipment constraints.
- Split gate or centroid processors should use four data points (N = 4) on each side of the beam peak value to minimize multipath and processing errors. For a simplified processor that is limited in processing time, only one data point (N = 1) could be used with a modest performance degradation.

- The Log IF video filter bandwidth has a significant effect on the multipath errors. If the bandwidth is too small the multipath errors increase. An RC filter characteristic with 3 dB attenuation at 20 kHz and 13 dB at 50 kHz was found to be a reasonable compromise between low signal level processor noise and multipath error.
- Autocorrelation measurements can be made with the receivers but are of very limited value in evaluating performance. Frequency response curves are more meaningful.

2.3 Characteristics of Multipath Effects

- The dwell gate processor implemented in the PDP-11 and LSI-11 software had smaller multipath errors than the phase 3 receiver in baseline tests for multipath separation angles between 1.0 and 1.5 degrees. The use of a tracking gate that is offset from the center of the beam discriminates against multipath on the opposite side of the beam and greatly reduces the peak mean and rms errors that occur with centered gates. A one degree per second rate limiter is effective in reducing the rms errors for -1 dB multipath.
- A split gate processor using four data points on each side of the peak amplitude (N = 4) has a significantly smaller mean and rms error at large separation angles than the dwell gate processor for the -1 dB multipath baseline test.
- Single edge processing (SEP) algorithms reduce multipath errors to less than half the magnitude for either the dwell gate or split gate processing techniques. An SEP is very effective in reducing elevation errors from hangar reflections. The digital SEP main lobe and first side lobe errors are about 0.7 as large as the analog SEP.

- An adaptive single edge or dual edge processor (DEP) can be used for both elevation and azimuth situations. The DEP should be effective in reducing elevation errors from hangar roof top multipath that can occur on either edge of the beam. An adaptive SEP may prove effective in reducing errors due to aircraft shadowing effects on azimuth data, such as from an aircraft turning off the runway or taking off.

- The algorithms presently used in the DEP require modifications in the technique used for selecting the unperturbed beam edge. In hangar scenario tests in which the peak multipath level did not exceed -7 dB the correct beam edge is not always selected until the multipath level and separation angles approach their peak values. Software modifications should be made to correct these problems if an operational need for the adaptive SEP is established.

- In a flare scenario the digital SEP peak errors will be about 70% of those for the previously tested analog SEP flare scenarios. It appears that the magnitude of the resulting errors are too large for directly measuring altitude rate from flare data. For closed loop flare control, complementary data is probably required from barometric altitude rate or accelerometer derived rate data.

2.4 Field Test Objectives

- The features of the LSI-11 processor included in the field test unit will greatly facilitate flight test evaluations of processing techniques. Multimode processing during a test run permits relative performance evaluations and only requires a limited amount of test data. The core memory in the LSI-11 processor permits changes or additions to the processing algorithms with a minimal effort.

- Only flight tests can evaluate the effectiveness of the split gate and adaptive single edge processors for reducing aircraft azimuth shadowing effects (from aircraft turning off the runway or taking off).

- The Australian flare unit at NAFEC can be used for both flare and hangar multipath tests. These tests should be supplemented with simulator evaluations to estimate the multipath levels during the flare and to provide additional verification of simulator data.
- Flight tests are required using the single edge processor with different beamwidths to verify the beamwidth correction algorithms developed with the simulator.
- Flight tests are required to evaluate the effectiveness of an adaptive single edge processor in reducing multipath errors at elevation sites where the multipath can occur on either edge of the beam.

Section 3.0
DESCRIPTION OF PROCESSOR TECHNIQUES

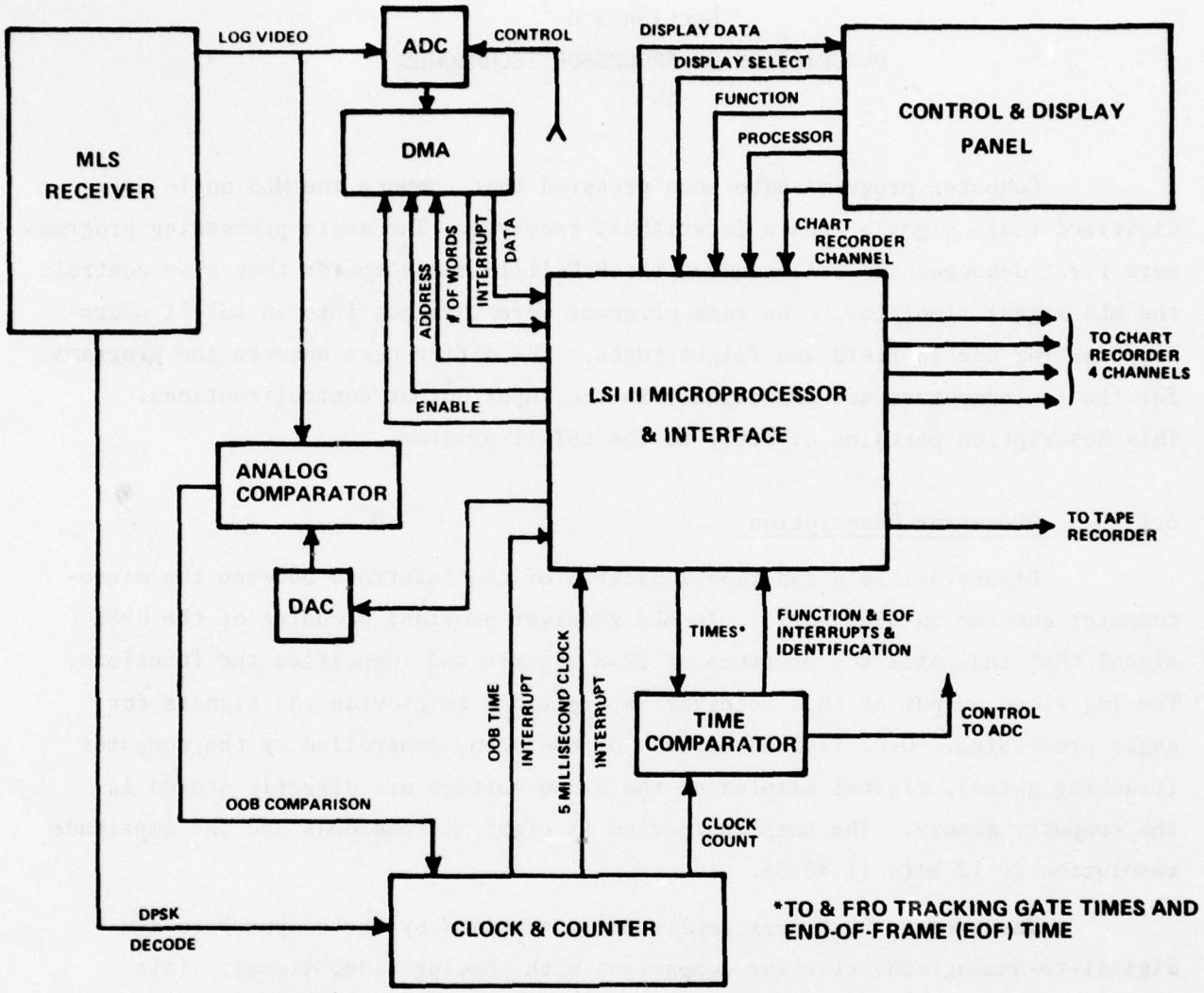
Computer programs have been prepared that compute the MLS angle using digitized video signals from a logarithmic receiver. The angle processing programs were first debugged and evaluated on the PDP-11/10 minicomputer that also controls the MLS signal simulator. The same programs were then put into an LSI-11 microcomputer for use in field and flight tests. The differences between the programs for the two computers are principally in the input/output control routines. This description pertains directly to the LSI-11 program.

3.1 Processor Description

Figure 3-1 is a functional diagram of the interface between the microcomputer and the outside world. An MLS receiver provides decoding of the DPSK signal that indicates the presence of TRSB signals and identifies the functions. The log video output of this receiver is digitized to provide the signals for angle processing. Over limited periods of the scan, controlled by the computer (tracking gates), digital samples of the video voltage are directly stored in the computer memory. The sampling period is eight microseconds and the amplitude resolution is 12-bits (1:4096).

The average beam peak amplitude is supplied by the computer to a digital-to-analog converter for comparison with the log video signal. This comparison is carried on throughout the scan except when the video signal is being digitized, that is, except during the tracking gate periods. If the comparison indicates a video signal greater than the beam peak amplitude, the time of occurrence of that signal is passed on to the computer on a program interrupt basis.

Real time is supplied to the computer by an interrupt that occurs every five milliseconds. This controls the missed scan count for each function. A crystal oscillator supplies the timing for this clock as well as for control of the analog-digital converter activity and the out-of-beam comparison times. The timing counters are reset at each DPSK function identity decode.



ADC – ANALOG TO DIGITAL CONVERTER
DAC – DIGITAL TO ANALOG CONVERTER
DMA – DIRECT MEMORY ACCESS CHANNEL
OOB – OUT-OF-BEAM (OUTSIDE THE TRACKING GATES)

Figure 3-1 FUNCTIONAL DIAGRAM OF MLS DIGITAL PROCESSOR USING LSI II MICROCOMPUTER

The front panel contains switches for control of the processor operations and a display of outputs. Computer speed has limited the number of processors that may be simultaneously exercised to four. These may be allocated in any way among the functions; azimuth, elevation, flare, and back azimuth, except that the dwell gate processor must be used for each function that is active. If the dual edge processor is in use, the single edge processor output will also be available but will not be counted in the limit of four.

Outputs are provided to a magnetic tape recorder (ARINC word), four analog chart recorder channels, and the front panel display. Processor selections for magnetic tape recording take precedence. The chart recorder selections may include any of the tape recorder selections plus others, not to exceed four overall. The chart recorder normally plots angle output but selection "A" provides a one degree calibration signal and selection"B" produces a plot of the flags for the function selected on the next lower numbered channel (as 1/2° offset when flag is present). Channel one monitors out-of-coverage signals in the "B" position.

The panel display is restricted to the functions and processors already selected for tape or chart recording. Identity, flags, and track/acquisition are indicated by LED's. Angle, frame count or confidence count appear on a numeric display.

3.2 Processing Programs

A control program and a display program provide the interface between the manual processor selection and the output signal recording. The display program is called up at the end of each function processing. Then the computer returns to the control program to determine whether changes in input selection have occurred. As these programs are peripheral to the signal processing task they will not be described further.

In the descriptions that follow, certain numeric parameters are indicated. These have been judiciously chosen but not all have been subjected to experimental confirmation. They are all variable parameters and may be changed if the results of tests so indicate.

The dwell gate processor (DGP) is central to the operation of the system as it controls the position and width of the tracking gates. The single edge processor (SEP) also needs the DGP angle to compute an angle bias correction. Neither the SEP nor the dual edge processor (DEP) can operate at very low signal/noise ratios so the DGP is necessary to provide weak signal tracking. The split gate tracker (SPGT) could carry out all of the DGP functions but it was not set up to do so in order to simplify the program. This is an adequate implementation for the purpose of investigating the characteristics of the SPGT.

The output of each of these processors is passed by an α,β filter to the selected recorder and display. The α,β filter parameters are the same as those used previously in the phase 3 receiver. A one degree/second rate limiter is available on the α,β filter output.

Acquisition

In the acquisition mode, the tracking gates are widened and preset to specific positions (0° for azimuth, +3° for elevation). The scan period outside the gates is examined for symmetrical peaks that exceed a threshold. This uses the same program that looks for out-of-beam multipath peaks that exceed the peak in track. Here, however, the threshold is varied to provide ten noise peak indications in each frame.

Within the tracking gates, the peak video amplitudes are examined for amplitude (they must exceed the average noise peak) and symmetry (within 96 microseconds). If peaks are found, either within or outside the tracking gates, a track is initiated with wide tracking gates centered on the position of the detected peaks. Control of the tracking gates then is carried out by the DGP. When symmetrical peaks are not found within the tracking gates, the peak values are assumed to be noise and are averaged to provide an average noise peak level.

After a track has been started, the acquisition program continues to examine the scan period outside the tracking gates for symmetrical peaks that exceed the amplitude of the signal in track. The appearance of such peaks will

cause a confidence count to be decremented while a scan without such peaks causes the confidence count to be incremented. If the confidence count falls to zero the existing track is dropped and a new track started at the position of the external peaks (see Section 3.2.5).

3.2.1 Dwell Gate Processor (DGP)

The DGP sets a threshold at 3 dB below the peak value of the stored video signal as indicated in Figure 3.2a. It then searches for an amplitude rise and fall through the threshold level that includes the peak. The rise and fall times must be separated by at least 20 microseconds to be accepted. The times of occurrence of these passages are linearly interpolated to 1/4 microsecond within the eight microsecond sampling interval. This process is carried out for both the TO and FRO scans and the raw angle is computed from the time difference.

The output angle is provided by a digital α,β filter using the raw angle input. This filtered angle is also used to set the position of the tracking gates on the next scan. The raw dwell gate width, the time between the signal rise and fall, is averaged by a low pass filter (ω = 0.05 radians/second). The average dwell gate width is used to set the tracking gate width.

At very low signal levels, the -3 dB threshold would fall below the noise amplitude of the receiver. Therefore, a fixed threshold of twice the average noise peak is used when the -3 dB threshold falls below this value. If the peak signal falls below this level the frame is skipped.

A frame count is incremented whenever a successful angle computation is made and decremented otherwise. The DGP angle output is flagged at any time the frame count is below a threshold value (see Section 3.2.5).

3.2.2 Single Edge Processor (SEP)

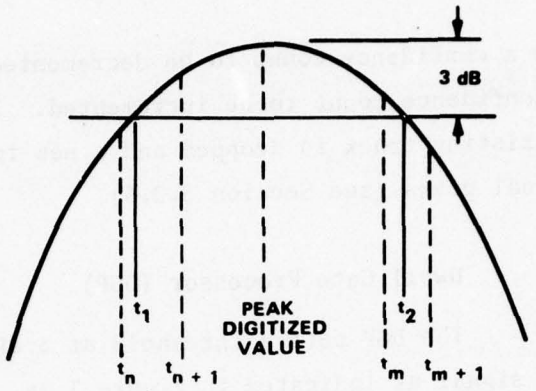
The single edge processor looks for a change in slope on the one edge of the beam in order to avoid multipath perturbations of the beam peak and its other edge. Since multipath typically distorts the inside edges of the elevation beam, the SEP uses the leading beam edge on the TO scan and the trailing edge on the FRO scan.

2a Dwell Gate Processor

t_1 and t_2 found by interpolation between sampling points (dashed lines)

Dwell Gate Width = $t_2 - t_1$

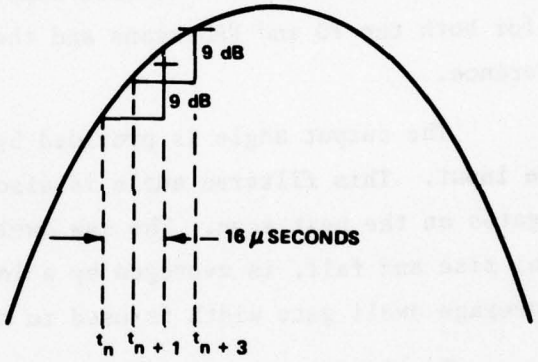
Beam Center Time = $\frac{t_1 + t_2}{2}$



2b Single Edge Processor

Time of 9 dB in 16 microseconds slope found by interpolation between times of greater and less slope

(Equivalent to analog delay and compare thresholding.)



2c Split Gate Processor

Difference of sums of four amplitudes on either side of peak ($\Sigma_1^+ - \Sigma_1^-$) is interpolated with shifted difference ($\Sigma_2^+ - \Sigma_2^-$) to determine beam centroid.

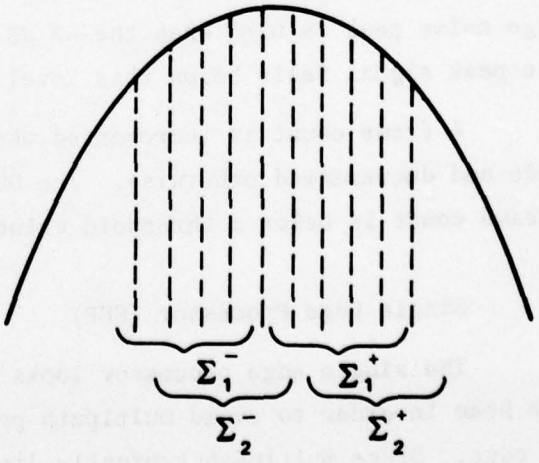


Figure 3-2 ILLUSTRATION OF PROCESSING PROCEDURES

The stored beam shape is examined and the slope is compared to 9 dB in 16 microseconds (two sampling intervals) as indicated in Figure 3-2b. The slope first exceeds this value and then drops below it. A linear interpolation estimates the exact time to 1/4 microsecond. The angle determined by the beam outside edge times is greater than that indicated by the beam centers so a bias correction is necessary to produce the true angle. This correction is taken as the difference between the SEP and DGP angles, averaged over about 20 seconds.

A count is kept of the number of SEP corrections averaged. If multipath occurs, as indicated by a deviation of the raw SEP correction from the average correction (>2 microseconds), the correction is not averaged and the count is decremented. Should the count fall to zero, approximately 30 seconds for a full count, the average correction is discarded and a new average correction started.

The SEP may fail if the beam amplitude falls too low or the beam is greatly distorted. A frame count is incremented on successful measurements and decremented on failures. The angle data is flagged if this count falls to zero (see Section 3.2.5).

3.2.3 Dual Edge Processor (DEP)

The dual edge processor makes single edge measurements on the insides of the scanning beam using the same subroutines as the SEP uses on the outside edges. It then computes the angle by averaging the inside and outside measurements. In this way it cancels out receiving system non-linearities that can affect the SEP.

A DEP equivalent beamwidth is computed from the difference between the outside and inside angles and low pass filtered (ω = 0.05 radians/second). If a high level in-beam multipath occurs, one of these measurements will be shifted so that the raw beamwidth is lengthened. When the raw beamwidth exceeds the average beamwidth by one microsecond the presence of multipath is indicated. The angle computation is then bypassed for several scans while a count is made to determine whether the inside or outside angle is the most perturbed. The least deviated angle is then corrected by the average beamwidth and used for the output. Any time that the raw beamwidth returns to within one microsecond

of the average beamwidth, the count is cleared and both inside and outside angles used for the measurement.

As with the other processors, a frame count is maintained to control the flag on the DEP angle data (see Section 3.2.5).

3.2.4 Split Gate Processor (SPGP)

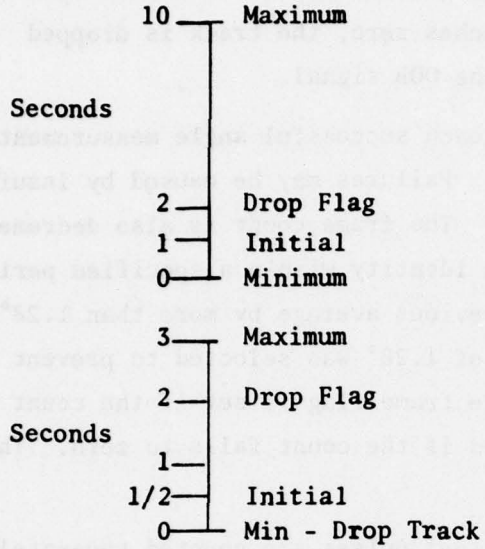
The split gate tracker finds the centroid of each beam by taking the difference of sums of four amplitudes (eight microsecond, apart) on each side of the peak amplitude, Figure 3-2c. The computation is repeated about a sampling point shifted in the direction toward making the difference zero. When the sign of the difference of the sums changes (i.e., sum on inside goes from greater to less than sum on outside), an interpolation finds the mean point to 1/4 microsecond. No beamwidth measurement is needed with this technique as a fixed number of samples (±4 samples at 8 microseconds) is adequate for the normal range of beams encountered (1/2° to 4°).

3.2.5 Flags

The output angles from these processors are flagged when any doubt exists concerning their reliability. In each case, a good measurement increments a count and a failure decrements it. The counters are most succintly described by the diagrams in Figure 3-3.

The SEP, DEP, and SPGP angle outputs remain flagged until the respective counts reach their maximum. This requires two seconds of continuous good data. If half the scans are missed there is no net increase in count. However, once the flag has been removed, it is not again set until the count falls to zero so the output can coast for short periods. If zero count is reached, the track is dropped and a new track is attempted. These processors are dependent on the DGP for the tracking gates. They will not operate if the DGP actually drops track. In that case, all processors lose signal and will quickly drop track.

The DGP angle is flagged if either the confidence or frame flags are set. The confidence count is incremented on each scan when no out-of-beam (OOB) signal is found that has both symmetry about the TO-FRO reversal time and an



Confidence Count

- Increment; No out-of-beam, large amplitude symmetrical signal
- Decrement; an OOB signal is found

Frame Count, Dwell Gate Processor

- Increment; successful measurement
- Decrement; dwell gate <20 microsecond
  Peak signal <Twice noise average
  Time out (missed scan)
  Maximum out-of-coverage count reached (3 seconds)
  Outlier (>1.28°)

Frame Count; SEP, DEP & SPGP

- Increment; successful measurement
- Decrement; failure (distorted signal)
  Failure (inadequate level)
  Outlier (1.28°)

Figure 3-3 DIGITAL PROCESSOR - FLAG CONTROL COUNTERS

amplitude greater than the signal in track. If an OOB signal is found, the confidence count is decremented. If the confidence count is less than one second, the confidence flag is set if it reaches zero, the track is dropped and a new track started at the position of the OOB signal.

The frame count is incremented on each successful angle measurement and decremented on each measurement failure. Failures may be caused by insufficient signal amplitude or too narrow a dwell gate. The frame count is also decremented by a missed scan count (failure to decode an identity within a specified period) or if the measured angle departs from the previous average by more than 1.28° (0.64° outlier limit in flare). An outlier of 1.28° was selected to prevent an overflow in the α, β filter computations. The frame flag is set if the count drops to two seconds and the track is dropped if the count falls to zero. The processor then reverts to acquisition mode.

Out-of-coverage (sidelobe suppression) pulses are counted separately when their amplitude reaches that of the signal in track. If the out-of-coverage count reaches three seconds, the frame is skipped and the frame count is decremented. This action is repeated each frame until the out-of-coverage count falls below three seconds or the track is dropped.

3.3 Program Operating Times

The software operating times in the LSI-11 microprocessor for the four processing modes are listed in Table 3.1.

Table 3.1 LSI-11 OPERATING TIMES

	Processor Only (Milliseconds)	All Proc. to Tape Output (Milliseconds)	Proc. to Tape Output, DGP to 4 Chart Rec. Channels (Milliseconds)
DGP	5.5	6.5	7
DGP + SEP	8	10	11
DGP + SEP/DGP	10.5	13.5	14
DGP + SEP/DEP + SPGP	12.5	16	17
DGP + SPGP	7.5	9.5	10

(Times from start of processing to end of display)

Notes: Elevation only, no multipath

3.4 The Need for a Dual Edge Processor

Simulation test results with the Single Edge Processor (SEP) show that the effect of multipath can be greatly reduced by making time measurements from that side of the beam opposite to the multipath. In elevation, multipath almost always perturbs the beam when it is pointing below the aircraft. Since the scan is down and then up, the SEP can be restricted to the outside beam edges with small chance that they will be perturbed, and with a significant error reduction.

The Dual Edge Processor (DEP) uses an SEP technique on each side of the beam and averages the two angles. If one beam edge is perturbed by multipath, the DEP switches to an SEP mode on the opposite edge until the multipath disappears. There are several disadvantages of the DEP, listed as follows:

1) The DEP program is over twice as large as the SEP program.

2) The DEP operating time is nearly twice as long as that for the SEP.

3) The multipath detection and edge selection algorithm is difficult to design for all significant multipath levels and separation angles. A fool-proof algorithm has not yet been devised.

4) If the selection algorithm is fooled, errors can be greater than those of a simple dwell gate or split gate processor.

The advantages of the DEP must out-weigh these disadvantages if it is to be utilized. The principal advantages over the SEP are as follows:

1) The DEP measurement is unbiased since it makes a symmetrical measurement on each side of the beam. The SEP requires a second, unbiased processor (dwell gate or split gate, for example) from which to derive a beamwidth or bias correction. Thus the DEP can operate alone. Unfortunately, the DEP, like the SEP, requires a 15 to 20 dB greater signal for acquisition than do the dwell gate or split gate processors. Therefore, the alternate processor is always needed for acquisition. It can be dispensed with when the DEP is in use at higher signal levels whereas it is needed with the SEP to accommodate possible beamwidth variations. This may be important when computer operating time is marginal.

2) The DEP, when properly implemented, can greatly reduce multipath errors regardless of which side of the beam they fall on. Azimuth curved approaches can result in multipath on either beam edge so the DEP would be useful. In elevation, there is a possibility of multipath on the lower side of the beam from hangar roofs. The DEP would reduce the errors in this case, so long as the other beam edge is clear.

3) The DEP is insensitive to receiver non-linearities. As the signal level changes, the logarithmic amplifier will distort the beam to a degree depending on the linearity of its gain curve. Since both beam edges are distorted symmetrically, the DEP angle is not affected by signal level. The SEP, in contrast, is perturbed a few hundredths of a degree by signal level changes with a logarithmic amplifier of good (±1 dB) linearity.

4) The effect of shadowing by obstacles in the path of the beam is different than that of multipath. Often one edge of the beam will be shadowed before or after the other so that one edge may be relatively free from distortion. With the proper algorithm, the DEP should be capable of using the best information available to produce a low error signal. This capability remains to be demonstrated.

Consideration of these points indicates that the DEP is marginally better than the SEP at its present stage of development. Unless a case can be made for serious multipath of the type that requires the DEP, operation with the SEP should be adequate. However, the DEP advantages in being unbiased and not affected by receiver non-linearities are great enough to make further development effort desirable. This effort is required to: 1) Improve the multipath detection/edge selection algorithm, 2) Reduce the program size and running time, and 3) Lower the required acquisition signal amplitude. A new approach to the whole DEP/SEP concept may be necessary to achieve the desired objectives.

Section 4.0
SIMULATION RESULTS

A series of tests were carried out on the multimode digital processor to measure the low signal level performance and multipath error characteristics of the four operating modes. The processor tests were performed with a Calspan breadboard log video receiver.

During a test the receiver video data is digitized in the processor and stored in computer memory for subsequent processing by the four algorithms or operating modes. In the LSI-11 the processor stores the digitized data on the two beam scans and can process as many as four different modes if only azimuth or elevation data are being recorded.

The algorithms were developed with the PDP-11/10 computer so that most of the simulation tests were done with the PDP-11. The software was then modified to fit into the LSI-11 microprocessor that could be packaged conveniently for field and flight tests. Only a limited number of simulation tests were conducted on the LSI-11 processor to verify the software operation and to show that performance of the two processors is similar. All the data presented in this report were taken with the PDP-11 processor unless labeled LSI-11 processor.

4.1 Description of Tests

Multipath error characteristics are measured over a 10 second test period with a multipath signal at a constant amplitude and 0.8 Hz scalloping frequency (frequency near 0 dB gain of elevation α,β filter). These tests are referred to as baseline tests in this and previous reports. Tests are run at different multipath separation angles. Rms and mean errors are computed near the 10 second test period and plotted versus separation angle. Peak-to-peak errors are typically three times the rms error.

A limited number of tests have been run with a 1/16 Hz scalloping frequency to measure the peak errors at multipath phases of 0° and 180°. Peak errors are plotted as a function of separation angle.

A few tests have been run with a multipath scenario that represents an approaching aircraft flying through the interference region resulting from hangar multipath reflections. Tests were run with the scenario from J.F. Kennedy Airport that was used by the AWOP assessment group.

In addition to multipath effects the low signal level performance was evaluated. Ten second test periods were used for the error statistics but no multipath signals were present. These tests evaluate the acquisition characteristics of the algorithm. Tests run at different signal levels show the noise in the processor algorithms.

4.2 Processor Characteristics

Frequency response curves were run with the LSI-11 processor. The amplitude and phase responses were found to be similar to those measured for the phase 3 receivers as reported in Reference 1. Response curves of the elevation channel are shown in Figure 4-1.

Figure 4-2 shows time history recordings of the noise in the four processing modes at a high signal level. The noise levels are extremely low. A similar recording is shown for the phase 3 receiver in Figure 4-3. The data quantization used in the phase 3 processor is larger than the 0.0025° used in the digital processor. Additional recordings are shown in Figure 4-4 for the dwell gate, single edge and dual edge processors at a lower signal level. The SEP as would be expected has the largest processing noise. Figure 4-5 shows the lower processing noise in the split gate mode compared to the dwell gate processor. Five data points (N = 5) on each side of the "peak" amplitude were used in computing the beam centroid and resulted in reduced processing noise relative to the dwell gate technique.

4.2.1 Split Gate Parameters

The effect of using a different number of points in the split gate processor for computing the beam centroid is illustrated in Figure 4-6. Rms errors are plotted versus peak signal levels for N = 1 and N-5. A similar curve is included for the dwell gate processor for comparison. These curves were run

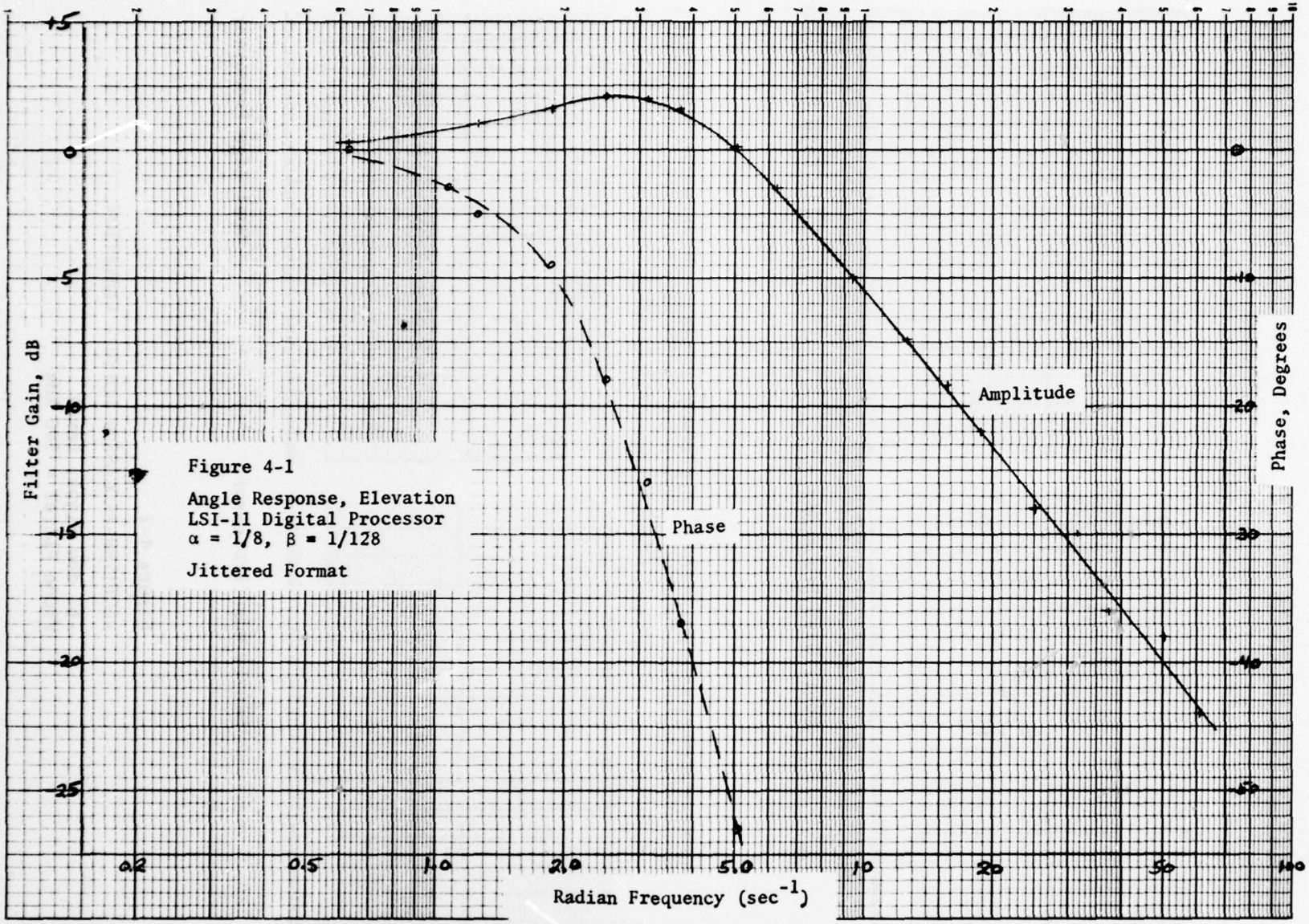
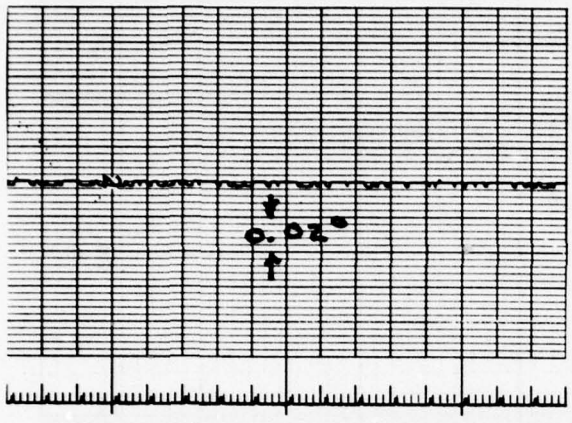


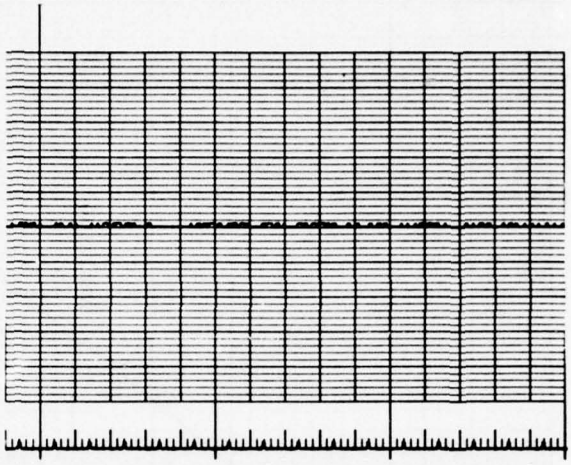
Figure 4-1

Angle Response, Elevation
LSI-11 Digital Processor
$\alpha = 1/8$, $\beta = 1/128$

Jittered Format

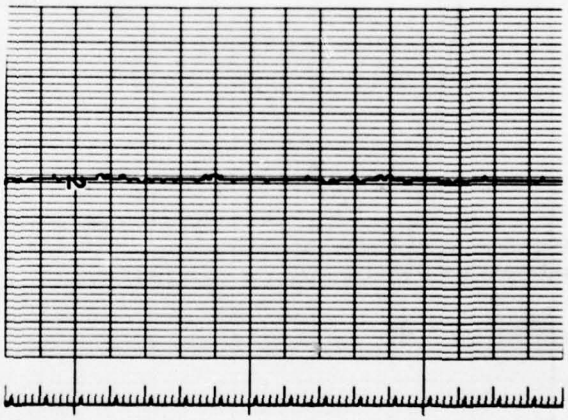


Dwell Gate Processor



Split Gate Processor

Single Edge Processor

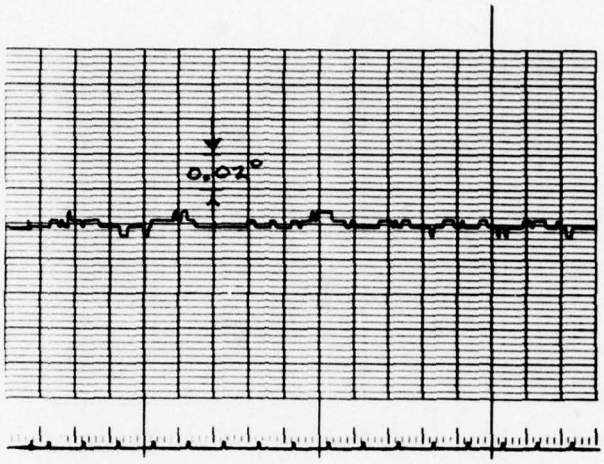


Dual Edge Processor

Figure 4-2

RECEIVER-PROCESSOR NOISE - ELEVATION

-65 dBm Signal Level
Video Filter = 300 kHz

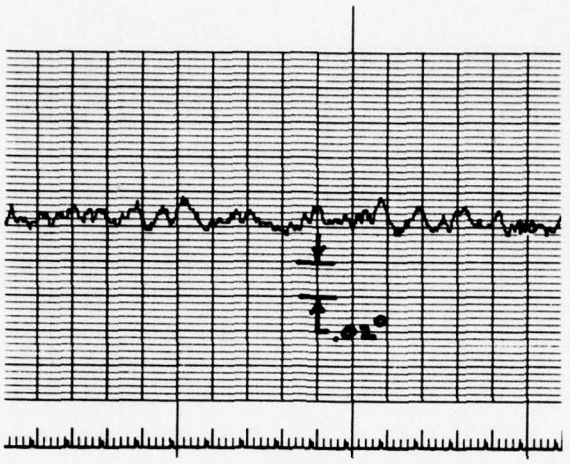


Azimuth - Centerline

Elevation - 3° Glide Slope

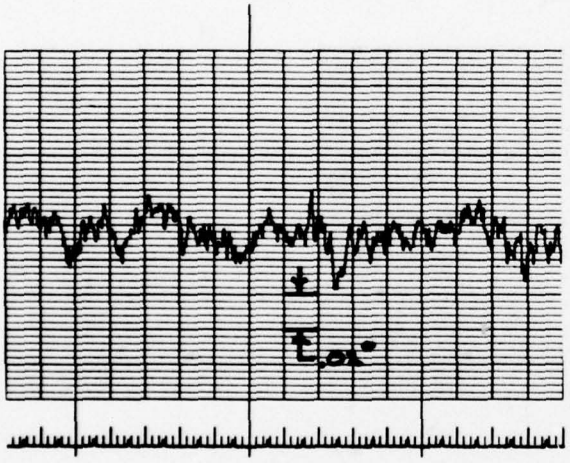
Figure 4-3
Error Time Histories

Receiver P101 (Modified to Reduce Processor Noise)
Approximate Signal Level -70 dBm



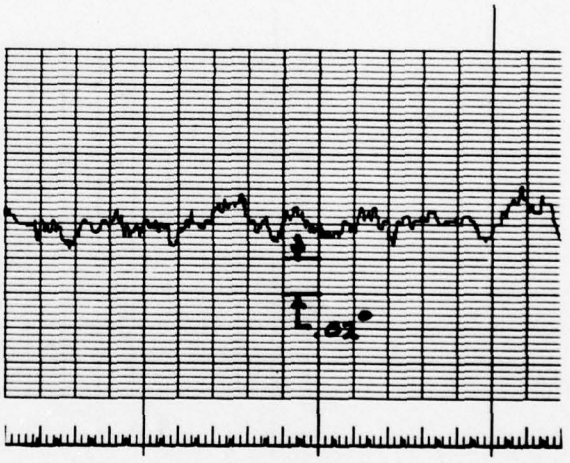
Dwell Gate Processor

σ = 0.004
m = +0.001



Single Edge Processor (SEP)

σ = 0.009
m = +0.009



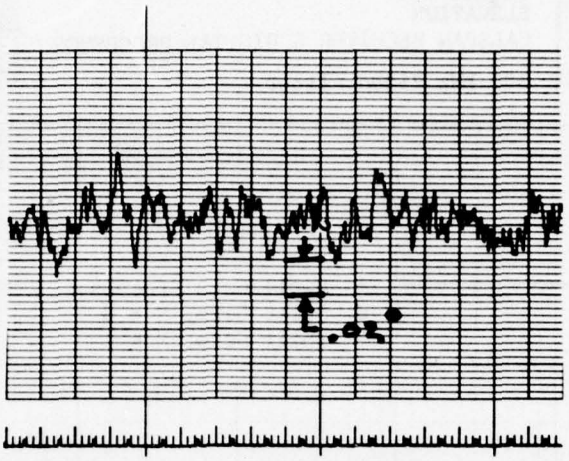
Dual Edge Processor

σ = 0.006
m = +0.003

Figure 4-4

RECEIVER-PROCESSOR NOISE - ELEVATION

-87 dBm Signal Level
Video Filter = 300 kHz



Dwell Gate Processor

σ = 0.011
m = -0.002

Split Gate Processor, N = 5

σ = 0.006
m = +0.001

Figure 4-5

RECEIVER-PROCESSOR NOISE - ELEVATION

-97 dBm Signal Level
Video Filter = 300 kHz

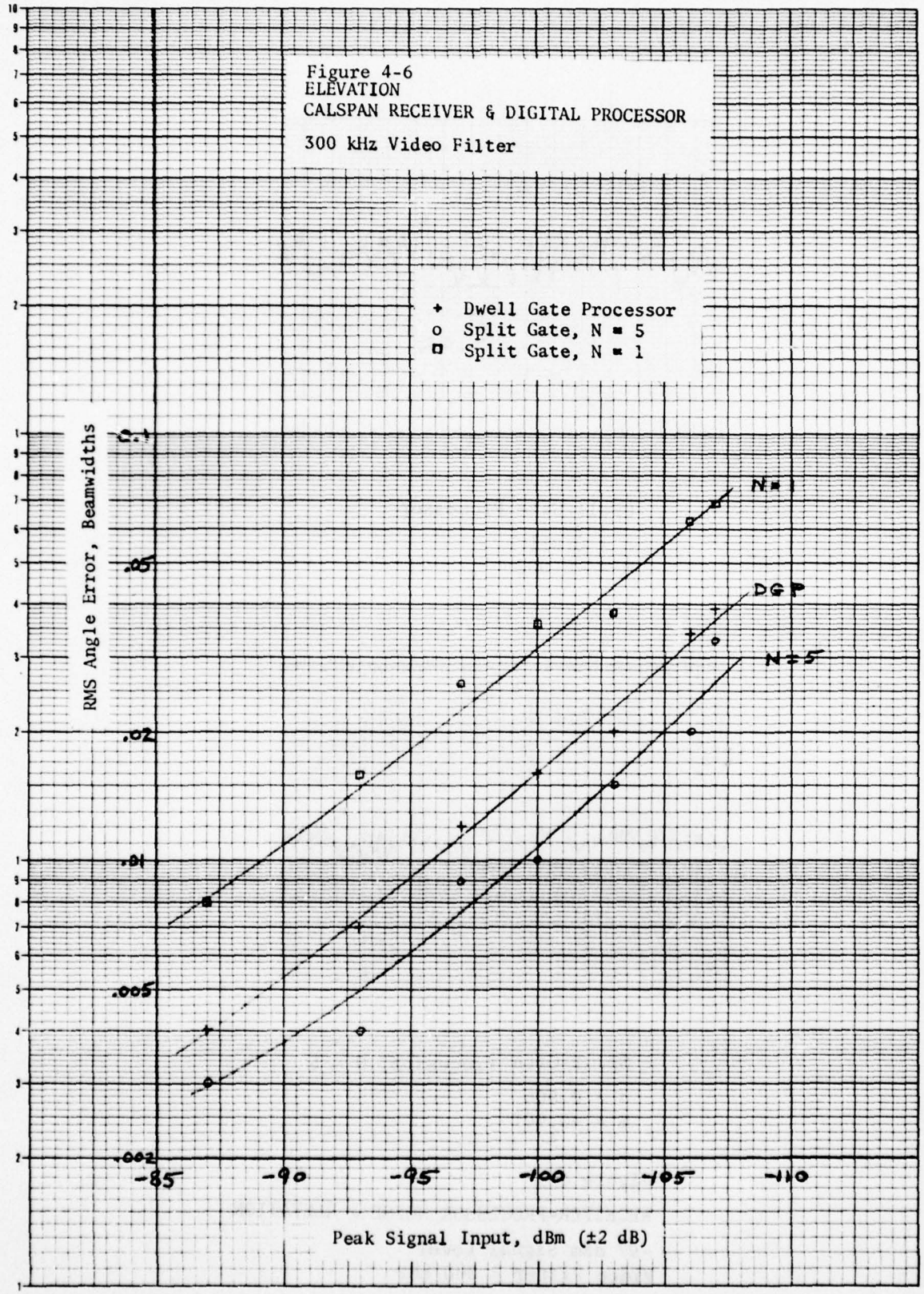


Figure 4-6
ELEVATION
CALSPAN RECEIVER & DIGITAL PROCESSOR
300 kHz Video Filter
+ Dwell Gate Processor
o Split Gate, N = 5
□ Split Gate, N = 1
RMS Angle Error, Beamwidths
.1
.05
.02
.01
.005
.002
N=1
DGP
N=5
-85
-90
-95
-100
-105
-110
Peak Signal Input, dBm (±2 dB)

with a filter cutoff frequency of 300 kHz used on the log IF video data. Figures 4-7 and 4-8 illustrate the reduction in the rms error for filter cutoff frequencies of 50 kHz and 26 kHz.*

The effect of the number of points (N) used in the split gate processor when high level multipath is present is shown in Figures 4-9 and 4-10. The mean error, rms and peak errors are plotted versus N for a -1 dB multipath baseline test. From the curves in Figures 4-9 and 4-10 it is seen that for N = 4 the increase in the multipath rms errors is relatively small compared to N = 1 which minimizes the mean multipath error.

Four data points (N = 4) were used in the LSI-11 processing algorithms. This number represents a good compromise between minimizing the rms processing error, multipath errors and for operation with a wide range of beamwidths.

4.2.2 Video Filter Bandwidth Effects

The bandwidth effects of the video filter are illustrated in Figure 4-11 in which rms noise error versus signal level is plotted for the dwell gate processor for 300 kHz, 50 kHz, and 26 kHz filter cutoff frequencies. Multipath errors versus video filter bandwidth are shown in Figure 4-12. From the data shown in these two figures it is apparent that filter bandwidth selection is a compromise between minimizing the noise error and multipath errors. A 50 kHz video cutoff represents a good compromise for this R-C filter characteristic. Two noise error curves are presented in Figures 4-13 and 4-14 for elevation and azimuth data with a 50 kHz cutoff. These data were taken with the LSI-11 processor for the dual mode split gate and dwell gate algorithms. For the parameters selected, 50 kHz video filter cutoff and N = 4, there is very little difference between the noise errors with these two algorithms.

4.2.3 Quantization Effects

The implementation of the digital processor used a 12-bit analog-to-digital converter (ADC) for digitizing the log video signal from the receiver.

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*One section of a Krohn-Hite model 3202 variable filter was used in the R-C mode. The attenuation at the cutoff frequency in this mode is 13 dB and the 3 dB attenuation point is 0.4 times the cutoff frequency. The attenuation at high frequencies falls off at 24 dB/octave.

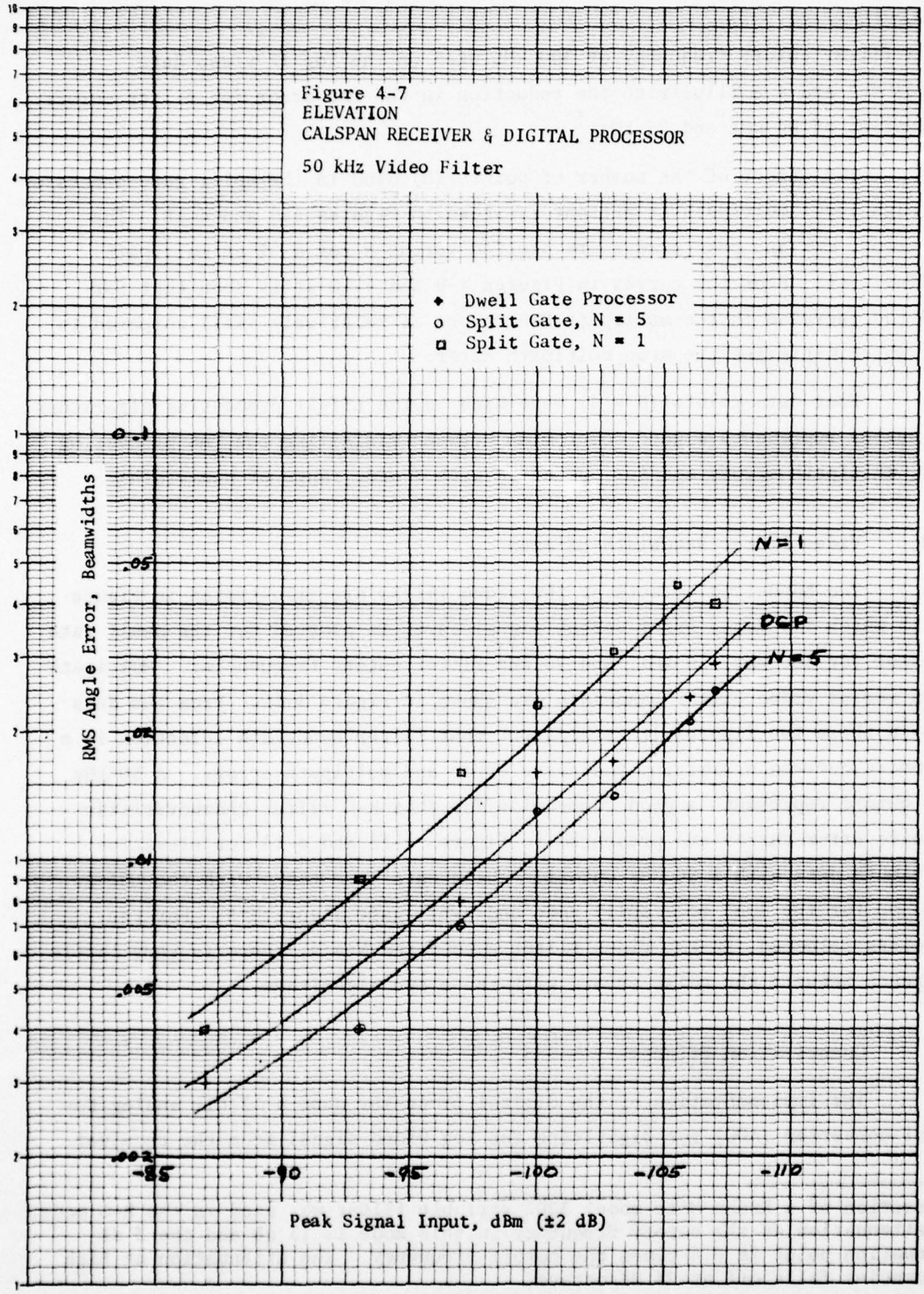


Figure 4-7
ELEVATION
CALSPAN RECEIVER & DIGITAL PROCESSOR
50 kHz Video Filter
◆ Dwell Gate Processor
o Split Gate, N = 5
□ Split Gate, N = 1
RMS Angle Error, Beamwidths
.1
.05
.02
.01
.005
.002
N = 1
DGP
N = 5
-85
-90
-95
-100
-105
-110
Peak Signal Input, dBm (±2 dB)

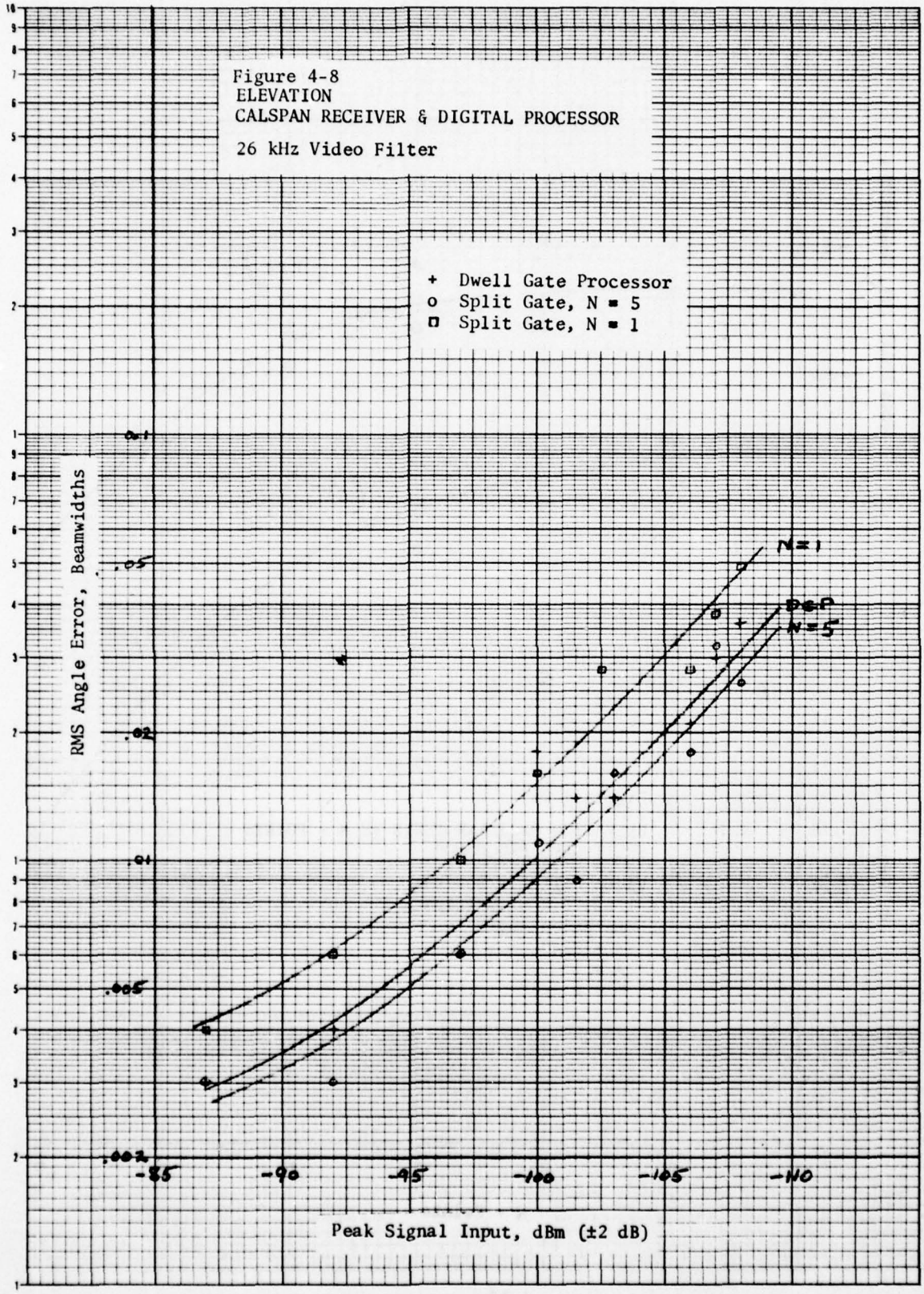


Figure 4-8
ELEVATION
CALSPAN RECEIVER & DIGITAL PROCESSOR
26 kHz Video Filter
+ Dwell Gate Processor
o Split Gate, N = 5
□ Split Gate, N = 1
RMS Angle Error, Beamwidths
.1
.05
.02
.01
.005
.002
N=1
N=5
-85
-90
-95
-100
-105
-110
Peak Signal Input, dBm (±2 dB)

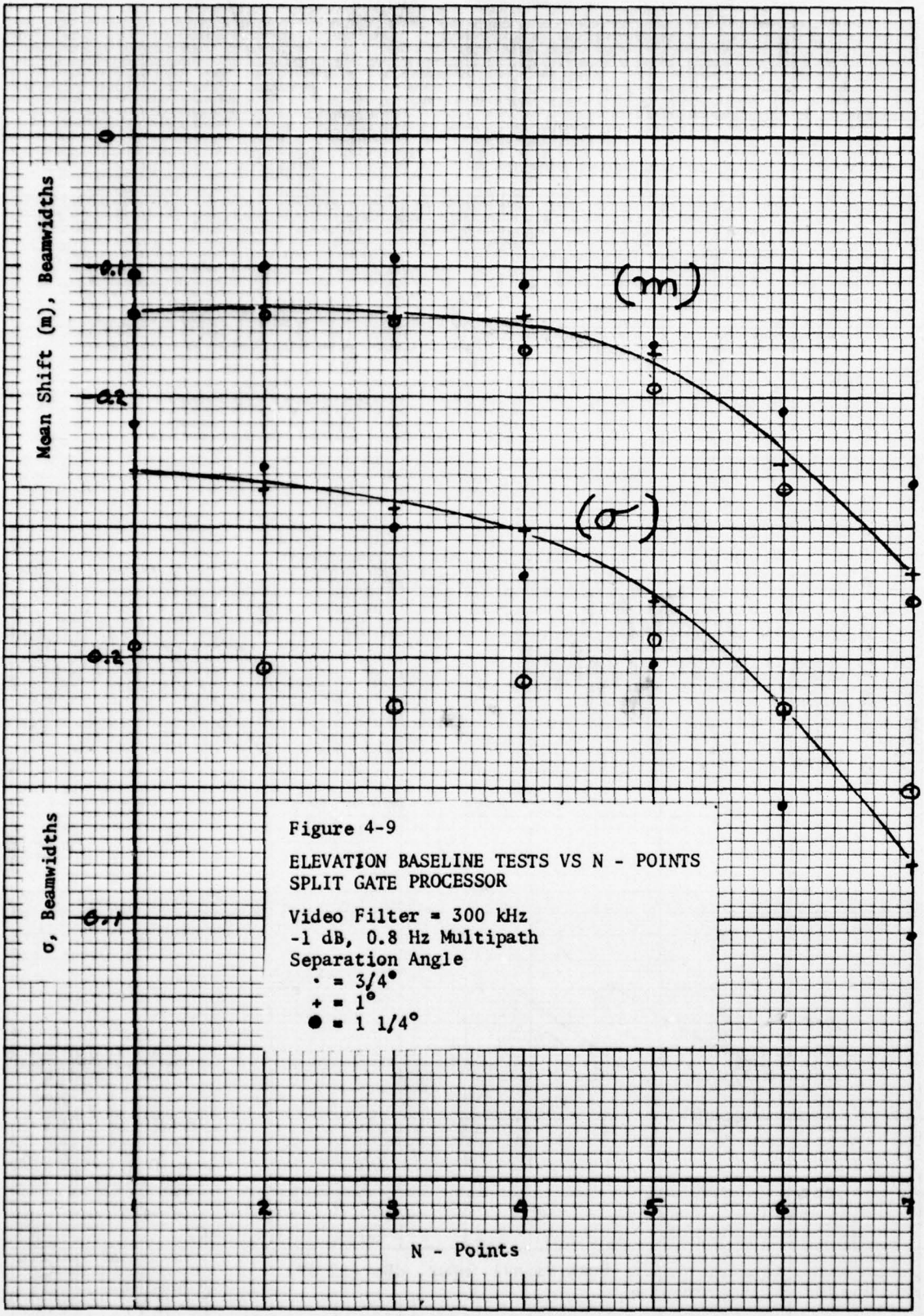


Figure 4-9

ELEVATION BASELINE TESTS VS N - POINTS
SPLIT GATE PROCESSOR

Video Filter = 300 kHz
-1 dB, 0.8 Hz Multipath
Separation Angle
· = 3/4°
+ = 1°
● = 1 1/4°

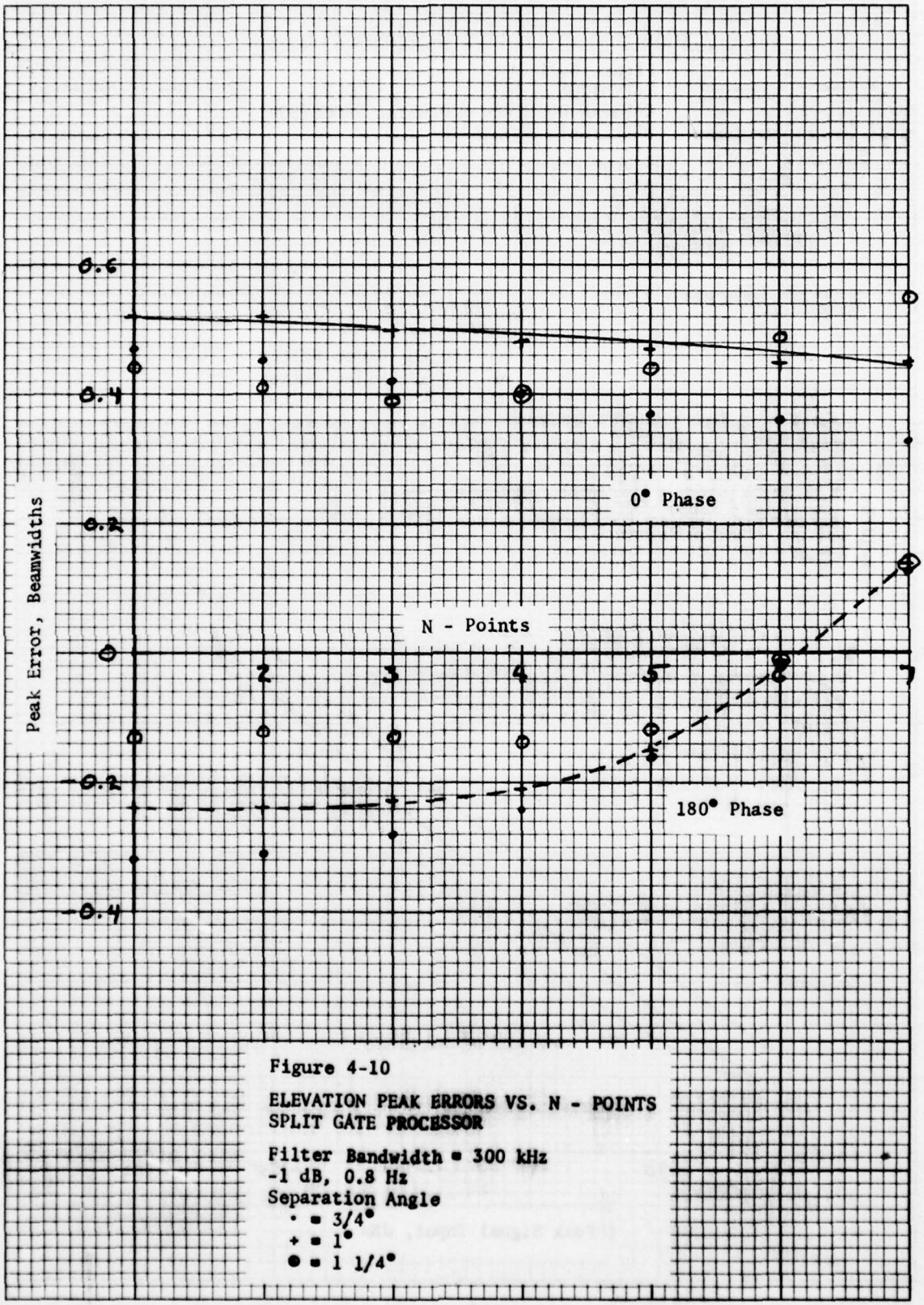


Figure 4-10

ELEVATION PEAK ERRORS VS. N - POINTS
SPLIT GATE PROCESSOR

Filter Bandwidth = 300 kHz
-1 dB, 0.8 Hz
Separation Angle
· = 3/4°
+ = 1°
● = 1 1/4°

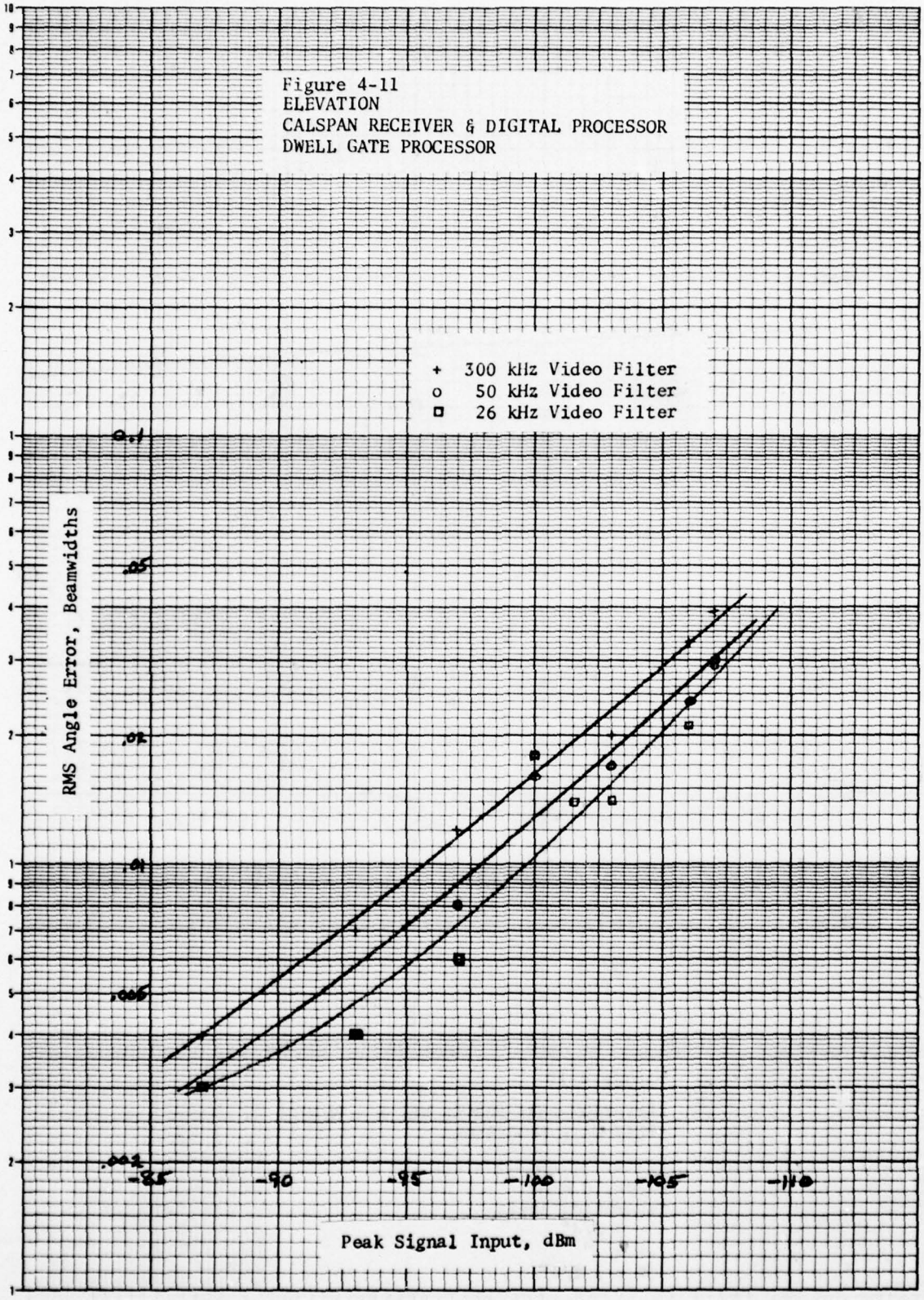


Figure 4-11
ELEVATION
CALSPAN RECEIVER & DIGITAL PROCESSOR
DWELL GATE PROCESSOR
+ 300 kHz Video Filter
o 50 kHz Video Filter
□ 26 kHz Video Filter
RMS Angle Error, Beamwidths
.1
.05
.02
.01
.005
.002
-85
-90
-95
-100
-105
-110
Peak Signal Input, dBm

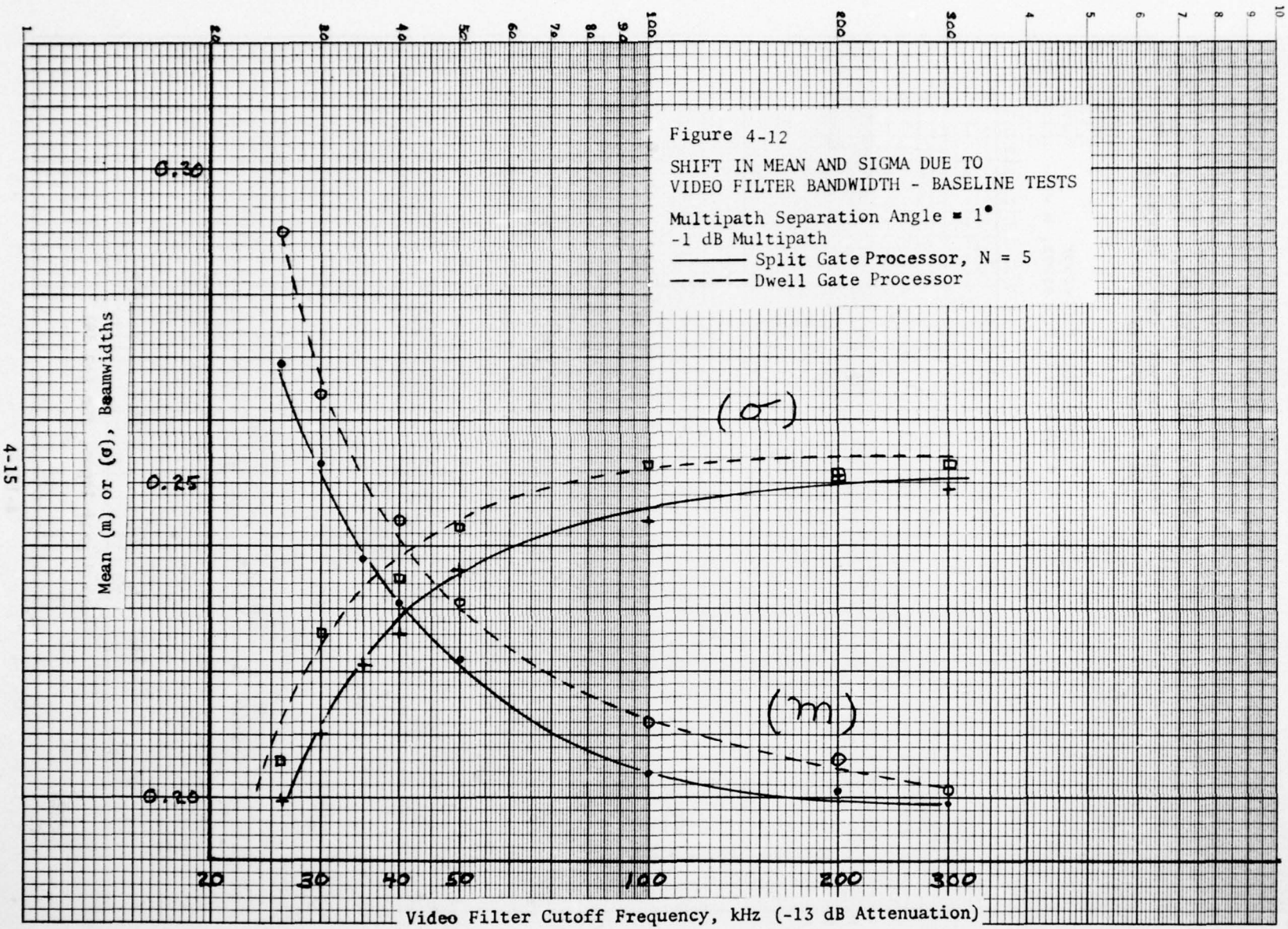


Figure 4-12

SHIFT IN MEAN AND SIGMA DUE TO
VIDEO FILTER BANDWIDTH - BASELINE TESTS

Multipath Separation Angle = 1°
-1 dB Multipath
——— Split Gate Processor, N = 5
– – – – Dwell Gate Processor

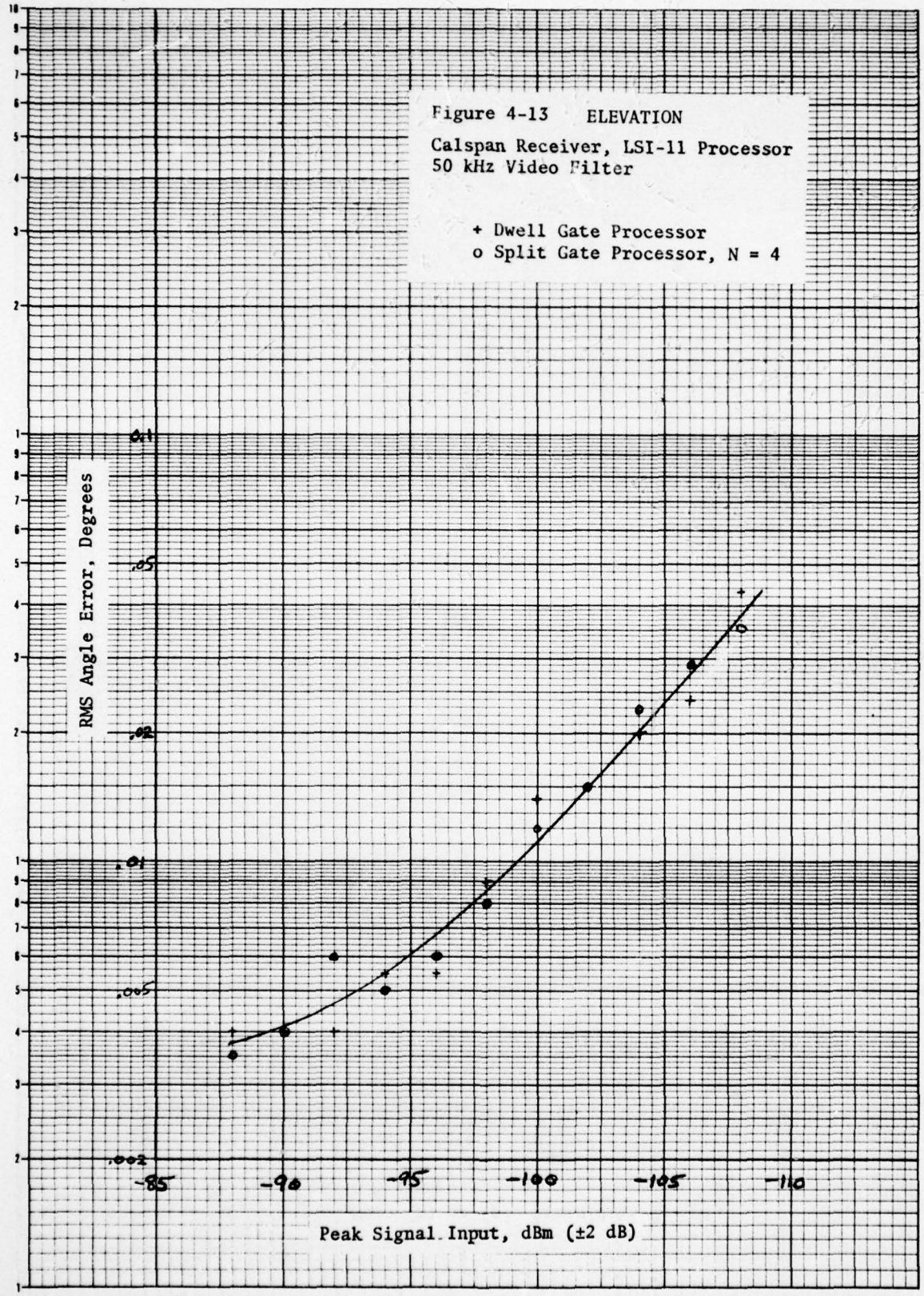


Figure 4-13 ELEVATION
Calspan Receiver, LSI-11 Processor
50 kHz Video Filter
+ Dwell Gate Processor
o Split Gate Processor, N = 4
RMS Angle Error, Degrees
.1
.05
.02
.01
.005
.002
-85
-90
-95
-100
-105
-110
Peak Signal Input, dBm (±2 dB)

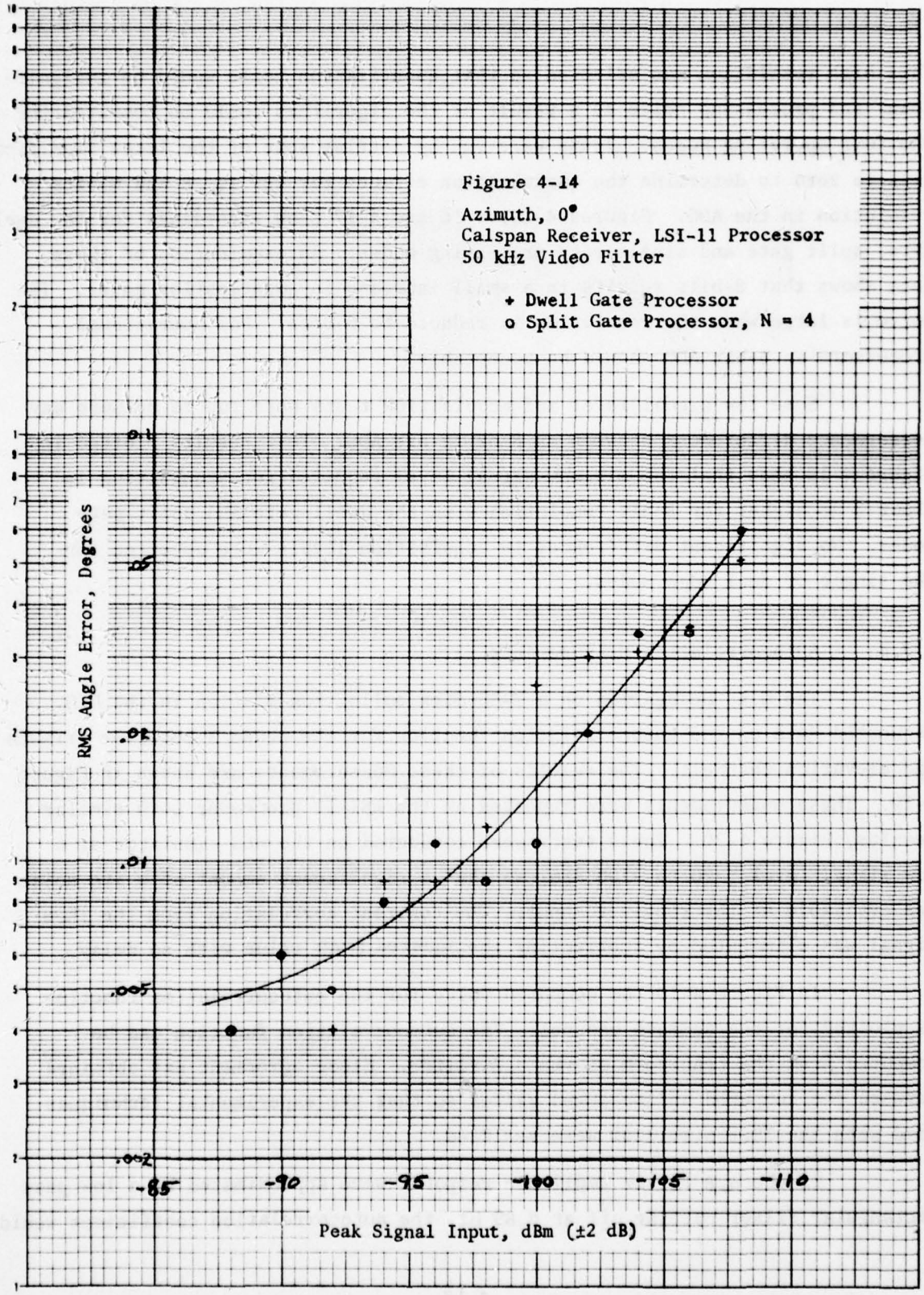


Figure 4-14
Azimuth, 0°
Calspan Receiver, LSI-11 Processor
50 kHz Video Filter
+ Dwell Gate Processor
o Split Gate Processor, N = 4
RMS Angle Error, Degrees
.1
.05
.02
.01
.005
.002
-85
-90
-95
-100
-105
-110
Peak Signal Input, dBm (±2 dB)

This high resolution was selected so that quantization noise would be insignificant and processing noise as a result of the algorithms could be compared for the four operating modes. Tests were run by setting some of the least significant bits to zero to determine the quantization effects for 12, 10, 8 and 6-bits resolution in the ADC. Figures 4-15, 4-16 and 4-17 show recordings for the dwell gate, split gate and single edge processing modes. An examination of these data shows that 8-bits results in a small increase in quantization noise. The noise is large when the resolution is reduced to 6-bits. For operational processors an 8-bit ADC should be acceptable.

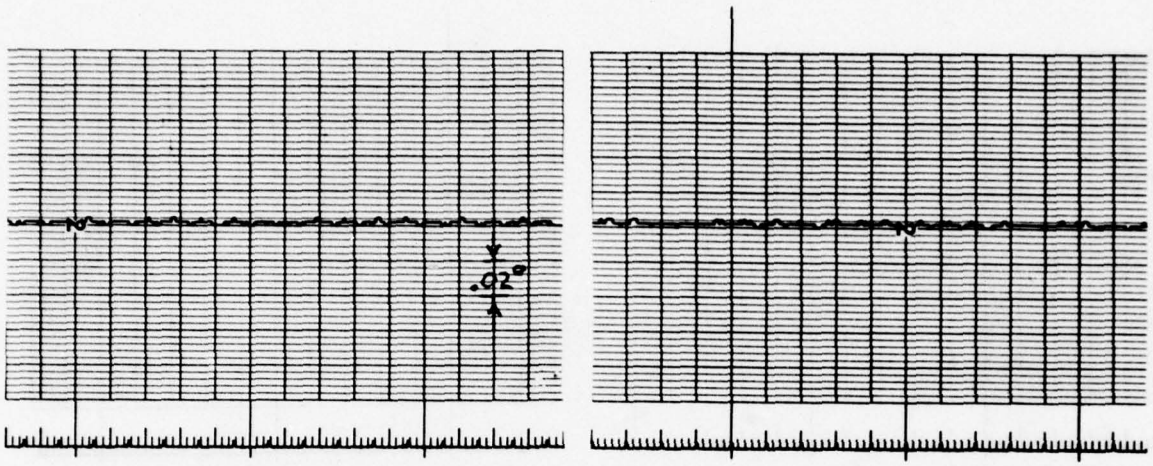
Some low signal level and acquisition tests were run to measure any performance differences between an 8 or 12-bit ADC. Test results plotted in Figure 4-18 show that the minimum signal level required for acquisition is about 2 dB higher for 8-bit resolution with the dwell gate and split gate modes. No significant differences in acquisition levels were detected for the single or dual edge modes.

4.2.4 Autocorrelation Measurements

The U.K. Delegation on a TRSB data collection mission in the U.S. requested data on the autocorrelation function for the phase 3 receiver azimuth and elevation channels. The results of these measurements are shown in Figure 4-19. These measurements were repeated on the LSI-11 processor with similar results, Figure 4-20. These tests were conducted on the MLS simulator at a low signal level (-90 to -100 dBm) so that a significant amount of white noise was available at the receiver input. The constant correlation from the TRSB signal was eliminated by subtracting the squared mean value with no delay.

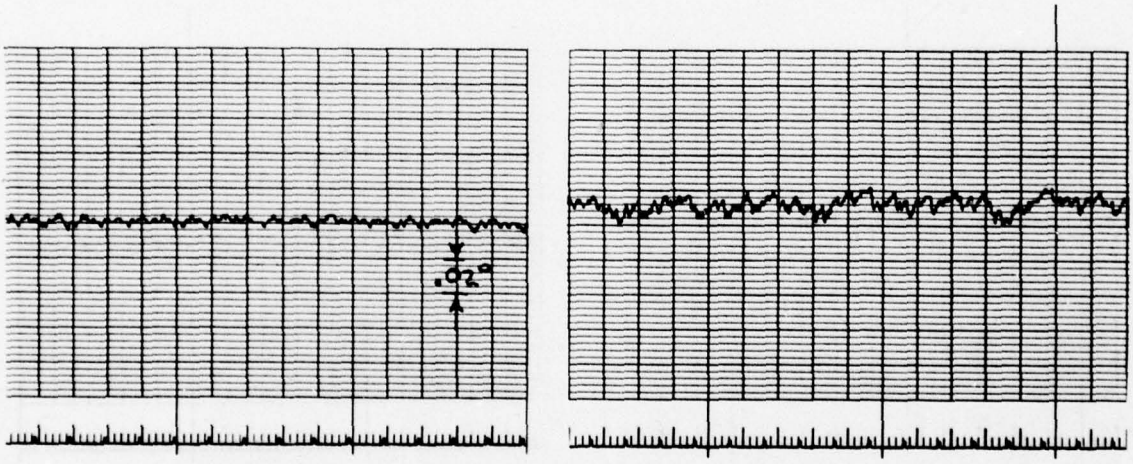
In Figure 4-19 the computed value for the autocorrelation function is plotted for the azimuth channel. The autocorrelation function can be computed from the transform of the α,β filter. Close agreement was obtained between the computed and measured values so that the experimental techniques used with the TRSB simulator were verified.

If the α,β filter amplitude response were approximated by a low pass rectangular filter cutting off at 0.89 Hz, the autocorrelation coefficient would



12 Bits

10 Bits

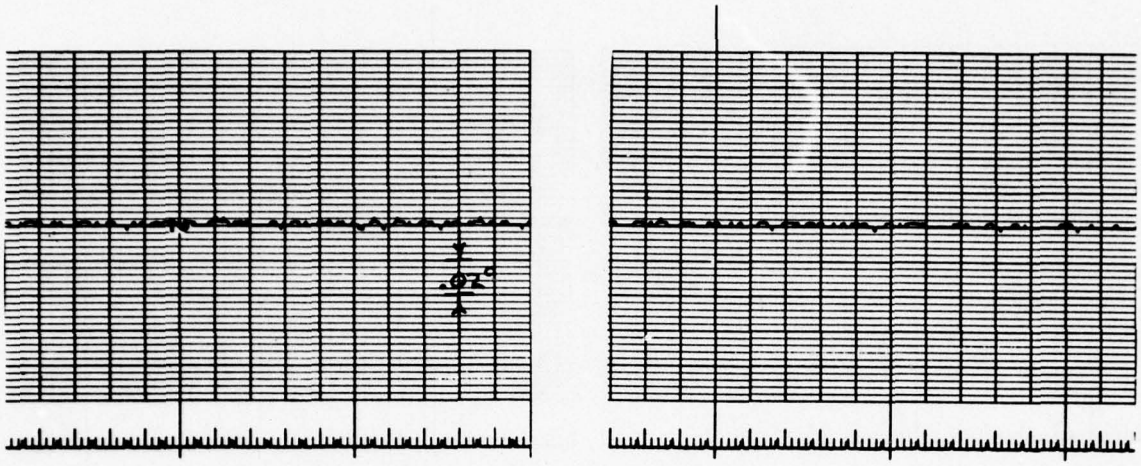


8 Bits

6 Bits

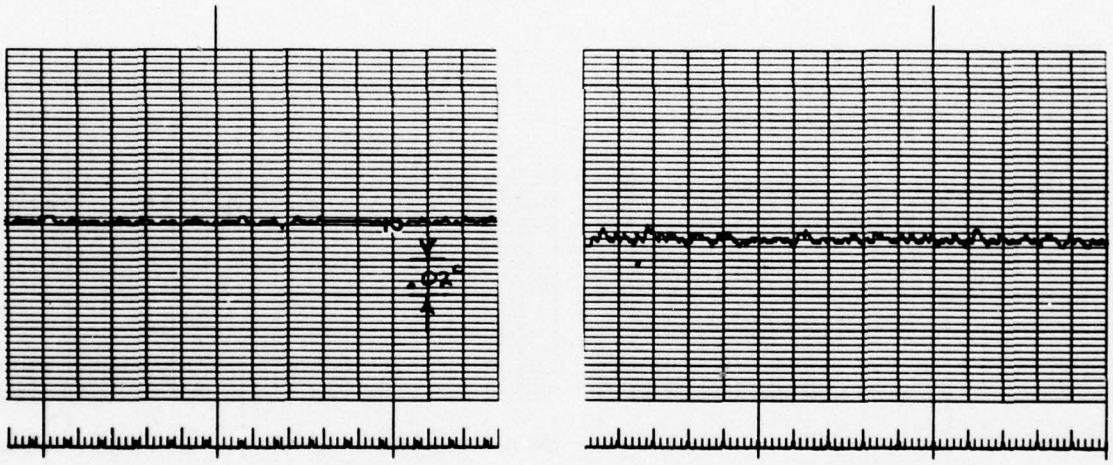
Figure 4-15 VIDEO SIGNAL QUANTIZATION EFFECTS ON DWELL GATE PROCESSOR (DGP)

-65 dBm Signal Level
No Multipath
Video Filter = 300K
Elevation Data



12 Bits

10 Bits

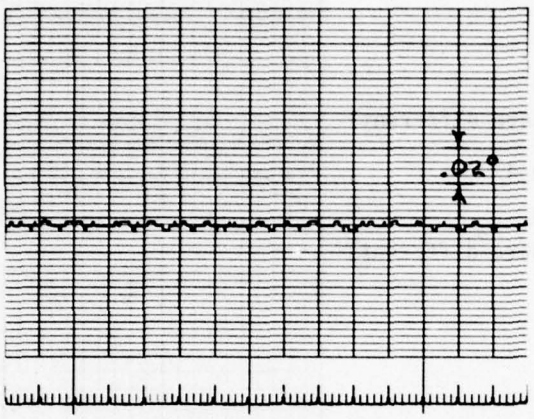


8 Bits

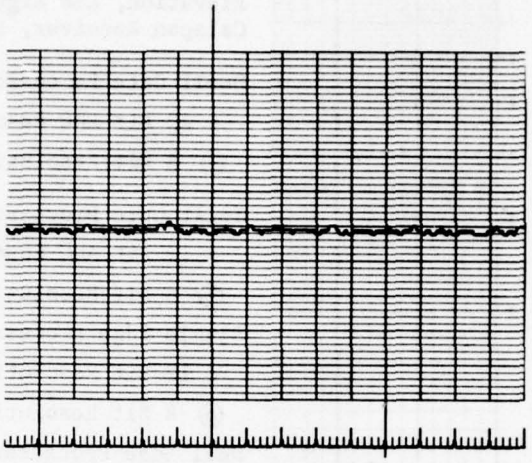
6 Bits

Figure 4-16 VIDEO SIGNAL QUANTIZATION
EFFECTS ON SPLIT GATE PROCESSOR (SPGP)

-65 dBm Signal Level
No Multipath
Video Filter = 300K
Elevation Data

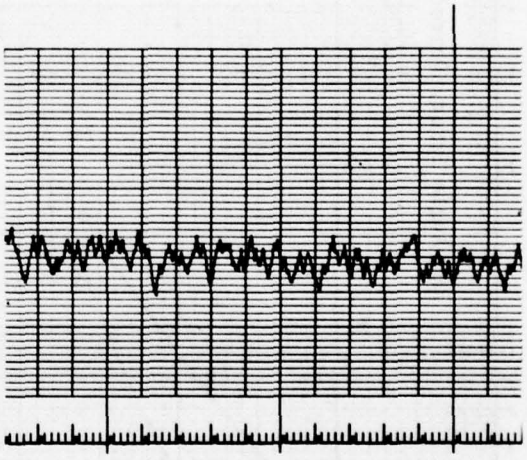


12 Bits



10 Bits

8 Bits



6 Bits

Figure 4-17 VIDEO SIGNAL QUANTIZATION
EFFECTS ON SINGLE EDGE PROCESSOR (SEP)

-65 dBm Signal Level
No MUltipath
Video Filter = 300K
Elevation Data

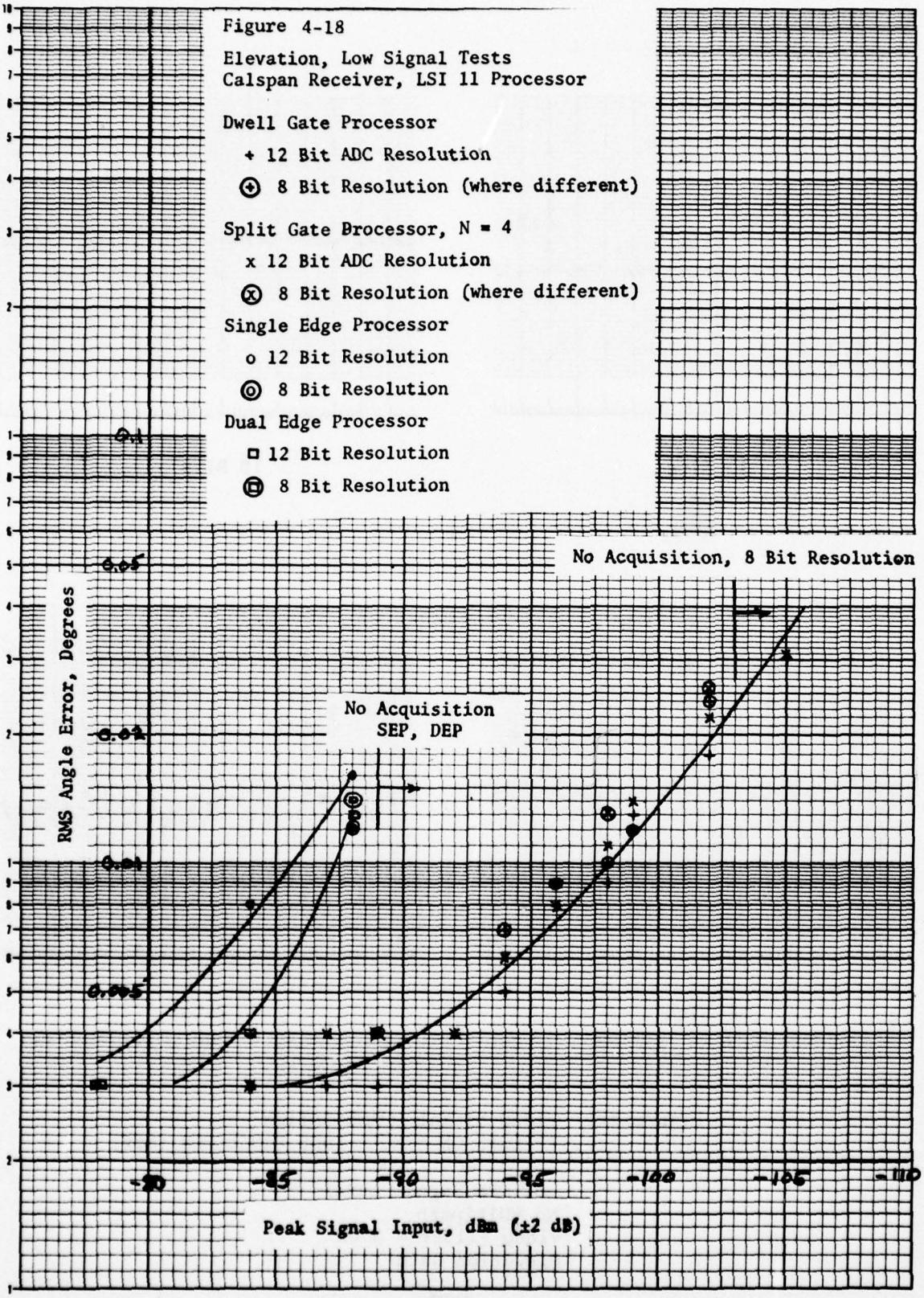


Figure 4-18
Elevation, Low Signal Tests
Calspan Receiver, LSI 11 Processor
Dwell Gate Processor
+ 12 Bit ADC Resolution
⊕ 8 Bit Resolution (where different)
Split Gate Processor, N = 4
x 12 Bit ADC Resolution
⊗ 8 Bit Resolution (where different)
Single Edge Processor
o 12 Bit Resolution
◎ 8 Bit Resolution
Dual Edge Processor
□ 12 Bit Resolution
⊡ 8 Bit Resolution
No Acquisition, 8 Bit Resolution
No Acquisition
SEP, DEP
RMS Angle Error, Degrees
0.1
0.05
0.02
0.01
0.005
-80
-85
-90
-95
-100
-105
-110
Peak Signal Input, dBm (±2 dB)

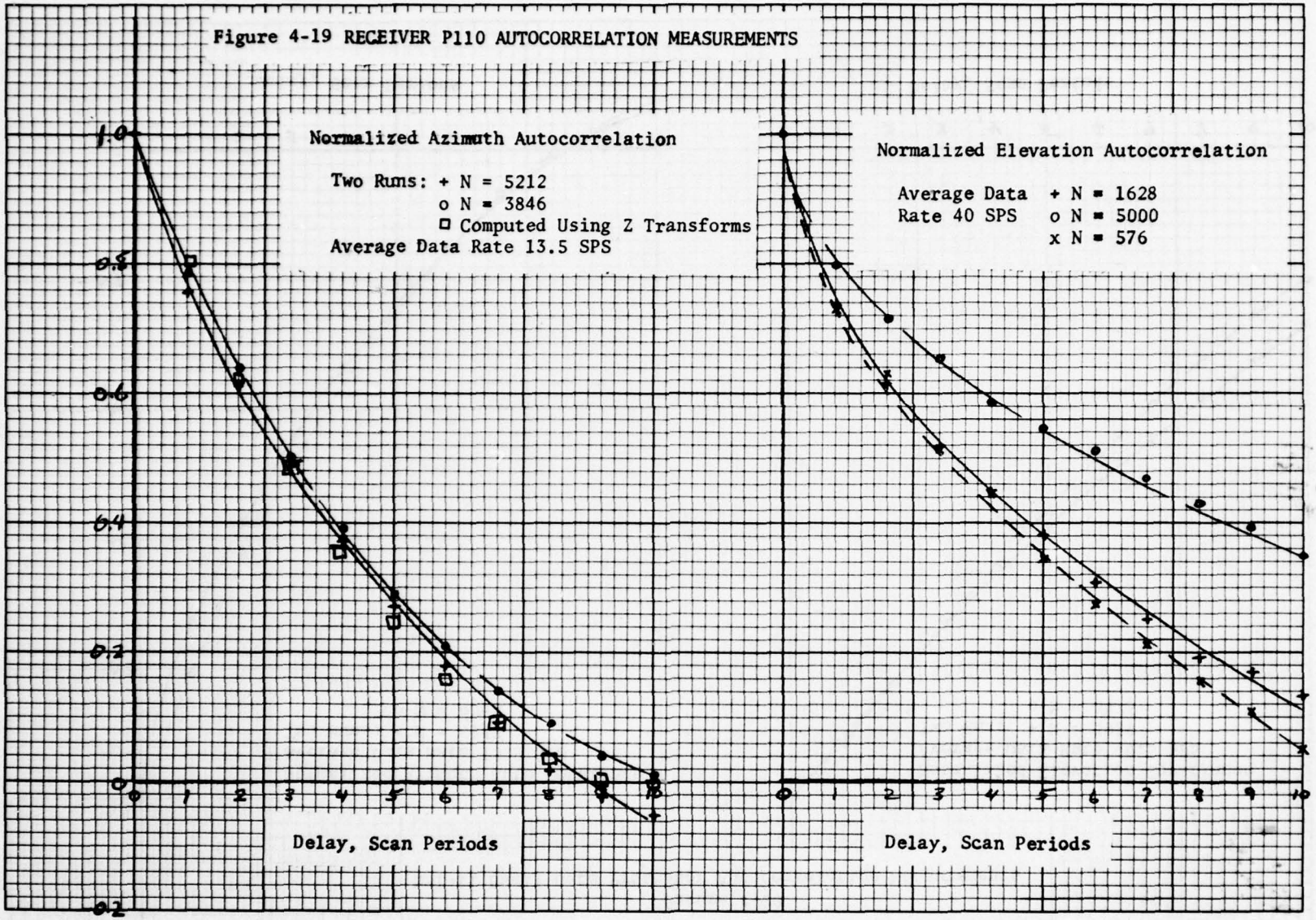
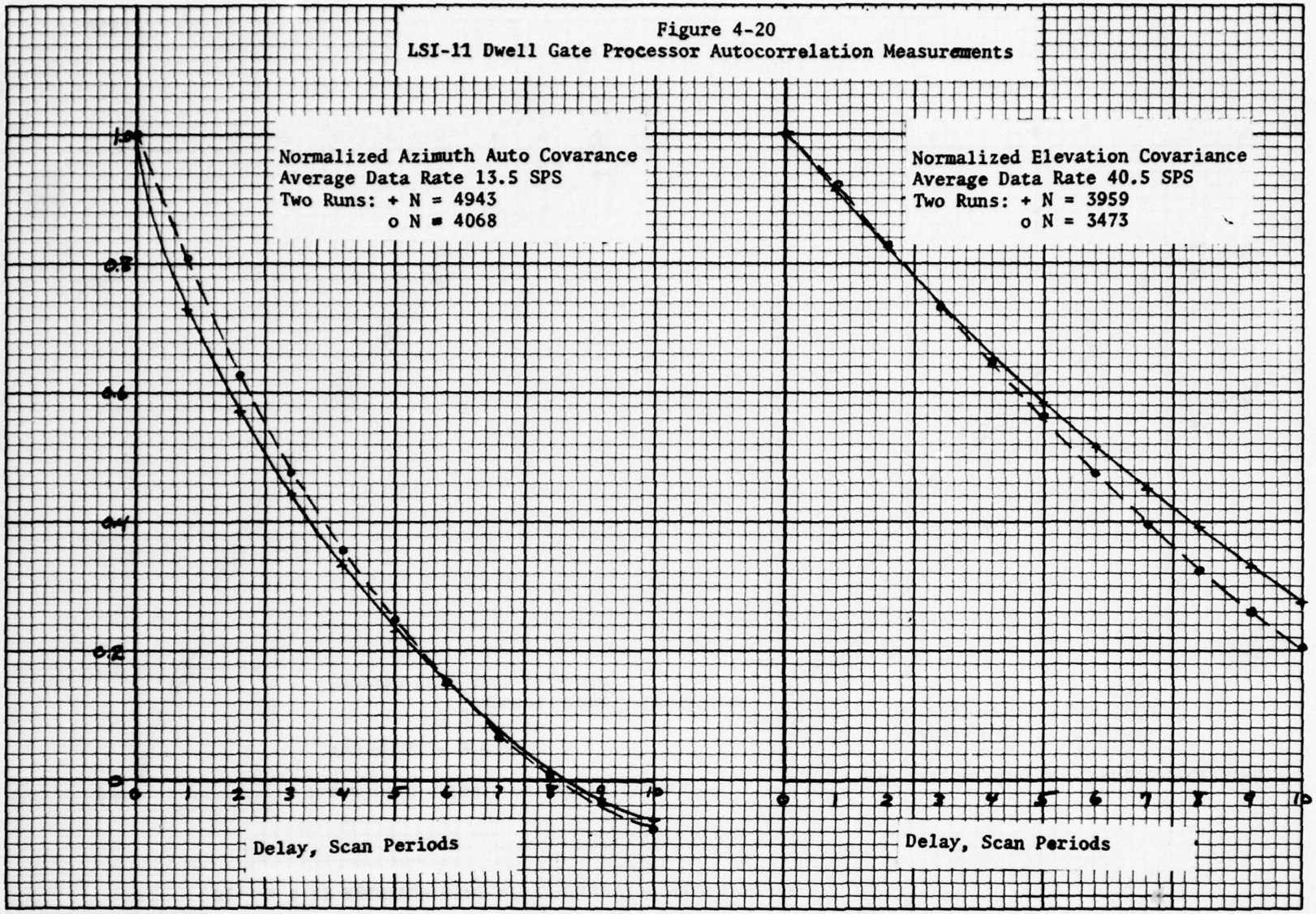


Figure 4-19 RECEIVER P110 AUTOCORRELATION MEASUREMENTS
Normalized Azimuth Autocorrelation
Two Runs: + N = 5212
o N = 3846
□ Computed Using Z Transforms
Average Data Rate 13.5 SPS
Normalized Elevation Autocorrelation
Average Data + N = 1628
Rate 40 SPS o N = 5000
x N = 576
1.0
0.8
0.6
0.4
0.2
0
-0.2
0 1 2 3 4 5 6 7 8 9 10
Delay, Scan Periods
Delay, Scan Periods

Figure 4-20
LSI-11 Dwell Gate Processor Autocorrelation Measurements



reach zero in 15 delays rather than 10 delays if the 1/bandwidth (Hz) approximation is used. The autocorrelation function is directly related to the filter characteristics.

The autocorrelation coefficient has not previously been used in the MLS receiver evaluations as it is difficult to measure and compute. The significance of autocorrelation measurements are not easy to evaluate compared to frequency response measurements resulting in amplitude and phase response curves.

4.3 Characteristics of Multipath Effects

Most of the data presented in this section are from baseline tests on the elevation channel. The baseline tests consisted of a ten second period of multipath at a constant amplitude and constant scalloping frequency of 0.8 Hz. Curves are plotted of the mean and rms errors versus multipath separation angle.

4.3.1 Dwell Gate and Split Gate Processors

As reported in Reference 1 the phase 3 dwell gate processor had large errors when multipath separation angles were between 1.0 and 1.5 degrees. Several techniques were tried with the algorithms in the digital processor to alleviate this characteristic. Figure 4-21 shows that if the tracking gate is offset 40 μsec the errors in this region, both mean and rms, are significantly reduced.

In most of the tests presented in this section the 1 deg/sec rate limiter included in the phase 3 receiver was not used. The limiter was included in the software and can be selected or deleted by a software change. It was easier to compare the performance of the processing algorithms without the limiter. The effects of the limiter are shown in Figure 4-22 for the dwell gate processor.

A comparison of the error characteristics between the dwell gate and split gate processors is shown in Figures 4-23 and 4-24 using the LSI-11 processor. The split gate processor significantly reduces both the mean and rms errors. Similar curves are presented for azimuth data in Figures 4-25 and 4-26. The amplitude of the azimuth rms error is reduced by the α,β filter that has a -2 dB gain at the 0.8 Hz scalloping frequency.

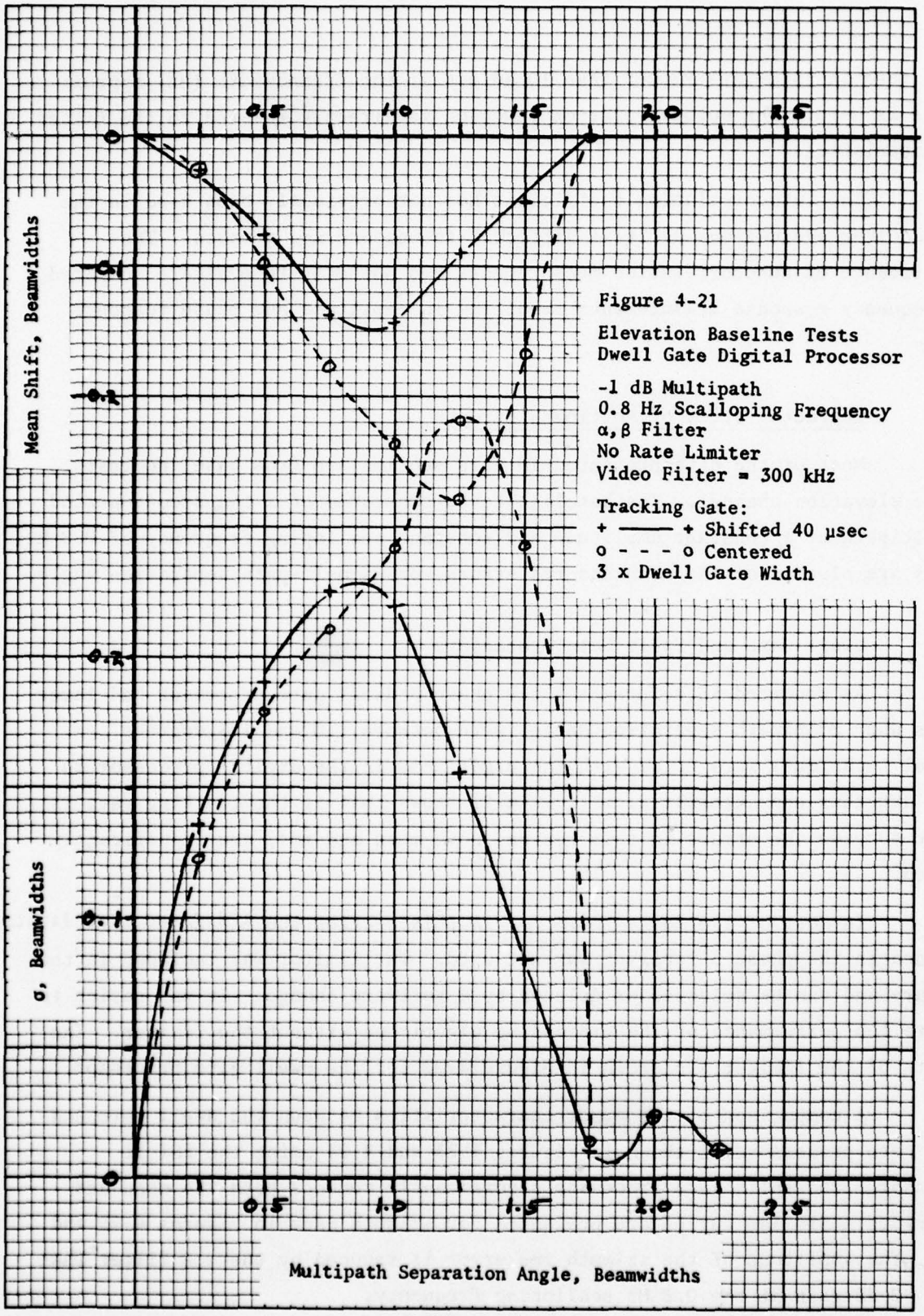


Figure 4-21

Elevation Baseline Tests
Dwell Gate Digital Processor

-1 dB Multipath
0.8 Hz Scalloping Frequency
α, β Filter
No Rate Limiter
Video Filter = 300 kHz

Tracking Gate:
+ ——— + Shifted 40 μsec
o - - - o Centered
3 x Dwell Gate Width

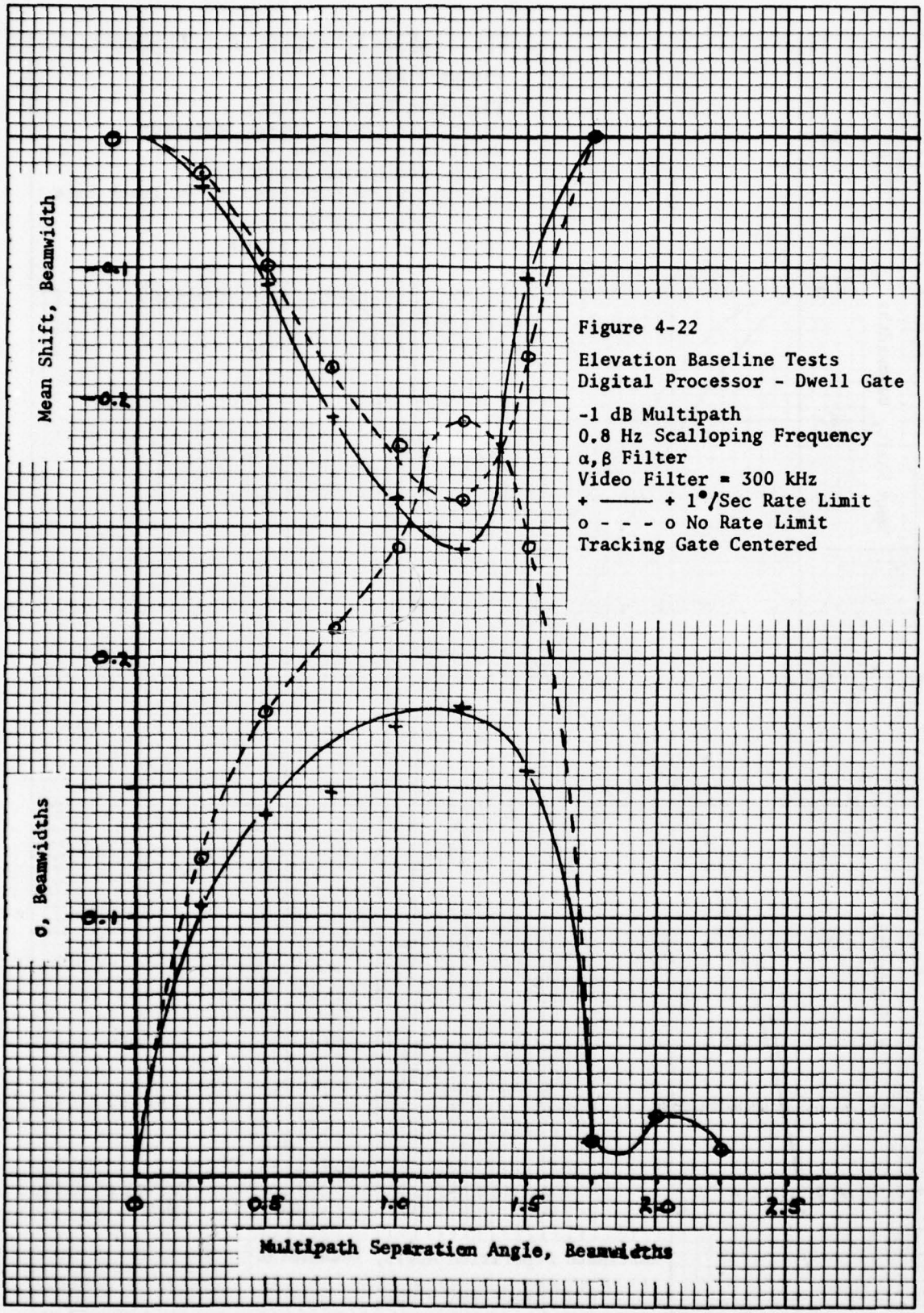


Figure 4-22

Elevation Baseline Tests
Digital Processor - Dwell Gate

-1 dB Multipath
0.8 Hz Scalloping Frequency
α, β Filter
Video Filter = 300 kHz
+ ——— + 1°/Sec Rate Limit
o - - - o No Rate Limit
Tracking Gate Centered

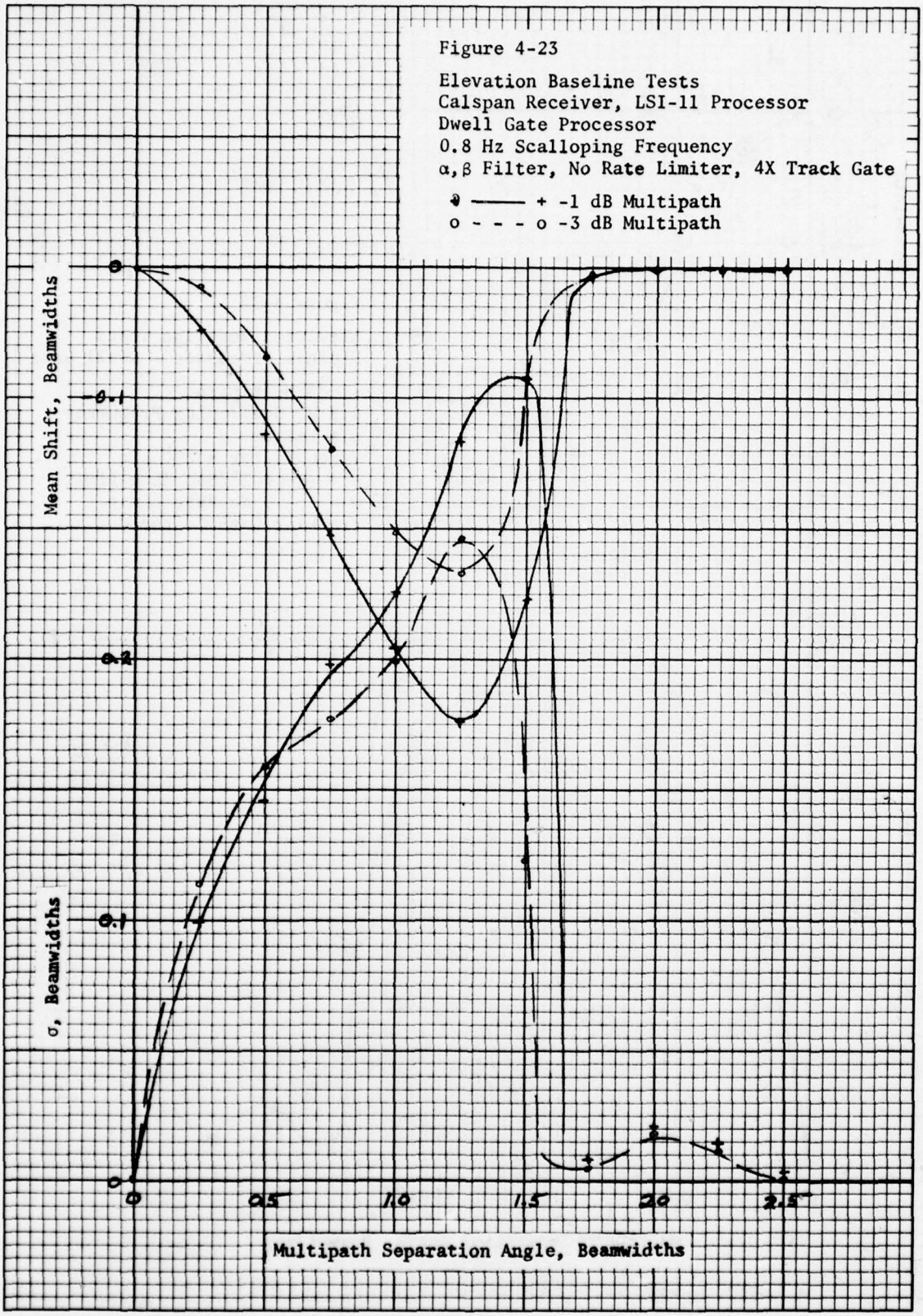


Figure 4-23
Elevation Baseline Tests
Calspan Receiver, LSI-11 Processor
Dwell Gate Processor
0.8 Hz Scalloping Frequency
α,β Filter, No Rate Limiter, 4X Track Gate
+ -1 dB Multipath
o - - - o -3 dB Multipath
Mean Shift, Beamwidths
σ, Beamwidths
0
0.1
0.2
0.1
0
0
.25
1.0
1.5
2.0
2.5
Multipath Separation Angle, Beamwidths

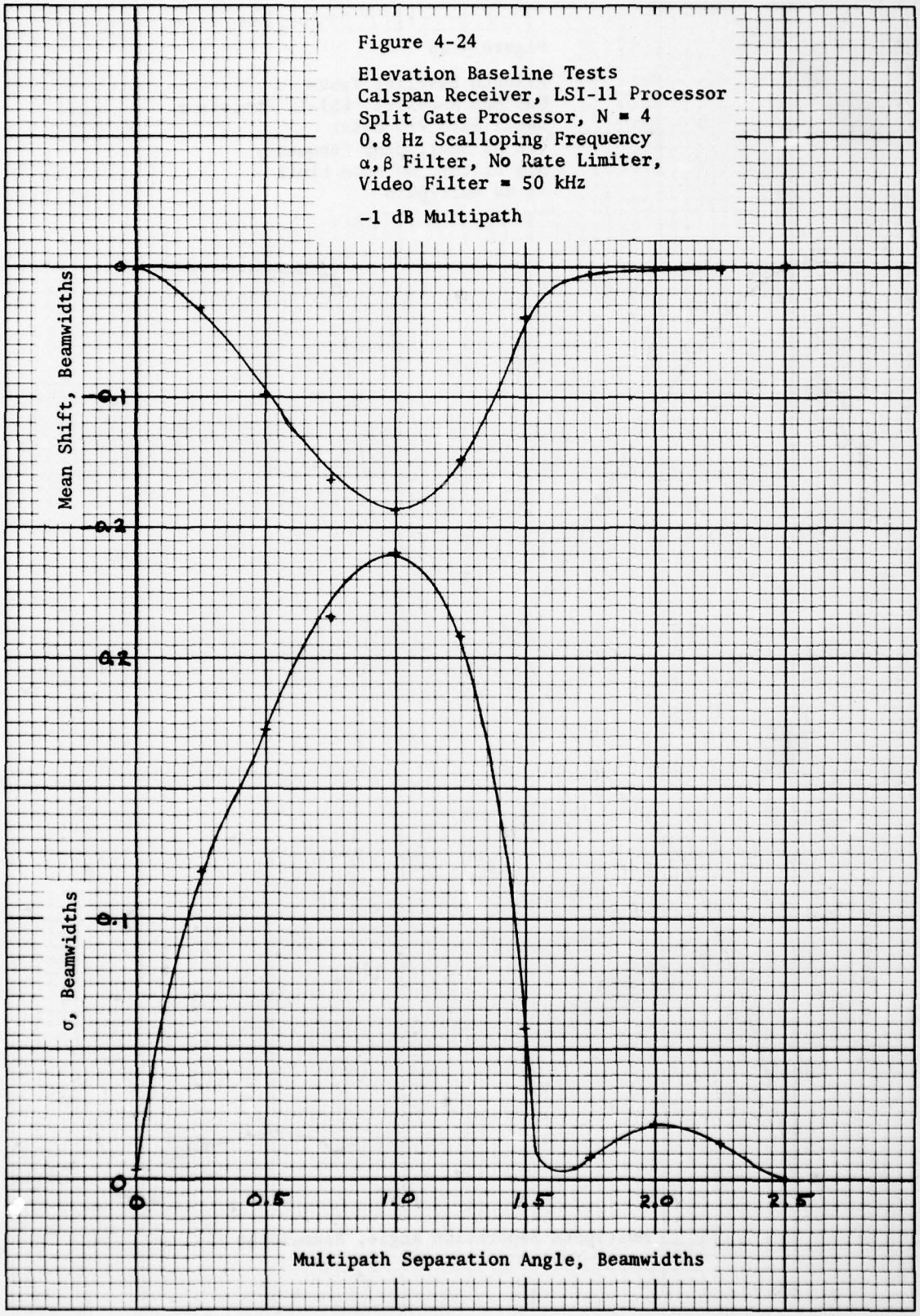


Figure 4-24
Elevation Baseline Tests
Calspan Receiver, LSI-11 Processor
Split Gate Processor, N = 4
0.8 Hz Scalloping Frequency
α,β Filter, No Rate Limiter,
Video Filter = 50 kHz
-1 dB Multipath
Mean Shift, Beamwidths
0
0.1
0.2
σ, Beamwidths
0.2
0.1
0
0
0.5
1.0
1.5
2.0
2.5
Multipath Separation Angle, Beamwidths

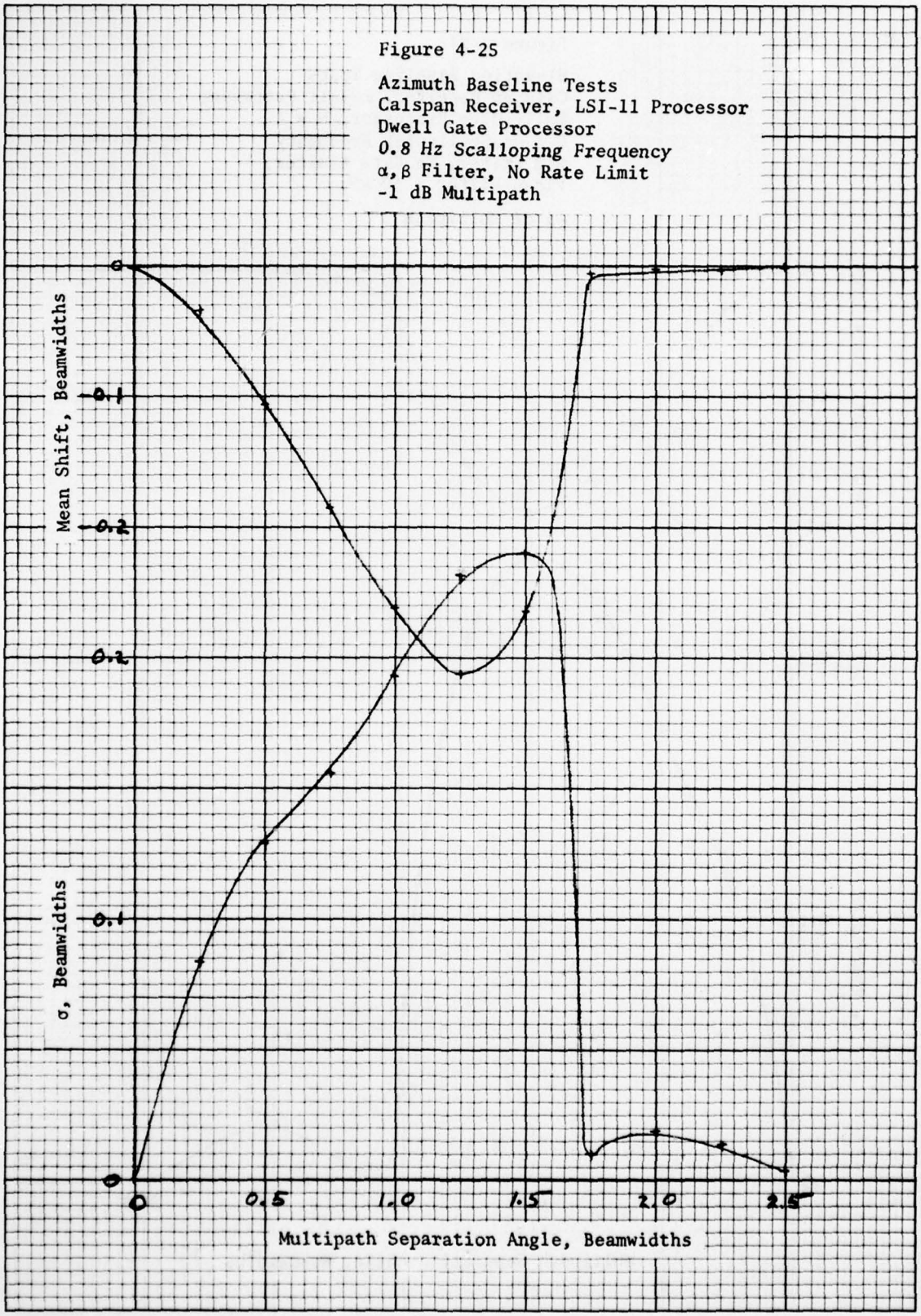


Figure 4-25
Azimuth Baseline Tests
Calspan Receiver, LSI-11 Processor
Dwell Gate Processor
0.8 Hz Scalloping Frequency
α, β Filter, No Rate Limit
-1 dB Multipath
Mean Shift, Beamwidths
σ, Beamwidths
0
-0.1
-0.2
0.2
0.1
0
0
0.5
1.0
1.5
2.0
2.5
Multipath Separation Angle, Beamwidths

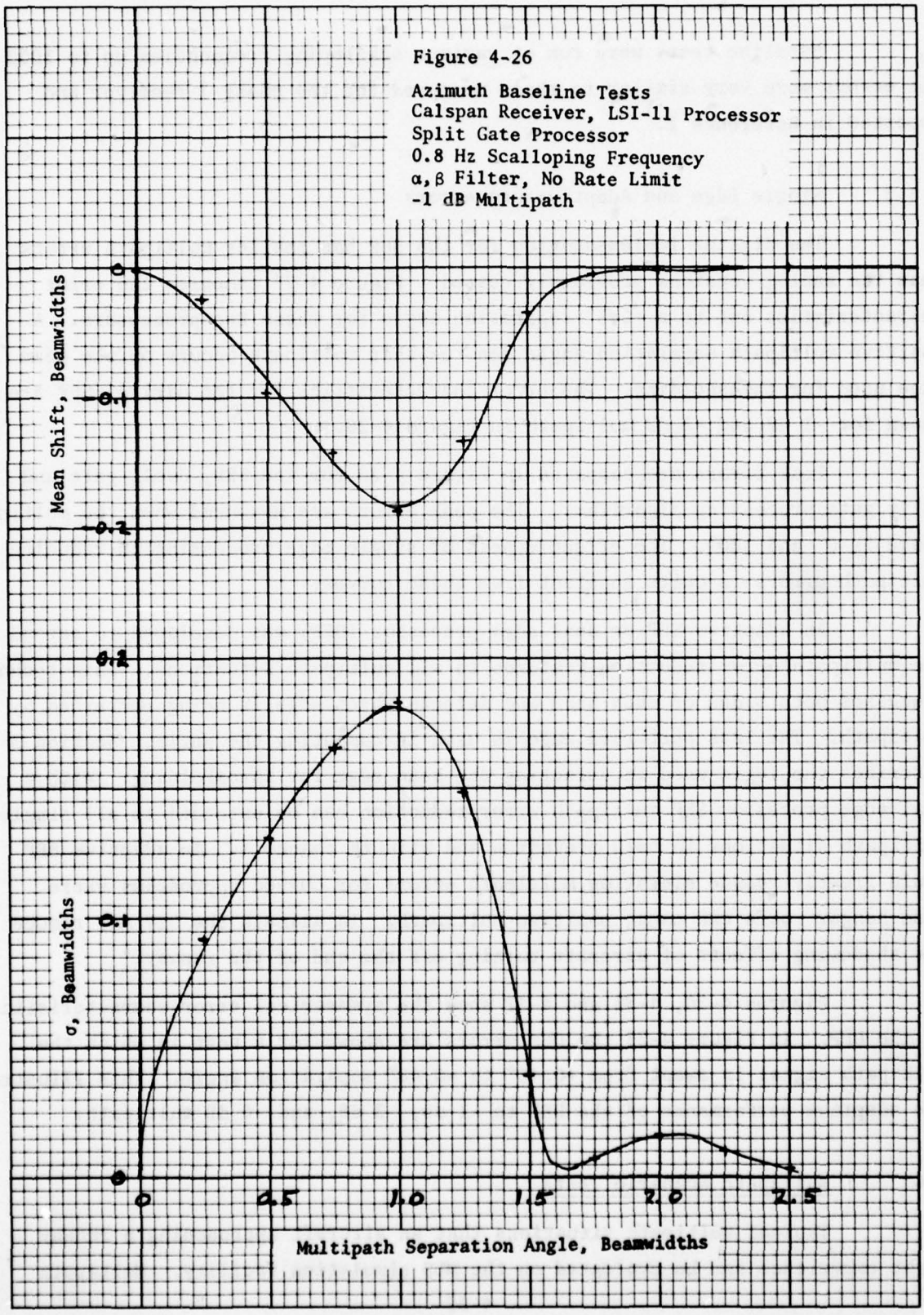


Figure 4-26
Azimuth Baseline Tests
Calspan Receiver, LSI-11 Processor
Split Gate Processor
0.8 Hz Scalloping Frequency
α, β Filter, No Rate Limit
-1 dB Multipath
Mean Shift, Beamwidths
0
-0.1
-0.2
0.2
σ, Beamwidths
0.1
0
0
0.5
1.0
1.5
2.0
2.5
Multipath Separation Angle, Beamwidths

Baseline tests were run at various scalloping frequencies up to 1000 Hz. The errors were very similar to those measured for the phase 3 receiver and reported in Reference 1.

4.3.2 Single Edge and Adaptive Processors

The digital implementation for the SEP has smaller multipath errors than the analog versions previously tested. Figure 4-27 compares the error characteristics out to a +0.5° separation angle for these two processors. A positive multipath separation angle denotes that multipath occurs on the beam edge used for thresholding. The error characteristics for the digital SEP are shown for -1 dB and -3 dB multipath in Figure 4-28.

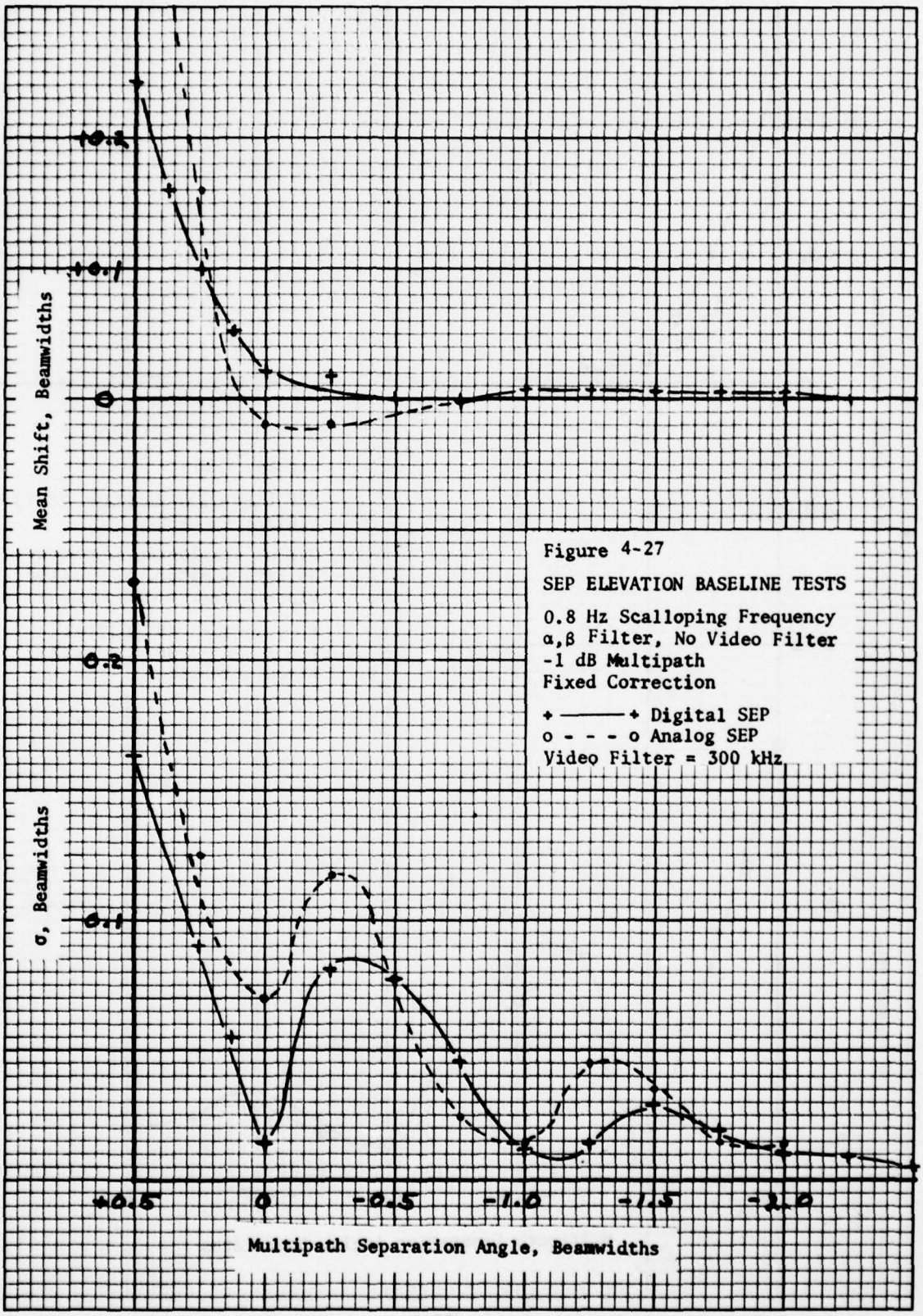
Peak errors are compared in Figure 4-29 for the SEP, dwell gate and split gate processing algorithms. The peak errors are measured when the multipath phase is 0° and 180°. The effectiveness of single edge processing in reducing multipath errors is quite apparent from these curves.

An adaptive SEP or dual edge processor (DEP) was developed to extend the multipath error reduction features to all multipath situations. This technique processes both sides of each beam and detects which edge is being perturbed by multipath. The less perturbed edge is used in computing the angle. Section 3 describes the logic used in selecting the beam edge for thresholding. With a dual edge processor SEP multipath error reduction can be extended to all single multipath situations in both elevation and azimuth channels. An adaptive SEP could greatly reduce elevation multipath errors for curved approaches where some hangar roofs can cause positive multipath. In azimuth the DEP may reduce the shadowing effects of aircraft turning off the end of the runway.

Figures 4-30, 4-31 and 4-32 show the symmetrical error characteristics of the DEP. In Figure 4-33 the DEP errors are shown for a test in which the multipath signal is swept from +0.48° to -0.48° separation angle. This illustrates the adaptive performance of the DEP to -1 dB, -3 dB, and -6 dB multipath.

4.4 Multipath Scenario Tests

Typical multipath situations that an aircraft approaching a runway might experience can be evaluated on the MLS simulation facility. Multipath


+0.2
+0.1
0
Mean Shift, Beamwidths
0.2
0.1
σ, Beamwidths
+0.5
0
-0.5
-1.0
-1.5
-2.0
Multipath Separation Angle, Beamwidths
Figure 4-27
SEP ELEVATION BASELINE TESTS
0.8 Hz Scalloping Frequency
α,β Filter, No Video Filter
-1 dB Multipath
Fixed Correction
+ ——— + Digital SEP
o - - - o Analog SEP
Video Filter = 300 kHz

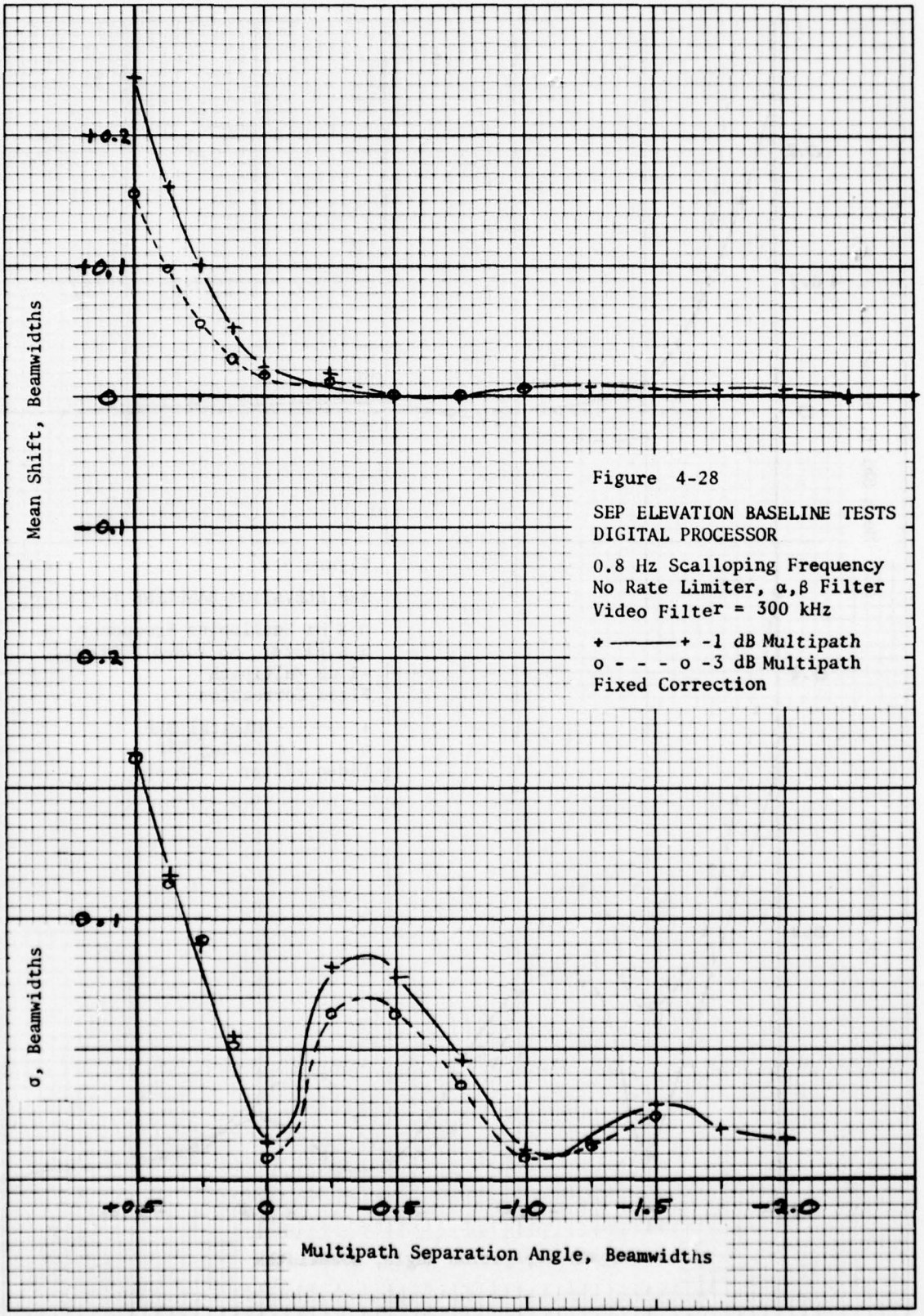


Figure 4-28

SEP ELEVATION BASELINE TESTS
DIGITAL PROCESSOR

0.8 Hz Scalloping Frequency
No Rate Limiter, α,β Filter
Video Filter = 300 kHz

+ ——— + -1 dB Multipath
o - - - o -3 dB Multipath
Fixed Correction

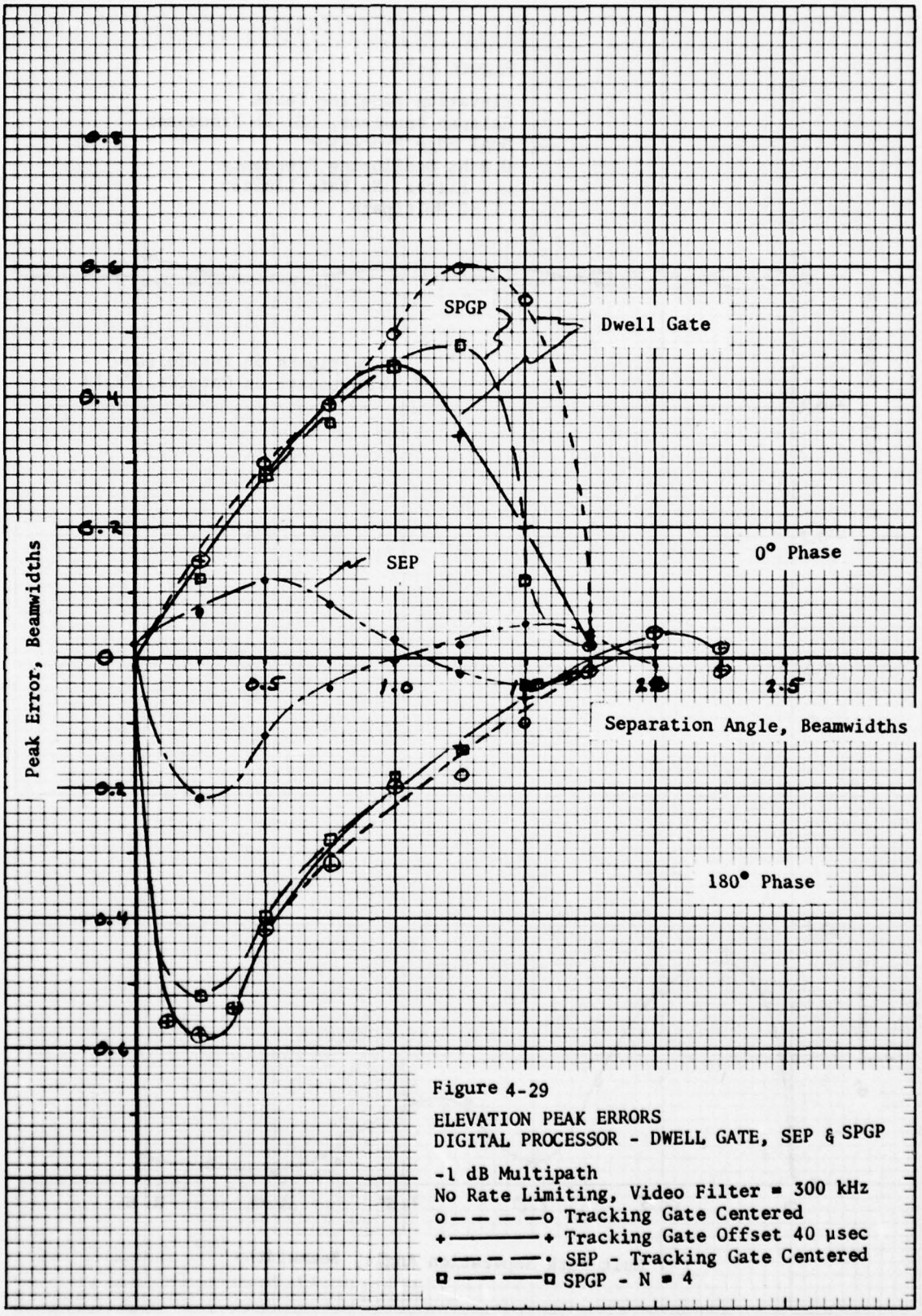


Figure 4-29

ELEVATION PEAK ERRORS
DIGITAL PROCESSOR - DWELL GATE, SEP & SPGP

-1 dB Multipath
No Rate Limiting, Video Filter = 300 kHz
o— — — —o Tracking Gate Centered
+————+ Tracking Gate Offset 40 μsec
•— — —• SEP - Tracking Gate Centered
□—— ——□ SPGP - N = 4

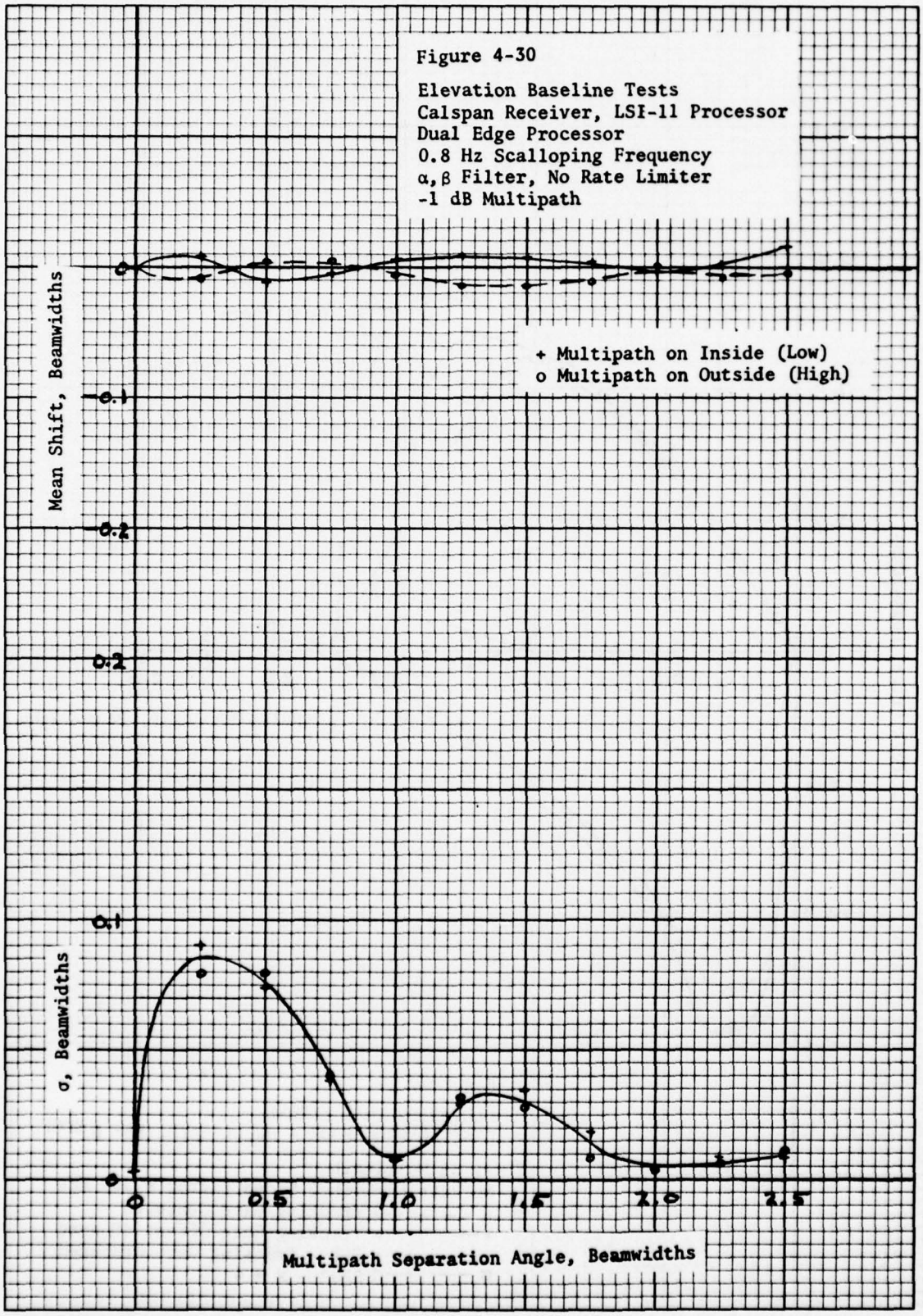


Figure 4-30
Elevation Baseline Tests
Calspan Receiver, LSI-11 Processor
Dual Edge Processor
0.8 Hz Scalloping Frequency
α, β Filter, No Rate Limiter
-1 dB Multipath
+ Multipath on Inside (Low)
o Multipath on Outside (High)
Mean Shift, Beamwidths
-0.1
-0.2
0.2
0.1
σ, Beamwidths
0
0.5
1.0
1.5
2.0
2.5
Multipath Separation Angle, Beamwidths

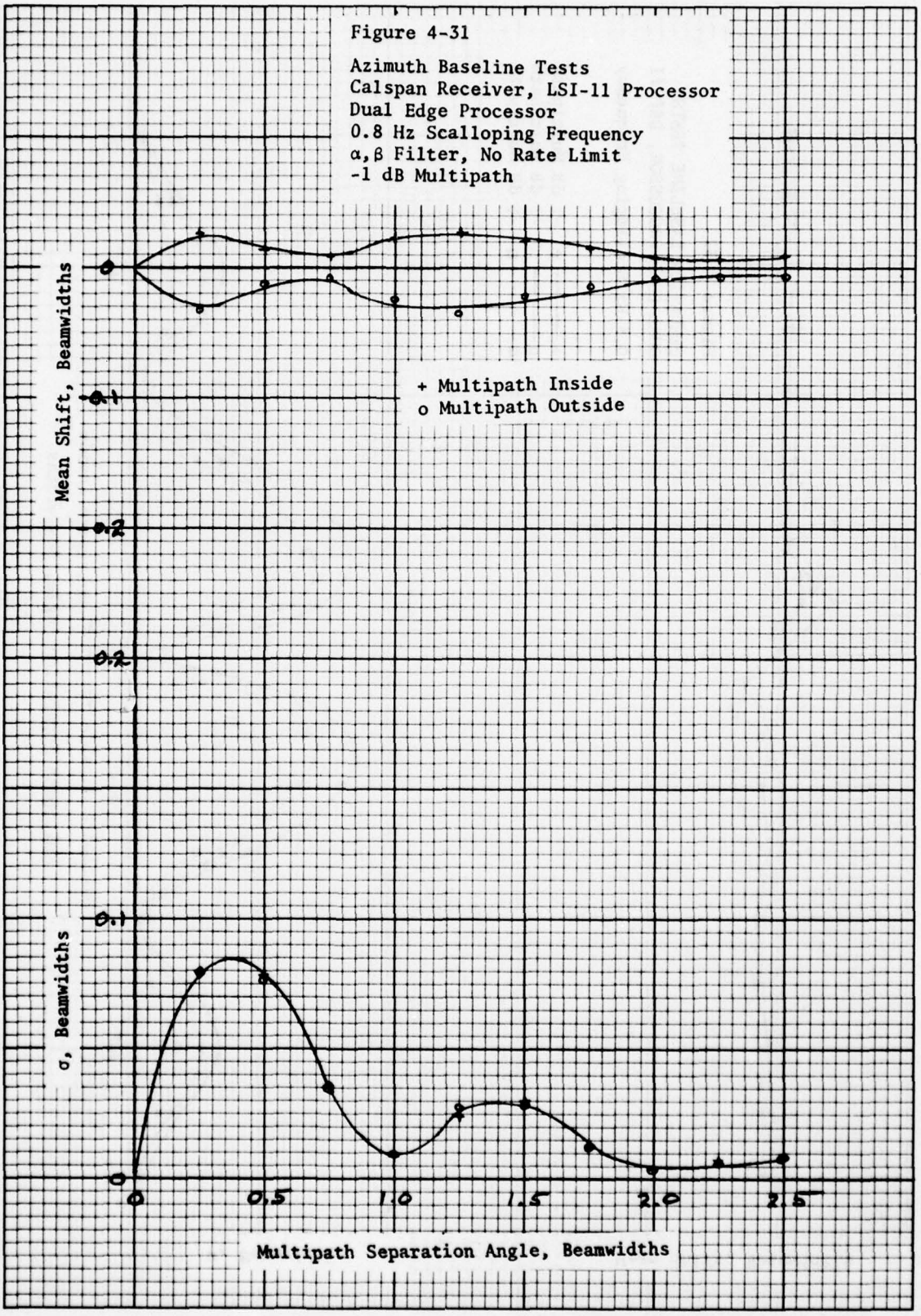


Figure 4-31
Azimuth Baseline Tests
Calspan Receiver, LSI-11 Processor
Dual Edge Processor
0.8 Hz Scalloping Frequency
α,β Filter, No Rate Limit
-1 dB Multipath
Mean Shift, Beamwidths
0
-0.1
-0.2
+ Multipath Inside
o Multipath Outside
0.2
σ, Beamwidths
0.1
0
0
0.5
1.0
1.5
2.0
2.5
Multipath Separation Angle, Beamwidths

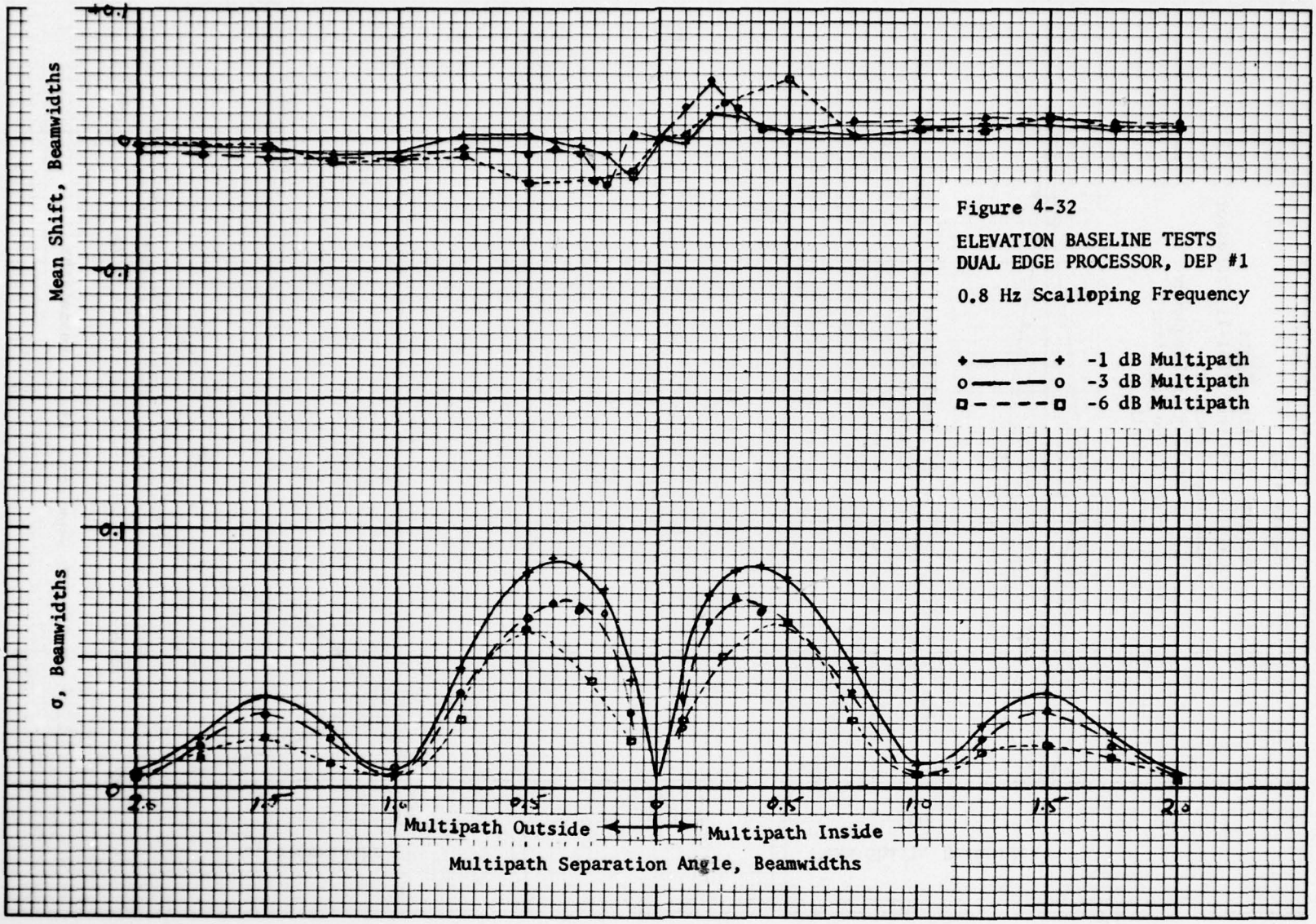


Figure 4-32

ELEVATION BASELINE TESTS
DUAL EDGE PROCESSOR, DEP #1

0.8 Hz Scalloping Frequency

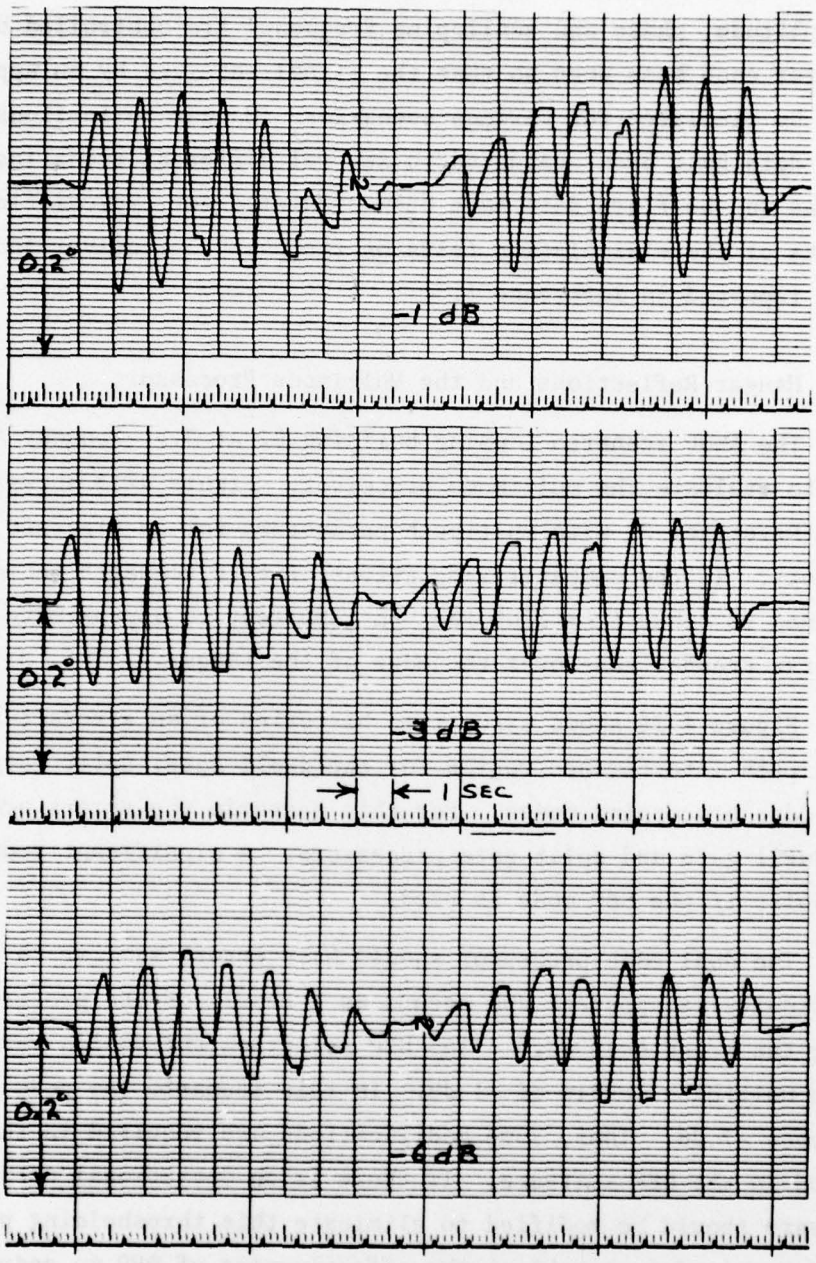


Figure 4-33

Multipath Error of Dual Edge Processor
Separation Angle Varied from -0.48° to +0.48°
Multipath = -1 dB, -3 dB and -6 dB

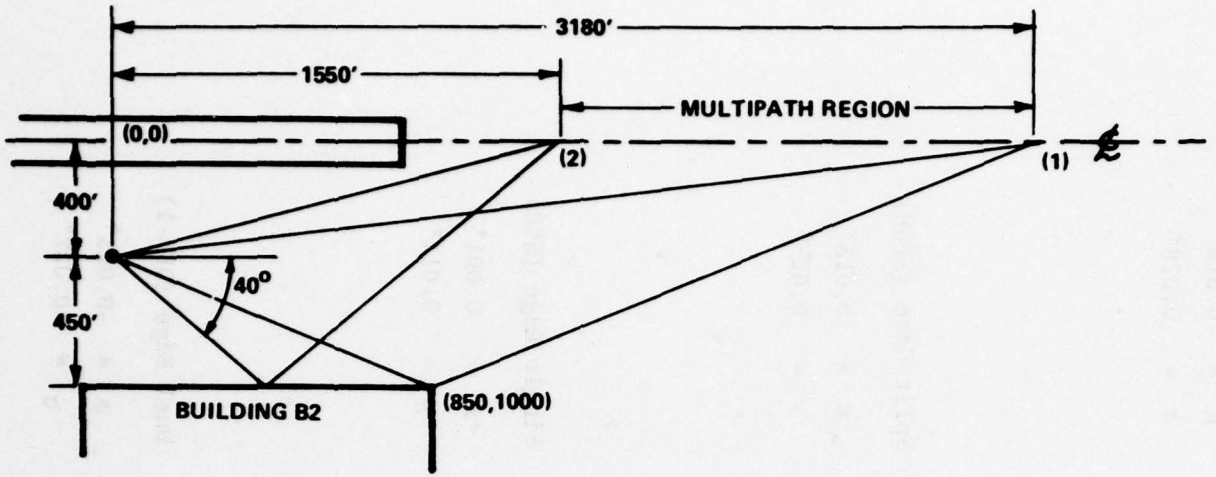
signal amplitude, phase and scalloping frequency are controlled by the PDP-11 computer for each beam scan so that the signal received by an approaching aircraft can be simulated for various scenarios. Hangar reflections in elevation and flare data have been evaluated in several different scenarios. Ground reflections in the flare data have been simulated for typical flare scenarios. The results of these simulation tests on the phase 3 receiver and analog SEP have been reported in Reference 1.

4.4.1 Hangar Reflections and the Multimode Processor

The AWOP scenario 1 using building B2 at J.F. Kennedy Airport was selected to evaluate the multimode processor. Figure 4-34 shows the scenario geometry (Reference 2) with multipath parameters for an aircraft approaching at 130 knots. In the computer simulations of this scenario the multipath region was extended to occur from 3300 feet to 1350 feet to approximate the passage of the first Fresnel zone over the edge of the hangar.

Figure 4-35 shows error time histories of an aircraft flying through this multipath interference region for the dwell gate, split gate, single edge and dual edge processing modes. For this scenario the errors are very similar for the dwell gate and split gate processors. A significant reduction in the error results if the SEP mode is used.

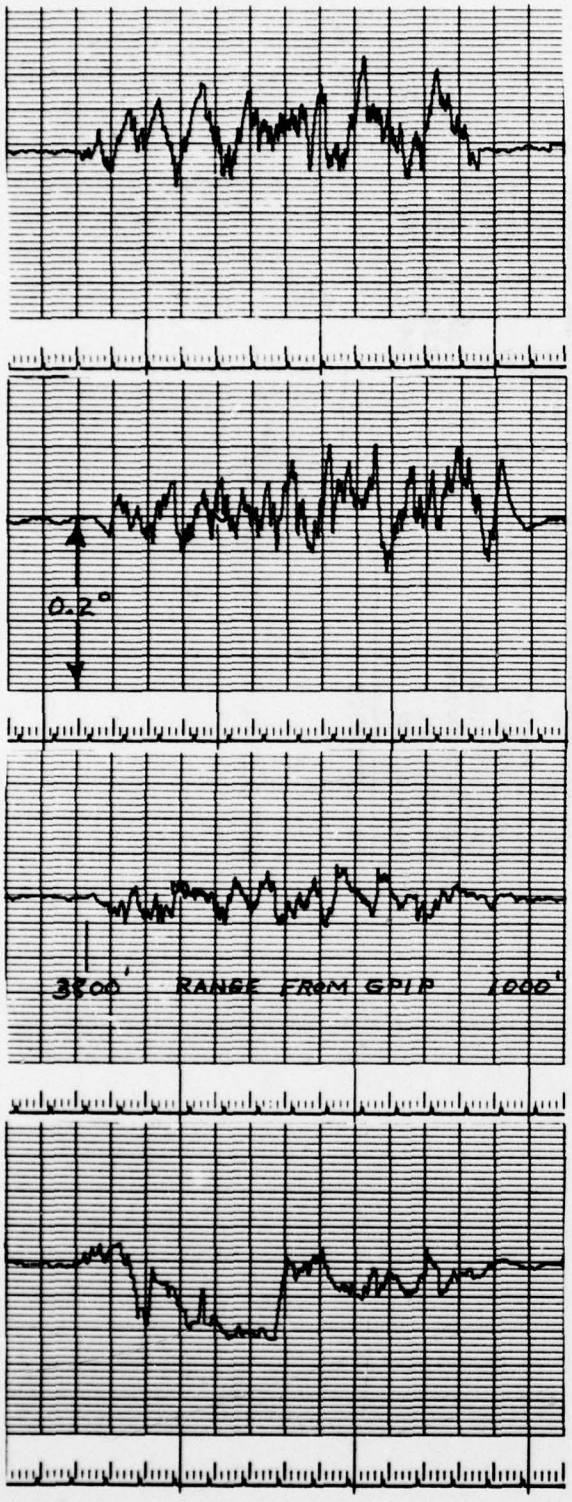
The dual edge processor should have errors similar to the SEP. However, a discontinuity is apparent and occurs as a result of the processing algorithms selecting the wrong beam edge. The DEP selection thresholds were set for operation with high multipath levels of -1 dB. In this scenario the peak multipath level only reaches -7 dB. Thus, some modifications are required in the threshold logic used in the DEP software. If there is an operational need for the DEP the software should be modified to eliminate this thresholding problem. Flight tests are required to establish the effectiveness of DEP to reduce aircraft shadowing effects and multipath errors from hangar roofs for some curved path approaches.



	POINT 1	POINT 2	
RANGE	3180	1550	FEET
SCALL. FREQ.*	75	228	Hz
A/C HEIGHT	159	77	FEET
REFL. HT. (GEOM.)	55	27	FEET
SEPARATION ANGLE	0.19	0.58	DEG.
GLIDE SLOPE	2.86	2.86	DEG.
PATH ATTEN	0.2	2.4	DB

*AT 130 KNOTS

Figure 4-34 AWOP SCENARIO 1, BUILDING B2



Dwell Gate (DGP)

$m = -0.019°$

$\sigma = 0.028°$

Split Gate (SPGP)

$m = 0.013°$

$\sigma = 0.027°$

Single Edge (SEP)

$m = 0.001°$

$\sigma = 0.014°$

Dual Edge (DEP-1)

$m = -0.013°$

$\sigma = 0.027°$

Figure 4-35 AWOP SCENARIO B-2 (Modified) Elevation

Peak Multipath -7 dB
LSI-11 Processor

4.4.2 Flare Scenarios

The SEP is the only processing technique proposed for flare data. Extensive flare scenarios have been simulated using the analog breadboard SEP and are reported in Reference 1. These simulations were not repeated for the digital SEP since its performance can be estimated from the error curves in Figure 4-27. These curves compare the analog and digital SEP error characteristics. The digital SEP main lobe and first sidelobe errors are about 0.7 as large of the analog processor. The peak errors for the flare scenarios in Reference 1 will be about 70% of those shown for the analog SEP.

From the flare simulations reported in Reference 1 it appears that the magnitude of error in the elevation angle is too large to permit using altitude rate computed directly from the elevation data in a flare coupler of the flight control system. Some type of complementary filtering will be required to augment altitude rate computed by differentiating the measured height with barometric altitude rate or accelerometer derived rate information. Thus, a closed loop simulation of the flare maneuver requires the optimization of several variables and requires a significant effort to evaluate a range of parameters. The extensive simulation analysis required to demonstrate the actual performance of the SEP was beyond the scope of the current program.

Closed loop simulations have been run (Reference 1) with the MLS simulator using actual processors. A closed loop flare simulation could be run with minor software changes in the PDP-11 control computer and with the addition of a simulated flare coupler. This type of simulation is eventually required to demonstrate the performance of the SEP over the complete range of multipath situations likely to occur in the real environment.

Section 5.0
FIELD AND FLIGHT TEST OBJECTIVES

The performance of the multimode digital processor has been evaluated in the MLS simulator with the results summarized in this report. However, a limited number of field tests are required to verify performance of the processing techniques in the field environment. Some performance characteristics are not easily evaluated in a simulator such as the sensitivity of azimuth processing algorithms to aircraft shadowing and the effectiveness of beamwidth measurements for the single edge processor. Flight test evaluations are essential to provide validation of the performance characteristics required for development of the airborne processor specifications.

5.1 Special Processor Features

The multimode processing capabilities of the LSI-11 software will permit simultaneous outputs of up to four processing modes on one function. Relative performance of the processing techniques can be easily evaluated with only a limited amount of flight test data.

The LSI-11 computer used for the digital processor was configured with a 4K core memory. Changes in the processing algorithms are readily made with a core memory, even in the field. Also, new processing algorithms can be added with a minimal effort.

5.2 Test Scenarios

Flight tests should be run to determine the relative sensitivity of the dwell gate, split gate and adaptive single edge processors to aircraft shadowing effects in the azimuth data. Two aircraft are required for these tests. While one aircraft is approaching the second should be turning off the runway in front of the azimuth antenna. Another test should be conducted with the large aircraft taking off. The adaptive features in the dual edge processor may reduce the rather large errors typical of aircraft shadowing.

Tests using the Australian flare unit should be conducted at NAFEC. The flare site is located so that during the flare tests data can also be collected on the effects of hangar multipath on elevation data. Both flight and pole tests are required. The pole tests would measure the M/D ratio and multipath separation angles for the hangar reflections. The pole test data in the flare region can be used with simulator data to estimate the magnitude of the M/D ratio for the flare antenna. The flight and pole tests will provide comparative performance data on the dwell gate, split gate and single edge processing techniques for both flare and hangar multipath.

Several approaches should be made to elevation units having different beamwidths. These data will determine the effectiveness of the beamwidth correction algorithms used for the single edge processor.

The adaptive single edge processor should be flown against elevation sites where positive and negative multipath can occur from hangar reflections. This type of environment has been reported from curved hangar roofs at J.F. Kennedy Airport.

REFERENCES

1. Beneke, J., Wightman, C.W., Offt, A.M. and Vallone, C.B., "Multipath Performance Tests of TRSB Receivers", Report No. FAA-RD-77-66, March 1977.

2. Calspan TN-13, "Phase 3 Receiver Tests", December 1977.

3. Calspan TN-14, "Measurements of Doppler Scan Format at JFK Airport", March 1978.

4. Shnidman, D.A. and Evans, J.E., "Multipath Characteristics of AWOP WG-A Multipath Scenarios", MIT Lincoln Laboratory, ATC Working Paper No. 44WP-5040, 25 June 1976.

5. "ICAO Test Plan for U.S. Microwave Landing System", FAA Internal Report, March 31, 1975.

6. Wightman, C.W., Beneke, J., Offt, A.M. and Vallone, C.B., "Dynamic Multipath Effects on MLS Scanning Beam and Doppler Scan Techniques", Report No. FAA-RD-73-181, October 1973.

Appendix A
FILTER APPROXIMATION TO AIRCRAFT PATH FOLLOWING

In previous tests with the MLS receivers in a closed loop elevation landing simulation, the model of the aircraft path following filter presented in the ICAO test plan (Reference 5) was compared to an analog/digital hybrid simulation of a medium weight transport aircraft. A large discrepancy was noted between the output time histories of the two models. A new filter model was developed that provided a closer approximation to the path following characteristics of an actual aircraft.

Brief Description of Simulation and Filter Models

The analog/hybrid simulation uses an analog computer to model the longitudinal three degree of freedom linear aircraft equations, an analog-to-digital and digital-to-analog interface, and a digital computer to control the MLS simulation parameters that includes an actual MLS receiver in the closed loop. The coupler and autopilot are modeled on the analog computer with error and command limiters. The aircraft equations are a small angle linear model but the coupler and autopilot can limit both the MLS receiver angle amplitude and commanded elevator angle. A more complete discussion of the simulation can be found in Reference 6. Figures A-1 and A-2 are taken from this reference and show the simulation parameters.

The ICAO elevation path following filter is modeled by a second order critically damped system with a corner frequency of 2.34 radians/second.

$$H_{EL1}(S) = \frac{1}{\left(\frac{S}{2.34} + 1\right)^2}$$

The response of the filter model and analog simulation to a unit step function appears in Figure A-3.

The large difference in time histories shows the need for a better model. A new filter model was developed which closely matched the step

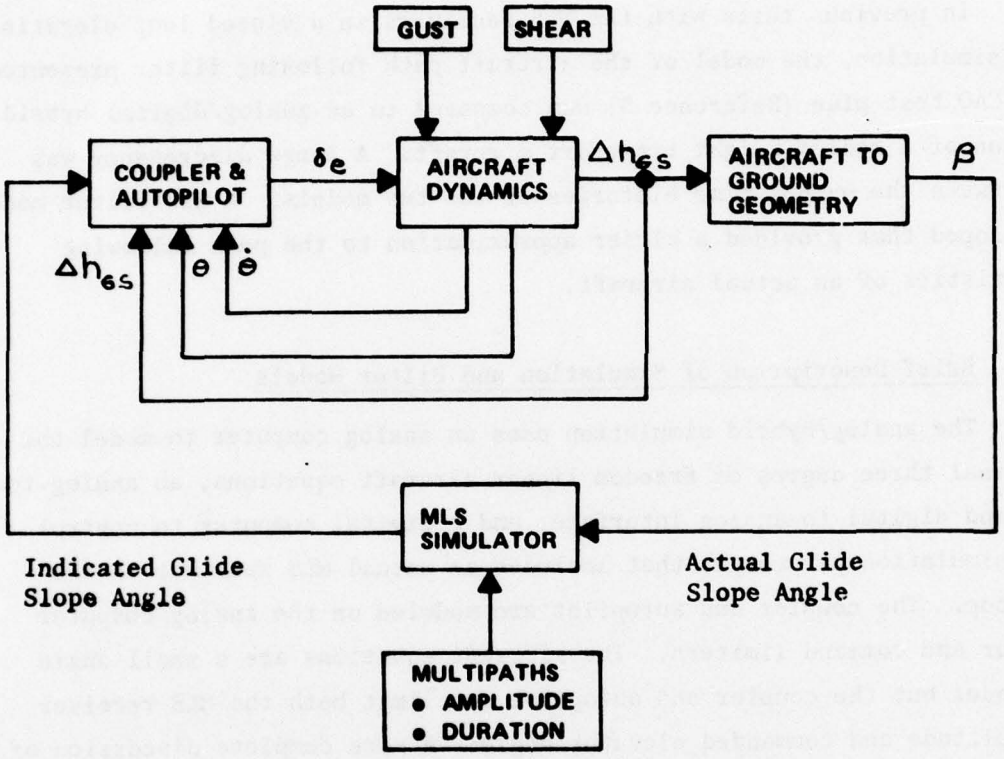


Figure A-1 LONGITUDINAL CLOSED LOOP SIMULATION

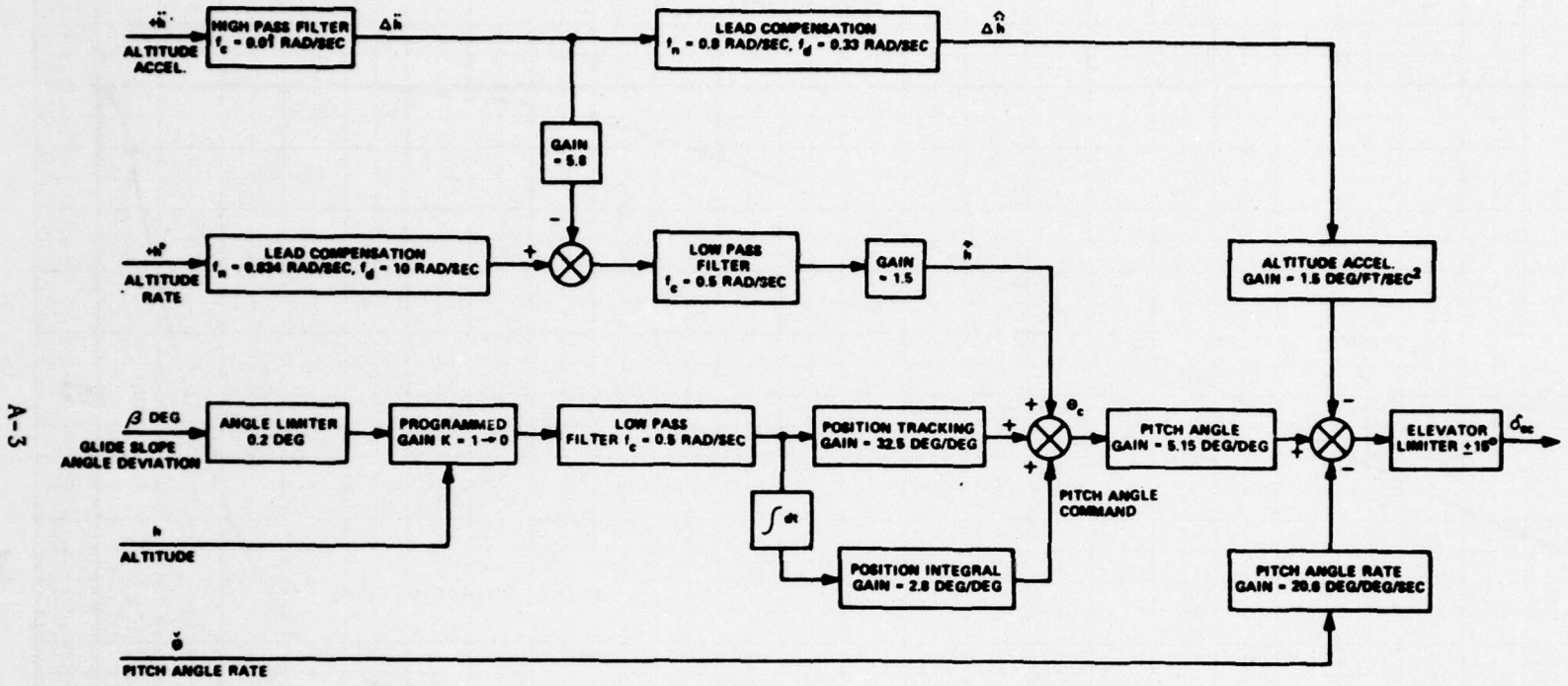


Figure A-2 LONGITUDINAL AUTOPILOT CONTROL LAW

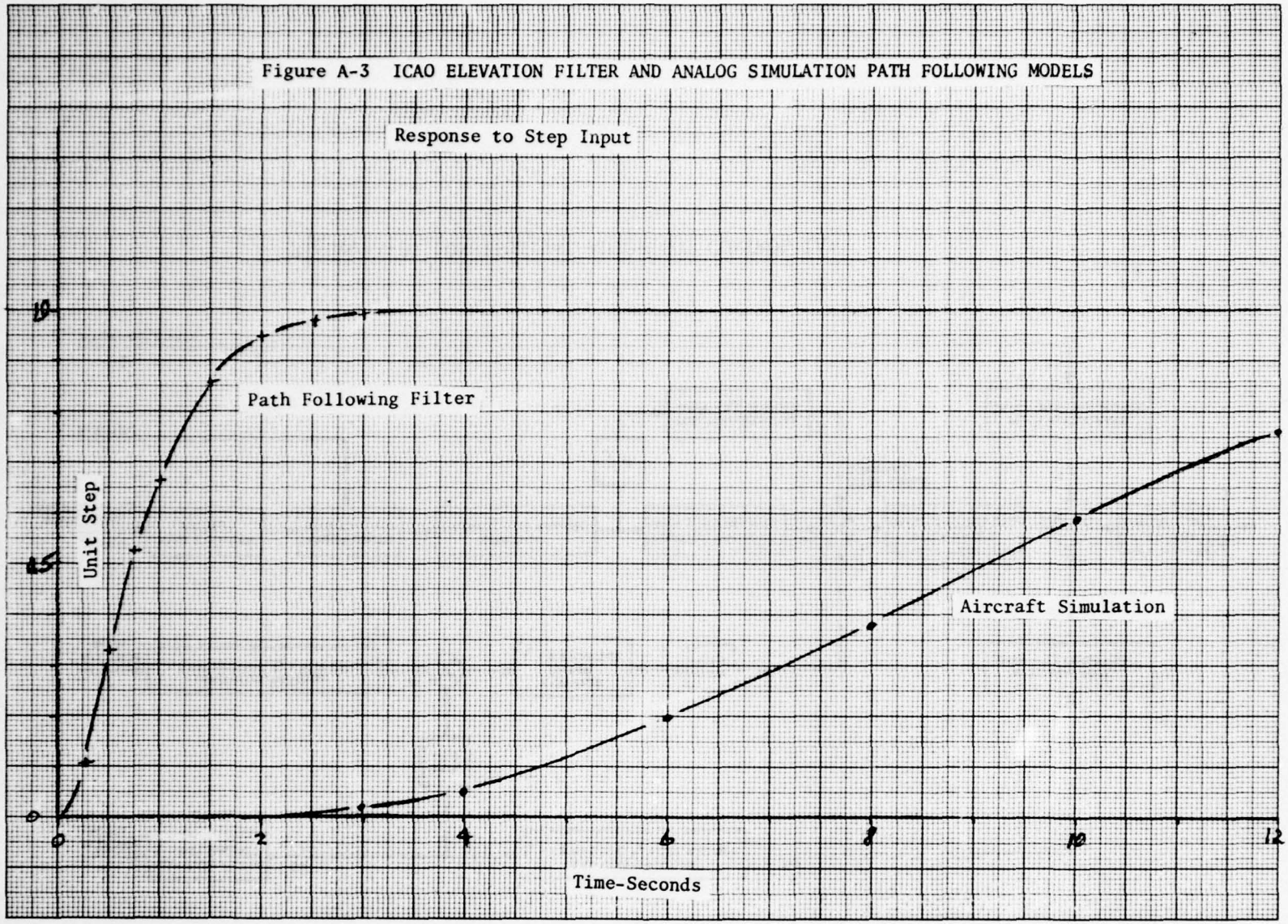


Figure A-3 ICAO ELEVATION FILTER AND ANALOG SIMULATION PATH FOLLOWING MODELS

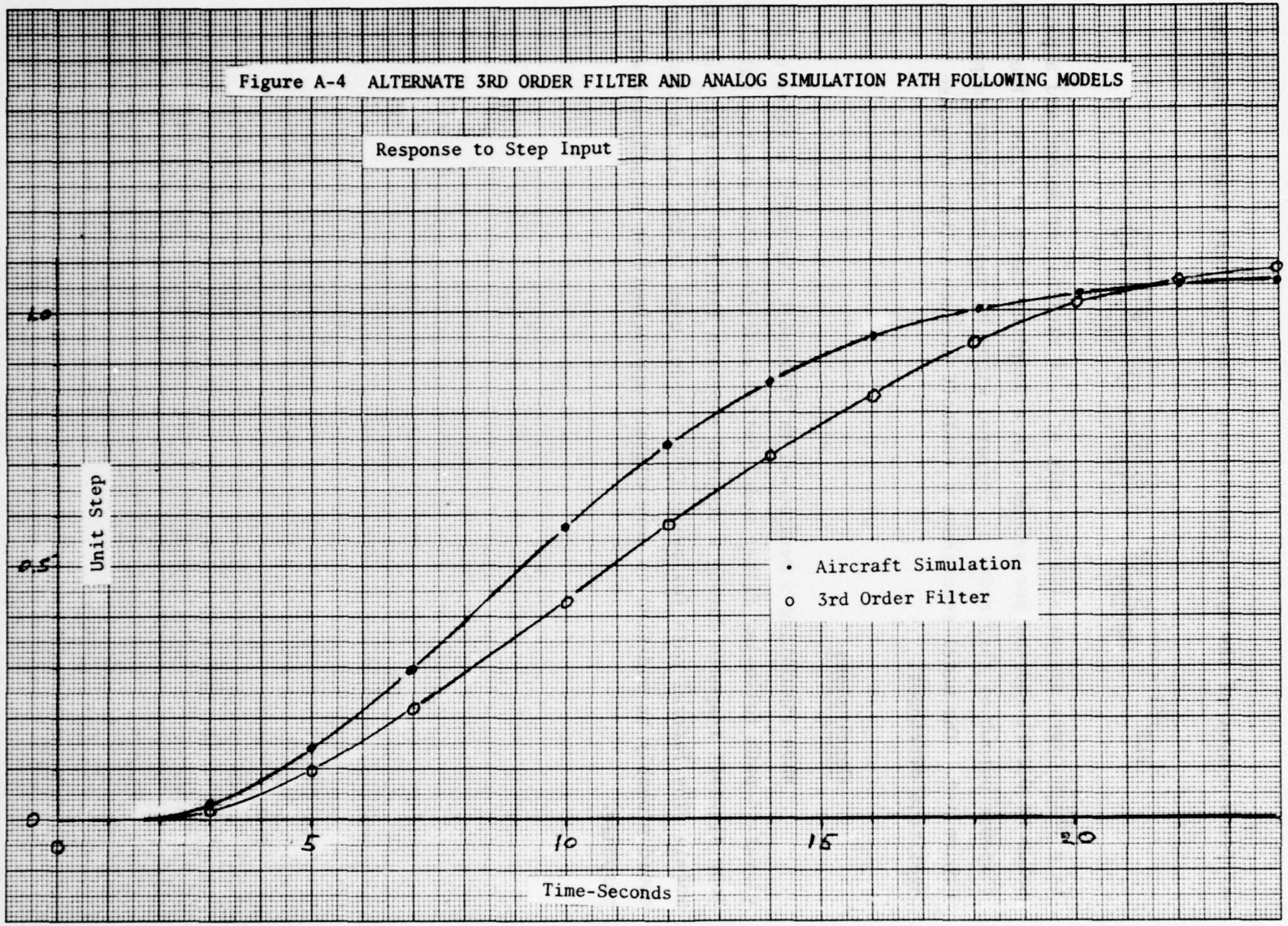


Figure A-4 ALTERNATE 3RD ORDER FILTER AND ANALOG SIMULATION PATH FOLLOWING MODELS
Response to Step Input
Unit Step
1.0
0.5
0
0
5
10
15
20
Time-Seconds
• Aircraft Simulation
o 3rd Order Filter

response output of the hybrid simulation. The resultant transfer function:

$$H_{EL2}(S) = \frac{1}{\left(\left(\frac{S}{0.169}\right)^2 + \frac{2(0.55)}{0.169} + 1\right)\left(\frac{S}{3.14} + 1\right)}$$

is a third order system with one pole at 3.14 radians per second and a pair of poles at 0.1411 radians per second with a dampling ratio of 0.55. The step response output of this model is compared with the analog systems response in Figure A-4. The model represents a tradeoff between initial response time and amplitude overshoot.

Conclusions

When simulating a medium weight transport aircraft, a third order elevation path following filter model better describes the longitudinal closed loop aircraft response during a coupled approach than the ICAO test plan filter model. The lateral path following filter model used in the test evaluations could probably be modified to more closely approximate an actual aircraft response.