LEVEL II

Research and Development Technical Report
ECOM-77-2684-1

COMPUTER AIDED ENGINEERING OF SEMICONDUCTOR INTEGRATED CIRCUITS

J.D. Meindl, K.C. Saraswat, R.W. Dutton, J.F. Gibbons,
W. Tiller, J.D. Plummer, B.E. Deal and T.I. Kamins
Integrated Circuits Laboratory
Stanford University
Stanford, California 94305

April 1978

Interim Report for Period 1 November 1976-30 April 1977

Distribution Statement

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Prepared for

ADVANCED RESEARCH PROJECTS AGENCY
1400 Wilson Boulevard
Arlington, Virginia 22209

Contract No. DAA-B07-77-C-2684
ARPA Order No. 2985

ECOM
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(18) (19) REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: ECOM-77-2684-1

2. GOVT ACCESSION NO.

3. RECIPIENT'S CATALOG NUMBER

(6) 4. TITLE (and Subtitle): Computer Aided Engineering of Semiconductor Integrated Circuits.

(9) 5. TYPE OF REPORT & PERIOD COVERED: Interim Report, 1 November 76 - 30 April 77

6. PERFORMING ORG. REPORT NUMBER

(10) 7. AUTHOR(s): J. D. Meindl, K.C. Saraswat, R.W. Dutton, J.F. Gibbons, J.D. Plummer, B.E. Deal, R.R. Razouk, T.I. Kamins and W. Tiller.

(15) 8. CONTRACT OR GRANT NUMBER(s): DAAB07-77-C-2684, ARPA Order No. 2985

9. PERFORMING ORGANIZATION NAME AND ADDRESS: Integrated Circuits Laboratory, Stanford University, Stanford, California 94305

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 6.1 1T1 61101 A 00A 00, 690000.211.13.27.00

11. CONTROLLING OFFICE NAME AND ADDRESS: Advanced Research Projects Agency (ARPA), 1400 Wilson Blvd., Arlington, Virginia 22209

(11) 12. REPORT DATE: April 1978

13. NO. OF PAGES: 84

14. MONITORING AGENCY NAME & ADDRESS (if diff. from Controlling Office): U.S. Army Electronics Command, Attn: DELET-I, Fort Monmouth, New Jersey 07703

15. SECURITY CLASS. (of this report): Unclassified

(12) 89 p.

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this report)

Approved for public release; distribution unlimited.

(16) 1T161101A00A (17) 00

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from report)

18. SUPPLEMENTARY NOTES

This research was sponsored by the Defense Advanced Research Projects Agency (DARPA) pursuant to ARPA Order No. 2985, dated 18 February 1975, Program Code W15P87.

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

MODELING, SEMICONDUCTOR DEVICES
SEMICONDUCTOR PROCESSING
PROCESS MODELING SEMICONDUCTORS

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The objectives of this program are to remove the empiricism associated with the design and manufacturing of custom integrated circuits for military applications and to reduce the cost of these circuits by devising improved computer-aided engineering techniques. Efforts of research covered by this report are in the areas of (1) ion implantation and diffusion of dopants, (2) thermal oxidation, (3) chemical vapor deposition of silicon, and (4) device simulation and statistical circuit modeling.

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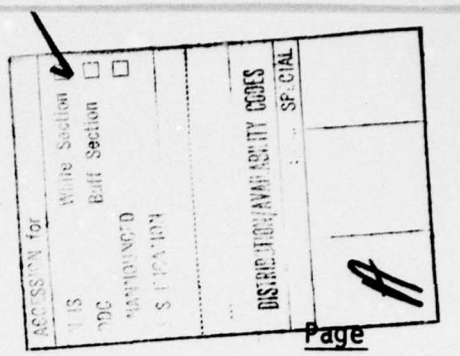
SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

78 06 27 035

409117



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COMPUTER-AIDED ENGINEERING OF SEMICONDUCTOR INTEGRATED CIRCUITS

ABSTRACT

Economic procurement of small quantities of high performance custom integrated circuits for military systems is severely impeded by inadequate process, device and circuit models to facilitate accurate computer-aided design at low cost. The salient objective of this program is to formulate physical models of fabrication processes, devices and circuits to allow total computer-aided design of custom large-scale integrated circuit subsystems to reduce development cycle time and cost. The basic areas under investigation are: (1) ion implantation and diffusion of dopants, (2) thermal oxidation, (3) chemical vapor deposition of silicon, and (4) device simulation and statistical circuit modeling. A brief discussion of the results of the first six months of the second year of the program is presented here.

INTRODUCTION

In military, industrial, commercial, and consumer applications, frequently there is a great necessity for "customizing" the design of an integrated circuit to fulfill the critical needs of a specific system or class of systems. A major barrier which prevents the economic production of small quantities of high performance custom integrated circuits is the cost of design. That is, the initial cost of designing optimum fabrication processes, device structures, and circuit configurations is prohibitively large because of the amount of empirical human effort which must be invested. The root cause of this problem is a glaring lack of adequate process, device, and circuit models and accompanying computer-aided design techniques to ease the burden of custom design. The salient objective of this program is the development of new basic models for integrated circuit processes, devices and circuits, which will permit accurate prediction of the characteristics of a monolithic structure on the basis of its proposed process parameters. These models will serve as the basis for economic computer-aided design of custom integrated circuits.

The four key generic integrated circuit fabrication processes which are being investigated are (1) ion implantation and diffusion, (2) thermal oxidation, (3) chemical vapor deposition of silicon, and (4) device simulation and statistical circuit modeling. This report describes the progress which has been made in the first six months of the second year of this program in all four areas.

1. ION IMPLANTATION

J.F. Gibbons, A. Chu, K.C. Saraswat

1.1 Objective

Our general objective is to produce process models for the following aspects of ion implantation in Si that are necessary for custom IC fabrication and which are currently empirical rather than analytical.

(1) Range and distribution calculations in multilayer targets based on the Boltzmann transport equation.

- implanted ion profiles
- damage distribution
- recoil implants ("knock-ons")

(2) Diffusive annealing behavior of implanted dopants (multi-stream model).

- profiles resulting from interaction of dopants/vacancies/dopant-vacancy complexes
- radiation-enhanced diffusion

(3) Study of damage.

- traps produced by knock-ons
- residual damage after annealing

1.2 Summary of Principal Accomplishments to Date

During the past two years (FY 76 and 77) the following important contributions have been made.

1.2.1 Development of the Boltzmann transport equation approach to analytically predict range, damage and knock-on distribution of heavy ions (such as arsenic), in Si, insulators (SiO_2, Si_3N_4) and a multilayer combination of them. Using the widely used LSS approach it is not possible to do all

the above calculations.

1.2.2 A multistream diffusion model has been developed, which apart from simple thermal diffusion of dopants, can also predict diffusive annealing behavior of ion implanted dopants and proton enhanced diffusion. The case of boron has been investigated by taking into account boron ions, positively charged vacancies and neutral boron vacancy pairs and their generation -- recombination kinetics to predict the resulting impurity profile of boron implanted in the dose range of 10^{16} to 10^{16} ions/cm^2 and annealed at temperatures of 800°C, 900°C and 1000°C. Transmission electron microscopy studies were conducted to relate the diffusion mechanism of boron to the negatively charged vacancies and boron vacancy complexes. Using these studies the phenomenon of precipitation of boron at higher dose implants was investigated. The generalized diffusion model can predict electrically active, inactive and precipitated boron as a function of time and temperature of diffusion.

A discussion of results obtained during the past six months is given in Section 1.3.

1.3 Detailed Discussion of Results

1.3.1 Calculation of Annealed Impurity Profiles of Ion Implanted Boron into Silicon

A multi-stream diffusion model is proposed for the calculation of the annealing behavior of boron that is ion implanted into silicon at room temperature and subsequently annealed [1.1,1.2]. This model is capable of predicting both the redistribution and the electrical activation of boron during the anneal, as a realistic model should. The calculated results compare very well with extensive experimental data reported in the literature. The comparison includes samples that are implanted at room temperature with

boron in the dose range from 10^{14} to 10^{16} ions/cm^2 and subsequently annealed in the temperature range from 800°C to 1000°C. This range of dose and annealing conditions includes both the typical applications of ion implantation as it is applied in the fabrication of devices and the unconventional cases of high dose implants and low temperature annealing.

The annealing model is in essence a diffusion model extended to include the following situations:

(1) precipitation of boron, when the boron concentration level exceeds the solid solubility limit, in high dose implantation cases

(2) trapping of boron by the strain fields associated with dislocation dipoles that form during annealing at low temperature

In both cases, the presence of this immobile and electrically inactive boron alters significantly the redistribution and electrical activation behavior of boron during the anneal.

The presence of boron precipitates makes it necessary to include four species in the annealing model. These species are substitutional (electrically active) boron, boron-vacancy pairs (electrically inactive), positively charged vacancies, and the aforementioned immobile boron. The electrically active boron is assumed to diffuse substitutionally by means of random encounters with neutral vacancies. The boron-vacancy pair is assumed to diffuse much more rapidly. The principal interaction among the species is the reaction of active boron with positive vacancies to form BV-pairs.

The parameters in the model are a set of diffusivities and lifetimes for various species and interaction. These parameters are

estimated from the examination of each diffusion and each interaction. The values of the most important parameters obey simple activation energy relations. In other cases, the modeling was either not carried to the extent necessary as to make the temperature dependence apparent, or else the parameters represent the composite effects of very complex interactions. In all cases, the mathematical model and the parameter set are universal in the sense that the same equations and parameters can be used for the prediction of ordinary diffusion, proton enhanced diffusion, and the annealing behavior of ion implanted boron at room temperature under conditions that include precipitation effects and low annealing temperature anomalies. Furthermore, in most cases of practical importance, high dose and low annealing temperature conditions are of limited interest and, as a result, the three stream diffusion model with an appropriate subset of parameters is sufficient. This reduced model is still very important and attractive because once the parameters associated with high dose and/or low temperature anomalies are deleted, the remaining parameters have simple activation energies and are determined by the specification of a single variable -- the temperature.

1.3.2 Epitaxial Silicon Growth on Ion Implanted Silicon

Ion implanted technology offers an attractive means for fabrication of buried collectors in silicon bipolar integrated circuits. High-dose implants (10^{15} - 10^{16} cm^{-2}) at fairly high energies (50-300 keV) are required for this purpose, resulting in heavy damage in the implanted region. Unless proper steps are taken it becomes difficult to grow an epitaxial layer free of defects such as stacking faults. An investigation is presented here on effects of process variation on the defects in the epitaxial layers grown from SiH_4 source on <100> and <111> oriented wafers implanted with

high doses of arsenic.

Boron doped silicon wafers of 5-15 Ω-cm resistivity were implanted with 100 keV As, at a dose of 5×10^{15} ions/cm^2. During the implant wafers were kept at room temperature or liquid N_2 temperature. The two temperatures were chosen to distinguish the effect of deep disordered regions produced by the high dose implants performed at higher wafer temperatures [1.3]. At high doses the implant layers become amorphous. If an annealing is done at temperatures above 500°C, the amorphous layer on the single crystal substrate regrows epitaxially [1.2]. For high anneal temperatures (900-1000°C) the resulting annealed layers are partly polycrystalline, but a sequential anneal results in completely single crystal layers [1.4]. Therefore, two anneal cycles were employed in our studies. (1) A single step, one hour anneal in nitrogen ambient at 900°C or (2) a sequential anneal -- one hour at 400°C in N_2 followed by 15 hours at 550°C in N_2 followed by one hour at 900°C in N_2. Following the annealing some wafers were subjected to one of the two drive-ins at 1250°C: (a) 15 minutes in O_2 followed by 165 minutes in N_2, resulting in 0.13 μm thick SiO_2 growth; (b) 10 minutes in O_2 followed by 60 minutes in wet O_2 followed by 100 minutes in O_2 followed by 10 minutes in N_2 resulting in about 1 μm thick SiO_2 growth. Control wafers without any implant were also subjected to drive-ins.

After stripping off the oxide, 5 μm thick epitaxial layers were grown in a horizontal rf-heated reacter at a temperature of 1070°C. SiH_4 partial pressure was kept at 1.1×10^{-3} atm to give a growth rate of 0.6 μm/min and AsH_3 partial pressure was kept at 2×10^{-10} atm to give As concentration of 10^{15} cm^{-3} in the epitaxial layer. Prior to the growth the wafers were subjected to an HCl etch at 1180°C. On most of the wafers 0.1

μm Si was etched from the surface, however on some wafers the etch thickness was increased to 0.45 μm. After the growth the wafers were subjected to a one minute secco etch [1.5] to reveal the defects in the crystal structure. The following conclusions were reached:

(1) For identical processing the density of defects (stacking faults and dislocations) is more for <111> orientation than for <100> orientation.

(2) Sequential annealing reduces the density of defects compared to one step annealing at 900°C. This supports the study [1.4] described earlier in this paper showing that samples with single step 900°C anneal do not fully regain their crystal structure.

(3) Wafers kept at liquid N_2 temperature during the implant show much less density of defects.

(4) As compared to the 0.1 μm HCl etch the 0.45 μm etch gives much less defects, and the crystal quality of the epitaxial layer is much less dependent on the anneal-drive-in parameters. This should be expected because the thicker etch physically removes the damaged layer prior to the growth.

(5) Wafers with 1 μm SiO_2 growth during drive-in showed much less defects than with 0.13 μm SiO_2 growth. Here also the difference being the removal of the damaged Si by converting it to SiO_2. However, the advantage of this method is that because the dopant piles up in Si during the oxide growth, it is not lost unlike the HCl etch.

(6) A combination of liquid N_2 substrate temperature during implant, sequential annealing, 1 μm SiO_2 growth during the drive-in and

0.45 μm HCL etch gave the best, defect free epitaxial layers for both orientations. For the 0.45 μm HCl etch the 1 μm SiO_2 growth and liquid N_2 steps were found redundant; only the sequential annealing was found adequate to give defect free epitaxial layers as long as the drive-in was done. For the shorter etch of 0.1 μm the liquid N_2 step was necessary to obtain the defect free layers.

(7) Without doing any drive-in it is not possible to grow a defect free layer.

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2. THERMAL OXIDATION

J.D. Plummer, B.E. Deal, W.A. Tiller, C.P. Ho, R.R. Razouk

2.1 Objective

The overall goals of the thermal oxidation portion of this program may be stated as follows.

2.1.1 To achieve accurate analytic prediction of oxide thickness under all process conditions encountered in modern technologies. These include the effects of high substrate doping levels, arbitrary silicon substrate orientation, the presence of a chlorine species during the oxidation, and the use of multiple species (such as O_2/H_2O mixtures) during oxidation.

2.1.2 To achieve accurate analytic prediction of oxide charge densities, also under all process conditions important to modern devices. These conditions include arbitrary silicon substrate orientation, ambient conditions during oxidation and high and low temperature anneals.

2.1.3 To achieve accurate analytic prediction of segregation and redistribution effects at the Si-SiO_2 interface. This includes accurate prediction of dopant profiles in both the SiO_2 and Si.

2.1.4 A further important goal is the determination of an atomic level, electrically accurate model of the Si-SiO_2 interface. Such a model is believed to be essential for achieving physical understanding of oxidation kinetics, the origin of oxide charges and segregation and redistribution.

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*This work represents a joint effort by the Stanford University Integrated Circuits Laboratory, Fairchild Camera and Instrument Corporation Research and Development Laboratory and the Stanford University Department of Materials Science.

2.2 Summary of Principal Accomplishments to Date

2.2.1 Complete characterization of <111> and <100> orientation kinetics for dry O_2 and wet O_2 between 700 and 1200°C has been done.

2.2.2 Complete characterization of O_2/HCl oxidation kinetics for 0-10% HCl and T = 900 - 1100°C has been completed.

2.2.3 Complete characterization of heavily doped phosphorus substrate kinetics for $N_D = 10^{15}$ to solid solubility, T = 800 - 1100°C and dry O_2 has been completed.

2.2.4 An empirical relationship of the form

$$\frac{B}{A} = C_o e^{-\frac{E_A}{kT}} \left(1 + k_1 C_{BC} e^{k_2 C_{BC}}\right)$$

where C_{BC} is the chemical phosphorus concentration in the substrate and C_o, k_1, and k_2 are constants has been derived to model the experimental results of 3.

2.2.5 Implementation of computer prediction of first order oxidation kinetics has been realized.

2.2.6 The kinetics of H_2O and H_2O/HCl mixtures using a pyrogenic system have been studied.

The remainder of this section describes the accomplishments of the past six months.

2.3 Detailed Discussion of Results

2.3.1 Thermal Oxidation of Heavily Phosphorus Doped Silicon -- Experimental Results and Empirical Models

A brief review of general oxidation theory indicates qualitatively what may be expected in the case of heavily doped substrates or diffused regions. The macroscopic model of Deal and Grove [2.1] for silicon

oxidation by water or dry oxygen involves the diffusion of the oxidizing species from the ambient through an existing oxide to react with silicon at the Si/SiO_2 interface. Analysis based upon requiring continuity of steady-state flux of the oxidant through the ambient/oxide/interface structure yields the familiar linear-parabolic growth relationship

$$\frac{X_o^2}{B} + \frac{X_o}{B/A} = t + \tau \qquad (2.1)$$

where the terms have the same meaning as in Eq. 2.1.

For thick oxides and oxidation times long relative to a characteristic time $A^2/4B$, the first term on the left hand side of Eq. 2.1 dominates, resulting in parabolic, diffusion limited growth. Under these conditions, B is the dominant rate constant and is given by

$$B = 2D_{eff}C^*/N_1 \qquad (2.2)$$

where D_{eff} = effective diffusion coefficient of the oxidant in the oxide, C^* = equilibrium concentration of the oxidant in the oxide, and N_1 = number of oxidant molecules incorporated per unit volume of oxide grown. B exhibits an Arrhenius temperature dependence with activation energies of 1.2 eV for dry O_2 and 0.71 eV for H_2O, apparently reflecting the activation energies for the diffusivity of O_2 and H_2O, respectively, in SiO_2 [2.1].

For thin oxides and oxidation times short relative to $A^2/4B$, the second term on the left hand side of Eq. 2.1 dominates, resulting in linear interface reaction limited growth. B/A is the governing rate constant under these conditions and is given by

$$\frac{B}{A} = \frac{kh}{k + h} \frac{C^*}{N_1} \simeq k \frac{C^*}{N_1} \qquad (2.3)$$

where h = gas phase transport coefficient for the oxidizing species from the ambient to the outer oxide surface and k = Si/SiO_2 interface reaction rate constant. An activation of energy of 2 eV is observed for B/A for both dry O_2 and H_2O ambients, apparently determined by the energy required to break a Si-Si bond [2.1,2.2].

In an idealized interpretation, then, factors likely to influence the interface reaction rate should alter B/A, while those affecting oxidant diffusion will change B. Sufficiently high impurity levels in the substrate should be expected to modify the interface reaction. Similarly, high impurity content in the oxide may affect diffusivity of the oxidizing species. The relative magnitudes of such effects should depend on the particular impurity involved and its behavior during oxidation.

Specifically, phosphorus, as with the other commonly used donor impurities arsenic and antimony, diffuses more slowly in the oxide than in the silicon and tends to segregate at the interface in favor of greater phosphorus levels on the silicon side. As a result, a pile-up of phosphorus at the interface to levels greater than bulk concentrations in the silicon may occur during oxidation, with relatively much lower levels in the oxide. In addition, the pile-up should be more substantial for H_2O than for dry O_2 oxidation due to even slower diffusion relative to oxide growth rate [2.3].

Therefore, oxidation regimes dominated by the linear rate constant should exhibit greater dependence on heavy phosphorus doping level than should regimes dominated by the parabolic rate constant. Shorter oxidations

which are interface reaction rate limited should show greater variation with heavy phosphorus doping than should longer oxidations which are diffusion limited. The influence of heavy phosphorus doping via large B/A variations should also diminish or saturate with increasing oxidation temperature, since diffusion-limited oxidation dominates at shorter oxidation times with increasing temperature.

Overall, then, this qualitative model indicates that greater influence of heavy doping levels of phosphorus (and also arsenic and antimony) should be seen at shorter oxidation times and lower oxidation temperatures, and that these effects should be greater for H_2O than for dry oxygen oxidations. The validity of this simple model for the enhanced oxidation rates observed over N^+ regions will now be considered *quantitatively*.

An extensive series of oxidations were done in a dry O_2 ambient at temperatures of 800, 900, 1000, and 1100°C. The data produced are shown in Figs. 2-1 and 2-2 as oxide thickness vs. oxidation time curves for each of five heavily doped sample types and the lightly doped control. At each temperature, the bottom curve represents the lightly doped control and agrees well with published data for <111> substrates, while the additional curves represent the heavily doped samples, in order of increasing substrate doping. Specific doping levels are indicated in Table I. Both SIMS and AES techniques were used to measure chemical phosphorus concentration C_{BC}; spreading resistance and anodic oxidation techniques were used to measure the electically active concentrations C_{BE}.

The data in Figs. 2-1 and 2-2 already lends qualitative support to the predictions based on the simple interpretations of doping effects

presented earlier. Clearly the greatest relative variations of oxide thickness occur at the shorter times and lower temperatures, the regions in which the interface reaction and hence B/A are expected to dominate, indicating that the increasing substrate phosphorus level has a very strong effect on the interface reaction. At the longer times and higher temperatures, in the diffusion-limited regime, substantially less variation of thickness with doping is seen, implying that oxidant diffusion and the parabolic rate constant are influenced to a much smaller extent by the increasing substrate phosphorus levels. Indeed, a few selected oxidations at 1200°C, when the characteristic time $A^2/4B$ for lightly doped substrate oxidations is only about 0.5 minutes and therefore oxidation is effectively entirely B dominated, produced essentially no variation of oxide thickness with increasing phosphorus doping that could be resolved within the limits of interferometer accuracy.

The variation of the effective B/A and B values with increasing initial substrate total chemical phosphorus concentration, representatively illustrated in Fig. 2-3 for 900°C dry O_2 oxidation, exhibits dramatically the expected behavior. B/A, reflecting interface reaction-limited oxidation, increases sharply by more than an order of magnitude as the phosphorus level rises toward solid solubility. On the other hand, B, which represents the diffusion-limited regime, is affected only slightly by the increasing substrate phosphorus doping. Clearly, the predictions of the simplified interpretations presented have been convincingly confirmed. We now consider the effects on B/A and B in detail.

(a) Linear Rate Constant. The temperature dependence of B/A is shown in Fig. 2-4, where log (B/A) is plotted against 1/T with substrate

doping level as a parameter. The lowest points are the values found for the lightly doped control samples, while the higher points correspond, respectively, to the increasingly heavily phosphorus doped substrate types used. To a reasonable approximation, Arrhenius temperature dependence may be assumed for the effective B/A values corresponding to each substrate doping level, leading to the least-squares fitted lines and apparent activation energies of the figure.

High impurity levels may produce the large increases of effective B/A by altering the activation energy and/or the pre-exponential factor. Apparently the basic limiting activation energy of approximately 2 eV associated with the interface reaction is not substantially altered by the high phosphorus levels, while significant dependence on dopant concentration may be found in the pre-exponential factor. A physical explanation for this relatively constant activation energy will be given later in this report.

Some indication of the nature of this dependence may be gained via examination of the variation of B/A with concentration at a given temperature, as was done in Fig. 2-3 for 900°C. The sharp increase of the linear rate constant suggests an exponential dependence on C_{BC}, the initial chemical substrate phosphorus concentration, a possibility that is tested further by investigating the variation of log (B/A) with C_{BC} in Fig. 2-5. Evidently log (B/A) eventually exhibits roughly a linear dependence on C_{BC}, and hence B/A an exponential dependence on C_{BC}, at each given temperature, but only after a stronger initial increase. There may be a slight temperature dependence in the magnitude of this initial increase, but to a large extent the substrate background phosphorus concentration dependence is very similar at all temperatures.

Clearly, many closed-form relationships for this C_{BC} dependence may be used to approximate this data to varying degrees of complexity, in the absence of an accurate physical model for that dependence. A fairly simple form, producing a reasonable first order approximation, might be

$$\frac{(B/A)}{C_o e^{-E_1/kT}} \equiv (B/A)' = 1 + k_1 C_{BC}^{n_1} e^{k_2 C_{BC}} \qquad (2.4)$$

where $C_o e^{-E_1/kT}$ is the published temperature dependence of the linear rate constant for lightly doped substrates with $E_1 \simeq 2$ eV [2.1]. Thus, the exponential eventually dominates, but the power law dependence produces the stronger initial increase. Optimal k_1 and k_2 values may be found by rewriting Eq. 2.4 in the alternative form

$$\log\left[\frac{(B/A)' - 1}{C_{BC}^{n_1}}\right] = \log k_1 + k_2 C_{BC} \qquad (2.5)$$

Plotting $\log\left[\frac{(B/A)' - 1}{C_{BC}^{n_1}}\right]$ vs. C_{BC} should therefore produce a linear dependence with intercept $\log k_1$ and slope k_2, for an appropriate value of n_1. Such analysis indicates that a value of $n_1 \simeq 0.5 - 1.0$ should be used, with $n_1 \simeq 0.5$ giving particularly consistent linear dependences. Thus, the curves plotted together with the experimental B/A values in Fig. 2-5 have been calculated using $n_1 = 0.5$ and the resulting appropriate k_1 and k_2 values. Agreement appears very reasonable. The fitted k_1 and k_2 values are presented vs. 1/T in Fig. 2-6, confirming that the temperature dependence is relatively

slight when compared with the overall dependence of B/A. In fact, appropriate constant values of k_1 and k_2 independent of T conceivably could be used for all temperatures. While agreement not surprisingly is not as good, using values of $k_1 = 5.9 \times 10^{-11}$ $cm^{3/2}$ and $k_2 = 3.0 \times 10^{-21}$ cm^3 gives reasonable agreement with the experimental results over the entire temperature range investigated. Use of Eq. 2.4 with these values for k_1, k_2 and n, allows calculation of effective linear rate constants for arbitrary substrate phosphorus doping levels.

(b) Parabolic Rate Constant. B has been found to be a much weaker function of high phosphorus concentrations. Nevertheless, it does appear to increase somewhat with concentration, as seen in Fig. 2-7, where log B is plotted vs. 1/T with substrate doping as a parameter. At each temperature, the lowest point represents the lightly doped control while the higher points correspond to the heavily doped samples. It is apparent that, unlike the case for B/A, the concentration dependence of B varies significantly with temperature. Dopant level has a greater effect at lower temperatures and virtually no effect at 1100°C. Also, for a given doping level, the net temperature dependence is not readily reconcilable with a single activation energy Arrhenius relation, implying changes in activation energy and a temperature-dependent pre-exponential factor, or addition of a new, phosphorus-related term with different activation energy. Fig. 2-8, presenting log B vs. C_{BC} with temperature as parameter, emphasizes this additional temperature dependence. Further, the dopant concentration effects at a given temperature become evident. As substrate doping level increases (and consequently the lower phosphorus level in the oxide also rises), B first increases rapidly and then begins to "saturate," increasing only very slowly, if at all.

As with B/A, a convenient closed-form approximation of the B variations may be made. For convenience, no new explicit T dependence is included, but the fitted "constants" should then reflect any dependence thus hidden. The initial rapid rise and subsequent sluggishness suggest a possible power law dependence on dopant levels. Initial substrate phosphorus level is used as the variable for this analysis, though actual levels in the oxide should be more directly relevant, as discussed in [2.4].

$$\frac{B}{B_o e^{-E_2/kT}} \equiv B' = 1 + k_3 C_{BC}^{n_2} \qquad (2.6)$$

where $B_o e^{-E_2/kT}$ is the published temperature dependence of the parabolic rate constant for lightly doped substrates with $E_2 \simeq 1.2$ eV for dry O_2 [2.1].

Appropriate k_3 and n_2 values may be extracted in a manner analogous to Eq. 2.5. This approach was used with the extracted B values for 800, 900, and 1000°C, with surprisingly good linear relations found. The calculated curves in Fig. 2-8 illustrate the very reasonable fit to the extracted B values produced by the above relation with the k_3 and n_2 values shown vs. 1/T in Fig. 2-9. The expected additional T dependence is clearly evident in k_3 and possibly, to a lesser extent, in n_2. A new additional activation energy is strongly suggested, and this will be explored. Until a model related to basic physical phenomena is derived to explain these effects on B, Eq. 2.6 can be used to calculate effective parabolic rate constants for substrates with arbitrary phosphorus doping levels.

2.3.2 H_2O and HCl/H_2O Pyrogenic Steam Oxidation Kinetics

The kinetics of steam oxidation of silicon over the temperature range 900° to 1100°C was investigated using a pyrogenic system. This system involves the direct reaction of H_2 and O_2 in the oxidation furnace to form H_2O. It was found that such a system does not permit 100 percent (760 Torr) water to be produced. Therefore, a ratio of H_2 to O_2 was selected which provides a vapor pressure of water equal to that obtained in a previous investigation where O_2 was bubbled through 95°C H_2O [2.1]. This H_2O pressure is 640 Torr.

A log-log plot of oxide thickness vs. oxidation time is presented in Fig. 2-10 for <111> and <100> oriented n-type silicon ($C_B = 10^{15}$ cm^{-3}). Data from [2.1] obtained at 1200°C for wet O_2 are also included in the figure, with little difference between <111> and <100> silicon being observed at this temperature. Data were also obtained in the pyrogenic system at 950° and 1050°C but are not included in Fig. 2-10 because of space limitations.

Rate constants, B and B/A, were obtained and are plotted vs. 1/T in Figs. 2-11 and 2-12. Activation energies are indicated and agree reasonably well with previous results. In the case of the linear rate constant, B/A, a constant ratio of 1.68 is obtained between the pre-exponential constants of <111> to <100> oriented silicon. On the other hand, the B/A activation energies of the two orientations (2.05 eV) are equal.

Included in Figs. 2-11 and 2-12 are corresponding data for dry O_2 oxidations. The one important observation is that previously the <100> Si B/A activation energy data for dry O_2 did not permit a straight line to be drawn through the scattered points. If the constant <111>/<100> ratio of 1.68 from steam oxidation is assumed, then a plot can be forced through the

dry O_2 <100> data points. This has been done in Fig. 2-12 and a reasonable fit for the data results.

Oxidations in H_2O with additions to 5 volume percent HCl were carried out over the temperature range 900° to 1100°C. Not only did the oxidation rate not increase, it actually decreased. This decrease was found to be approximately 5 percent, the same amount as the HCl added. It was therefore concluded that the addition of HCl to an H_2O oxidation ambient only serves to dilute the oxidizing species. On the other hand, the presence of the HCl provides a cleaning action, and the oxides produced exhibit much less contamination effects.

Table I

Electrically Active C_{BE} and Chemical C_{BC} Dopant Concentrations in Heavily Phosphorus Doped Samples

Sample	C_{BE}	C_{BC} SIMS	C_{BC} AES
A	($\sim 10^{15}$)	———	———
B	5.1×10^{19}	5.5×10^{19}	5.2×10^{19}
C	7.2×10^{19}	1.5×10^{20}	8.2×10^{19}
D	1.8×10^{20}	2.4×10^{20}	2.8×10^{20}
E	2.8×10^{20}	4.5×10^{20}	5.0×10^{20}
F	3.2×10^{20}	7.0×10^{20}	6.8×10^{20}

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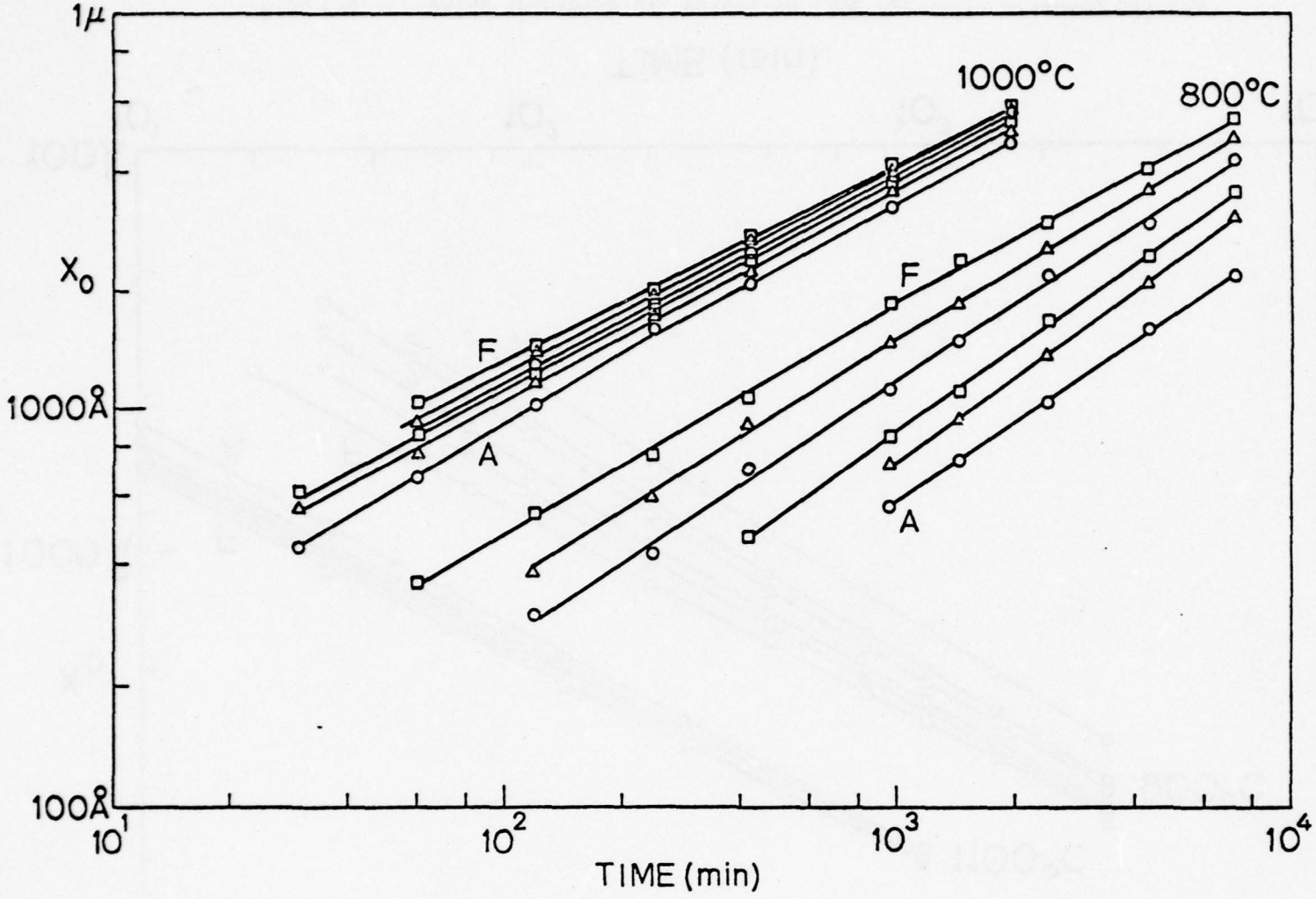

Fig. 2-1. Oxide thickness vs. oxidation time for <111> oriented silicon in dry O_2 ambient with substrate phosphorus doping level as parameter, at 800 and 1000°C.

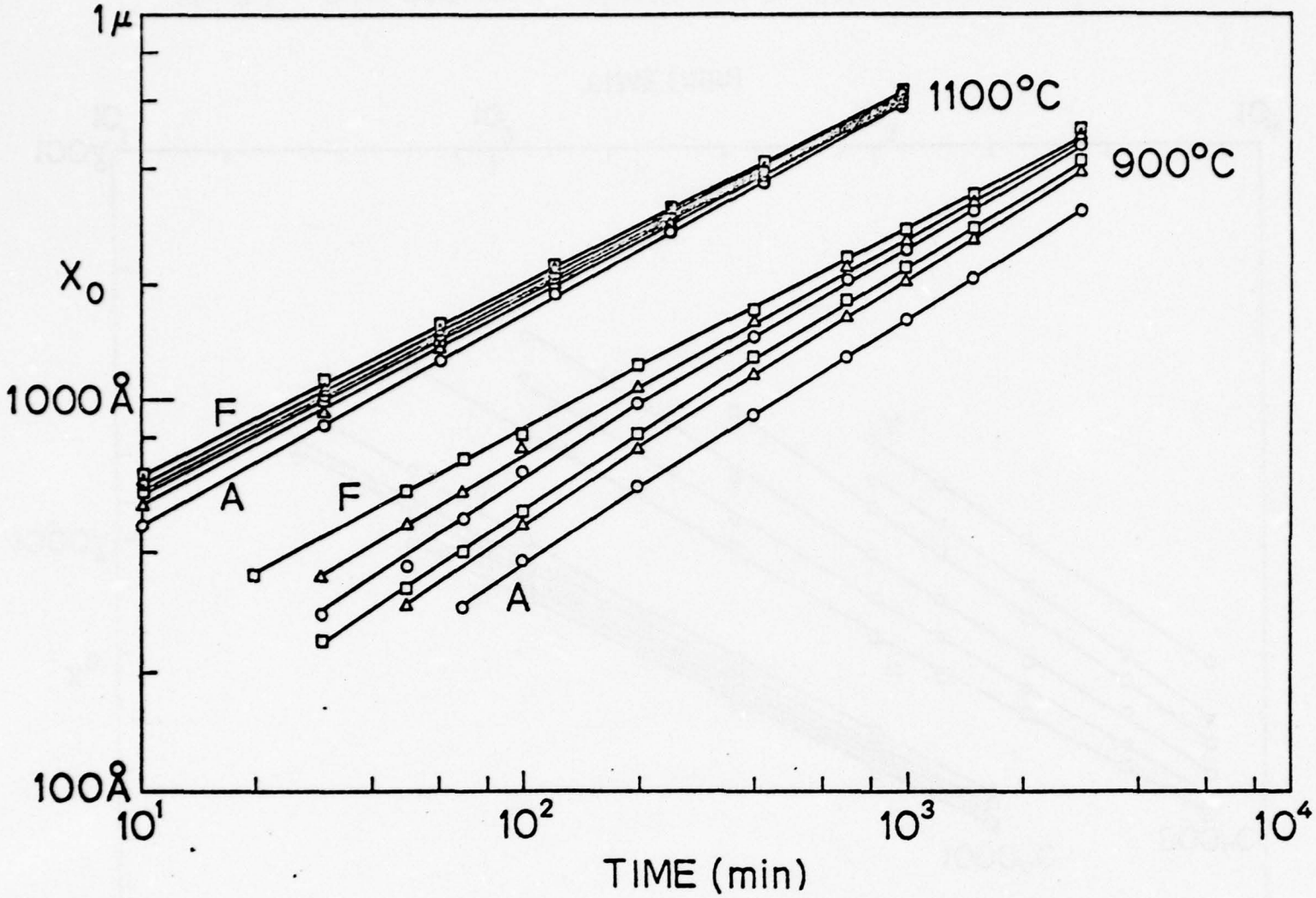

Fig. 2-2. Oxide thickness vs. oxidation time for <111> oriented silicon in dry O_2 ambient with substrate phosphorus doping level as parameter, at 900 and 1100°C.

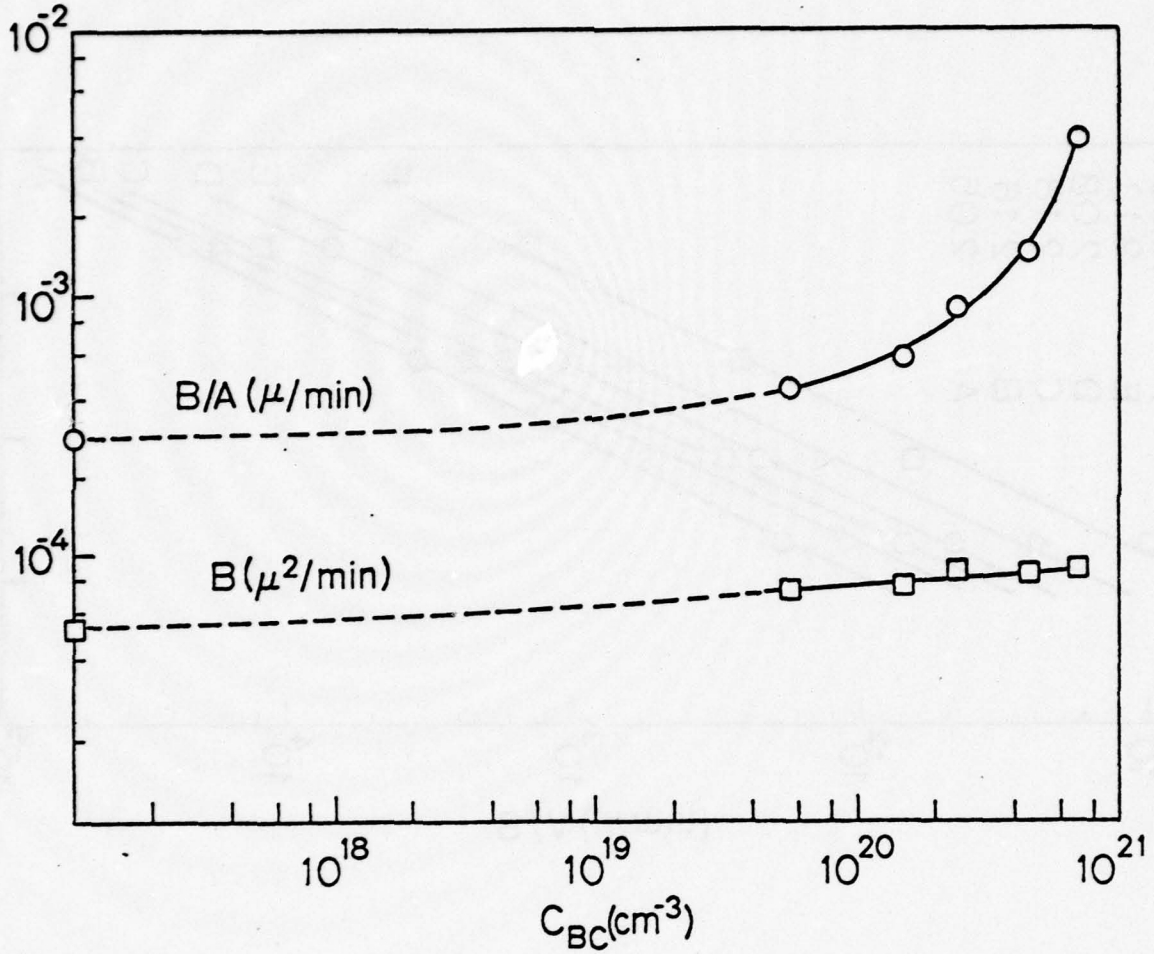

Fig. 2-3. Oxidation rate constants vs. initial substrate chemical phosphorus doping level at 900°C.

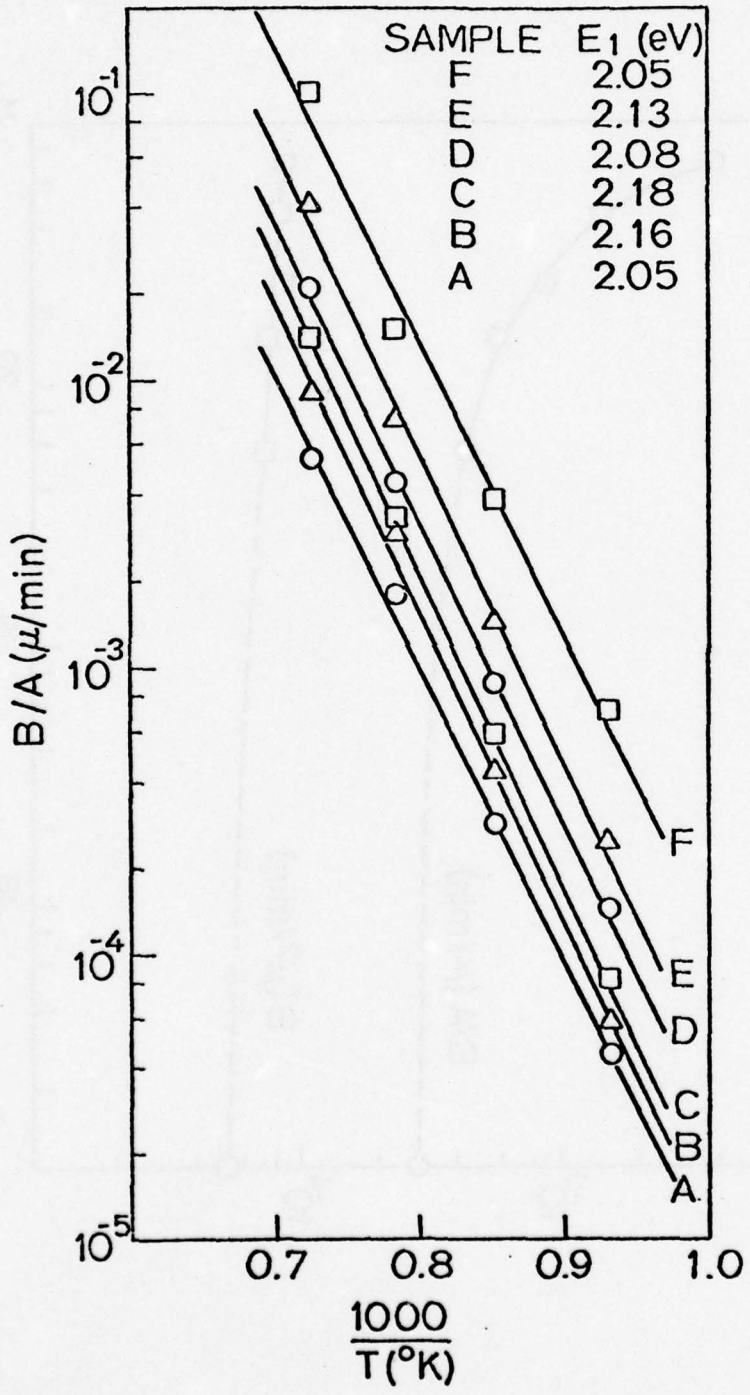

Fig. 2-4. Linear rate constant temperature dependence and effective activation energies with substrate phosphorus doping level as parameter.

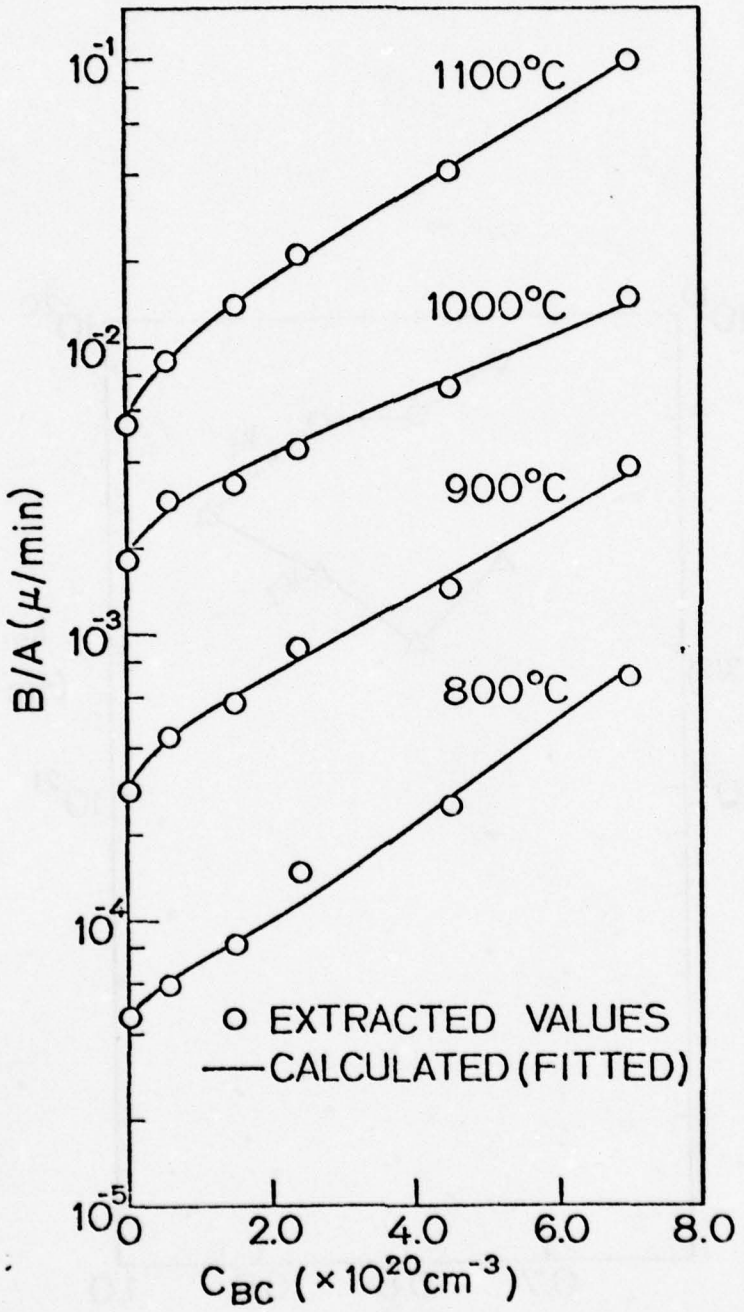

Fig. 2-5. Linear rate constant vs. initial substrate chemical phosphorus doping level with oxidation temperature as parameter.

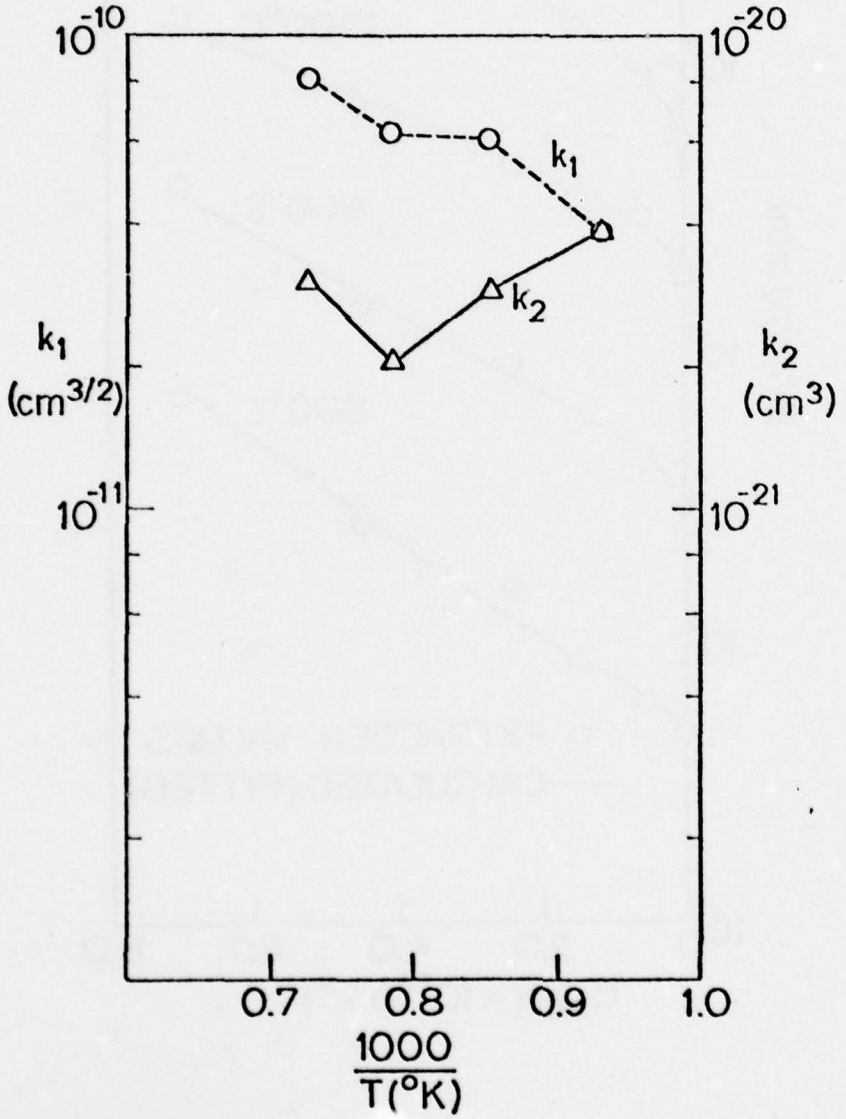

Fig. 2-6. Fitted parameters vs. 1/T for linear rate constant dependence on initial substrate chemical phosphorus doping level.

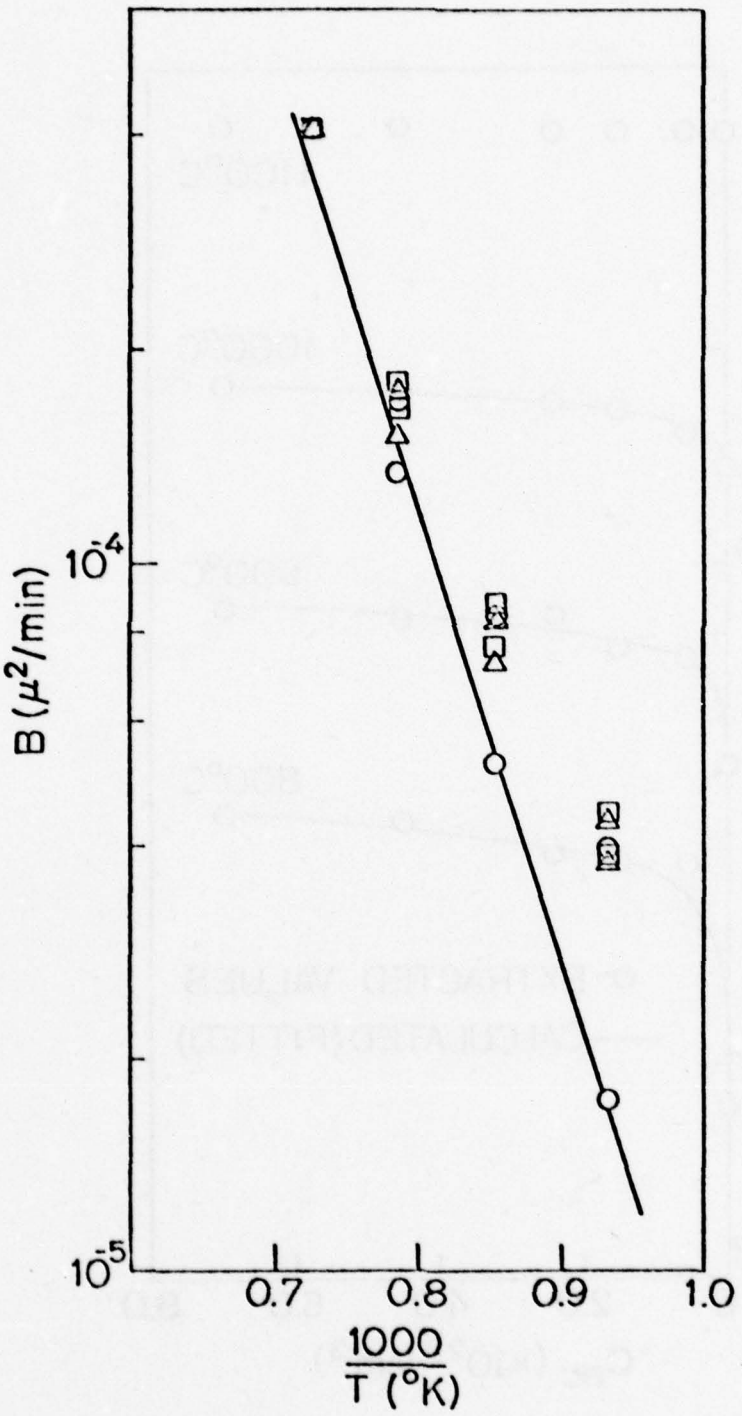

Fig. 2-7. Parabolic rate constant temperature dependence with substrate phosphorus doping level as parameter.

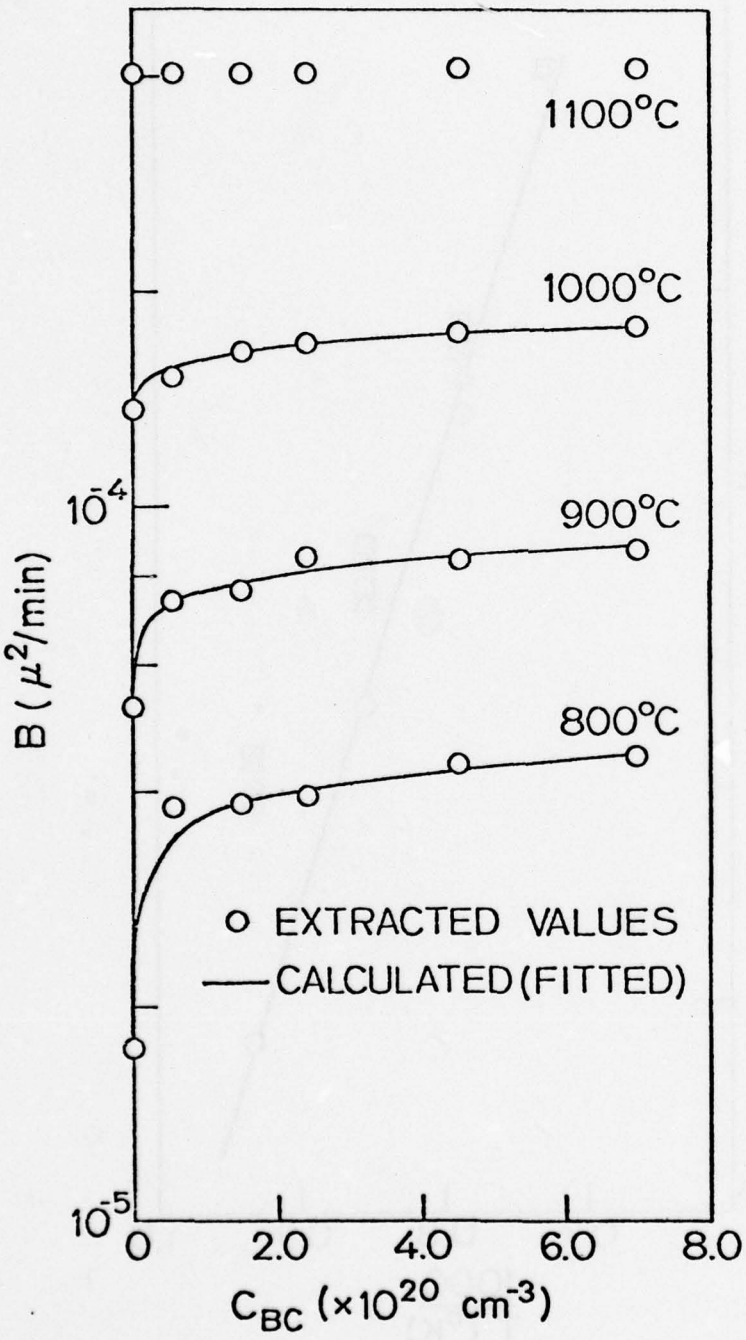

Fig. 2-8. Parabolic rate constant vs. initial substrate chemical phosphorus doping level with oxidation temperature as parameter.

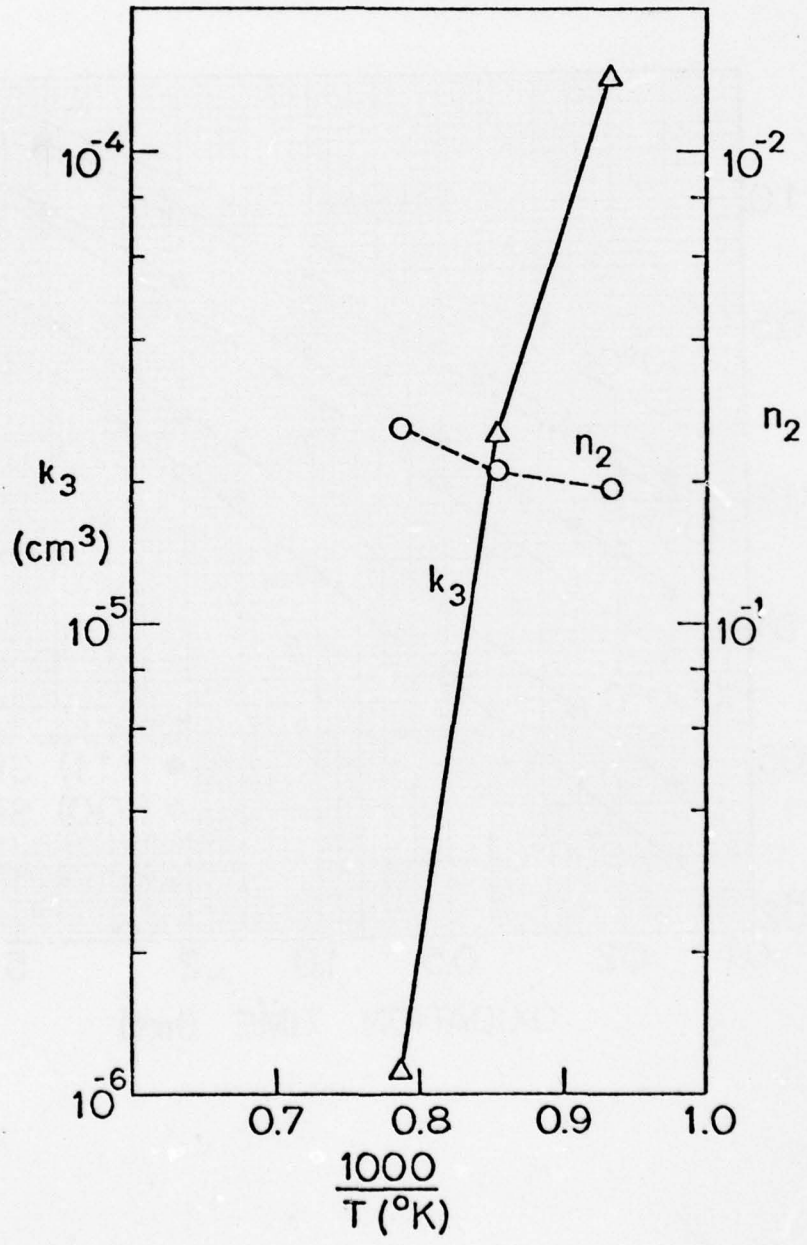

Fig. 2-9. Fitted parameters vs. 1/T for parabolic rate constant dependence on initial substrate chemical phosphorus doping level.

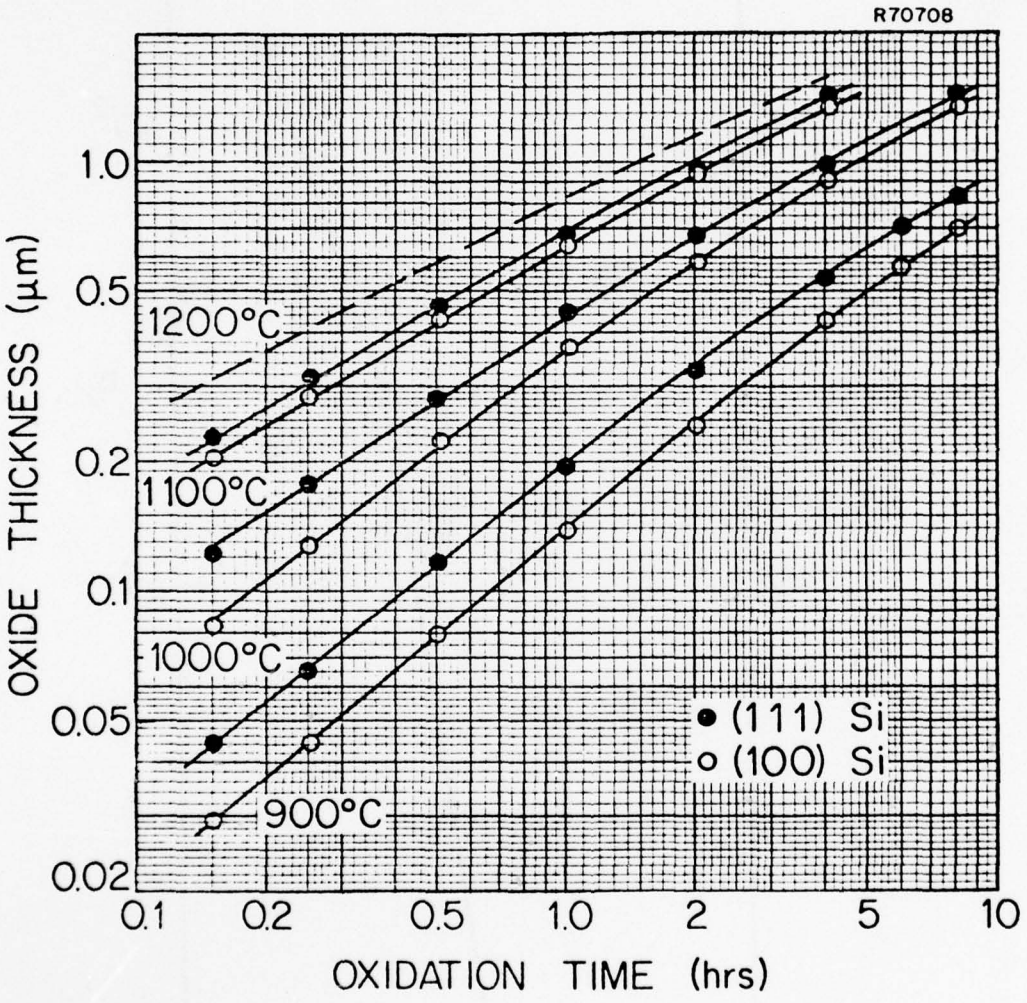

Fig. 2-10. Oxide thickness vs oxidation time for silicon oxidation in H_2O (640 Torr).

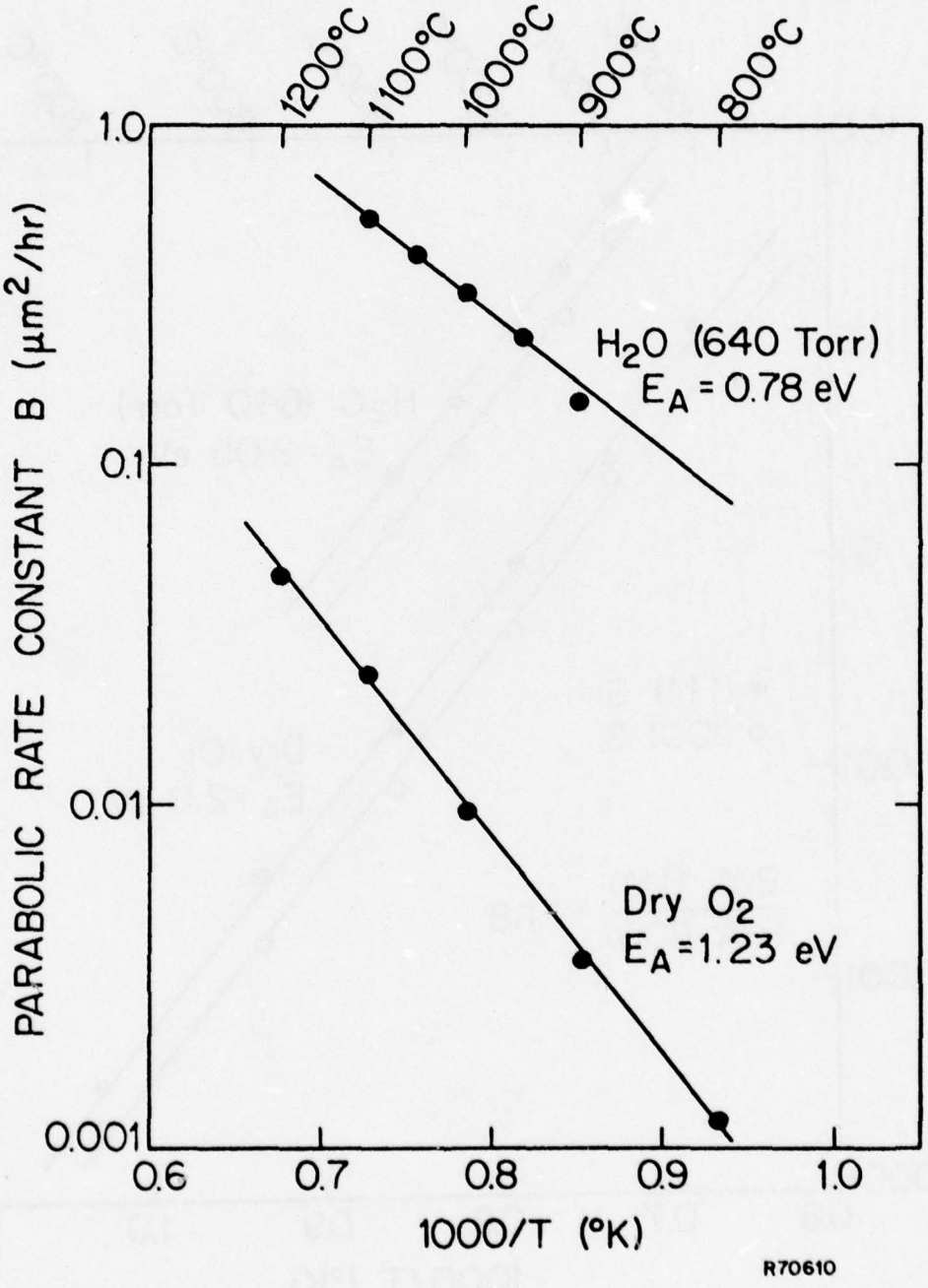

Fig. 2-11. Dependence of parabolic rate constant B on temperature for the thermal oxidation of silicon in pyrogenic H_2O (640 Torr) or dry O_2.

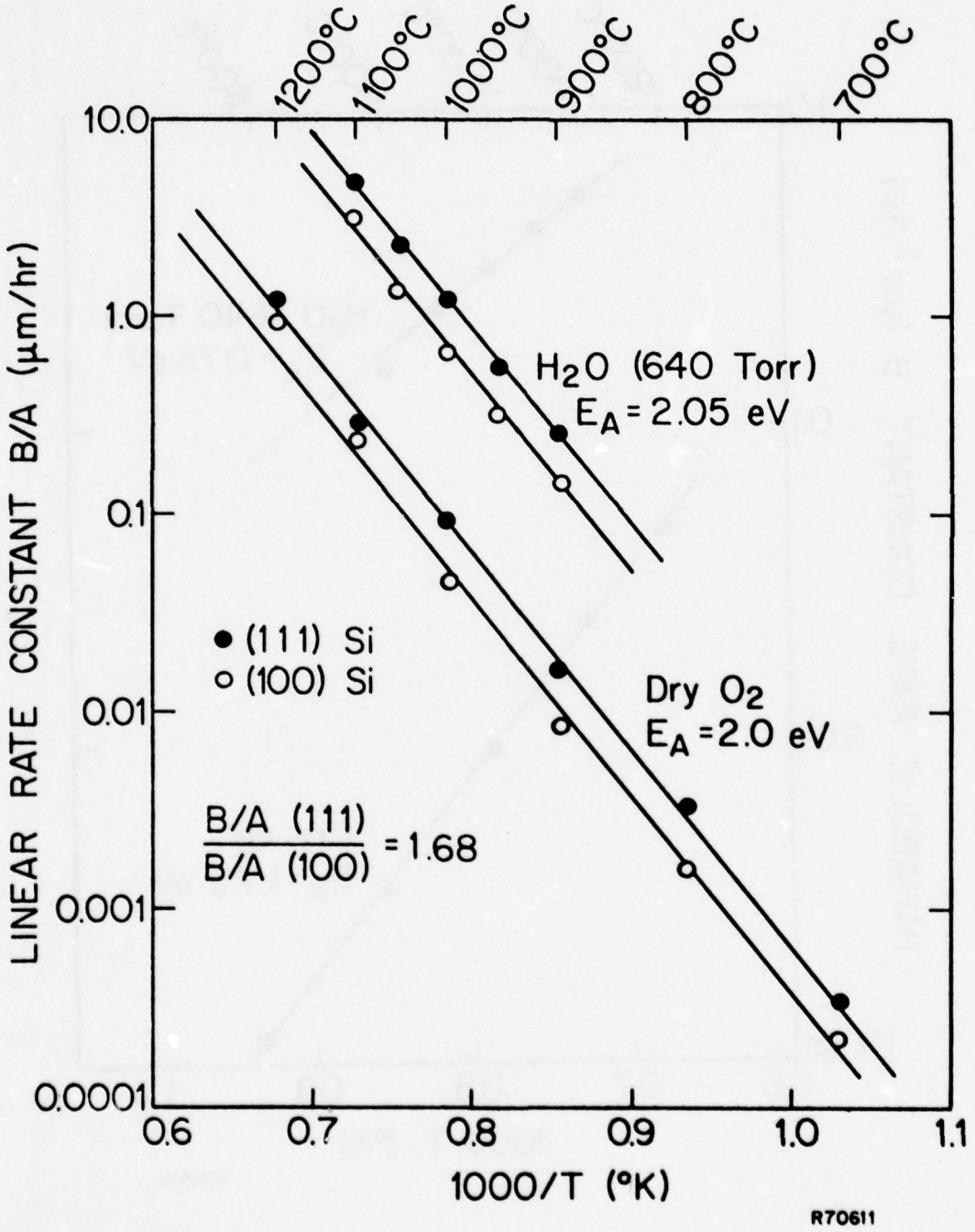

Fig. 2-12. Dependence of linear rate constant B/A on temperature for the thermal oxidation of silicon in pyrogenic H_2O (640 Torr) or dry O_2.

3. CHEMICAL VAPOR DEPOSITION OF SILICON

K.C. Saraswat, T.I. Kamins, R. Reif, M. Mandurah

3.1 Objective

The overall objective of the research in the field of chemical vapor deposition of silicon is to develop physical models in the following areas:

(1) Kinetics of growth of epitaxial silicon

(2) Kinetics of dopant inclusion in epitaxial layers

- growth of uniformly doped layers
- transient response study and system transfer function of the epitaxial reactor
- growth of arbitrarily doped layers using the transfer function approach

(3) Effects of existing layer dopants

- outdiffusion and autodoping
- substrate dopant effects on film induction and defects
- two dimensional effects: geometry limitations

(4) Polycrystalline silicon studies

- atmospheric and low pressure deposition modeling
- physical properties of the films
- electrical properties of the films

3.2 Summary of the Principal Accomplishments to Date

2.3.1 An investigation has been conducted to relate the steady state gas phase dopant (AsH_3, PH_3, B_2H_6 and $Sb(CH_3)_3$) concentration to the resulting doping density of As, P, B and Sb, in homogeneous epitaxial films of silicon grown from SiH_4 and $SiCl_4$, in the temperature range of 1050°C to 1180°C. The investigation is novel for AsH_3, B_2H_6 and $Sb(CH_3)_3$. For PH_3 the results

agree with work done by others.

3.2.2 An investigation has been conducted to study the effect of growth rate on dopant incorporation in the epitaxial films. The dopants studied were As and Sb (from AsH_3 and $Sb(CH_3)_3$). The trapping phenomenon was observed in the case of Sb. Similar study on B and P has also been started.

3.2.3 Transient response of the dopant (As and P) incorporation process has been determined by studying the doping profiles that resulted from step changes in the dopant gas (AsH_3 and PH_3) flow during the deposition while the SiH_4 flow was kept constant. The object of this project was to determine relationships between the time variation of the dopant gas flow and the spatial variation of the dopant concentration in the epitaxial film. By studying the step response of the system a transfer function has been calculated to achieve the above objective. This approach should be useful in fabricating arbitrarily varying dopant concentrations needed for certain desired device characteristics.

3.2.4 A fundamental study is being conducted to understand the following aspects of the dopant incorporation process.

(1) Dopant gas transport from the gas distribution system to the surface of the epitaxial film.

(2) Dissociation of the dopant gas into different constituents in thermodynamic equilibrium.

(3) Adsorption of these dopant constituents at the surface of the silicon.

(4) Surface chemical reactions.

(5) Desorption of the products of the chemical reaction.

(6) Dopant incorporation in the crystal lattice.

Thermodynamic equations have been written for each of the above six processes. By solving these equations a generalized model is being developed to explain various aspects of the dopant incorporation process in epitaxial films. With the help of experimental results obtained in 1, 2 and 3, various parameters of this model are being calculated. This model explains both the steady state as well as transient aspects of the dopant incorporation.

3.2.5 An investigation has been started to study the deposition of silicon at low pressure in a hot wall reactor. In the initial studies conducted, x-ray and TEM techniques have been used to determine the physical characteristics of these films and the effect of heat treatment on their properties.

Section 3.3 summarizes the principal results of the first six months of the second year of this program.

3.3 Detailed Discussion of Results

3.3.1 Transient and Steady State Response of the Dopant System of an Epitaxial Reactor: Growth Rate Dependence

A physical model for the dopant inclusion into silicon epitaxial films is being developed at the Stanford Integrated Circuits Laboratory [3.1, 3.2]. The transient and steady state response of the dopant system were studied at different growth rates to gather information about the fundamentals of dopant incorporation. The experiments showed the presence of two regions of operation and provide insight leading to a better understanding of the doping process.

The experiments were carried out in a horizontal, water-cooled, rf-heated epitaxial reactor with an effective cross section of 27 cm^2 above the susceptor. Hydrogen was used as the carrier gas at a velocity of 34

cm/sec (at room temperature). Silane was used as the silicon source, and arsine diluted in hydrogen was the dopant source. The corrected wafer surface temperature was approximately 1070°C.

The transient investigation involved the study of doping profiles that resulted from step changed in the dopant gas flow during the deposition while the silane flow was kept constant. The experiments reported here correspond to changes between arsine partial pressures which produce dopant concentrations of roughly 1×10^{15} and 3×10^{15} cm^{-3}. The transient experiment was carried out at 0.14, 0.32, 0.6 and 1.3 μm/min. The substrates were phosphorus-doped, (100)-oriented silicon wafers with resistivities between 5 and 10 ohm-cm. The resulting impurity profiles in the epitaxial layers were determined by capacitance-voltage measurements on planar p-n junctions, mesa p-n junctions and deep depletion MOS structures [3.3].

Typical results from the transient experiments are shown in Fig. 3-1, where the measured dopant concentration is plotted as a function of distance from the surface of the epitaxial film for a decreasing step change in the dopant gas flow during the deposition [3.1]. The impurity profiles obtained for growth rates of 0.6 and 1.3 μm/min are indistinguishable (solid curve), and both differ strongly from the one obtained at 0.14 μm/min, which changes much more abruptly with distance (dotted curve).

An excellent fit to the data can be obtained by using the expression [3.2]

$$N(x) = N_I + (N_F - N_I)\left[1 - \exp\left(-\frac{x-x_o}{L(g)}\right)\right] \quad \text{for } x \geq x_o \qquad (3.1)$$

where

N(x) = dopant concentration at a distance x from the substrate

N_I = initial doping level for $x < x_o$

N_F = final doping level

L(g)= decay length (a function of the growth rate g)

x_o = distance from the substrate at which the transient begins ($x_o = gT_o$)

The same expression also fits the doping profile corresponding to an increasing step change in the dopant gas flow [3.2].

Figure 3-2a shows the decay length as a function of growth rate. Each decay length was obtained by using data similar to Fig. 3-1 together with Eq. 3.1. At 0.6 and 1.3 μm/min the decay lengths are equal (see Fig. 3-1), but at lower growth rates the decay length decreases with decreasing growth rate. Let us call the low-growth-rate region of operation region I and the high-growth-rate region ($g \geq 0.6$ m/min) region II.

The fact that in region II the decay length is independent of the growth rate is very significant. The time that it takes to grow a thickness of epitaxial silicon equal to one decay length is given by L/g. Since in region II the decay length remains constant, the transient dies out faster at higher growth rates. This, in turn, implies that in this region of operation, the mechanism responsible for the transient behavior is related to the growing surface and not the gas phase.

The steady state experiments involved studying the effect of the silicon deposition rate on the impurity concentration of uniformly doped epitaxial layers. The arsine partial pressure was kept at 6.2×10^{-10} atm, and the silane partial pressure was adjusted to give growth rates varying from 0.13 μm/min to 1.2 μm/min (2.7×10^{-4} - 2.3×10^{03} atm). The thicknesses of the epitaxial layers were kept between 5.5 and 8.1 μm and were measured

by a groove-and-stain technique. A four-point probe was used to determine the resistivity of the layers. The substrates were boron-doped, (100)-oriented silicon wafers with resistivities ranging from 1-4 ohm-cm.

The results of the steady state experiments are shown in Fig. 3-2b, where the impurity concentrations of uniformly doped epitaxial layers are plotted vs. silicon deposition rate. A simple model considering mass transport through the boundary layer, physical-chemical reactions at the growing surface, and thermodynamic equilibrium is sufficient to explain the data. At growth rates greater than approximately 0.6 μm/min (region II) the doping density has been found here (Fig. 3-2b) and in other laboratories [3.4] to become inversely proportional to the silicon deposition rate as indicated by a slope of -1 on a log-log plot. In this region the dopant inclusion rate has reached a maximum and will be shown to be limited by the rate of a physical-chemical reaction taking place at the surface [3.5]. At growth rates less than approximately 0.6 μm/min the doping density varies less rapidly than g^{-1} and at very low growth rates (region I) tends to become constant at an impurity concentration dictated by thermodynamic considerations.

3.3.2 A Model for Dopant Incorporation into Silicon Epitaxial Films

A model has been developed to describe the incorporation of dopant atoms into silicon epitaxial films during deposition from a SiH_4-AsH_3-H_2 mixture in a horizontal, atmospheric-pressure, epitaxial reactor. The model explains both the transient and steady state responses of the dopant system [3.1,3.5] and can be used to derive the "transfer function" of the dopant system [3.2], i.e. an expression relating the time variation of the gas-phase dopant concentration to the spatial variation of the epitaxial

layer dopant concentration.

The model considers processes occurring both in the gas phase and at the surface. The sequence of steps in the gas phase is shown in Fig. 3-3: (1) Mass transport of the dopant compound (AsH_3) from the reactor-tube entrance to the deposition region. (2) Mass transport of AsH_3 from the well-mixed main gas stream through the boundary layer to the growing surface. (3) Gas-phase chemical reactions, in which AsH_3 may dissociate into several different As-containing compounds, particularly AsH_2. The sequence of steps occurring at the surface is shown in Fig. 3-4. (4) Adsorption of the As-containing compound on the growing surface. (5) Chemical dissociation into As and H in the adsorbed layer. (6) Surface diffusion and incorporation of adsorbed As at atomic steps and kink sites on the surface. (7) "Burying" of the incorporated As atoms by subsequently arriving Si atoms during epitaxial growth. (8) Desorption of hydrogen from the surface.

By analyzing the sequence of steps listed above, a model can be derived to describe mathematically the doping process. Under steady state conditions all of the steps occur at the same rate. Under this condition the epitaxial layer dopant distribution is uniform. However, when the dopant gas flow is a function of time, the doping process may be in a transient state. During this transient, all of the steps involved in the doping process no longer occur at the same rate, and the correct physical picture is properly described by considering mass-balance of the As-containing compounds at each of the steps in the process.

Considering conservation of As between each of the steps mentioned above, the following mass-balance-type equations result:

1. Mass balance of AsH_3 within the deposition volume:

$$\left[\begin{array}{l}\text{net rate of } AsH_3 \\ \text{entering the} \\ \text{deposition} \\ \text{volume } (r_M)\end{array}\right] - \left[\begin{array}{l}\text{rate at which } AsH_3 \text{ leaves} \\ \text{the main gas stream towards} \\ \text{the wafer surface } (r_m)\end{array}\right] = \left[\begin{array}{l}\text{rate of change of } AsH_3 \\ \text{concentration in the} \\ \text{main gas stream within} \\ \text{the deposition volume}\end{array}\right] \qquad (3.2)$$

2. Mass balance of AsH_3 above the gas-crystal interface:

$$\left[\begin{array}{l}\text{rate at which} \\ AsH_3 \text{ arrives at} \\ \text{the gas-crystal} \\ \text{interface } (r_m)\end{array}\right] - \left[\begin{array}{l}\text{net rate of} \\ AsH_3 \text{ adsorption} \\ \text{on the growing} \\ \text{surface } (r_1)\end{array}\right] - \left[\begin{array}{l}\text{net rate of} \\ \text{gas phase} \\ \text{chemical} \\ \text{reaction } (r_5)\end{array}\right] = \left[\begin{array}{l}\text{rate of change of gas} \\ \text{phase } AsH_3 \text{ concentra-} \\ \text{tion above the} \\ \text{gas-crystal interface}\end{array}\right] \qquad (3.3)$$

3. Mass balance of AsH_2 above the gas-crystal interface:

$$\left[\begin{array}{l}\text{net rate of} \\ \text{formation of} \\ AsH_2 \ (r_5)\end{array}\right] - \left[\begin{array}{l}\text{net rate of adsorption} \\ \text{of } AsH_2 \text{ on the surface} \\ (r_6)\end{array}\right] = \left[\begin{array}{l}\text{rate of change of gas} \\ \text{phase } AsH_2 \text{ concentration} \\ \text{above the gas-crystal} \\ \text{interface}\end{array}\right] \qquad (3.4)$$

4. Mass balance of AsH_3 adsorbed on the surface:

$$\left[\begin{array}{l}\text{net rate of} \\ \text{adsorption of} \\ AsH_3 \text{ on the} \\ \text{surface } (r_1)\end{array}\right] - \left[\begin{array}{l}\text{net rate of chemical} \\ \text{dissociation of } AsH_3 \\ \text{on the surface } (r_2)\end{array}\right] = \left[\begin{array}{l}\text{rate of change of the} \\ \text{surface density of} \\ \text{adsorbed } AsH_3\end{array}\right] \qquad (3.5)$$

5. Mass balance of AsH_2 adsorbed on the surface:

$$\left[\begin{array}{l}\text{net rate of} \\ \text{adsorption of} \\ AsH_2 \text{ on the} \\ \text{surface } (r_6)\end{array}\right] - \left[\begin{array}{l}\text{net rate of chemical} \\ \text{dissociation of } AsH_2 \\ \text{on the surface } (r_7)\end{array}\right] = \left[\begin{array}{l}\text{rate of change of the} \\ \text{surface density of} \\ \text{adsorbed } AsH_2\end{array}\right] \qquad (3.6)$$

6. Mass balance of As adsorbed on the surface:

$$\left[\begin{array}{l}\text{net rate of} \\ \text{formation of As} \\ \text{adsorbed on the} \\ \text{surface } (r_2 + r_7)\end{array}\right] - \left[\begin{array}{l}\text{net rate of incorporation} \\ \text{of adsorbed As into step} \\ \text{or kink sites on the} \\ \text{surface } (r_3)\end{array}\right] = \left[\begin{array}{l}\text{rate of change of the} \\ \text{surface density of} \\ \text{adsorbed As}\end{array}\right] \qquad (3.7)$$

7. Mass balance of As occupying incorporation sites:

$$\left[\begin{array}{l}\text{net rate of} \\ \text{incorporation of} \\ \text{As into step or} \\ \text{kink sites on the} \\ \text{surface } (r_3)\end{array}\right] - \left[\begin{array}{l}\text{rate of "burying" the} \\ \text{incorporated As by} \\ \text{silicon atoms } (r)\end{array}\right] = \left[\begin{array}{l}\text{rate of change of the} \\ \text{surface density of As} \\ \text{occupying incorporation} \\ \text{sites}\end{array}\right] \qquad (3.8)$$

When mathematical expressions are substituted in Eqs. 3.2-3.8 above, a system of seven first order linear differential equations results. These equations contain the mathematical description of the doping process and can be used to explain (1) the steady state dopant concentration in the epitaxial film as a function of gas-phase dopant molar fraction and epitaxial growth rate [3.5], and (2) the transient response of the dopant system and its growth rate dependence [3.1,3.5]. They may also be used to derive the "transfer function" of the dopant system [3.2].

One convenient way to handle this system of equations is to construct an electric circuit represented by an analogous system of equations. An R-C circuit corresponding to the system of equations derived for the dopant system is shown in Fig. 3.5. Each resistor represents one of the mechanisms occurring during the doping process; current is analogous to reactant flow, and voltage is analogous to the molar fractions of the dopant species. This circuit representation of the dopant system provides insight into the different mechanisms taking part in the doping process and their relative importance.

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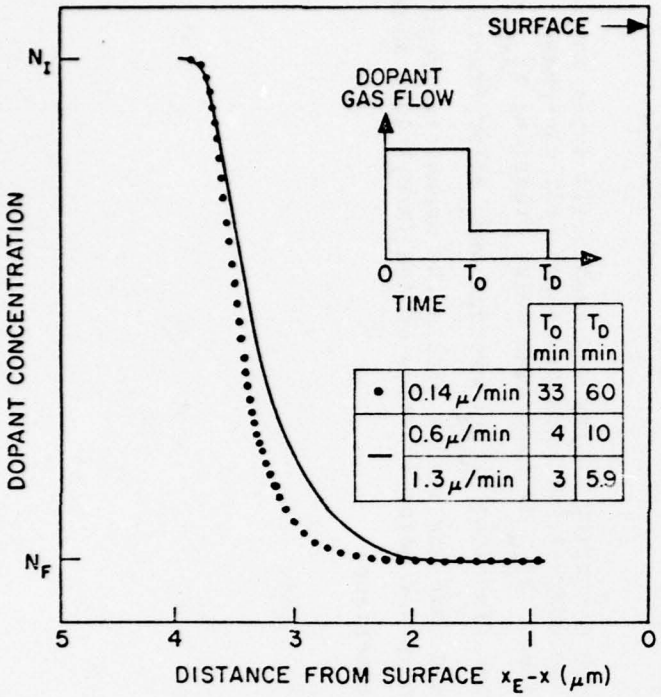

Fig. 3-1. Measured dopant concentration as a function of distance from the surface of the epitaxial film for a decreasing step change in the dopant gas flow, as indicated in the inset. x_E: total epitaxial thickness (gT_D); x: distance from the substrate.

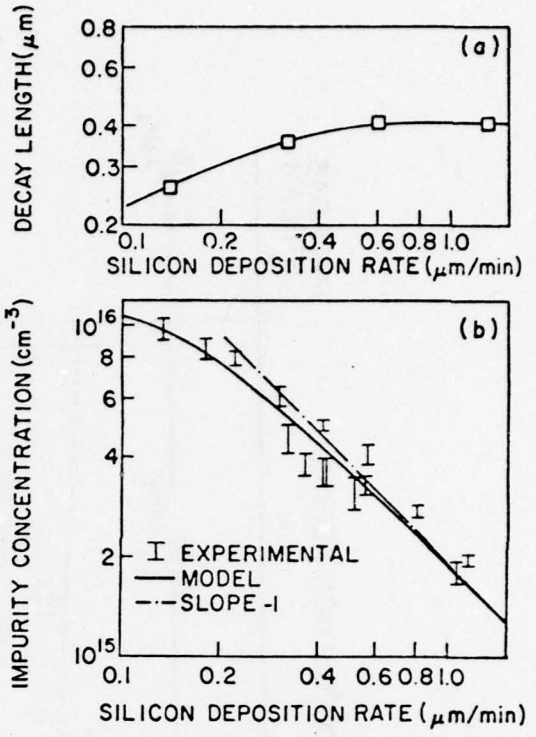

Fig. 3-2(a). Decay length of the transient as a function of growth rate. (b) Impurity concentration of uniformly doped epitaxial layers as a function of growth rate.

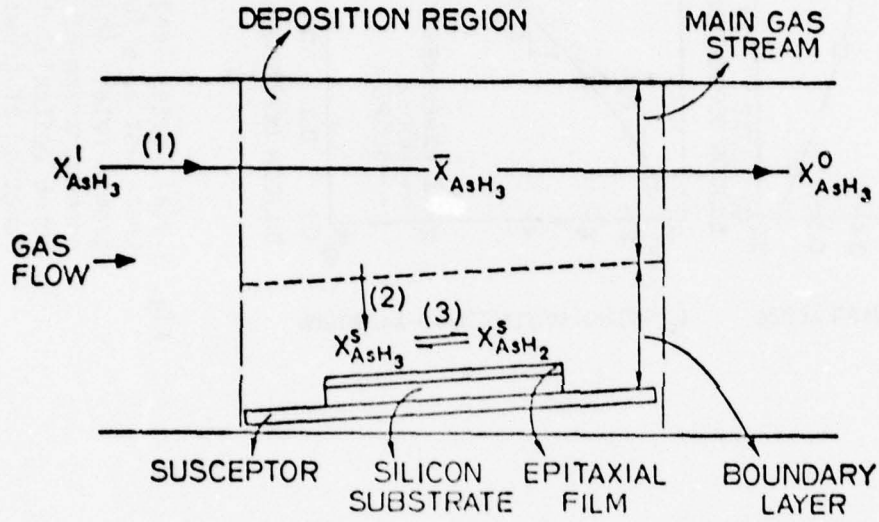

Fig. 3-3. Sequence of steps occurring in the gas phase: (1) input mass transport, (2) boundary-layer mass transport, (3) gas-phase chemical reactions. $X^{i}_{AsH_3}$: input AsH_3 molar fraction; $X^{o}_{AsH_3}$: output AsH_3 molar fraction; $\bar{X}_{AsH_3}$: average AsH_3 molar fraction in the well-mixed main gas stream within the deposition region; $X^{s}_{AsH_3(AsH_2)}$: gas-phase molar fraction of $AsH_3(AsH_2)$ just above the gas-solid interface.

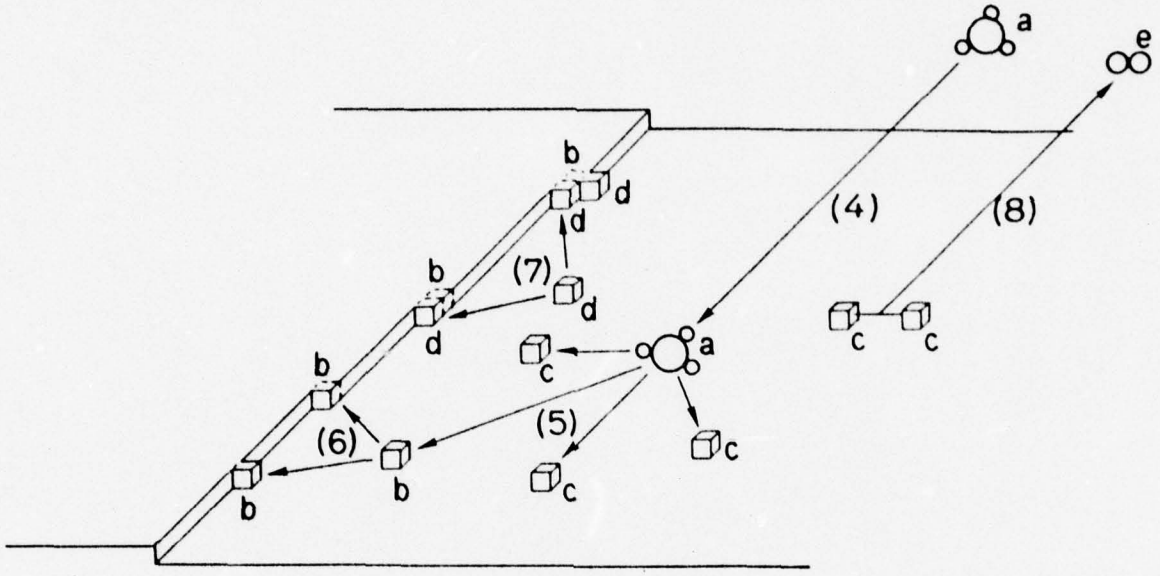

Fig. 3-4. Sequence of steps occurring on the surface: (4) adsorption of the As-containing compound; (5) surface chemical dissociation; (6) surface diffusion and site incorporation; (7) "burying" of As by subsequently arriving Si atoms; (8) desorption of hydrogen. a. AsH_3, b. As, c. H, d. Si, e. H_2.

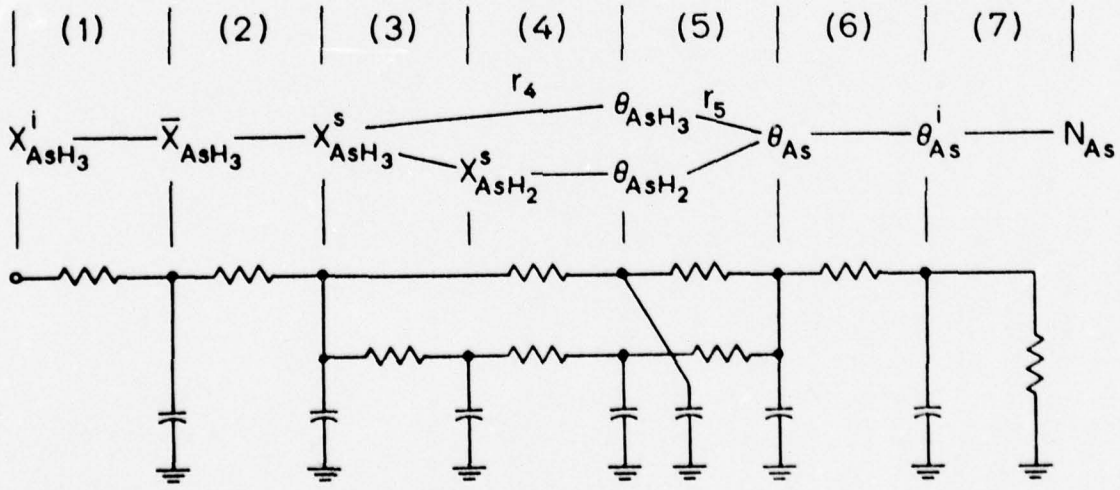

Fig. 3-5. Circuit representation of the dopant system. Each resistance corresponds to one of the steps in the doping process. $\theta_{AsH_3(AsH_2)(As)}$: fraction of adsorption sites occupied by $AsH_3(AsH_2)(As)$. θ^i_{As}: fraction of incorporation sites occupied by As. N_{As}: dopant concentration in the epitaxial film. Processes (1)-(7) correspond to the mechanisms shown in Figs. 1 and 2.

4. DEVICE SIMULATION AND STATISTICAL CIRCUIT MODELING

4.1 Objective

The overall project goals for this section deal with device modeling and statistical circuit design. The technical approach involves developing models and tools for using the models to predict process-dependent performance and yield for custom integrated circuits. Specific development goals include:

(1) One and two-dimensional device simulation codes which
- accept simulated impurity profiles
- predict statistical performance
- reduce to usable circuit models

(2) Analysis and extraction techniques for devices to determine
- parameter statistics and correlations
- parameters most appropriate for process control

(3) Statistical circuit design tools which
- use area scaling information and process variations as input data
- incorporate model parameter correlations directly

(4) Design language and overall simulation capabilities which
- include process, device, circuit and wafer statistical variations
- predict yields and aid in specifying design centers based on process variations

4.2 Summary of the Principal Accomplishments to Date

During the past six months accomplishments on specific topics include the following:

4.2.1 The demonstration of SUPREM as a vehicle to accept models for oxidation, epitaxy and ion implantation. The oxidation models discussed earlier for substrate doping, orientation and ambient effects have been implemented. A first order model for ion implantation clustering (precipitation) is also available as well as coupled species models for boron and arsenic.

4.2.2 The use of SUPREM and a one-dimensional bipolar device simulation program to predict bounds on the transport current for observed profile variations across the wafer.

4.2.3 The development of a statistical bipolar transistor model which predicts 75% of all observed parameter variations using only the parameter distribution for transport current. This model requires a factor of ten fewer statistical variables and correctly predicts parameter correlations.

4.2.4 The demonstration of an efficient Poisson solution program for two-dimensional devices of arbitrary electrode and doping profile geometries. Preliminary results on finite element analysis programs for time-domain carrier transport and bipolar emitter sidewall current transport are discussed.

4.2.5 The fabrication and evaluation of test structures which identify key geometry-limiting effects for DMOS, bulk CMOS and SOS device technologies.

4.2.6 Implementation of circuit simulation capabilities for geometry-based macro models and statistical process models. The statistical capabilities also include a facility for equation parsing.

Further details on each of these topics is given in section 4.3.

4.3 Discussion of Results

During the past six months the basic building blocks have been demonstrated for constructing statistical device models and predicting first order process dependencies and control conditions directly from process variables. Results of this work [4.1-4.6] illustrate feasibility both for bipolar and MOS technologies of the most recent results.

4.3.1 Process Simulation

An essential tool for efforts described below is a process simulator. This tool is needed to merge technology specific processing information with the general process modeling results described in previous sections. A process simulator called SUPREM [4.7-4.8] is presently being developed to meet these modeling needs. Fig. 4.1a shows a typical program input data and output plot for a multi-step boron processing sequence. Further details of the program structure and use are given elsewhere [4.8]. The basic simulation capabilities are shown in Fig. 4.1b. Using SUPREM, a multi-step process can be simulated to obtain a set of impurity profiles. Typical results are shown in Figs. 4.2a and 4.2b for a double-diffused bipolar process and a CMOS field threshold control implant. The subsequent use of the profiles for device and statistical process design are given below.

4.3.2 Bipolar Device Simulation[+]

A first generation capability for simulating bipolar transistor performance directly from process specifications has been demonstrated [4.9]. As a result of present efforts this work has been extended to include device

[+]Device simulator in this report means direct output of device model parameters. Device analysis, as described later, means two-dimensional analysis of the device physics. The output from the device analysis programs must be post-processed to generate model parameters.

simulation based on profiles from SUPREM and outputs which bracket observed device parameter variations [4.1-4.2]. Fig. 4.3a shows a comparison of nominal simulated and measured device parameters. Fig. 4.3b shows a comparison of typical parameter spreads based on measured process spread and the corresponding spread obtained by simulation. Fig. 4.3c shows the calculated upper and lower bounds on the measured distribution for I_S. The summary of results to date can be stated briefly. Using process inputs an adequate prediction of nominal device parameters as well as correct bounds on parameter variations can be achieved. However, the device simulators presently available are constrained to first-order formulations. Hence, many of the physical effects observed in high performance devices cannot yet be predicted. For example, a sidewall injection in bipolar devices and short-channel punch-through in MOS transistors are effects which are not modeled. Continuing efforts in device analysis, as described in section 4.3, are necessary to predict parameters associated with two-dimensional device efforts.

4.3.3 Bipolar Device Parameter Correlations

The observed parameter distributions such as the one shown in Fig. 4.3c describe only scalar relationships. That is, similar distributions for other parameters might initially be considered as independent. However, evaluation of experimental data reveals the expected result that device parameters are correlated [4.3,4.4]. Fig. 4.4a shows the plot of parameters I_S and β_F across a wafer [4.4]. The coefficient R defines the degree of correlation. A perfect straight line fit gives a value of ± 1 indicating perfect correlations; if the data points i.e. within a circle, a value of 0 indicates no correlation. Fig. 4.4b gives a graphical interpretation of R in terms of the major and minor axis dimensions of an ellipse which circumscribes the data points.

The correlation coefficient assumes linear relationships of the form:

$$Y = M X + C \tag{4.1}$$

For the parameters I_S and β_F, first order theory predicts that:

$$I_S = \frac{q A n_i^2}{GU_B} \tag{4.2}$$

and

$$\beta_F = \frac{GU_E}{GU_B} \tag{4.3}$$

where A is the emitter area and

$$GU_B = \int_{Base} \frac{N_A(x)}{D_n} dx \quad , \tag{4.4a}$$

$$GU_E = \int_{Emitter} \frac{N_D(x)}{D_p} dx \tag{4.4b}$$

To the extent that variations in A and GU_E are negligible, it follows that I_S and β_F should be perfectly correlated based on variations in GU_B.

In fact, the observed correlation coefficient is 0.55 in Fig. 4.4a. To understand the observed correlation, other experiments were pursued. The correlation plots for I_S on devices where the area A was varied, indicate that the GU_B variations account for 87% of the observed I_S variations. Using $1/I_S$ to estimate GU_B and β_F/I_S to estimate GU_E, it was determined that the

correlation for GU_B and GU_E was .94, reflecting the coupling between emitter and base impurity distributions. Although these studies do not resolve completely the physics of the observed I_S vs. β_F correlation, this is not surprising. The first order model neglects emitter space charge and surface effects. The two-dimensional device analysis efforts will provide a more complete basis for understanding the physics and predicting the correlations directly.

An example of the application of the parameter correlation studies is illustrated in Fig. 4.5a which shows the correlation coefficient matrix for the normal-active Gummel-Poon bipolar transistor model parameters [4.10] assuming the linear form for correlations given by eq. (4.1). A factor analysis study of the data has shown that 75% of all parameter variations can be predicted by the model shown in Fig. 4.5b [4.3, 4.4]. Plausibility for such a model can be argued based on the high correlation coefficients observed for I_S in Fig. 4.5a. This simple model has the key feature that I_S controls all other parameter variations. This simplifies the characterization process as well as specifications for process control. The dominance of I_S in all parameter correlations is characteristic of a phosphorus emitter bipolar technology.

4.3.4 Two-Dimensional Device Analysis

The bipolar transistor example used in the preceding sections is based on one-dimensional impurity profiles and device simulation. However, two-dimensional analysis is essential for small geometry MOS and bipolar devices. Present efforts focus on three aspects of device analysis. First, an efficient two-dimensional Poisson solution program has been developed and used to solve for potential distributions in devices with a variety of electrode and doping density configurations. Figure 4.6 shows the solution for

the equipotential lines within a buried channel CCD structure. The solution method follows that described elsewhere [4.11]. Ongoing work will define the transport limits for CCD structures based on electrostatic and dynamic charge effects. The second activity in device analysis is aimed at two-dimensional carrier transport including time domain effects such as charge pumping in SOS devices. The computer program used for this analysis is at an early stage of development. A finite element method is used to conserve grid allocations [4.12]. Figure 4.7 shows the grid used for an SOS MOSFET example which is the principle test example. Bench marks of this finite element analysis program for Poisson and transport solutions will be available within the next six months. The third effort in device analysis addresses minority charge storage in the sidewall of bipolar transistors. This effort has demonstrated that the sidewall charge can be estimated using triangular finite elements whose dimensions can be changed to follow current flow paths. Error limits for this quasi two-dimensional approach are being studied. The next objective of this work will be to directly incorporate the method into a device simulator.

4.3.5 Test Structure Results

Two-dimensional device analysis which predicts geometry and impurity dependent effects requires corroborative experimental data. Three sets of test structures for high performance MOS technologies have been fabricated and evaluated. The lateral spread of CMOS channel-stop diffusions are being characterized using special FET structures. Preliminary results show that MOSFETs with channel length parallel to the channel stop diffusion and width dimension across the diffusion can be used to obtain quantitative profile information for diffusions of widths of 3 μm and less. A detailed

analysis of the data will continue during the next six months. SOS test structures fabricated by Hewlett-Packard have been characterized. Device measurements show that for channel lengths less than 10 μm both avalanche generation of carriers and charge-pumping affect dynamic conductance. Present efforts are now focused on two-dimensional device analysis to provide the tools necessary to separate the effects of the two phenomena. The characterization of DMOS/VMOS structures is the final topic to be discussed in this section.

Results of a DMOS/VMOS study are a final illustration of process modeling for high performance MOS technologies [4.5, 4.6]. Figure 4.8a shows a cross section view of devices which are fabricated simultaneously. Fig. 4.8b shows vertical impurity profiles for two fabrication runs which scale the physical channel length from a maximum of 2 μm to a minimum of .5 μm. Figure 4.9a shows a plot of the linear region gain constant vs. inverse of physical "channel" length. The deviation from a constant slope for channel lengths less than 1 μm indicates the onset of transport which violates the one-dimensional and gradual channel approximations. At high drain voltages the behavior also violates conventional theory in that the depletion region spreads primarily into the n-type epitaxial region. Fig. 4.9b shows plots of observed output conductance compared with conventional theory and calculations based on a solution of Poisson's equation. The plots include data for devices with three different channel lengths. Model parameters for theoretical curves shown in Fig. 4.9b and the L_E data for Fig. 4.9a are based solely on spreading resistance data.

The structures and data shown in Figs. 4.8 and 4.9 represent preliminary considerations for one specific technology. Channel length limitations and two-dimensional carrier transport effects depend critically on

spreading resistance data.

The structures and data shown in Figs. 4.9 and 4.10 represent preliminary considerations for one specific technology. Channel length limitations and two-dimensional carrier transport effects depend critically on fabrication technology constraints. Availability of structures to characterize technology parameters and small geometry effects are essential for both device analysis and statistical circuit modeling.

4.3.6 Macromodels and Statistical Circuit Modeling

Circuit simulation is the primary synthesis and verification today for IC design. However, with increased circuit complexity, it has become increasingly difficult for the designer to efficiently control both geometry and technology inputs which effect circuit performance. For high performance devices, it is essential that both factors be accounted for since each can affect yield and performance. Two contributions are discussed in this section which enhance the designers ability to predict and control circuit performance based on direct input of a minimum set of variables related to device geoemetry and fabrication process.

For purposes of multiple cell design, a circuit simulator must provide a convenient format for assembling and scaling the sub-blocks to achieve accurate predictions of circuit performance. Figure 4.10a shows a circuit topology where area scaling of devices is essential to achieve optimum output speed and voltage drive capabilities. Each sub-block in Fig. 4.10a contains an area-scaled pair of CMOS devices as shown. Figure 4.10b shows the circuit simulation input file used to model this circuit. The macro-model allows the area scaling to be inputted directly from sub-block specifications. Internal program computations will reduce the macro-models to tabled sets of parameters for efficient simulation.

Statistical modeling with direct coupling to process-dependent parameters is the second which controls circuit performance. It was demonstrated in section 4.3.3 that frequently the device model parameters are interrelated parametrically based on process-dependent physical parameters. Figure 4.11 shows a statistical model implemented using the notation described by McCalla [4.13]. The data for an RTL inverter are given as an illustration and only β_F, β_R and I_S are specified on the MODEL card. The output can include a plot of delay time vs. I_S or other circuit parameters as desired. The statistical cards shown in Fig. 4.11 illustrate several features. First, only the model card has changed from the conventional circuit simulator form. It is also possible to specify the distribution on separate cards, allowing the conventional model to remain unchanged. Second, β_F and β_R are specified in terms of EQN 1 which is a user-defined equation. The equation is defined in terms of two constants M and C which represent the general form given in Fig. 4.5b:

$$\text{parameter} = MI_S + C \tag{4.5}$$

Third, each parameter equation references I_S and the value of I_S is taken from the distribution P1 according to EQN 2. Hence, I_S and its distributions control all other device parameters on the model card.

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Third, each parameter equation references I_S and the value of I_S is taken from the distribution P1 according to EQN 2. Hence, I_S and its distributions control all other device parameters on the model card.

The results shown in Fig. 4.11 represent preliminary results in implementing a statistical design language. Further work will demonstrate feasibility in using this language for analysis of a variety of statistical device models and circuit design examples. These applications are critical in demonstrating the overall capabilities for statistical design. The basic premise of this effort states that proper design centering can make it possible to achieve acceptable circuit yields. This design centering requires accurate device models which account for parameter correlations. In addition the underlying process variations must be understood so that designs can be centered within controllable limits. The proposed statistical circuit simulation capabilities will make it possible to simulate spreads in circuit parameters resulting from process variations.

4.4 Conclusion

In conclusion, Fig. 4.12 shows in block diagram form how the SUPREM program relates to the research efforts to be discussed. SUPREM, based on fabrication process specifications, generates doping profiles and associated physical and electrical information. The objective of the work discussed is

to develop device and circuit simulation tools to use directly the SUPREM-generated data. Specifically, device simulation and device analysis based on SUPREM input can generate Poisson and transport solutions for one- and eventually two-dimensional device structures. In addition, the electrical device model parameters can be generated for circuit simulation. A key point to be emphasized here is that in addition to determining model parameters from the device simulation, the underlying process and geometry sensitivities can be explained using the SUPREM capabilities. The final block in Fig. 4.12 indicates that circuit simulation based on device model equations is available. This report focuses on two aspects of circuit simulation -- geometry scaling and statistical circuit modeling. These capabilities are essential for understanding the distributions of circuit performance parameters -- propagation delay τ_d for example -- which result from both process and device geometry variations. The ability to simulate and understand process control variables has a direct relationship to yield and circuit reliability. The underlying assertion of the device simulation and statistical circuit modeling efforts is that for custom IC's the availability of computer tools will enhance reliability, procurement speed and technology documentation. Reliability depends on a precise understanding of technology limits and device sensitivities with process and geometry variations. These limits and sensitivities can be predicted using the tools discussed above.

Device Simulation and Statistical Circuit Modeling

[4.1] Dutton, R.W., D.A. Divekar, A.G. Gonzalez and S.E. Hansen, "Correlation of Fabrication Process and Electrical Device Parameter Variations," IEEE IEDM Tech. Digest, Paper 24.5, Dec. 1976, pp. 609-613.

[4.2] Dutton, R.W., D.A. Divekar, A.G. Gonzalez, S.E. Hansen, and D.A. Antoniadis, "Correlation of Fabrication Process and Electrical Device Parameter Variations," to be published in IEEE J. of Solid-State Circuits, Vol. SC-12, Aug. 1977.

[4.3] Divekar, D.A., R.W. Dutton and W.J. McCalla, "Bipolar IC Device Statistics - An Experimental Study," Proc. of IEEE ISCAS, Paper S15.3, April 1977, pp. 565-569.

[4.4] Divekar, D.A., R.W. Dutton and W.J. McCalla, "Experimental Study of Gummel-Poon Model Parameter Correlations for Bipolar Junction Transistors," submitted to IEEE J. of Solid-State Circuits.

[4.5] Combs, S.R., D.C. D'Avanzo and R.W. Dutton, "Characterization and Modeling of Simultaneously Fabricated DMOS and VMOS Transistors," IEDM Technical Digest, 1976.

[4.6] D'Avanzo, D.C., S.R. Combs, and R.W. Dutton, "Effects of the Diffused Impurity Profile on the DC Characteristics of VMOS and DMOS Devices," IEEE J. Solid-State Circuits, Aug. 1977.

[4.7] Dutton, R.W., A.G. Gonzalez, R.D. Rung, and D.A. Antoniadis, "IC Process Engineering Models and Applications," Semiconductor Silicon 1977, presented at the Spring Electrochemical Society Meeting, Philadelphia, May 9-13, 1977, pp. 910-922.

[4.8] Antoniadis, D.A., S.E. Hansen, R.W. Dutton, A.G. Gonzalez, "SUPREM I -- A Program for IC Process Modeling and Simulation," Stanford Technical Report SEL 77-006, May 1977.

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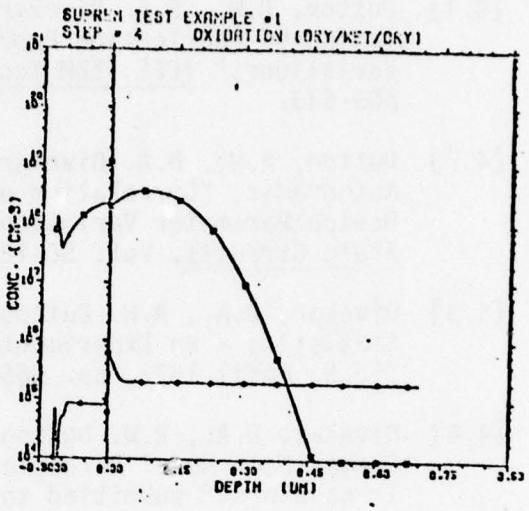
[4.10] Nagel, L.W. and D.O. Pederson, "Simulation Program with Integrated Circuit Emphasis (SPICE)," presented at the 19th Midwest Symp. Circuit Theory, Waterloo, Ont., Canada, April 1973.

[4.11] Kennedy, D.P., "Computer Aided Engineering of Semiconductor Integrated Circuits," Research and Development Technical Report, ECOM-75-1344-1, April 1976.

[4.12] Barnes, J.J., R.J. Lomax, "Finite Element Simulation of GaAs MESFETS with Lateral Doping Profiles and Submicron Gate," IEEE Trans. Electron Devices, Vol. ED-23, No. 9, Sept. 1976, pp. 1042-1048.

[4.13] McCalla, W.J., "Computer-Aided Circuit Simulation Techniques," EE 392B Course Notes, Stanford University, Spring 1977.

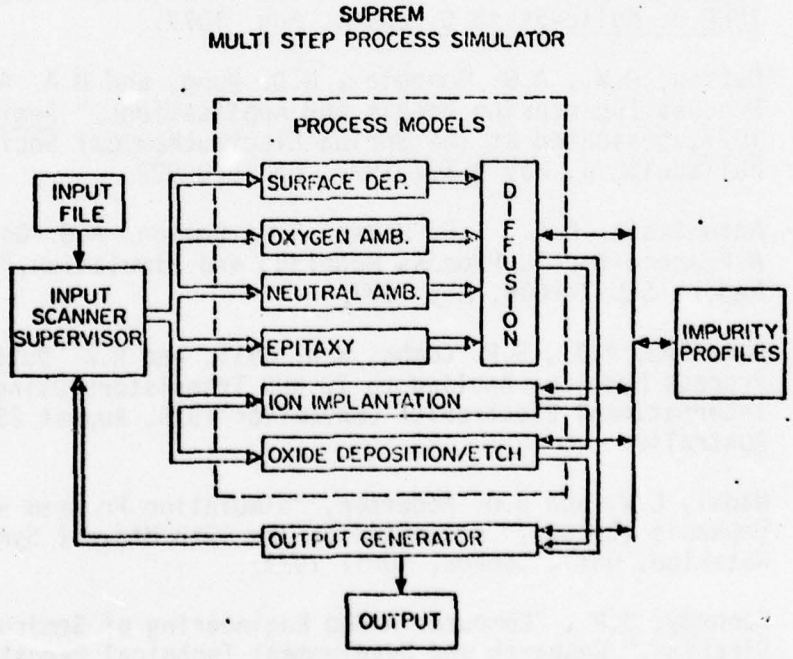
Output Data



Input Data

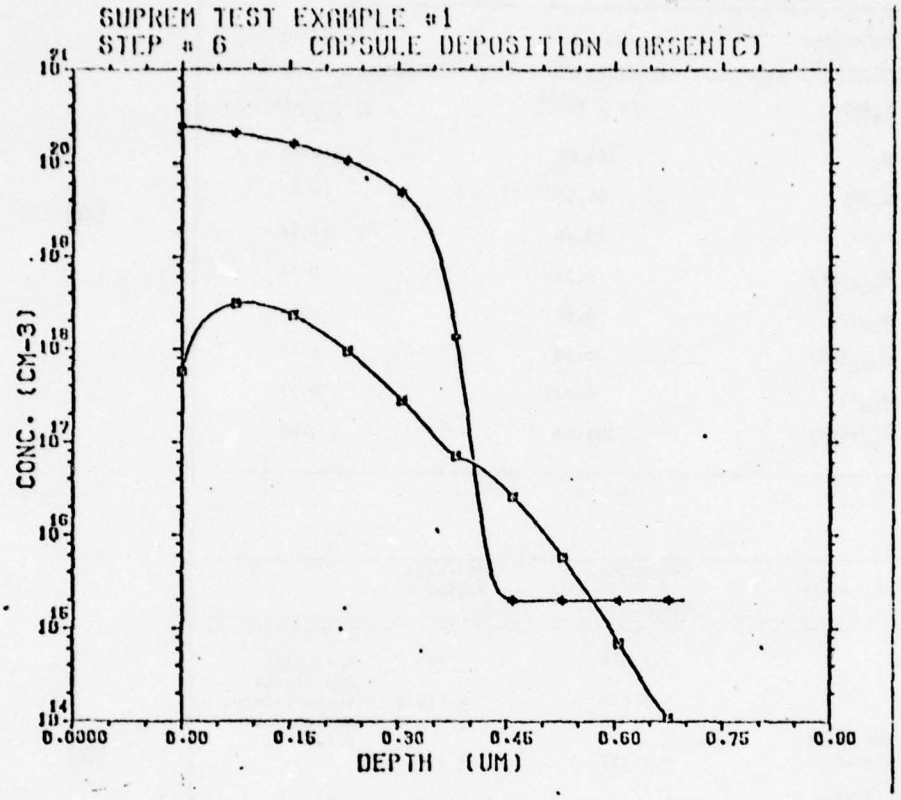
```
COMM  ION IMPLANT (BORON)
STEP  TYPE=IMPL, ELEM=B, DOSE=1.0E14, ENERGY=50

COMM  OXIDATION (DRY/WET/DRY)
STEP  TYPE=OXID, TEMPERATURE=900, TIME=10, MODEL=DRY0, MODEL=IFI
STEP  TYPE=OXID, TEMPERATURE=900, TIME=20, MODEL=WET0, MODEL=IFI
STEP  TYPE=OXID, TEMPERATURE=900, TIME=5, MODEL=DRY0, MODEL=IFI
```

(a)

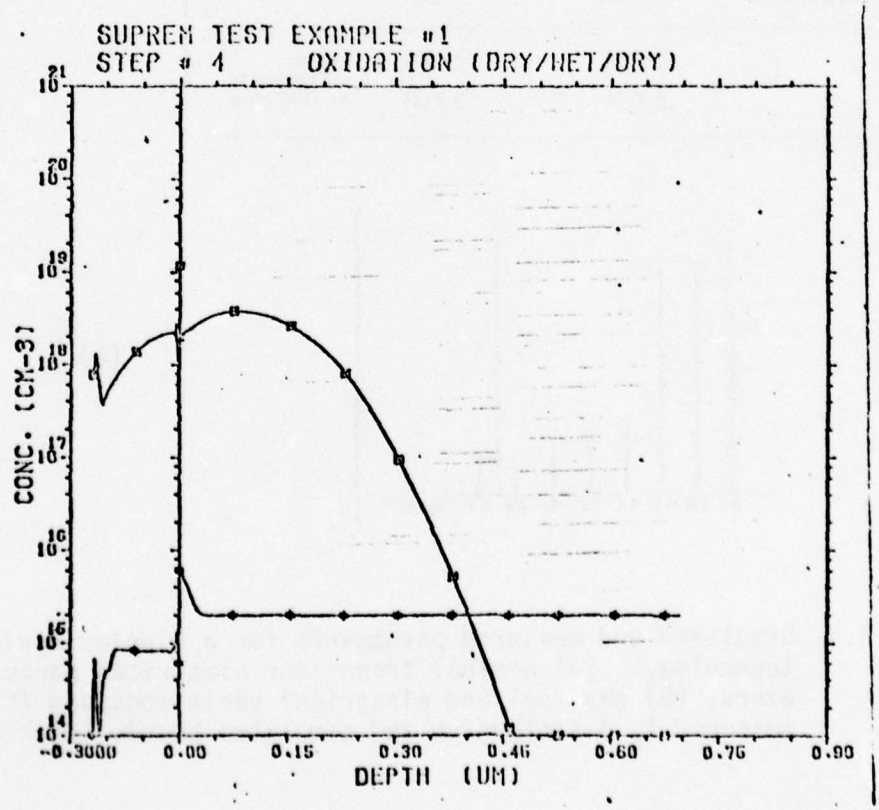


(b)

Figure 4.1. The SUPREM program (a) input and output examples, and (b) the overall program structure.



(a)



(b)

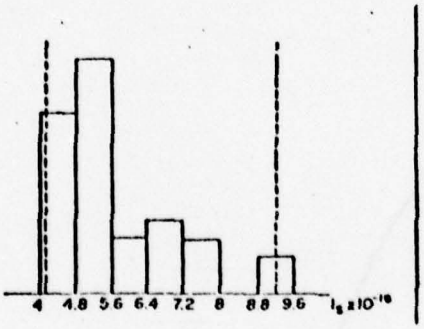
Figure 4.2. Two output plots from SUPREM (a) a boron redistribution example, and (b) boron and arsenic profiles for a bi-polar process.

Parameter	Simulated	Measured
I_S(A)	7.15×10^{-16}	7.64×10^{-16}
β_F	184.00	174.00
$R_C(\Omega)$	34.50	47.83
V_A(V)	20.20	17.67
C_{OCB}(PF)	0.391	0.36
ϕ_{CB}(V)	0.57	0.51
C_{OEB}(PF)	0.50	0.52
ϕ_{EB}(V)	0.721	0.77
τ_F(PSEC)	131.00	179.00

(a)

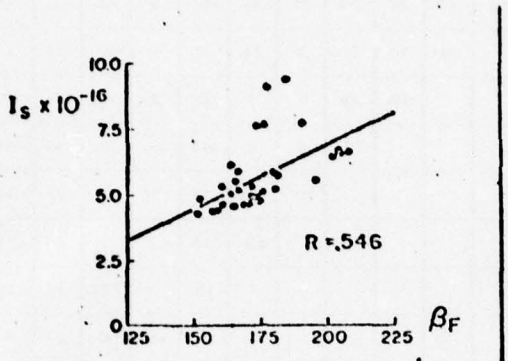
Parameter	Variation for Simulation	Measured Variation	
XJEB	± 5.41%	± 7%	Spreading resistance measurements on the test wafer
XJBC	± 3.86%	± 4.62%	
Emitter Sheet Resistance	± 2.95%	± 3.4%	
Pinched Base Sheet Resistance	±19.14%	± 29%	
I_S	±36.8%	± 40%	Device measurements on test chip
C_{OEB}	± 9.2%	± 8.3%	

(b)



(c)

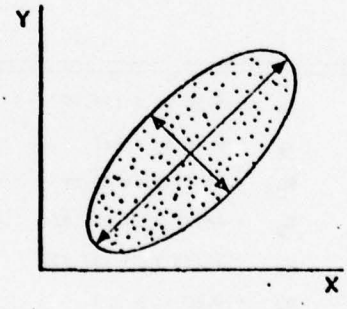
Figure 4.3. Simulated and measured parameters for a bipolar device technology: (a) nominal transistor electrical parameters, (b) physical and electrical variations, and (c) measured I_S distribution and simulated bounds (dashed).



(a)

CORRELATION COEFFICIENT

$$R = \frac{\Sigma(X-\bar{X})(Y-\bar{Y})}{\sqrt{\Sigma(X-\bar{X})^2 \cdot \Sigma(Y-\bar{Y})^2}}$$



$$|R| = 1 - \frac{\text{MINOR AXIS}}{\text{MAJOR AXIS}}$$

(b)

Figure 4.4. Electrical parameter correlations. (a) Scatter plot for I_S and β_F with correlation coefficient of R = .55, and (b) physical interpretation of R factor.

LINEAR CORRELATION COEFFICIENT MATRIX

$$X_i = k X_j + c$$

	β_F	β_R	R_{PB}	f_T	I_S	R_E	n_e	R_B	V_A	C_2	C_{OEB}	ϕ_{EB}	m_{EB}
β_F	1.0	.73	.26	.34	.55	-.15	-.06	.81	-.6	.01	.22	-.13	.6
β_R		1.0	.76	.57	.9	.30	.32	.57	-.88	.51	-.24	.25	.66
R_{PB}			1.0	.56	.83	.8	.67	.2	-.7	.71	-.7	.62	.31
f_T				1.0	.6	.4	.44	.28	-.54	.43	-.55	.41	.28
I_S					1.0	.54	.58	.56	-.81	.77	-.44	.35	.59
R_E						1.0	.66	-.2	-.38	.64	-.78	.68	.04
n_e							1.0	.11	-.25	.02	-.72	.66	.04
R_B								1.0	-.42	.23	.15	-.22	.55
V_A									1.0	-.46	.23	-.2	-.56
C_2										1.0	-.6	.45	.26
C_{OEB}											1.0	-.7	-.07
ϕ_{EB}												1.0	-.21
m_{EB}													1.0

(a)

$$\beta_F = 5.98\, I_S + 139.99$$
$$\beta_R = 0.19\, I_S + 1.2$$
$$R_{PB} = 26.39\, I_S + 23.19 \quad \text{(K-Ohms)}$$
$$R_B = 45.27\, I_S + 759.85 \quad \text{(Ohms)}$$
$$C_2 = 30.63\, I_S - 136.85$$
$$n_e = 0.06\, I_S + 1.2$$
$$R_E = 0.28\, I_S + 3.86 \quad \text{(Ohms)}$$
$$V_A = -10.95\, I_S + 106.53 \quad \text{(Volts)}$$
$$f_T = 15.87\, I_S + 582.67 \quad \text{(MHz)}$$
$$C_{OEB} = -0.01\, I_S + 0.5933 \quad \text{(Pf)}$$
$$M_{EB} = 0.01\, I_S + 0.31$$
$$\phi_{EB} = 0.01\, I_S + 0.71 \quad \text{(Volts)}$$

(I_S is a multiple of 10^{-16})

(b)

Figure 4.5. Statistical bipolar device model: (a) correlation coefficient matrix and (b) reduced model form based on linear regression.

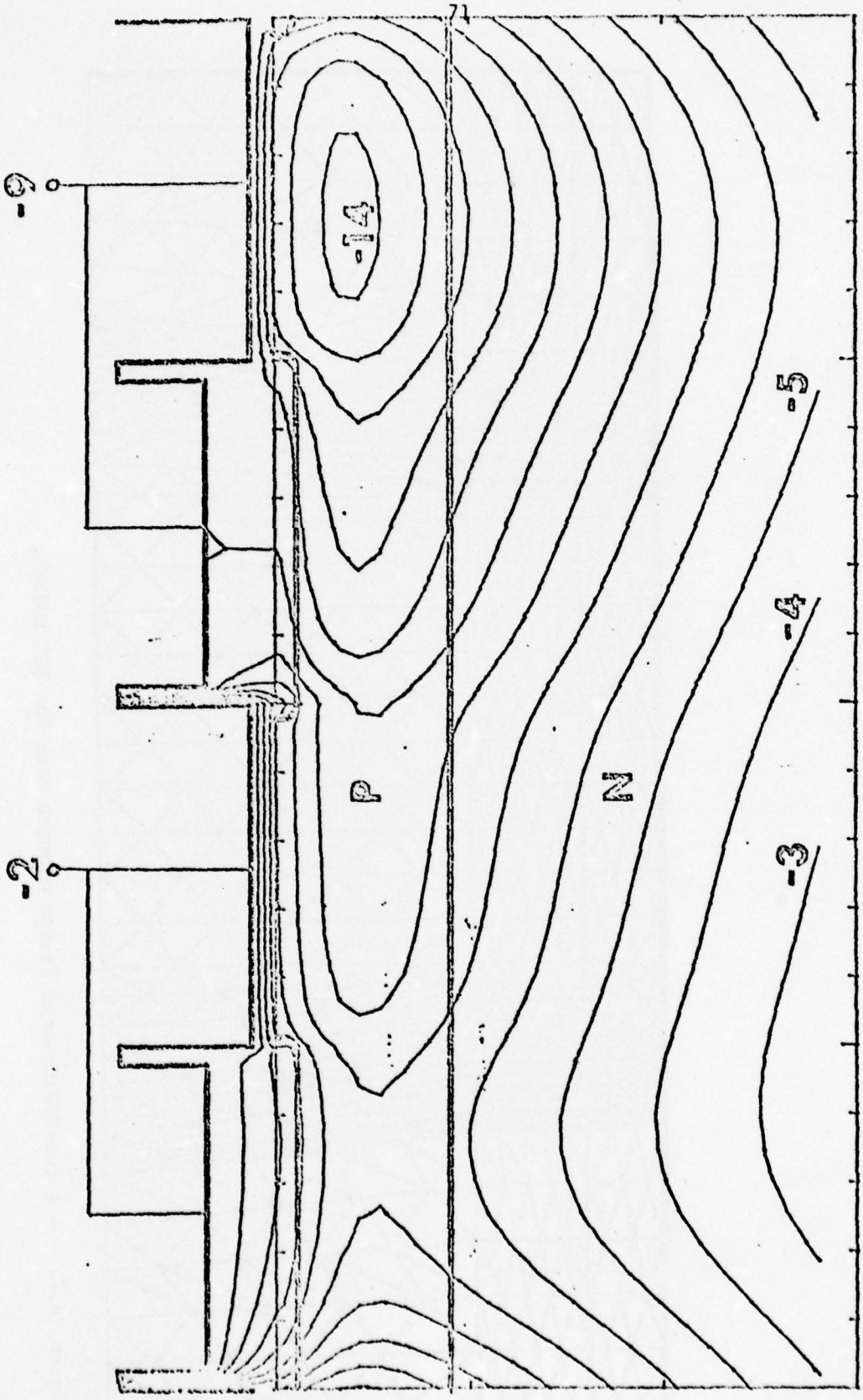


Figure 4. 6. Buried channel CCD structure and plot of simulated equi-potential surfaces.

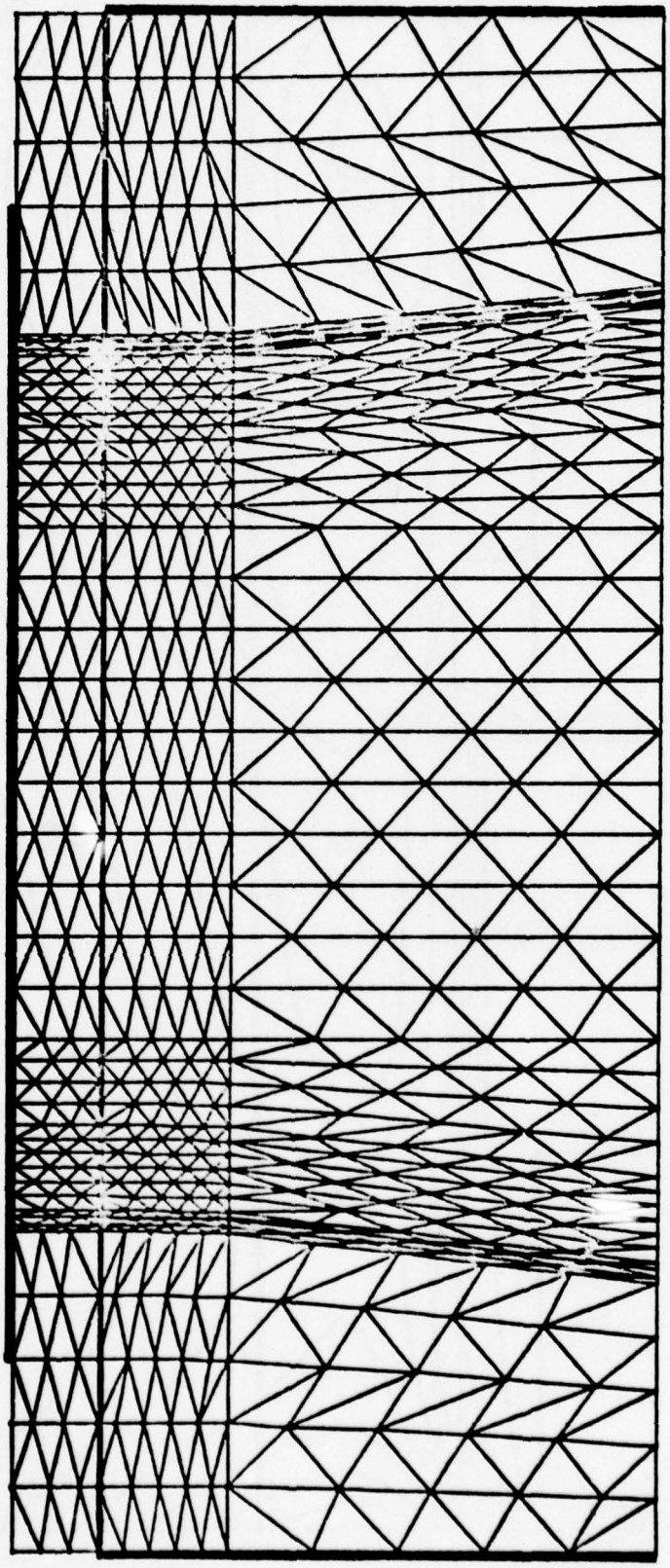


Figure 4.7. - A two-dimensional finite element mesh for SOS MOSFET.

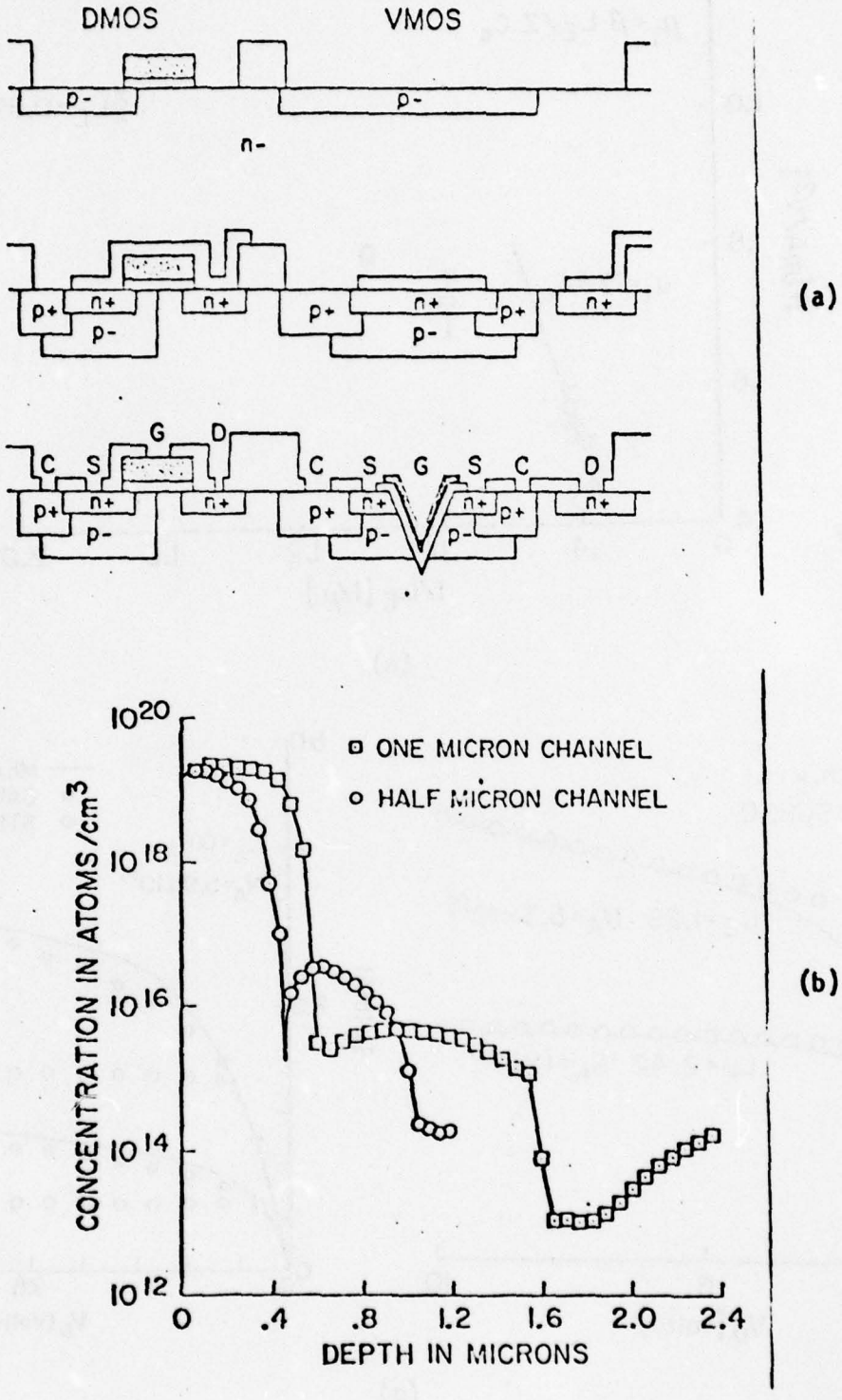
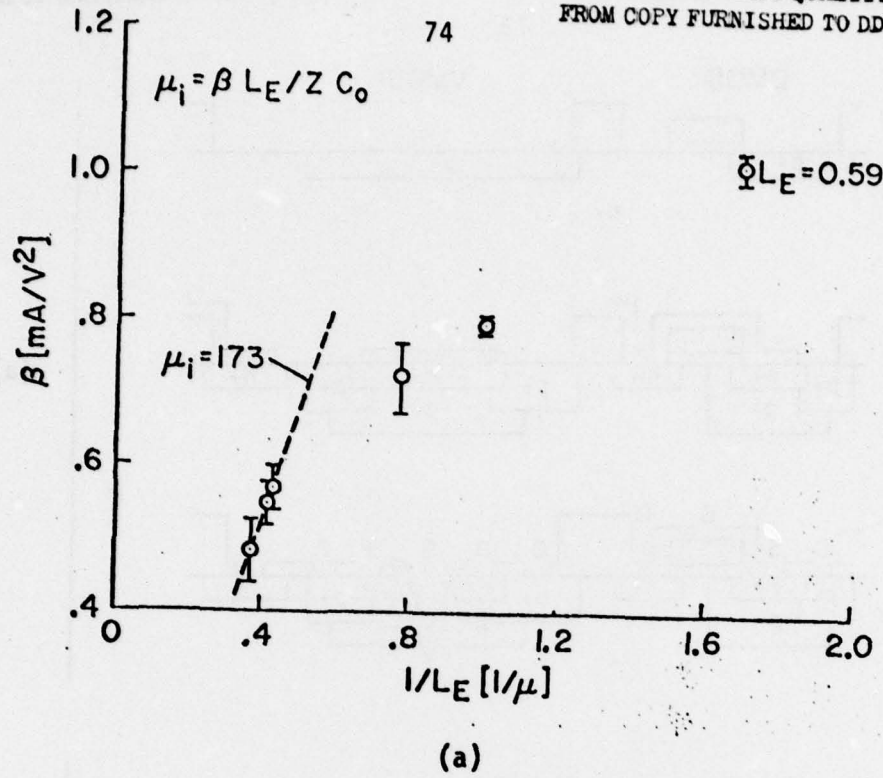
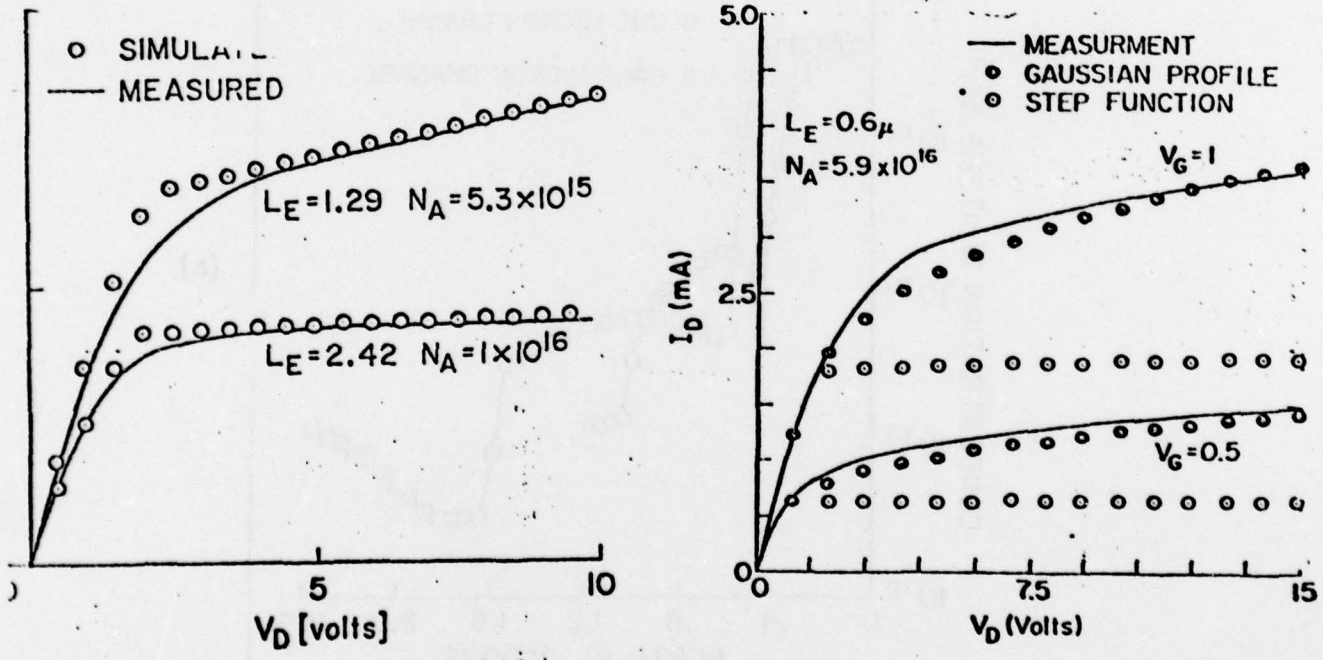


Figure 4.8 DMOS/VMOS test structure. (a) Fabrication sequence, and (b) vertical doping profile for different channel-length designs.

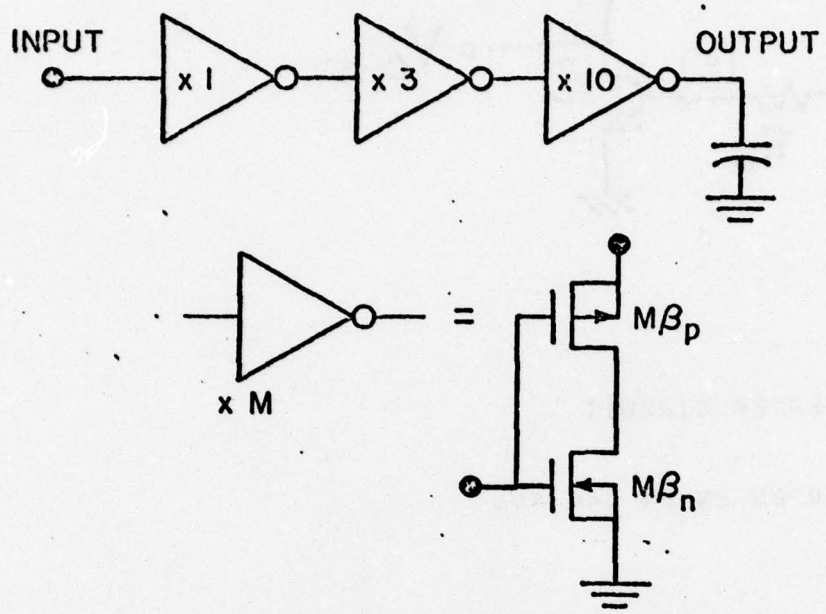


(a)



(b)

Figure 4.9 Electrical device characteristics for the VMOS structures: (a) linear region plot of β vs Y_{LE} and (b) output conductance plots and comparison with model results.

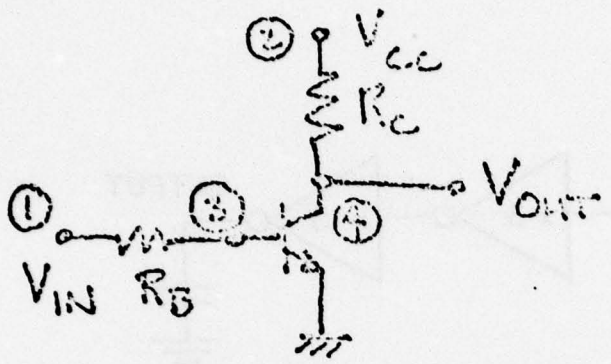


(a)

```
*
VIN    1  0 PULSE 0 12 10N 10N 10N 50N 100N
XI1    1  2 INV   1
XI2    2  3 INV   3
XI3    3  4 INV   10
CL     4  0 1.2
*
MACRO  1  2  12  0 INV 1.0
M1     2  1  12 12 MP 10#1 10
M2     2  1   0  0 MN 10#1 10
MEND
*
MODEL MN NMOS VTO= 2 UO=300 TOX=1000 UNB=3E15
MODEL MP PMOS VTO=-2 UO=260 TOX=1000 UNB=1E15
*
END
```

#1 = 1, 3 or 10

Figure 4.10. Macromodeling: (a) equivalent circuit for CMOS inverter drain, and (b) circuit simulator input including device area-scaling feature.




```
*
* SIMPLE RTL INVERTER CIRCUIT
*
VCC 2 0 DC 5
VIN 1 0 PULSE 5 0 2N 2N 2N 34N 40N
*
RC  2 4 1
RB  1 3 10
*
Q1  4 3 0 QMOD
*
MODEL QMOD NPN BFM 175 EQUATION EQN1 (5.98,QMOD:IS,139.99)
+              BRM 2.2 EQUATION EQN1 (0.19,QMOD:IS,1.2)
+              IS 6.8E-16 EQUATION EQN2 (P1)
*
* USE OF DUMMY PARAMETERS
*
P1 DISTRIBUTION TABLE TP1 NOMINAL MEAN
*
EQUATION EQN2 (X) = X * 1E-16
*
EQUATION EQN1 (M,X,C) = M * X * 1E16 + C
*
TABLE TP1 CONTINUOUS DENSITY
+ 4.0,0   4.8,10  5.6,13  6.4,3
+ 7.2,4   8.0,3   8.8,0   9.6,2
*
END
```

Figure 4.11. RTL inverter circuit and statistical circuit simulator input format. EQN 1 defines parameter correlation equations and EQN 2 gives I_S distribution data.

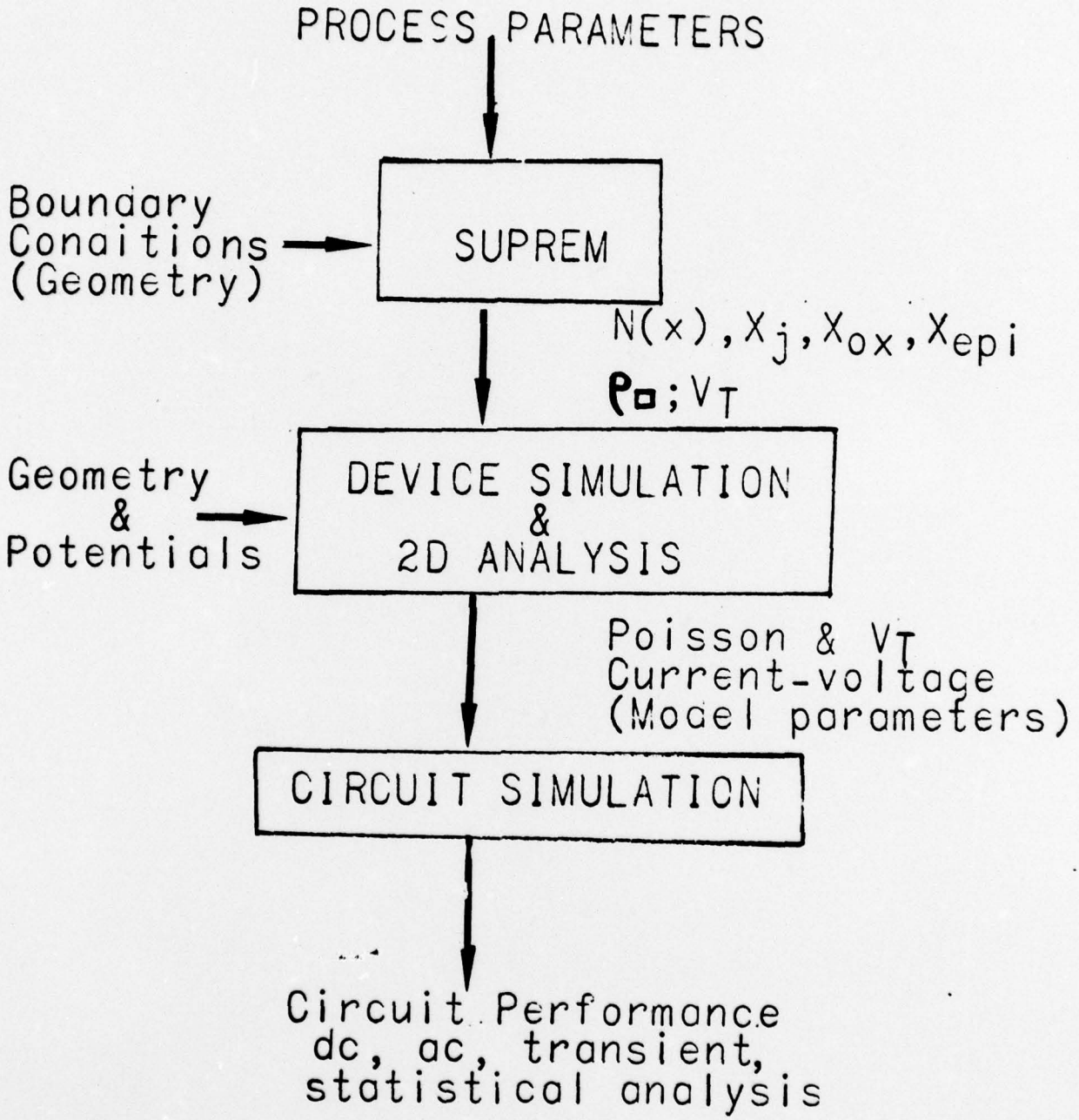


Fig. 4.12.

5. SUPREM I -- A PROGRAM FOR IC PROCESS MODELING AND SIMULATION

The Stanford University PRocess Engineering Models (SUPREM) program is a computer simulator capable of simulating most typical IC fabrication steps. The program is designed so that these steps can be simulated either individually or sequentially, just as they would occur during the actual fabrication process. The output of the program, available at the end of each step, consists of the one-dimensional profiles of all the dopants present in the silicon and silicon-dioxide materials. These profiles are displayed in various formats including line-printer printout, line-printer plots, and high-resolution (Calcomp type) plot. It is understood that, in sequential step simulation, the output of a process step constitutes the initial conditions for the following one. The junction depths and sheet resistances of all n or p layers formed during the process are also calculated.

The fabrication-step simulation is based on several process models. The models implemented in SUPREM are the following:

(1) oxidation/drive-in

(2) predeposition through the surface (gaseous or solid)

(3) epitaxial growth

(4) ion implantation

(5) etching

(6) oxide deposition

Solid-state diffusion is fully accounted for in any of the above models involving high temperature.

Communication between the user and SUPREM has been made as simple as possible. The input file consists of free format statements involving key

words and numbers. Typically, a single processing step can be simulated with an input specification involving less than 60 alphanumeric characters.

Several physical parameters have been stored in the program and constitute the default values used by the models. They may be overridden by user-specified parameters.

The following table lists the organizations currently using the SUPREM program.

Table I

PARTIAL LIST OF DISTRIBUTED COPIES OF SUPREM

Government		
1.	ECOM, Fort Monmouth, N.J.	Randy Reitmeyer
2.	National Bureau of Standards	Tom Leedy
3.	National Security Agency	Bill Bundy
4.	Harry Diamond Laboratories	Brian Biehl
DOD Contract Holders		
1.	TRW Defense and Space Systems Group	John Choma
2.	Hughes Aircraft Co., Carlsbad Research Center	Michael Jack
3.	Sandia Laboratories	Chuck Gwyn
4.	Northrop Corporation, Northrop Research and Technology Center	F.W. Pfeiffer
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	a. Allentown, Penn.	Paul Langer
	b. Murray Hill, N.J.	Dr. Jacques Ruch
	c. Holmdel, N.J.	Alexander Voshchenkov
3.	Intel	Chris Martensen
4.	Prime Computer Inc.	Mike Payne
5.	Texas Instruments, Dallas, Texas	Dr. William Daughton
6.	Tektronix, Beaverton, Ore.	Dr. Doug Ritchie
7.	Signetics, Santa Clara, CA	Tak Young
8.	Litronix: Advanced LSI Technology Inc. Cupertino, CA	Molz B. Khambaty
9.	Control Data Corporation, Minneapolis, Minn.	Chuck Naber
10.	Bell Northern Research	Michael Caughey
11.	National C.S.S., Santa Clara, CA	Mr. Wong
12.	National Semiconductor, Los Altos, CA	Darrell Erb
13.	Xerox, El Segundo, CA	Keming W. Yeh
14.	Philips Laboratories, Briarcliff Manor, N.Y.	Jerry S. Sullivan
15.	Solid State Scientific, Montgomeryville, Penn.	Jeff Steinwedel
16.	Hewlett-Packard, Corporate Engineering, Palo Alto	Hal Daseking
	a. Loveland Instruments Division	Dick Toftness
	b. Microwave Semiconductor Division	Craig Snapp
	c. Solid-State Laboratory	Ken Lisiak
	d. Integrated Circuits Laboratory	Skip Rung
	e. Data Systems Division	Wei Wu
	f. Colorado Springs Division	Grant Somners

Table I (cont'd)

Industry Foreign		
1.	Centre Electronique Horloger, Switzerland	Heinz W. Luginbuhl
Educational Institutions		
1.	University of Maryland	Prof. H.C. Lin
2.	University of California, Berkeley	David Angst
3.	University of Toronto	Prof. C.A.T. Salama

6. ONE DAY SYMPOSIUM ON PROCESS MODELING

A one day symposium was held at Stanford University on July 8, 1977, on Integrated Circuit Process Engineering Models. The main objective was to provide a summary of our recent advances in predicting and understanding ion implantation, diffusion, oxidation and epitaxy. The content of the symposium reflected ongoing research at Stanford under DARPA sponsorship. In all, six presentations were given to review the progress and stimulate the dialogue between researchers and users. Copies of three reports covering most of our recent work were distributed.

A wide cross section of people from industrial, educational and government organizations attended the symposium (see attachment 1), reflecting a widespread interest in this research program. Many of the attendees expressed desire (1) to get more information on our process modeling activities, (2) to get a copy of our process modeling computer program SUPREM I, (3) to be on our mailing list to get information on the future progress. We have thus far disseminated 28 copies of SUPREM I on magnetic (see attachment 2) tape and have a dozen additional requests for copies.

All of the presentations were recorded on video tapes for later use. Because of the immense interest shown by several industrial, educational, and government organizations, copies of the video tape will be shortly available for wide distribution. This will be highly useful for those who could not attend the symposium and for internal use at industrial locations.

During and after the symposium, discussions took place between the researchers working on this program and the attendees, which brought out interesting points. People remarked that they have rarely seen such an

integrated research program involving people from disciplines and organizations. Interesting technical questions were raised, which will be helpful to us in the future.

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