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Manufacturing Methods and Technology Report 1

Contract DAAB07-75C-0044

PHOTOLITHOGRAPHIC TECHNIQUES FOR SURFACE ACOUSTIC WAVE (SAW) DEVICES.

L. Dyal

GROUND SYSTEMS GROUP
HUGHES AIRCRAFT COMPANY
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Feb 1978

Quarterly Report #7, for Period 1 Sept 1977 to 28 Feb 1978

Prepared for
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NOTICES

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Disclaimers

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SAW Packaging

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The object of the program is the establishment of a production capability for surface acoustic wave devices of varied design and material for the purpose of meeting estimated military needs for a period of two years after the completion of the contract and to establish a base and plans which may be used to meet expanded requirements. The primary requirement is the pilot line production of devices that are reliable, reproducible, and low cost. → next page

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The first two phases of this program saw the design, fabrication and tooling of six device types - bandpass, pulse compression and tapped delay line SAW filters on both lithium niobate and ST-quartz substrates. The third phase involved fabrication of a larger quantity (50 ea.) of confirmatory devices which were sampled at a high rate and subjected to rigorous life and environmental testing. The fourth phase of the program is a pilot line production effort of 150 each of the devices scheduled to be delivered. Phase III has been successfully completed with delivery and acceptance of the confirmatory samples.

This report describes the progress to date on the pilot line phase of the program. The degree of attention to detail has been adjusted upward from original planning to adequately report pricing and yield data and to ensure accuracy in the device performance evaluation. Solder sealing has recently been identified as a potential problem area in the manufacture of SAW devices and is being addressed. New solder seal methods are being developed and documented and an alternate approach of projection weld sealing is being investigated. Results of these investigations are reported.

The remainder of the program will be devoted to completing the Pilot Line production run and doing a detailed cost analysis for future needs; to documenting the process in its entirety and to providing a Quality Control Manual.

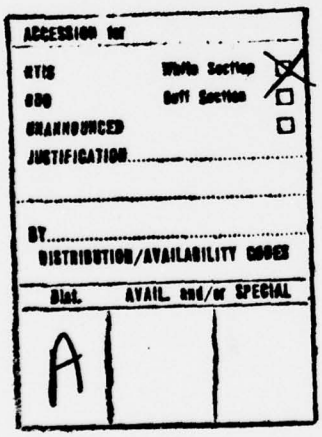

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

GLOSSARY

SAW - Surface Acoustic Wave

BP-Q - Bandpass Filter - ST Quartz Substrate

BP-LN - Bandpass Filter - Lithium Niobate Substrate

TDL-100 - Tapped Delay Line Filter - 100 MHz - ST Quartz Substrate

TDL-200 - Tapped Delay Line Filter - 200 MHz - ST Quartz Substrate

PC-Q - Pulse Compression Filter - ST Quartz Substrate

PC-LN - Pulse Compression Filter - Lithium Niobate Substrate

ST - Quartz orientation, ST cut (42^{o} 45'), X propagating

YZ - Lithium Niobate orientation, Y cut Z propagating

SECTION 1.0
INTRODUCTION

Section 1.0

INTRODUCTION

This report presents the progress to date on the Phase IV pilot production effort to include further advances in manufacturing techniques as required to satisfy this Manufacturing Methods and Technology Program devoted to the representative range of surface acoustic wave (SAW) device designs.

1.1 PROGRAM OBJECTIVES

Production engineering measures are to be established by Hughes for Surface Acoustic Wave Devices. Hughes is to establish or improve the producibility of specified devices; establish a quality control system; and take such actions as are necessary to reduce the time required for delivery of items required in large quantity production for current planning and in the event of an emergency.

The objective of this program is to establish a production capability for meeting estimated military needs for a period of two years after completion of the contract, and to establish a base and plans which may be used to meet expanded requirements

Reports and other information generated will be used for industrial mobilization and preparedness planning, to provide a basis for determining whether military requirements can be accomplished, to determine additional planning measures that may be required, and to assist in establishing additional sources.

1.2 PROGRAM PLAN

The program has been divided into four phases. The first addressed the design, fabrication and analytical testing of six prototype SAW devices representative of current and potential application of the technology. While these device requirements did not represent the state-of-the-art in an R&D sense, they were of such complexity as to require a serious design effort.

The second phase resulted in the design of those devices that failed to meet the intended design specification during Phase I. The net result of this effort was a final electrical specification imposed during the remainder of the program based on a cost effective production commitment.

The third phase tested and determined the impact of imposed environmental conditions on the various devices. The final phase has been designed to test the reproducibility of these devices in a high volume production environment. A key result of this phase will be the establishment of meaningful manufacturing yield and cost data on each device, and a comparison of this data with that of the prior low volume efforts.

1.3 PROGRAM ACCOMPLISHMENTS DURING THIS REPORTING PERIOD

Pilot line production of the Phase IV devices is approximately 75% complete. The attention focused on yield and cost aspects of this phase has been intensified so that final data will be accurate. Performance data of pilot line devices is being obtained at several stages of production using 100 percent inspection to enable a complete analysis of yield losses during processing and test. A new problem area in the manufacture of these devices has been identified during this reporting period resulting in several independent approaches to the solution. The problem is solder sealing of the device package to provide hermeticity. The solutions sought are:

1. A new fluxless soldering process.
2. Projection welding.
3. Tungsten inert gas welding.

SECTION 2.0
MMT DEVICE CONFIGURATION

Section 2.0

MMT DEVICE CONFIGURATION

2.1 DEVICE DESCRIPTION

The six devices to be designed and manufactured during this program are of three different classes on two different substrate materials. The classes of devices are bandpass filters, pulse compression filters and tapped delay lines. The substrate materials are ST quartz and YZ lithium niobate ($LiNbO_3$). (The terms ST and YZ denote crystallographic orientation.) The individual SAW devices are further identified in tables 2.1-1, 2.1-2 and 2.1-3.

TABLE 2.1-1. MMT SAW DEVICE DESCRIPTION DATA

Designation	Device Class	Substrate Material	Center Freq.	Package Marking
BP-Q	Linear Phase Bandpass Filter	ST-Qtz.	100 MHz	B-Q-10-02
BP-LN	Linear Phase Bandpass Filter	$LiNbO_3$	150 MHz	B-L-15-30
PC-Q	Linear FM Pulse Compression Filter	ST-Qtz.	150 MHz	C-Q-15-50
PC-LN	Linear FM Pulse Compression Filter	$LiNbO_3$	150 MHz	C-L-15-50
TDL-100	Biphase Coded Tapped Delay Line Filter	ST-Qtz.	100 MHz	T-Q-10-10
TDL-200	Biphase Coded Tapped Delay Line Filter	ST-Qtz.	200 MHz	T-Q-20-10

TABLE 2.1-2. SUBSTRATE WAFER, MATERIAL AND SIZE

Material	Size	Orientation
ST Quartz	2" x 2" x .025"	$\pm$ 0° 15'
YZ $LiNbO_3$	2.1" x 1.75" x .020"	$\pm$ 0° 15'

TABLE 2.1-3. INDIVIDUAL DIE TYPE, MATERIAL SUBSTRATE, SIZE, ARRAY SIZE, DIE/WAFER

Designation	Substrate	Size	Array Size	Die/Wafer
BP-Q	ST Qtz.	.586" x .172"	3 x 11	33
BP-LN	$LiNbO_3$	.500" x .200"	4 x 8	32
PC-Q	Quartz	.800" x .200"	2 x 10	20
PC-LN	$LiNbO_3$	.650" x .115"	3 x 15	45
TDL-100	Quartz	2.0" x .220"	1 x 9	9
TDL-200	Quartz	2.0" x .155"	1 x 12	12

These devices have been constructed and tested both electrically and environmentally and conform to those specifications called out in SCS-476, USAECOM Technical Requirements.

2.2 ASSEMBLY DETAILS

Photolithographic mask arrays of the transducer geometries designed during the engineering phases were procured for batch processing the piezoelectric SAW substrates. Tables 2.1-2 and 2.1-3 show the dimensions of the substrates, die and array sizes.

Once the transducer arrays are photolithographically defined on these substrates, the substrates are diced. The individual die is mounted with attendant tuning circuitry into a hermetic type package, interconnected, tested and sealed for delivery. The individual MMT device layout is shown in Figure 2.2-1 while a schematic representation of each is shown in Figure 2.2-2. The BP-Q, BP-LN and PC-Q all have series tuning inductors at each input and output prot; the PC-LN has no inductors; and the TDL-100 and TDL-200 have inductors on the input only.

Using the resistive properties of the thin film metallization, either series or shunt resistors (R) were fabricated as an integral part of the transducer patterns. All devices utilize a tapped resistor as shown in Figure 2.2-3A; if tap a or taps a and b are scribed successively, higher values of R can be obtained than if the taps are left unscribed. Figure 2.2-3B shows the shunt resistor configuration used on the PC-LN.

The toroid leads are soldered to the package pins. Interconnection between the SAW pattern and the pins is made with thermo-compression bonded 1 mil diameter gold wire. Both toroid and crystal are bonded in the package with silicone adhesive. The package lid is sealed to the base with solder to provide hermeticity; the problems associated with this process are discussed in Section 3.1.2.5.

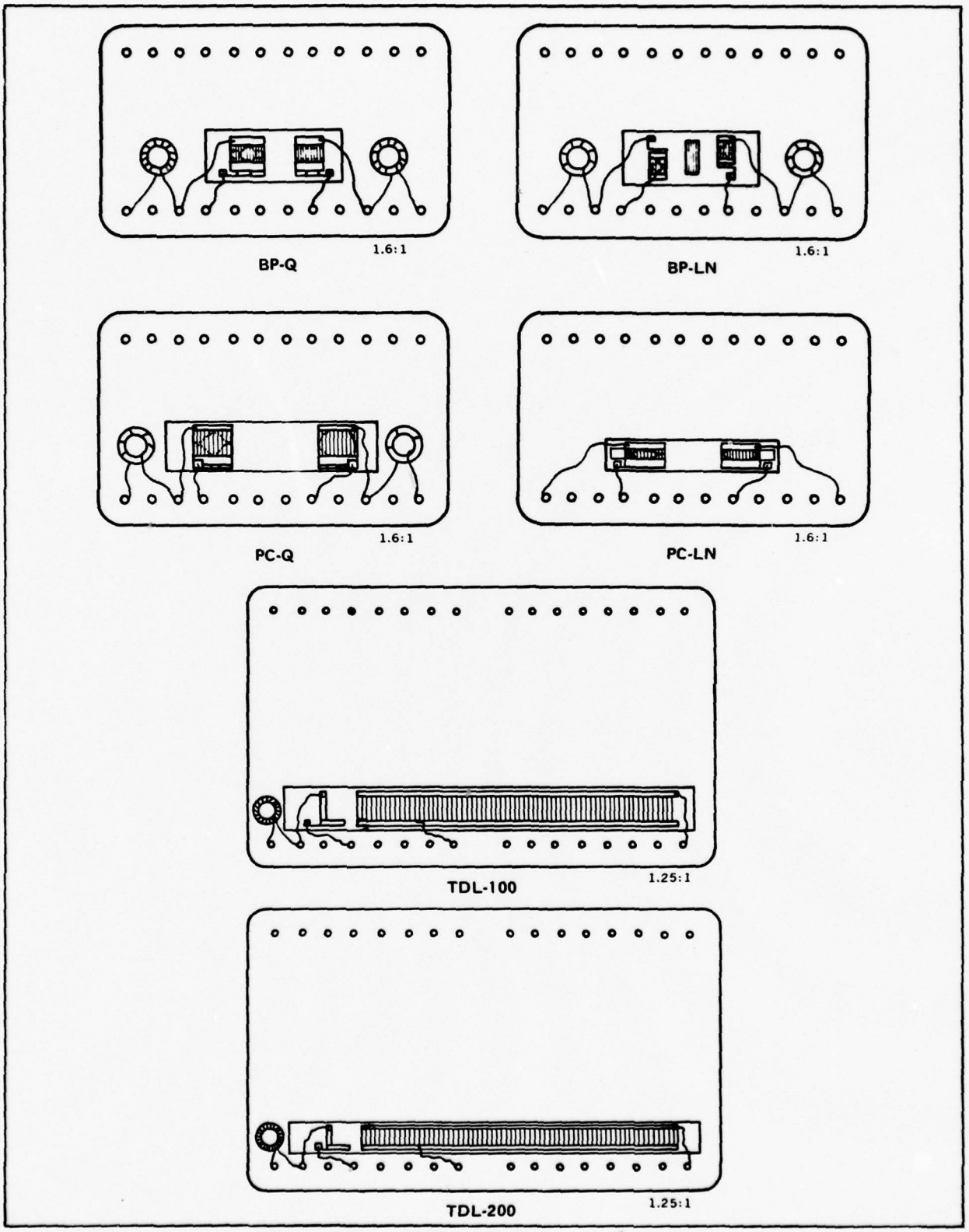

Figure 2.2-1. MMT SAW Device Configuration

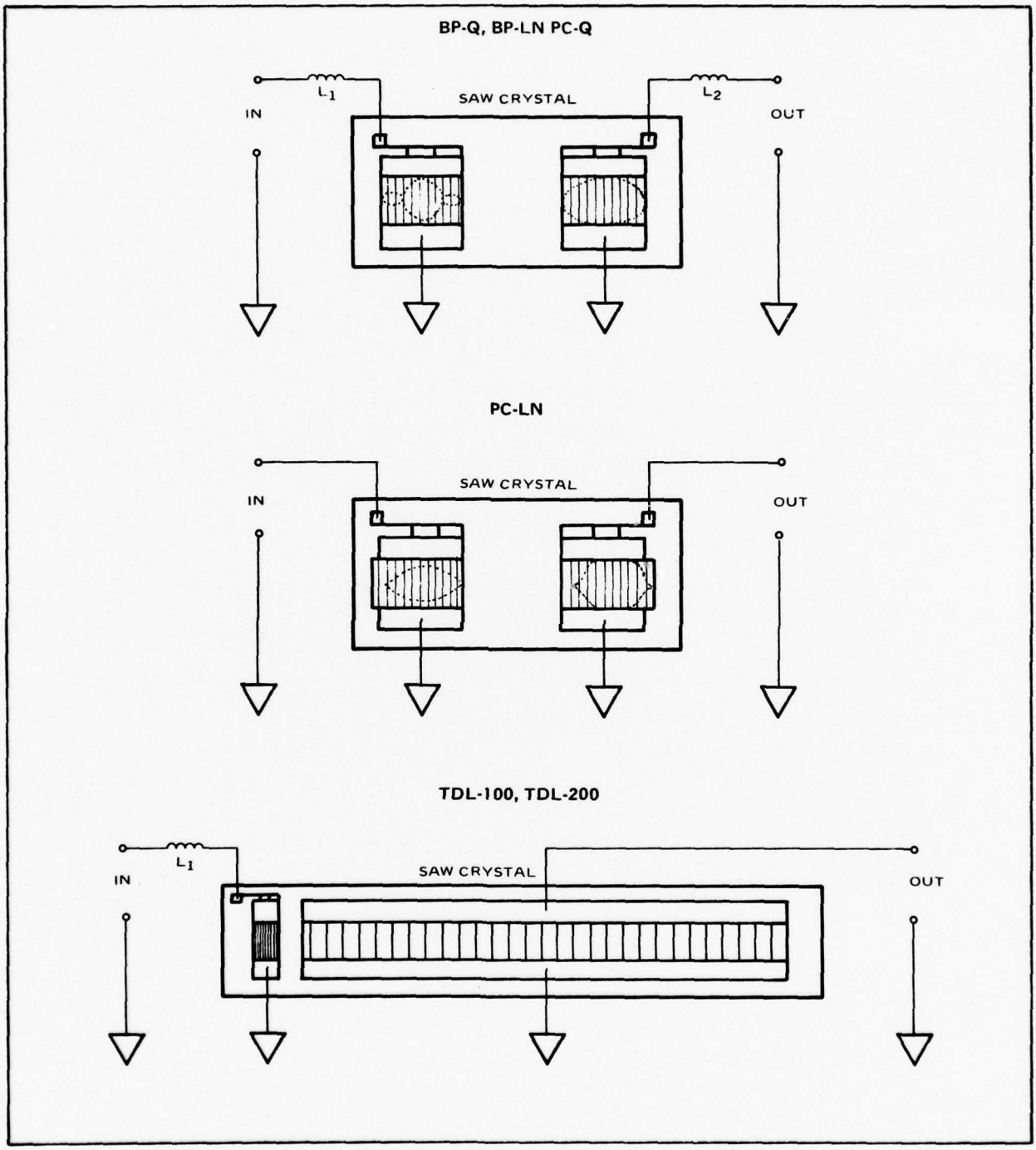

Figure 2.2-2. MMT SAW Device Schematic Representation

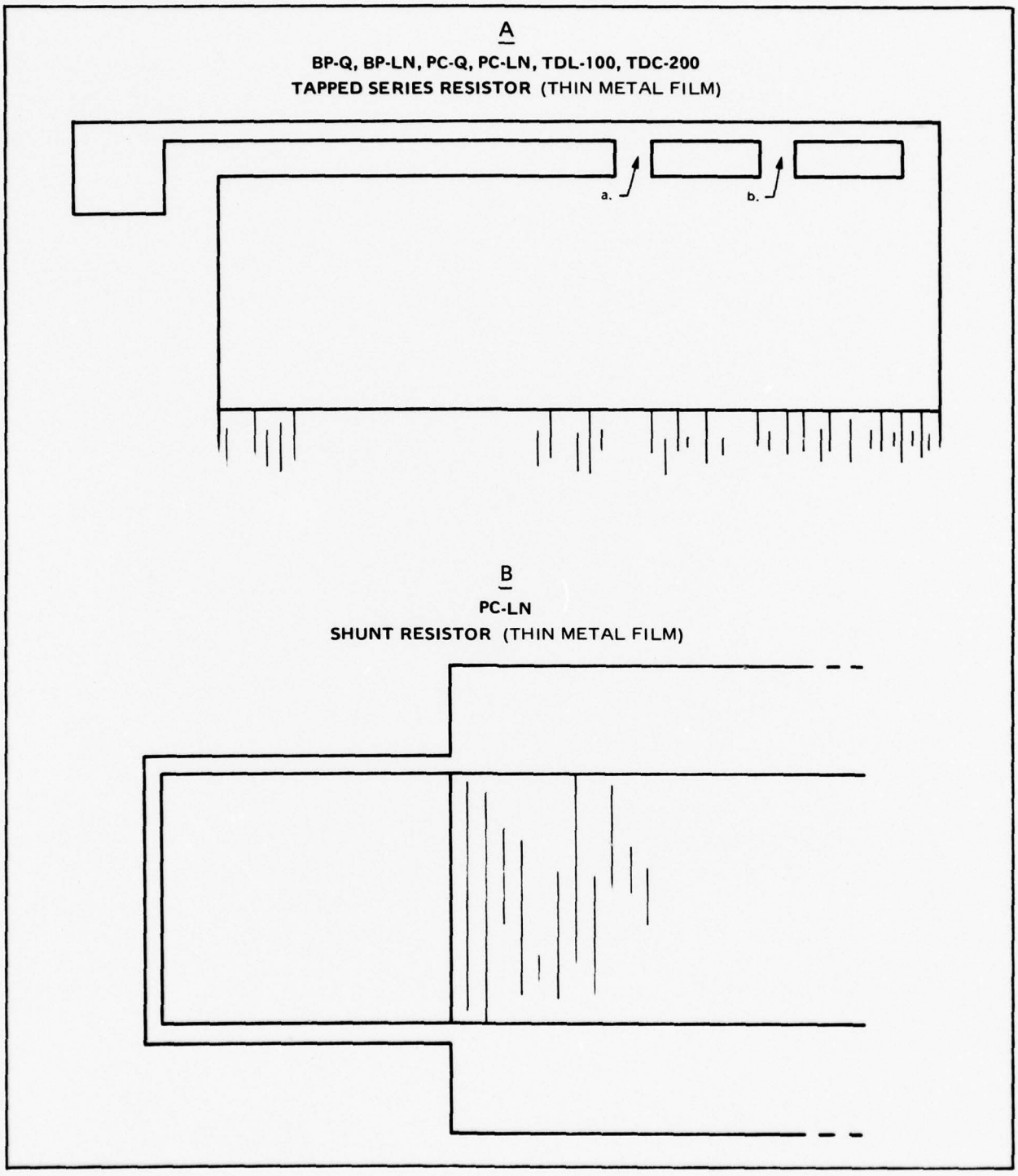

Figure 2.2-3. Resistor Detail

SECTION 3.0
PILOT LINE YIELD DATA

Section 3.0

PILOT LINE YIELD DATA (Reference Figures 3-1 through 3-6)

3.1 DISCUSSION OF YIELD LOSS FACTORS

3.1.1 Wafer Level

3.1.1.1 Photolithographic yield.

The reproduction of the surface wave transducer pattern from photomask to wafer depends on high-resolution photolithography. Ideally, the pattern is reproduced such that there is no deviation from master to print. Realistically, however, differences will appear, ranging from subtle variations in line/space ratio caused by slight variations in processing parameters, to gross defects in the electrode structure caused by foreighn particles in resist or damage to the resist image.

Once the photo process is completed there is a pre-dice inspection where the defects are mapped, their impact on electrical conformance analyzed, and yield is calculated. If the calculated yield is too low at this point, it is a simple matter to strip the wafer and reuse it in a successive lot. Higher cost is incurred in processing time, but the high cost of the substrate ($40-$50) may be saved. For the MMT effort the yield cutoff point was set at 75% or higher due to the relatively small size of the pilot runs, 8 to 35 wafers; however, it is reasonable to expect that in a full production mode (from hundreds to thousands of wafers) the yield cutoffs should be much higher, certainly above 90%. Wafers yielding lower than these established limits could be stripped and reprocessed.

One very valuable offshoot of mapping these defects, at least during pilot phases of production, is the establishment of a correlation between defect levels and device performance. Yields may be improved by establishing defect levels that are electrically acceptable.

DEVICE DESCRIPTION BP-Q PN 1950512-100

15		Wafer starts, thru photolithography, @ 33 die/wafer =495 die
	1 7	% Poor photolithographic yield - wafer reprocessed
	2 13	% Metalization scratched during capacitance probe
	2 13	% Metalization wrong thickness
		%
	0	Uninspected
10 67		% Wafers @ 33 die per Wafer OR
330		Die to precap inspection
	49 15	% Reject due to excess defects.
281 85		% Die to be diced
	44 16	% Narrow streets - excess chipping
	25 9	% Metalization scratched during capacitance probe
	15 5	% Die damaged in handling
		%
		%
	37	Unmounted spares
160 57		% Die Mount & Bond
		%
		%
	0	Unbonded
160 100		% Precap Test
	1 .6	% Bandwidth out of spec
	12 7.5	% VSWR out of spec
	2 1.2	% Insertion Loss out of spec
	1 .6	% Metalization scratched - handling
	2 1.2	% Foreign material on crystal - cleaned
		%
		%
	0	Untested
142 89		% Precap QC

Figure 3-1 Yield Analysis - BP-Q (Sheet 1 of 2)

DEVICE DESCRIPTION BP-Q PN 1950512-100

(CONTINUED)

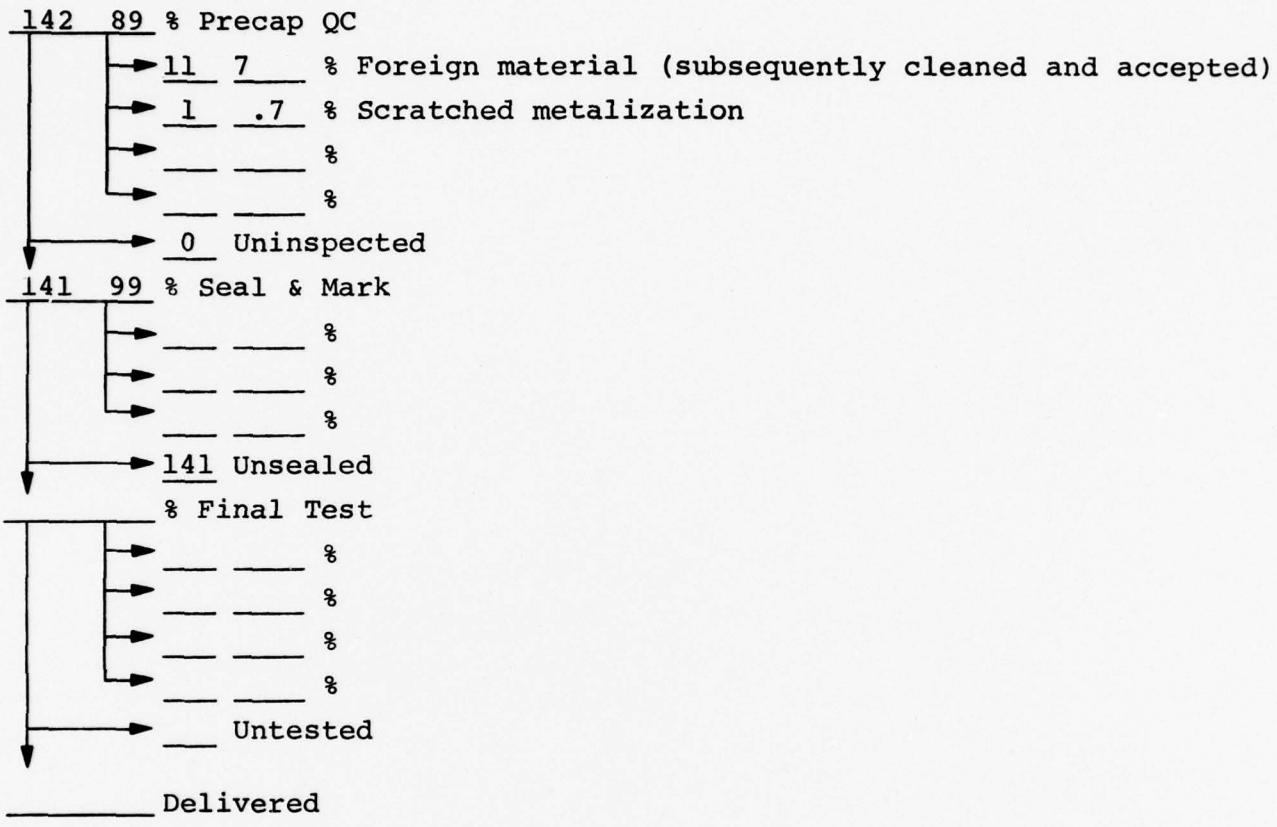

Figure 3-1 Yield Analysis - BP-Q (Sheet 2 of 2)

DEVICE DESCRIPTION BP-LN PN 1950515-100

14 Wafer starts, thru photolithography, @ 32 die/wafer = 448 die

- 2 14 % Poor photolithographic yield - wafer reprocessed
- ___ ___ %
- ___ ___ %
- ___ ___ %
- 3 Undiced

9 82 % Wafers @ 32 die per Wafer OR

288 Die to precap inspection

- 51 18 % Reject due to excess defects.

237 82 % Die to be diced

- 15 6 % Scratched in cleaning - handling
- ___ ___ %
- ___ ___ %
- ___ ___ %
- ___ ___ %
- 14 Unmounted

208 88 % Die Mount & Bond

- ___ ___ %
- ___ ___ %
- ___ Unbonded

208 100 % Precap Test

- 31 15 % VSWR out of spec
- 22 11 % Insertion Loss out of spec
- 12 6 % Sidelobes out of spec
- 7 3 % Die damaged in handling
- 4 2 % Bandwidth out of spec
- 1 5 % Toroid damaged during tuning
- ___ ___ %
- ___ Untested

131 63 % Precap QC

Figure 3-2 Yield Analysis - BP-LN (Sheet 1 of 2)

DEVICE DESCRIPTION BP-LN PN 1950515-100

(CONTINUED)

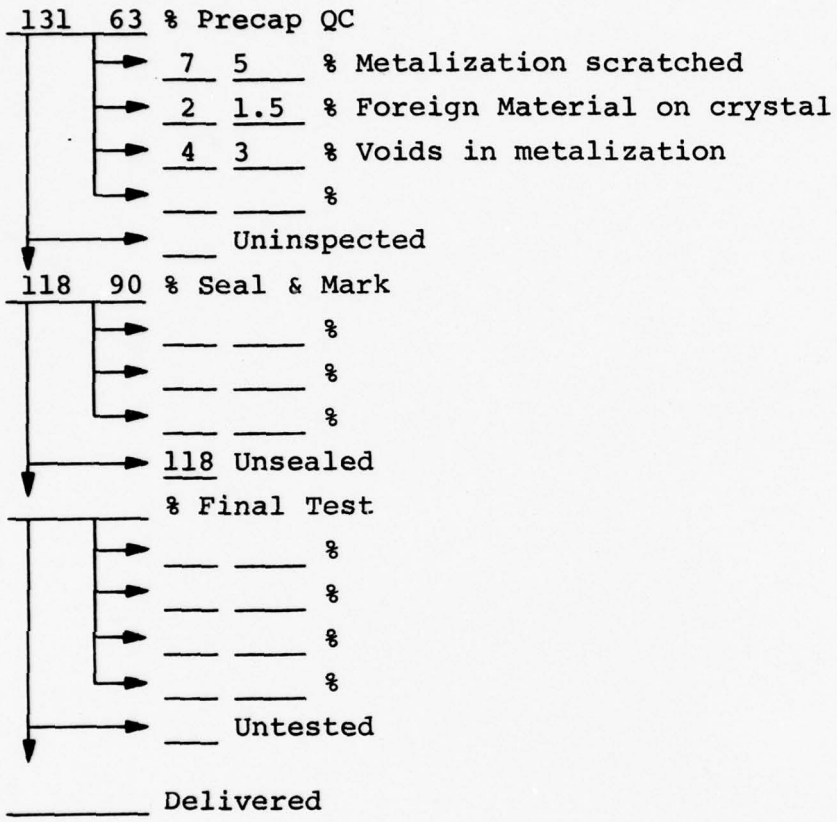

Figure 3-2 Yield Analysis - BP-LN (Sheet 2 of 2)

DEVICE DESCRIPTION PC-Q PN 1950518-100

19 Wafer starts, thru photolithography, @ 20 die/wafer = 380 die

- 2 11 % Poor photolithographic yield - wafer reprocessed
- ___ ___ %
- ___ ___ %
- ___ ___ %
- 2 Undiced spares

15 89 % Wafers @ 20 die per Wafer OR

300 Die to precap inspection

- 79 26 % Reject due to excess defects.

221 74 % Die to be diced

- 9 4 % Area between die too narrow. Excess chipping during dicing.
- 8 4 % Foreign material on crystal
- ___ ___ %
- ___ ___ %
- ___ ___ %
- 14 Unmounted spares

190 85 % Die Mount & Bond

- 30 16 % Die mounted incorrectly
- ___ ___ %
- ___ Unbonded

160 84 % Precap Test

- 8 5 % Insertion Loss out of spec
- 5 3 % Die damaged in handling
- 4 3 % Feedthru out of spec
- 3 2 % Sidelobes out of spec
- 1 1 % VSWR out of spec
- 1 1 % Metalization scratched open
- ___ ___ %
- ___ Untested

138 86 % Precap QC

Figure 3-3 Yield Analysis - PC-Q (Sheet 1 of 2)

DEVICE DESCRIPTION PC-Q PN 1950518-100

(CONTINUED)

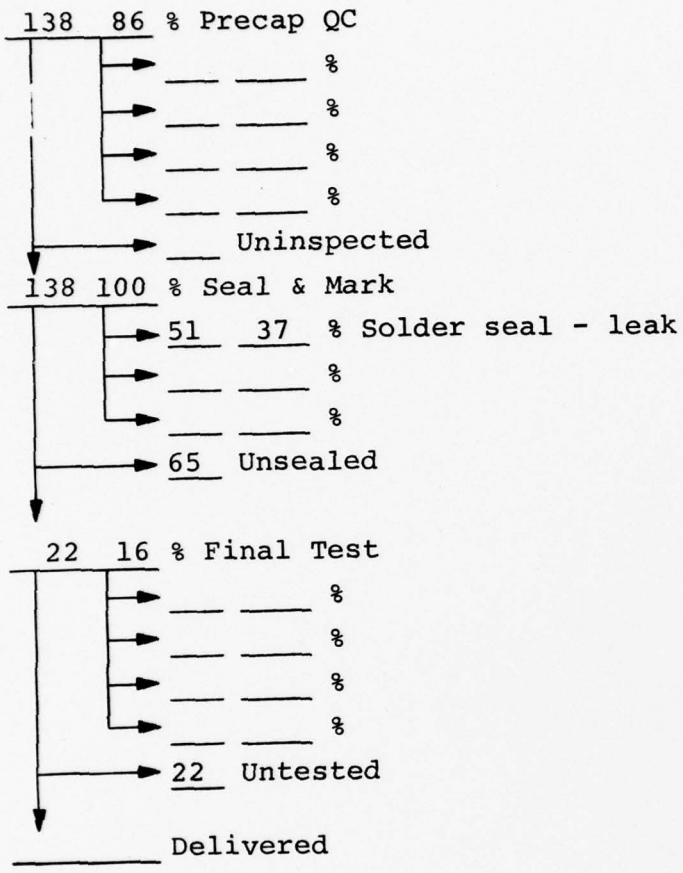

Figure 3-3 Yield Analysis - PC-Q (Sheet 2 of 2)

DEVICE DESCRIPTION PC-LN PN 1950521-100

11 Wafer starts, thru photolithography, @ 45 die/wafer = 360 die

- 1 12.5 % Poor photolithographic yield - wafer reprocessed
- ___ ____ %
- ___ ____ %
- ___ ____ %
- 3 Undiced spares

7 63 % Wafers @ 45 die per Wafer OR

315 Die to precap inspection

- 100 32 % Reject due to excess defects.

215 68 % Die to be diced

- 48 22 % - Damaged during dicing.
- 61 28 % - Wrong metal thickness
- ___ ____ %
- ___ ____ %
- ___ ____ %
- ___ Unmounted

106 50 % Die Mount & Bond

- ___ ____ %
- ___ ____ %
- ___ Unbonded

106 100 % Precap Test

- ___ ____ %
- ___ ____ %
- ___ ____ %
- ___ ____ %
- ___ ____ %
- ___ ____ %
- ___ ____ %
- ___ Untested

106 100 % Precap QC

Figure 3-4 Yield Analysis - PC-LN (Sheet 1 of 2)

DEVICE DESCRIPTION PC-LN PN 1950521-100

(CONTINUED)

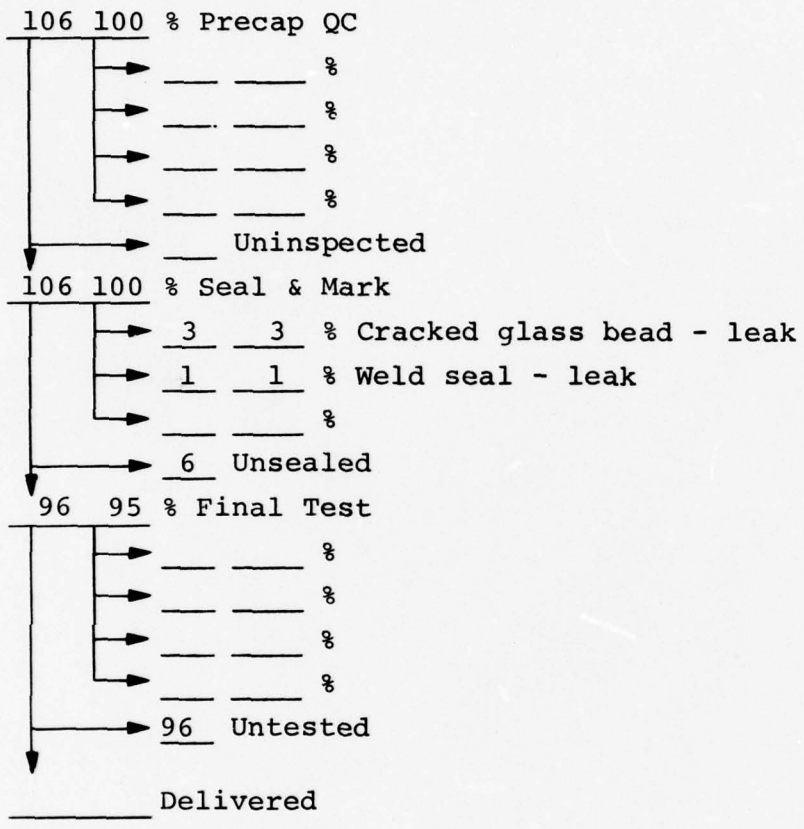

Figure 3-4 Yield Analysis - PC-LN (Sheet 2 of 2)

DEVICE DESCRIPTION TDL-100 PN 1950524-100

35 Wafer starts, thru photolithography, @ 9 die/wafer = 315 die

- 2 6 % Poor photolithographic yield - wafer reprocessed
- 3 9 % Scratched metalization
- ___ ___ %
- ___ ___ %
- ___ Uninspected

30 86 % Wafers @ 9 die per Wafer OR

270 Die to precap inspection

- 68 25 % Reject due to excess defects

202 75 % Die to be diced

- 35 17 % Damaged in handling
- ___ ___ %
- ___ ___ %
- ___ ___ %
- ___ ___ %
- 15 Unmounted spares

152 75 % Die Mount & Bond

- ___ ___ %
- ___ ___ %
- ___ Unbonded

152 100 % Precap Test

- 11 7 % Insertion Loss out of spec
- 1 1 % VSWR out of spec
- 1 1 % Damaged die
- ___ ___ %
- ___ ___ %
- ___ ___ %
- ___ ___ %
- 7 Untested spares

132 87 % Precap QC

Figure 3-5 Yield Analysis - TDL-100 (Sheet 1 of 2)

DEVICE DESCRIPTION TDL-100 PN 1950524-100

(CONTINUED)

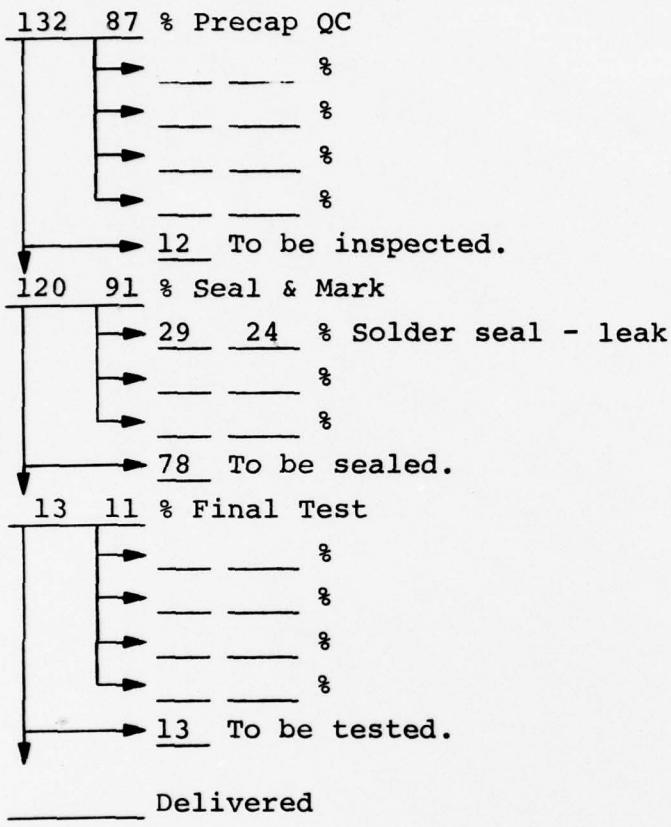

Figure 3-5 Yield Analysis - TDL -100 (Sheet 2 of 2)

DEVICE DESCRIPTION TDL-200 PN 1950527-100

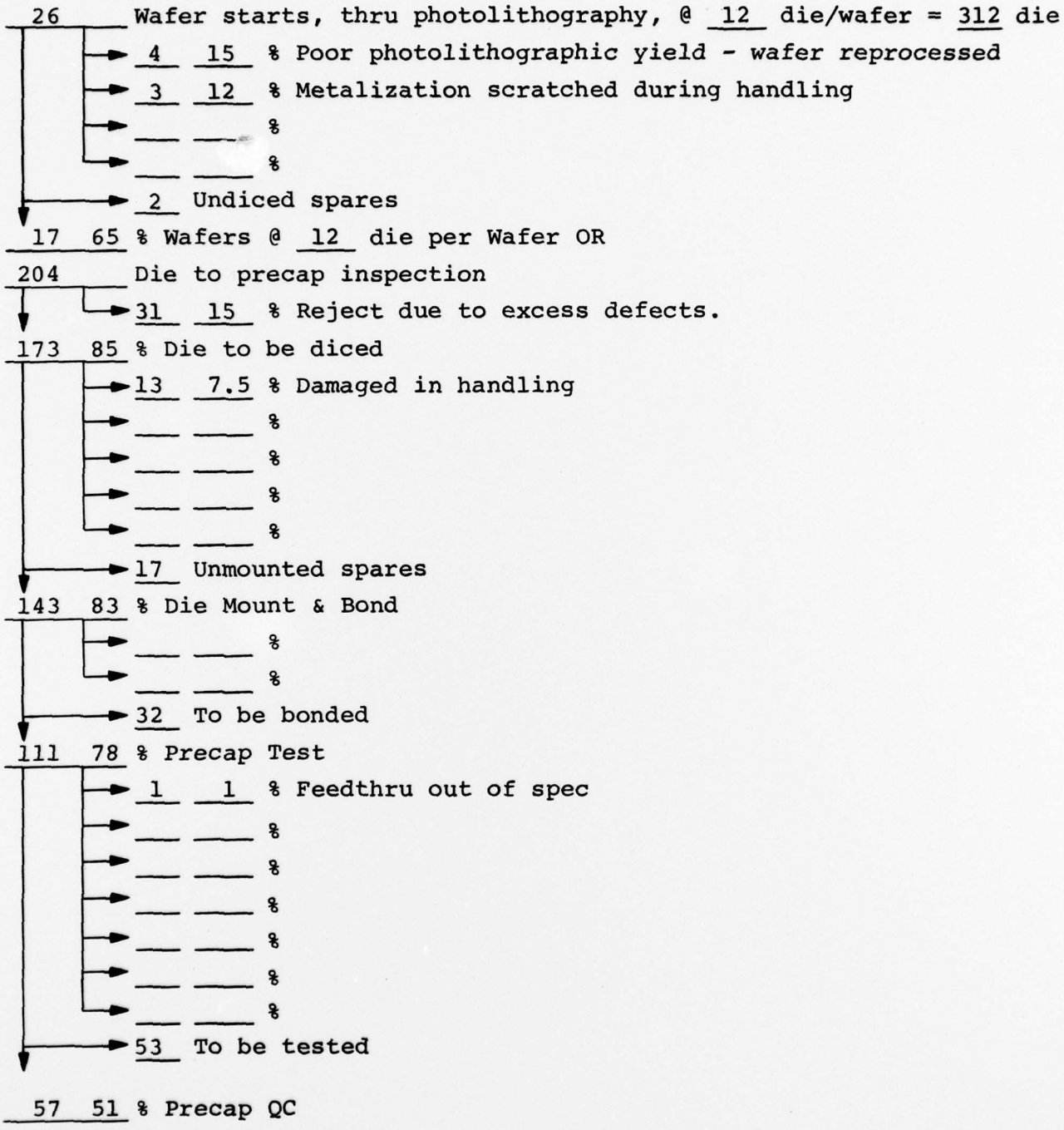

Figure 3-6 Yield Analysis - TDL-200 (Sheet 1 of 2)

DEVICE DESCRIPTION TDL-200 PN 1950527-100

(CONTINUED)

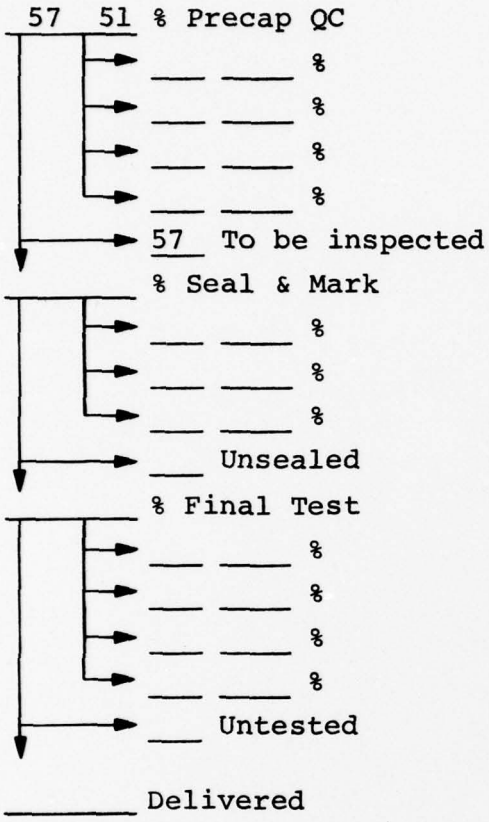

Figure 3-6 Yield Analysis - TDL-200 (Sheet 2 of 2)

Absolute defect levels for the MMT devices have not been established as it would involve substantial effort that is beyond the scope of this program. Further comments on this are offered in 3.1.3.

3.1.1.2 Scratched metallization.

Defects due to scratches in the metallized patterns are largely avoidable by using special production techniques to prevent anything from touching the top surface of a wafer from the time it is coated with metal to when the completed device is sealed in a package. The slightest touch with tweezer, probes, or even fingers, is enough to scratch completely through the metallization. Handling is minimized in the number of individual process steps the wafers are subjected to and the method in which the handling is done. The wafers are always stored and transported in semi-captivating containers and handled only by an extreme edge which has no transducer structure within a distance of 50 to 100 mils.

During the pilot phase of this program a new method of pre-dice wafer inspection was developed and implemented. This method is capacitance probing, an electrical inspection, rather than visual, that can be automated. This technique will be discussed more extensively in the final report, however, the resultant yield losses will be discussed here.

Essentially, capacitance probing involves bringing a probe array into contact with the transducer bonding pads and measuring the capacitance of the transducer structure; the measured capacitance is a function of the number of electrodes and the electrode size and spacing.

During the development of the probe process, several wafers were scratched during handling. This is a yield loss that would be overcome when the process is fully developed and in production.

Rework at this level involves stripping the old pattern and re-using the wafer in a successive lot; the loss being process and inspection time.

3.1.1.3 Metallization thickness.

Problems concerning transducer metallization thickness and resistivity were reported earlier in Quarterly Report #6, Sections 3.1.4.1 and 3.1.4.2 and the yield impact of these reported constraints is described here.

A transducer structure is designed with metal thickness (resistivity) such that the devices will operate to specified electrical parameters around the center of established tolerance limits (i.e., insertion loss, -20dB $\pm$2dB; center frequency, -150MHz $\pm$3MHz; etc.). Deviations from the design ideal due to fabrication will cause variations in measured device performance and will have resulting yield impacts. The MMT device transducers were designed using data characteristics for metallization from an R&D deposition system. When the pilot line was established for Phase III and the production deposition system was put into use, the physical characteristics of the metal films were discovered to be different with the production system depositing lower resistivity material. The measured device performance thus tended to be other than at the center of the specification limits and the shift within these limits was not the same for all performance criteria.

When insertion loss tended to be too low, even beyond specification limits, the metal was made thinner to bring the loss up, but because of the reduced mass of the electrode structure, there was a resultant upward shift in center frequency. Thus, to satisfy both specification requirements, a thickness was used that brought performance just inside the limits, increasing insertion loss just enough to be within specification, but not enough to cause the center frequency to be out of specification.

Thickness tolerances were now quite critical, often ±50Å. Yield losses resulted because of this, but the specification requirements were met.

In an actual production situation the quantities involved would justify a redesign effort to correct this problem, but redesign was felt to be unnecessary considering the scope of this program. Future SAW production will give proper attention to this condition. Rework at this level consists of stripping and reprocessing the wafer.

3.1.2 Die Level

3.1.2.1 Dicing

During the course of this program, several processing functions were upgraded to improve throughput and yield and whenever these processes could be automated at a reasonable cost, they were.

Because of the high substrate cost and the precision to which dicing of the processed wafers must be done, an automatic dicing saw technique was implemented offering very low kerf losses (of a few mils) plus the added benefit of repeatability inherent in a pre-programmed system. Problems were encountered in the actual use of this system. These problems were discussed in 3.1.5 of the Sixth Quarterly Report and 3.2 of the Fourth Quarterly Report. The yield impacts will be discussed here.

Production photomasks were fabricated prior to Phase III, consisting of an array of devices that would cover the standard 2"x 2" quartz or 2.1"x1.75" lithium niobate wafers. The die spacings had been established to maximize the number of die per wafer and were based on anticipated kerf losses of a few mils. The masks were generated and the wafers processed.

In dicing of quartz, the wider blade required to cut the material combined with the resultant chipping resulted in a substantial yield loss. When the chipping was excessive or would extend into the resistor patterns, those devices were lost. For a build of 150 each, as required in the pilot phase, it was decidedly less expensive to continue with die spacings as established and suffer the yield loss rather than generate new mask layout. Future production of quartz devices is planned to allow wider kerf.

The quartz wafers were mounted to glass plates with optical mounting pitch by using heat to melt the pitch, the cooled assembly being firmly bonded together. Removing small die from this sticky medium during demounting presents a handling problem and many parts were scratched or otherwise damaged in this step. Developments are continuing in the area of dicing to improve the saw function and mounting techniques. It is anticipated that the dicing of quartz will be just as efficient and cost effective as the dicing of lithium niobate.

3.1.2.2 Assembly.

An occasional die is lost during handling. If a die is inadvertently contaminated with RTV at the die attach stage it can be cleaned easily.

3.1.2.3 Bonding.

Thermocompression bonding is another operation where no parts are lost. It is suspected that ultrasonically bonded aluminum wire would be a less expensive method of interconnecting, but the yield impact could be no better than it is now. The assembly techniques presently being used result in nearly 100 percent yield.

3.1.2.4 Precap Test.

For a number of reasons, such as previously undetected defects in the transducers or the interconnects or an occasional faulty tuning coil the failures detected in precap test were random. Indicated yields due to these causes are in the high 80 to 90% range

and under volume production conditions would consistently be in the 90%+ range. Accept/reject criteria at the pre-dice inspection level could be refined much further than they are now so that the borderline devices would be screened out and would never go through assembly to test.

The BP-LN devices had higher yield losses at precap test than expected largely due to the metal thickness problem discussed earlier. This device seems to be more sensitive to low defect levels since it operates near the edge of several specification parameters (insertion loss, center frequency and bandwidth). This design also seems to tolerate fewer random defects in the device structure than the other designs, probably accounting for the sidelobe failures. There was also a problem with the tuning coils on the BP-LNs early in the build. The necessary inductance value could not be achieved without replacing the coils with one having one more turn. This accounts for the high VSWR losses.

3.1.2.5 Package Sealing.

It was discovered in Phase IV that the package sealing operation was not only labor intensive, but that its success or failure at hermeticity was primarily a function of operator expertise. The original decision to go with a solder sealed package was made for several reasons. There was a cost savings to be realized because the package did not need to be gold plated and less expensive tin plating was specified. Also, solder sealing had been an established process and no new tooling or equipment would be needed.

There is no longer a cost savings with the use of tin plated packages according to recent quotes we have received from the vendor. Tin plated packages with gold plated pins require a dual plating process and now cost more than if both package and pins are gold plated. There have since been problems with solder sealing the tin plated packages and presently devices sealed have a low chance of survival.

Rather than suffer the yield loss in order to get out the pilot line quantities solder sealing of packages has been suspended. The problem is being attacked in three areas. Since all the Phase IV devices have been assembled in tin plated packages a new process is being developed to solder seal them. At the same time an alternative means of sealing is being investigated. The smaller package for the bandpass and the pulse compression device was designed to be projection welded. Although projection welding works best with gold plated packages and gold plated or nickel lids, an attempt was made to projection weld the tin plated package with nickel lids. Out of 100 devices submitted, 96 sealed perfectly, 3 parts had damaged glass bead seals and 1 part leaked at the welded seal. This is an encouraging result and has caused us to pursue this method of sealing for other devices. Since it would take 3 months or more to procure enough nickel lids for the remainder of the bandpass and pulse compression devices, they are to be solder sealed after the process has been fully developed. The 100 projection welded parts are offered as proof of an improved alternative sealing method.

There are also plans to investigate the possibilities of Tungsten Inert Gas (TIG) welding to seal the package. Work has been done on other package designs with good success and initial feelings are that it would work for SAW type packages as well. The advantages of TIG welding are low capital investment and loading costs and high throughput.

3.1.3 Electrical performance as related to transducer defects.

A few general conclusions may be drawn at this time regarding electrical performance variations as a function of transducer defects. These defects can be categorized as either shorts (between electrodes emanating from opposite sum bars) or opens (missing metallization so as to cause the electrode(s) to become electrically isolated from their intended sum bar). Since shorts generally have a disasterous effect on insertion loss and VSWR, their continued presence is cause for device rejection. If these

shorts may be blown by applying a D.C. potential (similar to blowing a low current fuse) then these die may be saved.

Opens can vary in severity from there being only one or part of one isolated electrode to several randomly scattered opens, or several opens lumped together as in the case of a localized scratch. These opens have varying effects on electrical performance depending upon the particular device design. If the design is such that there are several electrodes that are active at a particular frequency, then the loss of one electrode may be of little or no consequence at all.

The BP-Q, as well as the PC-Q and PC-LN devices, seem to be relatively tolerant of low defect levels of up to a few opens in each transducer. This is evidenced by the percentage of devices that make it through precap test to be sealed. The tapped delay lines are quite tolerant of defects to the extent that three or four complete taps may be missing without ever seeing the effect on their performance. In fact, if a TDL has a short, the fix is to just scribe that tap out and as a result very few devices are lost to either shorts or opens.

The BPLN device on the other band is quite intolerant of open electrodes in the input or output transducers. The basis of rejection is VSWR, insertion loss or sidelobe levels being out of spec. The multi-strip coupler that lies between the transducers is not sensitive at all to low defect levels. Experiments whereby fully a third of the electrodes are rendered inactive has had no observable effect on performance. Whereas there is no redundancy of electrodes in the input and output transducers such that there are many electrodes sharing a common task, very low defect levels must exist. The multi-strip coupler has a high level redundancy to the extent that a significant number of the electrodes are not even needed.

Section 4.0

CONCLUSIONS

During this reporting period the Phase IV Pilot Line production has progressed to the point of package sealing. Work is being accomplished to overcome problems in this area.

Yield loss factors throughout the manufacturing process have been carefully documented and analyzed. As a result of continuous monitoring, problems in the manufacturing process have been investigated and changes implemented to improve device reproducibility and yield. As SAW device production continues to be refined, yield and cost analyses indicate that program goals are being met. High volume cost effective manufacture of military type surface acoustic wave devices is being demonstrated and is presently used for several production contracts for military systems. Costs continue to be driven down while reproducibility and reliability continue to be improved.

4.1 PROGRAM FOR NEXT INTERVAL

As the Pilot Line production run continues toward completion, process documentation and yield analysis will continue. Improvements in package sealing will be sought and the completed devices will be sampled and subjected to life and environmental testing.

APPENDIX I

Appendix I

MANPOWER SUMMARY

1 September 1977 to 28 February 1978

Function	Name	Title	Man Hours
PMO Support	L. Dyal	Group Head	71.5
Design	D. Smith	Staff Physicist	51.0
Fabrication	G. Blurton	Technician	171.9
	C. Smith	Technician	142.4
	R. Small	Technician	17.3
	P. Black	Technician	15.4
Testing	D. Coffey	Technician	252.7
Documentation	D. Nault	Supervisor	4.0
	A. Gagne	Clerk Typist	4.0
	W. Schultz	Draftsman	28.0
	L. Arakaki	Tech. Pub.	5.0
Quality Control	R. Ortiz	Supervisor	12.0
	O. Astgen	Inspector	37.0
	M. Parker	Inspector	13.5
	J. Knoop	Inspector	16.0
Quality Testing	E. Waddell	Technician	16.0

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