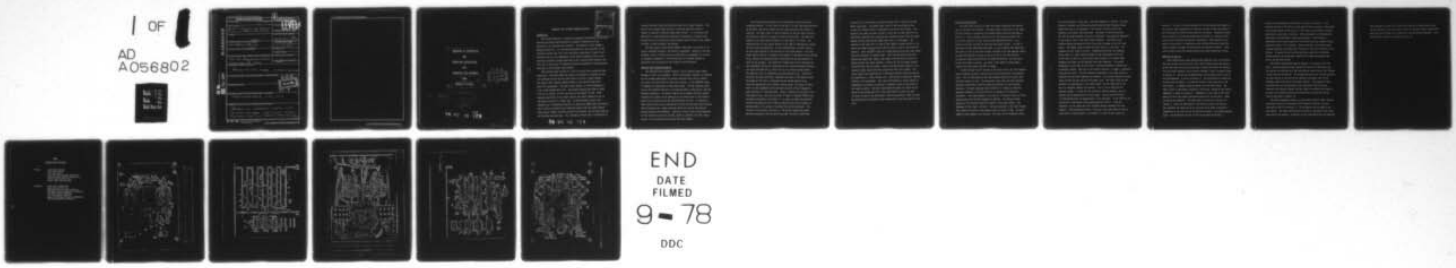
AD-A056 802 ROCKWELL INTERNATIONAL ANAHEIM CALIF F/G 14/3
HANDBOOK OF INFORMATION AND OPERATING INSTRUCTIONS FOR TRANSIEN--ETC(U)
1978 N62269-76-C-0462

UNCLASSIFIED NL

1 OF 1
AD A056802



END
DATE FILMED
9-78
DDC

AD A056802

AD No. ____
DDC FILE COPY

U

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

(1)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER —
2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER

LEVEL III

4. TITLE (and Subtitle)
HANDBOOK OF INFORMATION AND OPERATING INSTRUCTIONS FOR TRANSIENT DATA RECORDER.

5. TYPE OF REPORT & PERIOD COVERED

6. PERFORMING ORG. REPORT NUMBER

7. AUTHOR(s)
See

8. CONTRACT OR GRANT NUMBER(s)
N62269-76-C-0462

9. PERFORMING ORGANIZATION NAME AND ADDRESS
NORTH AMERICAN ROCKWELL

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
WF11-100-000/ZU701
WF11-123-702

11. CONTROLLING OFFICE NAME AND ADDRESS

12. REPORT DATE

13. NUMBER OF PAGES

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)
NAVAL AIR DEVELOPMENT CENTER
WARMINSTER, PA 18974

15. SECURITY CLASS. (of this report)
U

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)
APPROVED FOR PUBLIC RELEASE; DISTRIBUTION UNLIMITED

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)
62711N

DDC RECEIVED JUL 19 1978 F

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)
CHARGE COUPLED DEVICE, CTD, CCD

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)
HANDBOOK OF INFORMATION SUPPLIED WITH EQUIPMENT DELIVERED UNDER SUBJECT CONTRACT EQUIPMENT WAS CCD TRANSIENT DATA RECORDER.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE
S/N 0102-014-6601

389 126

U

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

(6) HANDBOOK OF INFORMATION

AND

OPERATING INSTRUCTIONS

FOR

TRANSIENT DATA RECORDER,

NADC

(15) N62269-76-C-0462

(12) 17 P.

(16) F1110D, F1112 3

(17) WF1110D00, WF11123702

(11) 1978

TRANSIENT DATA RECORDER HANDBOOK MATERIAL

INTRODUCTION

The enclosed material is intended to supplement the personal instruction which was provided to NADC personnel at Rockwell Laboratories on the operation of the transient data recorder. The material in this handbook package consists of: (1) a narrative description of the front face of the transient recorder box, (2) a brief functional description of each circuit section of the box, (3) photographs of the entire assembly as well as the individual electronic boards which make up the transient data recorder, and (4) a set of seven size "C" blueprints providing schematics of the electrical functions of the transient data recorder.

The transient data recorder is a set of circuits built around two high speed CCD's. Each high speed CCD contains two channels, one which is used as a reference channel and the other which is used as a signal channel. The input of this recorder obtains samples of the applied signal once every five nanoseconds. The input signal samples are then multiplexed to a set of 256 (2x128) data cells. One hundred twenty-eight (128) of these cells are in Channel "A" CCD, the other in the Channel "B" CCD. After complete acquisition of the signal samples, the signal samples are run to the output circuits at a slower rate. At the CCD output, each of the channels uses a differential amplifier to remove any common mode interference. This is done by subtracting the reference channel from the signal channel. After the two signals from the two CCD's are combined, they are then adjusted for DC offset and amplitude. This information stream then is transferred to

a sample-and-hold circuit and from this point to an output connector. The heart of the transient data recorder is the high speed CCD, which is capable of running at sampling speeds above 100 MHz. It is possible with these CCD's to fabricate(using multiplexing techniques) a transient data recorder which will operate at sampling speeds above 500 MHz if more complex circuitry is used to support the devices.

The high speed circuitry which supports these CCD's is critical as to layout, component placement, and choice of components. Because of the high frequency nature of these circuits, modification or adjustment of circuits or component replacement is not advised until the intended changes or adjustments are discussed with the original circuit designer.

TRANSIENT DATA RECORDER OPERATION

The transient data recorder requires a set of external power supply voltages in order to be operable. After required power supplies are obtained and the voltages adjusted (to the nearest one-tenth volt) using a digital volt meter, the unit should be ready for operation. A low bandwidth scope is adequate for observation of the output signal. (A high frequency scope such as the Tektronix 485 with 1.5 picofarads probe is required for the high frequency waveforms.) The output signals can be sampled from each channel individually by means of the connectors on the front panel or the combined output can be observed after the sample-and-hold circuits. If required, a lower sampling rate can be obtained by utilizing the alternate high frequency input connection and a signal generator which will provide the required voltage amplitude and frequency. During the initial setup a pulse generator will be required in order to provide a pulse to stimulate the input signal as well as to activate the arm control and input trigger.

The transient data recorder can be conveniently divided into three operating sections: (1) the input to the CCD's, (2) the high speed operation of the CCD's, and (3) the output and low speed operation after signal is acquired. The input signal is applied directly to the CCD input structure and should be limited to voltages less than 10 volts peak. The operating region for the input signal voltage is in the order of 1.0 volts. The sampling process of the signal applied to the input is obtained by a charge partition input configuration. In this configuration, the data recorder has the signal applied to the diffusion of the signal channel. The input range (charge capacity of sample) in the channel is determined by the setting of G_3, whereas the sampling window is controlled by the application of a pulse to the G_2 gates. The quantity of charge which will be delivered to the propagating structure is determined by the relative potentials between the input diffusion and G_3, which will act as a charge storage pocket. The sampling action is provided by the pulse applied to G_2. The barrier formed by this gate and Phase 1 determine the sides of the measuring well. The bottom of this well is determined by the voltage applied to G_3. After the sampling pulse has formed a charge packet, the charge is transferred to the propagation structure which consists of four propagation gates operated in a two-phase mode. Phases 1 through 4 are driven by the high speed drivers, which are described in detail in Drawing 770610-4 and indicated schematically on Drawing -7. In order to adjust the potential barriers and potential wells formed by these driving circuit signals to optimum height, a DC voltage is provided from the DC bias board. This circuitry is described on Drawing -5. The charge representing signal amplitude progresses into the device and after 128 cells of data have

entered each of the devices, the device changes down in speed to the low speed output mode. The output signal level is then determined by the on-chip FET follower which is connected to the end of each channel. The output of the upper and lower channels of each CCD are then applied to an operational amplifier which subtracts the reference channel from the signal channel thereby removing any common mode noise or interference. The function of the reset FET's in each of the channel's output circuits is to remove the charge from the gate of the FET which is used in the output FET follower. These reset the FET's gate to a predesignated value after each charge packet has produced its output signal. After the operational amplifier removes any common mode signals, the signal from each CCD unit goes to a sample-and-hold and signal combiner, in which the two CCD output signals are multiplexed into one output. Each of the CCD channels operates in an identical manner except that they acquire data 180° out of phase. This allows signal data acquisition at 5 nanosecond intervals while the devices are operating at a slower 100 MHz rate. Each CCD has an effective sampling interval of 10 nanoseconds. This input interleaving of signal samples is recombined at the output to provide a continuous signal at the output of the sample-and-hold. From this sample-and-hold output the signal may be taken to any conventional A/D if the proper buffer circuits are used. If access to each of the CCD outputs is desired separately, these can also be obtained from the separate output connections on the front panel of the unit.

FRONT PANEL DESCRIPTION

The front panel consists of input and output connections and controls for the transient data recorder. The power supply connections in the upper left hand corner are powered by the voltages whose values are recorded on Drawing -3. These voltages should be set to the nearest one-tenth volt. V_1 primarily supplies all the logic and the sampling amplifier. V_2 is used for the logic circuits and also the reset pulse circuit. It also is the supply for the sample-and-hold board. V_3 also supplies the sample-and-hold board as well as the final drivers and needs to be high amperage supply. V_4 similarly supplies all logic circuits as well as the final drivers. V_5 supplies sample-and-hold board, the sampling amplifier, and also parts of the final drive circuitry. V_6, which is the highest voltage supply, supplies the bias boards with their voltages.

On the left hand side of the box in the lower corner, the "low frequency cycle" connector provides a positive pulse during the entire low frequency cycle. This is interrupted by the high frequency operation at which time the pulse returns to zero. The pulse again rises after the high frequency operation and provides a positive-going pulse during the low frequency operation. The high frequency input connection is a means by which the operating frequency in the fast mode can be changed at the operator's discretion. This input requires a sine wave at a voltage at least 0.2 volts peak-to-peak with a maximum frequency of 200 MHz. The maximum voltage applied to this terminal should not exceed 10 volts peak-to-peak. The impedance of this input is 50 ohms. The next connector is the input trigger. This controls the start of the counter which will count to 256, the total number of data samples to be acquired. The input to this connector should

be a positive pulse, 1 volt peak. The input impedance is 50 ohms. The next connector provides a positive-going pulse during the high frequency signal acquisition part of the operation. This output is similar to the low frequency cycle output described above. The pulse is there only during the time the high frequency circuitry is operating. The connector immediately to the right of this is the input signal connector. The signal to be analyzed should not exceed 10 volts at any time or damage to the CCD's may result. The nominal range of signal for this input is 1 volt peak. The impedance of this input is 50 ohms. Immediately below the low frequency cycle output is a spare switch provided for the convenience of the user. To the right of this is a switch which selects between the internal high frequency oscillator and the external oscillator connector. The switch immediately to the right of this allows a selection between an internal and an external trigger. When put in the internal position, a trigger is generated every 256 data cells. The BNC connector immediately to the right allows an inspection of the clock frequency and waveform. This output connector provides access to both the fast and the slow output clock. The output level at this connector is approximately 1 volt peak-to-peak. On the right side of the box is a connector labeled "arm control". This is to be used with the external trigger. In order for the circuits to operate properly, the arm control must be operated prior to the trigger. The arm control requires a 10 microsecond pulse of approximately 1 volt amplitude. To the right of the arm control is the output of the sample-and-hold circuits. From this connector, one can obtain the total combined sampled waveshape from both channels. The potentiometer knobs in the upper right hand corner of the box allow offset of both Channels 1 and Channel 2 as well as gain control of

Channel 2. In order to allow adjustment of the two outputs with respect to one another, these adjustments are provided in order to have the output at the sample-and-hold output become properly interleaved. Immediately below the arm control and below the sample-and-hold output are connectors which allow access to Channel and Channel 2 separately. These connections are made at a point which is immediately after the CCD differential amplifier (which compares the signal in the CCD with its reference channel). These access points precede the sample-and-hold and channel adjusting circuits.

UNDERSIDE OF THE TDR

After removing the screws retaining the underside cover, and locating the fuses so they are on the lower left, the following discussion applies. On the left side of the box (at the top) is the DC bias board for Channel 2. This bias board schematic can be found on Drawing -5 with a pictorial shown on Drawing -6. The key to the abbreviations, which appear next to each of the potentiometers, is given on Drawing -6. The bias board for controlling the DC biases on Channel 1 is below the Channel 2 board and next to the fuse holders. In between these two boards lies the logic boards. The logic circuit is described on Drawing 1a and 1b and a layout of the circuit components is shown on Drawing -6. Immediately to the right of the logic board are the driver boards and mounting boards for the two CCD's. These two boards are identical. The upper board is the driver circuitry for Channel 2, while the lower board is the driver circuitry for Channel 1. The schematics for these two driver circuits can be found on Drawing -4. Immediately to the right of the two CCD driver boards is the sample-and-hold board. The description of this circuit can be found on Drawing -2.

Details of the connections to the CCD's are shown in Drawing -7. The physical location of the CCD is in the green circuit contacter in the middle of the driver boards on the top side. There are a large number of adjustments which can be made on circuits. These adjustments of potentiometers should not be touched unless absolutely necessary. If difficulty is experienced after a warm-up period of 15 minutes, the power supply voltages should be varied by small amounts. These variations in the power supply voltages should be no greater than 10 percent of the value indicated on the drawing. It should also be verified that power supplies of sufficient current capacity are being used, especially for those which supply the driver and the logic boards.

The output configuration shown on Drawing -7 is identical for both CCD's. Both the upper and lower channel FET drains are supplied by V_{10}. The sources are connected to a 25K load resistor, which forms a FET follower circuit with the on-chip FET. The voltages derived across the 25K resistors are then applied to the base of two separate transistors, one for the reference channel and one for the signal channel. The outputs of these two transistors are then applied to the operational amplifier which subtracts the reference channel from the signal and produces the signal to be used in the sample-and-hold and multiplexing circuitry that follows (and is described in Drawing -2).

The phase propagating gates ϕ_1-ϕ_4 have both DC and AC signal supplies. The drivers, which are indicated by the triangular amplifier sign are described in detail on Drawing -4. The DC supplies are provided at the bias boards. The input configuration to the CCD is described on the right hand side of the drawing. Connections to the input diffusion, the sampling

pulse applied to G_2 and the DC level which provides a charge bucket on G_3 are all indicated. The reset pulse, which is required to remove charge from the output FET follower gate is applied at the appropriate connector. A DC level is also applied to this gate via the .J7.

NADC

TRANSIENT DATA RECORDER

Photos:
- Logic Board (Front)
- Logic Board (Rear)
- D.C. Bias Board
- Transient Data Recorder (Underside)
- Transient Data Recorder (Topside) (2 ea)
- Driver Board (Top View) 2 ea
- Driver Board (Bottom View)

Drawings:
- Logic Board (770610-1a)
- Logic Board (770610-1b)
- Multiplex Sample & Hold (770610-2)
- CCD Sampling Pulse Amplifier (770610-3)
- CCD Driver Board (770610-4)
- D.C. Bias Board (770610-5)
- Logic & Bias Board Pictorial (770610-6)
- CCD Chip Connections (770610-7)

MC1550G
MC1539
μA7502
μA7502
SPEAKER
RED
GRN