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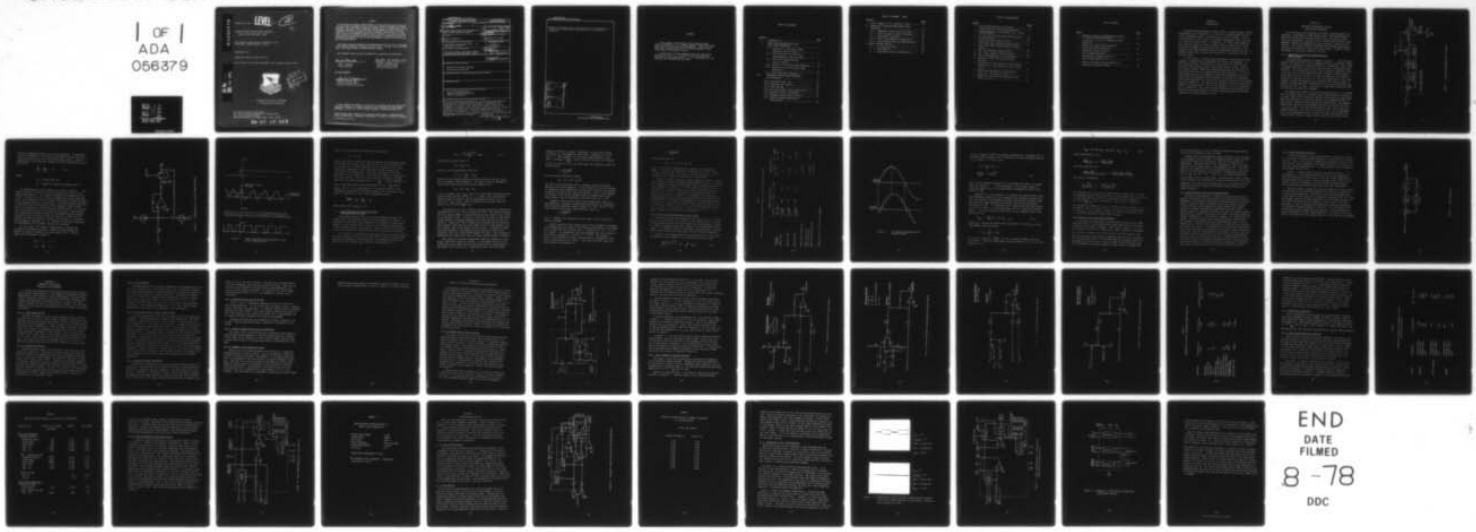

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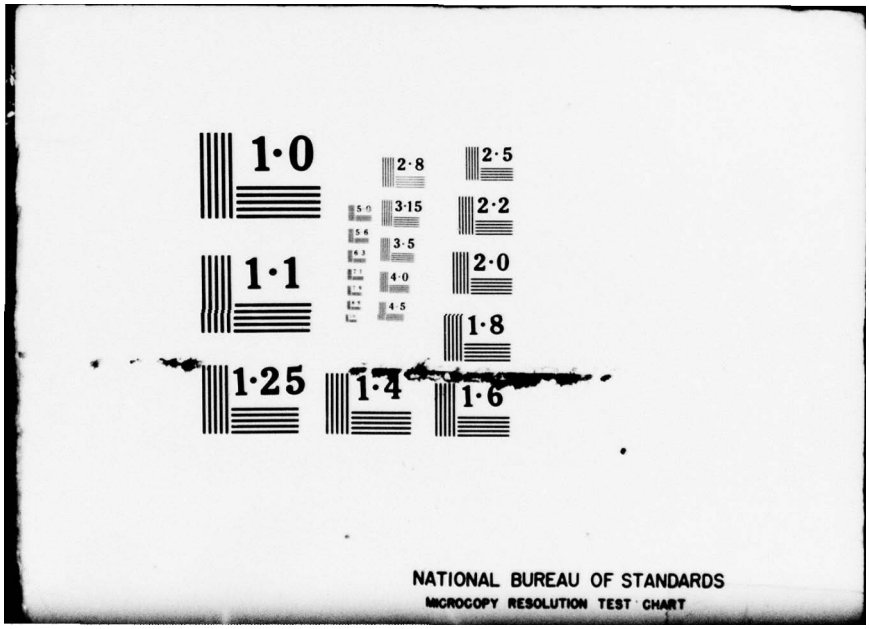
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LINEAR DEVICE APPLICATIONS ANALYSIS: DELTA SIGMA MODULATOR STUDY

The Charles Stark Draper Laboratory, Inc.
Cambridge, Massachusetts 02139

September 1977

TECHNICAL REPORT AFAL-TR-77-246

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The report describes the operation of the delta sigma modulator A-D converter and addresses the issues of integrating and hardening the circuit. The input/output relationship of the converter is stated for both DC and AC signals. A survey of commercial converters which use delta sigma modulation or related techniques is summarized. Various current switch designs, amplifier technologies, and resistive materials are examined to

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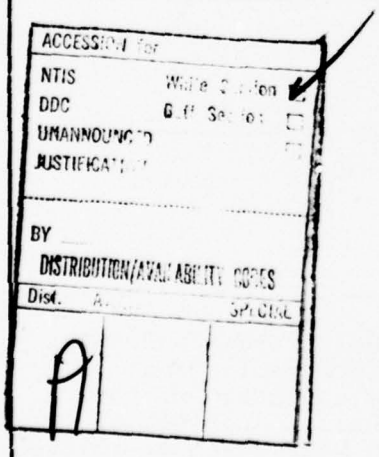
develop a radiation hard, integrated circuit configuration. A design which automatically nulls offset in the converter is outlined.



PREFACE

This report was prepared by the Charles Stark Draper Laboratory, Inc., under Contract F33615-75-C-1149 with the Air Force Avionics Laboratory. This work was done under the direction of Dr. Hans Hennecke of the Electronics Technology Division.

Publication of this document does not constitute approval by the U. S. Air Force of the findings and conclusions contained herein. It is published for the exchange and stimulation of ideas.

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SECTION I
INTRODUCTION

The delta sigma modulator offers, within a simple design, several advantages in A-D conversion. It utilizes a minimum number of precision components since it requires only a one bit ladder. Due to the simplicity of the circuit, its power requirements can be low and its size can be kept small. In addition, the delta sigma modulator has a unique feature in that it keeps track of quantization errors; therefore, averaging the digital output improves resolution. The output can be made available either in synchronous serial form or in parallel form, which allows user flexibility in the choice of the digital system.

In this report, the delta sigma modulator is described and the issues of integrating and hardening the circuit are examined. In the second section, the operation of the circuit is detailed and some past and potential uses of the converter are listed. Section III studies several commercial integrated circuits to determine if one can be utilized as a hardened delta sigma modulator. It is concluded that none of the commercial parts are satisfactory, so the fourth section discusses various methods of building an integrated delta sigma modulator with particular attention directed to the errors caused by radiation. Two designs are selected, with the final choice based on the application, and a block diagram of the chip configuration is presented. The fifth section describes a design which automatically nulls the offsets in a delta sigma modulator and outlines a method for integrating the circuit.

SECTION II

FUNCTIONAL DESCRIPTION OF THE DELTA SIGMA MODULATOR

In this section the operation of the delta sigma modulator A-D converter is described in block diagram form. The relationship between the analog input and the digital output is stated for both DC and low frequency AC signals, and it is shown how the delta sigma modulator removes the quantization error inherent in most A-D converters. The issue of moding is discussed and various applications for which the converter is well suited are listed. Finally, a brief description of the delta modulator is given.

II. 1. Operation of the Delta Sigma Modulator With DC Input

The delta sigma modulator is shown in Figure 1. The difference between the analog input and the feedback drives an integrator, whose output is converted to a binary waveform by a comparator. This signal is sampled once every clock cycle, giving rise to a synchronous waveform s(t). If the waveform is high (low) a positive (negative) level is fed back to the input summing junction through a current switch. Since the action of the loop is to keep the input of the integrator around null, the duty cycle of s(t) will be proportional to the input voltage. Though this waveform can be used as the digital output, a counter is often employed to measure the duty cycle by counting clock pulses while s(t) is high. The counter is then read periodically and is reset to zero after each reading.

To examine the output of the device quantitatively, it is assumed that the analog input is a constant signal constrained to be within $\pm V_m$ volts, and an N bit counter is used to form a parallel output word. The clock frequency is f_c and the counter is interrogated every 2^N clock pulses; hence the counting period T equals $2^N/f_c$. For maximum sensitivity, the gain at the summing junction is set such that for a $+V_m$ input signal, s(t) will be continuously high, and if the input signal equals $-V_m$, s(t) will be continuosuly low. It is impossible, due to the quantization error, to state an exact input/output relationship which assigns a unique digital word for each analog input

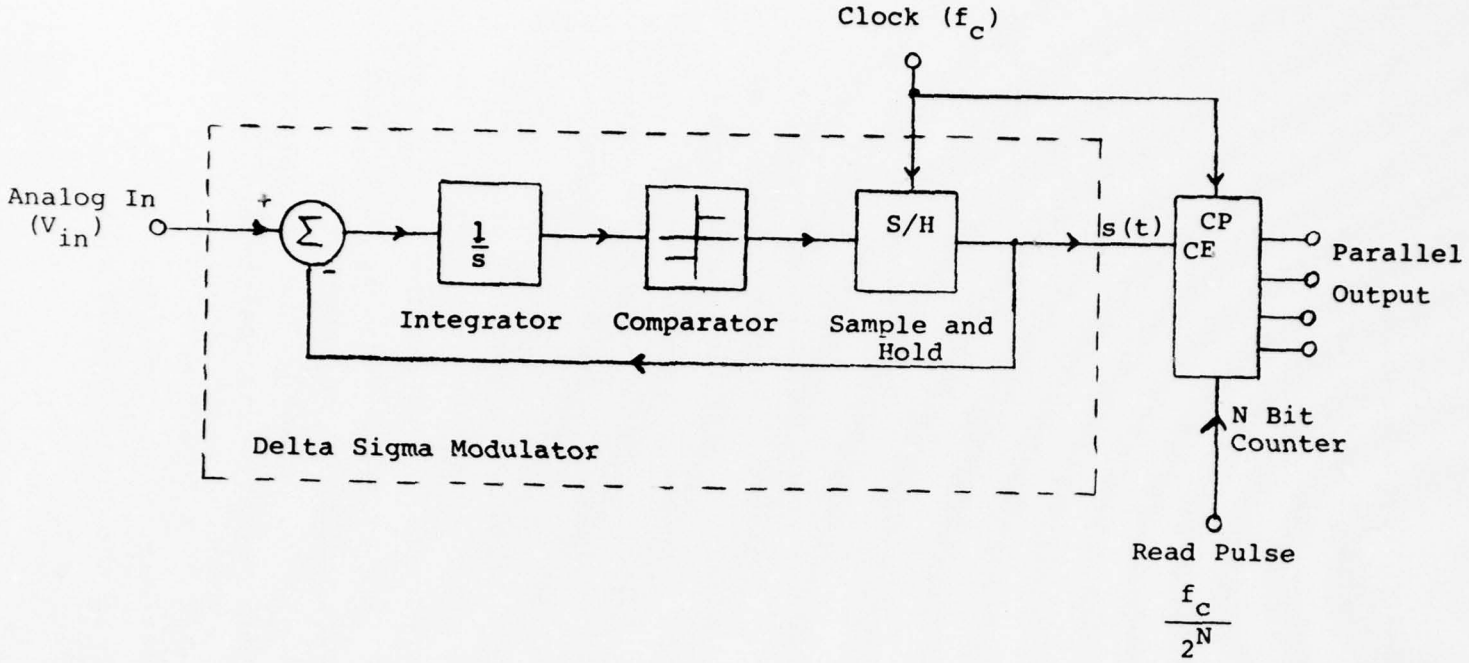


Figure 1: Delta Sigma Modulator with Counter

voltage, a phenomenon present in all A-D converters. As discussed in the next subsection, the delta sigma modulator allows the user to reduce the quantization to an arbitrarily small effect. Ignoring quantization, the relationship between the input voltage and the output word is

$$\frac{N_p}{2^N} = \frac{V_{in}}{2V_m} + 1/2 \qquad (2.1)$$

where:

V_{in} = analog input (DC)

N_p = output of counter at strobing time T

An implementation of the converter is shown in Figure 2. The summing junction is formed by adding currents at the input of the operational amplifier. The capacitor performs the integration, and a type D flip-flop is used as both the comparator and the sample and hold. As a comparator, the flip-flop would normally contain hysteresis, which provides some noise insensitivity. The zener protects the input of the flip-flop from excursions of the integrator output voltage. Since the integrator as constructed has a negative gain, s(t) is taken from $\overline{Q}$ to maintain positive gain through the circuit. The waveform s(t) controls the reference current in the summing junction through the switch: when the switch is open the current I_o flows into the junction and when the switch is closed a net current of I_o flows out of the junction (assuming $V_{in} = 0$). Usually, the current references are implemented with reference voltages and resistors.

For zero input, s(t) must be a square wave to balance the currents in the summing junction. A non-zero input upsets this balance and forces a change in the duty cycle of s(t). This is shown by the waveforms in Figure 3.

$$V_{in} = 0 \qquad t < 0$$

$$V_{in} = \frac{V_m}{3} \qquad t > 0$$

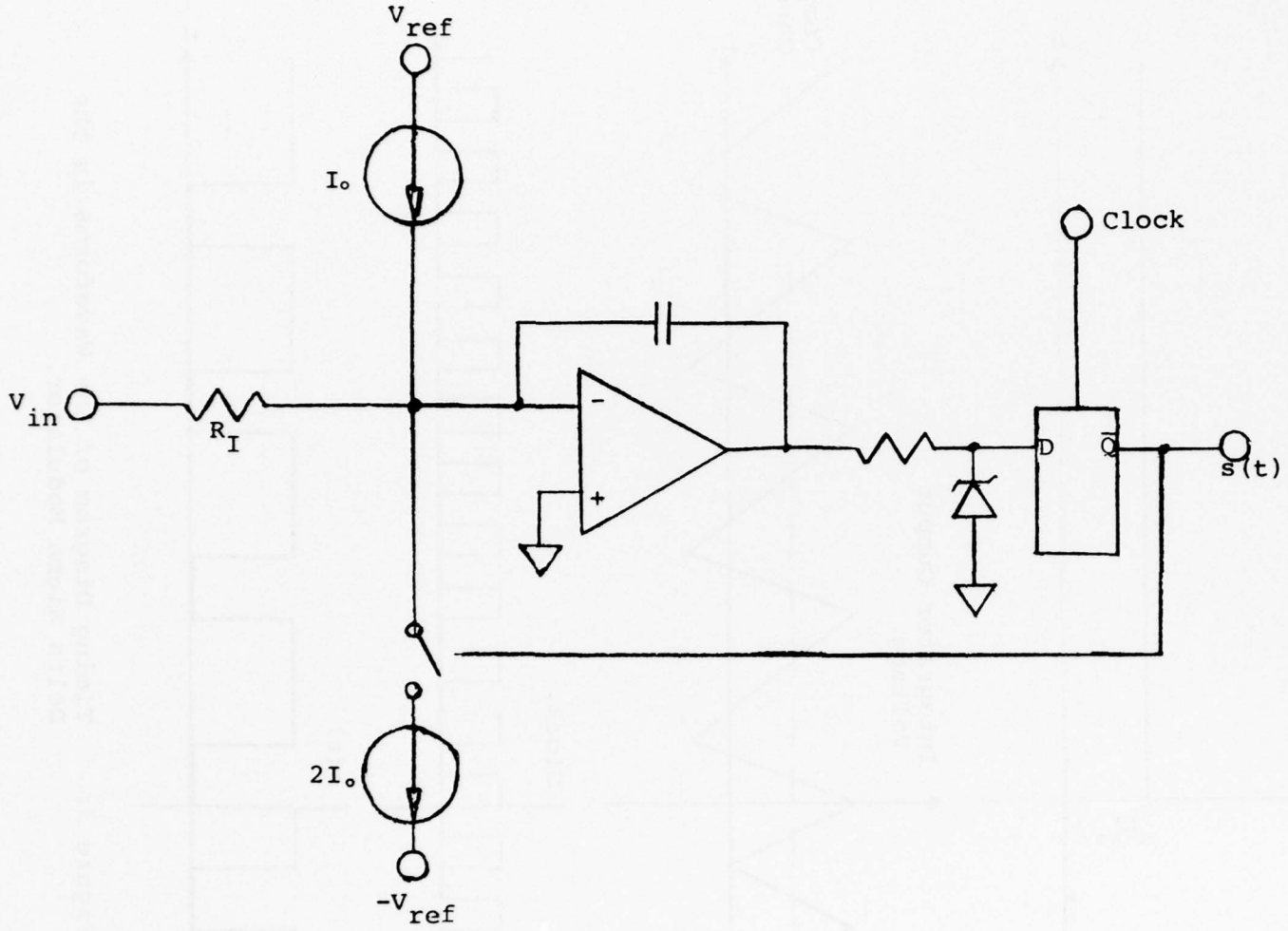


Figure 2: Implementation of Delta Sigma Modulator

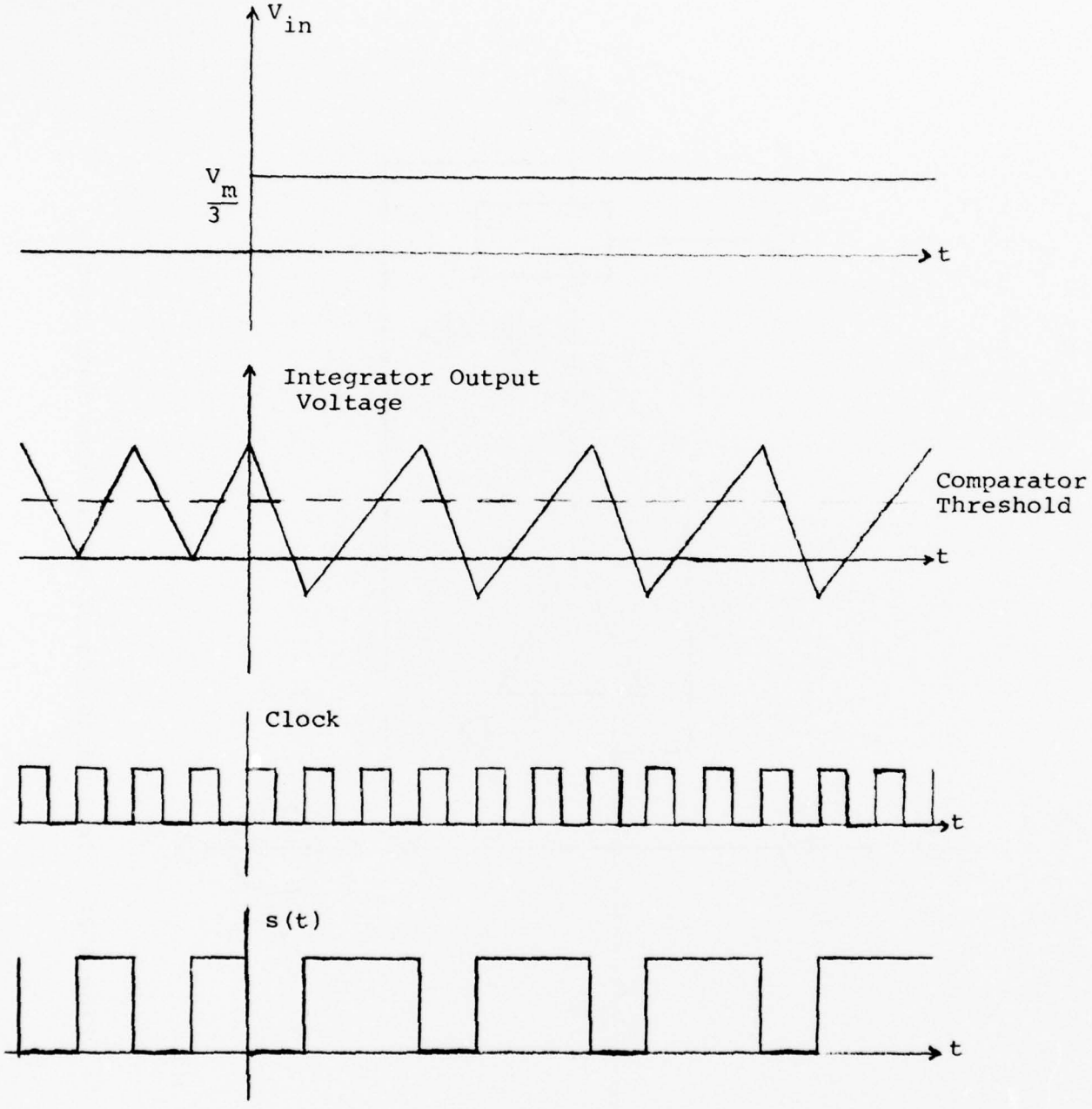


Figure 3: Timing Diagram of the Waveforms in the Delta Sigma Modulator.

where, to be consistent with the previous analysis

$$V_m = I_o R_I$$

While the input is zero the output voltage of the integrator ramps up and down with equal slope, the sign of the slope depending of the state of s(t). Each transition of s(t) occurs at the rising clock edge subsequent to the integrator voltage crossing the threshold of the comparator. Note that the Figure ignores any hysteresis in the comparator, which does not affect the analysis of the ideal circuit. After the input step the integrator voltage ramps up with slope proportional to $I_o - \frac{V_{in}}{R_I}$, which equals $\frac{2}{3} I_o$, and it ramps down with slope proportional to $-I_o - \frac{V_{in}}{R_I}$, which equals $-\frac{4}{3} I_o$. As a consequence of the negative slope of the integrator being twice the positive slope, s(t) will now be high twice as long as it is low. For a measurement time T:

$$\frac{t_{HIGH}}{T} = \frac{2}{3} = \frac{V_{in}}{2V_m} + \frac{1}{2}$$

which agrees with equation (2.1).

II. 2. Error Analysis For the Delta Sigma Modulator with DC Input

Quantization errors exist in all A-D converters because the analog input is continuous, but the digital output is discrete. An advantage of the delta sigma modulator A-D converter is that over a number of counting periods an input can be resolved theoretically to any accuracy despite quantization. Below is discussed the reason for the high resolution, and some practical limitations are shown.

The increase in resolution occurs because the integrator retains the error from one counting period and adds it onto the analog input during the subsequent counting period. To understand how this is beneficial, the voltage V_{Np} is defined: (see equation 2.1)

$$V_{Np} = \frac{2V_m (N_p - 2^{N-1})}{2^N} \text{ volts} \qquad (2.2)$$

such that the analog input is

$$V_{in} = V_{Np} + V_q$$

where V_q is the quantization error and

$$0 \leq V_q < \frac{2V_m}{2^N} = V_{LSB}$$

After the first counting period the output word will be N_p, and V_q will be stored in the integrator. The input to the A-D converter during the second counting period will appear to be

$$V_{in} + V_q = V_{Np} + 2V_q$$

If $2V_q$ is greater than V_{LSB} volts, the output word at the end of the second counting period will be $N_p + 1$. Hence, after observing the first two digital outputs, one can determine the value of V_{in} to within 1/2 (V_{LSB}) volts. After k observations, one can state the value of V_{in} to within $\frac{V_{LSB}}{k}$ volts.

The resolution will be limited in practice because the memory and characteristics of any circuit change with time. The effective resolution will be the number of counts made during the interval the circuit can be modeled as time - invariant. The limiting factor in the memory is the parallel resistance associated with the capacitor in the integrator. Charge will drain through the resistance and the resulting time constant, which may be on the order of 100 to 1000 seconds, will put an upper limit on the memory of the circuit. It should be noted that small changes in the capacitance will cause no error in the resolution since the stored charge remains the same. Other electrical parameters will change with time, and their effects deserve attention.

The offsets of a bipolar operational amplifier change at a rate usually specified roughly at 5%/week. If one models the drift as a random walk, which means that the deviations will be proporitonal to the square root of the time, a calculation shows that the offsets

change by 0.006% in a second. Therefore, if the initial offset voltage is V_e, the change in offset after t seconds is $6 \times 10^{-5} V_e (t)^{1/2}$. The resolution of the delta sigma modulator output after t seconds is $(\frac{2V_m}{f_c t})$. With V_m equal to 10V and, for a bipolar op amp, V_e equal to 1 mv, the time T when the resolution equals the drift will be

$$T = \frac{4.8 \times 10^5}{(f_c)^{2/3}}$$

and the maximum resolution becomes

$$f_c T = 4.8 \times 10^5 \ (f_c)^{1/3}$$

The limit of the resolution due to amplifier offset drifts thus improves with clock frequency. It is difficult to run the converter at frequencies much higher than 100 KHz due to errors in the analog switching circuitry which limit the accuracy. For a clock frequency at 100 KHz, T will be 220 seconds, which is compatible with the analog memory, and the resolution will be one part in 2×10^7.

Changes in the resistor values have an additional effect on the resolution. Assuming a stability specification of 0.05%/1000 hr, which through random walk theory beocmes 2.6×10^{-7} $(sec)^{-1/2}$, the time T when the resolution equals the gain error is

$$T = \frac{2.5 \times 10^4}{(f_c)^{2/3}}$$

For f_c = 100KHz, the resolution will be 1 part in 10^6, and T will equal 11 seconds.

Another source of time varying error to be considered is changes in the delays and rise times in the analog current switch. The assumption is made that the switching time, τ, drifts by $6 \times 10^{-5} \tau (t)^{1/2}$ in t seconds. By integrating, one can determine that the DC current error after t seconds is $4 \times 10^{-5} f_c I \tau (t)^{1/2}$. The current I, which is the maximum DC current from the switch, corresponds to the input voltage being at V_m. With τ = 500 nsec, the time T when the error equals the resolution is

$$T = \frac{2.15 \times 10^7}{(f_c)^{4/3}}$$

and the resolution is

$$f_c T = 2.15 \times 10^7 \, (f_c)^{-1/3}$$

Here, the resolution decreases with increasing clock frequency. With f_c = 100 KHz, the resolution is one part in 5×10^5. For f_c = 10 KHz, the resolution is one part in 10^6 and the time T is 100 seconds, which is under the limit set by the capacitor.

Another practical limitation to the resolution is due to temperature changes. Though in guidance applications the circuit is usually in a temperature controlled environment, small thermal variations are still possible. A change of 1° C will cause the offset voltage in the amplifier to vary by about 10μv, which corresponds to an error of one part in 2×10^6/°C. The resistance temperature coefficient might cause an error of 50 ppm/°C. An estimate of the temperature induced changes in the current switch was obtained by examining the specifications of the delta sigma modulator A-D converters discussed in Section III. The change in the switching times was approximately 0.2 nsec/°C in several of the devices. The resolution error would be $(2 \times 10^{-10} f_c)^{-1}$, which for f_c = 10 KHz is one part in 5×10^5/°C. Table 1 summarizes the errors in the converter.

II. 3. The Delta Sigma Modulator with AC Inputs

The above analysis has assumed that the analog input is constant; for a time varying input, the output of the counter will be a measure of the average value of the signal during the counting period. Figure 4 shows a sinusoidal input and a graph of the corresponding digital output. The transfer function of the delta sigma modulator is derived below, and the effects of quantization with AC inputs are examined.

To derive the transfer function for the converter at time T when the counter is read, equation 2.1 is rewritten for an AC signal.

$$\frac{2V_m \, (N_p - 2^{N-1})}{2^N} = \frac{1}{T} \int_0^T V_{in} \, dt \qquad (2.3)$$

TABLE 1

SUMMARY OF DRIFT AND TEMPERATURE ERRORS IN THE DELTA SIGMA MODULATOR

	AVERAGING TIME-T (sec)			RESOLUTION-T f_c	
	Relation	f_c = 10KHz	f_c = 100KHz	f_c = 10KHz	f_c = 100KHz
Capacitor Leakage	$\simeq RC \simeq$ 100-1000 sec	-	-	$10^6 - 10^7$	$10^7 - 10^8$
Offset Drift	$\frac{4.8 \times 10^5}{f_c^{2/3}}$	1034	223	10^7	2×10^7
Resistor Drift	$\frac{2.5 \times 10^4}{f_c^{2/3}}$	54	12	5×10^5	10^7
Analog Switch	$\frac{2.15 \times 10^7}{f_c^{4/3}}$	100	4.6	10^6	5×10^5
Offset Temp Coefficient				2×10^6/°C*	
Analog Switch Time Temp Coefficient				5×10^5/°C	5×10^4/°C
Resistor Temp Coefficient				5×10^5/°C*	

*Resolution Not a Function of Frequency

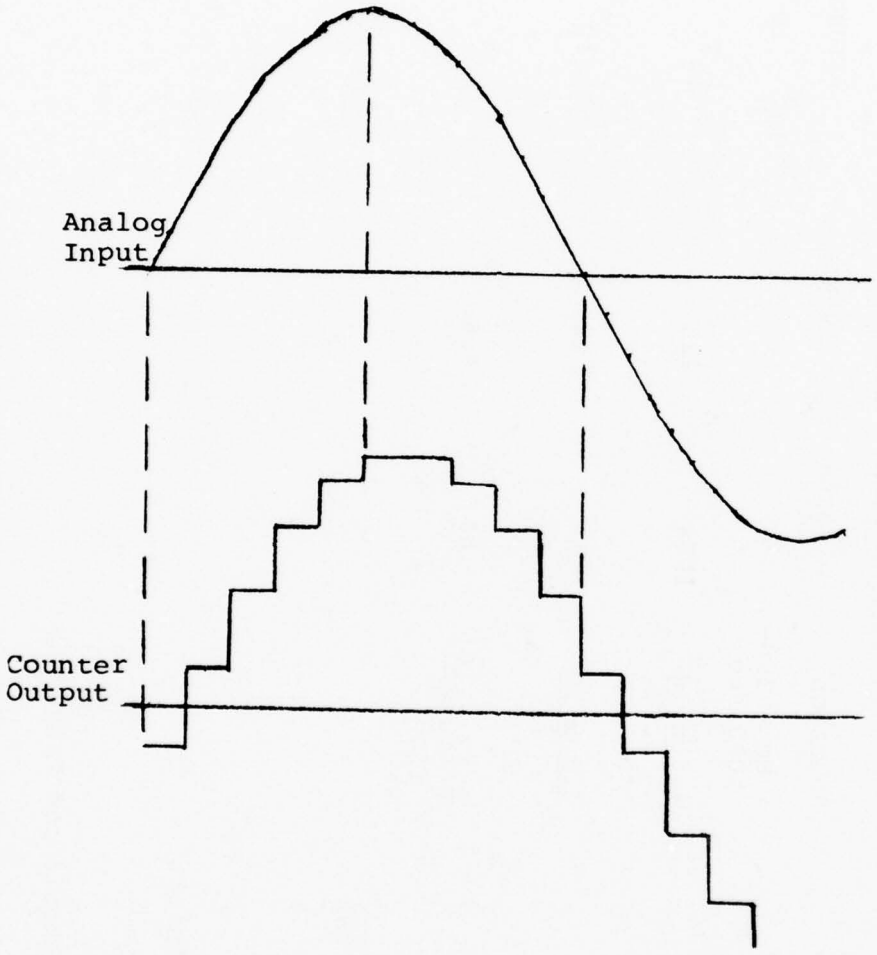


Figure 4: AC Input and Reconstructed Digital Output.

If V_{in} is equal to Ae^{st}, the Laplace transform of a sinusoid, and if the left side of equation 2.3 is defined to be the estimated value of V_{in} at time t = T, $\hat{V}(T)$, then

$$\hat{V}(T) = \frac{A}{sT}(e^{st} - 1)$$

$$\frac{\hat{V}(T)}{V_{in}(T)} = \frac{1 - e^{-sT}}{sT} \qquad (2.4)$$

6

This is the frequency response of a zero order hold and is in agreement with Figure 4. If the frequency ω of the input signal is much less than 1/T, then the phase shift introduced by the A-D converter is $\frac{-\omega T}{2}$.

Equation 2.3, like equation 2.1, neglects the quantization error; the remainder retention in the integrator can be used to reduce, but not to eliminate, the quantization error associated with an AC input. The lower the input frequency the smaller will be the achievable quantization error. To understand this, assume that the input signal is A cos ωt, where ω is fixed and known, and it is desired to determine A. Using the results stated above, at any sampling time T_1 the output will be

$$V_{Npl} = \frac{\sin \omega T}{\omega T} A \cos \omega T_1 - V_{ql} \qquad (2.5)$$

where V_{Npl} follows the definition of equation (2.2) and V_{ql} is the quantization error such that

$$0 \leq V_{ql} < \frac{2V_m}{2^N} = V_{LSB}$$

For a given frequency, $\frac{\sin \omega T}{\omega T}$ will be a constant number which will be called G. After the subsequent counting interval, $T_1 + T = T_2$, the output will be

$$V_{Np2} = GA\ (\cos \omega T_1 + \cos \omega T_2) - V_{Np1} - V_{q2} \qquad (2.6)$$

Now; from equation (2.5)

$$\frac{V_{Np1}}{G \cos \omega T_1} \leq A < \frac{V_{Np1} + V_{LSB}}{G \cos \omega T_1}$$

and from equation (2.6)

$$\frac{V_{Np2} + V_{Np1}}{G\ (\cos \omega T_1 + \cos \omega T_2)} \leq A < \frac{V_{Np2} + V_{Np1} + V_{LSB}}{G\ (\cos \omega T_1 + \cos \omega T_2)}$$

and after k measurements

$$\frac{\sum_k V_{Npk}}{G \sum_k \cos \omega T_k} \leq A < \frac{V_{LSB} + \sum_k V_{Npk}}{G \sum_k \cos \omega T_k}$$

The summation of $\cos \omega T_k$ will in general hover around zero. If only a continuous group of time intervals T_j is considered such that $\cos \omega T_j > 0$, then the summation of $\cos \omega T_j$ will reach a maximum value and the error $\frac{V_{LSB}}{\sum_j \cos \omega T_j}$ will be minimized. The lower the frequency ω, the greater the summation of $\cos \omega T_j$ and the smaller the error. In the special case $\omega = 0$ (DC), $\cos \omega T_k = 1$ for all k and the error goes to $1/k\ V_{LSB}$. As the frequency grows, the resolution decreases; for $\omega = 1/2T$, the resolution of the signal is V_{LSB}.

II.4. Moding in the Delta Sigma Modulator

To insure N bit resolution of each digital word the delta sigma modulator must be in the proper mode, which means that the loop must oscillate at the proper frequency. Referring to Figure 2.1, if $V_{in} = 0$ the signal s(t) will be a square wave, whose frequency is optimally $\frac{f_c}{2}$. In this 1:1 mode, s(t) will be high for one clock period, then low for one clock period, and the remainder stored in the integrator will never exceed 1 LSB. If the square wave has frequency $f_c/4$, the integrator will have twice as long to charge up and the upper limit of the remainder is doubled, becoming 2 LSB. Hence, the resolution

of an N bit converter in the 2:2 mode is the same as the resolution of an N-1 bit converter in the 1:1 mode:

Though a delta sigma modulator usually operates in the 1:1 mode, it can operate in the 2:2 mode. To understand this, recall that the phase shift around the loop must be - 180° at the frequency of oscillation. The phase shift of the integrator is -90° at all frequencies, and the phase shift of the comparator is zero. The phase shift of the sample and hold can be anywhere from 0° to - 360° f_m/f_c where f_m is the frequency of oscillation. The maximum loop delay for $f_m = \frac{f_c}{4}$ is - 90° - 90° = - 180°, so it is barely possible for the converter to be in the 2:2 mode. To prevent this, lead is sometimes included in the integrator to reduce its phase shift at $f_m = \frac{f_c}{4}$. Depending on the application, moding may not be a problem since the resolution will still improve if successive output words are considered together.

II. 5. Applications of the Delta Sigma Modulator

The delta sigma modulator is excellent for applications which require good accuracy and high resolution but where speed is not too important. The continuous integration associated with the converter makes it ideal for signal processing within low bandwidths servos. At CSDL the delta sigma modulator has been designed into several servos, all hardware systems with bandwidths less than 100 Hz. It has been used in a temperature control loop and in a platform stabilization servo to convert the analog error signal into proper coding for digital compensation. It was used in a torque - to - balance loop to convert an analog command into a switching waveform that drives a gyro torquer. Since with the delta sigma modulator there is no DC hangoff due to A-D conversion quantization, it was the best converter for these three servos. In particular with the platform stabilization servo, when the loop was simulated with a seven bit delta sigma modulator and a seven bit conventional A-D converter, the limit cycling in the servo error was found to be less with the delta sigma modulator. Since the output of the converter can be in synchronous serial form, it would be ideal for converting measurements from a remote low bandwidth sensor where the digital data must be multiplexed. Therefore, the converter could be utilized in avionic fly-by-wire controls.

II. 6. Delta Modulator Operation

A brief description of the delta modulator is given for, while it is similar to the delta sigma modulator, it should not be confused with it. Also, in the study of commercial integrated circuits in the next section, delta modulators were examined to see if one could be used as a delta sigma modulator. An understanding of delta modulators must precede such a study.

Figure 5 shows a block diagram of the delta modulator. The integrator is in the feedback path rather than in the feedfoward path, and the action of the loop is to set the output proportional to the derivative of the input. Often an automatic gain control is included to allow the integrator to track higher frequency signals while maintaining good noise rejection at the lower frequencies.

There are several reasons why the delta modulator is not suitable for the class of A-D conversion applications which are satisfied by the delta sigma modulator. The output is not directly proportional to the input, and the converter is relatively insensitive to DC. Also, the dynamic range of the delta modulator is small unless one uses an AGC, which then destroys the linearity of the circuit. The delta modulator is used in communications where the signals are primarily AC and where a matching decoder is used for D to A conversion after the signal has been transmitted and received. A delta modulator IC can be converted to a delta sigma modulator if the input of the integrator is available for the analog input and if any AGC can be bypassed.

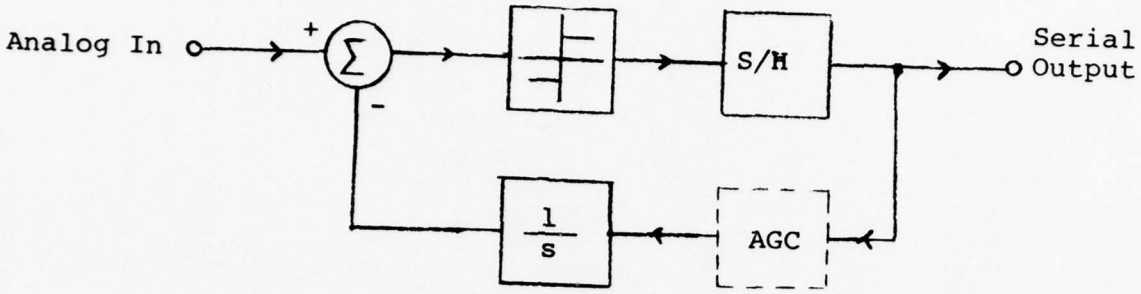


Figure 5: Delta Modulator

SECTION II
COMMERCIAL DELTA SIGMA MODULATOR A-D CONVERTERS

A survey was conducted to find commercial parts which could be used as delta sigma modulators. The companies surveyed were National Semiconductor, Analog Devices, Harris Semiconductor, Precision Monolithics, Motorola, Fairchild, Siliconix, Burr-Brown, Teledyne, Datel, Consumer Microproducts, and Hybrid Systems. No device was found which is suitable for use in a radiation hard system. The converters examined in the survey are described below, and a summary is included at the end.

III. 1. Burr-Brown ADC 100

The ADC 100 module is a delta sigma modulator with an internal reference and an internal clock, though an external clock may be used. The user can select an output word length of twelve, fourteen or sixteen bits with approximately 12.5 msec, 50 msec, and 200 msec minimum conversion times, respectively. With the bipolar converter, the input range is $\pm$ 10 volts. The maximum linearity error is 0.005% of full scale, externally adjustable to about 0.002%. Also, the gain error is below 0.05% of full scale, and the offset error is less than 0.05% of full scale. Both of these errors can be nulled externally by the user. The integrator stores the remainder after each conversion, enabling increased resolution through the averaging of several words.

III. 2. Teledyne 8700 Series

The 8700/8701/8702 devices are CMOS delta sigma modulators with 8/10/12 bit resolution. They have an internal clock, but require an external capacitor, a reference voltage, and two reference resistors. For 8, 10, and 12 bit word lengths, the conversion times are 1.8 msec, 6 msec, and 24 msec, respectively. Normally only unipolar operation is available, although an external bias circuit would allow for both positive and negative inputs. The linearity error is within $\pm$ 1/2 LSB; the gain variation is between + 5% and - 3% of nominal, and the maximum offset is 50 mv, although the gain variation and the offset error can be externally trimmed. Between each output word the integrator is discharged, so the remainder is lost.

III. 3. Datel ADC-EK

The ADC-EK seires is a group of CMOS delta sigma modulators similar to the 8700 series. An external capacitor, a reference voltage, and two reference resistors are required, and an external biasing circuit must be designed for bipolar operation. Available are models with 8, 10, and 12 bit outputs with corresponding 1.8 sec, 6 msec, and 24 msec conversion times. The gain error is + 5% to - 3% of nominal, and the offset is under 50 mv; both errors are externally adjustable. The maximum nonlinearity is $\pm$ 1/2 LSB. These devices apparently do not retain the remainder in the integrator.

III. 4. Siliconix LD110 - LD111, LD130, LD131

Siliconix manufactures three A-D converters that use "Quantized Feedback", a scheme equivalent to delta sigma modulation. The LD110, a bipolar - PMOS analog circuit, and the LD111, a PMOS digital circuit, comprise a $\pm$ 3 1/2 digit A-D converter. The LD130 and the LD131 are two monolithic CMOS converters with $\pm$ 3 digit and $\pm$ 3 1/3 digit outputs, respectively. Each device requires the addition of a clock, two capacitors, a reference voltage, and for the LD110, two reference resistors. In all three circuits, every measurement interval is followed by an autozero interval whose duration is one-third the total cycle. For autozeroing, the input is disconnected from the integrator and any offsets are automatically nulled. One of the consequences is that the remainder voltage on the capacitor is lost. The input range is about $\pm$ 5 volts, and for the fastest device, the LD131, the minimum total cycle time is 16.6 msec. The linearity error is less than 0.1% of the reading, and the gain errors can be nulled by the external components.

III. 5. Motorola MC3417 and MC3418

The MC3417 and MC3418 are two delta modulators which utilize I^2 L technology. Both devices can be connected as delta sigma modulators, and when so connected they are identical. The user supplies a clock signal, a capacitor, a reference voltage, and two reference resistors. In addition an external counter is required since the digital output is in serial form. The input voltage can be positive or negative; its

range is set by the input resistor. The data rate is determined by the clock frequency, which can be as high as 200 KHz. Since the devices are not intended to be used as delta sigma modulators, the linearity error must be estimated. It appears to be 2% of nominal, and the maximum offset is 7 mv. The remainder is stored in the integrator.

III. 6. Consumer Microcircuits FX-209

The FX - 209 is a PMOS delta modulator which can be used as a delta sigma modulator. To the circuit must be added a clock, a counter, and an integrator with amplifier. A reference voltage and two reference resistors are also needed. The clock frequency must be less than 125 KHz. The accuracy is not explicitly stated, but is approximately 2% of nominal, and the integrator will retain the remainder. [7]

Consumer Microcircuits has announced a new delta modulator, the FX-309. From the preliminary data it appears to be similar to the FX-209.

III. 7. Hybrid Systems DV620, Harris 55516/55532

The DV620, 55516, and 55532 are delta modulators which cannot be used as delta sigma modulators. None of these devices give access to the input of the integrator for the analog voltage, and all three circuits have an AGC in the loop which cannot be circumvented by the user.

III. 8. Summary of the Commercial Parts

None of the A-D converters seem to be suitable for a radiation hardened missile or avionic system. All of the devices, except for the ADC 100 and the 3417/3418, use MOSFET's in the analog circuitry which, as discussed in the next section, are easily damaged by radiation. The ADC 100 is the only converter designed as a delta sigma modulator which retains the remainder in the integrator, allowing very high resolution. Unfortunately, this device is not an integrated circuit, but a comparatively large module (2" x 4" x 0.4", 72 pins). The 3417/3418 is not designed or specified as a delta sigma

modulator and would require an external counter and control logic to form a parallel output word. It does not appear to be worth pursuing.

SECTION IV
DESIGN OF A RADIATION HARD DELTA SIGMA MODULATOR

In designing a radiation hard delta sigma modulator, the critical circuit areas are the current switch, the resistor summing junction, and the operational amplifier. The digital circuitry is easily hardened and the comparator is fairly simple to harden. Offset errors in the comparator do not significantly affect system performance (if they are stable) since the integrator which precedes it has near infinite DC gain. In this section various designs for the current switch are discussed and several semiconductor technologies for the amplifiers are considered with reference to the effects of radiation. The estimated radiation induced errors for different combinations of switch design, amplifier, and resistors are stated. The assumption was made in the analysis that the reference voltages would be externally supplied and possible errors in the references were not considered. Two designs are found to have comparable performances; the actual choice between them would depend on the specific application. A suggested chip configuration is shown and feasible electrical specifications are given.

IV. 1. Candidate Current Switch Designs

The current switch converts the digital output waveform of the sample and hold to an analog current whose average value will be equal and opposite that of the input current. An important requirement on the A-D converter is that it be able to accept both positive and negative inputs. One reason for this specification is that if the converter is to be used to measure the error signal in a servo loop, it must be able to respond to both positive and negative excursions of the error. The current switch is the subcircuit most affected by this feature, for it must be able to add or subtract current from the summing junction. One question to be answered in the selection of a configuration is whether there should be two switches and one resistor, or one switch and two resistors, since either will allow bipolar operation. Below, five switch designs are described.

A design often used in commercial D-A converters provides for closed loop control of the collector current in a sense transistor. In Figure 6, the digital input to Q_3 determines if Q_2 is on or off. During normal operation diode D_1 is off and the negative

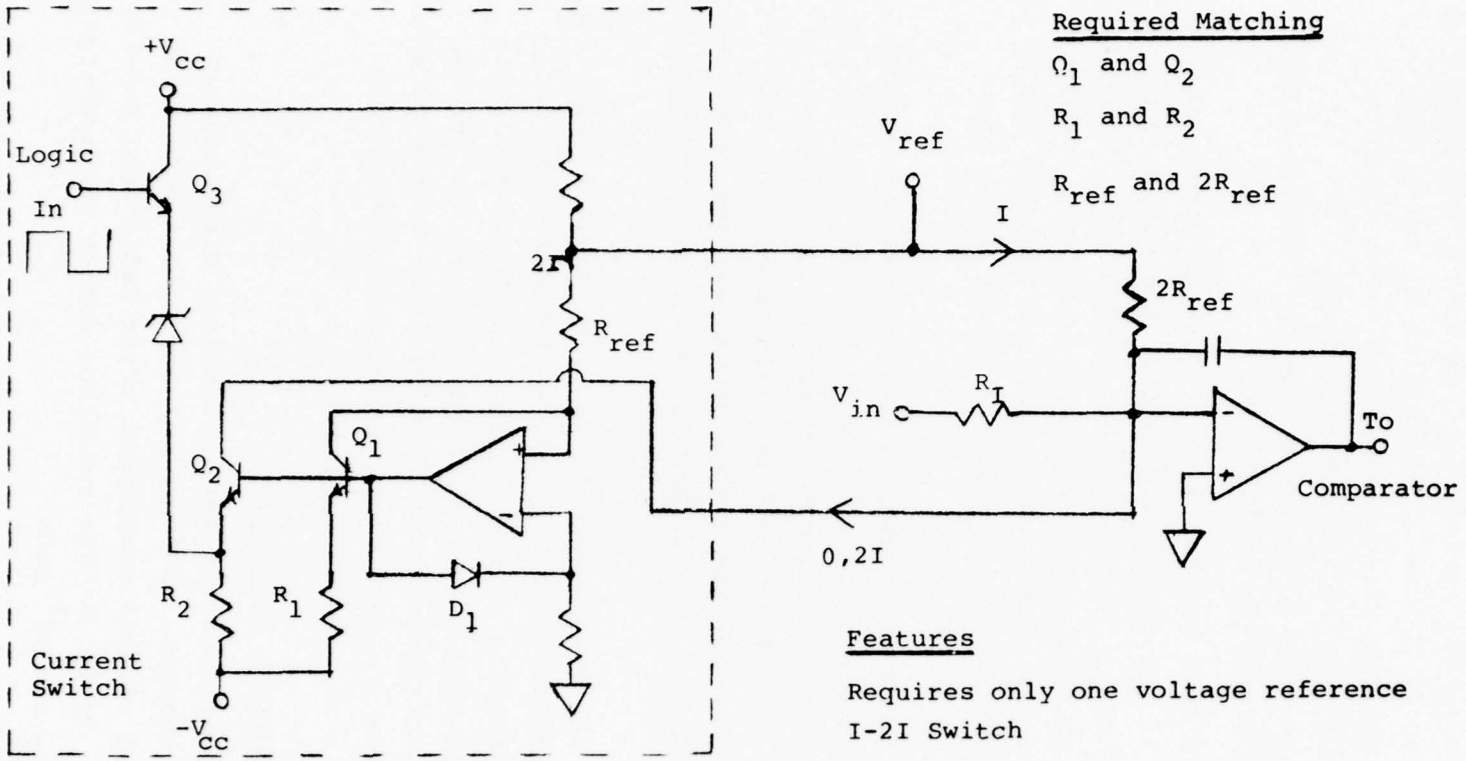


Figure 6: Transistor Match Current Switch

terminal of the differential amplifier is at ground. The collector current of Q_1 will equal V_{ref}/R_{ref} independent of transistor beta or base emitter voltage; so if Q_1 and Q_2 along with R_1 and R_2 are well matched, the output current will be regulated. The diode D_1 prevents the amplifier from latching into a high state. An advantage of this design is that it requires only one voltage reference, though it has an extra differential amplifier.

Another bipolar transistor switch, used by Sprague Electronics, is shown in Figure 7. If the transistor is off, the output current will equal $(V_{ref} - D_1 + D_2)/R_{ref}$, and when the transistor is turned on the output current drops to zero. To maintain accuracy the voltage drops across D_1 and D_2 must be equal, which requires that the diodes be matched and that the bias current through D_2 set by R_1 be equal to the output current.

This design appears to be modifiable into a one resistor scheme (Figure 8). When the transistor is off the resistor R_1 must supply current to the positive reference through D_2, and to the reference resistor and $-V_{cc}$ through D_1. Again, the currents through D_1 and D_2 must be nominally equal. When the transistor is on, the upper leg is off and the components D_3, D_4, R_{ref}, and R_2 form a current source similar to Figure 7.

In Figure 9 is an FET switch used by CSDL in previous radiation hard designs. The dual transistor scheme allows a faster turn off of the series switch by providing a low impedance path for the parasitic capacitance to discharge. Also, photocurrent from the series FET will be pulled to ground through the parallel FET. If the parallel FET is returned to the negative reference, a dual switching scheme using only one resistor is achieved (Figure 10).

IV. 2. Error Sources in Current Switches

The errors in each switch design were determined with emphasis on the radiation induced changes. Assumptions were first made as to the variations in critical circuit components after radiation, and the assumptions are stated in Table 2. The radiation dosage was arbitrarily chosen to be $3 \times 10^{14} \frac{n}{cm^2}$ and 10^6 rads.

Based on the data in Table 2, the errors in each design were calculated. In Figure 6, the main source of error besides resistor

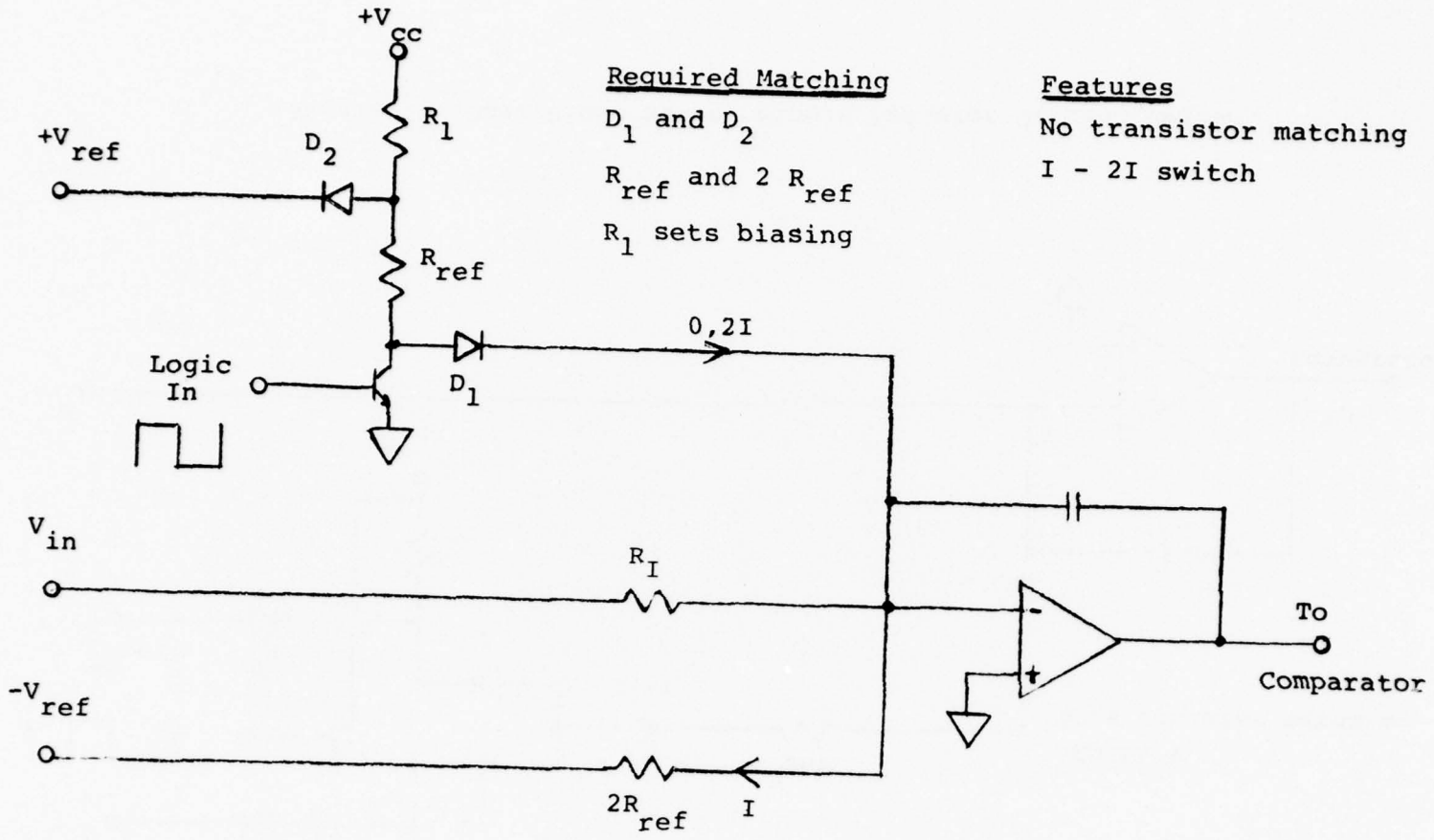


Figure 7: Diode Match Dual Resistor Current Switch

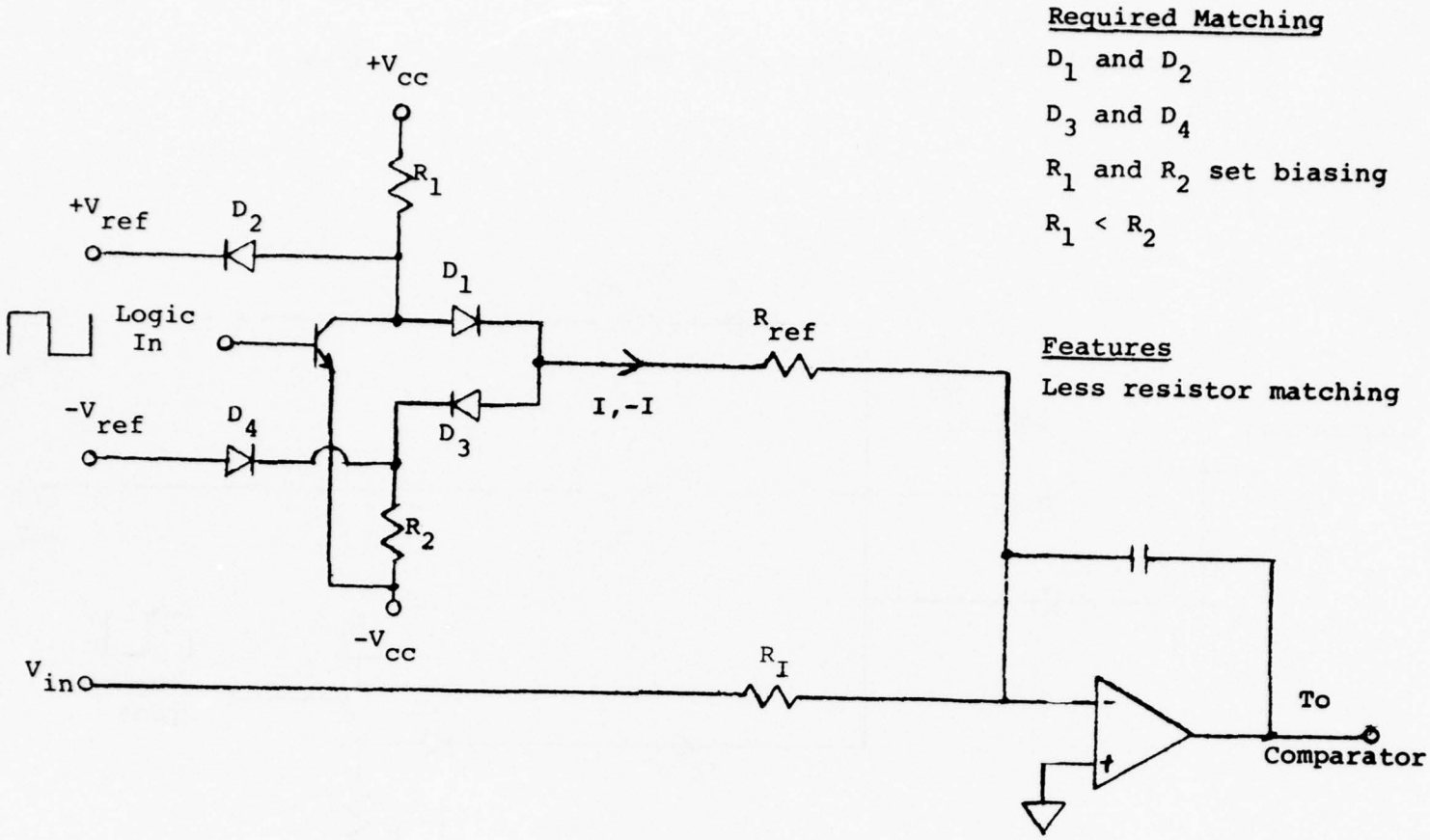


Figure 8: Dual Diode Match, Single Resistor Current Switch

Required Matching

R_{ref} and $2R_{ref}$

Features

I - 2I Switch

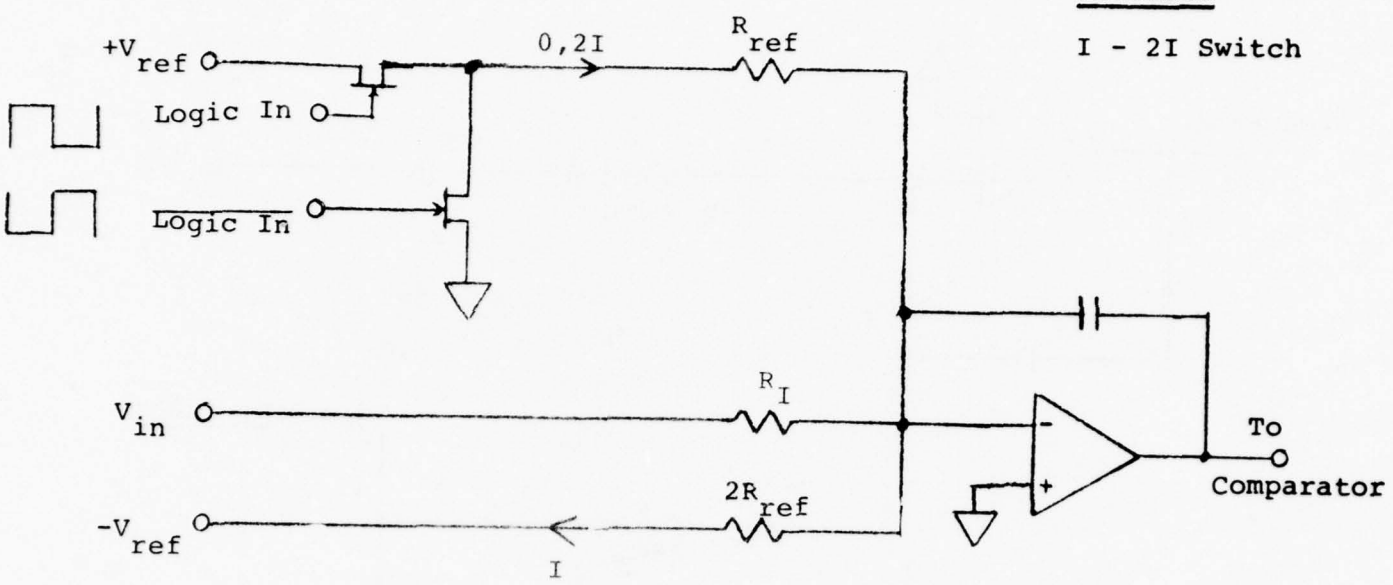


Figure 9: FET, Dual Resistor Current Switch

Required Matching

FET on-resistance

Features

Least matching requirements

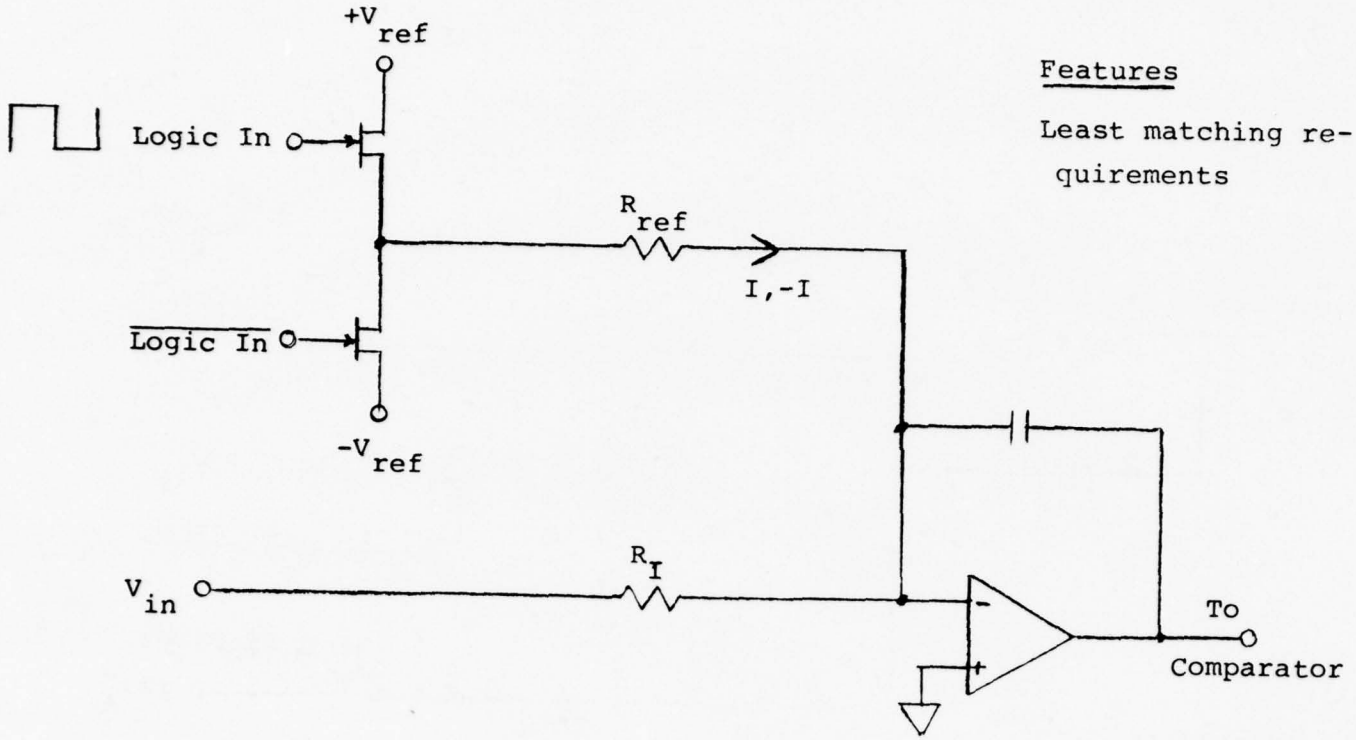


Figure 10: FET, Single Resistor Current Switch

TABLE 2

VARIATIONS IN CIRCUIT PARAMETERS AFTER RADIATION

PARAMETER	PRE RADIATION VALUE	POST RADIATION VALUE	ACHIEVABLE POST RADIATION MATCH IN IC
Resistance			
Bulk Silicon	R	2R	10%
Thin Film	R	1.005R	0.5%
FET On	1KΩ	2KΩ	10%
Transistor V_{BE}	-	-	2mv
Diode Voltage Drop	-	-	1mv
Transistor Beta	-	5	10%
Diode Reverse Current	1nA	10nA	
FET Off Drain Current	0.1nA	1nA	
Collector Base Reverse Current	10nA	100nA	
Switch Rise Time	500nsec	700nsec	

mismatch is in the transistor beta match. The post radiation beta mismatch would cause about a 2% error in the output current. In the two diode designs (Figures 7, 8) the primary source of error is resistor mismatch causing changes in the current flow through the matching diodes. The resulting voltage offset, which will be reflected as an error in the apparent reference voltage, will be 6 mv in the single switch scheme and 8.5 mv on the positive reference and 6 mv on the negative reference in the double switch scheme. These calculations assumed the use of thin film resistors. For the FET configurations, errors will be caused by changes in on-resistance upsetting the balance of the summing junction. Radiation induced delays in the switching will affect all of the circuits.

IV. 3. Operational Amplifier

Three semiconductor technologies for the operational amplifier have been considered: bipolar, MOSFET, and JFET - bipolar. Table 3 shows typical parameters of the amplifier for both pre and post radiation conditions. The assumed radiation dosage is the same as before: $3 \times 10^{14} \frac{n}{cm^2}$ and 10^6 rads. JFET - bipolar is a newer technology, and determining its post radiation characteristics required some estimating.

IV. 4. Delta Sigma Modulator Comparison

The various current switch designs, amplifier technologies, and resistor types were combined to form several delta sigma modulators. The analog input range was assumed to be $\pm$ 10 volts and the reference voltages were assigned the values of + 6 volts and - 6 volts. Table 4 gives the worst case offset and gain errors of the delta sigma modulators due to radiation. The value of the input resistor, R_I, is also given. Bulk silicon resistors were considered only in designs which used one current reference resistor, since their resistance changes would lead to large offsets otherwise.

From Table 4 several conclusions can be drawn. MOSFET amplifiers cannot be used due to their ultra high offsets, and bulk silicon resistors cannot be used when accurate gain is required. Diode matching is superior to transistor matching, though it should be noted that the design in Figure 6 requires only one reference. One resistor with two switches is superior to two resistors with one

TABLE 3

OPERATIONAL AMPLIFIER PARAMETERS BEFORE
AND AFTER RADIATION

OP AMP	PARAMETERS	PRE RADIATION	POST RADIATION
Bipolar	Voltage Offset	0.5mv	2mv
	Current Bias	1nA	500nA
	Current Offset	1nA	500nA
	Gain	150K	50K
JFET - Bipolar	Voltage Offset	1mv	5mv
	Current Bias	-	10nA
	Current Offset	-	10nA
	Gain	100K	30K
MOSFET	Voltage Offset	10mv	1v
	Current Bias	-	1nA
	Current Offset	-	1nA
	Gain	50K	15K

TABLE 4

RADIATION INDUCED ERRORS IN DELTA SIGMA MODULATORS

CIRCUIT TYPE	VALUE OF R_I BEFORE RADIATION	OFFSET	GAIN ERROR
Thin Film Resistors			
Bipolar Op Amp			
Transistor Match	5KΩ	0.60v	2.9%
Diode Match	5KΩ	0.12v	0.6%
Dual Diode	5KΩ	0.022v	0.6%
FET - 2R	260KΩ	0.63v	1.8%
FET - 1R	35KΩ	0.080v	5.3%
JFET - Bipolar Op Amp			
Transistor Match	100KΩ	0.62v	2.9%
Diode Match	100KΩ	0.15v	0.6%
Dual Diode	100KΩ	0.034v	0.6%
FET - 2R	1MΩ	0.22v	1.2%
FET - 1R	700KΩ	0.030v	1.0%
MOSFET Op Amp			
Any 2R		>6v	1-3%
Any 1R		>2.7v	1%
Bulk Silicon Resistors			
Bipolar Op Amp			
Dual Diode	5KΩ	0.024v	10%
JFET - Bipolar Op Amp			
FET - 1R	350KΩ	.030v	11%

switch, due to offset errors inherent in matching two current reference resistors. The double diode switch with the bipolar amplifier has better performance than the dual FET switch with the JFET-bipolar amplifier. However, the FET design uses less power in the resistor summing junction than the diode scheme. Both configurations should be considered depending on the particular design constraints.

IV. 5. Chip Configuration and Specification

A layout of the A-D converter as an integrated circuit is shown in Figure 11. Either an all bipolar technology or a JFET - bipolar technology can be used in the design. Since an input range of $\pm$ 10 volts is desirable, for it is the most compatible with any preamplifier, a $\pm$ 15 volt and 5 volt supply are required. The resistors are internally mounted in the chip; however provisions have been made for external gain adjustments. The integrating capacitor is externally mounted; this along with the external clock gives some flexibility to the user in choosing the sampling rate. The maximum allowable clock frequency will be limited by radiation induced changes in the switching times. The frequency probably cannot be above 100 KHz without adding gain errors greater than 1% post radiation. The positive input terminal of the amplifier is brought out to allow for offset correction. The digital output is available in serial form from the flip-flop or in parallel form from a counter. The eight bit word length was found to be satisfactory when the delta sigma modulator was used as an input to a microprocessor. Also, eight bits is about the resolution available post radiation due to the gain errors shown in Table 4 (0.6% $\simeq$ 1 part in 200). The converter specifications are summarized in Table 5.

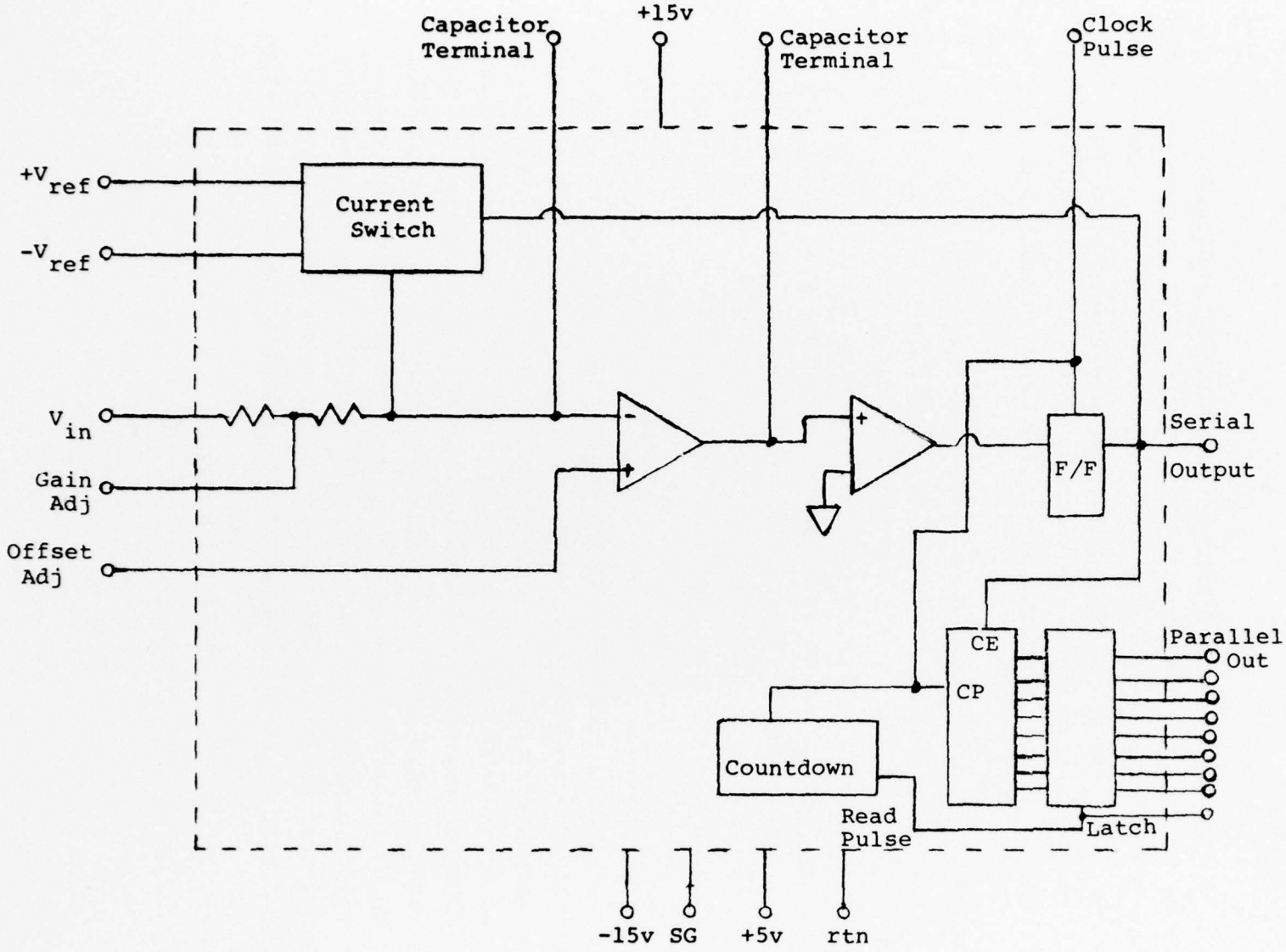


Figure 11: Delta Sigma Modulator IC Configuration

TABLE 5

PRE-RADIATION SPECIFICATIONS OF
DELTA SIGMA MODULATOR IC

Analog Input Range	± 10v
Offset Error	30mv*
Gain Error	±2% **
Clock Frequency	up to 100 KHz
Output Word Length	8 bits
Pin Count	23

*Externally adjustable to zero.

**At maximum clock frequency. Externally adjustable to zero.

SECTION V

OFFSET NULLING DESIGN

Work has been conducted to develop a method of nulling the offsets in delta sigma modulator converters. While presently it is possible to allow for manual offset adjustments, as shown in Figure 11, a design which automatically tracks long-term drifts would represent a significant advance. Any nulling technique must not interfere with the remainder voltage on the capacitor or with continuous observation of the input. A design was tested and shown to be feasible, and a block diagram of an integrated circuit which incorporates the scheme is presented. 3

V. 1. Circuit Description

The design uses two delta sigma modulators in parallel, with a chopper at the front end (Figure 12). Depending on the state of the chopper, which runs at a 50% duty cycle, each input is looking either at the analog voltage or at ground. The components with memory, the capacitors and flip-flops, are juggled between the converters synchronously with the input chopper. As a result, one capacitor and flip-flop continuously sense the analog input added to the offsets in the circuits, while the other capacitor and flip-flop sense just the offsets. If the outputs from the two flip-flops are subtracted by an up-down counter, the output word will be proportional to the input voltage and independent of the offsets. Additional logic in the converter is needed to route the signal from each flip-flop to the appropriate current switch. The resultant A-D conversion gain will be the average of the gains of the two converters.

V. 2. Test Results

The circuit was breadboarded with a four bit up-down counter to form the digital output, and as an aid for measurement, a DAC converted the output word back to an analog signal. Offsets were introduced by placing a voltage source within one of the summing junctions. Though the testing was minimal, it was demonstrated that the design virtually eliminated offsets. Table 6 shows the output of the test circuit with the input grounded and with various values of offset voltage. Ideally, with zero input the output of the D-A converter should be 5.00 v (corresponding to the four bit word 1000). The only

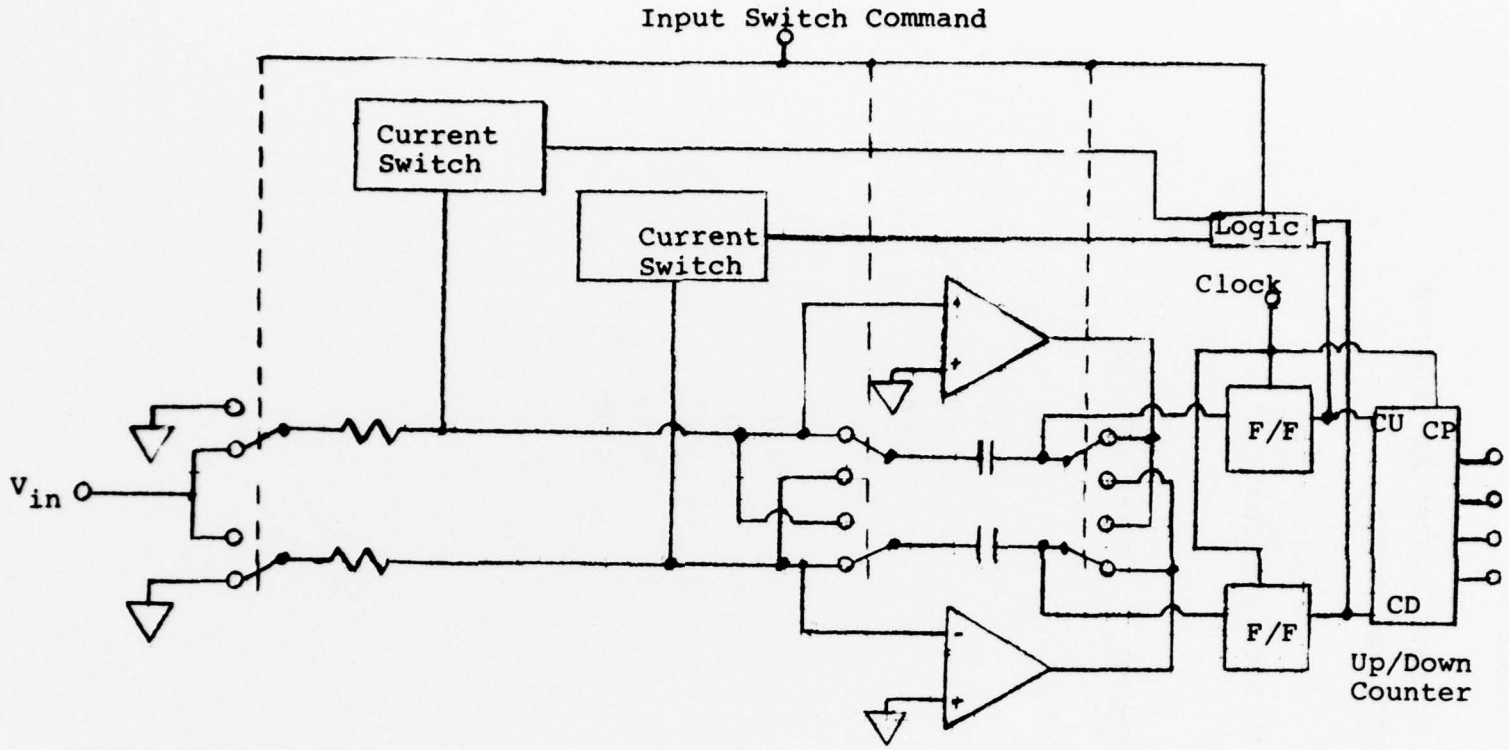


Figure 12: Automatic Offset Nulling Delta Sigma Modulator

TABLE 6

OUTPUT OF OFFSET NULLING SCHEME AS FUNCTION OF APPLIED OFFSET

(5.00V out ideal)

Offset Voltage (V)	Output (V)
0.00	5.00
0.10	5.00
0.20	5.00
0.30	5.00
0.40	5.00
0.50	5.00
1.00	4.99
2.00	5.00
3.00	5.00
4.00	5.00
5.00	5.00

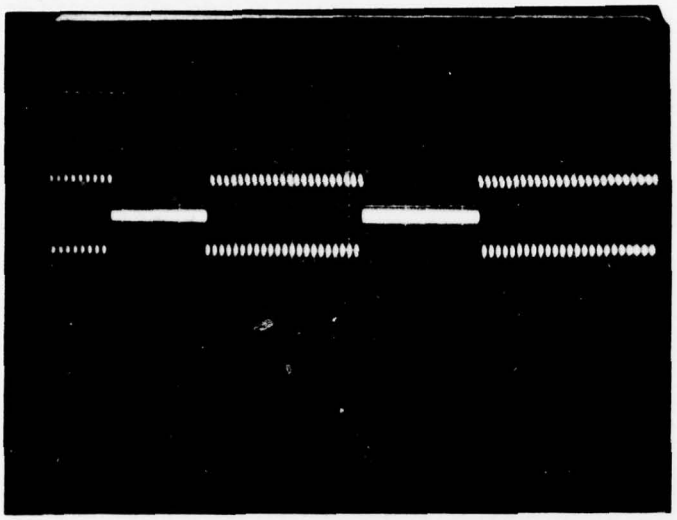
effect of the offset was in the limit cycle associated with the output. Due to the analog remainder in the integrator, the output of a delta sigma modulator will vary between two levels; so with offset nulling the output, which is the difference between two signals, will vary between three levels. Changes in the offset affected the shape of the output, which in turn had a slight effect on the reading from the DAC; Table 6 states that for an offset of one volt the output was 4.99v. Figure 13 shows the limit cycling at one volt offset and at two volts offset. It is not known if the change in the reading was due to a true DC shift or to inaccuracies in the D-A converter caused by the output pattern.

V. 3. Integrated Circuit Configuration

Though the design was not finalized it was concluded that the circuit held enough promise to warrant a study of possible IC layouts. The decision was made to suggest an integrated circuit which could be used as a simple delta sigma modulator while maintaining compatability with the offset nulling scheme. To build automatic offset nulling, the designer would need two of these delta sigma modulator converters and a third IC containing the required choppers.

In Figure 14 is shown the delta sigma modulator chip. It is similar to the configuration in Section IV except that it contains two extra pins, the positive terminal of the integrator is not brought out, and the counter is an up-down counter. The counter will count up when the flip-flop is high and will count down when the Companion Data pin is high. For operation of the chip as a simple A-D converter, the Amp Out pin is connected to the Comparator In pin, and the Input Switch pin and the Companion Data pin are tied low. The integrating capacitor is connected across the amplifier.

Figure 15 shows the chopper configuration. Putting the DPDT switches on a separate chip allow them to be made from large FET's characterized by low on-resistance. Chopper 1 is used to produce two square waves, V_{in} 1 and V_{in} 2, from the input voltage. These waveforms then become the inputs to the two delta sigma modulators for offset nulling. The Amp In pins from the two converters are connected to the inputs of the second chopper, and the two capacitors are con-



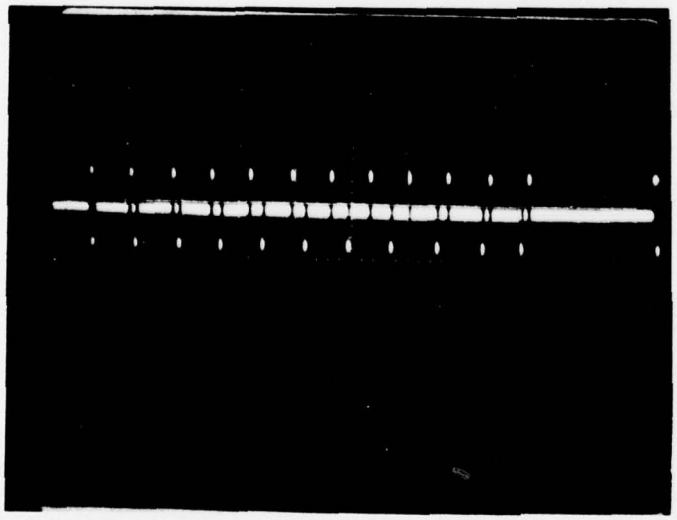
V_{in} = 0V

V_{offset} = 1V

Vert = 1V/cm (AC)

Hor = 10 msec/cm

V_{out} = 4.99 V



V_{in} = 0V

V_{offset} = 2V

Vert = 1V/cm (AC)

Hor = 10 msec/cm

V_{out} = 5.00 V

Figure 13: Comparison of Limit Cycling in the Parallel Outputs with 1 Volt Offset and with 2 Volts Offset (Counting Period Equals 625 μsec.)

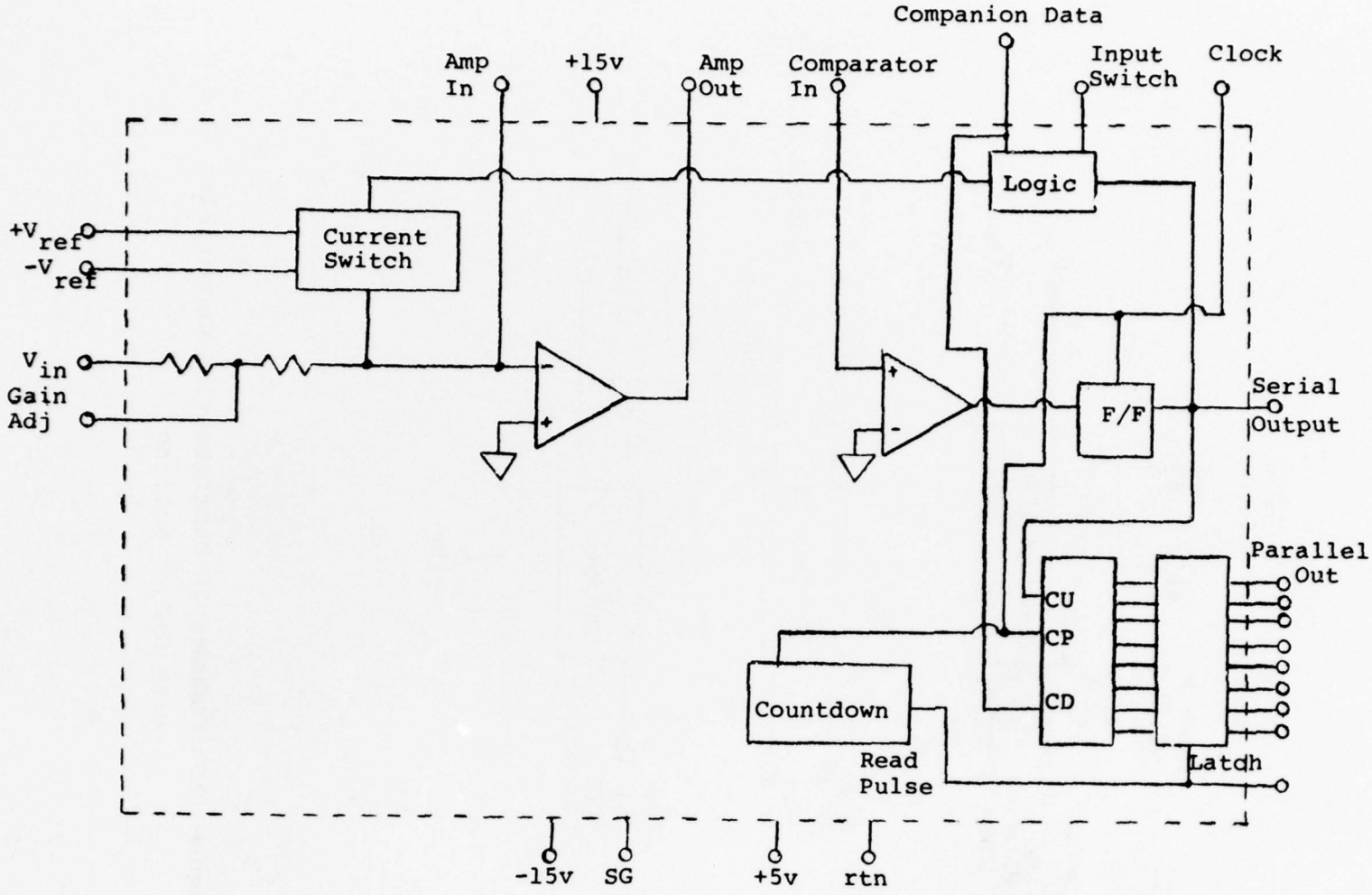


Figure 14: Delta Sigma Modulator IC Configuration Compatible with Offset Nulling

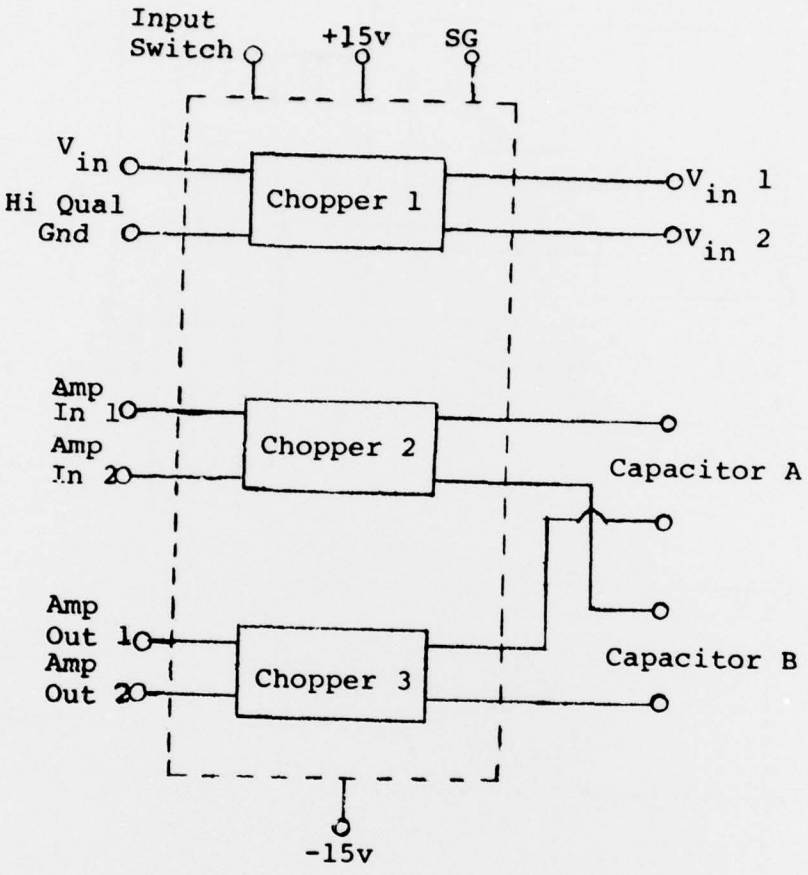


Figure 15: Chopper IC Configuration Compatible with Offset Nulling

nected between the outputs of the second and third choppers. Each output pin of the third chopper is also connected to the Comparator In pin of the delta sigma modulators. The inputs of the third chopper are connected to the Amp Out pins.

When two delta sigma modulators are connected to the chopper and the Serial Output pin from each is tied to the Companion Data pin of the other, the three chips form an offset nulling delta sigma modulator similar to Figure 12. The input switch should be a square wave whose frequency is the strobing rate of the counter, i.e., $f_c/256$.

The output of the flip-flop connected to capacitor A will be proportional to the input voltage; the other flip-flop will give the negative of the input. It should be noted that the output code of the offset nulling scheme is different from the code of the usual delta sigma modulator. This is due to the fact that zero input will cause the up-down counter to stay at its reset value in the offset nulling scheme, but zero input will cause a simple delta sigma modulator to count half way up. If a clock synchronous square wave is tied to the Companion Data pin when the circuit is used as a single chip converter, the resulting output code will be the same as that of the offset nulling scheme.

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