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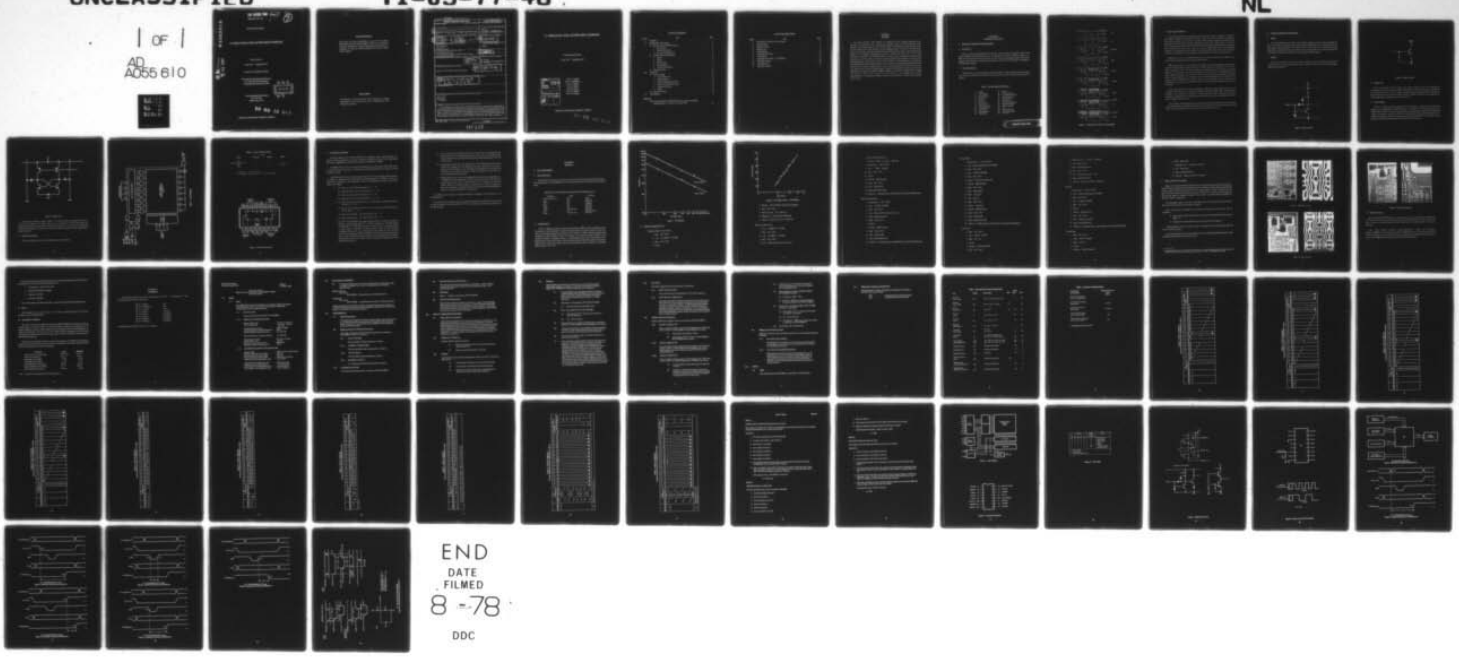

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Fort Monmouth, New Jersey 07703

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The technical and economic impact of electron-beam direct slice printing will be demonstrated on 256-bit bipolar RAMs. All electron-beam tapes necessary for fabricating the 256-bit bipolar RAMs have been generated. Advanced software techniques such as geometry sizing, sorting and increment/decrement were used. E-beam processes have been developed for all lithographic steps on the 256-bit bipolar RAMs. Because of the pattern distortion at epitaxial growth, the original alignment marker system was modified. Several lots using this new alignment marker system are in process. The design of the Automatic Slice Loader is complete.

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IC FABRICATION USING ELECTRON-BEAM TECHNOLOGY

Fourth Quarterly Report

1 June 1977 – 1 September 1977

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SECTION I
PURPOSE

The overall objective of the program is to implement e-beam writing technology for the fabrication of microcircuits. The technical and economic impact of electron beam direct slice printing will be demonstrated on 256-bit bipolar RAMs. The elimination of mask masters, masks, and the masking process will eliminate the most significant source of yield loss. This will permit greater circuit design complexity and flexibility which will lead to lower device costs with increased reliability. The complete implementation program is divided into three tasks. Task A, Yield Improvement Through Direct E-Beam Writing, is directed toward developing the manufacturing technology required for e-beam writing with existing equipment and existing resist processes and demonstrating the yield benefits of this technique. Task B, Cost Reduction for E-beam Writing Through High Speed Resist Implementation, is directed toward implementing identified high speed e-beam resists in order to significantly decrease cycle time and thus reduce the IC bar cost. Task C, Cost Reduction for E-Beam Writing Through Automatic Beam Diameter Control and Automatic Handling, is directed toward utilizing EBMIII's capability of computer-controlled beam size (large and small) on high density circuit ($\leq$0.1 mil) geometries. This program also included implementation of an automated handling system for slices to reduce cycle time and thus further reduce bar cost.

SECTION II
NARRATIVE AND DATA

A. SCHOTTKY BIPOLAR RAM PROCESSING

1. Introduction

There are many possible bipolar processes that could be used in conjunction with e-beam pattern definition to build memory devices. Among those are dielectric isolation, isoplanar, etc. While all of these processes have merit, the process chosen for this program will be the junction isolation double-level metal Schottky process which is used by Texas Instruments in building the 54S/74S series of RAMs.

2. Process Description

The process to be used is outlined in Table I and Figure 1. Some procedures such as clean-ups and etches are omitted from the table but of course are used and are typical of good production practice.

Table I. Schottky Bipolar RAM Process

1)	Substrate	14)	Base drive
2)	Initial Oxidation	15)	Emitter oxide removal
3)	DUF oxide removal	16)	Emitter deposition and drive
4)	DUF deposition	17)	Contact oxide removal
5)	DUF drive	18)	Platinum deposition
6)	Strip oxide	19)	Alloy platinum
7)	Epitaxial layer	20)	Ti-W, Aluminum deposition
8)	Second oxidation	21)	Metal removal (Leads I)
9)	Isolation oxide removal	22)	Dielectric deposition
10)	Isolation deposition	23)	Vias
11)	Isolation drive	24)	Aluminum deposition
12)	Base oxide removal	25)	Metal removal (Leads II)
13)	Base deposition	26)	Sinter metal

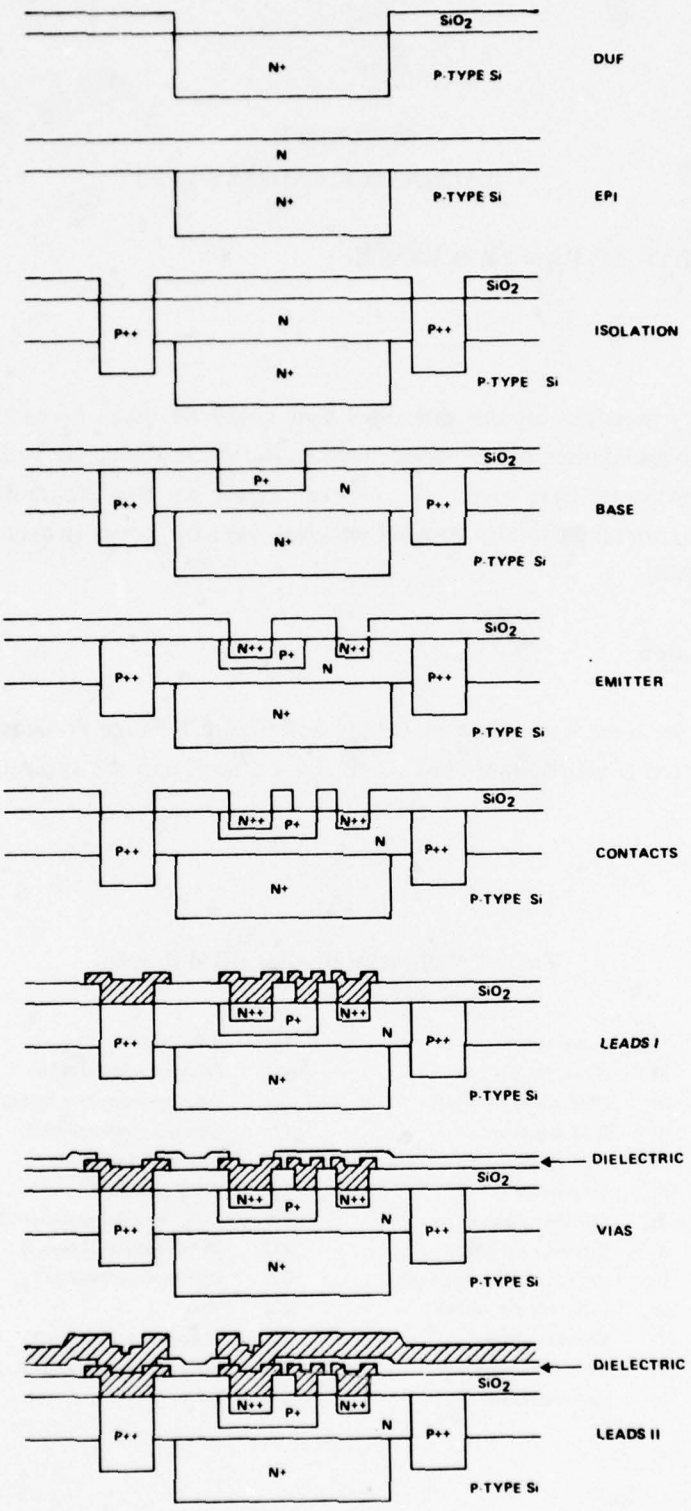

Figure 1. Sectional View of Slice at Various Steps

3. Resist and Etch Selection

Except for metallization, the patterning steps shown above involve etching between 2000 Å and 10,000 Å of SiO_2. Because plasma etch rates of SiO_2 are low and resist lifetimes are limited in the plasma environment, we intend to etch SiO_2 using common buffered HF solutions. Our requirements for electron resists are thus dominated by two factors: 1) high speed ($\geq 2.5\ \mu C/cm^2$) and 2) good adhesion to SiO_2 for wet chemical etching. Among the resists that we have investigated whose sensitivities are greater than $2.5\ \mu C/cm^2$, we have demonstrated good oxide patterning capability with polybutene sulfone (PBS) resist. Further, PBS, being a positive resist, leads to advantages in minimizing area scanned and increasing throughput for most of the pattern levels.

Metallization for the 256-bit RAM will be two levels of metal separated by a dielectric. The first level will be Ti-W/Al and the second level will be pure Al.

PBS cannot be used as a plasma etch mask and there are no other high-speed positive resists available. We will therefore use the negative resist TI309, which has a sensitivity of $\approx 2.5\ \mu C/cm^2$. Some experimental results have been completed which show that Al can be plasma etched using TI309 as a mask; however, we will not attempt to etch the first level of metallization using a plasma. Plasma etching gives very steep steps in the etched material and would make second level metal coverage impossible. Any attempts at plasma etching aluminum will be restricted to the second level of metallization. If difficulty arises in trying to plasma etch the second level of metallization, the wet chemical etchants, which will be used on the first metallization level, can be substituted.

Resist processing will be done on completely automated, cassette loaded spin coaters and developers. This will provide maximum throughput and reproducibility while minimizing slice handling. These machines are installed in a horizontal laminar flow clean room to minimize particulate contamination. Wet chemical processing will be performed in vertical laminar flow clean hoods installed in this same room.

The feasibility of IR baking for electron resist processing will be demonstrated. Cassette loaded ovens with belt drive through three temperature zones and nitrogen air curtains will be used. The wafers will load individually onto the belt and face the IR emitters directly.

B. SCHOTTKY BIPOLAR RAM DESIGN

1. Inputs

The circuit schematic for all of the inputs is shown in Figure 2. This circuitry was designed to give very low high- and low-level input currents and very high performance. The low input currents allow higher fan-out capability in an entire memory system. The use of Schottky diodes and transistors in the inputs increases the performance over non-Schottky devices. The inputs also have clamp diodes to protect the circuitry if the input voltage should go negative.

2. *Output*

The circuit schematic for the output is shown in Figure 3. The open-collector output permits connection of one, or for larger word capacities, a number of outputs to a common bus through a single pull-up termination.

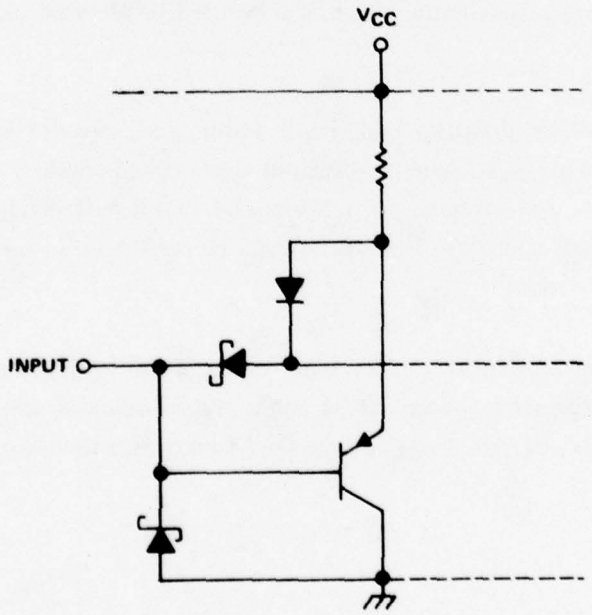

Figure 2. Input Circuitry

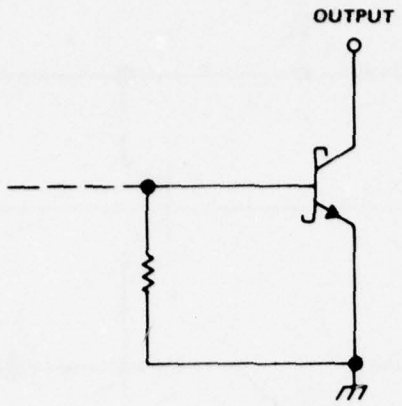

Figure 3. Output Circuitry

3. Memory Cell

The circuit schematic for the memory cell is shown in Figure 4. The cell is basically two cross-coupled inverters and two sense diodes. Information is written into the cell or read from the cell along the sense lines. The cell is enabled or disabled using the word line. When the word line is low, information can be read from or written into the cell. When the word line is in a high state the cell is disabled and no information can be read or written.

4. System Design

The IC is a single monolithic integrated circuit containing a 256-word by 1-bit fully static random access non-destructive readout memory. The memory if fully decoded requires only 8 address lines to select one of 256 storage locations. An additional line, write enable, is provided to enable the memory to modify the stored data. Separate Data Input and Data Output lines are provided for minimum interaction between input and output functions. Three chip enable lines are provided to simplify the decoding required to achieve the desired system.

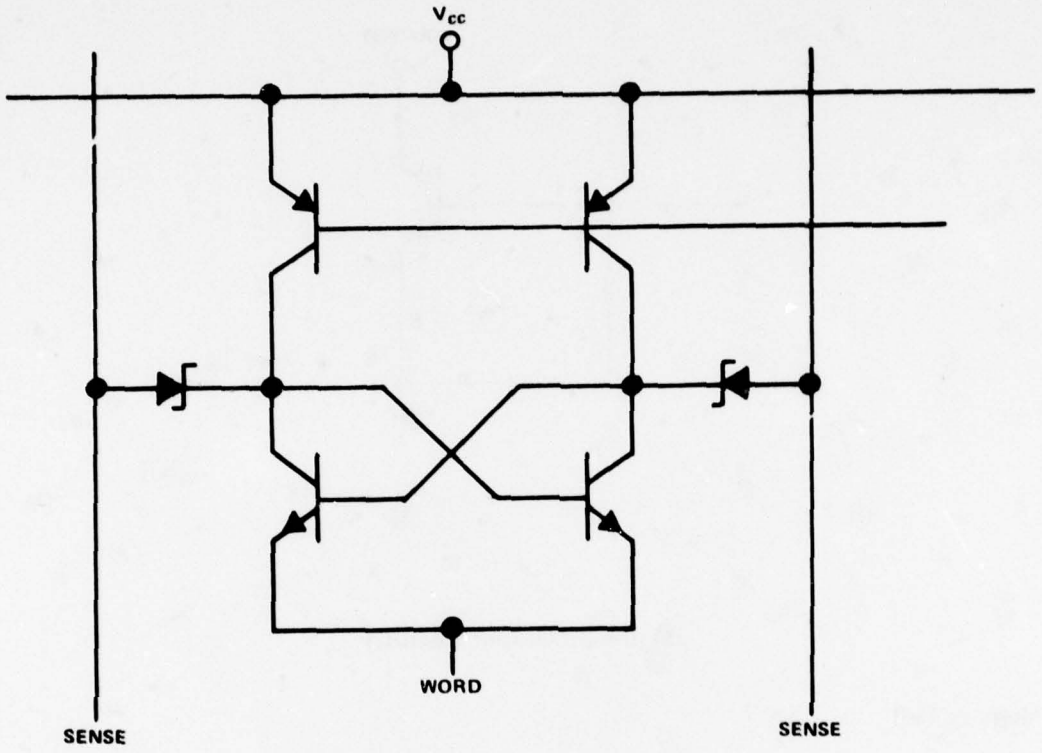

Figure 4. Memory Cell

The basic logic diagram is shown in Figure 5. The memory matrix is organized in an array of 16 rows and 16 columns. The address inputs A, B, C and H go to a 4-to-16 line decoder and determine the memory column selected. The address inputs D, E, F and G go to a 4-to-16 line decoder and determine the memory row selected. The logical operational mode (truth table) is shown in Table II.

5. Terminal Connections

The terminal connections for the 256-bit RAM are shown in Figure 6.

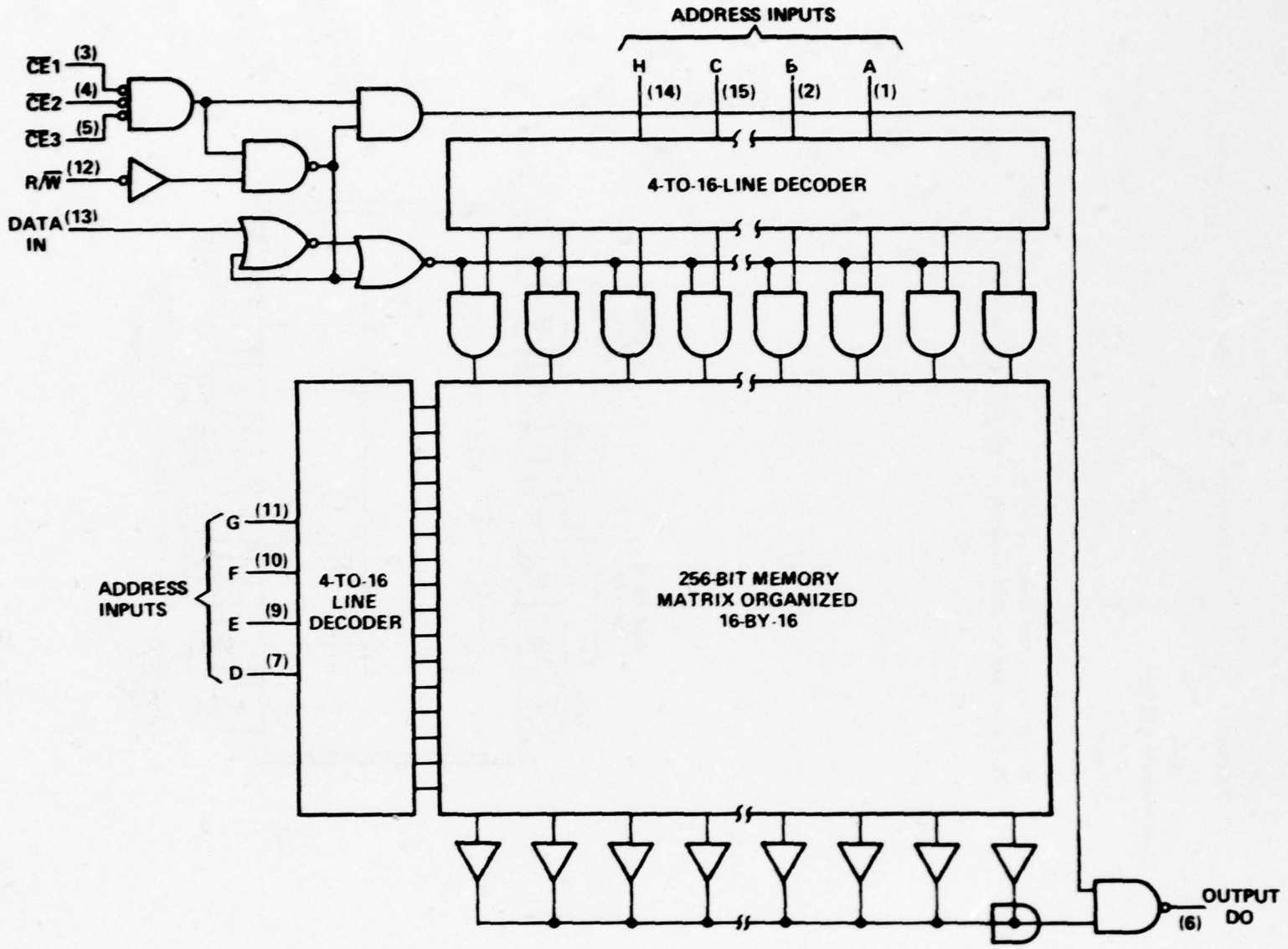

Figure 5. Logic Diagram

Table II. Logical Operational Mode

Function	Inputs: Chip Enable†	Inputs: Read/Write	Output
Write (Store Complement of Data)	L	L	H
Read	L	L	Stored Data
Inhibit	H	X	H

H = high level, L = low level, X = irrelevant

†For chip-enable: L = all $\overline{CE}$ inputs low; H = one or more $\overline{CE}$ inputs High

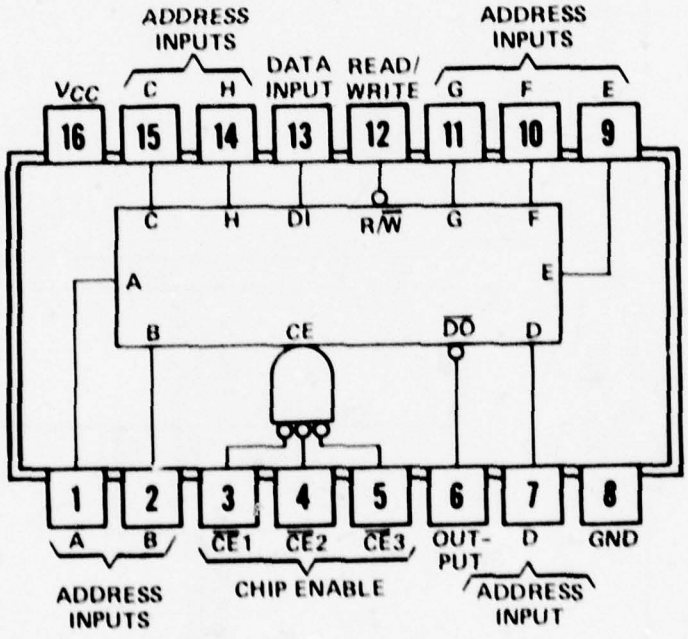

Figure 6. Terminal Connections

C. ELECTRICAL TESTING

Electrical testing for the 256-bit RAM will be accomplished using existing automatic test systems at Texas Instruments. The basic equipment proposed for the test is the High Speed Measurement (HSM) System and the Numerical Exerciser for Memories (NEM).

The HSM will be used to test the memories while they are in slice form. It will perform all the dc tests such as I_{CC}, V_{OL}, I_{OH}, etc. and will also do functional testing on the memory cells and peripheral circuitry.

The NEM will be used to test the memories after they have been packaged. Programming of the NEM is accomplished with a RAM memory supplying instructions for support as well as test instructions to implement exercise algorithms. Some of the algorithms presently in the software library are as follows:

1) (a) Write a zero in each device location (1, 2, 3 . . . N)

   (b) Read and verify a zero in each location (1, 2, 3 . . . N)

   (c) Write a one in each device location (1, 2, 3 . . . N)

   (d) Read and verify a one in each location (1, 2, 3 . . . N)

2) (a) Read a one in first cell, write back a zero, and read a zero. Repeat process for all cells (1, 2, 3 . . . N)

   (b) Read a zero in the first cell, write back a one; and read a one. Repeat process for all cells (1, 2, 3 . . . N)

   (c) Repeat (a) backwards — last cell first. (N, N-1, N-2 . . . 1)

   (d) Repeat (b) backwards — last cell first. (N, N-1, N-2 . . . 1)

3) Access 0-1-0: This algorithm starts with a memory full of zeros and a 1 in location 0. Begin by reading a background of "0", a reference location of "1" and again reading a background of "0". Repeating this process, thus, verifies the access time (address to data output) "both ways" between location 0 and all other locations, 1 through N; then writes a one into location 1 and verifies its access time with respect to all remaining locations 2 through N; then reiterates this process until a one is written into the final location N, whose accesss times with respect to all other locations have already been verified. Notice that data out complements for both directions of read access.

4) Access 1-0-1: This test initializes the device to all ones, then tests individual access times by using the same general procedures as in test 3 above except that all data zero/one references are reversed. This time the data output transitions for each read cycle are 1-0-1.

5) Random data pattern: This test will generate a 10 bit MLS pseudo random data sequence for writing into and reading from the device under test. The sequence repeats after 1023 memory cycles. This pattern will be displayed by one bit prior to each write all, read all such that after n loops, the random pattern will have been rotated completely through memory.

6) Walking Disturb: This is the most thorough single test of all present algorithms. It is a combination of the "walking ones and zeros", access time verify to and from every location and, address to write enable set-up check to and from every memory address. With the exception of memory enable/exercise, it will do an equal to or better than evaluation of any failure mode exercised by all the preceding algorithms. However, it does have a limitation; execution time.

The NEM system is designed such that generating new algorithms is almost limited to one's own imagination.

All of the final functional dc and ac testing will be performed on the NEM. The memories will be tested according to specification SCS-517 (2/12/76) and will meet all electrical requirements of that specification.

SECTION III
RESULTS

A. SLICE PROCESSING

1. General Discussion

Table III lists the process step, resist and etch process for each level in the fabrication process. The actual specifics of each lithographic step, such as spin speeds, bake temperatures, etc., are listed below.

Table III. Process Step, Resist, and Etch Process for Fabrication Level

Process Step	Resist	Etch Process
Alignment Markers I and II	PMMA	Plasma
DUF	PBS	Buffered HF
Isolation	PBS	Buffered HF
Base	PBS	Buffered HF
Emitter	PBS	Buffered HF
Contact	PBS	Buffered HF
Leads I	TI resist No. 309	Metex Etch
Vias	PBS	Ethylene Glycol/HF
Leads II	TI resist No. 309	Metex Etch

2. E-Beam Resists

TI-309 is a high-speed negative e-beam resist developed in SREL at Texas Instruments and is the material of choice for plasma etching of Si, Si_3N_4, poly Si, W, Ti, Mo, Ta and Al. It is also very effective for masking alkaline aqueous etches for Al. TI-309 is a rubbery material and makes good coatings from xylene solutions. Curves for thickness vs spin speed are shown in Figure 7. The unexposed material is thermally sensitive to crosslinking and must not be heated above 80°C. Resolution and contrast of TI-309 are very good when compared with other negative e-beam resists. Figure 8 shows a plot of line width vs dose for TI-309 where the exposure required for a nominally 200 μinch line is 2.6 $\mu C/cm^2$.

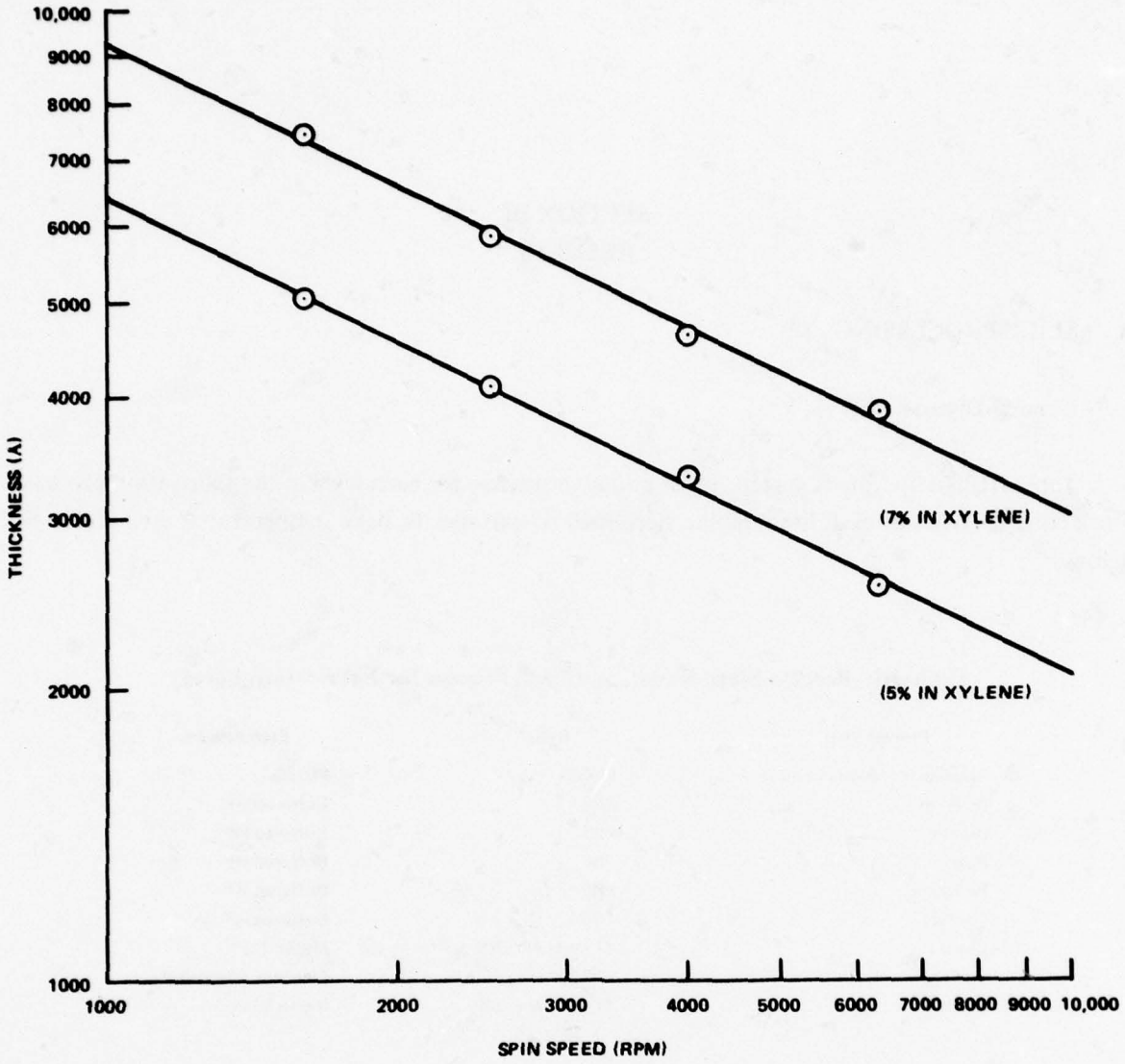

Figure 7. TI-309 Resist

3. E-Beam Lithographic Process

Alignment Markers I and II Steps

1. Bake – IR @ 160°C
2. Coat – 8% PMMA @ 1.5K RPM
3. Bake – IR @ 160°C
4. Expose

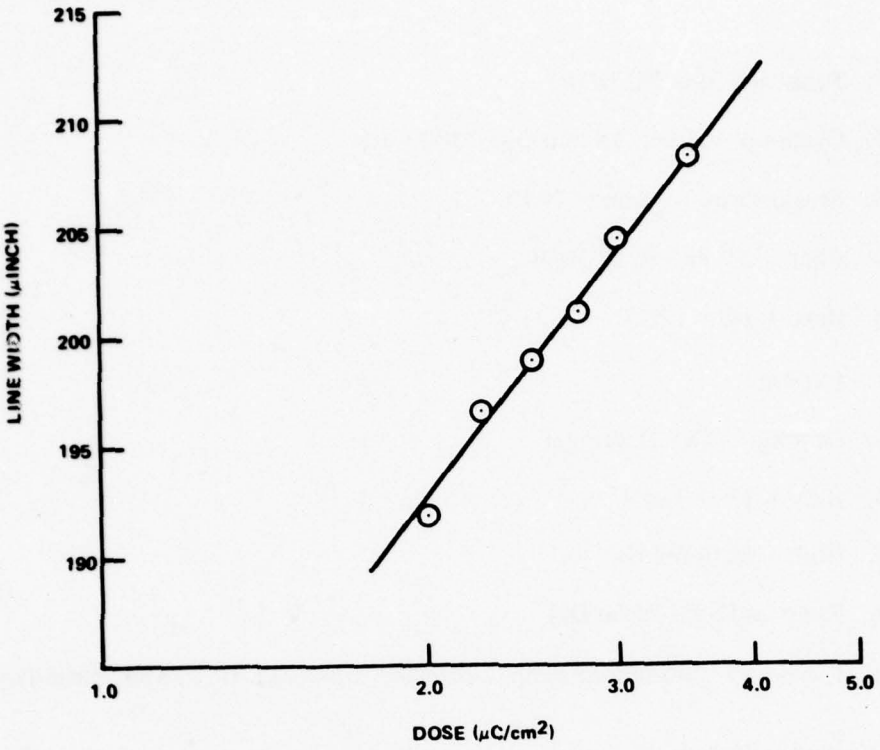

Figure 8. Line Width vs Dose – TI-309 Resist

5. Develop – 65/35 4-methyl-2-pentanone/2-propanol
6. Bake – IR @ 160°C
7. Plasma De-scum – O_2 @ 100 watts
8. Plasma etch – CF_4/O_2 (4%) @ 100 watts
9. Clean-up – Plasma, 10 min O_2 @ 300 watts

DUF and Isolation Steps

1. Coat – 8% PMMA @ 1.5K RPM
2. Bake – IR @ 160°C
3. Coat – 8% PMMA @ 1.5K RPM
4. Bake – IR @ 160°C
5. Etch – Buffered HF until back side clears

6. Rinse and Spin Rinse/Dry
7. Clean-up – Asher, 15 min O_2 @ 300 watts
8. Steam slices – 5 min @ 700°C
9. Coat 5% PBS @ 2K RPM
10. Bake – IR @ 120°C
11. Expose
12. Develop – PBS Developer
13. Bake – IR @ 120°C
14. Etch – Buffered HF
15. Rinse and Spin Rinse/Dry
16. Clean-up – 2-butanone Strip, 2-propanol rinse, D.I. H_2O, Spin Rinse/Dry

Base and Emitter Steps

1. Steam Slices – 5 min @ 700°C
2. Coat – 5% PBS @ 2K RPM
3. Bake – IR @ 120°C
4. Etch – Buffered HF until back side clears
5. Rinse and Spin Rinse/Dry
6. Bake – IR @ 120°C
7. Expose
8. Develop – PBS Developer
9. Bake – IR @ 120°C
10. Etch – Buffered HF
11. Rinse and Spin Rinse/Dry
12. Clean-up – 2-butanone Strip, 2-propanol Rinse, D.I. H_2O, Spin Rinse/Dry

Contact Steps

1. N_2 bake slices – 15 min @ 900°C
2. Coat – phenyl trichlorosilane @ 5K RPM
3. Bake – IR @ 160°C
4. Coat – 5% PBS @ 2K RPM
5. Bake – IR @ 120°C
6. Expose – P-Contacts and Schottky
7. Develop – PBS Developer
8. Bake – IR @ 120°C
9. Etch – Buffered HF
10. Rinse – D.I. H_2O
11. Dry – N_2 Box
12. Bake – IR @ 120°C
13. Expose – N-Contacts
14. Develop – PBS Developer
15. Bake – IR @ 120°C
16. Etch – Buffered HF
17. Rinse and Spin Rinse/Dry
18. Clean-up – 2-Butanone Strip, 2-propanol rinse, D.I. H_2O, Spin Rinse/Dry

Leads I Step

1. Bake – IR @ 160°C
2. Coat – TI309 @ 3K RPM
3. Bake – 50°C Air
4. Expose
5. Develop – Xylene/2-propanol
6. Bake – IR @ 160°C

7. Plasma De-scum – 2 min O_2 @ 100 watts
8. Etch – Metex Etch
9. Rinse and Spin Rinse/Dry
10. Bake – IR @ 120°C
11. Etch – Hydrogen Peroxide @ 30°C
12. Rinse and Spin Rinse/Dry
13. Clean-up – Plasma, 10 min O_2 @ 300 watts

Vias Step

1. N_2 bake slices – 30 min @ 450°C
2. Coat – phenyl trichlorosilane @ 5K RPM
3. Bake – IR @ 160°C
4. Coat – 5% PBS @ 2K RPM
5. Bake – IR @ 120°C
6. Expose
7. Develop – PBS Developer
8. Bake – IR @ 120°C
9. Etch – Ethylene Glycol/HF
10. Rinse and Spin Rinse/Dry
11. Clean-up – 2-butanone Strip, 2-propanol Rinse, D.I. H_2O, Spin Rinse/Dry

Leads II Step

1. Bake – IR @ 160°C
2. Coat – TI309 @ 3K RPM
3. Bake – 50°C Air
4. Expose
5. Develop – Xylene/2-propanol

6. Bake – IR @ 160°C
7. Plasma De-scum – 2 min O_2 @ 100 watts
8. Etch – Metex Etch
9. Rinse and Spin Rinse/Dry
10. Clean-up – Plasma, 10 min O_2 @ 00 watts

4. Chips at Various Process Steps

Figure 7 shows a chip after the lead pattern has been etched in the first level metal (Leads I), Figure 10 shows a chip after vias have been etched in the interlevel oxide to permit the second level metal to make electrical contact with the first level metal. Figure 11 shows a chip after the lead pattern has been etched in the second level metal (Leads II). Cross sections of a typical device at these process steps are depicted in Figure 1. There Leads I, vias, and Leads II correspond to Figures 9, 10 and 11 respectively.

The photographs shown in the above listed figures show the essential levels and fabrication steps of the two-level metal system this device employs.

There are basically two problem areas associated with this process.[1] They are in order of importance:

1) Step coverage of the second level metal over the oxide insulated first level metal, see Figure 11.

2) Pinholes in the oxide insulator over the first level metal, see Figure 10.

The first problem can be overcome by using an etching process on the first level leads that tapers or slopes their edges.

The second problem can be reduced through the use of an RF plasma deposited oxide for the insulating oxide between the two levels of metal.

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1. A.M. Wilson and P.B. Ghate, "A Two Level Metal System Designed For Large Scale Integrated Circuits", Proceedings of the Third International Symposium on Silicon Materials Science and Technology, 9-13 May 1977, Philadelphia, Pennsylvania.

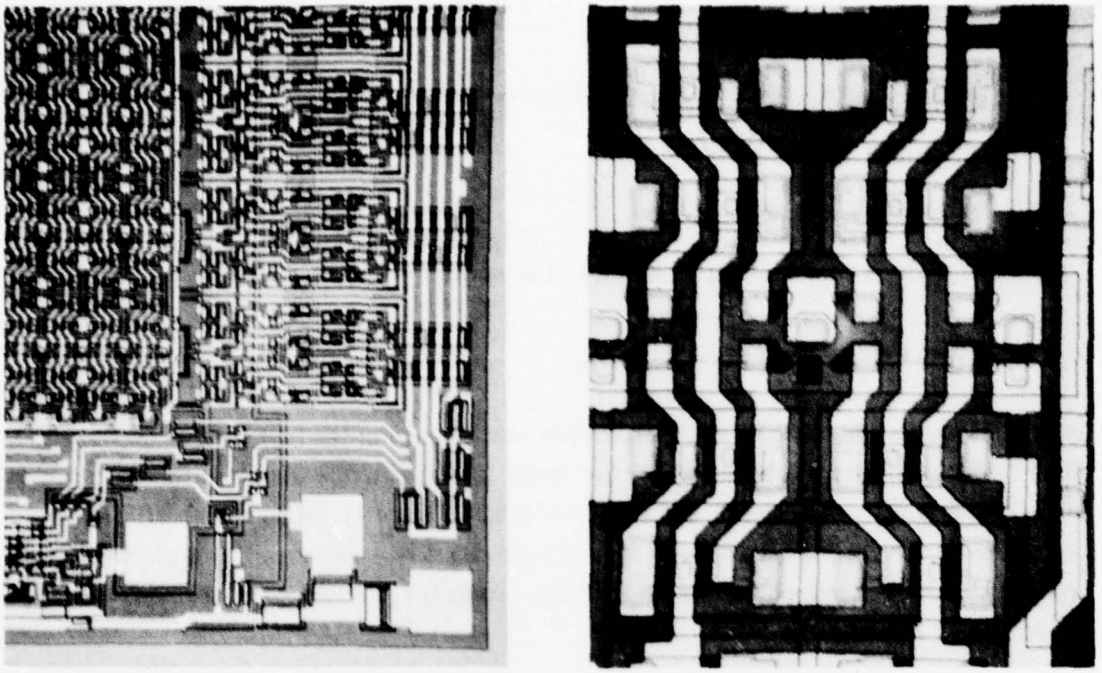


Figure 9. Chip After Leads I

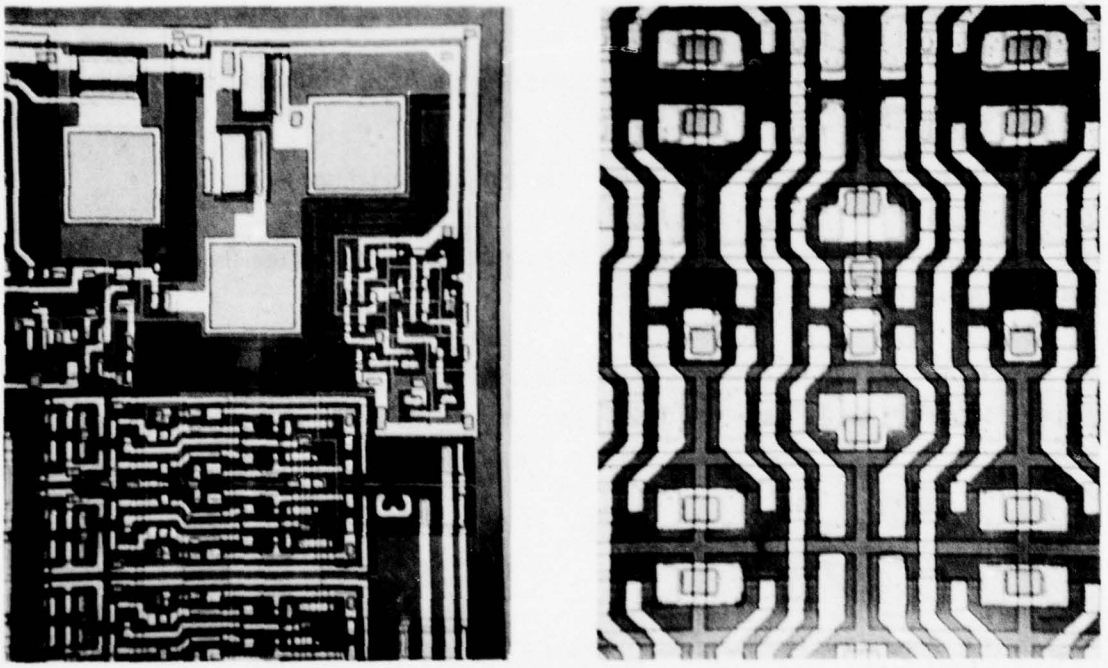


Figure 10. Chip After Vias

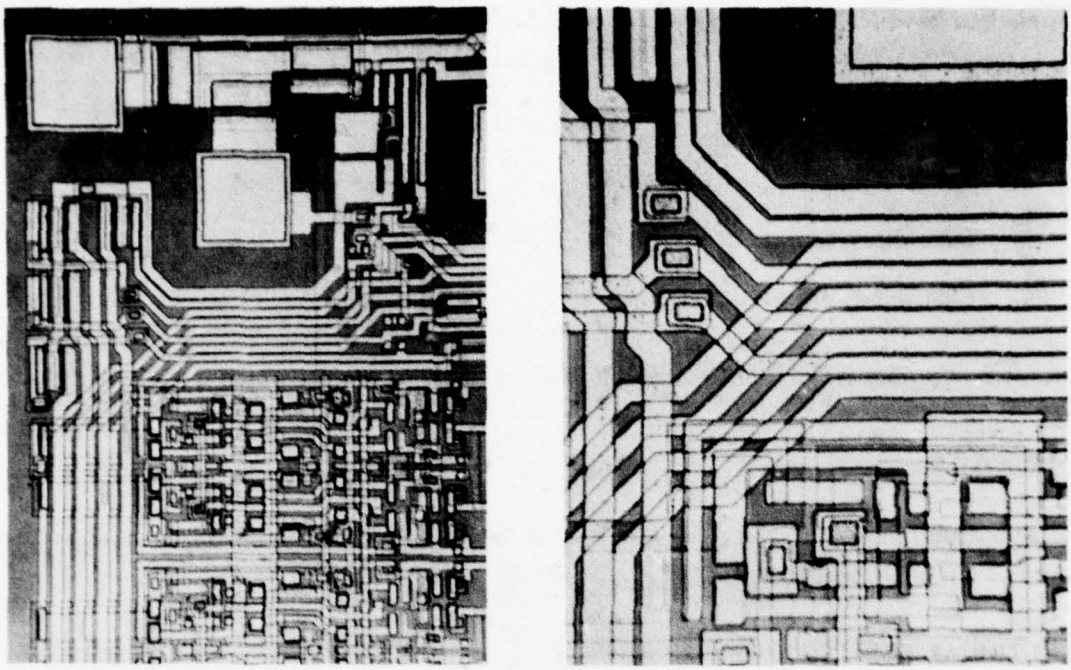


Figure 11. Chip After Leads II

5. Adhesion Promoters

We have experienced difficulties at the contact and vias steps due to inadequate resist adhesion to the slice surface. At contact O.R. the resist is spun on a phosphorus "glass" oxide and at vias the resist is spun on a plasma oxide. Both of these oxides etch very rapidly and have a tendency to undercut.

Two silane adhesion promoters, phenyltrichlorosilane (PTCS) and hexamethyldisilazane (HMDS), have been tried to increase the PBS adhesion to the previously mentioned oxides. The success of these methods has been mixed; however, generally PTCS has given better adhesion than HMDS. On all slices processed to date, PTCS has been used.

The method in which these adhesion promoters are used is by spinning them on the slices prior to applying the e-beam resist. The actual process steps are:

1. N_2 bake slices – 450°C-950°C in N_2
2. Spin PTCS or HMDS @ 5K RPM
3. Bake slices, IR 120°C
4. Coat slices with PBS

This method produces the thinnest possible coating of the promoter which is still effective.

6. Status

The remainder of Lot 1 and also Lot 3 is at Leads 1 metal removal. Lot 5 is at second oxidation. Lot 6 is at DUF diffusion.

B. ELECTRICAL TESTING

Part of Lot 1 has been through slice testing on the HSM. The HSM does continuity, functional and DC testing on the device in slice form. None of the devices appeared to be good because of an apparent high V_{OL} (low-level output voltage). This was thought at the time of measurement to be caused by the resistor in the base circuit of the output transistor limiting the base current and perhaps that the output transistor had a low h_{FE}, with a net effect of causing a low output current and consequent high V_{OL}.

However, the real problem was due to the contact resistance of the HSM test probe with the output terminal of the device on the slice. This was subsequently proven when units which failed this test at probe passed after they were packaged.

Parameter	Limit	Measured
Low-level output voltage (V_{OL})	0.45 V max	0.65 V*
Input low current (I_{IL})	–510 μA	–40 μA
Input high current (I_{IH_1})	25 μA	0.4 μA
Input high current (I_{IH_2})	1 mA	3 μA
Output leakage current (I_{CEX})	100 μA	0.8 μA
Input clamp diode voltage (V_{IC})	–1.5 V	0.88 V
Power supply current (I_{CC})	145 mA	57 mA

*Note: Over half the units tested didn't change output states during this test.

SECTION IV
MANPOWER

The following professionals worked on this program 1 June 1977 – 1 September 1977. The percentage of time worked is also shown.

Mr. P. L. Whelan	20%
Mr. R. A. Williamson	100%
Dr. G. L. Varnell	10%
Dr. J. L. Bartelt	Consultant
Dr. T. L. Brewer	Consultant
Dr. R. J. Dexter	Consultant
Dr. R. A. Robbins	Consultant
Mr. C. D. Winborn	Consultant

In addition, three technicians worked on the program.

Microcircuit Digital
256 BIT POLAR RANDOM ACCESS MEMORY (RAM)
Monolithic Silicon

1.0 SCOPE

1.1 Scope

This specification covers the requirements for a Schottky clamped monolithic silicon 256 words/1 bit per word random access memory (RAM) with tri-state output and three chip select inputs.

1.1.1 DEVICE CLASS.

Device shall be Class B as defined in MIL-M-38510.

1.1.2 ABSOLUTE MAXIMUM RATINGS.

Supply voltage range	−0.5 V dc to 7.0 V dc
Input voltage range	−1.5 V dc at −10 μA to 5.5 V dc
Storage temperature range	−65°C to 150°C
Lead temperature (soldering 10 seconds)	300°C
Thermal resistance, junction-to-case	J_C = 26° C/W
Thermal resistance, junction-to-ambient	J_A = 85° C/W
Output supply voltage	0.5 V dc to 7.0 V dc
Output sink current	+10 mA
Maximum power dissipation, P_D	853 mW dc
Maximum junction temperature, T_J	175°C

1.1.3 RECOMMENDED OPERATING CONDITIONS.

Supply voltage	5.00 V dc min to 5.5 V dc max
Minimum high level input voltage	2.0 V dc
Maximum low level input voltage	0.8 V dc
Normalized fanout (each output)	40 maximum (10 mA)
Ambient operating temperature range	0°C to 70°C
Address to write enable setup time	10 ns (minimum)
Address to write enable hold time	10 ns (minimum)
Chip enable to write enable setup time	10 ns (minimum)
Chip enable to write enable hold time	10 ns (minimum)

2.0 APPLICABLE DOCUMENTS

2.1 The following documents, of the issue in effect on date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein.

SPECIFICATION
MILITARY
MIL-M-38510 – Microcircuits, General Specification for

STANDARD
MILITARY
MIL-STD-883 – Test Methods and Procedures for Microelectronics

(Copies of specifications, standards, drawings, and publications required by suppliers in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

3.0 REQUIREMENTS

3.1 General Requirements

The RAM shall be a Schottky clamped monolithic silicon device which shall be in accordance with Class B requirements of MIL-M-38510 and as specified herein. In the event of conflict between MIL-M-38510 and this specification, this specification shall govern.

3.2 Design, Construction and Physical Dimensions

The design, construction and physical dimensions shall be as specified in MIL-M-38510, outline D-2, and herein.

3.2.1 LOGIC DIAGRAM

The logic diagram shall be as specified on Figure 1.

3.2.2 TERMINAL CONNECTIONS

Terminal connections shall be as specified on Figure 2.

3.2.3 TRUTH TABLES

The truth tables shall be as specified on Figure 3.

3.2.4 SCHEMATIC CIRCUIT

The schematic circuit shall be as specified on Figure 4.

3.3 Lead Material and Finish

Lead material and finish shall be in accordance with MIL-M-38510.

3.4 Electrical Performance Characteristics

The electrical performance characteristics are specified in Table I and apply over the full recommended ambient operating temperature range, unless otherwise specified.

3.5 Rebonding

Rebonding shall be in accordance with MIL-M-38510.

3.6 Electrical Test Requirements

Electrical test requirements shall be as specified in Table II for the applicable device type and device class. The subgroups of Table III which constitute the minimum electrical test requirements for screening, qualification, and quality conformance by device class are specified in Table II (subgroup 7 and 8 testing requires only a summary of attributes data).

4.0 QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for Inspection

Unless otherwise specified in the contract, the contractor is responsible for the performance of all inspection requirements as specified herein. Except as otherwise specified in the contract, the contractor may use his own or any other facilities suitable for the performance of the inspection requirements specified herein, unless disapproved by the Government. The Government reserves the right to perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure supplies and services conform to prescribed requirements.

4.2 Classification of Inspection

Inspection shall be classified as follows:

(1) First article inspection (does not include preparation for delivery). (See 4.5).

(2) Quality conformance inspection. (See 4.6).

4.3 Test Plan

The contractor prepared Government-approved test plan, as cited in the contract, shall contain:

(1) Time schedule and sequence of examinations and tests.

(2) A description of the method of test and procedures.

(3) Identification and brief description of each inspection instrument and date of most recent calibration.

4.4 Screening

Screening shall be conducted on all devices prior to first article and quality conformance inspection and shall be in accordance with Class B of Method 5004 of MIL-STD-883. The following additional criteria shall apply:

(1) Test samples for the group B bond strength test specified in Method 5005 of MIL-STD-883 may, at the manufacturer's option, be randomly selected immediately following the internal visual (precap) inspection and prior to sealing (See 4.6.2).

(2) Temperature cycling (Method 1010 of MIL-STD-883).

(a) Omit seal test as post-test measurement.

(3) Burn-in test (Method 1015 of MIL-STD-883).

(a) Test condition D or E, using the circuit shown on Figure 5, equivalent.

(b) T_A = 70°C, minimum.

(4) Reverse bias burn-in and interim electrical test in accordance with 3.1.11 of Method 5004 of MIL-STD-883 may be omitted.

(5) Interim and final electrical test parameters shall be as specified in Table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

(6) External visual inspection shall not include measurement of case and lead dimensions.

(7) Percent defective allowable (PDA). The PDA is specified as 10 percent for Class B devices based on failures from group A, subgroup 1 test after cooldown as final electrical test in accordance with Method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.

4.5 First Article

First article inspection shall be performed by the contractor.

4.5.1 FIRST ARTICLE UNITS

The contractor shall furnish 50 devices for first article inspection.

4.5.2 FIRST ARTICLE INSPECTION

First article inspections shall be those specified herein for groups A, B, and C (See 4.6.1, 4.6.2 and 4.6.3) except that the LTPD values shall not apply for first article inspection. All 50 devices shall be subjected to Group A inspections, no failures allowed. All 50 devices shall be subjected to group B, subgroup 1 and samples of 7, 5, and 5 shall be subjected to subgroups 2, 3, and 4 respectively with no failures allowed. The remaining 33 shall be equally divided and subjected to the group C tests, no failures allowed.

4.6 Quality Conformance Inspection

Quality conformance inspection shall be in accordance with MIL-M-38510.

4.6.1 GROUP A INSPECTION

Group A inspection shall consist of the test subgroups and LTPD values shown in Table I of Method 5005 of MIL-STD-883 and as follows:

(1) Tests shall be as specified in Table 1.

(2) Subgroups 4, 5 and 6 of Table I of Method 5005 of MIL-STD-883 shall be omitted.

4.6.2 GROUP B INSPECTION

Group B inspection shall consist of the test subgroups and LTPD values shown in Table II of Method 5005 of MIL-STD-883 and as follows: Bond strength test may be conducted on samples collected prior to sealing (See 4.4(1)).

4.6.3 GROUP C INSPECTION

Group C inspection shall consist of the test subgroups and LTPD values shown in Table III of Method 5005 of MIL-STD-883 and as follows:

(1) End-point electrical parameters shall be as specified in Table II.

(2) Subgroups 7 and 8 shall be added to the Group C inspection requirements for Class B devices and shall consist of the tests, conditions, and limits specified for subgroups 10 and 11 of Group A.

(3) Lead bend in only one direction is required for initial conditioning prior to moisture resistance and salt atmosphere tests.

(4) High-temperature storage test (Method 1008 of MIL-STD-883) conditions:

(a) Temperature: 150° ± 10°C.

(b) Duration: 1,000 hours, except as otherwise permitted by Appendix B to MIL-M-38510.

(5) Operating life-test (Method 1005 of MIL-STD-883) conditions, or equivalent:

(a) Test condition D or E, using the circuit shown on Figure 5, or equivalent.

(b) T_A = 70°C, minimum

(c) Test duration: 1,000 hours, except as permitted by Appendix B of MIL-M-38510.

(6) Omit steady-state reverse bias test.

4.7 Methods of Examination and Test

Methods of examination and test shall be as specified in the appropriate tables and as follows:

4.7.1 VOLTAGE AND CURRENT

All voltages given are referenced in the microcircuit ground terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.7.2 LIFE-TEST COOLDOWN PROCEDURE

When devices are measured at 25°C following application of the operating life or burn-in test condition, they shall be cooled to room temperature prior to removal of the bias. Alternately, the bias may be removed during cooling if the case temperature is reduced to room temperature within 30 minutes after removal of the test condition.

6.0 NOTES

6.1 Notes

The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Abbreviations, Symbols, and Definitions

The abbreviations, symbols, and definitions used herein are defined in MIL-STD-1313, and as follows:

GND	Electrical ground (common terminal)
V_{UB}	Voltage level at an input terminal.

Table I. Electrical Performance Characteristics

TEST	SYMBOL	CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNIT
Low Level Output Voltage	V_{OL}	V_{CC} = 5 V, I_{OL} = 20 mA, D_{in} = 4.5 V		.5	volt
High Level Output Voltage	V_{OH}	V_{CC} = 5 V, D_{out} = – 10.3 mA	2.5		volt
Short Ckt Output Current	I_{OS}	V_{CC} = 5.25 V	–32	–95	mA
Input Low Current	I_{IL}	V_{CC} = 5.5 V, V_{in} = 0.5 V		–510	μA
Input High Current	I_{IH_1}	V_{CC} = 5.5 V, V_{in} = 2.4 V		25	μA
Input High Diode Voltage	I_{IH_2}	V_{CC} = 5.5 V, V_{in} = 5.5 V		1	mA
Input Clamp Diode Voltage	V_{IC}	T_A = 25°C I_{in} = –18 mA		–1.5	volt
Power Supply Current	I_{CC}	V_{CC} = 5.25 V, all inputs at 4.5 V CE1, CE2, CE3 = GND outputs open		145	mA
Output Leakage	I_{OZL}	V_{CC} = 5.25 V, V_O = 0.4 V, D_{in} = 4.5 V		±30	μA
High Impedance State	I_{OZH}	V_{CC} = 5.25 V, V_O = 2.4 V, D_{in} = 4.5 V		±30	μA
Address Access Time	t_{AA}	See Note 1 and Figure 6(b)		100	ns
Enable Access Time	t_{EA}	See Note 2 and Figure 6(c)		45	ns
Enable Recovery Time	t_{ER}	Figure 6(d)		35	ns
Minimum Write Pulse Width	t_{WP}	See Note 3 and Figure 6(e)	120		ns
Propagation Delay Low to High (From R/W)	t_{PLH}	See Note 3 and Figure 6(f)		110	ns
Propagation Delay High to Low (From R/W)	t_{PHL}	See Note 3 and Figure 6(g)		55	ns

Table II. Electrical Test Requirements

MIL-STD-883 Test requirements	Subgroups (See Table III) Class B devices
Interim electrical parameters (Pre burn-in) (Method 5004)	1
Final electrical test parameters (Method 5004)	1*,2,3,7,9
Group A test requirements (Method 5005)	1,2,3,7,8,9
Group C end-point electrical parameters (Method 5005)	1,2,3
Additional electrical subgroups for group C periodic inspections	10,11

*PDA applies to subgroup 1 [Sec. 4.4(7)].

Table III. Group A Inspection
Terminal Conditions (pins not designated are open)

SUBGROUP	SYMBOL	MIL STD-883 METHOD	TEST NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	TEST LIMITS			UNIT
				A_1	A_0	E_1	E_2	E_3	D_{out}	A_4	GND	A_5	A_6	A_7	WE	D_{in}	A_3	A_2	V_{CC}	MEAS. TERM.	MIN	MAX	
1				mA	mA	mA	mA	mA		mA		mA	mA	mA	mA	mA	mA	mA					
$T_A = 25°C$	V_{IC}		1	−18							GND									1		−1.5	V
			2		−18															2			
			3			−18														3			
			4				−18													4			
			5					−18												5			
			6							−18										7			
			7									−18								9			
			8										−18							10			
			9											−18						11			
			10												−18					12			
			11													−18				13			
			12														−18			14			
			13															−18		15			

Table III. Group A Inspection
Terminal Conditions (pins not designated are open)

SUBGROUP	SYMBOL	MIL STD-883 METHOD	TEST NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	TEST LIMITS			UNIT
				A_1	A_0	E_1	E_2	E_3	D_{out}	A_4	GND	A_5	A_6	A_7	WE	D_{in}	A_3	A_2	V_{CC}	MEAS. TERM.	MIN	MAX	
1				V	V	V	V	V		V		V	V	V		V	V	V	V				
$T_A = 25°C$	I_{IL}	3009	14	0.5							GND								5.5	1		–510	μA
			15		0.5						↓								↓	2		↓	↓
			16			0.5														3			
			17				0.5													4			
			18					0.5												5			
			19							0.5										7			
			20									0.5								9			
			21										0.5							10			
			22											0.5						11			
			23												0.5					12			
			24													0.5				13			
			25														0.5			14			
			26								↓							0.5	↓	15		↓	↓

Table III. Group A Inspection
Terminal Conditions (pins not designated are open)

SUBGROUP	SYMBOL	MIL STD-883 METHOD	TEST NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	TEST LIMITS			UNIT
				A_1	A_0	E_1	E_2	E_3	D_{out}	A_4	GND	A_5	A_6	A_7	WE	D_{in}	A_3	A_2	V_{CC}	MEAS. TERM.	MIN	MAX	
				V	V	V	V	V		V		V	V	V	V	V	V	V	V				
1																							
$T_A = 25°C$	I_{IH_1}	3010	27	2.4							GND								5.5	1		25	μA
			28		2.4															2			
			29			2.4														3			
			30				2.4													4			
			31					2.4												5			
			32							2.4										7			
			33									2.4								9			
			34										2.4							10			
			35											2.4						11			
			36												2.4					12			
			37													2.4				13			
			38														2.4			14			
			39															2.4		15			

Table III. Group A Inspection
Terminal Conditions (pins not designated are open)

SUBGROUP	SYMBOL	MIL STD-883 METHOD	TEST NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	TEST LIMITS			UNIT
				A_1	A_0	E_1	E_2	E_3	D_{out}	A_4	GND	A_5	A_6	A_7	WE	D_{in}	A_3	A_2	V_{CC}	MEAS. TERM.	MIN	MAX	
1				V	V	V	V	V		V		V	V	V	V	V	V	V	V				
$T_A = 25°C$	I_{IH_2}	3010	40	5.5							GND								5.5	1		1	mA
			41		5.5															2			
			42			5.5														3			
			43				5.5													4			
			44					5.5												5			
			45							5.5										7			
			46									5.5								9			
			47										5.5							10			
			48											5.5						11			
			49												5.5					12			
			50													5.5				13			
			51														5.5			14			
			52															5.5		15			

Table III. Group A Inspection
Terminal Conditions (pins not designated are open)

SUBGROUP	SYMBOL	MIL STD-883 METHOD	TEST NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	TEST LIMITS			UNIT
				A_1	A_0	E_1	E_2	E_3	D_{out}	A_4	GND	A_5	A_6	A_7	WE	D_{in}	A_3	A_2	V_{CC}	MEAS. TERM.	MIN	MAX	
									V										V				
1 $T_A = 25°C$	I_{OS}		53	GND	GND	GND	GND	GND	0.0	GND	GND	GND		GND	CP	GND	GND	GND	5.25	6	−32	−95	mA

Table III. Group A Inspection
Terminal Conditions (pins not designated are open)

SUBGROUP	SYMBOL	MIL STD-883 METHOD	TEST NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	TEST LIMITS			UNIT
				A_1	A_0	E_1	E_2	E_3	D_{out}	A_4	GND	A_5	A_6	A_7	WE	D_{in}	A_3	A_2	V_{CC}	MEAS. TERM.	MIN	MAX	
1									V							V			V				
$T_A = 25°C$	I_{OZL}		54	GND	GND	GND	GND	GND	0.4	GND	GND	GND	GND	GND	GND	4.5	GND	GND	5.25	6	−30	+30	µA
	I_{OZH}		55	GND	GND	GND	GND	GND	2.4	GND	GND	GND	GND	GND	GND	4.5	GND	GND	5.25	6	−30	+30	

Table III. Group A Inspection
Terminal Conditions (pins not designated are open)

SUBGROUP	SYMBOL	MIL STD-883 METHOD	TEST NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	TEST LIMITS			UNIT
				A_1	A_0	E_1	E_2	E_3	D_{out}	A_4	GND	A_5	A_6	A_7	WE	D_{in}	A_3	A_2	V_{CC}	MEAS. TERM.	MIN	MAX	
1									mA							V			V				
$T_A = 25^\circ C$	V_{OL}	3006	56	GND	GND	GND	GND	GND	20	GND	GND	GND	GND	GND	CP*	4.5	GND	GND	5	6		.5	V
	V_{OH}	3006	57	GND	GND	GND	GND	GND	−10.3	GND	GND	GND	GND	GND	CP	GND	GND	GND	5	6	2.5		V

*CP = Clock Pulse

Table III. Group A Inspection
Terminal Conditions (pins not designated are open)

SUBGROUP	SYMBOL	MIL STD-883 METHOD	TEST NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	TEST LIMITS			UNIT
				A_1	A_0	E_1	E_2	E_3	D_{out}	A_4	GND	A_5	A_6	A_7	WE	D_{in}	A_3	A_2	V_{CC}	MEAS. TERM.	MIN	MAX	
1				V	V	V		V	V			V	V	V	V	V	V	V	V				
$T_A = 25^\circ C$	I_{CC}	3005	59	4.5	4.5	GND	GND	GND		4.5	GND	4.5	4.5	4.5	4.5	4.5	4.5	4.5	5.25	16		145	mA
2	Same tests, terminal conditions, and limits as for subgroup 1, except $T_A = 70^\circ C$ and V_{IC} tests are omitted.																						
3	Same tests, terminal conditions, and limits as for subgroup 1, except $T_A = 0^\circ C$ and V_{IC} tests are omitted.																						

Table III. Group A Inspection
Terminal Conditions (pins not designated are open)

SUBGROUP	SYMBOL	MIL STD-883 METHOD	TEST NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	TEST LIMITS			UNIT
				A_1	A_0	E_1	E_2	E_3	D_{out}	A_4	GND	A_5	A_6	A_7	WE	D_{in}	A_3	A_2	V_{CC} V	MEAS. TERM.	MIN	MAX	
7 $T_A = 25°C$	T_{AA}	See Fig. 6(b) Note 1	60	A	A	B	B	B	S	A	GND	A	A	A	C	D	A	A	5.25	6		100	ns
	T_{AA}		61																4.75			100	ns
	T_{EA}	See Fig. 6(c) Note 2	62																5.25			45	ns
	T_{EA}		63																4.75			45	ns
	T_{ER}	See Fig. 6(d)	64																5.25			35	ns
	T_{ER}	Note 2	65																4.75			35	ns
	T_{WP}	See Fig. 6(e) Note 2	66																5.25		120		ns
	T_{WP}		67	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	▼	4.75		120		ns
8	REPEAT 7 AT $T_A = 70°C$ AND $T_A = 0°C$																						

Table III. Group A Inspection
Terminal Conditions (pins not designated are open)

SUBGROUP	SYMBOL	MIL STD-883 METHOD	TEST NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	TEST LIMITS			UNIT
				A_1	A_0	E_1	E_2	E_3	D_{out}	A_4	GND	A_5	A_6	A_7	WE	D_{in}	A_3	A_2	V_{CC} V	MEAS. TERM.	MIN	MAX	
9 $T_A = 25°C$	T_{PLH}	3003 see Fig. 6(f) Note 3	68	A	A	B	B	B	S	A	GND	A	A	A	C	D	A	A	5.25			110	ns
	T_{PLH}	3003 see Fig. 6(f) Note 3	69																4.75			110	ns
	T_{PHL}	3003 see Fig. 6(g) Note 3	70																5.25			55	ns
	T_{PHL}	3003 see Fig. 6(g) Note 3	71																4.75			55	ns
10	Repeat Subgroup 9 at $T_A = 70°C$																						
11	Repeat Subgroup 9 at $T_A = 0°C$																						

NOTE 1:

ACCESS TIME ALGORITHM (galloping ones and zeros)

This program will test all bits in the array, the addressing, the interaction between bits, and pattern and sequence dependency for transient performance.

Description:

1. All cells are loaded with zeros (0 through 255).
2. A single one is written in cell number 0.
3. Cell number 1 is read (0).
4. Cell number 0 is read (1).
5. Cell number 2 is read (0).
6. Cell number 0 is read (1).
7. Cell number 3 is read (0).
8. The reading procedure continues back and forth between cell 0 and next higher numbered cell until cell number 255 is reached.
9. Now 1 is written in cell number 1 while rest of the cells are filled with zeros. Same reading procedure as shown in step 8 is followed. Finally, cell number 255 is filled with 1 and the same readout procedure is followed.

   Pass execution time: $2 (N+3N^2/2)$ X cycle time

   $N = 256$ (cells)

NOTE 2:

ADDRESS SELECT ALGORITHM

This test verifies that every cell can actually be addressed.

1. All cells are loaded with zeros
2. Cell zero is read (0)
3. A one is written in cell zero
4. Cell zero is read (1)
5. Cell one is read (0)
6. A one is written in cell one

7. Cell one is read (1)

8. This procedure is continued until cell 255 is written with a one and read.

9. Steps 2 through 8 are repeated except that the Data is reversed.

PASS EXECUTION TIME: (13N) X CYCLE TIME

N = 256

NOTE 3:

Checkerboard (alternate ones and zeros).

This program writes and tests alternate ones and zeros in all the cells.

Description:

1. A zero is written in cell number 0 and read.

2. A one is written in cell number 1 and read.

3. A zero is written in cell number 2 and read.

4. Same procedure (steps 1-3) is continued until cell number 15 is read which has a one (1).

5. A one (1) is written and read in cell number 16. Same procedure of alternate writing and reading of ones and zeros is followed until cell number 31 is reached which has a 0.

6. Now a 0 is written and read in cell number 31 and the same procedure is followed as explained in steps 1 through 5 and the same contents of the previous cell in every 16th cell is repeated, until all the cells are written and read.

7. Same test is reversed now and writing and reading is done from cell number 255 down to cell number 0, with writing a one (1) initially.

Pass execution Time: (4N) X cycle time

N = 256

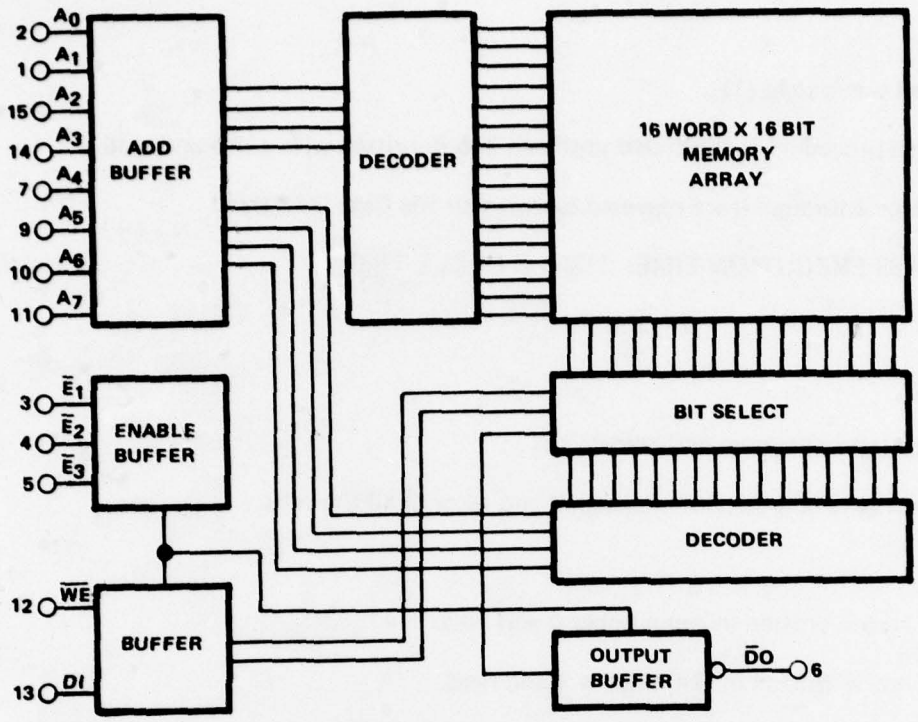


Figure 1. Logic Diagram

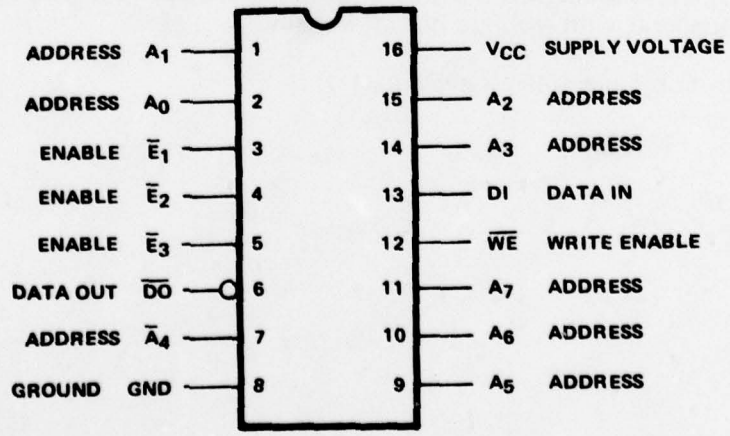


Figure 2. Terminal Connections

INPUTS					OUTPUT	MODE
$\overline{CS_1}$	$\overline{CS_2}$	$\overline{CS_3}$	$\overline{W_E}$	D_{IN}	OPEN COLLECTOR	
H	X	X	X	X	H	NOT SELECTED
X	H	X	X	X	H	NOT SELECTED
X	X	H	X	X	H	NOT SELECTED
L	L	L	L	L	H	WRITE "0"
L	L	L	L	H	H	WRITE "1"
L	L	L	H	X	$\overline{D_{OUT}}$	READ DATA FROM ADDRESS LOCATION

H = HIGH VOLTAGE
L = LOW VOLTAGE
X = DON'T CARE (HIGH OR LOW)

Figure 3. Truth Table

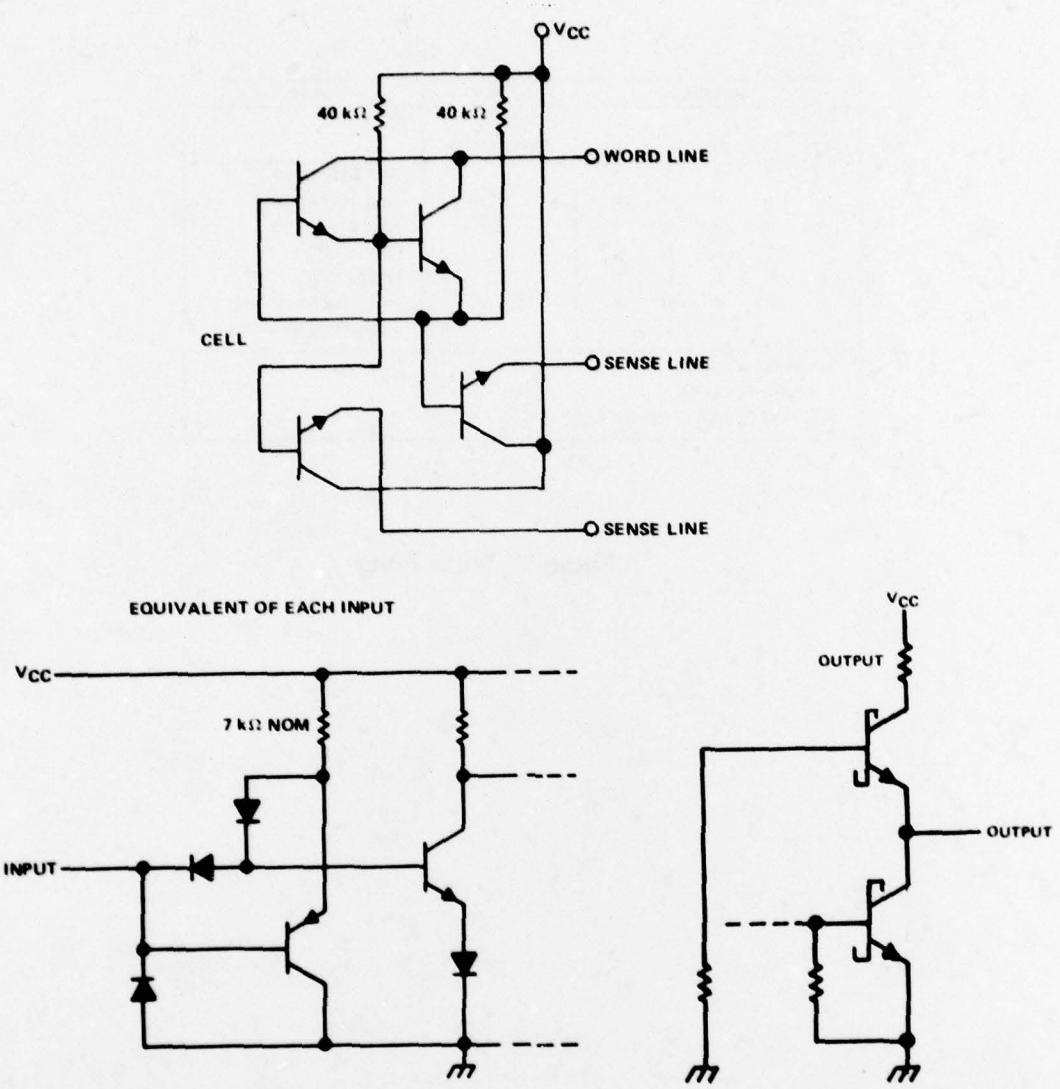
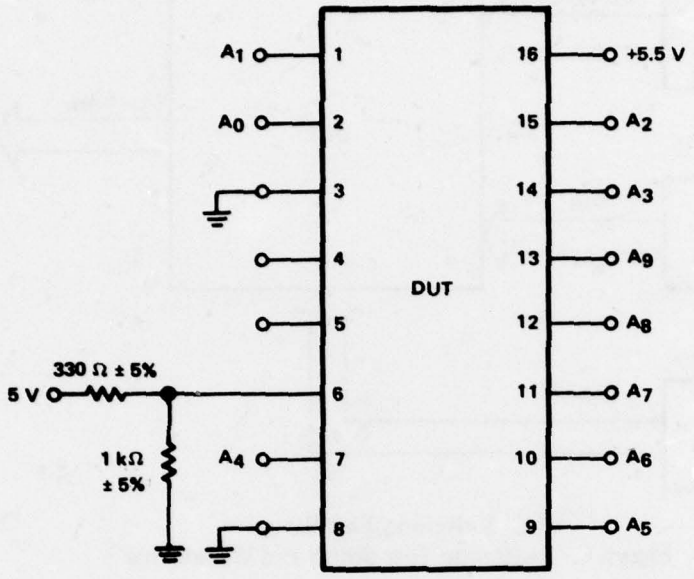
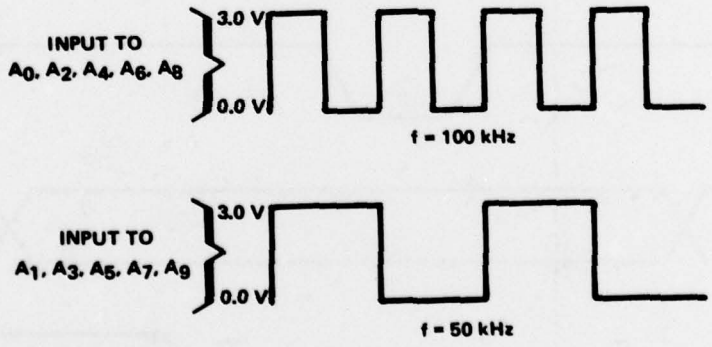


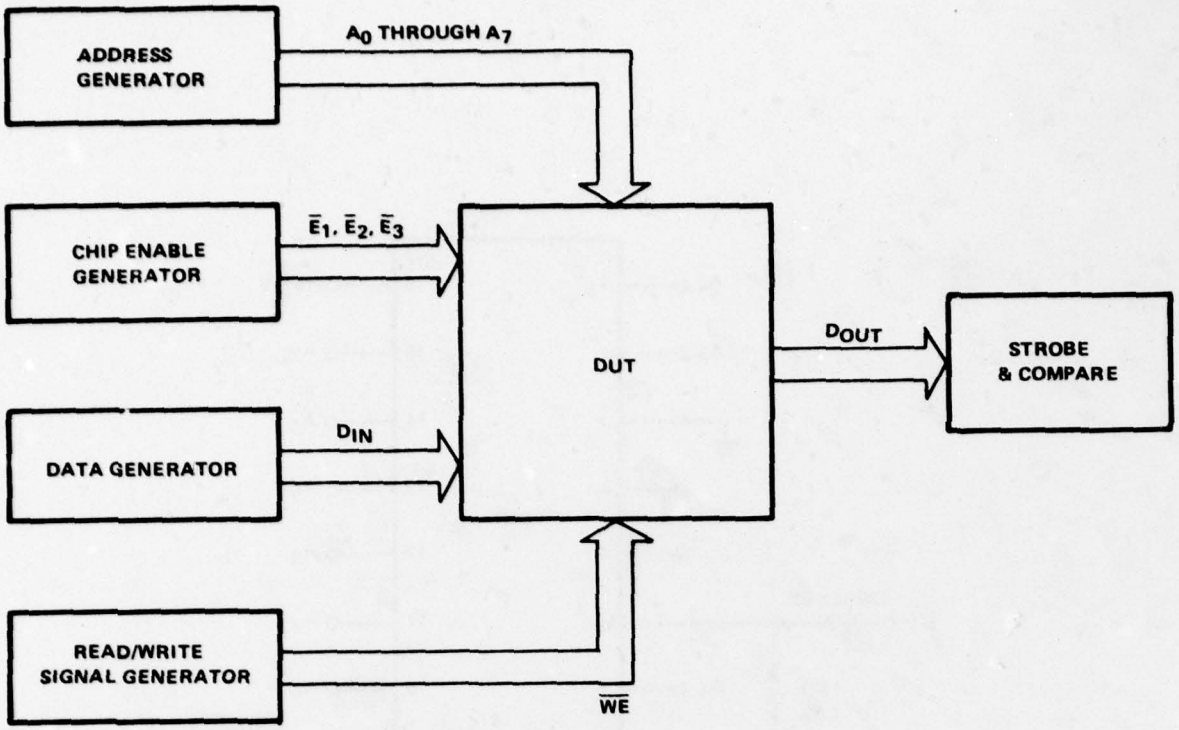
Figure 4. Schematic Circuits





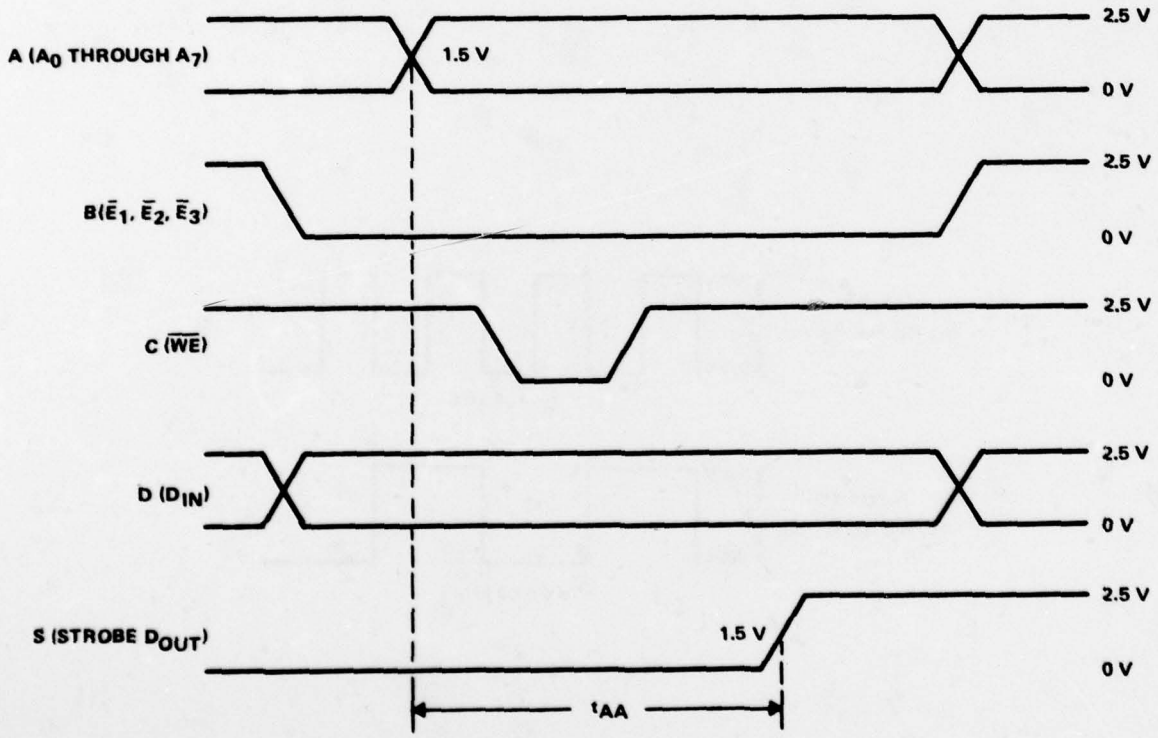
T_A = +70°C

Figure 5. Burn-In and Life Test Circuits



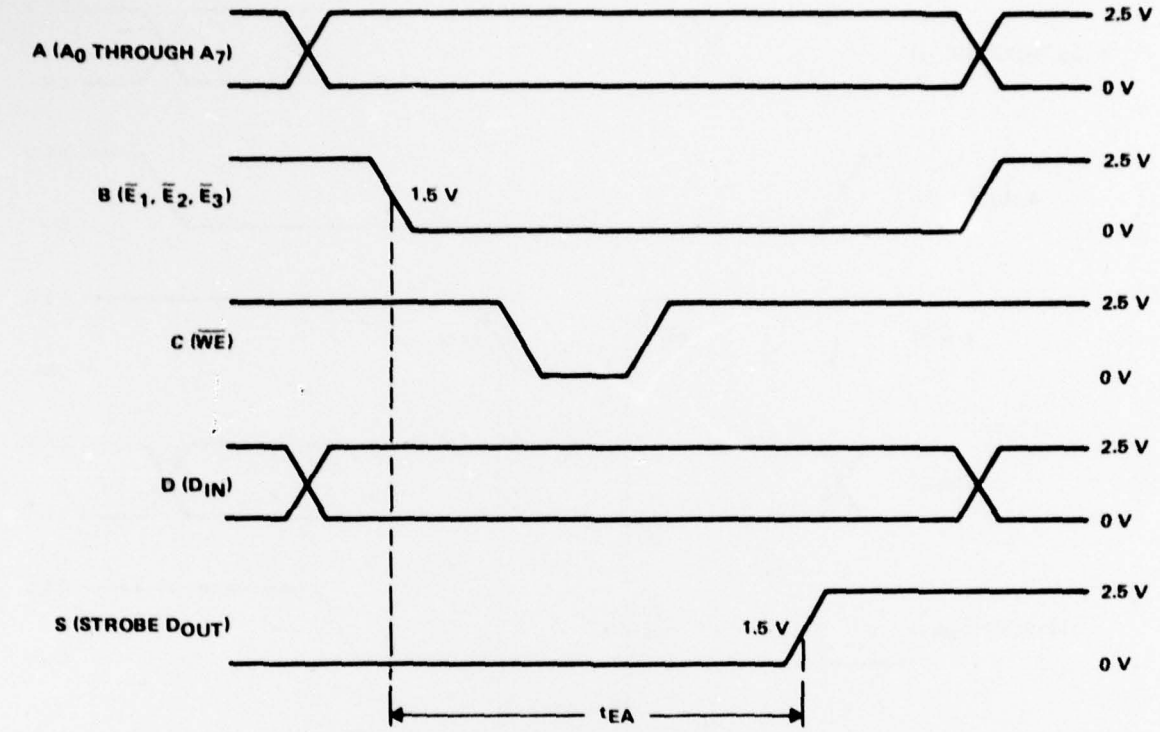
(a) Switching Test Setup

Figure 6. Switching Test Setup and Waveforms



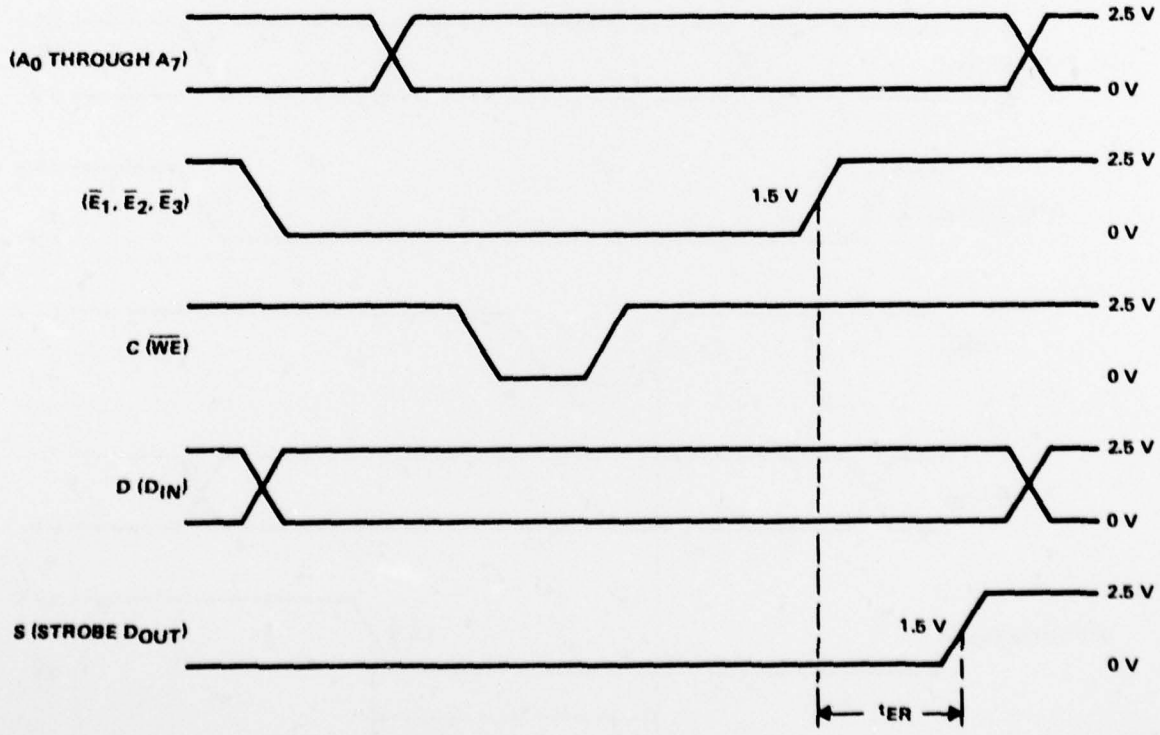
(b) Timing Waveforms for t_{AA}

Figure 6. Switching Test Setup and Waveforms



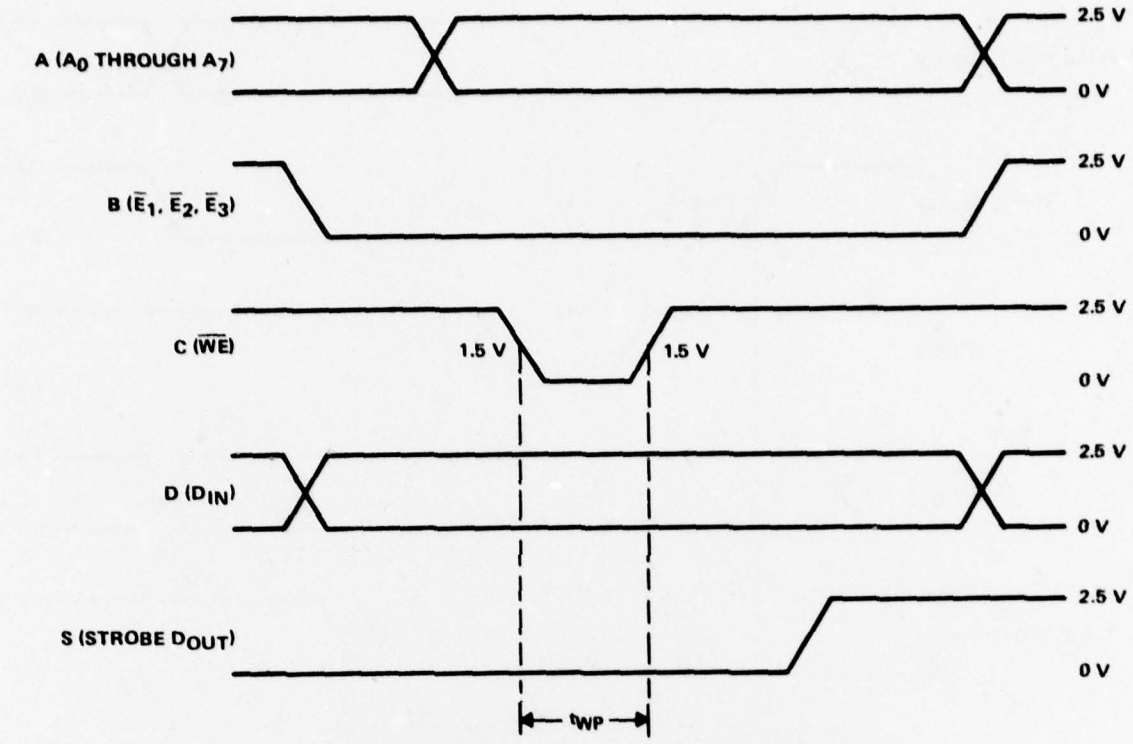
(c) Timing Waveforms for tEA

Figure 6. Switching Test Setup and Waveforms



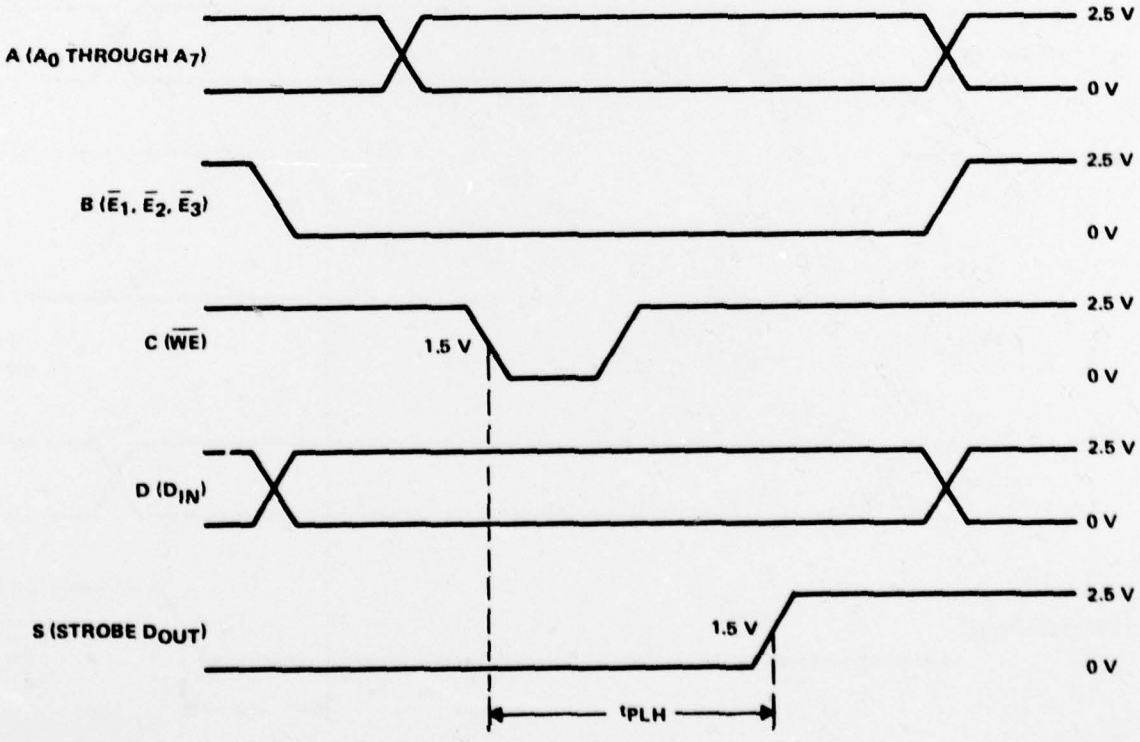
(d) Timing Waveforms for tER

Figure 6. Switching Test Setup and Waveforms



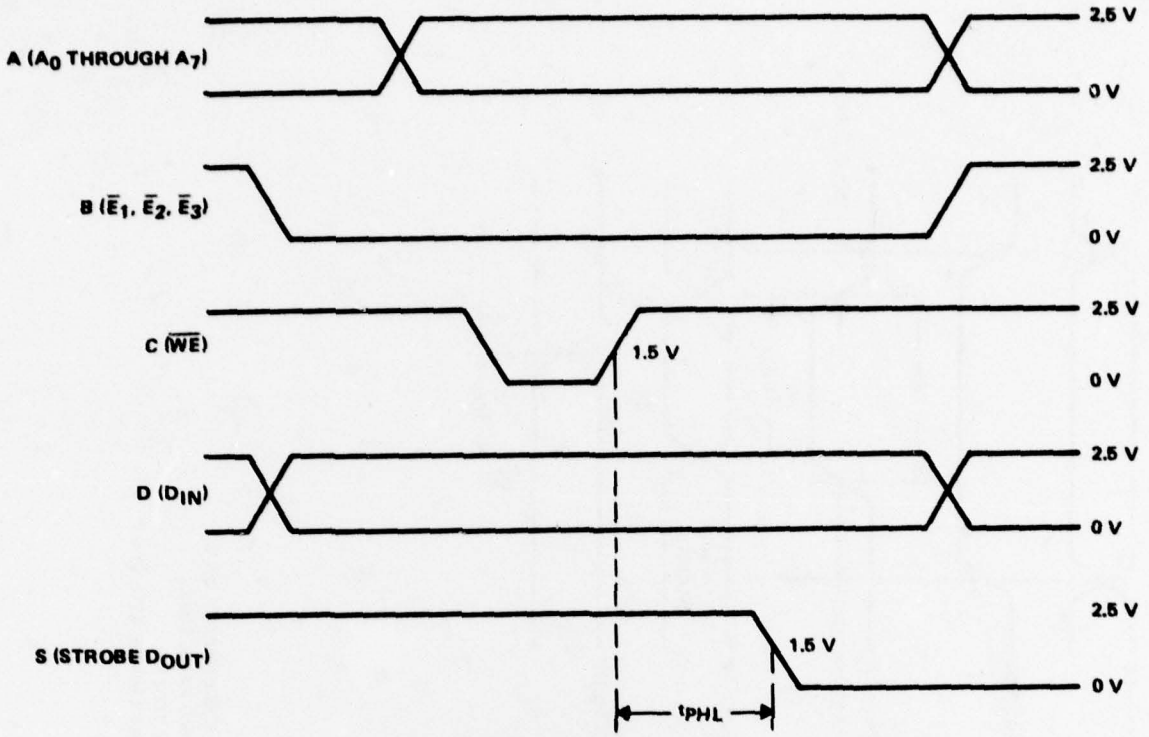
(e) Timing Waveforms for t_{WP}

Figure 6. Switching Test Setup and Waveforms



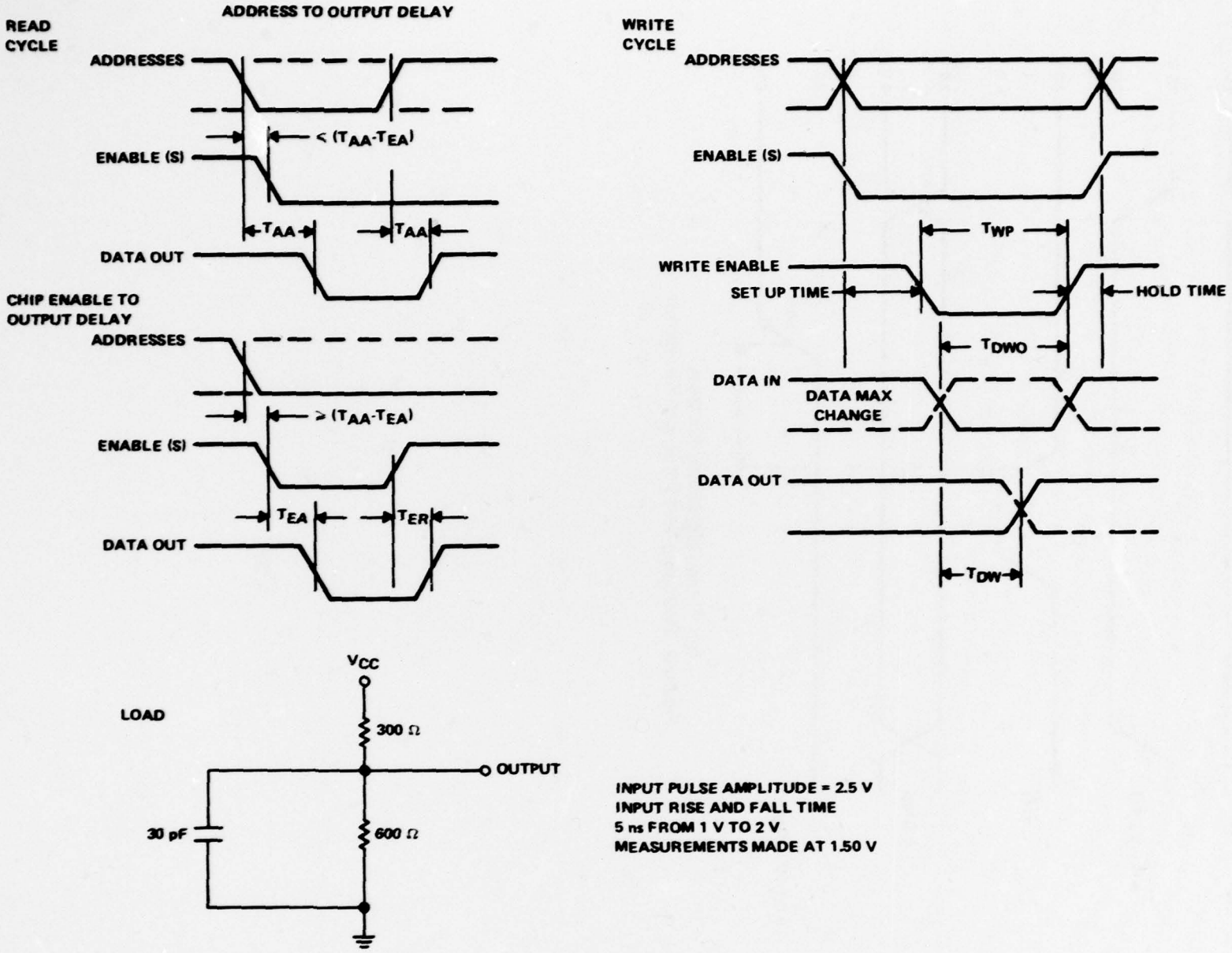
(f) Timing Waveforms for t_{PLH}

Figure 6. Switching Test Setup and Waveforms



(g) Timing Waveforms for t_{PHL}

Figure 6. Switching Test Setup and Waveforms



(h) Test Load and Timing Diagram

Figure 6. Switching Test Setup and Waveforms