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AN INDUSTRY SURVEY ON MANAGING THE TIMELY INTRODUCTION AND UTIL--ETC(U)
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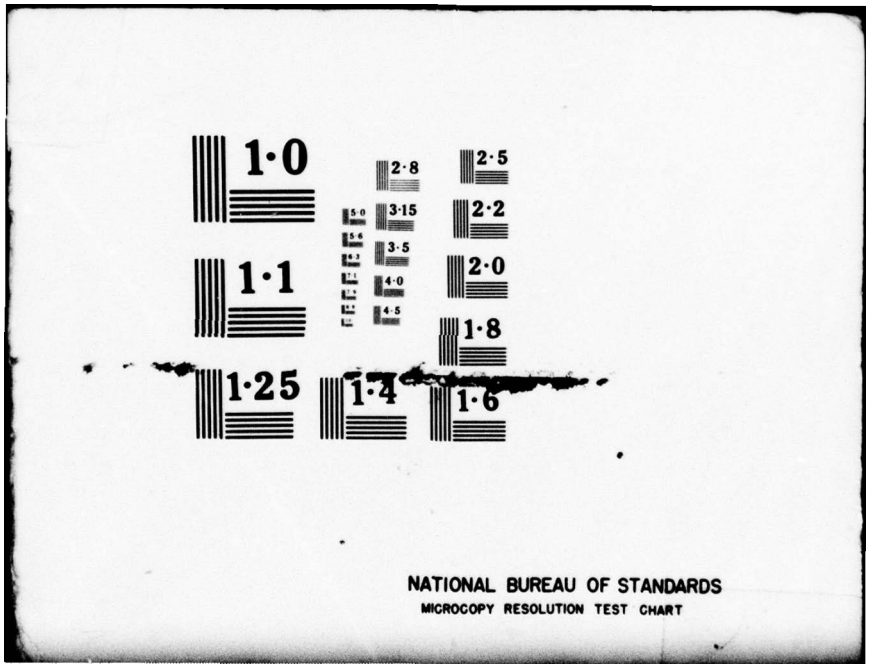
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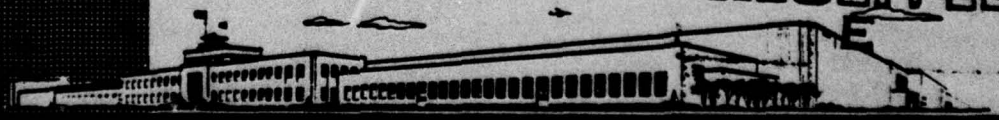
AN INDUSTRY SURVEY ON MANAGING THE TIMELY INTRODUCTION AND UTILIZATION OF LARGE SCALE INTEGRATED CIRCUITS IN MILITARY AVIONICS



NAVAL AVIONICS CENTER
INDIANAPOLIS, INDIANA 46218

NOTICES

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This report presents the results of an industry survey coordinated by the Naval Avionics Center to obtain information on issues involved in managing the timely introduction and utilization of large scale integrated (LSI) circuits in military avionics equipment. Responses were received from individuals in many companies representing semiconductor manufacturers, avionics equipment suppliers, and airframe contractors. The responses covered a wide range of issues involving LSI usage in military avionics, including LSI device introduction; device obsolescence; LSI specifications; testing and qualification; (over)

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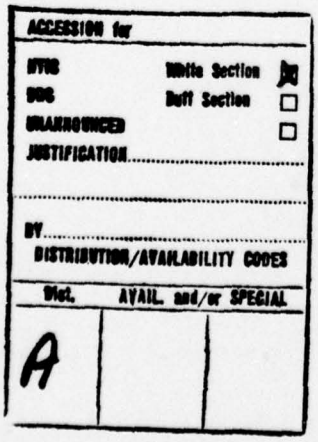
20. ABSTRACT

technologies needing Naval Air Systems Command development support; needed changes in MIL-specifications, standards, etc.; procurement practices; and standardization. Comments and suggestions receiving various degrees of concurrence among the respondents are identified and discussed. Detailed answers of the respondents to the survey questions are also included.

PREFACE

The use of large scale integrated (LSI) circuits, and especially custom LSI, in military equipment is currently lagging commercial applications by a wide margin. Levels of integration, i.e., the number of gates per chip, being used in commercial applications may exceed military applications by as much as two orders of magnitude. It has been estimated that even moderate increases (a factor of 10) in the average gate per chip density will result in significant cost savings over the life cycle of military electronics hardware.

A survey of industry has been conducted by the Naval Avionics Center in order to obtain information that will be useful in assisting Naval Air Systems Command management in an orderly introduction and utilization of advanced electronic technologies in Fleet hardware. Nineteen companies (two divisions of one company gave separate responses) provided comments in response to this survey. This technical report documents the survey results.



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The Naval Avionics Center wishes to thank the responding individuals and their respective companies for their thoughtful answers to our questionnaire exploring the complex management issues associated with the introduction of large scale integrated circuits into Navy equipments.

ABSTRACT

This report presents the results of an industry survey coordinated by the Naval Avionics Center to obtain information on issues involved in managing the timely introduction and utilization of large scale integrated (LSI) circuits in military avionics equipment. Responses were received from individuals in many companies representing semiconductor manufacturers, avionics equipment suppliers, and airframe contractors. The responses covered a wide range of issues involving LSI usage in military avionics, including LSI device introduction; device obsolescence; LSI specifications; testing and qualification; technologies needing Naval Air Systems Command development support; needed changes in MIL-specifications, standards, etc.; procurement practices; and standardization. Comments and suggestions receiving varying degrees of concurrence among the respondents are identified and discussed. Detailed answers of the respondents to the survey questions are also included.

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I. INTRODUCTION

This survey has been conducted to gather comments and suggestions from industry on a wide range of issues involved in the introduction and management of large scale integrated (LSI) circuits in military equipment. Letters containing a questionnaire were sent to over 100 companies comprised of semiconductor manufacturers, avionics equipment suppliers, and airframe contractors. The questionnaire, presented in Appendix A, consisted of questions designed to bring out discussions on the full range of issues considered important by the respondents. Companies providing responses to the survey are listed in Table 1 for reference.

The purpose of this report is to summarize the results of the survey, including detailed answers of the companies responding to the questionnaire. The comments and suggestions resulting from this survey are being considered in the formulation of a Naval Air Systems Command (NAVAIR) plan for utilization and management of advanced technologies; however, such a plan is not detailed in this report.

The replies were analyzed in order to identify common topics and suggestions being put forth by a number of respondents. While it is not necessarily true that these common suggestions are the best solutions, it is instructive to observe the issues on which various degrees of consensus are found. Section II presents comments and suggestions having the strongest concurrence among the respondents, and includes representative excerpts from their comments which discuss the issue in detail. Also included in the findings are comments and recommendations drawing common support from some of the respondents. Comments of a general nature are included in Section III. The detailed discussions of each survey question by each answerer are presented in Section IV.

A table of acronyms is provided in Appendix B.

TABLE 1. COMPANIES PROVIDING A RESPONSE TO THE SURVEY

Bendix, Communications Division
Delco Electronics Division, General Motors Corporation
General Electric Company, Aircraft Equipment Division
Harris Semiconductor, Programs Division
Honeywell, Inc.
Hughes Aircraft Company
IBM, Owego
Lear Siegler, Inc., Instrument Division
Litton, Data Systems
McDonnell-Douglas Corporation
Motorola, Inc., Semiconductor Group
Raytheon Company, Missile Systems Division
RCA, Government Systems Division
Rockwell International, Collins Division
Sperry Gyroscope
Sylvania, Electronic Components Group
Texas Instruments, Equipment Group
Vought Corporation
Westinghouse Electric Corporation, Advanced Technology Laboratories

II. SUMMARY OF FINDINGS

The answers to the survey were analyzed and a tabulation of recurring themes common to the various respondees was made to determine the degree of consensus among the companies. There were nine items for which there was a reasonably strong consensus, i.e., mention by six or more respondents. These nine items are given in Table 2 along with a matrix of the number of respondents adhering to each viewpoint. It should be noted that even though there was a consensus on these items, there was also a significant diversity of opinion on many issues, as can be seen in Section IV.

Although the companies responding to this survey are listed in Table 1 for reference, throughout the remainder of this report a reasonable attempt has been made to render their comments anonymous by removing company names and so forth. In some cases, responding individuals gave their personal views in answer to the questions, which were not necessarily the policies of their respective companies.

While the questions were designed to obtain the greatest amount of information on the various topics, the items discussed by the respondents are bounded by the set of questions used. The individuals answering the survey expressed similar ideas in different ways; therefore, the writer of this report has taken reasonable liberties in assessing the concurrence of their views.

TABLE 2. SUMMARY OF PREDOMINANT COMMENTS AND SUGGESTIONS

COMMENTS/SUGGESTIONS	COMPANIES MAKING COMMENTS/SUGGESTIONS*																				
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	TOTAL
A library of standard cells or building blocks and computer-aided design techniques should be utilized to design military custom LSI.	X	X					X	X	X	X	X	X	X	X				X			11
A means for second/multiple sourcing should be provided.	X		X		X			X	X		X	X			X					X	9
Integrated circuit technologies used in defense equipments should be restricted to those in the mainstream.	X	X		X				X			X	X	X	X			X				9
Radiation hardening technology developments should be funded by NAVAIR.				X	X		X	X	X	X	X	X	X								9
The assembly/module interface level should be functionally specified.		X		X			X		X	X	X			X	X						8
Long-term wafer storage for future logistics needs is probably technically feasible but may not be practical.		X	X	X	X			X			X	X									7
Circuit/device requirements should be introduced as functional specifications						X	X	X	X						X			X			6
Maximum use should be made of universal gate arrays, programmable logic arrays, read-only memories, and programmable function electronics in general.		X			X						X	X	X						X		6
MIL-M-38510 and MIL-STD-883 should be revised in light of LSI, especially in visual criteria.							X	X	X	X		X								X	6

*Companies have arbitrarily been assigned numbers in random order.

A. Predominant Comments and Suggestions

The comments and suggestions with the greatest concurrence among the respondents, as shown by Table 2, are as follows:

- A library of standard cells or building blocks and computer-aided design techniques should be utilized to design military custom LSI.
- A means for second/multiple sourcing should be provided.
- Integrated circuit technologies used in defense equipments should be restricted to those in the mainstream.
- Radiation hardening technology developments should be funded by NAVAIR.
- The assembly/module interface level should be functionally specified.
- Long-term wafer storage for future logistics needs is probably technically feasible but may not be practical.
- Circuit/device requirements should be introduced as functional specifications.
- Maximum use should be made of universal gate arrays, programmable logic arrays, read-only memories, and programmable function electronics in general.
- MIL-M-38510 and MIL-STD-883 should be revised in light of LSI, especially in visual criteria.

These are discussed in some detail by collecting excerpts from the survey answers, which follow later in this section. In general, the excerpts are as originally written. In a very few cases minor modifications have been made for continuity and readability. Material taken from the survey responses will be shown in script type for easy identification. Discussions taken from different respondents will be separated by asterisks (* * *).

1. A library of standard cells or building blocks and computer-aided design techniques should be utilized to design military custom LSI.

* * *

Standard cell approaches and design automation techniques are the best ways of attacking the development and turnaround time problems. DoD and NAVAIR might wish to consider further development programs in this area so as to lessen cost and development times.

* * *

CAD techniques should be used with emphasis on a Standard Cell approach. Automated LSI design systems have been developed by both NSA and NASA, and are in the public domain. Use of these systems greatly reduces turnaround time, cost, and risks because of the large amount of automated error checking. Standard cells have been carefully characterized so that their performance can be predicted accurately; therefore, automated layout using these cells has a high probability of success.

Every effort should be made to avoid the multiple try, minimum area procedures which are common in the commercial semiconductor industry. While this technique is sensible where an LSI chip will be manufactured in large quantities (hand calculators, for example), it does not make sense for a few thousand parts total.

Use of the Standard Cell family approach, while not minimizing the number of devices, would allow for a great degree of standardization

and encourage the use of new LSI. Basically, this gets back to the idea of owning both the designs and the process specifications, or placing them in the public domain.

* * *

Another way to reduce LSI qualification cost is to base LSI designs on the use of standard cells or universal arrays that have been qualified on previous programs. Changes in the interconnections of such approved cells are the only change made in revising the function being performed. This approach will reduce the cost of qualification of custom LSI families. Since a major portion of qualification cost is associated with the cost of the devices used in testing, the elimination or reduction in qualification testing on the basis of similarity within the family of devices generated from a standard cell library would result in substantial time and cost savings.

* * *

Computer placement and wiring of macro cells is an approach offered by a few vendors which provides moderate development cost and quick turnaround. NAVAIR should capitalize on the similarity of these LSI approaches by funding the development of common macro functions and the enhancement of the computer placement and wiring programs. These programs should be enhanced to permit input/output pin assignment as a design input. These developments should result in acceptable alternate sources.

Recurring costs of computer placed and wired macro cells are, of course, volume-dependent. Those functions that never achieve high volume would remain unchanged during their production life. However, those that achieve high volume should be redesigned using conventional hand placement and wiring to achieve minimum silicon die area and thus minimize cost. The initial computer placed-and-wired macro cell approach phase for known high volume functions offers quick development time at moderate cost, and hardware with which to test the designs in a system before committing to the long, costly hand layout of the desired LSI functions.

* * *

2. A means for second/multiple sourcing should be provided.

* * *

For custom LSI circuitry, limited avenues exist for insuring long term availability of parts. Initially, development of multiple sources capable of satisfying the device function should be established. Normally this will require some assurance on the manufacturer's behalf that these functions may ultimately be effective in the commercial market. A special protection could also include design disclosure documentation of suffucient detail to insure that any reputable company could produce the device even after the original company has lost interest due to economic considerations.

* * *

To protect against supplier catastrophe, multisourcing is the best alternative. However, NAVAIR must recognize that all sources must have sufficient annual business in order to remain an effective source.

* * *

To protect against vendor catastrophe, use off-the-shelf components with other sources. When a custom IC is developed, establish multiple sources.

* * *

The best protection against device obsolescence is to implement current standard multi-sourced devices to the maximum extent possible.

* * *

We have a strong internal standardization program which requires multiple sourcing, thereby increasing the probability that we have selected a technology which will have maximum life cycle.

* * *

When a CAD approach is used (for example, standard cells or universal arrays), the documentation (including line qualification devices) can be distributed to multiple vendors and requalification can easily be obtained at minimum cost.

* * *

3. Integrated circuit technologies used in defense equipments should be restricted to those in the mainstream.

* * *

Restrict the use of IC technologies to those which are in the technological mainstream, and for which some process commonality between suppliers exists.

A tentative list would be: ECL, S-TTL, CMOS, and CMOS/SOS.

Such technologies as CCD, I^2L, DMOS, VMOS, D-VMOS, etc., while technically attractive in certain applications, have too many process and layout variations from company to company to lend themselves to standardization at this time. As technologies develop, the preferred list can be upgraded.

* * *

The risk problem could best be solved by working with proven technologies manufactured by proven suppliers who are committed to supplying custom circuits, and in particular custom circuits for the DoD market. This also attacks the problem of maintaining reasonable business levels with suppliers.

* * *

Use a technology which is less likely to become obsolete. One example is CMOS/SOS, which is not presently used to any great extent commercially, but is supported by a great many system houses for internal use. While SOS chips are very expensive, by commercial standards, they are not an important part of the cost of the systems in which they are used. The existence of a relatively large number of firms which have committed this technology to military and commercial systems that can be expected to have long life spans practically assures that the technology will be available for a reasonable length of time.

* * *

The profit is not in the chips, but in the systems which use them. Therefore, there is much less incentive to abandon the technology for another which would require a very expensive system redesign.

* * *

Forward-looking technology selection should be encouraged. Government agencies can supply a strong influence and sense of direction to these efforts.

* * *

LSI technologies which are used should be proven processes that are reproducible from more than one semiconductor supplier.

* * *

For optimum quality and reliability performance, make technology selections where quality and reliability are built into the product utilizing processes that have been or will have been in use for one to two years, and where in-process controls can be utilized to monitor the operation.

* * *

NAVAIR can protect itself from the ever-increasing problems of devices/technologies that become obsolete during the operating life of avionics equipment by selecting technologies that are mainstream technologies and are supported by major semiconductor suppliers committed to exploitation of these technologies in the industrial and commercial marketplace. The success of a semiconductor supplier in building a large commercial catalog of parts and in stimulating a host of second source suppliers will assure longevity. In a successful technology, evolutionary transitions occur which lengthen the life of the technology. An example of evolutionary transitions is the shift in CMOS technology from Metal Gate to Silicon Gate to sapphire substrates. This evolutionary progression should be welcomed since it will extend the use of the basic logic technology for five to ten years or longer, and will not impact equipment designs as severely as might a more basic technological shift.

Avionics equipment designs should be implemented in broad-based technologies at the beginning of their production cycle in the semiconductor industry. Examples of technology to be considered for current applications are bulk CMOS silicon gate, CMOS/SOS, I^2L, and CCD; as opposed to considering RTL, DTL, T^2L, and other increasingly-obsolete technologies which may still be in production at some vendors, and which are used extensively in operational military systems designed a decade ago.

* * *

A general comment concerns the commonality of LSI processing over certain classes of devices. The technologies may be separated into bipolar, complementary bipolar, MOS (N or P channel), MNOS, CCD, etc. Within the bipolar, variations such as ECL, T^2L, and I^2L are made. However, within a given process family the effect of scale (size, number of active devices) has a less than direct effect on reliability. (Of course, scale has a very profound effect on the yield.) Processing commonality thus makes it possible to more quickly introduce larger scale integration into equipment.

* * *

4. Radiation hardening technology developments should be funded by NAVAIR.

* * *

Radiation-hard bipolar and MOS technologies needed for some future avionics systems will not likely evolve as spinoffs from nonmilitary products. Technologies such as CMOS and I^2L have the potential for high levels of integration because of low power consumptions. NAVAIR should, as a minimum, fund the development of radiation-hard I^2L because of its potential for extremely high integration levels and high radiation hardness levels. Funding the hardening of the CMOS technologies used in existing computer placed-and-wired macro cell approaches to LSI should also be considered.

* * *

One technology that will be required in future avionics systems and that will not be available in a timely manner as a spinoff from non-military products in Radiation Hardened Technology. CMOS/SOS is a technology that has inherent radiation hardness qualities. However, military funding is required to develop design aids such as standard cells and universal arrays that will enhance the inherent hardness and will be useful to meet custom LSI requirements for hardened avionics equipment.

NAVAIR should fund the development of this technology and the enhancement of its hardness capabilities as well as standard cell families and gate universal arrays. Technology choice is an ever-changing panorama.

* * *

The leading future commercial LSI and VLSI technology is NMOS. Unfortunately, NMOS is the least desirable of the future LSI semiconductor technologies when considering nuclear radiation hardening requirements. CMOS/SOS, I^2L, and T^2L offer increased capabilities in this area but they will not approach NMOS in commercial use. With the exception of I^2L, commercial use of LSI bipolar technologies will be inhibited by larger area per gate and power dissipation requirements. Future funding may be required to assure that essential CMOS/SOS and I^2L LSI products will be developed and refined to meet future military system requirements.

* * *

5. <u>The assembly/module interface level should be functionally specified</u>.

* * *

The technology can be managed at the shop replaceable assembly (SRA) level. The implementation of a standard modular approach such as that being developed in the Modular Avionic Packaging (MAP) Program will greatly facilitate the management of LSI in the future. This approach allows flexibility in achieving technological transparency through the use of form,

fit, and function specifications tailored to allow alternative approaches to the implementation of a given function. It will allow a modular function such as a minicomputer to be implemented with alternate LSI chip designs (e.g., Intel 8080A vs. AMD 9080A), yet permit the module level function to be completely transparent and amenable to advancing technology. Maximizing modularity of equipment design provides that necessary technology upgrading can be restricted to the afflicted subsystems and, therefore, does not require a complete system redesign. It allows the flexibility to introduce and sustain competition throughout equipment production programs. It also provides an environment compatible with the development of multiple sources.

* * *

6. Long-term wafer storage for future logistics needs is probably technically feasible but may not be practical.

* * *

In principle, wafer storage is feasible. In practice, however, it could be dangerous since semiconductor manufacturers might succumb to the temptation of shipping inferior products into storage. I believe that it is feasible to maintain a limited supply of semiprocessed wafers to achieve a fast turn-around for logic arrays, programmable logic units, etc. But products for spares or later production should be inventorized fully packaged and tested.

* * *

The aging characteristics of semiconductor devices in wafer form (if placed in the proper environment) can probably be neglected. However, we do not have long-term data in this area. I feel that the major problem involved in trying to do what they want would be in trying to keep all the peripheral areas intact and in good shape for a long period of time. Tooling would get lost and testing programs would not be kept up-to-date.

These kinds of things would be difficult to maintain in a high state of readiness with a high degree of confidence.

* * *

Devices should be stored preferably in the packaged state; however, if storage in the wafer state is necessary, a dry nitrogen atmosphere is recommended along with reinspection prior to use.

* * *

Technically, there is no major problem storing bipolar technologies, and we do not anticipate any major problem with surface related devices. The real problems are associated with planning and maintaining the resources required to provide the testing and packaging of the devices over an extended period of time.

* * *

This concept is feasible. However, we recommend, on technical grounds, against wafer storage due to possible handling damage. Dice storage would be more advisable. Storage would have to be in a dry, dust free, inert environment. Aging should not be a problem.

* * *

From an economic sense, NAVAIR would have to purchase the inventory and provide for the carrying cost of that inventory. NAVAIR would also have the problem of procuring the packaging and testing operation when the dice had to be packaged. In addition, NAVAIR would have to warranty that the dice were good beyond one year, since that is the semiconductor industry warranty period.

* * *

Semiconductor wafers could be stored in dry nitrogen with little or no apparent aging. I have a "gut feel" that due to the rate of change of the technology, they would probably not get used anyway.

* * *

We believe that parts should be stored in assembled, tested form rather than as wafers. For LSI parts, the cost of the package is

less than the cost of a good chip, so that potential cost advantages of storage in wafer form are offset by the risks of storing unprobed chips on unprotected wafers in unclean environments. If it is desired to store parts in wafer form, then wafers should be fully tested and inked, and complete test data stored for each good chip along with identification of the chip in the wafer matrix. All wafers should be stored in a flowing dry nitrogen ambient in a dust free cabinet. Preferably, a passivation technique should be used. Aluminum metallization cannot be exposed because it can corrode. We have experienced excessive leakage and lack of metal continuity in improperly stored CMOS wafers after several years.

* * *

7. Circuit/device requirements should be introduced as functional specifications.

* * *

Military equipment and device manufacturers have historically desired to "personalize" their product in their shop: that is, program a microprocessor, lay out the architecture of an FPLA, etc. There is a paradox here that must be considered. Device manufacturers want the freedom and flexibility to modify their products as they see the needs of the marketplace. Top-down technology direction from the Department of Defense (DoD), even though well-intentioned, could lead the IC industry into an area or product group which ultimately could turn out to be wrong. The present structure of the LSI/IC marketplace consists of multiple and distributed technologies, processes, and expertise, competing freely. While this structure is far from perfect, it may be preferable to a Federally-controlled device/technology program. A compromise solution may be for the military to identify its LSI needs from a functional rather than a device perspective. In this way the LSI manufacturers could competitively create what they feel are the best technologies, architectures, and processes to perform the required function.

* * *

LSI specifications should reflect terminal performance requirements, not internal architectural requirements. Knowledge of the internal workings of an LSI such as that necessary to do single gate fault testing may become less important as test philosophies for LSI evolve. It is already prohibitively costly in some cases to test an LSI exhaustively. As devices increase in complexity to VLSI, terminal performance testing/specifications (that is, testing for the function required in a specific application) may be the only practical test method.

* * *

Specify custom LSI parts replacement on the basis of functional equivalence as the best protection against the possibility of future parts unavailability and technology obsolescence. Functional equivalence is defined as a replacement part having identical electrical and logic characteristics to the original part, and having the same external packaging configuration (e.g., 24-pin DIP) with identical pin assignments. The acceptance of functionally equivalent parts will obviate the need to document the process by which the original parts were made and to re-establish an identical line after a lapsed time of perhaps ten years, during which process materials (resists, solvents, etc.) and equipment (furnaces, etchers, testers) may all have changed.

* * *

Complex custom LSI devices should be specified as a system with all necessary functional requirements included. Any attempt to specify detailed implementation (i.e., technology, topology, etc.) will unnecessarily restrict potential sources.

* * *

Function standardization is a possible solution. For example, standardize a bus interface function, but do not specify the technology in which it must be implemented.

* * *

8. Maximum use should be made of universal gate arrays, programmable logic arrays, read-only memories, and programmable function electronics in general.

* * *

Maximize the use of gate arrays (bipolar) and cell libraries (MOS). Make the use of an existing up-to-date CAD system a precondition for development contract awards.

* * *

The master chip and PLA concepts should be encouraged. A clearing house for available master chip designs and a catalog of equivalent MSI functions that can be implemented from these designs would encourage usage.

* * *

Experience indicates that LSI functions should be implemented with a technology which supports at least 1000 gates per 20,000 square mils of chip area, including interconnect. I^2L *satisfies this requirement well.*

* * *

To minimize design cost and cycle time, applications requiring fewer than 1000 gates of complexity (64 flip-flops, 500 gates, and I/O buffers) should employ a gate array technique. Cycle time to receiving functional parts with this approach is eight to ten weeks.

* * *

9. MIL-M-38510 and MIL-STD-883 should be revised in light of LSI, especially in visual criteria.

* * *

Pre-cap inspection of LSI and VLSI devices has become impractical due to the multiple levels of the device fabrication process and the extraordinarily geometric detail of the devices.

Pre-cap inspection criteria should be reduced to focus on inspection of the device packaging and bonding quality. Verification of functional attributes should be accomplished by functional testing at extended temperatures over a prescribed number of temperature cycles.

* * *

Chip testing was being considered by RADC/USAF as a tradeoff for the pre-cap visual inspection required by MIL-STD-883, Method 5004, due to the complexity of the device. RADC/USAF should be queried to determine what conclusions were reached in their 1975-1977 studies regarding tests/cost tradeoffs.

* * *

Develop a means of stressing the device electrically to augment the use of a pre-encapsulated visual inspection. A gross visual inspection, while being adequate for gross problems such as bond integrity and contamination, cannot reveal subtle defects that an electrical stress would identify.

* * *

Also, as device complexity increases, some form of electrical testing must also be used to replace at least some of the visual inspections.

* * *

For standard LSI circuits, such as memory and microprocessors, present MIL-M-38510 or equivalent specifications are more than adequate. In fact, some rethinking of MIL-STD-883 and MIL-M-38510 in light of the LSI needs might be in order. This is especially true in the area of visual criteria.

* * *

As microcircuit complexity increases, it becomes more difficult to perform cost effective quality and reliability tests (e.g., visual inspection, complete 100% electrical, etc.) New quality and reliability tests should be investigated and implemented into the military specification

system, MIL-M-38510/MIL-STD-883 (e.g., as High Temperature Acceleration Test, Guard Band Testing at above rated voltages). A study is needed on the effectiveness of static burn-in vs. dynamic burn-in for LSI devices.

* * *

The Joint Electron Device Engineering Council JC13.2 Committee on Government Liaison for Microelectronic Devices has recently developed a matrix of cost-effective suggestions related not only to LSI but to all JAN ICs.[1]

* * *

[1] A copy of the JC13.2 Committee proposal, along with a marked-up copy of MIL-M-38510 reflecting the ideas and their implementation paragraphs, was forwarded to NAC with this respondent's reply to the survey. The address of the JEDEC Solid State Products Council is 2001 Eye Street NW, Washington, D. C. 20006; telephone (202) 457-4971.

B. Comments and Suggestions Finding Some Concurrence Among Respondents

The following list is composed of those items finding at least some concurrence among the survey respondents:

- Wafers and/or tested dice should be stored for future logistic needs.
- The Navy should establish a semiconductor technology data base, including a "clearing house" function for LSI requirements and developments.
- The Navy should have a repository of graphic tapes for re-creation of mask sets, process specifications, test tapes, etc. for military custom LSI.
- All custom LSI circuits for Navy applications should be fully documented and owned by the Navy.
- Microcircuit technology upgrades should be planned prior to production start-up and should be provided for during the procurement cycle.
- Vertically integrated DoD contractors are the best source of custom LSI for military custom LSI.
- DoD should fund CAD/standard cell development and documentation.

- The Navy should commit to an LSI supplier early enough in the procurement cycle for the project contract production run.

- GaAs high speed logic development should be funded by NAVAIR.

- Additional data and further discussion is needed to truly identify problems and viable solutions.

- Test patterns should be used for device requalification.

- The existing MIL-M-38510 standardization system (DESC) should be utilized for LSI standardization.

- A family of military LSI devices should be identified and fabricated.

- A life cycle cost analysis should be performed to determine the impact of LSI on systems.

Detailed discussions of each of these items are found throughout Section IV.

III. GENERAL COMMENTS

Before proceeding to the detailed answers produced by the survey, some pertinent general comments from the respondents are presented. Throughout this Section, and also in Section IV, each respondent's comments are presented in a consistent format, i.e., comments from respondent 1 are always given first, followed in numerical sequence by respondents 2, 3, and so forth. If no answer was provided by a specific respondent, then a "no comment" will follow that number.

* * *

1. Your questions are very thought-provoking, and you will probably receive as many different answers to your questionnaire as people who answer it. The answers to many of the questions are opinions and are not based upon data or hard facts simply because there are none. I believe, therefore, that to a large degree the final direction upon which you decide to steer your suppliers will also be based upon your opinion and management decision, which are not based upon facts for the same reason. Your enclosure (2), Respondent Information, probably holds the key to your final decision. Let me at this time invite you or members of your staff to visit at your convenience. I believe a much more thorough understanding of both the question and the answer or position we might take could be gained by both parties if we met face to face and openly discussed each item.

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2. As a general comment, I would like to add my feeling that it will be impossible to resolve beforehand on paper all potential problems connected with the use of LSI. Naturally, a maximum of planning should be done. But in the final analysis it seems better to learn by doing (with some trials and errors) than to risk the obsolescence of our military electronic capabilities.

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3. No comment.

* * *

4. No comment.

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5. Existing Government standardization efforts by DESC and RADC are encouraging, and expansion/participation by other Government agencies should be considered. Standardization efforts could then be linked with cost benefit analyses to determine which components need reliability upgrading.

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6. No comment.

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7. No comment.

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8. No comment.

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9. The management of LSI introduction into military equipment is multifaceted due to the nature of the various technology approaches, the application requirements, and the industrial manufacturing base. There are three types of LSI to be managed:

a. Standard commercial LSI being offered to commercial original equipment manufacturers (OEMs) by major semiconductor manufacturers.

b. Quasi-standard LSI devices that may be modified to meet unique functional requirements (e.g., PLAs) and manufactured by either major semiconductor houses or aerospace system and subsystem manufacturers.

c. Custom LSI designed to meet unique functional performance requirements, usually designed and produced by aerospace system and subsystem equipment manufacturers.

The United States industrial capacity for LSI manufacturing consists of two distinct resources: (1) major commercial semiconductor manufacturers, and (2) equipment manufacturers vertically integrated to produce custom LSI. This latter resource is currently developing rapidly as a result of an inability of aerospace equipment manufacturers to economically motivate the semiconductor houses to provide low volume "special functions" in technologies compatible with the military environment. Major semiconductor houses are generally not willing to commit limited technical resources to developing custom circuits with a relatively limited market potential.

The industrial capacity resident in aerospace equipment manufacturing firms is essential to meeting future military electronics requirements. This capability will allow the military to meet increased performance capabilities, reduce equipment size and weight, and the full spectrum of anticipated environmental requirements without dependency on commercial manufacturers, whose major focus is on the high volume OEM market. The management of the introduction of LSI into military equipment is very similar to that of hybrid device management. Hybrid devices in the mid- and late 1960's offered comparable performance advantages with the same management problems as are being addressed in this survey. The same aforementioned aerospace complex has, over the last 15 years, developed and implemented the widely varying hybrid technologies in military electronics, supported virtually all types of logistic support concepts, and demonstrated high reliability in a cost-effective manner. The lessons learned from hybrid implementation might well provide a guide for the problems addressed in this survey.

Requiring the demonstration of second sourcing capability is an additional management constraint that obviates much of DoD's concern over product longevity and supportability.

We feel the key to the problem of introducing LSI into military electronics equipment will be through a concept called "technological transparency." This concept requires specification of an Avionics architectural element so that the functional interfaces and performance requirements are completely defined and modularly implemented without limiting the method or technology required to implement the function. These modular elements can then be replaced with equivalent elements incorporating advanced technology without impacting system design installation or software.

The constraining of any hardware level of complexity to be technologically transparent, though necessary, will result in some penalty in packaging efficiency (i.e., weight and volume). Equipment weight will continue to slowly decrease as numerous SSI and MSI devices are replaced by a single complex LSI device, although minimum weight will not be achieved because of architectural constraints.

The semiconductor industry pays little attention to the military industry for various reasons (low quantity, specification proliferation, specification interpretation, etc.) Semiconductor manufacturers have difficulty in predicting what the military "demand" will be. This is because of the diverse and widespread project-oriented method of the military complex. In the commercial world, semiconductor manufacturers can deal at industry corporate levels; and therefore, get a good feel for market demand. Such is not the case with the military complex. An example, many device suppliers indicate there is little demand existing for MIL-M-38510 qualified parts list devices for which they have qualified. Suppliers go through the effort of qualifying but then find little demand for these devices. A "Military Marketing Organization" (forecasters for future military needs) would help to alleviate this problem. Volume purchase agreements, similar to those used in the commercial market, could be instituted. The semiconductor industry would then pay more attention to the needs of the military.

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10. The questions posed in the Survey on Managing the Timely Introduction of Large Scale Integrated Circuits into Military Avionics cover a broad spectrum. It is difficult, if not impossible, to provide answers that are satisfactory to all parties concerned. These questions or similar questions have been asked and debated for some time. The Institute for Defense Analyses (IDA) held a three-day meeting in August (9th, 10th, and 11th) to discuss the Utilization of LSICs in Military Systems. At that time, quite similar questions and proposed solutions were discussed at length in both formal presentations and in small informal groups. We participated in the IDA meeting and came away from the meeting with two distinct feelings. First of all, those attending the meeting were serious in their attempts to propose satisfactory answers to the complex questions, and secondly, there appeared to be no answers satisfactory to all concerned. These feelings lead us to believe that perhaps the questions are too broad and attempt to cover too many diverse situations. Perhaps if the questions could be partitioned properly, the best answer for particular elements could be devised so that the overall problems could be adequately resolved.

The survey questions hint at two basic approaches, neither of which appears to be best for all situations. The one approach attempts to assure adequate parts are available to the Navy during the life of the equipment. The other approach attempts to assure adequate equipments are available with the parts availability remaining the responsibility of the equipment supplier.

In the situations where lifetime warranties are used, opportunities for upgrading and using newer technologies can be worked out so that obsolescence of technologies becomes less of a problem. In situations where the maintenance is best performed by the Navy, spares requirements for the life of the equipment or availability guarantees may have to be part of the initial equipment procurement to assure adequate parts.

An approach discussed at the IDA meeting suggested that the customer define the architecture such that there would be sufficient freedom to design modules and to update the modules without disrupting the system (or box) performance. It was believed that this approach could capitalize on the advantages of new technologies and also reduce the impact from the discontinuance of an older technology. The 1553 bus specification was cited as an example of a start in this direction. Again, this approach might be best for some situations but not for all.

* * *

11. We believe that LSI offers advantages of cost, reliability, size, weight, and performance. Military equipment procurement needs to insist on the use of LSI to achieve these advantages. The present emphasis on acquisition cost penalizes the use of LSI. Life cycle costing shows significant advantages from using LSI. All equipment production programs need to provide time and funding for the conversion of initial breadboards to LSI format before production startup.

LSI technologies are high performance technologies. CMOS and CMOS/SOS offer advantages of low power dissipation, high speed, and ease of circuit design which the Government should use.

It is necessary that the resources of the semiconductor producers and those of Government system contractors be used to provide Government agencies with the most cost-effective approach to designing and manufacturing equipments using LSI devices. We believe that Government agencies and contractors should work together under a framework of responsibilities similar to those outlined below:

NAVAIR

1. System performance requirements
2. System physical requirements
3. Classification level
4. Quality level

INDUSTRY

1. Subsystem partitioning and specification
2. Hardware configuration
3. Selection of technology and vendors
4. Design implementation
5. Production

Although we believe that the technology selection should be done by the responsible contractor, NAVAIR approves the technology choice through its selection of the successful bidder for a new program. The prime responsibility for a successful product meeting NAVAIR's requirements must remain with the chosen contractor.

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12. No comment.

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13. No comment.

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14. No comment.

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15. No comment.

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16. No comment.

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17. No comment.

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18. Increasing concern is being evidenced by both DoD and military equipment suppliers over the tardy entry of advanced large scale integration into military systems. A recent Arthur D. Little study, for example, presented at the IDA Sympoisum on "Future Applications of LSICs in Military Systems" (9-11 August 1977) pointed out that in military systems the average gate complexity per integrated circuit has flattened out over the last few years at about 30 gates per part. In commercial electronics (especially

consumer electronics), however, the average gate count per IC is escalating rapidly into the hundreds of gates per chip.

The continuing use of the basic vendor SSI/MSI standard functions is allowing military equipment to currently have low-risk development. However, future support problems could be projected due to the concern over long-term availability of even these parts, as well as the limited reliability, maintainability, and availability of weapons systems implemented with such large quantities of integrated circuits. The risk that has been associated with LSI chip development for military systems has been of enough concern to major programs to warrant their choice of the standard SSI/MSI functions. The development of LSI chips for military requirements has been fraught with unpredictable schedules, relatively high non-recurring costs, and limited sources of procurement. To look at alternate solutions to our present dilemma of limited LSI usage, we must look at a much wider scope than just that of the cost trade-off between LSI and their SSI/MSI equivalents.

The present DoD procurement system, device qualification, documentation, and long-term logistics and support of electronic systems must necessarily be considered. It is not adequate to have a better system (procurement, support, or documentation) but which is overlaid on top of the existing systems. We must be able to displace something that we are already doing in order to have a cost savings. However, there are very few of us in industry or DoD who have a sufficient breadth and detailed grasp of the very large trade-offs involved which cross the gamut from the design and procurement of devices through the qualification, support, and logistics of those devices in complex systems. This point makes answering of the very important NAC questions in a complete and significant fashion very difficult.

A strong suggestion could be made to gather data so that we could truly identify where tasks are being eliminated through the use

of LSI and where support, maintenance, and availability of electronic systems are improved. This in itself would help us identify how to use LSI to provide more easily maintainable systems and systems which provide greater availability of the complete aircraft, ship, and ground-based systems.

I don't think we really know what the problem is. The problem seems to be that we would like to use LSI to save costs and improve reliability of military systems, but we don't know what the costs are since they entail much more than just the development costs and even the procurement costs, but they also go into a myriad of long-term support and logistics costs with associated documentation and qualification costs. It is therefore hard to perceive where the leading factors are for potential reduction. I think a study and definition by DoD of these factors and sensitivity analysis of how, within the current (or alterable) framework of logistics and support, these costs can be reduced, would be of extreme benefit in learning how to best apply LSI. For example, we must know whether to apply LSI to basically imitate the SSI/MSI functions in a more cost-effective, smaller volume fashion, or whether we should also try to enhance the system with reliability, maintainability, built-in test, and/or self-healing features which could not have been justified using discrete components.

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19. No comment.

* * *

20. No comment.

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IV. ANSWERS TO SURVEY QUESTIONS

This section contains the detailed answers provided by the respondents to each survey question. An overview statement highlighting the comments for which a degree of consensus is evident and which lists other points made by the respondents is provided for each question by the editor, and precedes the detailed responses.

A. Question #1: How should the Naval Air Systems Command (NAVAIR) facilitate the use of advanced technology microcircuits, while insuring adequate support of logistics and potential mobilization needs, and protecting itself against supplier catastrophe?

Highlights:

There was a good measure of diversity in the answers provided to this question. This was expected because of the complexity of the problem. A list of the items receiving the most attention by the respondents is as follows:

- The Government should consider a repository of graphic tapes and so forth for re-creation of mask sets for custom LSI.
- Some form of second sourcing for LSI devices should be established.
- The utilization of IC technologies should be limited to those in the mainstream of technology usage, and where some process commonality exists between suppliers.

Question #1: How should the Naval Air Systems Command (NAVAIR) facilitate the use of advanced technology microcircuits, while insuring adequate support of logistics and potential mobilization needs, and protecting itself against supplier catastrophe?

- Computer-aided design techniques using standard cells should be perfected and used to design military custom ICs.

- The military should make "life of type" buys of IC device wafers and store for future logistic use and for protection against device obsolescence.

- LSI devices and modules of assembly level electronics should be defined and specified functionally. Permit the supplier to detail mechanization to meet functional requirements.

- Allow sufficient time and funding for development and procurement of custom LSI devices.

- A life cycle cost analysis should be done to determine the impact of LSI on electronics equipment. Project funding should be based on the total life cycle of the equipment, not on the minimum development costs only.

- Consider establishment of a Government-maintained semiconductor technology data base.

Question #1: How should the Naval Air Systems Command (NAVAIR) facilitate the use of advanced technology microcircuits, while insuring adequate support of logistics and potential mobilization needs, and protecting itself against supplier catastrophe?

Industry Replies:

1. Your first question has two parts. The first concerns logistics support and mobilization needs. Logistics, I assume, is the problem of providing the Fleet with adequate spare components to allow repair of the equipment while at sea or other installations. I would think a more aggressive use of LSI would, as a matter of fact, simplify the problem of repair at sea. It seems reasonable that if one LSI circuit provided the electronic complexity of one hundred simple small scale functions (even though the small scale functions may be used repeatedly throughout the system), the number of different components used has to be more favorable (fewer) with an increasing usage of the more complex functions. The answer, I feel, somewhat relates to the reason the Navy years ago decided to influence your suppliers to use the Navy Standard Hardware or NAC Modules. Even though this approach did present some problems, I imagine they were far more manageable than the alternate of not using NAC Modules.

Mobilization needs can easily be met by U.S. makers of LSI as long as the technology is still being produced. A repository of graphic tapes for re-creation of mask sets would be worth considering. The only way the Navy can protect itself against supplier catastrophe is to insist that each component have a demonstrated multiple source. On custom devices where no second source exists, the Navy should insist that as a part of the original design contract requirement that the manufacturer adequately document the process and provide not only this document but also sets of reproducible masks to the Navy, with certain proprietary rights that only in the case of a supplier catastrophe could the Navy provide this document to an alternate source.

* * *

Question #1: How should the Naval Air Systems Command (NAVAIR) facilitate the use of advanced technology microcircuits, while insuring adequate support of logistics and potential mobilization needs, and protecting itself against supplier catastrophe?

2. Restrict the use of IC technologies to those which are in the technological mainstream, and for which some process commonality exists between suppliers.

A tentative list would be: ECL, S-TTL, CMOS, and CMOS/SOS.

Such technologies as CCD, I^2L, DMOS, VMOS, D-VMOS, etc.; while technically attractive in certain applications, have too many process and layout variations from company to company to lend themselves to standardization at this time. As technologies develop, the preferred list can be upgraded.

Make sure that all circuit designs for military applications are fully documented and that ownership belongs to the Navy. Documentation should include circuit diagrams, truth table or transfer function, dynamic and static circuit specifications, mask layout on magnetic tape, and test program, also on tape. This assures second-sourcing at reasonable cost, if required.

* * *

3. Protect against vendor catastrophe by:

a. Using off-the-shelf components with other sources.

b. Establishing multiple sources when a custom IC is developed.

c. Formulating a "brute force" contingency plan to ensure mobilization capability; this might be a Government stockpile or inventory of parts. Could such a stockpile be used as a "damper" for the ups and downs in the semiconductor world that plague capitalization plans?

Question #1: How should the Naval Air Systems Command (NAVAIR) facilitate the use of advanced technology microcircuits, while insuring adequate support of logistics and potential mobilization needs, and protecting itself against supplier catastrophe?

NAVAIR should set up their own processing facility to fabricate the LSI circuits. They should also work with a second vendor to have a dual source capability. It would probably not be necessary to design LSI circuits themselves. This part of the work could be contracted out to an independent design group. Once the circuit has been designed, fabricated, and shown to be satisfactory, then the Naval Avionics Center should take charge of all tooling and coordinate the production of circuits and systems. The small volume production runs would not be very attractive to most of the larger semiconductor houses. This would be a major reason for setting up NAVAIR's own processing capability. However, if the process is similar to that of another vendor, then they could probably get parts processed from their own tooling at reasonable cost.

* * *

4. Concerning the first two questions, an in-house custom device facility responsive to system needs is the method we utilize to accommodate the timely introduction of technology with protection against loss of supply. Thus, the best way for NAVAIR to facilitate the use of LSI with appropriate safeguards is to procure to systems and/or line replaceable units (LRUs) specifications appropriate to require the introduction of this technology, and depend on the manufacturer of the larger equipment to handle logistics, mobilization, and multiple sourcing where necessary. Another vehicle for facilitating the introduction of microcircuits is to direct their use in the work statement and to allow sufficient time for their introduction. Many procurements have time phasing that makes it very difficult to use anything but currently existing components.

* * *

5. NAVAIR should run a survey to see what other Government agencies and industry are standardizing on, and attempt to standardize on

Question #1: How should the Naval Air Systems Command (NAVAIR) facilitate the use of advanced technology microcircuits, while insuring adequate support of logistics and potential mobilization needs, and protecting itself against supplier catastrophe?

the same devices. This will help to assure the use of a leading edge technology which is multi-sourced, or capable of being multi-sourced.

* * *

6. Introduce the circuit requirements as functional requirements which are deliberately specified as broadly as possible while still enabling the circuit to perform its duty. This will provide the flexibility of performing the function with multiple technology and provide for multiple sourcing.

* * *

7. NAVAIR should direct its efforts toward using devices that are standardized, where the "standard" trade-off includes: function, military second-source capability, mature and stable processes, and adequacy of documentation. The vendors should be capable of supplying the LSI devices from production lines located in geographically diverse areas, to preclude the possibility of natural or local (internal vendor) disasters.

* * *

8. Probably the most significant factor limiting the use of advanced technology microcircuits in military systems is the very long procurement time. By the time an avionics system has gone through all of the various development phases and is entering full scale production, three to five years have gone by and the microcircuit technology is at least "three to five year old vintage." To effect this situation, several possibilities present themselves:

a. Shorter development and procurement times.

b. Planned-for microcircuit technology upgrades prior to production start-up.

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c. Several planned-for technology upgrades during the course of system procurement in the case of long-term procurements would be advisable. Naturally, these planned-for technology upgrades would be implemented only if the then current state-of-the-art technology offered significant improvements for the system under consideration. Of course, this approach would necessitate consideration of the overall economics of the procurement not only from the DoD point of view, but from the system and microcircuit supplier perspective as well.

In order to insure support of logistic and mobilization needs, NAVAIR must consider either "life of type procurement" or else be prepared to make the business seem attractive to the microcircuit supplier. To protect against supplier catastrophe, multisourcing is the best alternative. However, NAVAIR must recognize that all sources must have sufficient annual business in order to remain an effective source.

* * *

9. The answer to this question is found in selecting the optimum level of hardware complexity to be technologically transparent. Clearly, the device level poses the most difficulty in assuring technological transparency for the range of future semiconductor technologies.

It is recommended that the technology be managed at the subassembly (SRA) level. The implementation of a standard modular approach such as that being developed in the Modular Avionic Packaging (MAP) Program will greatly facilitate the management of LSI in the future. This approach allows flexibility in achieving a technological transparency through the use of form, fit, and function specifications tailored to allow alternative approaches to the implementation of a given function. It will allow a

Question #1: How should the Naval Air Systems Command (NAVAIR) facilitate the use of advanced technology microcircuits, while insuring adequate support of logistics and potential mobilization needs, and protecting itself against supplier catastrophe?

modular function such as a minicomputer to be implemented with alternate LSI chip designs (e.g., Intel 8080A vs. AMD 9080A), yet permit the module level function to be completely transparent and amenable to advancing technology. It allows the flexibility to introduce and sustain competition throughout equipment production programs. It also provides an environment compatible with the development of multiple sources.

Rigorous adherence to meeting design-to-cost goals, compatible with Integrated Logistics Support (ILS) throw-away costs, will minimize and potentially eliminate the need to consider the problems associated with Navy procurement and sparing of LSI devices.

The above approach affords the most promise as a general management philosophy for the introduction and continued availability of logistics support spares. In the limited situations where a SAM (Standard Avionic Module) standardization program cannot be implemented, the LSI management problem is made more complex. In cases where these advanced technology microcircuits must be managed at the device level, NAVAIR should (1) make use of form, fit, and function specifications--specify the need, not the solution; and (2) allow some schedule flexibility, that is, trade off schedule for performance--advanced technology solutions to a problem are rarely the quickest solution.

Support/protection requirements can be met by (1) the form, fit, and function philosophy in which an exact copy is not demanded; and (2) establishing a technology data base which is available to contractors such as the cell library and automated design software system that NSA is establishing for selected LSI technologies.

Question #1: How should the Naval Air Systems Command (NAVAIR) facilitate the use of advanced technology microcircuits, while insuring adequate support of logistics and potential mobilization needs, and protecting itself against supplier catastrophe?

Additionally, component standardization activities should be strengthened in this area. A central Naval activity (e.g., NSWC or NAC) should be chartered to:

a. Oversee and fund mask interchange programs.

b. Limit the proliferation of devices.

c. Be a focal point for program offices considering LSI custom usage.

d. Develop a list of required custom LSI devices for the Navy that the commercial semiconductor industry will not produce due to low volume needs.

With the semiconductor industry shifting more and more of their assembly facilities off-shore due to the low labor cost, the Government should be concerned with this development since it could adversely affect any mobilization requirements. Japanese imports (especially memory devices) will also reduce the number of "on-shore" facilities. The aerospace equipment and system houses that are instituting their own semiconductor facilities are helping to lessen this concern. This industrial capacity, in view of the semiconductor technology requirements, will be an essential element in any future mobilization plan, and should be considered and supported as such.

* * *

10. A simplistic response would be to say that NAVAIR should procure enough spares at the early stages of the program to cover the

Question #1: How should the Naval Air Systems Command (NAVAIR) facilitate the use of advanced technology microcircuits, while insuring adequate support of logistics and potential mobilization needs, and protecting itself against supplier catastrophe?

logistic and mobilization needs throughout the life of the system. Although this may be the only feasible approach in certain very low volume high performance or highly secret applications requiring advanced technology microcircuits, it doesn't appear to be the best approach in other situations where the use of advanced technology microcircuits is proposed. Other approaches such as long-term warranties and repair contracts or sparing at a higher level (assembly, etc.) should be considered. If supported at the functional module level, newer technologies could be used when the original is obsoleted (unprocurable). The problem should be addressed at the beginning of a program. The risks involved in using advanced technology microcircuits should be evaluated in respect to the advantages. Guidelines should be established by NAVAIR and applied to all contracts to assure that the risks are minimized and are outweighed by the advantages. A knowledgeable Government body would be used to evaluate and assign risk factors for advanced technologies. In high risk technologies, this body could be used to pass judgement on the advisability and need for specific proposed applications.

* * *

11. NAVAIR can facilitate the use of advanced technology microcircuits (large scale integration (LSI) and very large scale integration (VLSI)) by supporting the development of design tools that will be cost effective and that can be used with confidence by NAVAIR contractors. The design tools should be applicable to technologies that are industry standards today and to future evolving technologies. These design tools will enable NAVAIR to assure adequate support of logistics and mobilization needs by making the design tools available to system and subsystem contractors and by having the devices supplied by multiple semiconductor industry sources. The specific design tools supportive of NAVAIR requirements are:

Question #1: How should the Naval Air Systems Command (NAVAIR) facilitate the use of advanced technology microcircuits, while insuring adequate support of logistics and potential mobilization needs, and protecting itself against supplier catastrophe?

- *Standard cells for Computer-Aided Design*
- *Universal Arrays*

These tools should be developed for the following technologies:

- *PMOS*
- *Bulk CMOS Metal Gate*
- *Bulk CMOS Silicon Gate*
- *CMOS/SOS Silicon Gate*
- *I^2L*
- *Radiation Hardened CMOS/SOS Silicon Gate*

NAVAIR should take the following actions to insure adequate support of logistics, mobilization needs, and protection against supplier catastrophe:

a. Encourage the design of custom LSI to implement functionally partitioned circuitry utilizing existing CAD tools such as those listed above.

b. Stockpile LSI arrays in adequate quantity to meet one to two year use requirements and long-term spare requirements for logistic support.

c. Stockpile mask sets and test program tapes so multiple vendor sourcing can be exercised with quick turnaround.

d. Select industry standard processes currently in widespread use. (Example: CMOS Bulk currently, and CMOS/SOS for future requirements.)

* * *

Question #1: How should the Naval Air Systems Command (NAVAIR) facilitate the use of advanced technology microcircuits, while insuring adequate support of logistics and potential mobilization needs, and protecting itself against supplier catastrophe?

12. *Maximum system advantage and minimal logistics problems can be assured by maximizing the use of advanced technology microcircuits which are members of families of compatible commercial components. The emergence of single-chip microprocessors and microcomputer product families is the manufacturer's answer to minimizing the proliferation of different LSI components and hence the product development cost. Similarly, this tends to maximize the volume of like products and thereby reduce user cost of these devices. The pervasive use of these devices obligates the manufacturer to maintain long-term production commitments both to commercial and military users. As technology improves, more advanced members of the family are developed. However, in order to maintain family compatibility, new members must maintain form, fit, and function (i.e., software) compatibility with prior generation devices.*

NAVAIR should encourage the qualification of selected families of commercial LSI and VLSI products for use in its applications. Qualification should be based on:

a. Existing and planned family functions which have general applicability.

b. Manufacturer capability to produce functions in a circuit technology which is applicable to LSI and VLSI circuits, and which meets military environmental requirements.

c. Strong linkage to a commercial product and computer family to provide comprehensive system and software development tools.

Qualification should not be restricted to one family.

Question #1: How should the Naval Air Systems Command (NAVAIR) facilitate the use of advanced technology microcircuits, while insuring adequate support of logistics and potential mobilization needs, and protecting itself against supplier catastrophe?

NAVAIR and industry would then have a framework whereby the number of devices to be developed and supported could be restricted. This will also encourage the development of multiple sources.

* * *

13. a. Mandate that all bidders for system-development programs perform life cycle cost vs. risk studies in their proposals, based on the expected deployment and spare quantities over the expected life of the system. Consider LSI, hybrid, and printed circuit MSI implementations.

b. Procure all devices expected to be required with one order. Store unused wafers at various locations to avoid the requirement for a second source.

c. Have military production capability in selected (industry standard) technologies. Insist that contractors' design development mask tapes be compatible with MIL-process. Deliver chips GFE.

d. Consider semi-custom approaches before all custom:

(1) Gate arrays/master slice

(2) Programmable functions (microprocessors, PLAs, PROMs, etc.)

* * *

14. In answering the question asked, several assumptions have been made which are based on prior conversations with NAVAIR and other Government agency personnel, and a knowledge of their procurement cycles.

Question #1: How should the Naval Air Systems Command (NAVAIR) facilitate the use of advanced technology microcircuits, while insuring adequate support of logistics and potential mobilization needs, and protecting itself against supplier catastrophe?

a. The basic problem is the low volume of parts required, ranging from a few hundreds to a few tens of thousands. This problem is compounded by the relatively long period of time during which the parts must be available. If millions of parts were required, there would be no problem in obtaining the devices needed.

b. The environmental requirements which the parts must meet are severe and the reliability under these adverse conditions must be very high. Therefore, the cost of quality control and testing is a substantial part of the device cost.

c. In many cases the LSI is part of a complex equipment. As a result, the cost of the LSI chip is not a significant part of the total equipment cost, so the price of the chip is a minor consideration. This is the opposite of many commercial situations.

The best answer to the question seems to be the use of designs owned by NAVAIR, including design rules, mask tooling, and process details. This approach may be accomplished readily by using the Standard Cell approach developed by NSA and NASA, which tends to make the manufacturing process independent of the supplier. The automated design procedures inherent in the approach facilitate the use of advanced technology and circuit techniques.

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15. For multiple reasons, a <u>custom</u> LSI circuit embodying a limited technology should be allowed only when either technical or economic reasons justify its use. The technical constraints would include size, weight, power, etc. Where the above considerations are not justifiable, the use of <u>standard</u> widely accepted LSI and MSI devices should be used.

Question #1: How should the Naval Air Systems Command (NAVAIR) facilitate the use of advanced technology microcircuits, while insuring adequate support of logistics and potential mobilization needs, and protecting itself against supplier catastrophe?

For applications requiring the use of custom LSI devices, general guidelines for use should include projected usage, multiple sources, total quantity buys, and so forth.

An important consideration is the present and projected commercial application of the item, since this arena constitutes the most significant factor in the life of electronic parts.

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16. NAVAIR should specify complex integrated circuits at the functional level and should standardize form, fit, and function here. A replacement part can then be introduced that obsoletes the old part without impacting the using equipment.

NAVAIR should consider the possible use of commercial-type LSI and ways to utilize it within the military environment. The design of circuitry in using equipments that accepts the constraints of commercial LSI would, over the long haul, pay high dividends.

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17. NAVAIR should encourage equipment manufacturers to use QPL and commercial parts where possible. An up-to-date preferred parts list other than QPL listings should be made available to OEMs during the design phase. NAVAIR might consider developing alternate sources for LSI products which are not otherwise available from more than one source.

LSI technologies which are used should be proven processes that are reproducible from more than one semiconductor supplier.

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Question #1: How should the Naval Air Systems Command (NAVAIR) facilitate the use of advanced technology microcircuits, while insuring adequate support of logistics and potential mobilization needs, and protecting itself against supplier catastrophe?

18. a. Specify custom LSI parts replacement on the basis of functional equivalence as the best protection against the possibility of future parts unavailability and technology obsolescence. Functional equivalence is defined as a replacement part having identical electrical and logic characteristics as the original part, and having the same external packaging configuration (e.g., 24-pin DIP) and identical pin assignments. The acceptance of functionally equivalent parts will obviate the need to document the process by which the original parts were made and to re-establish an identical line after a lapsed time of perhaps ten years, during which process materials (resists, solvents, etc.) and equipment (furnaces, etchers, testers) may all have changed.

b. Change procurement policies for replacement parts of custom LSI from yearly purchases to multi-year or lifetime procurement. In the case of custom LSI, annual replacement needs may be on the order of 50 to 100 units which may represent a few wafers for the year. To re-establish a line each year to produce these few wafers is not cost effective.

However, a study may be necessary to determine the effect of shelf life on microelectronic circuits. Little long-term (i.e., 10 year) aging data are available to support the premise that lifetime procurement of replacement parts is feasible.

To minimize the cost of inventorying parts over extended periods of time, it may be advisable to store the LSI chips in wafer form prior to dicing and packaging. However, storage of chips on tape chip carriers offers some distinct advantages over wafer form storage. First, each chip can be extensively tested and only the good units

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retained. Second, the individual chips can be stressed (i.e., temperature cycled) and concurrently tested to detect weaknesses. Third, the tape chip carriers can more easily be shelf tested periodically. Fourth, the tape chip carrier storage saves the cost of packages and packaging while retaining the advantage of automated bonding.

c. Since custom LSI is a non-standard part, it is generally required to undergo qualification testing. Rather than qualify each LSI part, it may be feasible to qualify a fabrication process and an associated set of design rules such that any custom LSI using this process and adhering to these design rules would become qualified. This concept could be extended to include "standard cell libraries" whose use would not require requalification.

d. Make provisions in developmental contracts to provide special incentives for the use of custom LSI where the advantages of doing so will clearly benefit the system in terms of performance, cost, size, or reliability even if the benefits would not be received until subsequent phases of the program (i.e., production or deployment).

At present, there does exist an added cost and risk in the use of custom LSI parts during early phases of system development where the system requirements may not be firm and/or the LSI design may not be verified. Under these circumstances, custom LSI will not be used if there is a choice in implementation. The incentive to use LSI in the system to capture its benefits might be in the form of additional reimbursement for non-recurring cost and additional time in the development schedule.

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e. Consider obtaining agreement among the major military suppliers of custom LSI parts to the form and substance of a data base for fabrication and testing of the parts such that procured custom LSI parts can be transportable without the cost and delay of having to retool the masks or rewrite testing programs.

In many cases the LSI technology is versatile and allows us to provide extremely dense functions at low cost and small size. Therefore, we can use the increased functional content of the chips to perform built-in test, redundant sparing of functions, or other features which enhance system effectiveness and availability.

Recent projections at several conferences show a 30:1 increase in the total number of IC functions produced per year by the semiconductor industry between now and 1985 (from 3×10^{12} to 10^{14}). This dramatic increase will be the result of many new product applications using highly complex LSI chips such as automobile and home electronics which will be supplied in quantities so large that they will dwarf the previous high quantities supplied to applications such as the mainframe computer companies. It is important for us to grow with this technology in our ability to use its rapidly increasing functional content and rapidly decreasing cost per function. The projected benefit of this technology over the period to 1985 will be a 5:1 cost per function decrease, at least a 10:1 increase in function per chip, and resulting benefits of reduced volume, increased reliability, and reduced power.

For the military to keep pace with this rapid evolution and to gain the benefits of this LSI technology, we must (1) reduce the risk of LSI commitment to major programs, and (2) reduce the cost and

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schedule of the LSI chip development. With regard to the risk, we need to sustain credible sources in business. At present, there are companies clearly interested in military LSI business, but these are largely captive IC divisions of major DoD systems manufacturers. They are therefore in the business to sustain the product developments necessary for their systems activities. This is important and does provide a credible source, but leads to the basic proprietary nature of the technologies that these houses provide. There would have to be a profitable business potential with much larger usage of military LSI to promote interest outside of these captive suppliers.

Going back to the projection of a 30:1 increase in the total annual production of IC functions per year by 1985, it is important to realize as well that on single chips, device complexities of over 100,000 transistors will be produced at that time. However, the recent flattening of IC complexity as measured in gates per chip in military systems is an indication that we are not keeping pace with that dramatic growth potential. Coupling that with the realization that there is no new standard logic family of LSI complexity devices foreseen in the future, it is then of concern whether there will be a long-term device technology on which DoD systems can count. We have in the past relied heavily on the standard SSI/MSI families of TTL, STTL, ECL, and CMOS, but can no longer project any more than a slow evolution of new functions being added to those families. Other than the basic microprocessors, their support circuits, and semiconductor memories, there is not evolving a complete family of LSI complexity devices that truly service the needs of high performance sensor processing military equipment.

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With regard to the microprocessors as a solution to this need for custom military circuits, one must realize that although the microprocessors provide low-cost standard functions, they require custom programming which is generally as costly as the custom LSI chip development, and their performance in the end is generally an order of magnitude below that of custom functions realized out of the same circuit technology. Furthermore, the basic microprocessor chip families in high-speed computers comprise generally only 15% to 20% of the total IC count in the computer. For example, a 1553 serial data bus interface will, in general, require more integrated circuit chips than an entire microcomputer built with high technology LSI devices. Therefore, the microprocessors will find many applications in military systems, but will also be restricted from many of the high data rate requirements, and even where they are effectively used, will comprise only a small part of the total IC parts count needed to make a complete system. Therefore, it has generally been accepted that some means of custom LSI will be very important to also reducing the parts count and power of the other support circuits that are unique to the systems and are necessary around the microprocessors where they are used.

We must attack the problem of the inherent risks imposed upon programs in LSI chip development through the unpredictable schedule and cost of the design and fabrication of first devices. There have been many contracts in the areas of LSI technology, but few have gone the full distance of building sufficient devices to characterize their reliability and to learn more about the efficient design of subsequent functions in that technology. Too often we have stopped with a single demonstration vehicle of a particular high-technology approach. It would be more important to have characterized a thousand devices with reliability history

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and with low error rates than to have squeezed out one more nanosecond performance. Much of this may hinge on new utilization of computer-aided design approaches and the development of such approaches as cell libraries and configurable gate arrays. In these cases, only the ultra-high performance or special devices are developed with full hand-crafted design engineering, and the remaining functions employ largely a computer-aided design approach based upon already known circuitry.

The basic procurement of military systems is still such that the risk of LSI utilization is amplified due to the extreme attention during the development cycle of cost-competitive procurement, followed by a rapid schedule-sensitive transition to production. Therefore, during the competitive development period, a contractor is ill-advised to invest his own money, not yet knowing who will be the successful production source, in a technology which yet provides added risk to even being able to demonstrate the system concepts that he is proposing. This is followed then by the rapid transition to production, wherein a contractor is not highly motivated to go back and make changes to the system which will only further delay its entry into production. Profit incentives here to utilize technologies such as LSI to reduce production costs or to improve reliability after a contractor is selected for production would be one alternative; there are probably others.

The basic market for military LSI needs a shot in the arm. If it were viewed as a profitable business outside of the basic systems contractors, then there would be custom LSI capabilities developed and second sources in the industry. Since it may require too large of a step function increase in the total LSI business level in military systems to reach that as a goal, we may instead at first consider means of better

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using the IC fabrication capabilities in most of the major system contractors. In these cases, DoD funding to sponsor common CAD design approaches involving cell libraries and gate arrays, etc., would enhance the sourcing of key LSI devices in future systems and relieve our major dependence on low level SSI/MSI ICs. Parallel programs to fabricate reasonable quantities of devices having major DoD interest would be a correct step in the right direction. For example, contracts to fabricate specific very high performance signal processing components or special military interface circuits would result in key technologies in the systems contractors becoming better known to program managers through extensive device reliability testing. Specifically, it could be recommended that million dollar-plus contracts be let to prove the device reliability of technologies at as many as a half-dozen systems contractors, with some requirement then that makes these device technologies available for outside sale. The availability of these technologies for outside sale will, in certain cases, be of concern because of the competitive nature between the companies. However, in many cases, including our own, there have been sales already directly to other systems contractors involving our most advanced LSI forms.

Finally, with regard to the specific questions in the NAC letter, there is a certain suggestion that LSI implies an increased exposure to supplier catastrophe or device technologies becoming obsolete during the operational life of avionics equipment. I would suggest that perhaps over the long-term life of many systems having support requirements of 10 to 15 years and more, that LSI may <u>not</u> be any more unprocurable over that life than what we currently know as the standard vendor SSI/MSI parts. The reasoning here is that the major growth projected in the IC technology

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is in custom or dedicated LSI and not in the standard SSI/MSI families such as TTL. Thereby, most new products including LSI will be using some form of dedicated or custom LSI; at least they will be using custom programs stored in ROMs or PROMs to control the standard microprocessor devices, and in many cases they will be using custom circuits uniquely designed for special requirements.

The projections show the majority of total IC product complexity to be met in the future with such dedicated or custom parts (exclusive, of course, of the standard RAMs and ROMs). Since we are not identifying a new family of standard high-level functions we thereby see the choice of relying on custom or programmable circuits, or of continuing to fall back on the standard families such as TTL which are already ten years old. To do the latter may be a risk in the ability to procure such devices over the next 15 years.

The strongest recommendation to add some protection to our ability to reprocure devices is probably to base our LSI military technologies on a common CAD design approach which will necessarily tend to result in similar to identical functions being redeveloped in the new technologies and processes that evolve over the years, that in itself provides a usable design documentation for reprocurement.

An examination of what the semiconductor industry and aerospace semiconductor houses are doing that may be applicable to the military-type applications of low to moderate volume with a short design cycle time and low non-recurring cost indicates a proliferation of gate arrays. Potential suppliers are going in different directions with regard to technology and gate array configurations. For example, gate

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arrays have been announced using I^2L, bulk CMOS, SOS CMOS, NMOS, ST^2L, and ECL technologies; in addition, the various gate arrays have a different number of gates (112, 168, 262, 640, 800, etc.) as well as different design rules (fan out, speed, load currents). Several of the gate array technologies utilize processes which are too new to have been stabilized, and modifications can be anticipated.

Selection of an approach using a mature process and standard 5400 Schottky T^2L cells appears to be a good starting point or springboard from which DoD could formulate and steer the direction of LSICs for near-term (and possible long-term) military applications. Without the leadership or direction of a third party, as DoD, industry will continue in a multitude of different directions.

Why select the standard cell/cell array technology? Key reasons are that LST^2L is a mature process and it is a technology that offers the high speed requirement needed in a major number of military systems, as pointed out in the report "Large Scale Integrated Circuits for Military Applications," IDA Paper P-1244, by Glenn W. Preston. A very useful set of SSI and MSI cells have been defined for use in PCB applications. For LSIC applications, the emulating of selected SSI/MSI functions with specific electrical and logic characteristics would allow DoD to specify common characteristics so that interchanging of cell types between different semiconductor establishments would be practical. In effect, DoD would or could be the custodian of the cell library. Custom LSICs would have common factors, as the cell dimensions, geometry of devices (transistors, resistors, and diodes), location of I/O pads, and specified electrical characteristics with compatible design guideline

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rules. The specific interconnect and logic function could be maintained proprietary to a company if so desired. DoD could coordinate the supplying of digital data or 10X reticle masks to different semiconductor houses, thereby enabling them to produce custom LSIC cell arrays.

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19. Wafer storage is the obvious solution.

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20. Current on-going major military programs should be reviewed to determine what commercial types of advanced LSI technology are being used. As an example, a composite microcircuit usage list has been developed on the F-18 Navy program as a result of inputs provided by major F-18 Avionics Parts Control Board members. This list, though not finalized, represents a major portion of the types of LSI being employed. Based on this list, plus similar lists on other major programs, the military would be in an excellent position to select those devices which should receive major attention for documentation under MIL-M-38510. In this way, standards would exist on which industry could bid, thereby opening up the door, through competition, for multi-sourced devices. At the same time a common number would be established whereby military contractors could procure the device. In this way the objectives of the Navy concerns re commonality and multi-sourcing would best be satisfied.

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B. Question #2: How should NAVAIR protect itself from the ever-increasing problem of devices/technologies that become obsolete (unprocurable) during the operational life of avionics equipment?

Highlights:

Following are the predominant suggestions mentioned by the respondents:

- Make life-of-type buys of parts.
- Emphasize functional specifications at the module or assembly level.
- Restrict the use of technologies to those in the mainstream, where a number of companies are committed to the technology for both military and long product cycle commercial applications.
- Establish multiple sources.

Other suggestions included:

- Use of LSI devices which have a firm vendor marketing plan for upward compatible product development.
- Use of bonded wafer storage.
- Communication of LSI needs between Government equipment suppliers and OEMs.

Question #2: How should NAVAIR protect itself from the ever-increasing problem of devices/ technologies that become obsolete (unprocurable) during the operational life of avionics equipment?

- Obtaining of design disclosed information by the Government on LSI so that another reputable manufacturing source can produce the product if needed.

- Development of a viable LSI standardization program.

Industry Replies:

1. Protection against devices/technologies that become obsolete during the operational life of avionics equipment can be overcome through a more conscious effort to communicate between suppliers, OEMs, and government agencies. Given greater visibility of logistics support, needs identified to the prime supplier followed with an annual review to determine both forecast needs and supplier's intentions to fulfill those needs by sustaining production would go a long way to protect against unplanned obsolescence. Similarly, if a supplier intends going out of business on a particular end item, and if he had visibility of its demand to support avionics equipment, proper notification could be afforded to allow "life of type" buys to occur routinely.

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2. a. By restricting the technologies designed into operational equipment.

b. By maximizing modularity of equipment designs so that the necessary technology upgrading can be restricted to the afflicted subsystems (ALUs, memories, multiplexers, etc.)

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Question #2: How should NAVAIR protect itself from the ever-increasing problem of devices/ technologies that become obsolete (unprocurable) during the operational life of avionics equipment?

3. This is a major problem since the military would probably use the same circuits for ten to twenty years. The circuits would certainly be obsolete long before the military stopped using them. Again, the answer to their problem would be for NAVAIR to have their own processing capability.

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4. Concerning obsolescence during the operational life of avionics equipment, with increased use of modularity and multiplex busing in systems, the effect of a changing technology can be accommodated.

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5. Where this protection cannot be guaranteed, the use of a multi-source leading edge technology will provide the best hedge. A strong and coordinated standardization program within the military would go a long way toward a solution to this problem.

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6. Project lifetime buy needs and enter into lifetime buy agreements with the devices stockpiled at a vendor's bonded storage area or at NWSC, Crane.

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7. Navy efforts should be directed to implementing those LSI devices as standards which have a firm vendor marketing plan for upward-compatible product development, and which are intended to functionally replace and enhance the product in present use, at the device level. We are using the technique of selecting functional standards for various classes of processing problems. For example, we use the following microprocessor classes: 8-bit, 16-bit, low-power, and bit slices. Basing present designs on the 8080 and then upgrading to the Z80A or 8085 is a typical example of an upward-compatible technology.

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An alternative to the component level of standardization is to disregard the device implementation for any subassembly function, and require only subassembly level compatibility. It is conceivable over the life cycle of a product that a subassembly can evolve from 100 flatpacks of discrete MSI logic to one or two LSI packages and still remain functionally identical, and/or more powerful, while keeping identical interfaces to the system in which it resides. Specifying page functional equivalence (and not component technology or processes) is by far less expensive and requires less technology forecasting on the military's part, and therefore less risk.

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8. The items discussed in Question 1 apply, namely:

- Life of type buys.
- Planned technology upgrades.
- Multisourcing.

As a final point on this question, we might add that the most unprofitable business for a microcircuit supplier is to build a few hundred or even a few thousand pieces of a device or a technology in which the "life of type" buy was completed several years prior. This situation is almost like "starting from scratch." Considering the facts that (1) this is a frequent and costly occurrence, and (2) that microcircuits represent a small percentage of an overall system procurement, NAVAIR might wish to consider a significant "over-buy" of microcircuits.

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9. We feel the most cost effective, least risk approach is to solve the problem at the assembly level through the use of standard avionic modules (SAM) functionally specified to be technologically

Question #2: How should NAVAIR protect itself from the ever-increasing problem of devices/technologies that become obsolete (unprocurable) during the operational life of avionics equipment?

transparent. The use of form, fit, and function specifications offers the potential to introduce competition and will enable the incorporation of up-to-date LSI device technology (within the SAM) via more cost-competitive functional solutions to the SAM function.

Quasi-standard and custom LSI device procurement problems can be overcome through the use of life cycle buys at a point when procurability becomes a potential problem. The procurement of total projected needs in wafer form is potentially a very cost effective solution. Requiring established dual sourcing capability would also afford a certain degree of protection.

The solution to commercial LSI device/technology obsolescence lies in the use of form, fit, and function specifications and the resulting technology transparency of the design.

Some progress in the practical side of this problem (mechanical structure, power supplies, etc.) is being made with the SEM approach and the quasi-standard 5-volt supply which can be used for T^2L, NMOS, CMOS, and I^2L. Thus, although exact replacements may not be available, functional equivalents should be available.

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10. It would appear that the only practical way for NAVAIR to protect itself from the obsolete devices/technologies problem is to minimize the effect of such obsolescence. In some applications, the stocking of a lifetime of spares would be the best answer. In others, interchangeability at some modular level would be the best answer. In instances where custom devices have been designed using standard cell libraries and CAD programs developed by the Government, a compatible process capability

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should be maintained. When industry would normally discontinue this process, the Government could subsidize a number of manufacturers (on a competitive bid basis) to maintain such processing. If industry was not interested, the Government could use its own processing facilities to build spares.

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11. NAVAIR can protect itself from the ever-increasing problems of devices/technologies that become obsolete during the operating life of avionics equipment by selecting technologies that are mainstream technologies and are supported by major semiconductor suppliers committed to exploitation of these technologies in the industrial and commercial marketplace. The success of a semiconductor supplier in building a large commercial catalog of parts and in stimulating a host of second source suppliers will assure longevity. In a successful technology, evolutionary transitions occur which lengthen the life of the technology. An example of evolutionary transitions is the shift in CMOS technology from metal gate to silicon gate to sapphire substrates. This evolutionary progression should be welcomed since it will extend the use of the basic logic technology for five to ten years or longer, and will not impact equipment designs as severely as might a more basic technological shift.

Avionics equipment designs should be implemented in broad-based technologies at the beginning of their production cycle in the semiconductor industry. Examples of technology to be considered for current applications are bulk-CMOS silicon gate, CMOS/SOS, I^2L, and CCD; as opposed to considering RTL, DTL, T^2L, and other increasingly-obsolete technologies which may still be in production at some vendors and which are used extensively in operational military systems designed a decade ago.

Question #2: How should NAVAIR protect itself from the ever-increasing problem of devices/ technologies that become obsolete (unprocurable) during the operational life of avionics equipment?

Designs should be evolved encouraging system partition on a functional basis so that new technologies can be introduced in a plug compatible form at the module level. Examples would be random access memory modules which can evolve from T^2L to NMOS technologies on a plug compatible basis.

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12. Where highly specialized or particularly unusual circuit functions are required, additional volumes of parts should be procured and stored for future use. This approach assures the least cost for providing a back-up reserve for future needs due to the batch processing and production techniques employed by the semiconductor manufacturer.

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13. a. Process, procure, and store all parts needed for the life of the equipment.

b. Buy from vendors who stress upward compatibility for such products at microprocessors and memories.

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14. The reason that devices become obsolete is simply that they become unprofitable to manufacture. If the processes and the designs belonged to NAVAIR, the procurement would always be possible, although perhaps expensive. An alternative would be to procure all devices at once and stockpile them. When the stockpile ran out, a redesign would become necessary. However, NAVAIR would be able to purchase initially in quantities large enough to attract suppliers, which would result in attractive prices.

A second alternative would be to use a technology which is less likely to become obsolete. One example is CMOS/SOS, which is not

Question #2: How should NAVAIR protect itself from the ever-increasing problem of devices/ technologies that become obsolete (unprocurable) during the operational life of avionics equipment?

presently used to any extent commercially, but is supported by a great many system houses for internal use. While SOS chips are very expensive by commercial standards, they are not an important part of the cost of the systems in which they are used. The existence of a relatively large number of firms which have committed this technology to military and commercial systems that can be expected to have long life spans practically assures that the technology will be available for a reasonable length of time.

The profit is not in the chips, but in the systems which use them. Therefore, there is much less incentive to abandon the technology for another which would require a very expensive system redesign.

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15. For custom LSI circuitry, limited avenues exist for insuring long-term availability of parts. Initially, development of multiple sources capable of satisfying the device function should be established. Normally this will require some assurance on the manufacturer's behalf that these functions may ultimately be effective in the commercial market. A special protection could also include design disclosure documentation of sufficient detail to insure thay any reputable company could produce the device even after the original company has lost interest due to economic considerations.

Stockpiling to cover the total projected usage of the devices is an expected approach but suffers from the aging effects of stored devices, the storage costs, investment dollars, inventory taxes, and the vagaries of predictions regarding needs.

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Question #2: How should NAVAIR protect itself from the ever-increasing problem of devices/ technologies that become obsolete (unprocurable) during the operational life of avionics equipment?

16. NAVAIR should issue a written document covering standard LSI modules, one provision of which could be a requirement for notification prior to ceasing production on a given module. NAVAIR could thus stockpile adequate replacement modules to last the lifetime of using equipments.

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17. Parts which are incorporated into new designs should be manufactured with LSI processes which are mature and will not be obsoleted soon. These processes should be manufactured by more than one semiconductor supplier. In the event that a product is to be obsoleted, detailed design and process data can be obtained and retained in bonded storage.

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18. No comment.

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19. Wafer storage is the obvious solution.

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20. The question implies that this occurs on a frequent basis. There are many factors involved in the selection of parts, and it is very difficult to isolate any single item as the cause for selection of very specialized parts. To minimize the risk of implementing parts into a design which later becomes non-procurable, minimum requirements should be established for equipments at the beginning of the program and packaging restrictions should be as reasonable as possible. This will help avoid use of specialized components which have a high tendency to become obsolete, particularly when business is expansive. Unfortunately, with miniaturization we continuously keep asking for more and more functions within less space, resulting in less use of standard functions.

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C. Question #3: Faced with an ever-decreasing market life cycle for semiconductor devices/technologies, how are the commercial/industrial producers/customers dealing or going to deal with device obsolescence?

Highlights:

The following items were the predominant answers given to this problem:

- Functional partitioning and modularization (the most frequent response).
- Shorter product life cycle.
- Strong internal standardization program.
- Plan for product technology upgrades.
- In-house LSI capability.

Industry Replies:

1. It is our opinion that with LSI we have a much different situation (not nearly as critical) than we did in discrete products. By this we mean that within LSI there will be a fairly limited number of technologies, well understood, fully developed, and in most cases readily available. So, even if a particular product were to be deactivated for a period of time (not produced) it would be fairly easy to reactivate the technology, specific device masks, and fabrication techniques to respond to a repeat demand after a fair amount of time has lapsed.

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2. In the commercial sector, technological obsolescence is being met by simply shortening the product life cycle. Just try to buy

Question #3: Faced with an ever-decreasing market life cycle for semiconductor devices/ technologies, how are the commercial/industrial producers/customers dealing or going to deal with device obsolescence?

a spare for a ten-year old washing machine. I believe that it would be cost effective for military electronic equipment also to reduce the operational life cycle from an average of twenty years to a ten-year period, which corresponds more closely to the major technology cycles.

* * *

3. Device obsolescence in the commercial area will certainly take place in a three to six-year time frame. The commercial area will need to continually update their circuits and systems with new parts of greater complexity which offer more functions in the same chip area, or redesigning the same circuit functions into a smaller chip, which means that the new design should offer a cost-savings approach. This has been the normal evolution of products in the commercial semiconductor field.

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4. The answer to device obsolescence in connection with commercial and industrial customers is out of my direct experience, but from my observations the equipment has been becoming obsolete as fast or faster than the componentry therein (i.e., the pocket calculator). Additionally, from the financial reports and business articles in recent years, some commercial firms have not coped with this very well.

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5. We have a strong internal standardization program which requires multiple sourcing, thereby increasing the probability that we have selected a technology which will have maximum life cycle.

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6. Redesign the electronic assemblies as required to meet the necessary functional requirements with current state-of-the-art devices. A cost incentive for effective redesign could be implemented. Also, close liaison between the IC industry and assembly suppliers can forecast

Question #3: Faced with an ever-decreasing market life cycle for semiconductor devices/technologies, how are the commercial/industrial producers/customers dealing or going to deal with device obsolescence?

industry trends early so that the true impact can be evaluated and corrective action may be initiated well in advance of an IC vendor's actual change or decision to no longer supply the device.

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7. We recommend that the Navy modify its focus away from devices, and toward the page, card, or box level. By specifying functions and performance at a level beyond the device level, the Navy can purchase functionally equivalent pages of "black boxes" independent of the component technology upon which they are based.

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8. Commercial/industrial users of microcircuits have significantly shorter product development cycles as well as product life cycles. They also plan for product technology upgrades within the product life.

* * *

9. Device obsolescence in the commercial/industrial equipment is more readily accepted as a way of doing business than it is in the military world. It must be remembered that the commercial/industrial producers/customers direct device obsolescence through their economic purchasing power and that the semiconductor industry only follows their wishes. The commercial market "demand" brought on the LSI revolution. The market life cycle of these LSI devices will be a function of market demand. Equipment manufacturers will be developing their own, if not Navy, standard functional assemblies to allow masking of LSI technological evolution in LSI technology. This approach affords the greatest potential for technological transparency. In many areas, no attempt will be made to prevent obsolescence. In some areas an upward/downward compatible philosophy will be attempted. An example might be the automobile engine controllers being introduced, in which features may be added or improvements made, but where a controller for a 1985 automobile might be

Question #3: Faced with an ever-decreasing market life cycle for semiconductor devices/technologies, how are the commercial/industrial producers/customers dealing or going to deal with device obsolescence?

required to control a 1980 car. The upgrade of the 8080 family to an 8048 is an example of the philosophy. Make a single chip do the function of several chips but keep the overall function performed compatible.

* * *

10. Device and/or technology obsolescence in the commercial/industrial market is mostly a matter of little concern to the device manufacturers themselves. The dilemma for the end user created by the sudden disappearance of a device is largely relieved by "replacement houses" such as Sprague, Sylvania, Motorola-HEP, RCA-SK, plus numerous other small name houses mainly handling devices from any place they can obtain them to cover the customer's needs. Replacements may require "cuts and jumpers" or replacement of an assembly, or both. New improved products often replace older models which are discarded rather than repaired.

Extremely complex devices are not being covered unless the users (manufacturers) undertake the sourcing themselves, either by developing in-house facilities or by contracting with custom houses to provide the device (assuming the end product justifies continuing).

There appears to be some evidence that large users sometimes do this initially to protect proprietary information. In doing so they can also procure sufficient quantities to protect their needs. Many "house numbers" fall into this category. When the equipment manufacturer's supplies are exhausted (assuming they no longer manufacture the product), the customer is pretty much out in the cold.

* * *

11. Commercial/industrial producers/customers are facing the ever-decreasing market life cycle for semiconductor devices/technologies

Question #3: Faced with an ever-decreasing market life cycle for semiconductor devices/technologies, how are the commercial/industrial producers/customers dealing or going to deal with device obsolescence?

by going to shorter system design cycles and faster product obsolescence, and also by designing system architectures that allow upgrading of modules at the subsystem level to incorporate new devices and technologies. For example, memory subsystem designs have evolved from the use of 1K RAMs and are now progressing to 16K and 64K memories without requiring complete system revision.

In addition to the upgrading of memory systems by the use of higher density memory devices, the system designers are making expanded use of architectures that include programmability by the use of microprocessor based designs and ROM logic matrices. The flexibility afforded by designing systems so that they can be modified to incorporate improved algorithms and additional functions results in prolonged equipment usefulness and deals with device obsolescence in a positive fashion.

However, most commercial/industrial producers/customers have significantly higher unit volume requirements than are characteristic of most military programs. This higher unit volume allows an earlier transition to the new technologies since the system redesign cost penalty is spread over many more units. Military agencies will therefore have to look at the use of system architectures that allow system performance upgrading capability. Such upgrading capability can be built into systems by the use of an initial design which incorporates devices that provide "overkill" capability for the requirement at hand. In the long run, however, such a design will allow the equipment to evolve to meet expanding requirements. One example of such an approach is the development of a bit-slice microprocessor in the CMOS/SOS technology that can be configured into processors with 8, 16, 24, 32-bit, or even longer word lengths. In addition to the flexibility of word length, these devices can be operated at speeds from static operation to clock rates greater than 10 MHz. The

Question #3: Faced with an ever-decreasing market life cycle for semiconductor devices/technologies, how are the commercial/industrial producers/customers dealing or going to deal with device obsolescence?

design also allows for the processor to be used with Special Function Devices such as a high speed multiplier or a fast Fourier transform circuit. The ability to operate such CMOS systems over a power supply range from 5 to 15 volts permits satisfying a range of power consumption and speed requirements and interfacing with a variety of non-CMOS peripheral circuits.

* * *

12. With the pervasiveness of electronics continuing to expand into new fields, we envision at least two types of system requirements. One is the innovator whose objective is to get to market quickly with a product which by design will have a relatively short life cycle; second is the user who has equipment complexities, capital investment, and reliability requirements that dictate that he select technologies which will drive longer life cycles by commitments. An example of the first case is TV games, and of the second is communications. Since commercial/industrial producers are the volume consumers in today's market, the military must be aware of the commercial user who has similar objectives, and utilize that business base and/or make decisions which will provide the commitments to dictate life cycle. For example, Minuteman ICs have been in production for more than ten years.

* * *

13. a. Really large users make their own ICs. They then choose when to stop production.

b. Design for form-fit-function, then replace old technology with a chip which is functionally (timing, voltage, current, etc.) acceptable.

Question #3: Faced with an ever-decreasing market life cycle for semiconductor devices/technologies, how are the commercial/industrial producers/customers dealing or going to deal with device obsolescence?

c. Producers of limited production items find it easy to live with changing IC technology because they issue new models each year if necessary.

d. Make all parts you need prior to shutting down an IC technology line.

e. Plan for upward compatibility (i.e., microprocessor software).

f. Stay with proven technologies.

* * *

14. By paying dearly for the devices or redesigning. Generally commercial/industrial customers do not require MIL-specification devices, therefore, devices are available in small quantities for a much longer time. As long as there is a need for quantities of devices, although they may be technologically obsolete, someone will manufacture them.

* * *

15. We use military grade parts exclusively, and therefore cannot knowledgeably address the question exactly. The inferred problem does extend to users of military grade parts, however, and is worthy of comment.

Considering the long development cycles and the myopia regarding expected life, it is almost impossible to design and build military systems without spanning several semiconductor technology life cycles.

It is observed that this problem is reduced by continuing to introduce improved hardware segments embodying the current technologies

Question #3: Faced with an ever-decreasing market life cycle for semiconductor devices/technologies, how are the commercial/industrial producers/customers dealing or going to deal with device obsolescence?

(i.e., replacement of modules or subsystems which are form-fit-function interchangeable with older items). This implies continuing design throughout the life of the product.

* * *

16. No comment.

* * *

17. Many designs can be partitioned such that critical parts can be replaced with products from new processes with a minimal amount of redesign. The ultimate limits of the process characteristics are not designed to in most cases; this makes replacement with a different technology impossible.

* * *

18. No comment.

* * *

19. Wafer storage is the solution.

* * *

20. Employ as much standard hardware as possible using custom LSI/hybrid devices only where essential to meet space/weight/performance considerations. In this way the possibility of obsolescence will be minimized. Where device obsolescence does occur it will, as in the past, have to be addressed on an individual basis.

* * *

D. Question #4: How should complex LSI devices be specified to insure adequate performance, and assure quality and reliability?

Highlights:

There was a degree of consensus on the following suggestions:

- Place more emphasis on functional device specifications and testing (at the device terminals), not on internal architectural requirements.
- Qualification should emphasize device family and process certification.
- LSI devices should be stressed electrically to augment visual inspection.
- Specify reliability and testing means.
- Make provisions to include LSI devices under MIL-M-38510.

Industry Replies:

1. Part of the answer to this question resides in the method of fabrication. It is our opinion that during fabrication, a great deal of attention should be directed to verification of the functionality of the basic building blocks that are utilized in each LSI circuit. Use of test patterns on the wafer through fabrication steps will give assurance that the target is being or has been met for each constituent part of the circuit. Once this determination has been made, the die should be packaged, and power exercised followed by similar component verification tests

Question #4: How should complex LSI devices be specified to insure adequate performance, and assure quality and reliability?

to determine degradation effects, if any. Provide a reasonable amount of package integrity tests to assure a match of die and package. These having been met will provide a quality product with the attendant reliability realized.

* * *

2. By circuit diagram, truth table, or transfer function, dynamic and static circuit specifications over temperature range, test programs, and pin-out.

* * *

3. No comment.

* * *

4. Specifications should be left to the manufacturer and first user.

* * *

5. Use the existing system, coordinating through DESC. If the device is a custom LSI, prepare a source control drawing and coordinate performance requirements, screening, and quality requirements with users and manufacturers.

* * *

6. It will be necessary to include LSI devices under MIL-M-38510 coverage, but it is necessary to keep the electrical performance requirements specified as maximum and minimum rather than typical. Also, there is a need for industry and Government agreement on standard testing approaches and reliability enhancement techniques and methods.

* * *

7. From the viewpoint of microprocessor (high function) components, it is impractical to specify "delay paths," or gate-level reactions and performance. As an alternative, the device may be tested by subdivision of its functional elements (that is, registers, Arithmetic

Logic Unit, instruction decoder, etc.) Each block would be exercised from the level of simplicity to the level of complexity, by using the device's own instruction set to stimulate each area. Only after one functional block has been tested could it be used as a performance "window" for a subsequent block. The sum of these element tests would equal a full functional test.

Performance testing simply exercises the functional block or blocks (using the appropriate area of the program developed previously) to stimulate and cause the delay of interest to occur, and thus be measured. This test is repeated for the voltage extremes, and over the military temperature range of -55°C to +125°C junction temperature.

The results of this testing yield a procurement specification which reflects performance testing at the required junction temperatures.

Static input/output terminal parameters of complex LSI devices should be specified to minimum acceptable limits over the device junction temperature range of interest. Specifically, parameter limits should be specified at the device junction temperatures of -55°C, 25°C, and 125°C for general avionics applications.

The dynamic performance characteristics of complex logic type LSI devices should be specified for maximum acceptable limits at 25°C device junction temperature at specified loading conditions. These limits should be set close to the delays measured on a realistic sampling of production lots (say 5 to 10). The optimum setting of these limits should be set by the trade-off of yield and cost. It should be necessary to specify only selected, easily testable paths through the LSI device. Similar limits on the selected paths should be determined for the extremes of junction temperature of interest.

Question #4: How should complex LSI devices be specified to insure adequate performance, and assure quality and reliability?

The above specifications should be imposed as follows: 100% screening for static terminal parameters at three junction temperatures, 100% screening for dynamic performance at 25°C junction temperature, and sample screening of dynamic performance at junction temperature extremes.

The major changes that should be incorporated to insure the quality and reliability of complex LSI devices are:

a. Develop a means of stressing the device electrically, to augment the use of a pre-encapsulated visual examination. A gross visual inspection, while being adequate for gross problems such as bond integrity and contamination, cannot reveal subtle defects that an electrical stress would identify.

b. Place more emphasis on functional testing and a high-stress static burn-in of the device.

* * *

8. There is no simple answer to this question. The answer depends on many factors such as the application, the circuit type, and the economics of the situation.

For example, for those applications which require the highest degree of reliability (such as strategic systems), baselining might be the answer. However, for custom LSI circuits in a less than strategic environment, a combination of process controls plus a parametric and functional part specification which meet the system needs (and no more) might be the best choice. For standard LSI circuits, such as memory and microprocessors, present MIL-M-38510 or equivalent specifications are more than adequate. In fact, some rethinking of MIL-STD-883 and MIL-M-38510 in light of the LSI needs might be in order. This is especially true in the area of visual criteria.

* * *

Question #4: How should complex LSI devices be specified to insure adequate performance, and assure quality and reliability?

9. LSI specifications should reflect terminal performance requirements, not internal architectural requirements. Knowledge of the internal workings of an LSI such as that necessary to do single gate fault testing may become less important as a test philosophy for LSI evolves. It is already prohibitively costly in some cases to test an LSI exhaustively. As devices increase in complexity to VLSI, terminal performance testing/specifications (that is, testing for the function required in a specific application) may be the only practical test method.

As microcircuit complexity increases, it becomes more difficult to perform cost effective quality and reliability tests (e.g., visual inspection, complete 100% electrical, etc.) New quality and reliability tests should be investigated and implemented into the military specification system, MIL-M-38510/MIL-STD-883 (e.g., as High Temperature Acceleration Test, Guard Band Testing at above rated voltages). A study is needed in the effectiveness of static burn-in vs. dynamic burn-in for LSI devices.

* * *

10. The principal concerns of the user are:

a. Functionality (truth table and input/output characteristics)

b. Speed

c. Reliability

Items a and b can be specified, whereas item c requires both a history of the quality of the specified vendor and some shake/bake/life testing which may be possible to be specified to a limited extent.

Question #4: How should complex LSI devices be specified to insure adequate performance, and assure quality and reliability?

In general, as device complexity increases, each manufacturer of a given device must develop his own "worst case" electrical tests for his particular die geometry, which cannot be specified by the user.

Also, as device complexity increases, some form of electrical testing must be used to replace at least some of the visual inspections. Government on-site verification of quality procedures at the facilities of device manufacturers could replace some details in specifying quality procedures, and also reduce the cost of Incoming Inspection test equipment at the user site, which becomes very expensive for complex and highly specialized devices.

* * *

11. Current practice is to develop MIL-M-38510 data sheets for catalogue-type LSI devices. This approach, together with the use of responsible vendors, assures quality and reliability. However, this approach impedes both the early introduction of new LSI devices into system applications and the development of custom LSI devices.

The long and arduous effort to generate MIL-M-38510 data sheets needs to be tailored so that the cycle for approval formalization can be reduced to a minimum. Custom LSI devices need to be qualified by a combination of family-based history and production line certification instead of the present need to qualify each type in the family. This is particularly important to military programs having low volume requirements, where the cost of parts qualification can seriously impact equipment cost.

* * *

12. Complex LSI and VLSI circuits must be specified in a way that will insure their function under operating conditions. Added tests should then be selected to exercise the part as much as practical, which will be a tradeoff of cost/test time vs. statistical probability of failure

(not practical to test all structures and all possible failure modes). For optimum quality and reliability performance, make technology selections where quality and reliability are built into the product utilizing processes that have been or will have been in use for one to two years and where in-process controls can be utilized to monitor the operation.

The tendency to demand advances in circuit speed as part of new LSI device developments should be suppressed. Emphasis should be placed on achieving the appropriate level of integration necessary to satisfy natural system or subsystem functional partitions. Once the LSI device is developed, then process improvements can be defined which can, through normal evolution, improve function speed if required. This approach is more consistent with that followed by commercial/industrial organizations when introducing LSI/VLSI functions into products.

* * *

13. a. Test at the I/O level only. Qualify a process (process and design rules such as oxide thicknesses - minimum line separation), not each device. Insist on being informed when design rules or processes are altered.

b. Burn-in and lot traceability are of questionable use and should be eliminated. 100% testing of MIL-LSI devices should be done.

* * *

14. No comment.

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15. Complex custom LSI devices should be specified as a system with all necessary functional requirements included. Any attempt to specify detailed information (i.e., technology, topology, etc.) will unnecessarily restrict potential sources.

Question #4: How should complex LSI devices be specified to insure adequate performance, and assure quality and reliability?

Reliability, being inherent to the design, should be one of the normal functional requirements stated in the specification and demonstrated during qualification. Quality assurance requirements should be carefully selected to insure that reliability and all other requirements are being met on a continuing basis.

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16. No comment.

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17. Performance can be specified by defining the I/O characteristics in detail, specifying timing information, and including logic simulation/truth table information.

* * *

18. No comment.

* * *

19. The simulation programs written to define system performance should be the basis for specifying LSI component performance in the form of a source program tape which exercises all functions, but not necessarily every step in a truth table.

Quality and reliability are satisfactorily covered by MIL-M-38510 and MIL-STD-883 plus programs in progress at RADC/RBRM to upgrade these documents for LSI.

* * *

20. The devices should be completely characterized, as was done by RADC/USAF on the Intel 8080A covered by MIL-M-38510/420. Concurrent with such efforts, associated hardware should also be developed. In the case of the 8080 microprocessor, the associated interface circuits also require military documentation, but this effort has lagged the development of the /420 specification.

* * *

E. Question #5: How can LSI device qualification and requalification be accomplished at reasonable costs?

Highlights:

The following items predominate the answers provided to this question:

- Qualify and monitor the vendor's process.
- Qualify a library of standard cells and design rules used in a computer-aided design system.

Industry Replies:

1. In our opinion, the rules which have been written governing the testing of limited usage (usually expensive) integrated circuits, now included in MIL-M-38510, should certainly be examined as candidates for application to LSI qualification and requalification to achieve what is termed "reasonable cost." The determination could be made as to the applicability of this suggested sequence of test and then modify segments of it to fit each situation. It is a fact that we are faced with a whole new ball game and the brain trust of the industry and government should be brought into play to work out the details of this question. Presently there are organized engineering committees within JEDEC of EIA addressing this question, and we're sure they would be responsive to a call for assistance to evolve a cost effective answer.

* * *

2. Qualify generically, utilizing design and construction analysis to assure process identity.

* * *

Question #5: How can LSI device qualification and requalification be accomplished at reasonable costs?

3. This would be a difficult thing for NAVAIR to do since their volumes would be small. New designs would require new testing set-ups and procedures specifically geared toward their circuits. This means quite a bit of money to set up the testing facilities for a small number of parts. It might be possible to requalify parts by using "similarity" arguments. This approach would allow then to use existing test set-ups to test the newer parts. However, this approach would depend upon how different the new parts are.

* * *

4. With understanding that an LSI device over 10,000 equivalent circuit elements is not 10,000 times more likely to fail than a single component; this too can be accommodated between the manufacturer and user. The use of test patterns to control devices that are closely related process-wise can also help requalification.

* * *

5. Use GIDEP to disseminate qualification test data information to industry. Make this a contractual requirement.

* * *

6. Use a sliding or inverse approach. That is, qualify the more costly devices less often and with fewer samples per submission. This requires an acceptance of a somewhat higher user risk and also requires vendor integrity on a commitment to not change his device in any manner which will affect performance or reliability. It would also be necessary for any contemplated changes to be thoroughly evaluated for actual impact.

* * *

7. When electrically testing any LSI device for performance characterizations, a considerable non-recurring effort is expended in initial device familiarization, test programming, and test debug. Recurring costs are incurred in the actual testing of the device and accumulation and analysis of data.

Question #5: How can LSI device qualification and requalification be accomplished at reasonable costs?

By committing to using large-scale LSI general purpose test equipment, the initial non-recurring cost is generated and saved in test software routines. By utilizing this approach, requalification from an electrical/performance viewpoint is relatively inexpensive. All that is involved is to reload the test equipment with the test software (via magnetic tape, disk, etc.) written earlier, and re-test the devices. The accumulation and evaluation of test results will be a recurring expense; however, this is relatively small compared to the initial program generation and debug. Without this approach, special purpose test equipment would be built for each new device--a very costly and time-consuming approach.

In terms of environmental qualification, the most effective way to qualify and requalify is to:

a. Qualify a vendor's process (i.e., NMOS, bipolar, ECL).

b. Qualify a product of greatest complexity within that process.

c. Monitor the vendor for process changes and quality controls; and when the vendor changes his process, requalify his manufacturing line.

* * *

8. The general consensus is that wherever possible, NAVAIR should rely more heavily on process, device, and manufacturer's qualification rather than lot qualification.

* * *

9. Three categories of devices should be considered: (1) commercial LSI, (2) quasi-standard, and (3) custom. For the high volume commercial LSI such as the 8080, the qualification test cost is not unreasonable when

Question #5: How can LSI device qualification and requalification be accomplished at reasonable costs?

the number of devices used is considered. These costs could be reduced by insuring that MIL-M-38510 slash sheet parametric specifications reflect the existing capability of several suppliers.

Qualification at the assembly level will preclude very costly specification preparation and performance testing for quasi-standard and custom devices. Manufacturer control of materials, processes, and "build" documentation" will result in repeatable LSI devices. For quasi-standard LSI or full custom LSI, the use of process coupons or TEGs has been suggested. While these do provide process tracking, they do not provide the overall design, process, and packaging confidence testing that is needed. The use of standard cell libraries or other design automation aids which could be "qualified" in some manner is a possible approach for the generic or full custom devices.

* * *

10. After examining the device manufacturer's test and quality procedures and schedules, a determination may be made by the user and government representatives as to the adequacy of these controls, and improvements possibly suggested.

After this is accomplished, generic qualification data, taken at reasonable intervals and with occasional monitoring by user and/or government personnel, and with "hard copy" data available, should satisfy the requirement of reasonable quality assurance data.

Since custom LSI normally has very limited applications and is supplied to a single end item manufacturer, the part history during the end item assembly, test, and field operation could be collected and used to supplement the requalification requirements. The failure data generated at device burn-in and end item or system burn-in would provide early warning of possible pending part problems.

* * *

Question #5: How can LSI device qualification and requalification be accomplished at reasonable costs?

11. LSI device qualification should be approached on a family basis so that each of several device types using the same production technology can be maintained in qualified status so long as the production line is actively building a few types from the family. Requalification should be required only when a production line has been discontinued or transferred.

When a CAD approach is used (for example, standard cells or universal arrays), the documentation (including line qualification devices) can be distributed to multiple vendors and requalification can easily be obtained at minimum cost.

Another way to reduce LSI qualification cost is to base LSI designs on the use of standard cells or universal arrays that have been qualified on previous programs. Changes in the interconnections of such approved cells are the only change made in revising the function being performed. This approach will reduce the cost of qualification of custom LSI families. Since a major portion of qualification cost is associated with the cost of the devices used in testing, the elimination or reduction in qualification testing on the basis of similarity within the family of devices generated from a standard cell library would result in substantial time and cost savings.

* * *

12. Initial qualification tests can be performed using conventional methods except where complexities may dictate electrical tests that are more functionally oriented toward end use. Requalification is not as effective as line monitoring through an effective process control system unless major design changes occur. Then careful examination should be made to determine if requalification is required.

* * *

13. a. Qualify only processes.

Question #5: How can LSI device qualification and requalification be accomplished at reasonable costs?

b. Eliminate the requalification problem by procurement of all needed devices early in the program.

c. Let industry continue to qualify devices under standards set and supervised by the military.

* * *

14. Elimination of MIL-M-38510 except for devices purchased in LARGE quantities might help. This is a very expensive procedure. It might be better to qualify the finished equipment rather than the individual parts.

* * *

15. Qualification of some type is performed by the manufacturer prior to introduction of a device technology into the marketplace as economic insurance. Characterization of an individual part type within the technology is a refinement applied to the unique part. The knowledge and data which is generated from these assessments should normally be sufficient to satisfy all normal qualification requirements.

Qualification and requalification should take maximum advantage of those tests which a manufacturer naturally performs for his own economic self-protection. This requires a more astute assessment on the part of the user, but undoubtedly reduces overall costs.

* * *

16. No comment.

* * *

17. Utilization of the supplier's standard test conditions and performance requirements will reduce the non-recurring test costs. Use can be made of test data on similar parts/processes to satisfy requirements for environmental tests.

* * *

Question #5: How can LSI device qualification and requalification be accomplished at reasonable costs?

18. No comment.

* * *

19. No comment.

* * *

20. This was being addressed by RADC/USAF during development of the MIL-M-38510/420 specification. Chip testing was being considered as a tradeoff for the pre-cap visual inspection required by MIL-STD-883, Method 5004, due to the complexity of the device. RADC/USAF should be queried to determine what conclusions were reached in their 1975-1977 studies regarding tests/cost tradeoffs.

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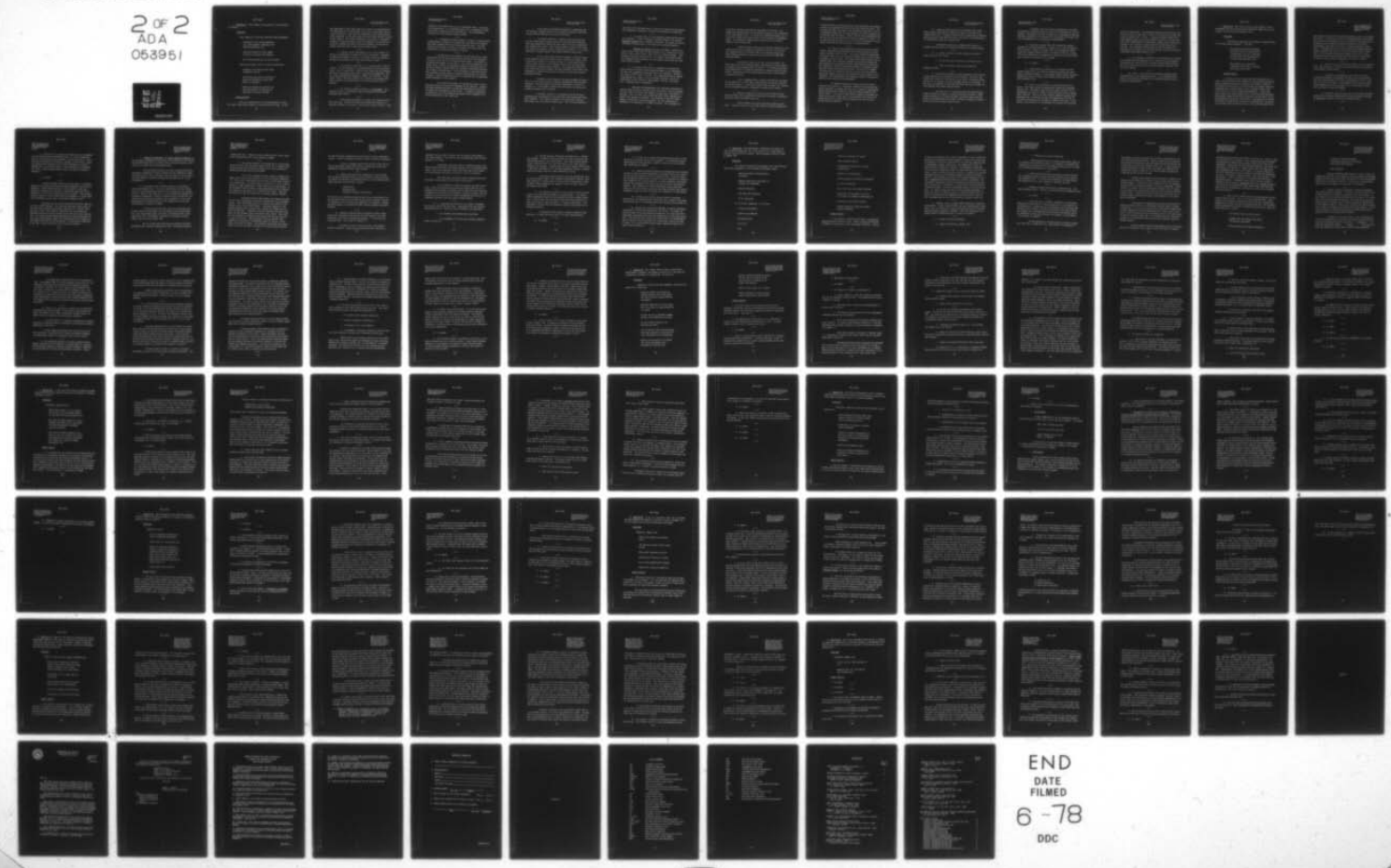

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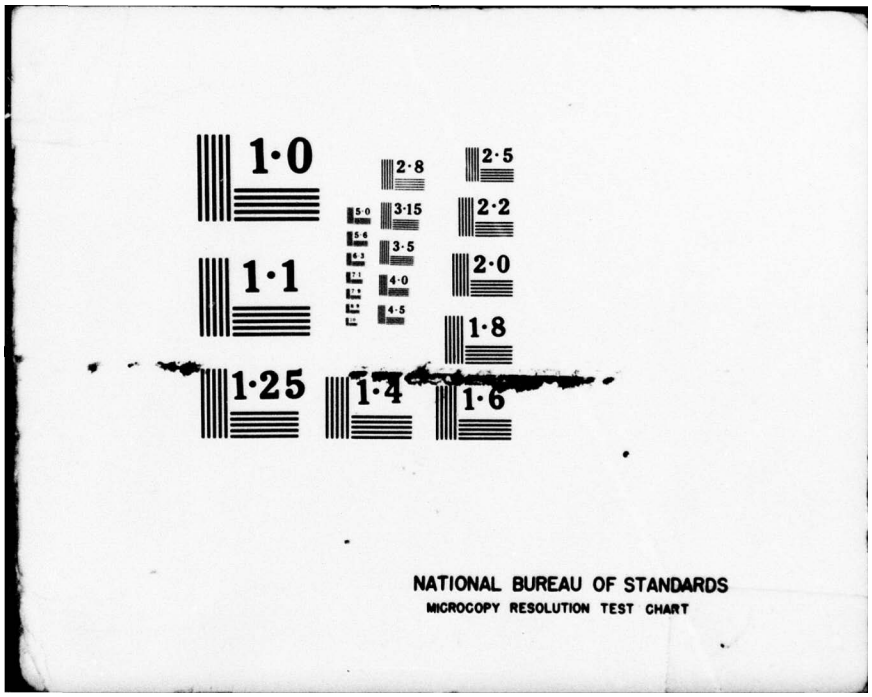
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F. Question #6: Please comment on the problem of testing complex LSI devices.

Highlights:

These suggestions found some concurrence among respondents:

- Standardize on LSI testing approaches, e.g., test equipment, interfaces, test software translators, etc.
- Judiciously select a critical number and type of functional test patterns.
- Build testing capability into chip circuitry.

Significant problems cited in LSI device testing were:

- Frequently, two vendors are not really "transparent" sources.
- The non-recurring costs for writing LSI device test programs can range from 6 months to 2 man-years.
- Vendor test programs are peculiar to a given test machine, and they must be translated to the user's machine.

Industry Replies:

1. If we as an industry were to test every function of every LSI circuit, there would probably be very few delivered on time. If they

Question #6: Please comment on the problem of testing complex LSI devices.

were deliverable on time, they would cost so much no one would want them. The problem with LSI circuits really is the users of them rather than the circuits themselves. Most users are accustomed to using single function simple components, testing them extensively, and finding industry receptive to this approach. The social environment of the business is components-oriented, not systems-oriented. Until our industry can be educated into living in a systems world and its associated problems, testing will be complex, deliveries will be long, and costs will be high.

* * *

2. Restrict pin-out terminations to 60 I/O and a total of 64. Utilize pin multiplexing to achieve this limit if necessary. Generation of complex test programs in itself is no problem, but the development of automatic test generation from truth tables should be funded.

* * *

3. The question is well put! It is very difficult to test LSI circuits. The first problem to be encountered would be the test program itself. This is a major chore. After the test program has been debugged, the testing of packaged parts should be reasonably straightforward. However, wafer testing before packaging is always a major problem. Testing efforts should be made and contracts let to develop cross-assembly techniques and allow test program writing to be done using higher level languages.

* * *

4. The testing of complex LSI devices is <u>very</u> <u>complex</u>. Test equipment, however, is continually reaching the market directed toward simplifying this problem.

* * *

5. Testing philosophy changes, of course, with application and with device type. Specialized testers and specialty test agencies are beginning to appear on the market. While neither of these provides a total

Question #6: Please comment on the problem of testing complex LSI devices.

solution to the problem, they can be of considerable value. In the case of a microprocessor, it is generally useful to run a comprehensive "board test" prior to insertion of the microprocessor. Then an application-oriented test of the completed function follows.

* * *

6. A standardized testing approach is needed to possibly include standardization on actual test equipment; then test tapes and interfaces can become standard with the costs shared among the users. This will enhance the possibility of achieving correlation and should reduce the possibilities of having conflicting test results.

* * *

7. Microprocessors and generally all LSI devices pose a significant problem to the test/characterization engineer since by definition and design, no two devices are architecturally similar. This requires a functional test program for each device. The increased complexity of the devices poses, at times, insurmountable problems in exercising areas of the device that are "buried" within the functional architecture and therefore cannot be directly tested. The test engineer is faced with testing the equivalent of several pages of heretofore discrete logic in a 40-pin component. Component manufacturers have not addressed the LSI testability problem adequately in their products.

On second-source products, the problem faced here is one of dissimilar processes being used to implement the same function. Complete electrical characterization has revealed that frequently two vendors are not really true "transparent" second sources. A composite specification is generated to cover the guaranteed performance and DC interfaces to be expected independent of the vendor used.

Question #6: Please comment on the problem of testing complex LSI devices.

We are faced with different approaches to implementing the same function, different processes, and different performance definitions on parts that are marketed as the same LSI part type.

The classical approach to testing SSI and MSI devices has been the "stuck fault" concept, which checks all static gate operations. While this approach was adequate for these devices, LSI poses significant test problems both because of the increased number of parts and the iterative closed-loop operation of many internal device functions. It is nearly impossible to perform adequate "stuck fault" testing on LSI devices.

Even if "stuck fault" could be performed, it would not necessarily guarantee proper device functioning at system (user) speeds. What is being done presently in LSI device testing is to judiciously select a critical number and type of test patterns, and run them at system speeds in the device, confirming proper operation. This algorithm selection is not a closed and precise technique, but relies heavily on the vendor's past performance on similar devices and our perception of the part's possible functional problems.

In addition to the problems of testing individual LSI devices, there is an even greater problem in testing subassemblies containing these components. Previous methods of testing MSI subassemblies are also not adequate (i.e., "stuck fault" testing of low-level logic) for testing subassemblies populated with LSI devices.

A compromise solution is to separately test the LSI logic (with functional test patterns) and the MSI logic (with conventional "stuck fault" patterns). This requires isolation of the LSI devices using tri-state buffers wired to external connector pins. These I/O pins usually are

Question #6: Please comment on the problem of testing complex LSI devices.

very rare in the subassembly design, since most of them would have already been committed to operational I/O and are not available for testability.

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8. At present, this is a very difficult problem and will become more difficult. In order to maintain reasonable bounds on this problem, reasonable judgement must constantly be exercised. For complex LSI devices, 100% fault coverage testing is very often not economically feasible.

Planning for testing could ease the problem. Building testing ease into a microcircuit is often possible (e.g., bringing out a reset line on a long counter chain so that it can be initialized easily). Specification consistency could also help. For example, specifications which have different loading conditions for each output or each input can create severe testing problems.

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9. In testing SSI/MSI devices, generating a functional test which 100% tests the gates and all possible patterns is not unreasonable. For LSI, such an exhaustive functional test is not practical. Patterns on the order of 100^{100} would be required. Some middle ground must be reached. (Approximately 90% of gates, verify functional partitions, execute all instructions or basic functions, data patterns: all ones, all zeroes, etc.) Guidelines must be established.

Generation and implementation of a reasonable functional test requires effort heretofore unheard of for a device test. The non-recurring costs for writing LSI device test programs can range from 6 man-months to 2 man-years. For a user this can be reduced by 20% to 30% by implementing a vendor's test program, if available. The difficulty is that the vendor's program is peculiar to a given test machine. The test program must be translated to be implemented on a different machine. This highlights one

Question #6: Please comment on the problem of testing complex LSI devices.

of the major problems associated with specifying an LSI device. For example, the functional test for the 8080A microprocessor (MIL-M-38510/420) lists 12,000 binary vectors. To convert this detailed functional test to a given test machine will require three to five man-months of programming effort. If a translator program already existed, this time could be reduced to about one man-month.

Another problem is that devices completely compatible at the system level may not be completely compatible at the device test levels. This situation came to the forefront when a test program developed for Intel's 8080A microprocessor could not be used to test the 9080A (AMD's equivalent 8080A).

Much study is needed in the area of device testing. The trend seems to be toward dedicated testers (microprocessors and peripheral) as opposed to large general-purpose LSI testers. For military procurement, some standard method of testing and standard test machines should be established. Translators for these standard machines should be made available to suppliers and users.

A set of standard vectors should be generated for the different LSI families (e.g., RAMs, ROMs, shift registers) to provide a baseline for industry testing. For LSI devices greater than 500 gates, the judicious use of on-chip BITE should be encouraged to simplify device testing.

* * *

10. Testing of complex LSI circuit devices can best be accomplished by taking into consideration the function of the part, the geometry of the die, and the technology being used.

Testing software must exercise all basic functions of the device. Tests for "worst case cross-talk" should be derived by taking into

Question #6: Please comment on the problem of testing complex LSI devices.

account the failure mechanisms peculiar to the technology being employed as well as the geometric placement of the cells within the device. All possible truth table combinations will probably be impossible to test in a reasonable testing time, but great assurance of proper performance may be obtained using this method. Likely, only the device manufacturer has all the facts and test equipment necessary to evaluate his product. For incoming inspection testing, an "in use" circuit at temperature extremes should insure that the received device is indeed functional.

* * *

11. There is great difficulty in testing LSI devices because of their complexity and the weakness of the design disciplines used so often in creating new LSI devices. LSI testing complexity stems primarily from the need to test for interactions between each of the thousands of elements in the LSI part. With a disciplined design approach, such as standard cells, this interaction problem can be minimized because the logic functions are designed and tested to eliminate the possibility of all interactions, and the interconnection matrix is designed to access the cells only at preselected access nodes. The logic on a standard cell design must be tested for function, of course, but the extensive testing for pattern sensitivity and interaction between elements can be eliminated. Such disciplined design approaches should be designated by NAVAIR as their preferred design approaches.

An additional approach to testing LSI devices that is presently being studied is a functional simulation/testing program that allows subelements of complex LSI devices to be exercised independently, thereby decreasing the complexity of the test pattern generation and testing problem. This area of study should be funded by government contracts with specific initial goals of testing today's LSI devices and generating ideas for testing the next generation of VLSI devices of greatly enhanced complexity.

* * *

Question #6: Please comment on the problem of testing complex LSI devices.

12. Testing of VLSI circuits is just evolving, and it seems that it will be impractical to fully test a part even with the use of computer-aided tools. Therefore, decisions will be made based on tradeoffs during the design cycle that will exercise the part to a level maximizing the probability of detecting a failure mode.

Considerable experience for judging these deicsions is available from the testing of calculator components and computer systems.

* * *

13. a. Complex LSI devices should be tested as we test PC cards, using only the I/O pins.

b. Custom LSICs must be designed to facilitate testing.

c. Obtain and duplicate vendor test programs for standard LSI parts.

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14. This difficult problem is greatly simplified if the designer is made responsible for specifying the test procedure. Not only is the designer best qualified to specify the test procedure, and knowing exactly what the LSI is expected to do, but untestable designs are eliminated. In many cases, the addition of a few extra pads which need not be brought out of the package will greatly simplify testing.

Very often LSI is so complicated that only computer-aided design procedures are capable of producing satisfactory results. NAVAIR should encourage the use of these programs, and should require that test vectors be generated before the design is released to production, both for the LSI and for the equipment using the part.

Question #6: Please comment on the problem of testing complex LSI devices.

Frequently, both Test and Design departments exist within an organization, and each expects the other to be responsible for the test sequence. The problems that may be created can be eliminated by requiring the Design department to be responsible for the content of the tests, and the Test department to be responsible for implementation.

* * *

15. Experience indicates that 100% screening for critical parameters at extended temperatures, voltages, etc. is the only effective test philosophy. Inasmuch as possible, the test configuration should emulate the intended application, for, with complex LSI devices, testing all possible combinations of parameters is difficult and costly to implement even when using automatic test equipment.

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16. No comment.

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17. Sophisticated test equipment is a necessity if a wide variety of parts are to be tested; but comparative testing can be performed on dedicated hardware. A governmental software library containing magnetic test tapes for commonly used hardware would reduce the OEM's test development costs.

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18. There are several levels of testing required for LSI devices. All levels require considerably more complex test algorithms than with MSI. Functional testing with known state conditions can be complemented very nicely by voltage contrast detection of these internal state conditions. That is, the same computer-controlled electron beam technology that is advancing the state and complexity of LSI (VLSI) is also able to provide new test information internal to the chip. In particular, fault isolation on a pre-packaged (or reopened) LSI chip can be

carried out efficiently. Test algorithms already exist that exercise LSI chips, but there are times when no amount of exercising of the chips will reveal the failure mode. However, a computer-controlled electron beam (high impedance probe) can be used to address any point on the chip; and with proper instrumentation and methodology, voltage state (nodal points) internal to the chip that are inaccessible by any other means can be measured. This information combined with the other more mature test algorithms can be the basis of new test procedures that must be developed concurrently with further advances in LSI.

* * *

19. The complexity, initial cost, and operating cost of testers has escalated with the complexity of LSI. Provision for test should be incorporated into each LSI device to simplify test and fault isolation. Up to 20% of the circuitry on the LSI device should be assigned to test and fault isolation.

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20. CAPT V. J. Ohm, USAF, was extensively involved with the characterization of the 8080 microprocessor. It is recommended that inputs be solicited from CAPT Ohm, who is intimately familiar with the testing of complex devices.

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G. Question #7: What should be done to make custom LSI circuit development costs and turnaround times affordable to NAVAIR and its contractors, with low system and schedule risks?

Highlights:

There were two suggestions that enjoyed a reasonable degree of concurrence among respondents. These were:

- Use computer-aided design techniques employing libraries of standard cells in technologies that are in the mainstream and which can be manufactured on high volume production lines.

- Make optimum use of semi-custom integrated circuits such as universal gate arrays and so forth.

Industry Replies:

1. Custom LSI circuit design costs and risk factors are, of course, directly related to the complexity of the design and how far the process technology must deviate from what is currently in production. LSI digital circuits should, if at all possible, be designed using well-established logic building blocks as used in standard catalog items such as 54LS or one of the standard MOS technologies. Provided the custom circuit does follow standard 54LS or other mainstream technology, the automated computer-aided design facilities using the library of the building blocks will provide a design with a high probability of meeting the systems requirements the first time it is manufactured. Processing of the custom circuit can then be done on a high volume production line

Question #7: What should be done to make custom LSI circuit development costs and turnaround times affordable to NAVAIR and its contractors, with low system and schedule risks?

using exactly the same process and product guidelines used on any standard 54LS circuit. In the case of linear or nonstandard digital circuits where the use of people (not machines) goes up, so does the risk factor and the probability of not meeting the systems requirements the first time. Unfortunately, there does not seem to be a foolproof approach in these cases. I personally believe more time should be spent breadboarding and computer simulating the circuit, and that "haste means waste" in these areas. There is usually such pressure brought to bear by the system manufacturer that the semiconductor house will commit a circuit design to layout and mask generation prematurely just to meet a schedule.

* * *

2. Maximize the use of gate arrays (bipolar) and cell libraries (MOS). Make the use of an existing up-to-date CAD system a precondition for development contract awards.

* * *

3. It would be very difficult to make custom LSI circuit development affordable (approximately $100,000/circuit) and turnaround times good (approximately 12-18 months) for NAVAIR-type circuits. Schedule risks must be considered. If the NAVAIR systems could be designed around standard parts, with few custom devices, then turnaround times and costs would be reduced considerably.

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4. We feel the answer to custom LSI is the in-house dedicated facility with a thorough understanding of systems requirements and with the motivation of having to deliver the successful system.

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Question #7: What should be done to make custom LSI circuit development costs and turnaround times affordable to NAVAIR and its contractors, with low system and schedule risks?

5. Consider the use of master slice/master gate as a breadboard of quick reaction custom semiconductor houses, i.e., Exor, Interdesign, RCA, etc. We would also question whether a custom LSI approach is consistent with the objectives of questions 1 through 3 of this survey. Except for extremely high volume and some specialty applications, we believe standard LSI is a far better solution. Where packaging size constraints are severe, a hybrid microelectronics approach can offer an attractive alternative.

* * *

6. No comment.

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7. Computer placement and wiring of macro cells is an approach offered by a few vendors that provides moderate development cost and quick turnaround. NAVAIR should capitalize on the similarity of these LSI approaches by funding the development of common macro functions and the enhancement of the computer placement and wiring programs. These programs should be enhanced to permit input/output pin assignment as a design input. These developments should result in acceptable alternate sources.

Recurring costs of computer placed and wired macro cells are, of course, volume dependent. Those functions that never achieve high volume would remain unchanged during their production life. However, those that achieve high volume should be redesigned using conventional hand placement and wiring to achieve minimum silicon die area and thus minimize cost. The initial computer placed-and-wired macro cell approach phase for known high volume functions offers quick development time at moderate cost and hardware with which to test the designs in a system before committing to the long, costly, hand layout of the desired LSI functions.

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Question #7: What should be done to make custom LSI circuit development costs and turnaround times affordable to NAVAIR and its contractors, with low system and schedule risks?

8. *Standard cell approaches and design automation techniques are the best ways of attacking the development cost and turnaround time problems. DoD and NAVAIR might wish to consider further development programs in this area so as to lessen cost and development times.*

The risk problem could best be solved by working with proven technologies manufactured by proven suppliers who are committed to supplying custom circuits, and in particular, custom circuits for the DoD market. This also attacks the problem of maintaining reasonable business levels with suppliers.

* * *

9. *CAD systems provide a partial solution to the problem of costs and development times. The use of cell libraries for chip designs or the use of customizable gate arrays or PLAs provides low risk, minimal cost LSI. However, these solutions to the cost/schedule/risk problems have performance disadvantages in that the resulting devices generally are not optimized for speed, power consumption, drive capability, or chip yield. Encouraging the development and use of such automated chip design CAD systems would be of benefit to NAVAIR.*

It should be recognized that custom LSI nonrecurring costs directly reduce the next higher level of assembly design and development cost. LSI significantly reduces the number of multilayer boards, interconnections, cost, and assemblies required for an equipment, and thus reduces system cost and schedule risks.

The use of SAMs offers the long-range potential of minimum development risks, reduced development lead times, and reduced production

Question #7: What should be done to make custom LSI circuit development costs and turnaround times affordable to NAVAIR and its contractors, with low system and schedule risks?

schedule lead times. Multiple sourcing of SAMs will also reduce system risks associated with sole source production problems.

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10. One approach would be to encourage the use of previously developed custom LSICs (government funded) and the use of computer-aided design programs with standard cell libraries for various technologies developed and maintained by the government.

Two or three information centers located in different geographic areas of the country could be set up for government contractors' use. These centers would maintain all the data on custom LSICs developed on Government funds. This data could be reviewed to see if any of these devices or simple modifications of them could be used in new designs. If the government owned the designs, simple modifications could be obtained at a fraction of the design cost of starting from scratch. (New masks would have to be made but a majority of the layout would be complete.)

Government-developed CAD programs with standard cell libraries for various technologies would also be maintained at the information centers. These CAD programs could be an extension and expansion of the programs such as those at ECOM and NSA. Government contractors could purchase computer time to design LSICs or obtain the programs for use in their own facilities. Either way, technical assistance and update information for the programs could be provided at these centers. This would have the advantage of standardizing the design rules and the cells used in custom LSIC designs. Wafer fabrication sources would have higher confidence in being able to successfully process the designs, and the design risks would be reduced. The government could design test pattern chips to check out new cells to be added to the cell libraries and also

Question #7: What should be done to make custom LSI circuit development costs and turnaround times affordable to NAVAIR and its contractors, with low system and schedule risks?

to check the process compatibility to the designs of various fabrication sources. A list of compatible fabrication sources could also be maintained.

The use of standard design rules and cells should make the task of redesigning existing LSICs into new technologies and processes somewhat less difficult and less time-consuming.

* * *

11. NAVAIR should adopt quick turnaround, low non-recurring cost LSI design approaches that have been developed by industry and that are familiar to personnel at government agencies. We have developed three design approaches that meet these criteria:

- Standard Cell
- Universal Array
- Handcrafted Computer-Aided Designs

The first two are established approaches which are now operational in several government agencies and at many military system contractor facilities. The standard cell and universal array approaches are affordable, reliable, and allow designs to be accomplished within typical equipment development schedules.

* * *

12. Experience indicates that LSI functions should be implemented with a technology which supports at least 1000 gates per 20,000 square mils of chip area, including interconnects. I^2L satisfies this requirement well. (See response to Question 8.)

To minimize design cost and cycle time, two approaches should be considered. Applications requiring fewer than 1000 gates of

Question #7: What should be done to make custom LSI circuit development costs and turnaround times affordable to NAVAIR and its contractors, with low system and schedule risks?

complexity (64 flip-flops, 500 gates, and 1/0 buffers) should employ a gate array technique. Cycle time to receiving functional parts with this approach is 8-10 weeks.

Applications requiring a level of integration greater than that provided by the gate array should consider use of an automated design system. With such an approach, design cycle times range from a minimum of 21 weeks upward, according to the device's level of integration.

All of the above cycle times assume a completed gate level description of the function at the outset of the project.

The requirement for custom LSI functions can often be minimized. Proper system partitioning permits most system functions to be implemented with standard microcomputer devices which have been programmed to implement the particular system function. With this approach, the only functions requiring custom LSI are readily implemented with the level of integration supported by the gate array described earlier.

* * *

13. a. Investigate the utility of a set (small) of standard gate arrays in the 200-500 gate range. Customization then only requires custom metallization. Qualify the parts independent of customization.

b. Use standard cell/automated design approaches.

c. Use programmable LSI devices when possible; purposely design for their use.

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Question #7: What should be done to make custom LSI circuit development costs and turnaround times affordable to NAVAIR and its contractors, with low system and schedule risks?

14. Use CAD techniques throughout with emphasis on a standard cell approach. Automated LSI design systems have been developed by both NSA and NASA and are in the public domain. Use of these systems greatly reduces turnaround time, cost, and risks because of the large amount of automated error checking. Standard cells have been carefully characterized so that their performance can be predicted accurately; therefore, automated layout using these cells has a high probability of success.

Every effort should be made to avoid the multiple try, minimum area procedures common in the commercial semiconductor industry. While this technique is sensible where an LSI chip will be manufactured in large quantities (hand calculators, for example), it does not make sense for a few thousand parts total.

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15. Non-recurring costs and the time required to develop special devices can be minimized by building on existing designs. This concept utilizes subelements which have been designed and proven in actual applications. It would also often be better to carry some unused functions in a device rather than to tailor the device to a specific application. Standardization of design rules and precautions against overspecifying are of paramount importance.

An additional costly pitfall is trying to embody too many functions in a single device when there is no real overriding reason.

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16. No comment.

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Question #7: What should be done to make custom LSI circuit development costs and turnaround times affordable to NAVAIR and its contractors, with low system and schedule risks?

17. We make use of internal MOS manufacturing facilities to meet the needs of low volume production requirements. For commercial products, NAVAIR should consider procuring a quantity of parts for re-sale to OEMs; thus eliminating lot charges.

* * *

18. Computer-controlled electron beam lithography can be developed not only to provide the high performance LSI required, but to do so with the shortest possible turnaround times at affordable costs. There are schemes and considerably advanced work in process to provide replication of submicron device patterns over an area as large as one square millimeter, and thereby increase the throughput of VLSI chips even more over direct electron beam exposure. This combination of computer-controlled electron beam lithography for both direct wafer exposure and mask making combined with advanced lithographic replication must be developed and committed in a timely manner.

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19. The master chip and PLA concepts should be encouraged. A clearing house for available master chip designs and a catalog of equivalent MSI functions that can be implemented from these designs would encourage use.

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20. Actively get involved with USAF/RADC to expedite development of detailed MIL-M-38510 specifications for LSI devices. In general, the military should look toward establishing common but very precise/detailed/contractual requirements that force all contractors to a common type procurement. There are many ways in which this could be done, but standardization must be required of every contractor in a uniform way to achieve the type of volume, in an ever-shrinking military market, which will result in continuous device production.

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H. Question #8: What semiconductor technologies are required for future avionics systems that will not be available in a timely manner as spin-offs from non-military products? What developments should be funded by NAVAIR? Why?

Highlights:

The following technological developments were identified most often by the respondents as requiring NAVAIR development support.

- Radiation hardened technology/device development
- Computer-aided design techniques and standard cell development
- CMOS/SOS technology
- High Speed GaAs technology
- I^2L LSI technology

A list of other suggestions is as follows:

- Silicon and GaAs MESFET
- Depletion-load NMOS/SOS
- Microwave devices
- LSI at GHz
- MICs

Question #8: What semiconductor technologies are required for future avionics systems that will not be available in a timely manner as spin-offs from non-military products? What developments should be funded by NAVAIR? Why?

- Dielectric Insulated (DI) devices
- High reliability hybrids
- Militarized low power 8-bit or 16-bit microprocessor
- Specific LSI building blocks
- Special packaging and handling technologies
- LSI testing techniques
- Multi-level logic and software techniques
- Acceleration of development of LSI and VLSI sooner than commercial demand warrants
- Militarized liquid crystal displays
- Computer-controlled E-beam direct wafer exposure technology

Industry Replies:

1. The industry is moving along the path of technological advancement about as fast as it can. Armies of people and GNP kinds of dollars are being spent on the semiconductor technology. However,

Question #8: What semiconductor technologies are required for future avionics systems that will not be available in a timely manner as spin-offs from non-military products? What developments should be funded by NAVAIR? Why?

I believe we should look at the unique environment of avionic systems and appreciate the fundamental failure mechanisms at work in this environment. The hostility of an avionic system must be one of the most difficult with its temperature extremes, shock forces, and probably most of all, the extreme changes in barometric pressures. The temperature extremes and shock forces are probably well within the state-of-the-art of any LSI technology. Change in barometric pressure, however, is probably the principal underlying cause for most operational failures of airborne electronics. There is a vast improvement necessary in the hermetic package area to provide a fundamental improvement necessary to meet this environment. The semiconductor manufacturer selects his package based primarily upon piece parts cost and yield. Reliability is considered for a broad spectrum of customers and usages, and does not adequately address the avionic environment. If I could encourage the Navy to fund any needed improvement, it would be to develop a hermetic package in a standard format, where reliability and appreciating the fundamental failure mechanisms at work in this environment would be the driving motivators, not piece parts cost.

* * *

2. CMOS/SOS, silicon, and GaAs MESFET technologies; depletion-load NMOS/SOS. I believe that SOS MESFET low power technology has a great future since it combines the low power and layout density of I^2L with the speed and radiation hardness of CMOS/SOS. Since this technology is not funded elsewhere, NAVAIR might want to consider its support.

* * *

3. a. Radiation hardened technologies.

b. Gigahertz technologies (MESFETs, etc.)

Question #8: What semiconductor technologies are required for future avionics systems that will not be available in a timely manner as spin-offs from non-military products? What developments should be funded by NAVAIR? Why?

c. *Extremely high quality technologies.*

High frequency devices for microwave applications might not be available from non-military sources. Developments in integrated high frequency LSI circuits for the GHz operating area might have to be funded to get something specifically for the military.

* * *

4. High speed digital logic using gallium arsenide and microwave integrated circuits are areas that will probably not spin off from the commercial world. In silicon-based technology, very large memories and hardened devices are also unlikely as commercial spin-offs.

* * *

5. Radiation hardened and dielectric isolated devices. Also, high reliability hybrids. Neither is being pursued by the commercial world.

* * *

6. No comment.

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7. In the near term, a reliable, competitive, and performance attractive low-power 8-bit or 16-bit microprocessor is not available for the military use. Problems have been experienced in all the current CMOS products in this category, related to architecture (since these products now available were originally designed for specific applications and now are attempting to answer general-purpose CPU problems), and performance in the military environment.

The CMOS technologies available today are capable of producing a "CMOS Z80" or "CMOS 9900," etc., that would be very attractive to

Question #8: What semiconductor technologies are required for future avionics systems that will not be available in a timely manner as spin-offs from non-military products? What developments should be funded by NAVAIR? Why?

the military's current requirements for low-power, general-purpose, and low-cost military microprocessors. However, vendors have not initiated this approach since they are commercial-market oriented and lack the marketing inputs to develop this product on their own. A funded effort now would yield products in twelve months, much before the industry would initiate this effort on their own. The typical budget requirement for a CMOS Z80 has been sized at 150-200K.

Radiation-hard bipolar and MOS technologies needed for some future avionics systems are not likely to evolve as spin-offs from non-military products. Technologies such as CMOS and I^2L have the potential for high levels of integration because of low power consumptions. NAVAIR should, as a minimum, fund the development of radiation hard I^2L because of its potential for extremely high integration levels and high radiation hardness levels. Funding the hardening of the CMOS technologies used in existing computer placed-and-wired macro cell approaches to LSI should also be considered.

In discussing LSI technologies that should be funded by the Federal government, there is a philosophical dichotomy which is briefly explored here. On the one hand, the military usually wants equipment that is field repairable; but the LSI manufacturer has a large capital investment in a process which has led to an inexpensive device cost, cheap enough to often be considered "throw-away." The military likes the "throw-away" concept, but is discouraged by the huge front-end investment required in capital equipment.

Military equipment and device manufacturers have historically desired to "personalize" their product in their shop; that is, program a

Question #8: What semiconductor technologies are required for future avionics systems that will not be available in a timely manner as spin-offs from non-military products? What developments should be funded by NAVAIR? Why?

microprocessor, lay out the architecture of an FPLA, etc. There is a paradox here that must be considered. Device manufacturers want the freedom and flexibility to modify their products as they see the needs of the marketplace. DoD-directed top-down technology direction, even though well-intentioned, could lead the IC industry into an area or product group which ultimately could turn out to be wrong. The present structure of the LSI/IC marketplace consists of multiple and distributed technologies, processes, and expertise, competing freely. While this structure is far from perfect, it may be preferable to a Federally-controlled device/technology program. A compromise solution may be for the military to identify its LSI needs from a <u>functional</u> rather than a <u>device</u> perspective. In this way the LSI manufacturers could competitively create what they feel are the best technologies, architectures, and processes to perform the required function.

* * *

8. Future avionics systems will require microcircuits with more functions that go faster. This is not unlike industrial needs. Consequently, the semiconductor industry will develop the basic technology to accomplish this without significant sponsorship from DoD. DoD and NAVAIR should concentrate their efforts on programs which get the technology into a form they can use, such as:

- *LSI building blocks (specific devices)*
- *Standard cells and computer-aided design technological improvements*
- *Special packaging and handling technologies*

Question #8: What semiconductor technologies are required for future avionics systems that will not be available in a timely manner as spin-offs from non-military products? What developments should be funded by NAVAIR? Why?

- *Low power and radiation hardened technologies designed to meet military needs rather than industrial*

- *GaAs development*

Of course, NAVAIR and DoD should be in search of those new technologies which have a high payoff for both the military and industrial markets, but have high risks as well; and therefore are not intentionally funded by the semiconductor industry. In these cases, DoD development funds could be very effective in initiating a new technology.

* * *

9. In terms of future semiconductor technology development, three areas should be considered: (1) design, (2) process, and (3) test. In the design area, new models for submicron devices are required. In the process area, new equipment and techniques are required. In the test area, new test philosophies are required. The design and process areas will be driven in the medium speed bipolar and medium to high speed MOS by the commercial markets. However, the very high speed bipolar processes such as GaAs will probably require additional military funding. In addition, the area of LSI testing could benefit from additional military funding in terms of test philosophy development.

In addition, a quote from Intel's G. Moore (BW October 24, 1977) may be appropriate here in terms of the thrust of new technology: "It's not clear that we know what to do with . . . (something) . . . 10 times more complex than today's . . . (devices) . . . . It may turn out to be more important to design better circuits of less complexity."

Question #8: What semiconductor technologies are required for future avionics systems that will not be available in a timely manner as spin-offs from non-military products? What developments should be funded by NAVAIR? Why?

The leading future commercial LSI and VLSI technology is NMOS. Unfortunately, NMOS is the least desirable of the future LSI semiconductor technologies when considering nuclear radiation hardening requirements. CMOS/SOS, I^2L, and T^2L offer increased capabilities in this area, but they will not approach NMOS in commercial usage. With the exception of I^2L, commercial usage of LSI bipolar technologies will be inhibited by larger area per gate and power dissipation requirements. Future funding may be required to assure that essential CMOS/SOS and I^2L LSI products will be developed and refined to meet future military system requirements.

* * *

10. We are not in a position to comment on the overall technology needs that should be funded. In the medium to high GHz frequency range, GaAs appears to be a viable technology to develop; however, at present we have no applications requiring these frequencies.

The trend toward use of radiation hardened devices suggests possible heavy military funding in development of technologies and process capabilities in this area.

We also suggest that NAVAIR take a good look at the possible development of multi-level logic devices and software techniques to evaluate their promises of even greater weight and size savings.

* * *

11. One technology that will be required in future avionics systems and that will not be available in a timely manner as a spin-off from non-military products is radiation hardened technology. CMOS/SOS is a technology that has inherent radiation hardness qualities. However,

Question #8: What semiconductor technologies are required for future avionics systems that will not be available in a timely manner as spin-offs from non-military products? What developments should be funded by NAVAIR? Why?

military funding is required to develop design aids such as standard cells and universal arrays that will enhance the inherent hardness and will be useful to meet custom LSI requirements for hardened avionics equipment.

NAVAIR should fund the development of this technology and the enhancement of its hardness capabilities, as well as standard cell families and universal arrays. Technology choice is an ever-changing panorama.

* * *

12. The basic manufacturing and circuit technologies required for future military systems are being developed and evolved by industry on its own. It is especially important that the military restrict the use of specialty technologies which are not likely to be used and developed by industry on its own. We believe that integrated injection logic (I^2L) best fulfills military requirements and is likely to be used widely in commercial LSI also. We are presently using I^2L in over 15 custom LSI circuits.

Government funding should be vectored toward the development of LSI and VLSI functions which are either unique to most military systems or which are required by military advanced development programs sooner than normal industry progress would permit. Unique functions should be restricted to items of general military applicability such as MIL-STD-1553 bus interface processors, NTDS bus interface processors, etc. However, these devices should be developed as compatible members of existing qualified families as indicated in the response to Question 1.

Government funding can also be vectored to accelerate development of devices sooner than commercial demand would warrant. This

Question #8: What semiconductor technologies are required for future avionics systems that will not be available in a timely manner as spin-offs from non-military products? What developments should be funded by NAVAIR? Why?

funding will likely have the long-term effect of stimulating commercial technology growth. For example, consider the case of a military advanced development program whose size, weight, power, and cost objectives require the use of a single-chip microcomputer device having twice the memory available in present commercially available devices. The probable reason the commercial market has not caused development of this device yet is that the trade-off of commercial volume versus price (manufacturing yield) is not yet favorable. Note that development of such a device is technically feasible. The smaller volumes required by the military in advanced development phases are not threatening to the semiconductor manufacturer. Therefore, government funding of advanced device functions such as this can accelerate availability of these functions for military advanced development while having the likely side effect of stimulating more rapid evolution of the commercial market.

Government funding should also be used to support testing and verification of device performance relative to unique military requirements such as radiation hardness testing.

Government funding should emphasize device development to increase the level of function integration per integrated circuit as opposed to emphasizing circuit speed. System requirements for speed should be met through use of improved system architectures which exploit the use of VLSI circuits. This is the approach which commercial technology has followed and which has caused the explosion of very low cost consumer and commercial electronics. If device speed continues to be a requirement, it is much more practical to improve circuit speed once the correct level of device integration has been achieved.

* * *

Question #8: What semiconductor technologies are required for future avionics systems that will not be available in a timely manner as spin-offs from non-military products? What developments should be funded by NAVAIR? Why?

13. I question whether it would be advisable to use any technology in military equipment which is (or was) not produced in quantity for commercial uses. The high volume commercial production helps mature and prove a technology as well as revealing any inherent failure mechanisms. If the expected market for ICs in automobiles is realized, technologies which meet military temperature and shake, rattle, and roll specifications should be available. Special technology development may be required to achieve radiation hardness, and unique environmental requirements such as a cryogenic atmosphere.

* * *

14. The only technology which comes to mind is SOS; however, other technologies with similar characteristics may exist. Such technologies would have some of the following characteristics:

a. Too expensive for commercial applications.

b. Superior performance characteristics.

c. Not limited to one or two suppliers.

d. A commitment or potential commitment by systems houses to use the technology in systems with a relatively long life span.

NAVAIR should consider funding improvement in the documentation of the existing CAD programs for automated chip layout and design. Although these programs presently exist, the documentation is generally inadequate. Any organization desiring to use the programs must pay a relatively high "initiation fee" in computer time and experimentation

Question #8: What semiconductor technologies are required for future avionics systems that will not be available in a timely manner as spin-offs from non-military products? What developments should be funded by NAVAIR? Why?

before enough is known about the programs to use them effectively. Good documentation of the "cook book" type would eliminate much of this and encourage additional use of the programs.

NAVAIR should also fund the development of additional standard cells and cell libraries in the SOS technology. At present the choice is very limited, forcing users to design their own custom cells. These, of course, are proprietary and not available to other organizations. It would probably be desirable to fund the development of a cell family with characteristics that are different from those of existing libraries. Possible examples are minimum area or greater operating voltages.

* * *

15. No comment on the first question. As to the second, development of mask generation capabilities utilizing multiple technologies should be established within each military contractor. Most military systems requiring the use of custom LSI do not result in sufficient production quantities to entice device manufacturers to commit engineering resources to the design effort. Therefore, the user must be capable of performing a significant portion of the design using the rules established by the device manufacturer.

* * *

16. No comment.

* * *

17. All currently available semiconductor processes are or soon will be available for use in military products. Liquid crystal displays, although not a semiconductor, are needed for future avionics systems. The current maximum operating temperature is 85°C but 100°C parts are needed for cockpit displays.

* * *

Question #8: What semiconductor technologies are required for future avionics systems that will not be available in a timely manner as spin-offs from non-military products? What developments should be funded by NAVAIR? Why?

18. Commercial semiconductor houses will soon provide advanced LSI (at the 2 micrometer design rules) using electron beam-fabricated low defect masks. However, high performance (low power, high speed) custom LSI using sub-micrometer design rules will not be available commercially until 1985 or later. Certain military avionics applications cannot wait that long--modest quantities of sub-micrometer LSI must become available by 1980-1981. In order to meet these new system needs, NAVAIR should support computer-controlled electron beam direct wafer exposure technology in general, and in particular high throughput electron beam system development, advanced resist development technology, advanced circuit design, and renovation of previous concepts on the transition from device concept to digitized pattern data tapes.

* * *

19. No comment.

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20. At the 19 October 1977 FSC 5962 coordination meeting held at DESC in Dayton, Ohio, an excellent presentation of how far ahead we would look and have a reasonable degree of certainty regarding the technology that would be employed in future equipments was provided by AIA. It is recommended that DESC be contacted for a copy of the AIA presentation including next generation technology requirements (3 years).

* * *

I. Question #9: What changes should be made to existing MIL-specifications, standards, requirements, and policies to facilitate the introduction of advanced LSI technologies? (Be specific.)

Highlights:

Suggestions resulting from the respondents' replies to this question are listed below:

- Change MIL-M-38510 qualification by allowing submittal of existing design test data to satisfy the qualification requirements.
- Update MIL-HDBK-217B to include reasonable failure data for complex monolithic LSI devices.
- Consider the JC13.2 Committee recommendations on MIL-M-38510 JAN IC devices.
- Lot qualification testing is too extensive and costly.
- Utilize the DESC "Selected Item Drawing" (mini-spec) approach to allow more efficient introduction of LSI technologies.
- Replace the controversial MIL-STD-883 chip visual requirements with a comprehensive electrical test.

Question #9: What changes should be made to existing MIL-specifications, standards, requirements, and policies to facilitate the introduction of advanced semiconductor technologies? (Be specific.)

- Develop translator programs to convert the test vector listing on the MIL-specification for standard LSI to popular test machines.

- Qualify various vendor cell libraries.

- Achieve confidence in process-related areas through facility certification.

Industry Replies:

1. The Joint Electron Device Engineering Council JC13.2 Committee on Government Liaison for Microelectronic Devices has recently developed a matrix of cost-effective suggestions related not only to LSI but to all JAN ICs. *(See page 19.)*

* * *

2. The qualification of device types is too cumbersome at present, even when well understood technologies are used. Lot qualification testing is also too extensive and costly.

* * *

3. No comment.

* * *

4. This is a highly complex question with business, technical, and pseudo-political ramifications. I will basically pass, except to say again that schedule times are often a severe limitation to the introduction of advanced LSI technologies.

* * *

Question #9: What changes should be made to existing MIL-specifications, standards, requirements, and policies to facilitate the introduction of advanced semiconductor technologies? (Be specific.)

5. DESC 7XXXX Mini-Specification.

* * *

6. No comment.

* * *

7. The changes that should be incorporated are:

a. Utilize industry to select the product base and then fund for the evaluation of these devices. This would alleviate the proliferation of devices.

b. Amend MIL-M-38510 to allow for the qualification of devices built "off-shore."

c. AR-10A must be clarified and revised for subassemblies containing both MSI and LSI components.

d. AR-10A should address fault detection separately from fault isolation. For example, fault detection should be to a specified percentage (85%) and fault isolation to a specified number of components (for example, 4).

These faults should be restricted to "relevant" faults, i.e., affecting the operation of the device, rather than all "possible" faults which could occur.

Measurement techniques must be developed for functional test coverage which are compatible with "stuck fault" test coverage so that a test coverage figure for the entire subassembly can be computed. Reliability data should also be factored into these calculations to give heavier weighting to those components with a higher failure rate.

Question #9: What changes should be made to existing MIL-specifications, standards, requirements, and policies to facilitate the introduction of advanced semiconductor technologies? (Be specific.)

e. Utilization of the DESC "Selected Item Drawing" (mini-spec) approach should be emphasized, since this will allow for more efficient introduction of LSI technologies and obtain industry standardization and control at the same time.

* * *

8. Appropriate changes have been previously suggested, namely:

a. Economics often dictates less than 100% test characterization (fault coverage).

b. Reduced visual criteria for LSI devices.

* * *

9. As a minimum, the following specifications will require changes: MIL-E-5400, MIL-M-38510, MIL-STD-883, MIL-M-28787, and MIL-STD-1389. For custom LSI low usage devices, the following should be considered as an addition or replacement to the present standard requirements and specifications placed on microcircuits:

a. Investigate new package schemes (e.g., chip carriers, tape bonding, etc.); MIL-M-38510.

b. Replace the controversial MIL-STD-883 chip visual requirements with a comprehensive electrical test such as Guard Band tests exceeding rated voltages.

c. Replace the standard qualifications with a mini-qual.

For standard LSI (i.e., microprocessors), translator programs which convert the test vector listing on the MIL-spec to popular test

Question #9: What changes should be made to existing MIL-specifications, standards, requirements, and policies to facilitate the introduction of advanced semiconductor technologies? (Be specific.)

machines (i.e., Sentry II, Tek 3260, MD 500, etc.) would speed up acceptance of MIL-devices.

For custom and quasi-standard LSI, create a new specification reflecting the final results of this survey. Minimize initial and requalification test costs. Specify the qualification of various vendors' cell libraries with the emphasis being placed on proof testing as opposed to trying to obtain universal agreement on the specification of process and design-related parameters such as line widths and spacings. Require vendors to requalify packaging related factors once per year (assuming no design or process changes) for each package configuration used, not for each package-LSI chip combination. Achieve confidence in process-related areas through a facility certification program similar to that being used in conjunction with MIL-M-28787.

* * *

10. The motivation for use of advanced LSIC technologies exists in the potential advantages they have to offer. However, the high costs of a conventional MIL-M-38510-type qualification can be devastating for a low usage application. Such LSICs are usually designed for a specific application as part of a larger entity (i.e., subsystem, system, etc.) which is itself subjected to environmental and reliability qualification tests. Allowances should be made to use the data generated in these tests to qualify the LSIC. (This is analogous to printed circuit board assemblies tested as part of a higher assembly.) The degree of additional testing on individual LSICs would be dependent upon the risks involved in the design. These risks could be minimized and thus the amount of testing reduced on designs which use the design rules and standard cells that have been qualified through the CAD design center program mentioned in the response to Question 7. The LSICs would also have to be fabricated

Question #9: What changes should be made to existing MIL-specifications, standards, requirements, and policies to facilitate the introduction of advanced semiconductor technologies? (Be specific.)

by a source that has demonstrated "process compatibility" to qualify for the minimum risk category.

Requalification test requirements should also be minimized by taking advantage of the device history generated in device burn-in, end item, or system tests including burn-in, and actual field data.

* * *

11. Military specifications should recognize the difficulty and increased cost involved in detailed visual inspection of complex LSI devices. High voltage and high temperature stress tests and extended burn-in tests should be substituted for visual inspection. This important approach was discussed at the August 1977 IDA Symposium addressing the use of LSI in military equipment. Test results reported there indicated that proper stress tests gave more reliable parts than present visual inspection criteria.

MIL-HDBK-217B handicaps the use of LSI devices by projecting unrealistically bad failure rates for LSI. Industry data does not support the MIL-HDBK-217B approach for predicting failure rates for LSI. MIL-HDBK-217B also unduly penalizes MOS technologies. Current favorable MOS field reliability data needs to be reflected in a revised MIL-HDBK-217B.

* * *

12. The following changes are recommended:

a. Specify device operating temperatures such that devices meeting a $-40^{o}C$ to $+85^{o}C$ operating temperature are acceptable for use. This is adequate for many military applications and allows adequate margins for early LSI device production distributing. As production processes mature, the standard $-55^{o}C$ to $+125^{o}C$ device operating temperature is achieved.

Question #9: What changes should be made to existing MIL-specifications, standards, requirements, and policies to facilitate the introduction of advanced semiconductor technologies? (Be specific.)

b. Allow use of devices packaged in plastic. Burn-in and additional screening may be specified.

c. Pre-cap inspection of LSI and VLSI devices has become impractical due to the multiple levels of the device fabrication process and the extraordinary geometric detail of the devices.

Pre-cap inspection criteria should be reduced to focus on inspection of the device packaging and bonding quality. Verification of functional attributes should be accomplished by functional testing at extended temperatures over a prescribed number of temperature cycles.

d. Reduce burn-in temperature from 125°C to the maximum operating temperature where applicable.

* * *

13. a. Accept warranties, production guarantees, or purchase of an adequate supply of parts as an alternative to second source requirements and to protect against technology changes.

b. Where possible, extend lead times on avionics developments to allow the "risk" of custom development to be minimized. This may require more multi-year contracts.

c. Require life cycle costs to be considered when awarding prototype development contracts. These should include the cost of attributes such as size, weight, power, reliability, etc.

d. Remove lot traceability requirements.

e. Alter MIL-STD-217B to better apply to LSICs.

* * *

Question #9: What changes should be made to existing MIL-specifications, standards, requirements, and policies to facilitate the introduction of advanced semiconductor technologies? (Be specific.)

14. Apply MIL-M-38510 to equipments rather than to LSI chips. Most semiconductor manufacturers are not willing to qualify a line for the small numbers of devices required in military systems. This situation should be recognized.

* * *

15. MIL-M-35810, paragraph 4.2.2, "Qualification," should be changed to allow submittal of existing design test data to satisfy the qualification requirements in lieu of a separate complete qualification test program.

MIL-HDBK-217B must be updated to include reasonable failure data for complex monolithic devices. Industry failure data indicates a significantly lower failure rate than that presently in MIL-HDBK-217B. The data should include necessary variations in failure rates for the specific technologies.

* * *

16. No comment.

* * *

17. No comment.

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18. No comment.

* * *

19. The work being coordinated by RADC/RBRM is in the proper direction.

* * *

20. No comment.

* * *

J. Question #10: In what ways could avionics equipment procurement practices and policies be changed to enhance the introduction of advanced semiconductor devices?

Highlights:

Predominant suggestions were:

- NAVAIR should commit to its LSI supplier early enough in the procurement process for the projected contract production run.
- More rapid equipment development, shorter equipment procurement cycles, and planned-for technology upgrades of equipment should be considered.
- There should be higher weighting of the impact of LSIC on life cycle cost analysis and program funding procedures compatible with minimum LCC, instead of minimum developmental cost.

Industry Replies:

1. It is suggested that you establish a team concept whereby the contractor and a semiconductor manufacturer are selected to work together to develop avionics gear which uses advanced semiconductor devices. In this way they are driven by the same motivations and quite likely you would see an introduced acceleration factor in the use of LSI to solve specific application requirements. This approach has been used quite successfully by the automotive/semiconductor houses in recent contracts for 1978 model year controls. If it worked there, it should work for NAVAIR.

* * *

Question #10: In what ways could avionics equipment procurement practices and policies be changed to enhance the introduction of advanced semiconductor devices?

2. I believe that the Navy would be better off to develop major electronic equipment independently of specific weapon systems, and to upgrade designs in five to ten year cycles. This in turn requires strong modularization at the subsystem level (computers, memories, etc.) and interface standardization. Trends in this direction do exist already, but present program management and procurement practices are not conducive to this approach.

* * *

3. Re-evaluate M.1 standards and attitudes, e.g., "plastic" packaging was bad ten years ago, ergo, it's bad today!

* * *

4. No comment.

* * *

5. When specifications are released, the Government should fund qualification and characterization programs rather than waiting for a manufacturer to use internal funding.

* * *

6. No comment.

* * *

7. NAVAIR should commit to its LSI supplier early enough in the procurement process for the projected contract production run. This would allow the supplier to amortize his non-recurring start-up costs and significantly reduce his recurring cost. Obviously, the technology/performance problem exists here, which makes such a commitment a serious gamble. There is no incentive for a NAVAIR program manager to commit to a production run on a new program even before the new product has been thoroughly evaluated. Or, at the very least, the supplier could be funded to buy and store LSI semiconductors in wafer form, pending the production authorization from NAVAIR.

Question #10: In what ways could avionics equipment procurement practices and policies be changed to enhance the introduction of advanced semiconductor devices?

Two major problems in procurement practices and policies are:

- *Semiconductor second sourcing*
- *Multiple small quantity procurements*

Each of these items is addressed in turn in the following paragraphs.

Custom LSI semiconductors are not practical when second sourcing is also required. Second sourcing requirements are imposed when competitive pricing is desired, when alternate sources of supply are required to avoid the effects of natural catastrophes (earthquakes, etc.), and to avoid "loss of recipe" problems. Most custom LSI is not amenable to second sourcing because the reproduction runs are insufficient to provide a viable economic opportunity for more than one supplier. The other issues of second sourcing can be dealt with by procuring sufficient devices at one time to satisfy the entire anticipated system production run, including spares. Since dicing and packaging of semiconductor devices is not generally a risky process, it is suggested that procurement of LSI devices be divided into discrete steps:

a. Procure sufficient fully packaged devices to satisfy immediate equipment needs and spare parts.

b. Provide front end funding to fabricate sufficient wafers through final test to ensure that the most difficult part of the fabrication process is complete and successful without incurring the costs of final packaging. The wafer fabrication process should provide sufficient quantity for the maximum procurement and sparing envisioned during the entire life of the equipment in question. These wafers should be placed in bonded storage geographically distributed.

Question #10: In what ways could avionics equipment procurement practices and policies be changed to enhance the introduction of advanced semiconductor devices?

c. Procure additional devices by funding the packaging and test of devices starting from wafers placed in long-term storage.

Following the suggestions above, it is possible to procure sufficient devices for a long-term system without incurring all the costs in the front end. The suggested approach also minimizes the risk associated with restarting a production process that may have become obsolete by the time the components are required in production equipment.

The introduction of advanced high-function devices (microprocessors, bit slices, Fast Fourier Transform chips, etc.) could be encouraged through specification of equipment function rather than device performance.

* * *

8. More rapid equipment development, shorter equipment procurement cycles, and planned-for technology upgrades of equipment could enhance the introduction of advanced semiconductor devices.

* * *

9. Establish a standard avionic module (SAM) program and manage the problem at this level wherever possible. Require SAMs to be specified for technological transparency as far as internal circuitry (including LSI) is concerned. Require SAM design cost goals which are compatible with logistic support throw-away cost thresholds. Do not require extensive performance and test specifications for quasi-standard and custom LSI devices; SAM specifications and testing will be adequate to verify functional capability. Require SAMs to be tested over the intended temperature range. Structure SAM test programs in a manner similar to that of MIL-M-28787A. Evaluate LSI designs which have higher development but lower production/maintenance costs on a life cycle cost basis. Allow

Question #10: In what ways could avionics equipment procurement practices and policies be changed to enhance the introduction of advanced semiconductor devices?

trade-offs between performance and schedule--minimum development time schedules preclude or minimize LSI usage.

* * *

10. Higher weighting of Design-to-Cost/Life Cycle Cost (DTC/LCC) features along with long-term warranty/maintenance features need to be imposed. The payoff for use of LSIC in low volume applications is normally long term rather than short term as for high volume applications. Incremental funding has a tendency to work against long term benefits. There needs to be some vehicle to offset this disadvantage.

It should also be recognized that the use of custom LSI in development programs requires the expenditure of "hard tooling" costs in this time period rather than in the production portion of the cycle. A certain amount of "hard tooling" funding must be made available during the development and prototype build cycle.

* * *

11. Avionic equipment procurement practices and policies should be modified to encourage the use of LSI devices. Specifically, procurement needs to emphasize minimum life cycle costs rather than minimum initial development costs and minimum acquisition costs for prototype systems.

LSI-based equipment designs are more reliable and cost less on a production basis than assemblages of catalog SSI and MSI devices. However, the initial design cost is often lower when available components are used. The current focus on minimizing acquisition costs saddles the equipment with an undesirable cost and reliability burden throughout the production cycle.

* * *

Question #10: In what ways could avionics equipment procurement practices and policies be changed to enhance the introduction of advanced semiconductor devices?

12. Requirements to use parts on existing qualified parts lists should be removed from all advanced development and most engineering development contracts. Instead, contractors executing on these programs should be required to specify VLSI device functions which are required to meet government-specified production size, weight, power, and cost goals. All advanced development and most engineering development, i.e., pre-prototype, programs should substitute modular implementations of the required VLSI functions. These modular implementations can be implemented using current off-the-shelf components and serve as high-fidelity models of the required VLSI chip developments. This approach allows a detailed assessment of the complexity (number of gates and bits of memory) of the proposed VLSI circuit development while providing a test bed for determining the functional requirements of the device.

* * *

13. a. Accept warranties, production guarantees, or purchase of an adequate supply of parts as an alternative to second source requirements and to protect against technology changes.

b. Where possible, extend lead times on avionics developments to allow the "risk" of custom development to be minimized. This may require more multi-year contracts.

c. Require life cycle cost to be considered when awarding prototype development contracts. These should include the cost of attributes such as size, weight, power, reliability, etc.

d. Remove lot traceability requirements.

e. Alter MIL-STD-217B to better apply to LSICs.

Question #10: In what ways could avionics equipment procurement practices and policies be changed to enhance the introduction of advanced semiconductor devices?

6. Allow military screening of commercial grade parts; don't insist on MIL-M-38510.

In a recent study of "large scale integrated circuits for military applications" for DDR&E by the Institute for Defense Analyses, it was shown that a decrease in avionics weight of one pound resulted in a total 6-8 pound weight savings in a miliary aircraft. Since the "flyaway" cost of a modern fighter plane is about $500/pound, LSI can save money by reducing the weight. For a satellite, this cost can be as high as $15,000/pound. The cost per watt has been estimated at $20 and $2,000 for a plane and a satellite, respectively. Increased reliability can again be translated into cost savings due to the reduced maintenance and spare parts requirements. Thus, more than acquisition costs should be considered in implementation studies.

* * *

14. Preference could be given to contractors who have the ability to design LSI devices, with emphasis on automated design. Use of advanced devices could also be evaluated favorably in the evaluation of proposals. A policy of purchasing all expected spares requirements at the time of the initial contract would alleviate the problem of obtaining them at a much later date. The necessary devices might be purchased as probed wafers and stored in a controlled environment.

* * *

15. The procurement practices must accommodate the limited life cycle of semiconductor technologies. This must include allowance for continued updating (i.e., redesign) of selected portions of systems.

Development times must be reduced to avoid designing during the life of one technology and trying to produce the equipment after the

Question #10: In what ways could avionics equipment procurement practices and policies be changed to enhance the introduction of advanced semiconductor devices?

technology peak has disappeared. This will also mean that "proven design" can no longer be a paramount consideration.

* * *

16. No comment.

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17. OEMs, upon receipt of a contract, should be authorized to make a one-time buy of all custom LSI parts in order to reduce the recurring lot charges. In this case, NAVAIR would assume all responsibility for the quantity ordered.

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18. No comment.

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19. No comment.

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20. No comment.

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K. Question #11: How should the Government LSI device standardization efforts be directed to minimize the proliferation of devices, but allow timely introduction of new LSI in avionics equipment?

Highlights:

Predominant suggestions resulting from the replies to this question are:

- Device standardization and timely introduction of new LSI in military systems seem to be mutually exlusive.
- Standardize on standard cell families and CAD techniques.
- Establish a national semiconductor LSI data base function to include forward projection of device needs and device developments.
- Restrict the technologies used.
- Focus on functional standardization at the module, interface, and device terminal levels.

Industry Replies:

1. Why not establish a standard parts list analogous to the previously established NAC module concept, which worked quite satisfactorily? In so doing, it would be well to coordinate to the greatest extent possible

Question #11: How should Government LSI device standardization efforts be directed to minimize the proliferation of devices, but allow timely introduction of new LSI in avionics equipment?

with other branches of the government to minimize the subsequent logistics support requirements supported by DSA.

* * *

2. a. Restriction of technologies in use.

b. Establishment of a national LSI device data bank accessible by computer terminal to military agencies and suppliers.

c. Standardization of CAD interfaces and of chip formats.

d. Availability of all chip design, mask, and test data of Navy-procured LSI designs to all contractors with an established need.

* * *

3. I feel that the two goals being considered here are diametrically opposite to one another. The standardization efforts to minimize proliferation of devices will automatically slow down the timely introduction of new LSI parts in avionic equipment. The standardization efforts will dictate that additional time be used to bring more vendors on line with a new part. This would certainly slow down the effort to get newer devices into avionics equipment. Moreover, NAVAIR volume is not going to be high enough to encourage vendors to expedite developments in order to meet the standardization requirements in a timely fashion.

* * *

4. Standarization in an area of rapidly changing technology is usually unsuccessful. Do not try to standardize too early.

* * *

5. The government should encourage forward projection studies as are presently being done by AIA and EIA, and publish this information to industry.

* * *

Question #11: How should Government LSI device standardization efforts be directed to minimize the proliferation of devices, but allow timely introduction of new LSI in avionics equipment?

6. No comment.

* * *

7. There are two viable levels of LSI device standardization that should be considered:

a. Architectural

In this standardization, the LSI architecture would be the same program code that could be run on all device families. For example:

- 8080, 8085, and 8086 from Intel
- Z-8, Z-80, and Z-8000 from Zilog
- Common interfaces such as 1553, RS-232, or IEEE-488

As these devices evolved from simple to higher levels of complexity, standardization which resulted in no changes to the program code used would be very beneficial to NAVAIR.

b. Device-based

In this standardization scheme, multiple chips could be merged into one complex function chip, such as Intel has done with the merger of the 8080 CPU, the Clock Generator, and the System Controller into the 8085 microprocessor. This merging of functions, especially if it can be implemented with no change to user programs, can significantly improve the introduction of LSI into Navy avionics equipment.

* * *

Question #11: How should Government LSI device standardization efforts be directed to minimize the proliferation of devices, but allow timely introduction of new LSI in avionics equipment?

8. Function standardization is a possible solution. For example, standardize a bus interface function, but do not specify the technology in which it must be implemented.

* * *

9. Standardization efforts should be focused at the SAM level to provide an added degree of insensitivity to LSI devices. The military-industrial complex has not found the need for, nor have they attempted to minimize the proliferation of hybrid devices. The use of LSI should not require military control significantly above and beyond that for hybrids.

Device standardization programs should concentrate on the high volume commercial LSI area, not on the quasi-standard of full custom LSI devices. For these high volume LSI devices, the present "mini-spec" issued by RADC/DESC should be used to inform other military complexes of their availability. Standardization should be based on a "moving window" in which new devices are added and devices fading away are deleted. Create an LSI standardization committee with the responsibility to review LSI needs at all phases of equipment development, including equipment R&D programs initiated by the DoD (Navy) laboratory community. A relatively small technically qualified group could strongly influence LSI standardization early in the development cycle and also maintain a sensitivity to LSI evolution as it affects military electronics.

* * *

10. The timely dissemination of information on previously designed LSICs and incentives for their use on new designs should go a long way to minimize proliferation of devices. However, there is danger in blindly following this approach. With the shorter life cycles of the IC technologies, nearly obsolete technologies could be designed into

Question #11: How should Government LSI device standardization efforts be directed to minimize the proliferation of devices, but allow timely introduction of new LSI in avionics equipment?

future equipment. Also, by defining system architectures, common functions can be better defined and standard LSICs developed.

* * *

11. Functionally partitioned systems can be updated to use LSI parts without several cost penalties. Proliferation of device types will result from the shift to LSI components since the greater logic complexity on a chip results in a more specialized chip function. General interface rules need to be used to define chip operation in a way that will make each LSI chip broadly useful to several agencies and contractors. These highly specialized custom LSI chips will be more cost-effective and give higher performance and better reliability than any assemblage of catalog parts. Stocking of spares and quick turnaround from stockpiled mask sets will make them available when needed.

* * *

12. See the response to Question 13. This indicates that careful attention should be directed at the beginning of an equipment development to assure a partitioning of discrete system functions consistent with the likely evolution of the components used to implement the function. This approach requires precise documentation of the form, fit, function, and signal interface on each system sub-function or partition. Implementation specifics such as power consumption, weight, and size should be specified as upper limits only to accommodate evolutionary re-implementations of the equipment to conserve these factors. General requirements for environmental conditions should also be specified. Above all, great care should be exercised to avoid specifying the subsystem function in a manner which denotes implementation technique specifics.

* * *

Question #11: How should Government LSI device standardization efforts be directed to minimize the proliferation of devices, but allow timely introduction of new LSI in avionics equipment?

13. a. The government could see that certain high usage standard devices (such as memories and microprocessor chips) are MIL-qualified such that they become de facto standards, and/or adopt commercial standard specifications.

b. Define standard military functions, enforce the standard, and fund development of prototype devices.

* * *

14. Use of the standard cell family approach, while not minimizing the number of devices, would allow for a great degree of standardization and encourage the use of new LSI. Basically, this gets back to the idea of owning both the designs and the process specifications, or placing them in the public domain.

* * *

15. Standardization for custom LSI devices should be directed toward encouraging the use of commercially accepted technologies.

* * *

16. Generally speaking, device standardization and timely introduction of new LSI are considered mutually exclusive. Consideration should be given to planned updates of standard devices--say every two to three years.

* * *

17. NAVAIR could make available a listing of specific LSI parts which are used in other equipment. The OEM's designs could possibly incorporate these same parts.

* * *

18. No comment.

* * *

Question #11: How should Government LSI device standardization efforts be directed to minimize the proliferation of devices, but allow timely introduction of new LSI in avionics equipment?

19. *Standardize on master chip families and associated software packages. On custom LSI, permit qualification on the basis of similarity.*

* * *

20. *No comment.*

* * *

L. Question #12: What documentation data should the Government require in order to realistically protect its interests in procuring and supporting avionics equipment?

Highlights:

Suggestions include:

- Utilize standardized documentation which is understood and accepted.
- Specify form, fit, and function only.
- Acquire all design and fabrication rights to custom LSICs developed on Government funding, including mask tapes, process specifications, cell descriptions, design rules, test tapes, qualification test and failure analysis data, etc.
- Insure second source viability.

Industry Replies:

1. The point in the LSI design process considered by manufacturers to be proprietary varies slightly from company to company. Almost without exception, semiconductor makers consider process parameters to be the secret ingredient which makes them better than competitors. Some process parameters affect mask design and are supplied to the government with great reluctance. The digitized data used for making masks is often supplied to equipment makers and ultimately to the government.

* * *

Question #12: What documentation data should the Government require in order to realistically protect its interests in procuring and supporting avionics equipment?

2. *No comment.*

* * *

3. *No comment.*

* * *

4. *The documentation should be similar to that required for simpler componentry. In very new and sophisticated componentry, gross process specifications may be appropriate.*

* * *

5. *Utilize standard documentation which is understood and accepted by the industry, i.e., Military Standard 38510 format. In addition, reliability data and complete electrical performance data as specified in MIL-STD-965 is needed. A strong standardization program would minimize the proliferation of data.*

* * *

6. *Tie the device specification to MIL-M-38510 requirements, but specify the parameters as maximum and minimum.*

* * *

7. *The Navy should follow the good example which it has set on the NAC SEM/SHP modules. That is, the Navy should specify only "form, fit, and function" (including performance parameters), but should not specify process-related parameters. By limiting its requirements to "functionally-specified," and not "design disclosure," the Navy can insure a more standardized functional family of LSI modules.*

* * *

8. *For a microcircuit supplier, a certificate of compliance should be adequate to insure that the device was manufactured to the requirements.*

* * *

Question #12: What documentation data should the Government require in order to realistically protect its interests in procuring and supporting avionics equipment?

9. At the SAM (assembly) level, the documentation requirements should be similar to those of MIL-M-28787. Particular areas of concern are the performance and test specifications and test procedures. Documentation should be limited to that necessary to functionally specify the SAM function (not the LSI devices within). The Navy documentation review and approval should assure testability and maximum technological transparency. This approach will allow development of replacement SAMs without requiring interchangeable advanced technology devices, and may very well result in reducing equipment acquisition costs through the introduction of competition via multiple SAM sources.

At the LSI device level, documentation data should be directed toward proof that a second source is available, not toward obtaining design/process details to the cookbook level. If data are required to show that a second source can produce the LSI devices in question, then true protection and support is ensured. Requiring a contractor to "tell all" (details in design and processing) rarely ensures that the devices can be made by another contractor in an emergency. Emphasis should not be placed on divulging processes (times and temperatures; equipment capabilities differ from contractor to contractor and may preclude direct copying of techniques), but on ensuring a second source for the parts. Make contractors prove that a second source exists in practice: masks exchanged, devices made and tested.

* * *

10. The government should acquire all design and fabrication rights to custom LSICs developed on government funding. Some sort of agreement should be worked out with the innovator of such designs so that he would receive some sort of royalty if the government or another contractor chose to purchase LSICs from those designs within a given number of years.

Question #12: What documentation data should the Government require in order to realistically protect its interests in procuring and supporting avionics equipment?

Any qualification test and failure analysis data on these devices should be procured by the government and made available to other potential users. See the response to Question 7.

* * *

11. LSI chip designs in one of the industry-standard techniques can best be documented in terms of the mask set used to fabricate the type and the program used to test it. Functionality and logic operation also need to be defined (as in a data sheet) to permit use by other contractors and government agencies. Characterization data should also be supplied to assure that the chips meet speed, drive, and other application requirements.

* * *

12. No comment.

* * *

13. a. Test data on the equipment itself, not on each component therein.

b. For custom LSI, the government must insist on masks and test documentation.

* * *

14. Design rules, process specifications, cell descriptions, and other information necessary to allow a variety of suppliers to manufacture the LSI. Mask tooling information is also necessary, but probably not stored in the form of physical masks. Coordinate information stored on magnetic tape would be superior because of the varying requirements for masks between different vendors. A complete description of the test vectors and test set-up required should also be made available.

* * *

Question #12: What documentation data should the Government require in order to realistically protect its interests in procuring and supporting avionics equipment?

15. The most important data is a functional specification which does not unduly restrict the method of implementation. No requirement should be specified which is not absolutely necessary to satisfy the intended application.

Since design disclosure data is essentially not available, cross-licensing certification should be considered as a method of insuring multiple sources.

* * *

16. Continue requirements for second source for components and procure sufficient design and process data to permit re-sourcing in accordance with these data.

* * *

17. Proprietary detailed design/process information could be contracted for and placed in bonded storage. This data should be sufficient to build parts, and as a minimum should consist of logic diagrams, magnetic tapes, test patterns, and detailed process steps.

* * *

18. No comment.

* * *

19. No comment.

* * *

20. No comment.

* * *

M. Question #13: If you, as a contractor, enter into a long-term warranty agreement with NAVAIR on a particular avionics equipment, how will you protect yourself against technology obsolescence?

Highlights:

Predominant comments were:

- Specify the function at the module level.
- Use long-term storage of wafers and/or devices.
- Make careful technology selection.
- Establish multi-sourcing of devices.
- Use a strong standardization program.
- Establish an in-house IC capability.

Industry Replies:

1. Semiconductor warranty is presently one year from the date of acceptance by our customers. It is possible that this warranty will be increased to two years in the future. We have not and see little possibility of entering into longer-term warranty situations.

The prime method of protecting against technical obsolescence is designing new equipment with new technology if multiple sources exist. Older technologies are discarded by producers when no longer popular or profitable.

* * *

Question #13: If [illegible], as a contractor, enter into a long-term warranty agreement with NAVAIR on a particular avionics equipment, how will you protect yourself against technology obsolescence?

2. No comment.

* * *

3. The two parts to this question are not really related. If a contractor enters into a long-term agreement with NAVAIR, then the contractor will set up a part of his operation to manufacture the required part to NAVAIR specifications. New avionics or technology will be covered under other contracts. A manufacturing area may continue producing obsolete parts under a certain government contract unless the contract calls for a continued upgrading of system devices and capabilities. Thus, the long-term warranty agreements are not directly related to technology obsolescence.

* * *

4. We would protect ourselves through modularity and the in-house facility.

* * *

5. As an aid toward solving this problem, we have a strong internal standardization and parts management program which maximizes the selection of long-term technologies which can be manufactured by more than one source. A long-term warranty agreement would require either warranty parts support by the procurement agency, or spares procurement coincident with production buys. Depending on the program, either method could be cost-effective. Additionally, NAVAIR might consider a program similar to the Air Force PRAM (Production Reliability Availability Maintainability) program. Under this program, items or spares which become difficult or non-cost-effective to support are modified or redesigned. The new design must be a form-fit-function replacement. This program has solved a number of difficult and costly long-term support problems.

* * *

6. No comment.

* * *

Question #13: If you, as a contractor, enter into a long-term warranty agreement with NAVAIR on a particular avionics equipment, how will you protect yourself against technology obsolescence?

7. We would concern ourselves with the function required, and not with the component which today might perform that function, but tomorrow may become obsolete.

If the Navy wants to repair electronic subassemblies in the field, it may be feasible to consider long-term bonded storage.

Before committing to a full production run, may be prudent to consider a technology upgrade, based on pin-for-pin and/or module-for-module replacements of equivalent functions.

The preferred method is to warrant the "black box" to a given function. Upon failure, the box would be returned to the manufacturer for repair or replacement. This repair-or-return activity could be done at any time with new technology which is transparent to NAVAIR.

* * *

8. As microcircuit suppliers, we are not the best people to answer this question. However, we would suggest that if you plan for technology updates, you can prevent obsolescence.

* * *

9. Form, fit, and function; and technology transparency as design philosophies (see answers to Questions 1 and 2) will provide the required protection against technology obsolescence. Every effort will be made to incorporate LSI into logical testable large function modules designed to maximize technology transparency (e.g., standard 5 volt supply, on-module BITE, etc.) We will maximize the use of SAMs.

When the source of supply becomes questionable for specific parts, advanced technology or otherwise, we will redesign the module

Question #13: If you, as a contractor, enter into a long-term warranty agreement with NAVAIR on a particular avionics equipment, how will you protect yourself against technology obsolescence?

to perform the same function but with up-to-date, procurable device technology. We may, as an interim measure, procure a larger-than-normal quantity of the device, or devices, in question as a hedge against schedule problems.

* * *

10. Usually in long-term warranty agreements where the original equipment designer and manufacturer has control of repairs and testing, there is more flexibility for incorporating and controlling design changes. Also, our Purchasing Department maintains good rapport with our vendors as well as following the industry trends. When one of our vendors decides he is going to discontinue providing certain parts, he usually notifies Purchasing and gives them a chance to make a final purchase of as many of the parts as they want. At this time a trade-off decision is made as to whether to redesign the part out of the system considering retrofit requirements, etc. or to purchase enough spares for the life of the equipments.

* * *

11. LSI parts are inherently reliable and will have a low failure rate. A modest quantity of spares will suffice for the life of the equipment. If excessive spares are required, the design or application is suspect, and redesign in a more modern technology or for a lower stress level in the application is in order.

* * *

12. Components used in an equipment implementation would be restricted to components which were members of a family of components having a strong linkage to a mainstream commercial product family and which were produced by at least one major semiconductor manufacturer, i.e., in the top four in domestic semiconductor sales. System design techniques would be encouraged which exploited the use of components likely to be developed as evolutions of existing members of the commercial component

Question #13: If you, as a contractor, enter into a long-term warranty agreement with NAVAIR on a particular avionics equipment, how will you protect yourself against technology obsolescence?

family. For example, system functional partitions would be established in a manner that would allow evolving implementations to naturally exploit evolutions in component technology. This approach is best exemplified by:

a. A medium scale integration (MSI) implementation using LSTTL components. Typically, this would require 200-300 components and 75 watts.

b. A microprocessor-based implementation using a microprocessor, memory devices, and a small number of LSTTL MSI components. Typically, this would require 30-40 components and 10 watts. This is representative of an LSI implementation.

c. The final implementation would use the very large scale integration (VLSI) technology coming available in the 1979-1980 period. With this approach, the function implemented in 12.a and 12.b can be implemented in a single chip microcomputer device. This approach requires one component and less than one watt of power. An important requirement is that the microprocessor used in 12.b and the microcomputer used in 12.c be members of a compatible family of computer components. Compatibility requirements include:

(1) Instruction set
(2) Memory architecture
(3) Input/output architecture

An additional aspect of this approach permits the combination of multiple system functions in a single microprocessor/microcomputer-based implementation.

Question #13: If you, as a contractor, enter into a long-term warranty agreement with NAVAIR on a particular avionics equipment, how will you protect yourself against technology obsolescence?

These actions at the beginning of the system development cycle provide an assurance that the equipment implementation must not, of itself, support the existence of the required components and that on-going component developments are likely to be compatible with components currently in use. Additionally, the business strength of the component supplier provides additional assurance of the continuing availability of the required or equivalent component functions.

Contractual arrangements would be negotiated which require the component manufacturer to notify the equipment manufacturer of changes in the product and/or production process which would prohibit availability of the required component function. The contract would have pre-negotiated quantities/prices for providing a reserve supply of components for future requirements.

The dual approach outlined maximizes the likelihood and the time period that the required component function will remain available. Furthermore, the system design technique tends to encourage the use of common component functions which are programmable to meet required equipment functions. This technique minimizes the number of different components used by the equipment implementation. Lastly, contractual procedures are outlined which provide for stockpiling components if the preceding measures become inadequate. These contractual procedures provide an acceptable level of risk for equipment and component manufacturers.

* * *

13. a. *Make our own custom LSICs.*

b. *Buy all chips we need in wafer form and store until needed if wafers are procured from outside. If internally produced and we wish to alter or discontinue the process, we would:*

Question #13: If you, as a contractor, enter into a long-term warranty agreement with NAVAIR on a particular avionics equipment, how will you protect yourself against technology obsolescence?

(1) Make all the wafers we need for the future.

(2) Produce in a form, fit, and function manner spare parts from the new technology.

* * *

14. By using a technology such as CMOS/SOS which can be expected to have a long life, and by using design rules acceptable to a large number of suppliers. In some cases, a quantity of devices sufficient for foreseeable spares requirements might be purchased, since there could be substantial savings available through quantity purchases.

* * *

15. No comment.

* * *

16. Long-term warranty agreements would apply only as long as vendors produce parts to the original or an analytically equivalent design. We would expect to renegotiate if parts are unavailable due to obsolescence/line shut-down; or try to tie any vendor to a production quantity that will satisfy any warranty agreement with any customer.

* * *

17. LSI parts which are used will be selected from proven technologies which are not likely to become obsolete in the near future. Devices normally will have more than one source, and lifetime spares may be procured in the event that the parts become non-procurable.

* * *

18. No comment.

* * *

19. Primarily by wafer storage (see answer to Question 14). We have also bought specific mask sets retained by the LSI manufacturer to

Question #13: If you, as a contractor, enter into a long-term warranty agreement with NAVAIR on a particular avionics equipment, how will you protect yourself against technology obsolescence?

assure that there will be no change during the production procurement lifetime. For small volume usage, we favor lifetime buys of packaged units.

* * *

20. The best protection is to implement current standard multisourced devices to the maximum extent possible.

* * *

N. Question #14: Comment on the concept and techniques for storing semiconductor devices in wafer form until logistics or mobilization needs require that they be diced, tested, and packaged. Comment on knowledge of the aging characteristics in wafer storage of the specific technologies with which you have had experience.

Highlights:

Comments finding concurrence among respondents are:

- Wafer storage is technically feasible; however, not practical because of management of peripherals such as masks, testing, packaging, etc., and economics.
- Store wafers in dry nitrogen (N_2)-rich environment.
- Leave the glass deposited over the chip metallization intact and continuous.
- Store fully packaged and tested devices.
- Store wafers for future logistics needs.

Industry Replies:

1. The concept of storing wafers is an excellent one. We would only like to encourage two considerations. First, the wafers should be stored in a nitrogen (N_2)-rich environment. Second, we would encourage leaving the glass deposited over the metallization intact and continuous. Do not etch the glass away from the bonding pads, thereby exposing the

Question #14: Comment on the concept and techniques for storing semiconductor devices in wafer form until logistics or mobilization needs require that they be diced, tested, and packaged. Comment on knowledge of the aging characteristics in wafer storage of the specific technologies with which you have had experience.

bonding area to any long-term oxidation. The risk factor is higher with this approach, but we believe reliability is certainly improved.

* * *

2. In principle, wafer storage is possible. In practice, however, it could be dangerous since semiconductor manufacturers might succumb to the temptation of shipping inferior products into storage. I believe that it is feasible to maintain a limited supply of semiprocessed wafers to achieve a fast turnaround for logic arrays, programmable logic units, etc.; but products for spares or later production should be inventorized fully packaged and tested.

* * *

3. The aging characteristics of semiconductor devices in wafer form (if placed in the proper environment) can probably be neglected. However, we do not have long-term data in this area. I feel that the major problem involved in trying to do what they want would be in trying to keep all the peripheral areas intact and in good shape for a long period of time. Tooling would get lost and testing programs would not be kept up-to-date. These kinds of things would be difficult to maintain in a high state of readiness with a high degree of confidence.

* * *

4. Semiconductor wafers could be stored in dry nitrogen with little or no apparent aging. I have a "gut feel" that due to the rate of the change of technology, they would probably not get used anyway.

* * *

5. Devices should be stored preferably in the packaged state; however, if storage in the wafer state is necessary, a dry nitrogen atmosphere is recommended along with reinspection prior to use.

* * *

Question #14: Comment on the concept and techniques for storing semiconductor devices in wafer form until logistics or mobilization needs require that they be diced, tested, and packaged. Comment on knowledge of the aging characteristics in wafer storage of the specific technologies with which you have had experience.

6. *No comment.*

* * *

7. *The best way to approach this problem would be to store "good die" from the wafers. The die would utilize less space and there would not be a need for wafer dicing or testing. The containers should be sealed and reside in a nitrogen atmosphere.*

Since we have no data on wafer storage aging characteristics, we cannot intelligently comment on this subject. However, the available aging with life data would indicate low risk in an intelligently managed wafer storage program.

* * *

8. *This concept is feasible. However, we recommend, on technical grounds, against wafer storage due to possible handling damage. Dice storage would be more advisable. Storage would have to be in a dry, dust free, inert environment. Aging should not be a problem.*

From an economic sense, NAVAIR would have to purchase the inventory and provide for its carrying cost. NAVAIR would also have the problem of procuring the packaging and testing operation when the dice had to be packaged. In addition, NAVAIR would have to warranty that the dice were good, beyond one year, since that is the semiconductor industry warranty period.

* * *

9. *If wafers are to be stored for logistic or mobilization needs, they must at least have been probe tested and a canned sample electrical test per wafer should be required. The wafers should come out of a*

Question #14: Comment on the concept and techniques for storing semiconductor devices in wafer form until logistics or mobilization needs require that they be diced, tested, and packaged. Comment on knowledge of the aging characteristics in wafer storage of the specific technologies with which you have had experience.

current production run in which final device yield statistics are available. The die required for the sample test could be taken from the wafer edge. The wafer should be stored in a dry box, back-filled with nitrogen. If wafers are procured and produced in large batches, extensive testing of a canned sample will assure more uniform device performance. This approach tends to reduce the lot-to-lot variations experienced in all semiconductor products by reducing the total number of lots and the time span in which they are produced. Substantial industry and military data is becoming available which indicates that aging is not a significant reliability risk and is predictable. For evolving and future technologies, accelerated aging testing will be necessary to assure predictable aging characteristics.

On the negative side, a policy requiring lifetime buys at the wafer level could have undesirable side effects. This policy may result in periods of high device manufacturing activity and periods of very low activity. From the manufacturer's point of view, there is a desire to maintain continuous production activity for obvious reasons.

* * *

10. Wafers, when stored for extended periods of time (more than six months) should be protected from corrosive or active gases, heat, light, and water. Preferable conditions include a hermetically sealed container, probably metal* providing a barrier to light and moderate electromagnetic

*Metal is suggested but not mandatory; however, the container material should provide static protection and not be a static generator. Additionally, it should not be a source of outgasing, vapors, or solids contamination. Therefore, the material itself should be carefully selected.

Question #14: Comment on the concept and techniques for storing semiconductor devices in wafer form until logistics or mobilization needs require that they be diced, tested, and packaged. Comment on knowledge of the aging characteristics in wafer storage of the specific technologies with which you have had experience.

and ionizing radiation. The atmosphere should be nitrogen at approximately one atmosphere of pressure and containing not more than 10 ppm of water.

No specific aging data has been volunteered by vendors; however, it is known that the above has yielded excellent results with heart pacer chips (wafers) stored for over a year.

* * *

11. We believe that parts should be stored in assembled tested form rather than as wafers. For LSI parts, the cost of the package is less than the cost of a good chip so that potential cost advantages of storage in wafer form are offset by the risks of storing unprobed chips on unprotected wafers in unclean environments. If it is desired to store parts in wafer form, then wafers should be fully tested and inked and complete test data stored for each good chip along with identification of the chip in the wafer matrix. All wafers should be stored in a flowing dry nitrogen ambient in a dust-free cabinet. Preferably a passivation technique should be used. Aluminum metallization cannot be exposed because it can corrode. We have experienced excessive leakage and lack of metal continuity in improperly stored CMOS wafers after several years.

* * *

12. Technically there is no major problem storing bipolar technologies and we do not anticipate any major problem with surface related devices. The real problems are associated with planning and maintaining the resources required to provide the testing and packaging of the devices over an extended period of time.

* * *

Question #14: Comment on the concept and techniques for storing semiconductor devices in wafer form until logistics or mobilization needs require that they be diced, tested, and packaged. Comment on knowledge of the aging characteristics in wafer storage of the specific technologies with which you have had experience.

13. The following technique involves the production, testing protection, and storage of low-cost semiconductor wafers in quantities sufficient to meet all expected usages in a military system. This quantity would be based on the maximum number of production systems expected, the expected system life, and expected failure rates, and a suitable safety factor. With the wafer sizes increasing and the device geometries decreasing, a very large number of LSICs can be realized in a limited number of wafers. For the small volume inherent in military systems, the nonrecurring costs predominate and the production cost of thousands of devices is small compared to the development and cost of producing hundreds. It is also small compared to the cost of obtaining a second source.

The concept of storing relatively inexpensive wafers for low volume, long-term needs has been around in various forms at semiconductor houses for quite a while. Every designer has a desk full of wafers or partial wafers that weren't needed to fill immediate customer needs, but he's saving them, "just in case." It is also common today to store "verification wafers" for parts that are manufactured periodically. These wafers are stored for years by semiconductor vendors and used every time a new run is complete. They use these wafers to verify the test setup and the test program (for automated testing) by comparing present-day readings with the values obtained when first tested.

Designers' experience with storing wafers suggests that it is a reasonable thing to do provided a few pitfalls are avoided. The wafers must be protected against various contaminations such as sodium (from fingers or dirty handling tools), as well as oxidation of the aluminum. The very nature of completed wafers makes them subject to both these killers.

Question #14: Comment on the concept and techniques for storing semiconductor devices in wafer form until logistics or mobilization needs require that they be diced, tested, and packaged. Comment on knowledge of the aging characteristics in wafer storage of the specific technologies with which you have had experience.

The wafer is coated with oxide, but in order to electrically test the die, the coating is etched to expose the bonding pads. The etching can introduce stresses that tend to "crack" this coating.

One technique that has a good chance to making this concept practical begins with the ability to deposit a high quality oxide over the wafer's active surface. One well-known electronics center has developed a low temperature nitride coating process. (Nitride is the best quality oxide available to semiconductor technology.) If the die on the wafer are electrically tested to determine if the wafer is worth storing, before the nitride coating is deposited, then there would be no need to etch the nitride until the die are needed. Thus stresses can be avoided, and the bonding pads will not be exposed. With a good quality nitride coating, the wafer is "sealed" and thus not subject to contamination or oxidation. Compared to conventional silox coatings, nitride will "seal" the surface such that wafers can be stored in an inert atmosphere in a dry box for a very long time. The die are still subject to high infant mortality rates and testing difficulties, and should be burned in when they are packaged; but the primary factors involved in long-term storage deterioration can be minimized with this nitride seal.

To avoid supplier catastrophe, these wafers can be stored in more than one location, and by processing partial wafers (pieces as small as 1/3 wafer can easily be handled for etching and testing), the total value of inventory can be reduced.

* * *

14. The concept is excellent provided that the wafers are first probe tested. They should be stored in a dry inert atmosphere at room

Question #14: Comment on the concept and techniques for storing semiconductor devices in wafer form until logistics or mobilization needs require that they be diced, tested, and packaged. Comment on knowledge of the aging characteristics in wafer storage of the specific technologies with which you have had experience.

temperature or lower. Storage life should be as good or better than storage life of packaged devices. Of course, if the surface is unstable in the first place, it will remain unstable whether the devices are packaged or stored in wafer form.

Although no specific data is available, personal experience has indicated that devices stored in a dry box which was kept in a clean room did not change over a five-year period.

* * *

15. No comment.

* * *

16. No comment.

* * *

17. Die should be selected from each wafer lot, packaged, and fully tested in order to prove the performance of the wafer lot. The remaining die can most effectively be stored in wafer form in a sealed container with dry nitrogen back fill.

* * *

18. No comment.

* * *

19. The concept of storing semiconductor devices in wafer form for future needs will be implemented when the need occurs. We have no present need. We have stored wafers as a contingency in the past (RTL logic) but were not funded for aging tests, nor were the devices ever used.

* * *

20. No comment.

* * *

O. Question #15: How can the procurement specifications for complex LSI devices be standardized to reduce the redundancy of documentation while requiring less effort on the part of suppliers in providing the specified testing, etc.?

Highlights:

Predominant comments were:

- Utilize the MIL-M-38510 approach for LSI.
- Emphasize form, fit, and function specifications only.

Industry Replies:

1. No comment.

* * *

2. No comment.

* * *

3. No comment.

* * *

4. This would require considerable study and effort. However, the use of certain generic types of devices coupled to certain types of test patterns can aid in this area.

* * *

5. Standardize on test methods and specification format as specified in MIL-STD-883 and MIL-M-38510, respectively.

* * *

6. Tie procurement specifications into a realistic MIL-M-38510 slash sheet.

* * *

Question #15: How can the procurement specifications for complex LSI devices be standardized to reduce the redundancy of documentation while requiring less effort on the part of suppliers in providing the specified testing, etc.?

7. a. Fund an agency, ideally a user, to define the characteristics electrically and allow for these characteristics to be specified for the MIL-M-38510 device prior to full qualification.

b. Allow "off-shore" build.

c. Utilize the MIL-M-38510 approach only to improve on "turnaround time" and standardize the product mix, and not as a universal specification requirement.

* * *

8. Establish one basic standard and insist on adherence to it.

* * *

9. In cases where custom LSI is being used in a SAM, very careful consideration should be given to the elimination or minimization of the detail device specification. The creation of an artificial intermediate level (LSI) device specification may have very little value to anyone and can result in considerable expense. If required, they should be purely form, fit, and function. If a second source for the device is available, the critical documentation will be the manufacturing build and test-related documents.

Current practices are not all that bad. In order to assure that each vendor knows the requirements and that the procurer will have a minimal problem of interchangeability between vendors' devices, the present system seems adequate except in the area of functional test (test vectors). The availability of test vector translators will reduce the efforts of both supplier and user. If possible, standardization efforts between agencies (NASA, NSA, Navy, Air Force, etc.) would be beneficial.

Question #15: How can the procurement specifications for complex LSI devices be standardized to reduce the redundancy of documentation while requiring less effort on the part of suppliers in providing the specified testing, etc.?

Generally speaking, equipment manufacturers prefer to structure test programs that precipitate failures at the lowest possible level, as this is usually the least expensive approach. Reducing commercial LSI supplier testing may be counter-productive and result in higher equipment costs due to increases in the equipment manufacturer's test costs. The cost of tooling a commercial LSI supplier (e.g., Intel, TI, etc.) and resulting recurring test costs, will be substantially less than establishing a device level test capability for each equipment manufacturer. This has been proven true in the past and will be so in the future. There is a reluctance on the part of commercial LSI suppliers to perform adequate testing because of competitive pressures. Effective test specifications will preclude vendor short cuts and the 50% LSI yield losses being experienced today by some equipment manufacturers at their incoming test operations.

* * *

10. The question can best be answered by suggestions from the suppliers themselves. Once the suppliers agree to a common approach, the suggestions should be submitted to the users for comment before incorporating them.

* * *

11. Procurement specifications in the MIL-M-38510 data sheet format seem sufficient to provide protection to the using agency. What is needed is rapid generation and availability of these data sheets from the appropriate agency.

* * *

12. The procurement specifications for VLSI circuits must be developed quickly with the manufacturer and/or manufacturers; however, due to the initial investment and volume usage of VLSI circuits, there

Question #15: How can the procurement specifications for complex LSI devices be standardized to reduce the redundancy of documentation while requiring less effort on the part of suppliers in providing the specified testing, etc.?

will be limited sources, and in many cases sole source suppliers. This will dictate very close liaison between supplier and vendor. Under current government regulations, this would suggest that future requirements from the government should be defined as system requirements, and place the responsibility on the equipment manufacturers to handle LSI/VLSI component selection and procurement.

* * *

13. Adopt a format which is similar to a commercial part data sheet. This would cover performance data. Quality and reliability documentation could be obtained by referencing existing documentation, such as MIL-M-38510.

* * *

14. Specify parametric testing on the basis of a standard test chip, and provide the test vectors and test set-up to be used for testing the wafers and packaged devices.

* * *

15. Procurement specifications should follow the general format of MIL-M-38510. Each requirement should be carefully considered relative to importance and overall impact on cost and long-term availability of the device. Above all, the specifications should clearly state the requirements and be devoid of ambiguities. Use of specification jargon should not mask the communication of requirements.

* * *

16. Use the format used by MIL-R-5757, which has basic requirements with a slash sheet covering the unique requirements for the device.

* * *

17. No comment.

* * *

Question #15: How can the procurement specifications for complex LSI devices be standardized to reduce the redundancy of documentation while requiring less effort on the part of suppliers in providing the specified testing, etc.?

18. No comment.

* * *

19. a. Coordination has been attempted between the government (DESC, RADC/RBRM, NAVELEX, SAMSO, NSA, NASA, etc.) and Industry (EIA, JEDEC, AIA, etc.) to standardize LSI procurement specifications. The results of these efforts have been minimal in proportion to the effort expended. Users shade their specifications toward high performance for a particular system rather than high yield with a compromise on performance. Manufacturers individually cater to these demands wherever there is a profit, while at the same time voicing an Industry Association position for a common specification. A firm commitment by DoD to enforce coordinated standardization at a performance level consistent with high level yield would be a step in the right direction.

b. In many cases the test requirements to meet government specifications differ from the manufacturer's standard product line. Coordination in this area could also be productive.

c. Strictly restricting government specifications to form, fit, and function would also help.

* * *

20. Issue MIL-M-38510 specifications/qualified parts lists. This will provide for common documentation and manufacturer processing and testing.

* * *

APPENDIX A

DEPARTMENT OF THE NAVY
NAVAL AVIONICS FACILITY
INDIANAPOLIS, INDIANA 46218

IN REPLY REFER TO:
908:RRJ:gh
5200
5 OCT 1977

Dear Sir:

The timely use of large scale integrated (LSI) circuits in Navy avionics equipments promises advantages such as lower cost, smaller hardware size, reduced power consumption, and improved reliability. However, the use of LSI poses problems related to the limited quantities required, long-term logistics support, and potential mobilization needs.

How should the Naval Air Systems Command facilitate the use of advanced technology microcircuits in avionic systems, while insuring adequate support of logistics and potential mobilization needs?

With input to this question and others from a broad spectrum of both industrial and Governmental activities involved in advanced electronic technologies and their applications, the Naval Avionics Facility, Indianapolis (NAFI), in support of the acquisition management wing of the Naval Air Systems Command, is working to formulate a management program for utilization and configuration control of commercial large scale integration and other advanced electronic technologies comprising Fleet hardware.

Your comments and suggestions to the questions provided as enclosure (1) are invaluable to the formulation of this program. Enclosure (1) is not to be considered as inclusive, so other considerations are solicited. Also, please provide the respondent information as requested by enclosure (2).

It is emphasized that this is a survey and this request does not commit the Government to pay any costs incurred in the submission of your input.

All communications or questions regarding this survey should be directed to Ronald R. Jennings at (317) 353-3080.

908:RRJ:gh
5200

In order to facilitate evaluation of the comments received, it is requested that your reply be forwarded to the following address on or before 25 November 1977:

Commanding Officer
Naval Avionics Facility
Attn: R. R. Jennings, Code 908
6000 East 21st Street
Indianapolis, Indiana 46218

Thank you for your consideration and assistance in this matter.

Sincerely,

ROBERT J. BARNETT
Acting Director of Engineering

Encl:
(1) Survey on Managing the Timely Introduction of Large Scale Integrated Circuits into Military Avionics
(2) Respondent Information

SURVEY ON MANAGING THE TIMELY INTRODUCTION
OF LARGE SCALE INTEGRATED CIRCUITS
INTO MILITARY AVIONICS

1. How should the Naval Air Systems Command (NAVAIR) facilitate the use of advanced technology microcircuits, while insuring adequate support of logistics and potential mobilization needs, and protecting itself against supplier catastrophe?

2. How should NAVAIR protect itself from the ever-increasing problem of devices/technologies that become obsolete (unprocurable) during the operational life of avionics equipment?

3. Faced with an ever-decreasing market life cycle for semiconductor devices/technologies, how are the commercial/industrial producers/customers dealing or going to deal with device obsolescence?

4. How should complex LSI devices be specified to insure adequate performance, and assure quality and reliability?

5. How can LSI device qualification and requalification be accomplished at reasonable costs?

6. Please comment on the problem of testing complex LSI devices.

7. What should be done to make custom LSI circuit development costs and turnaround times affordable to NAVAIR and its contractors, with low system and schedule risks?

8. What semiconductor technologies are required for future avionics systems that will not be available in a timely manner as spin-offs from non-military products? What developments should be funded by NAVAIR? Why?

9. What changes should be made to existing MIL-specifications, standards, requirements, and policies to facilitate the introduction of advanced LSI technologies? (Be specific.)

10. In what ways could avionics equipment procurement practices and policies be changed to enhance the introduction of advanced semiconductor devices?

11. How should Government LSI device standardization efforts be directed to minimize the proliferation of devices, but allow timely introduction of new LSI in avionics equipment?

12. What documentation data should the Government require in order to realistically protect its interests in procuring and supporting avionics equipment?

ENCLOSURE (1)

13. If you, as a contractor, enter into a long-term warranty agreement with NAVAIR on a particular avionics equipment, how will you protect yourself against technology obsolescence?

14. Comment on the concept and techniques for storing semiconductor devices in wafer form until logistics or mobilization needs require that they be diced, tested, and packaged. Comment on knowledge of the aging characteristics in wafer storage of the specific technologies with which you have had experience.

15. How can the procurement specifications for complex LSI devices be standardized to reduce the redundancy of documentation while requiring less effort on the part of suppliers in providing the specified testing, etc.?

16. Please discuss other considerations that you feel are important.

RESPONDENT INFORMATION

1. Name of person responding to the survey questions:

   _____

2. Mailing Address:

   Agency: _____

   Mail Code: _____

   Street: _____

   City, State, Zip Code: _____

3. Telephone Number: ( ) _____
   Area Code Number

4. May we contact you for further information? Yes_____ No_____

5. Would you be available for an on-site interview? Yes_____ No_____

6. Should another person at your facility be contacted?

   _____ ( ) _____
   Name Area Code Telephone

ENCLOSURE (2)

APPENDIX B

LIST OF ACRONYMS

ALU	Arithmetic Logic Unit
AR-	Aeronautical Requirement
CAD	Computer-Aided Design
CCD	Charge Coupled Devices
CMOS	Complementary Metal-Oxide Semiconductor
CMOS/SOS	CMOS/Silicon-on-Sapphire
DDR&E	Director of Defense Research and Engineering
DESC	Defense Electronics Supply Center
DIP	Dual In-Line Package
DMOS	Double-Diffused Metal-Oxide Semiconductor
D-VMOS	Double-Diffused Anisotropically Etched Metal-Oxide Semiconductor
DSA	Defense Supply Agency
DTC	Diode-Transistor Logic
ECL	Emitter-Coupled Logic
ECOM	Army Electronics Command
EIA	Electronic Industries Association
FPLA	Field Programmable Logic Array
GaAs	Gallium Arsenide
GFE	Government Furnished Equipment
IC	Integrated Circuit
I^2L (IIL)	Integrated Injection Logic
JEDEC	Joint Electron Device Engineering Council
LST^2L (LSTTL)	Low Power Schottky Transistor-Transistor Logic
MESFET	Metal Semiconductor Field Effect Transistor
MIC	Microwave Integrated Circuit
MOS	Metal-Oxide Semiconductor
MSI	Medium Scale Integration
NASA	National Aeronautics and Space Administration
NAVELEX	Naval Electronics Systems Command
NMOS	N-Channel Metal-Oxide Semiconductor

NSA	National Security Agency
NSWC	Naval Surface Weapons Center
NTDS	Navy Tactical Data System
PLA	Programmable Logic Array
PMOS	P-Channel Metal-Oxide Semiconductor
PROM	Programmable Read-Only Memory
RADC	Rome Air Development Center
RAM	Random-Access Memory
ROM	Read-Only Memory
RTL	Resistor-Transistor Logic
SAMSO	Space and Missile Systems Organization (USAF)
SOS	Silicon-on-Sapphire
SSI	Small Scale Integration
STTL	Schottky Transistor-Transistor Logic
T^2L (TTL)	Transistor-Transistor Logic
VLSI	Very Large Scale Integration
VMOS	Anisotropically Etched Metal-Oxide Semiconductor

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