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MODELING OF III-V FIELD EFFECT TRANSISTORS.(U)
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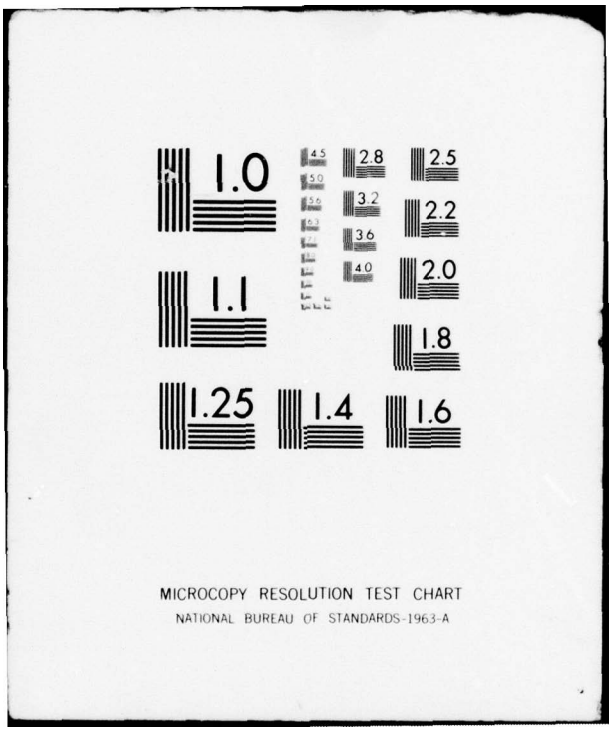
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MODELING OF III-V FIELD EFFECT TRANSISTORS

Final Scientific Report

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MODELING OF III-V FIELD EFFECT TRANSISTORS

Abstract

A two-dimensional time domain computer program has been formulated for investigating device physics of III-V field effect transistors. The program, with our modified version of Hockney's algorithm[1] for solving the two-dimensional finite difference Poisson's equation, is about two orders of magnitude faster than comparable programs using over-relaxation techniques[2-3]. The increase in computational speed makes it practical to simulate time domain behavior of the device in details. Internal mobile carriers and electrostatic potential distributions and the drain current can be examined as functions of time when the device is subjected to a time-step input signal. Relevant information is then derived from the large signal impulse response.

Using this technique we investigated the effect of gate length to channel width ratio, high field domain formation, tailoring of doping profile, vertical vs planar FETs and comparison of the GaAs and InP FETs. Additionally, the device cut-off frequency and intrinsic delay time as functions of gate length were determined. Significant findings are: 1) The dynamic transfer characteristic (drain current vs. time-step gate voltage) of the FET is like that of a series R-C circuit. 2) The device behavior depends strongly on the gate length to channel depth or L_G/d ratio. 3) For planar devices with a

$L_G/d < 4$ the static I_D-V_D characteristics have a pronounced slope beyond current saturation due to carrier injection into the semi-insulating substrate. 4) The f_T and the device intrinsic delay time are not determined by the metallurgical gate length alone due to the two-dimensional effect creating depletion regions extending beyond the gate. The simulation of InP FET was carried out over a limited range of operation.

Objectives and Accomplishments

The objectives of the past year's efforts are the following: 1) Develop the model and formulate the relevant mathematical equations needed to obtain a quantitative description of field-effect transistor physics, 2) Modify the existing subroutines developed under contract F44620-76-C-0043 in order to include time-dependent carrier response to electric field, carrier trapping and more flexible boundary conditions for the simulation of different device configurations, 3) Simulate and study device physics of planar GaAs and InP FETs and 4) Simulate and study device physics of vertical GaAs and InP FETs.

All the objectives with the exception of the study of effects of carrier trapping have been fully achieved. In the sections that follow we describe (a) the model, the physical mechanisms and the mathematical equations used in the computer program, (b) modification of Hockney's algorithm and the subroutine developed under F44620-76-C-0043 for simulations of planar and vertical FETs (c) major results of our investigations. A brief summary is given in section (d)

(a) The Computer Program

The physical models for the planar (one-sided) and vertical* (two-sided) are shown in Figure 1. The device internal physical effects treated in our program are the following: two-dimensional carrier transport from electric field and diffusion; carrier and charge conservation during transport and avalanche process; space charge effects resulting from mobile and fixed charges; field and time dependent avalanche process; nonlinear field-dependent carrier velocities and velocity over-shoot when applicable. The external boundaries are: ohmic contacts on the source and drain, Schottky barrier on the gate electrode, electrode voltages, and conservation of terminal currents.

The equations governing the two dimensional device are:

Poisson's equation

$$\nabla^2 \phi = -\frac{}{} (N_D + p - n) \tag{1}$$

and carrier transport equation

$$\left.\begin{aligned} \nabla \cdot (n \vec{v}_n) + \frac{\partial n}{\partial t} \\ \nabla \cdot (p \vec{v}_p) + \frac{\partial p}{\partial t} \end{aligned}\right\} = \alpha_n \; n \, | v_n | + \alpha_p \, p \, | v_p | \tag{2}$$

The symbols used in the above equations have the usual meanings. Experimental v-E characteristic for GaAs or InP is used in determining carrier velocities depending on the device material being simulated. However, instead of the electric field alone,

*We use the term 'vertical' to suggest the actual construction of such dual gate F.E.T.s on a substrate which would serve as the source.

the force field is defined to include diffusion so that

$$\vec{f}_n = \nabla\phi - \frac{T}{n}\nabla n \qquad \text{for electrons}$$

and

$$\vec{f}_p = -\nabla\phi - \frac{T}{p}\nabla p \qquad \text{for holes.}$$

These forces as defined are consistent with the concept of the quasi-fermi potential and are used in place of the electric field in the v-E characteristics. In this way the carrier saturation velocity cannot be exceeded, which would be the case if the electric and diffusion forces are treated separately.

To obtain good resolutions in the simulation, the two-dimensional device is devided into 96x48 cells as shown in Figure 2. Equations (1) and (2), in finite difference form, are computed using the explicit technique. Stable solutions of the transport equation are ensured by choosing the time increment $(\Delta t)_t$ (subscript t for "transport") such that

$$\frac{(\Delta t)_t}{\Delta x} \cdot v_{max} \leq \frac{1}{\sqrt{2}} \qquad (3)$$

where v_{max} is the maximum velocity a charge carrier can achieve. For computer economy, a larger time increment $(\Delta t)_p = m\ (\Delta t)_t$ is used for updating the Poisson's equation. The value of the integer, m, is determined by the size of $(\Delta t)_t$ and the device time constant. Typically, m ranges from 2 to 8.

(b) Modification of Previous Sub-routines

Sub-routines developed under AFOSR contract F44620-76-C-0043 for bipolar device simulation were modified for FET applications. However, one of the sub-routines, the Hockney fast algorithm for solving Poisson's equation, was found not to be compatible with the boundary conditions required to describe the FET. This difficulty was resolved by incorporating an innovation that is discussed here.

The FET, as shown in Figure 2, contains both Dirichlet and Neumann boundaries, while the Hockney technique is applicable to either, but not mixed, boundaries. In addition, the extent of the boundary is time dependent. To alleviate the difficulties, the Newmann boundary, which arises from the gate depletion region, is converted into Dirichlet in each time increment $(\Delta t)_p$. This could be done because no current can flow across the exterior boundary (x=a) of the depletion region; thus the condition $\frac{\partial \phi}{\partial x}\Big|_{x=a} = 0$ prevails. This condition, together with the known doping density and potentials at all electrodes permits the evaluation of $\phi_1(a,y,t)$ and $\phi_2(a,y,t)$ in Figure 2 via the one-dimensional Poisson equation in y. Thus, the potential $\phi(a,y,t)$ for $a \leq y \leq b$ is completely specified. The function $\phi(a,y,t)$ is Fourier-analyzed for each $(\Delta t)_p$. The resultant Fourier components are then applied to appropriate locations in Hockney's algorithm. This procedure is repeated for the boundary at x=0 for the vertical FET. The boundaries at y=0 and y=b are considered as planes of even symmetry appropriate to the cosine expansion used in the Fourier

analysis. Such symmetry property implies that the E_y is zero at these edges and does not produce error as long as the source and drain electrodes extend sufficiently inward.

(c) Major Results

At the inception of present work, it was decided that instead of a sinusoidal signal, a time step input would be used in probing the device. As will be seen later, the large signal impulse response produced more information on the device physics. Furthermore, a time step signal is consistent with logic device operation of the FET, which is of major interest at present.

In the simulation, the device was connected in the common source configuration with a fixed drain bias. The gate voltage V_{GS} was positive and equal to the Schottky barrier potential for $t < 0$. At $t=0$, the gate voltage was switched instantaneously to a negative value. The mobile carrier and electrostatic potential distributions and the drain particle current were then recorded as functions of time starting at $t=0$. For computer economy, a doping density of 5×10^{15} cm^{-3} in the active region and a channel depth of 1μM were used. For our purposes, these parameters do not restrict the validity of the computational results; the result for higher doping level can be scaled from that for the 5×10^{15} doping. The main physical variable in the investigation was the gate length. The major results are presented in the following sub-sections.

(1) Impulse Response

The drain currents under impulse conditions, for three different gate lengths, are shown in Figure 3. The devices simulated had a pinch-off voltage, V_p of 3.77V, according to the gradual channel approximation, while the gate input was -4V. In the long gate case ($L_G/d=8$), except for the slight Gunn oscillation, the semi-log plot of I_D versus t is indeed a straight line. Thus, the dynamic transfer characteristic of the FET can be represented by a series R-C circuit. The device time constant τ determined from the slope is related to the transconductance cut-off frequency by the relation[4]

$$f_o = \frac{1}{2\pi\tau} \tag{4}$$

Effects of L_G/d ratio are apparent when the drain current waveform is inspected. We shall discuss the gate length mostly in terms of this ratio rather than the absolute value of L_G. The dividing line between a long gate and a short gate device appears to be $L_G/d=4$. The short gate devices have two distinct features: softer pinch off at $V_g \geq V_p$ and larger degree of current oscillation. The time constant of short gate devices was determined from the initial slope of the drain current as indicated in Figure 3. For large values of t, the drain current becomes saturated permitting the study of steady state behavior.

A critical observer may note that the magnitude of the initial current in Figure 3 does not scale inversely with the length. This could be accounted for by the geometrical effect on the electric field and the peculiar velocity-field characteristic of GaAs. In the following sub-sections the dynamic behaviors, drived from impulse response, are described.

(2) Gunn Oscillation

Formation of a high field domain in the gate-drain region has been observed in two-dimensional computations [5-9]. Grubin[5] pointed out that the high field domain is not necessarily of negative differential mobility in origin, rather it could also arise from the geometrical effect within the FET. Additionally, Gunn oscillation has also been reported. Grubin[5] found that the oscillation can be suppressed by increasing the drain bias voltage while Yamaguchi et al.[9] defined a stable region where the channel depth is reduced to certain values. Our computer simulation not only supports these findings but also illustrates how and where the Gunn region exists.

Since the high field domain is of interest in understanding the GaAs FET device physics[10,11], we show our computational results in some details here. The time evolution of the mobile charge distributions in a short

gate ($L_G/d=2$) device under impulse conditions are shown in Figure 4. Although hundreds of carrier distribution frames are computed for one computer run, only pertinent snap shots are displayed to illustrate the device behavior. The undulation of the conducting channel, as shown in frames from t=40 picoseconds to t=68 picoseconds, is two-dimensional and Gunn effect in origin. These frames cover a time duration in the current saturation region (See Figure 3) and thus the oscillation is a steady state as well as transient behavior. At t=40 psec. the channel is widest near the drain. As the bulge disappears into the drain, a new one is initiated near the source. The cycle is complete at t=68 psec. The Gunn oscillation is further demonstrated by the potential distribution in Figure 5. By examining the time dependence of the equipotential lines, it is apparent that the most active region is in the conduction channel. This accounts for the strong Gunn oscillation in short-gate device since the drain voltage penetrates deeply into the channel. The steady state potential distribution in a long-gate device is also given in Figure 5 for comparison. The main body of the high field region appears to be "stationary" except for the slight shifting of the equipotentials.

Increasing the drain voltage diminishes but does not completely suppress the Gunn oscillation, as demonstrated

by the current waveform in Figure 6. Such undulating field region is not determined by the absolute value of the channel depth alone, rather it is a function of L_G/d ratio as illustrated in Figure 3. This is consistent with Yamaguchi's results since his stable region is found at $L_G/d>4$. Although Gunn oscillation can be minimized (5,9), in all our calculations it never completely disappears even after a very long time ($t>10\tau$). The fact that the drain current may appear to be relatively quiescent while the internal carriers go through two-dimensional undulation is because the drain current is an integral of the carrier motions. We suggest that the so-called "stationary" domain, based on external current observation, may only be an approximation to what actually transpires internally in the GaAs FET. It is noted, however, that our computations are far from exhaustive.

(3) Cut-Off Frequency and Switching Delay

Numerical result of the transconductance cut-off frequency as a function of gate length for the GaAs FET is shown in Figure 7. The values were determined from the impulse response drain current and equation (4). Carrier velociy over-shoot was neglected in these calculations because it was found[10,11] that this effect is insignificant for gate length of 1.0 μm and longer.

In an actual device, carriers are injected into the source region through an ohmic contact and traverse a finite source region before reaching the gate. Thus, the overshoot effect is not as significant as calculated in the case of one-dimensional approximation and using a more abrupt electric field slope.

For short-gate cases, velocity saturation takes place in the conducting channel and $f_o \approx f_T$, the current gain cut-off frequency. Although for a given device, f_T depends on operating parameters[12], our results compare favorably with published experimental data[12-15]. Thus, f_T as determined from the impulse response corresponds to that deduced from measurements at $V_{GS}=0$. It should also be noted that the two-dimensional simulator accounts for depletion regions at both ends of the gate. Consequently, the effective gate length is appreciably longer than the metallurgical value as suggested by Engelmann and Liechti[12]. The effective gate length probably accounts for the difference between our f_T and the one-dimensional results of Maloney and Frey[16].

The intrinsic device switching delay was also determined from the i_D-t characteristics. The delay time is defined as the duration in which the drain current is reduced to 10% of its intitial value. For nonpinched off cases such as in Figure 3 the initial slope was extrapolated to the 10% level. The delay time vs. gate length is

shown in Figure 8. Unfortunately, there is only one experimental data point[13] to compare with our results. According to Figure 8, the GaAs FET appears to be intrinsically a very fast logic device.

(4) Substrate Current

As demonstrated earlier, short gate ($L_G/d < 4$) GaAs FETs are prone to Gunn oscillation and require a larger gate voltage to effect pinch-off. The mechanism for these peculiarities is the deep penetration of drain voltage into the conducting channel as shown in Figure 5. In planar short gate FETs the deep penetration also causes carriers in the conducting channel to be injected into the semi-insulating substrate. The effect is demonstrated in Figure 9 where carrier densities in the substrate of a short- and a long-gate devices are compared. It is apparent that the substrate current is significant in the short-gate but not so in the long-gate device. Since the origin of carrier injection is in the drain voltage, we suggest that this is the mechanism for the pronounced rising slope of the drain current beyond the saturation point in sub-micron gate ($L_g \tilde{<} 1/4$ μm) devices[17]. As the gate length is made smaller, it becomes increasingly difficult to maintain uniform L_G and/or d in practice and hence the soft-pinch off behavior is determined by a region with the lowest L_G/d

ratio. Thus, our result implies that there might be a practical lower limit on the gate length base on device performance with current technology. Similar computation results on substrate current have been reported by Reiser[18]. However, he did not consider it as a function of gate length.

(5) Doping Profile

Tailoring of doping profile along the gate width has been reported by Siliger and Ward[19]. With a certain variation of N_D as a function of z (direction along the gate width) the linear dynamic range of the device was increased by several orders of magnitude.

We found that tailoring of doping profile along the gate length (y direction in Figure 2) can significantly increase the cut-off frequency f_o. A 2 μM-gate device with an exponentially tapered profile has an f_o=13.5 GHz as compared to 9 GHz for the uniform profile. In this device the doping density varied from 10^{16} cm^{-3} at the source to 10^{15} cm^{-3} at the drain. The increase in f_o is due not only to the higher conductivity in the source region, but also to the net lowering of the gate-to-source distributive capacitance.

A one-step doping variation along the gate produced an even more dramatic result. The doping level is $1 \times 10^{16} cm^{-3}$ from source to the middle of the gate and

$1 \times 10^{15} cm^{-3}$ from there to the drain. This doping scheme effectively moves the source to the middle of the gate, thus increasing the f_o to 17 GHz. It is not unreasonable that the f_o is higher than the 1 μm-gate device (see Figure 7) since the effective channel length is actually shorter. A comparison of impulse response drain current for the three types of doping profiles is given in Figure 10.

(6) GaAs vs. InP FETs

Barrera and Archer[20] found that for a one-μM gate device the InP FET has an f_T of 20 GHz as compared to 13 GHz for GaAs. They attribute the difference to the higher peak carrier velocity in InP. Turner and Wilson[21] also predict that cut-off frequency ratio of the two materials is 1.3 in favor of InP.

Our computer simulation results so far have not been adequate to confirm the above findings. The impulse responses of GaAs and InP FET of identical construction (2 μM-gate) and operated under identical conditions are shown in Figure 11. Similar results for the 4 μM gate, not shown, are also obtained. The notable feature is the more pronounced oscillation in the InP drain current; the macroscopic feature of current decay is about the same.

In actual experiments such as in Ref. (20), operating conditions can readily be varied to achieve best device performance. The electric field at which the velocity peaks is ≈10 kV/m for InP, and the peak velocity is larger as well as broader than that in GaAs. It is, therefore, feasible that the carrier traverse a large fraction of the conduction channel at near the peak velocity when the device parameters and operating conditions are appropriate. Our computer simulations have not covered sufficient range of conditions to permit any conclusion on the f_T. Rather, they only indicate that the InP FET is more prone to current oscillation.

(d) Summary

We have described the formulation of a time-domain two-dimensional computer program which is very fast in the execution. The program resolves the FET into 96x48 cells and simulates its dynamical behavior from transient to steady state. The time increment used for up-dating the internal dynamical quantities is small compared to the device time constant $[(\Delta t)_t \approx \frac{\tau}{48}]$. The fine spatial and temporal resolutions permit examination of the FET behavior in minute details.

Using this program the device physics was studied by observing its large signal impulse response. The resultant internal carrier density and potential distributions indicate persistent Gunn oscillation and significant substrate current

for short-gate devices. The latter explains the soft pinch-off characteristics of sub-micron gate devices. The computed f_T and intrinsic switch delay time agree well with available experimental data. The two-dimensional effects on the f_T was found to be significant. Finally, tailoring of the doping profile can increase device gain-bandwidth product at the expense of its power capability.

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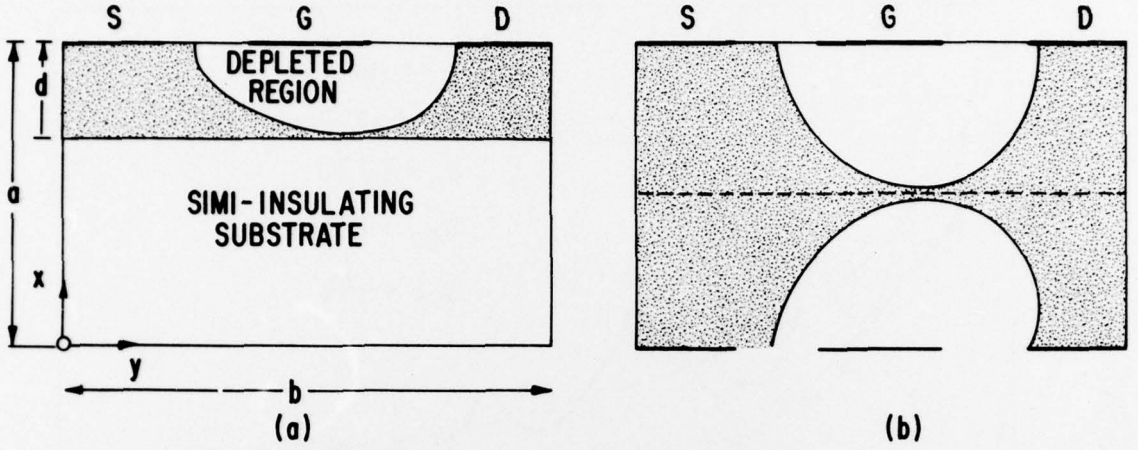


Figure 1. Physical Configuration of the Planar and the Vertical or Double-sided FET

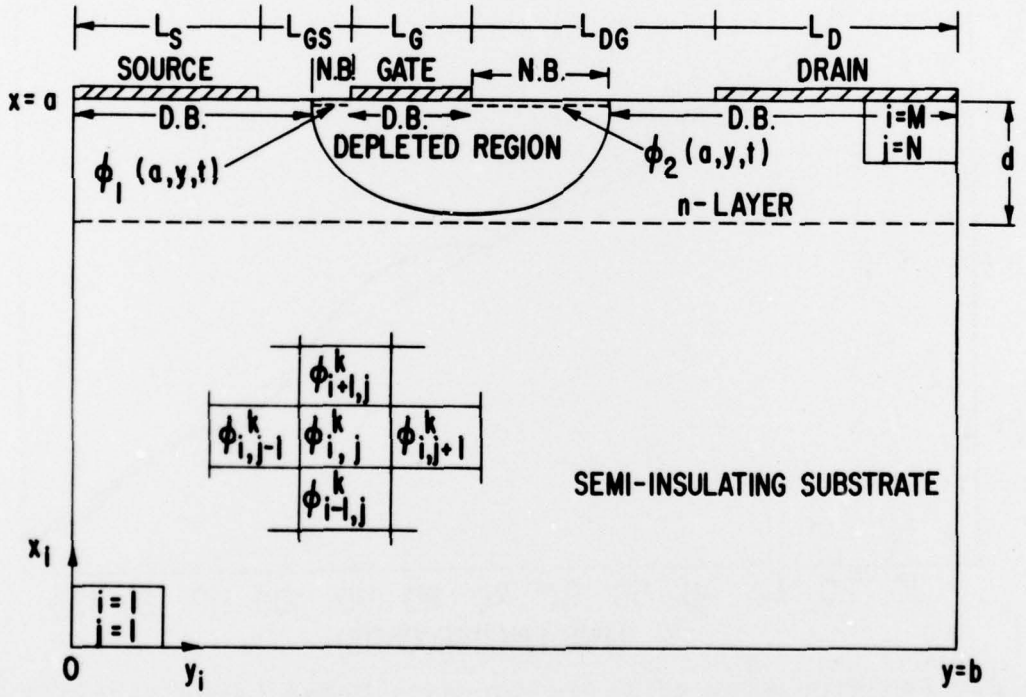


Figure 2. Computer Model for the Planar FET Showing the Coordinate System and Boundary Conditions. The space a x b is divided into 48 x 96 cells. D.B. denotes Dirichlet boundary and N.B. denotes Neumann boundary. The locations of demarcation between D.B. and N.B. are time dependent.

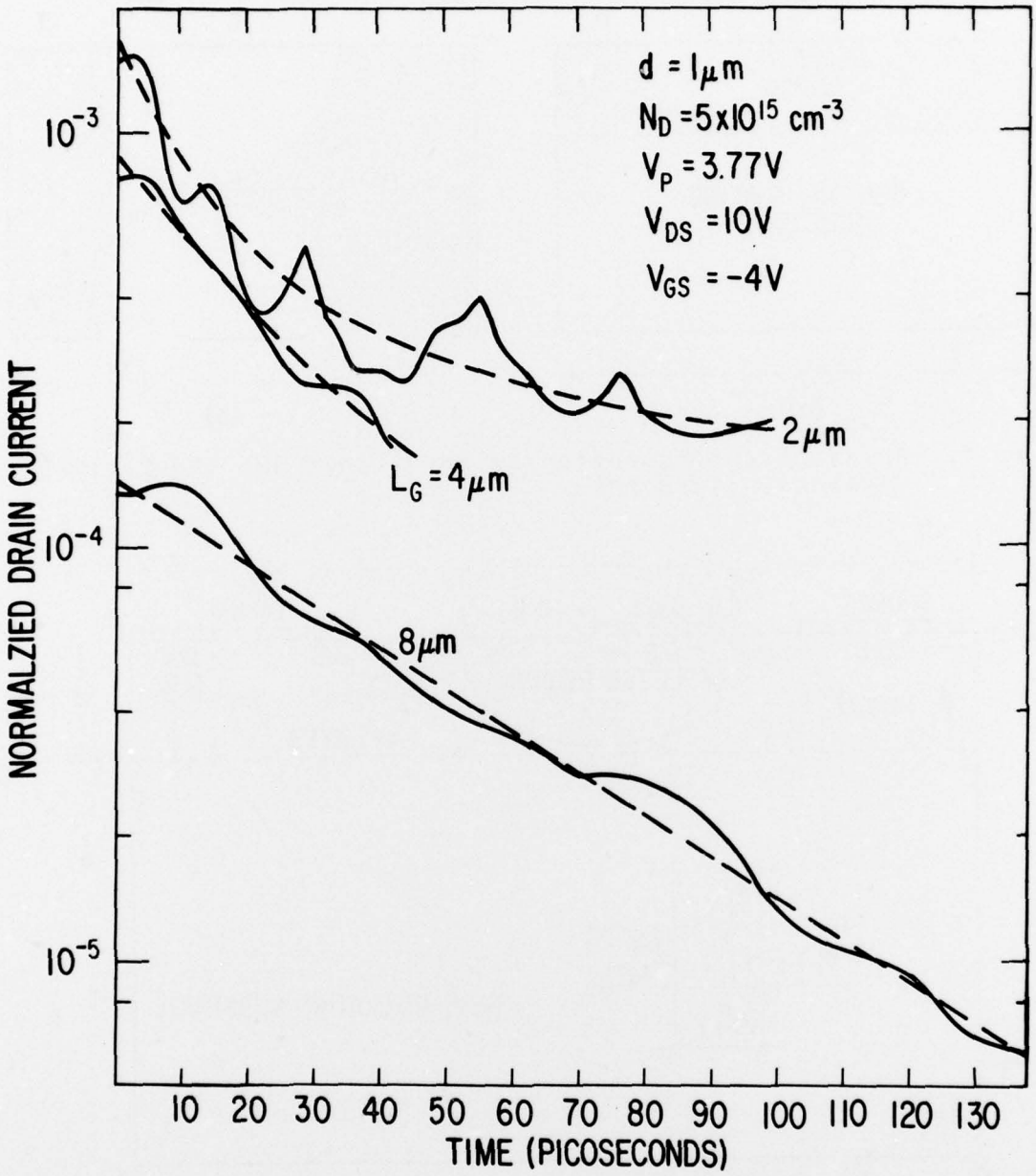


Figure 3. Semi-log Plot of Drain Currents Under Large Signal Impulse Condition. Note that the short-gate $L_G/d = 2$ device is not pinch-off and has a stronger Gunn oscillation. The initial slope of the macroscopic time dependence (represented by dashed lines) is used in the calculation of τ.

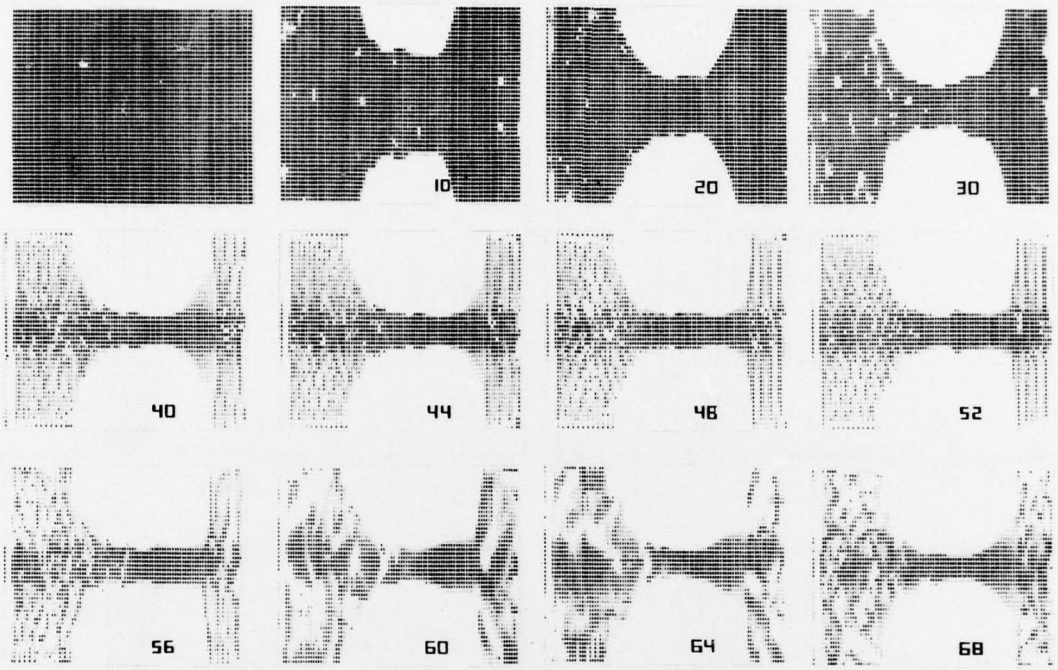


Figure 4. Time Evolution of Space Charge Distribution in a Double-sided FET with $L_G/d = 2$. The snap-shots show persistent Gunn oscillation with a complete cycle between t = 40 picoseconds and t = 68 picoseconds.

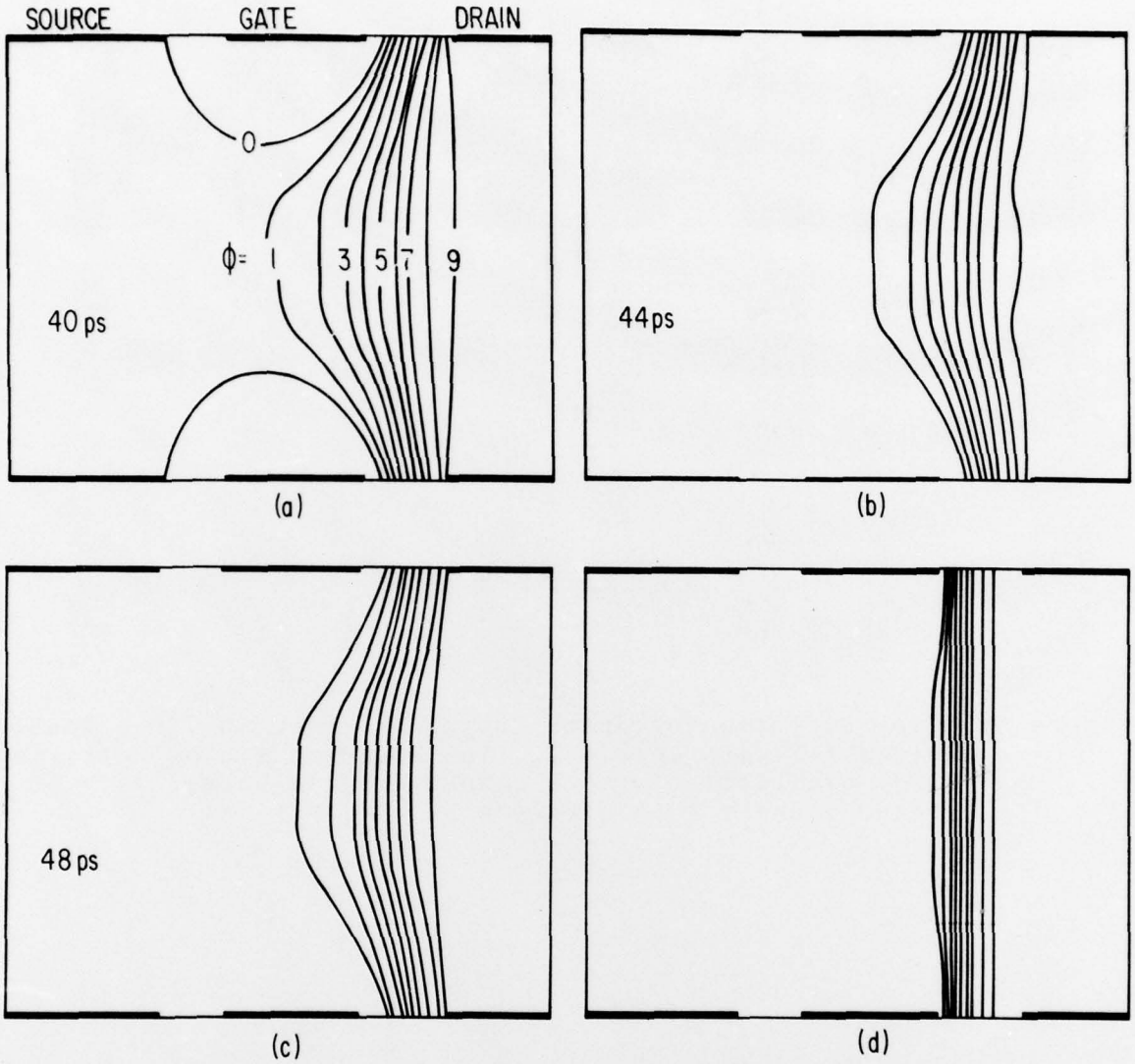


Figure 5. a, b, and c: Electrostatic Potential Distributions in the $L_G/d = 2$ Device. The degree of penetration of the drain voltage into the conducting channel is correlated to magnitude of Gunn oscillation in the drain current, as well as the time variation (indicated in ps) of the equipotential lines. Also shown (d) is the potential distribution of a long-gate device. Note the scale distortion. The full vertical side is 2μm for all frames while in the horizontal direction the gate length is 2μm in a, b, & c and is 8μm in d.

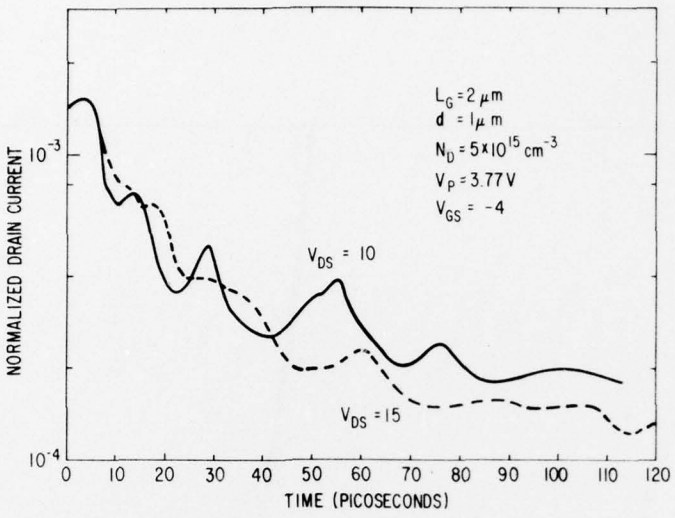


Figure 6. Impulse Response of the Drain Current Showing Effects of Drain Voltage on f_o and Gunn Oscillation

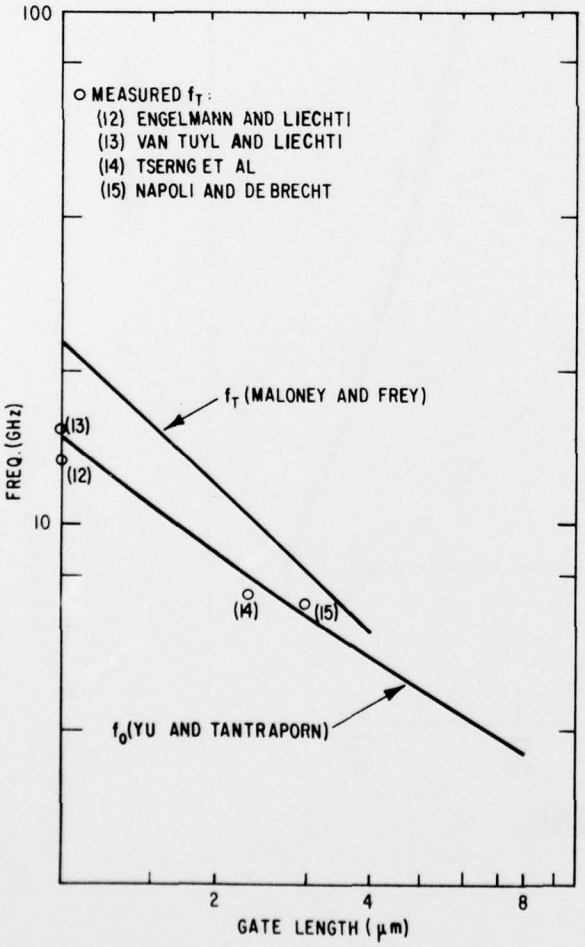


Figure 7. Computed Cut-off Frequency vs. Gate Length: Present Work and the Result of a One-dimensional Calculation of Maloney and Frey. Experimental data points are taken from the references cited.

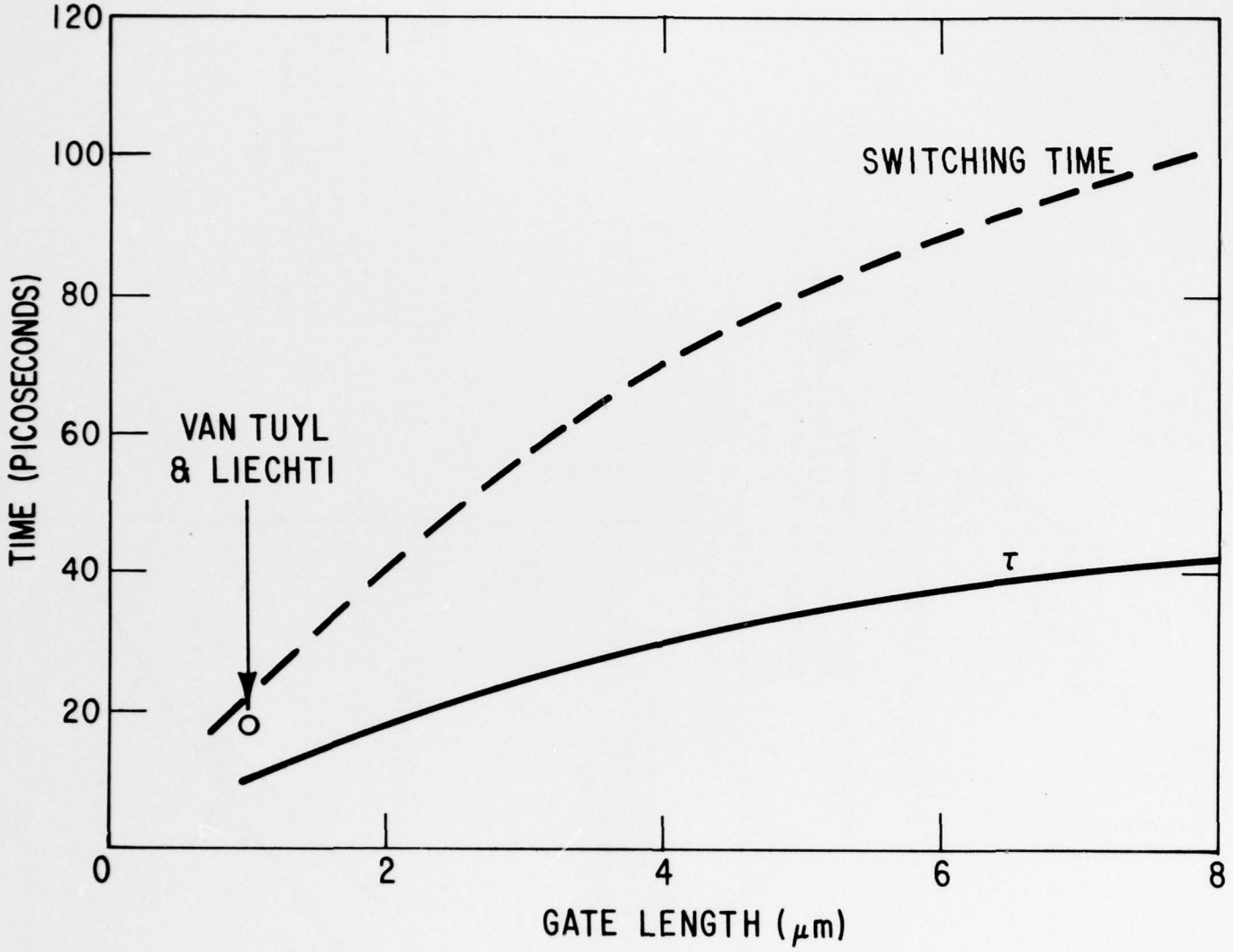
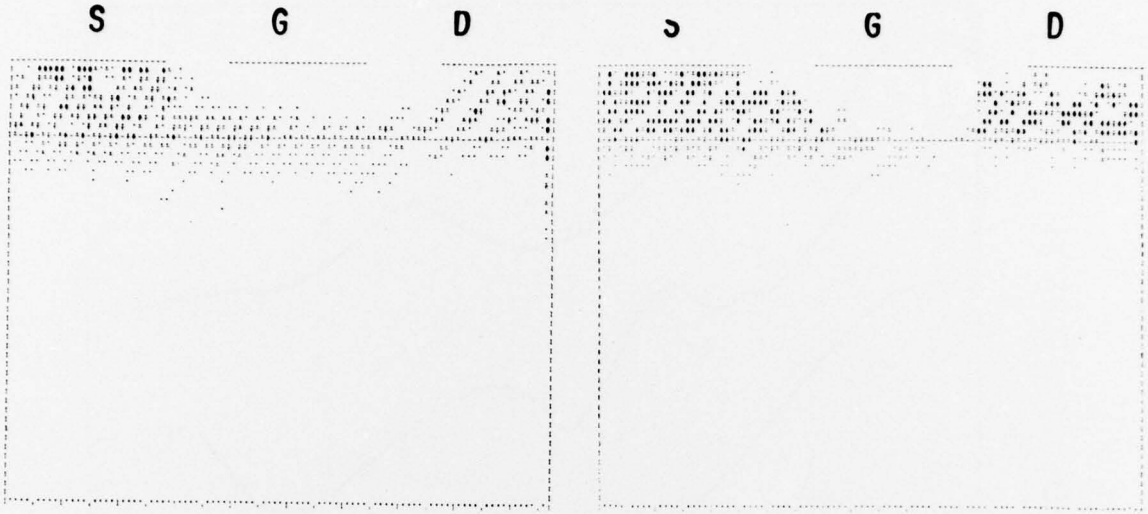


Figure 8. Device Time Constant τ and Intrinsic Switching Delay Time as Function of Gate Length. One experimental point from van Tuyl and Liechti (12) is shown.



(a) (b)

Figure 9. Steady State Distribution of Mobile Carriers in Short- and Long-Gate Devices. (a) Vertical frame = 5μm, active layer thickness d = 1μm with doping of 5 x 10^{15}cm^{-3} on 4μm insulating layer. Horizontal frame = 8μm with gate-length L_G = 2μm. (L_G/d = 2) S, G and D denote source, gate and drain electrodes. (b) Same as (a) except horizontal frame = 32μm and L_G = 8μm. Note the larger degree of carrier injection into the substrate in (a).

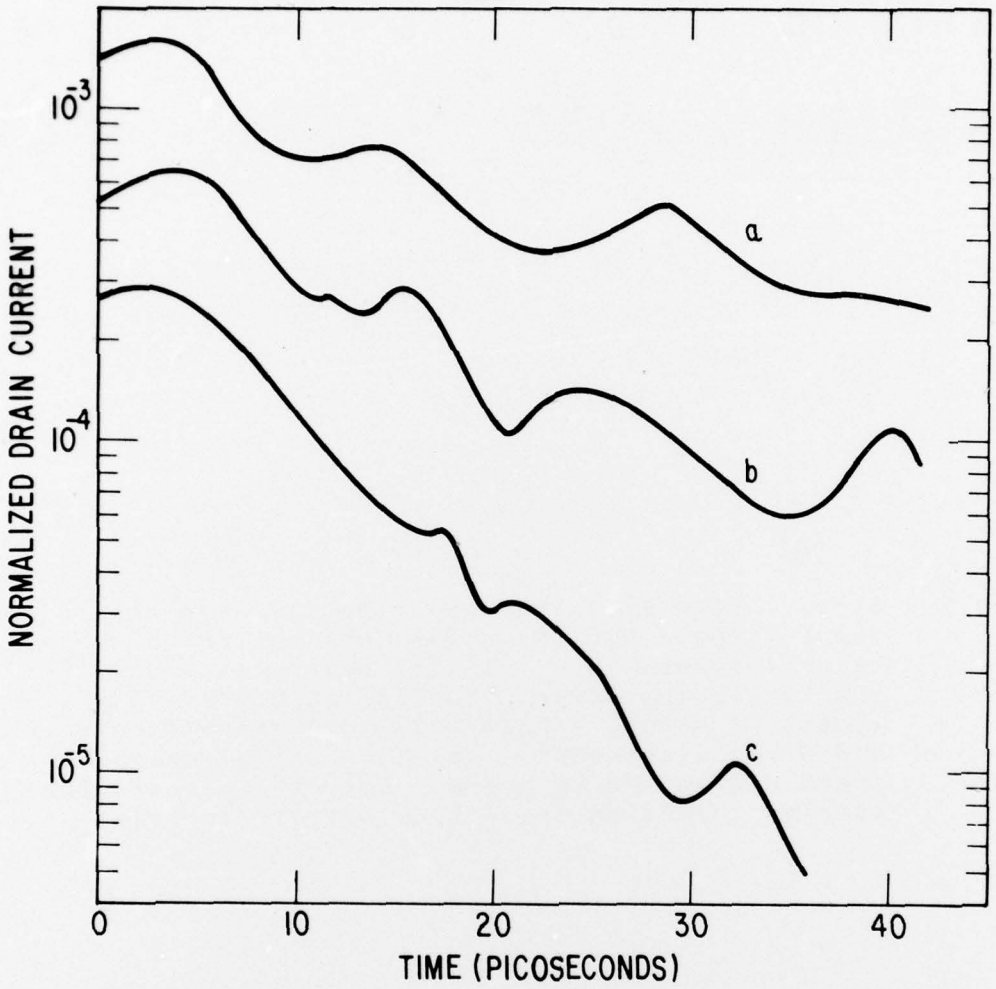


Figure 10. Impulse Response of the Drain Current for Three Identical Devices Except the Doping Profile $N_D(y)$. (a) Constant 5 x $10^{15}cm^{-3}$. (b) Exponentially decreasing from 1 x 10^{16} at the beginning to 1 x 10^{15} at the end of the gate. (c) Abrupt change from 1 x 10^{16} to 1 x 10^{15} at the middle of the gate. Other device parameters are: d = 1μm, L_G = 2μm, V_{GS} = -4 volts, V_{DS} = 10 volts.

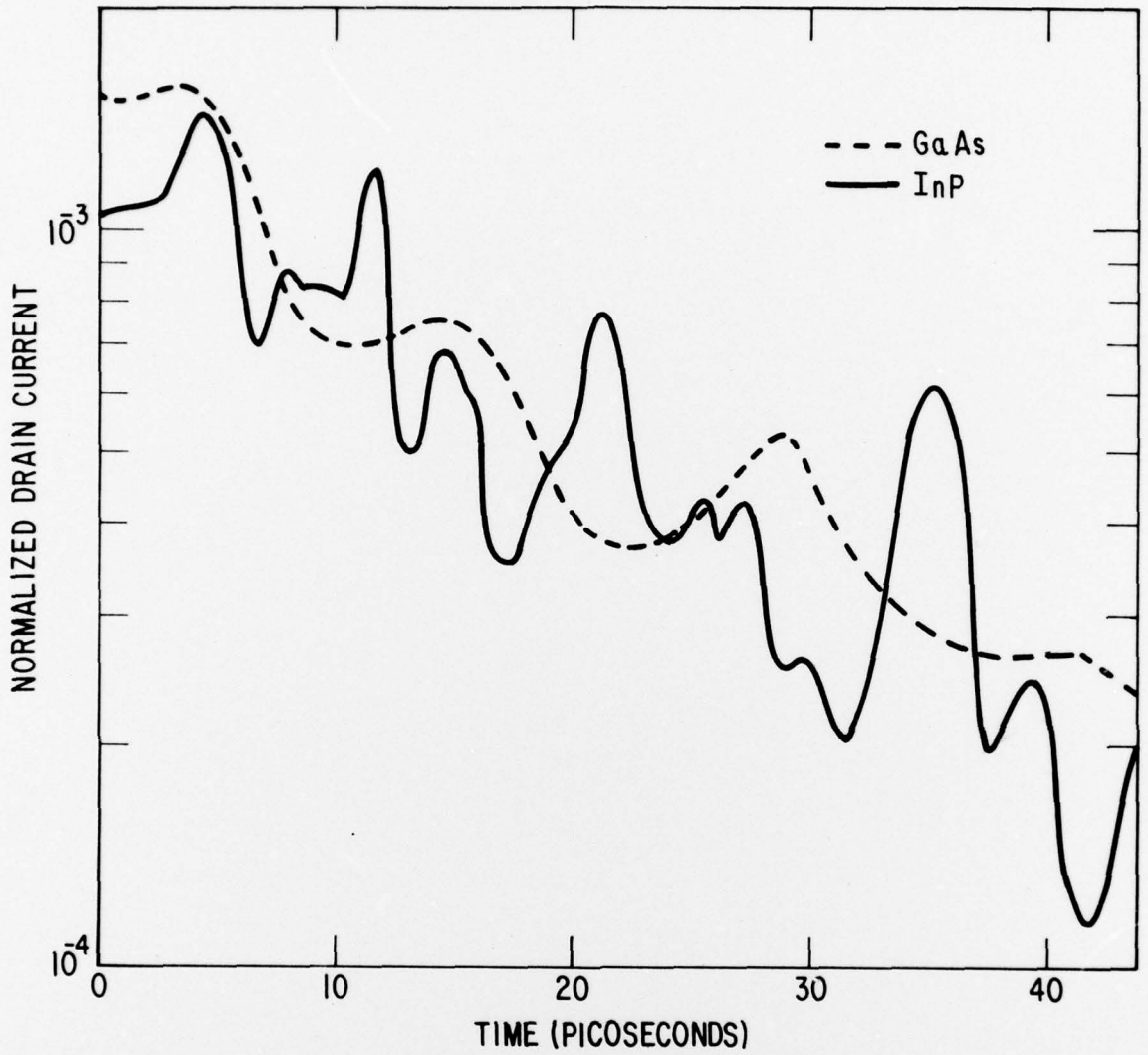


Figure 11. Impulse Response of the Drain Current for Identical Devices Except the Material Velocity-field Characteristics. Device parameters and the operation conditions are the same as in Figure 10a.

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The III-V field effect transistors were modeled using a time domain two-dimensional computer program. The device dynamics were deduced from the large signal time step impulse response. The computed cut-off frequency and intrinsic switching delay time as functions of gate length agree well with published data. The detailed internal carrier and potential distribution indicate persistent Gunn oscillation and significant current flow in the substrate for device with

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small gate length to channel width ratio $L_G/d<4$. The substrate current explains the experimental soft pinch-off of short gate ($L_G \leq 1/4\mu m$) device. Tailoring of doping profile along the gate-length direction can significantly increase the cut-off frequency.