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INTEGRATED THIN-FILM TRANSISTOR DISPLAY

FIRST QUARTERLY PROGRESS REPORT
28 SEPTEMBER TO 31 DECEMBER 1977

CONTRACT DAAB07-77-C-0583, CDRL C002, DI-S-1800

Prepared by
W. J. Helm, Project Engineer

for

US ARMY ELECTRONICS COMMAND
FORT MONMOUTH, NEW JERSEY

REPORT 5705-1

14 APRIL 1978

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BBD Bucket Brigade Device
EL Electroluminescence
TFT Thin-Film Transistor
Additive Thin-Film Deposition
Vacuum Deposition Chamber

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report summarizes the work performed during the first quarter (28 September 1977 through 31 December 1977) of a program whose purpose is to develop techniques for producing flat-panel electroluminescent displays with integrated thin-film transistor circuitry. Included are descriptions of the overall design and configuration of the display device; the design and structure of the electroluminescent elements, thin-film transistors, driver circuits, and addressing circuits of the display device; the processes and equipment being used to fabricate these devices; the process development and improvement efforts being conducted, their results to date, and plans for the next quarter's effort.

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AEROJET ELECTROSYSTEMS COMPANY

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ABSTRACT

This report summarizes the work performed during the first quarter (28 September 1977 through 31 December 1977) on a program whose purpose is to develop techniques for producing flat-panel electroluminescent displays with integrated thin-film transistor circuitry. Included are descriptions of the overall design and configuration of the display device; the design and structure of the electroluminescent elements, thin-film transistors, driver circuits, and addressing circuits of the display device; the processes and equipment being used to fabricate these devices; the process development and improvement efforts being conducted, their results to date, and plans for the next quarter's effort.

The report is submitted in accordance with approval letter DELSD-D-PC, dated 24 March 1978, from Headquarters, U.S. Army Electronics Research and Development Command, Adelphi, Maryland.

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PURPOSE

The purpose of the Integrated Thin-Film Transistor Display Program is to develop and demonstrate techniques for producing flat-panel electroluminescent (EL) displays consisting of integrated thin-film transistor (TFT) addressing and driving circuitry.

Major phases of this 25-month program indicated in Figure 1 (Program Schedule by Contract Line Item) consist of a 12-month Engineering sample phase, a 5-month confirmatory sample phase, and a 5-month pilot run phase.

During the current engineering sample phase, two of the key tasks are the development of manufacturing methods for producing both EL panels and the associated TFT circuits. The specific objective of both tasks is establishing reproducible, high yield processes.

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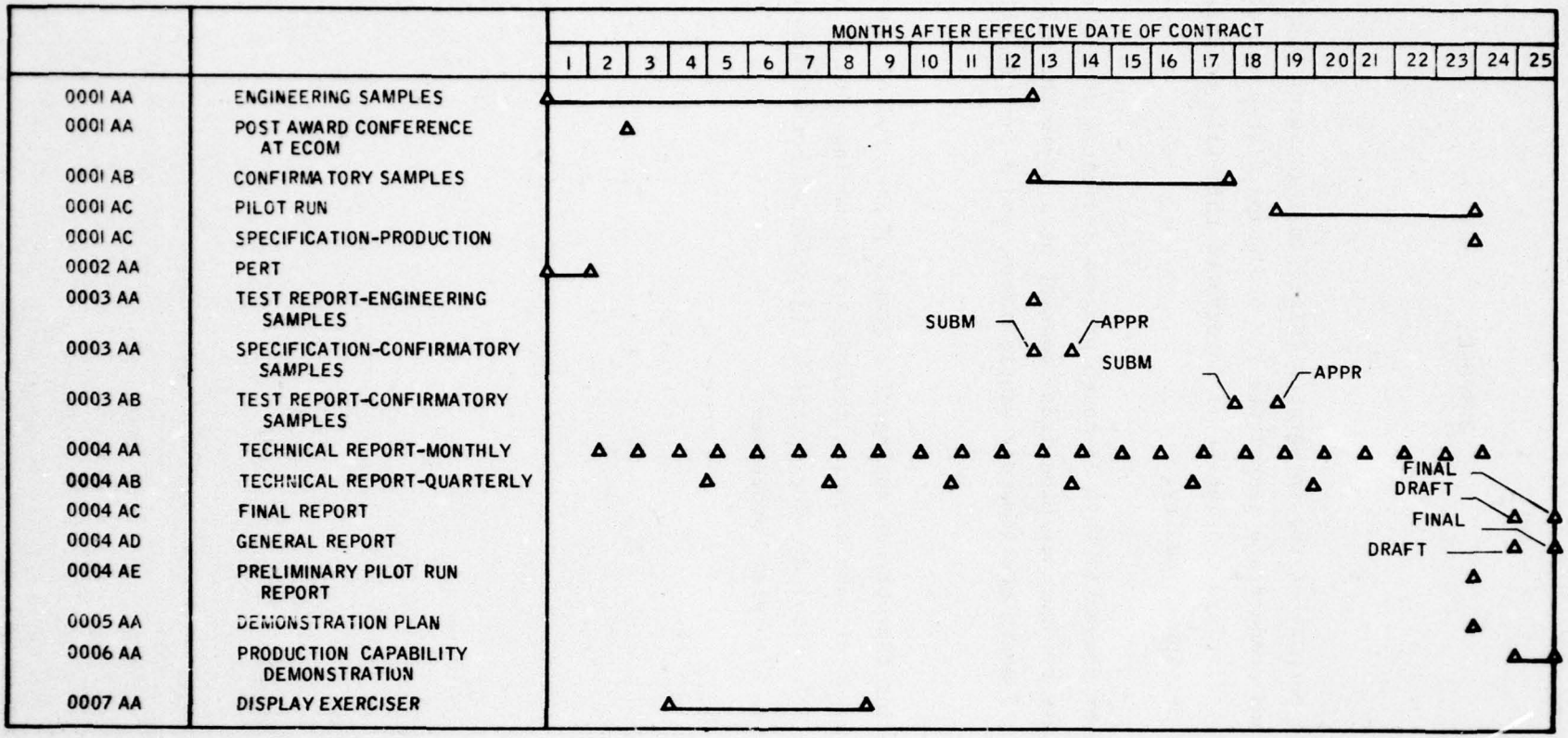

FIGURE 1 PROGRAM SCHEDULE BY CONTRACT LINE ITEM

GLOSSARY

BBD — Bucket Brigade Device - One form of charge transfer device which may be implemented with discrete transistors (e.g., TFTs) and capacitors. Under control of a two-phase clock, sampled signal data is propagated along the structure to provide a delay function.

EL — Electroluminescence - The emission of light resulting from the application of an electric field to a solid and not due to temperature alone. As used here, the term applies to a thin-film sandwich structure composed of layers of dielectric, e.g., Y_2O_3, and of doped active material, e.g., ZnS:Mn, excited by an applied a-c voltage.

TFT — Thin-Film Transistor - A field-effect transistor in thin-film form, fabricated by vacuum deposition of evaporated materials through a series of stencil masks onto an insulating substrate.

Section 1

NARRATIVE AND DATA

1.1 DEVICE DESCRIPTION

1.1.1 General

The integrated thin-film transistor display of interest on this program consists of an array of individually addressable and controllable electroluminescent elements. The major physical and performance specifications for the display are listed in Table 1.

1.1.2 Active Matrix Concept

The display design is based on the active matrix concept--that is, the matrix of light-emitting elements incorporates, at each site, an active circuit to store ON or OFF data and to provide the requisite switching state for controlling the EL element. A thin-film transistor (TFT) provides the switching function, with the ON or OFF gate control voltage stored on a capacitor. Charge leakage makes it necessary to update or refresh the control voltage periodically. Row and column AND gates, controlled by corresponding scan generators, are used to enable a data line to set the appropriate charge level on the selected capacitor. Parallel data lines addressing 7 of the 222 columns simultaneously are presently contemplated as a means of reducing the data rates for compatibility with thin-film transistor capabilities.

The selection of seven data lines conveniently accommodates the intended ASCII character format of five active and two inactive (but still addressable) columns per character. The column and row scan generators, to be implemented with TFT bucket brigade device (BBD) delay lines or shift registers, will consequently consist of 32 and 77 delay stages respectively. At the required rate of 30 frames/sec, the data rate is 32 x 77 x 30 = 73,920 bits/second on each of the seven data lines.

TABLE 1 MAJOR PHYSICAL AND PERFORMANCE SPECIFICATIONS OF INTEGRATED TF TRANSISTOR DISPLAY

Display Panel Maximum Dimensions	4.0 inches x 8.0 inches
Display Area	2.90 $\pm$ 0.05 inches x 6.60 $\pm$ 0.06 inches
Number of EL Elements	77 rows of 222 elements
EL Element Shape and Size	Rectangular, 0.015 x 0.021 inch minimum
Number of Alphanumeric Characters	256 (8 rows of 32 characters)
Character Format	5 x 7 element dot matrix configuration
Display Weight	7 oz. maximum
Power Dissipation	2.0 watts maximum all elements on; 1.0 watt maximum all elements off
Viewability	Characters viewable and recognizable with 2000 footcandle ambient light intensity on the display
Contrast	Ratio of on-element luminescence to luminescence of off-element or neighboring dark space (whichever is greater) to be 20 or more
Operating Life	600 hours minimum through ON-OFF cycles, including 500 hours of ON operation

1.1.3 Thin-Film EL Structure

The basic light-emitting element of the display matrix is a rectangular shaped capacitor fabricated by vacuum deposition techniques. The lateral dimensions of such an element are bounded by the specified minimum size of 0.015 by 0.021 inches and the approximate 0.030- by 0.038-inch center-to-center spacing defined by the specified display size and format.

Figure 2 is a sketch of an EL element structure which describes the typical materials, film thicknesses and structure of an EL element. When an a-c voltage is applied to these elements, a yellowish-orange light is produced and can be viewed through the substrate and transparent electrode. The luminescence or brightness of an element is a function of the excitation voltage, a function of frequency for a continuous sine wave drive, or of pulse shape and duty cycle for pulsed operation.

1.1.4 Thin-Film Transistor (TFT)

The thin-film transistor is an insulated gate, field effect device, fabricated by vacuum deposition techniques. In its simplest form the TFT consists of a thin layer of semiconductor with source and drain electrodes at either end; an insulating layer covering the semiconductor and partly covering the source and drain electrodes; and a gate electrode on the insulator centered over the source drain gap and extending slightly beyond the gap.

More commonly, TFTs are fabricated as double-gate devices, having an insulated gate both above and below the semiconductor. This construction provides double the transconductance for a given geometry since both gate fields are effective in modulating the semiconductor. In addition, the characteristics of the drain current in the saturated region are improved and flatter than those of single-gate transistors. The double gate structure is illustrated in Figure 3 which also notes representative materials and film thicknesses.

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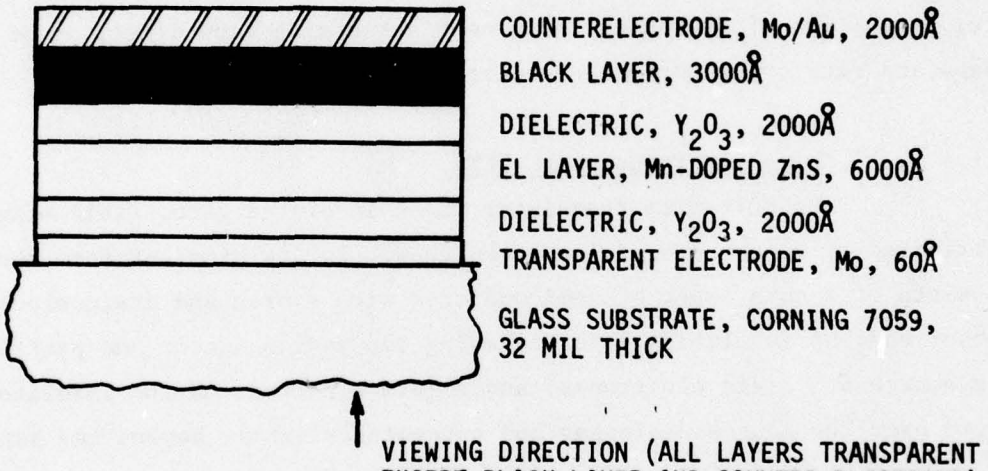

FIGURE 2 SKETCH OF ELECTROLUMINESCENT (EL) ELEMENT STRUCTURE - SHOWING TYPICAL MATERIALS AND FILM THICKNESSES

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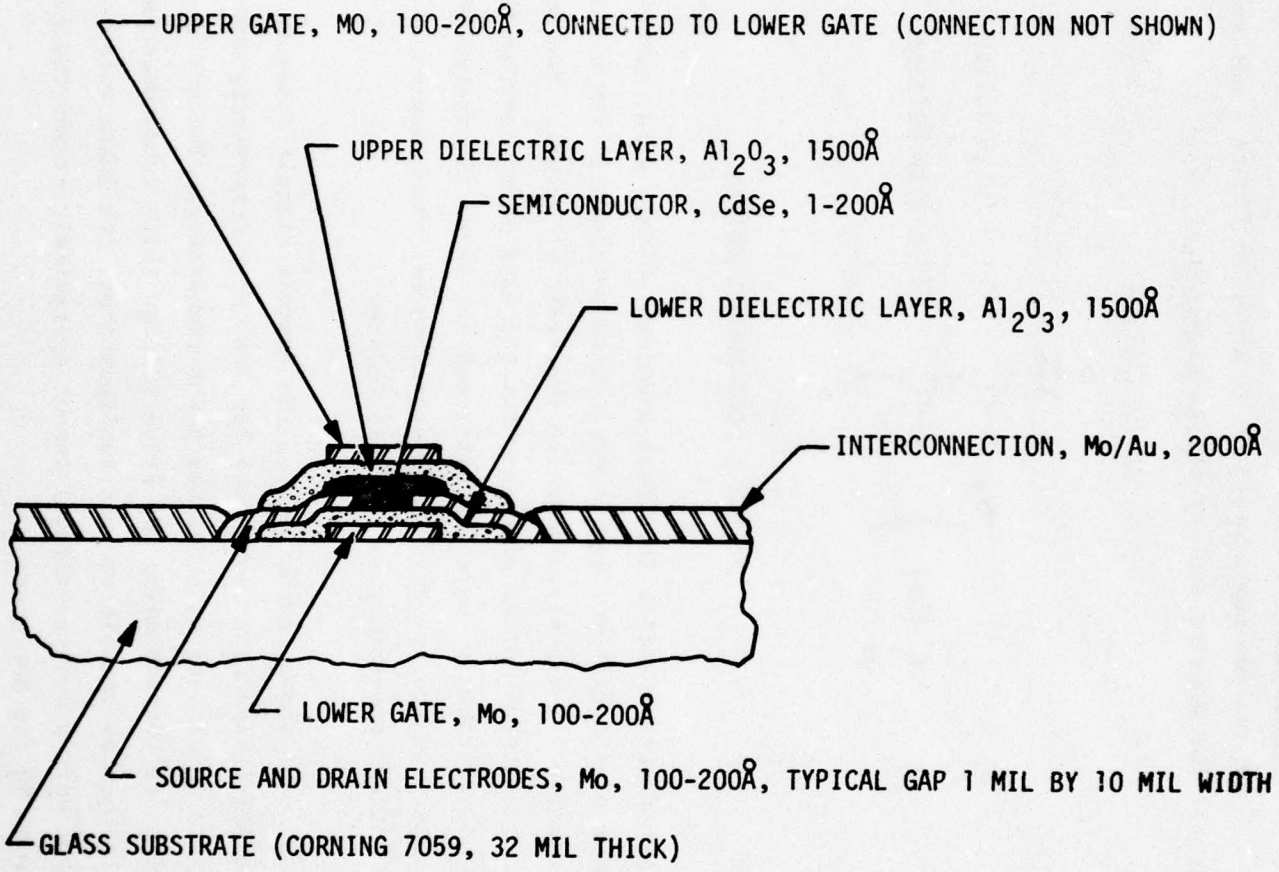

FIGURE 3 SKETCH OF THIN-FILM TRANSISTOR - SHOWING DOUBLE GATE STRUCTURE, TYPICAL MATERIALS AND FILM THICKNESSES

1.1.5 Driver Circuit

A cascode configuration, as shown in Figure 4 was selected as the circuit for driving each of the EL elements.

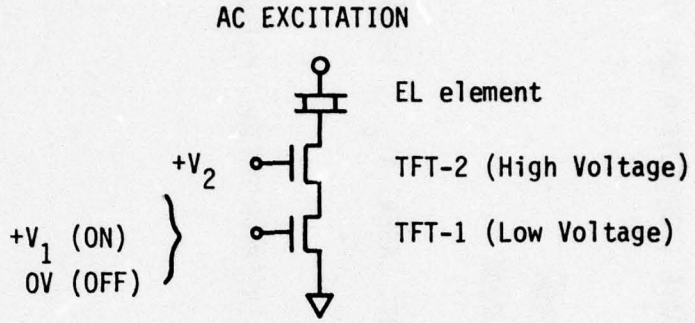

FIGURE 4 CASCODE EL DRIVER

The circuit configuration in effect provides voltage gain, permitting the switching of the high voltage EL excitation waveform (a few hundred volts p-p) by a relatively low gate-voltage (on the order of 5-10V). Two benefits are realized: external drive circuitry for the data lines can readily be implemented using standard logic circuits; and the power dissipated in charging and discharging the row and column capacitances, which scales as the square of the voltage excursion, is markedly reduced.

As shown in the figure, the cascode circuit consists of a high voltage TFT (thick gate insulator) for the upper transistor, and low voltage (thin gate insulator) unit for the lower transistor. The use of a low-voltage TFT, with its corresponding low drive voltage (high transconductance), is possible because in this circuit configuration, its drain voltage (equal to the upper unit's source voltage) cannot appreciably exceed the gate voltage V_2 (~40 V) in the OFF state.

Current requirements are less than 1 mA peak for EL elements of approximately 0.25 mm^2 area to be utilized in the display. TFTs whose source-drain gap dimensions are 0.001 x 0.010 in. can supply that order of current;

low voltage units at gate voltages below 10V, and high voltage units with approximately 40V on the gate.

The cascode circuit configuration can be fabricated using a pair of separate TFTs or as a so-called virtual cascode illustrated in Figure 5.

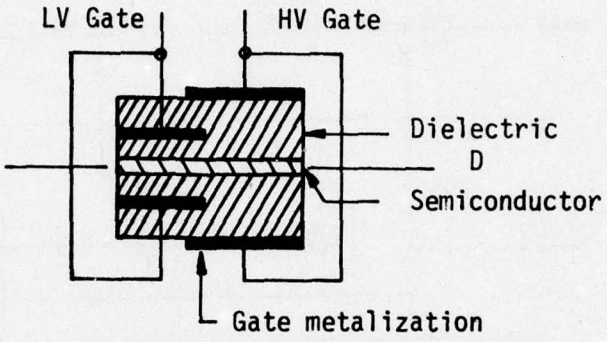

FIGURE 5 VIRTUAL CASCODE CONFIGURATION

The virtual cascode configuration uses a combination of a low voltage (thin gate dielectric) and a high voltage (thick gate dielectric) TFT. It makes possible an appreciable size reduction by eliminating unneeded connections, and provides for physical separation of the high and low voltage gates even for the overlap case indicated in Figure 5.

1.1.6 Addressing Circuit Concept

The addressing concept developed on the program to date for the integrated thin-film transistor display is illustrated in Figure 6 - the addressing circuit for a 2-row by 4-column display. A timing diagram showing the proper sequence of various controlling waveforms is given in Figure 7, and the sequence of events during a complete frame time is listed in Table 2.

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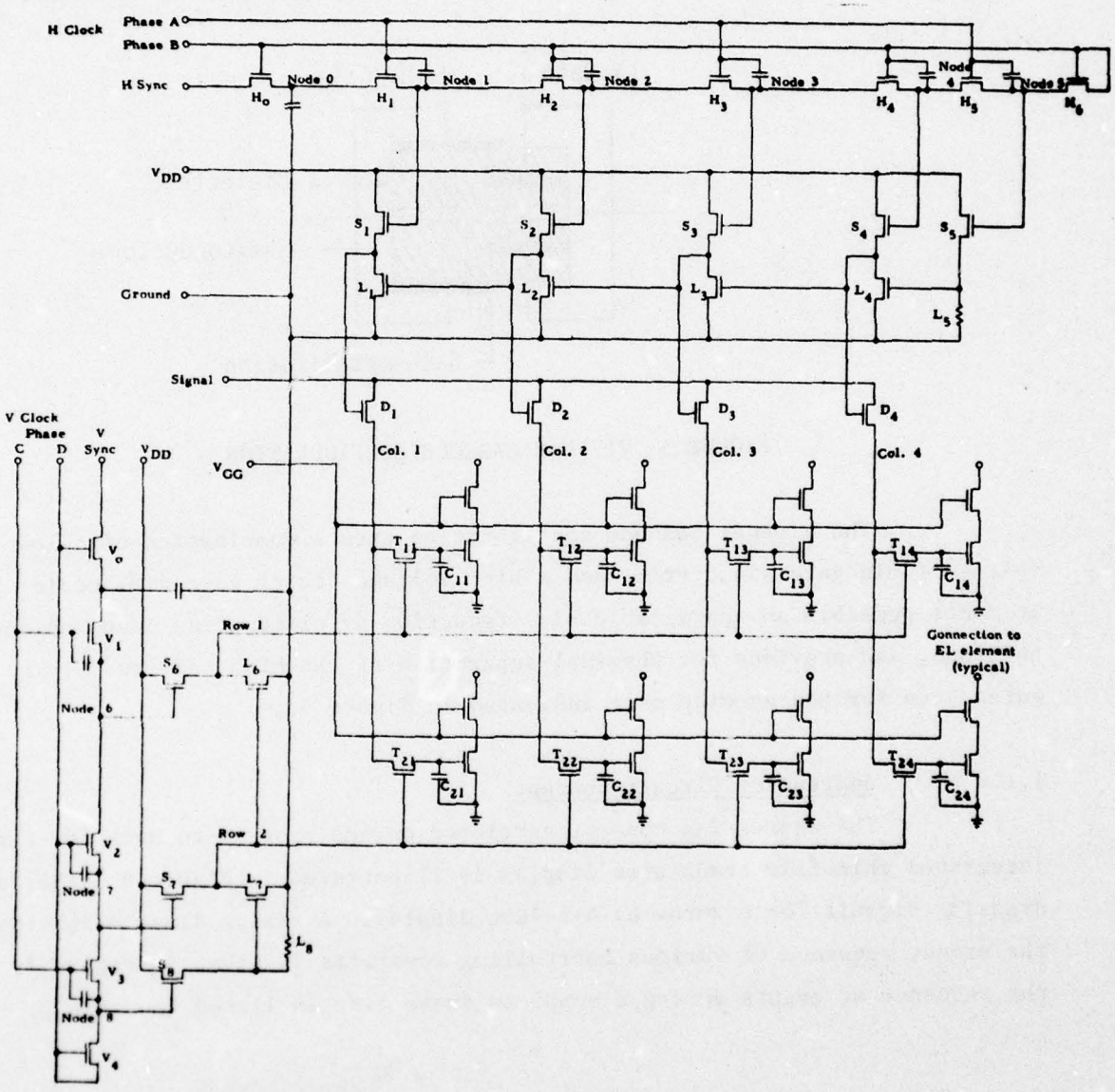

FIGURE 6 SIMPLIFIED DISPLAY ELECTRONICS CIRCUIT DIAGRAM

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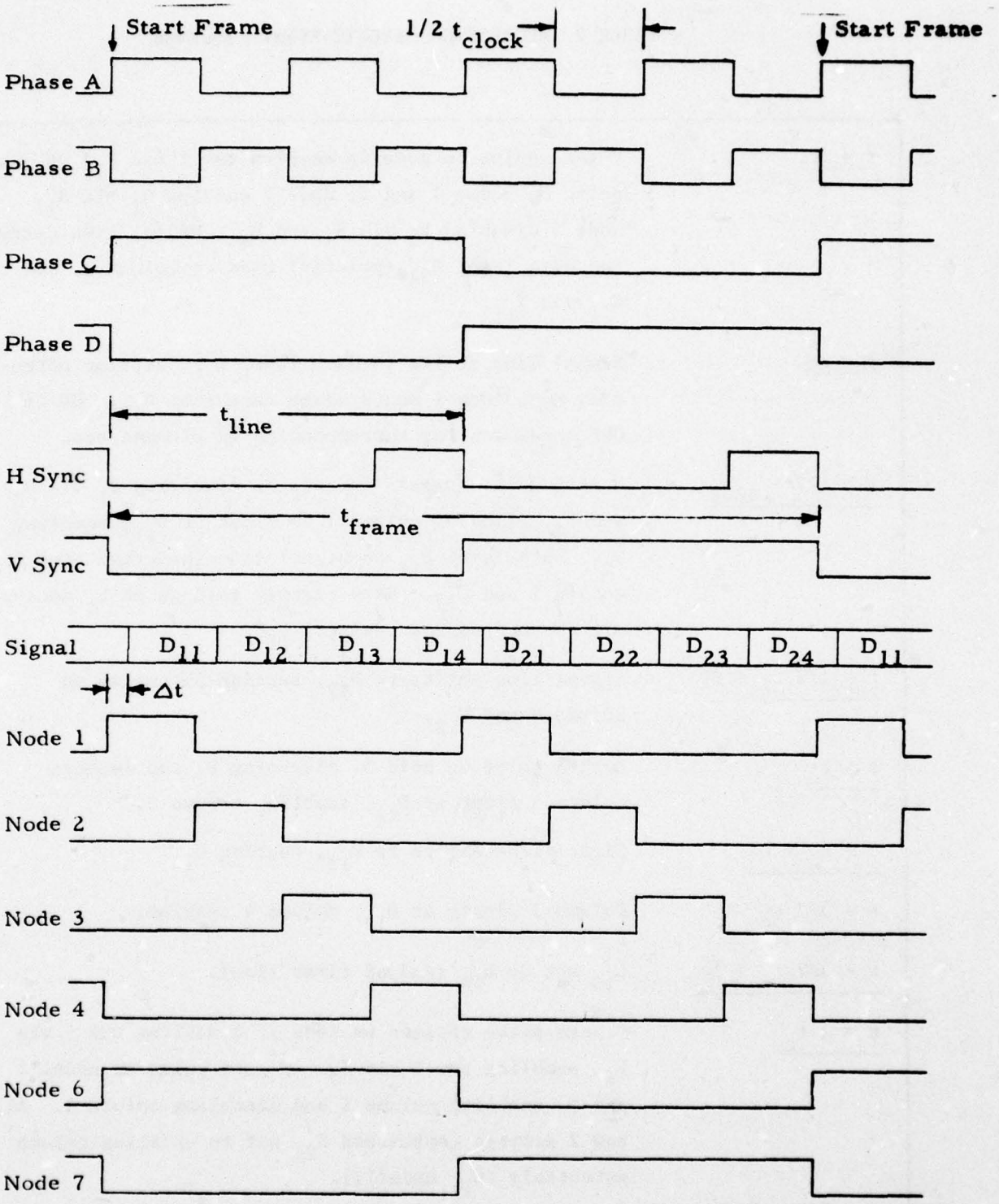

FIGURE 7 TIMING DIAGRAM

TABLE 2 ADDRESSING CIRCUIT EVENT SEQUENCE

$t = 0$	V gate pulse on node 6; enables row 1 via S_1. H gate pulse on nodes 1 and 5; node 1 enables D_1 via S_1, node 5 disables D_4 via S_5 and L_4. Signal line carrying data level D_{24} (briefly) tied to column 1, and to C_{11} via T_{11}.
$t = \Delta t$	Signal line shifts to data level D_{11}, setting potential on column 1 and storage capacitor C_{11}. ON or OFF condition for corresponding EL element set.
$t = 1/2\ t_{clock}$	H gate pulse appears on node 2, disabling D_1 via S_2 and L_1, allowing column 1 to float at D_{11}; enabling D_2. Data level D_{11} on signal line (briefly) tied to column 2 and C_{12}. Gate circuit voltage on L_4 decays off through source resistor L_5.
$t = 1/2\ t_c + \Delta t$	Signal line shifts to D_{12}, setting potential on column 2 and C_{12}.
$t = t_c$	H gate pulse on node 3, disabling D_2 and letting column 2 float at D_{12}, enabling column 3.
$t = t_c + \Delta t$	Signal line shifts to D_{13}, setting C_{13}.
$t = 3/2\ t_c$	Column 3 floats at D_{13}, column 4 enabled.
$t = 3/2\ t_c + \Delta t$	C_{14} set to D_{14} (end of first line).
$t = 2\ t_c$	V gate pulse appears on node 7, disabling row 1 via L_6, enabling row 2 via S_7. H gate pulse on nodes 1 and 5, enabling column 1 and disabling column 4. All row 2 storage capacitors C_{2j} set to existing column potentials (C_{21} briefly).
$t = 2t_c + \Delta t$	C_{21} set to D_{21}.

TABLE 2 ADDRESSING CIRCUIT EVENT SEQUENCE (CONT.)

$T = 5/2\ t_c$	D_1 disabled, D_2 enabled.
$t = 5/2\ t_c + \Delta t$	C_{22} set to D_{22}.
$t = 3\ t_c$	D_2 disabled, D_3 enabled.
$t = 3\ t_c + \Delta t$	C_{33} set to D_{23}.
$t = 7/2\ t_c$	D_3 disabled, D_4 enabled.
$t = 7/2\ t_c + \Delta t$	C_{24} set to D_{24} (end of line 2 and of frame)
$t = 4\ t_c$	V gate pulse on nodes 6 and 8, enabling row 1 and disabling row 2.
	Continue through frame sequence.

It is the function of this circuit (Figure 6) to distribute digital (i.e., ON and OFF) data from the signal line to the storage capacitors C_{ij} at each display element site. The ON or OFF voltage level so stored on each capacitor controls the state of the cascode switch in series with the corresponding EL element.

Distribution of the data is controlled by means of gating pulses used to enable rows and columns one at a time through the use of bucket brigade device (BBD) shift registers. TFTs V_i together with their associated capacitors constitute the vertical shift register. A synchronizing pulse introduced to its input once each frame time is used to enable the row lines in sequence as the pulse is shifted along the register at the line rate in synchronism with the vertical clock pulses. (Source followers S_i, along with their active source loads L_i are used to minimize loading of the BBD nodes).

In a similar fashion, the horizontal sync pulse, introduced into the horizontal shift register (TFTs H_j and associated capacitors) once each line time, is shifted along that register at the element rate. The pulse is coupled via a source follower to each column data gate, D_j, in sequence, allowing data appearing on the signal line to be impressed on the columns, one after the other. The column voltages charge up corresponding storage capacitors in the enabled row via TFTs T_{ij}, establishing the ON or OFF states for the cascode switch circuits.

It can be seen that as each data gate D_j turns off (aided by the active load L_j) its associated column floats at the potential established during the on time of the gate. (This feature must be provided, since the column line is still connected via T_{ij} to the storage capacitor in that column and in the selected row). The timing of data as shown for the signal line in Figure 2 is delayed with respect to the clock transitions to ensure that the column just addressed is completely disconnected from the signal line before the next data transition occurs.

At the end of a line time, all columns are floating at the potentials established during that line time. Thus when the next row is enabled, all of the storage capacitors are set to the potentials of corresponding elements in the row above. Elements at the ends of the lines could thus be in the wrong state for a full line time (other elements for a shorter time in proportion to their positions). In our two-row example, this would be totally unacceptable, but for the 77-line display to be implemented on this program, the contrast ratio for the elements most affected would still be 77. It has tentatively been concluded that this slight contrast degradation is more acceptable than the added circuit complexity and power dissipation required to eliminate it.

1.2 FABRICATION PROCESSES AND EQUIPMENT

1.2.1 Additive Thin-Film Deposition

All of the electronic and light emitting elements of the integrated thin-film transistor display are fabricated using additive, thin-film deposition processes. These processes involve the evaporation of metallic, dielectric, and semiconductor materials in a vacuum by electron beam gun or resistance heating; and the deposition of each evaporated material though a stencil mask onto a substrate, typically glass or ceramic. Each material and mask combination results in a deposition pattern on the substrate. Sequences of depositions of different materials through each of a set of masks are used to produce devices, circuits or complete subsystems such as the integrated thin-film transistor display.

1.2.2 AESC Vacuum Deposition Chambers

The equipment being used to fabricate the integrated thin-film transistor display consists of three vacuum deposition chambers currently installed and available in the AESC Vacuum Deposition Laboratory. These chambers have been designed and developed by AESC over the past ten years. Key features of their design, installation, and operation are as follows:

a. The vacuum disposition systems are installed in a clean room (class 10,000). Access to this room is controlled and clean room garments are required for all personnel. All pneumatic, hydraulic, and high voltage lines are installed beneath a second floor surface for both cleanliness and personnel safety.

b. All chambers are of a top loading design--the bell jars and cylinders are provided with gasket seals at the system base. The deposition mechanism forms the top of the cylinder and is similarly gasket sealed. This design permits direct mechanical linkage between the deposition mechanism and the control knobs on the top of the chamber. It also permits quick turnaround between operations--the entire mechanism is lifted from the top of the chamber for installation or removal of masks and substrates.

c. The deposition mechanisms are designed to hold six masks and six substrates. Six configurations of as many as 11 deposition materials (i.e., as many as 66 depositions) can be made on six substrates during a single pumpdown of a single chamber. The deposition mechanism uses ball and socket connections which register each mask to each substrate to an accuracy of 0.1 mil (0.0001 inch).

d. The chambers are typically evacuated to 10^{-7} to 10^{-8} torr for thin-film electronic depositions. Four stages of pumping are used for rapid evacuation. A Stokes mechanical pump (375 CFM) assisted by a Roots blower (500 to 800 CFM) is used to bring chamber pressure down to 100 microns. Sorption pumps (Zoelite pellets chilled to liquid nitrogen temperature) further reduce pressures to about 5×10^{-4} torr. A helium cold finger or liquid nitrogen cold trap is used to reduce pressures to 10^{-5} torr; and a titanium getter-type ion pump, together with quartz-iodine lamp bakeout, bring the system down to 3×10^{-8} torr.

e. Electron beam guns are used to vaporize deposition materials, both by direct beam impingement on the material and indirectly by beam heating of the material boat or container. Direct electron beam vaporization avoids possible contamination by boat materials and permits deposition of very high melting point materials. (Sapphire, Al_2O_3, for example, is frequently used as a dielectric and sealant.) A system of rotatable trays and shields permits a selection of up to 11 different materials in any sequence during a single chamber pumpdown. Techniques and schedules have been developed and standardized for the deposition of a wide variety of conductor, semiconductor and dielectric materials.

f. Very accurate automatic control of the deposition process is provided by a system which uses a quartz crystal vibration at 5 megahertz inside the chamber. Deposition of material on the crystal increases its mass and reduces its frequency. The control system converts frequency to thickness or deposition rate of a given meterial, or both, and adjusts the power to the electron beam gun accordingly, shutting off the gun when a desired thickness

is achieved. The desired thickness and deposition rate are entered into the control system prior to the deposition and deposition thicknesses are commonly controlled to one Angstrom (10^{-8} cm).

In addition, the electrical characteristics of devices being formed can be measured and observed during the deposition process. Electrical leads contact the edge of the substrate where a sample or monitoring transistor is deposited, and are connected to an external oscilloscope where the changes in electrical characteristics during the deposition process can be directly observed.

1.2.3 EL Deposition

The EL structure is fabricated in three sequences. For each of these, the vacuum chamber is prepared by cleaning deposition shields, cleaning and loading glass substrates and masks (if required), loading source materials, pumping down the chamber, and outgassing sources and substrates. During the first step, both sides of the substrate are coated with a 60 Å layer of molybdenum (together with copper edge electrodes for electrical contact). One layer will serve as the transparent electrode, while the other will be used for substrate heating during the next sequence in which the actual EL layer is fabricated. Several substrates may be coated simultaneously.

For the second step, electrical contacts are made to the heater layer, and access to the transparent electrode contacts is preserved by masking them from subsequent depositions, when the substrates are mounted in the chamber. The first deposition, carried out in an O_2 background pressure of 5×10^{-5} torr with a substrate temperature of 300°C, results in the first dielectric layer of 2000 Å of Y_2O_3. The heater is turned off and the substrate is allowed to cool, prior to deposition of the Mn-doped ZnS layer. Thickness and Mn doping concentration may be varied to achieve different brightness-voltage characteristics; typical values are 6000 Å and 3 percent by weight, respectively. After the ZnS:Mn deposition cools, the second 2000 Å Y_2O_3 dielectric layer is deposited in an O_2 background. Finally, a 3000 Å thick black layer is applied. The desired counter electrode pattern, which defines

the geometry of the display, is deposited through a metal stencil mask as a separate step.

1.2.4 Electronic Deposition

For fabrication of thin-film transistors, chamber preparations similar to those described above for EL fabrication are carried out. The first deposition is that of an Al_2O_3 dielectric layer, carried out in a high (2×10^{-4} torr) O_2 background. (This step is found useful in obtaining better device uniformity over the substrate.) The transistor structure shown in Figure 3 is then built up by successive depositions, through corresponding metal masks, of Mo lower gate electrode; lower Al_2O_3 gate insulator (again in an O_2 background); Mo source and drain electrodes; CdSe semiconductor; upper gate insulator; upper gate electrode (using the same mask as for the lower one); Mo/Au interconnecting electrodes; and finally a protective Al_2O_3 overcoat.

During the CdSe deposition, the characteristics of a test device are monitored, permitting the development of transistor action to be observed. If the as-deposited semiconductor is found to be improperly conductive, either too high or too low, as a result either of source material properties or of deposition conditions, the stoichiometry is adjusted by the carefully controlled addition of Cd or Se, as appropriate, until the desired TFT characteristics are observed.

As the upper gate insulator is deposited, the TFT characteristics can be seen to change dramatically, approaching an open circuit. A post-deposition heat treatment is required to regain the desired TFT character. Again a test device is used, with resistance between drain and gate-source being the quantity monitored.

1.2.5 Process Improvement Efforts and Results

Thin film display work at Aerojet ElectroSystems during the two years prior to this program has demonstrated that high quality electro-luminescent films and electronic devices can be made by additive, vacuum

deposited, thin film processes. However, little information has been obtained on the reproducibility and yield of these processes as used in various display component experiments and demonstrations.

The development of high yield, reproducible processes is obviously critical to the success of this program and to any future application of thin film technology to military or industrial needs. The investigation of process variables--determining the material, process, and procedural factors which cause nonuniformity and non-reproducibility--is an essential first step towards high yield processes which will permit routine fabrication of displays in a manufacturing environment, and has been the principal activity during this first quarter of the program. Fabrication procedures outlined in the preceding sections are the results of the evolution which took place during these investigations; this evaluation is described in the following paragraphs for the two areas.

1.2.5.1 EL Processes

At the beginning of the program, EL fabrication, as now, began with deposition of the Mo transparent electrode, and of the Y_2O_3 dielectric, but with substrate heat supplied by quartz-iodine lamp radiation. The need for substrate heating had been established earlier, in order to minimize cracking of the films because of thermal stress during the subsequent heat treatment. Quartz-iodine lamps, already used for pre-deposition substrate outgassing, were adapted for this use.

While radiative heating was helpful during the early development in obtaining high quality EL films, yield and uniformity were poor because of uncontrollable temperature variations over a given substrate or between one substrate and another. Initially on the program, a copper coating, slightly oxidized to increase absorption, was applied to the back of the substrate - the side on which the radiation was incident - in an attempt to obtain more uniform heating. This was somewhat more successful, but uniformity and reproducibility were still inadequate. Next the use of the transparent electrode as a resistance heater was tried. First experiments involved deposition

of Y_2O_3 dielectric only on the transparent electrode, followed by heat treatment in a separate vacuum oven and by visual examination for cracking or crazing. From these experiments it was determined that reproducible temperatures, reasonably uniform over a sizeable fraction of the substrate, could be obtained, and that a temperature of about 300°C was required to avoid problems of thermal stress during the subsequent 500-550°C vacuum oven bake cycle. However, allowance must be made for the difference in sticking coefficients for the arriving vapor stream between the heated substrate and the room temperature quartz crystal thickness monitor.

Full EL film fabrication was then attempted, still using resistance heating via the transparent electrode during both Y_2O_3 depositions. With the Mn-doped ZnS present, deposited at room temperature and prior to its heat treatment, problems were encountered during the second Y_2O_3 deposition with electrical breakdown, presumably due to conductive regions in the ZnS as the result of non-uniform Mn distribution. This problem was avoided by going to a second, dedicated heater, electrode on the back of the substrate. With this approach, the way was also opened for performing the ZnS heat treatment in place, immediately after its deposition. Studies are still underway to determine the optimum heat cycle; a temperature of 500°C for 1 hour is fairly successful.

1.2.5.2 TFT Processes

As with EL display elements, TFTs fabricated prior to this program had demonstrated characteristics suitable for the purposes of this program; in this case, for distributing gating signals via a BBD shift register; for directing on-off data to storage capacitors; and for switching EL elements in response to this stored data. Again, however, yield was low because of problems with reproducibility, and to a lesser extent, with uniformity.

Part of the reproducibility problem was felt to be related to the quality of a particular batch of CdSe semiconductor material; it was found that certain batches of CdSe produced good transistors while others produced bad or nonfunctional transistors. The "good" and "bad" batches of material were often obtained from the same supplier, were used in identical deposition procedures, and when subjected to chemical analysis produced results which indicated that both were of the same high and specified purity.

A possible reason for the differences between batches is thought to be very small variations in cadmium-to-selenium ratios, or stoichiometry. A material batch, for example, that was cadmium poor by one part in 10^6 would be difficult or impossible to identify by chemical analysis (impurities of less than one part per million can be readily measured, but these impurity techniques don't apply to measuring a variation among majority constituents) but could significantly or even radically affect the electrical properties of the semiconductor. Until recently, the only way to be assured of "good" material was to deposit transistors from samples of all batches. Those material batches that produced good transistors were good and those that did not were bad--a time consuming and costly method not appropriate to production of thin film devices.

To remedy this situation, a technique for adjusting and controlling stoichiometry during the deposition process was demonstrated. A nominally "poor" batch of CdSe was used to fabricate transistors. Transistor characteristics of double-gated sample devices were measured before application of the upper gate and dielectric layers. The devices did not exhibit transistor

action, i.e., there was no response to gate voltage steps. Cadmium was then deposited through the semiconductor masks and onto the existing CdSe layers at a very slow and controllable rate while transistor characteristics were continuously monitored. As the cadmium deposition proceeded, transistor action could be observed in the sample devices. The deposition and device monitoring were continued until the normal or "good" transistor characteristics were achieved. The cadmium deposition was stopped and transistor fabrication completed. The resulting devices exhibited both excellent performance and uniformity. This procedure has now been incorporated as a part of the standard TFT fabrication process.

As noted earlier, a heat treatment is required to develop the desired transistor characteristics. It is here that the results of uncontrolled process variables are first seen: it has not been found possible to use a single time-temperature cycle. The freshly-made transistors were formerly given a vacuum bake of 300°C for 3 hours, and then were tested at room temperature. Based on the results, one of a number of time-temperature cycles was selected for a second bake, followed by retesting, and so on until the desired characteristics were obtained. Overbaking must be avoided, for then the zero-gate-voltage drain current i_{dss} becomes excessive.

The mechanisms involved in changing the transistor characteristics have not been identified, but it is speculated that several are present. Grain regrowth in the polycrystalline semiconductor undoubtedly occurs; this results in increased carrier mobility and consequently in transconductance. Carrier density, and therefore threshold voltage, are also likely to change. Further threshold voltage changes can result from modification of interface states at the semiconductor-insulator boundary. There may also be diffusion of the source/drain material into the semiconductor, resulting in a decreased effective gap length.

Fortunately, these effects appear to be fairly uniform over a given substrate, permitting all devices to become operational with the same bake cycle.

Studies in this area have been aimed at obtaining desired transistor characteristics through real-time control of the bake cycle. The high-temperature resistance characteristics (drain to gate-source) are now monitored and correlated with room-temperature measurements. With this correlation firmly established, it is possible for each substrate to be custom baked, as it were, without the need for repeated testing and rebaking.

The rationale for this approach is based on experience at AESC in the fabrication and processing of PbS infrared detectors. Here, too, a polycrystalline semiconductor film sandwiched between dielectrics has its characteristics improved by heat treatment.

Additional studies have examined the effects of higher background oxygen pressure during Al_2O_3 dielectric deposition. Until recently, these higher pressures were limited to the mid-10^{-5} torr range by overheating of the sputter-ion pumps. Shortly before the program began, a turbomolecular pump was acquired and installed on the vacuum chamber used for TFT fabrication. With this added capability, it has been found that a background O_2 pressure of 2×10^{-4} torr results in improved dielectric strength and in more stable devices.

Based on this favorable experience, two more turbomolecular pumps are being purchased by the company for use on the vacuum chambers used in EL fabrication.

Section 2

CONCLUSIONS

During the past quarter, several important improvements were demonstrated in device fabrication processes, and are now incorporated in the deposition and post-deposition procedures. These are summarized below:

- Resistive heating of the EL substrate, both during dielectric deposition, and for heat treatment of the ZnS:Mn. Benefits which result from the more uniform and reproducible temperature are elimination of dielectric crazing, and more repeatable EL characteristics.
- In-chamber monitoring and adjustment of TFT semiconductor stoichiometry during fabrication, for more reproducible characteristics independent of CdSe batch.
- Capability of maintaining higher O_2 background pressure during TFT gate insulator deposition for improved dielectric properties.
- In-process monitoring and control of TFT characteristics during post-deposition heat treatment, again for better repeatibility of characteristics.

These process refinements taken together represent a major advance in progressing from procedures suited to a research atmosphere to processes appropriate to a manufacturing environment.

Circuit design has proceeded to the detailed layout of a small-scale display addressing circuit--two rows of four elements. This circuit which incorporates all of the features required to address the full-scale display, will permit assessment of performance, and will help identify and resolve any problem areas which may be encountered.

Section 3

PROGRAM FOR THE NEXT QUARTER

During the coming quarter, emphasis will shift from a largely investigative effort to one concerned more with fabrication and testing of devices and circuits suitable for use in the ultimate end product, a thin film EL display with integrated TFT addressing circuitry. Specifically, the following areas will be pursued:

a. Fabrication of metal masks for, and deposition of, the cascode switching circuit and the small-scale display addressing circuit

b. Beginning life tests of EL elements and TFTs.

c. Continuing design activities, especially in the area of display element--TFT integration

In addition, under company funding, the two vacuum chambers used for EL deposition will be equipped with turbomolecular pumps.

Section 4

PUBLICATIONS AND REPORTS

Neither presentations nor publications directly associated with this contract effort were generated during this reporting period.

Section 5

IDENTIFICATION OF PERSONNEL

The people who performed technical work on the program during the report period are listed in Table 3 together with the number of hours worked on the program by each. Resumes of each of these technical people are also included.

TABLE 3 PROFESSIONAL AND TECHNICAL PERSONNEL AND MANHOURS EXPENDED DURING FIRST QUARTER

Ken O. Fugate	179
William J. Helm	57
Jack M. Graf	24
William E. Staley	230
Mitchell E. Shaheen	60
Duane L. Bassi	136
Donald R. McMichael	72

K. O. FUGATE--Manager, Thin Film Devices Laboratory

Experience Brief

As Manager of the Thin Film Devices Laboratory, Mr. Fugate is responsible for the applied research, development, testing and production of thin-film devices, both for research and for operational system applications. Mr. Fugate has been associated with the laboratory for the past three years, and for 16 years has been with Aerojet in various capacities of engineering and engineering supervision and management associated with signal processing, communications, microwave, electroacoustic, infrared, and microelectronics research, development, and production programs.

Mr. Fugate was instrumental in converting the thin-film transistor from a laboratory curiousity to a viable integrated circuit technology used in a number of Aerojet systems and devices. Among his other achievements in the field, he recently demonstrated (under an Air Force contract) the feasibility and advantages of thin film charge transfer devices, and he initiated development of and then successfully demonstrated high-brightness thin film electroluminescent matrices for flat panel display applications.

He has a BS degree (EE and mathematics) from Oklahoma State University.

W. J. HELM--Project Engineer, Integrated TFT Display Program

Experience Brief

Mr. Helm joined Aerojet in 1958 with a BS degree in Physics from Heidelberg College and an MS degree in Physics from Case Institute of Technology. He has been involved since in a wide range of activities in electro-optics; the design, development, and operation of measurement instruments--radiometers, spectrometers, interferometers and entire measurement systems; the development, manufacture and characterization of visible and infrared detector materials and devices; the development of electronics for electro-optical reconnaissance and surveillance systems.

Mr. Helm has been a major contributor to the development of thin film electronics technology and fabrication capability at Aerojet, particularly in the design and development of the thin film deposition equipment and facilities. He led the effort to establish manufacturing processes for thin film, hybrid preamps for a spaceborne surveillance system--processes which have subsequently yielded tens of thousands of preamps and millions of hours of spaceborne operation.

JACK M. GRAF--Senior Engineering Analyst

Experience Brief

Mr. Graf currently supervises the high-resolution photo-fabrication of deposition masks for thin-film applications, and configuration design for high-yield photo sensitive detector devices. With Aerojet since 1958, he has engaged in optical design of advanced sensor devices, and testing of a wide variety of imaging instrumentation for ground-based and spaceborne applications in various spectral ranges from ultraviolet to infrared.

Mr. Graf designed and built special photo-fabrication facilities for the production of special modulation devices. This task included responsibility for production of the first metal-etched, high actuance, photo-fabricated, continuous modulation device known.

He has undertaken specialized studies in photo fabrication processes, photo instrumentation systems and techniques, and related electronic and optical technologies at the University of Southern California, University of California at Los Angeles, New York University, and New York Institute of Applied Arts and Sciences.

WILLIAM STALEY--Senior Engineer Analyst

Experience Brief

Mr. Staley has had 25 years of engineering experience including 18 years in basic research at Allegheny Industries Corporation where he received the Frank Loundsberry award for engineering achievement, and was granted three patents in metallurgical processing and testing.

Mr. Staley has been a key member of the Thin Film Devices Laboratory since joining AESC in 1968. His many contributions to thin film technology include the development of: techniques for deposition of a wide variety of insulating, conducting, electroluminescent and semiconductor materials; devices and procedures for improving alignment and registration of thin film depositions; cryogenic testing fixtures for thin film circuits; improvements in electron beam gun vaporization techniques and equipment; substrate scribing techniques. He is a specialist in the techniques, procedures and equipment of thin film deposition and has been a major contributor to their development. He is at present project leader in electroluminescent films.

He majored in chemistry and metallurgy at Pennsylvania State College.

M. E. SHAHEEN--Senior Member Technical Staff

Experience Brief

Mr. Shaheen who has been at AESC since 1973 works on photo lithographic processes and the development and fabrication of the masks used in thin film deposition. He has worked previously as a Materials and Process Engineer for Itek's Applied Technology Division, as a Quality/Process Engineer for Fairchild Semiconductor, as a Process Control Engineer for Lockheed Missile and Space Co., and as a Physical Metallurgist for Pratt and Whitney Aircraft. Mr. Shaheen has a BS degree in Chemical Engineering from Northeastern University.

DUANE L. BASSI--Engineering Technical Specialist

Experience Brief

Mr. Bassi has worked at AESC for the past 13 years on various electronic programs and assignments and was Instrumentation Foreman on the SNAP-8 Program from 1963 to 1971.

From 1971 to the present, Mr. Bassi has been associated with the Thin Film Devices Laboratory and has become a specialist in the operation of vacuum deposition systems. He was a key participant in the development of stable lead sulfide thin film transistors, and has most recently been project leader in the development of the cadmium selenide thin film transistor to an equivalent high level of performance.

D. R. McMICHAEL--Senior Engineering Laboratory Technician

Experience Brief

Mr. McMichael has been at Aerojet since 1965 and has been associated during this time with the development of microelectronics and thin film technology at the company. He has worked as a microelectronics manufacturing technician in every phase of testing, data gathering and analysis; has done everything from design layout through breadboarding in the development of digital circuitry; has been responsible for the design and setup of manufacturing work stations and assembly aids.

Mr. McMichael has been a member of the Thin Film Devices Laboratory since 1971, working on the development of electroluminescent displays and associated circuitry, particularly the test and evaluation of display elements and devices.

He has been an Air Force Radio and Radar Repairman (15 months of Air Force education), has an AA degree in Electronics Studies from Oklahoma State University and is currently working for a B.S. Engineering at California State Polytechnical University.

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