DAMAGE PROFILES IN SILICON AND THEIR IMPACT ON DEVICE RELIABILITY

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Technical Report Number 2
April 1, 1977 - September 30, 1977

Prepared by

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Contract No. N00173-76-C-0303
Effective Date of Contract: 10/1/76
Contract Expiration Date: 4/1/78
Amount of Contract: $277,120.00

Advanced Research Projects Agency
ARPA Order No. 3231, Program Code No. 6D10
Form approved budget bureau No.: 22-R0293

Unclassified

Security Classification

DOCUMENT CONTROL DATA - R&D

(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1. ORIGINATING ACTIVITY (Corporate author)
International Business Machines Corporation
System Products Division, East Fishkill
Hopewell Junction, N.Y. 12533

2a. REPORT SECURITY CLASSIFICATION
Unclassified

2b. GROUP

(6) 3. REPORT TITLE
DAMAGE PROFILES IN SILICON
AND THEIR IMPACT ON DEVICE RELIABILITY

(9) Technical rept. no. 2.
1 Apr – 30 Sep 77.

4. DESCRIPTIVE NOTES (Type of report and inclusive dates)
Scientific April 1977 to September 1977

5. AUTHOR(S) (First name, middle initial, last name)

(10) G.H. Schwuttke and K. H. Yang

6. REPORT DATE	7a. TOTAL NO. OF PAGES	7b. NO. OF REFS
(11) September 1977	77	34

8a. CONTRACT OR GRANT NO.	9a. ORIGINATOR'S REPORT NUMBER(S)
(15) N00173-76-C-0303	(14) TR22.2157
b. PROJECT, TASK, WORK UNIT NOS. ARPA Order-3237	
c. DOD ELEMENT	9b. OTHER REPORT NO(S) (Any other numbers that may be assigned this report) NRL 535440
d. DOD SUBELEMENT (12) 109p.	

10. DISTRIBUTION STATEMENT
APPROVED FOR PUBLIC RELEASE
DISTRIBUTION UNLIMITED

11. SUPPLEMENTARY NOTES	12. SPONSORING MILITARY ACTIVITY
	Advanced Research Projects Agency

13. ABSTRACT

The influence of oxygen on the minority carrier lifetime of silicon is reported. Bulk annealed, oxygen-rich crystals subsequently sliced into wafers show lifetime degradation with annealing time. Silicon oxide precipitates and punched out dislocation loops induced during annealing are identified as electrically active defects responsible for the observed lifetime degradation. Increase in device yields (diodes) and improved lifetime in epitaxial films obtained with oxygen-rich wafers as substrates are a result of 'intrinsic gettering' of oxygen-rich wafers. It is shown that 'external gettering' can not improve minority carrier lifetime in silicon wafers if during processing 'intrinsic gettering' is activated. It also shows that "external gettering" such as impact sound stressing (ISS) is very effective in improving lifetime for wafers not containing 'intrinsic gettering' sources.

Unclassified

Security Classification

401917

i

14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Silicon Oxygen precipitation Impact Sound Stressing Defect analysis Transmission Electron Microscopy						

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Introduction

This contract is a continuation of Contract No. DAHC 15-72-C-0274 entitled "Damage Profiles In Silicon and their Impact on Device Reliability". Results of the previous contract are published in Technical Reports numbered 1 - 7. The Tables of Contents of these reports are given in the preface.

Research to be performed under the present contract which started October 15, 1976 is outlined in the Research Plan. The work under the present contract is essentially a continuation of the original work (silicon) and also an application of this work to other materials (damage gettering in GaAs).

The following Technical Report No. 2 concludes and summarizes the investigation on the influence of oxygen in annealed silicon (bulk and wafer form) on minority carrier lifetime. It is self-contained and therefore published as a separate technical report. The other work performed during the time period April 1, 1977 to September 30, 1977 relates to the influence of ion implantation in silicon on minority carrier lifetime and to damage studies in GaAs after ISS. This work is being reported separately in quarterly reports and will be summarized in the forthcoming Technical Report 3.

RESEARCH PROGRAM PLAN

1. Study point defects in silicon and GaAs crystals, their generation and reactions during wafer processing and their interactions with damage profiles introduced by:
   a. Impact Sound Stressing
   b. Ion Implantation
   c. Diffusion

2. Produce damage profiles in silicon wafers through ion implantation techniques and study their influence on minority carrier lifetime before and after annealing.

3. Determine the influence of studies listed under (1) and (2) for Czochralski and Float Zone silicon crystals.

4. Study epitaxial layer perfection of silicon deposited on ion implanted silicon surfaces in the presence and/or absence of Impact Sound Stressed wafer backsides.

5. Study minority carrier lifetime in epitaxial layers produced as listed under (4).

6. Use advanced modern analytical characterization techniques for the studies listed under (1) to (5) such as Transmission Electron Microscopy, Scanning Electron Microscopy, X-ray Topography, Precision Lattice Parameter Measurements and Lifetime Measurements.

7. Develop new characterization techniques as needed.

8. Correlate damage measurements with electrical measurements whenever possible (relate damage profile to junction quality).

Highlights of the Report

Variations of minority carrier lifetime observed in silicon wafers cut from bulk annealed crystals and observed in wafers prepared from crystals not pre-annealed but annealed as "standard" wafers are reported.

The investigations are done on silicon containing high (~ 10^{18} atoms/cm^3) and low amounts (5 x 10^{17} atoms/cm^3) of oxygen. The investigations include zero dislocations and approximately 10^4 dislocations/cm^2 wafers and cover the temperature range from 900°C to 1250°C.

Bulk annealed crystals subsequently sliced into wafers show lifetime degradation with annealing time. The lifetime decrease is less severe in dislocated crystals with an original lifetime of 10 μsec as compared to dislocation-free crystals with an original lifetime of 100 μsec. The lifetime values in both types of crystals converge after 40 hours of annealing to approximately 1 μsec.

The lifetime degradation is correlated with the actual defect state produced in the active device area through annealing. Silicon oxide precipitates and punched out

dislocation loops are identified as electrically active defects responsible for the observed lifetime degradation.

Evidence is presented that under actual semiconductor device (diode) processing conditions silicon wafers cut from crystals not pre-annealed may influence "leakage limited yield of diodes" depending on the amount of oxygen present in the silicon wafers.

Findings on the out-diffusion of oxygen in oxygen-rich ($\sim 10^{18}$ atoms/cm^3) wafers, as a result of semiconductor device processing, (reported previously by other workers in the field) are confirmed.

Increase in device yield (diodes) and improved lifetime in epitaxial films obtained with oxygen-rich silicon wafers as substrates are correlated with the "intrinsic gettering" action of oxygen-rich wafers.

It is shown that "external gettering" cannot improve minority carrier lifetime in silicon wafers if during processing "intrinsic gettering" is active.

It is also shown that "external gettering" is very effective in improving lifetime in silicon wafers not containing "intrinsic gettering" sources.

In such wafers external gettering techniques such as Impact Sound Stressing (ISS) improve the lifetime distributions to values obtained in oxygen-rich wafers.

A total Transmission Electron Microscopy analysis of the defect state in all wafers investigated has also been performed and the results are correlated with the lifetime properties measured.

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MINORITY CARRIER LIFETIME IN ANNEALED SILICON CRYSTALS CONTAINING OXYGEN

by

K. H. Yang, H. F. Kappert and G. H. Schwuttke

1. INTRODUCTION

Today one of the most urgent research problems in silicon relates to the control of minority carrier lifetime in heat treated silicon. By now it is well established that lifetime in silicon depends strongly on variations in the structure of complex micro defects that form or dissolve during high temperature processing of the silicon wafer. Such micro defects are summarized under the term "swirl" which relates to their swirl-like distribution observed in a wafer. The density of defect clusters in a "swirl" is not homogeneous and can vary substantially across a wafer surface and also from wafer to wafer even if cut from the same crystal. The defect density in a swirl is called high if the cluster density is approximately 10^6 to $10^7 cm^{-3}$. In a low swirl concentration one counts approximately 10^3 clusters per cm^3. Normally the swirl density is determined

by chemical etching which reveals each defect cluster as a tiny etch pit. Swirl distributions in silicon wafers are readily seen in X-ray topographs because the crystal defects in the swirl produce excess diffraction contrast.

Swirl formation is typical for dislocation-free crystals. During crystal growth from the melt, the crystal region adjacent to the melt will contain the vacancy equilibrium concentration associated with the melting point of silicon (1420^{o}C). During cooling of the crystal the vacancy concentration decreases and the crystal becomes supersaturated with vacancies at room temperature. If the crystal contains dislocations the vacancies precipitate along the dislocations (jogs) and are thus annihilated. If the crystal is dislocation-free no vacancy sinks are present and the crystal becomes supersaturated with vacancies resulting in the nucleation and growth of vacancy clusters. This process becomes more complicated when impurities are present in the crystal. Therefore, swirls in Float Zone crystals (pure) differ in their crystallographic structure from swirls in Czochralski crystals which contain large amounts of oxygen (carbon) and sometimes metallic impurities. Swirls in Float Zone crystals consist of interstitial dislocations loops and precipitates (1,2). Such defects have been shown to cause excess leakage

currents in p-n junctions (3,4). In Czochralski crystals swirls are readily observed after annealing at high temperature in crystal sections where the oxygen concentration was high before annealing. Therefore, swirl defects in Czochralski crystals are commonly related to oxygen precipitation phenomena (5-10). The dominant crystal defects generated in the precipitation process are oxide precipitates, punched out dislocation loops, extrinsic stacking faults, and interstitial dislocation loops (6-9). Such bulk defects act as sources for micro-plasmas, are recombination centers, and cause leakage current in p-n junctions (11-13).

Czochralski crystals are still the main silicon wafer source for the semiconductor industry (bi-polar and MOS devices). Consequently, a large amount of research has been expended in the study of swirl defects and their influence on device properties (14-18). Most interesting are the results of Tan, et al.(19) which indicate that swirl defects can act as intrinsic gettering sites in Czochralski crystals and thus improve device yield.

These results (19) are supported by the work of Graff and Pieper (20) which investigates the influence of swirls in Float Zone and Czochralski crystals on minority carrier

lifetime after annealing in the range of 200 to 800°C. They observe variations in minority carrier lifetime after every annealing cycle and relate these changes to variations in the complex structure of micro defects making up the swirls. They observe several maxima for the minority carrier lifetime below 700°C annealing and another one around 800°C. Higher annealing leads to continuous decline in minority carrier lifetime. To explain these variations in lifetime they point to the importance of defect reactions with oxygen and other impurities which result in a "gettering" effect. Gettering is activated at certain temperatures. This is observed experimentally as an improvement in minority carrier lifetime. Such a gettering cycle (350°C to 450°C; formation of oxygen donor complexes) is followed by a cycle where oxygen complexes are dissolved resulting in a decrease of carrier lifetime. These measurements have been confirmed in part by Helmreich and Sirtl (21). They point out that the high temperature maximum (800°C) reported in Ref. (20) must be related to a pronounced formation of nucleation centers which starts at 800°C. Such centers are certainly preferred locations for precipitation of impurities such as copper.

Our investigations address variations of minority carrier lifetime versus swirl formation in Czochralski silicon after

annealing in the temperature range of approximately 900°C to 1250°C. This temperature range is most interesting for semiconductor processing. In this context a number of experiments are performed. The experiments deal with the measurement of minority carrier lifetime by MOS C-t measurements after various annealing cycles of substrates containing low and high amounts of oxygen as well as zero dislocations and $10^4/cm^2$ dislocations. The use of the MOS C-t technique enables us to measure lifetime distribution across a wafer surface before and after heat-treatment. The lifetime measurements are correlated with the actual defects state in the crystal under the MOS capacitor. Thus an exact correlation between defects and lifetime is obtained after every annealing temperature. In addition, the crystallography of single defects is determined through high resolution transmission electron microscopy.

2.0 EXPERIMENTAL

Silicon crystals used for this study are Czochralski grown and doped with boron to a resistivity of about two Ω-cm. Both <001> and <111> oriented crystals are investigated. The <001> oriented crystals are dislocation-free, while the <111> crystals have a $10^4/cm^2$ dislocation density of grown-in dislocations as determined by x-ray topography and

preferential etching. Three slugs, each about 2 inches in length, are cut from each crystal. The letters A, B, and C indicate the position of the slug cut from somewhere near the crystal seed (A), from the middle (B), and from the very end of the crystal (C).

Lifetime measurements are made through the MOS C-t technique described by Fahrner and Schneider (22). This technique allows relatively fast large-scale measurements of generation lifetime in the range 1 msec to 0.1 nsec. For the measurements a metal oxide semiconductor (MOS) capacitor is biased into strong inversion and subsequently switched into deep depletion. An appropriate experimental setup prints out or displays a typical MOS recovery time, which is introduced into a computer fed by a theoretical generation-lifetime model and the pertinent wafer data. Thus minority carrier generation lifetime values of the silicon under the MOS capacitor (depletion zone) are obtained. The error limit of this technique, compared with a Zerbst plot, is less than 20% for lifetime values $\tau \leq 10$ μsec. For $\tau > 1$ msec the error can increase to 100%.

Silicon wafers are processed to contain two groups of circular MOS capacitors. Each group consists of 72 capacitors of different dot size. One group uses 1.5 mm

diameter dots, and the other 0.5 mm dots. For MOS processing the wafers are first cleaned in a solution of NH_4-H_2O_2, HCl-H_2O_2, and HF. Subsequently, a 5000 Å thick oxide is grown at 1000°C using a dry-wet-dry oxidation cycle. Aluminum metallurgy is used. After metallization, the wafers are annealed for 15 minutes at 400°C in forming gas.

For device studies phosphorus diffused N^+-p diodes are made by first growing a 5000 Å thick oxide at 1000°C using a dry-wet-dry oxidation cycle. After pattern etching, $POCl_3$ is deposited at 870°C and driven in at 1000°C. The junction depth of the diodes is 1.4 μm. At least 148 diodes are measured on each wafer.

The n-type epitaxial films are grown on 15 ohm-cm, (001), p-type substrates by the hydrogen reduction of $SiCl_4$ at 1100°C. The films are 6 μm thick. The dopant (arsenic) concentration in the film ranges from 0.8 to 1.6 10^{16} As atoms/cm^3. After the epitaxial deposition a dry oxide, 1400 Å thick, is grown on the epitaxial film at 1100°C. The minority carrier lifetime in the film is measured using capacitors of 0.5 mm in diameter.

For the study of swirl formation, wafers and longitudinal sections (parallel to the growth axis) are cut from each

A,B,C section of a crystal. The sections are annealed at temperatures of 1000, 1050, 1100 and 1150 ^{o}C in oxygen or nitrogen ambient. The annealing time is 2, 4, 8 or 16 hours.

For the study of bulk defects, A, B, C slugs are first heat-treated and subsequently cut into wafers. Longitudinal sections are cut from the A, B, C slugs with the surface normals in <110> directions. Before processing, all wafers are lapped, first chemically and then chemically-mechanically polished.

X-ray topographs used in the study are recorded with $MoK\alpha_1$ radiation. Oxygen concentrations in silicon wafers are calculated from the infrared absorption at 9 μ (23). In the transmission electron microscopy (TEM) investigations specimens are examined in a Hitachi microscope with 200 keV accelerating voltage and a $\pm$ 30^{o} tilting stage, or in a JEOLCO microscope with 100 keV accelerating voltage and a $\pm$ 60^{o} tilting stage.

3.0 Swirl Defects and Minority Carrier Lifetime

3.1 Electrical Measurements in Substrates

Lifetime measurements made on annealed silicon samples

(oxygen concentration ~ 10 x 10^{17} atoms/cm^3 for (001), ~ 15 x 10^{17} for (111) crystals) are summarized in Fig. 1. The swirl defects are induced by annealing the crystals at 1100°C for several different time periods. After annealing the [001] crystals are sliced into (001) and (110) slices. The [111] crystals are sliced into (111) wafers. The heat-treatment of crystal slugs allows one to avoid the problems associated with out-diffusion of oxygen encountered during the annealing of wafers. Thus direct measurements of the influence of swirl defects on generation lifetime can be made using the MOS technique. Figure 1 shows that before annealing the lifetime is typically in the range of 100 μsec for the (001) wafers and the (110) slices. Due to formation of swirl defects, the lifetime decreases to about 1 μsec after 40 hours of annealing in N_2. Further annealing does not seem to degrade the lifetime significantly. For (111) wafers the lifetime before annealing is relatively low, about 7 μsec, due to the presence of dislocations. The dislocation density in these wafers is about 5-10 x 10^3 per cm^2 as determined by etch pit counts. The lifetime decreases to 1.5 and 0.9 μsec after 20 and 40 hours of annealing in dry oxygen, respectively.

3.2 Formation of Swirl Defects in Substrates

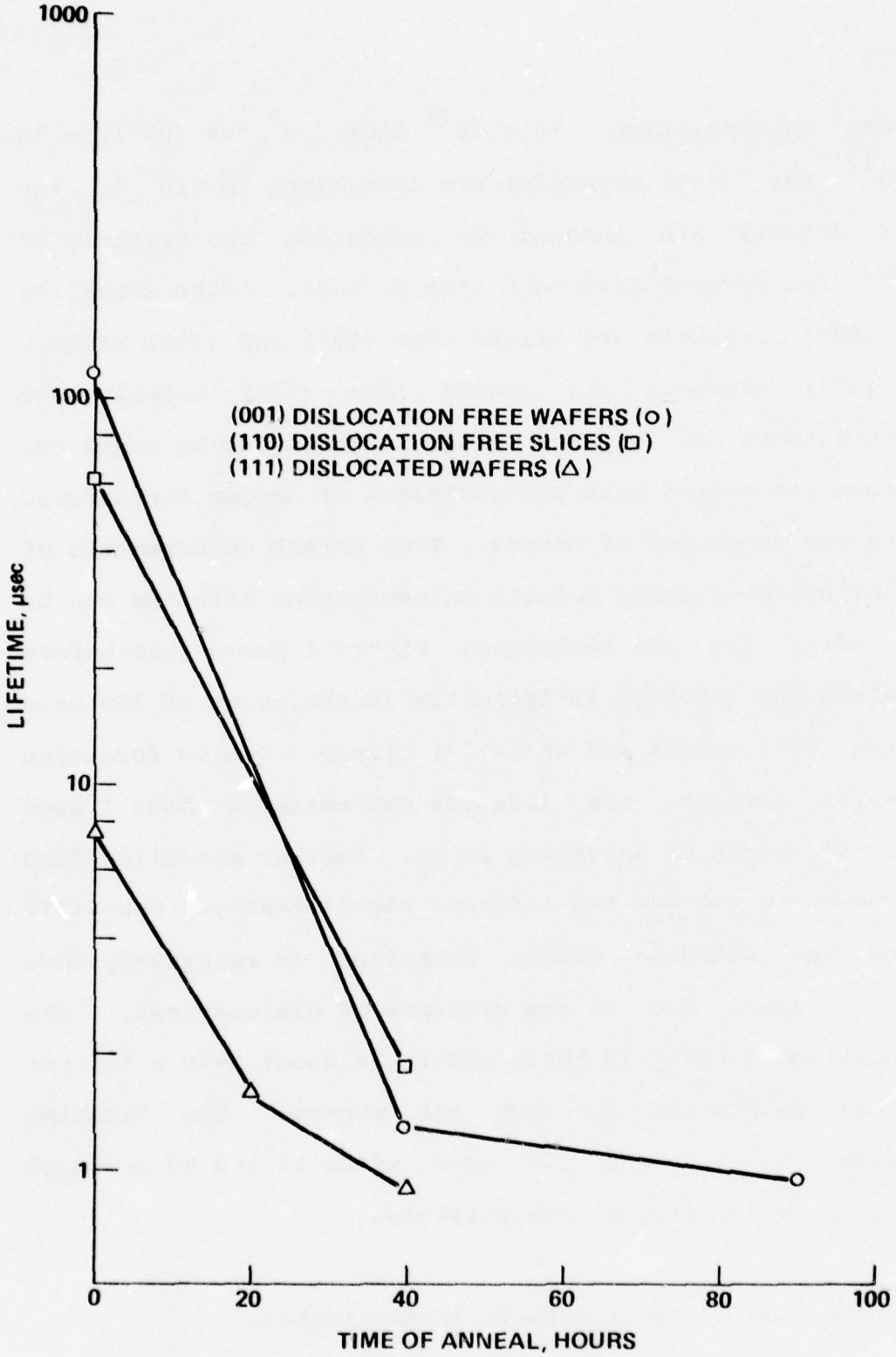


Fig. 1. The influence of annealing on the lifetime of silicon. Annealing temperature 1100°C

3.2.1 Oxygen Concentration and Swirls

Infrared measurements indicate that the dissolved oxygen concentration varies significantly with crystal position. As shown in Table I, the concentration decreases monotonically from section A through section B to section C. The concentration is about ~ 10-11 x 10^{17}, ~ 8-9 x 10^{17} and ~ 5 x 10^{17} atoms/cm^3 in section A, B, and C, respectively. After annealing, section A and B show a sharp decrease in oxygen concentration while the concentration in Section C remains nearly the same. The solubility of dissolved oxygen in silicon is about 4 x 10^{17} atoms/cm^2 at 1100°C. These measurements indicate that oxygen precipitation occurs only in wafers having an initial oxygen concentration exceeding the solubility limit at the annealing temperature.

The formation of swirl defects is therefore strongly dependent on wafer position in the bulk crystal. After annealing, swirl defects are only observed in wafers cut from section A and B, but not in those cut from section C even after 60 hours of annealing at 1100°C.

X-ray topographs representing section A, B and C wafers are given in Figs. 2(a),(b),(c), respectively. Quite often, swirl defects assume cloudy or spiral patterns in section A, and appear as concentric rings in section B.

TABLE I. Oxygen Concentration in Silicon Wafers Before and After Heat Treatment

Crystal	Orientation	Dislocation density	Section	Oxygen Content	
				Before anneal 10^{17} atoms/cm^3	After anneal 10^{17} atoms/cm^3
1*	(001)	0	A	9.3 - 10.4	7.2 - 8.1
			B	8.7 - 9.5	7.4 - 8.0
			C	4.6 - 5.3	3.9 - 4.5
2*	(001)	0	A	9.5 - 11.8	6.5 - 7.5
			B	9.3 - 9.8	7.5 - 8.0
			C	4.9 - 5.4	4.2 - 5.0
3**	(111)	5 - 10x10^3/cm^2	A	14.1 - 18.1	6.3 - 7.3

*Heat-treated in dry oxygen at 1100°C for 16 hours
**Heat-treated in dry oxygen at 1100°C for 60 hours

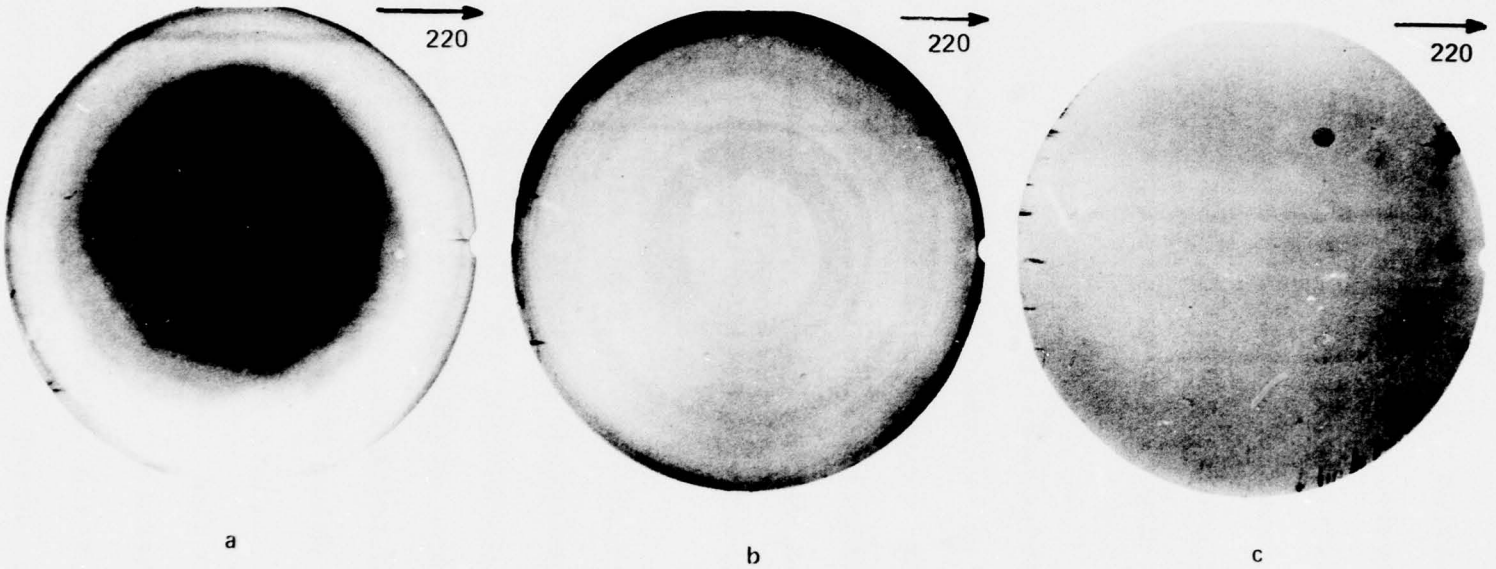
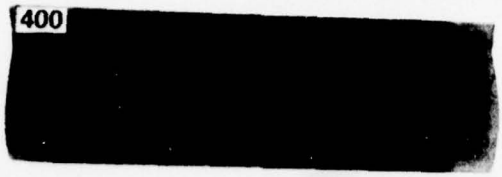


Fig. 2. X-ray topographs showing swirl formation in (a). Section A, and (b). Section B, but not in (c). Section C of a crystal after 16 hours of annealing at 1050°C in dry oxygen.

The swirl formation is also greatly affected by the annealing temperature. For wafers of section A and B, swirl formation, as determined by its detectability in x-ray topographs, requires approximately eight hours of annealing at 1000°C, four hours at 1050°C, two hours at 1100°C or 90 min. at 1150°C in dry oxygen or nitrogen ambient.

From these observations, it follows that swirl defects are only observed in wafers initially supersaturated with oxygen, and that swirl formation is accompanied by a reduction of dissolved oxygen. The process of swirl formation accelerates as the degree of oxygen supersaturation and the annealing temperature increases.

Longitudinal sections of silicon slugs are also investigated. Before annealing striated contrast is faintly visible in x-ray topographs as shown in Fig. 3(a). This contrast indicates the existence of internal strain at the position of the isotherm of the solid-melt interface after crystal growth. Using the double-crystal method, Abe et al. (24,25) showed that the internal strain arises from localized distortion of the lattice parameter at the solid-melt interface. The striated contrast has been observed in crystals grown by various techniques (26). After annealing, x-ray contrast is much more intense as



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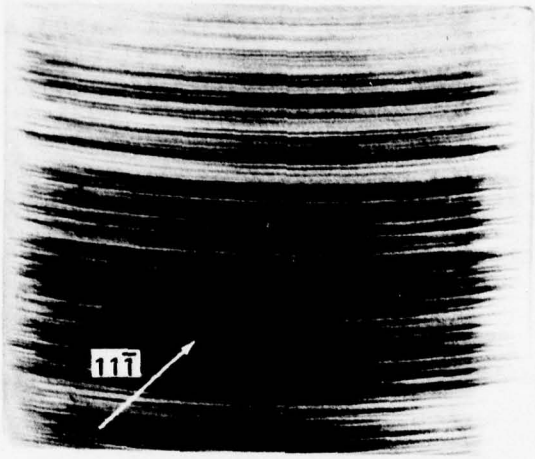

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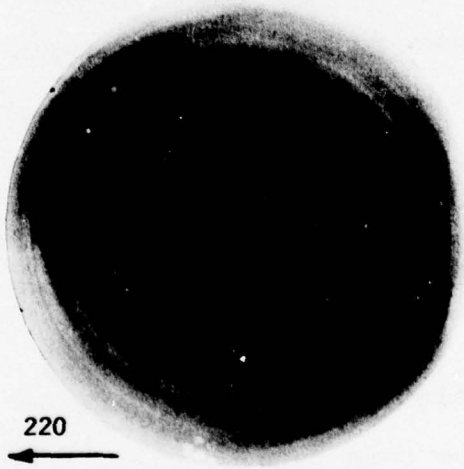


c

Fig. 3. X-ray topographs showing (a) the strain centers at solid-melt interface after crystal growth (longitudinal view (011) surface), (b) striated patterns as the shape of solid-melt interface developed after 90 hours of annealing at 1100°C in nitrogen (longitudinal view (011) surface) (c) cross-sectional view of (b), (001) surface.

shown in Fig. 3(b) for the longitudinal view and in Fig. 3(c) for the cross-sectional view. A comparison of Figs. 3(a),(b) suggests that swirl formation arises from precipitation of supersaturated oxygen at strain centers existing after crystal growth. The swirl pattern in Fig. 3(c) is the projection of the striated pattern shown in Fig. 3(b).

3.2.2 Analysis of Swirl Defects in Dislocation-Free Crystals

Chemical Etching and X-ray Topography

X-ray topography and preferential etching are used to obtain an overview of the nature of swirl defects. A portion of Fig. 3(b) is shown in Fig. 4(a) at highest magnification. It reveals that there are two types of major defects present in the annealed crystals. The first ones are defects arranged in a striated pattern at a regular spacing of 100 to 500 μm. The other ones are stacking faults.

Using the $(1\bar{1}1)$ reflection, faults lying in $(11\bar{1})$, $(\bar{1}11)$ and (111) planes can be seen in Fig. 4(a). Faults in the $(\bar{1}1\bar{1})$ plane are out of contrast for this reflection. Sirtl etching of a similar area reveals that the defects in the striated patterns consist of bands of etch pits with a band spacing of 100 to 400 μm, almost equal to the spacing

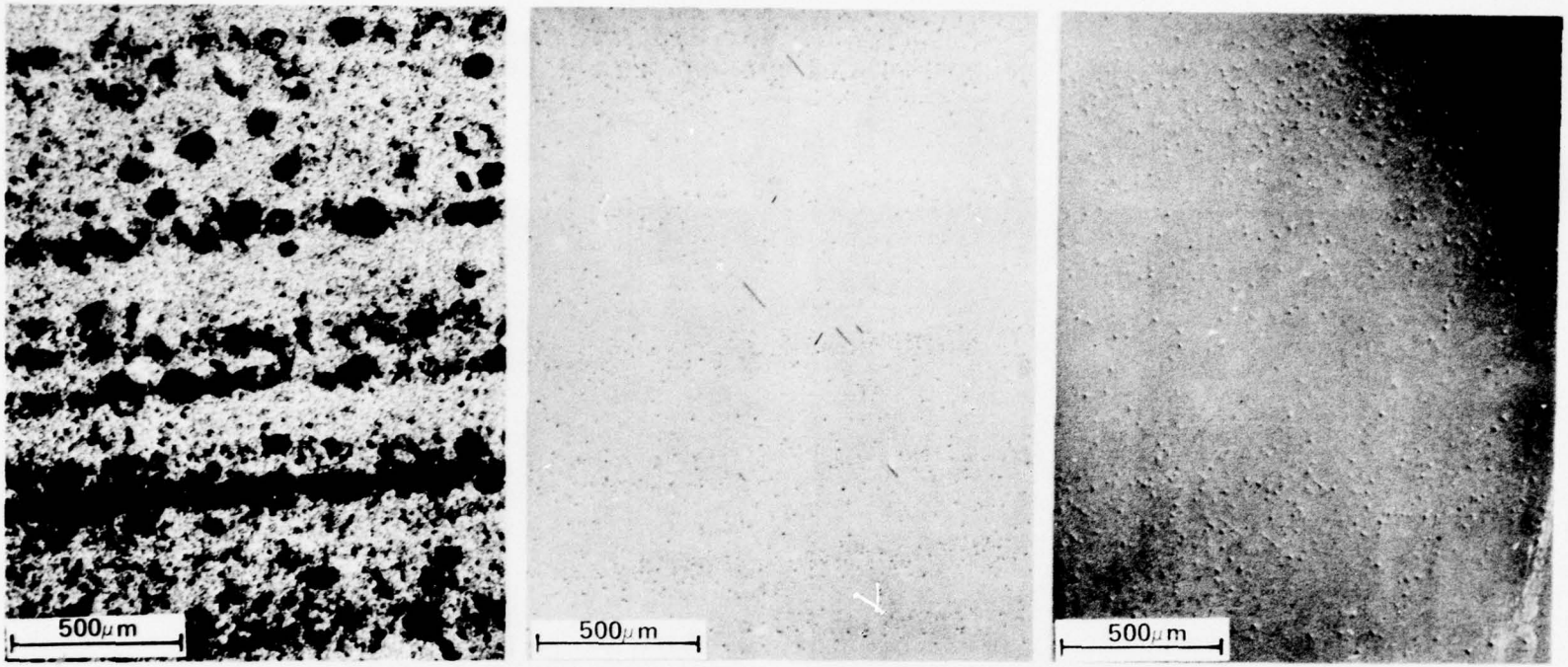
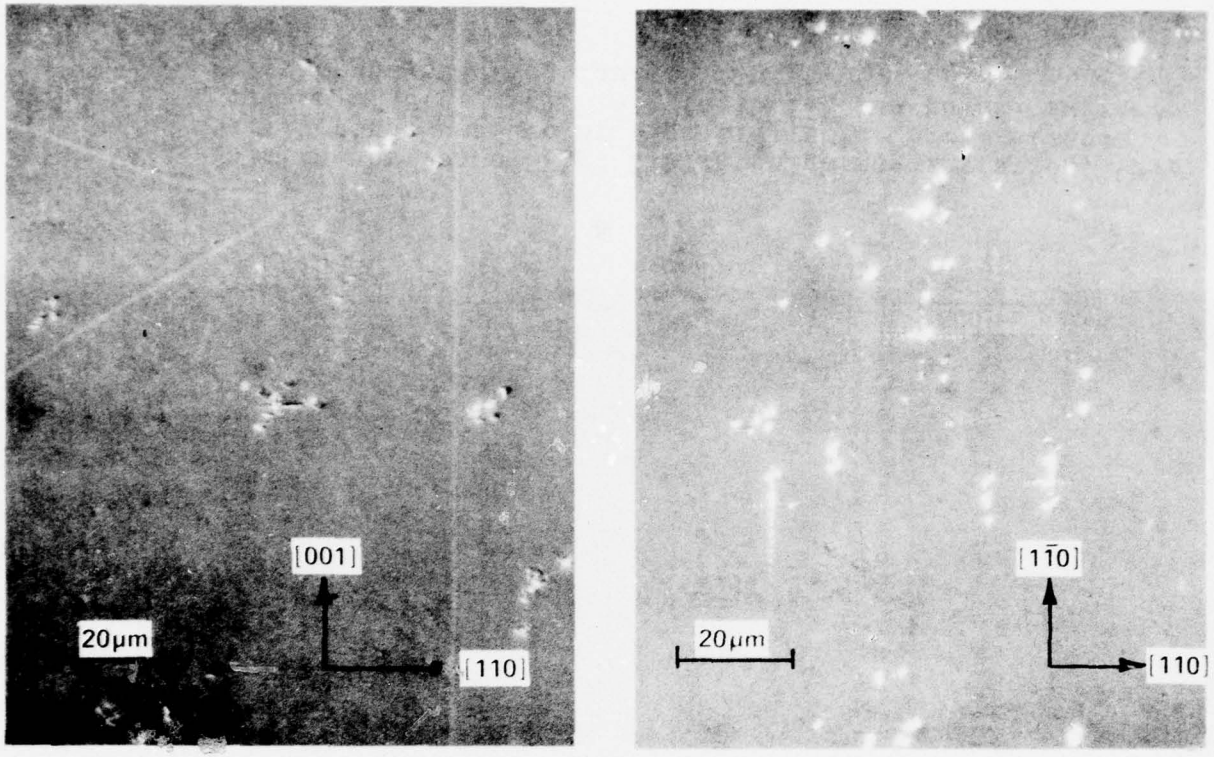


Fig. 4. (a). A portion of Fig. 2(b) at high magnification, (b). Sirtl etched surface of Fig. 2(b),(c). Sirtl etched surface of Fig. 2(c). All these figures reveal swirl defects and stacking faults.



d e

Fig. 4. (d) and (e), a portion of (b) and (c), respectively, at high magnification.

estimated from the X-ray topographs. In addition, Sirtl etching reveals also those stacking faults lying in $(11\bar{1})$ and $(\bar{1}1\bar{1})$ planes perpendicular to the (011) surface, but fails to reveal these faults in $(\bar{1}11)$ and (111) planes making an angle of 35.3^{o} with the surface. Investigation of etched (001) surfaces (cross-sectional view Figs. 4(b),(c)) shows essentially the same result. Stacking faults intersecting the surface in <110> directions can also be seen in Figs. 4(b),(c). The etch pits are shown at high magnification in Figs. 4(d),(e) for (110) and (001) surfaces, respectively. The nature of the swirl defects is further investigated by transmission electron microscopy.

Transmission Electron Microscopy (TEM) of Precipitates

TEM investigation indicates that in the area of swirl defects a high density of dislocation loops exists, punched out by precipitates. The geometric shape of the precipitates varies with the different projections in the Transmission Electron Microscopy. They are square, rhombic and hexagonal on (001), (011) and (111) projections, respectively. The (001) and (011) projections are obtained from the cross-sectional and the longitudinal view of a <001> oriented crystal and are shown in Figs. 5 and 6(a). This shape of the precipitates is confirmed by tilting the

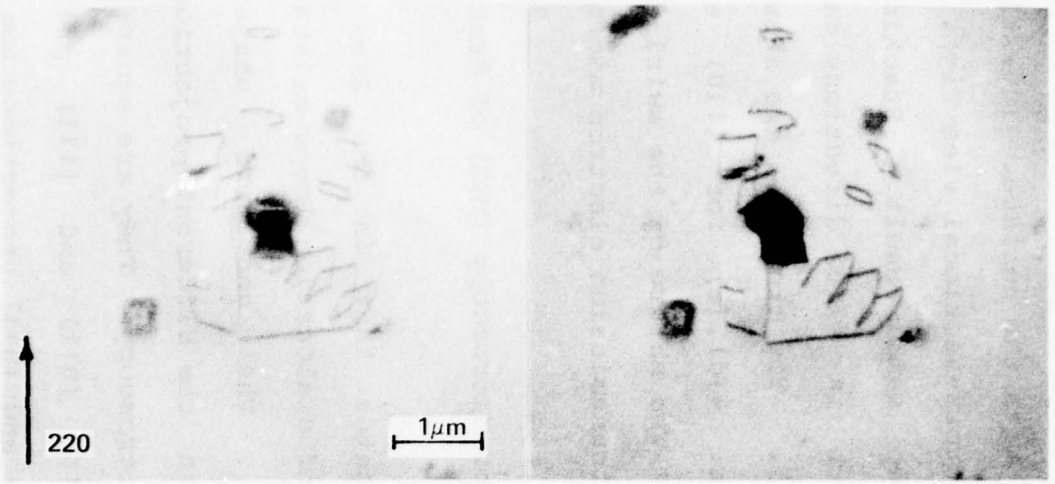


Fig. 5. Stereomicrograph showing a precipitate on (001) projection.

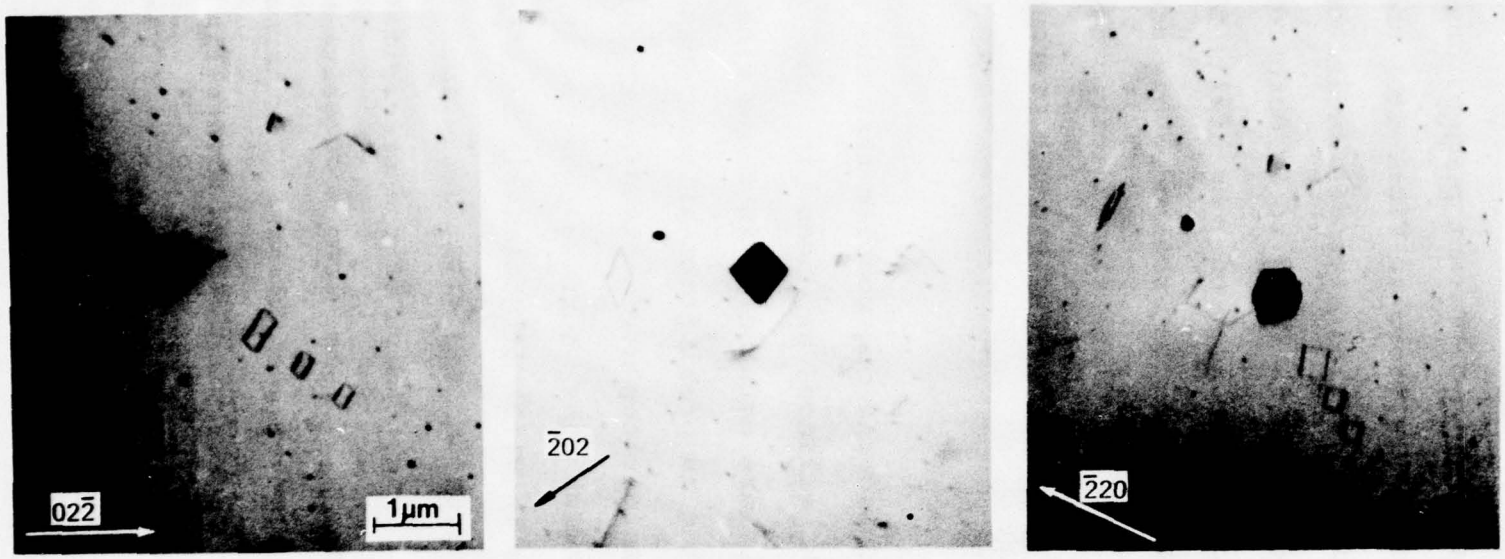


Fig. 6. TEM micrographs showing a precipitate on (a) (011) projection, (b) (010) projection, (c) (111) projection

specimen of Fig. 6(a) into different projections. The (010) and (111) projections are shown in Figs. 6(b) and 6(c). The geometric shape of the precipitates can be deduced from such tilting experiments. It is found to be octahedral with the precipitate-silicon interface on the {111} planes of the silicon matrix. A schematic drawing of one precipitate is shown in Fig. 7 and its different geometric shapes as they appear in the different projections are presented in Figs. 8(a) through 8(d).

These geometric considerations confirm that the precipitates in annealed bulk silicon as seen in the transmission electron microscope are octahedral in shape with the silicon {111} planes serving as precipitate-silicon interfaces. The edges of the precipitates are defined by the directions of intersections between the surface planes and the <111> planes. They are in <110> directions in both the <001> and <111> oriented samples, and in <112> directions in the <011> oriented samples. The shape of the precipitates suggests that their formation arises from successive reactions of oxygen with the {111} silicon planes. Furthermore, it also suggests that the precipitates are crystalline. However, electron diffraction patterns fail to reveal extra dots resulting from the precipitates. Thin platelet precipitates

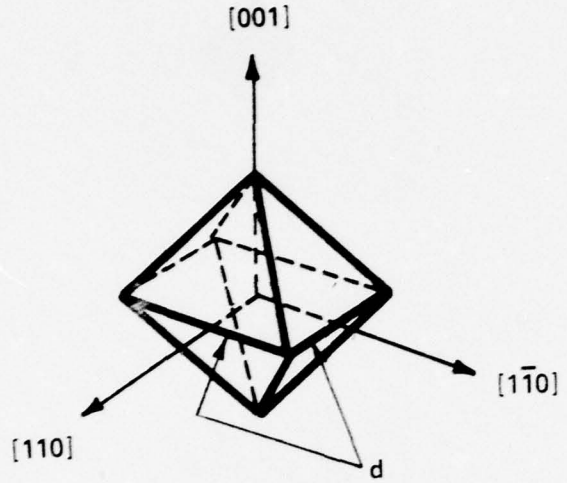


Fig. 7. A schematic drawing of the shape of a precipitate.

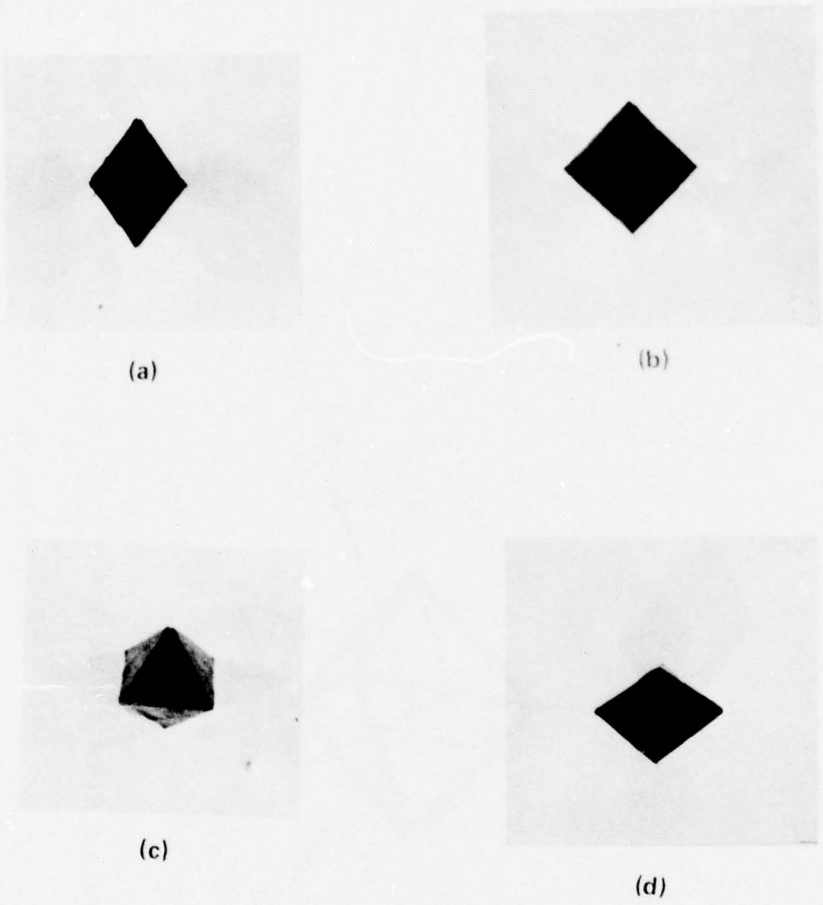


Fig. 8. A model of a precipitate on (a) (011), (b) (010), (c) (111), and (d) (101) projection.

having {001} habit plane as observed in the sub-surface of annealed silicon wafers (7-9) have not been found in the present study.

The precipitates formed during a particular annealing cycle are quite uniform in size. The size, d in Fig. 7, increases with annealing time as shown in Fig. 9. The growth of the precipitates follows nearly a parabolic law. This implies that the growth is diffusion-controlled rather than reaction-controlled. In a diffusion-controlled process, the growth is determined by the diffusion of oxygen from super-saturated areas to strain centers. Based on the diffusion-controlled growth, the size of the precipitates is calculated in the Appendix.

Transmission Electron Microscopy of Dislocation Loops

Dislocation loops punched out from the precipitates are observed in nearly every case. These loops lie in {110} planes with the loop axis in one of six possible <110> directions. This is seen in the stereo-micrographs of Figs. 10(a) and (b) for (001) surface orientation and in Fig. 10(c) for the (011) surface orientation. The loops located in the inclined {110} planes, labelled PE and PF in Fig. 10(a) and PD and PE of Fig. 10(c) are completely etched out.

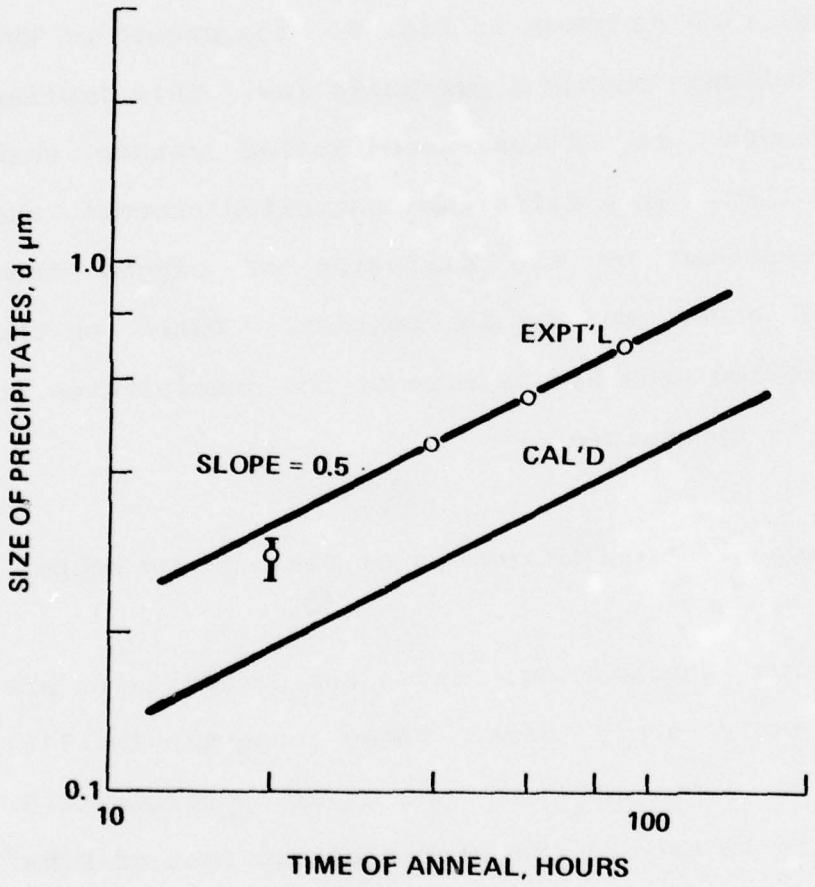
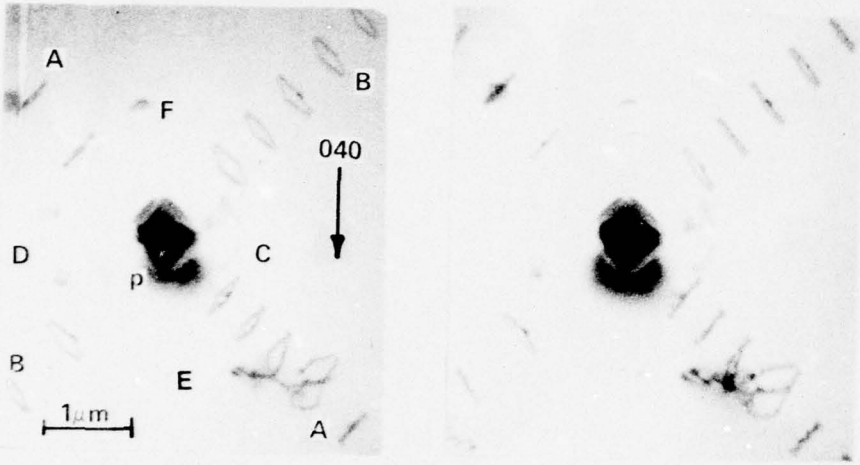
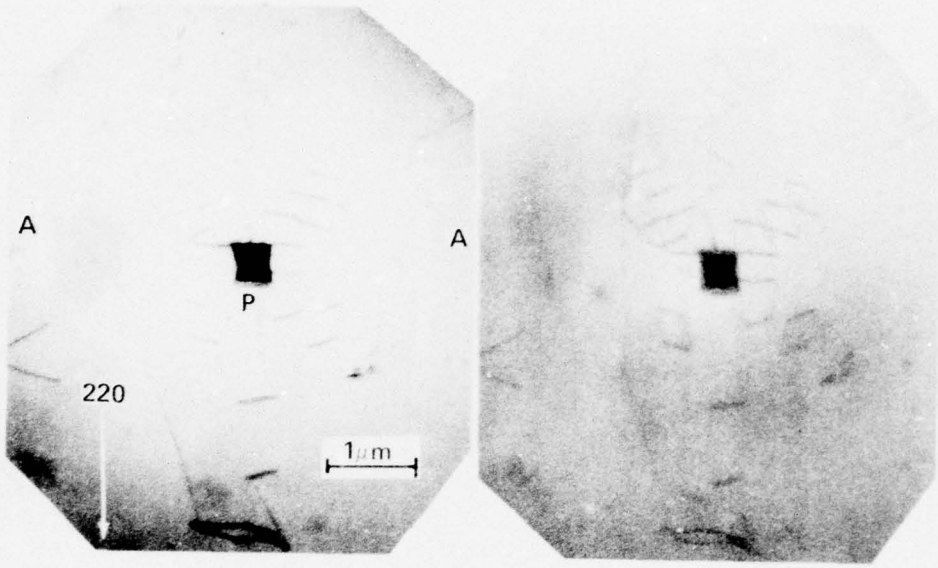


Fig. 9. The size of precipitates as a function of time of annealing at 1100°C



a

Fig. 10. Stereomicrographs showing dislocation loops punched out from a precipitate in <110> directions. (a) and (b) (001) surface orientation, (c) (011) surface orientation. Samples annealed at 1100°C for 90 hours in N_2.



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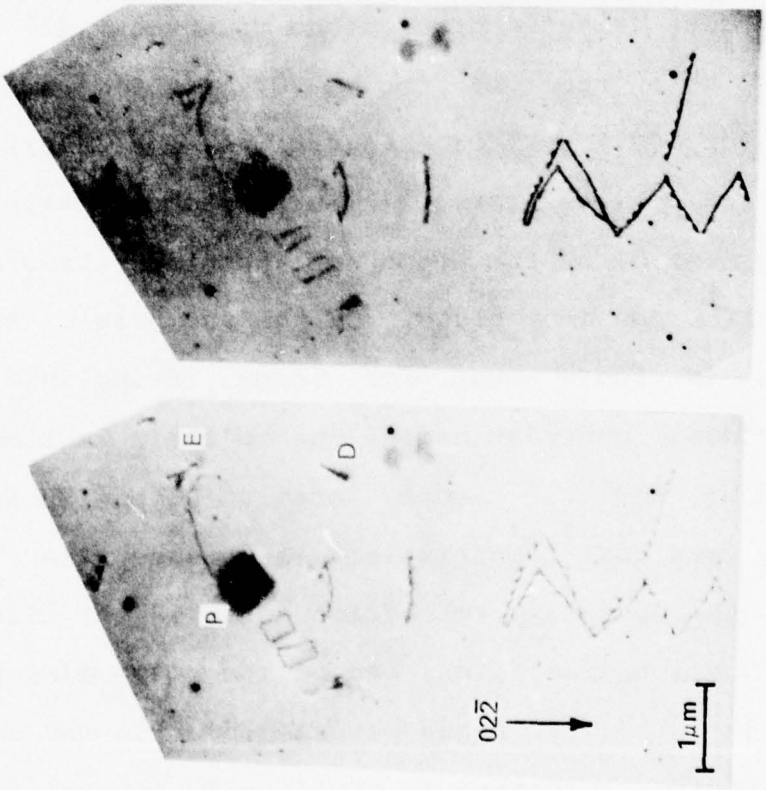


c

The loops located on the (101) plane in Fig. 10(c) are also etched out. The loops in the (011) plane of Fig. 10(c) can only be observed when a large tilting angle is used in the microscope.

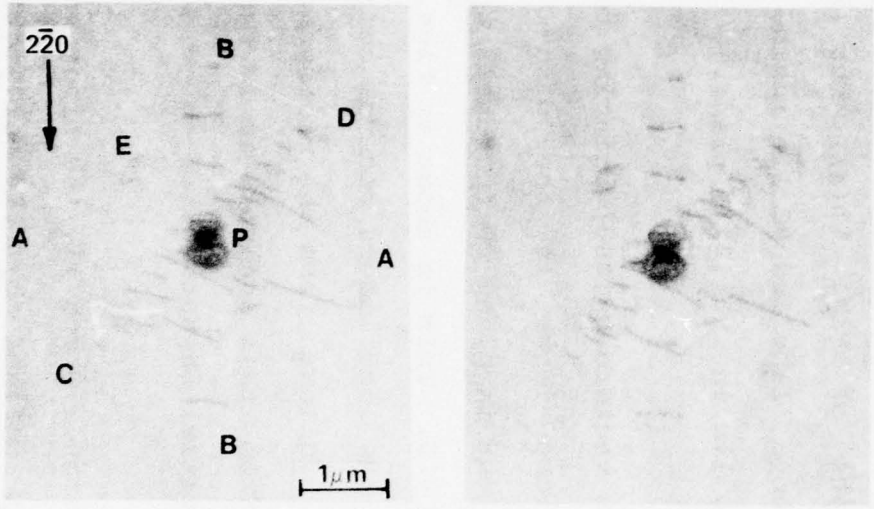
The Burgers vectors of the loops are determined by using the standard contrast criteria of electron microscopy (27). TEM micrographs were recorded for (220), (400) and (113) reflections for (001) surface orientations, and (220), (400) and (111) reflections for (011) surface orientation. The Burgers vectors, b, of the loops are thus identified as 1/2 <110> normal to the loop plane. In the analysis of Burgers vectors, it is found that for loops in inclined {110} planes, residual contrast arises due to their inclination. This is shown for the loops labelled PC and PD in Fig. 10(a). The residual contrast arises because $g.(b \times u) \neq 0$, where g is the operating reflection and u is the direction of the dislocation line, i.e., one of the <112> directions. For loops in a (110) plane perpendicular to the surface plane, the residual contrast is practically non-existent as shown for the loops labelled PA in Fig. 10(b) because $g.(b \times u) = 0$.

The nature of the loops, interstitial or vacancy, is determined from the image displacement observed in different

Transmission Electron Microscopy micrographs recorded with the same diffraction vector g but with the reversed excitation error(s), or from micrographs recorded with reversed g but with the same excitation error (27). The sense of inclination of the loop plane is determined from the stereo-micrographs of Fig. 11(a). For (001) surface orientation, the loops labelled PC lie in the (011) plane and those labelled PD lie in the $(0\bar{1}1)$ plane.

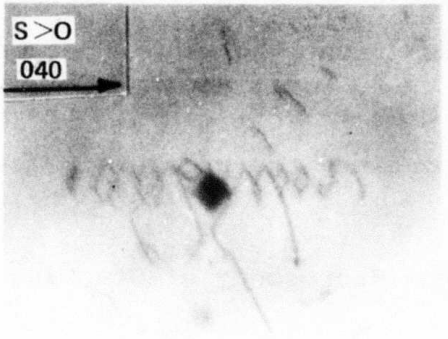
With the diffraction vectors g=[040] pointing to the right, the size of the loop image in the plane labelled PC decreases while the one in plane PD increases upon changing s from $s > 0$ to $s < 0$. This is shown in Figs. 11(b),(c). The size changes of the loop images reverse completely if g is reversed. This follows from the micrographs shown in Figs. 11(d),(e). From this analysis it is concluded that the loops are interstitial in nature.

As can be seen in Figs. 10 and 11, the sizes and shapes of the loops are well defined by the projection of the octahedral precipitates onto the {110} planes. The generation of these prismatic loops has been analyzed in great detail by Tan and Tice (7). They identified such loops as shear loops on {111} planes. The prismatic loops are generated by cross-slips of the generator loops. They



a

Fig. 11. (a) Stereomicrographs showing the loops in PC lies in the (011) plane and those in PD in the (0$\bar{1}$1) plane. (b) and (c) with g - 040 pointing to the right, the size of loop image in PC decreases and that in PD increases upon changing s from >0 (b) to <0 (c). (d) and (e). With opposite g = 0$\bar{4}$0, the size changes of loop image is reverse. Sample annealed at 1100°C for 40 hours in N_2.



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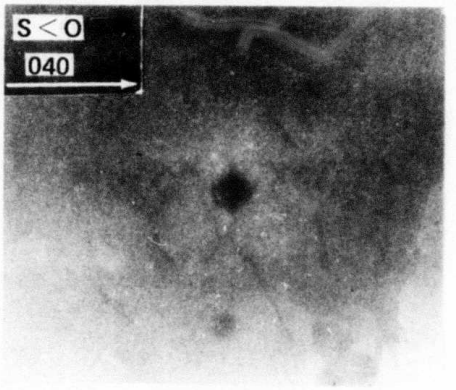

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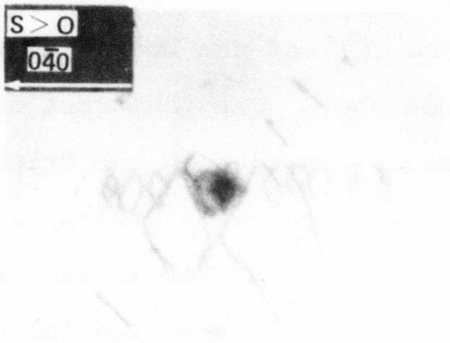
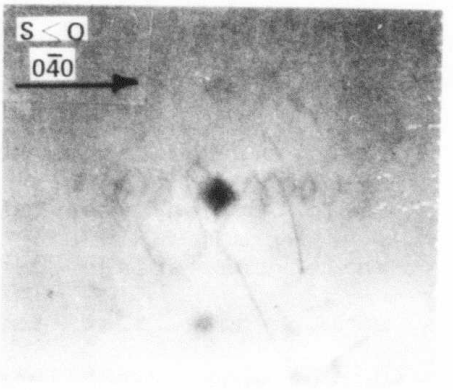


d



e

also explained that the generation of a helix as shown in Figs. 10(b),(c) results from the pinning of one end of a generator loop by a precipitate, thus leaving the other section of the loop to continue the cross-slip movements.

Transmission Electron Microscopy of Stacking Faults

As discussed before, annealing of the crystals also generates stacking faults in the bulk. The nature of these faults is determined from the analysis of Figs. 12(a)-(d). The sense of the inclination of these faults is established by knowing the top surface (T) and the bottom surface (B) of the foil in the microscope. The contrast of the outer fringe at the bottom surfaces changes in the bright and dark field images when taken with the same diffraction vector g while the fringe contrast at the top surface remains the same. Note that the contrast is reversed for opposite g. Using well established microscopy rules (28), the fault is identified as extrinsic in nature. Note, a precipitate at one end of the fault in Fig. 12. The interaction between fault and precipitate usually causes the fault to deviate from the normal growth, which is the circular shape.

3.2.3 Analysis of Swirl Defects in Dislocated Crystals

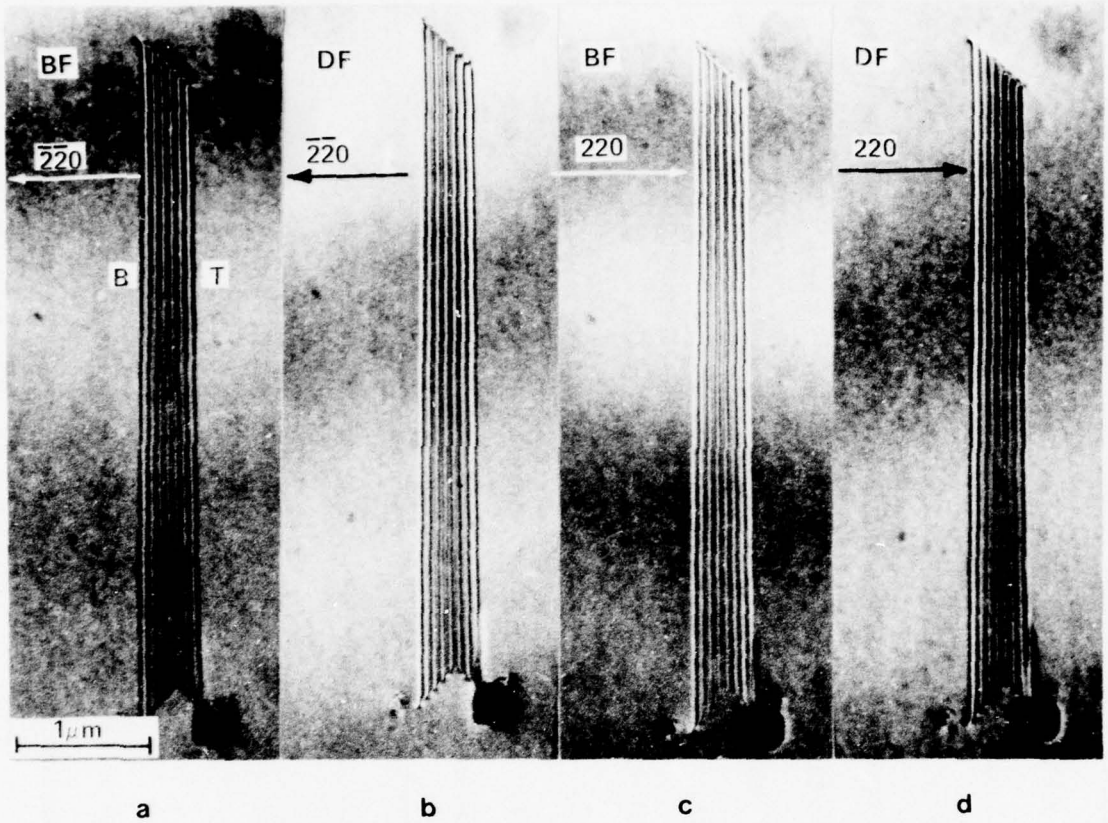


Fig. 12. Determination of fault nature, (a). BF, g = $\bar{2}\bar{2}0$, (b). DF, g = $\bar{2}\bar{2}0$, (c). BF, g = 220, (d). DF, g = 220 Sample annealed at 1100°C for 40 hours in N_2.

Chemical Etching

As in dislocation-free crystals, annealing of crystals containing dislocations also causes significant reduction of dissolved oxygen. The oxygen data before and after annealing are summarized in Table I. A representative x-ray topograph showing swirl formation after annealing is given in Fig. 13(a). The corresponding etch figures obtained after Sirtl etching are shown in Fig. 13(b). The circle and line defects are stacking faults which lie in all possible {111} planes. It is interesting to note that a significantly higher density of stacking faults is always observed in dry-oxygen annealed crystals compared to nitrogen annealed crystals. This observation is true for both dislocation-free and dislocated crystals. The size of the precipitates in dislocation-free crystals is nearly independent of annealing ambients, but is mainly controlled by the annealing temperature and time.

The defects revealed by etching are characterized in detail by transmission electron microscopy investigations in the following.

Transmission Electron Microscopy of Precipitates

Precipitates obtained after dry oxidation for 20 hours are

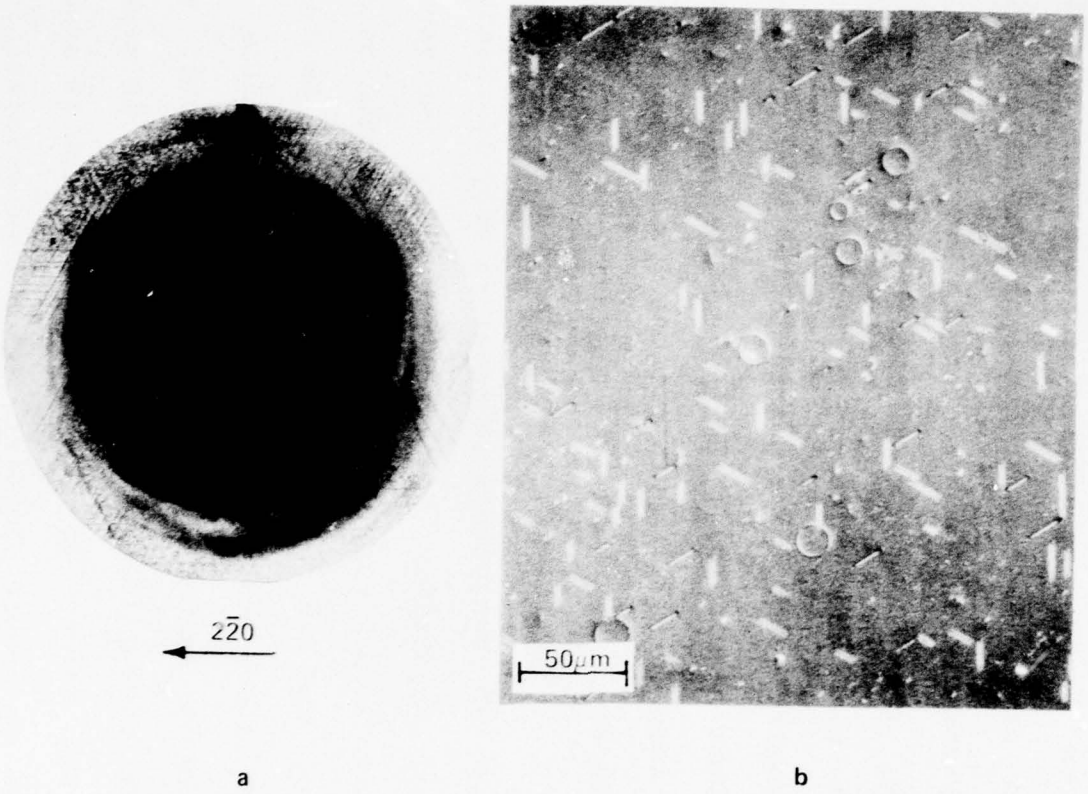


Fig. 13. (a). X-ray topograph showing swirl formation in <111> dislocated crystal after 20 hours of annealing at 1100°C in dry O_2. (b) Sirtl etched surface of (a).

similar to those observed in dislocation-free crystals and are shown in Figs. 14 and 15. At this stage the precipitates are very small, ~ 0.25 to 0.3 μm in size, and dislocation loops are still attached to them. Analysis of the loop nature indicates that loop A in Fig. 14 lies in a $(\bar{1}11)$ plane and has a Burgers vector b=1/2 [101]. Therefore, this loop is a shear loop. This is in good agreement with the results reported by Tan and Tice (7). They reported that loops generation by precipitates is due to a shear mechanism. As shown before, the shape of the precipitates in (111) projections is hexagonal. This is evident in Fig. 15.

This type of precipitate is found in very low densities in dislocated crystals. In such crystals, another kind of precipitate is dominant. The dominant precipitates align in rod shape and are shown in Figs. 16 and 17. In Fig. 16, a helix is seen to wind around the precipitate rod and eventually a dislocation loop (A) is punched out. The loop lying in the (110) plane with b=1/2 [110] is a prismatic loop. The nature of the punched out loops is essentially the same as found in dislocation-free crystals. Various examples of rather complex forms, such as dislocation helices, loops, entangles, and even stacking faults, are given in Fig. 17. The fact that discrete precipitates align

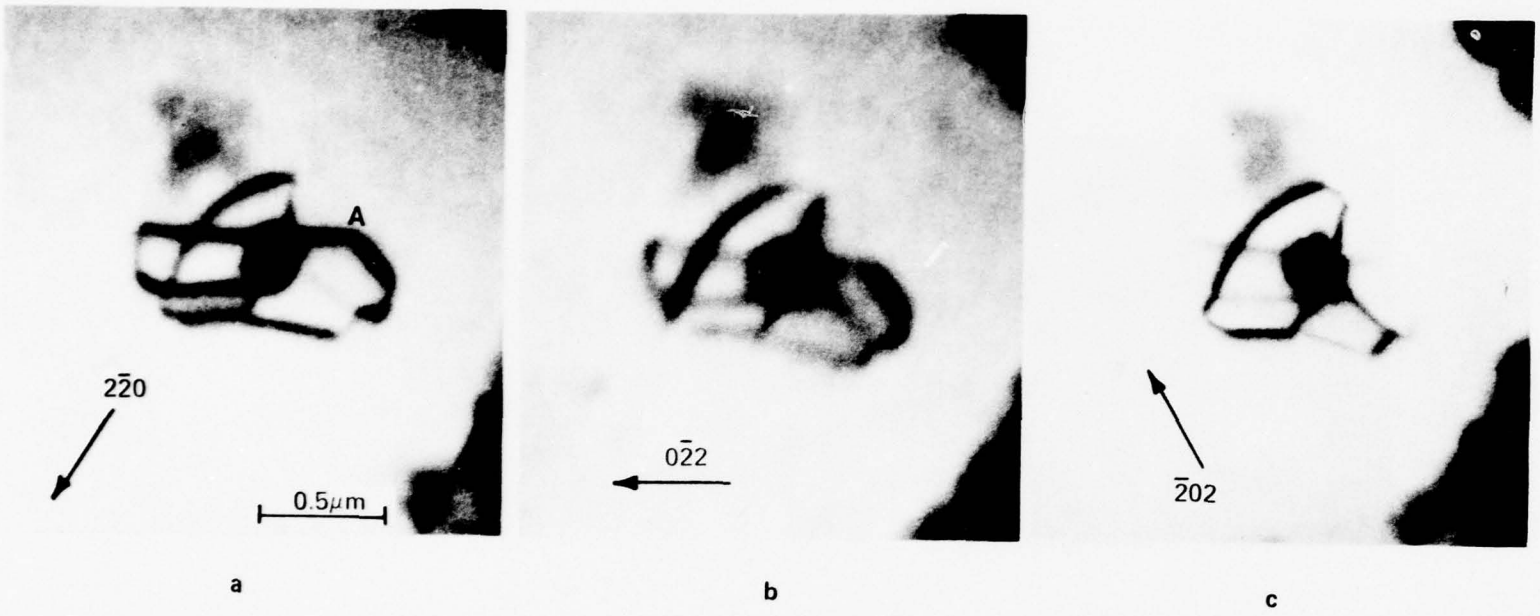


Fig. 14. Electron micrographs showing a precipitate with dislocation loops. (a) $g = \bar{2}02$, (b) $g = 0\bar{2}\bar{2}$ and (c) $20\bar{2}$. Sample annealed at 1100 C for 20 hours in dry O_2.

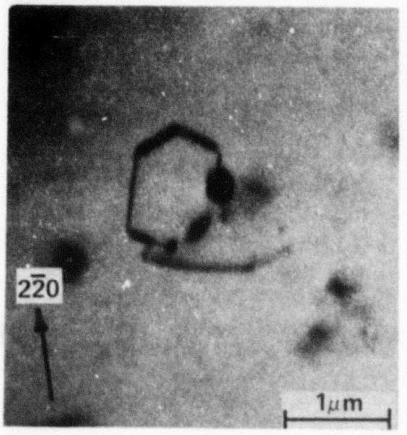


Fig. 15. Electron micrographs showing the shape of precipitate is hexagonal on (111) projection.

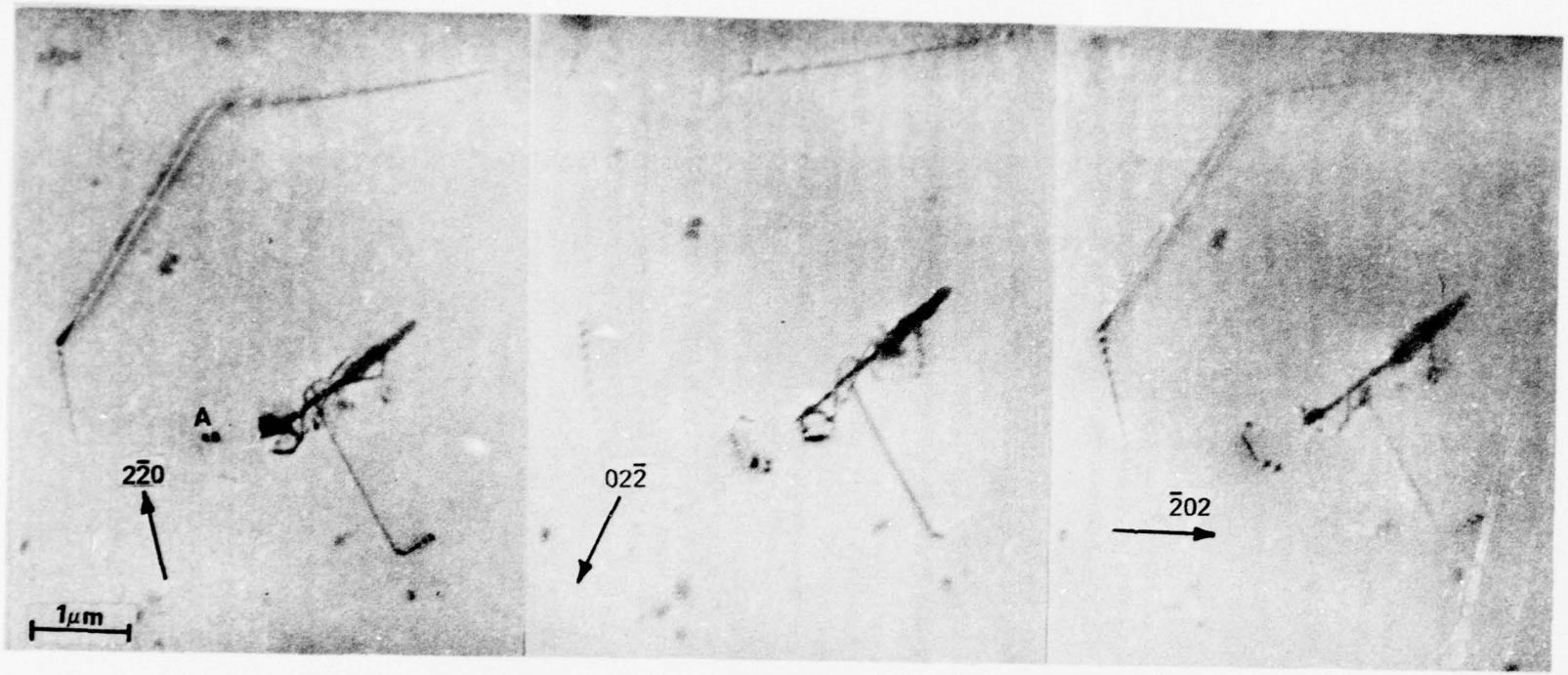


Fig. 16. Electron micrographs showing that the precipitates in dislocated crystal align in rod shape with a helix winding them. (a) $g = 2\bar{2}0$, (b) $g = 02\bar{2}$, and (c) $g = \bar{2}02$

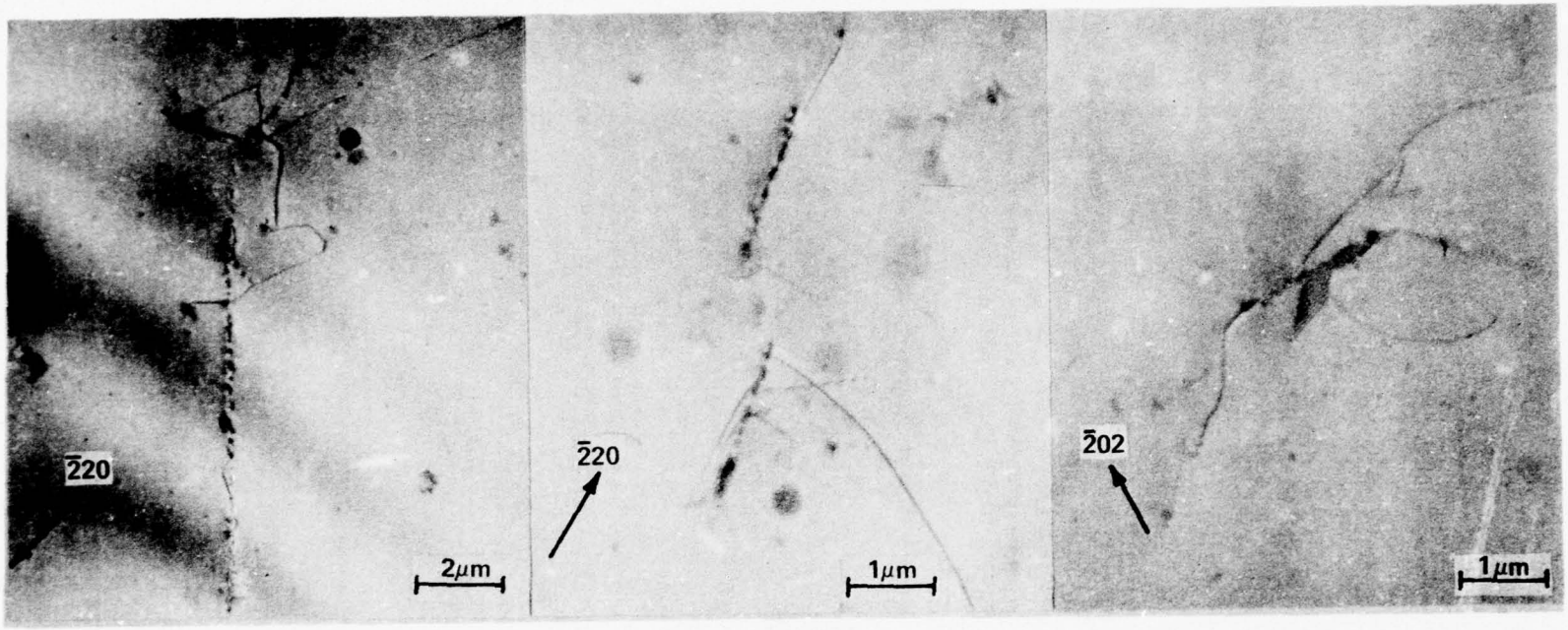


Fig. 17. Electron micrographs showing various examples of dislocation helices, loops, entangles and even stacking faults in the vicinity of precipitate rod. (a) and (b) sample annealed at 1100°C in dry O_2 for 20 hours and (c) for 40 hours.

in rod shape suggests that precipitation occurs predominantly along existing dislocation lines. In this case, dislocation lines serve as strain centers and attract the oxygen precipitant. This explains also that the occurrence of precipitates similar to those observed in dislocation-free crystals is much less in dislocated crystals. Preferential precipitation of oxygen at dislocations induced by sawing has been previously reported (29).

Transmission Electron Microscopy of Stacking Faults and Dislocation Loops

As revealed by Sirtl etching, a high density of stacking faults is generated in the crystals if annealed in a dry oxygen ambient. The nature of these faults is determined from the micrographs given in Fig. 18. Using the same rules as discussed before, the faults, labelled F1 and F2, in Fig. 18 are extrinsic in nature. Another fault, at F3, is out of contrast for this reflection.

Electron micrographs of circular faults are given in Fig. 19 The faults, F1, F2 and F3, lie in (111), $(1\bar{1}1)$ and $(11\bar{1})$ planes, respectively. In Fig. 19(a) it can be seen that the contrast of the partial dislocation bounding F1 increases as

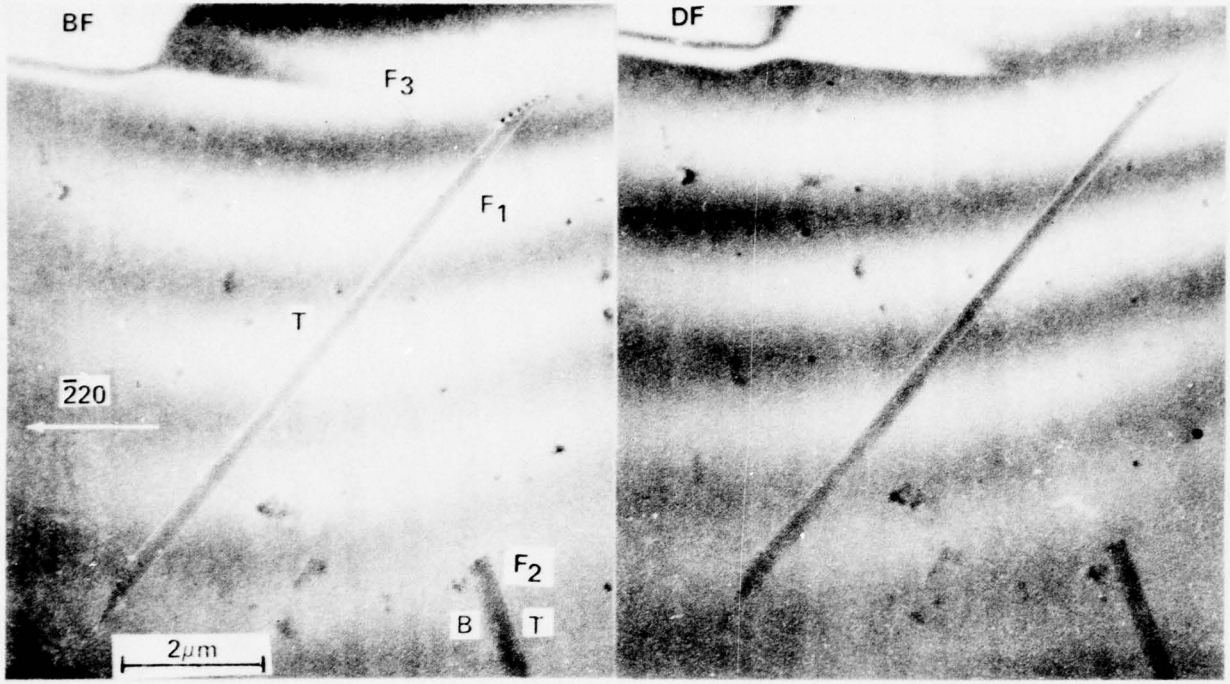


Fig. 18. Determination of fault nature, (a) BF, g = $\bar{2}20$ and (b) DF, g = 220. Fault F3 is out of contrast.

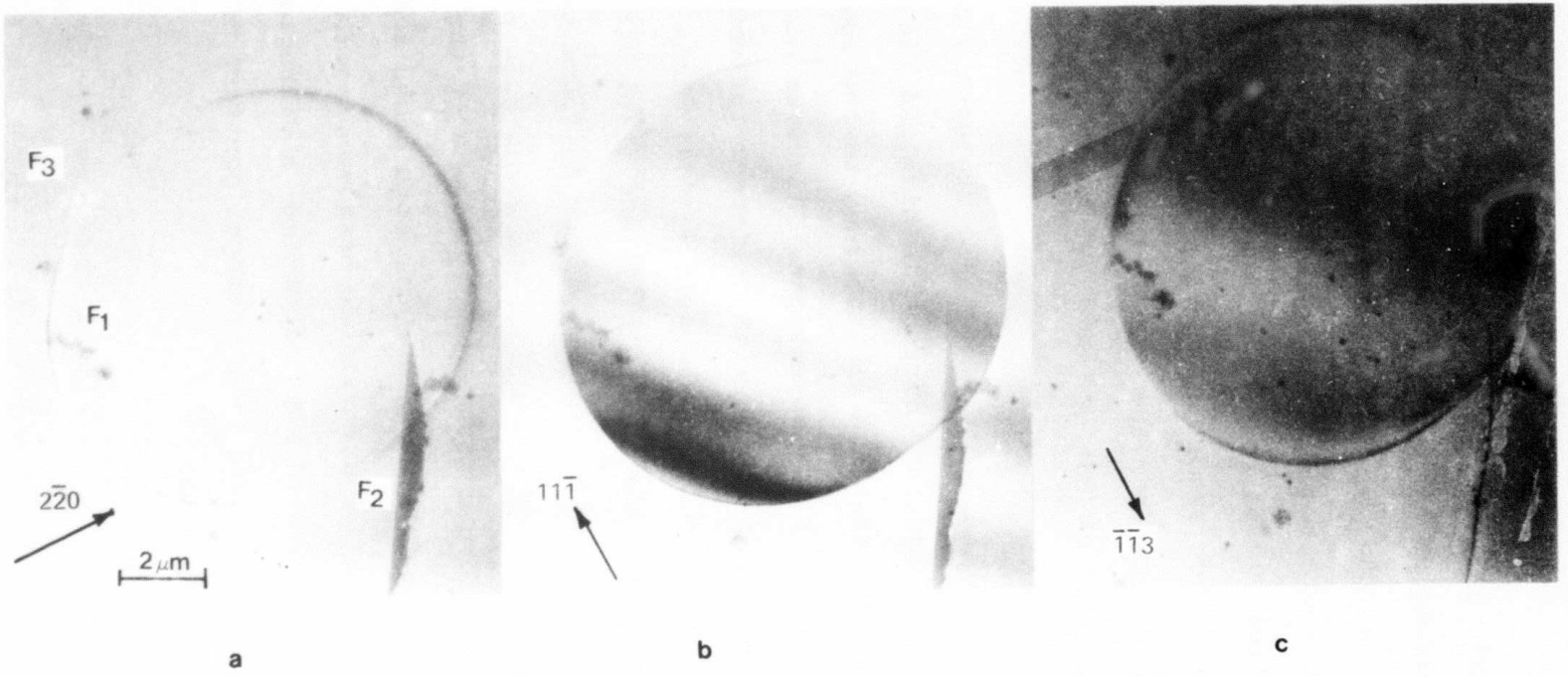


Fig. 19. Electron micrographs showing that stacking faults lie in different {111} planes. (a) g = 2$\bar{2}$0, (b) g = 11$\bar{1}$, and (c) g = $\bar{1}\bar{1}$3.

the value of g.(b x u) increases. The contrast of the partial dislocation has nearly disappeared in a direction parallel to g and is most intense perpendicular to g. On tilting, the characteristic fringes of a stacking fault can be seen in Figs. 19(b),(c). The fault vector is identified as b=1/3 <111>. For example: the fault vector of F2 is 1/3 [1$\bar{1}$1]. This follows from the micrograph given in Fig. 19(c) for which the fault is out of contrast (g=($\bar{1}\bar{1}$3)).

Hexagonal dislocation loops are also frequently observed. These loops are several microns in size and lie in {111} planes with b=1/2 <110> and are inclined to the loop plane. Their edges are in <110> directions. Electron micrographs of a hexagonal loop taken with different reflections are given in Fig. 20. The loop lies in a ($\bar{1}$11) plane with its edges A, B and C in the [101], [0$\bar{1}$1] and [$\bar{1}\bar{1}$0] directions, respectively. The contrast of the loop is found to depend strongly on the value of g.b and on the value g.(b x u). In the micrograph recorded with g=[02$\bar{2}$], edge B of the loop is invisible (Fig. 20(b)) because of both g.b=0 and b.(b x u)=0. Edges A and C are visible because of g.(b x u)$\neq$0. This is further checked by recording a micrograph with g=[11$\bar{1}$]. In Fig. 20(c), the residual contrast of edge B arises due to g.(b x u)$\neq$0.

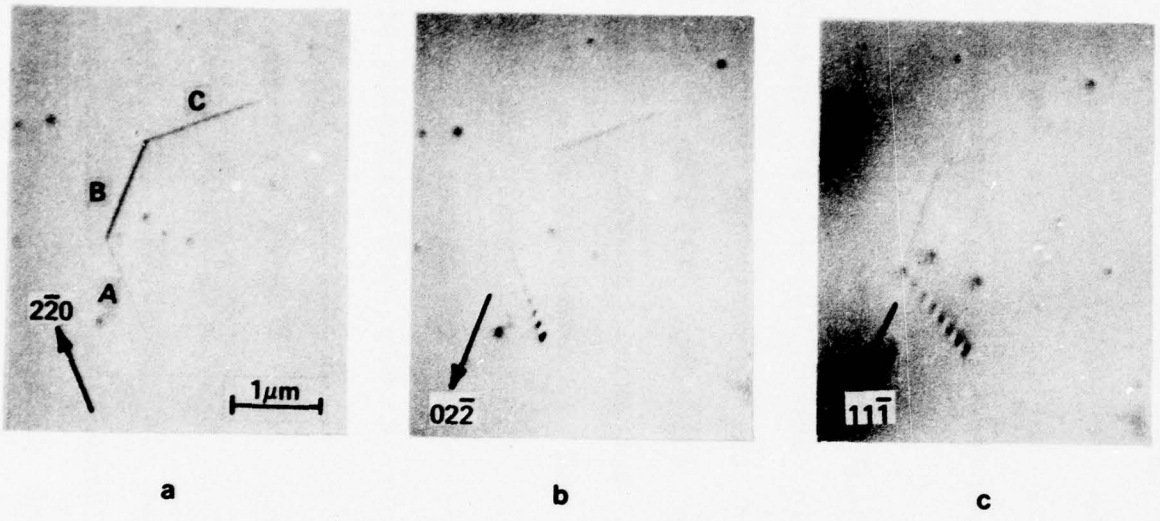


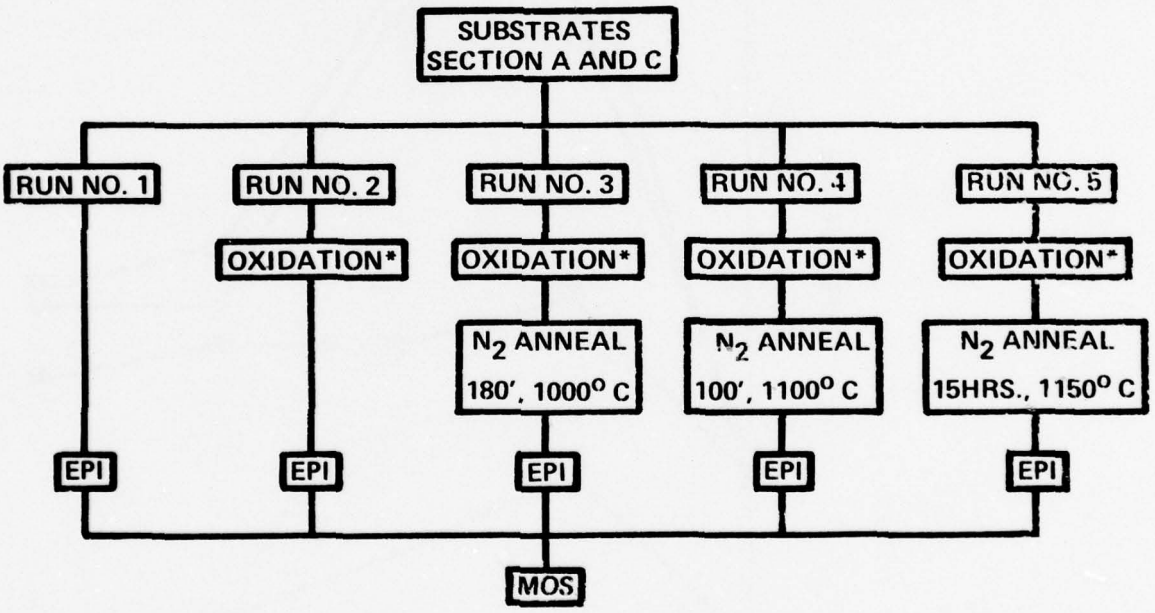
Fig. 20. Electron micrographs of a hexagonal loop. (a) g = $\bar{2}$20, (b) g = 0$\bar{2}$2, and (c) g = 11$\bar{1}$.

3.3 Electrical Measurements in Epitaxial Layers

The presence of large amounts of oxygen in substrates and its influence on the generation lifetime of n-type epitaxial layers deposited on such substrates was also investigated. The experimental matrix used is outlined in Table II. Accordingly, experiments in run 1 use substrates sliced from section A and C. These wafers received no heat treatment prior to epitaxial deposition. The oxygen concentration in these wafers is about 10×10^{17} atoms/cm^3 and 5×10^{17} atoms/cm^3. For the experiments conducted in run 2, an oxidation step [15'-dry, 135'-wet, 15'-dry] at 925°C] preceeding the epitaxial growth is introduced. In run numbers 3, 4 and 5 experiments a nitrogen anneal is introduced after the oxidation. The N_2 anneal is done at different temperatures for different lengths of time. All the oxides grown during the annealing cycles are removed prior to epitaxial deposition. After deposition, MOS capacitors using 1400 Å thick dry oxide, grown at 1000°C, are made on the n-type epitaxial layers and the minority carrier lifetime is measured. In Fig. 21 the average lifetime is plotted as a function of run number. The average lifetime is obtained from at least four wafers out of the same group. The lifetime variation between wafers in the same group are found to vary by a factor of 5 while

variations between the different groups are different by orders of magnitude. Therefore, the statistical significance of the data in Fig. 21 is assured. Figure 21 shows that the lifetime of epitaxial layers grown on section

TABLE II. Experimental matrix for the study of oxygen in substrates and its influence on the generation lifetime of epitaxial layers



*OXIDATION: DRY (15') – WET (135') – DRY (15') AT 925° C

HEAT-TREATMENTS PRIOR TO EPITAXIAL DEPOSITION

RUN NO. 1: NO TREATMENT
RUN NO. 2: 15′ (DRY) – 135′ (WET) – 15′ (DRY)
OXIDATION AT 925° C
RUN NO. 3: STEP NO. 1 PLUS 180′ N_2 ANNEAL AT 1000° C
RUN NO. 4: STEP NO. 1 PLUS 100′ N_2 ANNEAL AT 1100° C
RUN NO. 5: STEP NO. 1 PLUS 15 HOURS N_2 ANNEAL AT 1150° C

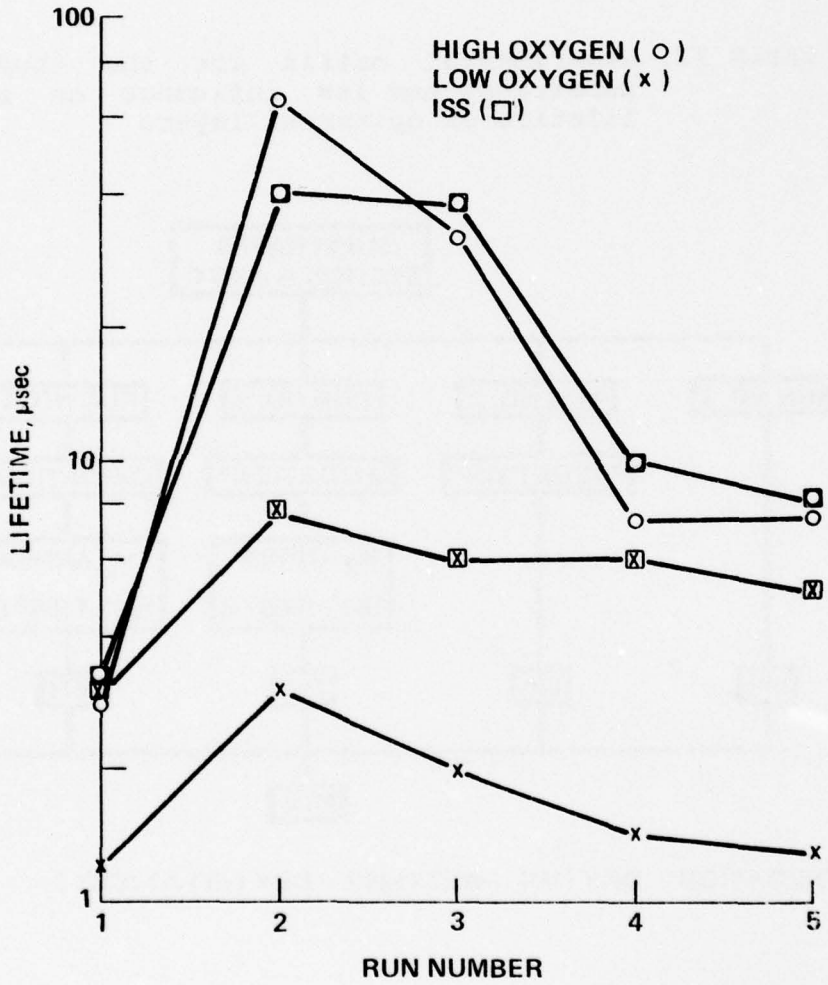


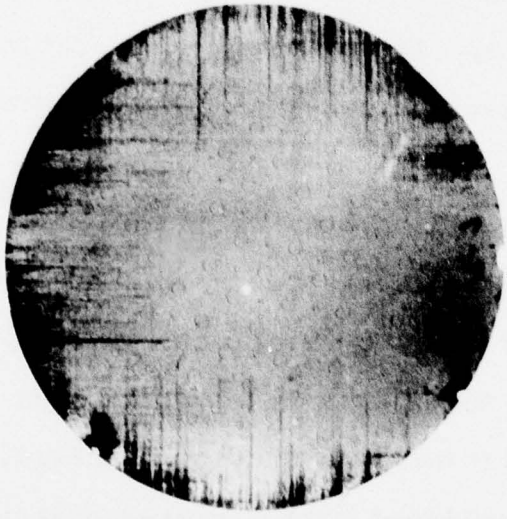
Fig. 21. The influence of various heat-treatments on the lifetime of epitaxial layers

A wafers is consistently higher than the one on section C wafers. This is true for all runs. The data indicates also that the lifetime of section A wafers is strongly influenced by the various heat-treatments. It is interesting to note that the lifetime of section C wafers is relatively insensitive to heat-treatments.

Investigations done by x-ray topography indicate that in run 1 no resolvable swirl defects are present either in section A or in section C wafers, Figs. 22(a),(b). Slip generation during the epitaxial process is revealed in these topographs. The slip results mainly from edge damage in the wafer periphery. Quite often a higher density and greater penetration of slip is observed in section C wafers indicating that oxygen can cause silicon resistant to slip.

In run 2, an oxidation step is added prior to epitaxial deposition. The result of such a heat-treatment is swirl formation during epitaxial deposition. This is true for all section A wafers. An example is given in Fig. 23(a). Note that no swirl defect forms in section C wafers, Fig. 23(b). Generally it is believed that repeated heat-treatments of silicon wafers result in degradation of minority carrier lifetime through generation of crystal defects. Therefore it is surprising to find that the epitaxial layers grown in

a



b

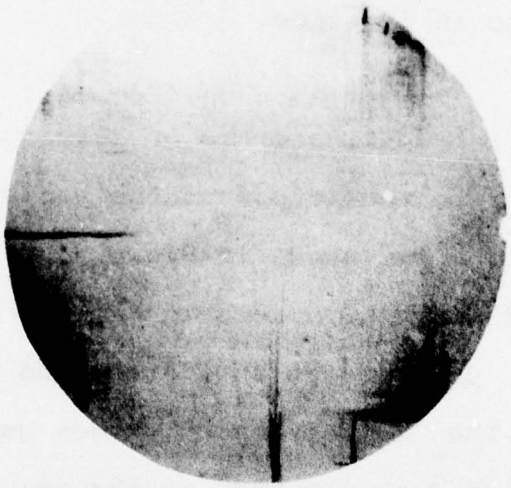
Fig. 22. X-ray topographs showing in run 1 no resolvable swirl defects present in (a) a section A wafer and (b) a section C wafer

run 2 show significantly longer lifetimes as compared to those grown in run 1. The only difference between the two groups of wafers is that swirl formation occurs in wafers of run 2 but not in run 1 wafers. This can be seen in the x-ray topographs shown in Fig. 23.

In another experiment swirl defects are also induced prior to epitaxy by an additional N_2 anneal. This is done in runs 3, 4 and 5. As seen in Fig. 21, this additional annealing results in a degradation of lifetime as compared to run 2. However, the lifetime measured in wafers processed in runs 3, 4, 5 is still higher than the one for run 1. The difference in heat-treatment time between run 3, 4 and 5 cause a difference in lifetime.

The influence of heat-treatments on lifetime as summarized in Fig. 21 can be understood on the basis of "intrinsic" oxygen gettering. As shown in Fig. 22(a), no appreciable precipitation of oxygen occurs in run 1. However, oxygen atoms begin to cluster at this stage and form nuclei for precipitation. The efficiency of oxygen gettering at this stage is not as good as compared to the one observed in run 2 and 3. In these runs, massive precipitation occurs during epitaxial deposition and generates a high density of oxide precipitates and crystal defects in the bulk wafer Fig.

a



b

Fig. 23. X-ray topographs showing in run 2 swirl defects present in (a) a section A wafer, but not in (b) a section C wafer

23(a). The formation of precipitates and defects is the driving force for the gettering of impurities. The large decrease in lifetime observed in run 4 and 5 results partially from surface degradation, which occurs during annealing prior to epitaxial deposition, and also partially from a smaller amount of precipitation, and thus less gettering action during subsequent expitaxy.

The experiments indicate that "gettering" through swirl defect formation is most effective when swirls form during epitaxial deposition and not prior to epitaxy.

Figure 21 suggests that the relatively low lifetime found in section C wafers is a result of the absence of defects and thus of gettering sites. If this is true, one would expect to see lifetime improvement by producing effective external gettering sites on the backside of such wafers. Impact Sound Stressing (ISS) has been shown to be an effective gettering technique and has successfully improved lifetime in both silicon substrates as well as in epitaxial layers (30). For this investigation, we applied ISS to section A and C wafers before any heat-treatment. The result of the ISS treatment of the wafers is also shown in Fig. 21. For section A wafers, the lifetime remains almost the same,

independent of the ISS treatment. For section C wafers, however, significant improvement of lifetime is observed for every single run.

The results of the investigation are summarized in Fig. 21.

The findings formulated in the following can provide guidance for successful application of external gettering techniques for Czochralski silicon wafers:

Swirl defects are effective internal gettering sites. If they are present in nascent state in silicon wafers, external gettering techniques cannot improve minority carrier lifetime in silicon substrates at epitaxial layers.

The relatively low lifetime obtained in low oxygen concentration wafers is due to the absence of internal gettering sites. The lifetime of such wafers can be improved significantly by means of external gettering techniques such as ISS.

Figure 21 shows that the lifetime in C wafers has been improved through ISS to values almost equal to the ones obtained for section A wafers.

3.4 Defect Studies in Epitaxial Layers

To assess the defect state in the epitaxial layer surface the MOS capacitors are removed and the surface is Sirtl etched. After etching defects present in the surface are optically visible. Thus, it is possible to count the defects in areas previously occupied by MOS capacitors; therefore, a direct correlation between defect density and measured lifetime is possible.

Main defects in the epitaxial silicon are (a) grown-in stacking faults, (b) oxidation-induced stacking faults, and (c) mounds. Examples of such defects are shown in the photomicrographs of Figs. 24, 25 and 26, respectively. After etching, the grown-in faults display the well-known "square" figure which results from the intersection of the four faulted <111> planes with the (001) surface. Their density in the epitaxial film is quite low ($10/cm^2$). The oxidation-induced stacking faults in the epitaxial films are very similar to the faults observed in oxidized substrate surfaces. They are also of the Frank type (extrinsic). The mounds observed in the epitaxial films are partially developed stacking faults. The reason for their small size has not been investigated in the context of this work and is presently not understood. However, it was noted that an HF

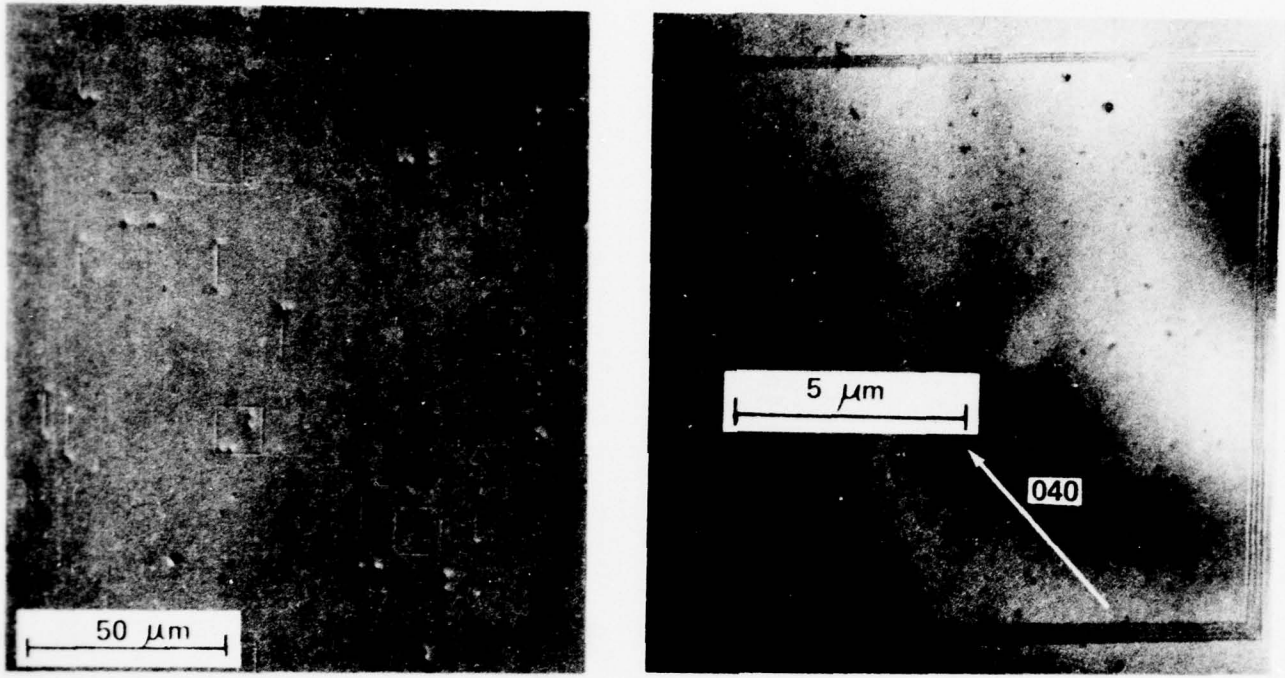
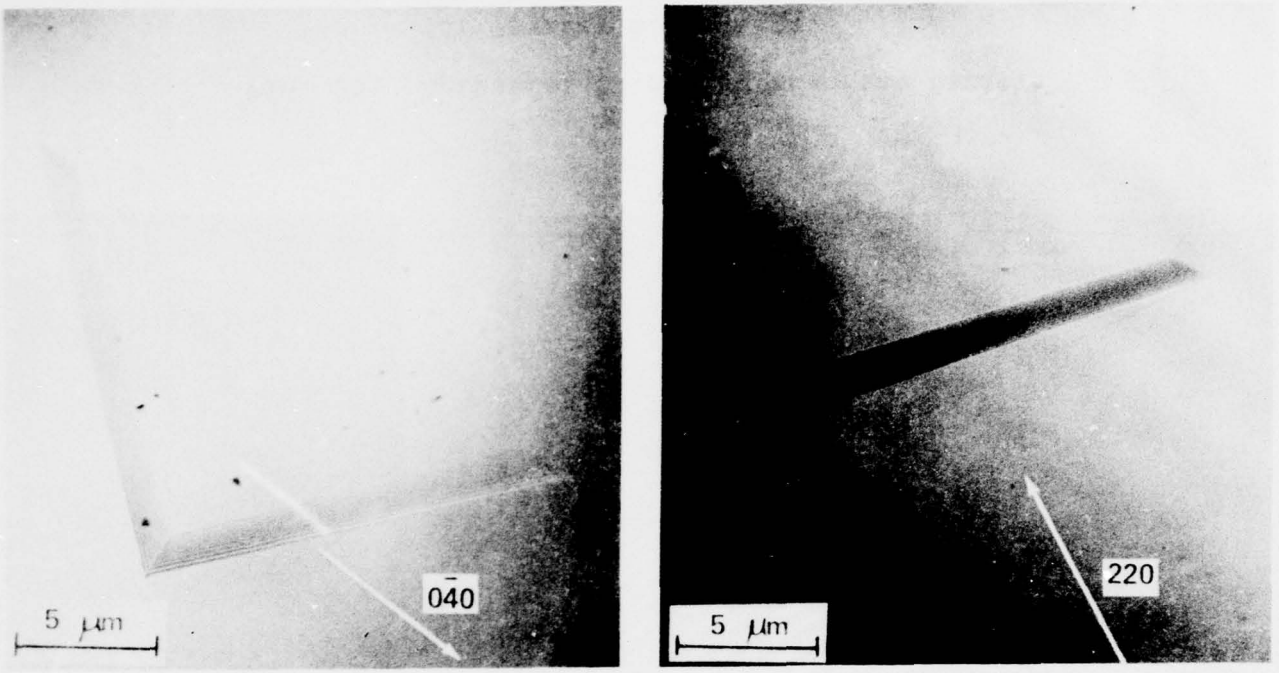


Fig. 24. Epitaxial stacking faults.

(a) Optical micrograph.
(b) TEM of single square-type fault.



c d

Fig. 24. Epitaxial stacking faults.

(c) TEM of L-shaped type.
(d) TEM of linear type.

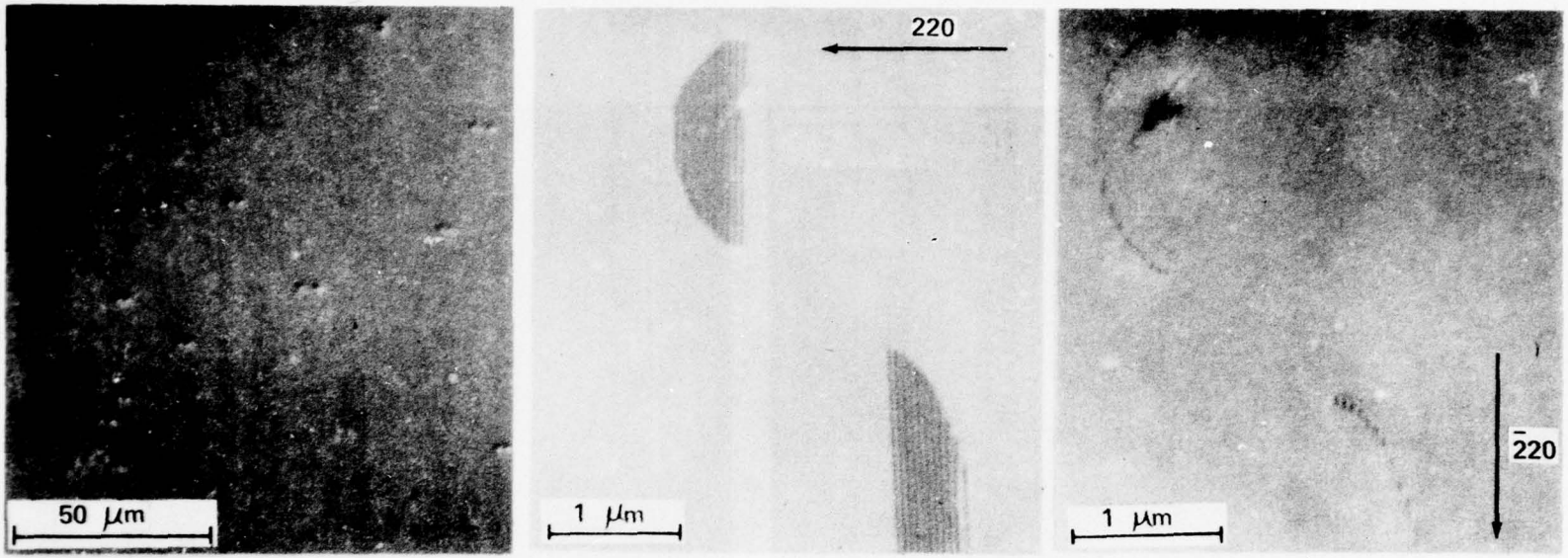


Fig. 25. Epitaxial oxidation stacking fault.

(a) Optical micrograph.
(b) TEM g = $2\bar{2}0$.
(c) TEM g = $\bar{2}20$.

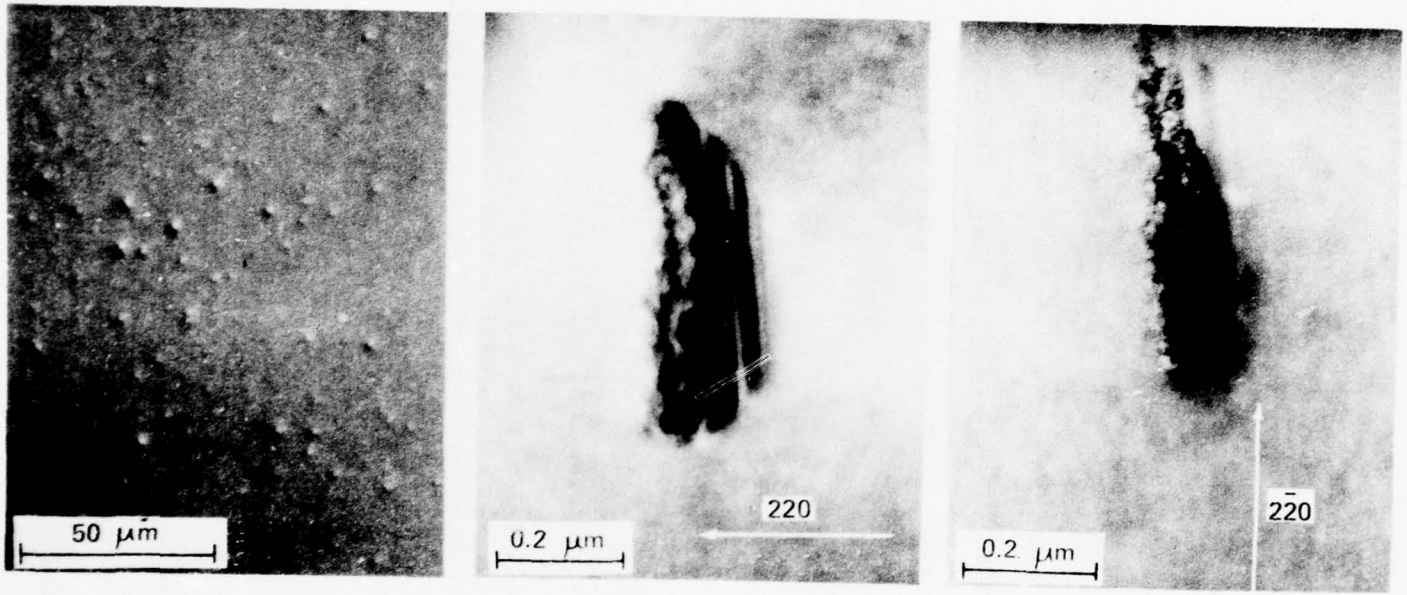


Fig. 26. Epitaxial mound defect.

(a) Optical micrograph.
(b) TEM g = 220.
(c) TEM g = 2$\bar{2}$0.

treatment of the epitaxial surface before oxidation caused the mounts to develop into standard oxidation type stacking faults.

The defect density found in epitaxial silicon covers quite a large range. This made it possible to obtain a fairly accurate lifetime vs. defect correlation. The lifetime data are correlated with the defect density found under every single MOS dot. The lifetime vs. defect dependency thus obtained for the samples is given in Fig. 27. In making this correlation it was observed that practically all MOS dots, free of defects after Sirtl etching, had a lifetime between 10 to 100 μsec. A rapid decrease in lifetime was noted with the number of defects present under each MOS dot. Another general finding is that oxidation-induced stacking faults are more detrimental to lifetime than mounds. It was also noted that backside ISS'ed wafers exhibited a considerably lower defect density and a larger lifetime than non-stressed wafers sliced from Section C.

Using the method of linear regression, a best fit of the data summarized in Fig. 27 is obtained. The curves are plotted in Fig. 27. Accordingly, one obtains the following correlation between lifetime and defect density. For oxidation-induced stacking faults:

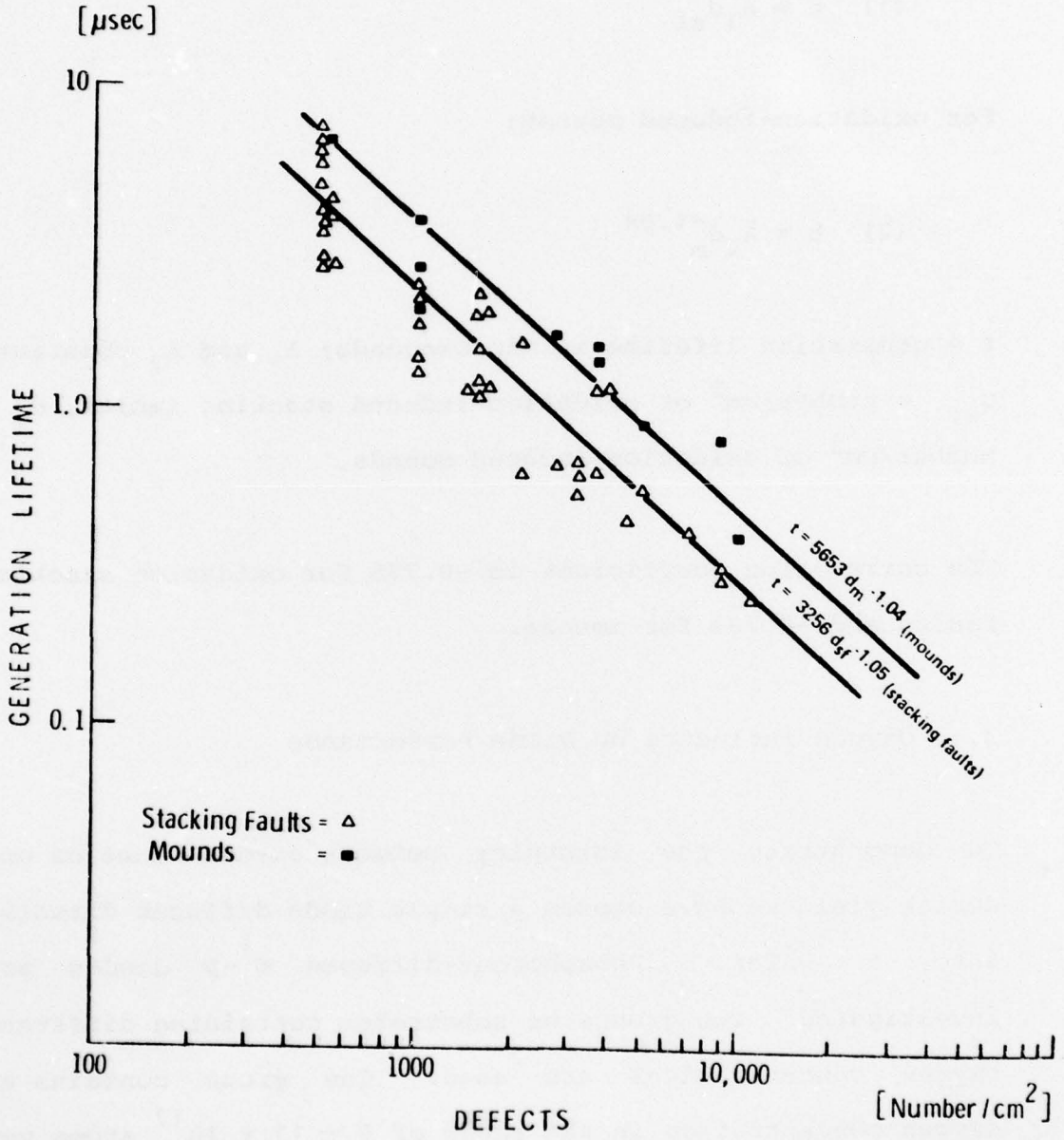


Fig. 27. Lifetime vs. defect dependency.

$$(1) \quad t = A_1 d_{sf}^{-1.05}$$

For oxidation-induced mounds:

$$(2) \quad t = A_2 d_m^{-1.04}$$

t = generation lifetime in microseconds; A_1 and A_2 constants d_{sf} = number/cm^2 of oxidation-induced stacking faults, d_m = number/cm^2 of oxidation-induced mounds.

The correlation coefficient is -0.775 for oxidation stacking faults and -0.707 for mounds.

3.5 Oxygen Influence on Diode Performance

To demonstrate the interplay between oxygen kinetics and device yield we have chosen a simple diode diffused directly into a wafer. Phosphorous-diffused N^+-p diodes are investigated. Two groups of substrates containing different oxygen concentrations are used. One group contains an oxygen concentration in the range of 9 ~ 11 x 10^{17} atoms per cm^3, and the other one a concentration in the range of 4.7 ~ 5.3 x 10^{17} atoms per cm^3. Each group had four wafers with 148 diodes. The reverse I-V characteristics of the diodes

were studied by probing the diffused diodes on the wafer. The diodes were classified as either reasonably good or soft using the following requirements for a hard diode:

a) Low current: the voltage at 20 μa reverse current must be within 10% of the voltage at 200 μa.

b) High current: the voltage at 200 μa must be within 10% of true avalanche breakdown.

In this way the wafers were mapped and the number of hard diodes was determined in percent of the total number of diodes per wafer.

The results are shown in Table III. The sample numbers refer to the position of the wafer relative to the seed end. Table III indicates that substrates of higher oxygen concentration give significantly higher diode yields than those of lower oxygen concentration. This is in good agreement with our lifetime measurements reported previously (31) and again illustrates the importance of understanding the role of oxygen in silicon during device processing.

TABLE III. The Influence of Oxygen on the Yield of N^+-p diodes

Crystal Section	Oxygen Conc. atom/c.c.	Sample No.	Yield, %	Avg. Yield, %
A	$9 \sim 11 \times 10^{17}$	23 26 49 67	97.3 93.5 93.2 78.2	90.6
C	$4.7 \sim 5.3 \times 10^{17}$	275 284 286 288	73.0 75.0 59.5 66.9	68.6

4.0 DISCUSSION

For a discussion of our experimental results it is important to realize that there is a difference between annealing silicon in bulk form or in wafer shape. In a bulk crystal precipitation of oxygen occurs homogeneously throughout the crystal volume. If the bulk crystal is shaped into wafers after annealing each wafer will have a relative uniform distribution of precipitates and dislocations throughout its volume. Consequently, the wafer surface will contain defects. Thus the active device area (depletion width of MOS device) contains precipitates which will degrade

minority carrier lifetime as shown in Fig. 1.

This situation does not prevail during actual silicon device manufacturing. Silicon bulk crystals are sliced into wafers before any major high temperature annealing occurs. Note that the 700°C annealing of silicon crystals, as practiced in the industry to dissolve oxygen donors complexes (to stabilize resistivity), actually corresponds to a lifetime maximum (20).

Silicon wafer processing steps, such as diffusion and/or epitaxy, can lower the oxygen content in the wafer surface through out-diffusion of oxygen. This means that certain processing steps lower the supersaturation of oxygen in the silicon surface. As a result oxygen precipitation occurs only in the center of the wafer leaving the wafer surface (active device area) free of precipitates. Under such conditions the sequential event: SiO_x precipitates --> generation of dislocation --> gettering of impurities is activated. It is not surprising to see that oxygen-rich wafers can provide better device yield as shown in our experiment for diodes and can also improve the lifetime in epitaxial films if used for substrates. This intrinsic gettering effect of oxygen has been used successfully to

improve leakage limited yield during bi-polar device processing (19). The improvements reported by these workers are in good agreement with our lifetime measurements.

5.0 SUMMARY

Variations of minority carrier lifetime observed in silicon wafers cut from bulk annealed crystals and observed in wafers prepared from crystals not pre-annealed but annealed as "standard" wafers are reported.

The investigations are done on silicon containing high (~ 10^{18} atoms/cm^3) and low amounts (~ 5 x 10^{17} atoms/cm^3) of oxygen. The investigations include zero dislocations and approximately 10^4 dislocations/cm^2 wafers and cover the temperature range from 900°C to 1250°C.

Bulk annealed crystals subsequently sliced into wafers show lifetime degradation with annealing time. The lifetime decrease is less severe in dislocated crystals with an original lifetime of 10 μsec as compared to dislocation-free crystals with an original lifetime of 100 μsec. The lifetime values in both types of crystals converge after 40 hours of annealing to approximately 1 μsec.

The lifetime degradation is correlated with the actual defect state produced in the active device area through annealing. Silicon oxide precipitates and punched out dislocation loops are identified as electrically active defects responsible for the observed lifetime degradation.

Evidence is presented that under actual semiconductor device (diode) processing conditions silicon wafers cut from crystals not pre-annealed may influence "leakage limited diode yield" depending on the amount of oxygen present in the silicon wafers.

Findings on the out-diffusion of oxygen in oxygen-rich (~ 10^{18} atoms/cm^3) wafers, as a result of semiconductor device processing, (reported previously by other workers in the field) are confirmed.

Increase in device yield (diodes) and improved lifetime in epitaxial films obtained with oxygen rich silicon wafers as substrates are correlated with the "intrinsic gettering" action of oxygen rich wafers.

It is shown that "external gettering" cannot improve minority carrier lifetime in silicon wafers if during processing "intrinsic gettering" is active.

It is also shown that "external gettering" is very effective in improving lifetime in silicon wafers not containing "intrinsic gettering" sources.

In such wafers external gettering techniques such as Impact Sound Stressing (ISS) improve the lifetime distributions to values obtained in oxygen-rich wafers.

A total Transmission Electron Microscopy analysis of the defect state in all wafers investigated has also been performed and the results are correlated with the lifetime properties measured.

6.0 ACKNOWLEDGMENTS

Technical Support was given by Mr. H. Ilker, Transmission Electron Microscopy, Mr. C. P. Schneider, Electrical Measurements, and Mr. C. Hoogendoorn, X-ray Topography.

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APPENDIX

In dislocation-free crystals, the growth of the precipitates follows almost a parabolic law. This would imply that the growth process is diffusion-controlled. Based on reasonable assumptions, the size of the precipitates can be estimated from the following simplified model.

Consider that a dislocation-free crystal initially supersaturated with oxygen of concentration C_o has precipitation sites widely separated from each other. Assume that the rate of precipitation is mainly diffusion-controlled rather than reaction- controlled, and that the oxygen concentration at strain centers is at the solubility limit C_s. The diffusion-controlled precipitation was extensively treated by Ham (33). In initial growth, the radius of a spherical precipitate (34) is

$$b = [\, 2DV_p\ (C_o - C_s)\, t]^{1/2}$$

where D is the diffusion coefficient of oxygen in silicon,

V_p is the atomic volume of oxygen, and

t is the time of annealing

As discussed before, the precipitates in the present case is

octahedral. Assume that the volume of octahedral precipitates is equal to that of spherical precipitates. The size of the octahedral precipitates is therefore

$$d = (2\sqrt{2}\,\pi)^{1/3}\ b$$
$$= (8\pi)^{1/3}\ [V_p (C_o - C_s)\ Dt]^{1/2}$$

This equation explains quantitatively the following experimental results:

1) The precipitates grow by a parabolic law. For similar oxygen supersaturations, the precipitate size is essentially determined by the diffusion length $(Dt)^{1/2}$. It is of interest to compare the precipitate size for different annealing conditions. The size, d_1, is about 0.47 μm at 1050°C after 60 hours annealing (square precipitates in Ref. (7)). This is about the same size as the one obtained after annealing 40 hours at 1100°C (d_2 = 0.46 μm, Fig. 9). The diffusion coefficient of oxygen in silicon according to (32) is 6.5×10^{-11} at 1050°C and 10×10^{-11} cm^2/sec at 1100°C. The ratio of

$$\frac{d_1}{d_2} \cong \sqrt{\frac{D_1 t_1}{D_2 t_2}}$$

is approximately equal to one. This is in good agreement with the experimental results. These findings support this simplified diffusion-controlled model.

2) The rate of precipitation is determined by the degree of oxygen supersaturation and diffusivity. Oxygen supersaturation decreases, but diffusivity increases with increasing temperature. This explains why precipitation occurs only in oxygen-supersaturated wafers (section A and B wafers). This also explains that the rate of precipitation increases from $1000^{o}C$ to $1150^{o}C$ because the diffusion term is dominant in this temperature range. At an annealing temperature around $1300^{o}C$ and higher, swirl formation does not occur due to negligible supersaturation.

3) As in previous studies (6-9), this investigation can not reveal the constituents of the precipitates from electron diffraction pattern. These precipitates are generally assumed to be SiO_2 based on the measured reduction of oxygen concentration in the wafers after annealing. This assumption can be tested by comparing the precipitate size as given by the above equation. Taking $V_p \simeq 1 \times 10^{-23} cm^3/atom$, $(C_o - C_s) = 0.5 \times 10^{18}$ atoms/cm^3 and $D = 1 \times 10^{-10} cm^2/sec$ at $1100^{o}C$, the calculated values of precipitate size are given in Fig. 9. The calculated values are about half of the experimentally observed values. This indicates that the precipitate size can be predicted reasonably well by using the properties of oxygen, i.e., supersaturation and diffusion coefficient. We conclude that the precipitates are SiO_2.