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LINEAR TIME-DELAY GENERATOR USING ECL TECHNOLOGY.(U)
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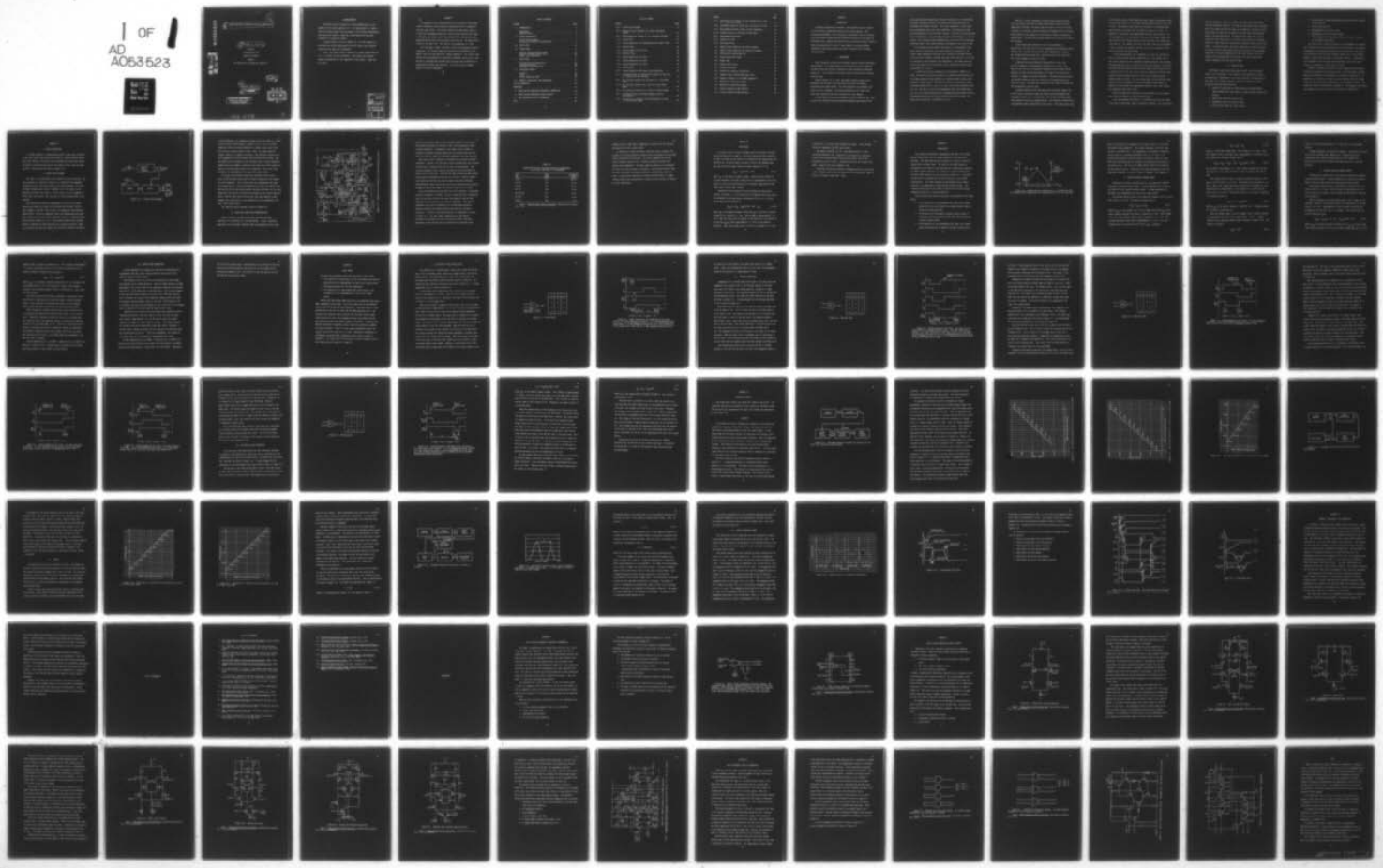

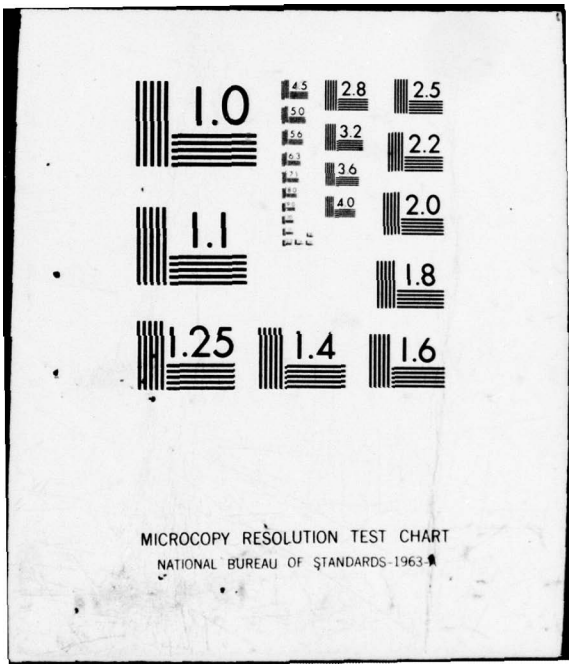
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LINEAR TIME-DELAY GENERATOR USING ECL TECHNOLOGY

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The University of Tennessee, Knoxville

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ABSTRACT

The purpose of this research project was to develop a wide-range, linear, time-delay circuit having an output pulse that is compatible with ECL logic levels. The circuit requires an input pulse width of 4 nsec, has a propagation delay of 8 nsec, and has rise and fall times of 2 nsec on the output pulse. The linearity error between the delay generated and the delay dial setting is less than 1%. The output pulse jitter is less than 0.2%. The circuit is retriggerable in 3 nsec.

The wide-range, linear, time-delay circuit was developed using ECL technology. The voltage comparison functions were performed by four AM685's which are high-speed ECL voltage comparators. The various logic functions were performed with three MECL integrated circuit chips. One MC10104 IC performed AND and NAND logic functions and two MC10105 IC's performed OR and NOR logic functions. The circuit used a minimum number of discrete components.

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CHAPTER I

INTRODUCTION

Time-delay generation has become a very important area of interest in the electrical engineering field for the design engineer. The increasing development of the electronics technology in the last fifteen years has created a great need for time-delay circuitry in the areas of instrumentation, computers, microprocessors, and special purpose circuits. Delay gate generators are used in large numbers in nuclear research laboratories for gating scalars and other instruments and for timing synchronization.

I. BACKGROUND

Early time-delay circuits were developed around the basic monostable multivibrator. The linear portion of a RC run-up was used to generate the delay which was varied by varying the R and switching in different values of C. The linearity of the delay range was poor and the recovery time was long.

Hewlett Packard [1], in 1962, developed a general purpose pulse generator with the delay circuitry being controlled by blocking oscillators and tunnel diodes. The pulse generator was designed to be used as a test instrument. The delay generated was not linear with delay dial setting and the delay circuitry was very complex.

A linear delay circuit was introduced in 1963 by Rakovich [2]. This circuit was a modified collector-coupled monostable multivibrator with

the coupling network operating in exactly the same way as a conventional Bootstrap integrator circuit, thus enabling the timing capacitor to discharge with constant current. The circuit generated a linear sweep and a rectangular pulse (TTL logic compatible), the duration of which was varied linearily with a dc control voltage. A linearity error of less than 1% was achieved over a very wide range of pulse-width variations (1 μsec to 4 msec). The input pulse width depended on the turn-on time of the input gate transistors used. The recovery time was long compared to the turn-on time.

Two engineers from the Sperry Gyroscope Co. [3] developed a time-delay circuit controlled by the stored charge in a transistor. The stored charge phenomenon associated with saturated or bottomed transistors was used to obtain a variable time delay from 0.58 μsec to 4.65 μsec by switching in four different type transistors. The output pulse had a slow rise time of 0.2 μsec and the circuit required an input trigger pulse width of 1.5 μsec.

A useful gate and delay generator was introduced by ORTEC [4] in 1966. The delay circuitry was primarily a monostable multivibrator with the timing capacitor being charged by a constant-current source, which produced a linear run-up. The delay was varied by varying the current to produce delays from 0.1 μsec to 11 μsec, with a delay linearity error of ± 2%. The delay circuit was retriggerable after the desired delay plus 0.1 of the range setting, with a minimum input pulse width of 25 ns. The generated delay was not linear with the delay dial setting. The delay dial setting had a reliability of ± 5%.

EG&G [5], in 1970, introduced a delay and gate module with the delay time being controlled by tunnel diodes which resulted in very complicated circuitry. The delay range was from 0.1 μsec to 110 μsec. In addition to varying a control voltage, the charging rate of the delay timing capacitors was changed for each decade of range to produce the desired delay. The delay dial setting accuracy was 10 nsec or 5% of the dial setting.

A wide range, linear, time-delay circuit was published by Rakovich [6], in 1970, with the circuit comprised of a monostable multivibrator and a bistable multivibrator using complementary switches. The voltage-controlled delay had a linearity error of less than 0.1% over a delay range of 15 μsec to 6 msec.

A gateable delay gate generator having five IC's and a few discrete components was developed by Tatavczuk [7] in 1972. The heart of the unit was two monostable unibrators with the delay being produced by using the trailing edge of the output of the first univibrator to trigger the second univibrator. The delay and pulse width was variable between 30 nsec and 10 msec with a minimum input pulse width of 30 nsec. The delay dial setting was not linear with delay and the retriggerable time was long.

A highly flexible circuit providing delay and gating signals for on/off control of NIM fast logic and nuclear counting equipment was developed in 1975, by J. F. Pierce [8]. The circuit contained timers which operated on the dual ramp principle. This approach eliminated the long deadtime effect experienced in early units. The timing cycle could

be started by either a NIM-standard fast logic signal having a pulse width of less than 4 nsec, or a TTL signal having a minimum width of less than 20 nsec. The period of each timer was selectable by calibrated front panel controls for delays over the range of 10 nsec to 11 secs. In addition to both normal and complementary NIM fast logic outputs, this circuit generated a 10 nsec pulse at the end of the normal timing cycle. The linearity error between generated delay and front dial setting was less than 10%. The random jitter was less than 5 parts in 10,000 FWHW or 1 nsec, whichever was greater, and the circuit had a deadtime of less than 10 nsec for any time setting.

A dual gate generator with a deadtime of 10 nsec was developed in 1975 by LeCroy Research Systems Corporation [9]. The timing cycle of the circuit operated on the logarithmic rundown principle, and therefore the generated delay was not linear with delay dial setting. The circuit had presettable delay pulse widths in decade ranges from less than 100 nsec to greater than 11 sec. The circuit could be triggered by NIM fast logic signals having a minimum width of 5 nsec or by TTL signals having a minimum width of 20 nsec. The circuit provided a 10 nsec NIM fast logic signal, which was triggered by the trailing edge of gate output in addition to both normal and complementary NIM fast logic level outputs. The propagation delay was 14 nsec.

There are many other time-delay circuit designs, but the variable delay types are similar to those discussed above.

From the preceding discussion, it is evident that work still needs to be done in wide-range, linear, time-delay circuitry. All of the delay

circuits mentioned, except two, require TTL logic inputs and produce TTL logic computable outputs. TTL logic was the fastest logic available until a few years ago when ECL logic was introduced. ECL logic is much faster than TTL logic and has replaced TTL logic where the switching speed is the governing factor. In addition, ECL logic levels can be converted to TTL logic levels, with very little increase in switching speeds, by simply adding an off-the-shelf integrated circuit chip to the output. As indicated above, delay gate generators are used extensively in nuclear research laboratories where the need exists for wide-range, linear delay circuitry compatible with ECL logic levels. Also, the computers and microprocessors of the future will need linear delay circuits compatible with the fast ECL logic.

II. SCOPE OF STUDY

Wide-range, linear delay and gating circuitry, with ECL output levels, will be necessary in the future, if the benefits of the fast switching device technology is to be fully realized. The objective of this study was to design, construct, and test a time-delay circuit having the following characteristics:

1. Capable of operating with either Nuclear Instrument Module (NIM)-standard fast logic inputs or inputs from ECL logic level devices.
2. Input pulse width of 5 nsec or less.
3. Propagation delay of 10 nsec or less.
4. Rise and fall times of 2 nsec or less.

5. Linearity error between generated delay and delay dial setting of less than 1%.
6. Jitter less than 0.5%.
7. Retriggerable in 10 nsec or less.
8. Complementary ECL logic level outputs.
9. A NIM-standard fast logic output pulse of 10 nsec at the end of the normal output pulse.

The scope of this study was limited to the development of a circuit that exhibited the desired characteristics outlined above. The rigorous development of switching speed equations was not pursued in this study. These equations would have been extremely complex due to the nonlinear parasitic capacitances inherent in high-speed circuitry. Additionally, the development of the switching speed equations for one ECL circuit would have encompassed a thesis study in itself.

Chapter II presents the circuit in block diagram form and briefly outlines the operation of each major block. Also, high-speed switching design and fabrication considerations are discussed in Chapter II. In Chapters III, IV, and V, the input or level-shifting block, the timing block, and the logic block, respectively, are discussed in detail. The laboratory results are presented in Chapter VI. The summary, conclusions, and suggestions for future studies are contained in Chapter VII.

CHAPTER II

CIRCUIT DESCRIPTION

In normal operation, a negative-going input trigger pulse initiates an ECL logic level output pulse whose width is a linear function of the delay dial setting. The circuit can be divided into three basic blocks; The input or level-shifting circuit, the timing circuits, and the logic circuits. These blocks are shown in Figure II-1.

I. CIRCUIT BLOCK DIAGRAM

The input or level-shifting block performs two basic functions. The first function is to match the circuit to a standard 50 ohm impedance transmission line. The second function this block performs is to shift the input voltage pulse, which is normally a -0.7 volt pulse, to be compatible with ECL logic levels. If the circuit is to be triggered by an ECL logic level device, then the input or level-shifting block is not required.

The timing block generates complementary ECL logic level output pulses whose widths are linear with the delay dial setting. When an input trigger is applied to the circuit, two comparators simultaneously change states. The first comparator starts the complementary ECL logic level output pulses and the second comparator turns on a constant-current source having a current of +1 mA. The constant-current source linearly charges a high-quality timing capacitor in a positive direction. When the voltage on the capacitor reaches the value of the reference voltage on

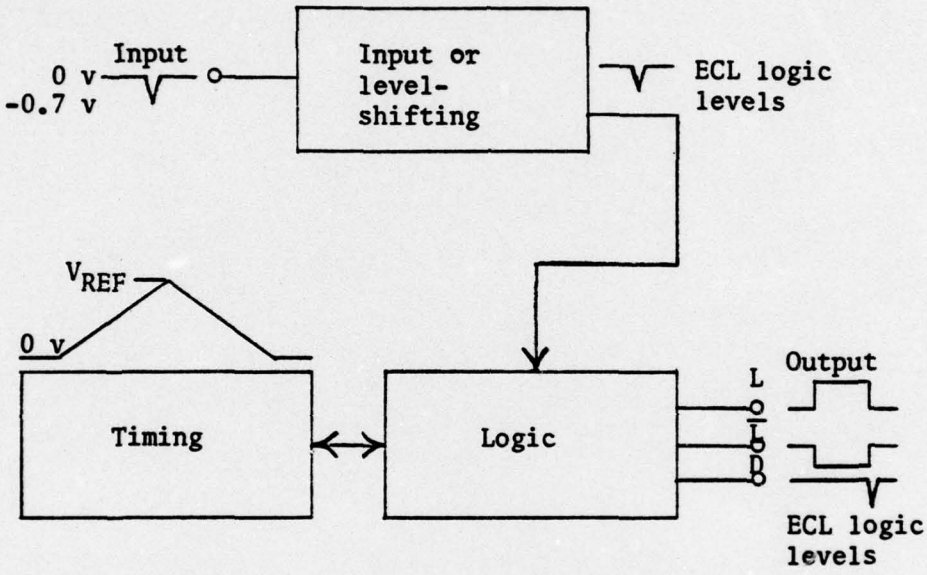


Figure II-1. Circuit Block Diagram.

a third comparator, this comparator changes states and turns on a second constant-current source having a current of -1 mA. Also, the third comparator causes the second comparator to change states, which turns off the first constant-current source. Then, the timing capacitor charges linearly in a negative direction. The reference voltage on the third comparator is varied linearly with the delay dial setting. When the capacitor has discharged to its starting value, a fourth comparator changes state and triggers a portion of the logic block which causes the negative constant-current source to be turned off. Also, this action terminates the complementary ECL logic level output pulses.

The logic block performs three basic functions in the circuit. First, an OR ECL logic gate senses the input voltage pulse and triggers the first comparator. This action starts the complementary ECL logic level output pulses. Second, one NAND ECL logic gate, one AND ECL logic gate and two OR ECL logic gates perform latching operations for the three comparators that govern the charge and discharge of the timing capacitor. Third, a NOR ECL logic gate and an OR ECL logic gate generate a NIM-standard fast output pulse at the termination of the complementary ECL logic level output pulses.

The complete circuit diagram is shown in Figure II-2.

II. DESIGN AND FABRICATION CONSIDERATIONS

Modern electronic systems require more and more switching operations to be performed in a few nanoseconds. Linear, time-delay generation can be extremely dependent upon the propagation delay times

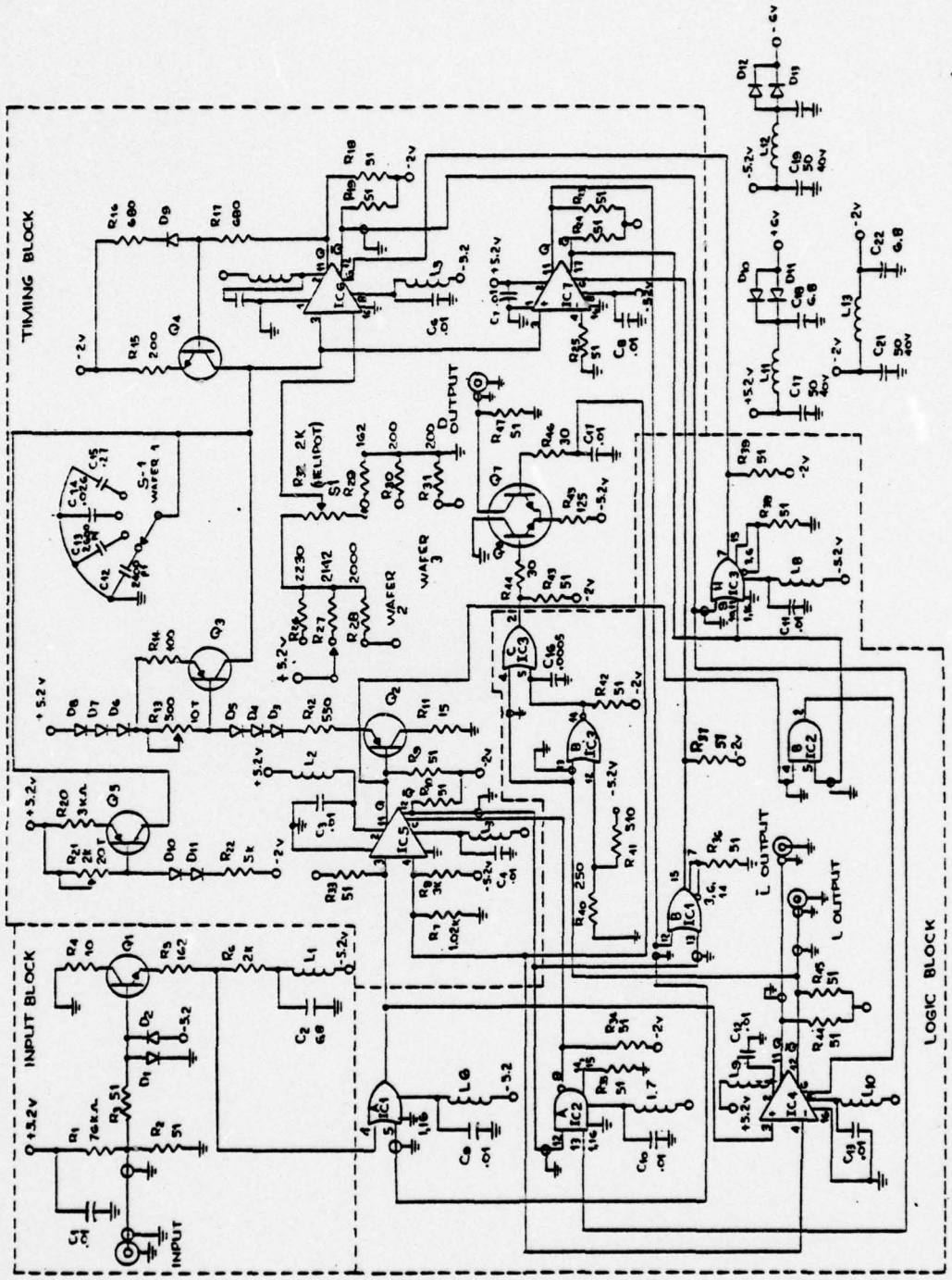


Figure II-2. Complete Circuit Schematic for Linear Time-Delay Circuit.

and the rise and fall times of the switching elements in the circuit. When generating delays of 100 nsec or less, each nanosecond becomes extremely important. Consequently, each logic circuit element is required to perform switching operations with minimal delay and very fast rise and fall times for time-delay generation less than 100 nsec.

Many logic circuit elements are available that perform switching operations. However, very few logic circuit elements meet the criterion of being able to change states in less than five nanoseconds. The typical propagation delay time for the majority of the available TTL devices is 50 to 100 nsec. Schottky TTL logic devices are much faster, having typical propagation delays of 15 to 20 nsec. Emitter-coupled logic (ECL) devices have the shortest delay times when switching. AND/NAND/OR/NOR logic function ECL devices are available having typical propagation delays and output rise and fall times of 2 to 3 nsec.

When interfacing the analog world with logic elements, a high-speed precision comparator is needed. If such a comparator had a propagation delay of less than 10 nsec, the costly and complex circuitry that designers are now forced to use could be simplified. This type of comparator would play an important role in high-speed analog-to-digital conversion and sample-and-hold functions for time-delay circuitry. A survey of available monolithic IC comparators is shown in Table II-1. ECL logic family comparators are the fastest. Designers of time-delay circuitry striving for linear time-delay generation in the 100 nsec and less range will be using ECL logic

TABLE II-1

PROPAGATION DELAY OF AVAILABLE MONOLITHIC COMPARATORS,
100 mv INPUT STEP WITH A 5 mv OVERDRIVE

Type No.	Logic Family	Propagation Delay
AM 111	TTL	200 ns
µA 710	TTL	40 ns
AM 106	TTL	40 ns
µA 760	TTL	25 ns
ME 527/529	TTL	25 ns
MC 1650	ECL	12 ns
AM 685	ECL	6 ns

Source: Advanced Micro Devices Data Book, Advanced Micro Devices, Inc., 1974.

elements and ECL logic family comparators to squeeze the last possible nanosecond out of the overall delay.

In addition to using the fastest switching circuit elements, the maximum in switching speeds are achieved when the designer utilizes high-speed interconnection techniques. The source impedance for the ECL circuit elements should be low. Parasitic coupling increases with higher source impedances. The power supplies should be well decoupled as close to the device supply as possible. Lead lengths should be kept as short as possible and wherever possible a ground plane should be used. A ground plane substantially reduces the possibility of output current spikes from coupling back to inputs and also reduces the effects of stray capacitance.

CHAPTER III

INPUT BLOCK

The input circuit is shown in dashed lines in the upper left-hand section of Figure II-2, page 10. The first function of this circuit is to match the input of the circuit to a standard 50 ohm transmission line. Resistors R1, R2, and R3 match the input to the 50 ohm impedance and bias the base of the input emitter follower transistor, Q1, at

$$V_{B\text{-}Q1} = V_{CC}(R2/(R1 + R2)) \qquad \text{(III-1)}$$

where V_{CC} is the positive supply voltage. Since the base current of Q1 flows through R1, the base voltage of Q1 is approximately zero volts. Diodes D1 and D2 provide protection for Q1 against large positive and large negative-going input signals.

Transistor Q1 and resistors R5 and R6 perform the function of shifting the normal -0.7 volt input pulse to compatible ECL logic levels. In the absence of an input pulse, the emitter of Q1 is at -0.7 volts. The voltage between R5 and R6 is

$$V_{R5\text{-}R6} = (V_{EE} - V_{BE})R5/(R5 + R6) - V_{BE} \qquad \text{(III-2)}$$

where V_{EE} is the negative supply voltage and V_{BE} is the base to emitter voltage of Q1, typically 0.7 volt. This voltage is approximately -1.0 volt. When the input pulse is applied to the base of Q1, the emitter of Q1 and also $V_{R5\text{-}R6}$ shifts approximately 0.7 volts in the negative direction. Thus, the voltage on pin 4 of IC1-A is normally -1.0 V and

is driven to -1.7 V with a fast negative NIM signal. These voltage levels are compatible with ECL logic levels.

The emitter follower, Q1, is a Type MPS2369 which is a fast switching transistor [10]. Capacitor C2 and inductor L1 comprise a filter so that current spikes from the power supply line are not transmitted to pin 4 of IC1-A. Resistors R5 and R6 are 1% metal film types. Diodes D1 and D2 are IN4002's [11].

Transistor Q1 typically exhibits a propagation delay of less than 1 nsec. However, due to the low base drive the rise and fall times of Q1 will be slightly larger than 1 nsec.

CHAPTER IV

TIMING BLOCK

The timing block generates complementary ECL logic level output pulses having widths that are linear functions of the delay dial settings. The right-hand portion of Figure II-2, page 10, shows the timing block in dashed lines. The width of the output pulses is determined by the length of time required for a high-quality capacitor to charge linearly from zero to a preset but variable voltage level, and then return linearly to zero as shown in Figure IV-1. The preset voltage level is determined by the dial setting of a very linear potentiometer. The linear charging and discharging of the timing capacitor is accomplished by using constant-current sources. The constant-current sources are turned on and off by very fast voltage comparators that have a latching capability.

The following three distinct functions are performed by the timing block:

1. The initiation of the complementary ECL logic level output pulses which turn on the positive constant-current source to charge the timing capacitor.
2. The turning on of the negative constant-current source to discharge the timing capacitor which turns off the positive-constant current source.
3. The termination of the complementary ECL logic level output pulses which turns off the negative constant-current source.

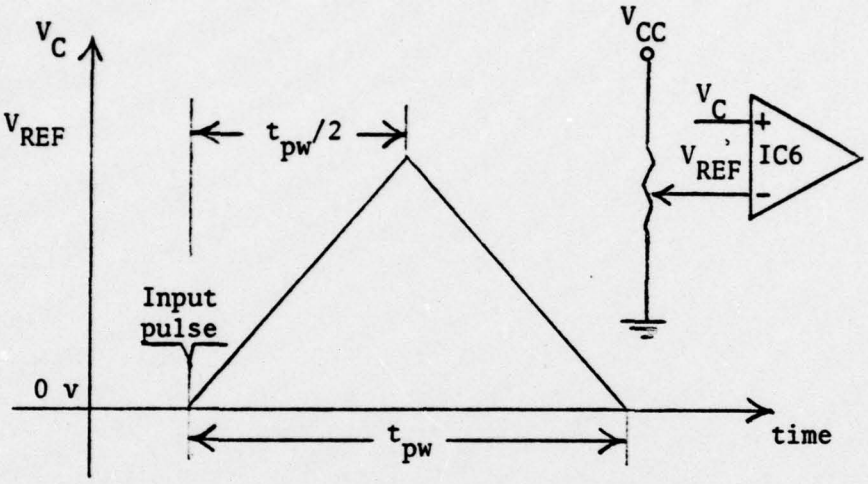


Figure IV-1. Timing Capacitor Voltage, V_C, as a Function of Time. The charging and discharging of the timing capacitor is at the same rate.

Each of the functions is dependent on the output states of a very fast switching voltage comparator. The voltage comparator utilized in this circuit is the AM685 [12]. This comparator is a monolithic integrated circuit that has a maximum propagation delay of 6.5 nsec at 5 mV overdrive and typically exhibits output rise and fall times of 2 nsec. These fast switching times are essential for generating time-delays of 100 nsec or less. The use of the AM685 greatly reduces the complexity of the timing circuitry. Functional and design information on this new high-speed comparator is given in detail in Appendix A and Appendix B.

I. POSITIVE CONSTANT-CURRENT SOURCE

Transistors Q2 and Q3, resistors R11-14, and diodes D3-8 comprise the positive constant-current source. Voltage comparator IC5 is the on/off control for the constant-current source. Voltage comparator IC4 generates the complementary ECL logic level output pulses.

The constant-current source is off when the Q output of IC5 is in the High state or -0.8 volt. The emitter voltage of Q2 is

$$V_{E-Q2} = V_{Q-IC5} + V_{BE} , \qquad \text{(IV-1)}$$

where V_{Q-IC5} is the voltage level of the Q output of IC5 and V_{BE} is the base to emitter voltage of Q2 which is typically 0.7 volt. This voltage is 0.7 volt more positive than the base, therefore at -0.1 volt. The voltage drop across each diode is approximately 0.7 volt. Thus, the voltage level at the positive side of R13, V_{R13}, is given by

$$V_{R13} = V_{CC} - 3V_D \qquad \text{(IV-2)}$$

where V_D is the diode voltage drop. This voltage is +3.1 volts. With the Q output of IC5 in the High state, approximately 1.2 mA flows in Q2. This current sets the base voltage of Q3 at

$$V_{B-Q3} = V_{R13} - (V_{R13} - 3V_D - V_{E-Q2})/(R12 + R13) \; . \qquad \text{(IV-3)}$$

This voltage is approximately +2.7 volts, thereby causing Q3 to be off. Transistor Q3 is not turned off hard in order to minimize the turn-on time.

The constant-current source is turned on when the Q output of IC5 goes to the Low state or -1.8 volts. The emitter of Q2 now goes to -1.1 volts. Again, the voltage drop across each diode is a nominal 0.7 volt. Transistor Q2 has approximately 2.4 mA flowing in it, which sets the base of Q3 at +2.3 volts. The emitter of Q3 is at +3.0 volts, resulting in a constant-current of

$$I_{PCC} = (V_Y - V_{E-Q3})/R14 \qquad \text{(IV-4)}$$

where V_{E-Q3} is the emitter voltage of transistor Q3. A constant-current of 1 mA flows in transistor Q3.

When IC5 changes states, IC4 also changes states, thereby starting the complementary ECL logic level output pulses. Also, the timing capacitor starts charging toward a preset reference voltage on IC6. The reference voltage is

$$V_{REF} = TI/2C \qquad \text{(IV-5)}$$

where C is the timing capacitance, T is time, and I is the constant current.

Voltage comparators IC4 and IC5 are AM685's. Transistors Q2 and Q3 are the fast switching type, MPS3640 [10]. Diodes D3-8 are low capacitance, fast current switching type No. FD777 diodes [13]. Resistors R12 and R14 are 1% metal film types and R13 is a ten-turn helitrim.

II. NEGATIVE CONSTANT-CURRENT SOURCE

Transistor Q4, resistors R15-17 and diode D9 comprise the negative constant-current source. Voltage comparator IC6, along with resistors R26-32, are the on/off control for the constant-current source.

The constant-current source is off when the Q output of IC6 is in the Low state or -1.8 volts. With the base of transistor Q4 at -1.8 volts, there is less than 0.5 volts between base and emitter, resulting in Q4 being off.

When the voltage at the noninverting input of IC6 is equal to the reference voltage at the inverting input, the Q output goes to the High state or -0.8 volt. Approximately 0.4 mA of current flows from IC6 through R16, R17 and D9 to the -2 volt supply. This current sets the base of transistor Q4 at

$$V_{B-Q4} = V_{Q-IC6} + (V_A + V_D - V_{Q-IC6})/(R16 + R17) \qquad \text{(IV-6)}$$

where V_{B-Q4} is the base voltage of transistor Q4, V_{Q-IC6} is the voltage level of the Q output of IC6, V_D is the diode voltage drop and V_A is the

negative supply voltage for transistor Q4. This voltage is approximately -1.1 volts. The emitter of Q4 is at -1.8 volts, resulting in a 1 mA constant-current in transistor Q4 as given by

$$I_{NCC} = (V_A - V_{E-Q4})/R15 \qquad \text{(IV-7)}$$

where V_{E-Q4} is the emitter voltage of transistor Q4. The voltage at the noninverting input of IC6 is the capacitor voltage. The reference voltage at the inverting terminal of IC6 is controlled by a very linear, ten-turn helipot.

The dial setting of the helipot corresponds to the specific delay desired and is translated into a control voltage. When IC6 changes states, a logic function is performed that results in IC5 changing states, which then turns off the positive constant-current source.

When the negative constant-current source is off, transistor Q4 is turned off much harder than transistor Q3 is when it is in its off state. Therefore, transistor Q4 does not turn on in a minimum time. This condition allows the capacitor voltage to overdrive the reference voltage at the inverting input of IC6. Thus IC6 is latched with the Q output in the High state before the capacitor voltage can underdrive the reference voltage and switch the Q output back to the Low state. When transistor Q4 is fully on, the timing capacitor discharges at the same rate that it charged.

Voltage comparator IC6 is an AM685. Transistor Q4 is a 2N3904 [11]. Diode D9 is type No. FD777. Resistors R15-17 and R26-31 are 1% metal film type and R32 is a very linear, ten-turn helipot.

III. OUTPUT PULSE TERMINATION

Voltage comparator IC7 performs the functions of terminating the complementary ECL logic level output pulses and turning off of the negative constant-current source.

The $\overline{Q}$ output of IC7 is in the Low state during the linear charge and discharge of the timing capacitor. When the timing capacitor voltage discharges to zero volts, which is the reference voltage at the inverting input of IC7, the $\overline{Q}$ output goes to the High state. This action triggers an ECC logic gate which releases the latch of IC6. When the latch of IC6 is released, the output of the comparator changes states and causes the negative constant-current source to turn off. The $\overline{Q}$ output of IC7 is latched in the High state and remains at that level until a new trigger pulse is applied to the circuit and the latch on IC5 is set.

Transistor Q5, resistors R20-22 and diodes D10-11 perform a current compensating function. With the circuit at rest, the very low input bias currents, approximately 5 μA, of IC6 and IC7 cause the timing capacitor to charge to a small negative voltage. The leakage currents of transistors Q3 and Q4 effectively cancel each other. Therefore, a current source, turned just about full off, provides the necessary input bias currents for IC6 and IC7. With this arrangement, the voltage on the timing capacitor is maintained at approximately zero volts.

Voltage comparator IC7 is an AM685. Transistor Q5 is a 2N3906 [11]. Resistors R20, R22 and R26-31 are 1% metal film type and R21 is a twenty turn helitrim potentiometer. Diodes D10-11 are type 1N4002. Capacitors

C12-15 are the dip-mica type. Resistors R26-31 are selected so that the positive side and the negative side of R32 is at the voltage levels calculated by Equation IV-5. The values of T are the times at the low and high end of each delay range.

CHAPTER V

LOGIC BLOCK

The logic block performs three basic functions in the circuit:

1. The sensing of an input pulse to start the timing cycle and the generation of the complementary ECL logic level output pulses.
2. Latching operations for the four comparators.
3. The generation of a NIM-standard fast output pulse at the termination of the complementary ECL logic level output pulses.

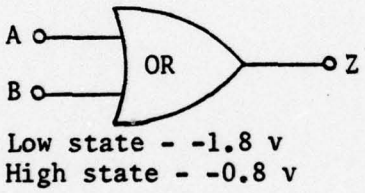
The logic OR, NOR, AND and NAND functions are accomplished with three MECL integrated circuit chips. Two of the chips are the type MC10105 and are used for OR and NOR logic operations. The other chip is a type MC10104 and is used for the logic AND and NAND operations [14]. The design of the necessary logic circuitry with discrete circuit components having less than 5 nsec propagation delays and output rise and fall times would have been highly complex, if possible. Therefore, the MC10104 and MC10105 integrated circuit chips were selected to perform the logic functions. These IC's have typical propagation delays and output rise and fall times of 2 to 3 nsec. Functional information on the MC10104 and MC10105 MECL integrated circuit chips is given in Appendix C. The logic block of the circuit is shown in dashed lines in the lower portion of Figure II-2, page 10.

I. INITIATION OF THE TIMING CYCLE

The timing cycle is started when an input pulse causes the ECL OR gate, IC1-A, to change states. When IC1-A changes states, IC4 and IC5 change states. The complementary ECL logic level output pulses are initiated and the positive constant-current source is turned on. The symbol and truth table for an OR gate are shown in Figure V-1. A timing diagram for IC1-A is shown in Figure V-2.

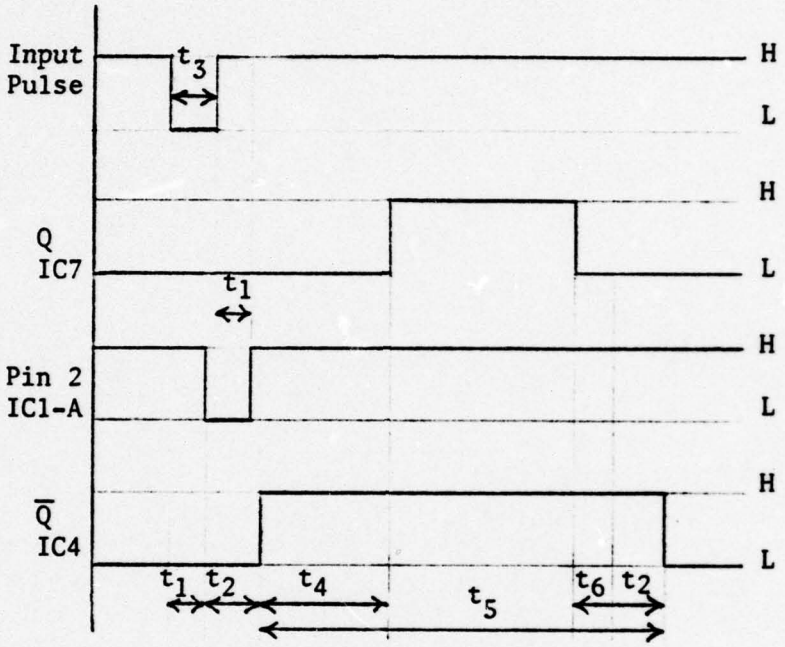
In the absence of an input pulse, pin 4 of IC1-A is in the High state or approximately -1.0 volt. Pin 5 of IC1-A is held in the Low state by the Q output of IC7. Therefore, the output of the OR gate, pin 2 of IC1-A, is in the High state.

When an input pulse is applied to the circuit, pin 4 of IC1-A goes to the Low state or approximately -1.7 volts. This action causes the OR gate output to go to the Low state, thus causing voltage comparators IC4 and IC5 to change states. The input pulse is required to be present long enough for the $\overline{Q}$ output of IC4 and IC5 to be latched in the High state. The latch of IC5 is enabled approximately two ECL gate propagation delays before IC7 has its latch released. When the latch on IC7 is released, the Q output of IC7 and pin 5 of IC1-A go to the High state. This action prevents the timing block from responding to another input signal until the timing cycle has ended. When the Q output of IC7 goes to the Low state at the end of the timing cycle, the circuit is ready to process another input signal. However, to ensure that the 10 nsec NIM output pulse is generated, the $\overline{Q}$ output of IC4 should remain in the



A	B	Z
L	L	L
L	H	H
H	L	H
H	H	H

Figure V-1. OR Gate Data.



H State - 0.8 V, L State - 1.8 V

Figure V-2. Timing Diagram for the Complementary ECL Output Pulses. The times shown are as follows: t_1 is the propagation delay of IC1-A, t_2 is the propagation delay of IC4, t_3 is the minimum input pulse width, t_4 is the propagation delays of IC2-A, IC1-B and IC7, t_5 is the output pulse width, and t_6 is the propagation delay of IC1-B.

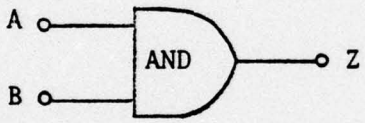
Low state for 10 nsec before a new input pulse causes it to change states. Thus, the retriggerable time is 10 nsec minus the propagation delays of IC4 and IC1-A, or approximately 3 nsec.

II. LATCHING OPERATIONS

Comparator IC4 is latched with the $\overline{Q}$ output in the High state when triggered by the OR gate, IC1-A. The $\overline{Q}$ output remains in the High state until IC7 reacts to the timing capacitor voltage as it ramps back down to zero volts. The latching operation for IC4 is accomplished with the AND gate, IC2-B. The symbol and truth table for an AND gate are shown in Figure V-3. A timing diagram for the latching operation on IC4 is shown in Figure V-4.

With the circuit at rest, pin 5 of IC2-B is held in the High state by the $\overline{Q}$ output of IC7. Pin 4 of IC2-B is held in the High state by the Q output of IC5. The output of the AND gate is in the High state. With the output of IC2-B in the High state, IC4 operates normally. When OR gate, IC1-A, causes IC4 and IC5 to change states, pin 4 of IC2-B goes to the Low state. This action causes pin 2 of IC2-B to go to the Low state and latches IC4 in its output states of $\overline{Q}$ High and Q Low. The changing of states of IC5 results in the output of IC7 being unlatched. When the latch on IC7 is released, pin 5 of IC2-B goes to the Low state. This action ensures that the output of IC2-B remains in the Low state when IC5 changes states half-way through the timing cycle.

The required input pulse width to ensure that IC4 is latched properly is the latch set-up time of IC4 plus the propagation delay of



A	B	Z
L	L	L
L	H	L
H	L	L
H	H	H

Figure V-3. AND Gate Data.

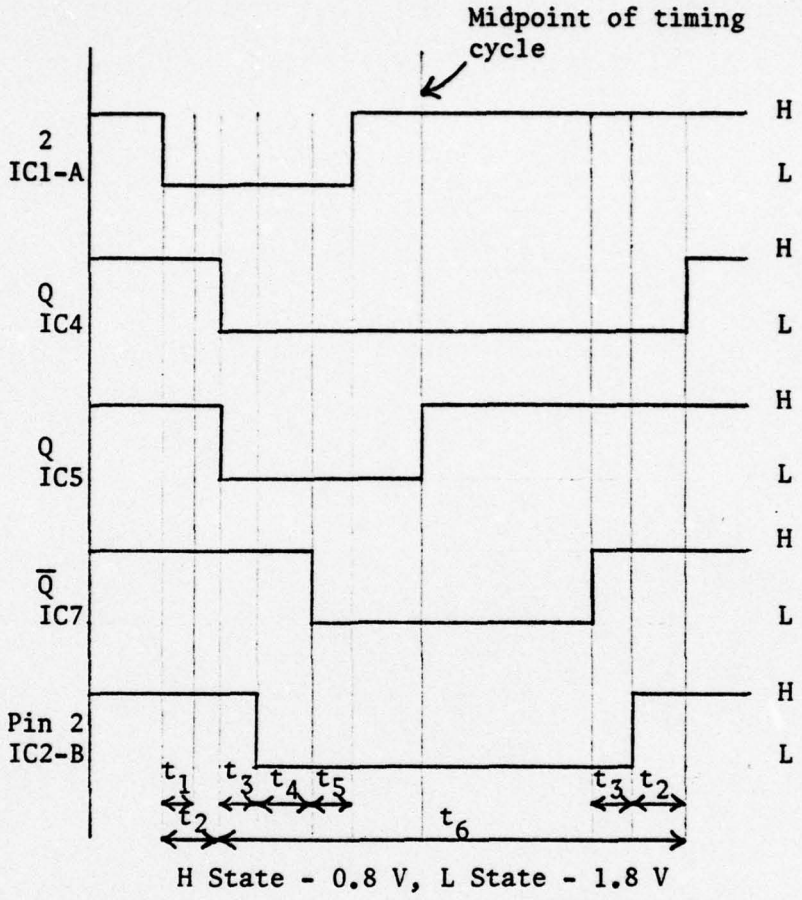


Figure V-4. Timing Diagram for IC4 Latch. The input pulse is long compared to propagation delay times. The times shown are as follows: t_1 is the latch enable setup time of IC4, t_2 is the propagation delay of IC4 and IC5, t_3 is the propagation delay of IC2-B, t_4 is the propagation delay of IC7, t_5 is the propagation delay of IC1-A, and t_6 is the output pulse width.

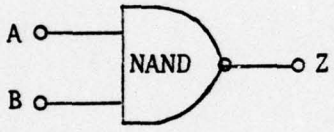
an OR gate. The propagation delay of the circuit is the time from the midpoint of the negative transition of the input pulse to the midpoint of the positive transition of the $\overline{Q}$ output of IC4. This delay is the propagation delay of an OR gate plus the propagation delay of IC4.

Comparator IC4 remains latched with the $\overline{Q}$ output in the High state until the timing capacitor voltage ramps back down to zero volts. When the voltage reaches zero volts, IC7 changes states. Pin 5 of IC2-B goes to the High state causing pin 2 of IC2-B to go to the High state and unlatches IC4. The input to the noninverting input of IC4 is in the High state and causes the comparator to immediately change states when the latch is released. This action terminates the complementary ECL logic level output pulses.

Comparator IC5 changes states simultaneously with comparator IC4, when the OR gate, IC1-A, responds to an input pulse. The latching operation for IC5 is performed by the NAND gate, IC2-A. The symbol and truth table for a NAND gate are shown in Figure V-5. A timing diagram for the latching operation on IC5 is shown in Figure V-6.

With the circuit at rest, pin 12 of IC2-A is held in the Low state by the $\overline{Q}$ output of IC5. Pin 13 of IC2-A is held in the High state by the $\overline{Q}$ output of IC6. Pin 9 of IC2-A is in the High state so that IC5 is not latched and functions normally. Comparator IC5 changes states when an input pulse triggers the OR gate, IC1-A. This action causes pin 12 of IC2-A to go to the High state. Pin 9 goes to the Low state and IC5 is latched in its output states of Q Low and $\overline{Q}$ High.

Comparator IC5 remains latched until IC6 changes states. Pin 13 of IC2-A then goes to the Low state causing the output of IC2 to go to the High state,



A	B	Z
L	L	H
L	H	H
H	L	H
H	H	L

Figure V-5. NAND Gate Data.

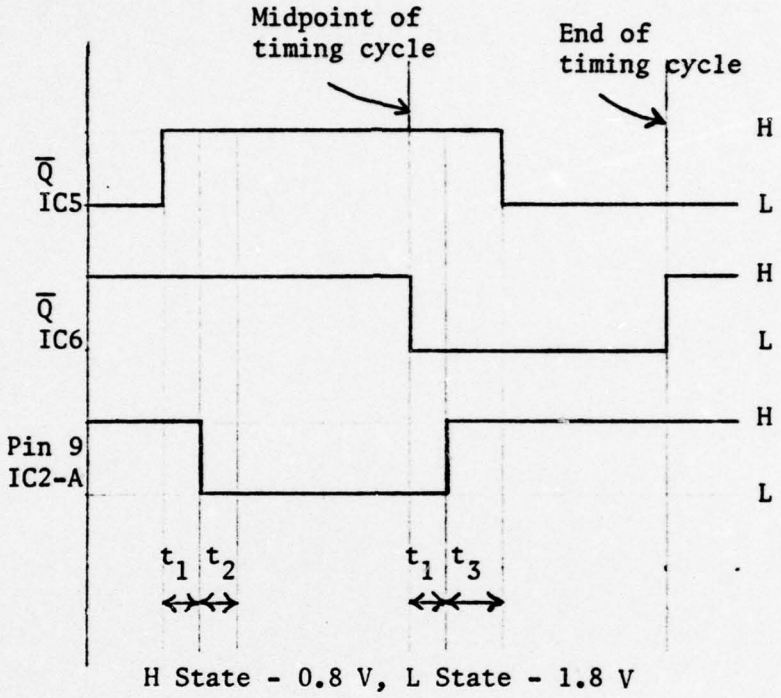


Figure V-6. Timing Diagram for IC5 Latch. The times shown are as follows: t_1 is the propagation delay of IC2-A, t_2 is the latch setup time for IC5, and t_3 is the propagation delay of IC5.

and unlatches IC5. The input to the noninverting input of IC5 is in the High state so that the comparator immediately changes states when unlatched. When IC5 changes states, the positive constant-current source is turned off.

The latching operation for comparator IC6 is performed by the OR gate, IC3-A. A timing diagram for the latching operation on IC6 is shown in Figure V-7. With the circuit at rest, pin 9 of IC3-A is held in the High state by the $\overline{Q}$ output of IC6. Pins 10 and 11 of IC3-A are held in the Low state by the $\overline{Q}$ output of IC7. Pin 7 of IC3-A, the output, is in the High state so that IC6 is not latched and, therefore, functions normally. When the positive-ramping voltage on the timing capacitor causes IC6 to change states, pin 9 of IC3-A goes to the Low state. The output of IC3-A then goes to the Low state and latches IC6 in its output states of Q High and $\overline{Q}$ Low.

Comparator IC6 remains latched until IC7 changes states, which occurs when the negative-ramping voltage on the timing capacitor reaches zero volts. Pins 10 and 11 of IC3-A then go to the High state. This action causes the output of IC3-A to go to the High state and release the latch on IC6. The input to the noninverting input of IC6 is at a lower voltage level than the reference voltage at the inverting input. Thus, the release of the latch causes the comparator to immediately change states, which turns off the negative constant-current source.

The latching operation for IC7 is performed by the OR gate, IC1-B. A timing diagram for the latching operation on IC6 is shown in Figure V-8.

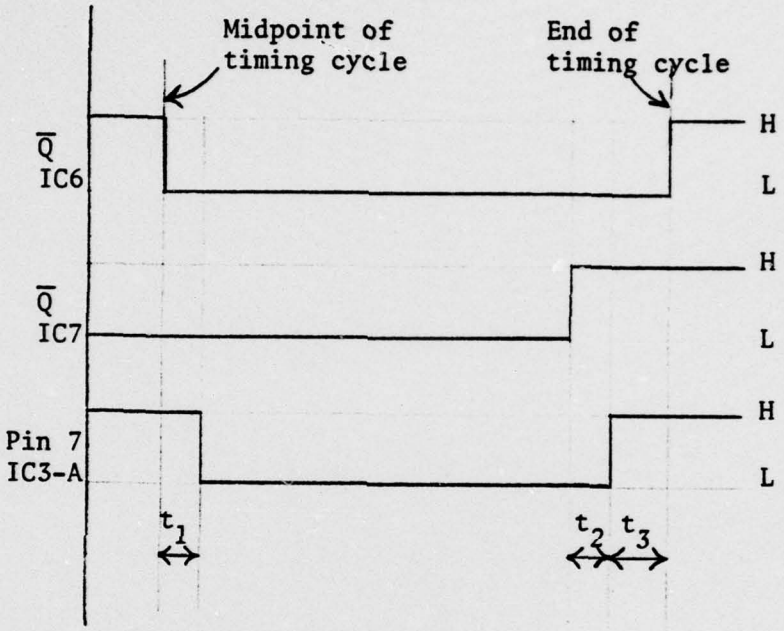


Figure V-7. Timing Diagram for IC6 Latch. The times shown are as follows: t_1 is the propagation delay of IC3-A, t_2 is the propagation delay of IC3-A, and t_3 is the propagation delay of IC6.

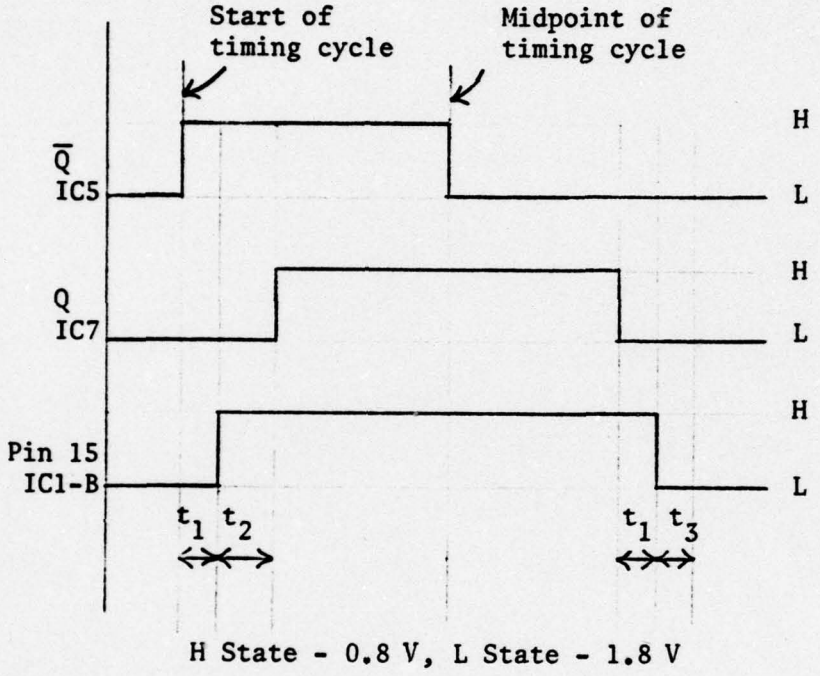


Figure V-8. Timing Diagram for IC7 Latch. The times shown are as follows: t_1 is the propagation delay of IC1-B, t_2 is the propagation delay of IC7, and t_3 is the latch setup time of IC7.

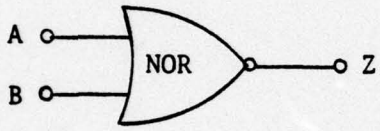
With the circuit at rest, pin 12 of IC1-B is held in the Low state by the Q output of IC7. Pin 13 of IC1-B is held in the Low state by the $\overline{Q}$ output of IC5. Pin 15 of IC1-B is in the Low state. Therefore, IC7 is latched in its output states of Q Low and $\overline{Q}$ High. When an input signal causes IC5 to change states, pin 13 of IC1-B goes to the High state. This action causes the output of IC1-B to go to the High state and release the latch on IC7. The voltage level at the input of the noninverting input of IC7 is higher than the reference voltage at the inverting input. Thus, the release of the latch causes the comparator to immediately change states.

Pin 13 of IC1-B goes back to the Low state when IC5 is unlatched. IC7 responds normally and changes states when the negative-ramping timing capacitor voltage reaches zero volts. Pin 12 of IC1-B then goes to the Low state. The output of IC1-B goes to the Low state and the latch is again applied to IC7.

III. NIM OUTPUT PULSE GENERATION

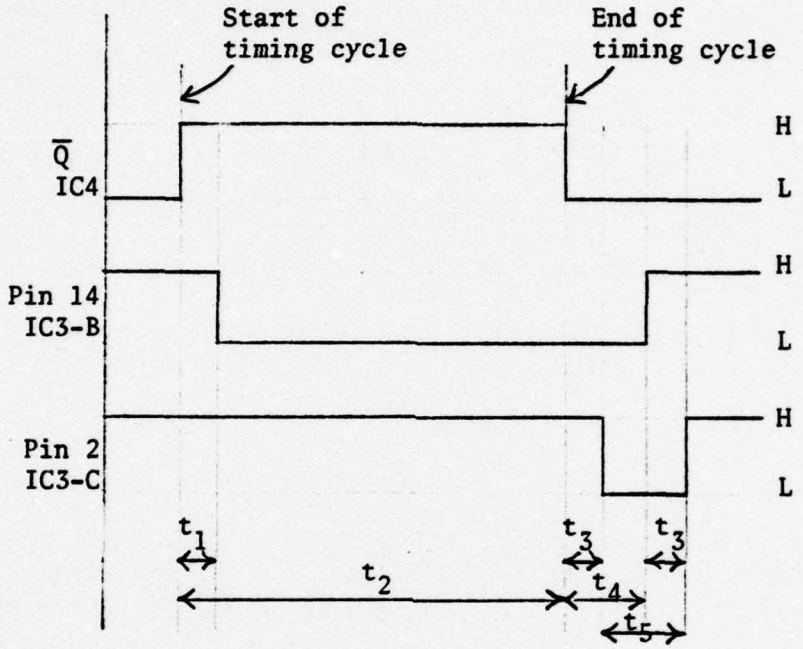
An OR gate and a NOR gate provide the logic functions necessary to generate a NIM-standard fast output pulse at the termination of the complementary ECL logic level output pulses. The symbol and truth table for a NOR gate are shown in Figure V-9. A timing diagram for the generation of the NIM-standard fast output pulse is shown in Figure V-10.

The OR gate is IC3-C and the NOR gate is IC3-B. With the circuit at rest, pin 13 of IC3-B is held in the Low state by the $\overline{Q}$ output of IC4. Pin 12 of IC3-B is in the Low state. The voltage on pin 12 of IC3-B is



A	B	Z
L	L	H
L	H	L
H	L	L
H	H	L

Figure V-9. NOR Gate Data.



H State - 0.8 V, L State - 1.8 V

Figure V-10. Timing Diagram for NIM Output Pulse Generation. The times shown are as follows: t_1 is the propagation delay of IC3-B, t_2 is the output pulse width, t_3 is the propagation delay of IC3-C, t_4 is the increased propagation delay of IC3-B, and t_5 is the NIM-standard fast output pulse width.

$$V_{12} = (V_{EE})R_{40}/(R40 + R41) \qquad (V\text{-}1)$$

where V_{EE} is the negative supply voltage. This voltage is approximately -1.7 volts. Pin 14 of IC3-B, the output, is in the High state, causing pin 5 of IC3-C to also be in the High state. Pin 4 of IC3-C is held in the Low state by the $\overline{Q}$ output of IC4. Therefore, the output of IC3-C is in the High state.

When IC4 changes states at the beginning of the timing cycle, pin 13 of IC3-B and pin 4 of IC3-C go to the High state. This action causes the output of IC3-B to go to the High state. However, this action does not change the output of IC3-C. At the end of the generated delay output pulse, pin 13 of IC3-B and pin 4 of IC3-C go to the Low state. The output of IC3-C now goes to the Low state, but changes back to the High state after one propagation delay of the NOR gate. This action occurs because the output of the NOR gate goes to the High state. Pin 5 of IC3-C is set to the High state and the output of IC3-C is forced to change back to the High state. A capacitor is placed between pin 5 of IC3-C and ground to increase the propagation delay of the NOR gate to about 10 nsec. As a result, the output pulse from IC3-C is a negative going NIM-standard fast pulse of approximately 10 nsec.

The NIM-standard fast pulse having ECL logic levels is not suitable for driving common, in-the-rack instruments, such as time-to-pulse-height converters. These instruments require a NIM-standard fast pulse with no dc level. Transistors Q6 and Q7 form a current switching pair. The current in the switching pair is

$$I_{SP} = (V_E - V_{EE})/R45 \qquad (V\text{-}1)$$

where V_E is the common emitter voltage of Q6 and Q7. This current is approximately 25 mA.

The base of Q7 is biased at -1.3 volts. When the circuit is at rest and while the normal output pulse is being generated, Q6 is on and Q7 is off. The voltage at the base of Q6 is -0.8 volts. Therefore, the voltage at the collector of Q7 is zero volts. When the approximate 10 nsec pulse is propagated from IC3-C, Q6 is turned off and Q7 comes on. The voltage at the base of Q6 goes to -1.8 volts during the pulse. This action produces a negative-going voltage pulse at the collector of Q7. This voltage pulse has the approximate amplitude and time duration of the pulse at the base of Q6. Thus, the NIM-standard fast output pulse is generated at the end of the complementary ECL logic level output pulses.

Transistors Q6 and Q7 are the fast switching type, MPS2369. Resistors R44, R45 and R46 are the 1% metal film type. The function of R44 and R46 is to keep the switching pair from oscillating when switched rapidly.

CHAPTER VI

LABORATORY RESULTS

The linear delay circuit was tested for linearity and jitter. The generated time delay as a function of dial setting was extremely linear. The jitter of the complementary ECL logic level outputs was measured to be less than 0.2%.

I. LINEARITY

Two methods were used to determine the linearity of the time delay produced as a function of the dial setting. One method was used for short delays and another method was used for longer delays. In the method used for the shorter delays, the time delay was converted into a voltage pulse with a time-to-pulse-height converter. Then, the amplitude of the resulting pulse was determined accurately with a multichannel analyzer. This method was restricted by the time-to-pulse-height converter to the evaluation of time delays below 80 μsec. For time delays longer than 80 μsec, an oscilloscope was used to determine the time delay as a function of dial setting.

The first linearity test used the instrument setup as shown in Figure VI-1. A negative-going pulse is transmitted from a pulse generator to a discriminator. The output of the discriminator is a NIM-standard fast pulse. The NIM pulse is simultaneously fed into the circuit and a time-to-pulse-height converter. The D output of the circuit, a NIM-standard fast pulse, is fed into the time-to-pulse-height

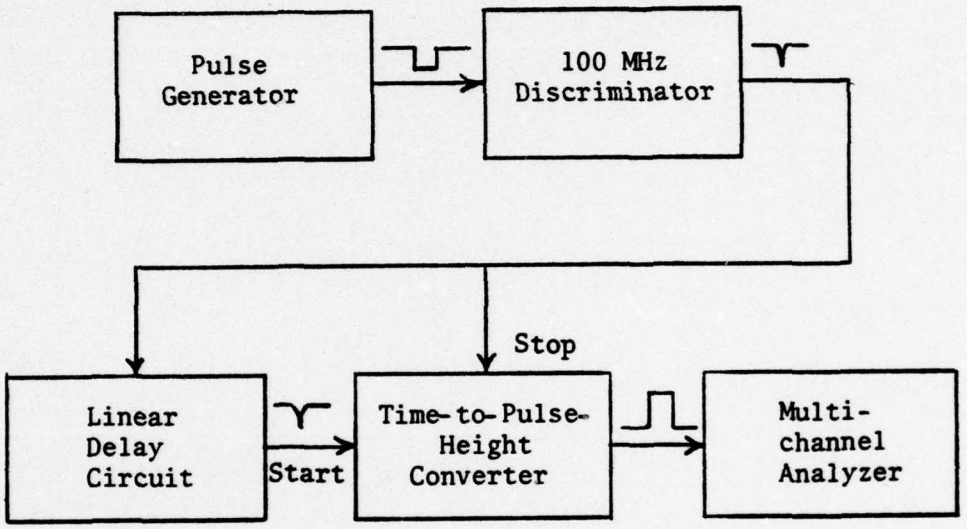


Figure VI-1. Instrument Setup for Testing the Linearity of the Delay as a Function of Dial Setting.

converter. The time-to-pulse-height converter determines the time difference between the two NIM input pulses. This time difference is converted to a voltage level ranging from 0 to 10 volts.

The purpose of the first test was to determine if linear incremental variations of the delay dial setting produced linear time incremental variations in the complementary ECL logic level output pulses. The delay dial was set on a major division. Then, the generated time delay pulse width was converted to a voltage level and fed into a multichannel analyzer. The multichannel analyzer translated the voltage level to a channel number from 0 to 4096. Then, the channel number was plotted as a function of major division dial setting. This procedure was used to check linearity from 100 nsec to 60 μsec. Sixty μsec approached the upper limit of the time-to-pulse-height converter. The results of this linearity test are shown in Figure VI-2, Figure VI-3, and Figure VI-4. The curves of the plots of channel number as a function of major division dial setting are straight lines. Therefore, the linearity of the time delay as a function of dial setting is excellent.

The second method used to test the linearity of the time delay produced as a function of the dial setting used the instrument setup shown in Figure VI-5. A negative-going pulse is transmitted from a pulse generator to a discriminator. The output of the discriminator is a NIM pulse and is fed into the linear delay circuit. The L output of the circuit, the positive-going pulse, is fed into an oscilloscope. The generated time delay pulse width is the width of the L output of the circuit. The oscilloscope external trigger ensures that the oscilloscope sweep starts at the same point each cycle.

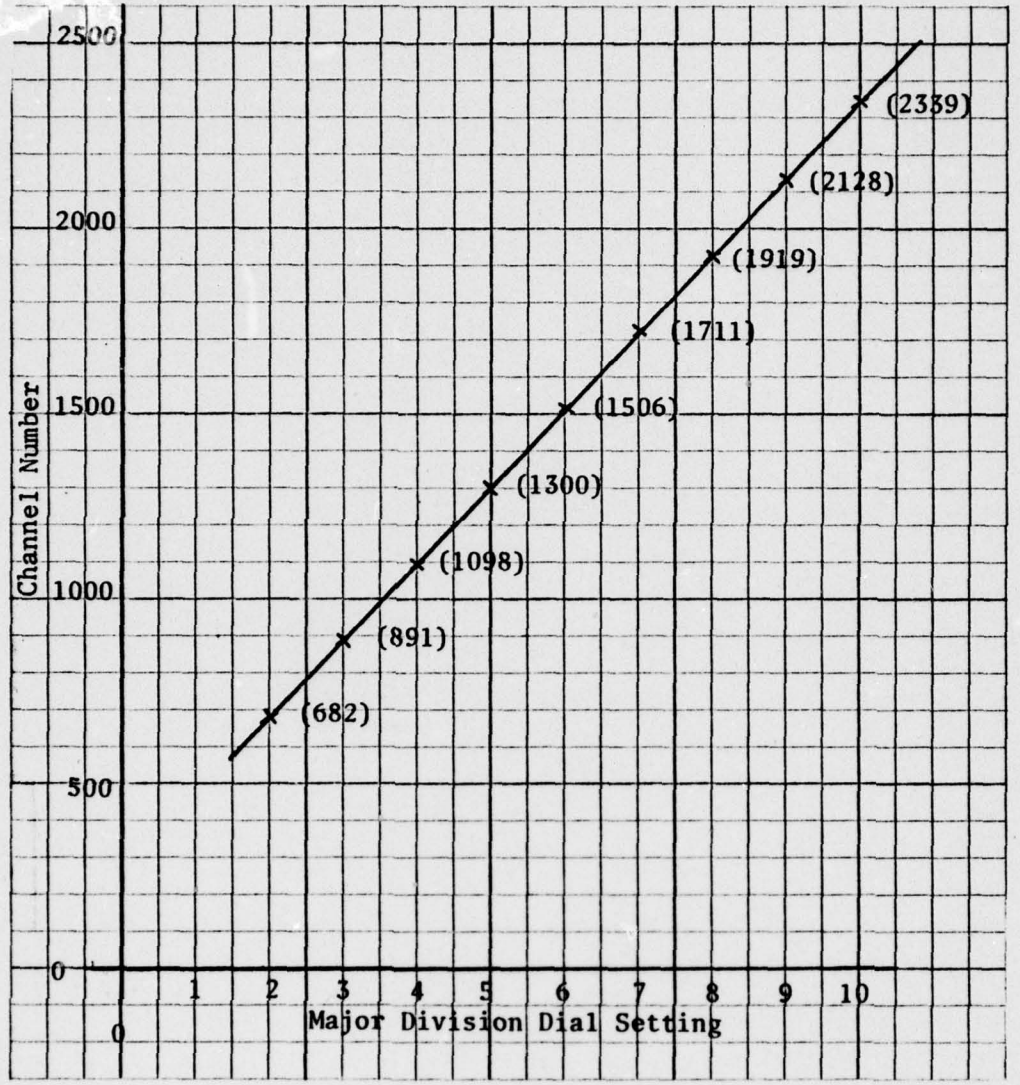


Figure VI-2. Deal Setting Linearity for 100 nsec to 1.1 μsec Delay Range.

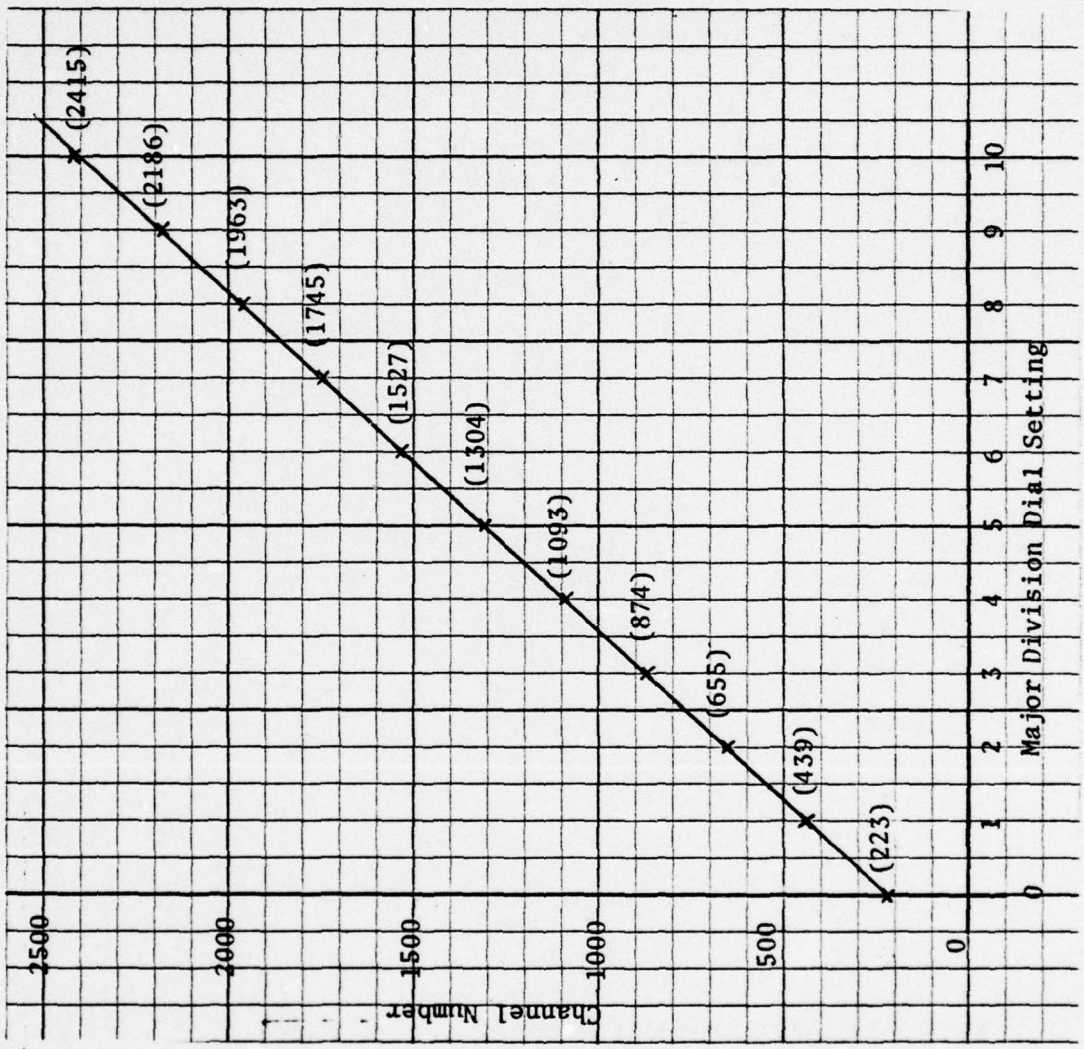


Figure VI-3. Dial Setting Linearity for 1 μsec to 11 μsec Delay Range.

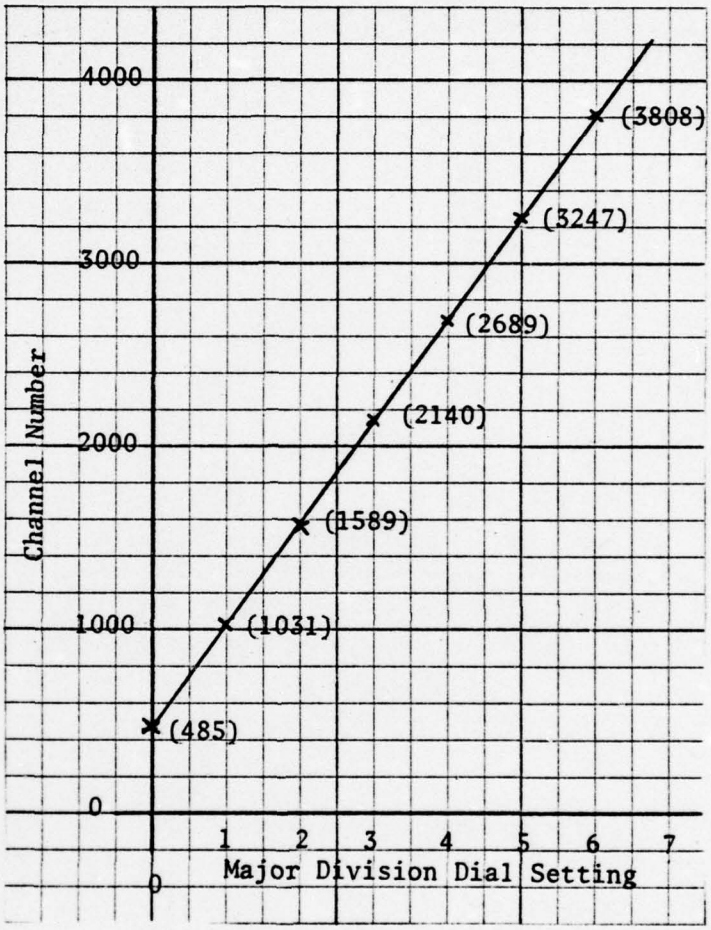


Figure VI-4. Dial Setting Linearity for 10 μsec to 110 μsec Range.

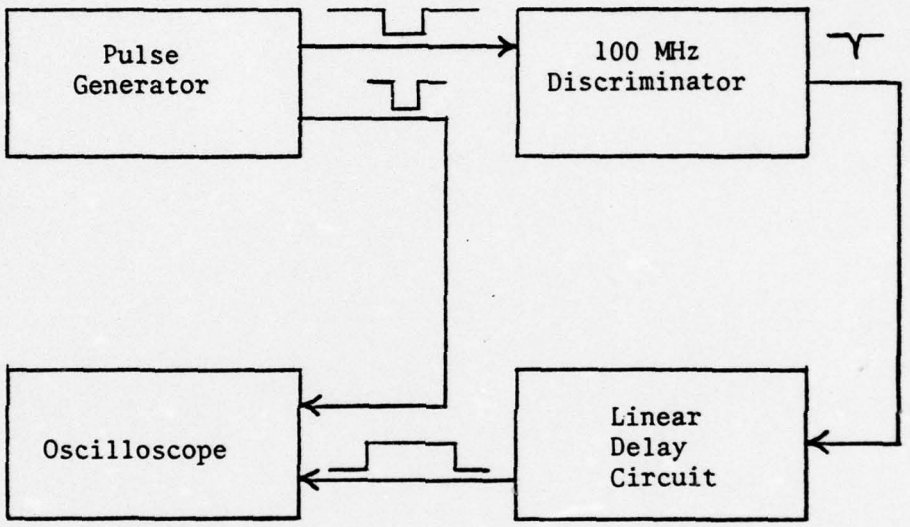


Figure VI-5. Instrument Setup for Testing Linearity with an Oscilloscope.

The purpose of the second linearity test was the same as the first linearity test. This test was conducted for the time-delay ranges of 10 μsec to 110 μsec and 0.1 msec to 1.1 msec. With the delay dial setting at 0.00, the time delay generated should be the time delay value at the low end of the range. With the delay dial setting at 10.0, the time delay generated should be the time-delay value at the high end of the range. The results of this test are shown in Figure VI-6 and Figure VI-7. The curves of the plots of time delay as a function of major division dial setting are straight lines. The time delays observed on the oscilloscope by the naked eye correspond exactly to the time delay desired at a particular delay dial setting. Therefore, the linearity of the time delay produced as a function of the dial setting is excellent.

II. JITTER

Two methods were also used to measure the jitter. One method was used for time delays varying from 100 nsec to 10 μsec and another method was used for time delays ranging from 10 μsec to 1 nsec. The jitter for time delays from 100 nsec to 10 μsec was determined by evaluating data obtained from the multichannel analyzer. The jitter for time delays from 10 μsec to 1 nsec was determined by observation of an expanded oscilloscope display.

Jitter is pulse width fluctuations that occur at a constant delay dial setting. Power supply fluctuations and noise generated in the circuit are only two of many circuit disturbances that cause the pulse

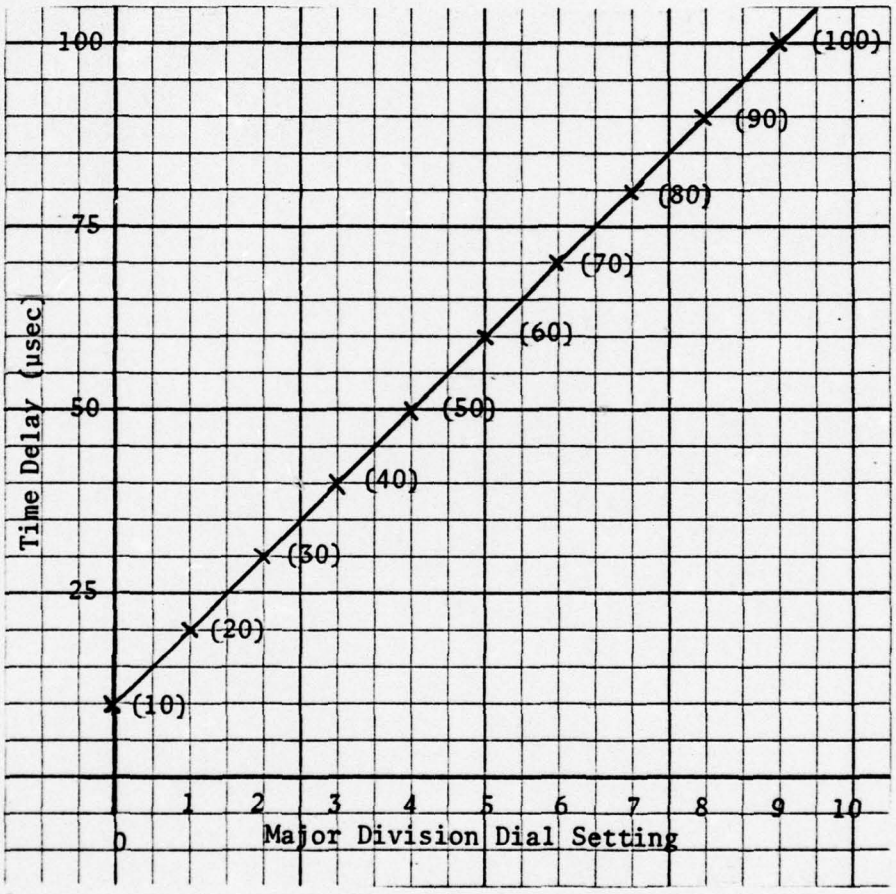


Figure VI-6. Time Delay as a Function of Dial Setting for 10 µsec to 110 µsec Delay Range.

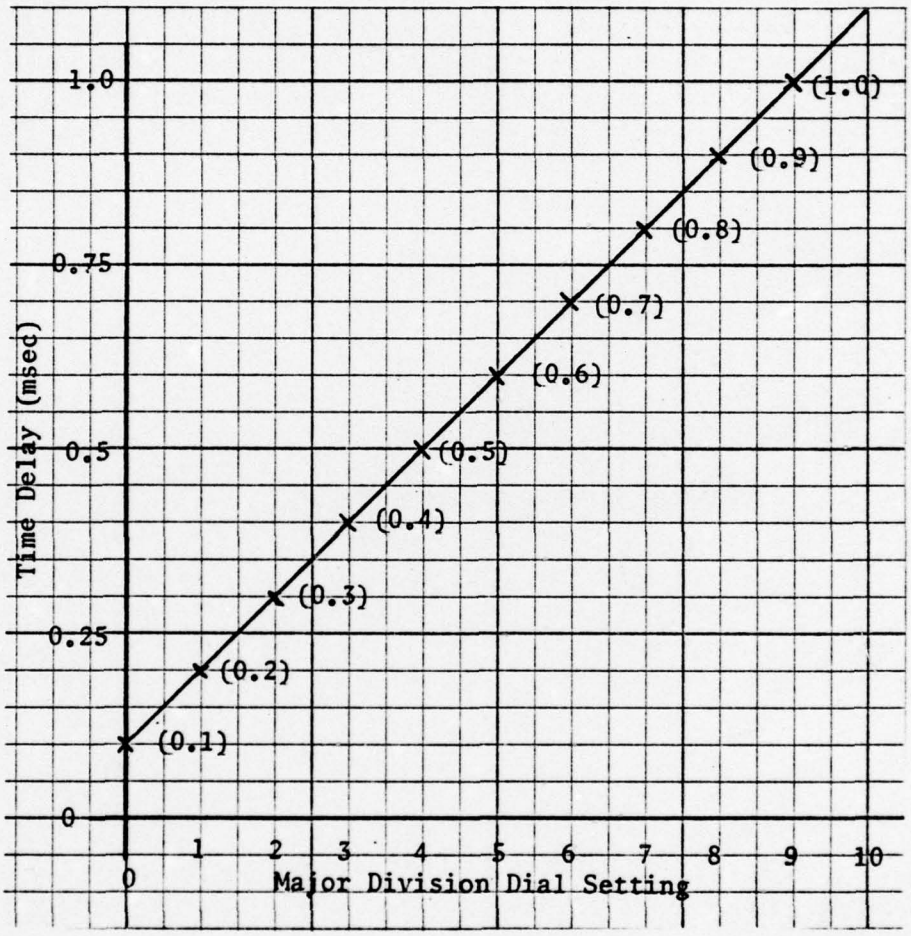


Figure VI-7. Time Delay as a Function of Dial Setting for 0.1 msec to 1.1 msec Delay Range.

width to vary slightly. These disturbances cause the pulse to terminate slightly before or after the ideal pulse termination. A circuit with zero jitter would have the pulse start and stop at the same point each time that the circuit is triggered.

The first segment of the jitter test used the instrument setup shown in Figure VI-8. A negative-going pulse is transmitted from a pulse generator to a discriminator. The output of the discriminator is a NIM pulse. The NIM pulse is simultaneously fed into the linear delay circuit and through a delay box to the start input of the time-to-pulse-height converter. Also, the D output from the linear delay circuit that occurs at the end of the delay pulse is fed into the time-to-pulse-height converter. The output of the time-to-pulse-height converter is fed into a multichannel analyzer. Two inputs are fed into and stored in the memory of the multichannel analyzer. The first input has no delay introduced by the delay box. The second input has a known delay introduced by the delay box.

Data are accumulated in the multichannel analyzer for both inputs so that the system can be calibrated and so that the jitter can be determined. The jitter is calculated by analyzing the information shown on the display screen of the multichannel analyzer. The two distributions are shown in Figure VI-9. The number of picoseconds per channel is

$$Z = D/X \qquad \text{(VI-1)}$$

where Z is picoseconds per channel, D is the amount of delay in

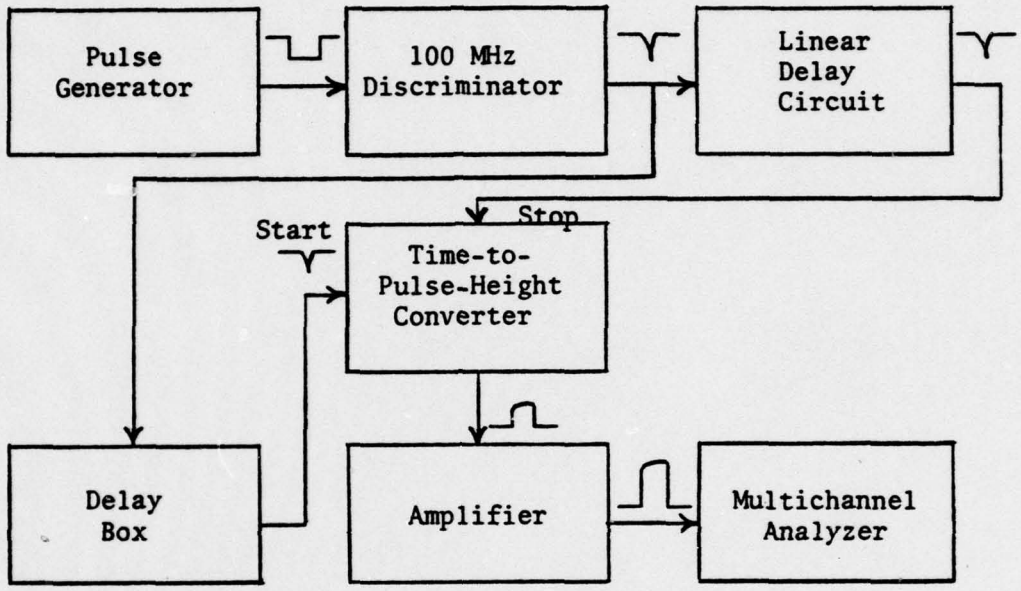


Figure VI-8. Instrument Setup for Jitter Test, 100 nsec to 10 μsec.

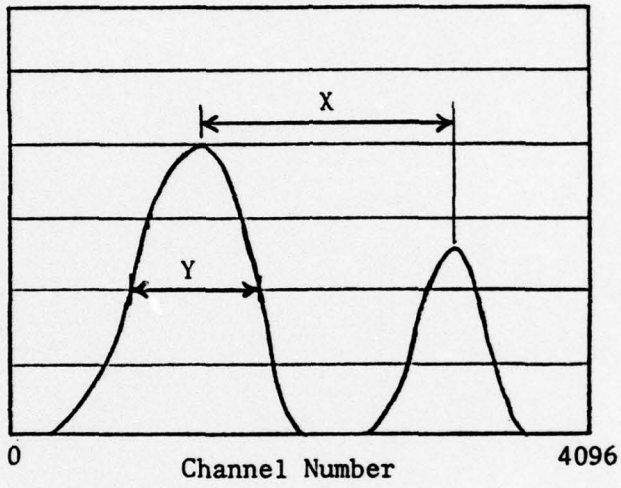


Figure VI-9. Multichannel Analyzer Display Screen Information. X is number of channels peak-to-peak. Y is the number of channels FWHM-full width half-maximum.

picoseconds added to the second input to the multichannel analyzer with the delay box and X is the number of channels peak-to-peak. Then, the jitter is

$$J = YZ \qquad \text{(VI-2)}$$

where J is the jitter in picoseconds and Y is the number of channels at the full width of the half-maximum points of the pulses displayed on the screen of the multichannel analyzer. When the jitter is divided by the time-delay, the percent jitter is

$$\% J = (100\%)J/TD \qquad \text{(VI-3)}$$

where TD is the pulse width of the circuit output time-delay pulse.

The second segment of the jitter test used the instrument setup shown in Figure VI-5, page 48. A negative-going pulse is transmitted from a pulse generator to a discriminator. The output of the discriminator is used to trigger the linear delay circuit. The positive-going L output of the linear delay circuit is fed into an oscilloscope. Also, a negative-going pulse from the pulse generator is fed into the oscilloscope at the external trigger input. The oscilloscope is adjusted so that the trailing edge of the pulse is displayed. The amount of jitter is determined by estimating the width, in time, of the trailing edge of the pulse at the midpoint of the negative excursion. The amount of jitter determined by this method is an estimate. The percent jitter is calculated using Equation (VI-3).

The jitter introduced by the test system was measured and found to be negligible compared to the jitter generated by the delay circuit. The results of the jitter tests are shown in Figure VI-10. The jitter was found to be less than 0.2%.

III. CIRCUIT OPERATING TIMES

The linear delay circuit operating times were measured by using an oscilloscope capable of displaying very fast rise and fall times. Two probes were used to observe the waveforms at two different points in the circuit. The two probes were identical so that the delay introduced by each probe would be equal.

The minimum output pulse width required for proper operation of the circuit is 4 nsec as shown in Figure VI-11. The circuit propagation delay is 8 nsec. The output pulse rise and fall times are approximately 2 nsec. The propagation delay of comparators IC4, IC5 and IC6 is 4 nsec. The propagation delay of comparator IC7 is 6 nsec. The propagation delay High to Low for NAND gate, IC2-A, is 3 nsec and the propagation delay Low to High is 2 nsec. The propagation delay High to Low for AND gate, IC2-B, is 3 nsec and the propagation delay Low to High is 1.5 nsec. The propagation delay for OR gate, IC1-A, is 3 nsec. The propagation delay Low to High for OR gate, IC1-B, is 3 nsec and the propagation delay High to Low is 1.5 nsec. The propagation delay High to Low for OR gate, IC2-A is 4 nsec and the propagation delay Low to High is 1.5 nsec. The propagation delay High to Low for NOR gate, IC3-B, is 3 nsec and the propagation delay Low to High is approximately 8 nsec. The propagation

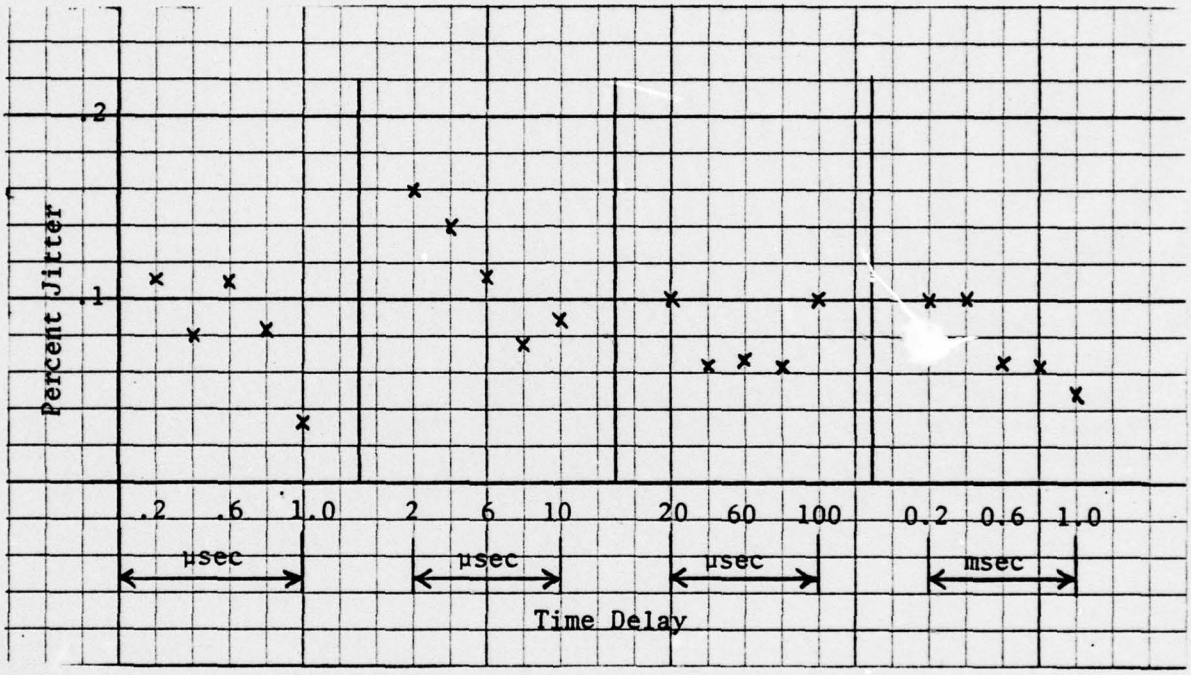


Figure VI-10. Percent Jitter as a Function of Time Delay.

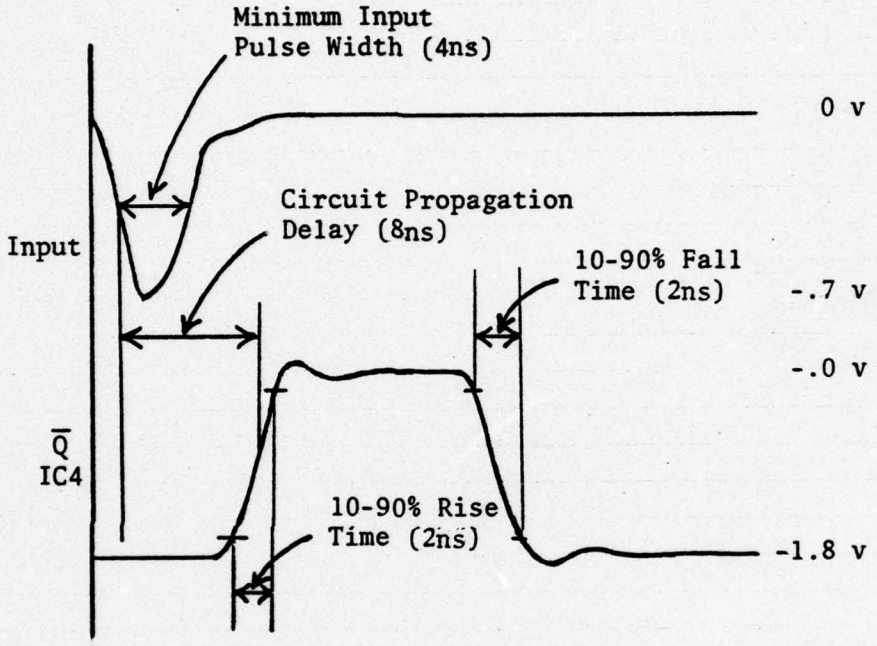


Figure VI-11. Input/Output Pulse Data.

delay High to Low for OR gate, IC3-C, is 9 nsec and the propagation delay Low to High is approximately 10 nsec. The complete timing cycle timing diagram with the various measured propagation delays is shown in Figure VI-12. The measured NIM output pulse operating times are shown in Figure VI-13.

The following is a list of the seven primary instruments used to test the circuit:

1. Hewlett-Packard Model 215A Pulse Generator.
2. Hewlett-Packard Model 1710A Oscilloscope.
3. ORTEC Model 6240 Multichannel Analyzer.
4. ORTEC Model 444 Gated Biased Amplifier.
5. ORTEC Model 425 Delay Module.
6. ORTEC Model 436 100 MHz Discriminator.
7. ORTEC Model 467 Time to Pulse Height Analyzer.

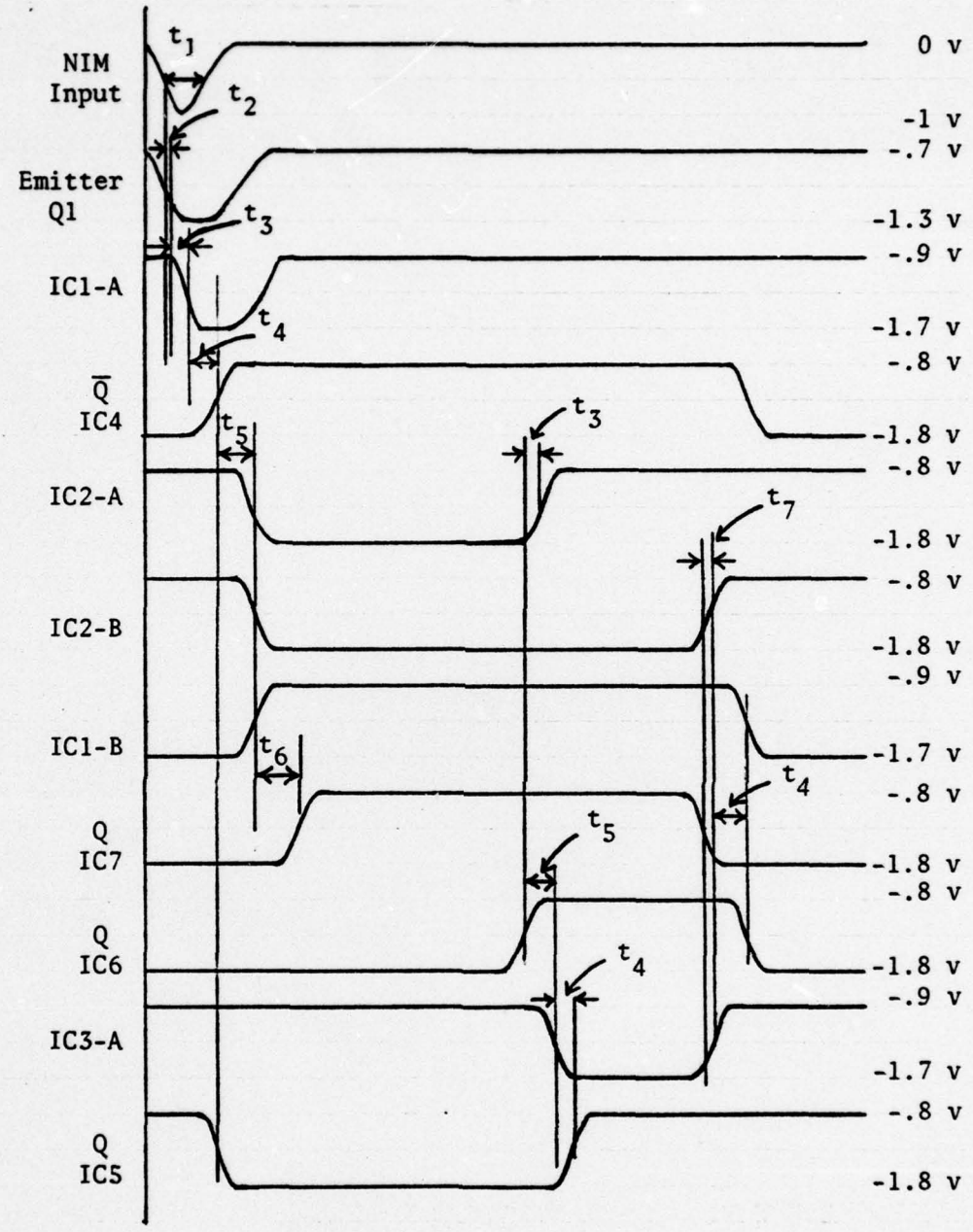


Figure VI-12. Timing Cycle Data. The times shown are as follows: t_1 = 7 ns, t_2 = 1 ns, t_3 = 2 ns, t_4 = 4 ns, t_5 = 3 ns, t_6 = 6 ns, and t_7 = 1.5 ns.

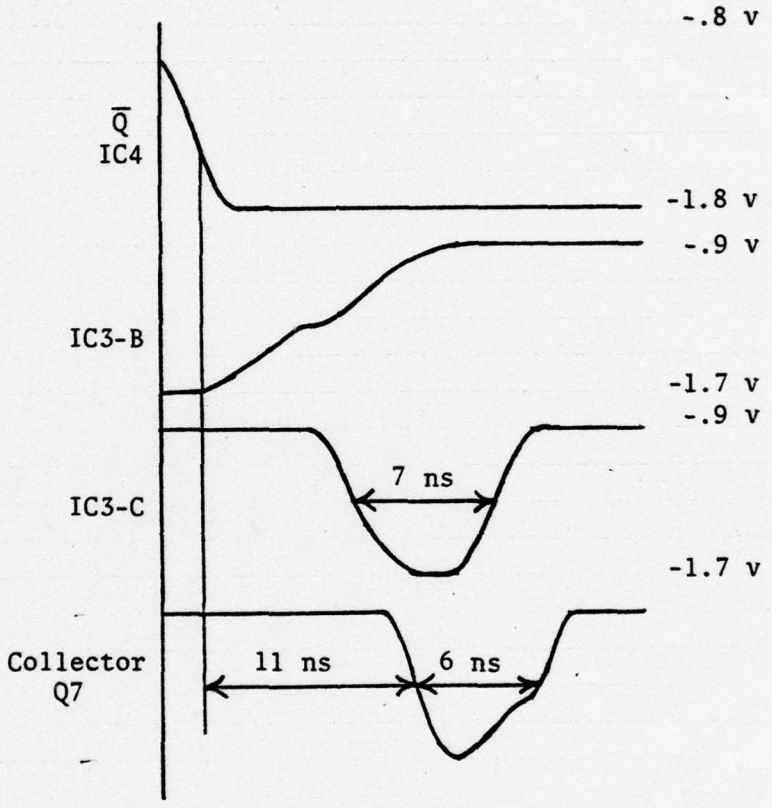


Figure VI-13. NIM Output Pulse.

CHAPTER VII

SUMMARY, CONCLUSIONS, AND SUGGESTIONS

An extensive literature review revealed that the study of a linear time-delay generator having ECL logic level outputs was warranted. The linear time-delay generator should have output pulse rise and fall times of approximately 2 nsec and a circuit propagation delay of 10 nsec or less. The time-delay generator should have a delay range linearity of less than 1%. Also, the jitter should be less than 0.5%. The objective of this study was to develop a circuit using ECL technology that would meet or exceed the above performance specifications. The development of equations to determine theoretical rise and fall times and also propagation delays was not attempted in this study. The attempt was not made because the parasitic effects of stray capacitances effectively limit the speed of very fast circuits. The stray capacitances vary significantly from one circuit layout to another. Thus, general equations for rise and fall times and also propagation delays would be superficial.

The timing cycle of the delay circuit was developed around the linear charge and discharge of a high quality capacitor by constant-current sources. New ECL logic gates and high-speed precision voltage comparators with extremely fast switching speeds were utilized to control the various functions in the timing cycle. The use of these high-speed devices greatly reduced the complexity of the circuit.

The linear delay circuit, as evidenced by the results in Chapter VI, performed as desired with one exception. The percent jitter of the

circuit was greater than desired, but not alarming for a bread-board model. A better layout on a printed circuit board could be expected to not only reduce the jitter but also decrease the rise times of the output pulses. The time delay generated as a function of the dial setting was very linear.

Computers and more accurate instrument systems will require a greater use of ECL circuits so that speed can be maximized. This study demonstrates only one of many possible applications of these high-speed devices. The increased demand for ECL devices will undoubtedly precipitate a reduction in prices, thus making them competitive pricewise with slower devices. Also, devices in many circuits will undoubtedly be replaced by ECL devices, since the ECL devices are far superior in their speed of operation.

However, ECL devices are still relatively new and have several peculiarities. Many studies similar to this one should be undertaken to explore the various assets and liabilities of these devices. These studies would make the transition from other devices to ECL devices more orderly and cost effective.

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LIST OF REFERENCES

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APPENDIXES

APPENDIX A

AM685 VOLTAGE COMPARATOR FUNCTIONAL INFORMATION

The AM685 is manufactured by Advanced Micro Devices, Inc., and is a very fast voltage comparator. The AM685 is manufactured with an advanced bipolar NPN, Schottky barrier diode high-frequency process that makes possible very short propagation delays (6.5 nsec) without sacrificing the excellent matching characteristics that previously were associated with the slow, high performance linear IC's. The circuit has differential analog inputs and complementary ECL logic compatible outputs. The output is suitable for driving terminated 50 ohm transmission lines, and the input has low offset voltages and currents. Thus, the AM685 is suited for high-speed applications.

The comparator has a latch function. If the latch enable input is High, the comparator functions normally, but if the latch enable is Low the comparator outputs are locked in their existing logical states. When the latch function is not used, the latch enable must be connected to ground.

There are four distinctive characteristics of the comparator, and are as follows:

1. 6.5 nsec maximum propagation time at 5 mv overdrive.
2. 3 nsec latch setup time.
3. Complementary ECL outputs.
4. 50 ohm line driving capability.

The basic functional diagram is shown in Figure A-1. The pin connection diagram is shown in Figure A-2.

The following is a list of the most important interconnection techniques that should be utilized to ensure that the maximum switching speeds are realized.

1. The impedance at the inputs should be as low as possible.
2. Lead lengths should be as short as possible.
3. The device should be soldered directly onto the printed circuit board instead of using a socket.
4. A ground plane must be provided for a good low inductance ground current return path.
4. Open wiring on the inputs should be limited to less than one inch.
5. The terminating resistor should be at the driven end.
6. The supply voltages should be well decoupled with RF capacitors connected to the ground plane as close to the device supply pins as possible

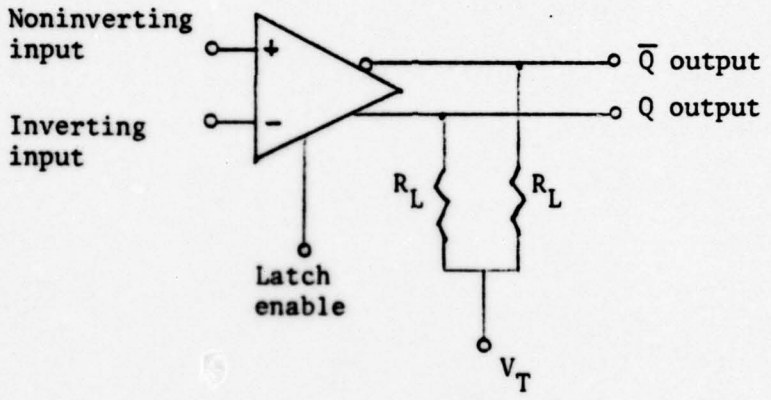

Figure A-1. AM685 Voltage Comparator Functional Diagram. The outputs are open emitters, therefore external pull down resistors are required. These resistors may be in the range of 50-200 ohm connected to -2.0 volts, or 200-2000 ohm connected to -5.2 volts. V_T is the output load terminating voltage. R_L is the output load resistance.

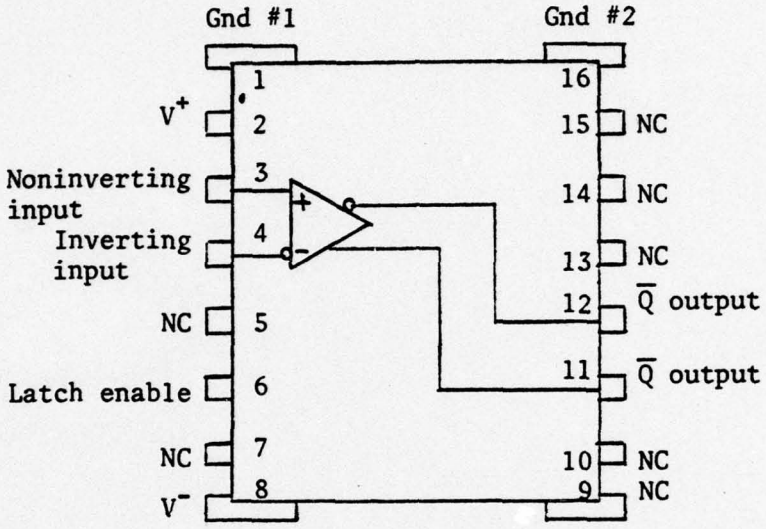

Figure A-2. AM685 Voltage Comparator Pin Connection Diagram. Unused outputs are grounded through 50 ohms.

Source: Advanced Micro Devices Data Book, Advanced Micro Devices, Inc., 1974.

APPENDIX B

AM685 VOLTAGE COMPARATOR CIRCUIT DESIGN

Simplicity is the most important consideration in designing wideband circuitry. There are three primary objectives that must be obtained to achieve simplicity.

1. The fewest possible number of active devices in the signal path.
2. The lowest possible impedance levels.
3. The lowest possible capacitance.

A simple, common-emitter differential amplifier can be designed to meet the objectives with one major exception: the shunting effect of the source impedance is multiplied by the voltage gain of the stage (the Miller effect). A solution is to add an additional pair of common-base transistors to form a differential cascode amplifier, as is shown in Figure B-1. The circuit now has the performance features of a common-emitter amplifier without feedback capacitance. However, circuitry now has to be added to bias the cascode transistors.

The signal at the output of the cascode must be shifted down to a lower voltage to drive the inputs of the second stage. The use of PNP transistors would degrade the frequency response. Three possibilities exist:

1. A chain of forward-biased diodes.
2. A programmed voltage drop across a resistor.
3. A zener diode.

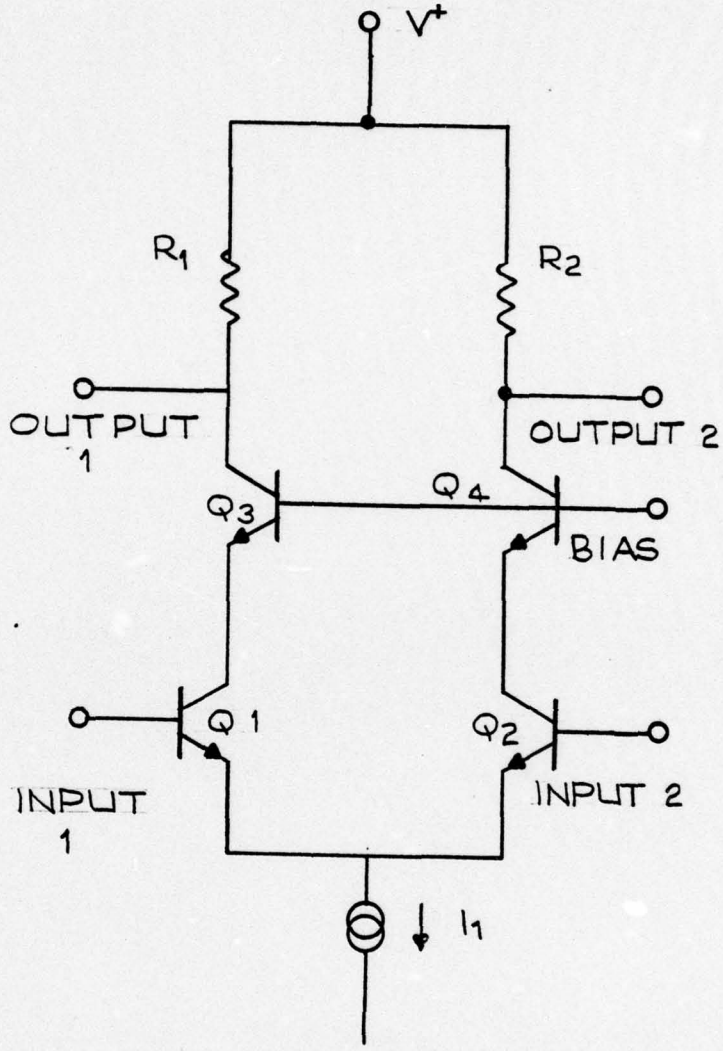

Figure B-1. Differential Cascode Amplifier.

Source: Advanced Micro Devices Data Book, Advanced Micro Devices, Inc., 1977, pp. 8-46-49.

The zener diode is superior for high-frequency applications because of the low shunt capacitance to ground. The zener diodes must be closely matched to ensure low offset voltages at the inputs.

The zener diodes are buffered from the cascode transistors by emitter followers, as shown in Figure B-2. The pull down current through the zener-follower combination must be large enough to discharge the node capacitance when the emitter follower swings in the negative direction. The minimum value of current is determined by the node capacitance, the signal swing and the amount of delay that can be tolerated. The signal swing is reduced by the addition of Schottky clamping diodes across the collectors of the cascode. The use of the Schottky diodes allows the cascode transistors to be biased closer to the positive supply without fear of saturation at the extremes of the signal swing.

The design of the output stage varies little from that of a standard ECL gate. The output gate is shown in Figure B-3. The output emitter follower is able to handle 50 ohm transmission line loading and doesn't have much capacitance. A current source is used to supply the emitters of the stage, rather than the normal resistor to the negative supply. The current source provides the correct logical "1" and "0" levels at the output. The propagation delays to either output of the gate are equal, whereas in the standard ECL gate they are slightly different. The difference in the ECL gates is due to additional capacitive loading on the $\overline{Q}$ output caused by multiple input transistors.

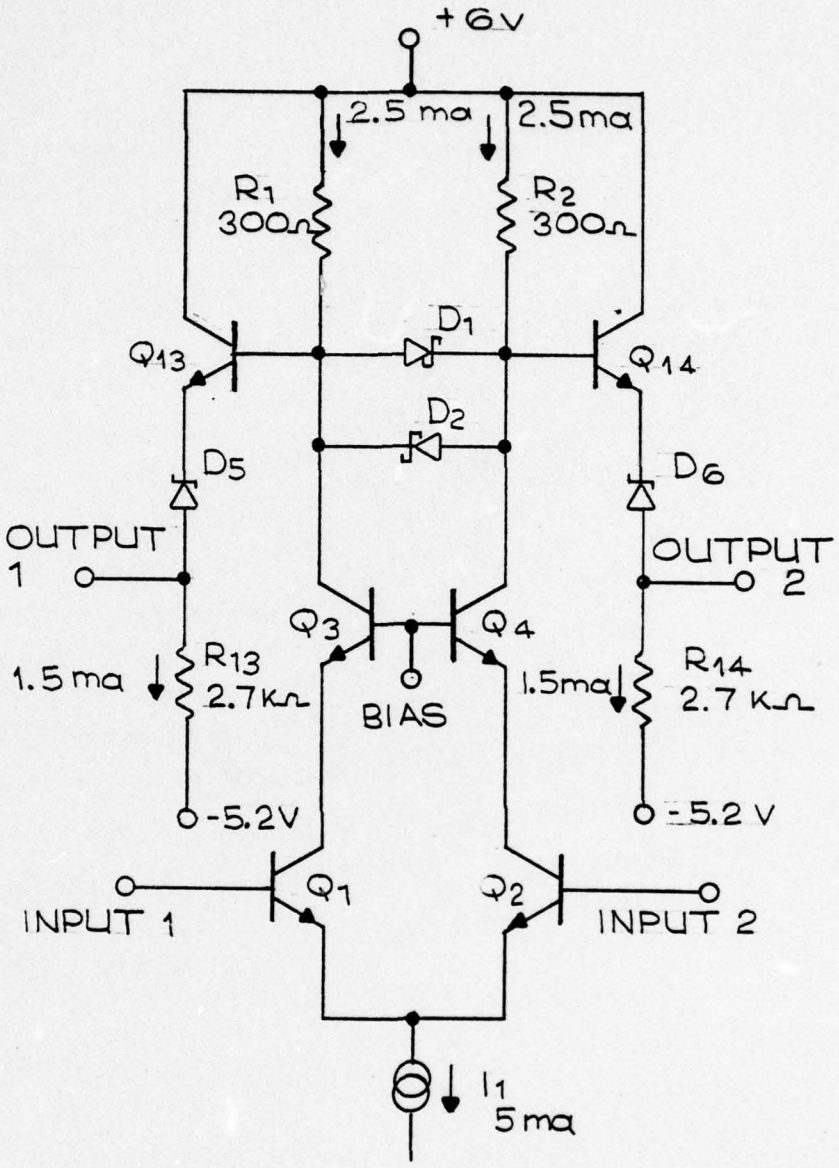

Figure B-2. Basic Cascode Gain Stage.

Source: Advanced Micro Devices Data Book, Advanced Micro Devices, Inc., 1977, pp. 8-46-49.

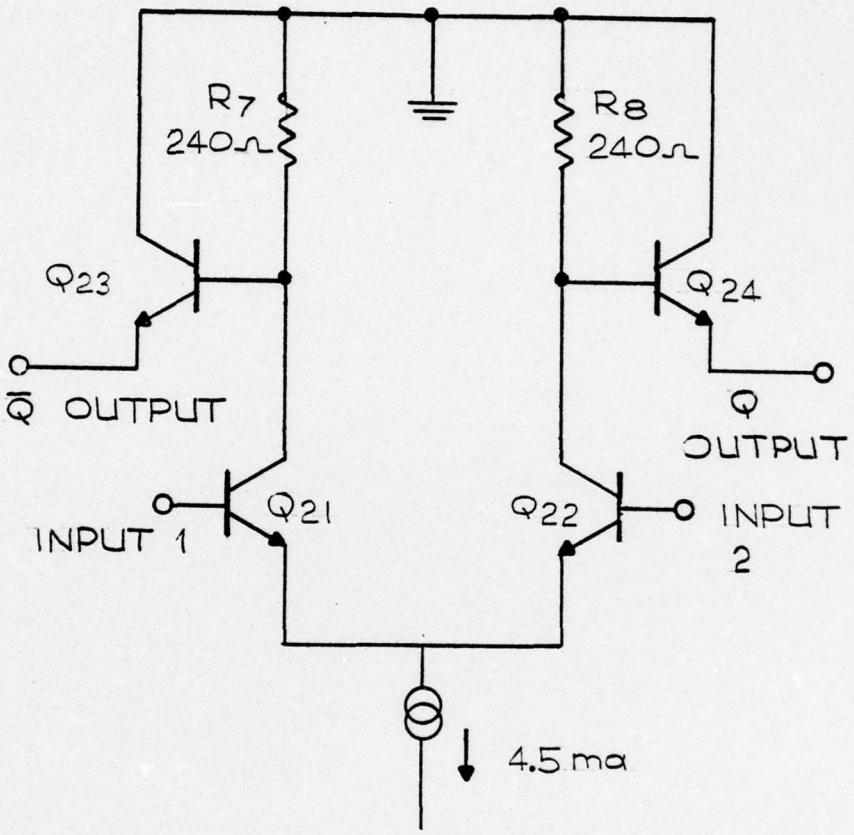

Figure B-3. Output Gate.

Source: Advanced Micro Devices Data Book, Advanced Micro Devices, Inc., 1977, pp. 8-46-49.

The latch function is accomplished without interfering with the normal operation of the comparator and without degrading speed. Also, it is as close to the input as possible so that short signals can be acquired and held. A simple method of adding a latch to a differential amplifier is shown in Figure B-4. A pair of transistors, Q5 and Q6, are cross-coupled at the collector of the input transistors, Q1 and Q2. Current source I2 is switched on when the latch is desired. If I2 is larger than I1, the positive feedback via Q5 and Q6 holds the circuit in the state it was in when latched.

The circuit of Figure B-4 is not the best for speed due to the added capacitance of Q5 and Q6. However, the circuit can be adapted to the cascode stage easily. The addition of the latch circuit to the cascode stage is shown in Figure B-5. Drive for Q5 and Q6 is taken from the level shifter with the collectors at the emitters of the cascode. The current source is switched by the differential amplifier, Q9 and Q10, which is referenced to the ECL logic threshold voltage. The latch enable can now be driven from a standard ECL gate. The latch enable time is very fast since only currents are being switched.

The latch current source must be 1 mA greater than the input current source to ensure proper latching. With 5 mA in the input stage, at least 6 mA is required to power the latch. Transistors Q7 and Q8 are added to reduce power consumption by cutting the latch stand-by power to zero. The addition of Q7 and Q8 is shown in Figures B-6 and B-7.

Transistors Q7 and Q8 function as if they are connected in parallel with Q1 and Q2 as far as the net effect at the collector load resistors is

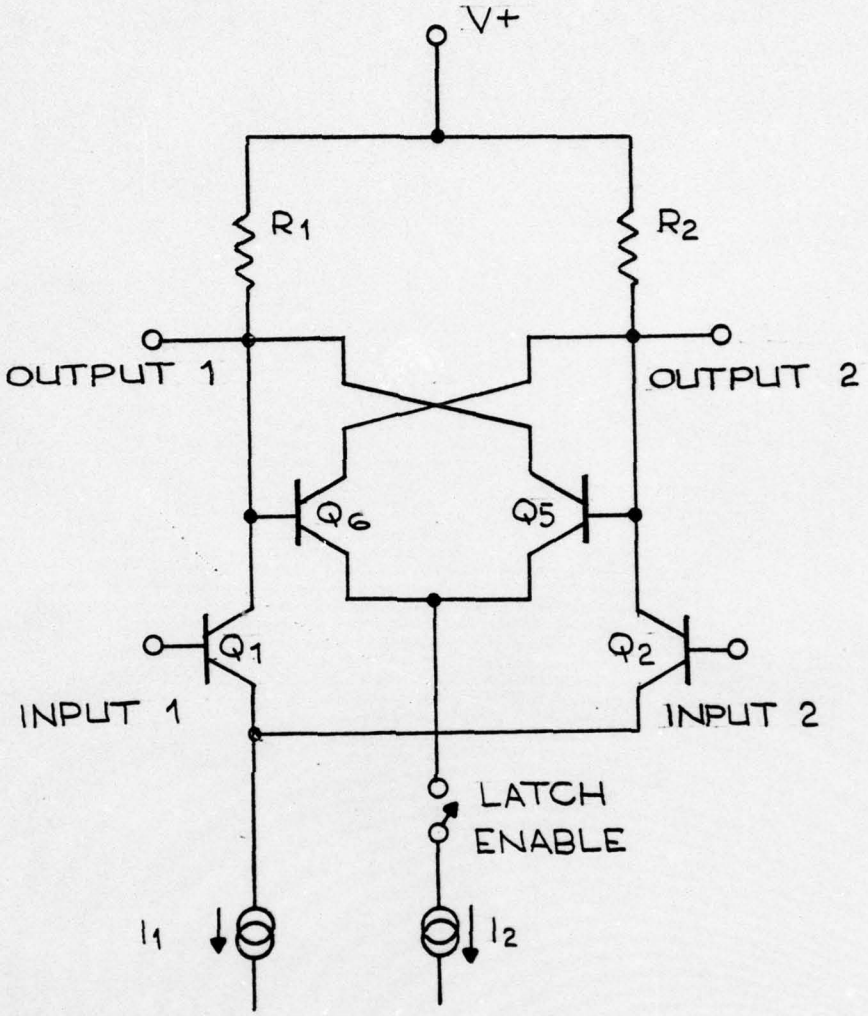

Figure B-4. Simple Latch Circuit.

Source: Advanced Micro Devices Data Book, Advanced Micro Devices, Inc., 1977, pp. 8-46-49.

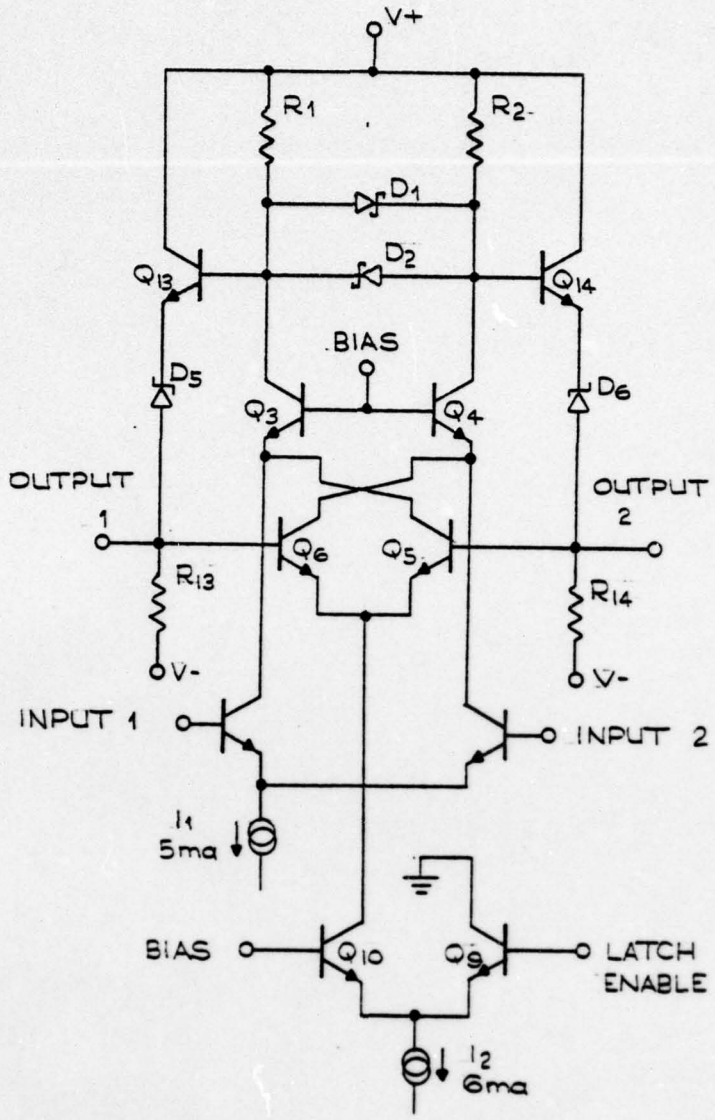

Figure B-5. Cascode with Latch.

Source: Advanced Micro Devices Data Book, Advanced Micro Devices, Inc., 1977, pp. 8-46-49.

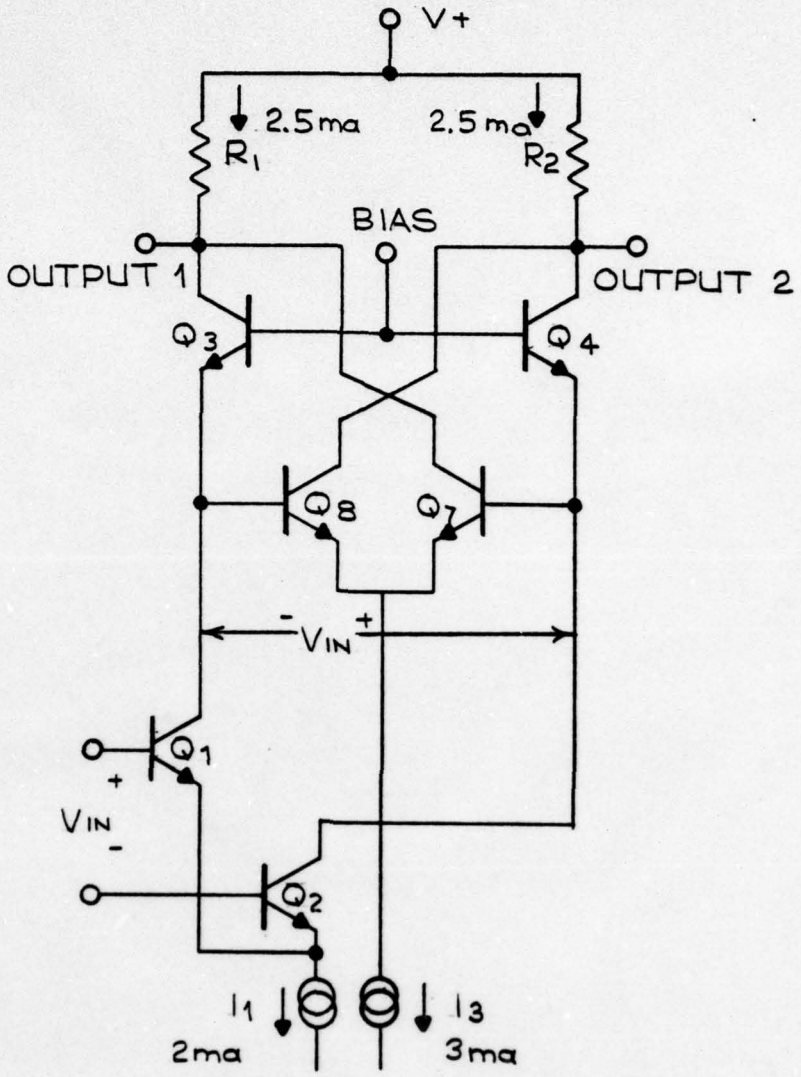

Figure B-6. Cascode with Parallel Transistors.

Source: Advanced Micro Devices Data Book, Advanced Micro Devices, Inc., 1977, pp. 8-46-49.

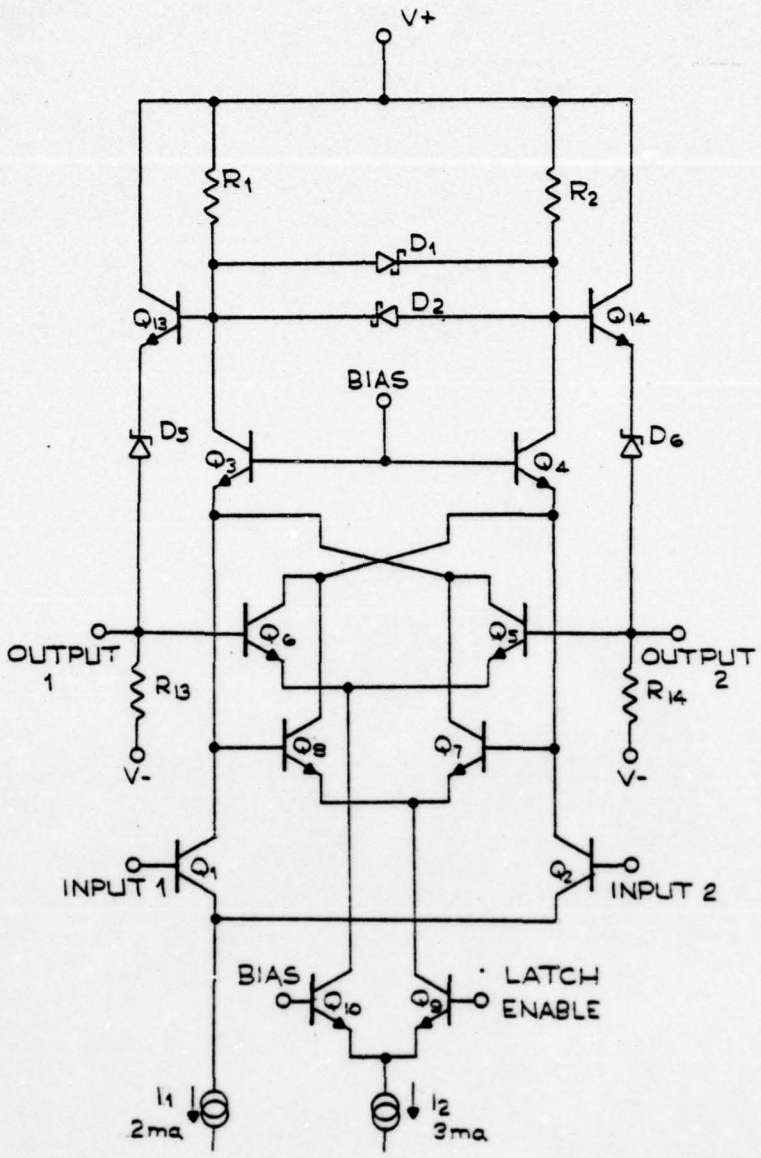

Figure B-7. Complete Input Cascode Stage with Latch.

Source: Advanced Micro Devices Data Book, Advanced Micro Devices, Inc., 1977, pp. 8-46-49.

is concerned. To obtain the desired total stage gain, I1 can be 2 mA and I2 can be 3 mA. With the latch enable in the High state, Q9 will be on and 3 mA supplied to Q7 and Q8. The comparator functions normally with no current being used in the latch. When the latch enable goes to the Low state, Q10 comes on, robbing 3 mA from the gain stage and giving it to the latch. The latch current is now 1 mA greater than the input stage current, but the total current is only 5 mA.

The complete circuit diagram for the comparator is shown in Figure B-8. This diagram includes additional refinements and dc biasing. The dc bias chain causes the output logic levels to track those of other ECL circuits connected to the same negative supply. The achieved design objectives for the high-speed precision comparator are as follows:

1. Propagation delay less than 10 nsec measured at a 100 mV input step, with 5 mV overdrive.
2. ECL-compatible outputs.
3. Latch capability.
4. A gain of greater than 1600.
5. An input offset voltage of less than ± 2 mV.
6. A common-mode range of greater than ± 3 V.

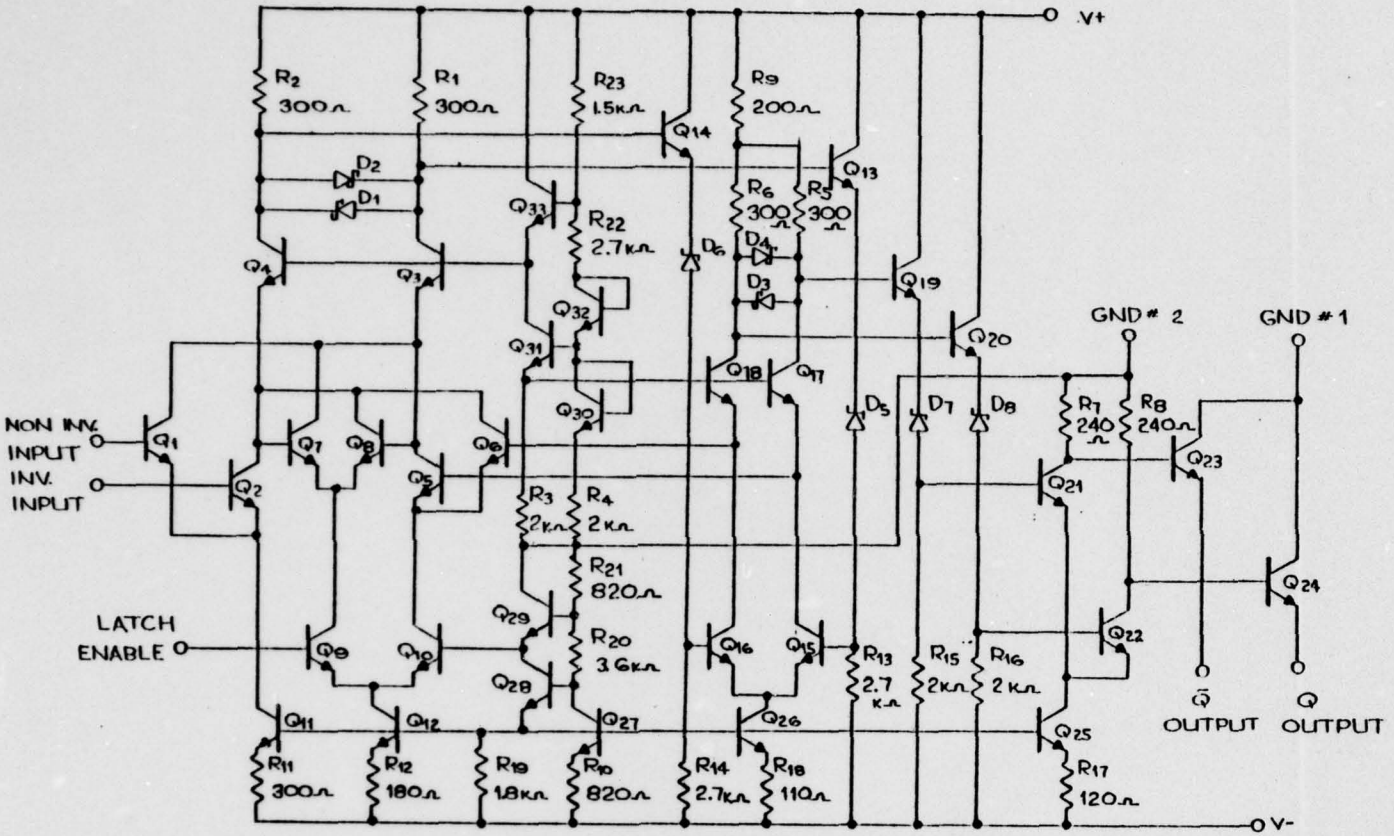

Figure B-8. Complete Schematic of the AM685 Comparator.

Source: Advanced Micro Devices Data Book, Advanced Micro Devices, Inc., 1977, pp. 8-46-49.

APPENDIX C

MECL INTEGRATED CIRCUIT INFORMATION

There are only two types of standard high-speed logic integrated circuits commonly available: Schottky-clamped TTL logic (TTL-S) and nonsaturating emitter-coupled logic (ECL).

The conventional TTL logic is a saturated form of logic. This means that during turn-on the emitter-base and the collector-base junction of a transistor are forward biased. This action causes an accumulation of charged carriers in the base regions. When the transistor turns off, this accumulation of charge must discharge through the collector. The finite time required for this charge to dissipate causes a delay in turning the transistor off. This storage-time delay is inherent in all saturated logic forms.

The Schottky-clamped TTL logic is similar to conventional TTL logic in its circuit configuration and operating characteristics. However, the Schottky-clamped TTL logic reduces the storage time by means of Schottky-diodes between the base-collector junctions. These diodes tend to keep the transistor out of saturation, but they also tend to increase the input capacitance of the TTL-S. Thus, TTL-S is faster than TTL due to the reduction of the charge storage time. However, the increase in speed is limited by the RC time constant of the transistor input.

Emitter-coupler logic completely avoids the transistor charge storage time by being nonsaturating in design. Gate delays of less than a nanosecond are currently feasible. The complementary outputs common

to ECL logic gates cause the normal function and its complement to appear simultaneously at the outputs. The complementary outputs are achieved without the use of external inverters. Timing differential problems that arise from time delays introduced by inverters are reduced. Also, system power requirements are reduced. Therefore, the choice of ECL logic devices for use in high-speed circuitry is well justified.

The MECL integrated circuit device MC10104 used in the linear. time-delay circuit provides low power, high-speed AND and NAND logic functions. High impedance pulldown resistors eliminate the need to tie unused inputs to an external supply and allow high dc and ac Outputs should be terminated through 51 ohm resistors to -2.0 volts. The pin connection diagram for the MC10104 is shown in Figure C-1.

The MECL integrated circuit device MC10105 used in the linear, time-delay circuit is a triple 2-3-2 OR/NOR, high-speed gate. Input pulldown resistors eliminate the need to tie unused inputs to an expernal supply. Outputs should be terminated through 51 ohm resistors to -2.0 volts. The pin connection diagram for the MC10105 is shown in Figure C-2.

A circuit diagram of the MC10104 is shown in Figure C-3. A circuit diagram of the MC10105 is shown in Figure C-4.

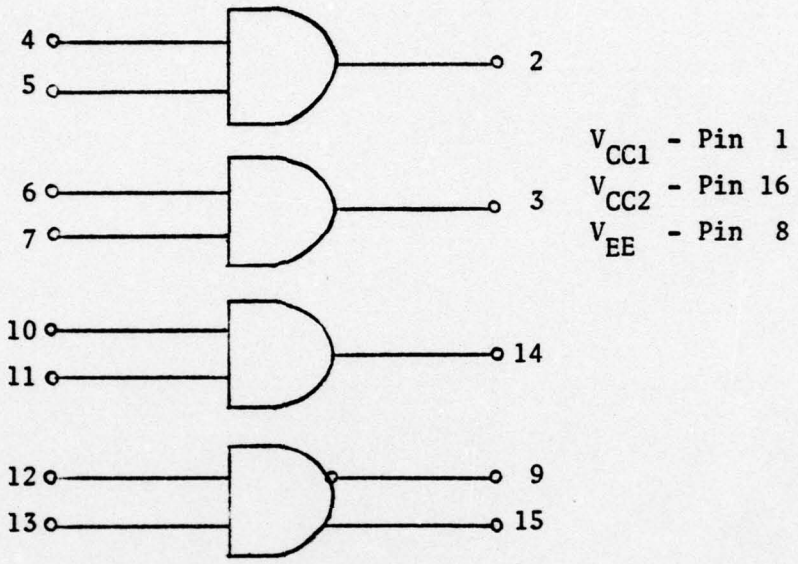

Figure C-1. MC10104 Pin Connection Diagram. All unused outputs connected to a 51 ohm resistor to ground.

Source: MECL Integrated Circuit Data Book, 3rd Edition, Motorola Inc., 1973.

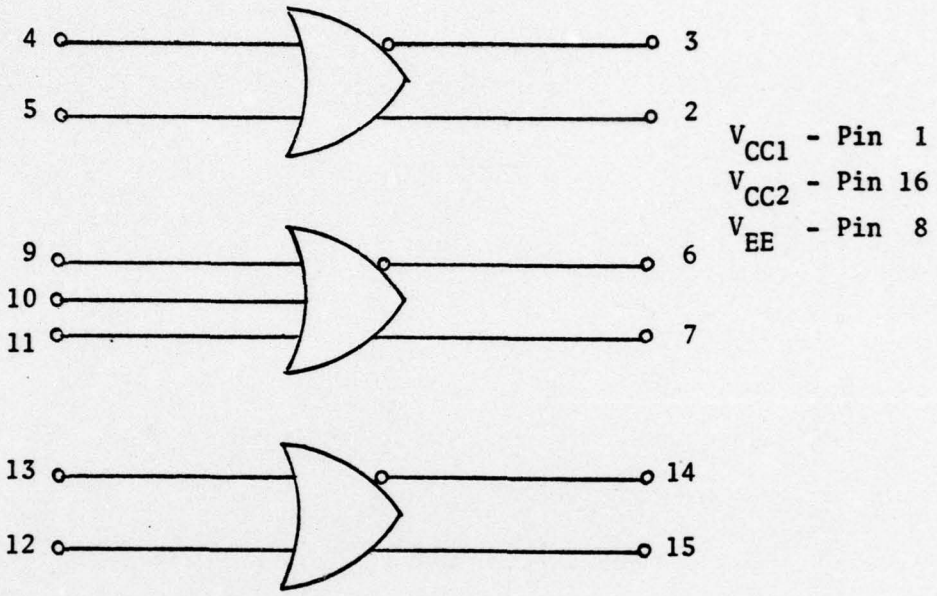

Figure C-2. MC10105 Pin Connection Diagram. All unused outputs connected to 51 ohm resistors to ground.

Source: MECL Integrated Circuit Data Book, 3rd Edition, Motorola Inc., 1973.

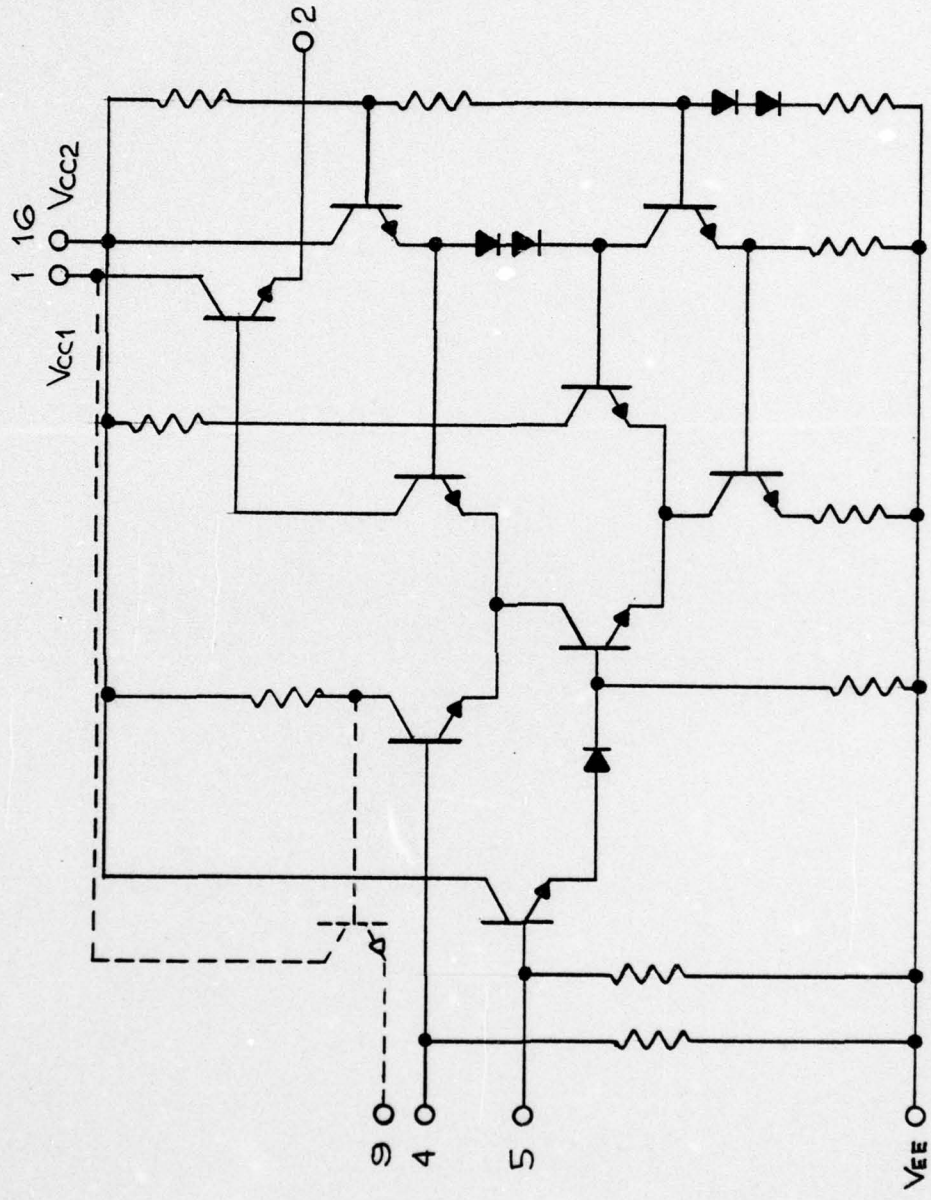

Figure C-3. Circuit Diagram for MECL MC10104. AND/NAND Gate. One-Fourth of Circuit Shown.

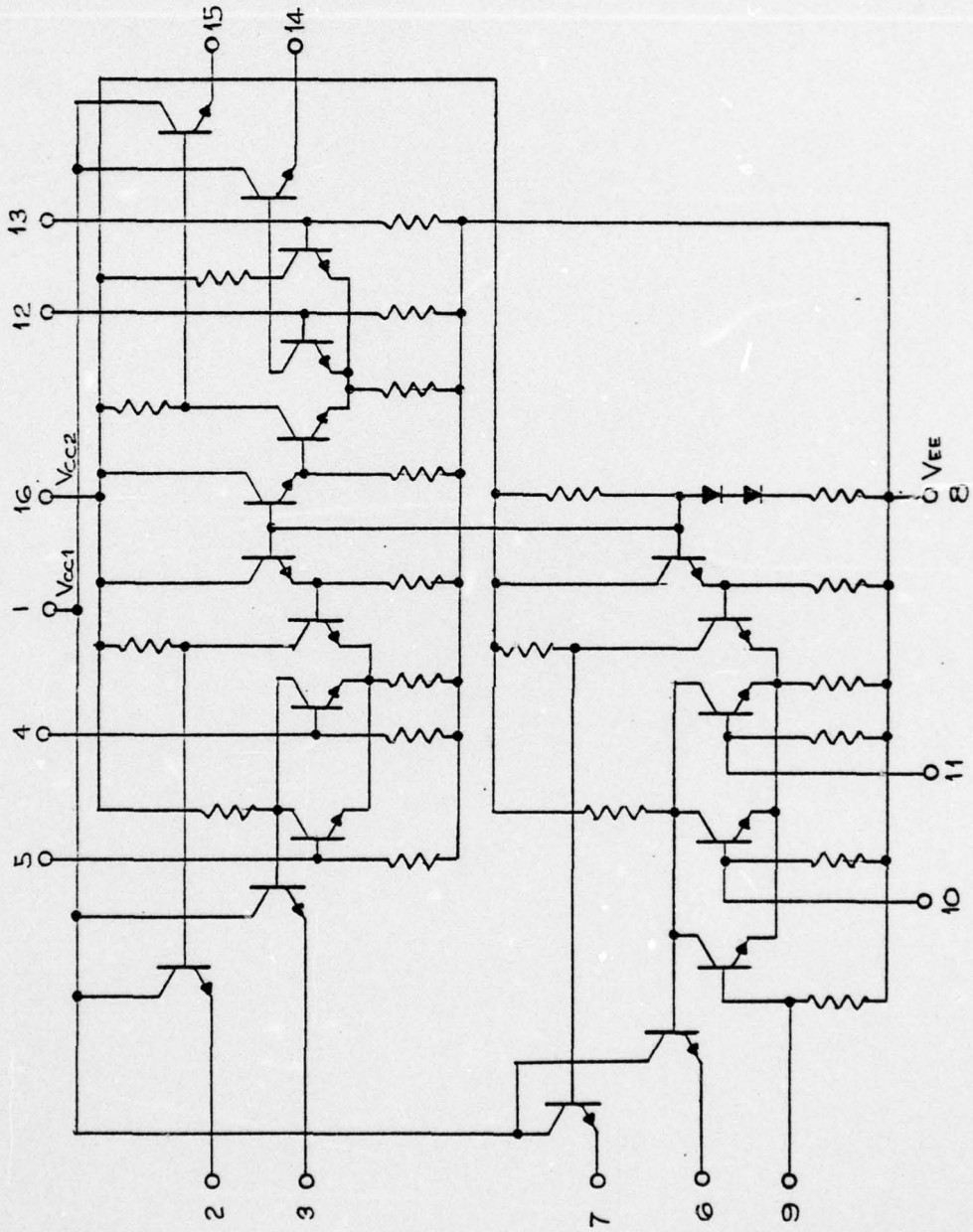

Figure C-4. Circuit Diagram for MECL MC10105. OR/NOR Gate.

VITA

Karle L. Severson was born in Barnesville, Minnesota, on August 18, 1946. He attended elementary school in that city and was graduated from Barnesville High School in May 1964. The following September he entered North Dakota State University on an athletic scholarship, track and cross-country. In December 1968 he received a Bachelor of Science degree in mechanical engineering and was commissioned a 2nd Lt. in the Signal Corps of the U.S. Army. From December 1968 until June 1969, he was employed at the Veterans Administration Center in Fargo, N.D., in an Engineer Trainee program.

He entered active duty with the U.S. Army in June 1969 and has become a career Army officer, presently holding the rank of Captain. In addition to duty in the continental United States, he has served three years in Germany and two years in Korea.

He entered the Graduate School of The University of Tennessee, Knoxville, in January 1976 on a U.S. Army fully sponsored program. He received the Master of Science degree with a major in electrical engineering in December 1977.

The author is an alumni of Sigma Phi Delta, a professional engineering fraternity. Captain Severson's next assignment in the U.S. Army will be with the Research and Development Laboratories of the U.S. Army Electronics Command, at Fort Monmouth, New Jersey.

He is married to the former Diane Jensrud of Fertile, Minnesota, and is the father of three children (Jon, Dawn, and James).

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