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THERMAL CHARACTERISTICS OF HYBRID CIRCUITS.(U)
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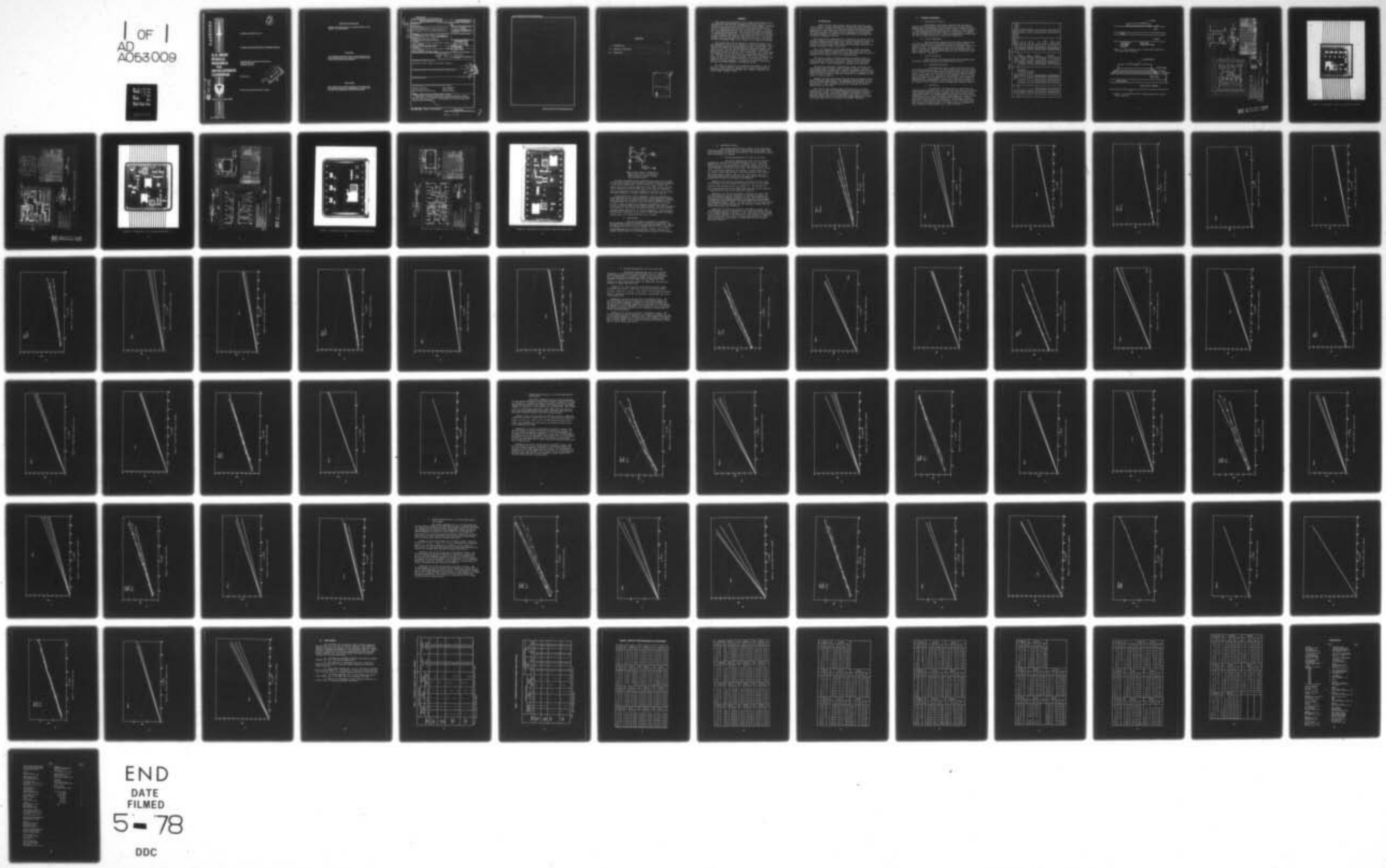

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U.S. ARMY MISSILE RESEARCH AND DEVELOPMENT COMMAND

Redstone Arsenal, Alabama 35809

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THERMAL CHARACTERISTICS OF HYBRID CIRCUITS

Advanced Systems Development and Manufacturing
Technology Directorate
Engineering Laboratory

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20. ABSTRACT (*Continue on reverse side if necessary and identify by block number*)

This report presents an evaluation of thermal resistance in hybrid microelectronics. Four different package types were used with and without multiple layer thick circuitry. Chip components were attached using both epoxy and eutectic methods.

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CONTENTS

SUMMARY

This report is an evaluation of the thermal characteristics of several different microelectronic packages and assembly techniques. The packages are of the flat pack and double-dual in-line design. The mounting of the semiconductor die is done with the standard gold-silicon eutectic technique and with the use of a gold filled epoxy. The influence of an additional dielectric and gold conductor layer was compared to a simple gold metallization. The substrate attachment was performed by epoxy mounting using either a silver filled resin (H-417) or an electrically insulative and thermally conductive epoxy (H-74). The thermal impedance from the junction to the case and the junction to the static air with the package plugged into a socket of a p-c board was evaluated.

The recorded data were the ambient air temperature (preset), the case temperature, and the power necessary to raise the junction to 175°C. The data were graphed as the temperature difference versus power. The slope of the graph is the thermal impedance expressed in degrees centigrade per Watt. The data were recorded for any offsets due to self-heating and averaged to constant value if applicable. The thermal impedance expressed as a constant for each of the packaged types of 3/4- and 1-in. flat packs and 16- and 24-pin double-dual in-line packages is given for each of the assembly techniques. The greater the thermal path length and the lower the thermal conductivity of the material, the greater the thermal impedance. The larger the package's surface area, the lower the thermal impedance from junction to air.

The report is intended to be an empirical development of the subject for a selected group of variables and therefore correlated by a comparison matrix indicating packages type, assembly techniques, and actual thermal impedance values.

I. INTRODUCTION

Modern military system designs require high-reliability electronic circuits. Present techniques for insuring that these requirements are met include the limitation of maximum allowable semiconductor junction temperatures to some value lower than that specified by the manufacturer. With the increasing use of hybrid circuit technology in these systems, the hybrid designer is charged with the responsibility of insuring that reliability requirements are met.

Operating junction temperatures are a function of the device and its package. Thermal resistance values for discrete semiconductor devices can be readily determined from simple tests. However, thermal resistance figures for various hybrid circuit fabrication techniques, materials, and packages have been, at best, a gray area.

Due to the uniqueness of most hybrid designs, thermal resistance data and maximum junction temperatures to be experienced could only be estimated within ±20% from tables of thermal conductivity for the materials involved and data sheets of the active components used.

This report provides information needed by the hybrid designer in order to make calculations to within ±5%, thereby allowing intelligent design tradeoffs to be made with respect to materials and fabrication techniques. Thus, costly overdesigns or redesigns can be minimized.

The study was undertaken to determine the thermal resistance variations brought about by several common assembly techniques. Variables investigated include package styles, substrate attachment materials, chip bonding techniques, and multilayer circuitry (typical of analog circuitry). Thick film test circuits were specially fabricated for measurement of the effects of these variables.

Thermal resistance calculations were made using strategically placed power dissipating semiconductors and temperature sensors inside the hermetically sealed hybrid packages. New techniques for measuring junction temperature of a power dissipating device were developed and used to generate data for the study.

Test results show comparable detailed thermal data for various assembly plans in light of the maximum junction temperature allowed in a hybrid circuit design. Measurement techniques are discussed in detail such that further study can be accomplished by the reader in order to generate thermal data for his own particular hybrid application, including package types, specific materials, and assembly techniques.

II. TECHNICAL DISCUSSION

A. Experimental Procedure

This section of the report identifies the technique by which the thermal impedance data were generated for the four different package types. The circuits were built with standard assembly techniques, the data were derived by maintaining the test chamber at a given temperature and supplying sufficient power (Watts) to the package to stabilize the junction temperature at 175°C. The case temperature was recorded when the total package configuration stabilized in temperature.

B. Circuit Preparation

The circuits were prepared with the typical manufacturing and assembly techniques used throughout the hybrid microelectronic industry. Figures 1 and 2 present the typical cross-sectional views of the hybrid circuits. The thicknesses are also listed in Figures 1 and 2. Table 1 indicates the package bonding types and corresponding serial numbers of the circuits. The assembly drawing and view of the circuits are shown in Figures 3 through 10.

C. Circuit Evaluation

This section of the report describes the techniques which were used to measure and analyze the manufactured circuits.

1. Measurement Technique

The transistors used for power dissipators were used with constant current sources. The zener diodes and all resistors needed for the constant current sources were outside the hybrid and were discrete parts. In this way, the only device dissipating power inside the hybrid was the device under test. In addition, the calibration current was kept small with respect to the capability of the particular chip to minimize heating effects. Where possible, silicon diodes were used to verify and measure substrate temperature at various points and were calibrated, in this case, at 1 mA. A typical circuit configuration is shown in Figure 11.

2. Calibration

The junction to be used (sensor or dissipator) was calibrated before the power run. All transistors were set up with constant current sources using the same base voltage as was used for actual tests. A test chamber which was nitrogen cooled and electric heated was used for temperature control. An iron/constantan thermocouple, in intimate contact with the bottom of the header, monitored header temperature; a similar thermocouple monitored the oven temperature. The reference junction was mounted in a large aluminum block maintained at 72°F. The thermocouples were initially calibrated against a lab standard digital thermometer and were periodically checked during the running of the tests.

TABLE 1. SAMPLE DESIGN

Serial No.	Package Type	Substrate Design	Bonding Techniques	
			Die Attach	Substrate Bond
H 215-3	3/4-in. Flat Pack	Single layer	Eutectic	H-417
H 215-4	3/4-in. Flat Pack	Single layer	Epoxy (A41)	H-417
H 215-1	3/4-in. Flat Pack	Multilayer	Eutectic	H-417
H 215-2	3/4-in. Flat Pack	Multilayer	Epoxy (H41)	H-417
H 214-3	1-in. Flat Pack	Single layer	Eutectic	H-417
H 214-4	1-in. Flat Pack	Single layer	Epoxy (H41)	H-417
H 214-1	1-in. Flat Pack	Multilayer	Eutectic	H-417
H 214-2	1-in. Flat Pack	Multilayer	Epoxy (H41)	H-417
H 217-3A	16-Pin DDIL	Single layer	Eutectic	H-74
H 217-3B	16-Pin DDIL	Single layer	Eutectic	H-417
H 217-4A	16-Pin DDIL	Single layer	Epoxy (H41)	H-74
H 217-1A	16-Pin DDIL	Multilayer	Eutectic	H-74
H 217-1A	16-Pin DDIL	Multilayer	Eutectic	H-417
H 217-2B	16-Pin DDIL	Multilayer	Epoxy (H-41)	H-74
H 217-2B	16-Pin DDIL	Multilayer	Epoxy (H-41)	H-417
H 216-3A	24-Pin DDIL	Single layer	Eutectic	H-74
H 216-3B	24-Pin DDIL	Single layer	Eutectic	H-417
H 216-4A	24-Pin DDIL	Single layer	Epoxy (H41)	H-74
H 216-4B	24-Pin DDIL	Single layer	Epoxy (H41)	H-417
H 216-1B	24-Pin DDIL	Multilayer	Eutectic	H-417
H 216-2A	24-Pin DDIL	Multilayer	Epoxy (H41)	H-74
H 216-2B	24-Pin DDIL	Multilayer	Epoxy (H41)	H-417

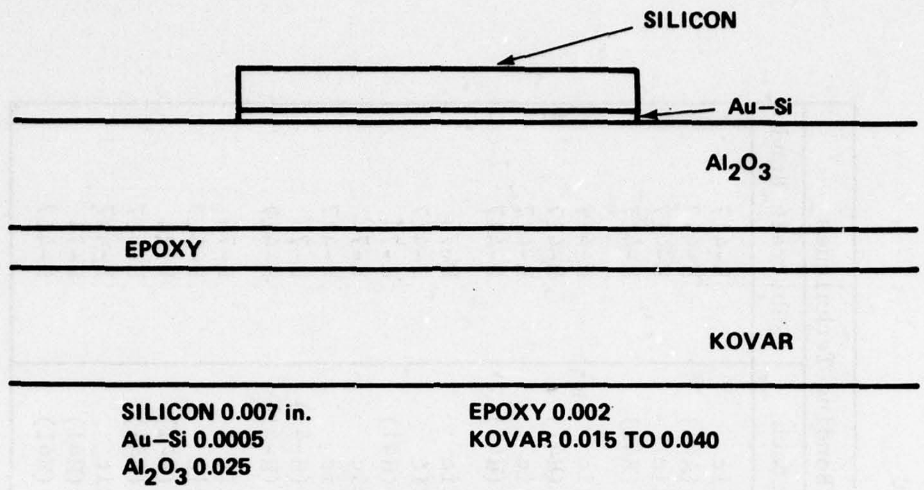


Figure 1. Cross-sectional view of eutectically mounted die on single layer substrate.

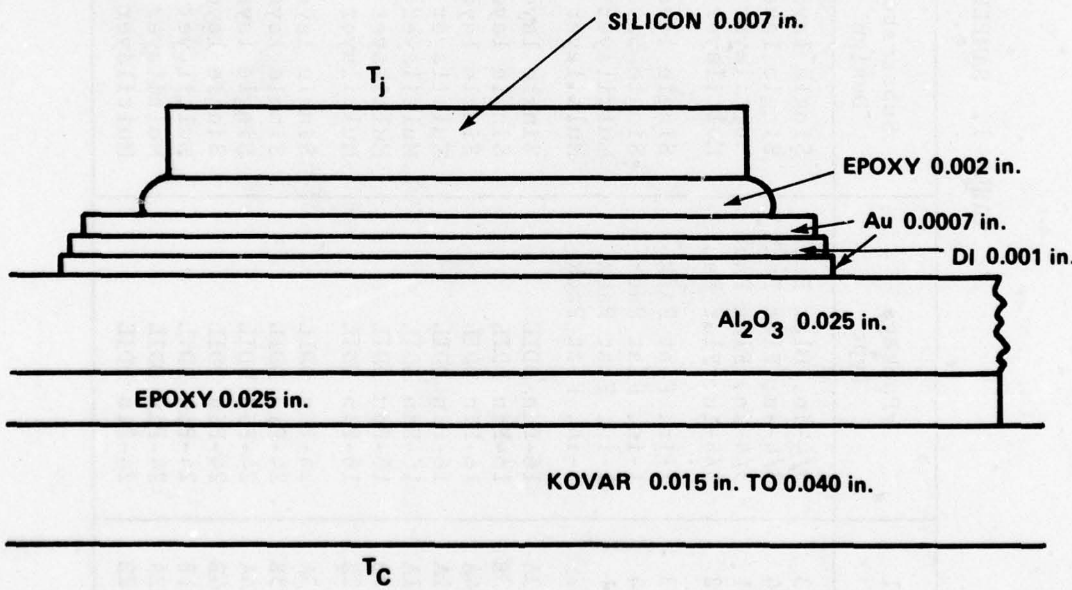


Figure 2. Cross-sectional view of epoxy mounted die on multi-layer substrate.

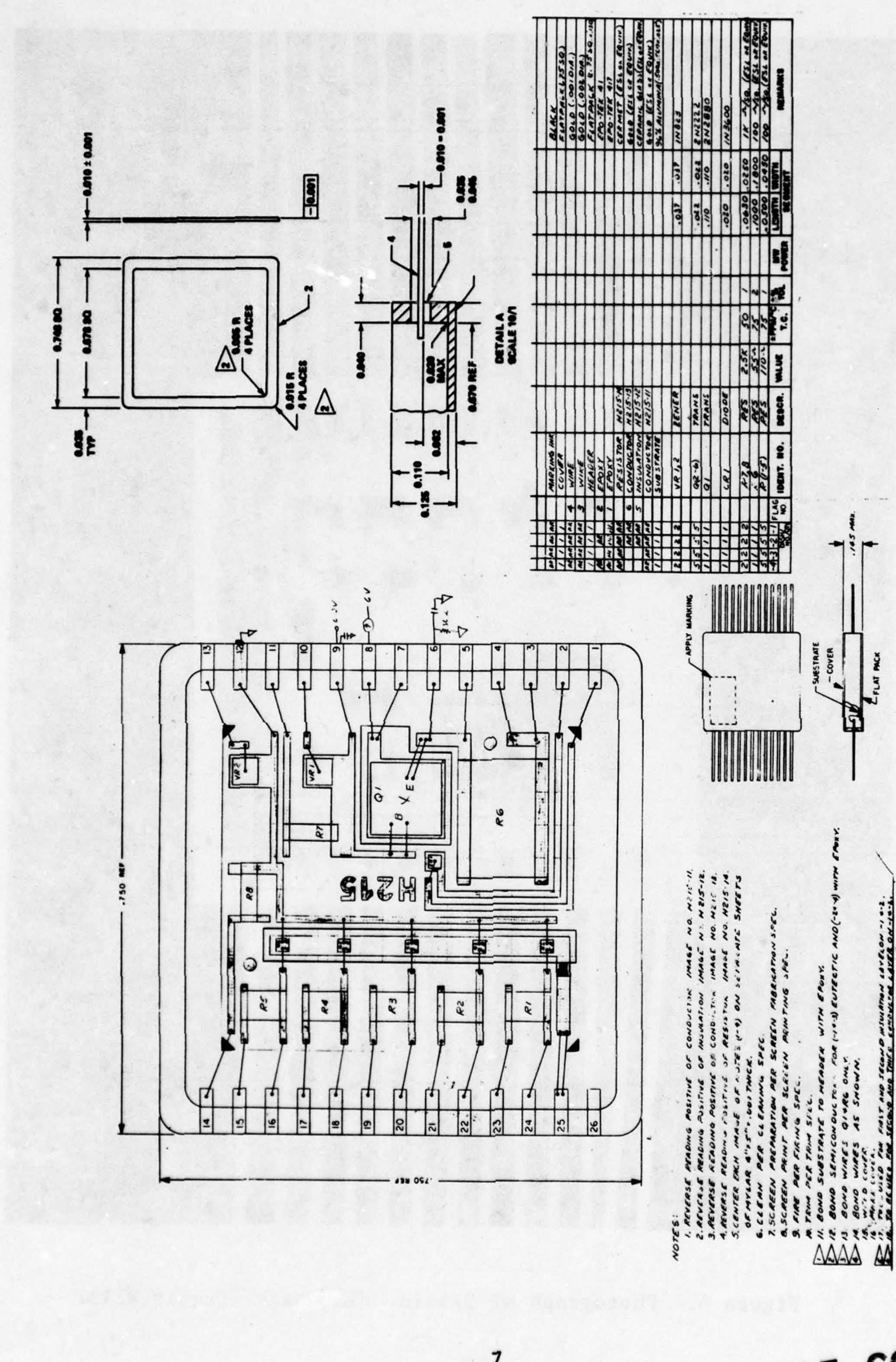


Figure 3. Assembly drawing of 3/4-in. flat pack.

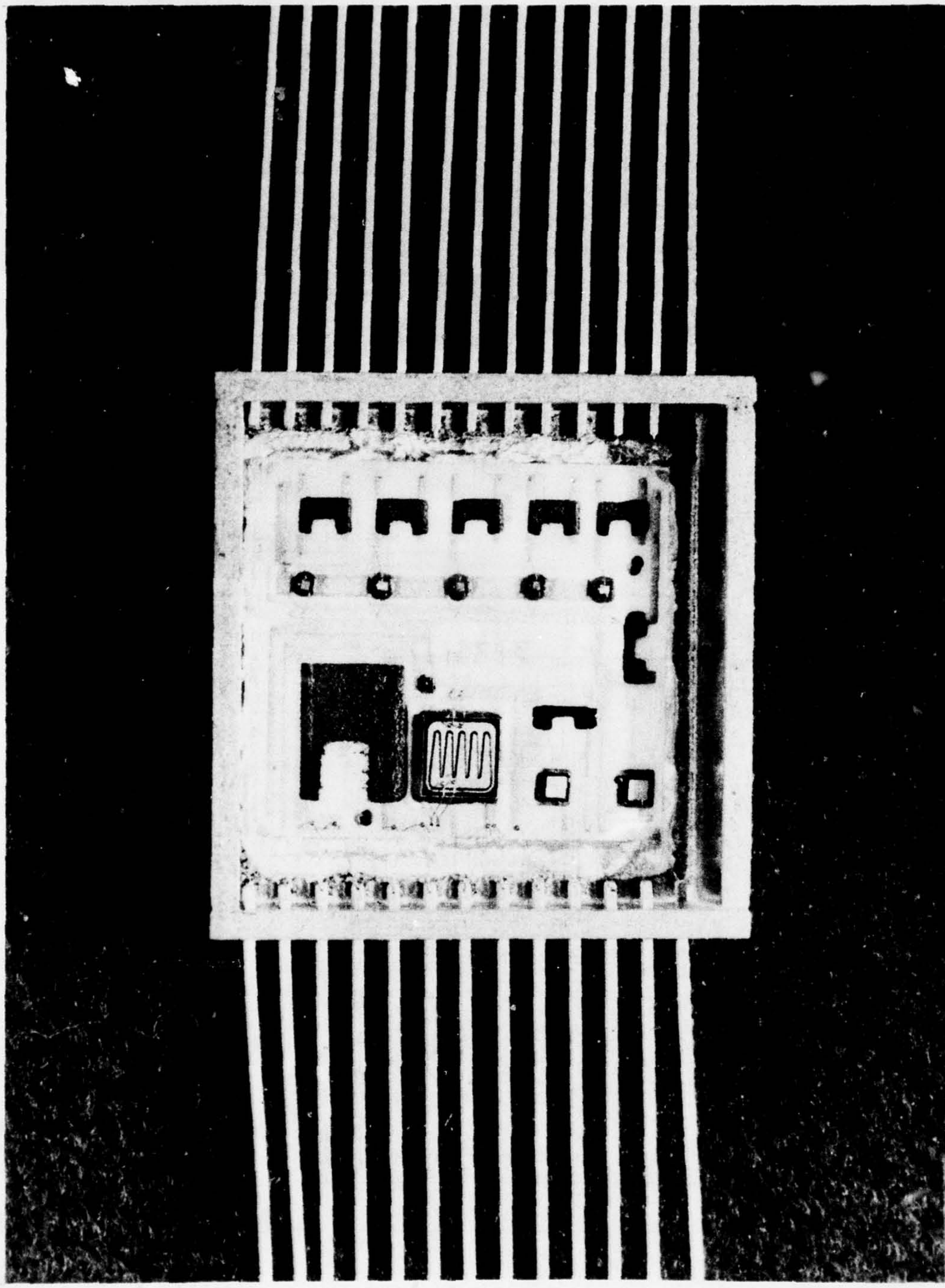


Figure 4. Photograph of 3/4-in. flat pack circuit H215.

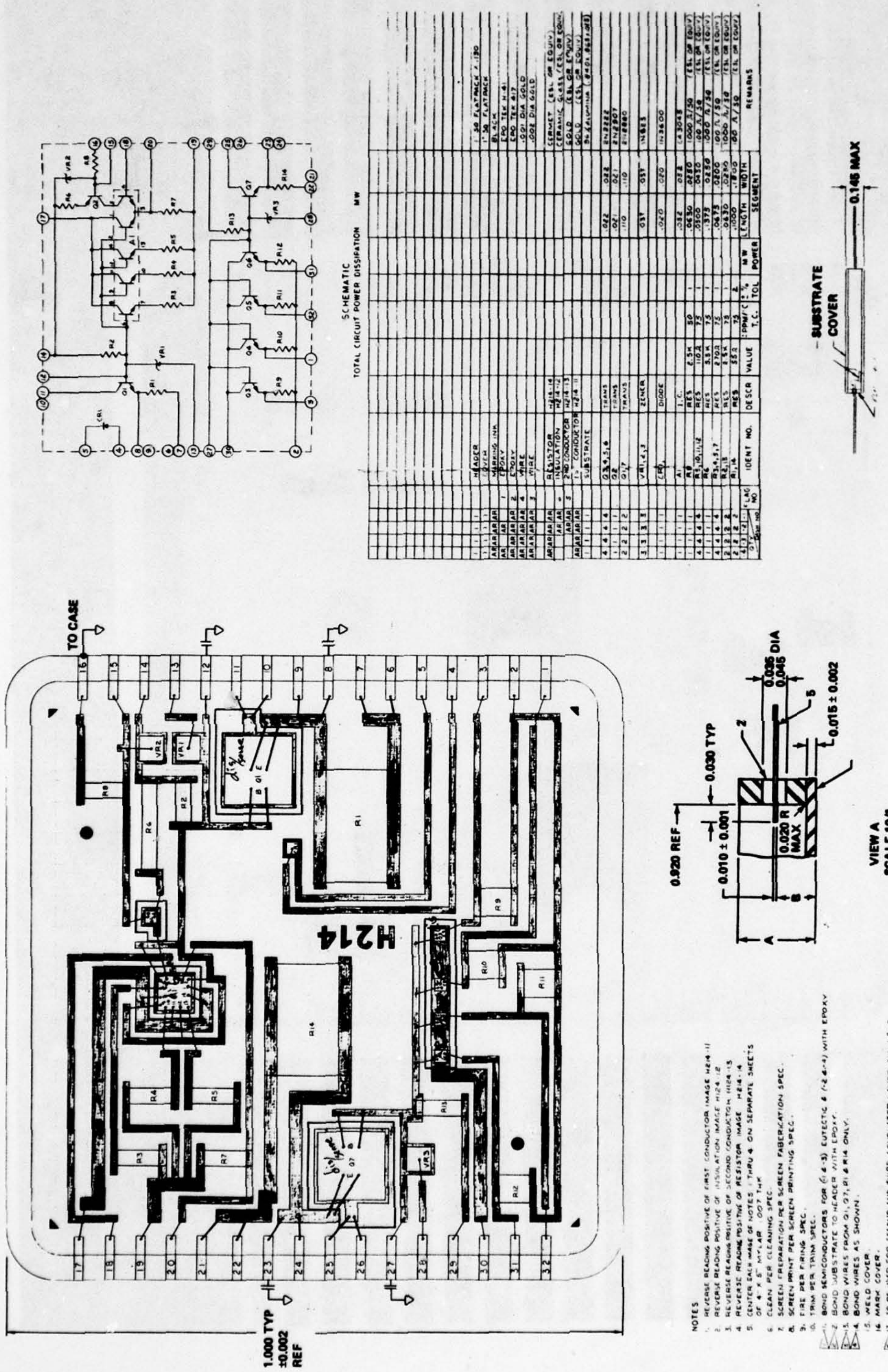


Figure 5. Assembly drawing of 1-in. flat pack.

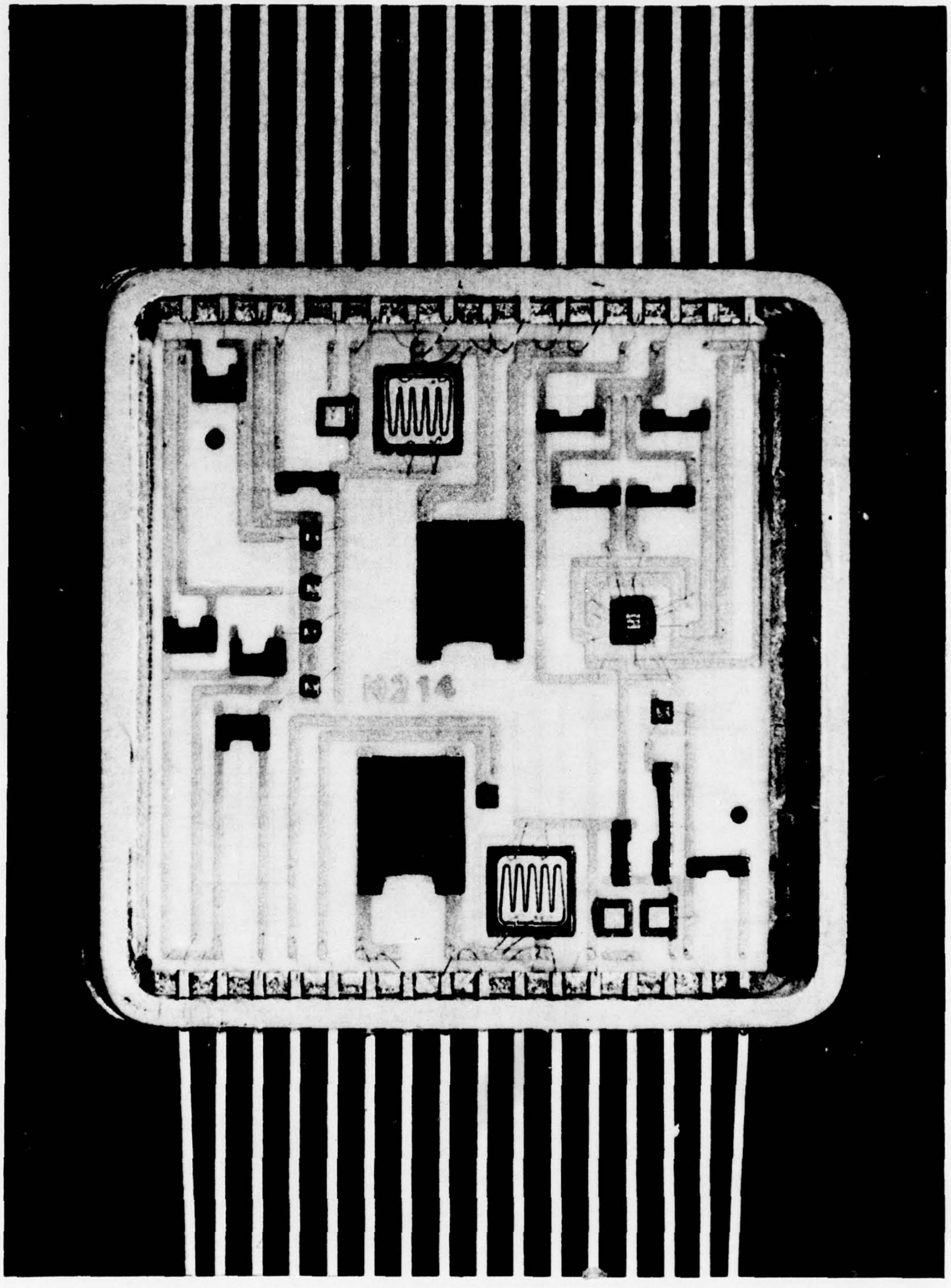
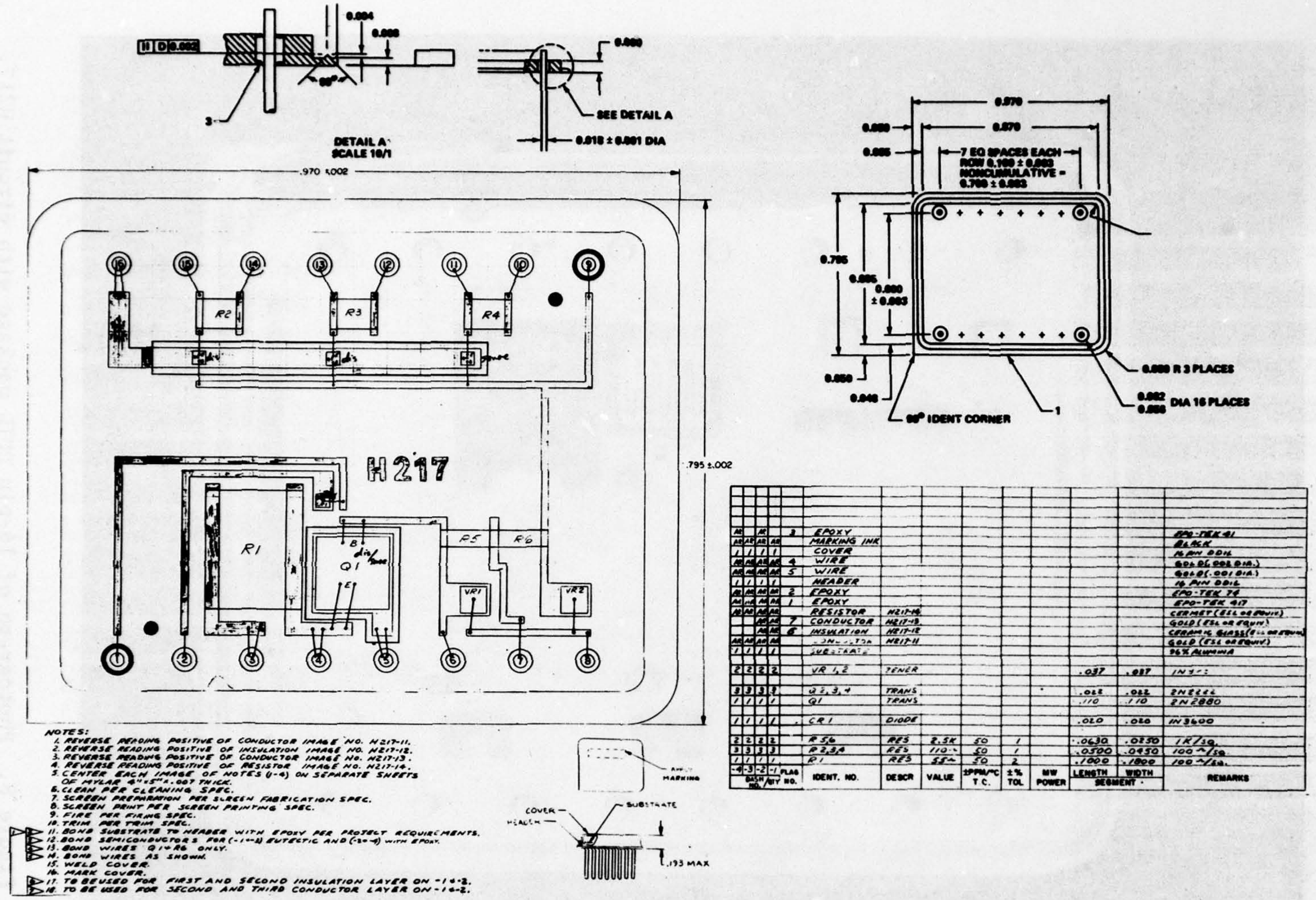


Figure 6. Photograph of 1-in. flat pack circuit H214.



-4	-3	-2	-1	Flag No.	Ident. No.	Descr	Value	±PPM/°C T.C.	±% Tol	MW Power	Segment Length	Segment Width	Remarks
AR		AR		3	EPOXY								EPO-TEK 41
AR	AR	AR	AR		MARKING INK								BLACK
1	1	1	1		COVER								16 PIN DDIL
AR	AR	AR	AR	4	WIRE								GOLD (.002 DIA.)
AR	AR	AR	AR	5	WIRE								GOLD (.001 DIA.)
1	1	1	1		HEADER								16 PIN DDIL
AR	AR	AR	AR	2	EPOXY								EPO-TEK 74
AR	AR	AR	AR	1	EPOXY								EPO-TEK 417
AR	AR	AR	AR		RESISTOR	H217-14							CERMET (ESL OR EQUIV.)
		AR	AR	7	CONDUCTOR	H217-13							GOLD (ESL OR EQUIV.)
		AR	AR	6	INSULATION	H217-12							CERAMIC GLASS (ESL OR EQUIV.)
AR	AR	AR	AR		CONDUCTOR	H217-11							GOLD (ESL OR EQUIV.)
1	1	1	1		SUBSTRATE								96% ALUMINA
2	2	2	2		VR 1,2	ZENER					.037	.037	[illegible]
3	3	3	3		Q2,3,4	TRANS					.022	.022	2N2222
1	1	1	1		Q1	TRANS					.110	.110	2N2880
1	1	1	1		CR1	DIODE					.020	.020	1N3600
2	2	2	2		R5,6	RES	2.5K	50	1		.0630	.0250	1K/sq.
3	3	3	3		R2,3,4	RES	110Ω	50	1		.0500	.0450	100Ω/sq.
1	1	1	1		R1	RES	55Ω	50	2		.1000	.1800	100Ω/sq.

Figure 7. Assembly drawing of 16-pin DDIL.

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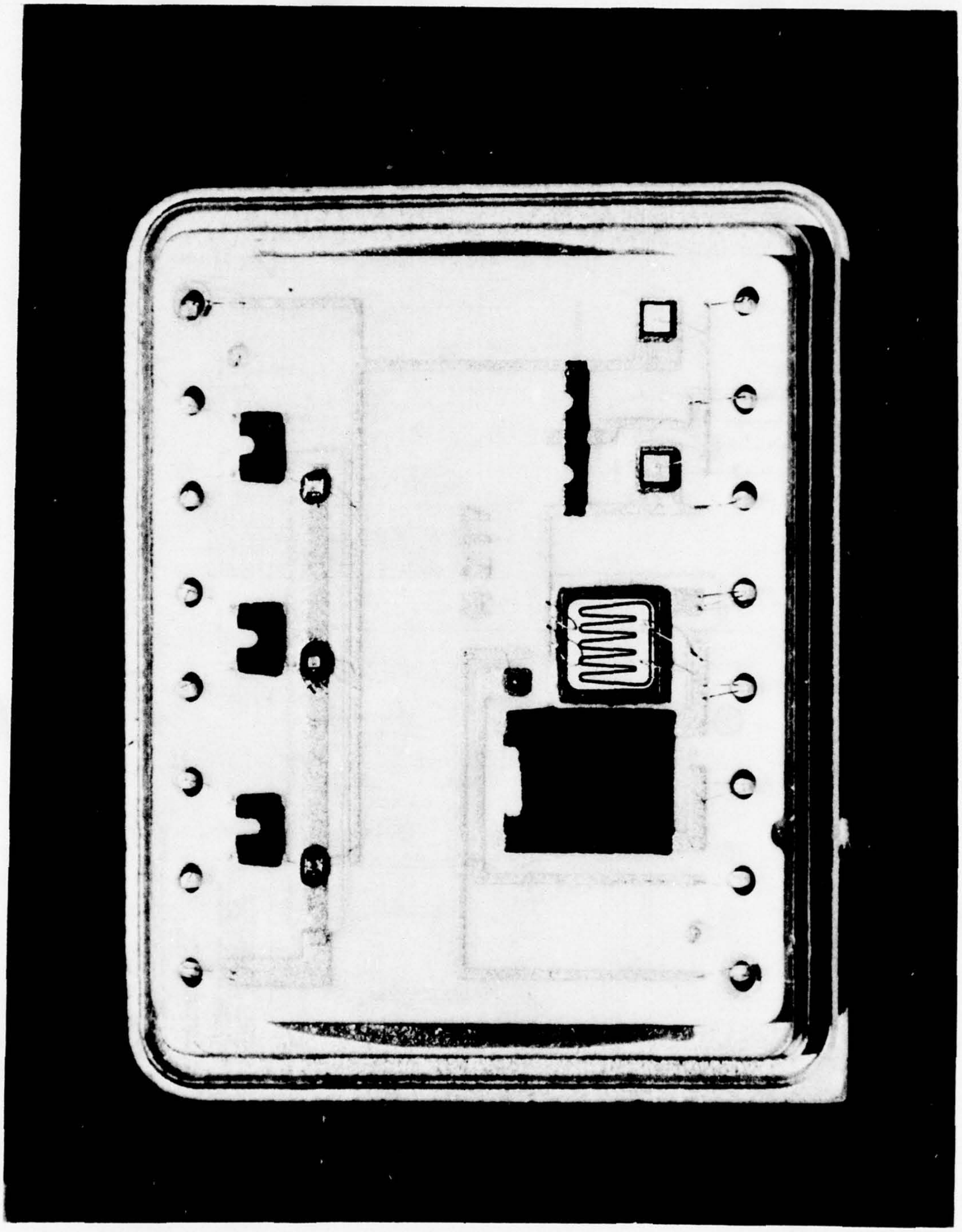

Figure 8. Photograph of 16-pin DDIL package with circuit H217.

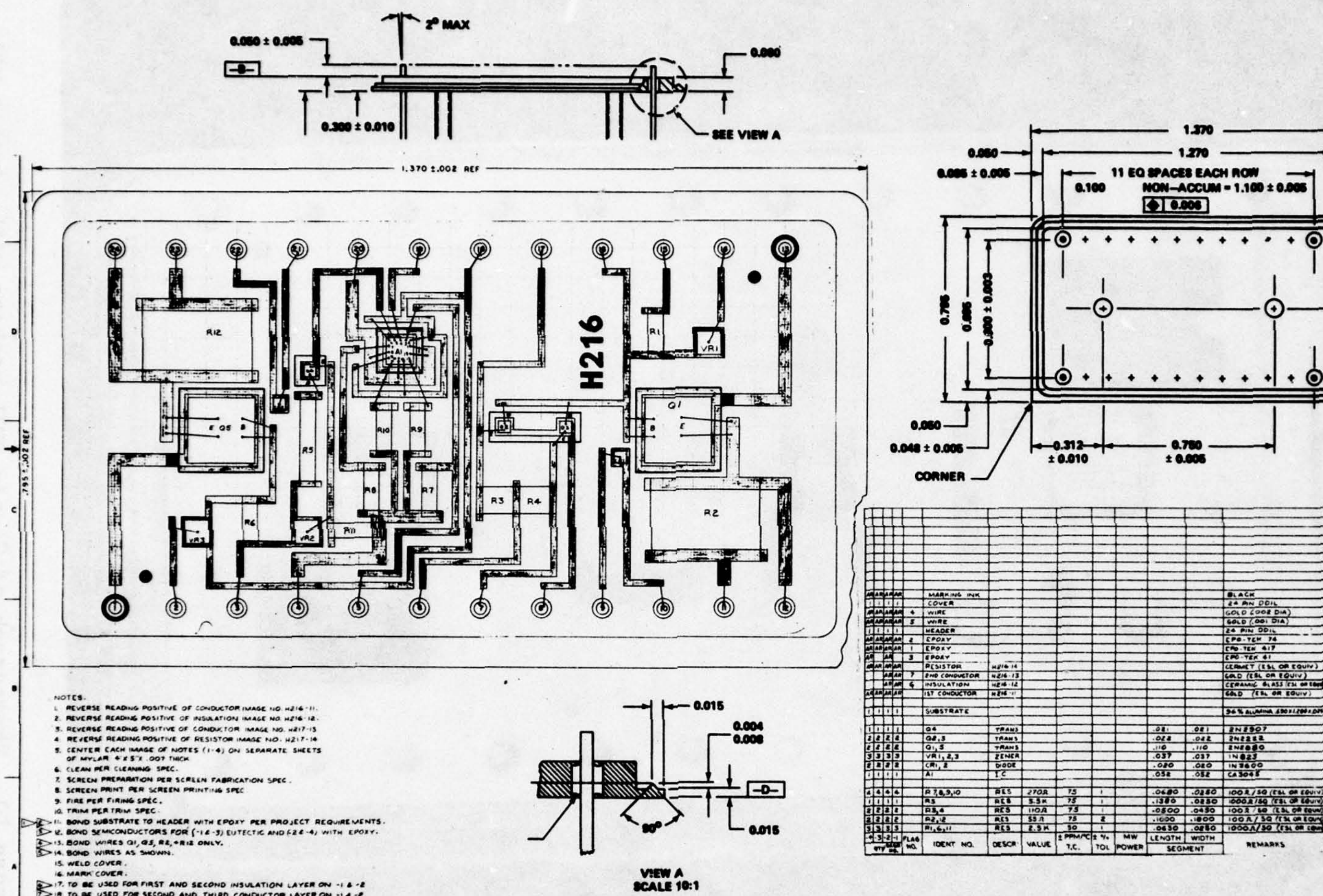

Figure 9. Assembly drawing of 24-pin DDIL.

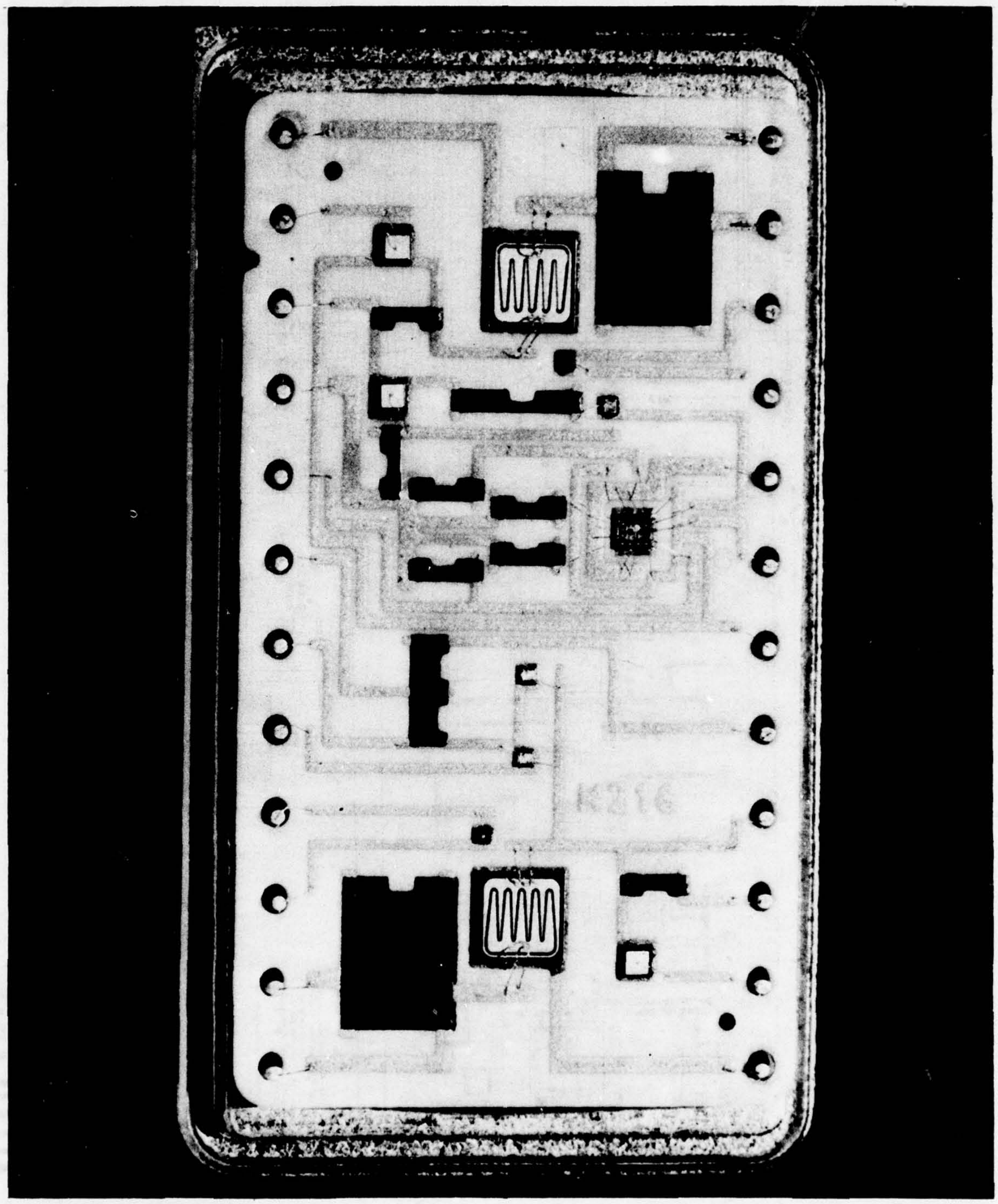

Figure 10. Photograph of 24-pin DDIL package with circuit H216.

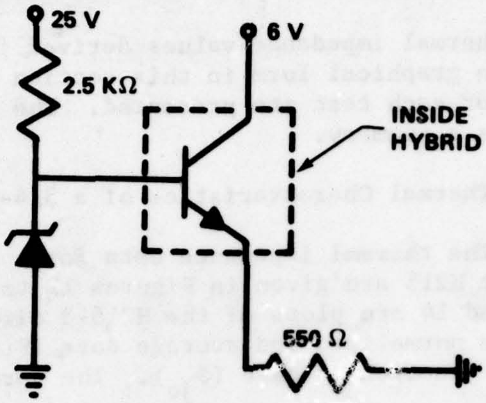

Figure 11 Test circuit configuration. (The 2.5 kΩ resistor and zener were substituted by a constant voltage source in most tests.)

The basic technique used for calibrating the junction was to apply the base and collector voltage (Figure 11) and then stabilize the package at the required temperature, read and record the V_{BE} (voltage base to emitter) at all the required temperatures from -55°C to 150°C, and then draw a calibration curve from which V_{BE} at 175°C junction temperature could be interpolated. The power dissipated during this test was always very small compared to the power capability of the chip involved.

It was decided that junction temperature would be maintained at a fixed temperature for all tests; therefore, a given package was installed inthe oven, the oven was stabilized at the required temperature, and the collector voltage was increased to the point that V_{BE} equalled the V_{BE} at 175°C. Power dissipation was computed by multiplying collector current (a constant) times collector-emitter voltage. The power dissipation was recorded on a chart along with header temperature and the V_f of any reference diodes available on the substrate (Appendix). This information allowed direct computation of θ_{jc} as well as power capability of a given package type at all temperatures from -55°C to +150°C.

3. Data Analysis

All raw data taken are provided in the Appendix. The thermocouple voltage was converted to equivalent temperature. The wattage per device and total for the package was calculated. The junction was maintained at 175°C. A plot of wattage versus $T_j - T_c$ was made on each package type and each bonding technique. Table 1 indicates the package, bonding types, and corresponding serial numbers of the circuits.

D. Experimental Results

The thermal impedance values derived from the experimental data are presented in graphical form in this section of the report. The actual data points for each test are presented. The normalized and average data are presented as a summary.

1. Thermal Characteristics of a 3/4-in. Flat Pack

The thermal impedance data for a 3/4-in. flat-pack designated as circuit H215 are given in Figures 12 to 23. The first Figures of 12, 13, and 14 are plots of the H215-3 circuit for the raw data (Figure 12), the normalized and average data (Figure 13) of the thermal impedance of junction to case (θ_{jc}). The normalized and average data of the thermal impedance of the junction to static ambient air θ_{ja} (Figure 14) are also presented. The three different lines indicate the three packages analyzed. (SN 7, 8, 9). This circuit (-3) was a eutectically mounted die, single layer substrate with the substrate to header bond via silver filled epoxy, H-417 (Table 1).

Figures 15, 16, and 17 are the plots of the H215-4 curcuit. The raw data (Figure 15) and averaged data (Figure 16) for θ_{jc} are provided along with the averaged data for θ_{ja} (Figure 17). This circuit (-4) was an epoxy mounted die (H-41) single layer substrate with the substrate to header bond via silver filled epoxy H417 (Table 1).

Figures 18, 19, and 20 are the plots of the H215-1 circuit. The raw data (Figure 18) and the normalized and averaged data (Figure 19) are of the thermal impedance of junction to case. The normalized and averaged data of the thermal impedance of the junction to static ambient air (Figure 20) are also presented. The three different lines indicate the three packages analyzed. (SN 1, 2, 3) this circuit (-1) was a eutectically mounted die, multilayer substrate with the substrate to header bond via silver filled epoxy, H-417 (Table 1).

Figures 21, 22, and 23 are the plots of the H215-2 circuit. The raw data (Figure 21) and the normalized and averaged data (Figure 22) are of the thermal impedance of junction to case. The normalized and averaged data of thermal impedance of the junction to static ambient air (Figure 23) are also presented. This circuit (-2) was an epoxy mounted die, multi-layer substrate with the substrate to header bond via silver filled epoxy H-417 (Table 1).

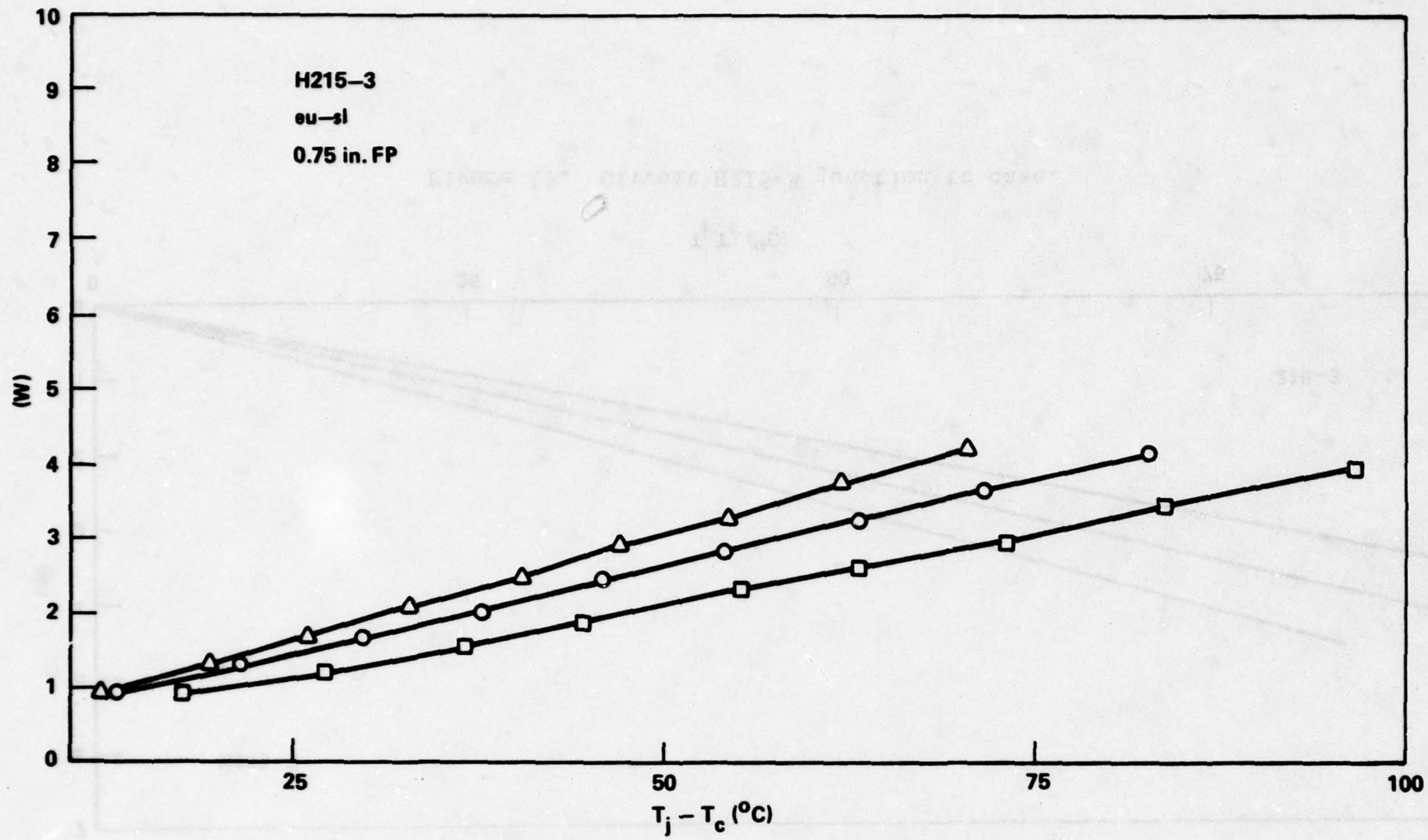

Figure 12. Circuit H215-3 raw data.

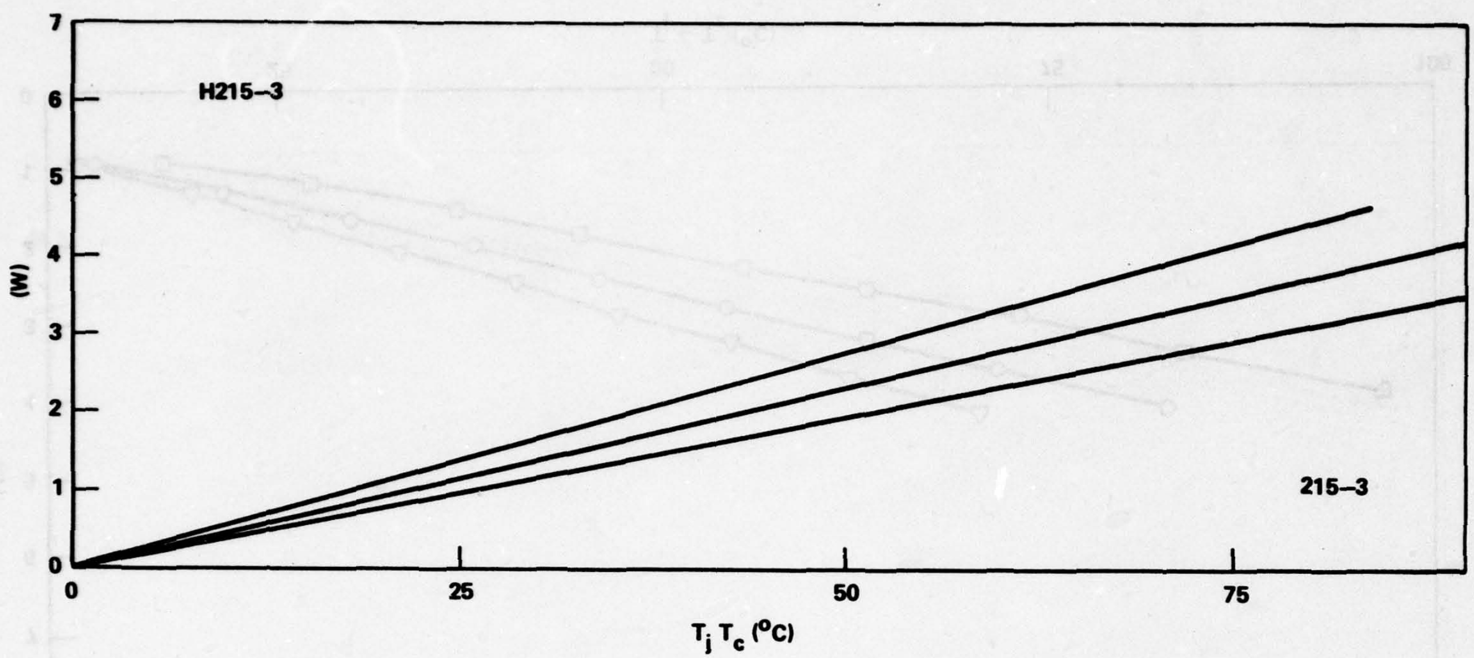

Figure 13. Circuit H215-3 junction to case.

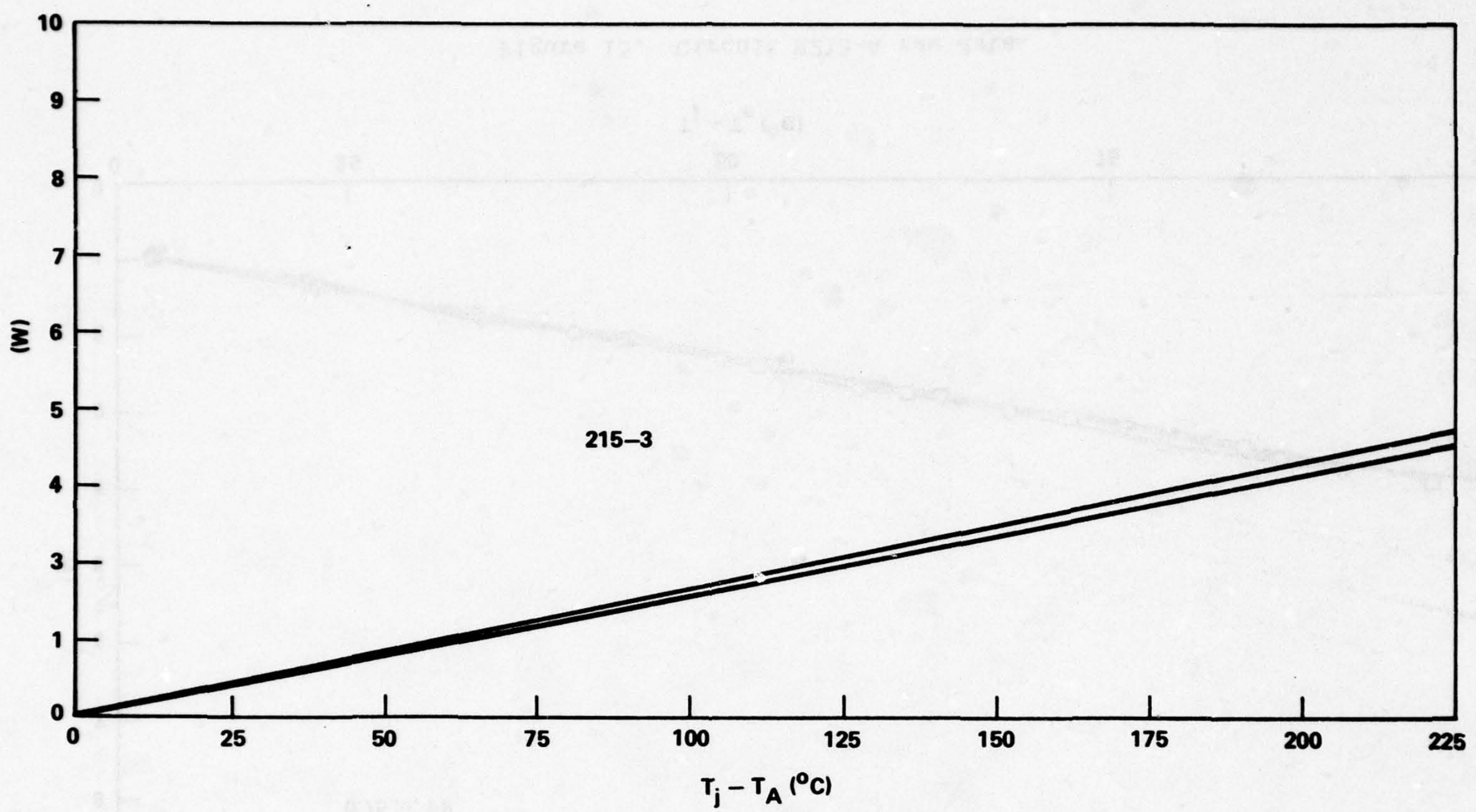

Figure 14. Circuit H215-3 junction to ambient.

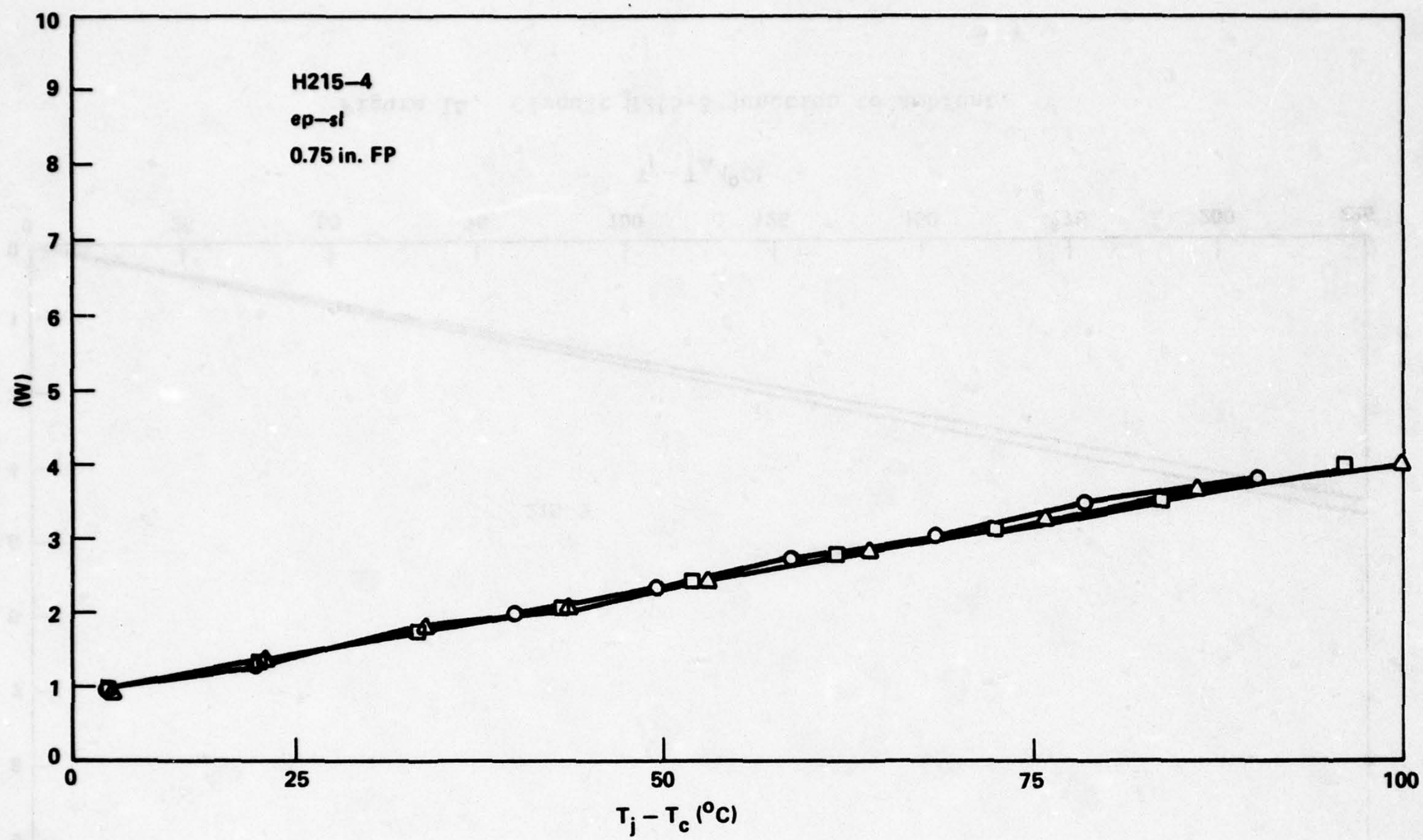

Figure 15. Circuit H215-4 raw data.

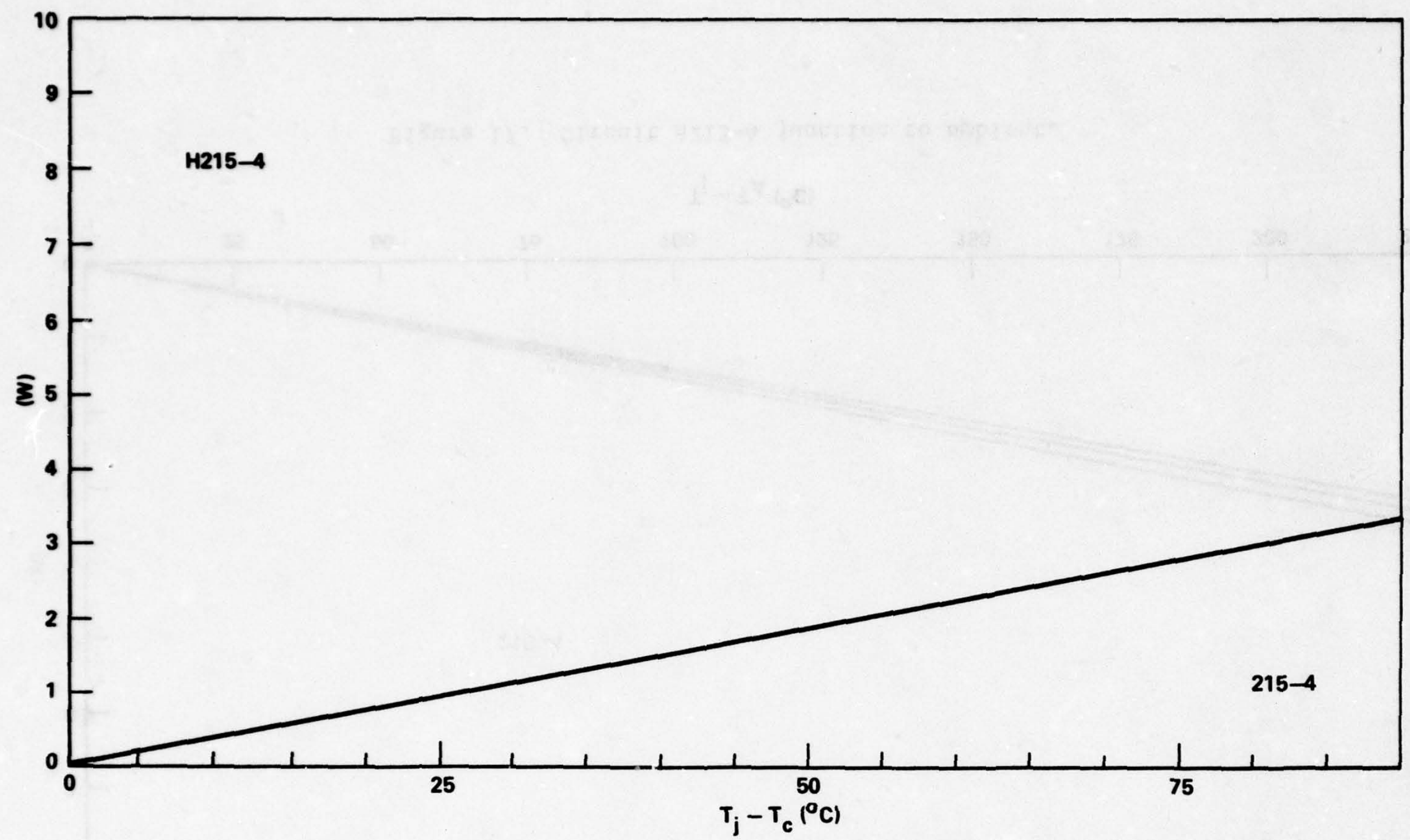

Figure 16. Circuit H215-4 junction case.

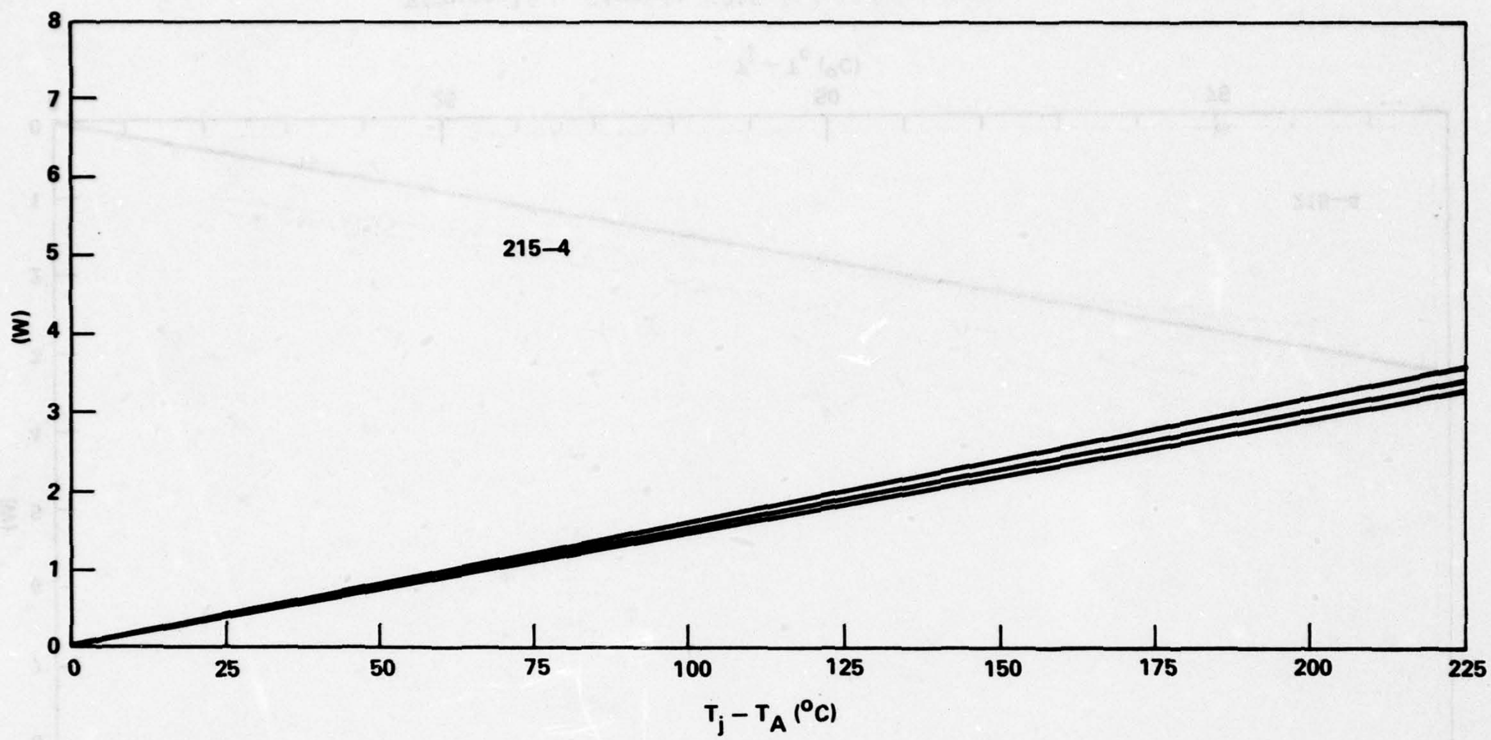

Figure 17. Circuit H215-4 junction to ambient.

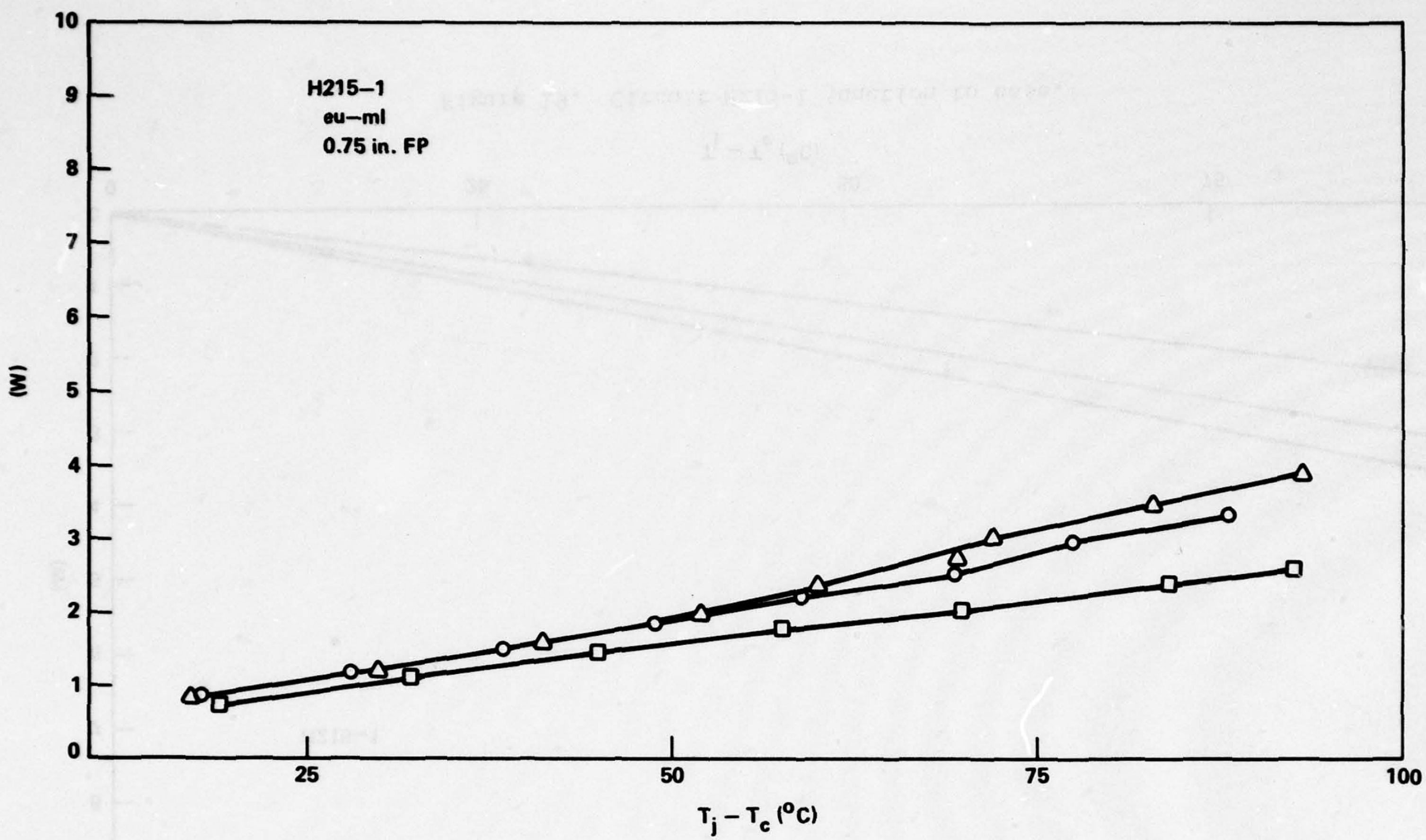

Figure 18. Circuit H215-1 raw data.

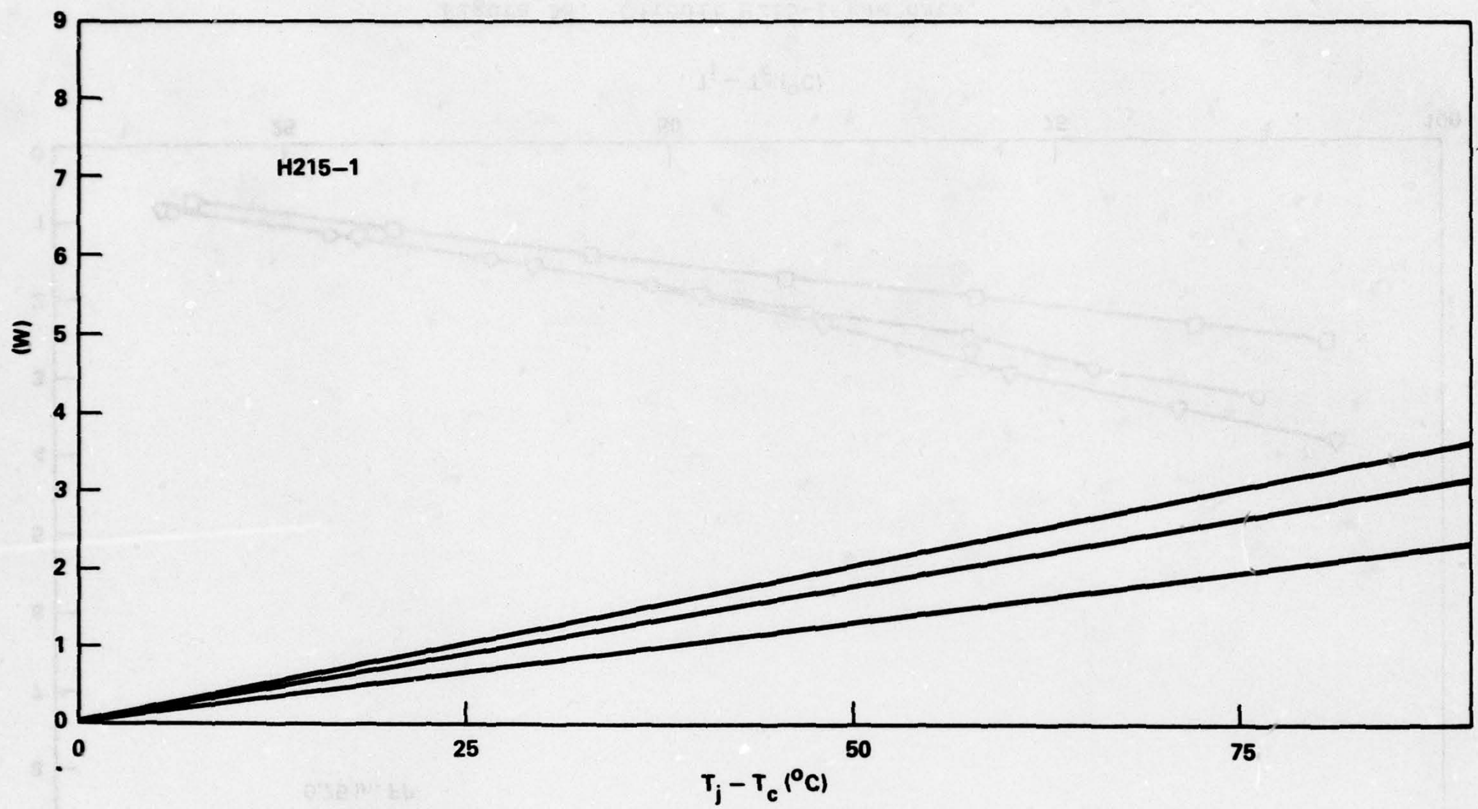

Figure 19. Circuit H215-1 junction to case.

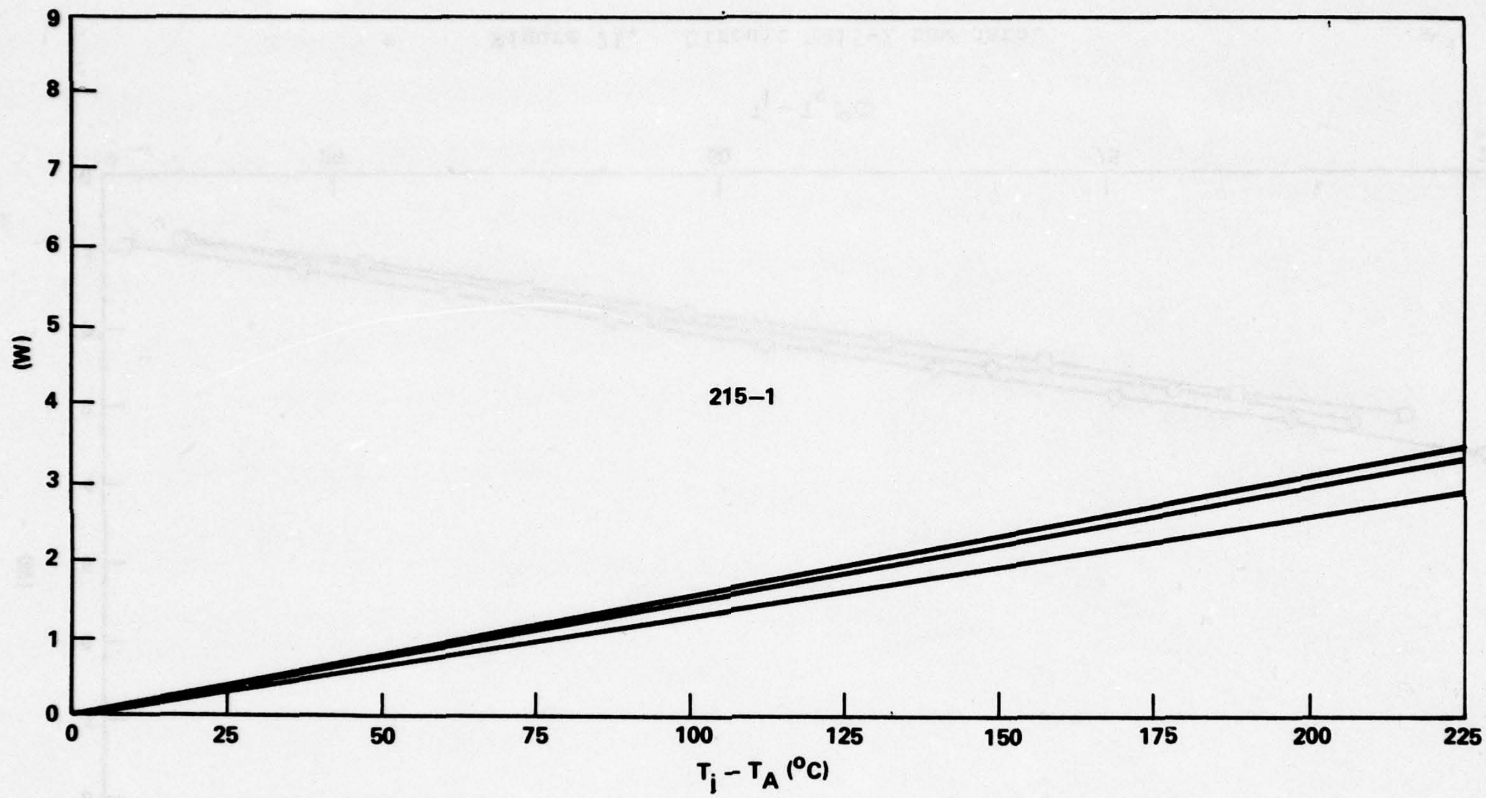

Figure 20. Circuit H215-1 junction to ambient.

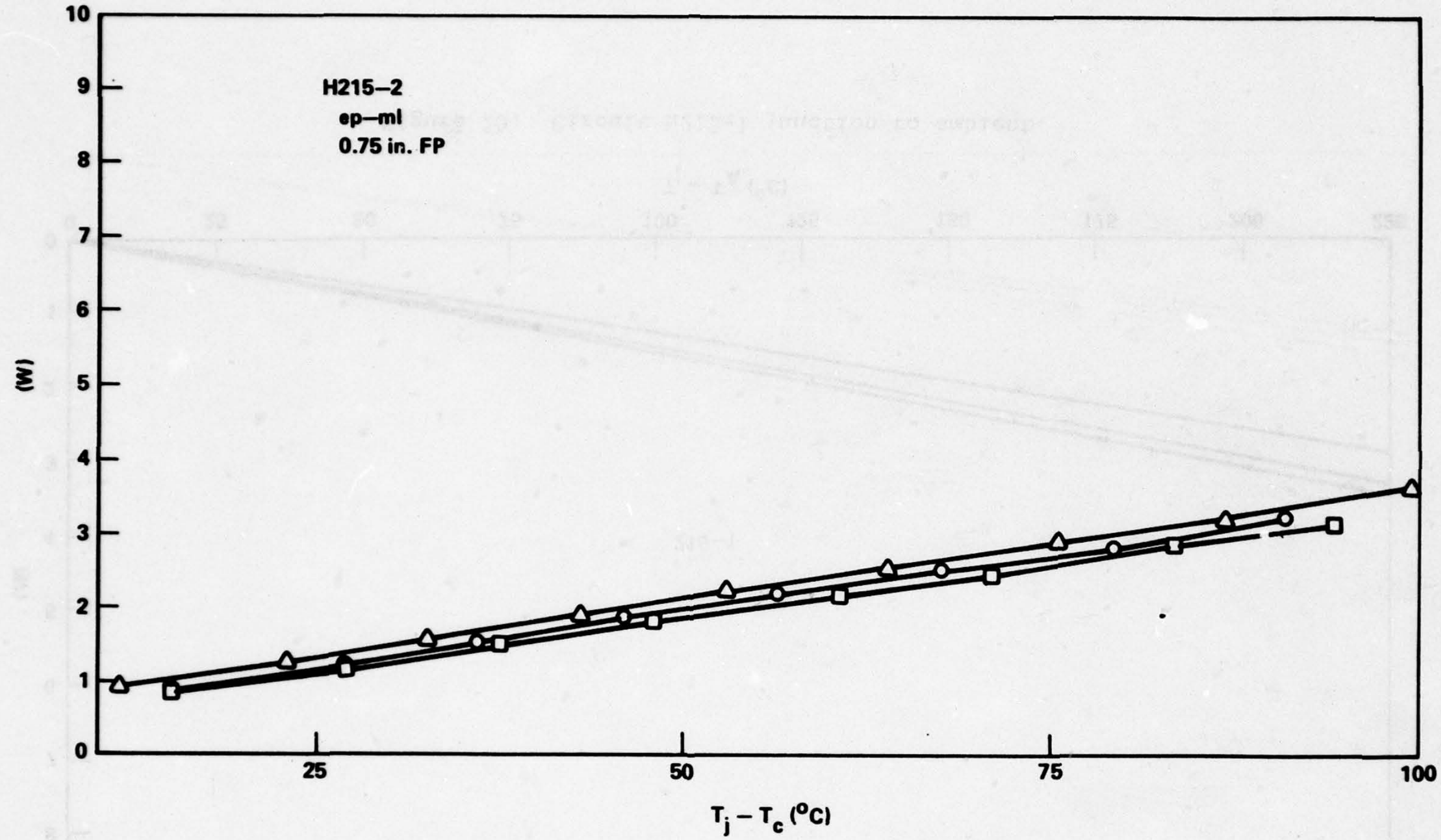

Figure 21. Circuit H215-2 raw data.

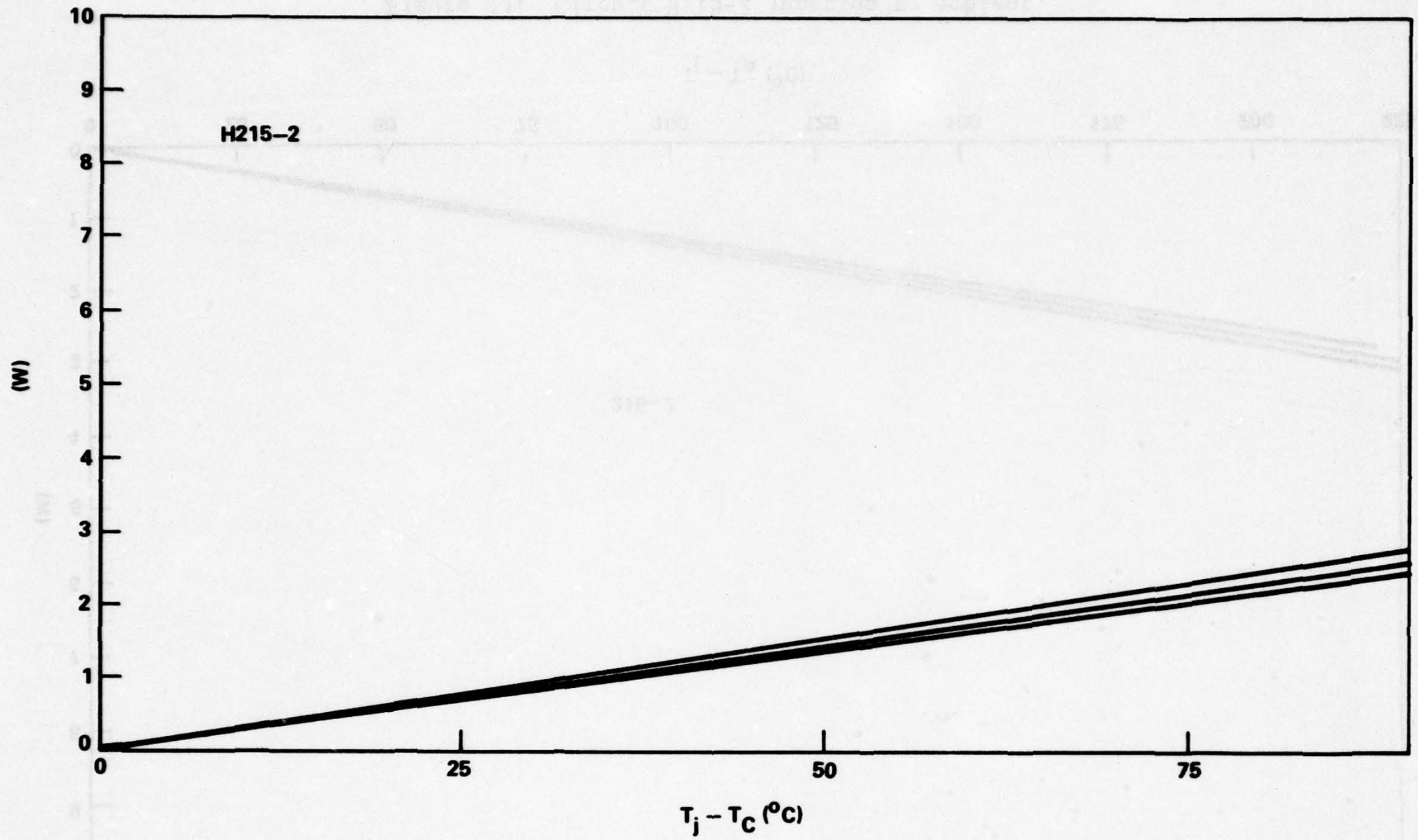

Figure 22. Circuit H215-2 junction to case.

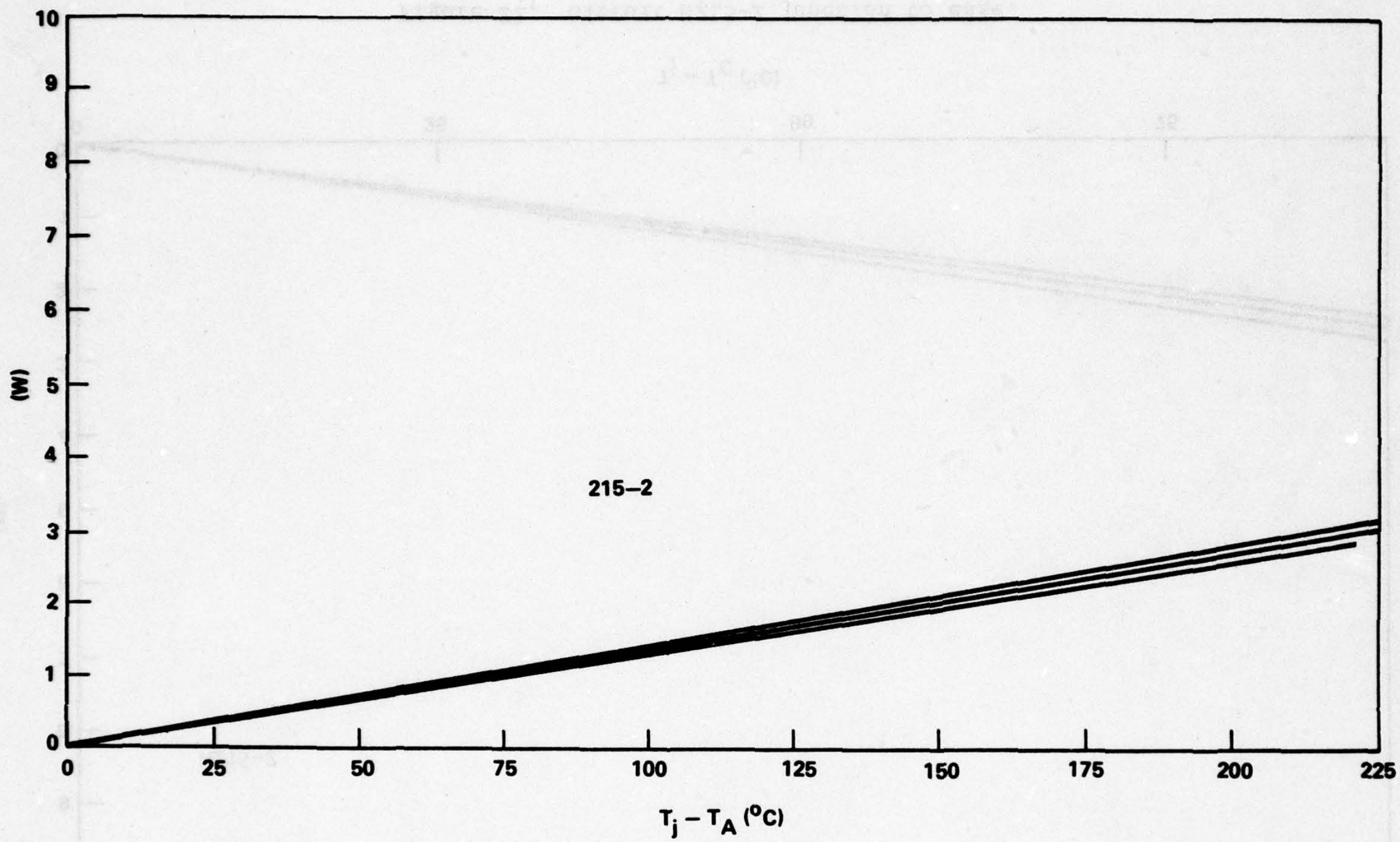

Figure 23. Circuit H215-2 junction to ambient.

2. Thermal Characteristics of a 1-in. Flat Pack

The thermal impedance data for a 1-in. flat pack designated as circuit H214 are given in Figures 24 to 35. Figures 24, 25, and 26 are plots of the H214-3 circuit for the raw data (Figure 24), the normalized and averaged data (Figure 25) and the thermal impedance of junction to static ambient air θ_{ja} (Figure 26). This circuit (-3) was a eutectically mounted die single layer substrate and substrate to header bond with H-417.

Figures 27, 28, and 29 are plots of the H214-4 circuit. Figure 27 presents the raw data. Figure 28 is the θ_{jc} (linearized and normalized). Figure 29 is the θ_{jc}. This circuit (-4) was epoxy die mounted (H-41), single layer substrate, and substrate to header bond with silver filled epoxy (H-417).

Figures 30, 31, and 32 are the plots of the H214-1 circuit. The raw data (Figure 30) and the normalized and averaged data (Figure 31) are of the thermal impedance of junction to case. The normalized and averaged data of the thermal impedance of the junction to static ambient air (Figure 32) are also presented. This circuit (-1) was a eutectically mounted die, multilayer substrate with the substrate to header bond via silver filled epoxy (H417).

Figures 33, 34, and 35 are the plots of the H214-2 circuit. The raw data (Figure 33) and the normalized and averaged data (Figure 34) are of the thermal impedance of junction to case. The normalized and averaged data of thermal impedance of the junction to static ambient air (Figure 35) are also presented. This circuit (-2) is with the substrate to header bond of silver filled epoxy (H-417).

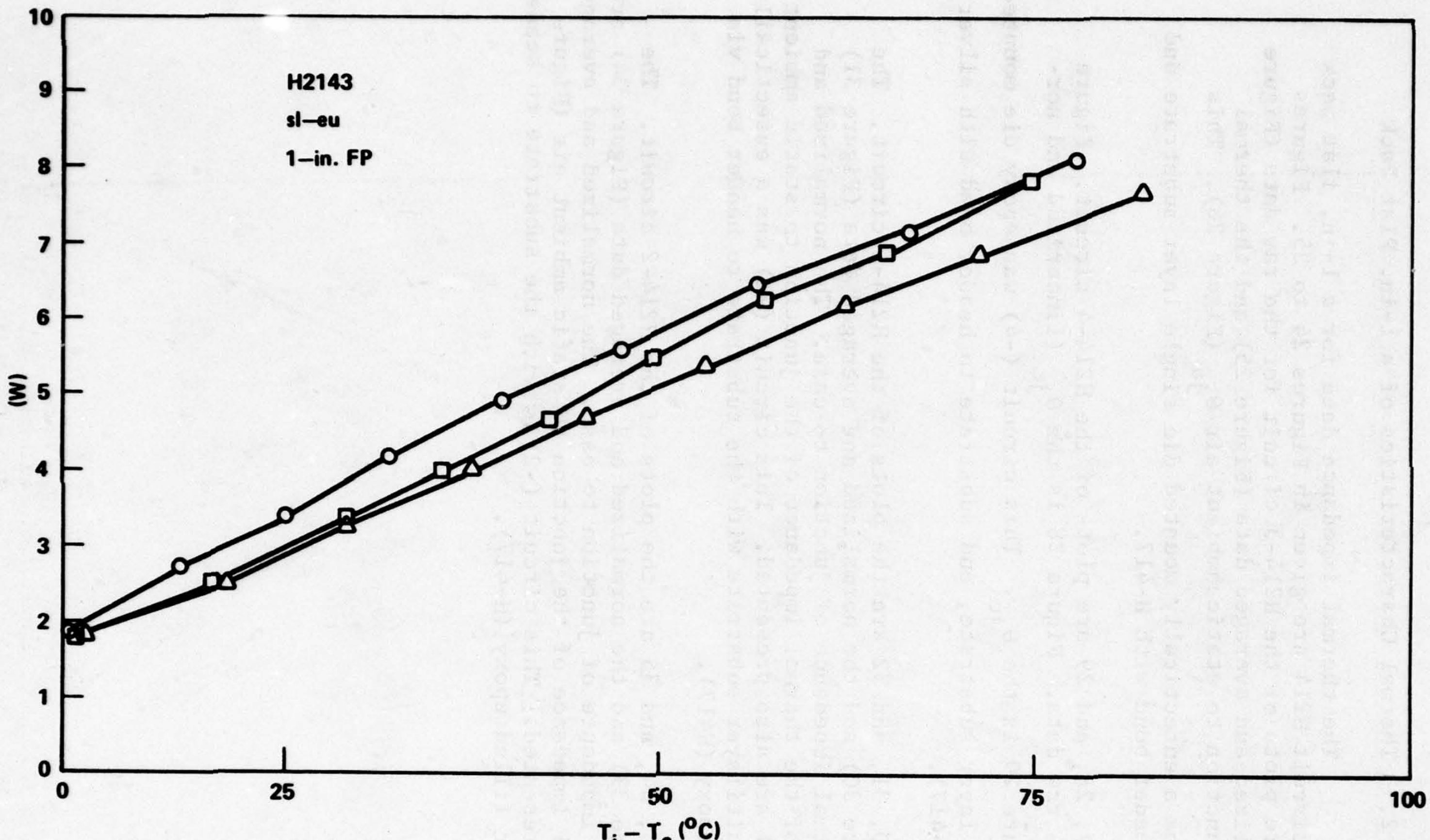

Figure 24. Circuit H214-3 raw data.

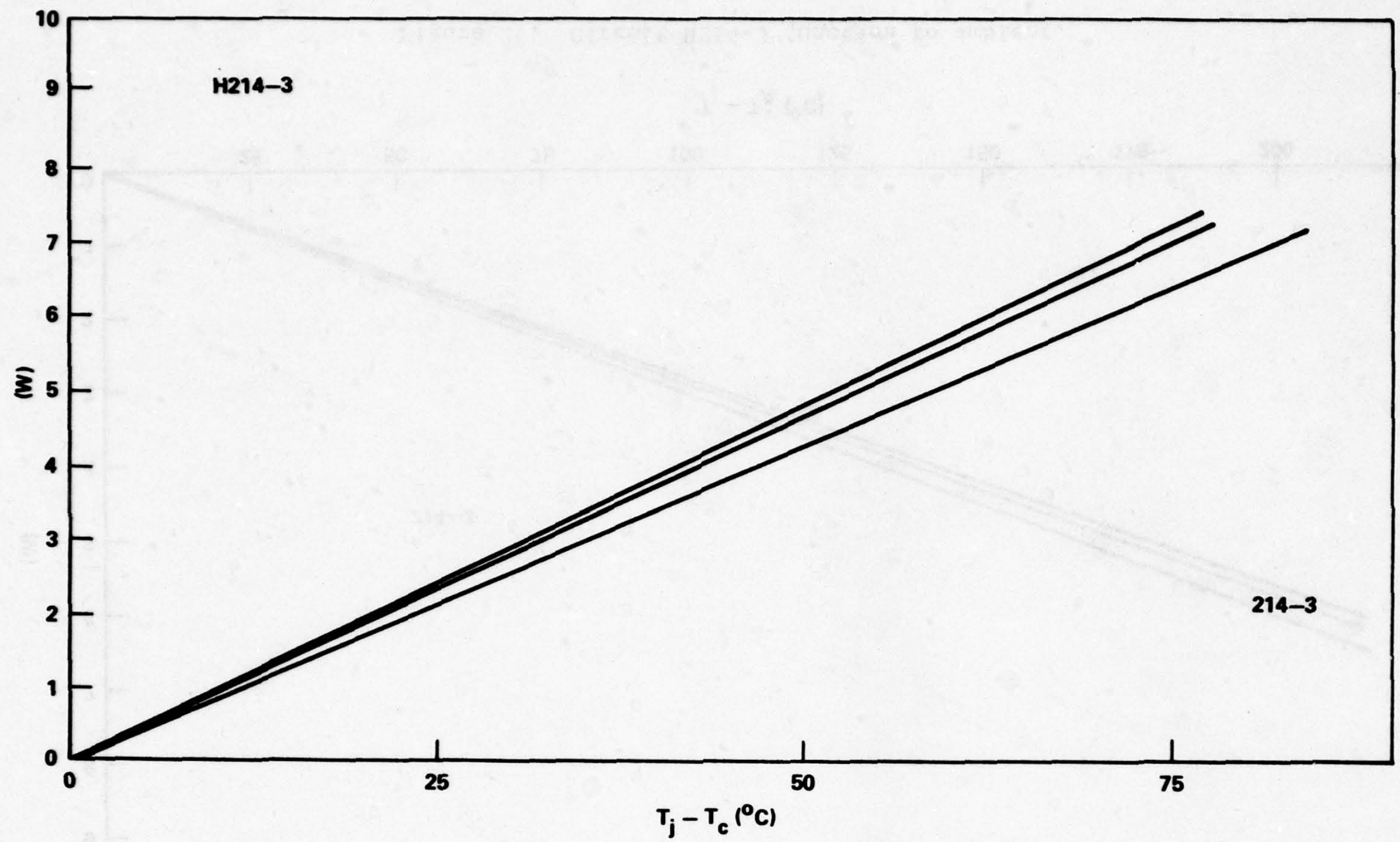

Figure 25. Circuit H214-3 junction case.

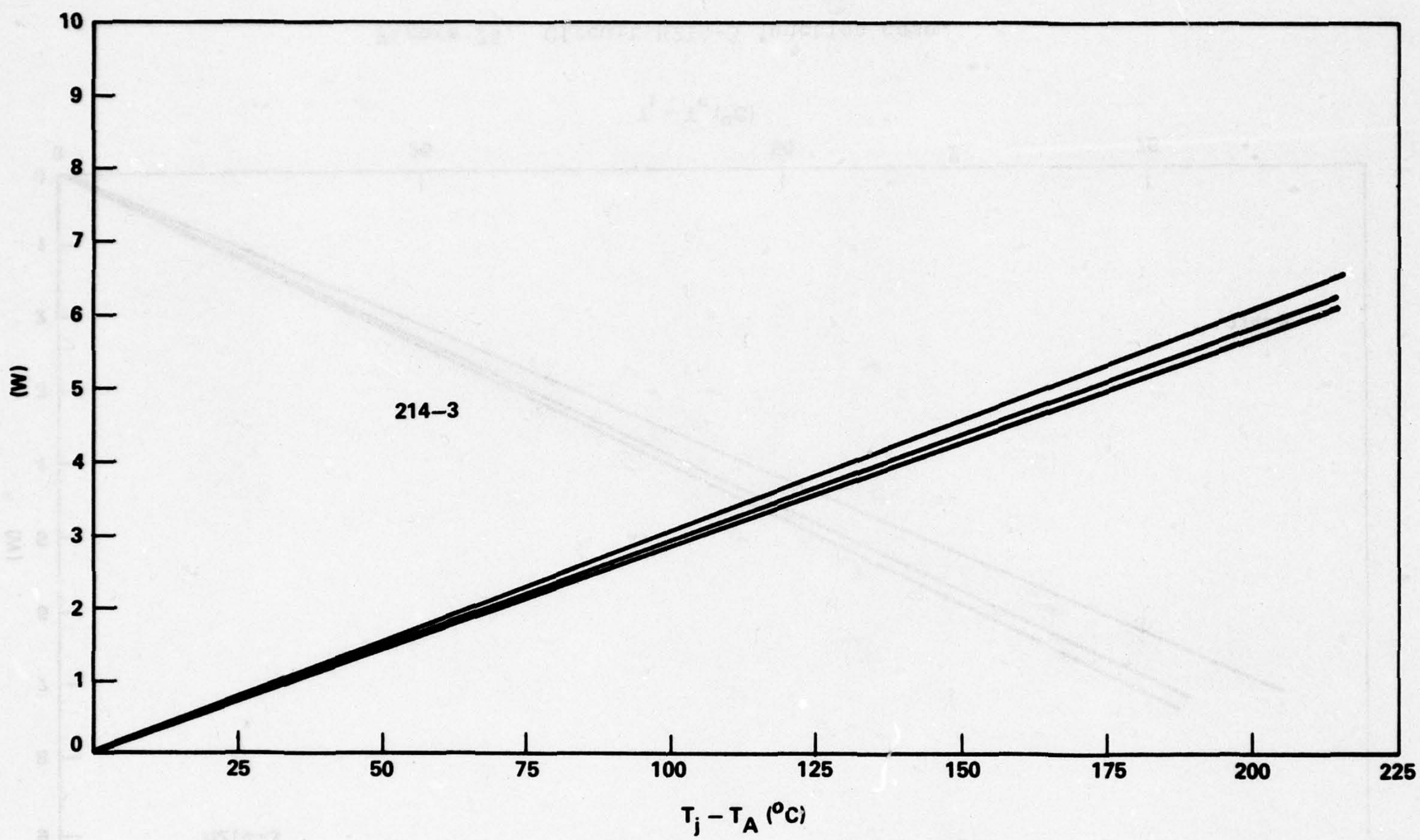

Figure 26. Circuit H214-3 junction to ambient.

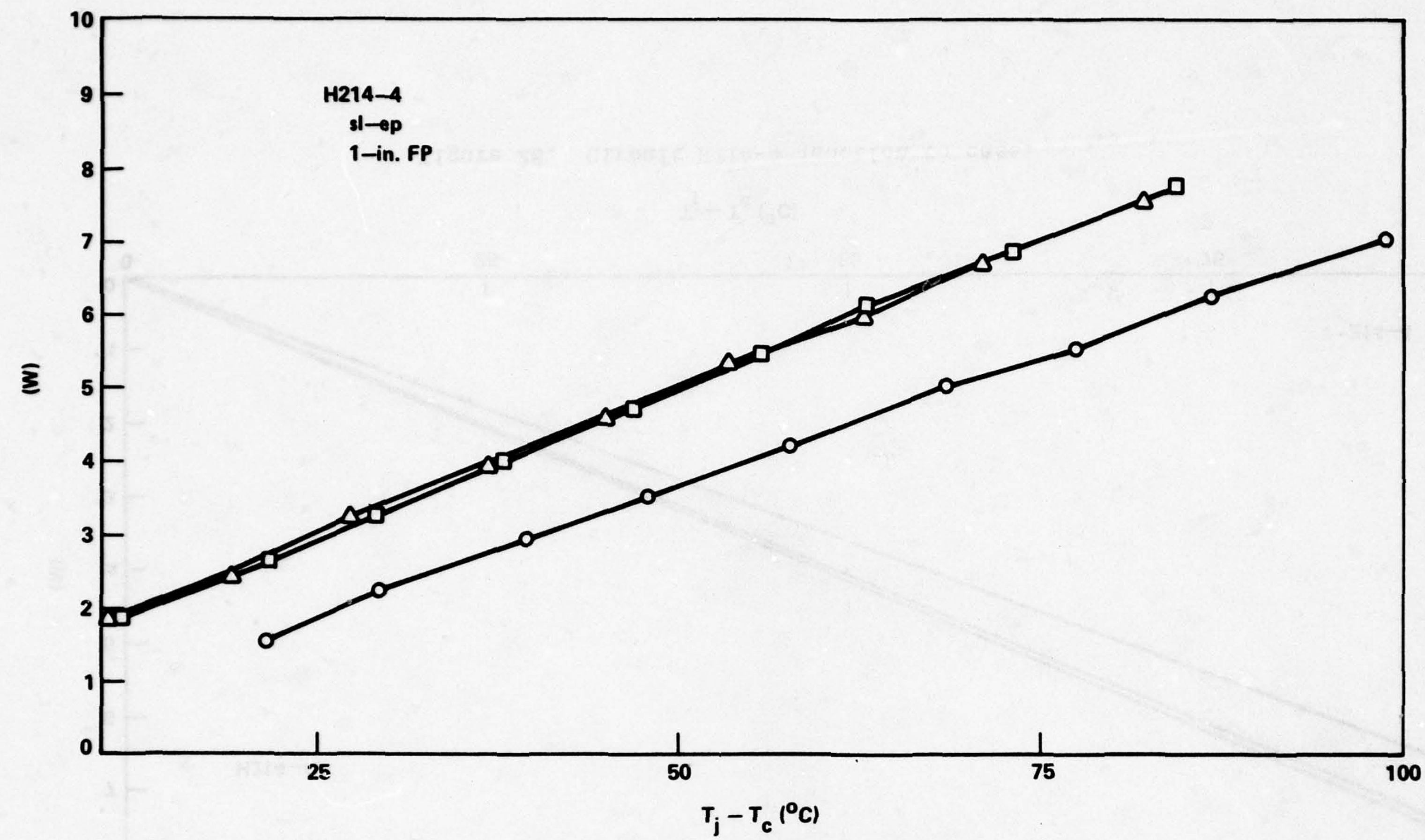

Figure 27. Circuit H214-4 raw data.

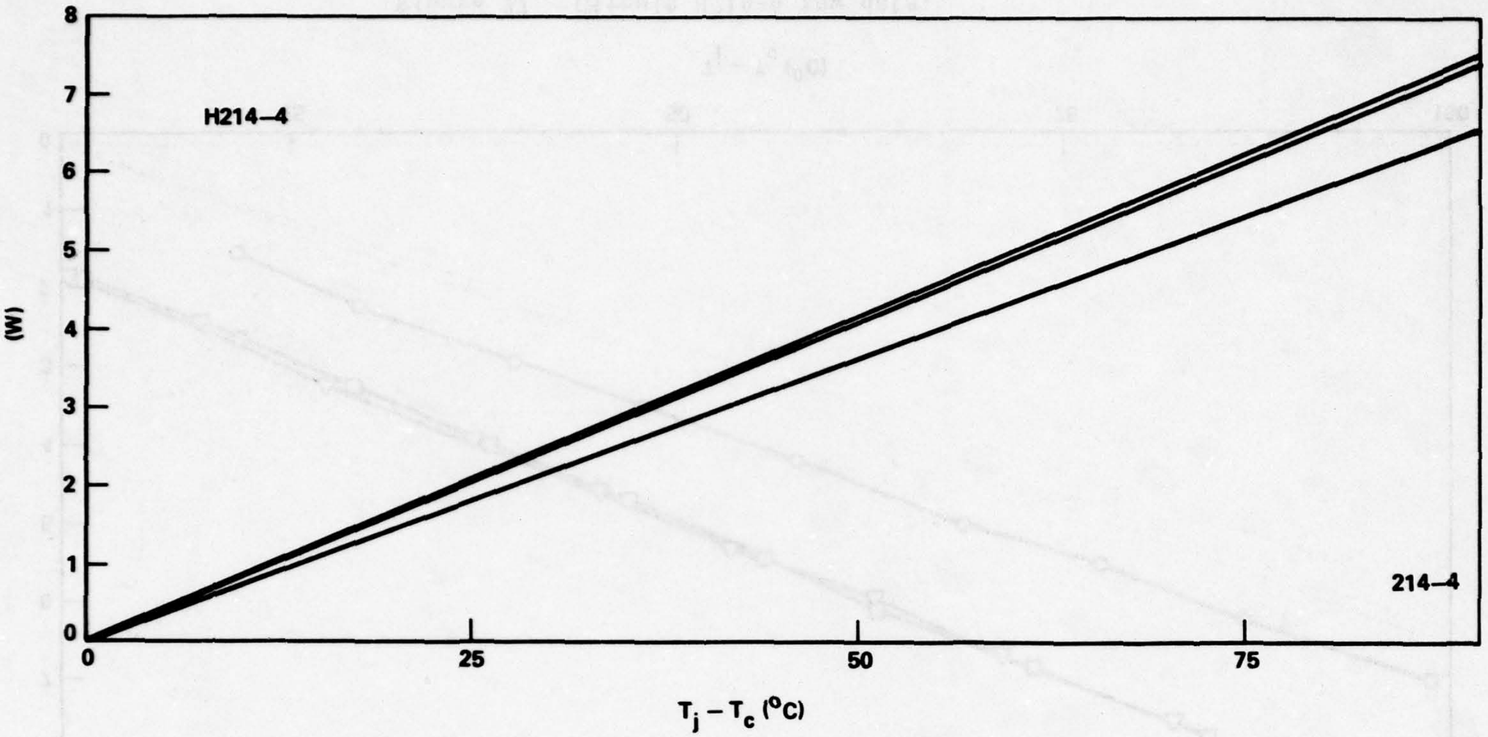

Figure 28. Circuit H214-4 junction to case.

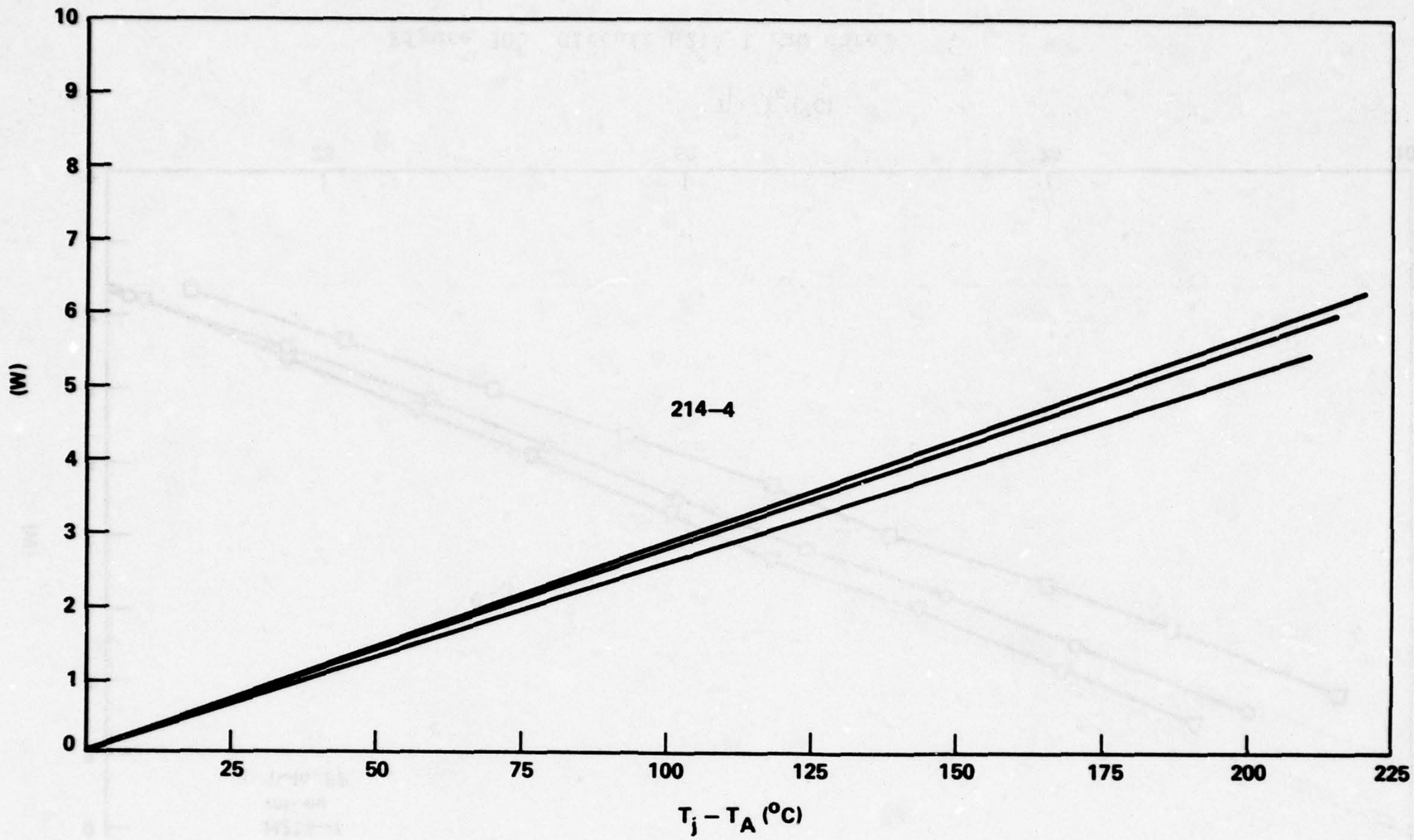

Figure 29. Circuit H214-4 junction to ambient.

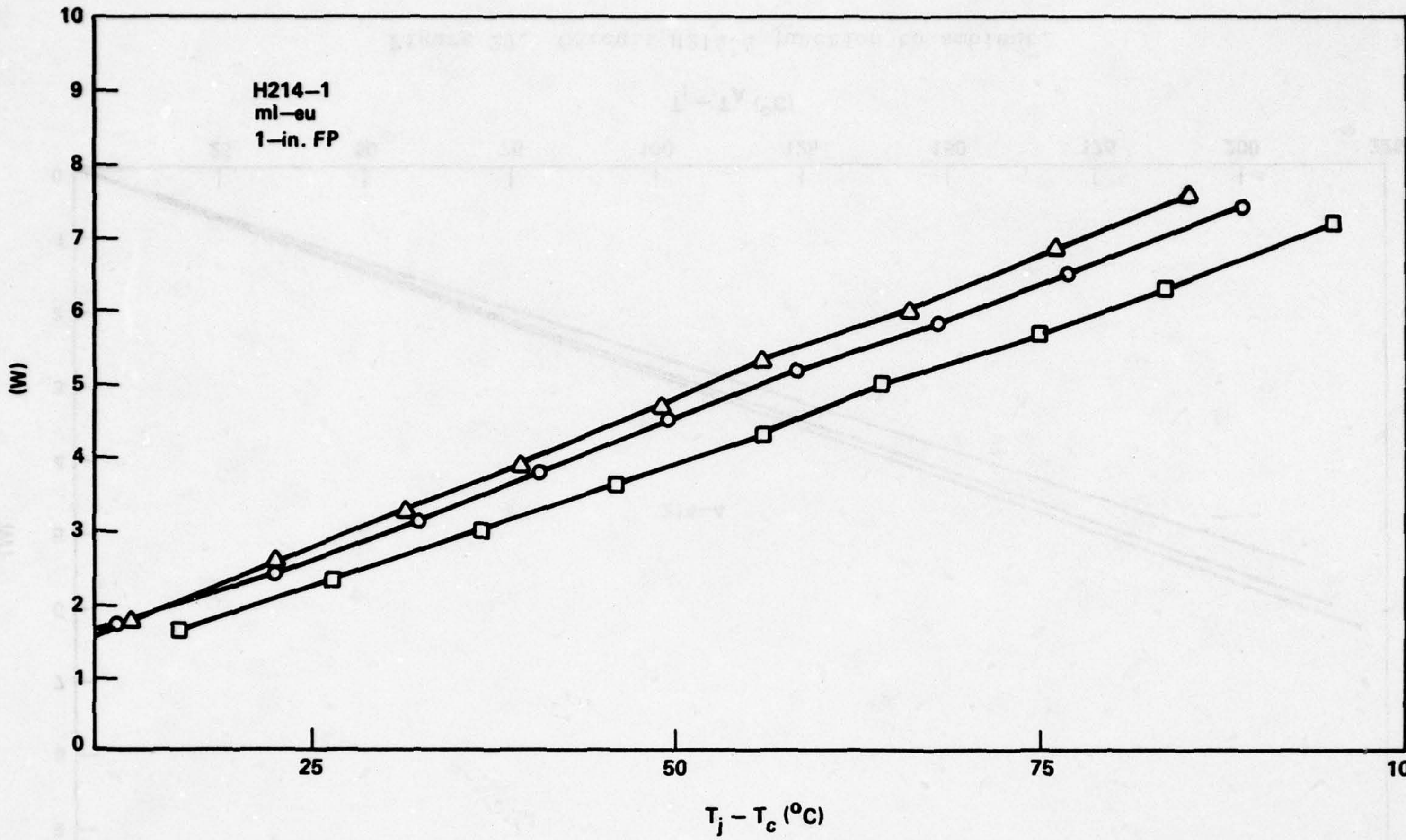

Figure 30. Circuit H214-1 raw data.

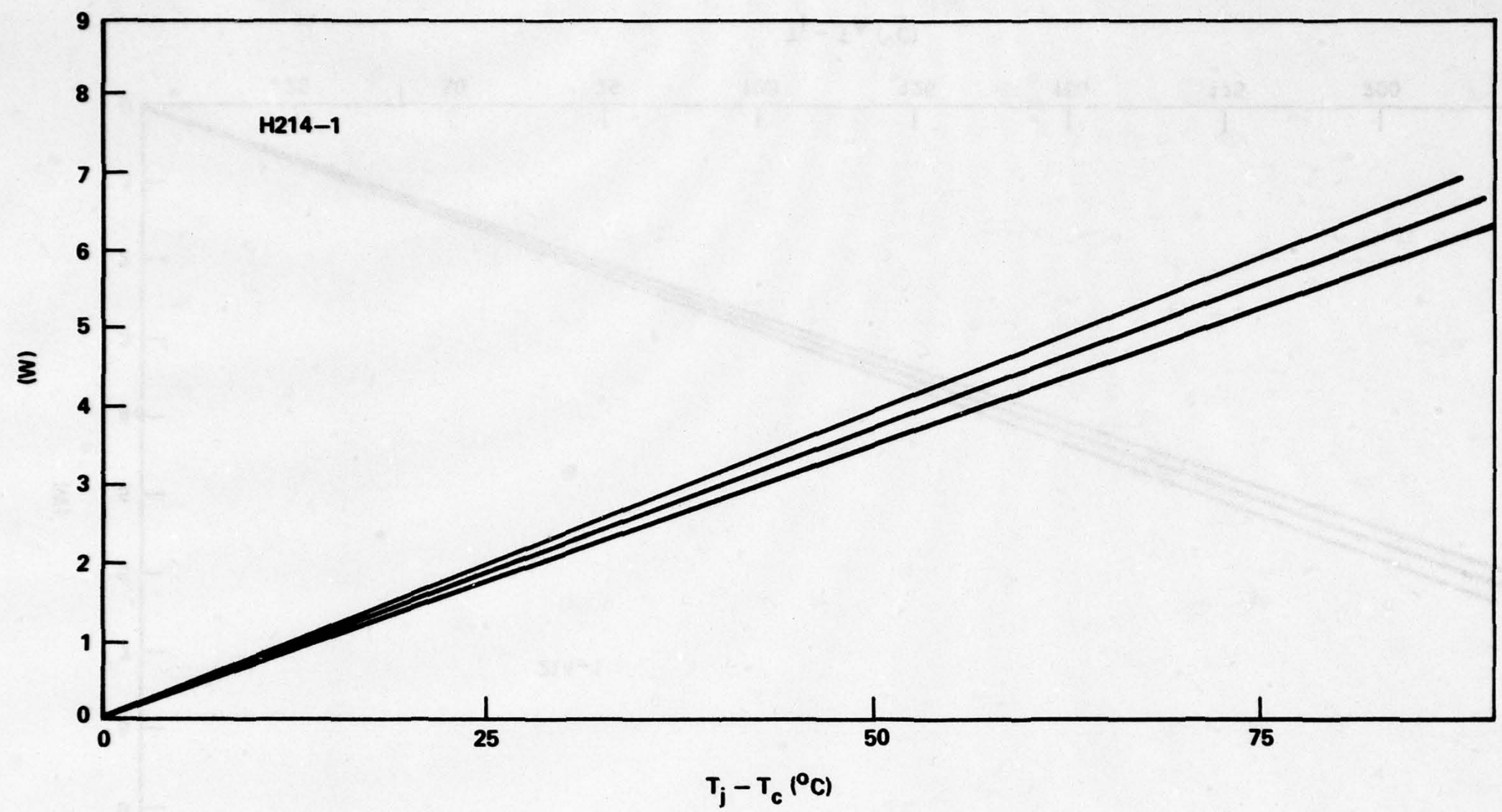

Figure 31. Circuit H214-1 junction to case.

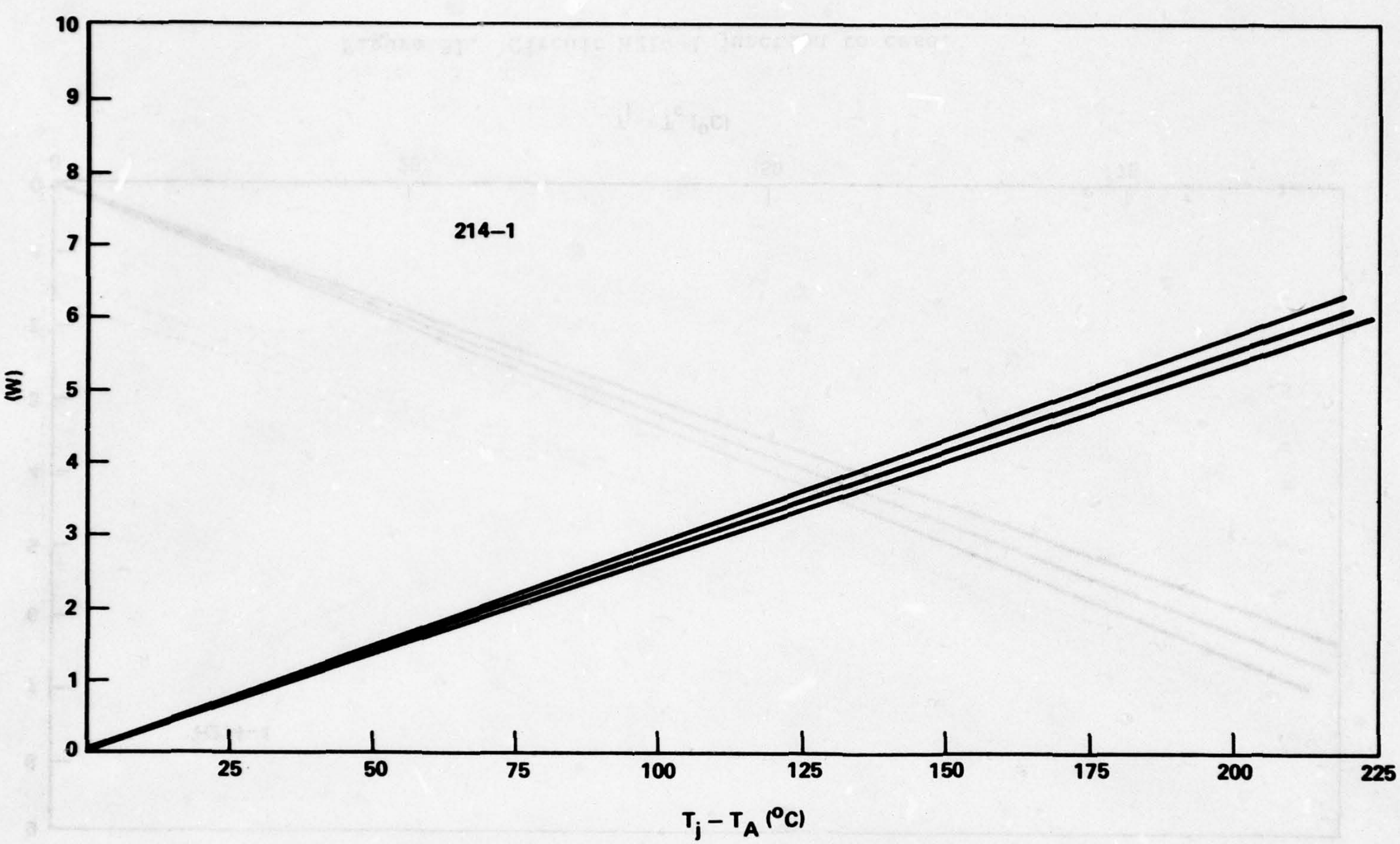

Figure 32. Circuit H214-4 junction to ambient.

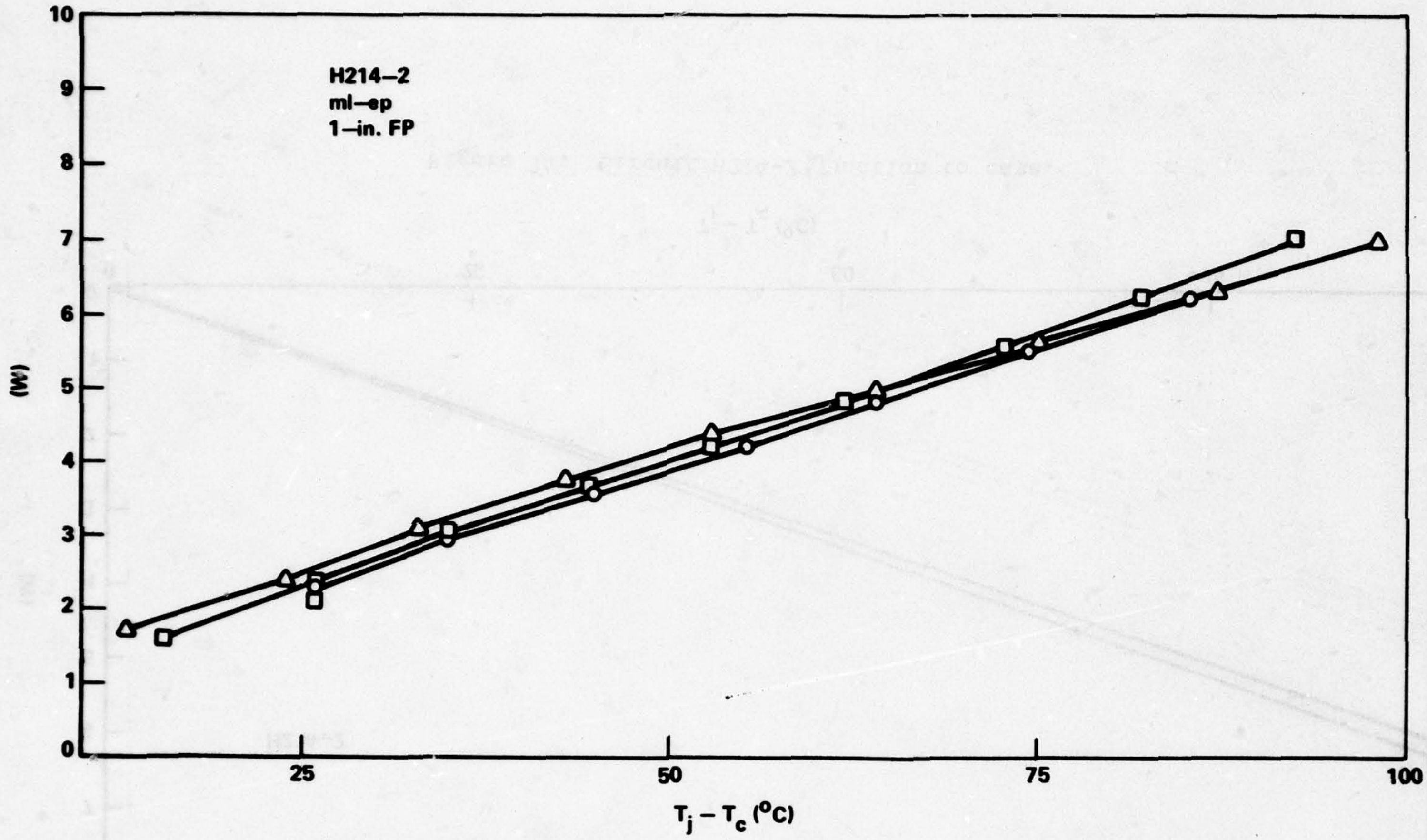

Figure 33. Circuit H214-2 raw data.

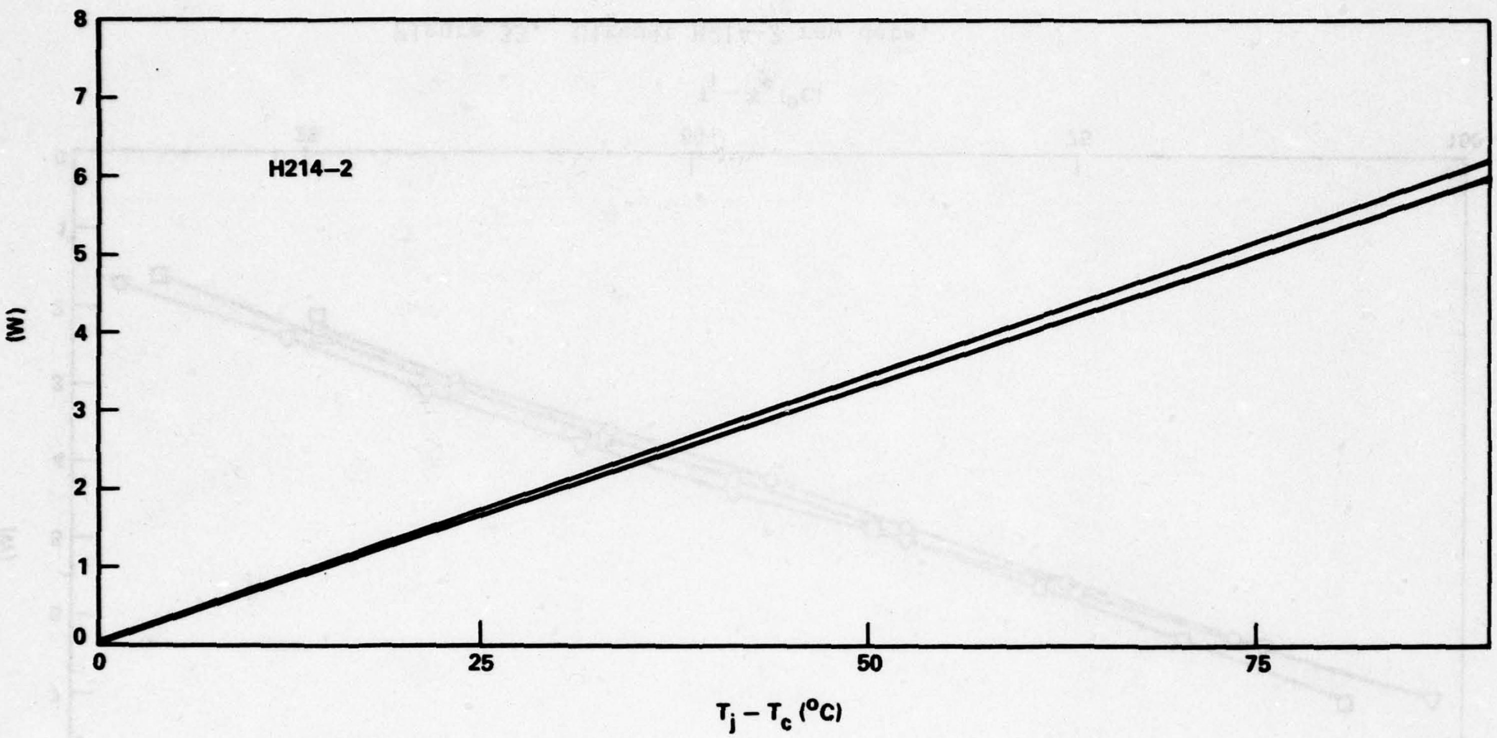

Figure 34. Circuit H214-2 junction to case.

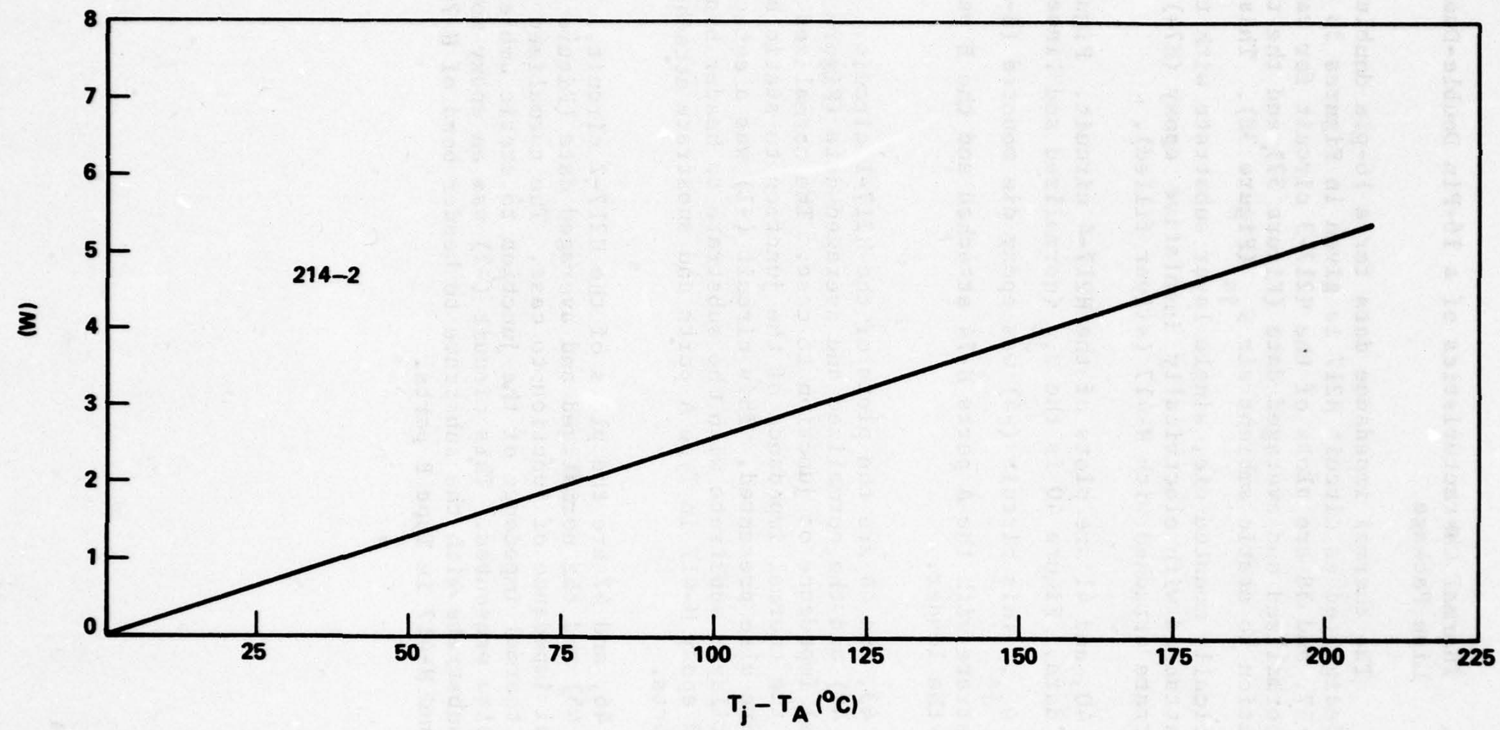

Figure 35. Circuit H214-2 junction to ambient.

3. Thermal Characteristics of a 16-Pin Double-Dual-In-Line Package

The thermal impedance data for a 16-pin double-dual in-line package designated as circuit H217 is given in Figures 36 through 47. Figures 36, 37, and 38 are plots of the H217-3 circuit for raw data (Figure 36), the normalized and averaged data (Figure 37), and the thermal impedance of junction to static ambient air θ_{ja} (Figure 38). This circuit (-3) was a eutectically mounted die, single layer substrate with the A parts substrate attached with electrically insulative epoxy (H74) and the B parts substrate attached with H-417 (silver filled).

Figures 39, 40, and 41 are plots of the H217-4 circuit. Figure 39 presents the raw data. Figure 40 is the θ_{jc} (normalized and linearized). Figure 41 is the θ_{ja}. This circuit (-4) was epoxy die mounted (H-41), single layer substrate with the A parts H-74 attached and the B parts H-417 attached to the leader.

Figures 42, 43, and 44 are the plots of the H217-1 circuit. The raw data (Figure 42) and the normalized and averaged data (Figure 43) are of the thermal impedance of junction to case. The normalized and averaged data of the thermal impedance of the junction to static ambient air (Figure 44) are also presented. This circuit (-1) was a eutectically mounted die, multilayer substrate with the substrate to header bond via silver filled epoxy H-417 in Type A parts and substrate attached with H-74 in Type B parts.

Figures 45, 46, and 47 are the plots of the H217-2 circuit. The raw data (Figure 45) and the normalized and averaged data (Figure 44) are of the thermal impedance of junction to case. The normalized and averaged data of thermal impedance of the junction to static ambient air (Figure 47) are also presented. This circuit (-2) was an epoxy mounted die, multilayer substrate with the substrate to header bond of H-74 in Type A parts and H-417 in Type B parts.

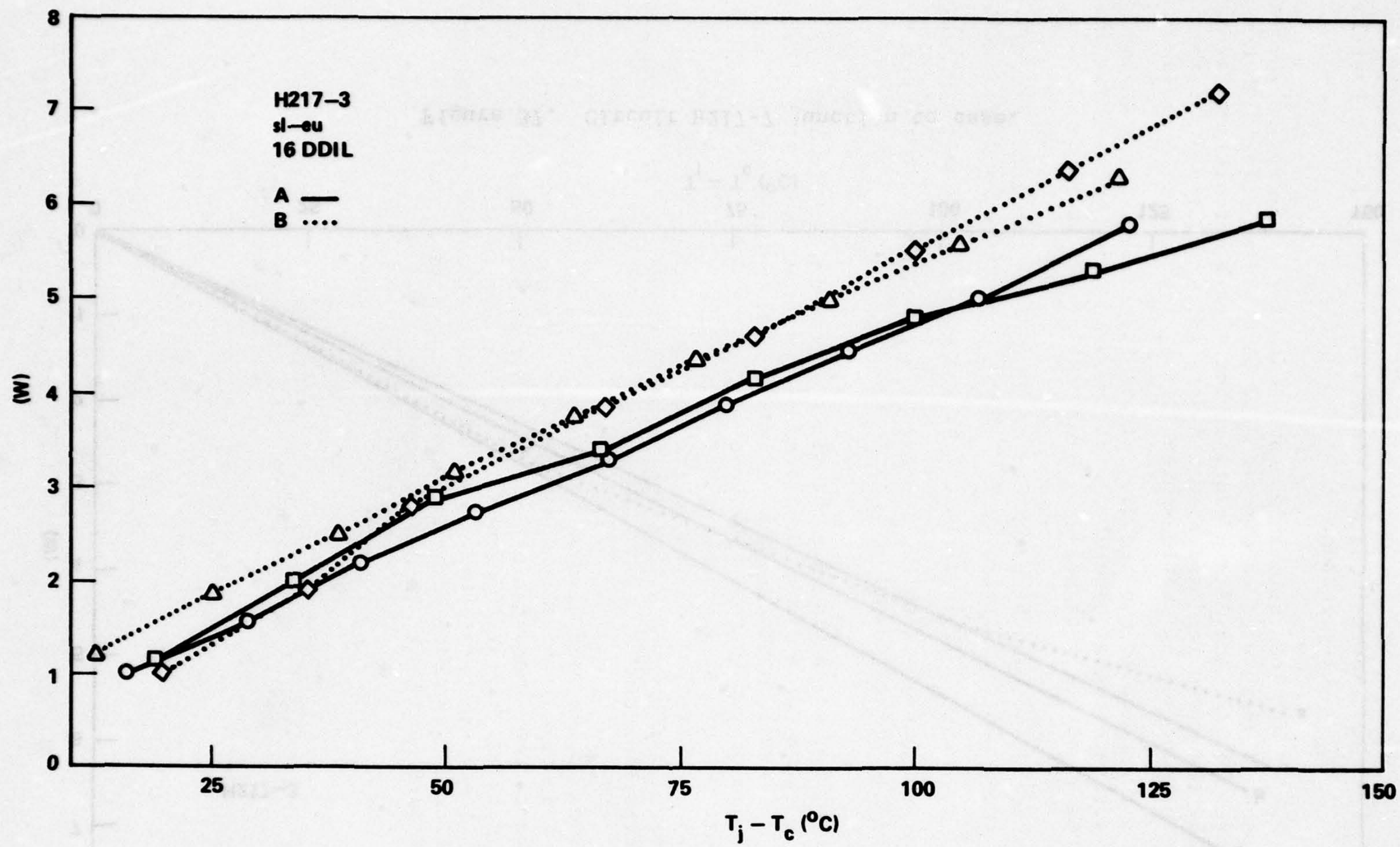

Figure 36. Circuit H217-3 raw data.

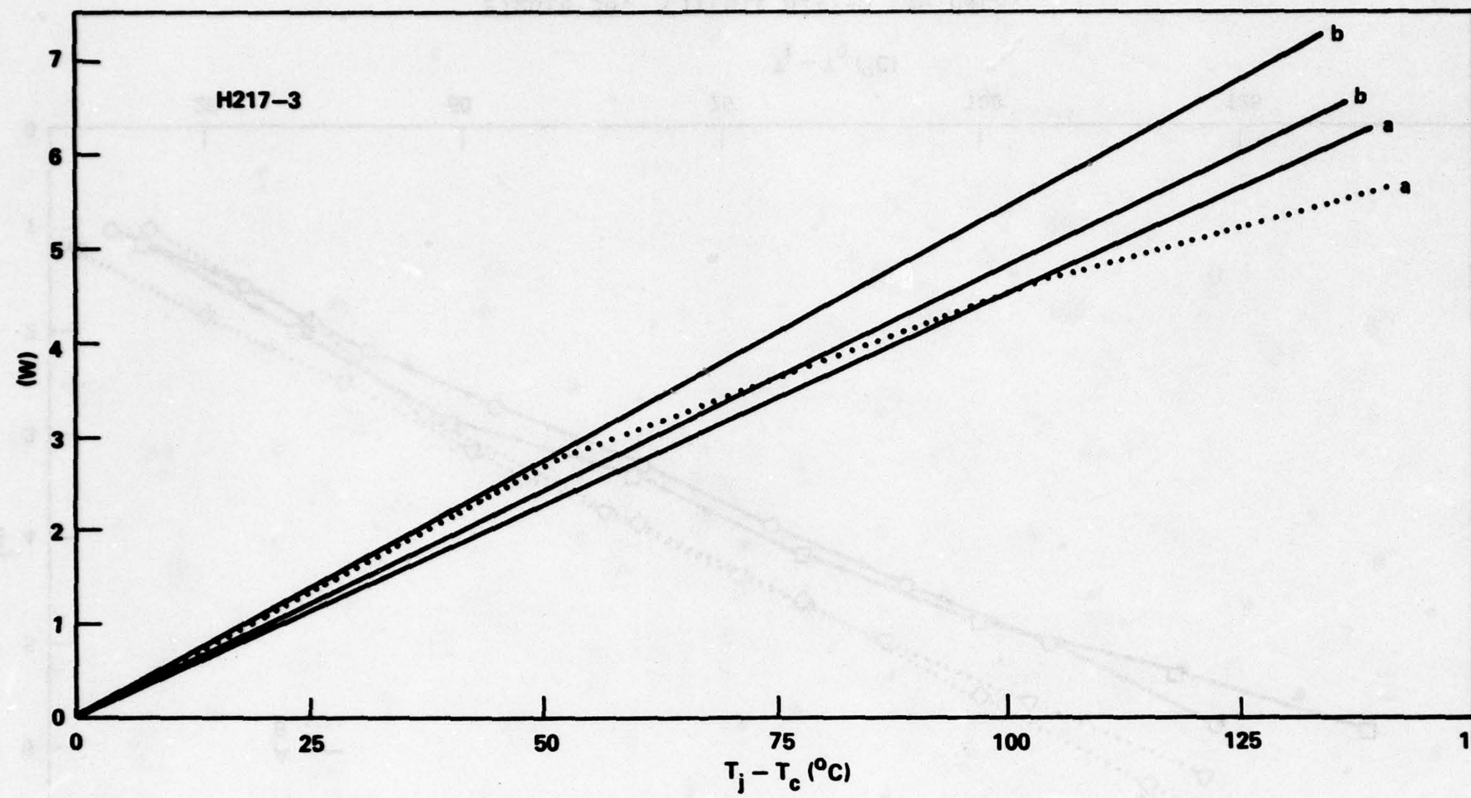

Figure 37. Circuit H217-7 junction to case.

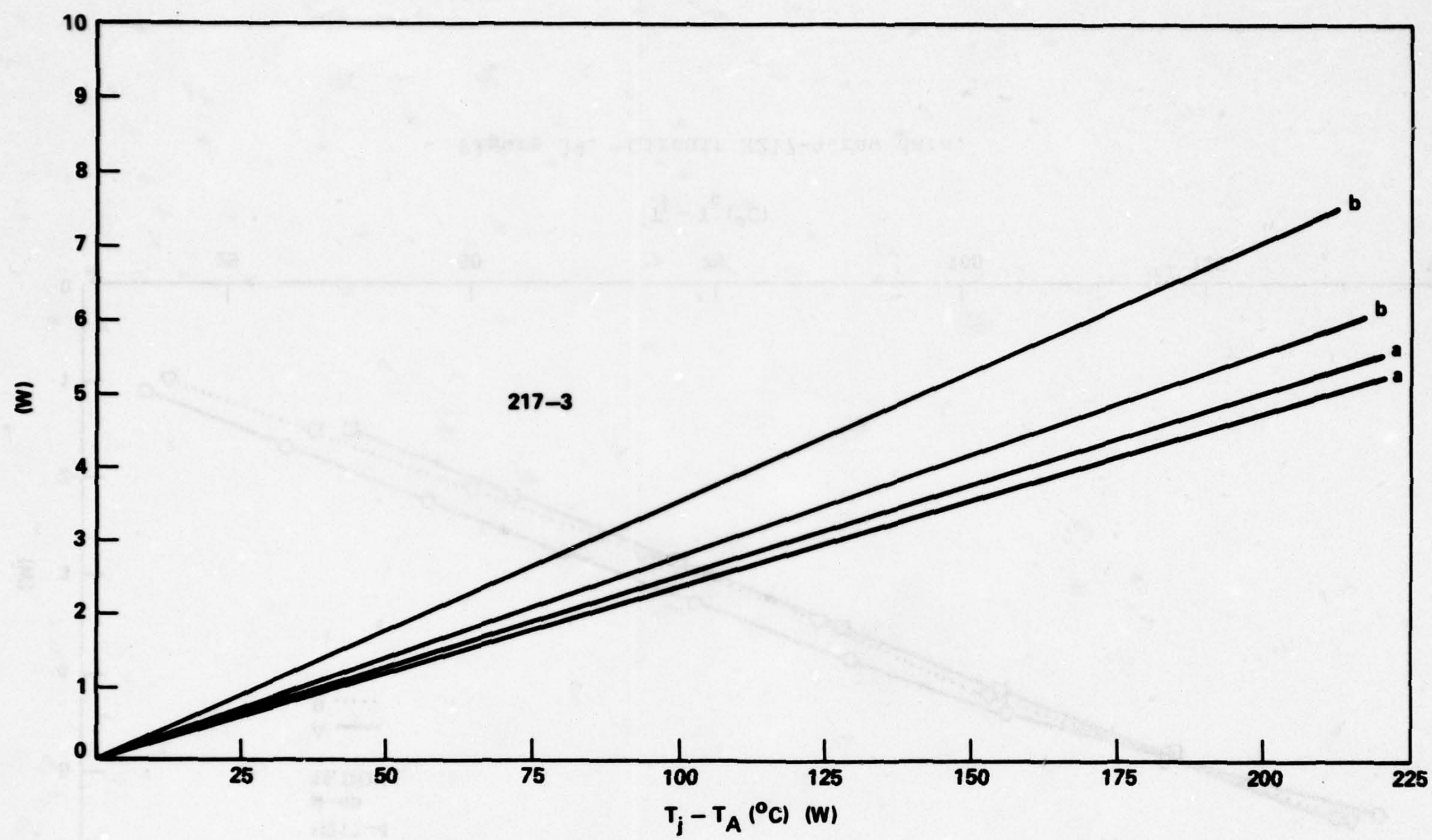

Figure 38. Circuit H217-3 junction to ambient.

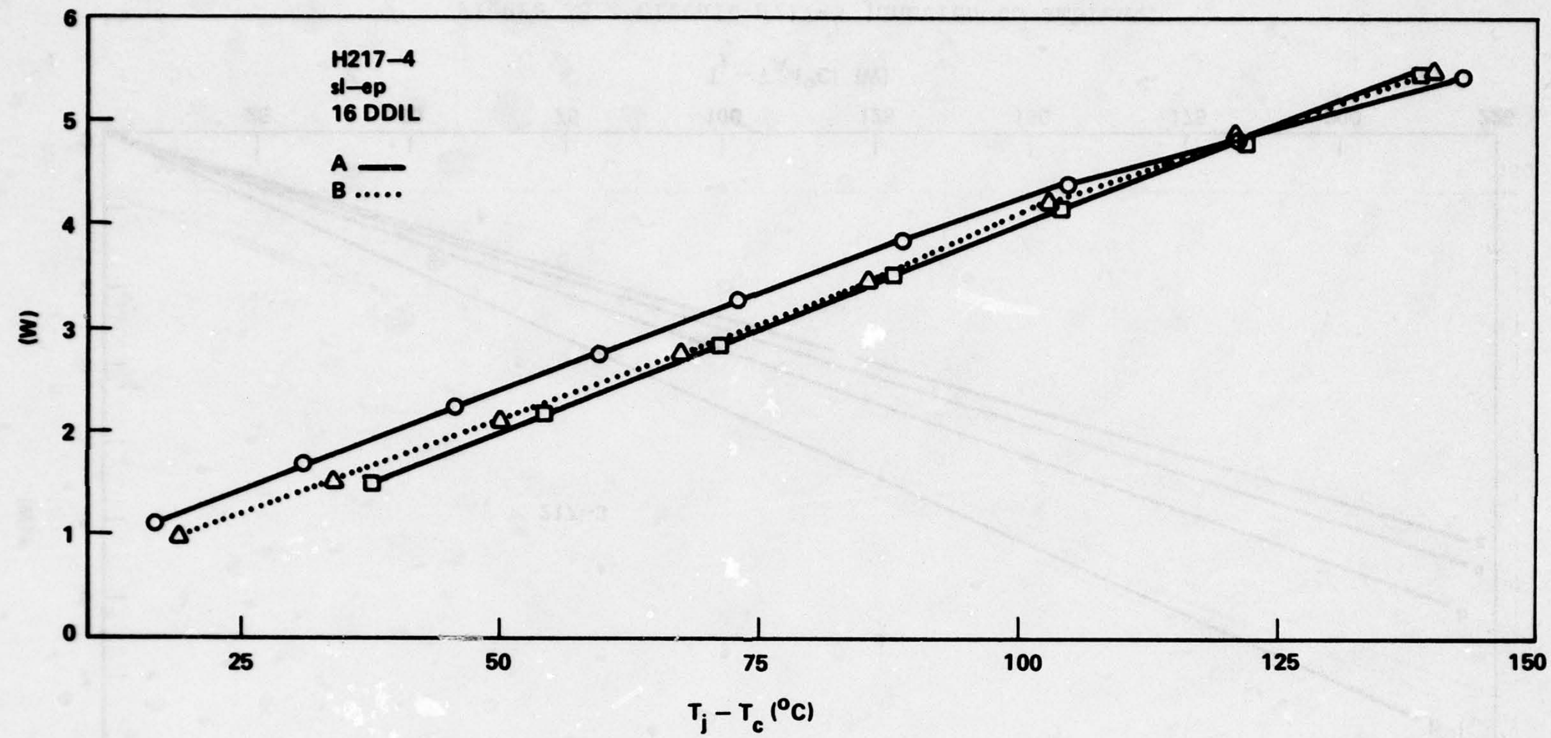

Figure 39. Circuit H217-4 raw data.

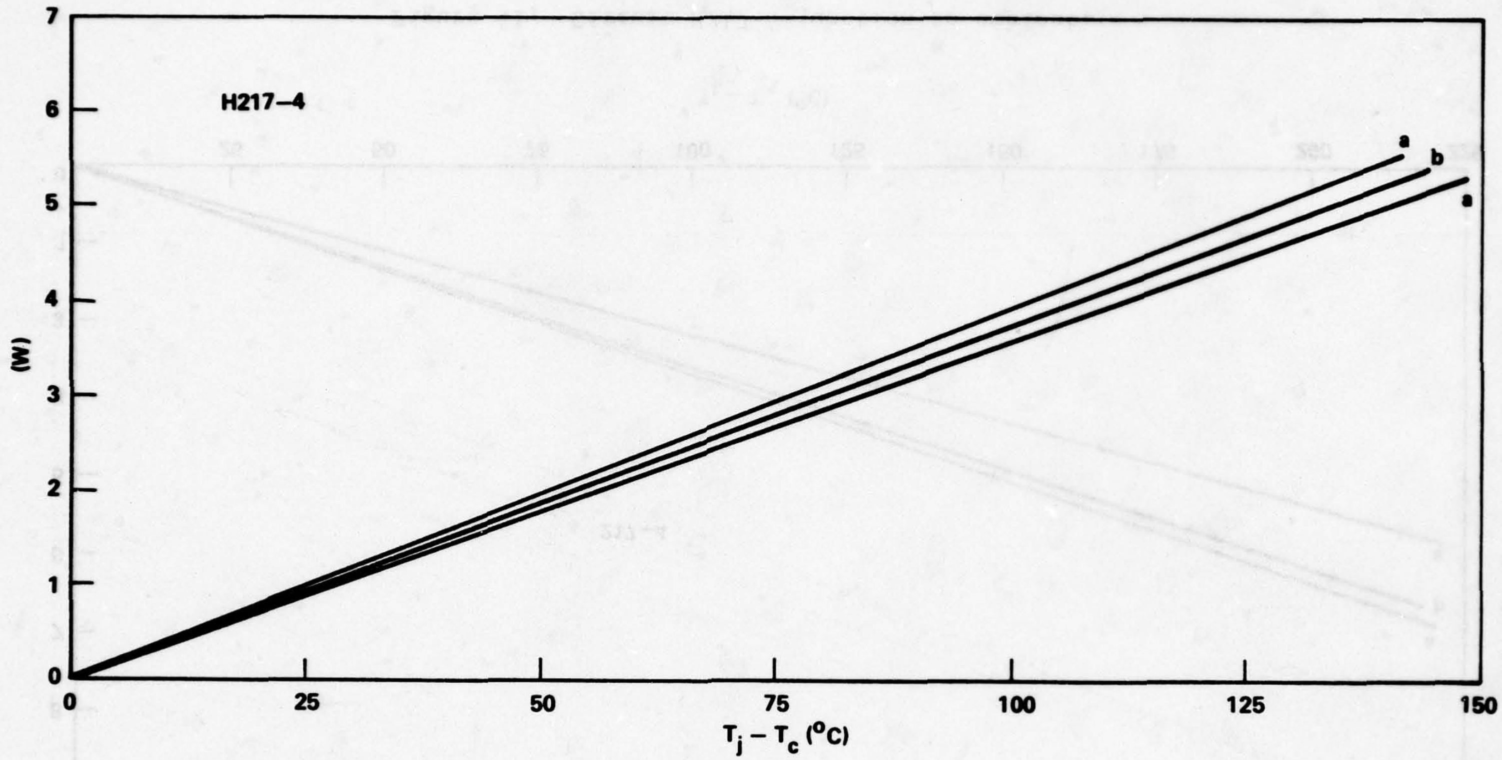

Figure 40. Circuit H217-4 junction to case.

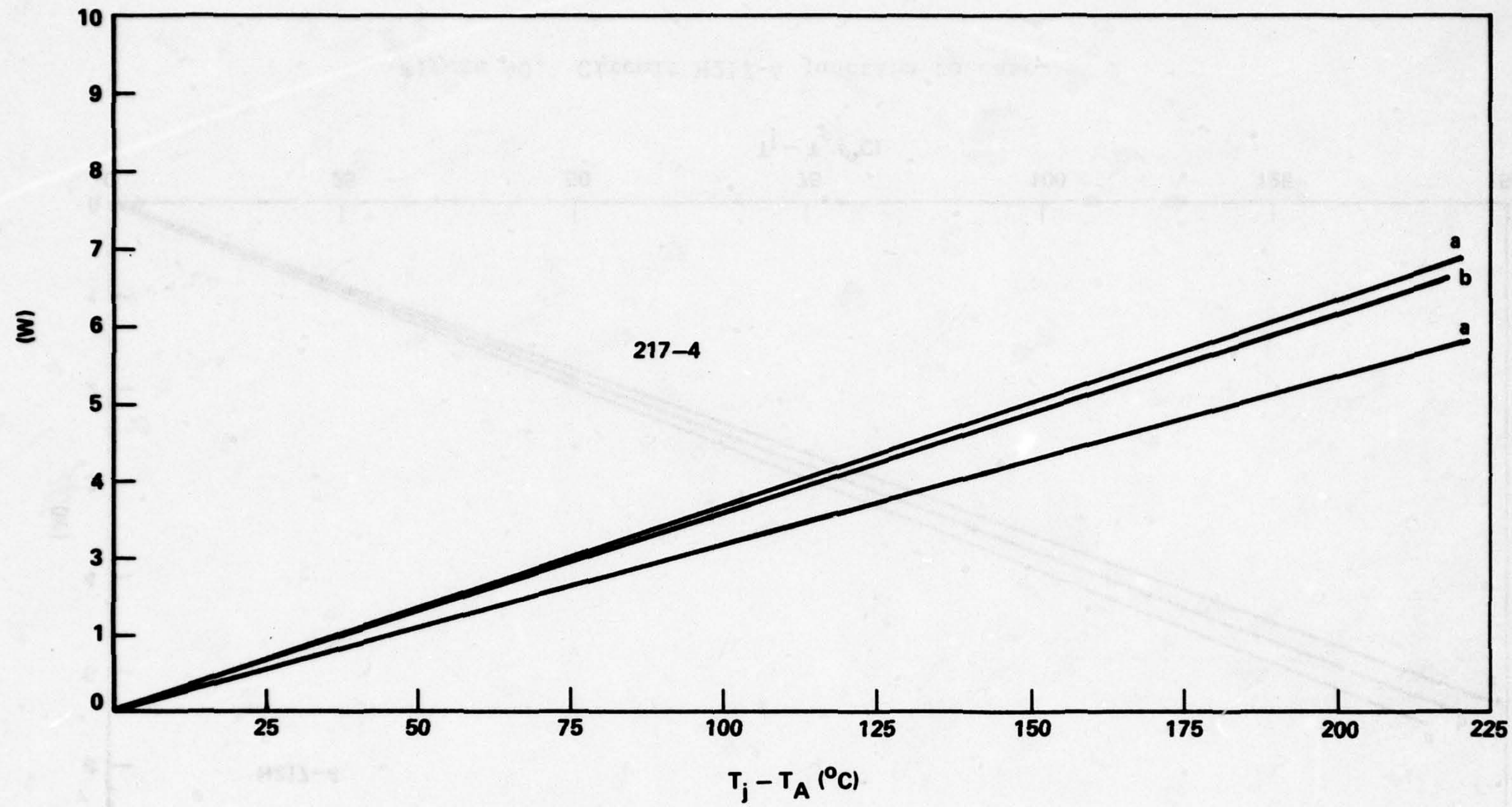

Figure 41. Circuit H217-4 junction to ambient.

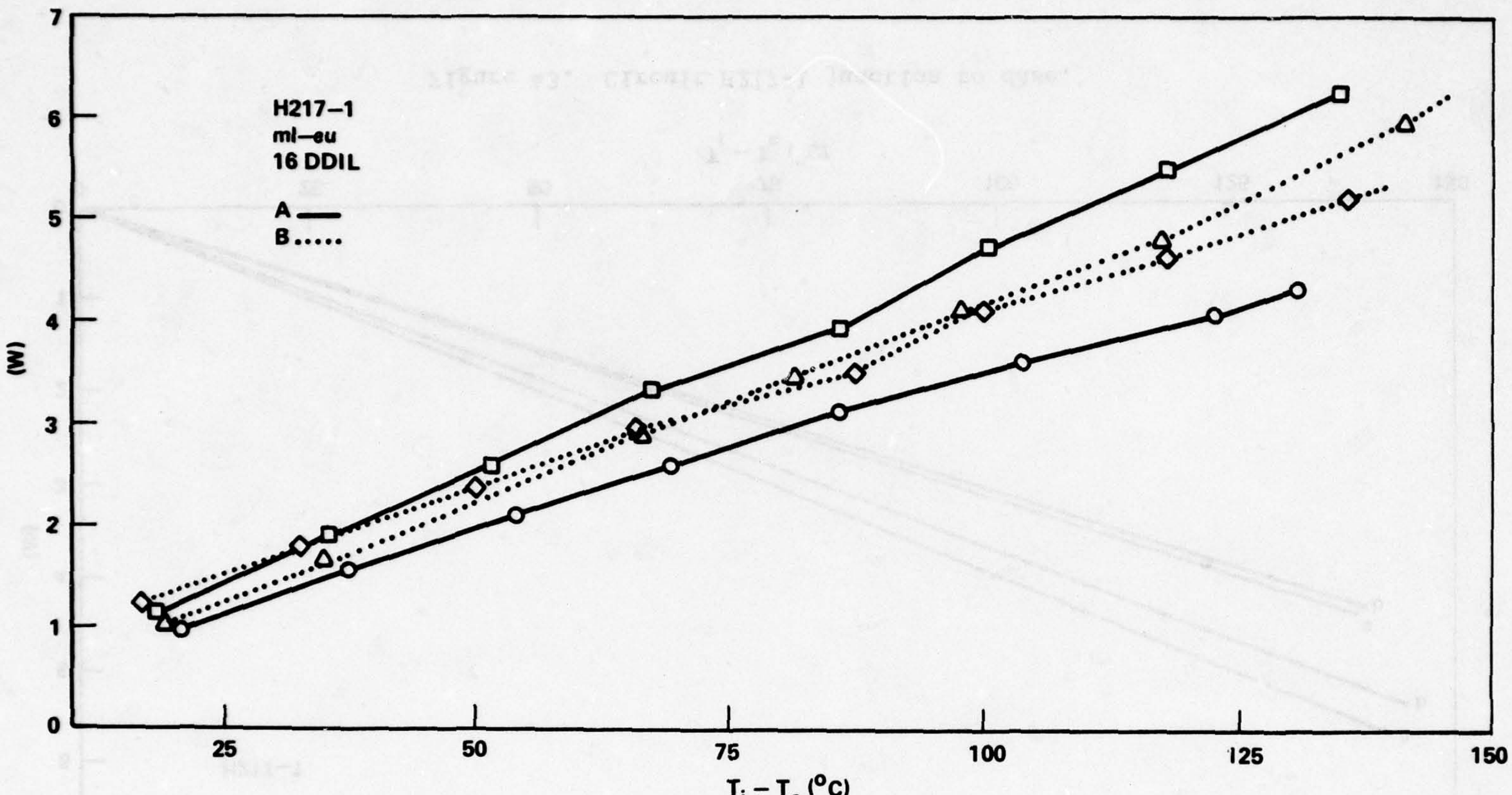

Figure 42. Circuit H217-1 raw data.

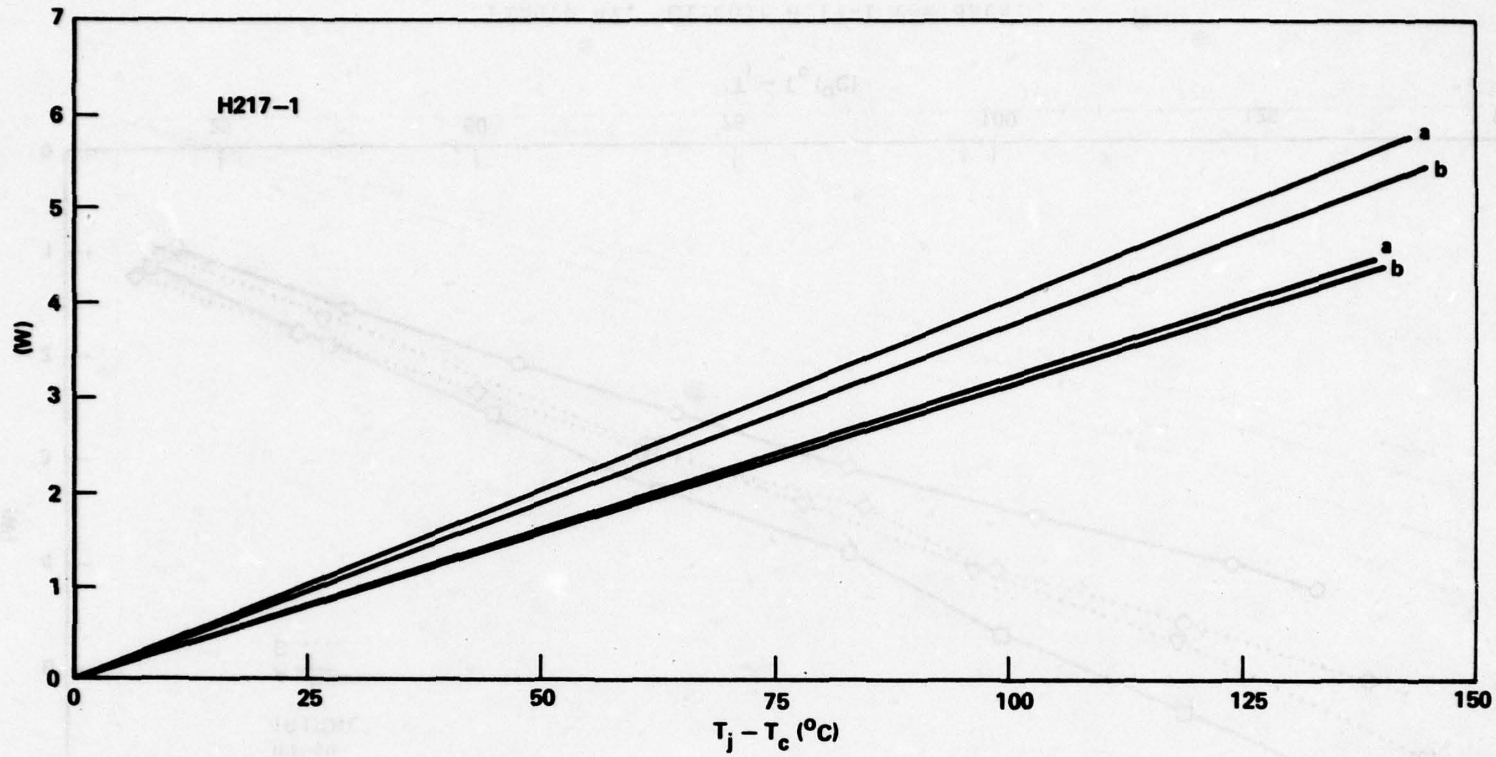

Figure 43. Circuit H217-1 junction to case.

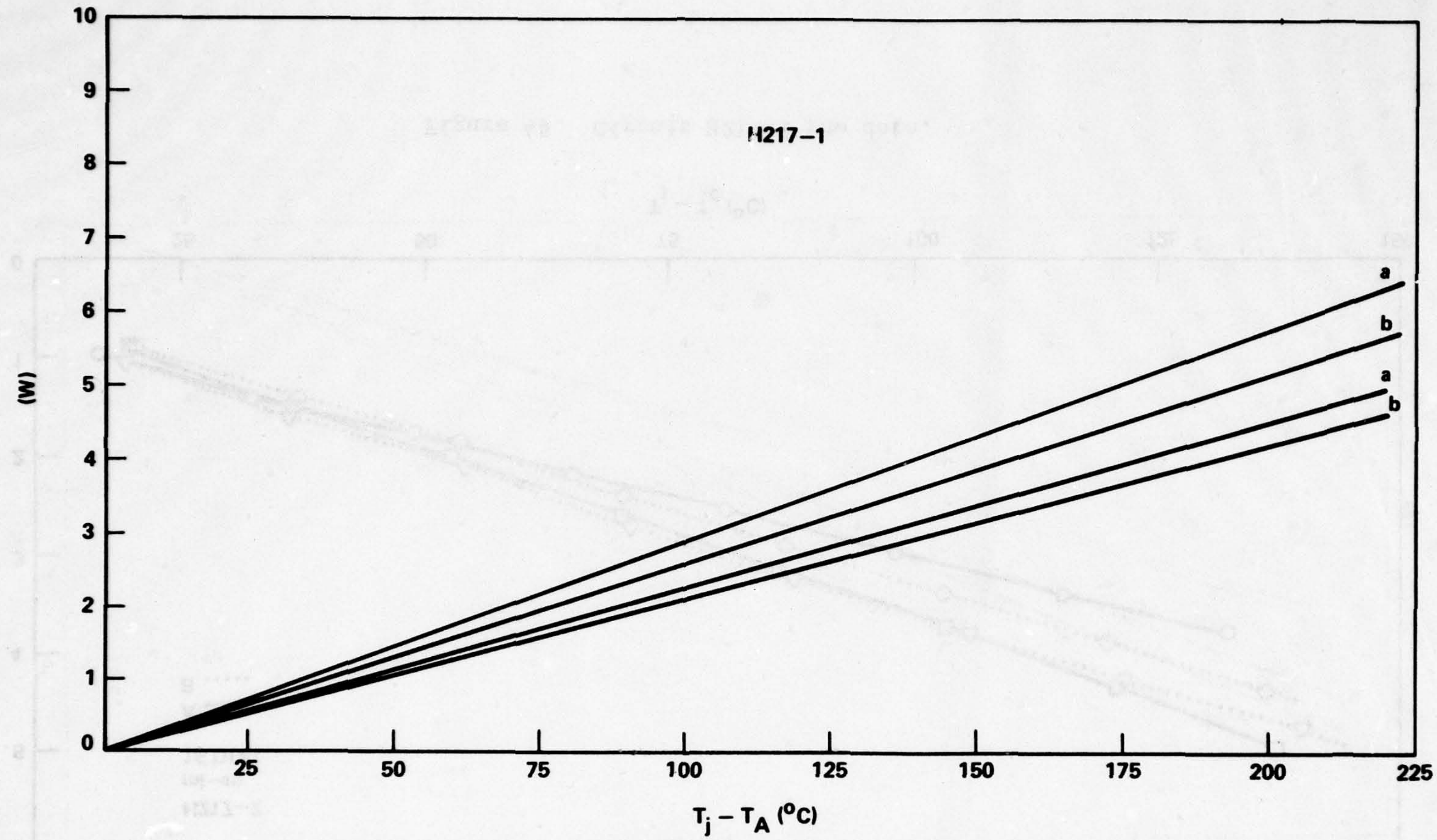

Figure 44. Circuit H217-1 junction to ambient.

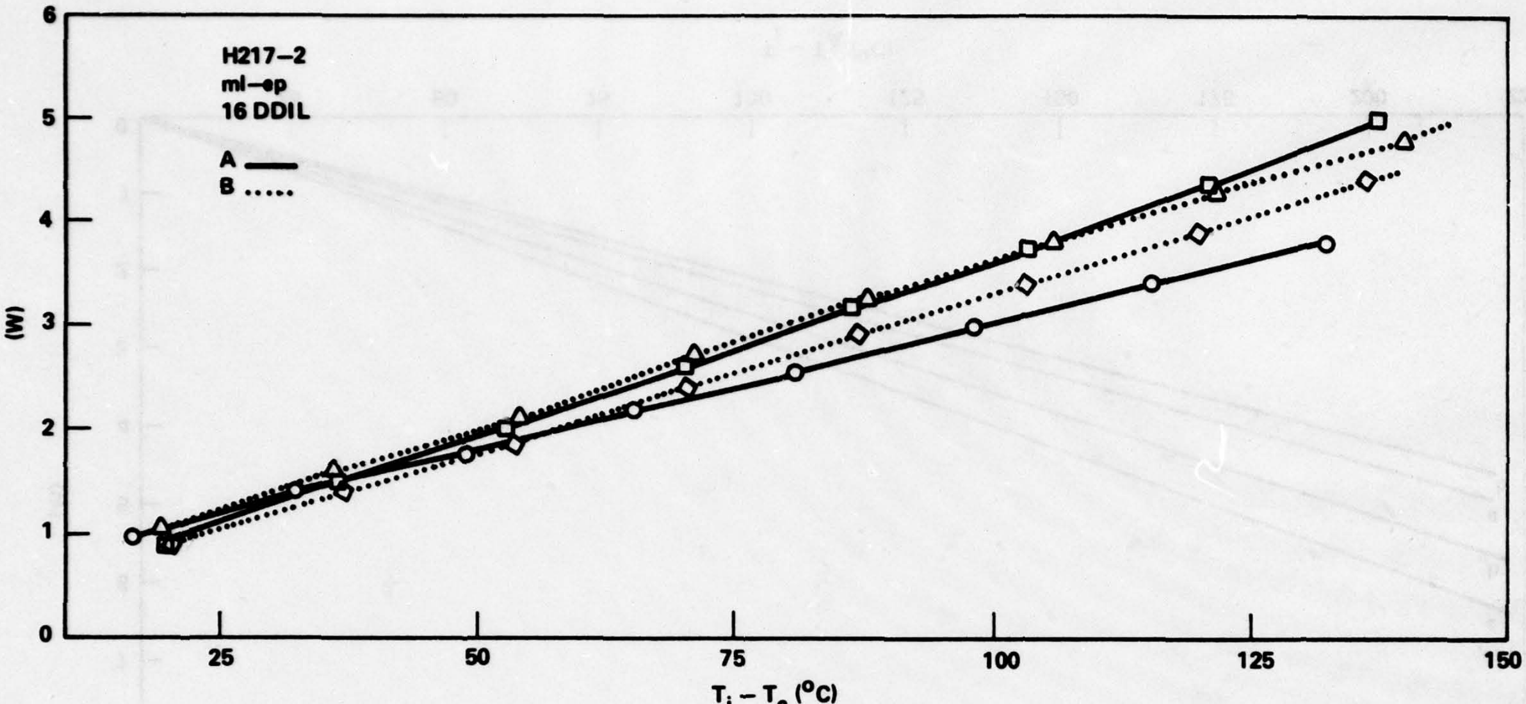

Figure 45. Circuit H217-2 raw data.

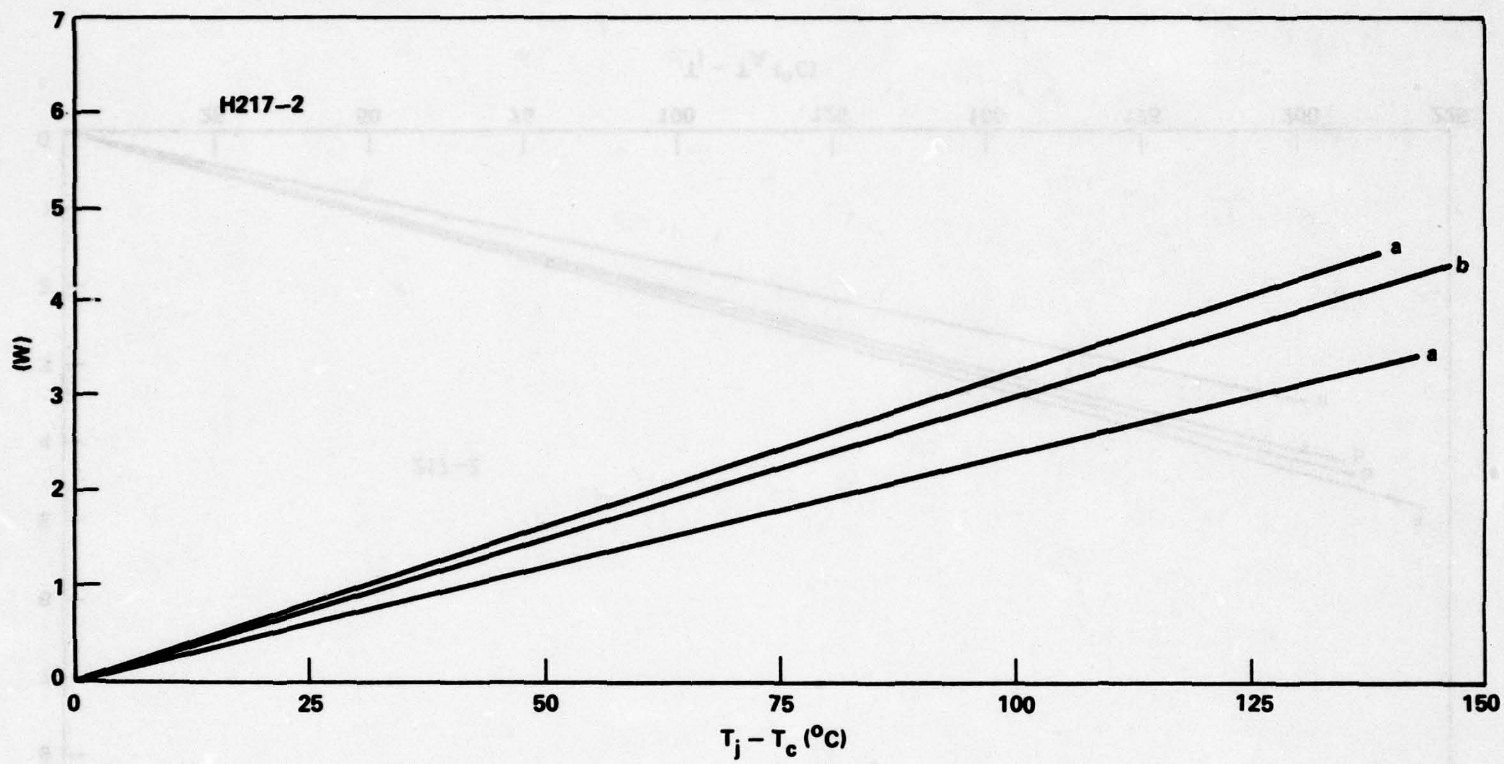

Figure 46. Circuit H217-2 junction to case.

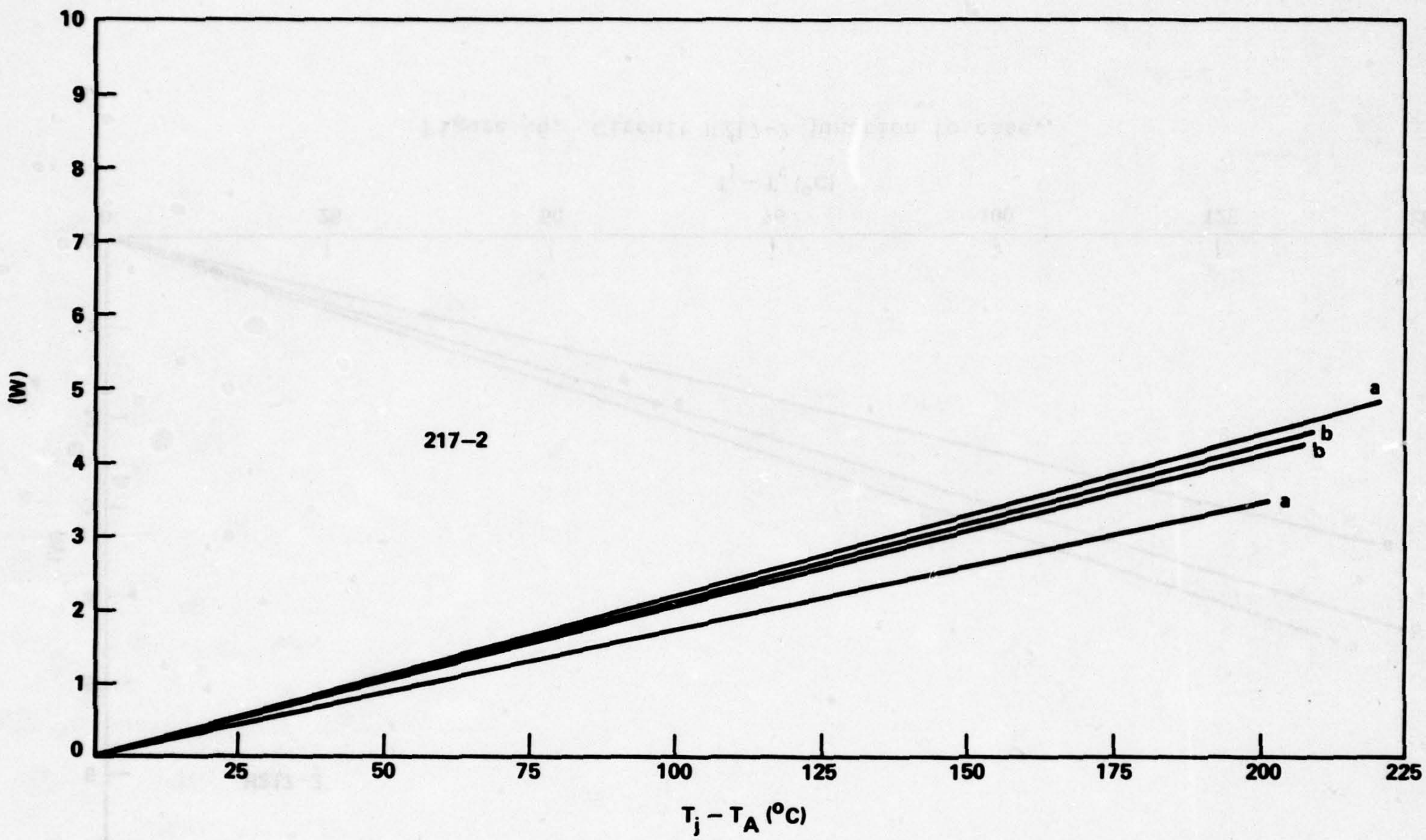

Figure 47. Circuit H217-2 junction to ambient.

4. Thermal Characteristics of a 24-Pin Double Dual In-Line Package

The thermal impedance data for a 24-pin double-dual in-line package designated as circuit H216 are given in Figures 48 through 59. Figures 48, 49, and 50 are plots of the H216-3 circuit for the raw data (Figure 48), the normalized and averaged data (Figure 49), and the thermal impedance of junction to static ambient air θ_{ja} (Figure 50). This circuit (-3) was a eutectically mounted die, single layer substrate with the A parts substrate attached with electrically insulative epoxy (H-74) and the B parts substrate attached with H-417.

Figures 51, 52, and 53 are plots of the H216-4 circuit. Figure 51 presents the raw data. Figure 52 is the θ_{jc} (normalized and linearized). Figure 53 is the thermal impedance of junction to static ambient air. This circuit (-4) was epoxy die mounted (H-4) single layer substrate with A parts H-74 attached and B parts H417 attached to the header.

Figures 54, 55, and 56 are the plots of the H 216-1 circuit. The raw data (Figure 54) and the normalized and averaged data (Figure 55) are of the thermal impedance of junction to case. The normalized and average data of the thermal impedance of the junction to static ambient air (Figure 56) are also presented. This circuit (-1) was a eutectically mounted die, multilayer substrate with the substrate to header bond via silver filled epoxy for Part B and H-74 for Part A.

Figures 57, 58, and 59 are the plots of the H216-2 circuit. The raw data (Figure 57) and the normalized and averaged data (Figure 58) are of the thermal impedance of junction to case. The normalized and averaged data of the thermal impedance of the junction to static ambient air (Figure 59) are also presented. This circuit (-2) was an epoxy mounted die, multilayer substrate with the substrate to header bond of H-74 in Type A parts and H-417 in Type B parts.

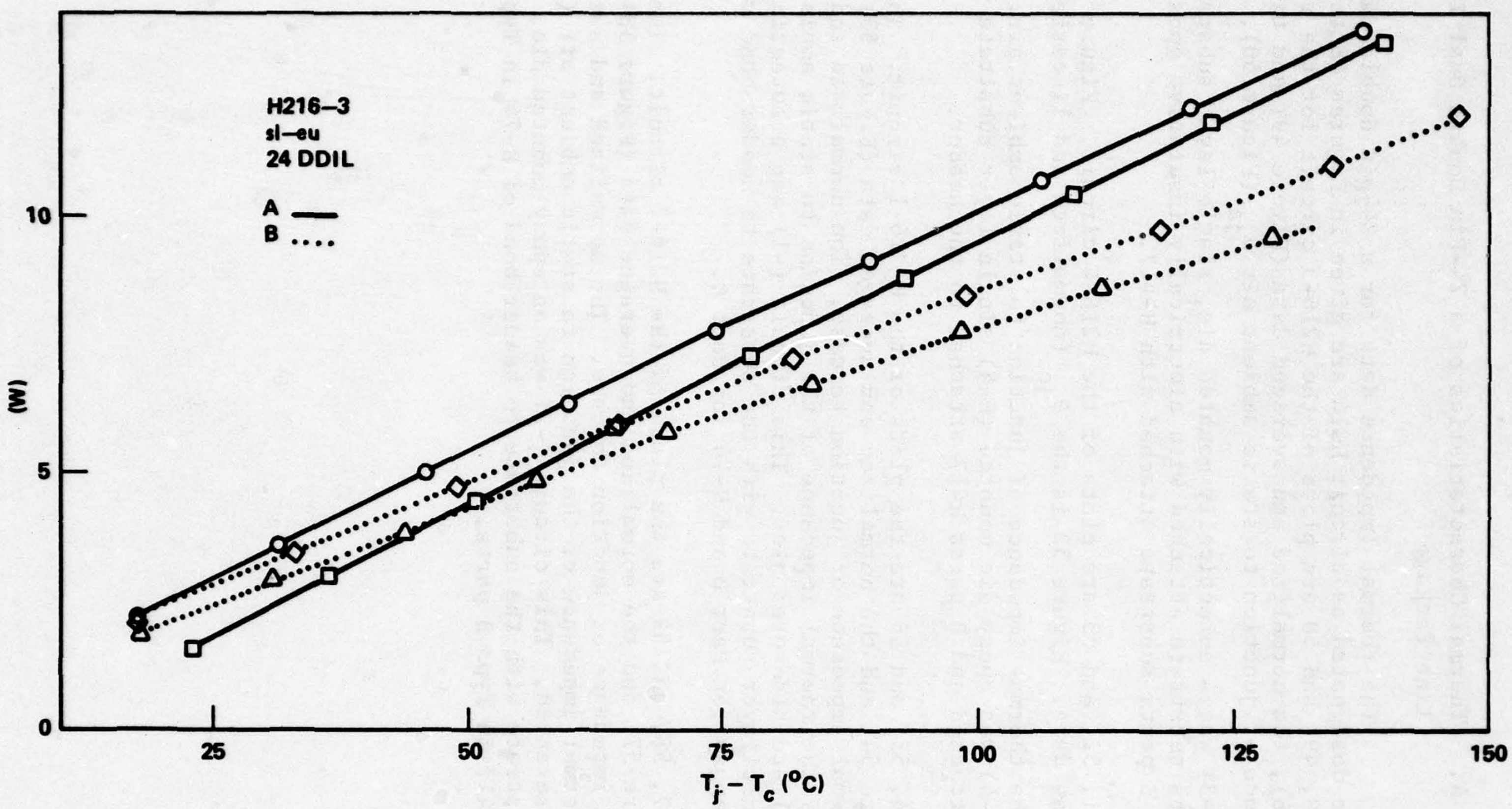

Figure 48. Circuit H216-3 raw data.

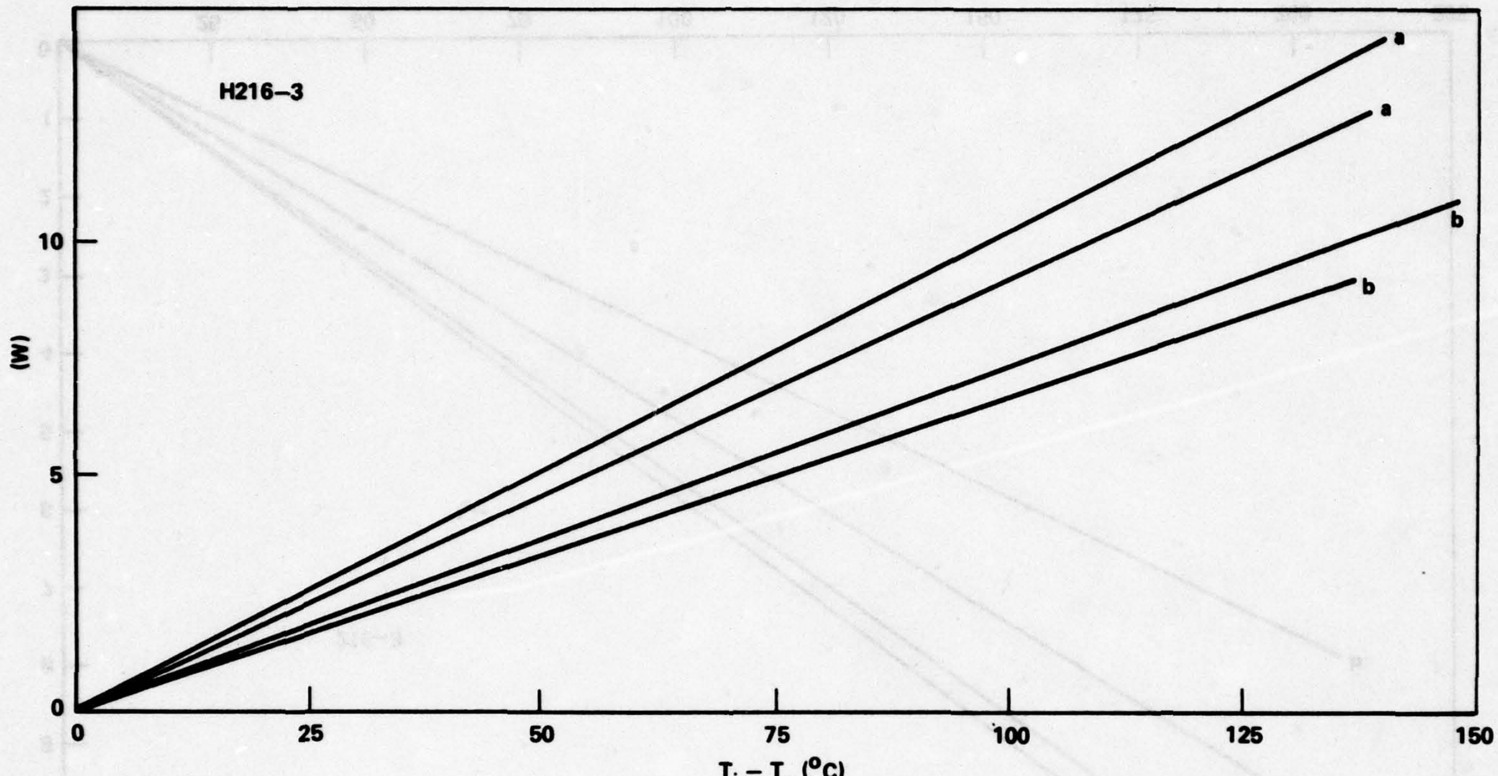

Figure 49. Circuit H216-3 junction to case.

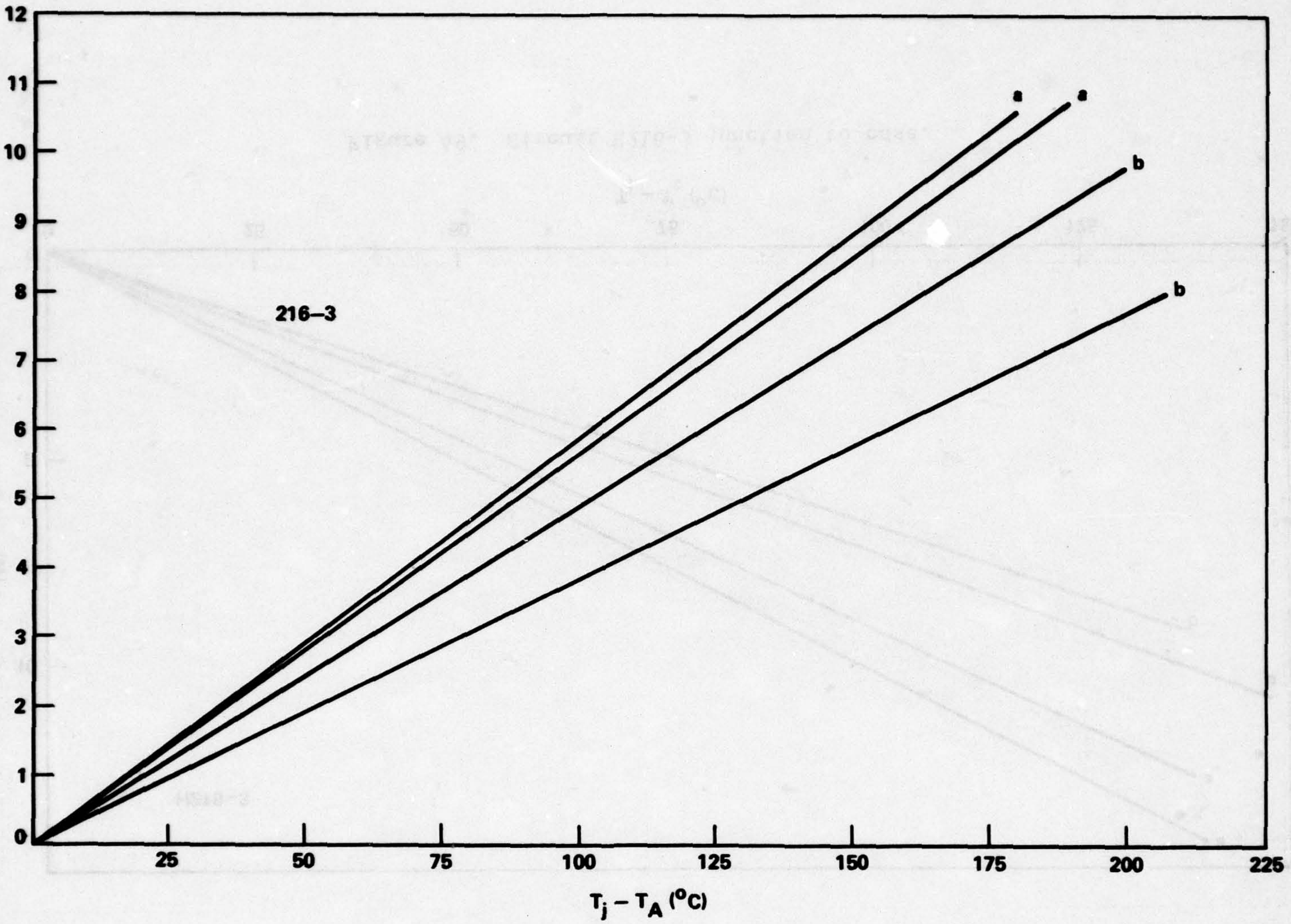

Figure 50. Circuit H216-3 junction to ambient.

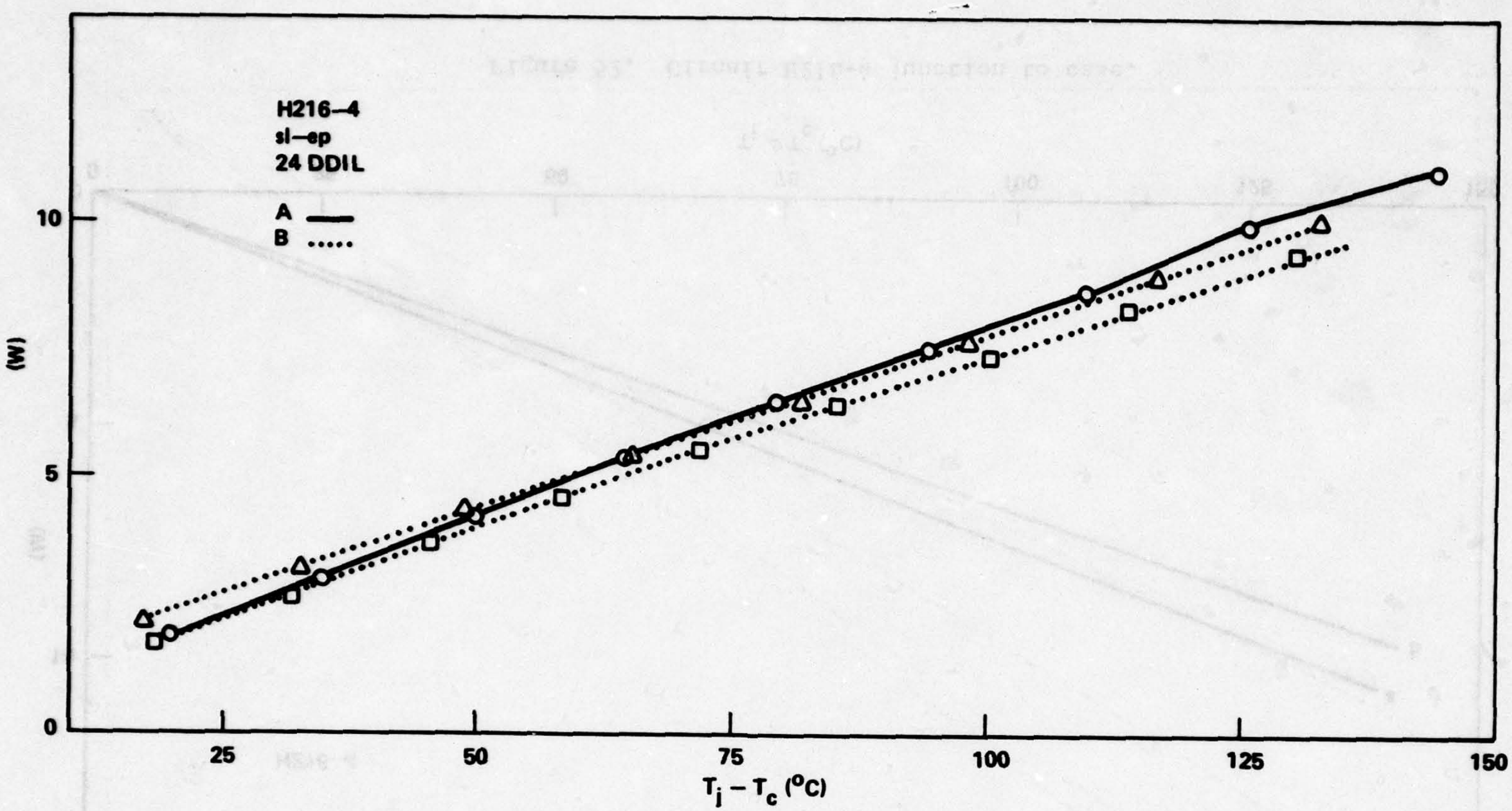

Figure 51. Circuit H216-4 raw data.

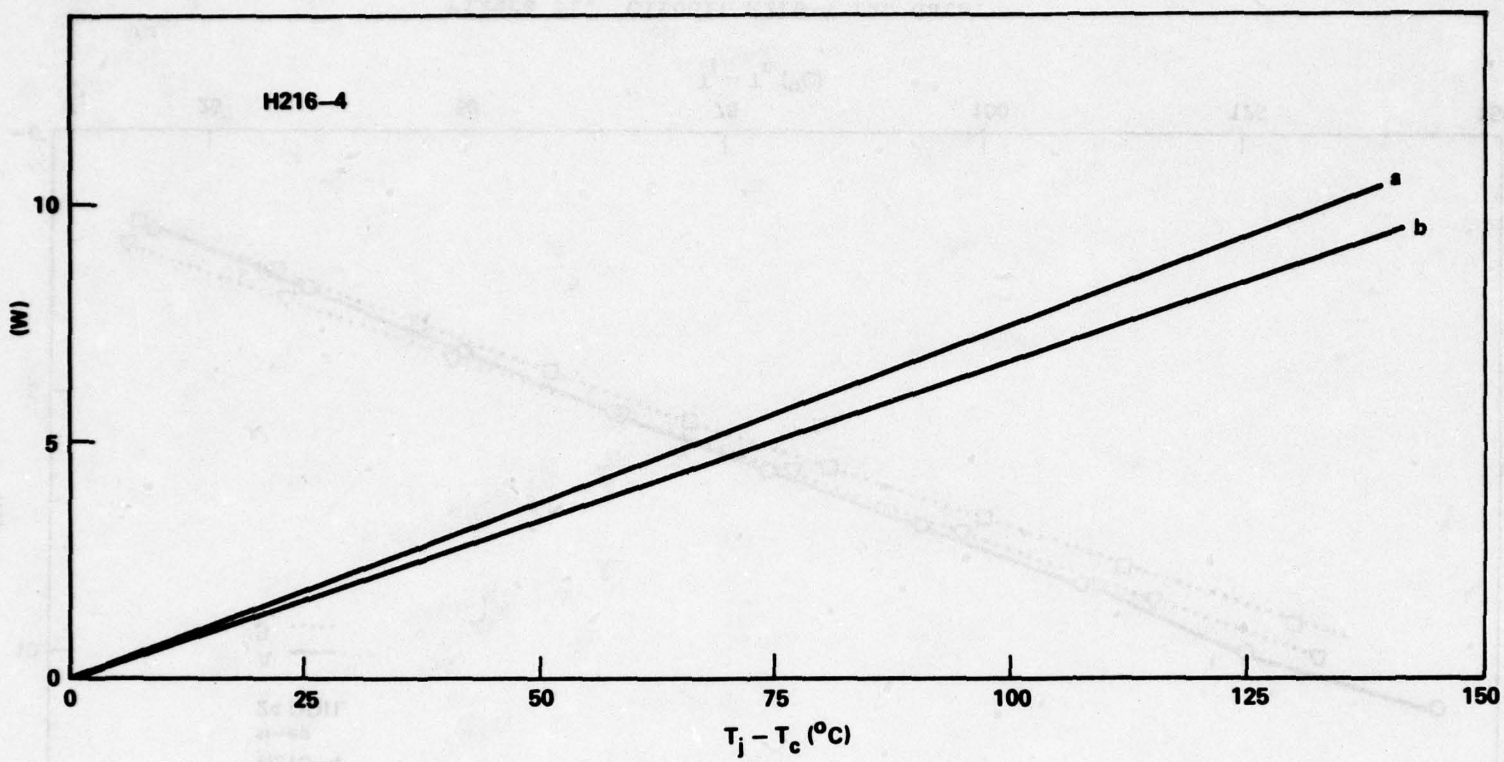

Figure 52. Circuit H216-4 junction to case.

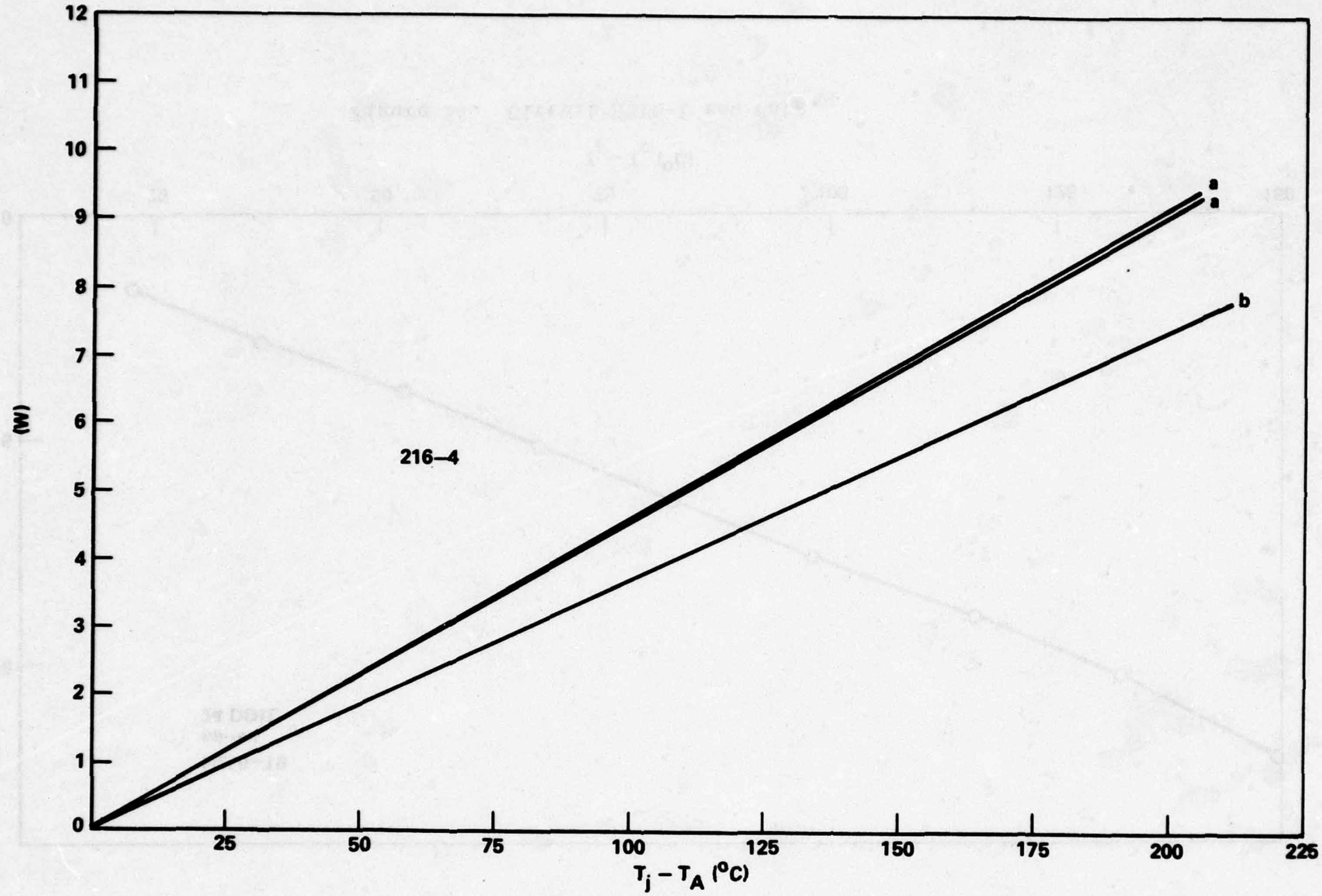

Figure 53. Circuit H216-4 junction to ambient.

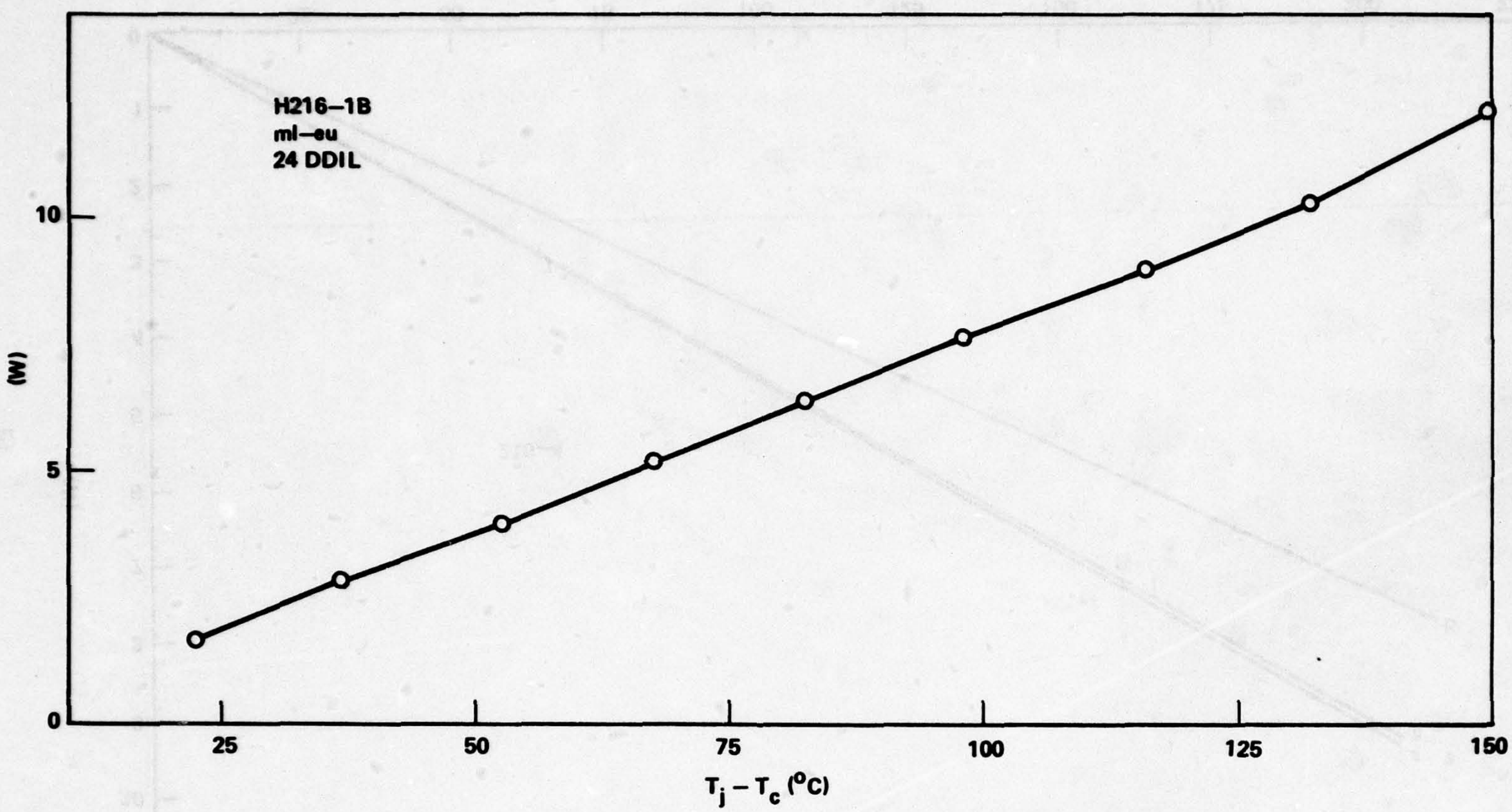

Figure 54. Circuit H216-1 raw data.

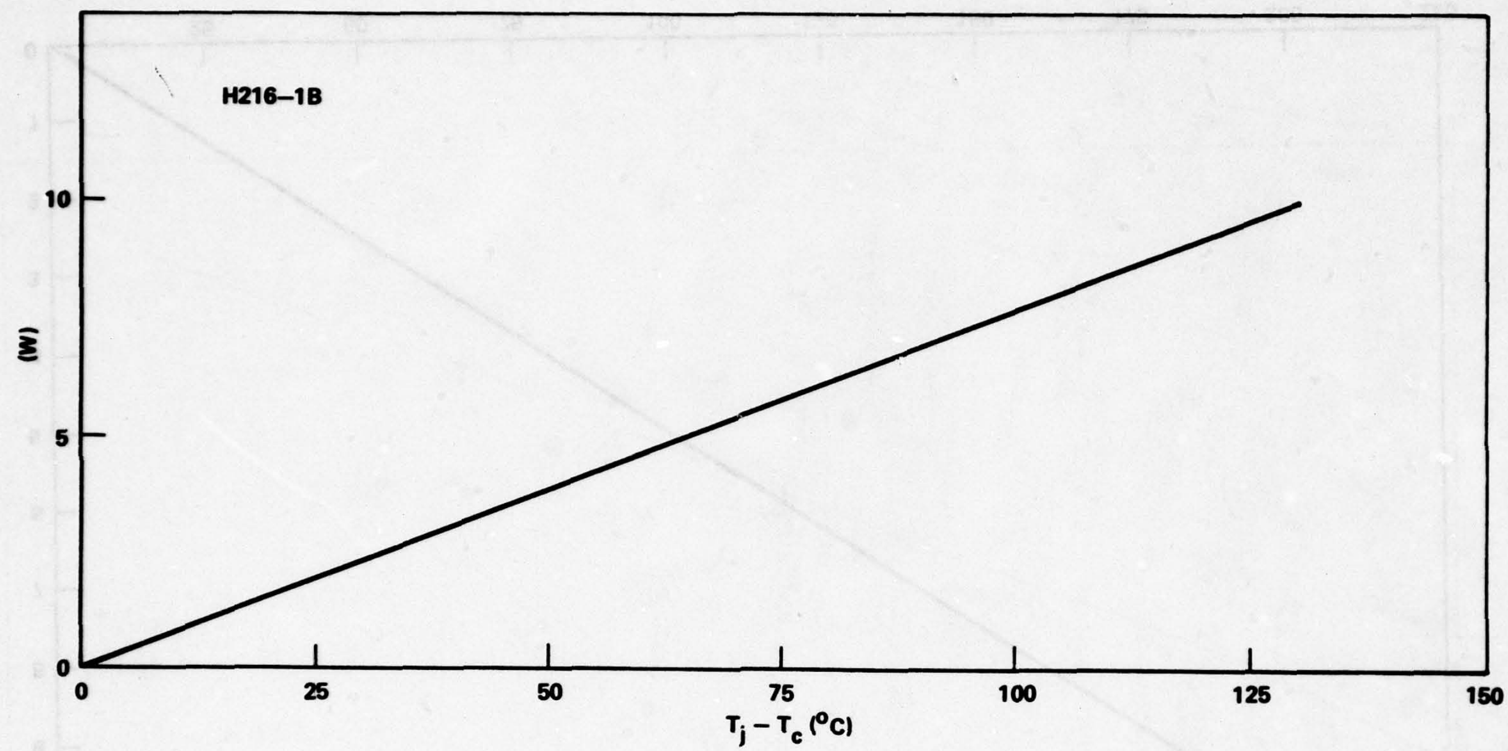

Figure 55. Circuit H216-1 junction to case.

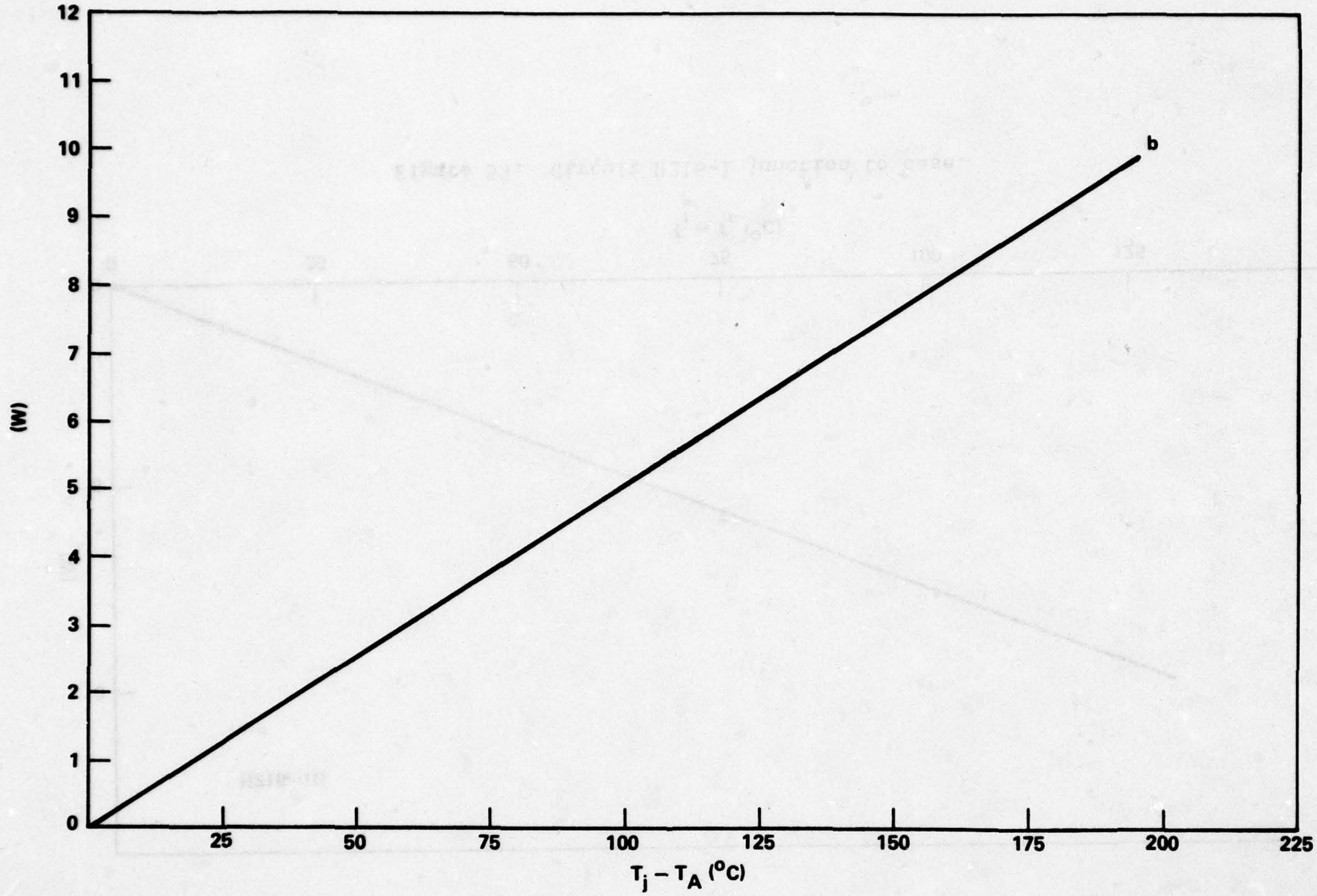

Figure 56. Circuit H216-1 junction to ambient.

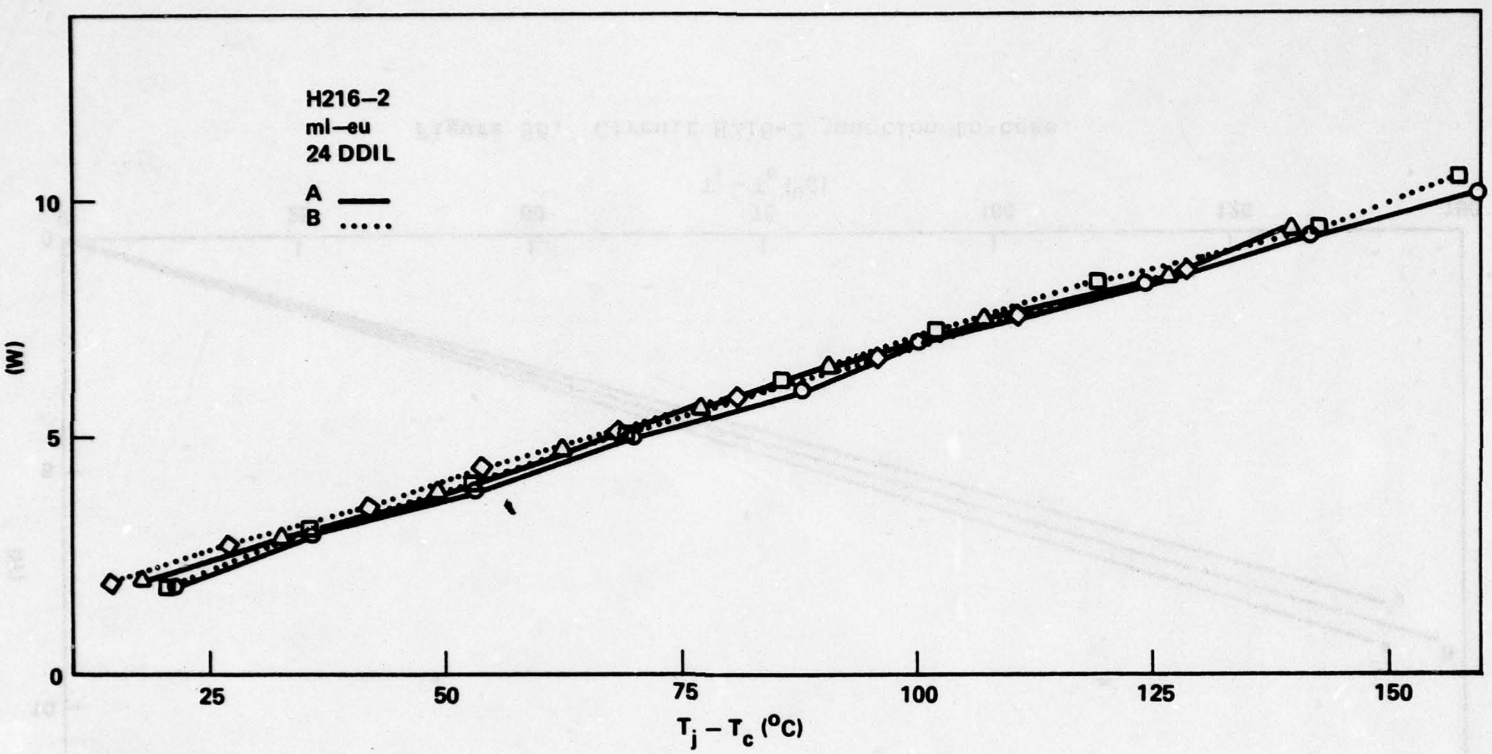

Figure 57. Circuit H216-2 raw data.

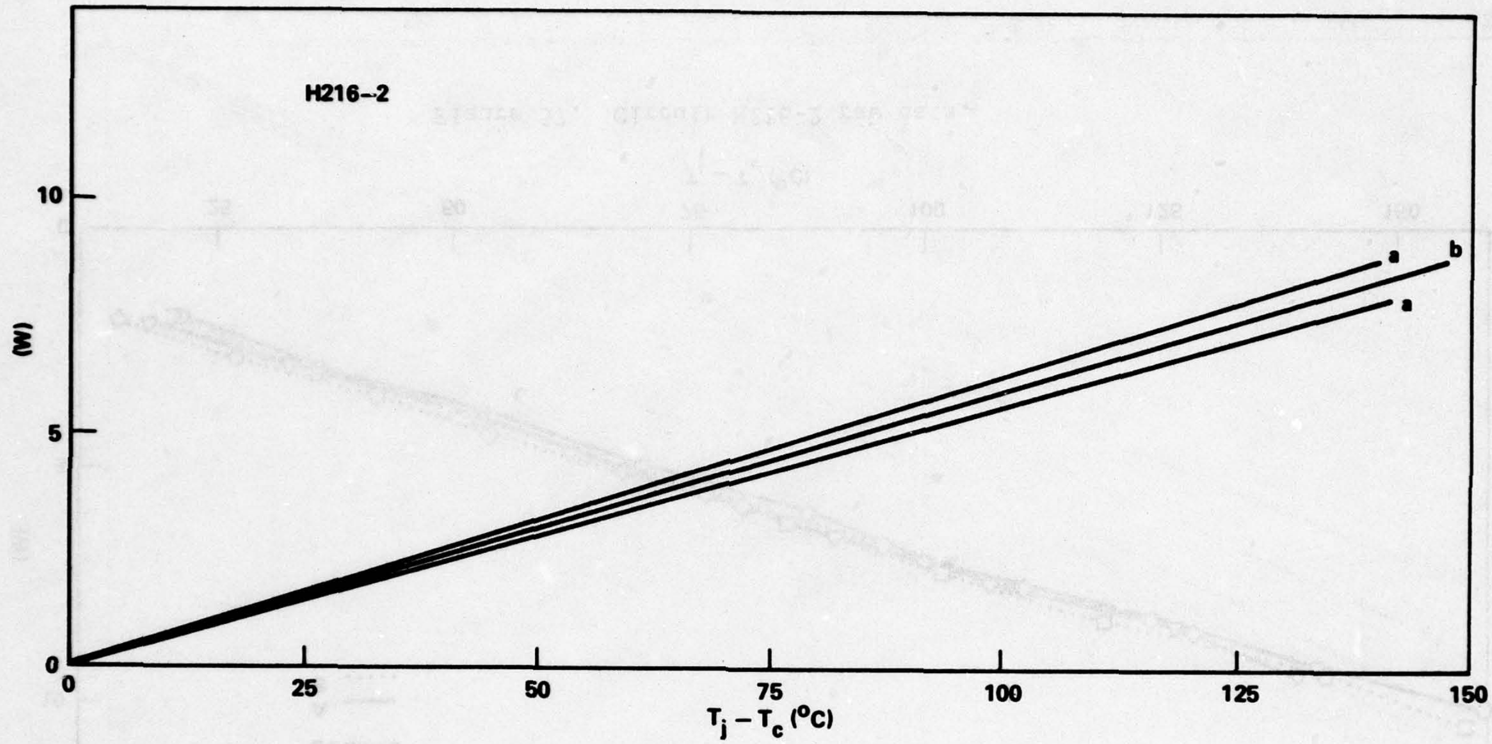

Figure 58. Circuit H216-2 junction to case.

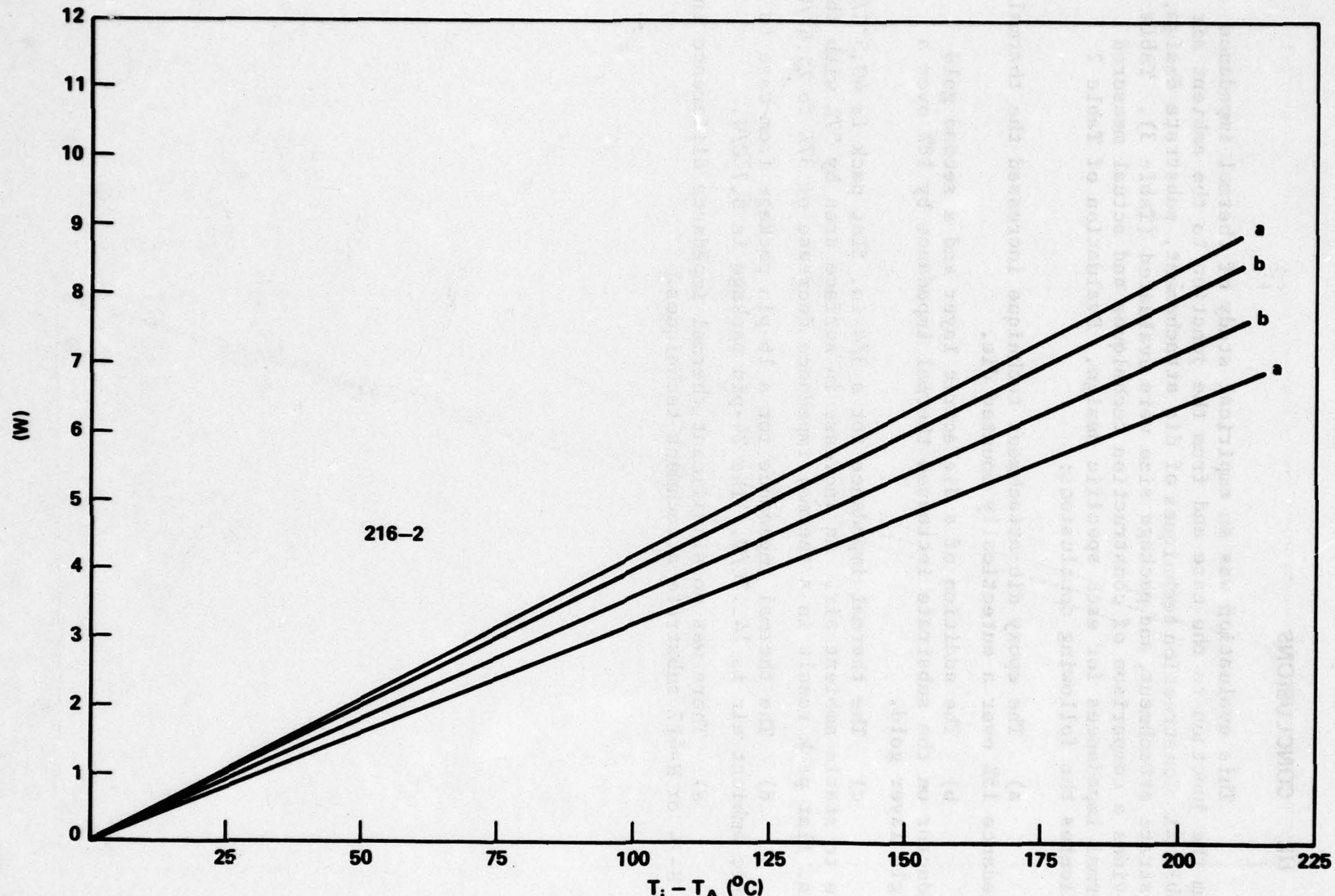

Figure 59. Circuit H215-2 junction to ambient.

III. CONCLUSIONS

This evaluation was an empirical study of thermal impedance from the junction to the case and from the junction to the ambient air (Table 2). Construction techniques of die attachement, substrate design, substrate attachment, and package size were evaluated (Table 3). Table 2 provides a comparison of construction techniques and actual measured thermal impedances for each specific design. Evaluation of Table 2 indicates the following conclusions:

a) The epoxy die attachment technique increased the thermal impedance 15% over a eutectically mounted die.

b) The addition of a dielectric layer and a second gold conductor on the substrate increased thermal impedance by 18% over a single layer gold.

c) The thermal impedance for a 3/4-in. flat pack is 40.5°C/W case to static ambient air. An increase in surface area by 57% with the 1-in. flat pack result in a thermal impedance decrease of 37% to 25.5°/W.

d) The thermal impedance for a 16-pin package from case to static ambient air is 14.1°C/W. The 24-pin package is 8.7°C/W.

e) There was no significant thermal impedance difference in the H-74 or H-417 substrate attachment techniques.

TABLE 2. CONSTRUCTION TECHNIQUE AND THERMAL IMPEDANCE

Package Type	Construction Technique: Substrate Attachment		Die Attachment		Substrate Design		Thermal Impedance Junction to Case (°C/watt)	Thermal Impedance Junction to Ambient (°C/watt)
	H-74*	H417*	Eutectic	Epoxy	Single Layer	Multi Layer		
3/4-in. Flat Pack		x	x		x		21.8	62.5
		x		x	x		27.2	67.5
		x	x			x	31.0	71.8
		x		x		x	34.6	74.7
1-in. flat pack		x	x		x		11.0	40.5
		x		x	x		12.7	36.8
		x	x			x	13.4	35.7
		x		x		x	13.0	38.1
16-pin DDIL	x		x		x		22.0	39.8
		x	x		x		19.7	34.8
	x			x	x		27.0	41.6
		x		x	x		27.0	35.5
	x		x			x	28.1	41.1
		x	x			x	29.3	41.5
	x			x		x	36.3	52.9
		x		x		x	33.5	48.6
23-Pin DDIL	x		x		x		10.4	17.2
		x	x		x		14.3	23.1
	x			x	x		13.5	24.5
		x		x	x		15.0	21.7
		x	x			x	13.0	19.8
	x			x		x	17.0	26.4
		x		x		x	16.9	27.6

*Note: H-74 is electrically insulative and thermally conductive epoxy.
H417 is silver filled epoxy.

TABLE 3. CONSTRUCTION TECHNIQUE AND MAXIMUM POWER DISSIPATION

Package Type	Construction Technique						Maximum Power Dissipation			
	Substrate Attachment		Die Attachment		Substrate Design		Infinite Heat Sink $T_j = 175°C$		Free Air $T_j = 175°C$	
	H-74*	H417*	Eutectic	Epoxy	Single Layer	Multi Layer	(W) T = 125°C	(W) T = 85°C	(W) T = 125°C	(W) T = 85°C
3/4-in. Flat Pack		x	x		x		2.3	4.1	0.8	1.4
		x		x	x		1.8	3.3	0.7	1.3
		x	x			x	1.6	2.9	0.7	1.3
		x		x		x	1.4	2.6	0.7	1.2
1-in. Flat Pack		x	x		x		4.5	8.2	1.2	2.2
		x		x	x		3.9	7.1	1.4	2.4
		x	x			x	3.7	6.7	1.4	2.5
		x		x		x	3.8	6.9	1.3	2.4
16-Pin DDIL	x		x		x		2.3	4.1	1.3	2.3
		x	x		x		2.5	4.6	1.4	2.6
	x			x	x		1.9	3.3	1.2	2.2
		x		x	x		1.9	3.3	1.4	2.5
	x		x			x	1.8	3.2	1.2	2.2
		x	x			x	1.7	3.1	1.2	2.2
	x			x		x	1.4	2.5	0.9	1.7
		x		x		x	1.5	2.7	1.0	1.9
24-Pin DDIL	x		x		x		4.8	8.6	2.9	5.2
		x	x		x		3.5	6.3	2.2	3.9
	x			x	x		3.7	6.7	2.0	3.7
		x		x	x		3.3	6.0	2.3	4.1
		x	x			x	3.8	6.9	2.5	4.5
	x			x		x	2.9	5.3	1.9	3.4
		x		x		x	3.0	5.3	1.8	3.3

*Note: H-74 is electrically insulative and thermally conductive epoxy
H-417 is silver filled epoxy

Appendix. RAW DATA FROM EXPERIMENTAL MEASUREMENT

H 214-1		SN 001			SN 002			SN 003		
T_a	T_j-T_a	T_c	T_j-T_c	(W)	T_c	T_j-T_c	(W)	T_c	T_j-T_c	(W)
-55	230	86.3	88.7	7.431	80.2	94.8	7.199	89.8	85.2	7.594
-25	200	98.2	76.8	6.549	91.6	83.4	6.316	98.8	76.2	6.883
0	175	106.8	68.2	5.845	100.1	74.9	5.703	108.8	62.2	6.085
25	150	116.8	58.2	5.140	110.8	64.2	4.962	118.3	56.7	5.333
50	125	125.4	49.6	4.446	119.1	55.9	4.343	125.9	49.1	4.683
75	100	134.4	40.6	3.772	129.2	45.8	3.645	135.6	39.4	3.896
100	75	142.6	32.4	3.153	138.4	36.6	3.056	143.6	31.4	3.278
125	50	152.5	22.5	2.430	148.7	26.3	2.383	152.5	22.5	2.582
150	25	163.5	11.5	1.740	159.3	15.7	1.664	162.4	12.6	1.789
H 214-2		SN 004			SN 005			SN 006		
T_a	T_j-T_a	T_c	T_j-T_g	(W)	T_c	T_j-T_c	(W)	T_c	T_j-T_c	(W)
-55	230	70.7	104.3	6.054	82.7	92.3	7.054	76.9	98.1	7.039
-25	200	89.8	85.2	6.204	92.8	82.2	6.246	87.9	87.1	6.339
0	175	100.4	74.6	5.496	102.2	72.8	5.591	99.5	75.5	5.679
25	150	110.9	64.1	4.807	113.0	62.0	4.842	110.8	64.2	4.997
50	125	119.7	55.3	4.215	121.1	53.9	4.272	122.0	53.0	4.393
75	100	129.7	45.3	3.554	130.3	44.7	3.638	131.4	43.6	3.753
100	75	140.0	35.0	2.930	139.8	35.2	2.974	141.05	33.95	3.110
125	50	149.1	25.9	2.282	149.3	25.7	2.337	151.05	23.95	2.460
150	25			1.6316	159.6	15.4	1.6383	162.0	13.0	1.7236
H 214-3		SN 007			SN 008			SN 009		
T_a	T_j-T_a	T_c	T_j-T_c	(W)	T_c	T_j-T_c	(W)	T_c	T_j-T_c	(W)
-55	230	97.5	77.5	8.151	100.5	74.5	7.869	93.0	82.0	7.787
-25	200	108.4	66.6	7.176	110.1	64.9	6.873	103.9	71.1	6.903
0	175	118.8	56.6	6.463	118.2	56.8	6.241	111.75	57.25	6.190
25	150	128.0	47.0	5.665	125.6	49.4	5.463	121.8	53.2	5.393
50	125	135.4	39.6	4.906	132.5	42.5	4.696	129.8	45.2	4.673
75	100	142.6	32.4	4.148	139.7	35.3	3.973	137.6	37.4	4.026
100	75	150.0	25.0	3.397	146.0	29.0	3.385	146.0	29.0	3.330
125	50	157.1	17.9	2.701	154.9	20.1	2.520	154.0	21.0	2.526
150	25	164.5	10.5	1.840	164.05	10.95	1.851	163.4	11.6	1.858
H-214-4		SN 010			SN 011			SN 012		
T_a	T_j-T_a	T_c	T_j-T_c	(W)	T_c	T_j-T_c	(W)	T_c	T_j-T_c	(W)
-55	230	76.4	98.6	7.086	90.9	84.1	7.774	92.9	82.1	7.580
-25	200	88.2	86.8	6.247	101.8	73.2	6.888	103.7	71.3	6.730
0	175	97.6	77.4	5.569	111.9	63.1	6.122	112.3	62.7	6.076
25	150	106.3	68.7	4.947	119.3	55.7	5.465	121.4	53.6	5.368
50	125	117.3	57.7	4.205	128.2	46.8	4.693	130.05	45.0	4.603
75	100	126.8	48.2	3.541	136.6	38.4	4.037	137.9	37.1	3.996
100	75	135.6	39.4	2.913	145.9	29.1	3.265	147.6	27.4	3.247
125	50	145.7	29.3	2.247	153.3	21.7	2.656	156.0	19.0	2.519
150	25	156.0	19.0	1.557	163.5	11.5	1.8592	164.4	10.6	1.869

T_a	T_j-T_a	T_c	T_j-T_c	(W)	T_c	T_j-T_c	(W)	T_c	T_j-T_c	(W)
	H-215-1	SN 001			SN 002			SN 003		
-55	230	74.2	100.8	3.792	52.6	122.4	3.351	81.1	93.9	3.921
-25	200	87.1	87.9	3.328	67.6	107.4	2.960	92.1	82.9	3.485
0	175	97.7	77.3	2.961	82.4	92.6	2.631	102.8	72.2	3.093
25	150	105.4	69.6	2.544	91.3	83.7	2.398	105.4	69.6	2.701
50	125	115.9	59.1	2.203	105.1	69.9	2.052	115.1	59.9	2.332
75	100	126.1	48.9	1.860	117.4	57.6	1.753	123.0	52.0	1.983
100	75	136.4	38.6	1.521	129.4	45.6	1.462	133.7	41.3	1.606
125	50	146.9	28.1	1.172	142.9	32.1	1.117	145.1	29.9	1.211
150	25	157.2	17.8	0.8269	155.8	19.2	0.7947	157.8	17.2	0.8539
	H-215-2	SN 004			SN 005			SN 006		
T_a	T_j-T_a	T_c	T_j-T_c	(W)	T_c	T_j-T_c	(W)	T_c	T_j-T_c	(W)
-55	230	71.9	103.1	3.629	67.1	107.9	3.539	75.4	99.6	3.661
-25	200	83.9	91.1	3.235	80.7	94.3	3.152	88.2	86.8	3.261
0	175	95.3	79.7	2.892	91.5	83.5	2.844	99.4	75.6	2.915
25	150	107.5	67.5	2.518	104.1	70.9	2.475	110.8	64.2	2.551
50	125	118.4	56.6	2.180	114.4	60.6	2.176	122.1	52.9	2.215
75	100	128.8	46.2	1.851	126.3	48.7	1.828	132.2	42.8	1.895
100	75	139.0	36.0	1.535	137.4	37.6	1.497	142.7	32.3	1.577
125	50	148.2	26.8	1.213	148.1	26.9	1.198	151.8	23.2	151.8
150	25	159.7	15.3	0.8869	159.9	15.1	0.8518	163.3	11.7	0.9351
	H-215-3	SN 007			SN 008			SN 009		
T_a	T_j-T_a	T_c	T_j-T_c	(W)	T_c	T_j-T_c	(W)	T_c	T_j-T_c	(W)
-55	230	92.3	82.7	4.188	78.4	96.6	4.005	104.5	70.5	4.251
-25	200	103.5	71.5	3.688	90.8	84.2	3.501	113.2	61.8	3.773
0	175	111.8	63.2	3.277	102.1	72.9	3.026	120.7	54.3	3.366
+25	150	120.9	54.1	2.850	112.0	63.0	2.636	128.1	46.9	2.905
+50	125	129.2	45.8	2.447	119.9	55.1	2.337	134.5	40.5	2.532
+75	100	137.4	37.6	2.063	130.4	44.6	1.910	142.1	32.9	2.100
+100	75	145.5	29.5	1.684	138.6	36.4	1.586	149.0	26.0	1.703
+125	50	153.7	21.3	1.292	148.2	26.8	1.204	155.7	19.3	1.321
+150	25	161.9	13.1	0.918	157.7	17.3	0.819	163.2	11.8	0.917
H-215-4		SN 010			SN 011			SN 012		
T_a	T_j-T_a	T_c	T_j-T_c	(W)	T_c	T_j-T_c	(W)	T_c	T_j-T_c	(W)
-55	230	84.8	90.2	3.884	79.0	96.0	3.951	76.2	98.8	4.045
-25	200	96.5	79.5	3.450	91.3	83.7	3.536	88.9	86.1	3.606
0	175	106.4	68.6	3.076	102.5	72.5	3.116	99.3	75.7	3.230
25	150	116.3	58.7	2.695	113.3	61.7	2.744	110.9	64.1	2.817
50	125	125.5	49.5	2.326	123.1	51.9	2.387	121.9	53.1	2.439
75	100	135.1	39.9	1.963	131.8	43.2	2.088	131.6	43.4	2.077
100	75	144.1	30.9	1.625	141.9	33.1	1.719	141.3	33.7	1.736
125	50	152.8	22.2	1.266	152.9	22.1	1.331	151.9	23.1	1.350
150	25	163.0	12.0	0.927	162.8	12.2	0.971	162.7	12.3	0.975

H 216-1B		SN 004		
T_a	T_j-T_a	T_c	T_j-T_c	(W)
-55	230	24.1	150.1	12.144
-25	200	43.0	132.0	10.283
0	175	59.0	116.0	8.951
25	150	77.0	98.0	7.604
50	125	92.4	82.6	6.406
75	100	107.6	67.4	5.187
100	75	122.5	52.5	3.962
125	50	138.1	36.9	2.817
150	25	152.6	22.4	1.636

H 216-2A		SN 005			SN 006		
T_a	T_a-T_j	T_c	T_j-T_c	(W)	T_c	T_j-T_c	(W)
-55	230	35.0	140.0	9.422	14.7	160.3	10.186
-25	200	50.3	124.7	8.411	33.1	141.9	9.252
0	175	67.2	107.8	7.505	50.4	124.6	8.266
25	150	84.1	90.9	6.525	69.6	105.4	7.016
50	125	97.9	77.1	5.648	87.3	87.7	6.003
75	100	112.3	62.7	4.728	104.8	70.2	4.943
100	75	126.1	48.9	3.790	122.3	52.7	3.889
125	50	142.5	32.5	2.863	139.3	35.7	2.946
150	25	157.2	17.8	1.941	153.6	21.4	1.885

H 216-2B		SN 007			SN 008		
T_a	T_j-T_a	T_c	T_j-T_c	(W)	T_c	T_j-T_c	(W)
-55	230	16.8	158.2	10.575	46.2	128.8	8.549
-25	200	37.3	137.7	9.375	63.9	111.1	7.575
0	175	55.4	119.6	8.299	79.0	96.0	6.722
25	150	72.7	102.3	7.222	93.9	81.1	5.880
50	125	89.2	85.8	6.175	106.4	68.6	5.122
75	100	106.1	68.9	5.124	120.5	54.5	4.328
100	75	122.0	53.0	4.063	133.3	41.7	3.558
125	50	139.3	35.7	3.045	148.0	27.0	2.790
150	25	154.8	20.2	1.868	160.5	14.5	1.901

H 216-3A		SN 009			SN 010		
T_a	T_j-T_a	T_c	T_j-T_c	(W)	T_c	T_j-T_c	(W)
-55	230	36.9	138.1	13.651	34.4	140.6	13.416
-25	200	53.5	121.5	12.143	51.8	123.2	11.784
0	175	68.6	106.4	10.722	65.7	109.3	10.406
25	150	85.7	89.3	9.156	82.1	92.9	8.752
50	125	100.3	74.7	7.781	96.9	78.1	7.278
75	100	115.1	59.9	6.352	110.5	64.5	5.873
100	75	129.2	45.8	4.970	124.3	50.7	4.430
125	50	143.5	31.5	3.584	138.5	36.5	2.984
150	25	157.7	17.3	2.174	152.2	22.8	1.555

H 216-3B		SN 011			SN 012		
T_a	T_j-T_a	T_c	T_j-T_c	(W)	T_c	T_j-T_c	(W)
-55	230	46.1	128.9	9.557	27.9	147.1	11.986
-25	200	62.5	112.5	8.587	40.3	134.7	10.902
0	175	76.5	98.5	7.746	57.1	11.9	9.760
25	150	91.2	83.8	6.706	76.0	99.0	8.454
50	125	105.2	69.8	5.797	93.0	82.0	7.209
75	100	118.2	56.8	4.859	110.0	65.0	5.943
100	75	131.1	43.9	3.867	126.2	48.8	4.689
125	50	144.2	30.8	3.854	142.2	32.8	3.435
150	25	157.1	17.9	1.804	157.7	17.3	2.160

H 216-4A		SN 013			SN 014		
T_a	T_j-T_a	T_c	T_j-T_c	(W)	T_c	T_j-T_c	(W)
-55	230	30.8	144.2	11.046	44.6	130.4	9.359
-25	200	48.9	126.1	9.815	60.9	114.1	8.296
0	175	65.2	109.8	8.681	74.4	100.6	7.388
25	150	80.4	94.6	7.577	89.4	85.6	6.411
50	125	95.5	79.5	6.482	102.9	72.1	5.547
75	100	110.4	64.6	5.355	116.4	58.6	4.605
100	75	124.8	50.2	4.217	129.4	45.6	3.670
125	50	139.8	35.2	3.033	142.9	32.1	2.684
150	25	154.7	20.3	1.890	156.4	18.6	1.739

H 216-4B		SN 015					
T_a	T_j-T_a	T_c	T_j-T_c	(W)			
-55	230	31.7	143.3	11.389			
-25	200	42.1	132.9	10.017			
0	175	57.9	117.1	8.896			
25	150	76.4	98.6	7.690			
50	125	92.7	82.3	6.579			
75	100	109.4	65.6	5.437			
100	75	125.8	49.2	4.347			
125	50	142.3	32.7	3.193			
150	25	157.7	17.3	2.120			
H 217-1A		**SN 001**			**SN 002**		
T_a	T_j-T_a	T_c	T_j-T_c	(W)	T_c	T_j-T_c	(W)
-55	230	21.1	153.9	4.891	19.4	155.6	7.085
-25	200	44.2	130.8	4.324	40.1	134.9	6.256
0	175	52.1	122.9	4.158	57.1	117.9	5.490
25	150	70.8	104.2	3.636	74.6	100.4	4.738
50	125	89.2	85.80	3.136	89.1	85.9	3.921
75	100	105.8	69.2	2.598	107.2	67.8	3.346
100	75	121.0	54.0	2.110	123.6	51.4	2.596
125	50	137.3	37.7	1.566	139.6	35.4	1.901
150	25	154.2	20.8	0.977	156.4	18.6	1.148
H 217-1B		**SN 003**			**SN 004**		
T_a	T_j-T_a	T_c	T_j-T_c	(W)	T_c	T_j-T_c	(W)
-55	230	10.2	164.8		18.0	157.0	5.822
-25	200	33.6	141.4		39.2	135.8	5.227
0	175	57.6	117.4		56.8	118.2	4.640
25	150	76.9	98.1		74.8	100.2	4.120
50	125	93.6	81.4		92.6	82.4	3.522
75	100	108.7	66.3		108.9	66.1	2.955
100	75				125.0	50.0	2.396
125	25	155.7	19.3		142.2	32.8	1.808
150	25	155.7	19.3		158.0	17.0	1.216

H 217-2A		SN 005			SN 006		
T_a	T_j-T_a	T_c	T_j-T_c	(W)	T_c	T_j-T_c	(W)
-55	230	23.3	151.7	4.289	17.5	157.5	5.609
-25	200	42.8	132.2	3.814	37.6	137.4	4.934
0	175	59.6	115.4	3.399	54.0	121.0	4.367
25	150	77.0	98.00	2.980	71.5	103.5	3.747
50	125	94.1	80.9	2.556	88.3	86.7	3.164
75	100	109.8	65.2	2.178	104.8	70.2	2.596
100	75	125.9	49.1	1.773	121.8	53.2	2.022
125	50	142.6	32.4	1.394	138.6	36.4	1.507
150	25	158.4	16.6	0.967	155.2	19.8	0.905

H 217-2B		SN 007			SN 008		
T_a	T_j-T_a	T_c	T_j-T_c	(W)	T_c	T_j-T_c	(W)
-55	230	12.4	162.6	5.344	18.8	156.2	4.978
-25	200	34.1	140.9	4.823	28.7	136.3	4.394
0	175	53.1	121.9	4.342	55.0	120.0	3.901
25	150	69.1	105.9	3.810	71.3	103.7	3.418
50	125	86.8	88.2	3.257	88.0	87.0	2.920
75	100	104.0	71.0	2.705	104.5	70.5	2.411
100	75	120.8	54.2	2.161	121.2	53.8	1.877
125	50	139.1	35.9	1.574	138.1	36.9	1.404
150	25	155.8	19.2	1.081	155.1	19.9	0.903

H 217-3A		SN 009			SN 010		
T_a	T_j-T_a	T_c	T_j-T_c	(W)	T_c	T_j-T_c	(W)
-55	230	52.1	122.9	5.809			
-25	200	68.0	107.0	5.056	37.4	137.6	5.866
0	175	81.9	93.1	4.454	55.9	119.1	5.382
25	150	94.7	80.3	3.888	74.4	100.6	4.817
50	125	107.5	67.5	3.309	91.8	83.2	4.160
75	100	121.7	53.3	2.722	108.3	66.7	3.450
100	75	133.8	41.2	2.173	125.7	49.3	2.875
125	50	146.2	28.8	1.558	141.2	33.8	2.018
150	25	158.7	16.3	0.999	155.9	19.1	1.154

H 217-3B		SN 0011			SN 012		
T_a	T_j-T_a	T_c	T_j-T_c	(W)	T_c	T_j-T_c	(W)
-55	230	52.9	122.1	6.306	21.6	153.4	6.306
-25	200	70.0	105.0	5.584	42.4	132.6	5.584
0	175	84.2	90.8	4.997	58.4	116.6	4.997
25	150	98.1	76.9	4.357	75.1	99.9	4.357
50	125	111.2	63.8	3.756	91.9	83.1	3.756
75	100	124.0	51.0	3.165	108.0	67.0	3.165
100	75	136.6	38.4	2.493	128.6	46.0	2.493
125	50	149.7	25.3	1.849	139.6	35.4	1.849
150	25	162.3	12.7	1.205	155.2	19.8	1.205
H 217-4A		SN 013			SN 014		
T_a	T_j-T_a	T_c	T_j-T_c	(W)	T_c	T_j-T_c	(W)
-55	230	37.2	137.8	5.431	16.6	158.4	6.059
-25	200	36.5	138.5	4.878	36.1	138.9	5.458
0	175	70.2	104.8	4.380	53.3	121.7	4.793
25	150	86.8	88.20	3.822	70.2	104.8	4.146
50	125	101.8	73.2	3.286	87.1	87.9	3.501
75	100	115.7	59.3	2.763	103.7	71.3	2.816
100	75	129.4	45.6	2.232	120.8	54.2	2.176
125	50	144.0	31.0	1.667	137.6	37.4	11.499
150	25	158.4	16.6	1.113	153.8	21.2	0.856
H 217-4B		SN 015					
T_a	T_j-T_a	T_c	T_j-T_c	(W)			
-55	230	11.0	164.0	6.205			
-25	200	35.2	139.8	5.525			
0	175	53.4	121.6	4.834			
25	150	71.8	103.2	4.181			
50	125	89.6	85.4	3.448			
75	100	107.7	67.3	2.753			
100	75	124.7	50.3	2.131			
125	50	140.8	34.2	1.519			
150	25	156.2	18.1	0.959			

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