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This report presents the second-quarter results of a program to develop an ion implanted planar GaAs integrated circuit process technology. The program involves three subcontractors (California Institute of Technology, Cornell University, and Crystal Specialties, Inc.) in addition to the Rockwell International Science Center.

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(continued)

20. Abstract (continued)

Work on growth of semi-insulating GaAs in this quarter has emphasized reduction of crystal plane slippage and dislocation density of GaAs crystals. The slippage problem has been considerably reduced by orienting the crystal growth in the <110> direction.

Data have been obtained for high-dose selenium implants carried out at room temperature and annealed at 850°C. and for room temperature silicon implants annealed at 850°C. or 900°C.

The mask set designed in the first quarter has been used in the fabrication of integrated circuits at the Science Center. A second layer interconnection process has been implemented.

Devices and test circuits fabricated with the first mask set have been evaluated. Scaling of FET saturation currents with channel widths required for low power operation has been demonstrated down to a width of 1 μm. The Schottky diode FET logic gate designed for this first mask set has shown excellent low frequency performance. Measurements on seven stage ring oscillators utilizing 20 μm gate width FET NOR gates have given propagation delays as low as τ_d = 82 picoseconds with approximately 2 mW/gate dissipation. Dynamic switching energies as low as 46 femtojoules were obtained for 10 μm gate width ring oscillators.

The development of a computer model for the electron dynamics in the channel of a GaAs FET has been continued at Cornell University.

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FOREWORD

The research covered in this report is carried out in a team effort having the Rockwell International Science Center as the prime contractor with two universities and a crystal growth company as subcontractors. The effort is sponsored by the Materials Science Office of the Defense Advanced Research Projects Agency. The contract is monitored by the Air Force Office of Scientific Research. Program manager is F. Blum. The principal investigators for each organization are:

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1.0 TECHNICAL SUMMARY

This report covers the second quarter of a GaAs integrated circuit (IC) program. The purpose is to develop an ion implanted planar technology for GaAs Ics with the goal of developing LSI capability in a short period of time. The fabrication approach is based on multiple localized implantations directly into the semi-insulating GaAs substrate to form device areas insulated by the unimplanted regions of the substrate. A new circuit concept involving a combination of Schottky diodes and depletion mode Schottky barrier FETs is being employed to form a logic gates capable of high speed and very low power operation.

This program requires a research effort on all the multiple facets of the process development. It is carried out by the Science Center with the support of three subcontractors, Caltech, Cornell and Crystal Specialties, Inc. The research activities range from substrate fabrication and ion implantation technology to design, fabrication and evaluation of test circuits.

The following is a summary of the accomplishments of the program in the second quarter. Details will be found in the following sections of the report.

1. Bulk Crystal Growth (Sec. 3.1). Crystal Specialties has continued supplying all the qualified semi-insulating substrate material required by the program. Surface preparation has been improved responding to the requirements of fine line projection lithography. The surface flatness is currently better than 5 μm over 2.5 inch wafers. Crystal growth in the (110) direction has been successfully implemented leading to near elimination of slippage problems.

2. Evaluation of Alternative Sources of Semi-Insulating GaAs (Sec. 3.2). Qualification tests for ion implantation have shown a decrease of the yield of qualified crystals from Crystal Specialties. This yield now stands at ~30%. Sampling of suppliers has shown a parallel decrease of qualified material from Morgan Semiconductors. Sumitomo material has again failed to pass the qualification tests, while a new Japanese supplier, Mitsubishi-Monsanto has provided two samples one of which passed the qualification test.

3. Ion Implantation (Sec. 4.1). Study of high dose Se implantation for ohmic contacts have been continued at the Science Center. The purpose is to lower the anneal temperature so that it becomes compatible with the temperature required by the low-dose implants for FET channels and diodes (850°C). The dose and implantation temperature are being investigated for optimization. Investigation of Si implantation as a substitute for Se implantation in the low resistivity ohmic contact areas has been continued as a cooperation effort between the Science Center and Cal Tech. Although the best activation (90%) has been reached using 900°C anneals, lower temperature anneals (800 and 850°C) have yielded a sheet resistance lower than that from high-dose Se implants annealed at the same temperature.

4. Device and Circuit Fabrication (Sec. 4.2). At the Science Center the mask set designed in the first quarter has been used in fabrication of integrated circuit wafers. All the process steps have been implemented, including the second layer metallization. The Canon projection mask aligner (4 to 1 reduction) has proved to meet all the fine line lithography requirements. Excellent resolution, and alignment of the numerous 1 μm features in the mask layout demonstrate the soundness of this lithography approach. A second layer interconnect process has been implemented. A preliminary evaluation of three dielectrics has shown that plasma deposited Si_3N_4 is the most promising one for isolation of the second layer metallization from the first layer.

5. Device and Circuit Testing (Secs. 5.1 and 5.2) At the Science Center, devices and test circuits fabricated with the first mask set have been evaluated. FETs and diodes show excellent characteristics in agreement with their design. Scaling of FET saturation currents with channel width, required for low power operation, has been demonstrated, down to 1 μm width. The Schottky diode-FET logic gate designed has shown good low frequency performance. Finally, measurements of oscillation frequency and power consumption of ring oscillators have shown results quite compatible with the goals of the program. A 120 ps propagation delay per gate, with dynamic switching energy as low as 46 fJ/gate have been demonstrated from 9-stage ring oscillators employing 10 μm wide FETS.

6. Switching Speed Analysis (Sec. 5.3). The development of a computer model for the electron dynamics in the channel of a GaAs FET to be integrated into logic circuit analysis has been continued at Cornell University. This model, which demands very little computer time (0.25 seconds per point) has been tested against a much larger two-dimensional calculation showing good agreement.

2.0 INTRODUCTION

The objective of this program is to develop a planar ion implanted IC process technology for GaAs. This is necessary in order to produce high speed low power digital integrated circuits which take advantage of the superior electrical properties of GaAs . The goal of the first phase of the program, which is of 17 months duration, is to acheive the capability of fabricating circuits of MSI complexity. This program requires efforts in a number of different areas including the growth of semi-insulating GaAs substrates ion implantation studies, development of processing and process monitoring techniques, and design and testing of demonstration circuits. The bulk of the research effort is to be carried out at the Rockwell International Science Center. However, significant assistance is being obtained from three subcontractors, Crystal Specialties Inc., California Institute of Technology and Cornell University.

During the first quarter of the program the basic fabrication approach was demonstrated by the successful fabrication of planar FETs and Schottky diode structures. During that quarter, a mask set was designed which contained test patterns for monitoring the fabrication process, a variety of device designs to be used in the development of design rules and circuits to permit determination of the propagation delay which can be achieved in GaAs ICs. The most significant single achievement on the program during the present (second) quarter involves the successful fabrication of IC wafers using this mask set and the testing of the ring oscillator circuits on these wafers. The results of these ring oscillator tests, which are described in detail in this report, clearly demonstrate that the expected low propagation delays and low dynamic switching energies can indeed be achieved in depletion mode GaAs integrated circuits. Propagation delays less than 100 psec have been measured, and power-delay products as small as 46 femtojoules (46fJ)have been observed. These excellent results obtained early in this program are a clear demonstration of potential benefits to be derived from the development of this planar ion implanted integrated circuit process technology.

This second quarterly report report contains significant results in other areas in addition to the ring oscillator measurements. Growth of semi-insulating GaAs in the 110 direction rather than the <111> direction shows promise of reducing the boat wetting problem which has previously been reported. The acceptance rate of semi-insulating materials during this quarter, however, has been lower than that achieved during the first quarter. Ion implantation studies have been continued on Se and Si implantations for ohmic contact regions.

A number of wafers are being processed utilizing the mask set previously mentioned. Emphasis has been placed on the development of the second layer metallization process. A plasma deposited Si_3N_4 layer has proved to be the most adequate dielectric to provide isolation between the first and second layer metallizations. Experiments leading to this conclusion are presented. In addition to high frequency measurements on ring oscillators a number of measurements have been carried out at dc or low frequencies on various test circuits included in the mask set. These results are also summarized in this report.

The development of a new two-dimensional model of a GaAs Schottky gate FET has been continued and used for calculation of FET parameters. The proposed model can be used for computer aided design of GaAs FET logic elements.

3.0 MATERIAL

In this section the activities on growth and evaluation of semi-insulating GaAs substrate material will be discussed. This material is grown at Crystal Specialties, which supplies all the substrates required by the program while carrying on research aimed at improving material quality and wafer size, as well as availability and cost of semi-insulating GaAs. The Crystal Specialties contribution will be discussed in Sec. 3.1. In Sec. 3.2 the evaluation of the material in terms of its qualification for ion implantation will be discussed. This will be done in conjunction with the evaluation of alternate suppliers of semi-insulating GaAs.

3.1 Bulk Growth of Semi-Insulating GaAs (Crystal Specialties)

Successful growth of high quality GaAs by the horizontal Bridgmen process depends upon tight control of several variables mentioned in the previous reports. In addition the the problems of boat wetting, orientation of growth has now been identified as one important factor affecting crystalline quality.

The problem of post growth crystal plane slippage has been reduced considerably by orienting the growth in a (110) direction. This has been demonstrated by growing a large number of crystals in the (110) direction. The reason for the improvement in this direction of growth is the crystals ability to "step facet" and thus adjust to the horizontal isotherm. This ability to follow the isothermal interface shape instead of one large facet across the entire growing interface reduces the thermal strain of the growing crystal. Consequently, slippage dislocation density has been considerably reduced, and so has the number of failures due to formation of polycrystalline ingots.

The dislocation densities of the GaAs crystals ranges between 5×10^3 and 1×10^4 cm^2. Efforts to further reduce the dislocation density are being made. Several factors contribute to the dislocation density. Those of greatest importance are: wetting of the quartz boat by the growing crystal,

thermal stress, seed quality and seeding techniques. Wetting has been reduced measurably in the past several months. It is not known how much of the dislocation generation is still due to boat wetting.

Thermal gradients within the crystals, which cause the crystal to cool unevenly, also generate crystalline defects. The change in growth direction allowing the growing interface to better adjust to the thermal isotherm has reduced the stress in the growing crystal. The quality of the seed material and techniques of seeding are also known sources of dislocations. It has been proved that highly dislocated or slipped seeds result in bulk ingots with the same defects.

The yield of single crystals over this reporting period was 68%, about the same as that reported in the first quarter. This yield should increase, however, after recently incorporated personnel gain experience. The yield of compensated material has slightly decreased to 82%, which is still quite acceptable.

Thermal conversion of the semi-insulating material is the most important problem remaining to be solved. The thermal conversion problem results in a limitation in the availability of semi-insulating material suitable for ion implantation processing and the necessity for a test procedure to select substrate material. The present procedure is to cut samples from the front and back of the crystal for the user to evaluate. The slowness of this evaluation produces an excessively large inventory of crystals waiting to be processed.

Facility improvements are being made at Crystal Specialties. A change in the furnace design is planned, in order to enable the operator to react the Ga and As in about one-fourth the time. It is expected that this should greatly reduce the Si intake during the reaction phase, possibly reducing the probability of thermal conversion of the resulting semi-insulating GaAs.

3.2 Evaluation of Alternate Sources of Semi-Insulating GaAs (Science Center

During the second quarter, additional wafers from previously sampled sources were received (Morgan Semiconductor Inc. and Sumitomo Electric Ltd). Samples were also obtained from a new source, Mitsubishi-Monsanto Chemical Co. Chromium doped wafers were not available during this period from Laser Diode Inc. All wafers were evaluated using the procedure and specifications outlined in Quarterly Technical Report No. 1, Section 3.0.[1]

The physical properties of the wafers as received were within specification except for flatness which was $\pm$ 4 μm for Mitsubishi-Monsanto $\pm$ 5 μm for Morgan and $\pm$ 6 μm for Sumitomo Electric. The valve for Morgan semiconductors represents a significant improvement when compared with previous shipments. Crystal Specialties, which is producing the flattest wafers, has also made improvements in wafer flatness. At present, Crystal Specialties can achieve a flatness of $\pm$ 2-3 μm/in, permitting fabrication of 2.1 x 2.1 cm patterns.

The new material from Crystal Specialties was grown in the (110) direction and slices were cut parallel to the (100) direction. These slices have the (110) plane on a diagonal through the slice. In order to use the material more efficiently, device wafers were cut not aligned parallel to a cleavage plane. Since all devices are sawed instead of scribed this condition has been accepted on a temporary basis.

As to the electrical qualification for ion implantation, the thermal conversion section of our material qualification test was deleted due to the duplication involved in the Krypton bombardment and anneal test. Originally, the thermal conversion test was instituted to screen out the low quality samples prior to Kr bombardment.

Table 3.2-1 contains a summary of results of the electrical qualification tests performed on all the samples received during this quarter. The overall fraction of electrically qualified material from all substrate sources is rather low. (Note that the experiments on growth in the ⟨110⟩ direction may be partly responsible for this low yield.) The yield of qualified Crystal Specialties material was 24% during this period. Sumitomo Electric has failed 4 of 4 and has yet to deliver qualified samples to the Science Center. The Morgan semiconductor material received this quarter has all failed to pass the qualification test, although previous deliveries were successful. One sample of Mitsubishi material passed the qualification test. Therefore, a small quantity of the qualified Mitsubishi-Monsanto material for device evaluation. The present cost of the Mitsubishi wafers is not yet competitive with other suppliers. Competitive pricing has been promised when Mitsubishi attains full production capacity.

TABLE 3.2-1

Substrate Qualification for Ion Implantation Sheet Resistance ($\Omega/\square$)

	Front		Tail		
Supplier	No Kr	Kr	No Kr	Kr	
Crystal Specialties, Inc.					
3546	10^8	10^4	10^8	10^5	
3552	10^8	10^8	10^7	10^8	Qualified
3558	10^3	10^4	10^3	10^8	
3596	10^3	10^4		10^4	
3608	10^8	10^6	10^8	10^6	Qualified
3602	10^8	10^6	10^8	10^6	Qualified
3618	10^7	10^4	10^8	10^4	
3646	10^8	10^6	10^8	10^5	
3640	10^8	10^4	10^8	10^4	
3648	10^3	10^5	10^5	10^4	
3650	10^8	10^5	10^8	10^6	
3683 Te	10^3	10^4	10^7	10^3	
2440	Control	10^8			
3396	Control	10^8			
Sumitomo Electric Ltd.					
FS20454	p type			5×10^5	
FS20455	3×10^3			5×10^3	
Morgan Semiconductor Inc.					
MSI 2-78	10^7	10^5	10^8	104	
MSI 11-105A	10^8	10^5	10^8	10^5	
MSI 1-89	10^8	10^4	10^8	10^4	
Mitsubishi-Monsanto Chemical Co.					
G101-30F	10^8	2×10^4			
G101-36F	10^8	10^7			Qualified

4.0 PROCESS DEVELOPMENT

This section is concerned with the development of the integrated circuit fabrication process. The discussion includes work on ion implantation in Sec. 4.1 and the actual fabrication of IC wafers in Sec. 4.2.

4.1 Ion Implantation

The work on selenium and silicon implantation, which was described in the first Quarterly Report,[1] was directed at developing a method of achieving high electron concentrations utilizing a post implantation annealing temperature of 850°C. The earlier work on selenium implantation showed that when the implantations were carried out at 200°C and the annealing was performed at 850°C a dose of about 4×10^{13} seleniun ions per cm^2 would give the minimum sheet resistance . Electron concentration and mobility profile data have now been obtained for a selenium implanted sample which is thought to be typical of the results for such selenium implants. In addition, measurements have been carried out on samples implanted with selenium at room temperature. The study of room temperature silicon implants have been extended. The work includes measurements of sheet electron concentration as a function of implanted dose and anneal temperature for samples annealed with a reactively sputtered silicon nitride cap, and determination of electron concentration and mobility profiles for some of those samples. These results are described in the two following subsections.

4.1.1 Selenium Implantation (Science Center and Caltech)

In the preceding quarterly report the sheet resistance, sheet electron concentration and mobility were given as a function of implanted dose for GaAs implanted with 300 keV selenium ions at 200°C and annealed at 850°C or 875°C. No profile data for these implants were available at that time. Figure 4.1-1 shows electron concentration and mobility profiles for a sample which was implanted with 3×10^{13} selenium ions per cm^2 and annealed at a 875C. Since the earlier work showed little difference between samples annealed at 850°C or 875°C, it is felt that these profiles are

SAMPLE 1404
Se → GaAs, $3 \times 10^{13} cm^2$
300 keV, 200°C
875°C-30'-H_2

ELECTRON CONCENTRATION (cm^{-3})

10^{17}

10^4

MOBILITY (cm^2/volt·sec)

10^3

0 0.1 0.2 0.3 0.4 0.5

DEPTH (μm)

Fig. 4.1-1 Electron concentration and mobility profiles for a semi-insulating GaAs sample implanted with selenium.

typical of results which would be obtained for doses of 3-4 x 10^{13} ions cm^{-2} if annealing was carried out in the range of 850°C to 875°C. The maximum electron concentration of about $6x10^{17}$ cm^{-2} is three to four times the electron concentration in the channel region of FETs in the integrated circuits fabricated under this program. This is thought to be adequate for the doping of the contact regions of these FETs.

It is desirable to be able to perform all implantation in the IC process at room temperature. We have therefore investigated room temperature implants with doses in the same range as for the earlier investigation carried out for 200°C implants. Table 4.1-1 shows some results. Electron concentration measured for these implants are nearly an order of magnitude below those obtained for samples implanted at 200°C. Measured sheet resistances are five or six times higher than those obtained for the hot implants. Thus it appears that room temperature implantation of selenium cannot be used for doses in the range of a few times 10^{13} per cm^2. It is possible however that good activation of such implants could be obtained using an implantation temperature of less than 200°C. This is expected to be the subject of future investigation.

4.1.2 Silicon Implantation (Caltech and Science Center)

Room temperature silicon implants into semi-insulating GaAs were carried out at Caltech at an energy of 300 keV with several different doses. The samples were annealed using a reactively sputtered silicon nitride cap. Table 4.1-2 shows the samples that were prepared with different doses and anneal treatments. The measured sheet electron concentration, N_s, is plotted versus the implantation dose, N_d, for different anneal temperatures in Fig. 4.1-2. The highest percentage of electrically active dopant was obtained for the 900°C anneal temperature. The ratio of N_s over N_d reached a maximum value of 0.88 for sample No. 13. For the 800°C and 850°C degree anneals N_s/N_d decreases for the highest dose of $1.74x10^{15}$ cm^{-2}.

TABLE 4.1-1

Results for 300 keV Se Implantation at Room Temperature
850C - 30 min Anneal

Dose Ions cm^{-2}	Sheet Resistance ($\Omega/\square$)	Sheet Electron Conc. (cm^{-3})	Mobility (cm^2/volt sec)
$5x10^{13}$	724	$2.54x10^{12}$	3400
$5x10^{13}$	859	$2.45x10^{12}$	2960
$7x10^{13}$	637	$2.95x10^{12}$	3330

Table 4.1-2

Sample Identification

Implantation Dose $N_d(cm^{-2})$	800^oC-30'-H_2	Annealing Cycles 850^oC-30'-H_2	900^oC-30'H_2
1.74×10^{13}	11	12	13
5.74×10^{13}	21	22	23
1.74×10^{14}	31	32	33
5.74×10^{14}	41	42	43
1.74×10^{15}	51	52	53

$Si \rightarrow GaAs$
300 keV, R.T.
Si_3N_4 Encapsulation

○ 800°C–30′–H_2
● 850°C–30′–H_2
× 900°C–30′–H_2

$N_s (cm^{-2})$

10^{12} 10^{13} 10^{14} 10^{15} 10^{16}

10^{13} 10^{14} 10^{15} 10^{16}

$N_d (cm^{-2})$

Fig. 4.1-2 Sheet electron concentration versus implant dose for Si implantations.

Sheet resistivity, ρ_s, vs implantation dose data are presented in Fig. 4.1-3. Lowest values of ρ_s were obtained for the 900°C anneals than for 800 or 850°C anneals. The lowest value of 22.7 ohm/□ was achieved for sample No. 53. This result is quite encouraging since it is about a factor 2 lower than the lowest value of ρ_s reported for selenium implants which were performed at elevated (350°C) temperatures.

Electron concentration and mobility profile data for some of the samples of Table 4.1-2 as shown in Figs. 4.1-4 and 4.1-5, respectively, the electron concentration profiles are much deeper than the LSS prediction. This is probably due to diffusion during the post implantation anneal. Sample No. 53 exhibits a relatively flat profile with a carrier concentration of about 2×10^{18} cm^{-3} which extends to a depth of at least 1 μm. This shows that the relatively low sheet resistivity measured for this sample results from a very deeply doped layer rather than an extremely high electron concentration. The maximum concentration observed for sample No. 42 is also about 2×10^{-18} cm^{-2}. These values are comparable to the maximum concentrations observed in earlier work on selenium implantation in GaAs. The electron mobilities measured for samples 42 and 53 are about 1000 cm^2 per Vsec. This result is somewhat lower than expected for uncompensated material with carrier concentrations of 2×10^{18} cm^{-3} and suggest that there are some compensating centers in these implanted layers

These additional results on silicon implantation in GaAs at room temperature are a further indication that silicon may be the most useful dopant for achieving high electron concentration in the integrated circuits process. Future work will be directed measurements of electron concentration and mobility profiles for other samples listed in Table 4.1-2.

4.2 Device and Circuit Fabrication (Science Center)

This section will review the progress on fabrication of planar GaAs integrated circuits in the last quarter. The reader is referred to a detailed

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$Si \rightarrow GaAs$
300 keV, R.T.
Si_3N_4 Encapsulation
○ 800°C–30′–H_2
● 850°C–30′–H_2
× 900°C–30′–H_2

$\rho_s \left(\frac{\Omega}{\square}\right)$

10^0 10^1 10^2 10^3 10^4

10^{13} 10^{14} 10^{15} 10^{16}

$N_d\ (cm^{-2})$

Fig. 4.1-3 Sheet resistivity versus implant dose for Si implantations.

10^{19}
$n(cm^{-3})$
R_p
Si → GaAs
300 keV, R.T.
Si_3N_4 Encapsulation
10^{18}
○ $Nd = 1.74 \times 10^{13} cm^{-2}$
850°C-30′-H_2
+ $Nd = 5.74 \times 10^{14} cm^{-2}$
850°C-30′-H_2
● $Nd = 1.74 \times 10^{15} cm^{-2}$
900°C-30′-H_2
10^{17}
0.2 0.4 0.6 0.8 1.0 1.2 1.4
d (μm)

Fig. 4.1-4 Electron concentration profiles for Si implants.

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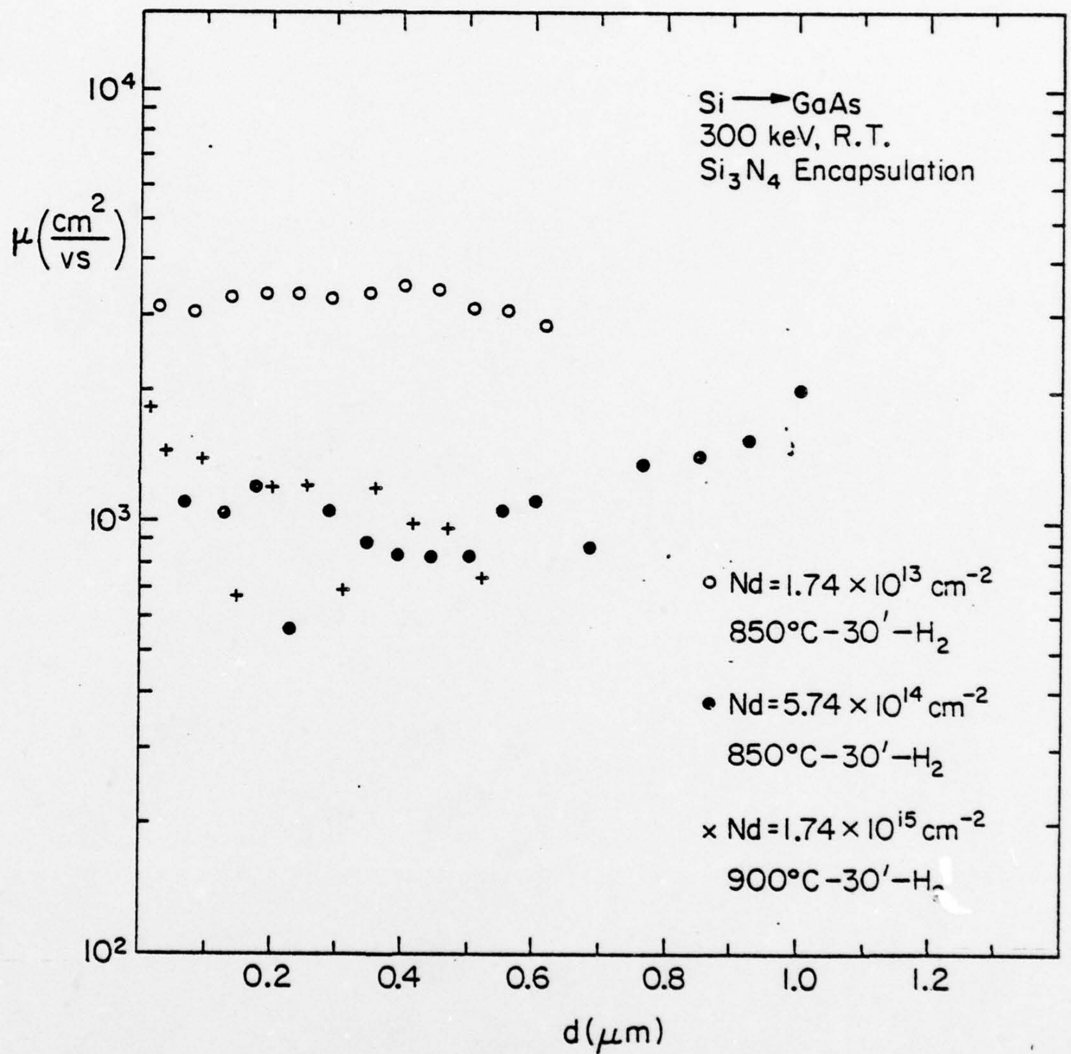


Fig. 4.1-5 Mobility profiles for Si implants.

description of the fabrication process steps in the first Quarterly Report.(1) The discussion here will be concerned with the current status of fabricated wafers and the development of a multi-layer interconnect process.

4.2.1 Planar GaAs IC Process Status

All circuits are being currently fabricated using the new 4X mask set (AR1), following the multiple-localized planar ion implanted process described in the last Quarterly Report.[1]. Fig. 4.2-1 is a cut away view of a planar GaAs IC showing the various devices and exhibiting the planar structure of this approach. The key feature is the utilization of two localized implantations in order to optimize the various discrete devices used in these circuits. A selenium implantation is used to produce the desired FET channel regions while sulfur is used for optimizing the high speed switching diodes. Both implants are incorporated in the ohmic contact and voltage level shifting diode regions of the circuits.

Sixteen planar GaAs IC wafers have been started in four wafer lots with the new AR1 mask. These GaAs ICs are being processed utilizing the 4X projection mask aligner (PMA) for all of the six photolithography steps. At this point in the process technology development, two implantation steps are being used. The optional third n^{++} ohmic contact implant step has not been incorporated yet. A 21 mm^2 wafer is currently used. A 7 mm^2 projected mask area is stepped four times on the PMA yielding a 14 mm^2 circuit area centered within the wafer.

Four wafers have been completed through the entire planar GaAs IC process including the second level interconnection process (discussed in Sec. 4.2.2). One of the completed wafers (AR1-1 was used for deliverables. Performance measurements, including ring oscillator results on some of these wafers are discussed in Sec. 5.2. Except for a few losses, the other wafers were at different stages of the process at the end of the reporting period.

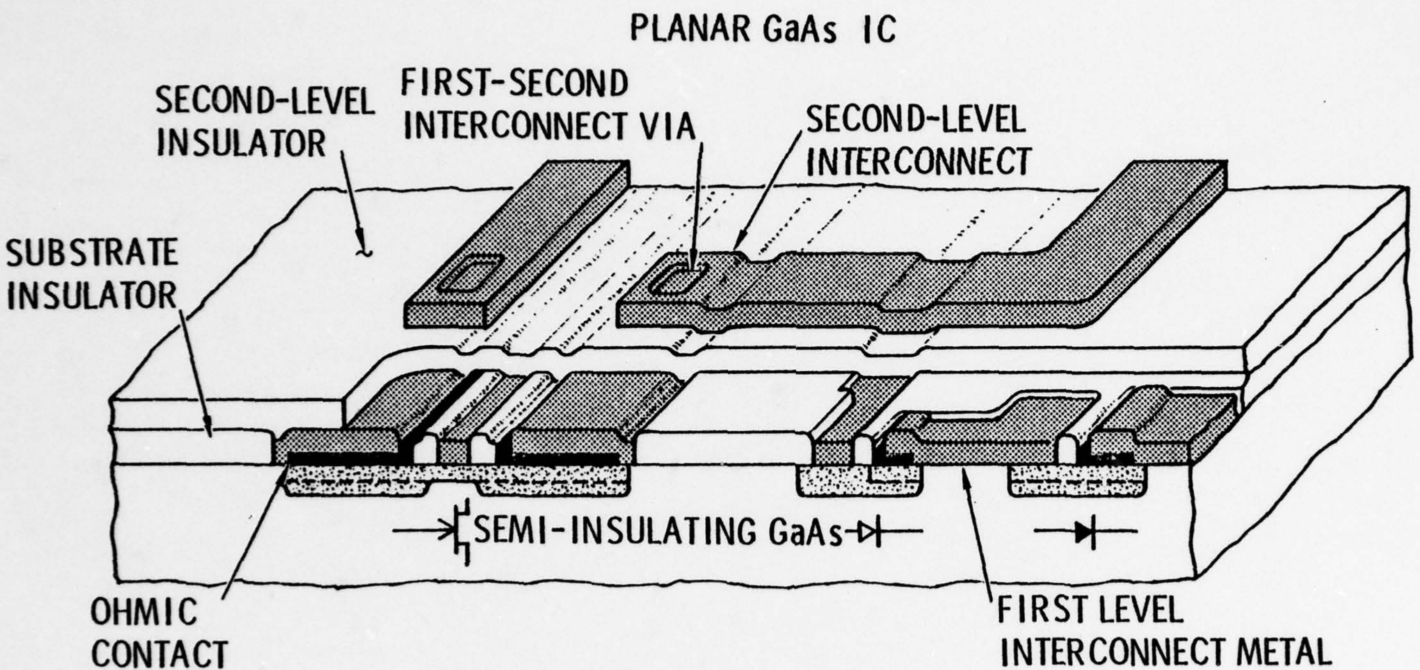


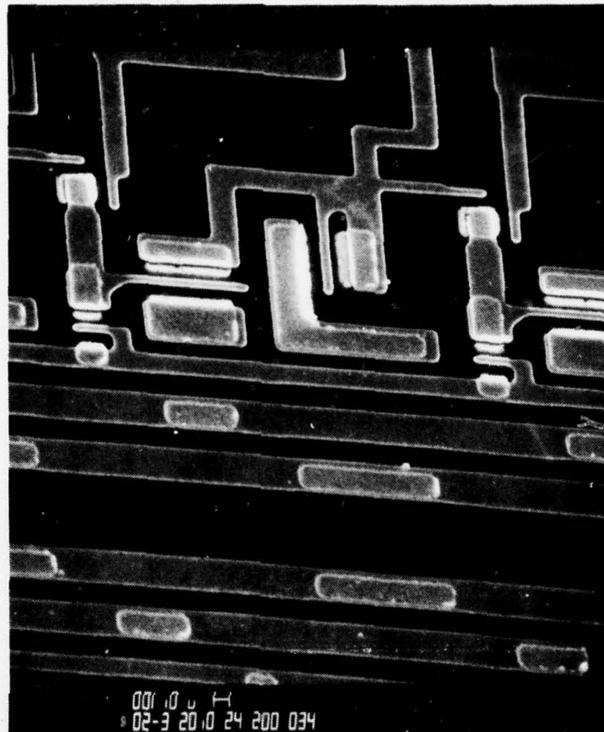
Fig. 4.2-1 Cut away view of various planar GaAs IC devices showing two implants, insulators, metalizations, and second level interconnect lines.

The GaAs ICs fabricated in this work are fully planar. A scanning electron micrograph (SEM) of a portion of a ring oscillator composed of 10 m NOR gates from wafer AR1-3 is shown in the upper photograph of Fig. 4.2-2. The smooth surfaces and absence of semiconductor or metallization steps demonstrate the planar featureless surfaces of these GaAs ICs. Excellent resolution of the lithography processes is evidenced by the small 1 μm resolved geometries of the FET gates and diode tabs which are precisely aligned within this high density circuit. The second level interconnects are not yet fabricated on this circuit in contrast to the lower photograph of Fig. 4.2-2 showing a completed 7 stage 20 μm NOR gate ring oscillator with second level interconnects. Power-delay performance results were determined for ring oscillator structures such as these (Sec. 5.2).

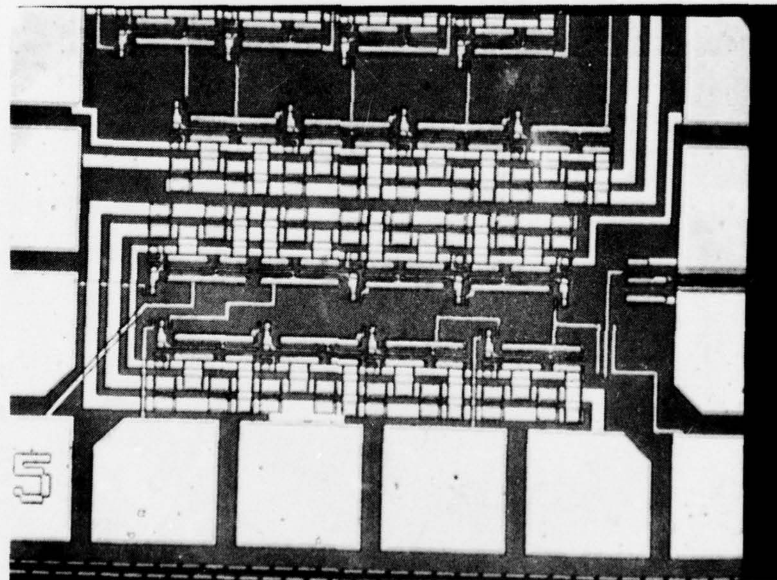
4.2.2 Second Level Interconnect Process

The planar GaAs IC in Fig. 4.2-1 shows the second level interconnect structure necessary for any complex digital logic circuit. There are a number of requirements which a multi-level interconnect fabrication process on GaAs must satisfy. The first and second level metal interconnections must be separated by a high quality dielectric material in order to electrically isolate interconnect crossover patterns. The dielectric must be pinhole free, relatively strain free, and have excellent adherence qualities to both semiconductors and metals. Any dielectric deposition technique must take into consideration the potential effects that heat and plasma fields may have on the GaAs device and circuit performance characteristics. Finally, the metal interconnect crossovers must be made as small as possible in order to minimize the additional capacitances that those crossovers contribute to the circuit.

Three possible dielectrics have been explored. They are RF sputtered phosphorus doped glass, pyrolytic SiO_2 grown by chemical vapor deposition (CVD) and plasma deposited Si_3N_4. Si_3N_4 was judged from the start of this program to be the best candidate for this application since it is a high quality pinhole free dielectric generally used when an excellent



AR1-3 SEM MICROGRAPH



AR1-2 RING OSCILLATOR

Fig. 4.2-2 (top) SEM micrograph of a 10μm NOR gate. (bottom) Photograph of a completed 7-stage ring oscillator composed of 20μm NOR gates.

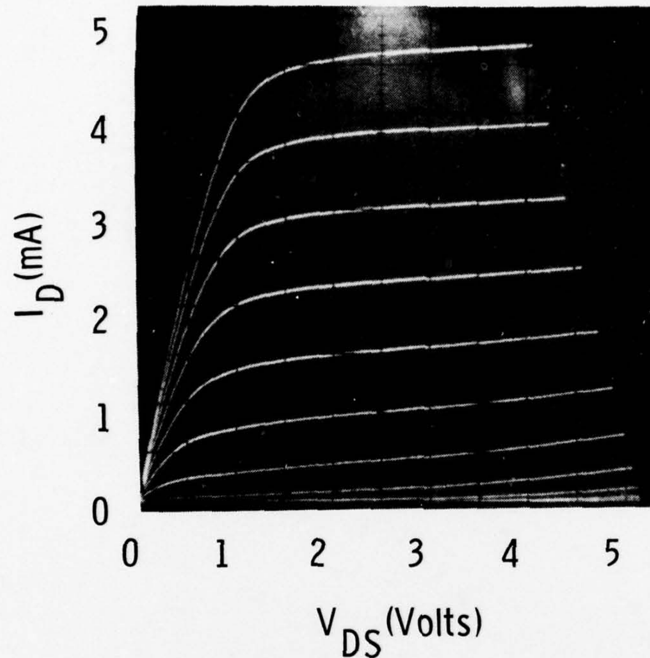
diffusion barrier is necessary. However, the only existing capability for depositing Si_3N_4 at the Science Center at the start of this program was the reactively sputtered Si_3N_4 system used for post implantation encapsulation. This type of deposition is unacceptable due to the relatively high temperatures and high powers utilized in sputtering. Therefore, a plasma deposition system for Si_3N_4 at the LFE Corporation (which manufactures this equipment) was used, while the other two dielectric approaches were being explored using facilities available at the Science Center.

The initial exploratory work soon indicated that plasma deposited Si_3N_4 was the most promising approach for the multi-level interconnect application. Therefore, a system was ordered from the LFE Corporation with delivery scheduled in February 1978. Plasma deposited Si_3N_4 films were used in the fabrication of the planar GaAs ICs whose performance characteristics are reported in Sec. 5.2.

The second-level interconnect process sequence utilizing plasma Si_3N_4 starts after the completion of first level interconnects, once the devices and circuits are dc tested and mapped for a go decision to continue the process The wafer is cleaned using a low energy O_2 plasma to remove any organics and to prepare the surface for adherence of the plasma Si_3N_4 film. A 3000A layer of Si_3N_4 is deposited on the GaAs ICs at a temperature of $\sim 300^oC$. A photoresist pattern is defined in order to open the via windows required to connect the first level interconnects to the second level interconnects. Via holes are plasma etched through the Si_3N_4 layer down to the underlying Au interconnect which serves as an automatic etch stop for the process. This is followed by the second level interconnect photolithography step and the evaporation of a metal layer composed of Ti-Pt-Au. The second level interconnects are then defined by a lifting technique completing the circuit fabrication.

Performance characteristics of planar FETs measured before and after the process just described are shown in Fig. 4.2-3 for wafer AR1-2. The dc I-V

BEFORE PLASMA Si_3N_4 ENCAPSULATION



PLANAR FET GEOMETRY

W = 50 μm Lg = 1 μm

V_{SAT} = 1.2 VOLTS

V_{PE} = -1.2 VOLTS

I_{DSS} = 2.25 mA/mil

g_m = 2.1 m mho/mil

AFTER SECOND LAYER INTERCONNECT PROCESS

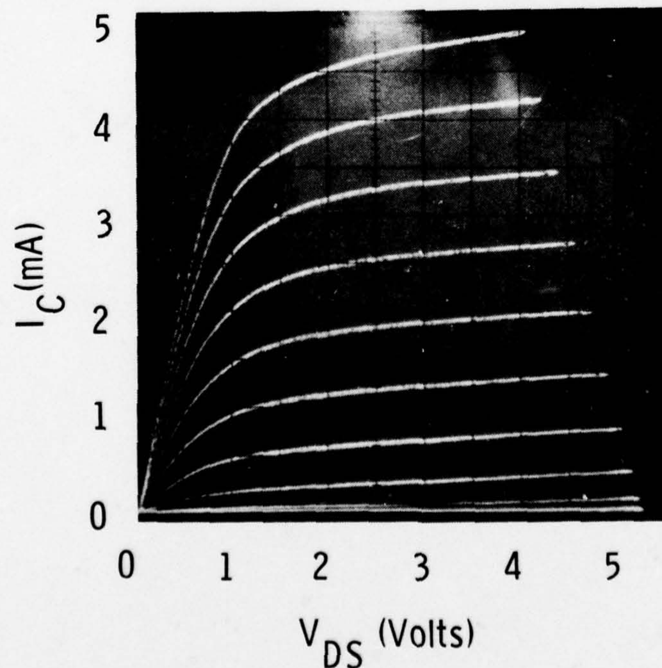
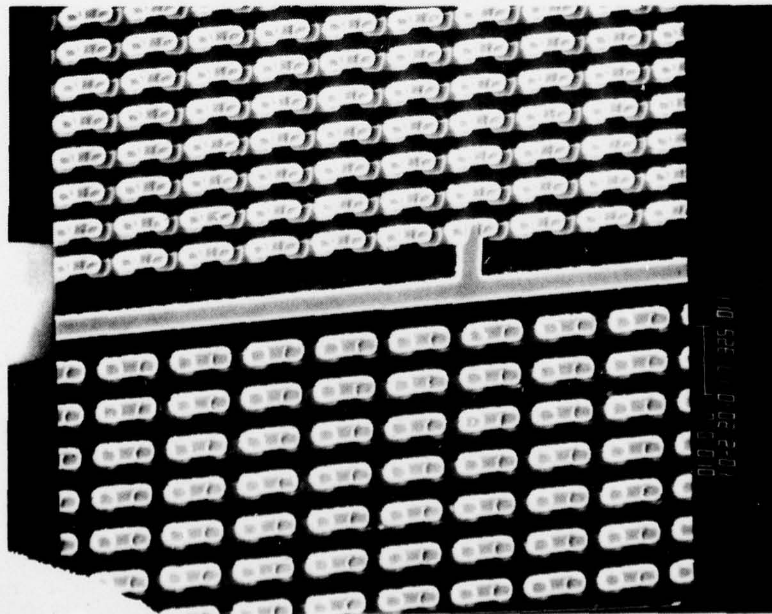


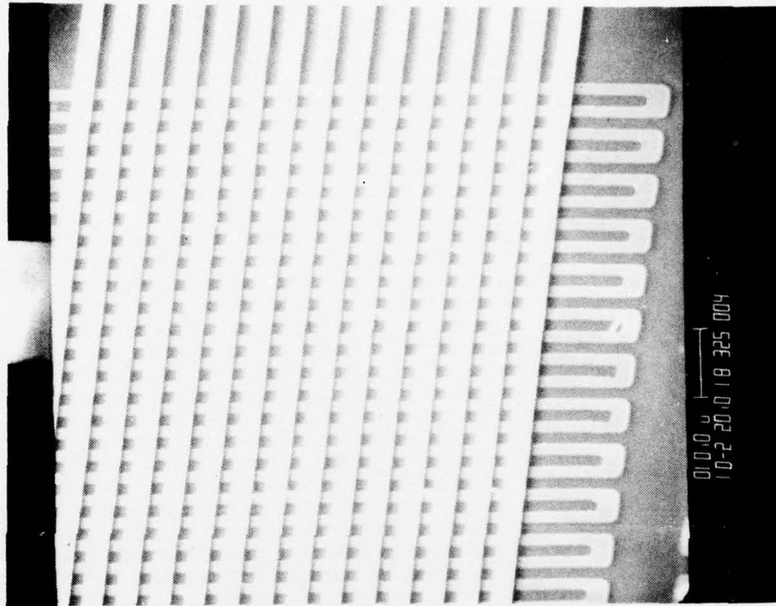
Fig. 4.2-3 I-V characteristics of a planar GaAs FET shown before and after the second level interconnect process.

characteristics for these 50 m wide planar FETs remain practically unchanged after the process. This is particularly significant since the devices tested have low currents and low pinch-off voltages. Other aspects of the second layer interconnect process have been equally successful. The very small, micron resolved, via windows and metal crossovers required for this high speed GaAs IC technology have been fabricated with little difficulty. Test patterns in the PM region of the IC mask containing chains of via connections and interconnect patterns have been evaluated and are shown in the scanning electron micrographs of Fig. 4.2-4. The left photograph shows a current path consisting of 3 μm wide alternating first and second level interconnect lines separated by Si_3N_4 and connected through 2 μm holes. As many as a thousand such via connections have been measured without continuity failure. On the right of the same figure 3 μm wide second level metal lines crossing over 1.5 μm wide first level metal lines are shown. Again, no failures were recorded from six hundred of these crossovers.

Although plasma Si_3N_4 is already the main approach used in this work, a brief summary of the experiments carried out with the other two alternative dielectrics follows. It is general knowledge that phosphorus doped glass has been used as a device encapsulant and has also been used in multi-level interconnect processes. However, the phosphorus glass applications have mainly been in Si technology, and its GaAs process capability is not clearly established. Experiments were conducted by coating low noise FETs with sputtered phosphorus doped SiO_2 in order to observe whether the deposition process altered the electrical performance of these devices. A RF sputtering system equipped with a SiO_2 sputtering target composed of 10% by weight of phosphorus pentoxide (P_2O_5) was used to deposit these layers. The sputtering was carried out using a 5 cm gap from anode to cathode, and a pressure of 20 microns of Argon. The initial results of this work showed that deposition power above 50 watts would degrade the FET performance. Therefore, subsequent experiments were conducted at 50 watts only. The best result was obtained at 50 watts for 20 minutes, depositing



WAFER AR1-1



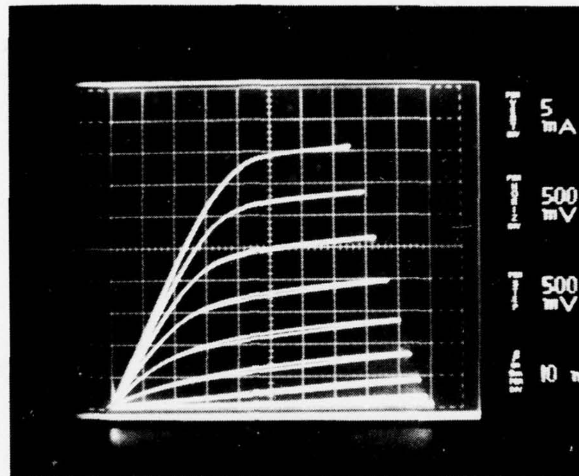
WAFER AR1-1

Fig. 4.2-4 SEM micrographs of via hole chains and crossovers showing first to second level interconnects separated by 3000Å of Si_3N_4.

only ~360A of phosphorus doped SiO_2. Figure 4.2-5 shows the I-V characteristics of an FET before and after this deposition process. The FET I-V characteristics were degraded significantly. Notice that the current level is lower after deposition, and the transconductance has also dropped. This device is coated with ~400A of SiO_2 which is much too thin for the multi-level interconnect process. If the power is increased to deposit glass at a higher rate in order to produce the ~3000A layer required in this application, the device degrades even further than what Fig. 4.2-5 shows. It is anticipated that full ICs will degrade even further than the tested FETs, because of their operation at low voltage thresholds. Due to these rather poor results, and the impractical deposition rates required, the phosphorous glass approach was abandoned.

Similar work was carried out using pyrolytic SiO_2 deposited at 300°C by CVD. Results on these experiments looked more encouraging from the device performance standpoint, but difficulty was encountered with the reliable adherence of the deposited SiO_2 on the metal interconnects. Investigation of this process will continue. In view of the initial experiments using plasma Si_3N_4, which showed little device performance changes and no adherence problems, plasma Si_3N_4 has become the main process approach, with pyrolytic SiO_2 as a potential backup process. Future work on second layer interconnects will undertake the development of a dry etching process. Ion milling (ion beam etching) will be the main approach investigated.

BEFORE P-DOPED SiO_2 ENCAPSULATION



150μm WIDE BY 1μM LONG FET

AFTER P-DOPED SiO_2 ENCAPSULATION

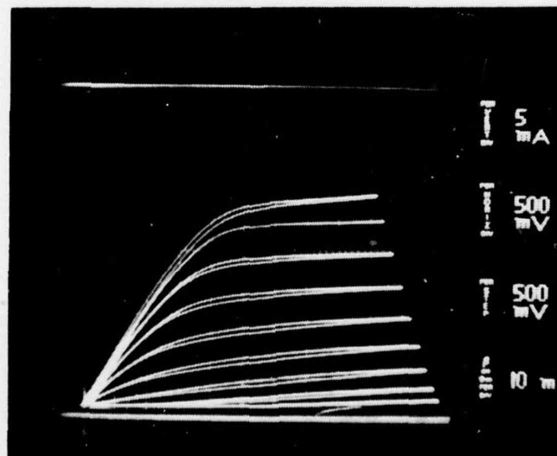


Fig. 4.2-5 I-V characteristics before and after sputter deposition of a P-doped SiO_2 on a standard low noise FET.

5.0 CIRCUIT MONITORING AND TESTING

An important factor defining the number of logic gates attainable per unit chip area is the circuit design used. Where in previously published GaAs FET digital IC work, GaAs FETs themselves are used as the linear logic elements, with this planar, multiple implantation approach, optimized GaAs Schottky barrier switching diodes can be fabricated. Inasmuch as GaAs Schottky barrier diodes are among the fastest switching semiconducting devices existing and their switching energy and required chip area are very low, their use as logic elements in GaAs digital ICs seems quite desirable. A logic circuit approach using such high speed GaAs Schottky barrier switching diodes for most logic functions, with GaAs Schottky gate FETs used for inversion and gain, will be described in section 5.1. This approach, called Schottky diode FET logic (SDFL) allows major saving of chip areas as compared to previous approaches. In the same section, circuit components, FETs and switching diodes, fabricated with our planar process, will be evaluated. Finally, the operation of the SDFL NOR gates will be presented and discussed. In section 5.2 measurements of the oscillation frequency of ring oscillators made with SDFL will be presented. For ring oscillators using 10 μm NOR gates propagation delays as low as 120 ps were measured with dynamic switching energies as low as 46 fJ observed (at $P\tau_D$ = 140 ps). For larger, 20 μm NOR gates, propagation delays as low as 82 ps with speed power products in the 200-250 fJ range have been measured. Finally, in Section 5.3 a theoretical analysis of switching speeds of depletion mode, FETs, carried on at Cornell University, will be presented.

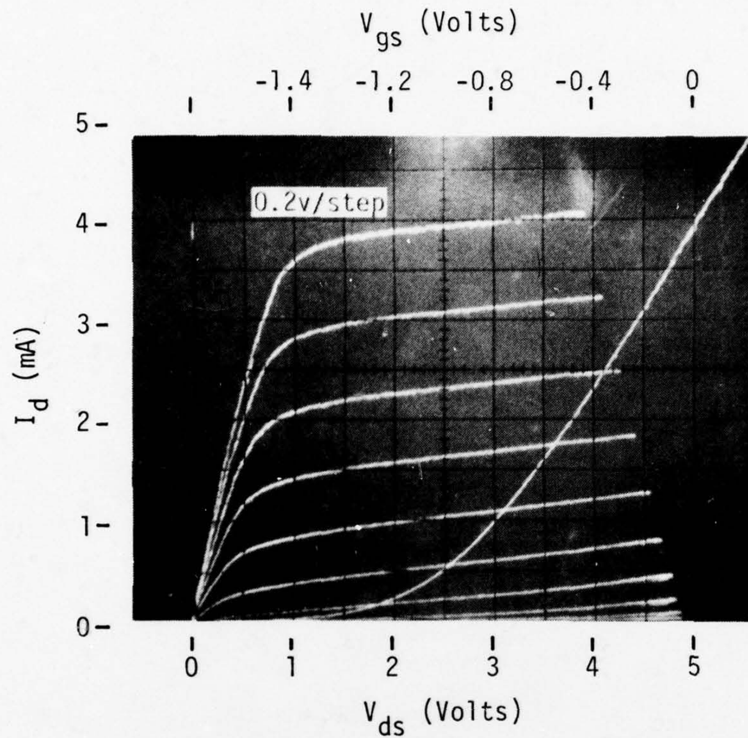
5.1 Low Frequency Measurements (Science Center)

In Section 4.2 on Device and Circuit Fabrication some results on low frequency measurements on FET devices have been anticipated in order to evaluate the effect of the second layer metallization process on the FET characteristics. Here the properties of the Schottky-gate FET and Schottky barrier switching diodes which constitute the principal circuit elements in our circuit approach will be reviewed. Fig. 5-1-1 shows the I-V character-

istics of a typical FET and a typical switching diode. Both devices are among numerous test elements which have been incorporated in the mask currently used for the process (see the previous Quarterly Report).(1) Both devices exhibit excellent characteristics. The characteristics shown on the top portion of Fig. 5.1-1 correspond to a 50 μm wide FET with a 1 m long gate. The device has a saturation current of 3.8 mA. The saturation voltage is only 0.9 volts with low on resistance, R_{on} = 200 ohms, indicating good ohmic contacts. The effective pinch-off voltage (defined as the zero crossing of a linear extrapolation of V_{gs} vs V_{ds}) is -0.95 volts. The transconductance is 4.1 mmho, corresponding to 2.05 mmho/mil. These figures are quite satisfactory for the logic circuit requirements.

The I-V characteristics shown on the bottom part of Fig. 5.1-1 correspond to a switching diode with an area of only 1 μm by 2 μm. These dimensions are identical to those used in all the tests circuits designed on the mask. The forward characteristic is near ideal up to a current on the order of 100 μA. This is the range in which the device is required to operate in most of the circuits. The voltage drop at 50 μA is 0.69V. At higher current, the deviation of the I-V characteristic from that of an ideal diode due to the limiting series resistance of the implanted area forming of the diode and the ohmic contact resistance became appreciable. The series resistance determined from an analysis of the I-V characteristic shown in Fig. 5.1-1 is only 900 ohms. Since this diode has an estimated capacitance of 2×10^{-15} F, the cutoff frequency is as high as 90 GHz. The reverse characteristic, not shown in the figure, indicates a breakdown voltage of 14V, which is expected for the 10^{17} cm^{-3} carrier concentration of implanted layer on which the diode is formed.

An important issue is whether scaling FET dimensions can achieve the low operating current required by high circuit density. This issue was addressed when the mask set currently in use was designed by incorporating a test on the effect of scaling the dimensions of active loads (FETs with the gate connected to the source). This test is on Lot PD12 of the process



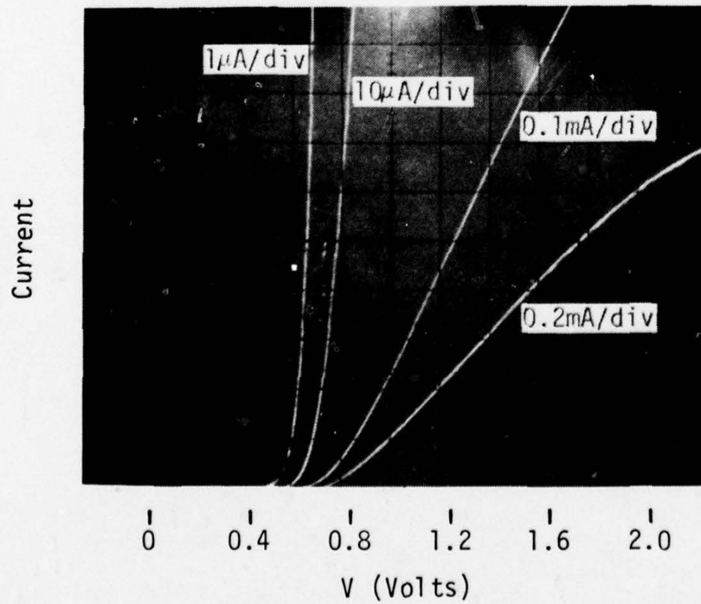
Wafer AR1-3
FET

W=50μm   Lg=1μm

I_{dss}=1.9mA/mil

g_m = 2.05 m mho/mil

V_{pe} = -0.95V



Wafer ARI-3
Switching Diode

Area: 2μm x 1μm

Series Resistance
R_s = 900Ω

Ideality factor
n = 1.4

Fig. 5.1-1 I-V characteristics of a typical FET and a typical switching diode. The devices are in test pattern T2 of mask ARI.

development chip (see previous Quarterly Report).[1] The results of this test from wafer AR1-9 are presented in Figs. 5.1-2. In this figure the logarithm of the saturation current of the active loads is plotted against the logarithm of the channel width for 1 μm and 2 μm gate devices. This is done for a channel width varying from 40 μm to 1 μm. The results in Fig. 5.1-2 are quite satisfactory. Both the 1 μm gate and 2 μm gate saturation currents fall on straight lines at 45°, indicating that the saturation current scales linearly with channel width. As the figure shows, this scaling can be accomplished effectively down to 1 μm wide channels.

In Fig.5.1-2, two types of active load design have also been compared. The black circles and squares correspond to active loads designed like FETs with their gates connected to the sources. The white circles and squares correspond to a simpler design in which the gate is formed by extending the Schottky metal contact on the source 1 or 2 μm into the channel. This second design has not been used in the test circuits of this mask because achieving the proper 1 or 2 μm extension of the Schottky metal into the channel depends on its alignment with the ohmic contact. While in the FET-like active load the gate length is by the Schottky metal mask without any critical alignment. However, the fact that in Fig. 5.1-2 all the data points for the extended source design fall very close to those for the FET-like design, speaks very highly for the quality of the alignment achieved.

As mentioned earlier in Sec. 5.0, the circuit design makes full use of the high switching speed of Schottky barrier diodes and of their very low switching energies. This logic circuit approach, developed previously to the inception of this contract, is called Schottky diode FET logic (SDFL). An SDFL NOR gate is presented in Fig. 5.1-3. The top portion of this figure shows a micrograph of a two-input NOR gate with a 10 μm wide FET (Lot PD31 of the process development chip)[1]. Each electrical node in this gate circuit is connected to a contact pad for test purpose. The bottom part of Fig. 5.1-3 is a schematic of the gate. Note that the logic OR function is performed by

WAFER AR1-9 CHIP 42
ACTIVE LOADS

● SHORTED GATE, Lg = 1μm
○ EXTENDED SOURCE, Lg = 1μm
■ SHORTED GATE, Lg = 2μm
□ EXTENDED SOURCE, Lg = 2μm

Lg = 1μm
Lg = 2μm

Lg = 1μm I_{ds} = 62μA/μm
Lg = 2μm I_{ds} = 29μA/μm

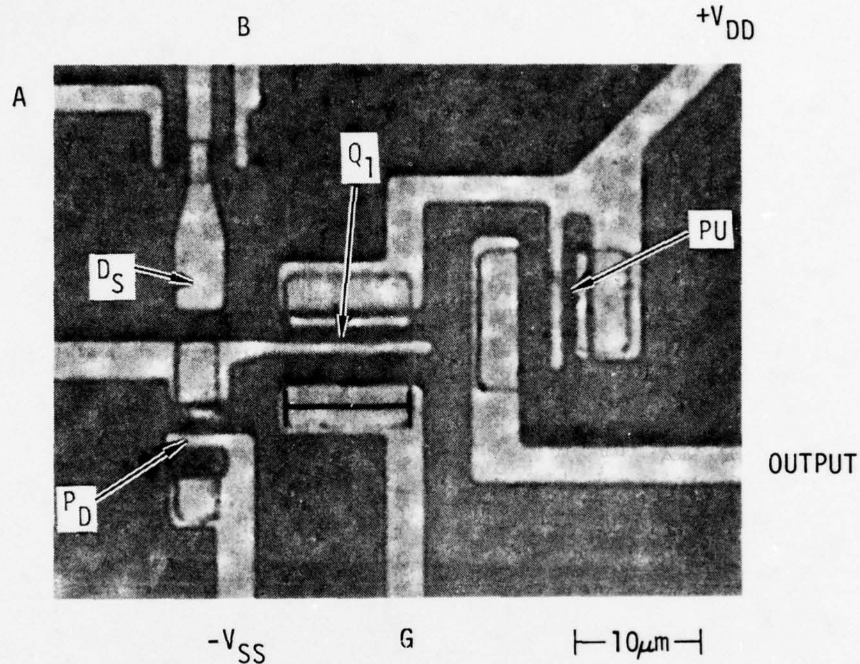
I_{ds} (mA)

1
0.1

W(μm)

1
10

Fig. 5.1-2 Scaling of active load current with channel width, W, and gate length, Lg.



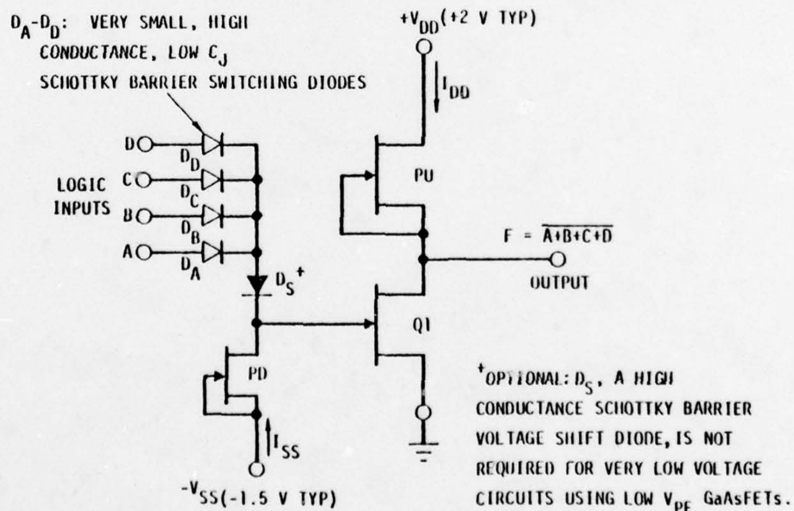


Figure 3. Circuit diagram for a 4-input NOR gate in the Schottky diode-FET logic (SDFL) circuit approach. All GaAs FET's and active loads are depletion-mode (normally-on Schottky gate types.

Fig. 5.1-3 Micrograph and circuit diagram for a NOR gate in the Schottky diode-FET (SDFL) circuit approach. All GaAs FETs and active loads are depletion-mode (normally-on) Schottky gate types.

the very small area switching diodes. The active load pull down (PD), with or without an additional diode D_S provides level shifting from the positive logic polarities at the FET drain, to the required negative gate voltages to be applied to FET Q1. The FET Q1 with an active load pull up (PU) provide inversion and gain.

The approach presented in Fig. 5.1-3 allows major savings of chip area as compared to the previous approaches in which FETs have been used as the logic elements.[2,3] For example, a four-input NOR gate in FET logic (enhancement or depletion) would have a minimum of four switching FETs (each input is an FET gate) plus an active load. On the other hand, as shown in Fig. 5.1-3, the SDFL approach requires only the single FET with its load, and four very small switching diodes. Besides performing the OR logic function, the switching diodes also provide some or all of the level shifting required in depletion mode logic. In addition to the savings in area because of the much smaller size of the Schottky barrier diodes as compared to FETs, additional area is saved because a diode is a two terminal device, so that the many overcrossings associated with the use of three terminal logic elements such as FETs are largely avoided.

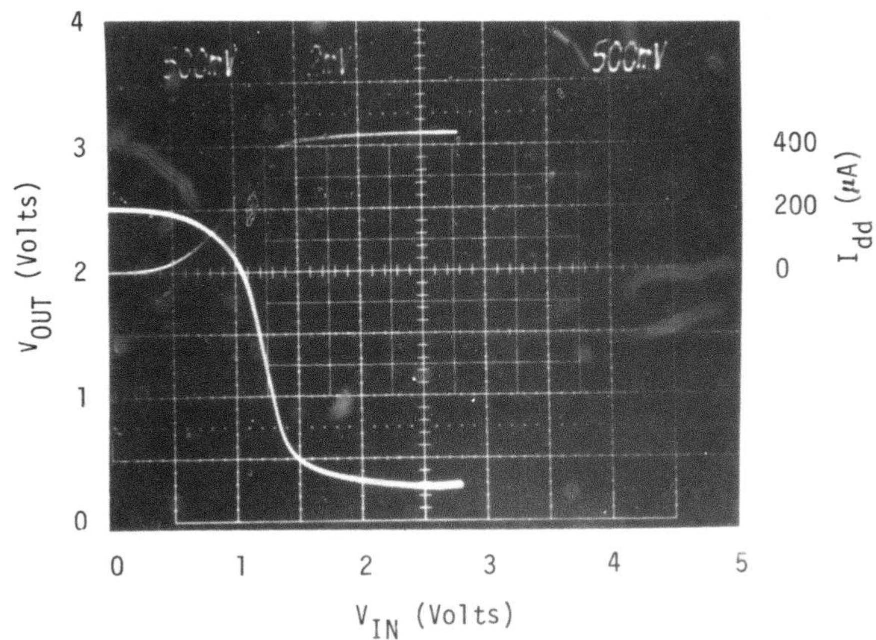
Fig. 5.1-4 shows the low frequency input-output transfer characteristic for a 10 μm NOR gate. This gate, nearly identical to the one shown in Fig. 5.1-3, is in test lot T2 (see previous Quarterly Report).[1] For this measurement one of the two inputs was left open, which is equivalent to a "low" logic input so that the gate is operating like an inverter. The threshold voltage is 1.5V and the ac gain at threshold is approximately 4. The positive supply current is also shown in Fig. 5.1-4. The value of 440 μA determined by a 7 μm wide active load corresponds to the 60 μA/μm saturation current determined in Fig. 5.1-2.

The performance of the NOR function is demonstrated in Fig. 5.1-5. This oscilloscope picture was taken with the A and B input voltages applied to the horizontal and vertical amplifiers while the output was applied to the Z

Wafer AR1-2

Chip 11

Subchip PD24 (T2)



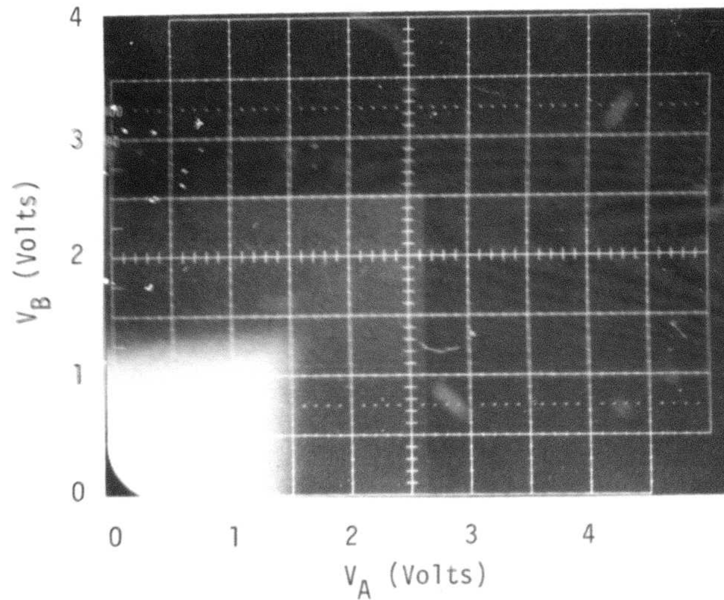
V_{dd} = 2.5V
V_{ss} = -2.0V

Fig. 5.1-4 Low-frequency (quasi-static) switching characteristics for a 10μm GaAs SDFL gate of the type shown in Fig. 5.1-3. The larger curve is the output voltage, while the smaller curve near center is the positive supply current.

Wafer AR1-9

Chip 12

Subchip PD42 (T_2)



V_{dd}=3.0V

V_{ss}=-1.1V

Fig. 5.1-5 Demonstration of the logic function of a two-input NOR gate of the type shown in Fig. 5.1-3. The x and y axis represent the voltages applied to the A and B inputs respectively. The output voltage is represented by the z intensity (bright corresponds to $V_{OUT} > 1.3$ Volts)

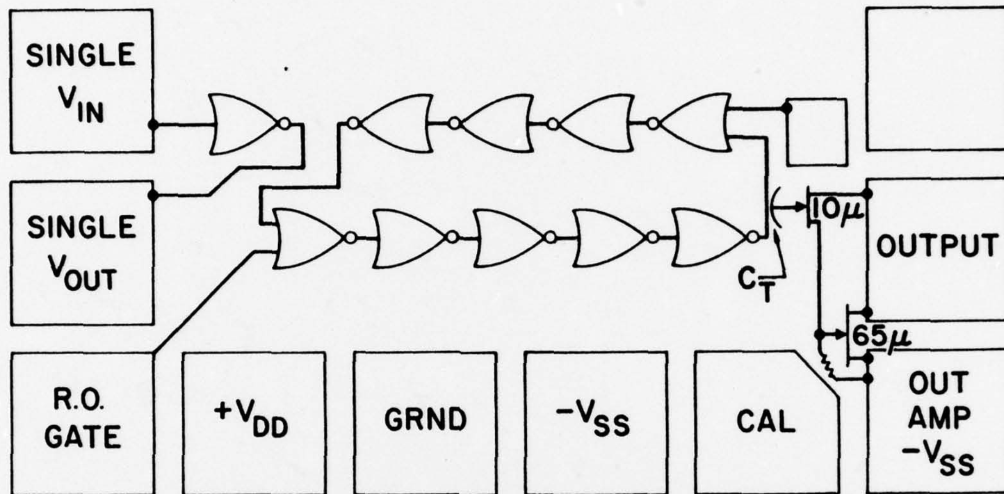
input of the oscilloscope. The intensity was adjusted so that "bright" corresponds to V_{out} 1.3V, which corresponds to a "high" logic state. Fig. 5.1-5 shows that the output is "high" only when both inputs are "low", as required for a NOR gate.

In the next section results on the high speed performance of the SDFL circuits will be presented.

5.2 High Speed Measurements (Science Center)

Measurement of propagation delay and switching waveforms has been facilitated by the use of ring oscillator chains composed of an odd number of SDFL NOR gate or inverter stages. This provides a simple way of determining gate propagation delay from a measurement standpoint since the ring oscillator provides its own signal source, and there are many propagation delays cascaded in the ring. This allows measurements to be made in a frequency or speed range in which highly accurate equipment is more readily available. The oscillation frequency is determined by $f_o = 1/(2N\tau_d)$, where τ_d is the propagation delay and where N is the number of gates in the ring which is typically chosen to result in an f_o below 1 GHz. All dynamic measurements of propagation delay carried out on this program have utilized ring oscillators.

Figure 5.2-1 presents a schematic diagram and an SEM photograph of a 10 μm NOR gate implemented, 9-stage SDFL ring oscillator. Dynamic switching measurements were carried out on both the 10 μm, 9-stage and 20 μm, 7-stage ring oscillators. Both types of ring oscillators were designed in versions which included or excluded a level shift diode between the input Schottky diode or gate and the FET inverter. Two of the gates at the corners of the ring oscillator loop have two inputs, one of which can be utilized for gating the oscillations with a lower frequency pulse. Also included in all cases is an additional single input gate for low frequency characterization of gate transfer characteristics.



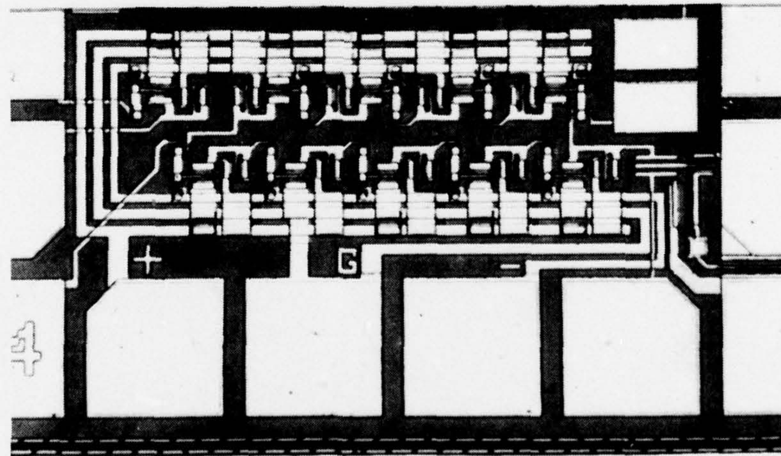


Fig. 5.2-1 Schematic diagram and SEM photograph of 10μm, 9-stage ring oscillator.

The outputs of all devices in the ring oscillator loop are loaded with a fanout of one. The output for high speed measurements is obtained through a capacitively coupled output buffer amplifier. This consists of a Darlington connected 1 μm long x 10 μm wide source follower driving a 1x65 μm output pad driver as shown in Fig. 5.2-1. This permits driving a 50Ω load without significantly changing the transfer characteristics of any ring oscillator gates through loading. The output stage is DC isolated from the ring oscillator so that a separate power supply can be used. Thus, the power dissipation of the buffer amplifier does not affect the accurate measurement of ring oscillator power dissipation.

A separate measurement station has been set up for high speed measurements. This system utilizes a custom built prober which is presently operational in a manual mode. Automatic probing will be introduced at a later stage when hardware required to interface between an Apple II microcomputer and the control systems of the probe station is completed.

A block diagram of the measurement system utilized to determine switching waveforms and propagation delays on ring oscillators is shown in Fig. 5.2-2. This measurement system is capable of operation in principally two different modes: CW ring oscillator operation, and gated ring oscillator operation. In CW operation the output of the B&H DC3002 preamplifier is split between a Tektronix 7L13 spectrum analyzer and a Tektronix 7834, 400MHz storage oscilloscope. The spectrum analyzer has an associated TR502 tracking generator, the output of which is measured through a ÷10 prescaler on a DC505 frequency counter. Observation of the frequency spectrum of the ring oscillator output on the spectrum analyzer enables us to see the oscillating frequency, the general richness of the harmonic content (which relates to rise time) and the waveform symmetry which is reflected in the relative amplitudes of the even harmonics as compared to the odd harmonics (the even harmonic amplitudes should be zero for a perfectly symmetrical square wave). For frequency measurements, the spectrum analyzer is simply tuned to the peak of

DEVICE UNDER TEST
FG502
SINGLE V_{IN}
SINGLE V_{OUT}
TO 7834 HORIE INPUT
TO 7834 VERT INPUT
$V(\tau)$ V_H V_L TIME,τ
R.O. GATE
$+V_{DD}$
GRND
$-V_{SS}$
CAL
OUTPUT
OUT AMP $-V_{SS}$
C_T 10µ 65µ
50Ω .01
10Ω I_{DD} 10Ω I_{SS}
+ COM - PS503A
+ COM - PS503A
-3V
1K 10K
.01
50µA
BIAS NULL METER
50 dc X 10
B&H DC 3002 DC TO 3GHZ 20dB GAIN
GATING PULSE GENERATOR
TEKTRONIX PG502
SYNC
SAMPLING OSCILLOSCOPE
7704A DIGITAL PROCESSING OSCILLOSCOPE
7512
S-6 S-53
DC 505 FREQUENCY COUNTER
PRESCALER −10
TR502 TRACKING GENERATOR
7613
7L13 SPECTRUM ANALYZER 0-1.8GHZ
50Ω RESISTIVE POWER DIVIDER
SIGNAL INPUT
ALTERNATE CONNECTION FOR UNGATED WAVEFORM SAMPLING OSCILLOSCOPE MEAS.
X10
B&H AC3020
7834
400M HZ TRANSIENT STORAGE OSCILLOSCOPE
LOW FREQUENCY INPUTS FROM SINGLE GATE FOR TRANSFER CHARISTICS AND I_{DD}, I_{SS} CURRENT MONITORS
ALTERNATE CONNECTION FOR MEASURING UNSYNCHRONIZED SIGNALS AND TRANSIENTS WITH SINGLE-SHOT STORAGE

Fig. 5.2-2 Circuit and block diagrams of dynamic switching measurements on ring oscillators.

the fundamental, and the output of the tracking generator is measured on the counter. CW ring oscillations are also conveniently observed with the Tektronix 7834 high speed transit storage oscilloscope by simply directly recording a short segment of the ring oscillator output. The frequency can also be measured directly with a 7D14 525MHz counter in the other horizontal compartment of the 7834. The limited bandwidth of the 7384 (somewhat over 400MHz) makes the waveform fidelity for higher frequency ring oscillator outputs poor. Some success with sampling measurements of CW ring oscillator outputs has been obtained by amplifying the B&H DC3002 signal output with a B&H AC3020 x 10 amplifier to drive the S53 trigger recognizer input on a 7S12 sampling oscilloscope plug-in for the Tektronix 7704A/digital processing oscilloscope system. Here, the other output from the power divider is run to the S-6 sampling head input for direct measurement of the CW ring oscillator output waveform with bandwidth limited only by the output amplifier.

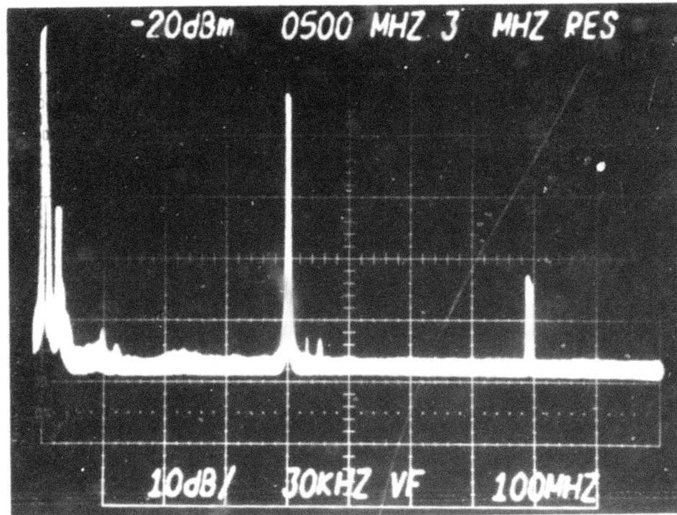
Clean, very low jitter ring oscillator output waveforms may be measured by using the gating technique. In this technique, the output of the ring oscillator is gated by applying a pulse input signal to one of the extra ring oscillator NOR gate inputs as shown in Figs. 5.2-1 and 5.2-2. When the gating signal is at a logic "HI", the output of that particular NOR gate is held "LO" and, consequently, the ring oscillations cease. When that gate input is dropped "LO", then the ring oscillator is free to operate normally and a burst of ring oscillator output pulses is observed at the output amplifier. Clean sharp startup characteristics of this burst indicate good logic gate gains as required for general logic applications.

The digital processing oscilloscope is usually utilized for the gated ring oscillator measurements so that signal averaging techniques can be used to minimize the influence of sampling noise in the output signal, and also so that most of the effects of direct capacitive feed through from the ring oscillator gate pulse to the output amplifier can be subtracted out. This is accomplished by first signal averaging and storing the gated ring

oscillator output under normal (oscillating) bias conditions, and then reducing $-V_{SS}$ below the threshold for ring oscillation and again signal averaging and storing the waveform (consisting principally of direct capacitive feedthrough of the gating signal to the output amplifier). The digital processing oscilloscope then is utilized to subtract this direct gating feedthrough waveform from the composite ring oscillator plus feedthrough waveform to get the gated ring oscillator output. At the present time a Tektronix PG502 pulse generator having approximately a 1ns rise time is being utilized for the gating source, operating in a square wave mode at a typical 5-10MHz frequency. Spectrum analyzer measurements of the gated ring oscillator output show, as would be expected, a breakup of each of the harmonic lines into a broad spectrum of lines separated by the gating pulse repetition frequency because of the effective amplitude modulation of the ring osicllator output by the gating signal.

High speed ring oscillator performance on wafer AR1-2 was measured on 10 μm and 20 μm, two-diode versions. These versions are identified as subchips PD52 and PD51, respectively.[1] Because of the repetitive mask format, 32 subchips of each type are available for probing. These are referred to as chips and are identified by the usual matrix notation (chip 11 through chip 66). Note that chips 22, 25, 52 and 55 are utilized for PM lot assignments.

The lowest dynamic switching energy ($P\tau$ product) was measured on PD52. A spectrum analyzer scan of CW oscillations from chip 51 with 100 MHz/division and 10 dB/division scales is shown in Fig. 5.2-3. The oscillation frequency as measured from the tracking generator was 397.4 MHz. This results from a propagation delay $\tau_d = 1/(2Nfo) = 139.8$ ps per gate and it yields a dynamic switching energy of 46.4 fJ/gate. Power dissipation per gate (10 gates are powered on the subchip) was 331.8 μW.



AR1-2
CHIP 51
SUBCHIP PD52

Fig. 5.2-3 Spectrum analyzer measurement of lowest dynamic switching energy ring oscillator. This CW output was obtained from a 10μm, 9-stage device. V_{DD} = 1.600 volts at 1.85 mA and V_{SS} = -0.863 volts at -0.415 mA. P = 331.8μW/gate, f_{OSC} = 397.4 MHz. τ_D = 139.8 pS. $P\tau_D$ = 46.4 fJ/gate.

Time domain measurements of the switching waveform under gated operation were made using the sampling oscilloscope . This is shown in Fig. 5.2-4. This waveform resulted from a 68 nsec gating pulse applied to the ring oscillator gate pad shown in Fig. 5.2-1. Operating V_{DD} and V_{SS} bias was shifted slightly to achieve optimum turn-on characteristics. Under these conditions, an oscillation frequency of 393.74 MHz was measured. This frequency yields a $P\tau_d$ product of 47.3 fJ/gate. The clean startup of the ring oscillator as soon as the gating hold off signal is removed is indicative that gate gains are significantly high and real logic functions are capable of being performed at these speeds.

The 20 m SDFL NOR gates in subchip PD51 give, as expected, consistently higher speed results than the 10 μm SDFL NOR gates, though at the expense of power dissipation and $P\tau_d$ product. The highest speed 20 μm, 7-stage ring oscillator from AR1-2, PD51 had an oscillation frequency of 864.2MHz corresponding to a propagation delay of 82.65 ps per stage. A spectrum analysis of this device output is shown in Fig. 5.2-5. Power dissipation per gate was 2.782 mW for a $P\tau_d$ product of 0.231 pJ/gate.

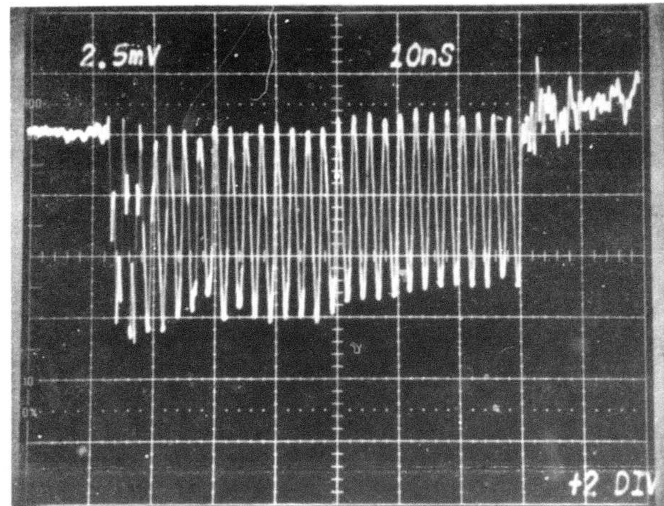
In conclusion, these initial results on GaAs FET logic integrated circuits using the high density SDFL approach are very promising, indicating that this technology can indeed realize very high performance integrated circuits of LSI or VLSI complexity.

5.3 Switching Speed Analysis (Cornell University)

A new two-dimensional model of a GaAs Schottky gate FET described in the previous report has been used for the calculation of FET parameters.

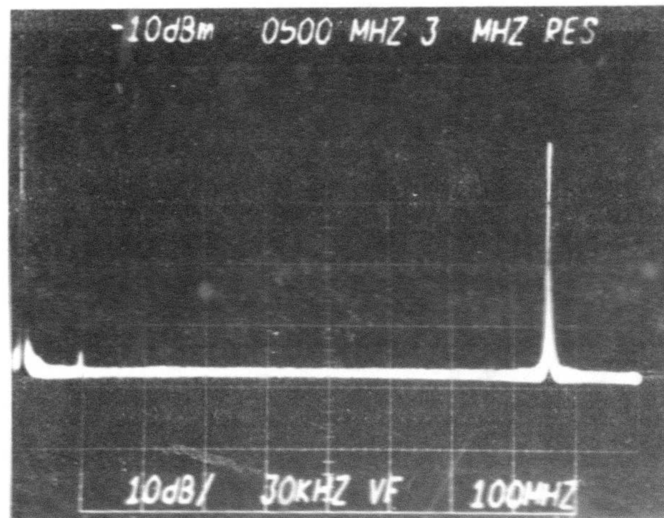
The main features of this model are as follows:

1. It divides the MESFET into three sections: (a) a source-gate portion which is assumed to behave like an ohmic resistor, (b) a channel under



AR1-2
CHIP 51
SUBCHIP PD52

Fig. 5.2-4 Sampling oscilloscope measurement of 9-stage ring oscillator output waveform with gating pulse applied to the R.O. GATE pad of the chip of Fig. 5.2-1. V_{DD} = +1.684 volts at 1.83 mA, V_{SS} = -0.783 volts at -0.345 mA (for 10 gates). P_D = 335.2μW/gate, f_{osc} = 393.74 MHz, τ_D = 141.1 pS, $P_D\tau_D$ = 0.0473 pJ (47.3 fJ).



AR1-2
CHIP 65
SUBCHIP PD51

Fig. 5.2-5 Spectrum analyzer plot of CW oscillations from the fastest 20μm SDFL ring oscillator. V_{DD} = 2.724 volts at 7.50 mA and V_{SS} = -1.162 volts at -1.57 mA. P = 2.782 mW/gate, f_{osc} = 864.2 MHz, τ_D = 82.7 pS and $P\tau_D$ = 0.230 pJ/gate.

the gate, (c) an adjacent Gunn domain extending towards the drain which might form if the electric field at the drain side of the channel is larger than a sustaining domain field E_S. In this aspect the model is similar to one developed in Ref. 4. (See Fig. 5.3-1).

2. The x-component of the electric field under the gate is always smaller than the electron velocity peak field E_p. The heating of electrons under the gate is thus negligibly small.

3. The carrier concentration changes gradually at the boundary of the depletion layer due to diffusion effects. This distribution is approximated by a sinusoidal function and a two-dimensional solution of Poisson's equation for the approximated carrier distribution is used.[5]

4. The drain current I_D has two components, the channel current, I_{ch}, flowing through the channel and the Gunn domain, and a leakage current, I_S, in the non-ideal interface and substrate regions which have an effective shunt resistance R_S. This feature is also similar to one considered in Ref. 4.

5. The ohmic resistances, R_{gs} and R_{dg}, of the gate-source and gate-drain portions, and the contact resistances, R_{gc} and R_{dc}, are considered as in series with the channel and the Gunn domain.

The computation in the frame of this model involves only one iteration process to determine the field distribution under the gate. It requires about 0.25 seconds of computer time per point. The results obtained agree well with the results of full two-dimensional computer calculations.

This model was applied to a calculation of current voltage characteristics, switching time and small-signal parameters of GaAs FETs (such as transconductance g_m, and gate-to-source capacitance C_{gs}).

Fig. 5.3-1 MESFET Geometry

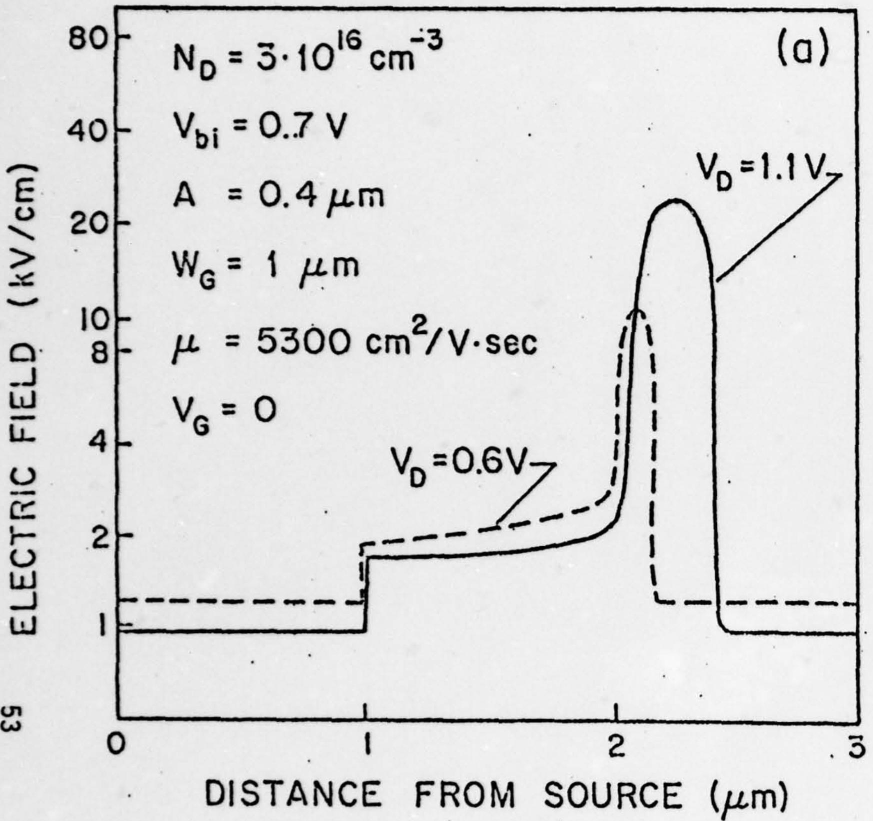
In Fig 5.3-2 and 5.3-3 the results of the calculations in the frame of the above model are compared with those of a two-dimensional computer analysis.[6] The agreement is very good but the calculations for $V_G = 0$ show a region where the I_D vs V_D curves exhibit hysteresis. This hysteresis is related to the well-known behavior of the Gunn domain which is illustrated by a qualitative curve in the inset in Fig. 5.3-3. It is also well established that such a hysteresis can be actually observed only in very homogeneous samples when the doping density is relatively small ($n \;\; 5 \times 10^{16}$ cm^{-3} for GaAs), and when special boundary conditions are satisfied at the cathode contact.[7] Otherwise the current-voltage characteristic looks as shown by the dotted lines in Fig. 5.3-3. This shape is better generated by the two-dimensional computer calculations.[6] The two-dimensional computer calculation indicates that the external field E_{ext} is smaller than the domain sustaining field E_s (though at the peak value of the current E_{ext} is close to E_s),[6] indicating that the negative resistance is stable and no domain propagation occurs.

In Fig. 5.3-4 and 5.3-5 the results of our calculation for a GaAs Schottky barrier FET with $A = 0.16\ \mu m$ and $N_D = 1.1 \times 10^{17}$ cm^{-3} are compared with experimental results.[4] The agreement is very good except in the regions of the current-voltage characteristics exhibiting hysteresis not observed experimentally (see the discussion above).

The characteristic switching time τ is defined as

$$\tau = \frac{Q}{I_{ch}}$$

where I_{ch} is the channel current and Q is the total positive charge under the gate. The dependences of τ and of cut-off frequency f_T on the drain voltage are shown in Fig. 5.3-6. The minimum value of τ and the maximum value of f_T correspond to the threshold drain voltage which is necessary for the stationary domain formation.



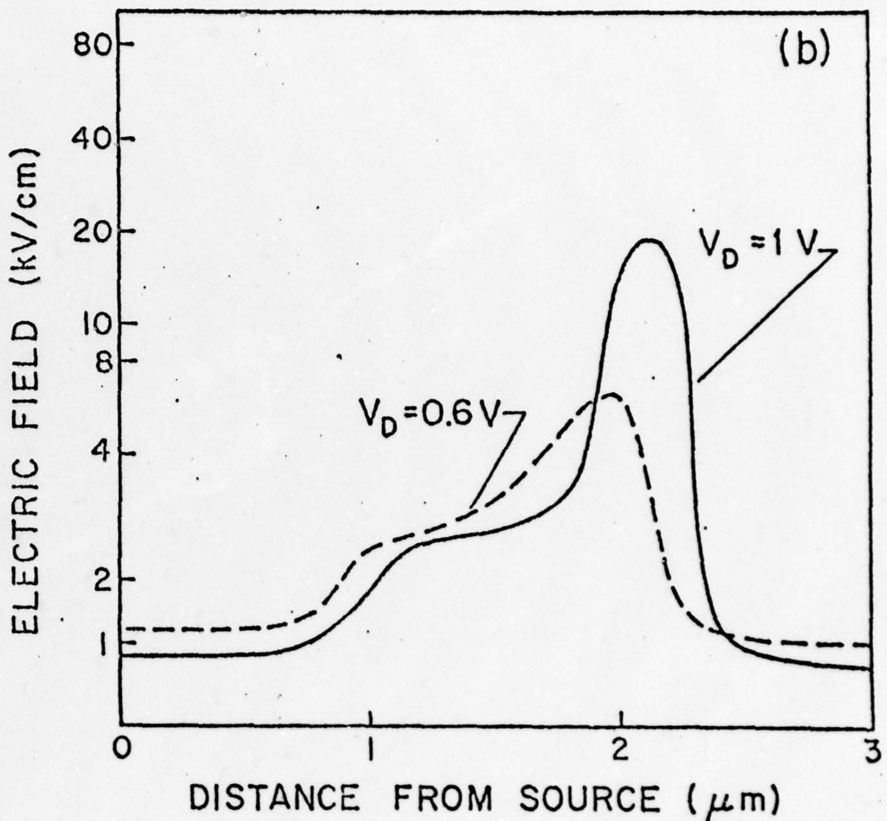
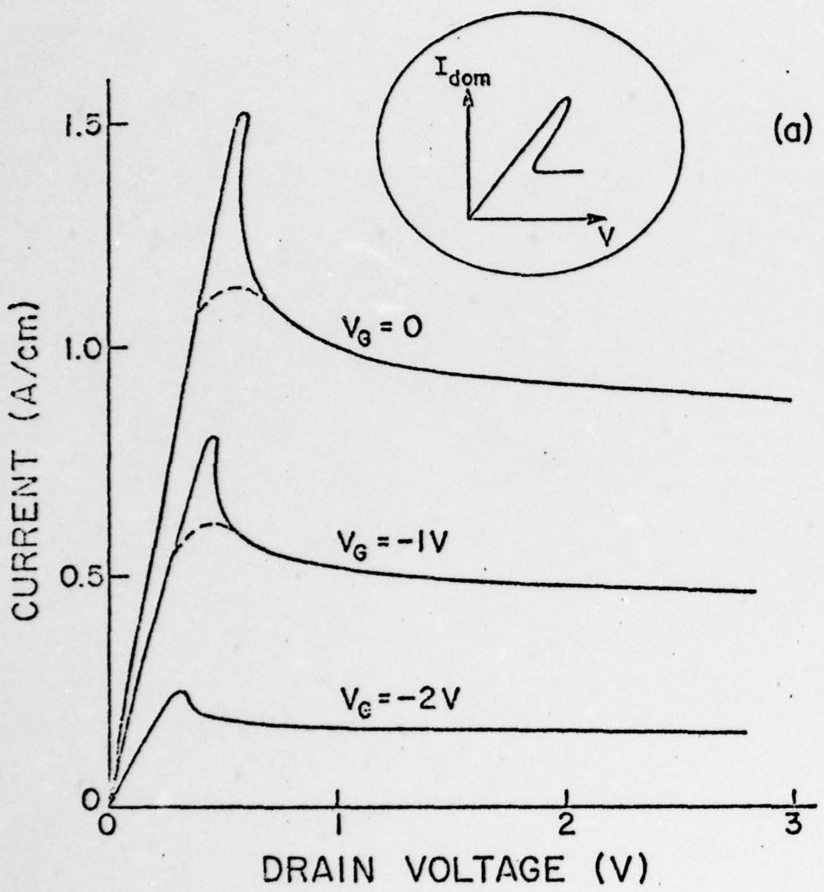


Fig. 5.3-2 - Electric Field Distribution Along Line O-A (See Fig. 5.3-1)



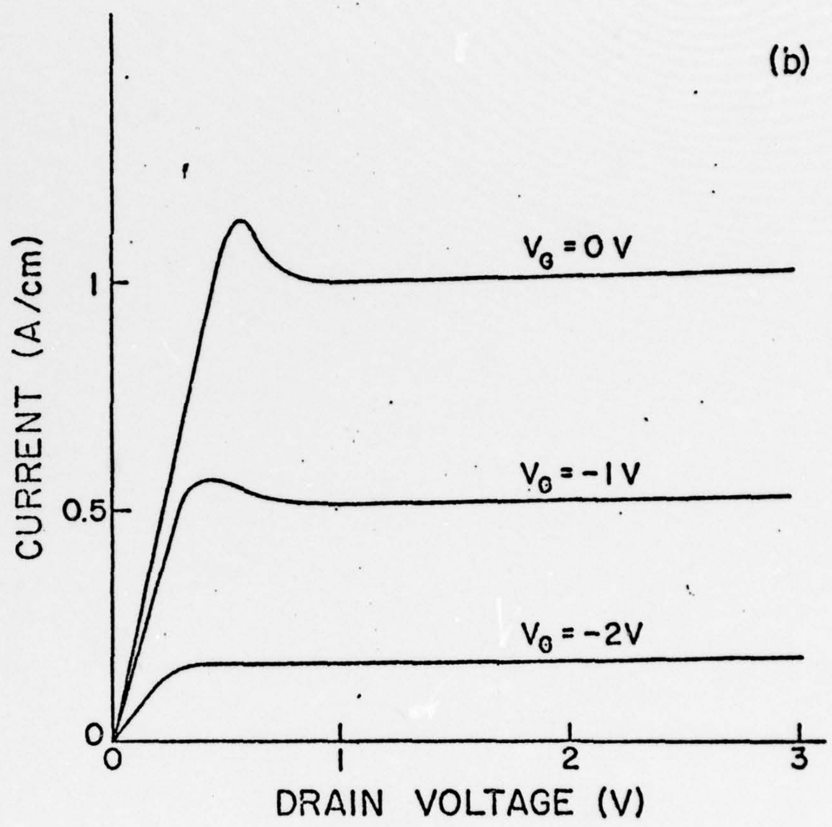


Fig. 5.3-3- Calculated Current-Voltage Characteristics of a GaAs FET

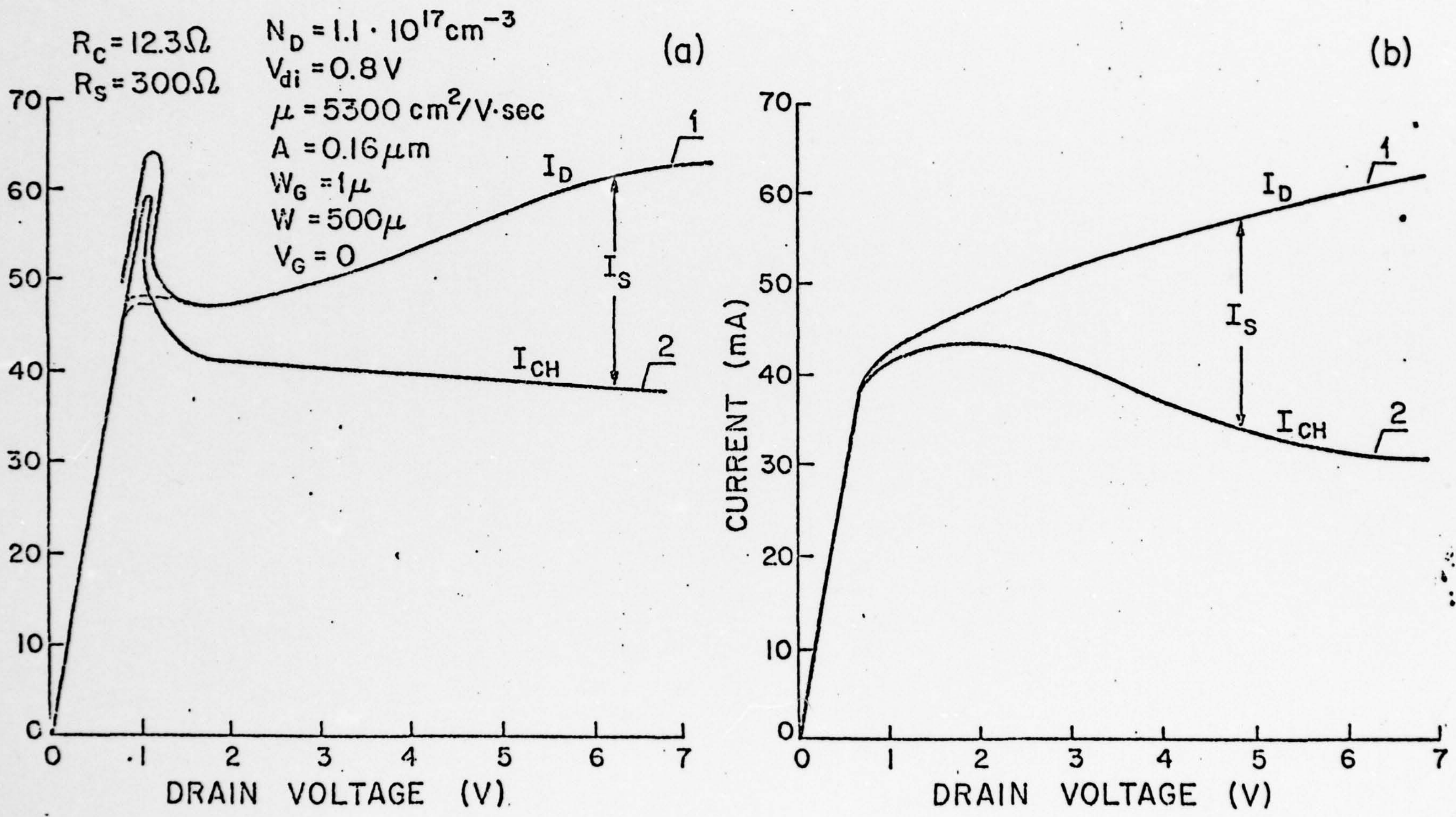


Fig. 5.3-4 - Current-Voltage Characteristics of the GaAs FET with d = 0.16

Fig. 5.3-5 - Transconductance (a) and Gate-to-Source Capacitance (b) versus Drain Voltage for the GaAs FET with A = 0.16μM.

Fig. 5.3-6- Current-Gain Cutoff Frequency f_T and Switching Time τ Versus Drain Voltage for the GaAs FET with A = 0.16 μM

The power-delay product for a 10 μm wide device is plotted in Fig. 5.3-7. A rather large contact resistance was simulated in the calculation. For a negligibly small contact resistance the value of the power-delay product at the drain voltage corresponding to the minimum switching time is only 16 fJ (i.e., more than in two times smaller).

The computed dependences of the switching time and the power delay product on the thickness of the active layer A are shown in Fig. 5.3-8. An interesting conclusion is that a slight increase of the device thickness (from 0.16 μm to 0.2 μm) leads to a considerably shorter switching time without an appreciable increase of the power-delay product.

In conclusion, a simple two-dimensional model of a GaAs FET has been proposed. The model takes into account diffusion processes and the Gunn domain formation. Electric field distributions under the gate, current-voltage characteristics, transconductance, gate-to-source capacitance, switching time and power-delay products have been calculated. The results agree well with the results of a two-dimensional computer analysis and with experimental data.[1]

In the next quarter work toward the development of analytical model to describe current-voltage characteristic, small signal parameters, switching times and power-delay products of a GaAs MESFET will be initiated.

POWER-DELAY PRODUCT (fJ)

400
300
200
100
90
80
70
60
50
40
30

1 2 3 4 5 6 7

DRAIN VOLTAGE (V)

Fig. 5.3-7 - Power-Delay Product Versus Drain Voltage for a GaAs FET with A = 0.16 μm, and 10 μm channel width.

Fig. 5.3-8- Switching Time (a) and Power-Delay Product (b) Versus Device Thickness; 1. Without a domain (lower drain voltage). 2. With a domain (higher drain voltage).

6.0 CONCLUSIONS

The successful fabrication of integrated circuit wafers indicates that the various process steps ranging from capping and implantation through second layer metalization are viable. The excellent results obtained for seven and nine stage ring oscillators demonstrate that the Schottky diode FET logic approach is capable of yielding the expected low propagation delays and low dynamic switching energies. Work in the near future will emphasize experiments to optimize and further develop various process steps. These experiments will be carried out both on integrated circuit test wafers and upon test wafers processed in parallel with the IC wafers. Emphasis will be placed upon correlation of both low frequency and high frequency performance data with the variation of selected process parameters. Acquisition and analysis of the large volume of static test data needed will be facilitated by the expected completion of an automatic data acquisition system for static device and circuit parameters.

7.0 REFERENCES

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