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SPECIFICATIONS FOR MICROCIRCUIT ELECTRICAL OVERSTRESS TOLERANCE--ETC(U)
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Final Technical Report
March 1978

SPECIFICATIONS FOR MICROCIRCUIT ELECTRICAL OVERSTRESS TOLERANCE

Robert J. Antinone

The BDM Corporation

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

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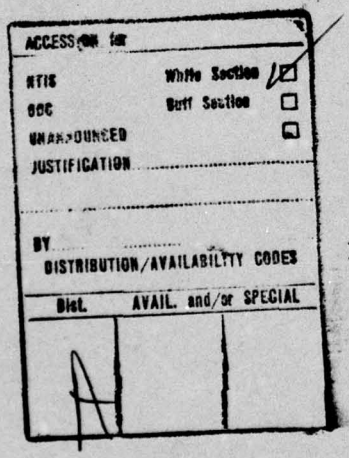

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The objective of this program is to develop an inexpensive electrical overstress quality assurance sample qualification test to be applied to all future Air Force microcircuit purchases. The maximum ratings presently specified refer only to dc limits and do not reflect the ability of a microcircuit to withstand short duration, high amplitude transients. The new electrical overstress tolerance specification has been developed to provide this information.

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During a literature search and survey, two types of transients were identified as being important in microcircuit applications. These are electrostatic discharge transients resulting from handling and system transients generated within a system or within the environment in which it operates. It was found that the static discharge transient could be simulated by a decaying expoential pulse with a short circuit time constant of 150 nanoseconds, delivered through a source impedance of 1500 ohms. Provisions were made for varying the peak amplitude of the pulse, but a charging voltage of 1000 volts was found to provide the best screening.

Further, it was found that the system transients could be simulated by a decaying expoential pulse with a short circuit time constant of 10 microseconds, delivered from a 100 ohm source impedance. Provision was made for varying peak voltage. Different technologies require different charging levels, but a level of 50 volts was found to separate microcircuit types into sensitive and non-sensitive categories.

A pulser having the capability of delivering either the static discharge or system transient simulation pulse was fabricated. Total parts costs were approximately $1,000. This pulser was used in subsequent procedure evaluation and sample qualification tests.

The proposed screening procedure was evaluated using a sample of 5 each of 10 microcircuit types representing a broad range of technologies. Each device was step stressed to failure. That is, each device was subjected to increasingly higher charging voltages until failure occurred. Failure was defined in terms of inability to pass the dc parameter and functional tests of the appropriate MIL-M-38510 slash sheet, or manufacturer's specification sheet. The results of the tests indicated that the procedure was basically sound. Thus, the proposed procedure was documented.

During the sample qualification testing, 15 each of 40 microcircuit types, representing all commonly used technologies, were step stressed to failure. Very few failures due to the electrostatic discharge transient were noted. Only MOS device types failed below the maximum charging voltage of 1000 volts, and only a small percentage of these devices failed. Several device types failed the system transient test at a level below 50 volts. These include high-speed Schottky TTL (54S), first generation I^2L, certain NMOS device types, certain voltage regulator sense inputs, and certain line receivers. As a result of the sample qualification tests, the proposed procedure was modified slightly and resubmitted.

The results of the program indicate that a viable electrical overstress tolerance specifications sample qualification test has been developed. The proposed specification should be implemented on a trial basis and further statistics should be gathered. Emerging technologies, such as advanced I^2L, should be characterized to evaluate their sensitivity to electrical overstress transients.

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EVALUATION

This report describes a preliminary lot qualification test for microcircuits which is directed at the problem of measuring and assuring a level of tolerance to system generated and electrostatic discharge types of electrical overstress. A method for determining the specification level for existing and new device types is also included which will allow the user to test to realistic overstress pulse conditions.

Using this test, it will be possible to identify those device types which are extremely susceptible to damage by electrical overstress. Users can then employ precautionary handling and design procedures to minimize exposure to overstress conditions.

This study has shown that a simple and inexpensive lot qualification test for electrical overstress tolerance is practical on a sampled basis. It is intended that this test method be submitted for tri-service coordination as an addition to Mil-Std-883, Methods 30XX and 5005. Hopefully, application of this test will contribute to a better understanding of the design and process factors which influence overstress tolerance and will encourage manufacturers to improve the capabilities of their product whenever possible.

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SECTION I
PROGRAM OVERVIEW

A. PROGRAM OBJECTIVE

The objective of this program is to develop an inexpensive electrical overstress quality assurance sample qualification test to be applied to all future Air Force microcircuit purchases. The characteristics of such a qualification test include:

(1) Practicality.
(2) Requirement for inexpensive equipment.
(3) Inexpensive application.
(4) Minimal impact on yield.
(5) Identification of devices which are highly sensitive to electrical overstress.

Clearly, a qualification test which is impractical or expensive is of little use since vendors will request, and normally be granted, variance from the specification. Likewise, a qualification test which does not identify sensitive devices is of little use. This report documents an effort to meet these sometimes conflicting goals in order to define a useful qualification test.

Five major tasks have been identified as steps in meeting the objectives of this program:

(1) Environment Definition
(2) Generator Design and Fabrication
(3) Procedure Evaluation
(4) Procedure Documentation
(5) Qualification Testing

This report summarizes the work in all five tasks.

The goal of the environment definition task was to identify the characteristics of those electrical transients which microcircuits may experience during handling, equipment buildup, and field use. Published literature and other available data sources such as in-house data were used to evaluate transient environments. The amplitude, shape, and duration of

those pulses required to simulate a practical worst-case transient overstress were determined along with a decision of which microcircuit pin combination must be tested.

The next task required the design and construction of an inexpensive pulser capable of delivering the transient overstress environments defined in the first task. The third task, procedure evaluation, involved using the pulser to conduct qualification testing on a sample of five units each of 10 device types representing the principal microcircuit technologies. The results of this experimental qualification testing were used to modify the qualification procedure. In the fourth task, the procedure was documented in a manner compatible with MIL-STD-833.

The final task involved applying the procedure to representative devices of the various microcircuit technologies. In all, 15 units of each of 40 device types were tested, most under several conditions.

B. PROGRAM ACCOMPLISHMENTS

1. Environment Definition

There are two basic types of electrical transients. These are static discharge transients and system transients. The static discharge transients result primarily from handling by personnel and are usually experienced during the handling and equipment buildup phases. The system transients result from sources within the system such as switching inductive loads, and from external sources, such as lightning.

Because static discharge transients are a serious problem for MOS device manufacturers, a great deal of previous work has been done to characterize these transients. The results of some of this work have been published in the technical literature (References 1 through 5), and this published information has been used as a basis for the static discharge specification developed by BDM. Figure 1 shows the equivalent circuit for the static discharge transient. The capacitor represents the body capacitance on which the static charge is being stored and the resistor represents the effective body resistance during discharge. Published reports show a wide variation in parameter values, but the following values appear to represent a practical worst case:

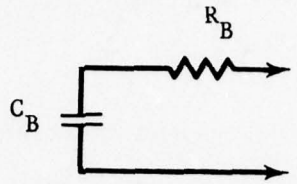


Figure 1. Static Discharge Equivalent Circuit

C_B = 100 pF
R_B = 1500 ohms
V_C = 1000 V

The capacitor voltage in particular may be varied to reflect differences in practical worst case conditions.

System transients are not so easily defined. Sources of these transients are many and varied and are usually system-specific. Because these transients do not lend themselves to easy investigation, there is very little published information available (References 6 and 10). The small amount of published information was supplemented by discussions with system builders. The approach taken by BDM has been to define a waveshape and duration which represent a practical worst case. Figure 2 shows the waveform which was chosen based on the results of the data search, discussions with experienced persons, and on engineering judgment. The Thevenin equivalent voltage amplitude for the transient varies for specific applications. The Thevenin equivalent source impedance may also vary with application, but the data search and engineering judgment indicate that a 100-ohm resistive source is a good representative value.

Past experience has indicated that microcircuits of various technologies and functions are most vulnerable to electrical transients on their inputs and least vulnerable to transients on their power and output terminals as shown in Figure 3. However, in system applications, power terminals are more likely to see transients than are input terminals because system transients are frequently propogated on power distribution lines. Output terminals also frequently see electrical transients. Pins for local use such as operational amplifier compensation pins generally are not subjected to transients and are not treated for system transients. However, these

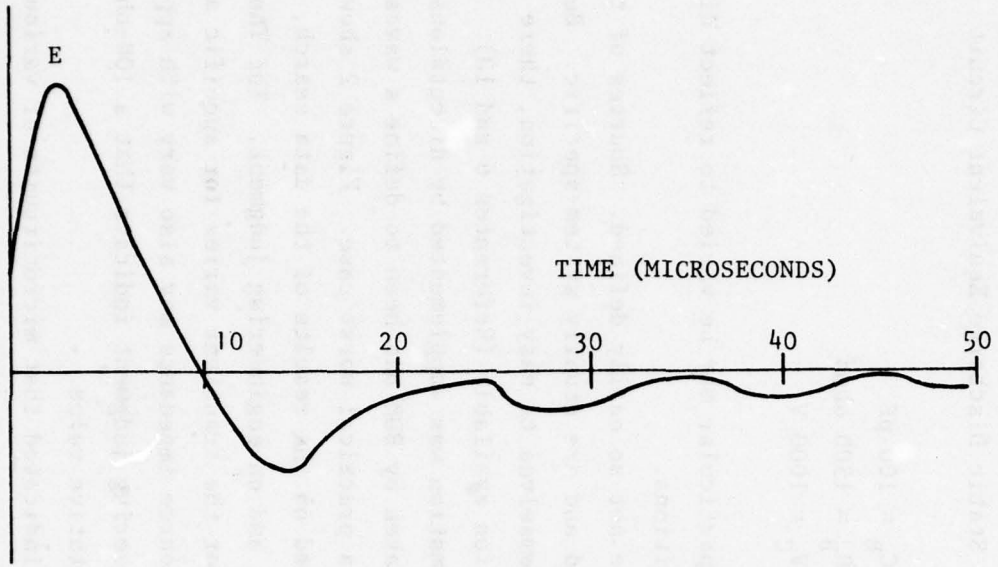


Figure 2. System Transient Waveform

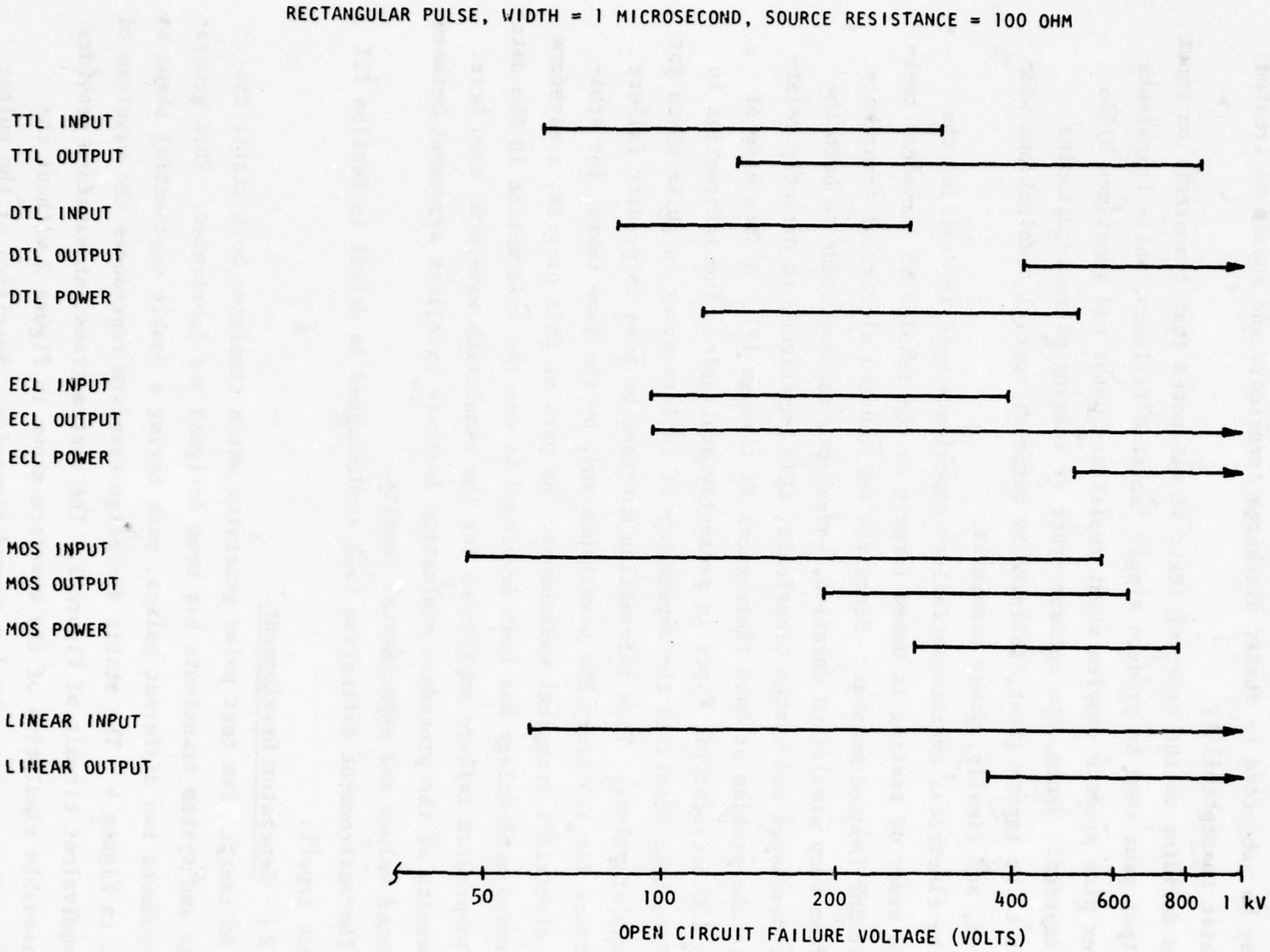


Figure 3. Thevenin Failure Voltage for Various Microcircuit Categories (Based on a Mixture of Types, Functions, Manufacturers, and Date Codes from Data in References 11, 12, and 13)

pins may be subjected to static discharge transients and should be treated for static susceptibility.

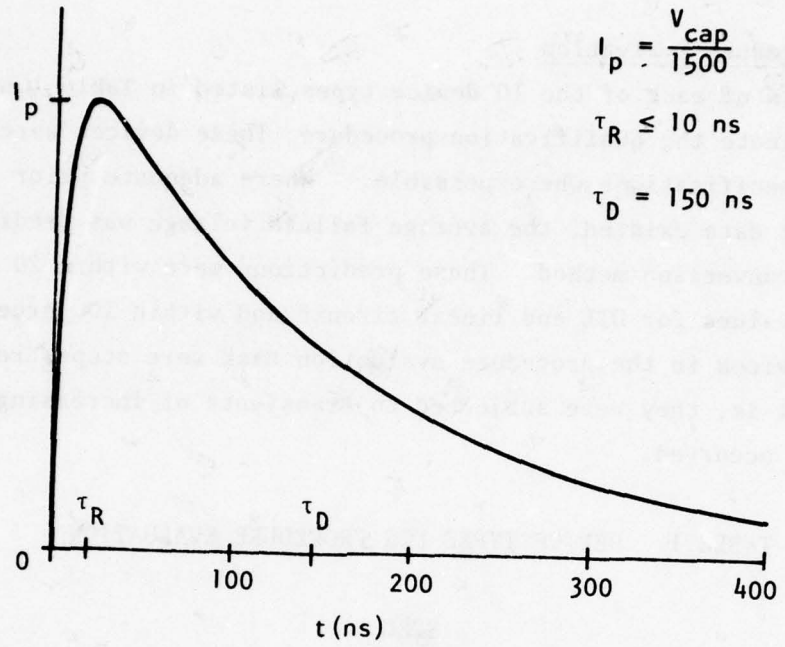
In deciding on the order of test, it was noted that transients on input and output pins tend to produce single isolated failures, while transients on power pins produce complex shunt resistance paths and sometimes blown metallization. Hence, the optimum order of testing microcircuit pins appears to be inputs first, followed by outputs, special combinations when required, and finally, power terminals.

The electrical overstress failure experience used in deriving the desired order of testing is based largely on the results of component testing for EMP-induced burnout. Since the EMP-induced electrical transients are often very similar in duration, waveshape, and amplitude to both the static discharge and system transients, this experience is directly relatable to the problem at hand (References 11 through 17). A data base of nearly 100 microcircuit types is presently available. The information in this data base describes the dependence of failure power on pulse width for rectangular pulses. This information may then be used to predict failure amplitudes for arbitrary EMP waveshapes and, by the same token, for arbitrary electrical transient waveshapes. As part of this program, a waveform conversion methodology has been developed to use the information in the data base to predict failure amplitudes for the simulation waveforms used here. The results of the procedure evaluation indicate excellent agreement between predicted values and experimental results.

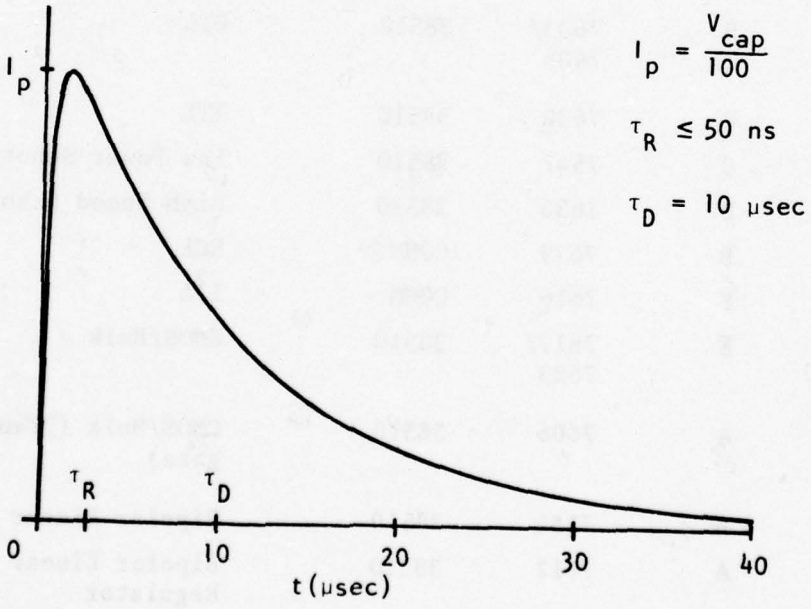
The environment definition task is discussed in detail in Section III of this report.

2. Generator Development

An inexpensive test pulse generator which simulates both static discharge and system transients has been designed and fabricated. This generator produces two different pulses, each having a double exponential shape as shown in Figure 4. The static discharge waveform reproduces the waveform of the equivalent circuit of Figure 1. The system transient waveform provides a reasonable simulation of the waveform shown in Figure 2 without the expense of generating complex damped sinusoids. Specifics of the pulser design are discussed in Appendix A of this report. It should be possible to build a copy of this generator for a materials cost of less than $1000.



(a) Static Discharge Short Circuit Waveform



(b) System Transient Short Circuit Current Waveform

Figure 4. Test Pulse Generator Waveforms

3. Procedure Evaluation

Five units of each of the 10 device types listed in Table 1 have been tested to evaluate the qualification procedure. These devices were purchased to military specifications where possible. Where adequate prior rectangular pulse test data existed, the average failure voltage was predicted using the waveform conversion method. These predictions were within 20 percent of the measured values for DTL and linear circuit and within 10 percent for TTL circuits. Devices in the procedure evaluation task were step-stressed to failure. That is, they were subjected to transients of increasing amplitude until failure occurred.

TABLE 1. DEVICE TYPES FOR PROCEDURE EVALUATION

TYPE	MFCR	DATE CODE	SPEC. TESTED TO	TECHNOLOGY
946	B	7633/ 7405	38510	DTL
5400	C	7630	38510	TTL
54LS00	C	7542	38510	Low Power Schottky TTL
54S00	D	7630	38510	High Speed Schottky TTL
10102	B	7639	COMM	ECL
401	F	7616	COMM	I^2L
4001	E	7617/ 7623	38510	CMOS/Bulk
4066	A	7606	38510	CMOS/Bulk (Transmission gate)
741	A	7534	38510	Bipolar Linear - Op Amp
723	A	7612	38510	Bipolar Linear - Voltage Regulator

Failure was defined in terms of inability to meet the electrical specifications of the appropriate MIL-M-38510 slash sheet or the manufacturer's electrical specifications.

The qualification procedure and the test equipment appear to be adequate for the devices tested. These tests served to establish starting failure levels for those technologies for which sufficient prior data were not available and to verify the predicted amplitudes where prior data exist. The results of these tests are documented in Section III of this report.

4. Procedure Documentation

The resulting procedure is documented in Section II of this report along with a rationale for its application and a discussion of a procedure for determining testing levels.

5. Qualification Testing

Fifteen units of each of the 40 device types listed in Table 2 were tested using the qualification procedure. Because of uncertainty in appropriate testing voltages for newer technologies, the devices were step-stressed to failure. Otherwise, all devices of a given type might have been destroyed without gaining any useful information. Failure statistics were obtained along with information regarding setup time and test time. Failure analysis was conducted on representative units of each type to determine failure paths and mechanisms. The results of this testing are documented in Section III of this report.

Figure 5 shows an overall flow diagram for the various tasks.

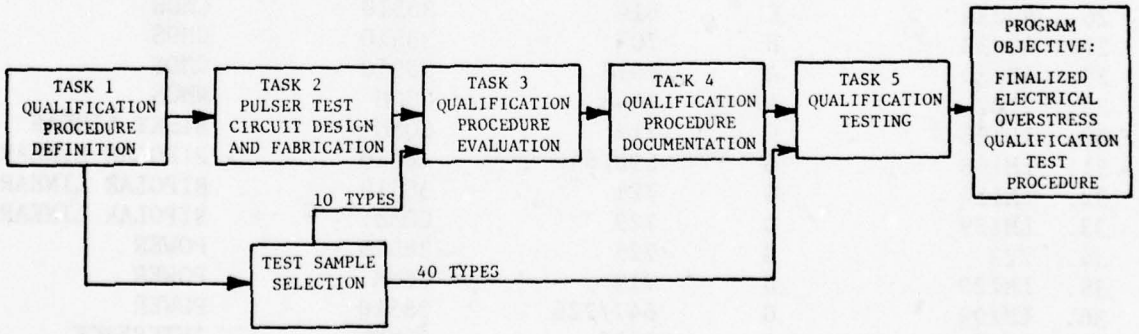


Figure 5. Task Flow for Electrical Overstress Specification Program

TABLE 2. DEVICE TYPES FOR QUALIFICATION TESTING

	TYPE	MFCR	DATE CODE	SPEC. TESTED TO	TECHNOLOGY
1.	946	A	7705	38510	DTL
2.	5400	A	7618	38510	TTL
3.	54153	G	340/344	38510	TTL
4.	5483	A	7604	38510	TTL
5.	54H00	A	7528/7709	38510	HTTL
6.	54H183	G	340/344	38510	HTTL
7.	54L74	G	352/724	38510	LTTL
8.	54S00	A	7650	38510	STTL
9.	54S138	A	7609	38510	STTL
10.	82S34	D	7339/7625	COMM	STTL
11.	82S67	D	7211	COMM	STTL
12.	7620	I	7712	COMM	STTL
13.	54LS00A	A	7735	38510	LSTTL
14.	54LS00B	G	716	38510	LSTTL
15.	54LS00C1	D	7720	38510	LSTTL
16.	54LS00C2	D	7720	38510	LSTTL
17.	54LS153	A	7609	38510	LSTTL
18.	54LS192	A	7547	38510	LSTTL
19.	10102	A	7718	COMM	ECL
20.	10130	A	7634	COMM	ECL
21.	XC401	F	7616	COMM	I2L
22.	XC402	F	7616	COMM	I2L
23.	XC404	F	7621	COMM	I2L
24.	4001	A	7630	38510	CMOS
25.	4066	A	7727	38510	CMOS
26.	4023A	E	614	38510	CMOS
27.	4023B	E	705	38510	CMOS
28.	4023D	A	7618	38510	CMOS
29.	2102	A	7645	COMM	NMOS
30.	LF156	G	719	COMM	BIFET LINEAR
31.	LM108	G	630/646	38510	BIPOLAR LINEAR
32.	LM124	G	721	38510	BIPOLAR LINEAR
33.	LM139	G	729	COMM.	BIPOLAR LINEAR
34.	723	G	725	38510	POWER
35.	LM120	G	719	COMM	POWER
36.	LM109	G	647/726	38510	POWER
37.	9615	A	7618	COMM	INTERFACE
38.	9616	A	7730	COMM	INTERFACE
39.	55107	A	7730	COMM	INTERFACE
40.	55109	A	7646	COMM	INTERFACE

SECTION II
PROPOSED SPECIFICATION

A. INTRODUCTION

A proposed overstress specification has been developed based on existing information and on a review of MIL-STD-883 and MIL-M-38510. The proposed overstress specification will require the addition of two new test procedures to the 3000 series test procedures plus additions to Method 5005, Qualification and Quality Conformance Procedures. In addition, the test levels must be added to the appropriate MIL-M-38510 slash sheet. The remainder of this section presents the proposed overstress specification, a method for establishing test levels, and the impact of applying the specification.

B. ELECTRICAL OVERSTRESS TOLERANCE TEST PROCEDURE FOR MICROCIRCUITS, METHOD 30XX

1. PURPOSE. This method establishes the means for assuring device performance to the limits specified in the applicable procurement document in regard to electrical overstress due to static discharge and system generated transients. This method applies to digital microcircuit devices such as TTL, DTL, ECL, MOS, and I^2L and to Linear Microcircuit types using bipolar and bifet technology.

2. APPARATUS. The apparatus used for this electrical overstress test shall include a suitable source generator (see 2.1) and suitable instrumentation for determining device response (see 2.2) following the overstress test.

2.1 Source Generator. Two source generators are required and depend on the overstress test to be performed.

2.1.1 Static Discharge Test. The source generator for static discharge tests shall be configured and use the component values shown in Figure 6. This generator shall produce the short circuit current waveform shown in Figure 7. The capacitor voltage shall be as specified in the applicable procurement document.

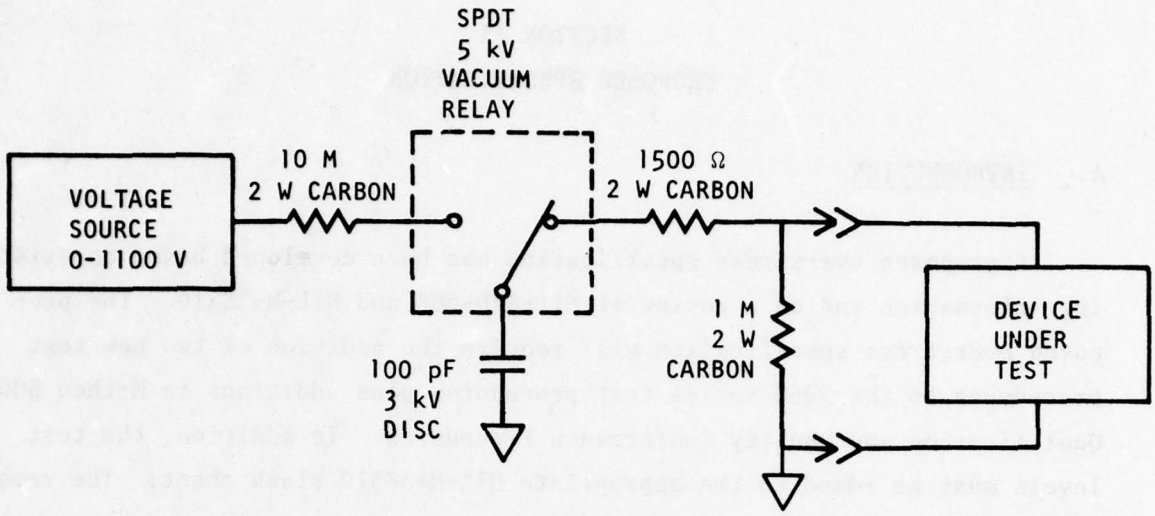


Figure 6. Static Discharge Source Generator

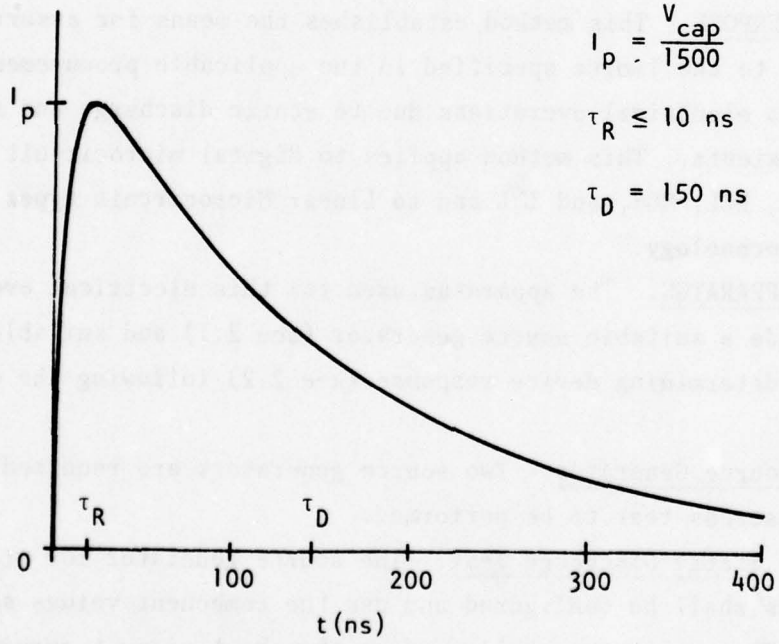


Figure 7. Static Discharge Short Circuit Current Waveform

2.1.2 System Transient Test. The source generator for the system transient test shall be configured and use the component values shown in Figure 8. This generator shall produce the short circuit current waveform shown in Figure 9. The capacitor voltage shall be as specified in the applicable procurement document.

2.2 Response Instrumentation. The instrumentation for determining posttest microcircuit response shall be capable of measuring dc parameters as per the applicable procurement document.

3. PROCEDURE. The microcircuits shall be subjected to a pretest characterization consisting of the dc electrical parameters. The microcircuits shall then be subjected to the pulse sequence given in 3.1 for static discharge tests or in 3.2 for system transient tests as specified in the applicable procurement document.

3.1 Static Discharge Tests. The microcircuits shall be subjected, in order, to the following pulse sequences, unless otherwise specified in the applicable procurement document:

3.1.1 Pin Combinations for Digital Microcircuits

(1) INPUT (+) to COMMON

(2) OUTPUT (-) to COMMON

(3) INPUT (+) to OUTPUT

(4) V+ (-) to COMMON

3.1.2 Pin Combinations for Linear Microcircuits

(1) INPUT (+) to COMMON

(2) INPUT TO INPUT

(3) OUTPUT (-) to COMMON

(4) V + (-) to COMMON

3.2 System Transient Tests. The microcircuits shall be subjected, in order, to the following pulse sequences, unless otherwise specified in the applicable procurement document:

3.2.1 Pin Combinations for Digital Microcircuits

(1) INPUT (+) to COMMON

(2) OUTPUT (-) to COMMON

(3) V + (-) to COMMON

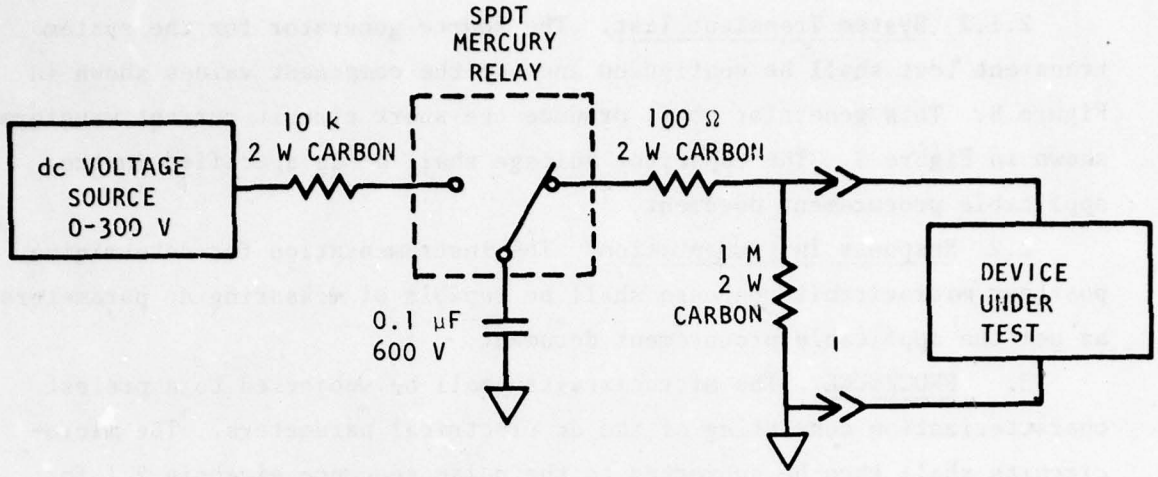


Figure 8. System Transient Source Generator

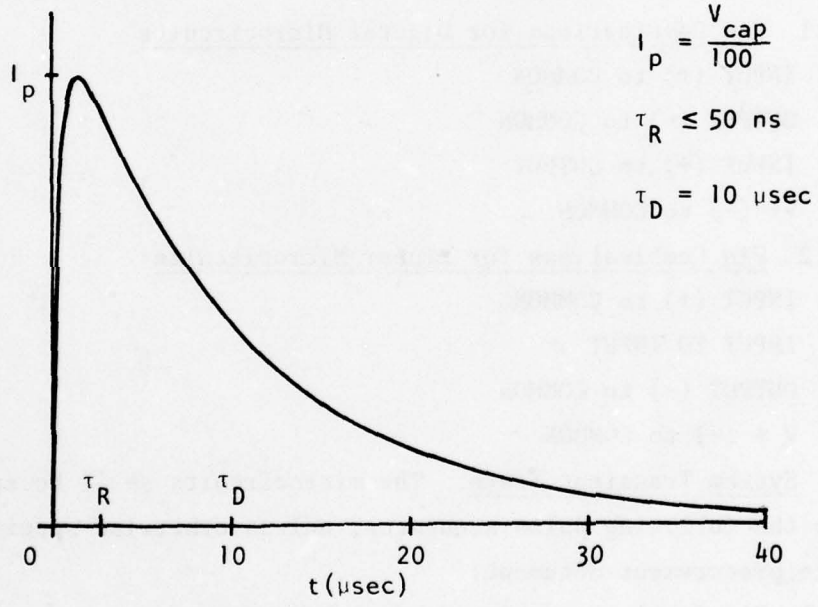


Figure 9. System Transient Short Circuit Waveform

3.2.2 Pin Combinations for Linear Microcircuits

(1) INPUT (+) to COMMON

(2) INPUT to INPUT

(3) OUTPUT (-) to COMMON

(4) V + (-) to COMMON

4. Summary. The following details shall be specified in the applicable procurement document:

(1) Static Discharge and/or System Transient Tests

(2) Test Amplitudes

(3) Additional Test Pin Combinations and/or Revised Polarities.

C. ESTABLISHING ELECTRICAL OVERSTRESS TESTING LEVELS AND PIN COMBINATIONS, METHOD 30YY

1. Purpose. This method establishes the means for determining the appropriate electrical overstress tolerance testing levels and pin combinations for microcircuits. It is to be used for determing test conditions for use with method 30XX. This method may be used for a microcircuit technology for which testing conditions have not been previously determined, or for a particular microcircuit type which does not fit a category having established testing conditions.

2. Apparatus. The appartus used for establishing electrical overstress testing levels and pin combinations shall include a suitable source generator (Section 2.1) and suitable instrumentation for determining device response (Section 2.2) following the overstress test.

2.1 Source Generator. Two source generators are required.

2.1.1 Static Discharge Test. The source generator for static discharge tests shall be configured and use the component values shown in Figure 6. This generator shall produce the short circuit current waveform shown in Figure 7. The capacitor charging voltage shall be varied to determine the failure level.

2.1.2 System Transient Tests. The source generator for the system transient tests shall be configured and use the component values shown in Figure 8. This generator shall produce the short circuit current waveform

shown in Figure 9. The capacitor charging voltage shall be varied to determine the failure level.

2.2 Response Instrumentation. The instrumentation for determining posttest microcircuit response shall be capable of measuring dc parameters applicable to the microcircuit under test.

3. Procedure. There are three steps to determining testing levels and pin combinations. First, probable failure paths must be determined from the microcircuit schematic. Next, a small sample must be tested to failure to determine worst case failure paths and gather failure statistics. Finally, the data gathered must be evaluated statistically to establish the testing level.

3.1 Determining Probable Failure Paths

The manufacturer's equivalent circuit schematic shall be used to determine probable failure paths. Since these equivalent circuit schematics do not always reflect the true construction of the microcircuit, the schematic will be supplemented with visual inspection of the microcircuit, where practical.

The following guidelines are provided for determining probable failure paths for electrostatic discharge transients:

(1) Unprotected MOS gates.

(2) Unprotected CMOS transmission gate inputs.

(3) Poorly protected MOS gates.

(4) Pinned-out MOS capacitors in Linear Microcircuits.

(5) Thin oxide underpasses (when known to exist).

Testing a path for static sensitivity should generally be done in both polarities. Poor protection networks will generally fail when protection diodes are reverse biased. Good protection networks will generally fail when protection diodes are forward biased.

The following guidelines are provided for determining probable failure paths for system transients.

(1) Inputs are usually the most sensitive.

(2) Choose a pin with the smallest fan-in; that is, with the smallest number of shunting paths.

(3) Choose the lowest impedance path with the smallest number of junctions to breakdown.

(4) Choose a polarity which causes the emitter-base junction of a small transistor to be reverse biased or which causes a small diode to be reverse biased.

Where a microcircuit has multiple, identical inputs or outputs only one such input or output need be tested. All reasonable failure paths identified shall be tested in order of suspected sensitivity. When a level is being established for a new technology, several representative device types shall be considered. Large scale devices should be included, where applicable.

3.2 Step-Stressing Procedure. Failure statistics shall be determined by step-stressing for both the static discharge and system transients. The test sample shall be subjected to the starting transient level as a group. They shall then be tested for proper electrical functioning. The transient level shall be incremented and the electrical functioning again tested. When a particular device fails to pass the electrical function tests it shall be removed from the sample and its failure level shall be recorded. The remaining devices in the test sample shall then be subjected to the next increment in transient level. The step-stressing shall continue until all devices in the test sample have failed. The test for proper electrical functioning shall be the dc parameter tests from the appropriate MIL-M-38510 slash sheet.

The initial testing level for the static discharge charge transients shall be determined by selecting one device from the test sample. It shall be step-stressed in the assumed weakest configuration starting at 200 volts and incrementing in 25 volt steps until failure occurs. The failure level shall be recorded and the starting transient level for the subsequent tests shall be set at 250 volts lower than the failure level of the first device.

The initial testing level for the system transient shall be determined by selecting one device from the test sample. This device shall be step-stressed in the assumed weakest configuration starting at 25 volts and incrementing in 2.5 volt steps until failure occurs. The failure level shall be recorded and the starting transient level for subsequent tests shall be set at 25 volts lower than the failure level of the first device.

Approximately 10 devices shall be tested in the assumed weakest configuration. An additional sample of 5 devices shall be tested at the

highest failure level observed in all other potential failure configurations. If any failures occur, an addition sample of 10 devices shall be tested in that configuration. The true weakest configuration shall be determined from these data. In cases of substantial overlap, more than one weak configuration may be found.

An additional sample of 15 devices shall be step-stressed in the true weakest configuration to give a total sample of 25 devices. A sample size of 25 is adequate for determining testing levels if the data spread between highest and lowest failure is no greater than a factor of two. Most microcircuits meet this criterion.

3.3 Statistical Interpretation. The failure levels from the sample of 25 devices in the worst case configuration shall be plotted in the form of a histogram. The failures shall be assigned to a bin beginning at the highest no-fail voltage and ending at the failure voltage. The mean and standard deviation of the sample shall be calculated from

$$\bar{V} = \frac{1}{N} \sum_{i=1}^{N} V_i$$

and

$$S = \sqrt{\frac{\sum_{i=1}^{N} (V_i - \bar{V})^2}{N-1}}$$

where

$\bar{V}$ = sample mean

S = sample standard deviation

N = sample size (usually 25)

V_i = highest no-fail voltage for the ith device.

The 90 percent confidence interval for the sample mean and standard deviation shall then be computed and the minimum estimate of the mean and maximum estimate of the standard deviation shall be determined from

$$\mu_{min} = \bar{V} + \frac{S}{\sqrt{N-1}} t_{N-1,.95}$$

and

$$\sigma_{max} = S \sqrt{\frac{N}{\chi^2_{N-1,.1}}}$$

where

μ_{min} = minimum estimate of mean

σ_{max} = maximum estimate of standard deviation

$t_{N-1,.95}$ = 95 percentile point of Student's t Distribution with N-1 degrees of freedom

= 1.71 for N = 25

$\chi^2_{N-1,.1}$ = 10 percentile point of chi-square Distribution with N-1 degrees of freedom

= 15.7 for N = 25

The testing level shall be determined from

$$V_T = \mu_{min} - 2 \sigma_{max}$$

For an assumed normal distribution having parameters μ_{min} and σ_{max}, only two percent of the devices would have a failure level less than V_T as shown in Figure 10.

The LTPD allowances for classes A, B, and C are set at 5, 10, and 15 respectively. Figure 11 shows schematically three possible minimum distributions which correspond to these LTPD's.

D. ADDITION TO METHOD 5005

A new subgroup, tentatively subgroup 7, will be added to Table IIa. "Group B Tests for Class A Devices," of Method 5005, "Qualification and Quality Conformance Procedures." The subgroup to be added is presented in Table 3. A new subgroup, tentatively subgroup 4, will be added to Table IIb, "Group B Tests for Classes B and C," of Method 5005. The subgroup to be added is presented in Table 4.

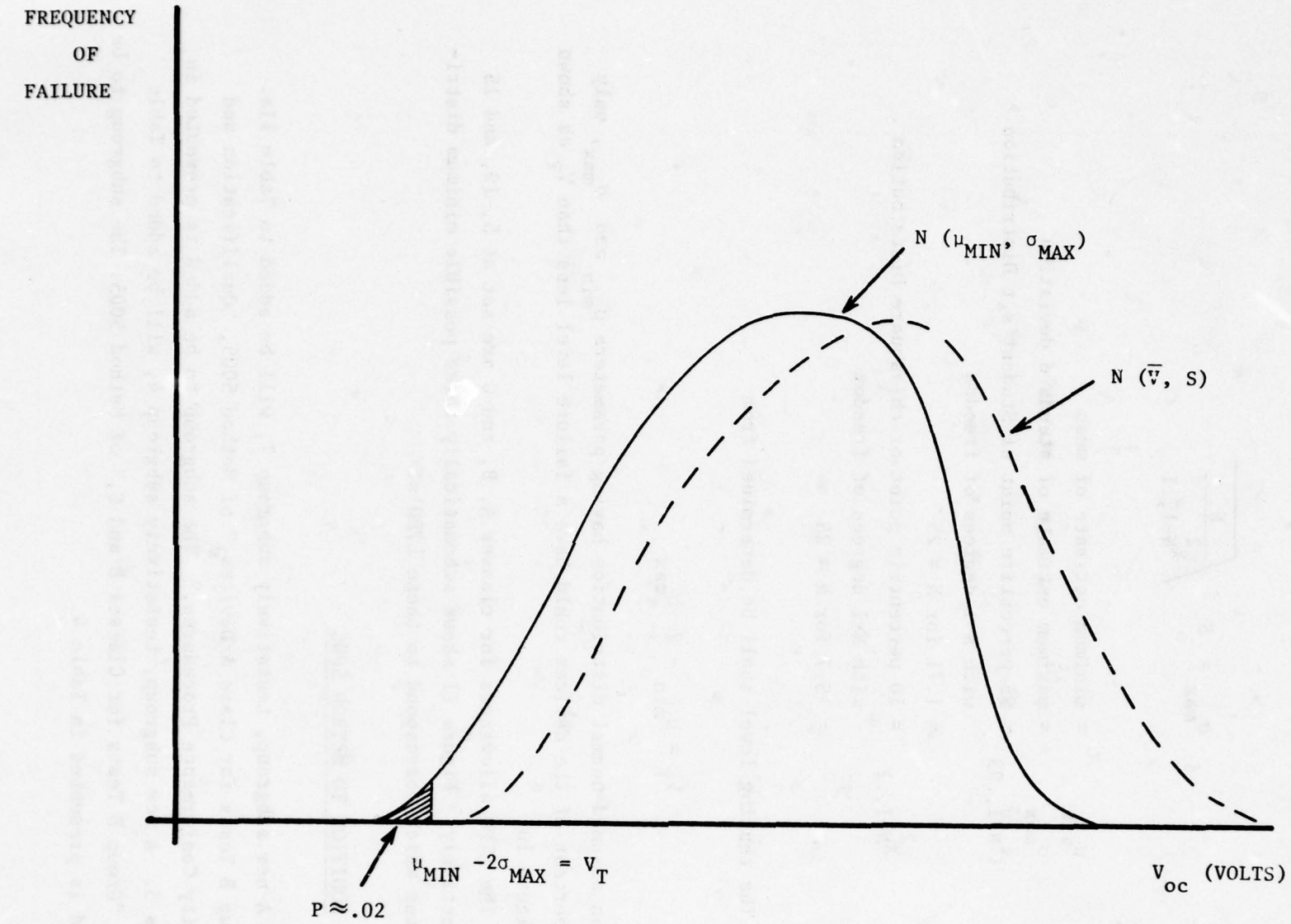


Figure 10. Setting Testing Level

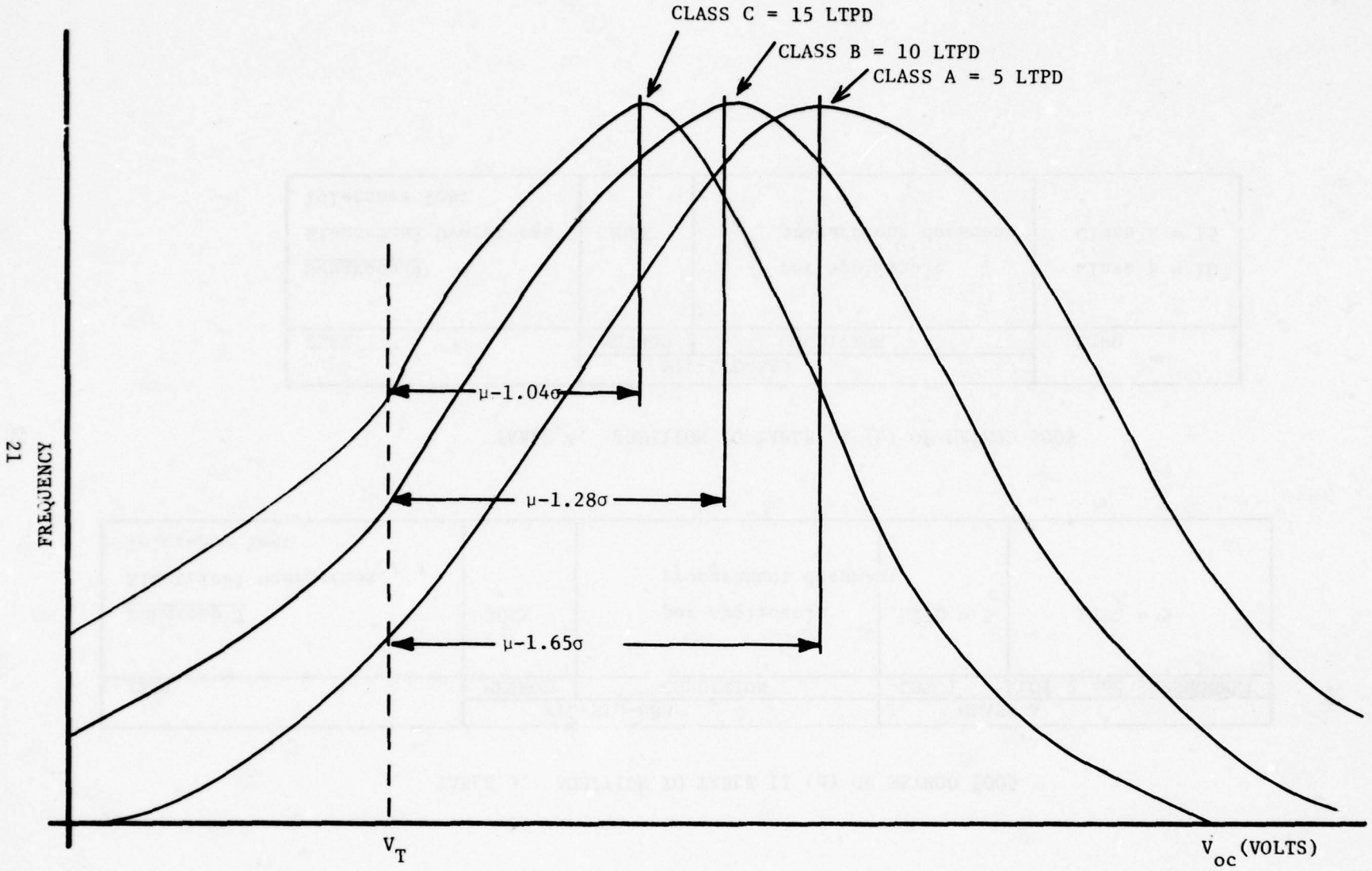


Figure 11. Worst Case Acceptable Distribution for Classes A, B, and C

TABLE 3. ADDITION TO TABLE II (a) OF METHOD 5005

TEST	MIL-STD-883		CLASS A	
	METHOD	CONDITION	LOT 1	LOT 2 and SUBSEQUENT
Subgroup 7 Electrical Overstress Tolerance Test	30XX	per applicable procurement document	LTPD = 5	LTPD = 5

TABLE 4. ADDITION TO TABLE II (b) OF METHOD 5005

TEST	MIL-STD-883		LTPD
	METHOD	CONDITION	
Subgroup 4 Electrical Overstress Tolerance Test	30XX	per applicable procurement document	Class B = 10 Class C = 15

E. RATIONALE FOR THE SPECIFICATION

The specification assumes that there are two types of transients which might damage microcircuits - electrostatic discharge transients and system transients. Certain microcircuit types, usually those employing MOS technology, are known to be susceptible to damage from electrostatic discharge during assembly and repair. These devices are generally not affected by static during actual equipment operation. All microcircuits are potentially susceptible to damage from transients generated within a system or by the environment within which the system operates. Possible sources of such system transients include spikes due to switching of inductive loads, lightning induced transients, and even transients generated by automatic test equipment. These two types of transients are fundamentally different in nature, and it is necessary to use two different pulses to simulate them.

As discussed in more detail in Section III of this report, there are a number of different equivalent circuits currently being used to simulate electrostatic discharge transients. Most of these use a capacitor discharged through a resistor, but the values of capacitance, resistance and charging voltage vary widely. Some of the studies discussed in Section III have found static buildups well in excess of 10,000 volts. It is clear that MOS devices are not going to withstand such voltages, so a more practical approach is needed.

During the period of this study, BDM participated in two electrostatic discharge seminars sponsored by the Reliability Analysis Center where people from industry and government detailed their experience with electrostatic discharge. A speaker at the 1977 seminar (Ebel of Singer) reported that when reasonable precautions to prevent static buildup are used in conjunction with a screening technique, a 100-pf capacitor charged to 1000 volts and discharged through a 1500-ohm resistor, losses of microcircuits due to electrostatic discharge can be held to a minimum. Microcircuits which fail this specification require very careful handling.

Unfortunately, it is not possible to analytically derive the optimum equivalent circuit and charging voltage to screen for electrostatic discharge sensitivity. Therefore, it is necessary to rely on experience. Based on experience, Ebel's circuit was adopted. This circuit was also

originally used in the MIL-M-38510/50B ZAP test. Some might argue that a charging voltage higher than 1000V is required, since static buildups to 10,000 volts or more are not uncommon. However, device manufacturers would be forced to design massive protection networks which would seriously degrade performance in order to meet a much higher specification. This would probably be unacceptable to users as well as to manufacturers. On the other hand, some might argue for a much lower specification. In fact the MIL-M-38510/50B ZAP test level has been lowered to 400 volts. Experience indicates that devices which fail to meet the 1000-volt specification require additional special precautions for handling, which is unacceptable to users.

A similar approach based on engineering judgment has been used to define the system transient simulation pulse. As discussed in Section III of this report, the duration and amplitudes of system transients span many decades. It is possible to use a multiple pulse width testing approach to determine a damage constant as developed by BDM for use on EMP damage programs (see References 11 through 13). However, it was felt that this approach is too complex and costly to serve as a practical microcircuit screen. Instead, a simple decaying exponential pulse with a 10-μsec time constant was chosen as a compromise pulse to determine relative sensitivity of devices. A source impedance of 100 ohms has been chosen as a representative value.

While this screen does not give as much information as a multiple pulse width damage constant test, it does indicate the relative sensitivity of microcircuits to typical system transients. Furthermore, it does not require monitoring voltage and current waveforms, nor does it require complex data reduction. This screen gives substantially more information than the present specifications which are based only on steady state power limitations.

Past experience indicates that for pulse widths of 100 nanoseconds to 100 microseconds, most microcircuit failure powers can be modeled by

$$P_F = At^{-B}$$

Normally, the value of the exponent, B, does not differ greatly from the classical value of 0.5 for the Wunsch damage model. Thus, it is not unreasonable to choose a single pulse width to determine relative sensitivity. A waveform conversion procedure has been developed to predict failure voltages using the system transient simulation pulse from data obtained from EMP test programs.

The appropriate charging voltage depends on the type of microcircuit being tested. However, it has been found that a voltage of 50 volts generally separates sensitive devices from the nonsensitive ones. If the median failure voltage is less than about 50 volts, the devices are considered particularly susceptible to system transient induced damage.

The two simulation pulses described here, static and system, represent reasonable simulations of handling, buildup, and field use transients. They are simple to apply and interpret. The system transient pulse should be applied to all microcircuits. The static transient pulse should be applied to those microcircuits known to be static sensitive and to those which are sensitive to the system transient pulse (i.e., whose median failure level is less than 50 volts).

The static pulse, when applied at the 1000-volt level, and the system transient pulse, when applied at the 50-volt level, can, as a minimum, separate microcircuits into groups which are sensitive and nonsensitive.

F. IMPACT OF THE SPECIFICATION

The goal of the specification is to identify those microcircuit technologies or device types which are especially sensitive to electrostatic discharge or system transients and to identify production lots of microcircuits which are appreciably more sensitive than normal for that device type. The specification will provide incentive to the manufacturer to decrease the sensitivity of his parts wherever possible.

The cost of applying the specification should be minimal. The environment simulator for both pulses can be built for a materials cost of around $1000. With a simple universal test fixture, included in the cost, this simulator can be used for virtually all microcircuits. It is assumed that

adequate test equipment and test programs to measure the dc parameters and function of the microcircuit will already exist.

The job of initially establishing the weakest configurations and screening levels can be accomplished in 2 to 4 hours with a sample of about 25 devices. Actual pulsing of devices can be accomplished at the rate of about five devices per minute. Of course, the amount of post pulse testing time will depend on the equipment and program used. Changeover from one pulsing configuration to another can usually be done in less than 2 minutes.

The impact of the pulse test on the reliability of the tested devices is not presently known. Therefore, it would be best to limit the test to a lot sample qualification until the reliability impacts can be assessed.

SECTION III
PROGRAM RESULTS

A. QUALIFICATION PROCEDURE DEFINITION

A literature search and survey was conducted to identify and characterize the types of electrical overstress environments that microcircuits are likely to encounter. Two types of overstress conditions likely to produce failure have been identified. The first is static discharge which occurs primarily when microcircuits are being handled during equipment manufacture or repair. The second type of overstress, referred to as system transient, occurs during equipment operation and is due to transients generated within the equipment. For example, the deenergizing of a coil may produce a power-line transient which is several hundred volts in amplitude. System transients may also result from the environment within which the equipment is operated. Lightning is a prime example of this.

1. Electrostatic Discharge Transients

Electrostatic discharge transients are characterized by short duration high amplitude spikes. The source of these transients is usually static buildup on persons and machinery handling the parts. Because the phenomenon is quite common and has such a serious impact on the yield of MOS devices, it has been studied in-depth previously. Appendix C lists the references used to characterize static discharge transients.

Most of the studies indicate that the equivalent circuit shown in Figure 1 models the phenomenon very well. The capacitance C_B represents the body capacitance on which the charge is stored, while resistor R_B represents the effective body resistance during discharge. Different experimenters have measured different values for these parameters as shown in Table 5. Note that capacitance values range from 60 to 218 pF with the most common value being 100 pF. The resistance varies over three orders of magnitude with a value of 1.5 kilohms being representative.

At present, the "ZAP" test of MIL-M-38510/50B is using values of 100 pF and 1.5 kilohms. Since these values appear to be representative of a number of studies and since they have been proven to provide a practical screen in actual applications, they were also chosen for the static discharge test

TABLE 5. BODY MODEL VALUES

DATA SOURCE	C_B(pF)	R_B(OHMS)
RCA (REF 5)	100	560
BENDIX (KIRK) (Ref 5)	218	100
BENDIX (REF 5)	132-190	87-190
MARTIN-MARIETTA (REF 5)	150	200K
WESTERN ELECTRIC (REF 2)	60	1K-100K
M38510/50B(ZAP)	100	1.5K
FAIRCHILD (LENZLINGER)(REF 1)	100	1.5K
SINGER (EBEL) (REF 5)	100	1.5K

under this program. These values give a short circuit discharge time constant of 150 nanoseconds.

With this model for the static discharge transient, the peak voltage and maximum energy available in the pulse depend on the voltage on the capacitor. Electrostatic voltages have been measured for several conditions as shown in Table 6. Obviously, no microcircuit could be expected to survive a 39-kV transient. Fortunately, the voltage value for a person working at a bench is the most likely value to be seen. This still gives a range of from 500 to 3000 volts. At present, the ZAP test of MIL-M-38510/50B uses a value of 400 volts. The previously used value of 1000 volts has been chosen for the static discharge test under this program.

The capacitor voltage in the MIL-M-38510/50B ZAP test was lowered to 400 volts since some CMOS devices are apparently unable to withstand a higher voltage. None of the devices tested in this program has failed at a capacitor voltage below 950 volts. Experience by Ebel at Singer cited in Section II indicates that devices which fail well below 1000 volts should be considered extremely sensitive.

With this static discharge model, variations in specification level can be accomplished by simply varying the capacitor charge voltage. No component substitution will be required. Thus, it will be easy to accommodate various levels of reliability for various component types within one experimental setup.

2. System Transients

The literature search and survey have provided only limited information on system transients (References 6 through 10). Three general types of transients have been identified. The first of these is due to insufficient regulation within a system which allows a signal to modulate a power supply line. These types of transients are normally on the order of 1 or 2 volts maximum and are not a problem in terms of overstress failure.

The second of these transient types is due to switching inductive loads within the system which produces large amplitude spikes. These spikes have an exponential decay and may have ringing associated with them. The amplitude of these spikes may range from a few volts to hundreds of volts and may have durations ranging from nanoseconds to milliseconds. The equivalent source impedance for these transients may range from 1 or 2 ohms to

TABLE 6. REPRESENTATIVE VALUES OF ELECTROSTATIC VOLTAGES (AFTER SPEAKMAN[2])

	MOST COMMON READING	HIGHEST READING
PERSON WALKING ACROSS CARPET	12,000	39,000
PERSON WALKING ACROSS VINYL TILE FLOOR	4,000	13,000
PERSON WORKING AT BENCH	500	3,000
16 LEAD DIP'S IN PLASTIC BOX	3,500	12,000
16 LEAD DIP'S IN PLASTIC SHIPPING TUBE	500	3,000

ALL READINGS WERE RECORDED DURING FEBRUARY AND MARCH WITH AN AMBIENT RELATIVE HUMIDITY RANGING FROM 15 TO 36 PERCENT.

several thousand ohms, depending on the frequency content of the spike, and on system parameters such as cable length, cable inductance and capacitance, proximity to other cables, and discrete circuit element impedances. A relay coil with suppression may still generate a large amplitude, short duration transient during the time it takes the suppression device to respond.

The third transient type is due to coupling of a high energy external signal into the system from sources such as lightning, a nearby radar transmitter, or EMP from a nuclear weapon. These sources are capable of producing large amplitude signals within a system over a very wide range of frequencies. The internal signals are normally assumed to be a damped sine wave. The frequency and decay times of these transients may vary from 10 kHz to 100 MHz or more and from tens of nanoseconds to tens of milliseconds. As with the internally generated transients, the equivalent source impedance may vary over a wide range.

Since field use transients vary over such a wide range of amplitudes, decay times, and source impedances, and since the failure thresholds of microcircuits are pulse width dependent, it is not possible to select one or two pulses that will adequately simulate all transient environments. It is possible, however, to select a pulse within the range of the anticipated environment that can be used to separate microcircuits within a family (TTL, DTL, etc.) or type (5400, 709, etc.) into classes that are relatively sensitive or non-sensitive to electrical overstress damage.

Figure 2 shows the transient waveform specified by MIL-STD-462, Method CS06. Both discussions with engineers and the limited field use transient data available suggest that this waveform is reasonably representative of system transients in shape and duration. Hence, this waveform has been selected as representative of system transients. Variations in specification level can be achieved by varying the amplitude, while holding the waveshape and duration constant.

After surveying the literature and information available, a source impedance value of 100 ohms was selected. This represents a compromise over many possible impedances, but it appears to be most representative of typical transients. Nominal values of from 50 to 200 ohms were quoted with 100 ohms being the most frequent.

3. Selecting Pin Combinations

It would be time consuming and expensive to test all possible pin combinations on a microcircuit, especially on an LSI microcircuit. The number of pin combinations requiring testing can be greatly reduced by considering only those which have the greatest susceptibility to overstress and those which are most likely to experience overstress.

Both a great deal of past experience and a number of published reports (References 11 through 15) were used in determining pin combinations to be tested. Input terminals pulsed with respect to common are generally the microcircuit pins most susceptible to electrical overstress damage. Thus, this pin combination will always be included in any overstress qualification testing.

Normally, only one input will be tested per microcircuit. A representative input may be selected at random if all inputs are essentially the same. Alternatively, each input could be pulsed on a small sample of devices to determine if one pin is slightly softer than the others. Frequently, an input pin will be connected internally to more than one circuit as shown in Figure 12. In such a case, the input with the smallest fan-in would be chosen for testing since it offers the least number of paths to shunt the overstress pulse. This would be pin B in the example in Figure 12.

Output pins with respect to common and power terminals with respect to common are often likely to experience overstress conditions. As with inputs, output pins may be connected to multiple paths within the microcircuit. Examples of this are devices with tri-state outputs and direct output I^2L gates using wired-OR configuration. Figure 13 illustrates this latter case. Pin E would be chosen for qualification testing since it has a minimum of shunt paths to dissipate the overstress pulse. Likewise, a device with smaller junction area would be chosen for testing over a larger device.

The more negative voltage pin of a microcircuit, V- or GND, is generally chosen as common for microcircuits employing NPN technology (virtually all bipolar logic circuits and linear devices). This choice is made because it results in reverse biasing emitter-base junctions, usually the softest junctions in the device, when a device is pulsed with respect to

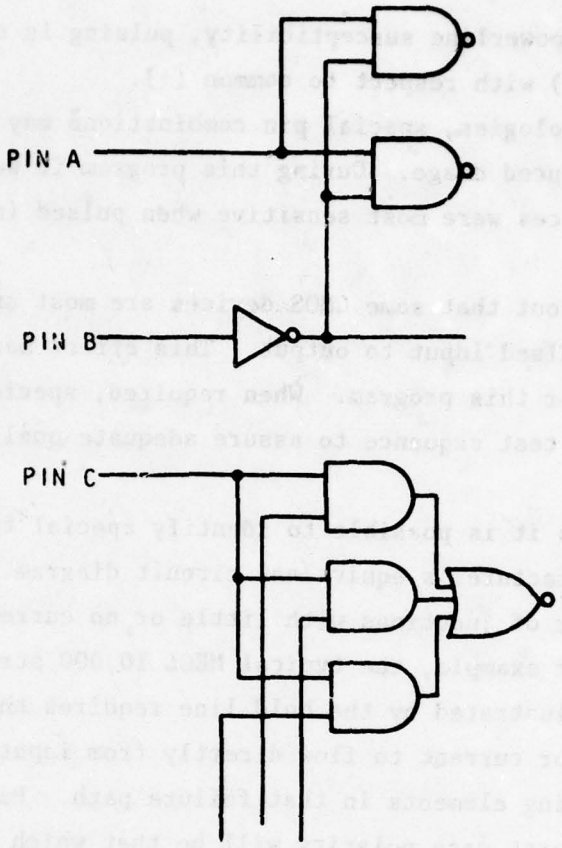


Figure 12. Microcircuit with Multiple Fan-In

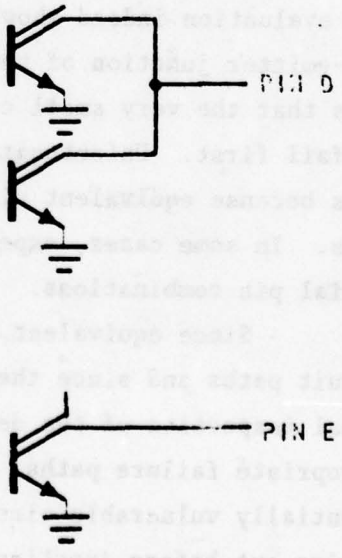


Figure 13. Microcircuit with Multiple Output Paths

common. Hence, in testing powerline susceptibility, pulsing is usually done at the positive terminal (-) with respect to common (+).

For certain technologies, special pin combinations may be the most sensitive to overstress-induced dmage. During this program it was found that ECL 10,000 series devices were most sensitive when pulsed input to output.

RADC has pointed out that some CMOS devices are most susceptible to static discharge when pulsed input to output. This effect has been seen on some devices tested under this program. When required, special tests must be added to the usual test sequence to assure adequate qualification testing.

In many instances it is possible to identify special test requirements by studying the manufacturer's equivalent circuit diagram. Pin pairs connected by a small number of junctions with little or no current limiting are suspect. Consider, for example, the typical MECL 10,000 structure shown in Figure 14. The path illustrated by the bold line requires that only two junctions be broken down for current to flow directly from input to output. There are no current limiting elements in that failure path. Past experience indicates that the worst case polarity will be that which reverse biases a base-emitter junction. In this case, that is done by pulsing the input negative with respect to the output. Experiments done in the procedure evaluation indeed show that this is the worst case polarity and the base-emitter junction of the output transistor fails. Later testing indicates that the very small collector-base junction of the input transistor may fail first. Unfortunately, it is not always possible to predict such paths because equivalent circuits do not always reflect the true current paths. In some cases, experimental evidence is the only means to determine special pin combinations.

Since equivalent circuit diagrams do not always reflect true circuit paths and since they rarely reflect parasitic current paths, a visual inspection of the device layout is often helpful in determining appropriate failure paths. Parasitic isolation junctions often protect potentially vulnerable circuit elements which results in metallization burning out before junctions. Furthermore, the existence of thin oxide

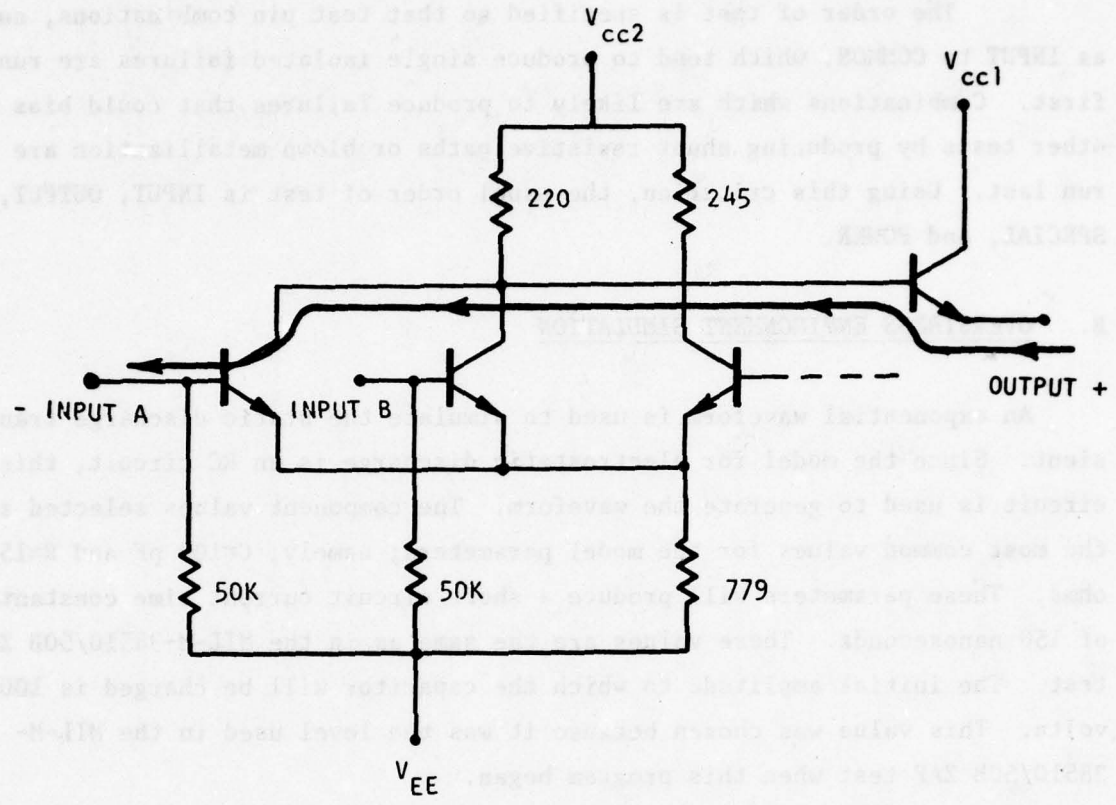


Figure 14. MECL 10,000 Damage Path

crossunders accessible from the terminals may be detected and tested for static transient susceptibility.

The order of test is specified so that test pin combinations, such as INPUT to COMMON, which tend to produce single isolated failures are run first. Combinations which are likely to produce failures that could bias other tests by producing shunt resistive paths or blown metallization are run last. Using this criterion, the usual order of test is INPUT, OUTPUT, SPECIAL, and POWER.

B. OVERSTRESS ENVIRONMENT SIMULATION

An exponential waveform is used to simulate the static discharge transient. Since the model for electrostatic discharge is an RC circuit, this circuit is used to generate the waveform. The component values selected are the most common values for the model parameters; namely, C=100 pF and R=1500 ohms. These parameters will produce a short circuit current time constant of 150 nanoseconds. These values are the same as in the MIL-M-38510/50B ZAP test. The initial amplitude to which the capacitor will be charged is 1000 volts. This value was chosen because it was the level used in the MIL-M-38510/50B ZAP test when this program began.

An exponential waveform has also been chosen to simulate the system transient. This waveform was chosen because it reasonably approximates the MIL-STD 462 waveform for a worst-case condition, it can be related to other waveforms more easily than complex waveforms such as damped sines, and it is simple to generate. The first half cycle of the MIL-STD-462 waveform can be approximated by an RC discharge having a discharge time constant of 10 μs. The component values to produce the 10-μs time constant are a capacitor of 0.1 μF and a resistor of 100 ohms. The amplitude of the simulation waveform will be discussed later in this section.

A pulse generator has been designed and fabricated to produce these two simulation waveforms. Figure 6 shows how the static discharge waveform is implemented while Figure 7 shows the short circuit current waveform delivered by the circuit. Likewise, Figures 8 and 9 show how the system transient waveform is implemented and what short circuit current waveform is

delivered by the circuit. Specifications for the environment generator are given in Table 7.

Several features have been included in the generator to provide added safety and provide for flexible operation. The capacitors in both the system and static discharge sections are normally uncharged. They are charged when the trigger button is depressed and the pulse generated when the trigger button is released. Only one type of simulation can be run at a time. All power is removed from the unused section to avoid accidental discharge and possible shock.

The device fixture boards utilize zero insertion force sockets and jumper wires to connect to the pulser output. The jumpers provide the flexibility required when testing a wide variety of microcircuit types and test pin combinations.

A detailed description of the generator is given in Appendix A of this report.

C. PROCEDURE EVALUATION

1. Setting Test Levels

The two simulation waveforms maintain the same waveshape and duration, but their amplitudes can be varied to allow testing at various levels. Selection of the test levels is critical to obtaining a meaningful specification. There are two sources of data available to determine the optimum levels. The first of these sources is an existing data base which has terminal failure data on nearly 100 microcircuit types. (REF 11-17) The second of these sources is the failure tests run on this program. Both of these data sources were used in establishing the test levels.

A large quantity of failure threshold data for microcircuits has been generated on other programs (References 11 through 15). These data were mostly taken using rectangular pulses of various pulse widths so that a functional relation between pulse width and failure threshold could be established. For example, Figure 15 shows a plot of the terminal failure power versus time to failure for TTL microcircuits tested in the INPUT to GROUND configuration. A wide range of TTL types, manufacturers and data codes are represented. The line through the data represents the least

TABLE 7. ENVIRONMENT GENERATOR SPECIFICATIONS

1. STATIC DISCHARGE SIMULATION

AMPLITUDE:	0-1000 V CONTINUOUSLY VARIABLE
TIME CONSTANT:	150 ns (SHORT CIRCUIT CURRENT)
ACCURACY:	2 PERCENT

2. SYSTEM TRANSIENT SIMULATION

AMPLITUDE:	0-300 V CONTINUOUSLY VARIABLE
TIME CONSTANT:	10 μs (SHORT CIRCUIT CURRENT)
ACCURACY:	2 PERCENT

GENERAL

MONITOR:	ANALOG METER ON FRONT PANEL WITH AUXILIARY PLUG FOR EXTERNAL DVM
RANGES:	2, SWITCH SELECTED WITH INDEPENDENT DEVICE FIXTURE BOARDS
DEVICE FIXTURE BOARDS:	1-14 PIN DIP AND 1-16 PIN DIP WITH ZERO INSERTION FORCE SOCKETS. JUMPER WIRES ARE USED TO CONNECT TEST PINS.
POWER:	117 Vac, 60 Hz, 2 A

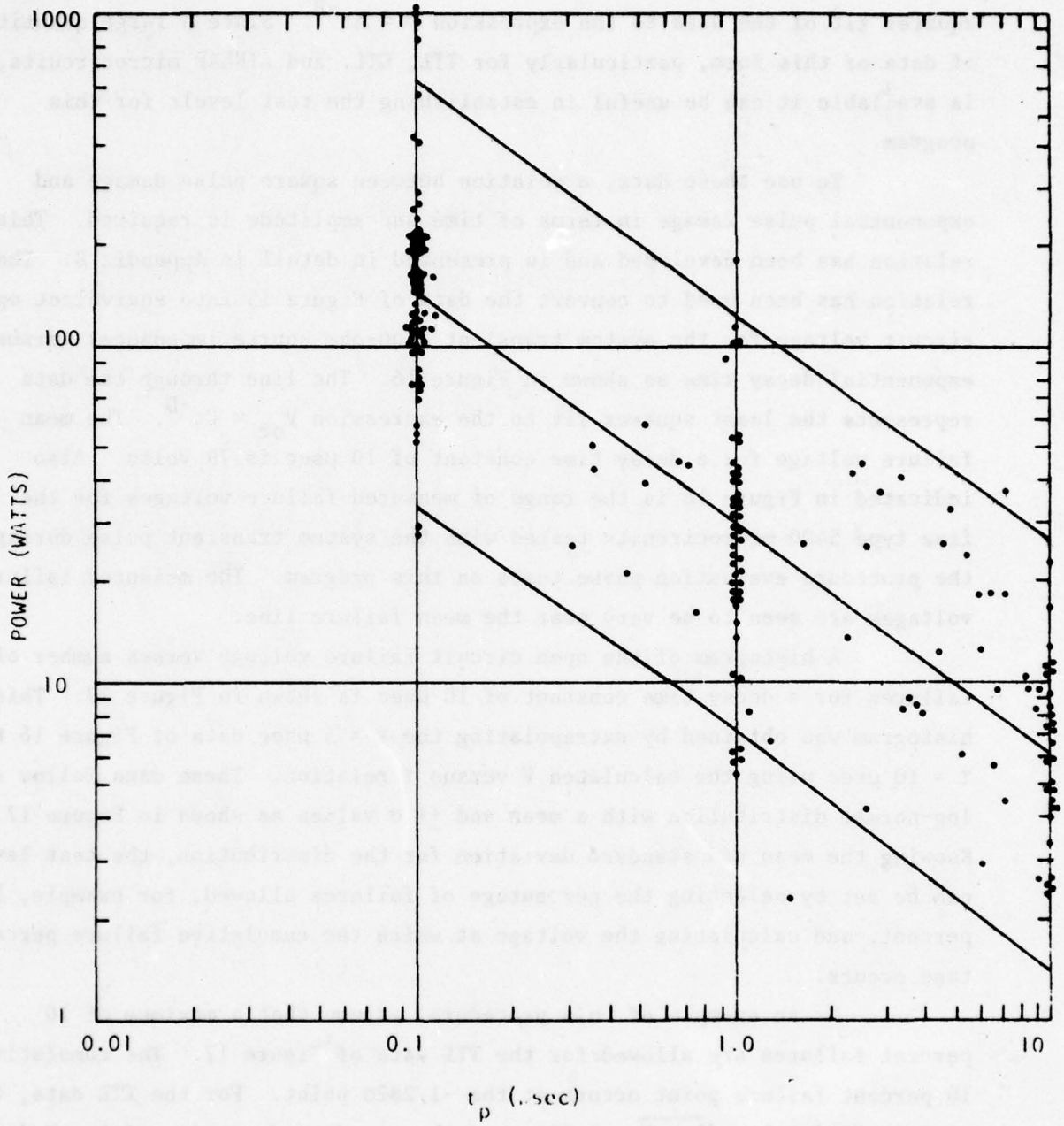


Figure 15. TTL-Input Category Failure Thresholds (Represents numerous TTL types, functions, manufacturers and date codes)

squares fit of the data to the expression $P = At^{-B}$. Since a large quantity of data of this form, particularly for TTL, DTL, and LINEAR microcircuits, is available it can be useful in establishing the test levels for this program.

To use these data, a relation between square pulse damage and exponential pulse damage in terms of time and amplitude is required. This relation has been developed and is presented in detail in Appendix B. The relation has been used to convert the data of Figure 15 into equivalent open circuit voltage for the system transient (100-ohm source impedance) versus exponential decay time as shown in Figure 16. The line through the data represents the least squares fit to the expression $V_{oc} = Ct^{-D}$. The mean failure voltage for a decay time constant of 10 μsec is 79 volts. Also indicated in Figure 16 is the range of measured failure voltages for the five type 5400 microcircuits tested with the system transient pulse during the procedure evaluation phase tests on this program. The measured failure voltages are seen to be very near the mean failure line.

A histogram of the open circuit failure voltage versus number of failures for a decay time constant of 10 μsec is shown in Figure 17. This histogram was obtained by extrapolating the τ = 5 μsec data of Figure 16 to τ = 10 μsec using the calculated V versus τ relation. These data follow a log-normal distribution with a mean and $\pm 1\ \sigma$ values as shown in Figure 17. Knowing the mean and standard deviation for the distribution, the test level can be set by selecting the percentage of failures allowed, for example, 10 percent, and calculating the voltage at which the cumulative failure percentage occurs.

As an example of this procedure, assume that a maximum of 10 percent failures are allowed for the TTL data of Figure 17. The cumulative 10 percent failure point occurs at the -1.282σ point. For the TTL data, the mean is 79.4 volts ($\overline{\log V} = 1.90$), and the standard deviation of log V ($\sigma_{\log V}$) is 0.147. Therefore, the 10 percent failure threshold voltage is calculated as:

$$\log V_{TH} = \overline{\log V} - 1.282\sigma_{\log V}$$

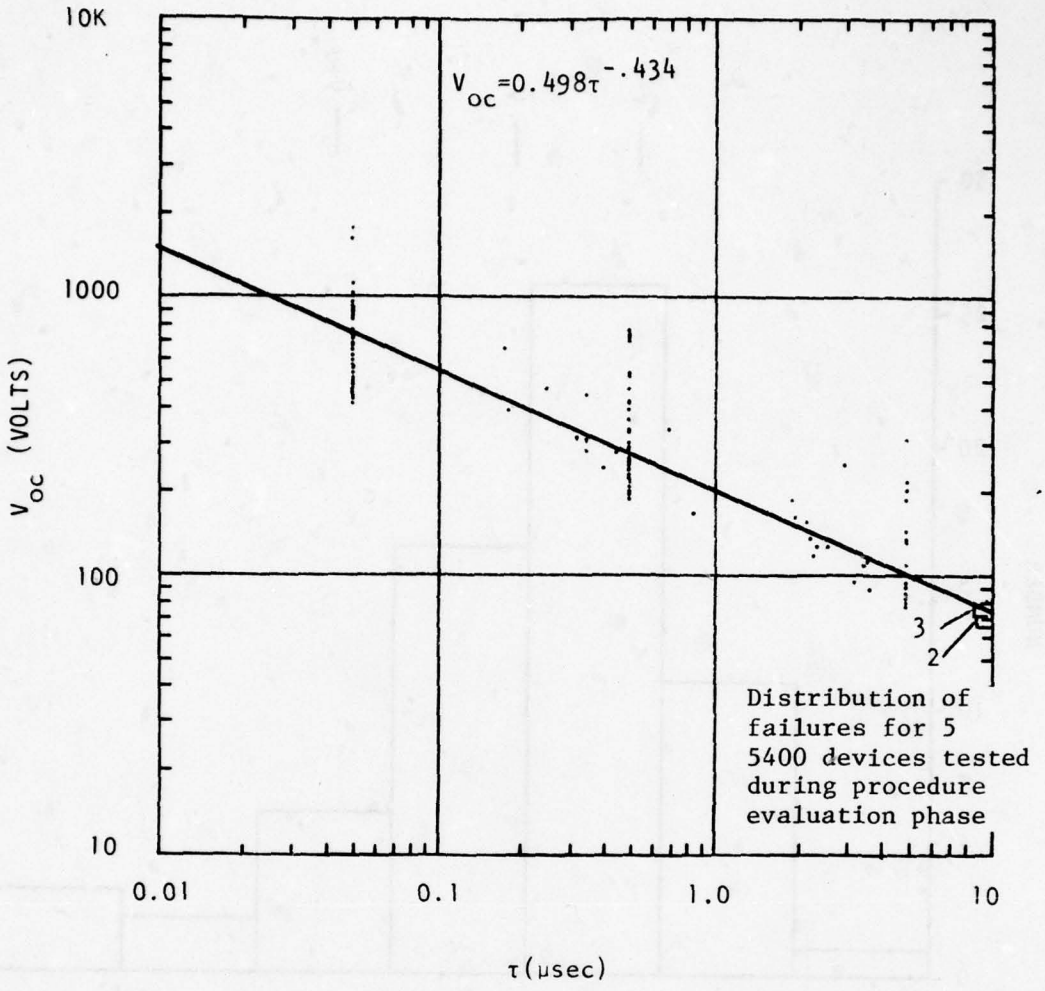


Figure 16. Plot of Open Circuit Failure Voltage Versus Exponential Decay Time for TTL Input Category (for 100-Ω source impedance, double exponential waveform)

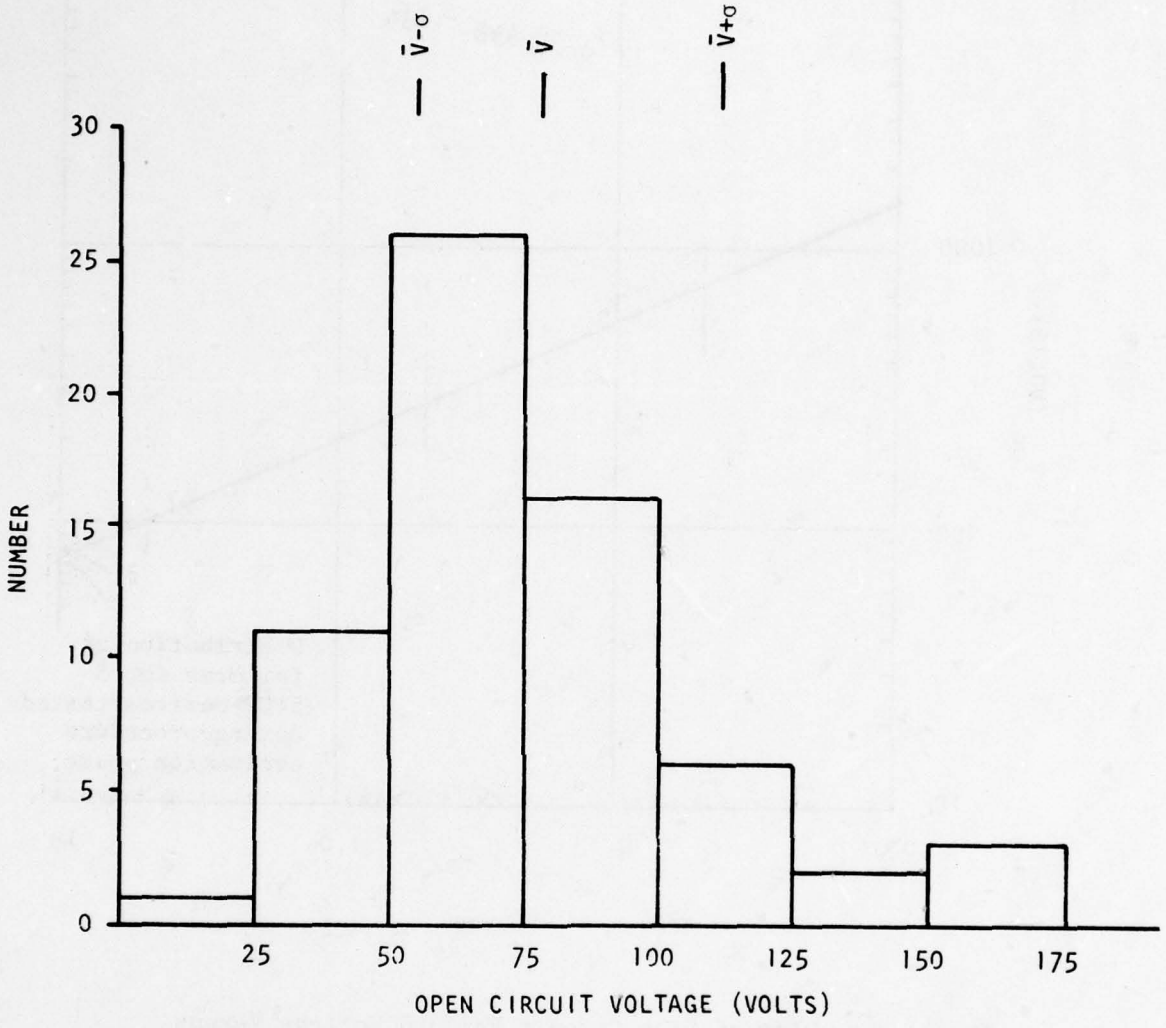


Figure 17. Failure Voltage Histogram for TTL Input Category, $\tau \simeq 10$ μsec, Projected Data from Figure 16.

$$\log V_{TH} = 1.90\text{-}1.282(0.147)$$

or

$$V_{TH} = 51.4 \text{ volts.}$$

Sufficient data are available to use this method for TTL, DTL, and certain LINEAR microcircuit types.

For newer technologies where such information is not yet available, the results of the tests conducted under this program and other similar small sample tests are the only practical guide to setting test levels. Initial test level estimates have been made based on the lowest observed failure level. It will be necessary to adjust these levels as more data become available.

The above example illustrated screening at a level that should produce 10 percent failures based on an assumed log-normal distribution. With the small sample sizes characteristic of this program, it is usually not possible to distinguish normal and log-normal distributions. Therefore, the normal mean and standard deviation are usually calculated. Also, it is risky to set the testing points as high as the 10 percent failure level unless the distributions are well characterized. Thus, the testing levels are usually set at the -2σ point; that is, at the level defined by the mean minus two standard deviations.

Testing at this level would be expected to produce 2 to 3 percent failures based on a well characterized normal distribution. When only a limited sample is available for determining the failure voltage distribution, the 90 percent confidence interval and worst case V and σ can be used to set $V_{TH} = V_{MIN} - 2\,\sigma_{MAX}$.

At present, the static test level of 1000 volts appears to be suitable for all technologies tested under this program. Very few failures were observed in the static discharge tests.

2. Experimental Results

The test procedures used during the first test phase differ from the procedures that would normally be used in qualification testing in that additional pre- and posttest data were taken and that the microcircuits were step-stressed to failure. Both of these variations in procedure were used

to obtain additional failure data not required for normal microcircuit qualification. The additional data obtained from these modifications aided in the overall procedure evaluation.

Prior to testing, each microcircuit type was subjected to a pretest analysis to determine worst case pulse polarity, candidate pin combinations, and test sequence. The circuit analysis was based on the manufacturer's schematic or equivalent circuit diagram. The starting pulser levels for the step-stressing were obtained by taking the minimum failure voltage for all microcircuits of the family tested on previous programs and applying the waveform correction and source resistance described previously.

A pretest characterization of all devices was run using an Alma 480B Integrated Circuit Tester. The characterization included both functional and parametric tests. In addition, curve tracer measurements were taken to determine the normal V-I characteristics of each device.

The microcircuits were pulsed using the test setup shown in Figure 18. The Tektronix 556 oscilloscope with C27 camera was used to record the transient voltage and current waveforms. For each microcircuit tested, the pulser was set to the starting amplitude and the microcircuit pulsed. The microcircuit was then tested using the Alma 480B to determine if it would still meet its specifications. If the microcircuit showed no damage, the pulser level was increased and the pulse and posttest cycle repeated until the device failed. Following failure, parametric tests were run to obtain voltage and current measurements on the failed device terminal to be used in failure analysis. Finally, the microcircuits were decapped and the chip photomicrographed.

Table 8 summarizes the results of the system transient tests on the first 10 microcircuit types. Included in Table 8 are the worst case test pin combinations, the predicted and measured mean failure voltages, the standard deviation of the failure voltage, the 90-percent confidence intervals and the voltage at the V_{MIN} $-2\sigma_{MAX}$ point. Predicted values of failure voltage are given only for those technologies for which sufficient data were available from other programs.

Except for the 4066, all microcircuit types were tested in three different configurations: input to ground, output to ground, and power to ground. The 4066 was tested across the transmission gate only. In some

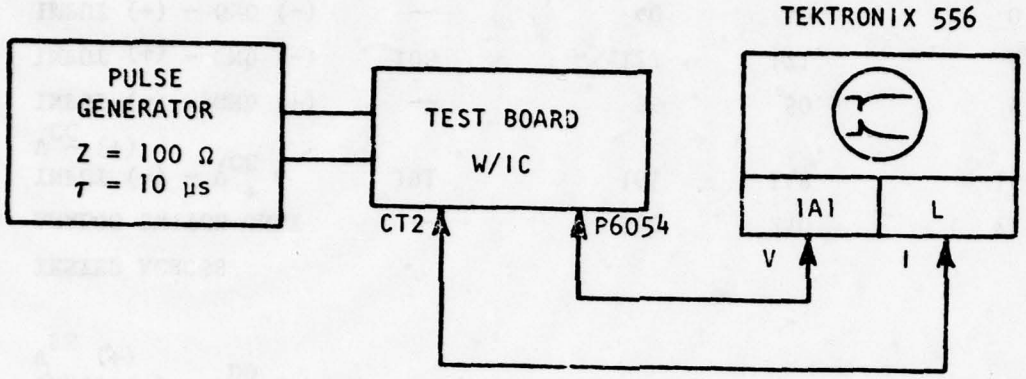


Figure 18. Pulse Test Setup

TABLE 8. MICROCIRCUIT TEST RESULTS SUMMARY
(PROCEDURE EVALUATION PHASE)

TYPE	WORST CASE TEST PIN COMBINATION	$\overline{V}$ PREDICTED (VOLTS)	$\overline{V}$ MEASURED (VOLTS)	$\overline{V}$ MIN (90% Conf)	σ	σ_{MAX} (90% Conf)	$\overline{V}_{MIN} - 2\sigma_{MAX}$ (Volts)
5400	INPUT (+) - GND (-)	79	73	70.5	2.7	5.1	60.3
54LS00	INPUT (+) - GND (-)	79	87	82.8	4.5	8.5	65.8
10102	INPUT (-) - OUT (+)	--	116	106	10.6	20	66.0
4001	INPUT (-) - V_{DD} & V_{SS} (+)	--	226	205	21.9	41.3	122
	TESTED ACROSS						
4066	ANALOG SWITCH ONLY	--	260	240	21.6	40.8	158
µA741	INPUT (-) - V_{CC}^{+} & V_{CC}^{-} (+)	191	161	148	14.2	26.8	94.4
XRC401	INPUT (-) - GND (+)	--	56	50.5	5.9	11.1	28.3
946	INPUT (+) - GND (-)	108	127	121	6.8	12.8	95.4
54S00	INPUT (+) - GND (-)	--	40	40	0	0	40
µA723	$\overline{V}$ (-) - V^{+} (+)	--	99	92.6	6.8	12.8	67

cases, the worst case pin combinations were other than the three given above. In those cases, an additional combination was tested and is indicated in Table 8.

The predicted and measured mean voltages are in good agreement. The largest observed difference is 18 percent in the μA741. The standard deviations for the test samples are much smaller than those of the data used for the prediction. This is to be expected since the data used for the prediction include more devices, devices of different types, and several manufacturers. The data show that the waveform conversion technique presented earlier can be used to predict the test levels for the specification where sufficient previous data exist.

The 4001 and the 4066 were tested for static discharge transients in the three test configurations listed previously. These initial tests were run with the V_{DD} and V_{SS} pins tied together. This configuration may have influenced the test results by making the devices less likely to fail. Therefore, all subsequent tests were run with respect to V_{DD} or V_{SS} individually. In addition, the 4001 was tested from input to output. These tests were run at 1000 volts peak voltage. There were no failures observed during any of these tests. Several Schottky TTL devices were also tested for static discharge sensitivity with no failures observed.

Each of the microcircuit types that failed during the test has been analyzed to determine the mode and mechanism that produced the failure. This analysis consisted of additional electrical measurements and a decap and microscopic inspection of the chip. With the exception of the 4066, all failures were due to an increase in leakage current at the test terminal so that the microcircuit failed to meet its specifications. The 4066 failed due to an open metallization path to the transmission gate as shown in Figure 19. Under overstress conditions, the transmission gate appears as a low resistance which permits a heavy current to flow through the signal input metallization and cause the burnout (see Figure 20).

Additional electrical tests were run to try to isolate the component that failed. These tests included parametric tests on the Alma 480B integrated circuit tester and pin-to-pin curve tracer measurements. Die probing was not done, but failure paths were verified by optical inspection where possible. The measurements indicate that the 5400 and 54S00 failures

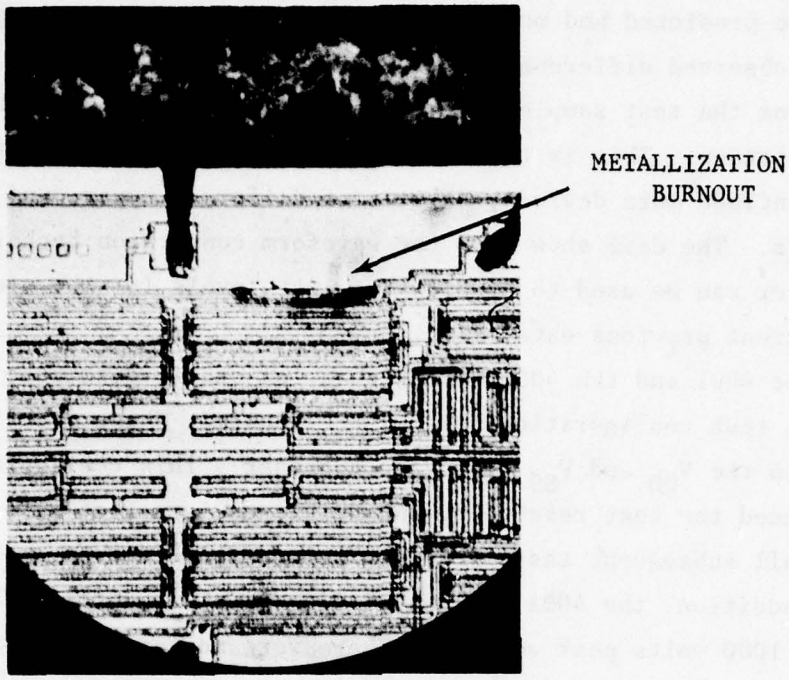


Figure 19. Metallization Burnout in the 4066 Due to Simulated System Transient Overstress Environment

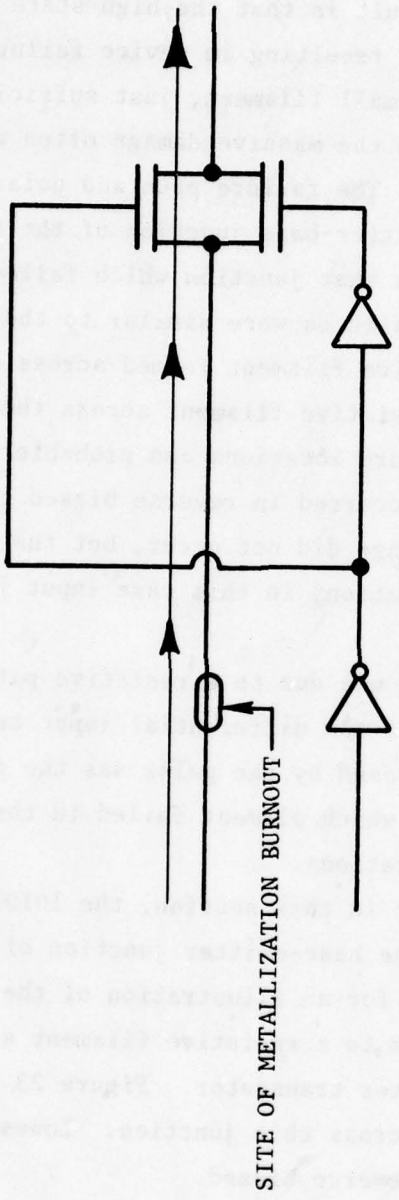


Figure 20. Damage Path for 4066 Transmission Gate

are due to a resistive filament across the emitter-base junction of the multiple emitter transistor. The dashed line in Figure 21 shows the location of this filament. The result is that the high state leakage current is increased beyond specification, resulting in device failure. Because the devices were step-stressed, a small filament, just sufficient to cause failure, was formed rather than the massive damage often associated with electrical overstress failure. The failure path and polarity shown in Figure 21 indicate that the emitter-base junction of the input transistor was reverse biased, thus it was that junction which failed.

The 946 and 54LS00 failures were similar to those in the TTL structure except that a resistive filament formed across the input diode. The 54LS00 also exhibited a resistive filament across the input clamp diode. Figure 22 illustrates the failure locations and probable failure paths. Note that the failures again occurred in reverse biased junctions. Because of step stressing, massive damage did not occur, but the level at which the device failed to meet specification, in this case input leakage current, was determined.

Failure in the μA723 was due to a resistive path across the emitter-base junction of one of the differential input transistors. Whichever transistor was reverse biased by the pulse was the one that failed. It was not possible to determine which element failed in the μA741, but input bias current exceeded specifications.

As discussed earlier in this section, the 10102 failure was due to a resistive filament across the base-emitter junction of the output transistor. Refer back to Figure 14 for an illustration of the failure path. The XC401 I^2L gate failure was due to a resistive filament across the base-emitter junction of the inverter transistor. Figure 23 shows that the full pulser potential is applied across this junction. Lowest failure level occurs when the junction is reverse biased.

The 4001 failure was due to a resistive path across the input protection diode that is connected to V_{DD}. There were no observed oxide punchthroughs.

At RADC's suggestion, several additional static discharge tests were run. Test configurations included INPUT to COMMON for Schottky TTL and

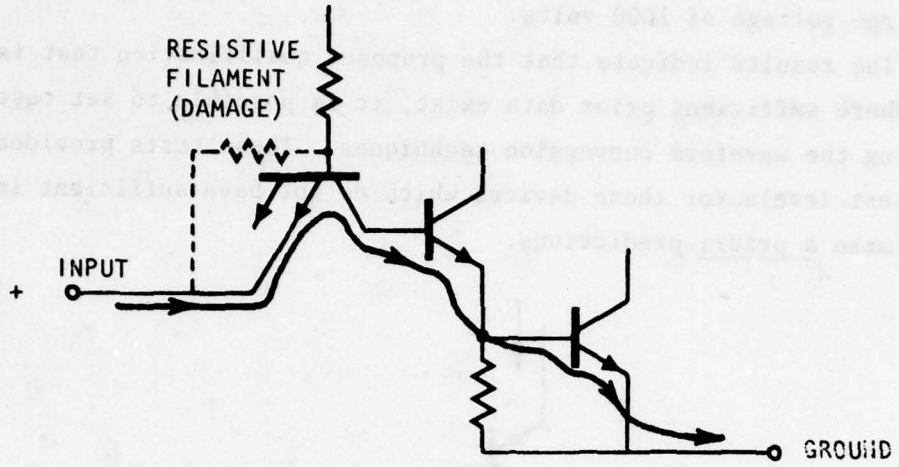


Figure 21. Damage Path in TTL Input Failure

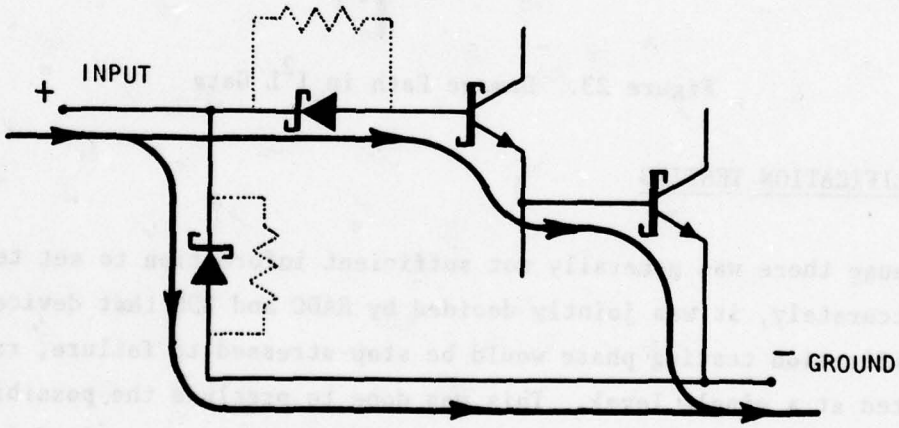


Figure 22. Damage Paths for 54LS00

INPUT to OUTPUT for CMOS. No failures were seen for any configuration with a full charge voltage of 1000 volts.

The results indicate that the proposed qualification test is viable. Where sufficient prior data exist, it is possible to set test levels using the waveform conversion techniques. These tests provided starting test levels for those devices which do not have sufficient information to make *a priori* predictions.

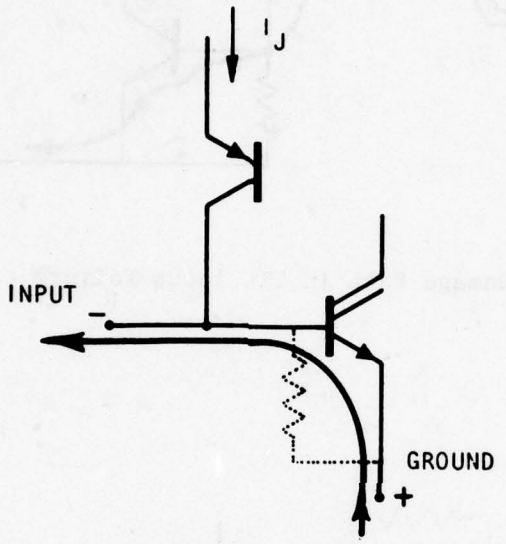


Figure 23. Damage Path in I^2L Gate

D. QUALIFICATION TESTING

Because there was generally not sufficient information to set testing levels accurately, it was jointly decided by RADC and BDM that devices in the qualification testing phase would be step-stressed to failure, rather than tested at a single level. This was done to preclude the possibility of failing all devices at the initial level which would have resulted in no information being gained.

A sample of 15 units of each of the 40 device types listed in Table 2, representing all major microcircuit technologies, were tested in the appropriate configurations. Representative devices were subjected to failure analysis to determine the failure modes and failure paths. The results of the qualification testing are presented and discussed by technology in the

following subsections. A summary of the results is presented in the final subsection.

1. Bipolar Logic

a. Diode Transistor Logic (DTL)

Since DTL devices are not widely used in new designs, little emphasis was placed on this technology. Only one type, the 946 NAND gate, was tested. Figure 24 shows the histogram for failure voltages for the 946 input along with a normal distribution having the same mean and standard deviation as the sample. The histogram bins indicate failure between the highest no-fail voltage and the voltage at which the device failed. The mean failure level observed here is much lower than the failure level seen during procedure evaluation. Two different manufactures were used, and it is not uncommon for DTL failure levels to vary greatly with manufacturer, especially at relatively long pulse widths. In general, the failure levels of DTL devices are comparable to those of TTL devices (see the summary in subsection 6).

All devices failed dc parametric limits only, specifically I_{IH}. Failure analysis indicated filaments formed across the associated input diode, which led to the parametric failure. This was the same failure mode seen during procedure evaluation and is the common failure mode for DTL devices subjected to electrical overstress. Other pin combinations tested include output to ground and V_{CC} to ground. No failures occurred at the highest input failure level (75 volts).

When combined with previous data, these results suggest that a testing level of 50 volts is probably appropriate for DTL devices. The weakest configuration is input positive with respect to common.

b. Gold-Doped Transistor-Transistor Logic (TTL)

Three versions of gold-doped TTL were tested; standard (54), high speed (54H), and low power (54L). In standard TTL, one small scale integrated circuit, the 5400 NAND gate, and two medium scale integrated circuits, the 5483 full adder and the 54153 multiplexer, were tested. Plots of the failure histograms are shown in Figures 25 through 27 along with a normal curve having the same mean and standard deviation as the sample. In

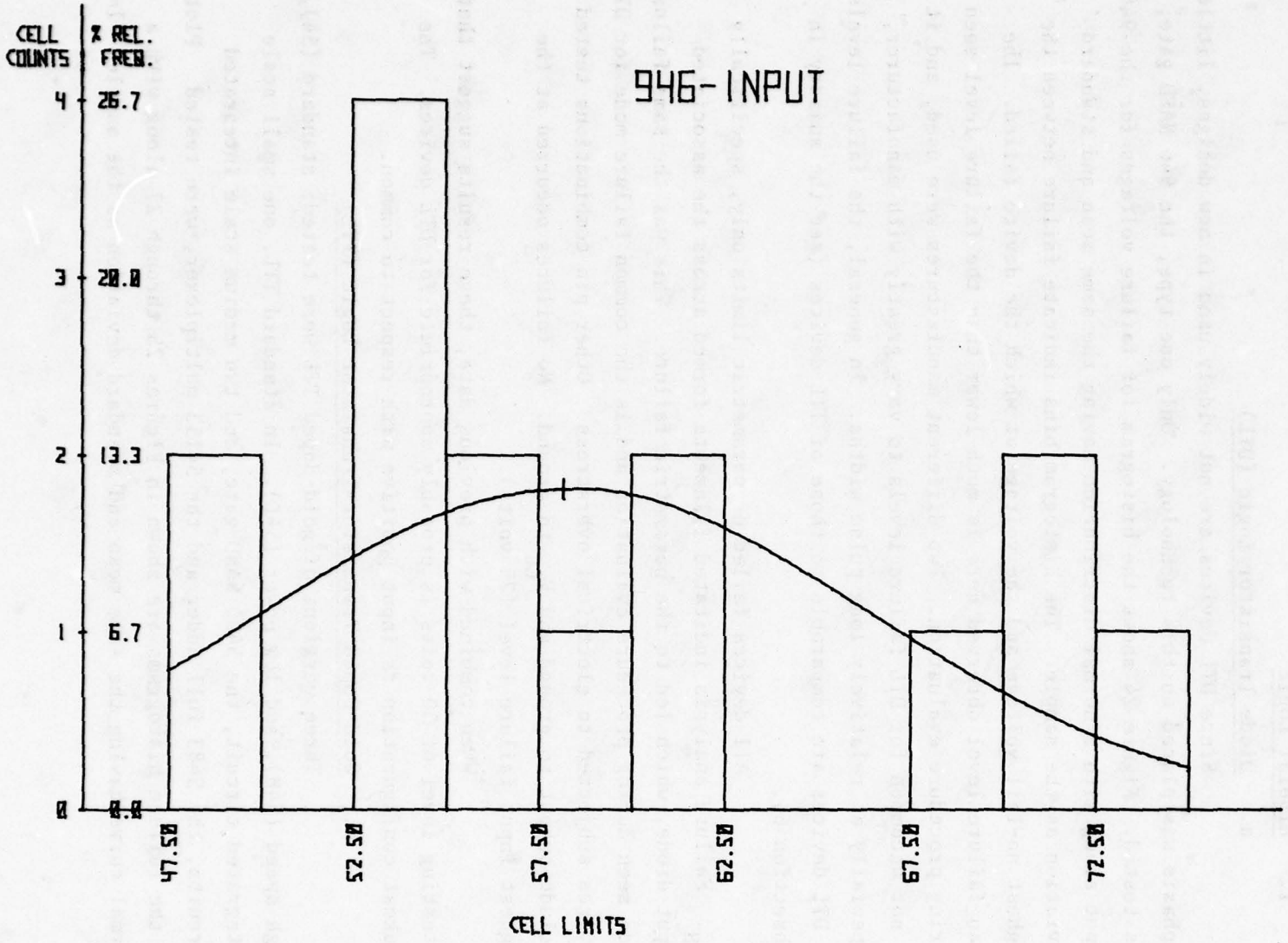


Figure 24. Histogram of Failure Voltages for the DTL 946 Input System Transient Tests.

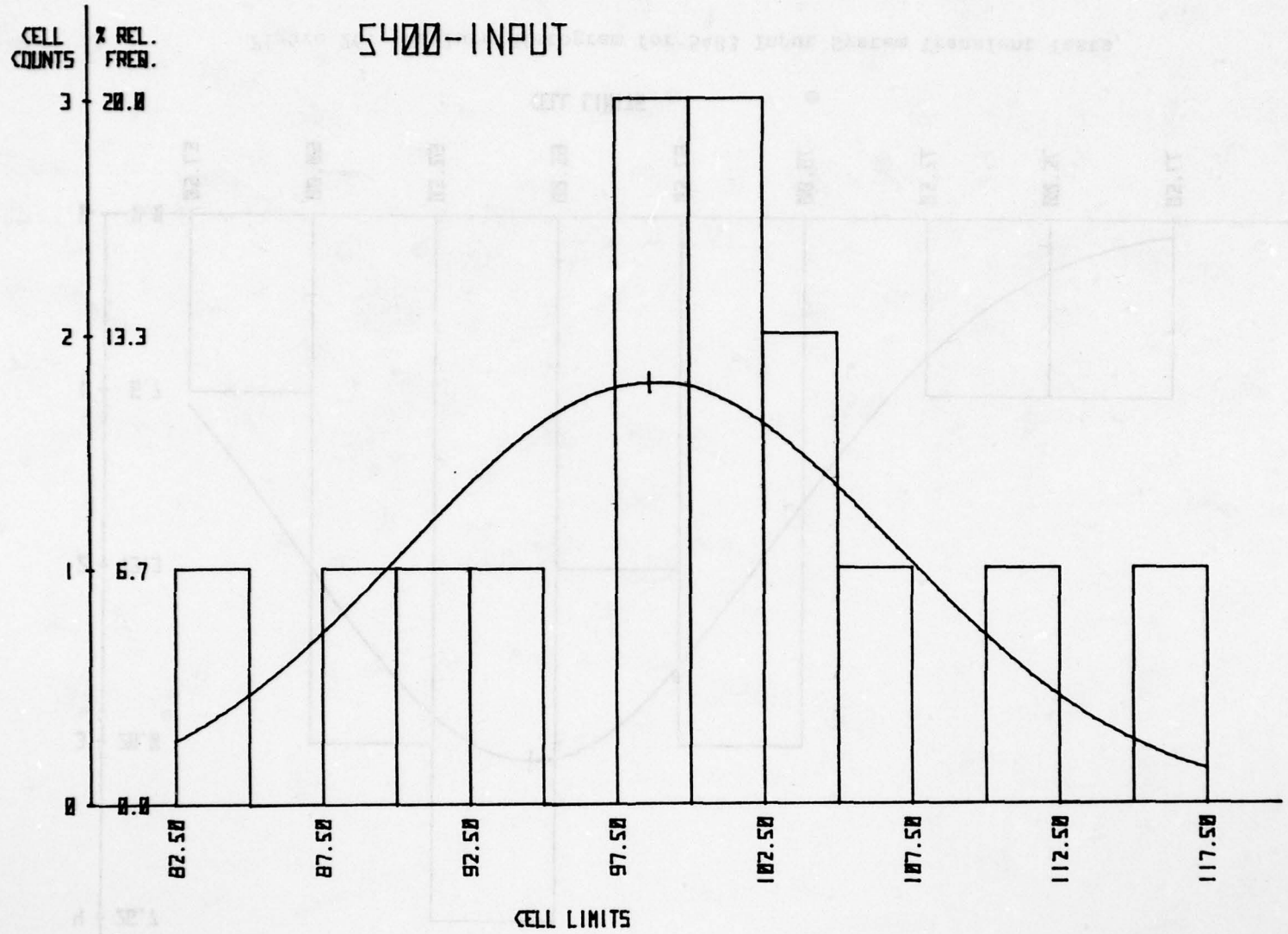


Figure 25. Failure Histogram for 5400 Input System Transient Tests

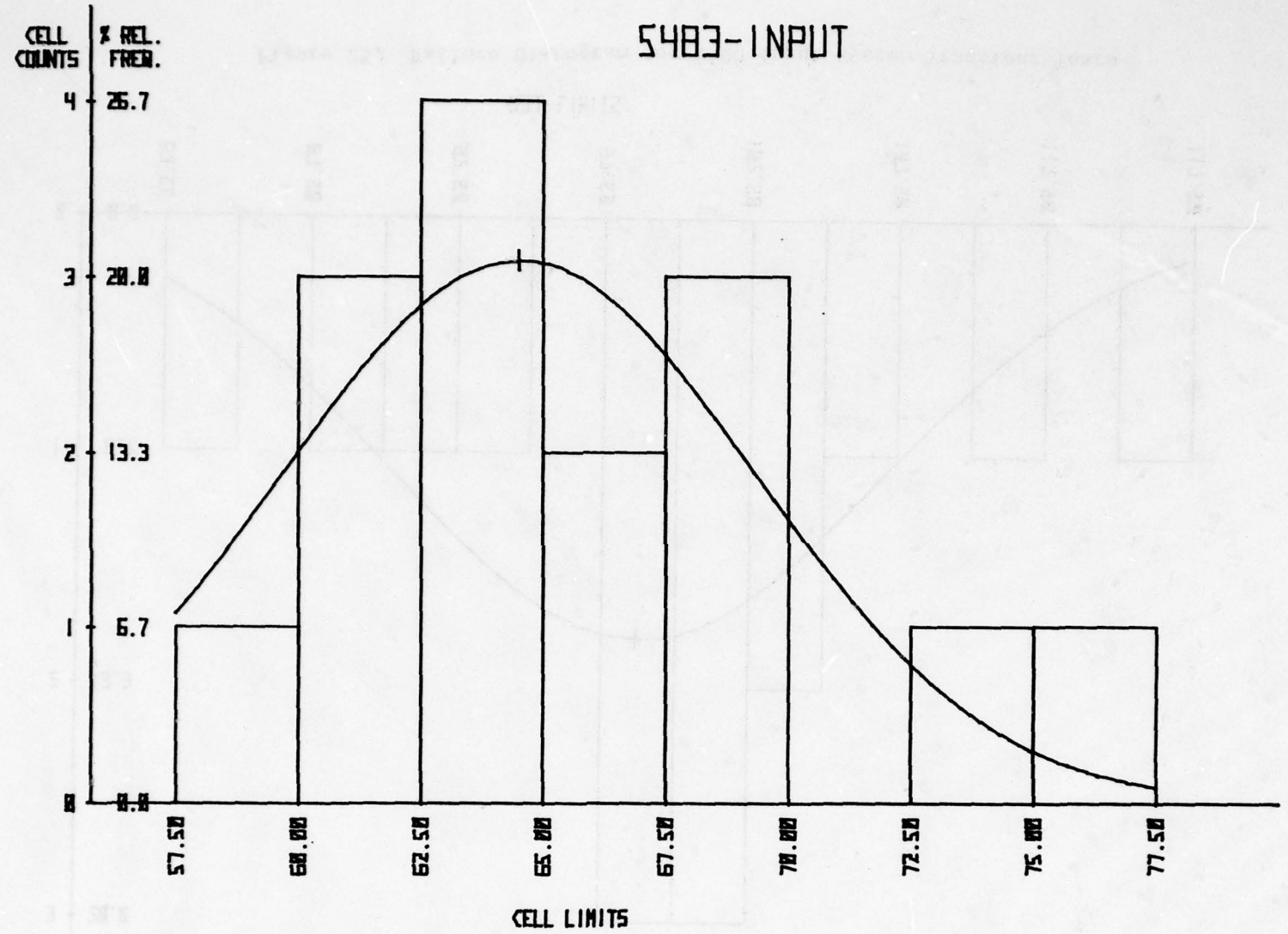


Figure 26. Failure Histogram for 5483 Input System Transient Tests

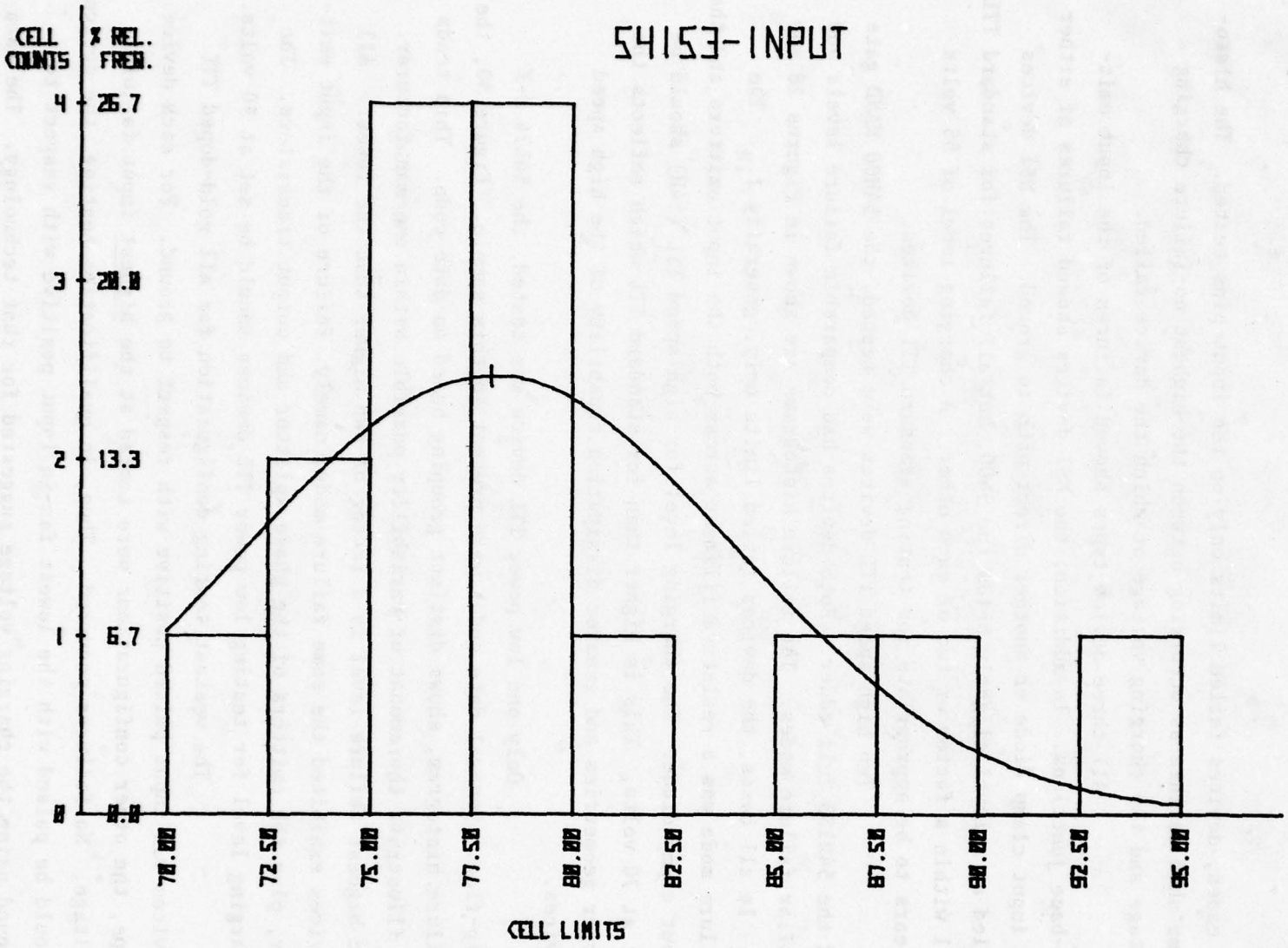


Figure 27. Failure Histogram for 54153 Input System Transient Tests

all cases, devices failed limits only on the input pins tested. The histograms show failure as occurring between the highest no-failure charging voltage and the charging voltage at which the device failed.

All three device types showed failures of the input emitter-base junctions. In addition, the MSI devices showed failures of either the input clamp diode or another direct path to ground. The MSI devices failed at a level slightly below the 5400, but all failures for standard TTL fell within a factor of two of each other. A charging level of 55 volts appears to be appropriate for testing standard TTL devices.

Two high speed TTL devices were tested, the 54H00 NAND gate and the 54H183 full adder. Both devices had comparable failure levels and similar failure modes. The failure histograms are shown in Figures 28 and 29. In all cases, the devices failed limits only, generally I_{IH}. The failure mode was a resistive filament across both the input emitters and the input clamp diode. The charging level for high speed TTL (54H) should be set at 70 volts. This is higher than for standard TTL which reflects the larger geometries and greater dissipation capability of the high speed devices.

Only one low power TTL device was tested, the 54L74 J-K flip-flop. Several date codes were present in this sample. Figure 30, the failure histogram, shows distinct grouping based on date code. This tends to illustrate the amount of variability possible within one manufacturer. The highest failure level is a factor of two higher than the lowest. All devices exhibited the same failure mode, namely, failure of the input emitter, plus the emitters of the phase splitter and output transistors. The charging level for testing low power TTL devices should be set at 50 volts.

The weakest testing configuration for all gold-doped TTL devices was input pulsed positive with respect to ground. For each device type, the other configurations were tested at the highest input failure voltage. No failures occurred. Thus, in qualification testing, the devices should be pulsed with the lowest fan-in input positive with respect to ground using the charging voltage suggested for that technology. The data are summarized in Subsection 6.

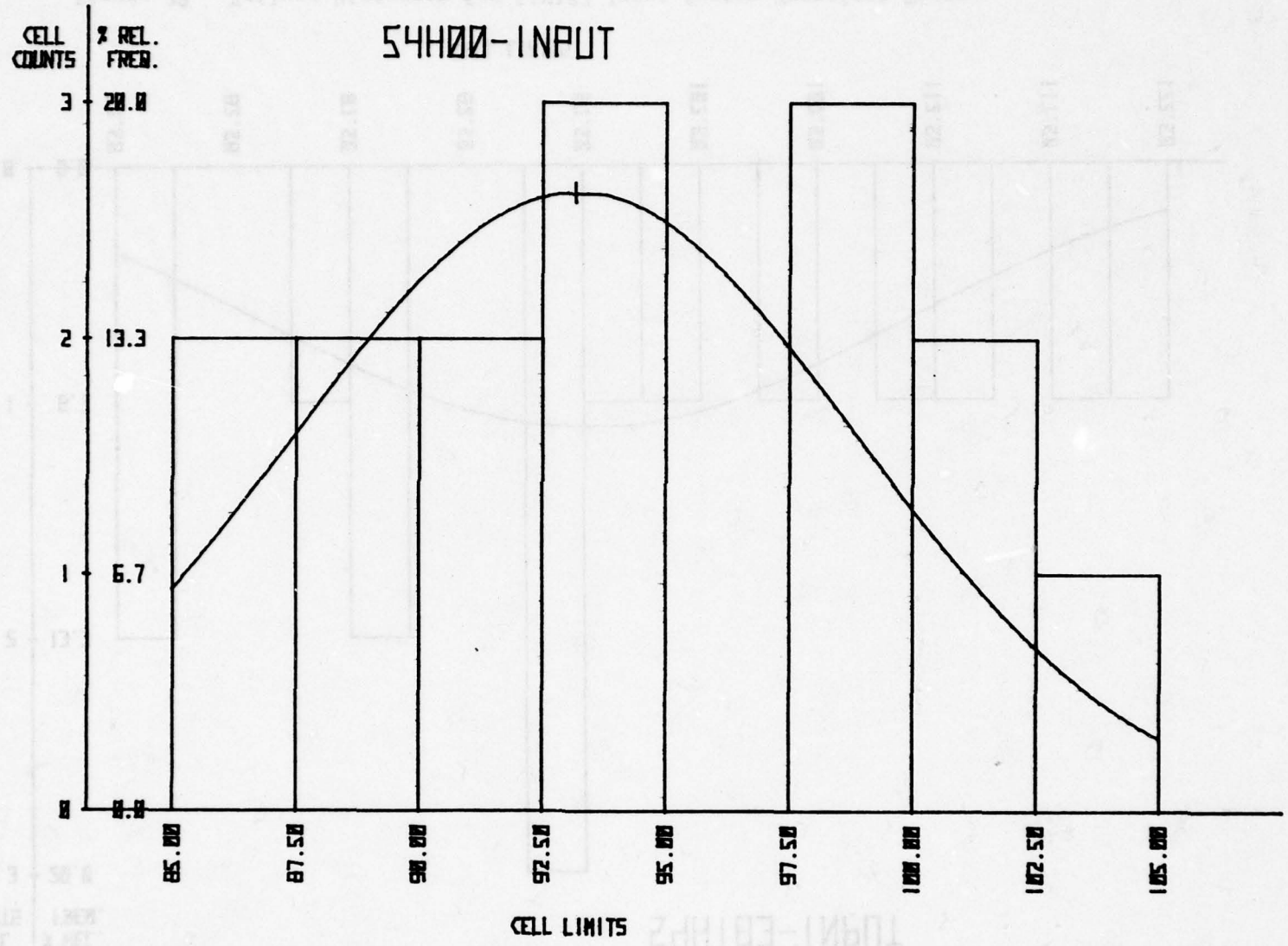


Figure 28. Failure Histogram for 54H00 Input System Transient Tests

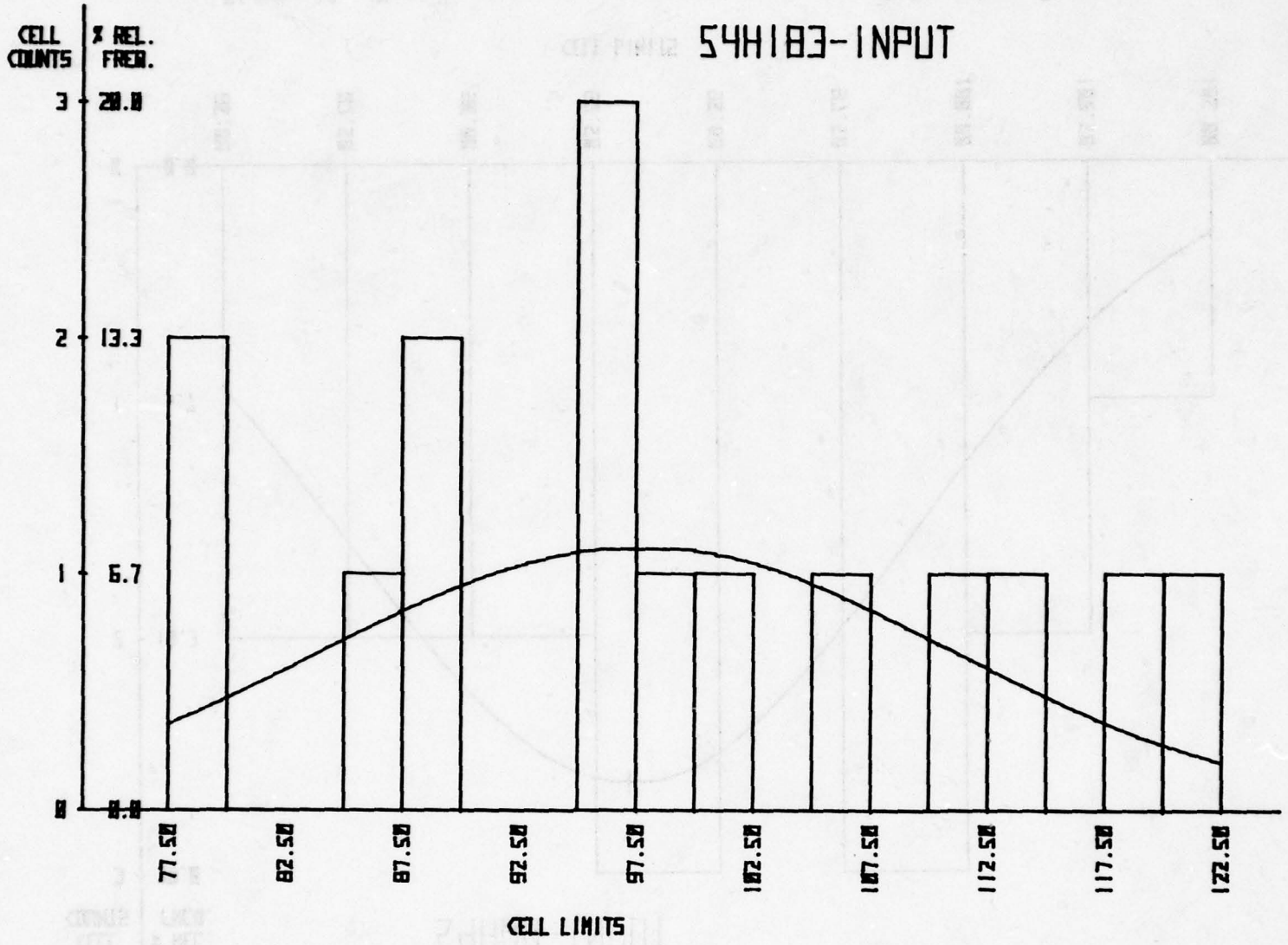


Figure 29. Failure Histogram for 54H183 Input System Transient Tests

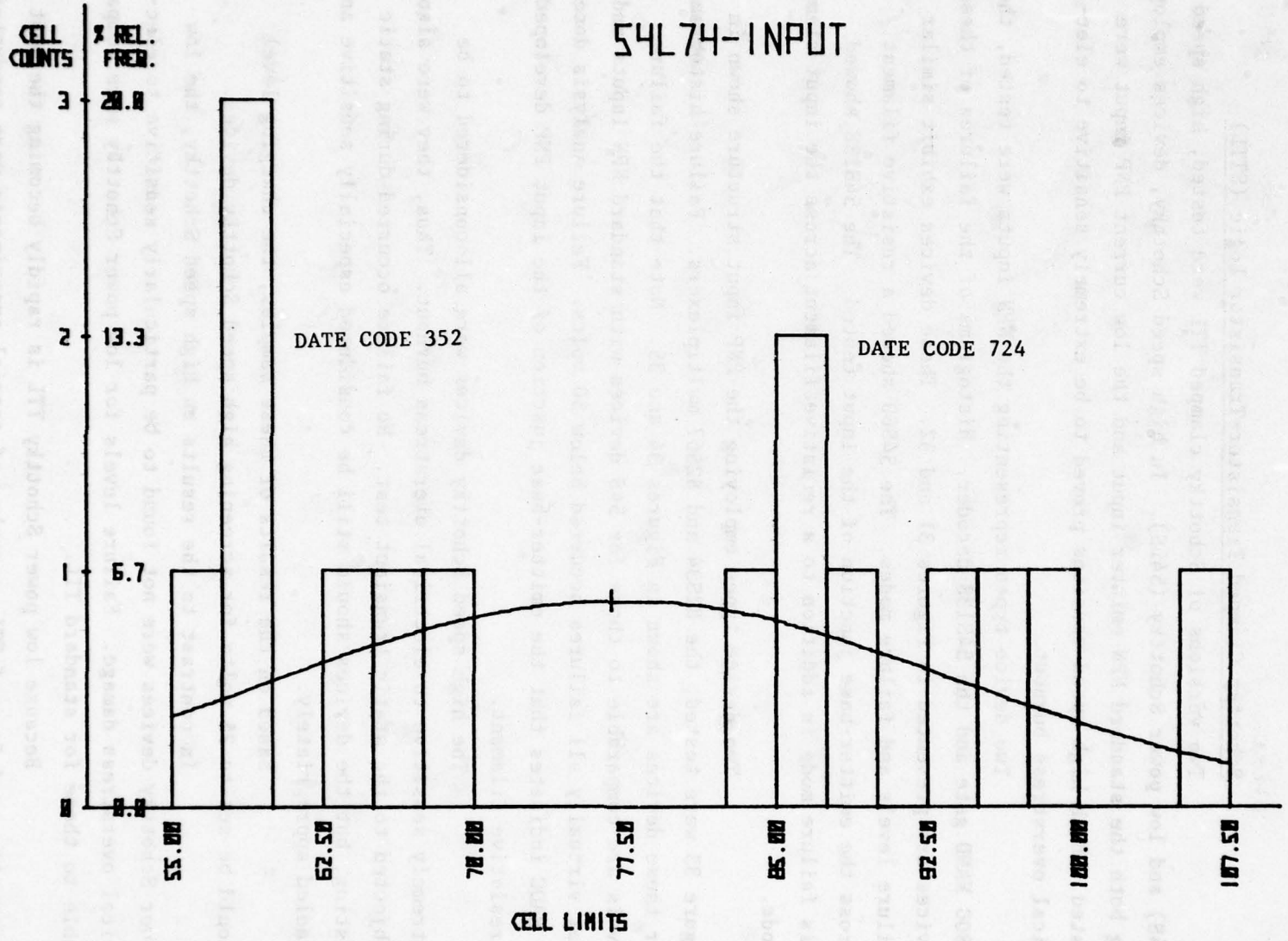


Figure 30. Failure Histogram for 54L74 Input System Transient Tests

c. Schottky Clamped Transistor-Transistor Logic (STTL)

Two versions of Schottky clamped TTL were tested, high speed (54S) and low power Schottky (54LS). In high speed Schottky, devices employing both the standard NPN emitter input and the low current PNP input were tested. Both high speed versions proved to be extremely sensitive to electrical overstress burnout.

Two device types representing the NPN inputs were tested, the 54S00 NAND gate and the 54S138 decoder. Histograms of the failures of these devices are presented in Figures 31 and 32. These devices exhibit similar failure levels and failure modes. The 54S00 showed a resistive filament across the emitter-base junction of the input tested. The 54S138 showed this failure mode in addition to a resistive filament across the input clamp diode.

Two device types employing the PNP input structure shown in Figure 33 were tested, the 82S34 and 82S67 multiplexers. Failure histograms for these devices are shown in Figures 34 and 35. Note that the failure levels are comparable to those for 54S devices with standard NPN Inputs and that virtually all failures occurred below 50 volts. Failure analysis done by RADC indicates that the emitter-base junction of the input PNP developed a resistive filament.

The high speed Schottky devices were all considered to be extremely sensitive to electrical overstress burnout. Thus, they were also subjected to the static transient test. No failure occurred during static testing, but the devices should still be considered especially sensitive and handled appropriately.

Based on the results of these samples, the charging level should be set to 25 volts for screening high speed Schottky devices.

In contrast to the results on high speed Schottky, the low power Schottky devices were not found to be particularly sensitive to electrical overstress damage. Failure levels for low power Schottky were comparable to those for standard TTL.

Because low power Schottky TTL is rapidly becoming the most frequently used form of TTL, a number of special experiments were conducted with this technology. A total of 7 representatives of this technology were included among the 40 device types. Samples of the 54LS00 NAND gate were

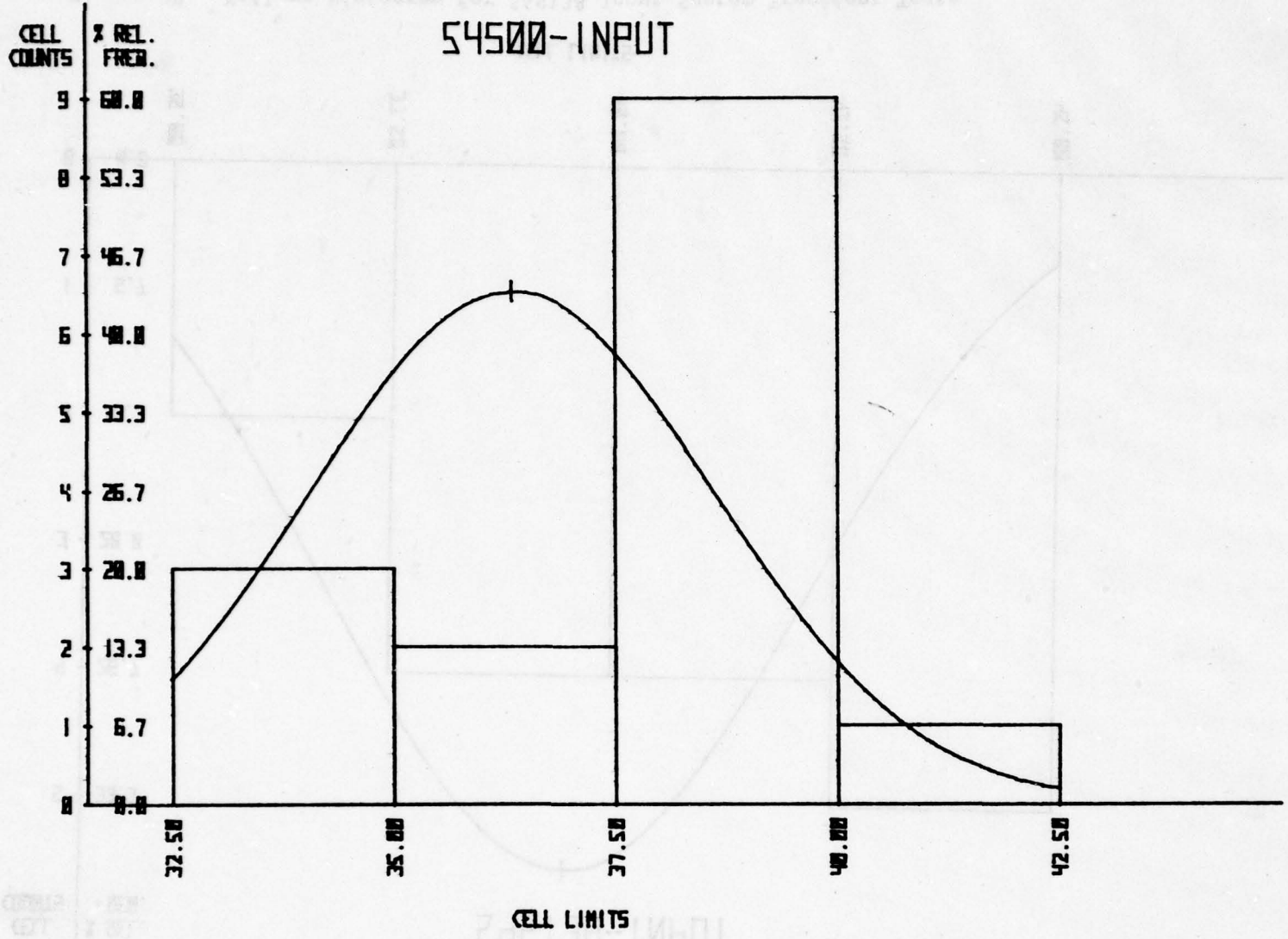


Figure 31. Failure Histogram for 54S00 Input System Transient Tests

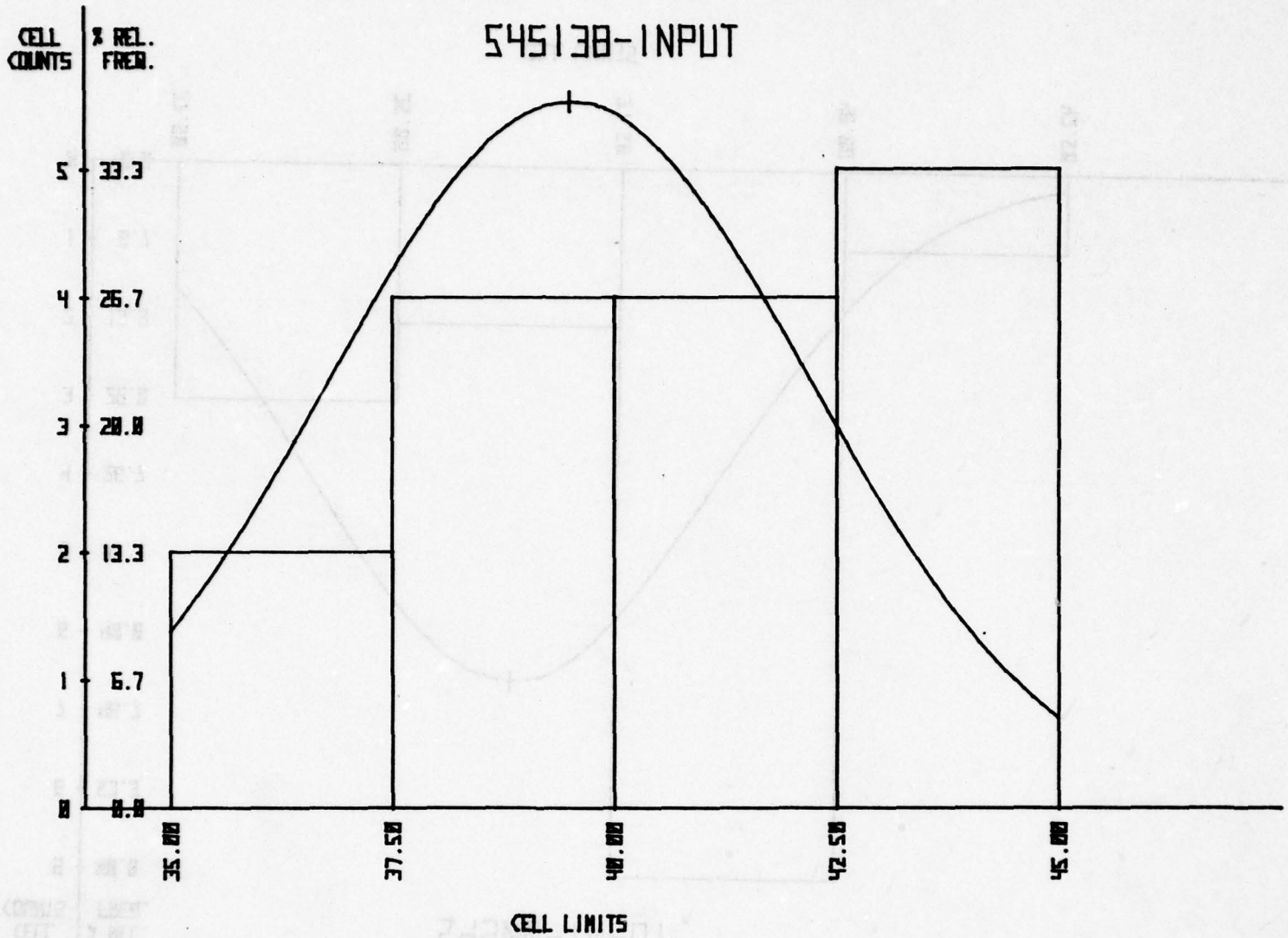


Figure 32. Failure Histogram for 54S138 Input System Transient Tests

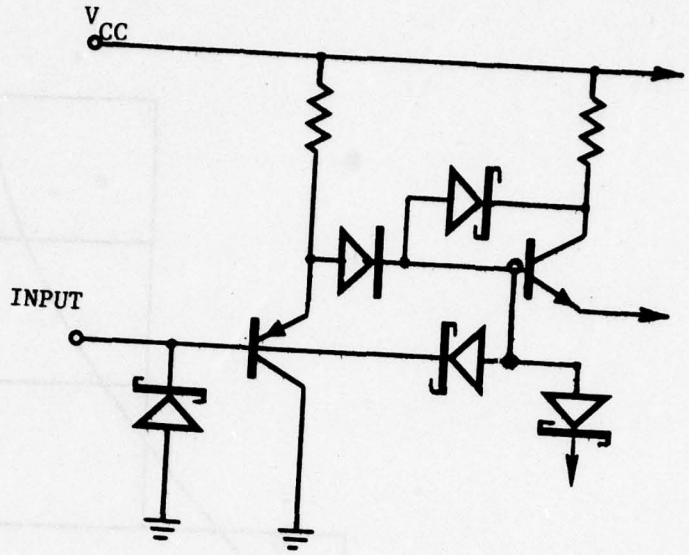


Figure 33. Alternate Input Structure for High Speed Schottky Clamped TTL

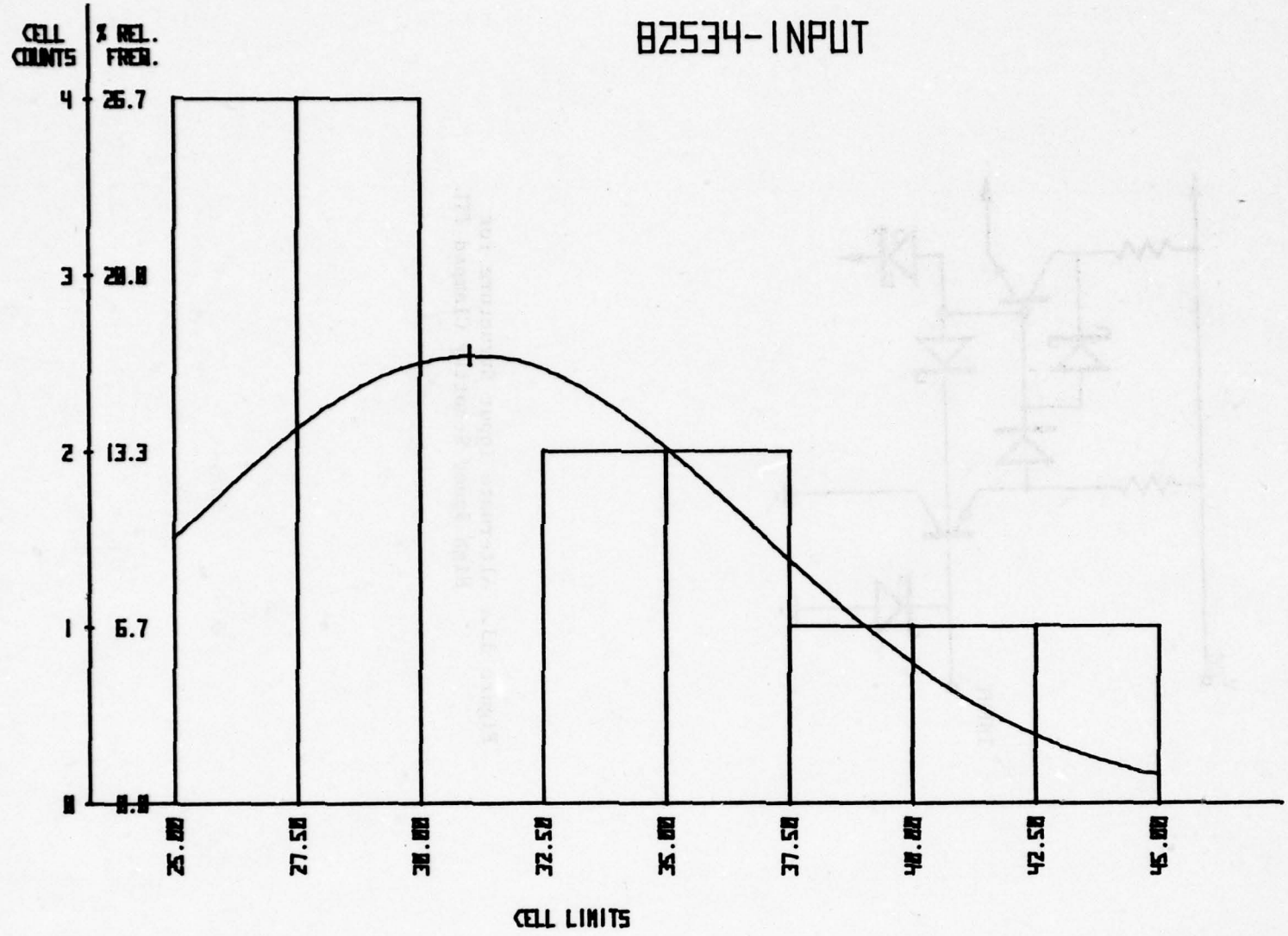


Figure 34. Failure Histogram for 82S34 Input System Transient Tests

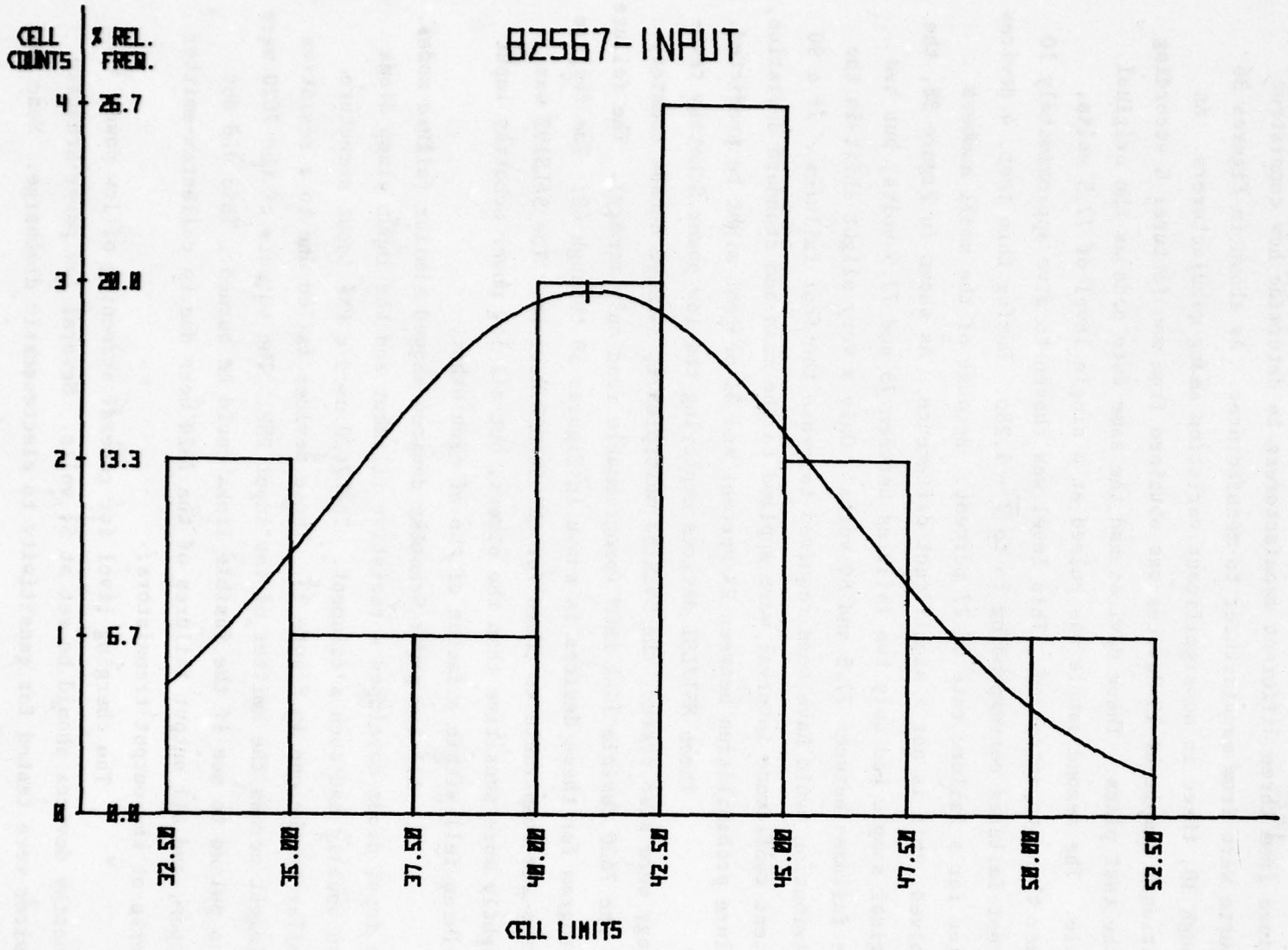


Figure 35. Failure Histogram for 82S67 Input System Transient Tests

obtained from three different manufacturers to determine how consistent products were from manufacturer to manufacturer. As shown in Figures 36 through 38, there is no significant variation among manufacturers. An additional sample of 15 devices was obtained from manufacturer C according to the test plans. These devices had the same date code as the original sample. The second sample was pulsed at a single level of 77.5 volts, rather than step-stressed. This level was chosen to give approximately 10 percent failures corresponding to to $\overline{V} - 1.28\sigma$. During this test, 4 devices failed for a failure rate of 27 percent. Because of the small numbers involved, this is not a significant difference. As shown in Figure 38, the original sample had only two failures between 75 and 77.5 volts, but had five failures between 77.5 and 80 volts. Only a very slight shift in the distribution would have been required to cause the four failures. If a 90 percent confidence interval were applied to the mean and standard deviation, failure probabilities between 27 percent and 41 percent might be predicted.

Three MSI/LSI devices employing the low power Schottky technology were also tested, the 54LS153 multiplexer, 54LS192 decade counter, and the 7620 fusible link PROM (programmable read only memory). The failure histogram for these devices is shown in Figures 39 through 42. The failure levels are comparable to those for the 54LS00 devices. The 54LS192 was slightly more sensitive than the others, but all low power Schottky input failures fell within a factor of two of each other.

All low power Schottky devices showed similar failure modes. The input diode developed a resistive filament and the input clamp diode also usually had such a filament. The 7620 used a PNP input structure similar to the one in Figure 33. These devices failed due to a resistive filament across the emitter of the input PNP. The outputs of the 7620 were also pulsed to see if the fusible links could be burned. This did not happen, and all output failures of the 7620 were due to collector-emitter shorts of the output transistors.

The charging level for general screening of low power Schottky devices should be set at 51 volts. Several low power Schottky devices were tested for sensitivity to electrostatic discharge. None was found.

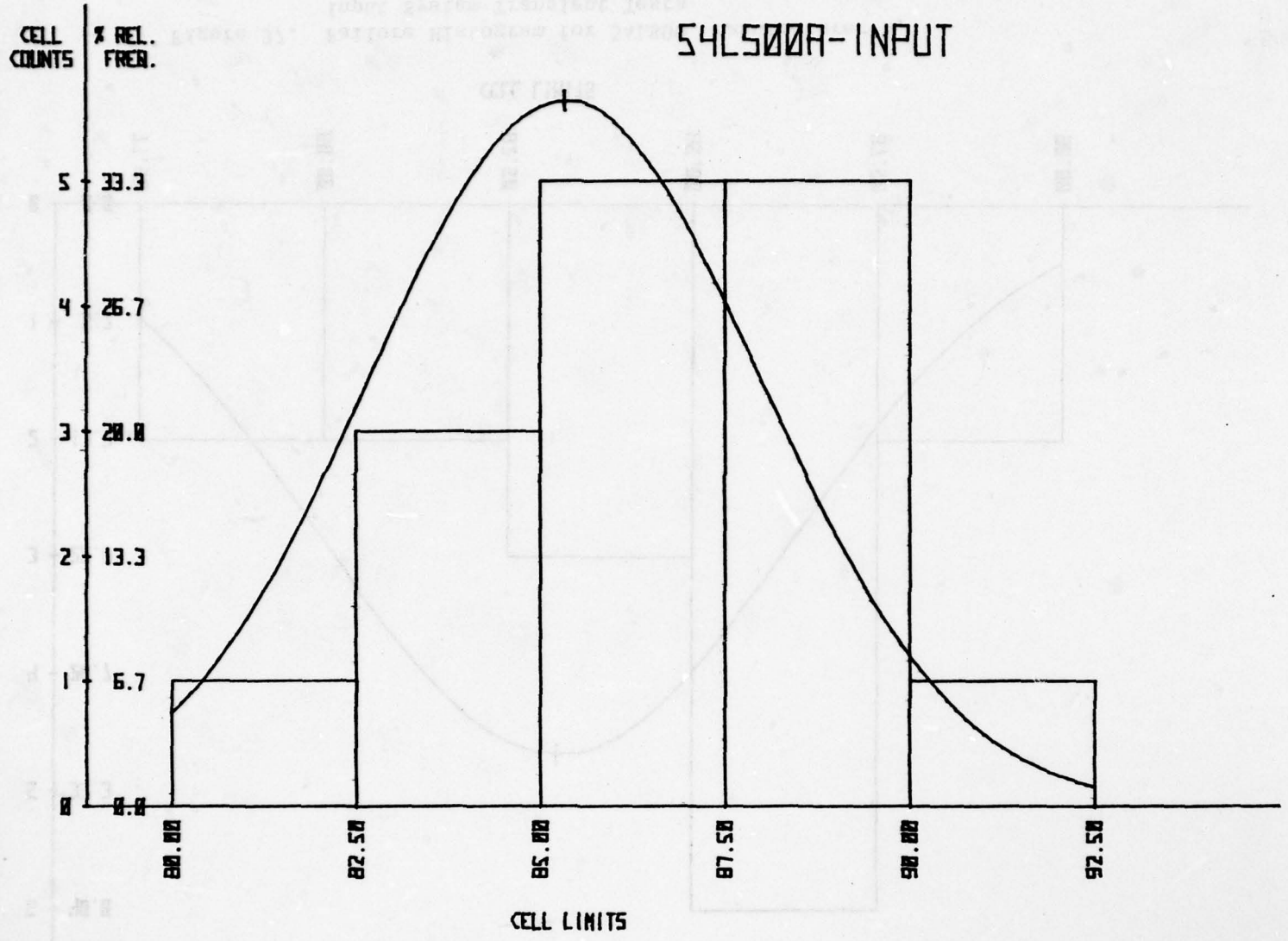


Figure 36. Failure Histogram for 54LS00, Manufacturer A, Input System Transient Tests

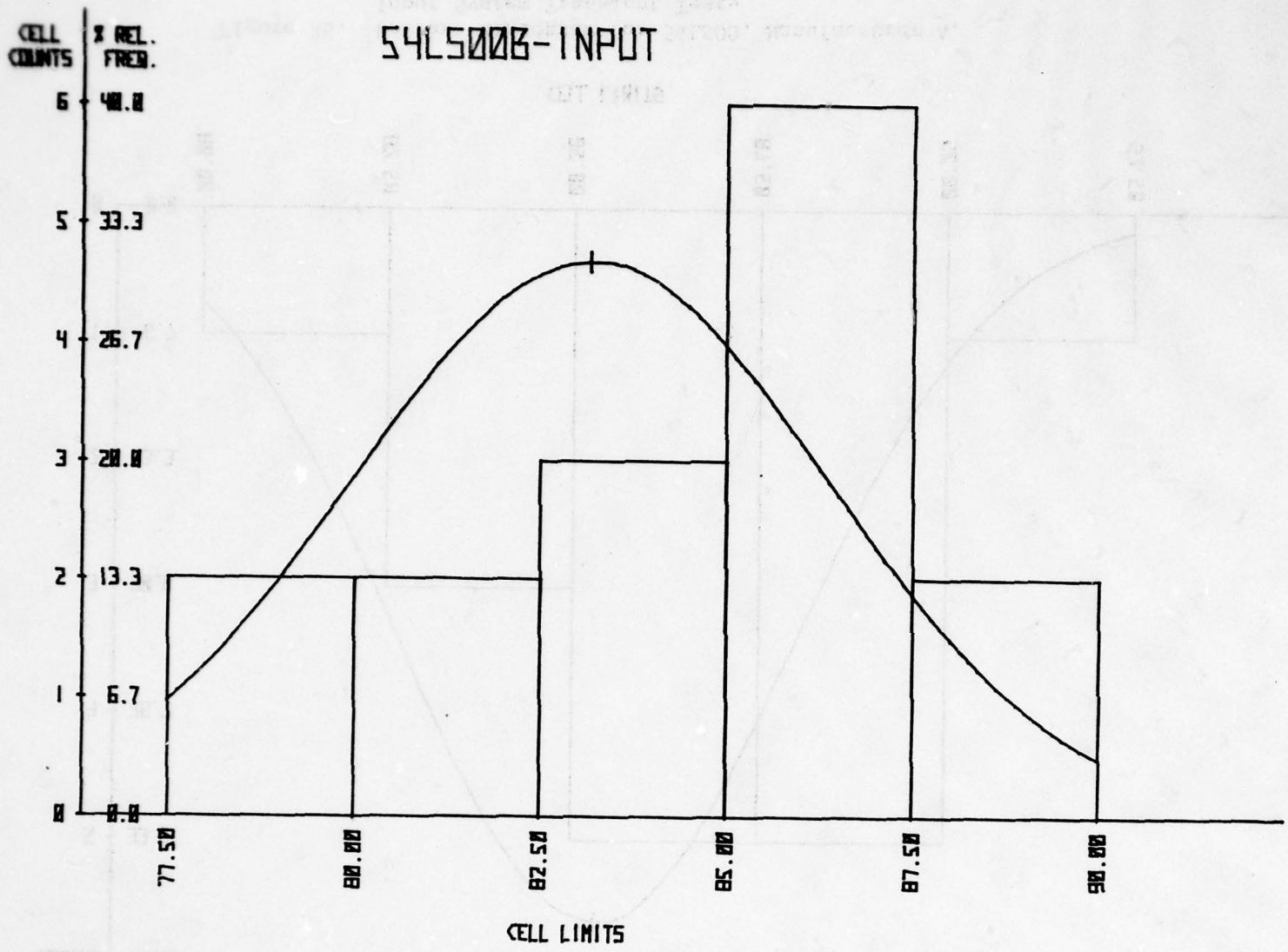


Figure 37. Failure Histogram for 54LS00, Manufacturer B, Input System Transient Tests

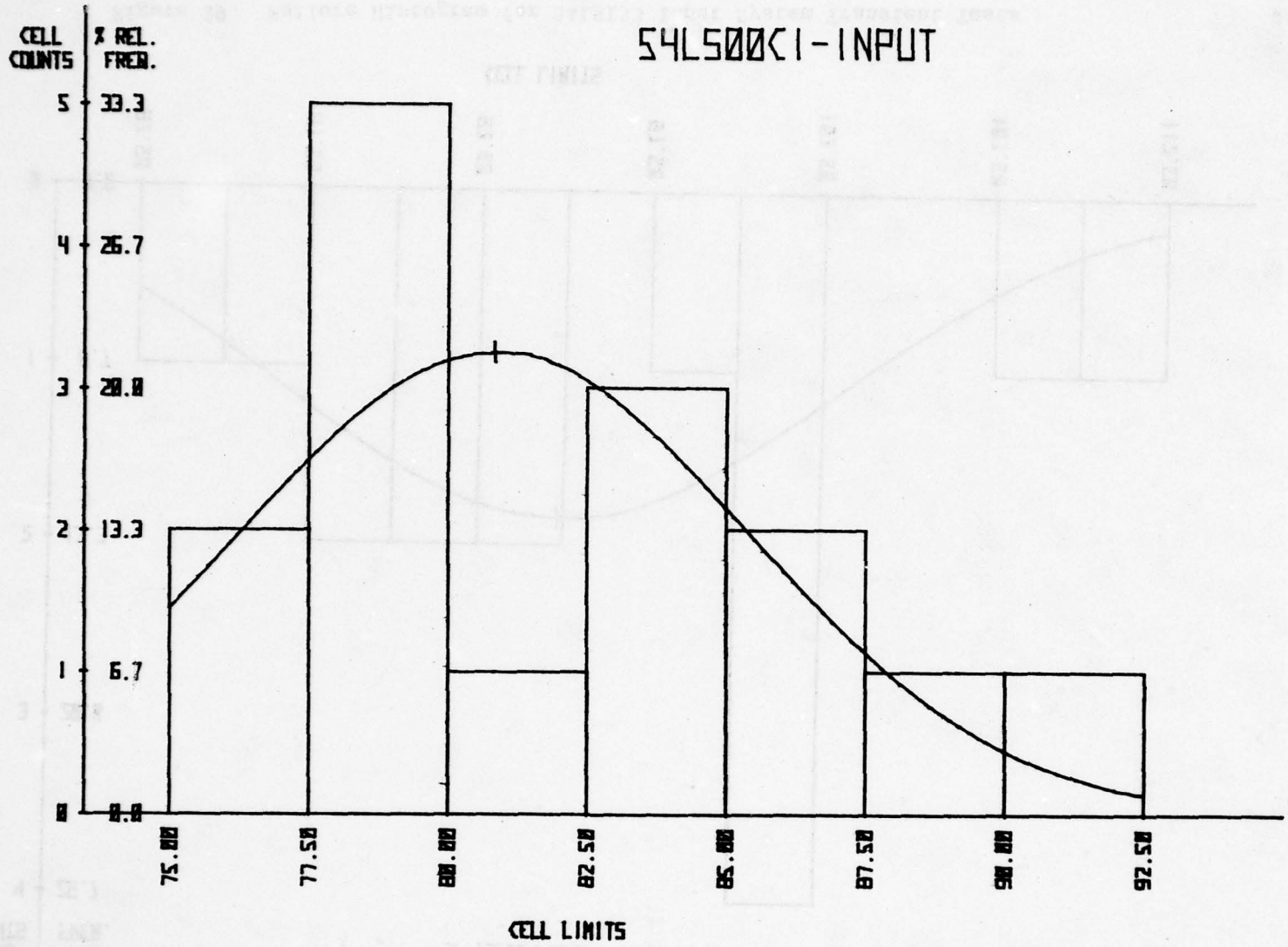


Figure 38. Failure Histogram for 54LS00, Manufacturer C, Input System Transient Tests

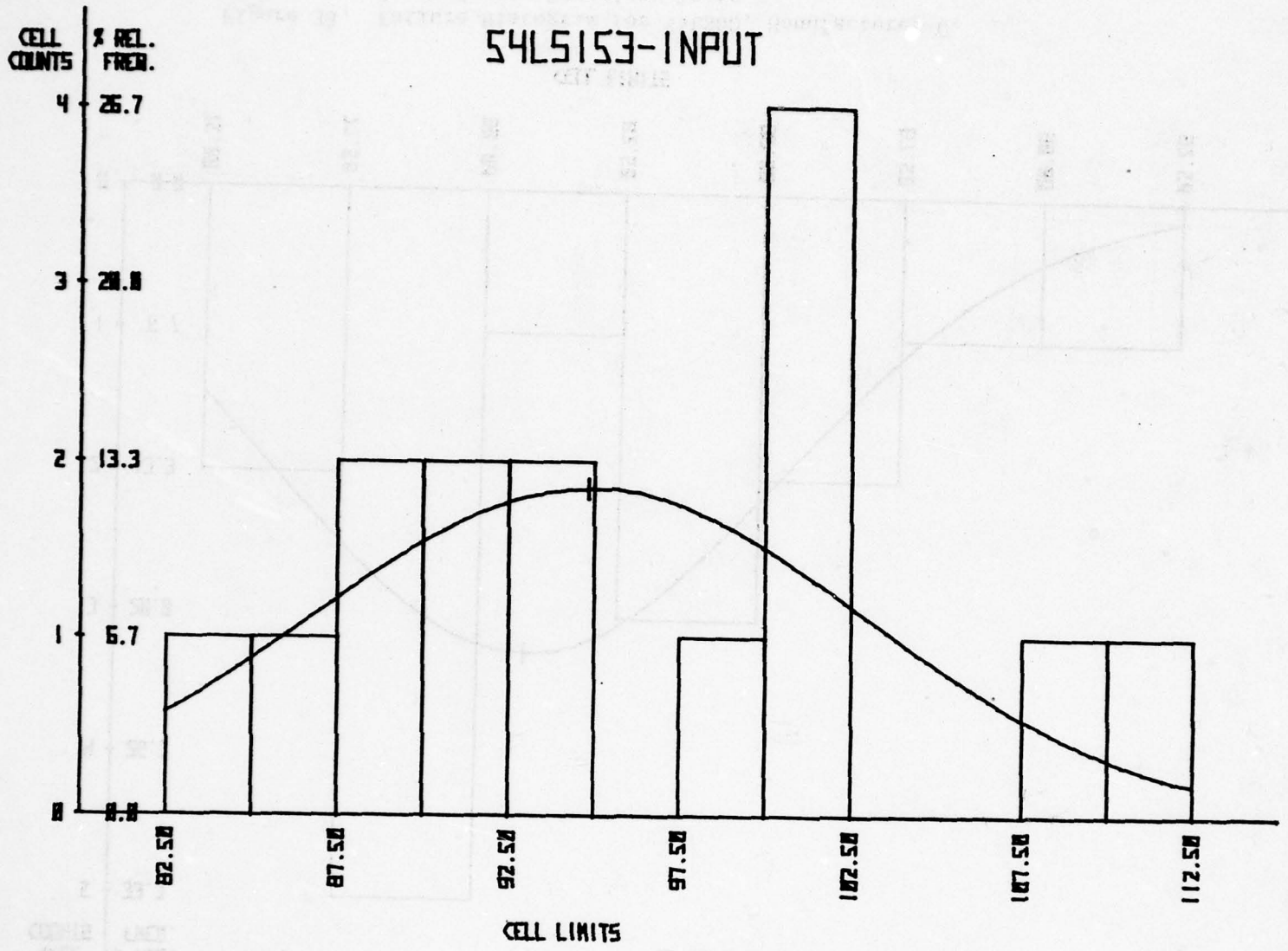


Figure 39. Failure Histogram for 54LS153 Input System Transient Tests

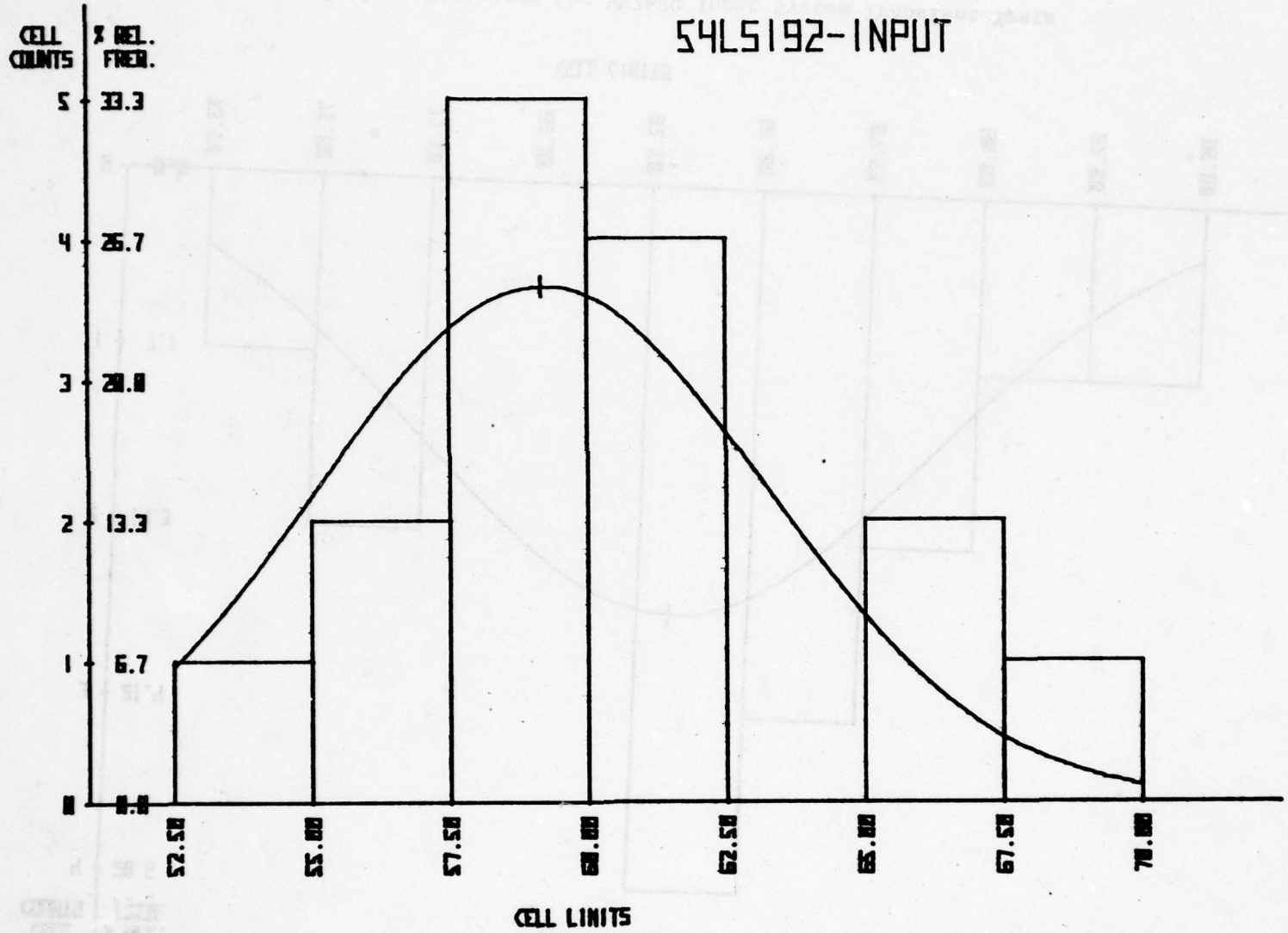


Figure 40. Failure Histogram for 54LS192 Input System Transient Tests

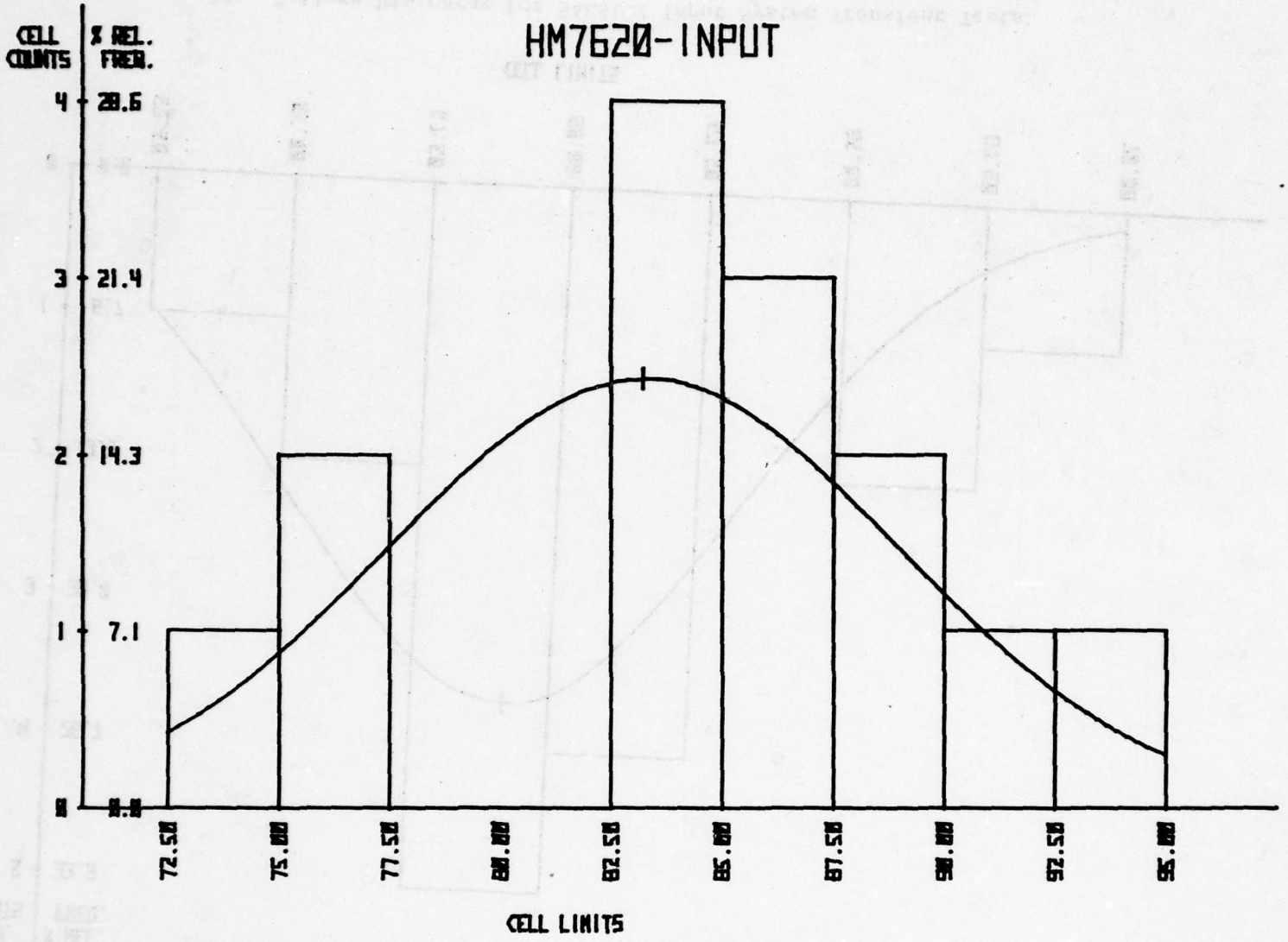


Figure 41. Failure Histogram for HM7620 Input System Transient Tests

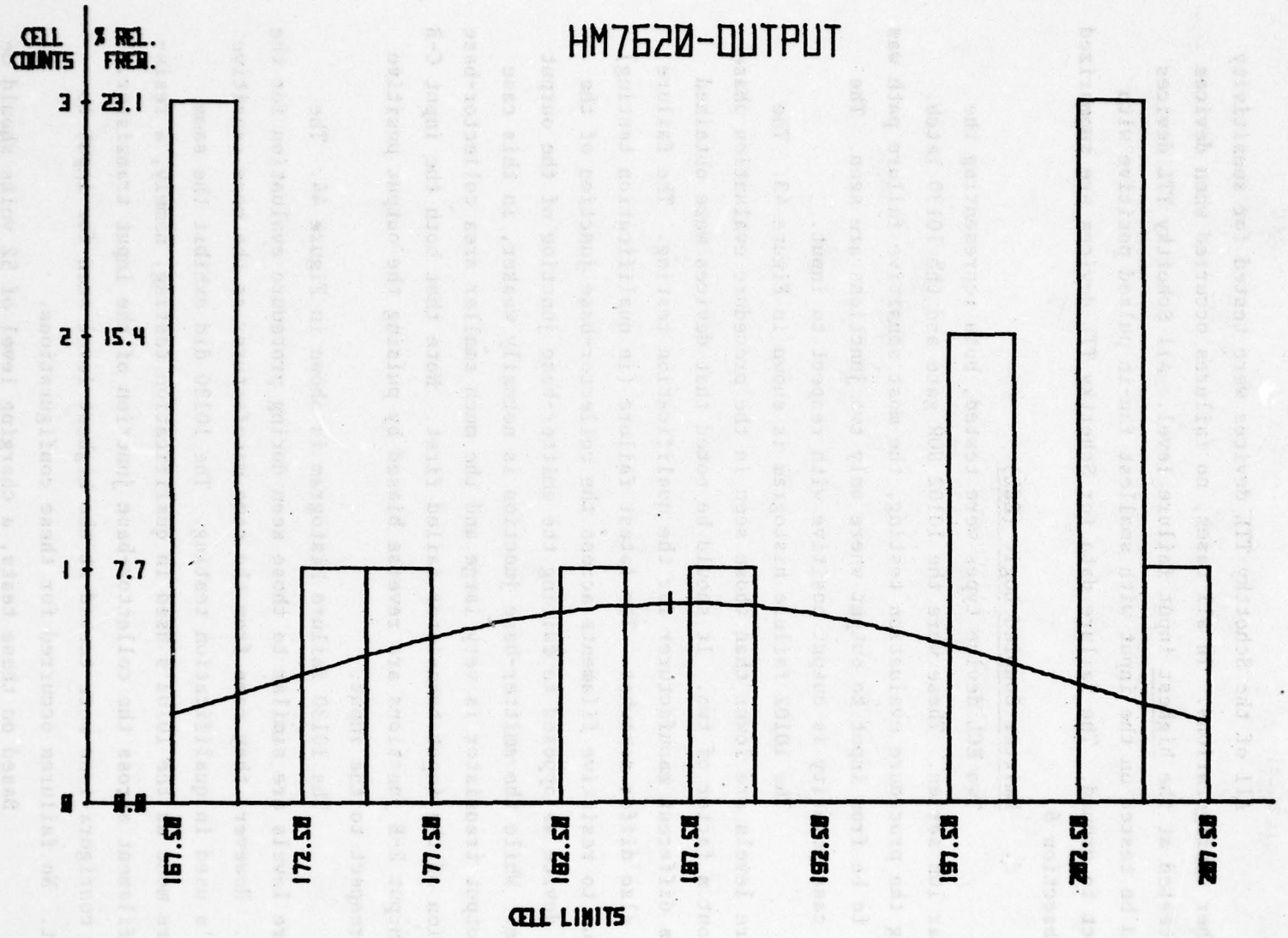


Figure 42. Failure Histogram for HM7620 Output System Transient Tests

All of the Schottky TTL devices were tested for sensitivity in other configurations. In all cases, no failures occurred when devices were tested at the highest input failure level. All Schottky TTL devices should be tested on the input with smallest fan-in pulsed positive with respect to ground. The failure data for Schottky TTL devices are summarized in Subsection 6.

d. Emitter Coupled Logic (ECL)

Two ECL device types were tested, both representing the popular 10K series. These were the 10102 NOR gate and the 10130 latch. During the procedure evaluation testing, the most sensitive failure path was found to be from input to output where only two junctions are seen. The worst case polarity is output positive with respect to input.

The 10102 failure histogram is shown in Figure 43. The failure levels are lower than those seen in the procedure evaluation phase by about a factor of two. It should be noted that devices were obtained from a different manufacturer for the qualification testing. The failure modes also differ somewhat. The latest failure (in qualification testing) was due to resistive filaments across the collector-base junction of the input device as opposed to failing the emitter-base junction of the output device. While the emitter-base junction is normally weaker, in this case the output transistor is very large and the much smaller area collector-base junction of the input transistor failed first. Note that both the input C-B and output E-B junctions are reverse biased by pulsing the output positive with respect to the input.

The 10130 failure histogram is shown in Figure 44. The failure levels are similar to those seen during procedure evaluation for the 10102. However, they came from the same manufacturer as the more sensitive 10102's used in qualification testing. The 10130 did exhibit the same failure mode as the 10102's used in qualification testing, namely, a resistive filament across the collector-base junction of the input transistor. Other configurations were tested at the highest level seen for input-to-output. No failures occurred for these configurations.

Based on these tests, a charging level of 52 volts should be used for screening ECL devices. The worst case configuration is an output pulsed positive with respect to an associated input.

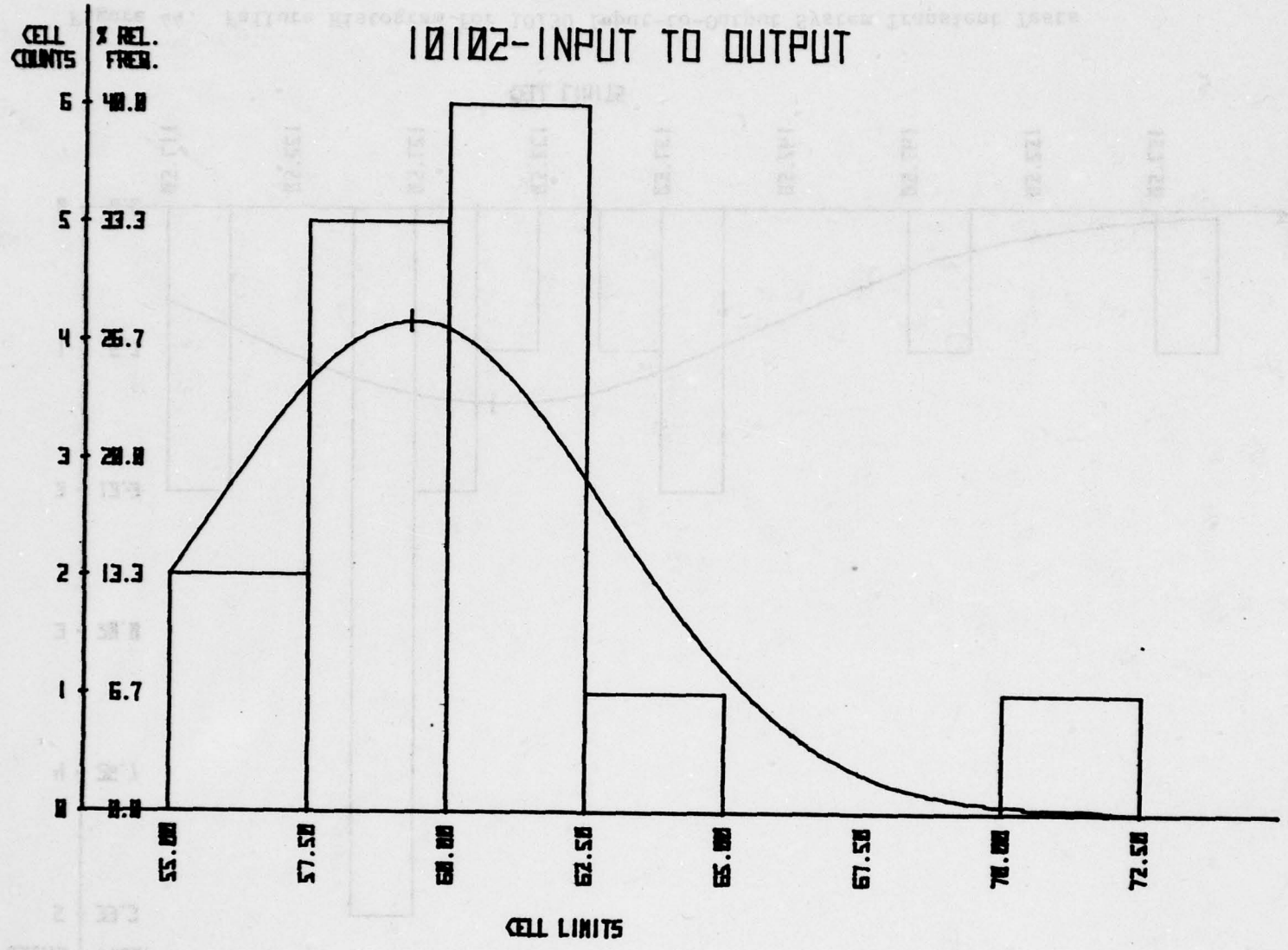


Figure 43. Failure Histogram for 10102 Input-to-Output System Transient Tests

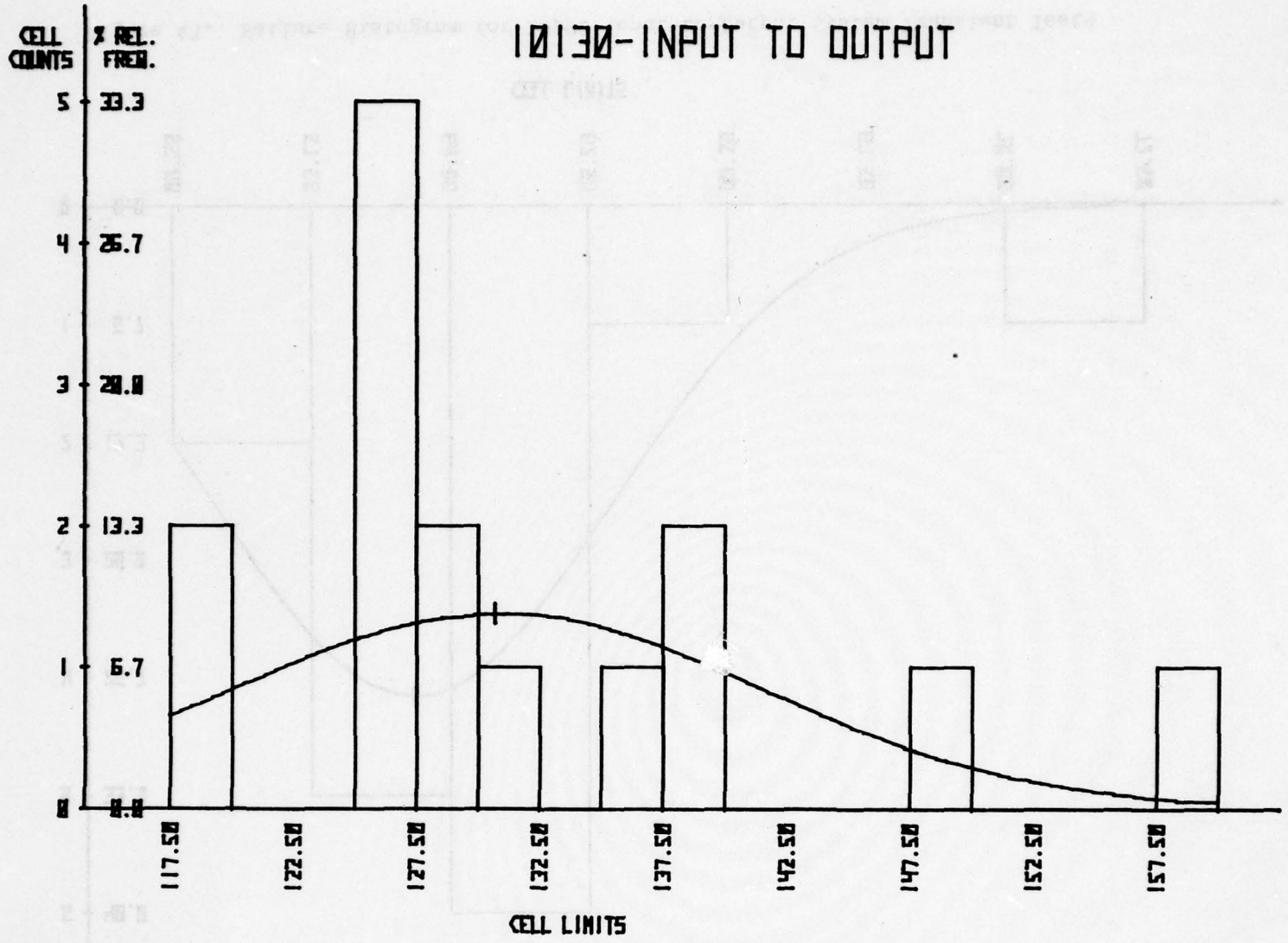


Figure 44. Failure Histogram for 10130 Input-to-Output System Transient Tests

e. Integrated Injection Logic (I^2L)

The I^2L technology is rapidly evolving at this time. There are dozens of variations of the basic configuration. A number of I^2L parts are available commercially, but most are LSI devices. In order to test devices from which meaningful data can be obtained, BDM chose to test I^2L kit parts using first generation I^2L technology. The reader is cautioned that results obtained here may not apply to all I^2L devices. As the technology matures, it may be necessary to categorize I^2L by its principal fabrication features and develop overstress tests for each category.

Three I^2L device types were tested, the XC401 inverter, XC402 NOR gate, and the XC404 D-flip-flop. It was found that there were three configurations with essentially the same failure levels, input (-) to ground, output (+) to ground, and input (-) to injector. The failure histograms for these devices in these configurations are shown in Figures 45 through 52.

Figure 53 shows the basic I^2L configuration. Pulsing the input negative with respect to ground generally results in failure of the merged emitter-base of the NPN, collector-base of the PNP. Pulsing the output positive with respect to ground results in failure of the collector-base junction of the NPN. Note that, since the NPN is actually run in inverted mode, this would normally be considered the emitter-base junction. In the XC402 where each output is connected to two transistors, there was current sharing and the failure levels were above 80 volts.

In the simple inverter structure of the XC401, pulsing injector positive with respect to input resulted in a resistive filament across the merged emitter-base of the NPN, collector-base of the PNP. However, in the more complex structures of the XC402 and XC404, failure occurred in the collector-base junction of the output associated with the pulsed input. The failure path for this mechanism is shown in Figure 54. Note that the failed junction is reverse biased and of small geometry since it would normally be considered an emitter-base junction. This failure path would suggest that the NPN collector-base junction is more sensitive than the merged NPN emitter-base, PNP collector-base. The worst case testing configurations should be set up to test such a path whenever possible.

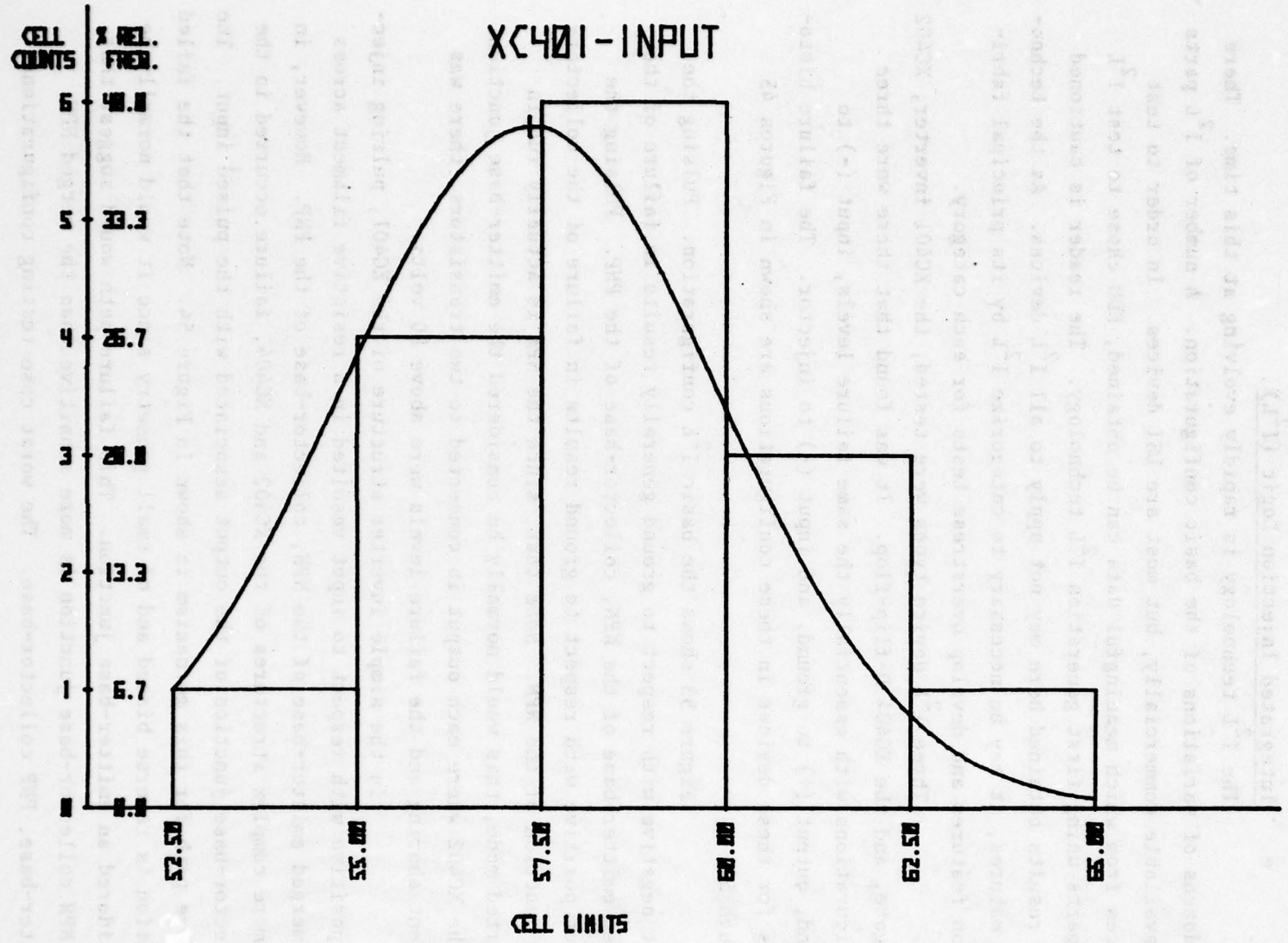


Figure 45. Failure Histogram for XC401 Input System Transient Tests

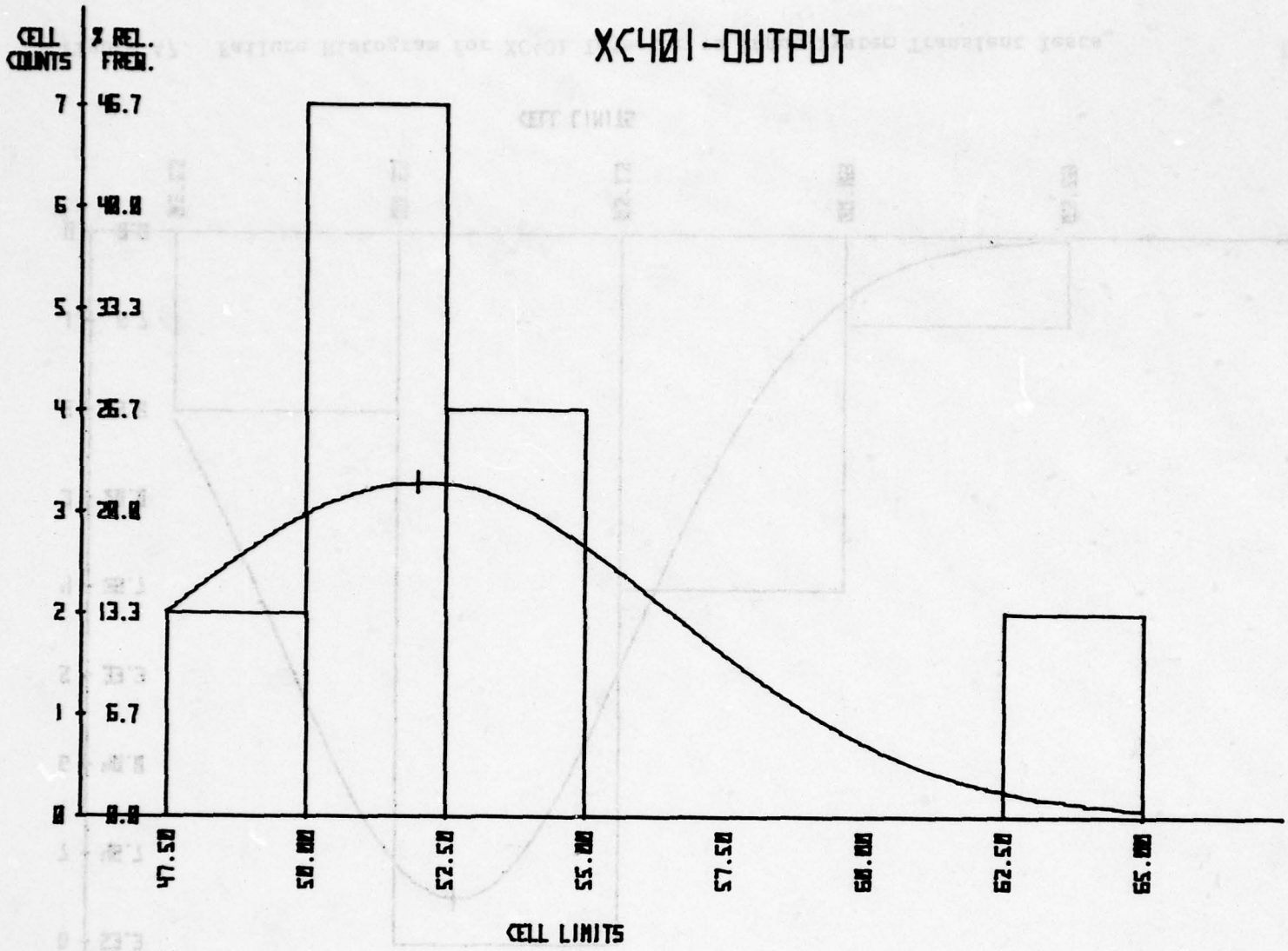


Figure 46. Failure Histogram for XC401 Output System Transient Tests

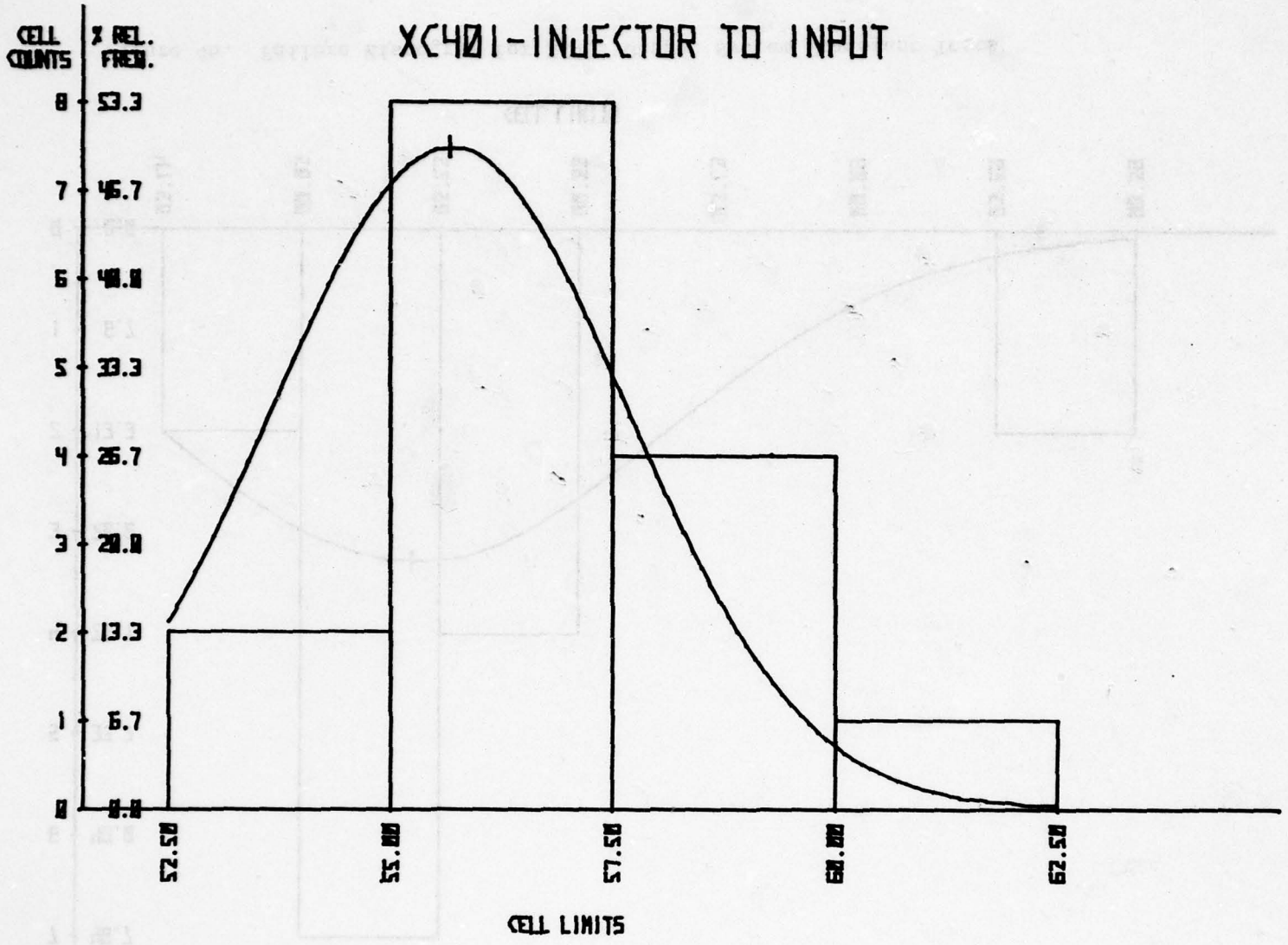


Figure 47. Failure Histogram for XC401 Injector to Input System Transient Tests

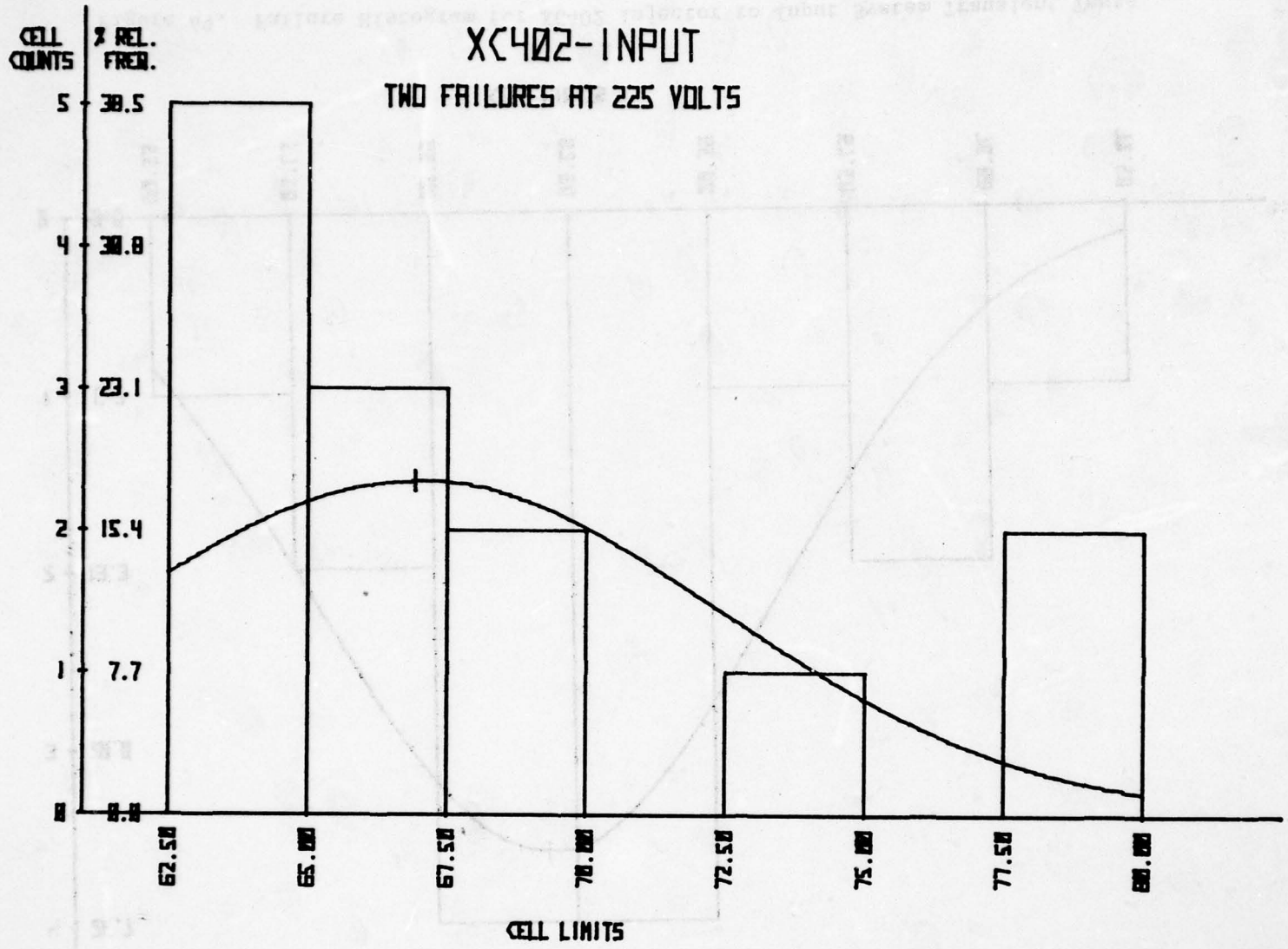


Figure 48. Failure Histogram for XC402 Input System Transient Tests

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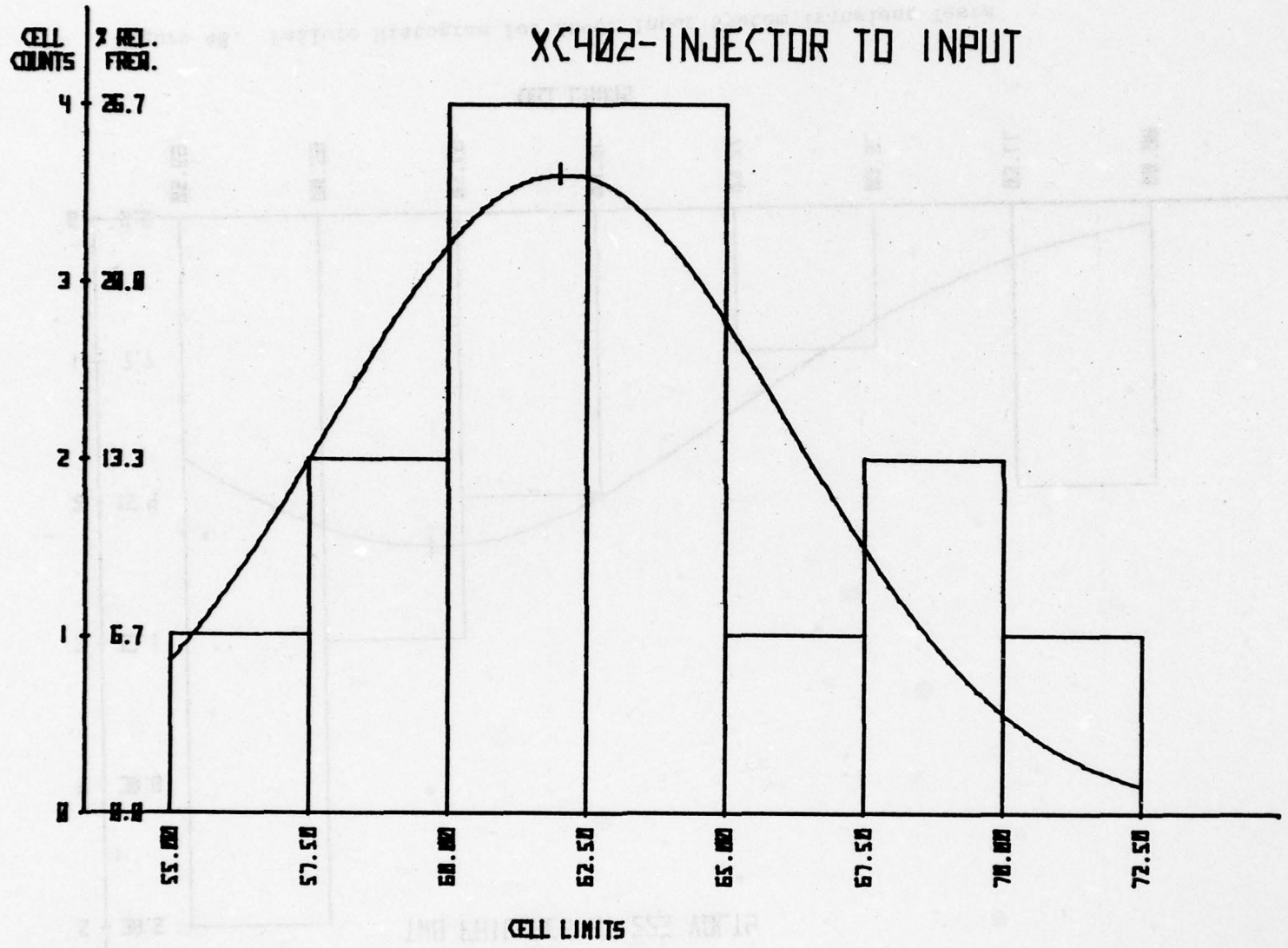


Figure 49. Failure Histogram for XC402 Injector to Input System Transient Tests

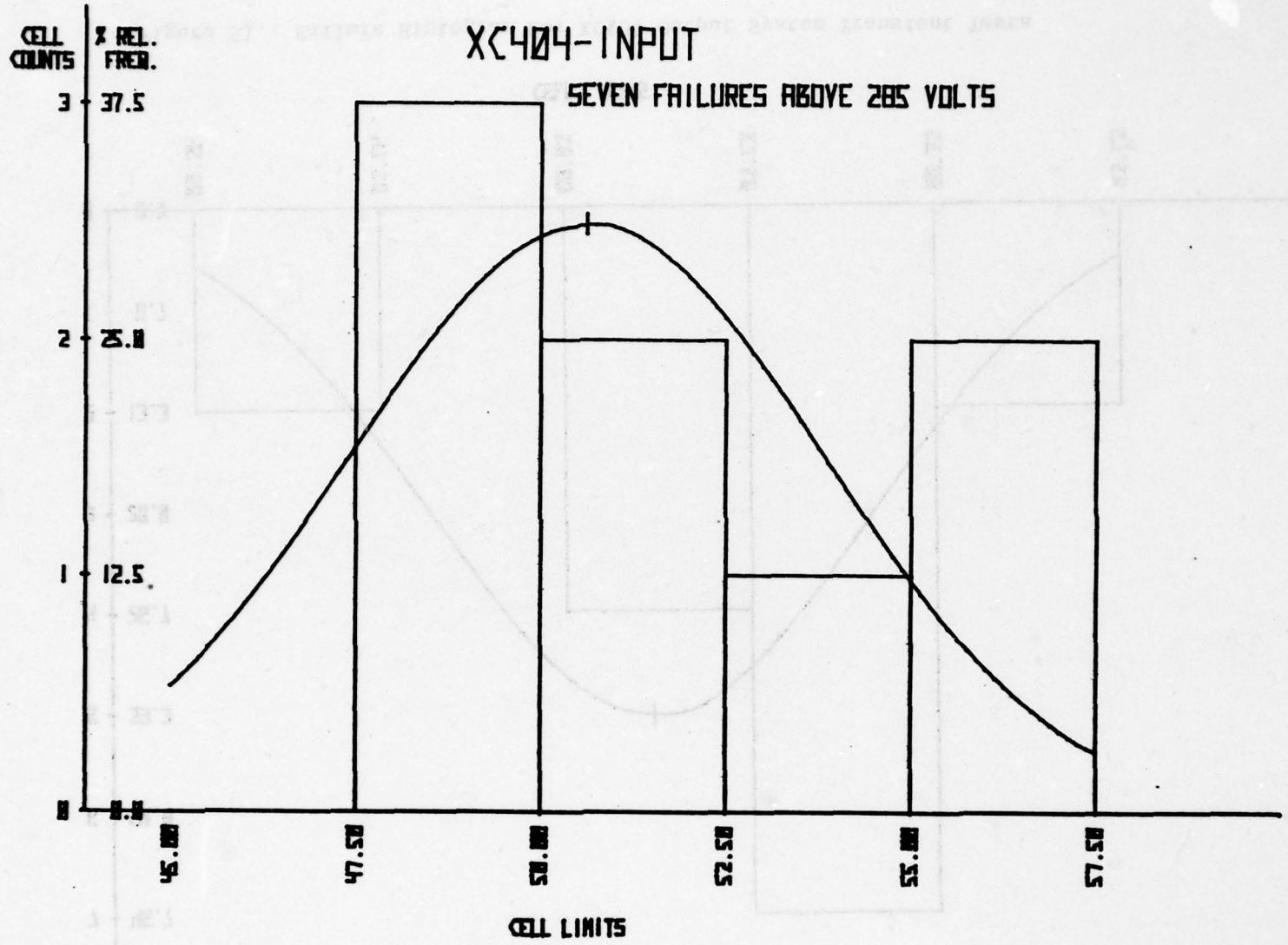


Figure 50. Failure Histogram for XC404 Input System Transient Tests

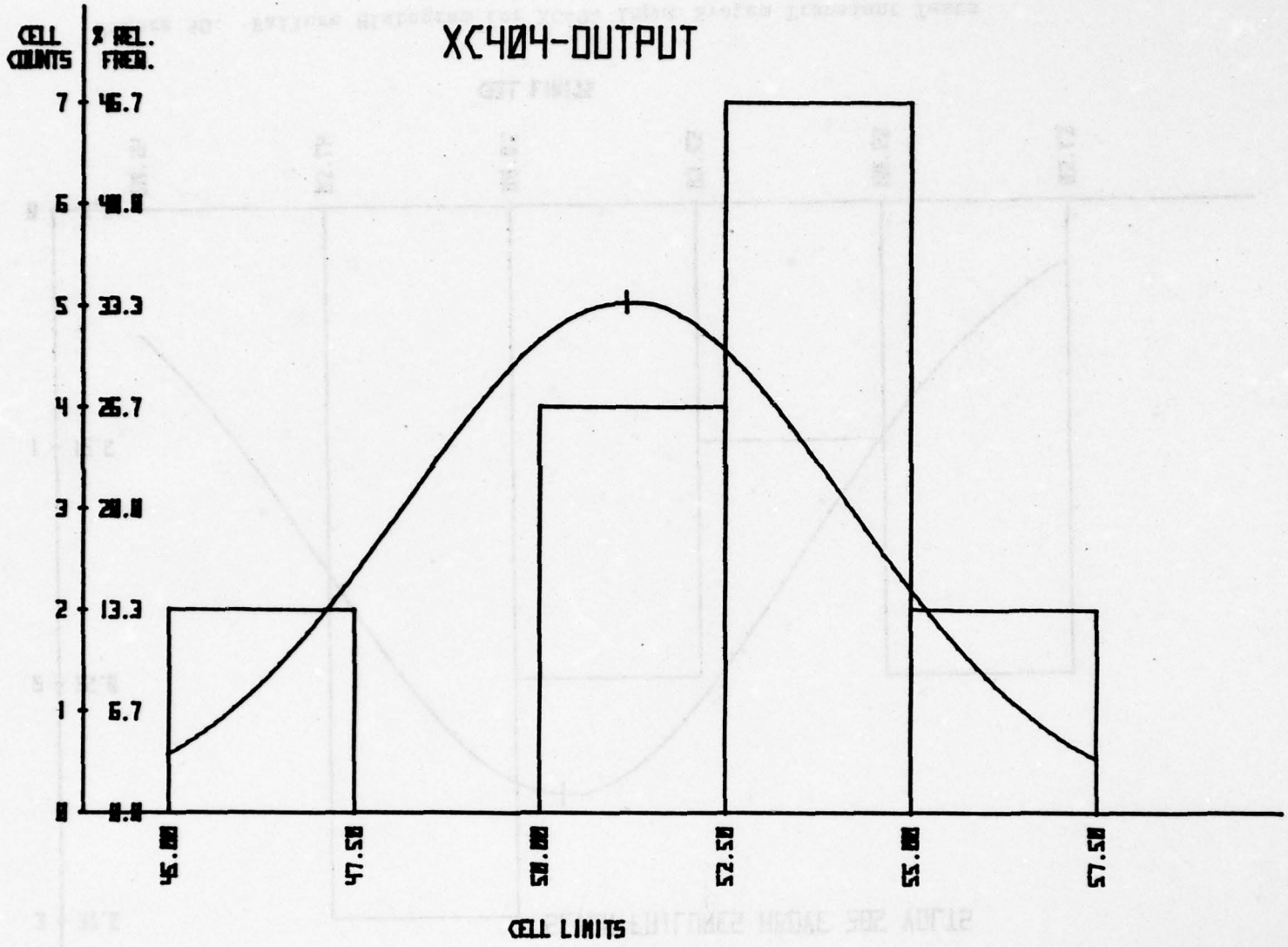


Figure 51. Failure Histogram for XC404 Output System Transient Tests

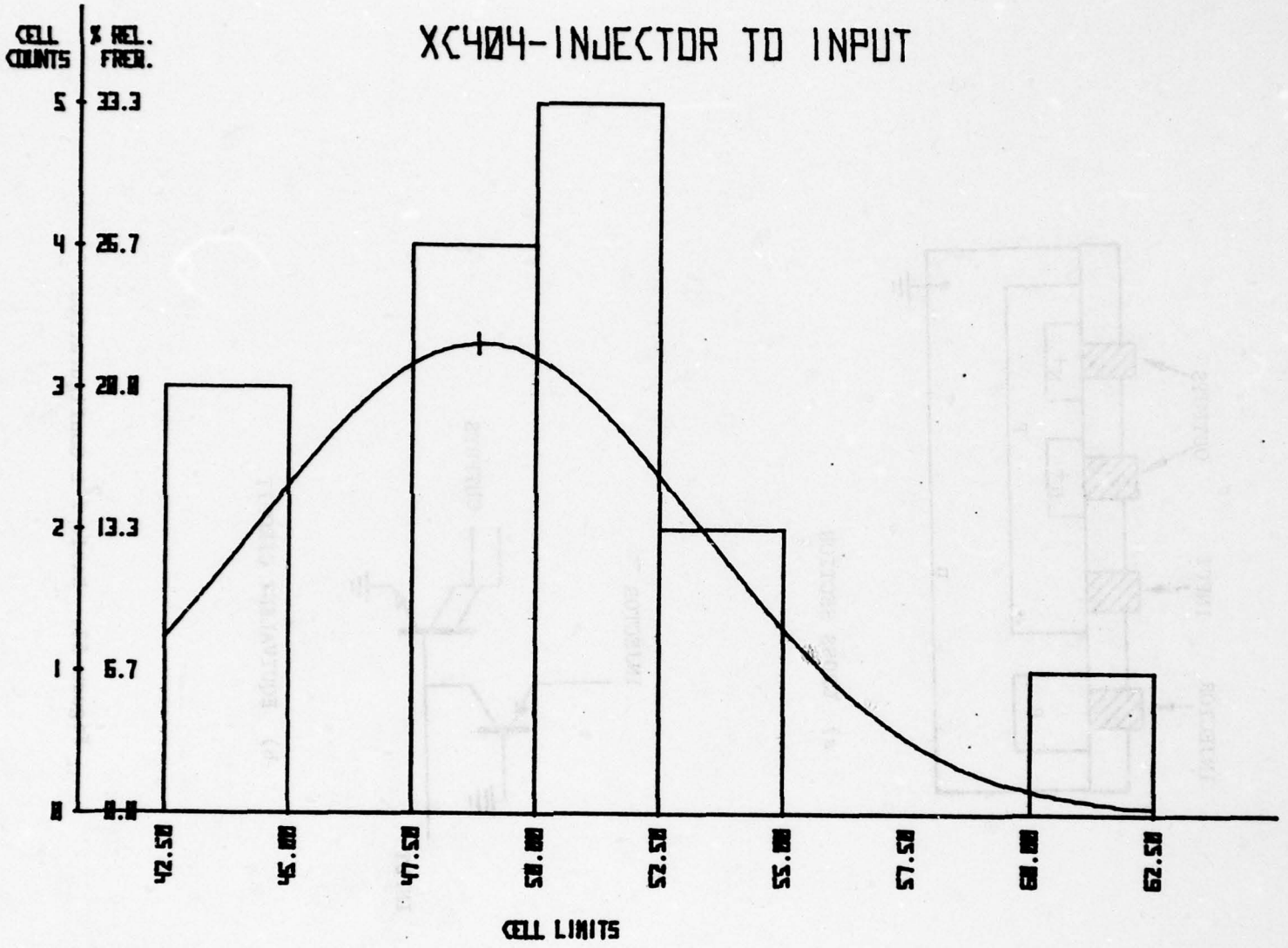
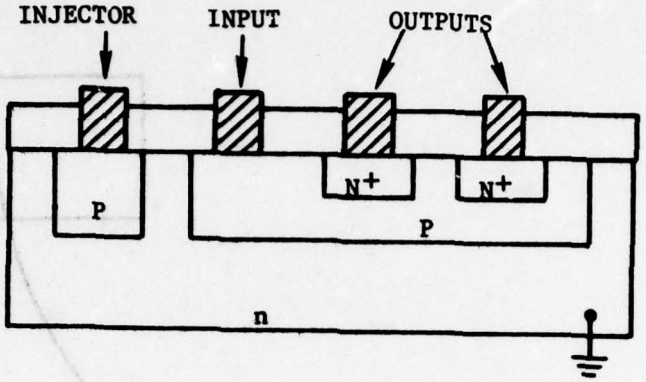
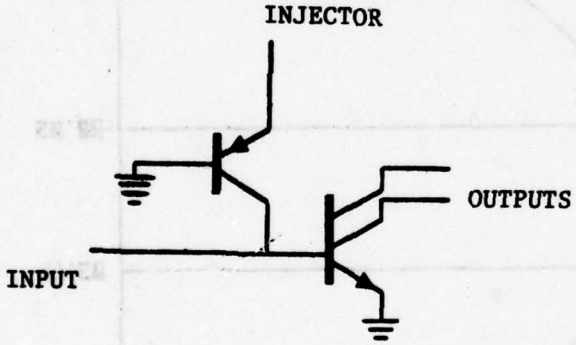


Figure 52. Failure Histogram for XC404 Injector to Input System Transient Tests



a) CROSS SECTION



b) EQUIVALENT CIRCUIT

Figure 53. Basic I^2L Configuration

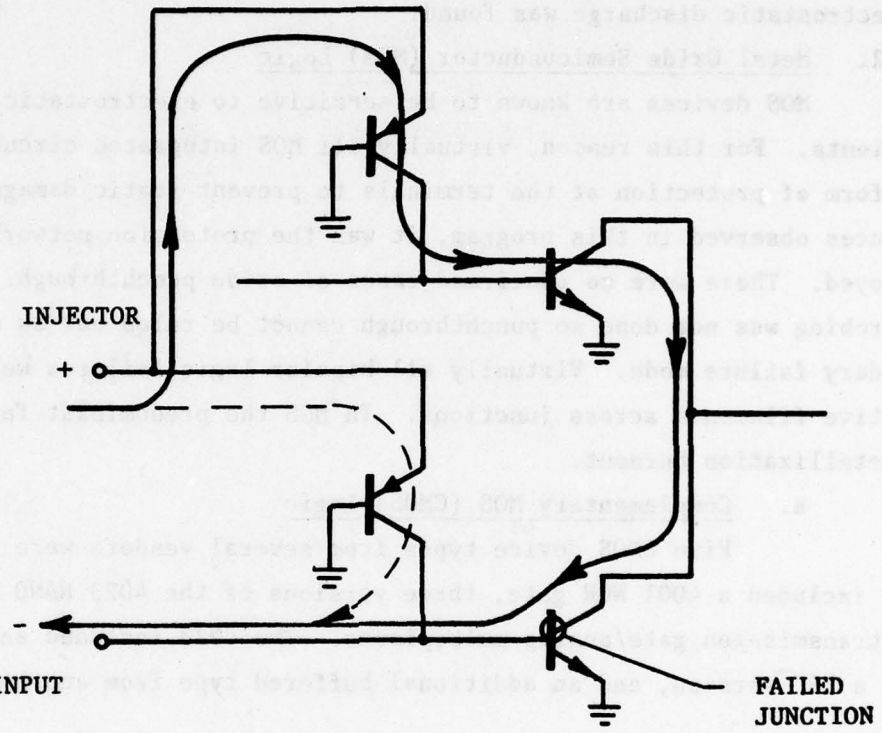


Figure 54. Failure Path for Injector to Input Test of Complex I^2L Devices

The charging voltage should be set to about 40 volts for screening these I^2L devices. However, it is not clear that this screening level will apply to other forms of I^2L. These devices should be considered to be extremely sensitive to electrical overstress damage. No sensitivity to electrostatic discharge was found.

2. Metal Oxide Semiconductor (MOS) Logic

MOS devices are known to be sensitive to electrostatic discharge transients. For this reason, virtually all MOS integrated circuits employ some form of protection at the terminals to prevent static damage. In most instances observed in this program, it was the protection network that was destroyed. There were no confirmed cases of oxide punchthrough. However, die probing was not done so punchthrough cannot be ruled out as a possible secondary failure mode. Virtually all bipolar logic failures were due to resistive filaments across junctions. In MOS the predominant failure mode was metallization burnout.

a. Complementary MOS (CMOS) Logic

Five CMOS device types from several vendors were tested. These included a 4001 NOR gate, three versions of the 4023 NAND gate and a 4066 transmission gate/analog multiplexer. The 4023 included an "A" version, a "B" version, and an additional buffered type from another manufacturer.

The 4001 was tested in three different input configurations using the system transient pulse. As shown in the failure histograms of Figures 55 through 57, the failure distributions were very similar. Failure analysis revealed that in each case a poly-silicon interconnect run had opened up. This poly-silicon run was connected directly to the input pin and served a part of the input protection network because of its relatively high resistance. The failure depended only on the current flowing and was largely independent of failure path.

The device was tested for electrostatic discharge sensitivity in a number of configurations. Of the 15 devices, there was only one failure which occurred at a charging level of 950 volts in the static pulse test. The configuration was between a pair of adjacent inputs. The failure mode was identical to the system transient tests, an open poly-silicon run.

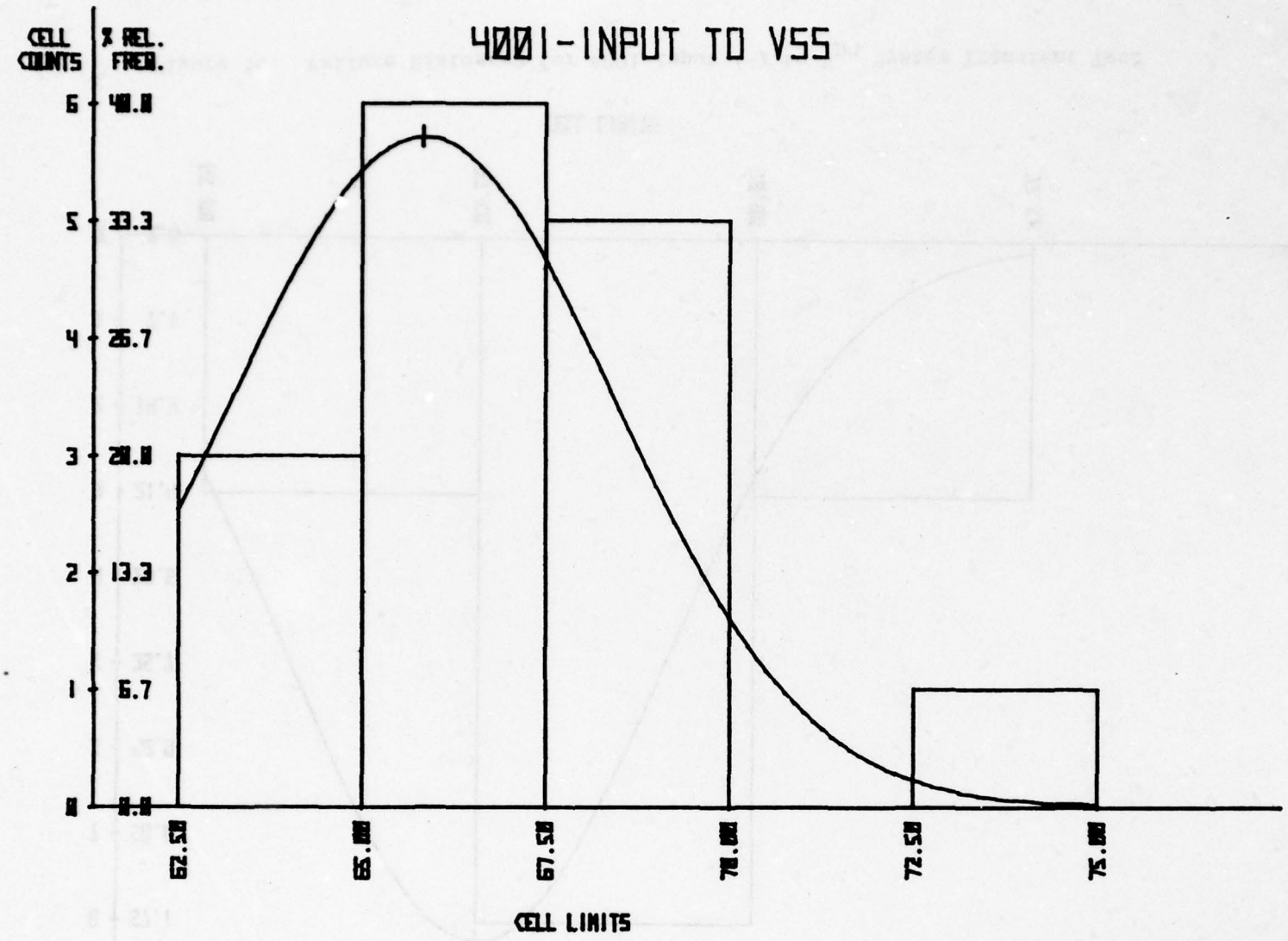


Figure 55. Failure Histogram for 4001 Input to V_{SS} System Transient Test

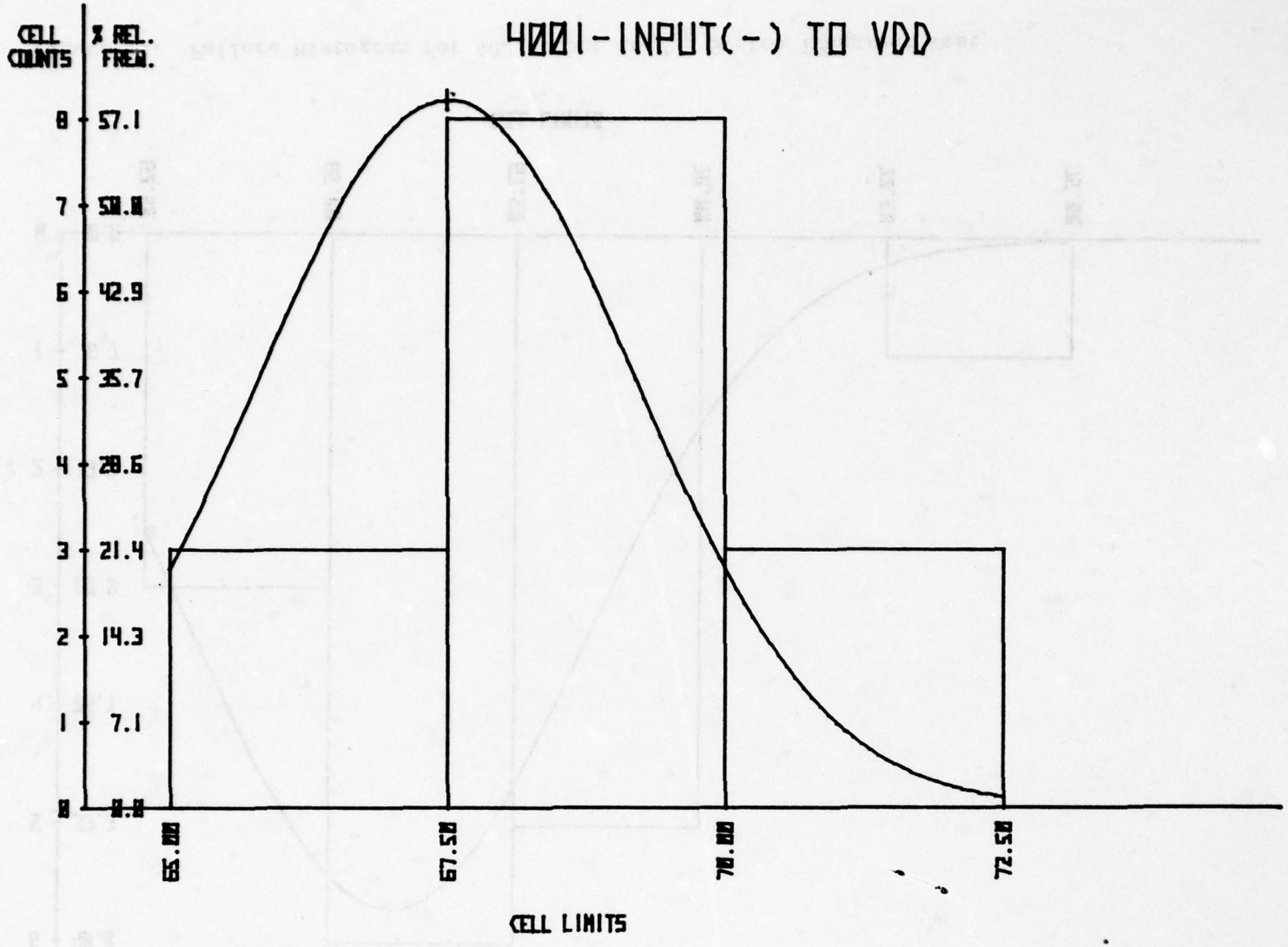


Figure 56. Failure Histogram for 4001 Input (-) to V_{DD} System Transient Test

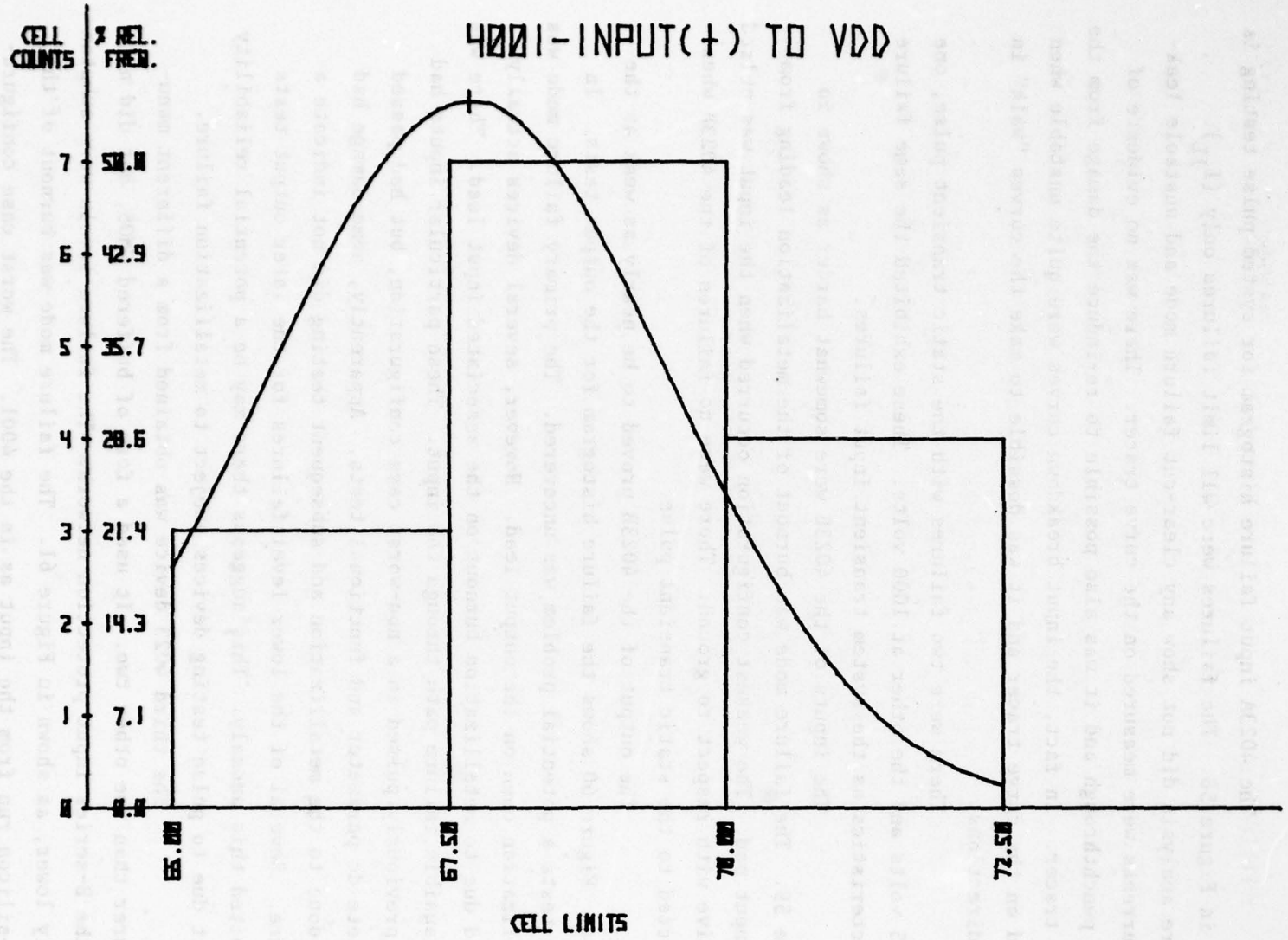


Figure 57. Failure Histogram for 4001 Input (+) to V_{DD} System Transient Test

The 4023A input failure histogram for system pulse testing is shown in Figure 58. The failures were all limit failures only (I_{IL}). Failure analysis did not show any clear-cut failure mode and unstable leakage currents were measured on the curve tracer. There was no evidence of oxide punchthrough and it was also possible to re-induce the damage from the curve tracer. In fact, the input breakdown curves were quite unstable when viewed on the curve tracer and it was possible to make the curves "walk" in both directions.

There were two failures with the static transient pulse, one at 975 volts and the other at 1000 volts. These exhibited the same failure characteristics as the system transient input failures.

The inputs of the 4023B were somewhat harder as shown in Figure 59. The failure mode was burnout of the metalization leading from the input pad. The weakest configuration occurred when the input was pulsed negative with respect to ground. There were no failures of the 4023B when subjected to the static transient pulse.

The output of the 4023B proved to be nearly as weak as the inputs. Figure 60 shows the failure histogram for the output tests. In these tests a potential problem was uncovered. The primary failure mode was metallization open on the output lead. However, several devices actually failed due to metallization burnout on the associated input lead. There was no plausible failure path through the input. These particular inputs had been previously pulsed in a non-worst case configuration, but had passed complete dc parameter and functional tests. Apparently, some damage had been done to the metallization and subsequent testing did not indicate a failure. Several of the lower level failures for the later output tests exhibited this anomaly. This suggests there may be a potential reliability impact due to pulse testing devices subject to metallization failure.

The third 4023 device was obtained from a different manufacturer than the other two. It used a form of buffered CMOS, but did not use the B-series input protection network. The failure levels were substantially lower, as shown in Figure 61. The failure mode was burnout of the poly-silicon run from the input as in the 4001. The worst case configuration was the input pulsed negative with respect to ground. Failures to the static transient pulse were seen in two configurations. There were three

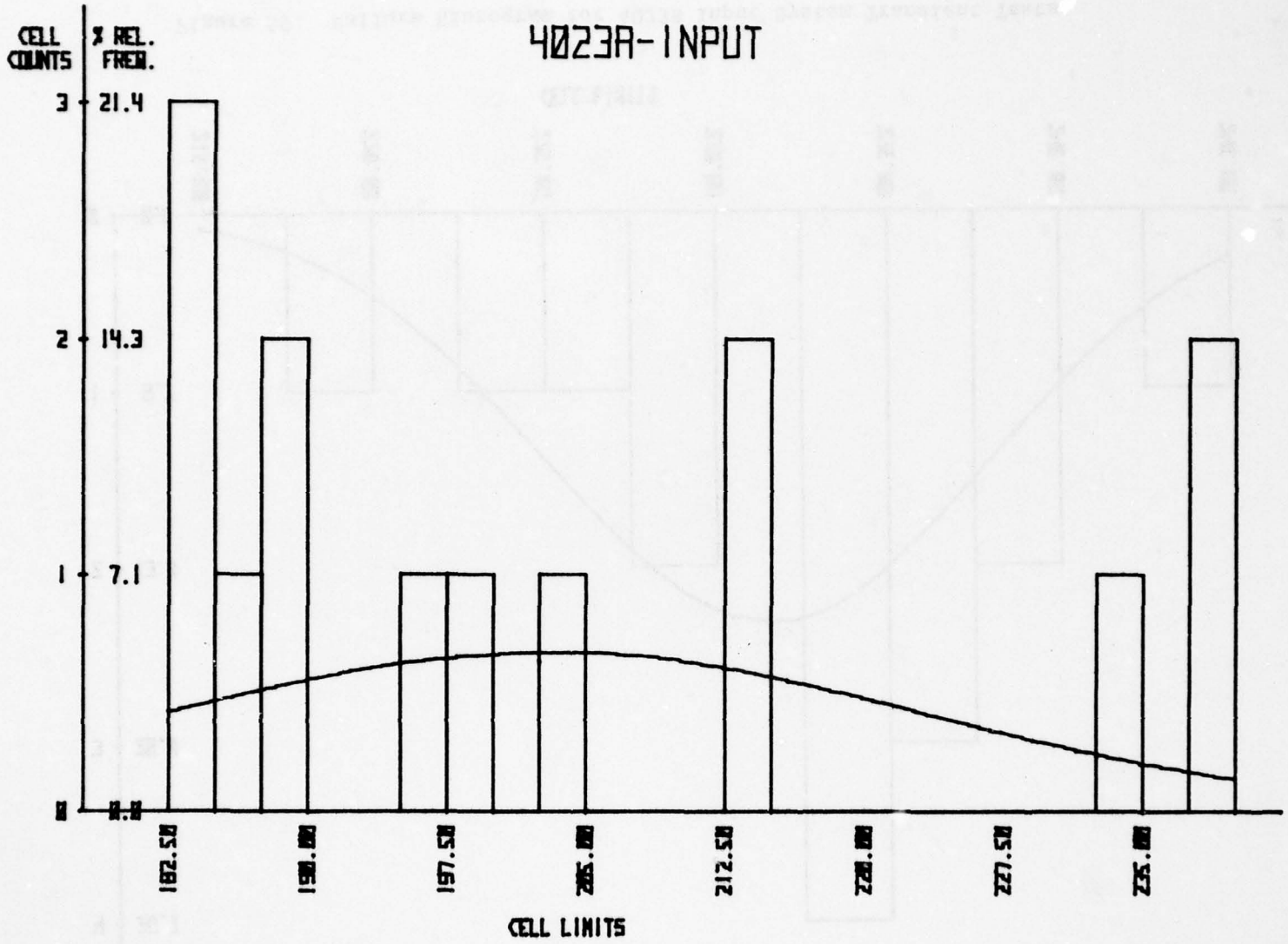


Figure 58. Failure Histogram for 4023A Input System Transient Tests

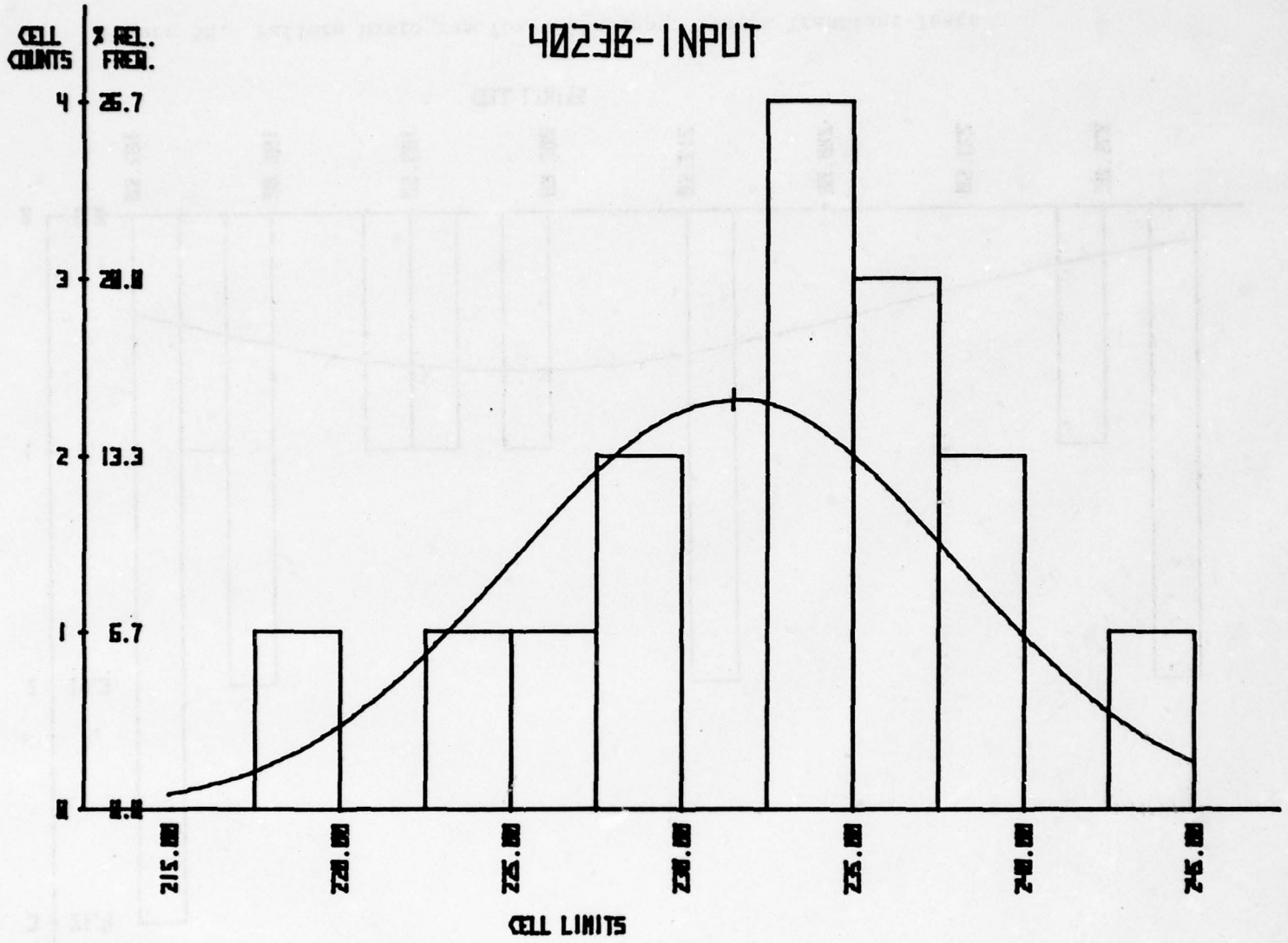


Figure 59. Failure Histogram for 4023B Input System Transient Tests

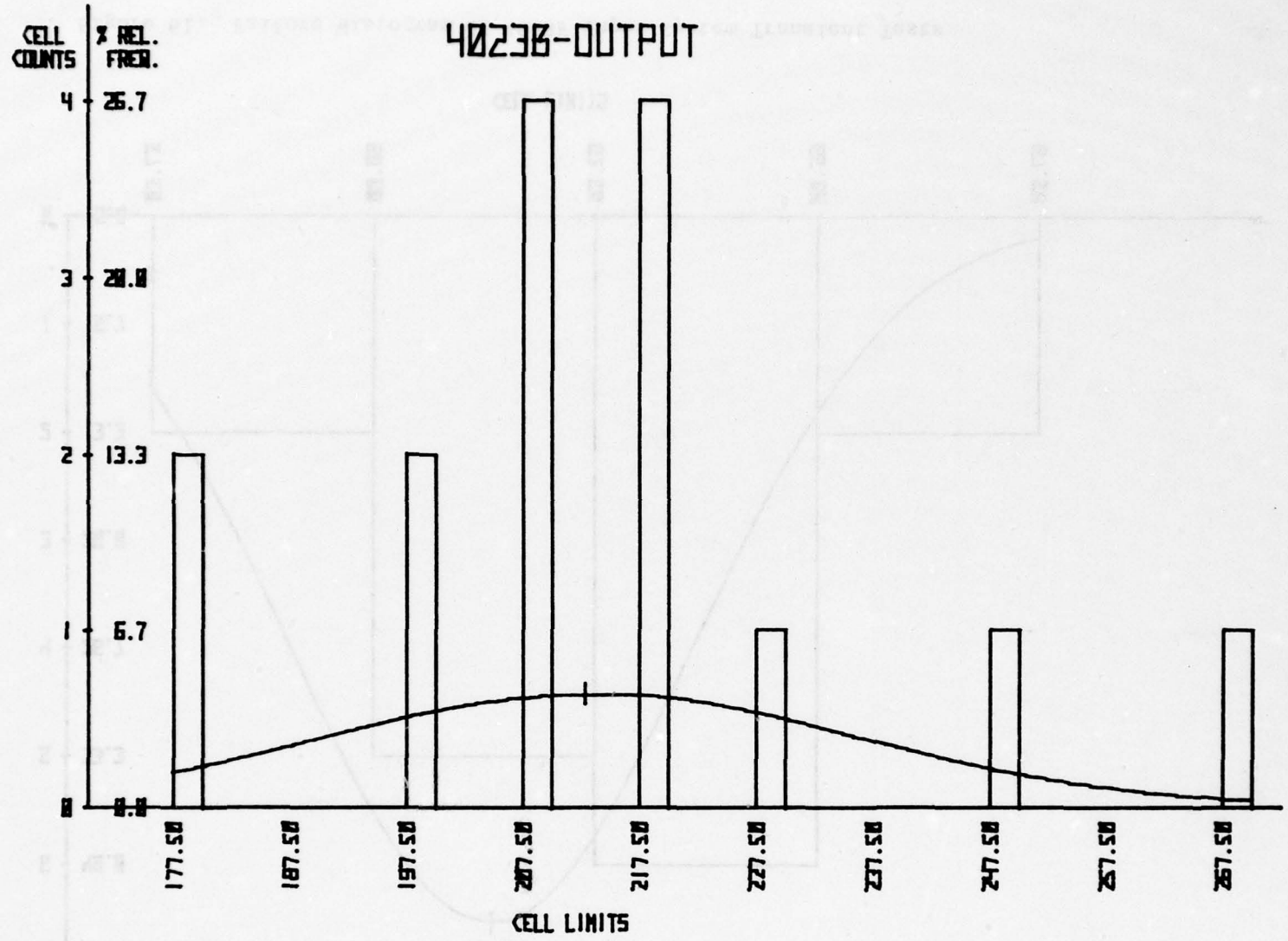


Figure 60. Failure Histogram for 4023B Output System Transient Tests

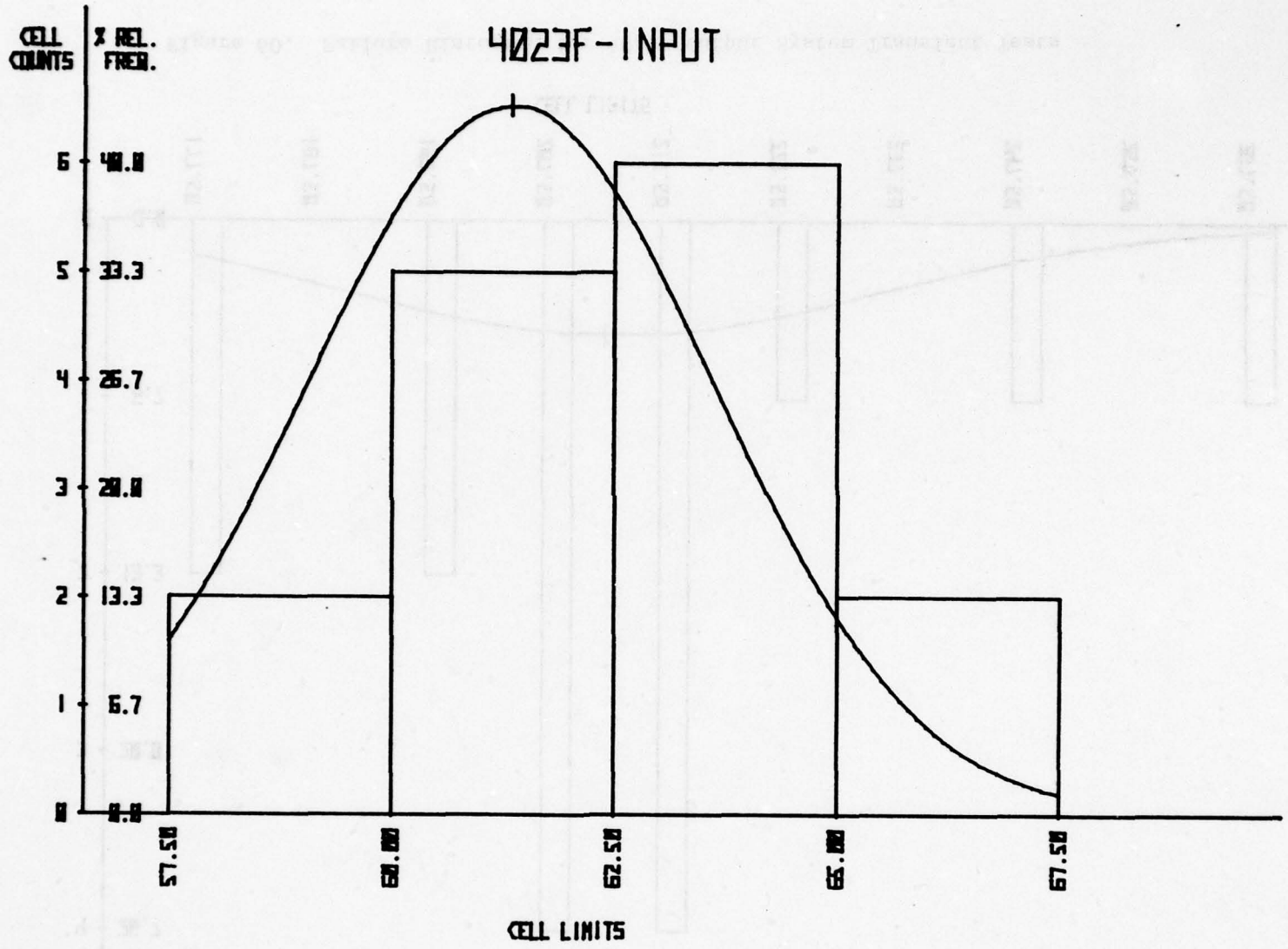


Figure 61. Failure Histogram of 4023F Input System Transient Tests

failures at 1000 volts when pulsed with the input negative with respect to ground. There were two more failures, one at 950 and the other at 1000 volts when pulsed input negative with respect output. The failure mode was the same as for the system transient tests, open circuit of the poly-silicon run leading to the input pad.

The 4066 was tested across the analog switch. The failure histogram is presented in Figure 62. The failure mode was metallization burnout of the lead coming from the switch. No static sensitivity was seen across the switch. Generally, the worst case configuration appears to be the input pulsed negative with respect to V_{SS}. The charging voltage should be set at 55 volts for screening CMOS to the system transient and at 1000 volts for screening to the static transient. These results may apply only to CMOS microcircuits with poly-silicon resistor elements.

b. N-Channel MOS (NMOS)

Only one NMOS device was tested, the 2102 RAM (Random Access Memory). There were no static transient failures on this device. The failure histogram for the system transient failures is shown in Figure 63. The weakest configuration is the input pulsed positive with respect to ground. All of the failures exceeded limits (I_{IH}) on the input pin. The input failure mode appears to be a resistive filament across the lower input protection diode. It was possible to simulate the failures on the curve tracer and to watch the devices go into second breakdown and fail at voltages below 50 volts.

The charging voltage should be set at 32 volts for screening NMOS inputs to the system transient. The charging voltage should be set to 1000 volts for screening NMOS to the static transients. These devices should be considered extremely sensitive to electrical overstress and should be handled accordingly.

3. Linear Devices

Previously, all analog circuits had been lumped together as linears. For this program, two new categories have been created: power and interface. Only low level circuits such as operational amplifiers (op amp) and voltage comparators are now considered to be in the linear category.

Four linear circuits were tested, the 108 super-beta op amp, the 124 quad op amp, the 139 quad voltage comparator, and the LF156 JFET input

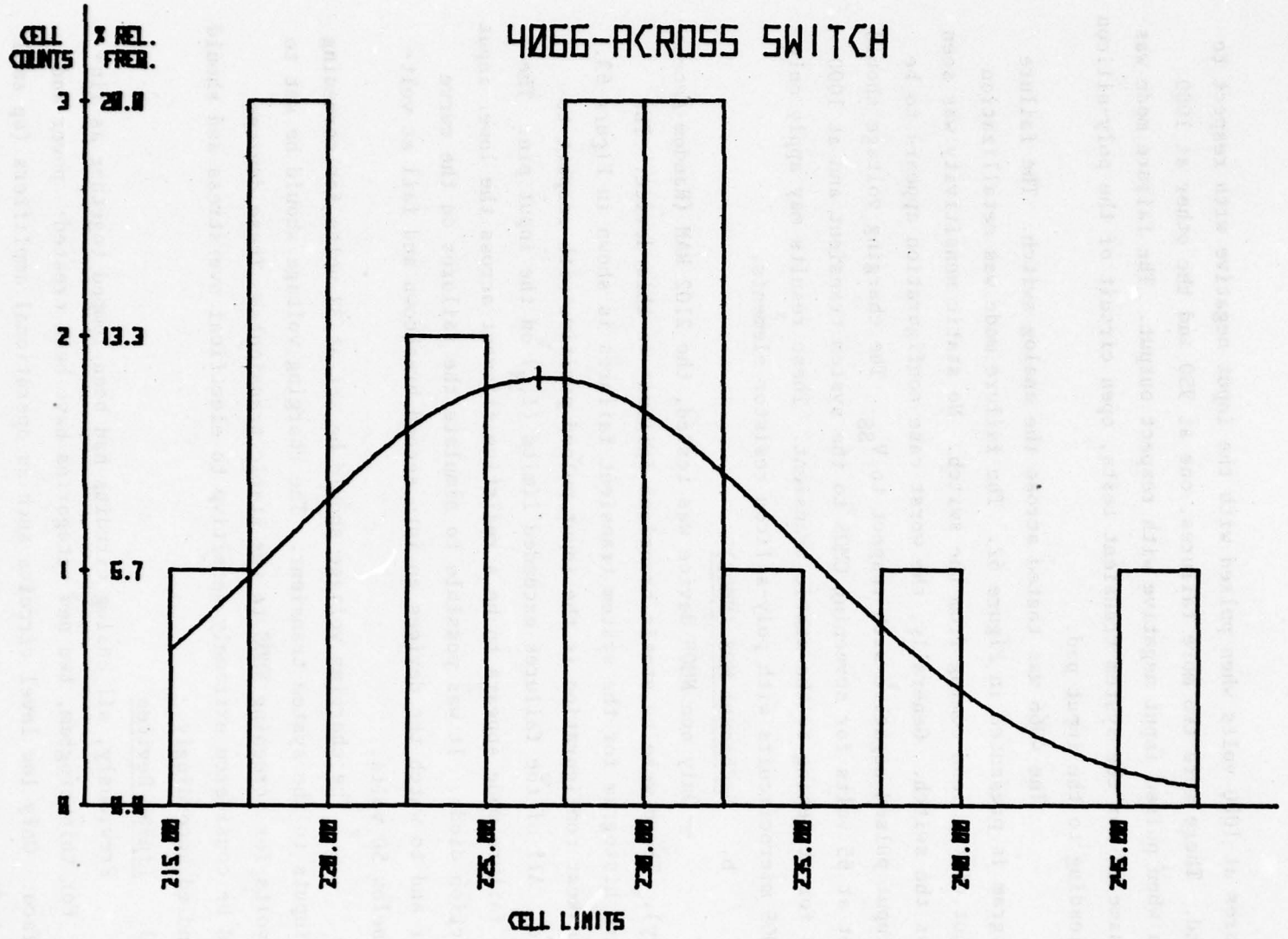


Figure 62. Failure Histogram of the 4066 Tested Across the Switch With the System Transient Pulse

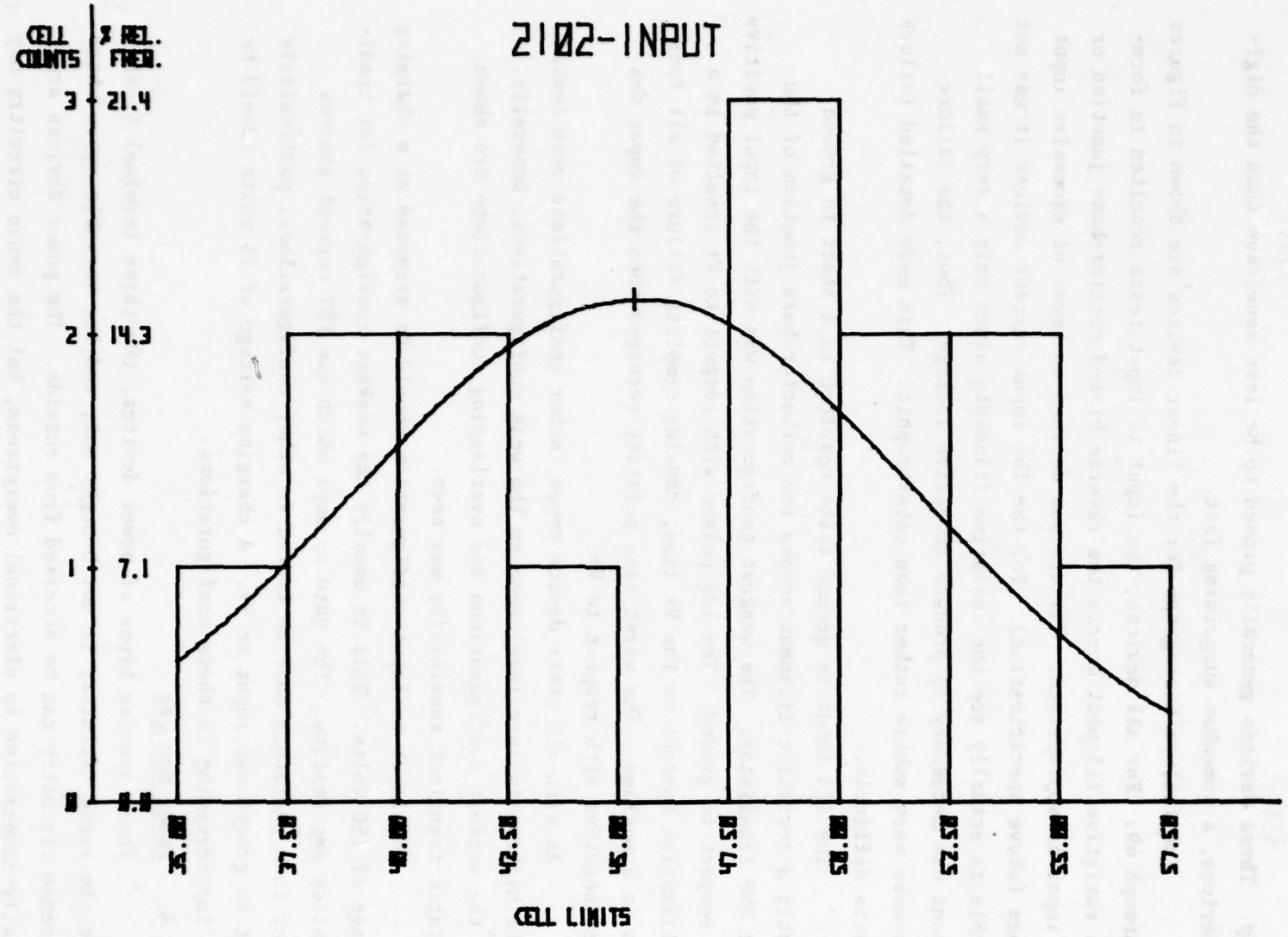


Figure 63. Failure Histogram for 2102 Input System Transient Tests

op amp. These devices generally proved to be less sensitive than the digital devices, a somewhat surprising fact.

The failure histograms for the linear devices are shown in Figures 64 through 69. For all devices, the input to input tests resulted in forming a resistive filament across the reverse biased emitter-base junction or JFET input as appropriate. Failure was defined in terms of excessive input leakage (above specification). For the low input current devices it was not possible to actually see the resistive filaments since only a very small filament was necessary to produce excessive leakage. Thus, the failure modes were very subtle rather than catastrophic. This made detailed failure analysis difficult.

The 124 input to ground tests resulted in a short to ground, probably a resistive filament across the collector-base junction of the input PNP transistor. The weakest configuration was with the input positive with respect to ground. The 139 pulsed with respect to V+ resulted in a metallization burnout on the V+ line, causing complete failure of all four units in a package. The worst case polarity occurred when the input was pulsed negative with respect to V+.

As with all other device types, other configurations were tested at the highest failure level seen on the weak configurations. Generally, only the weakest configurations and overlapping configurations are shown. No static transient sensitivity was seen.

The input to input configuration should be screened at a charging voltage of 150 volts. This is usually the weakest configuration for traditional op amp designs. The quad op amps which use FET current sources rather than resistors must be tested in other configurations, particularly input to ground and input to V+. A charging voltage of 75 volts should be used for screening in these configurations.

4. Power Devices

There are two types of power devices, the three terminal types where the sense circuitry is not brought out, and the variable types where the sense circuitry can be accessed from outside. The power devices are normally insensitive to electrical overstress, but the sense circuitry may prove vulnerable.

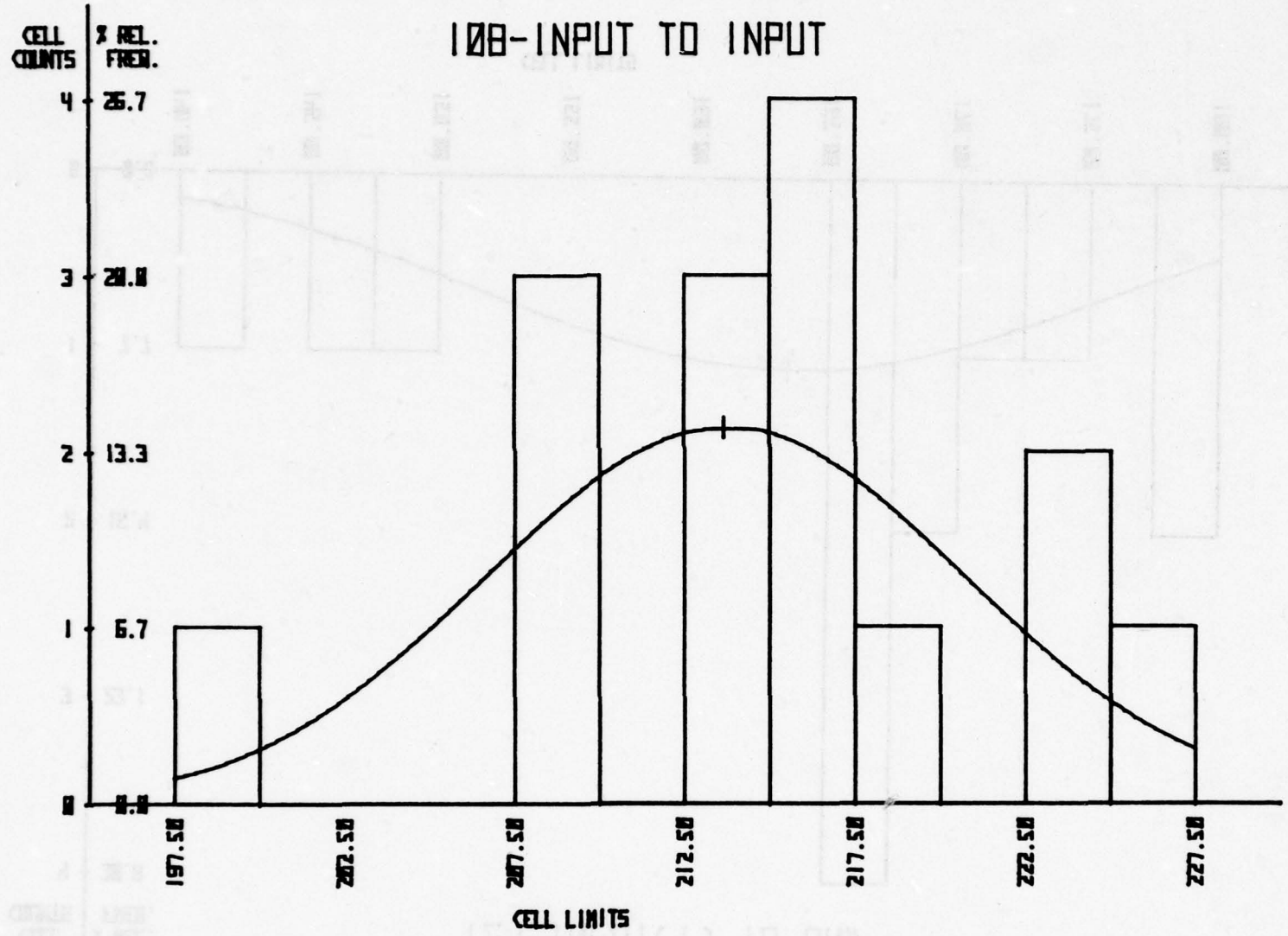


Figure 64. Failure Histogram for 108 Input-to-Input System Transient Tests

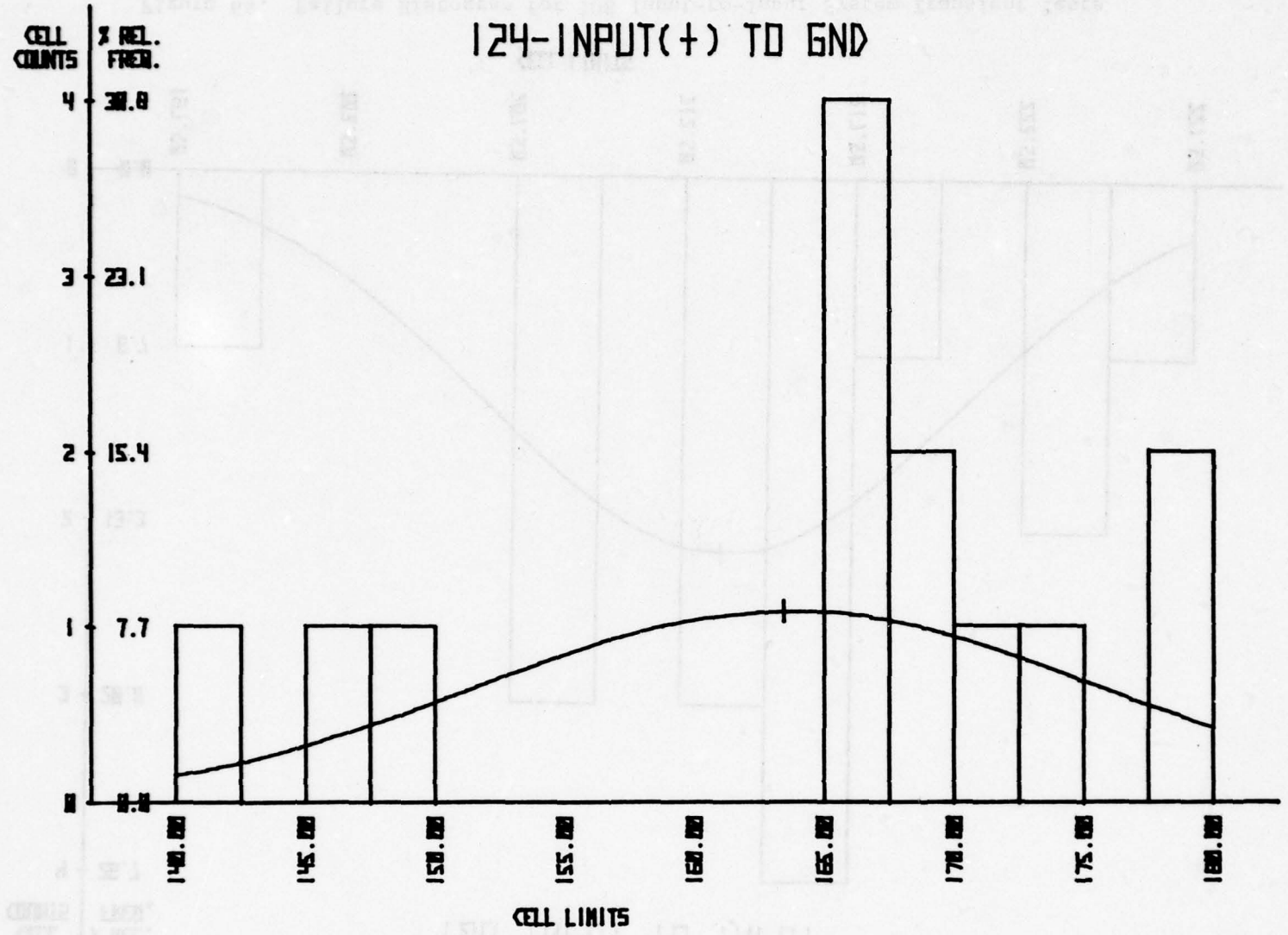


Figure 65. Failure Histogram for 124 Input-to-Ground System Transient Tests

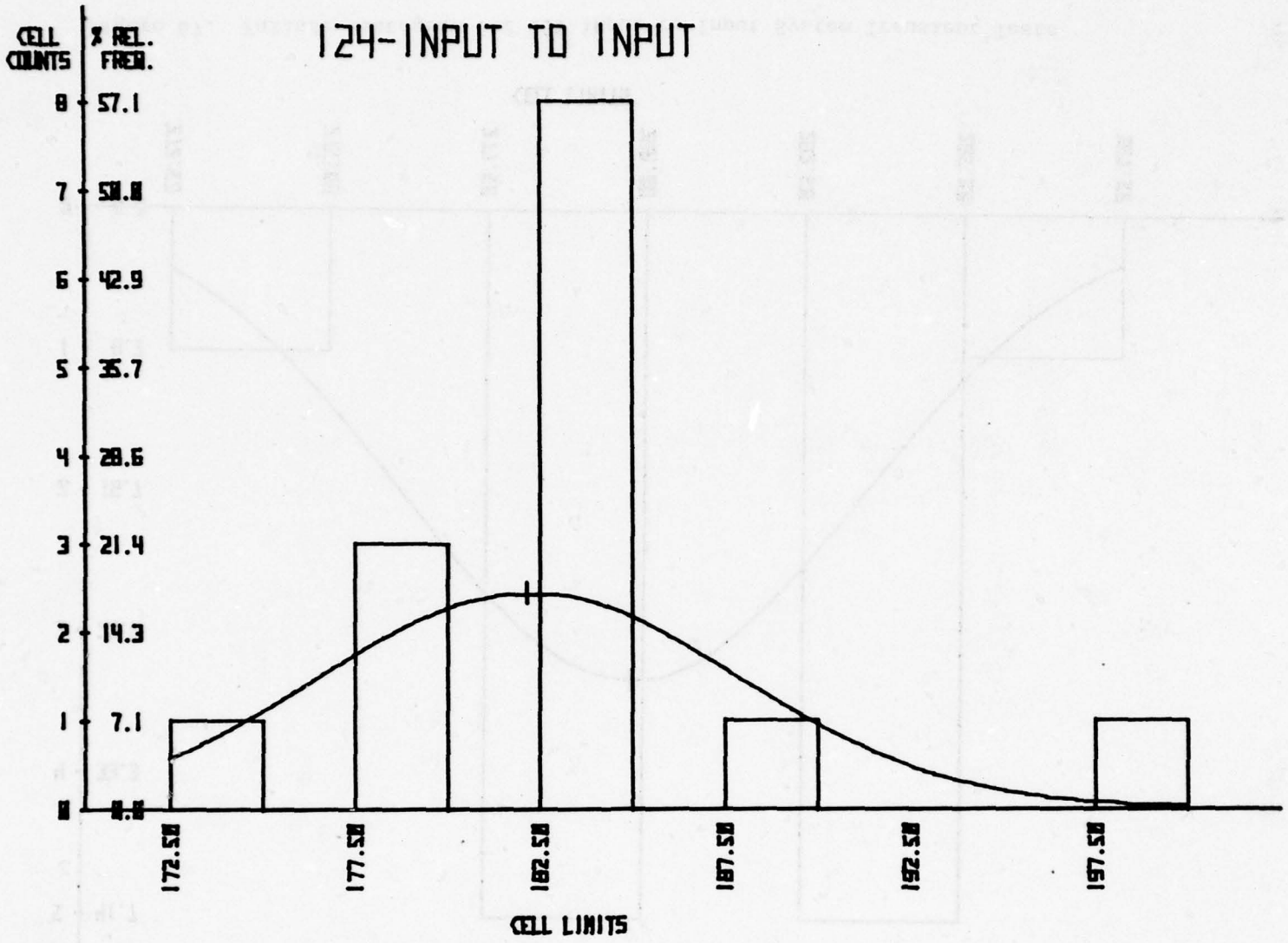


Figure 66. Failure Histogram for 124 Input-to-Input System Transient Tests

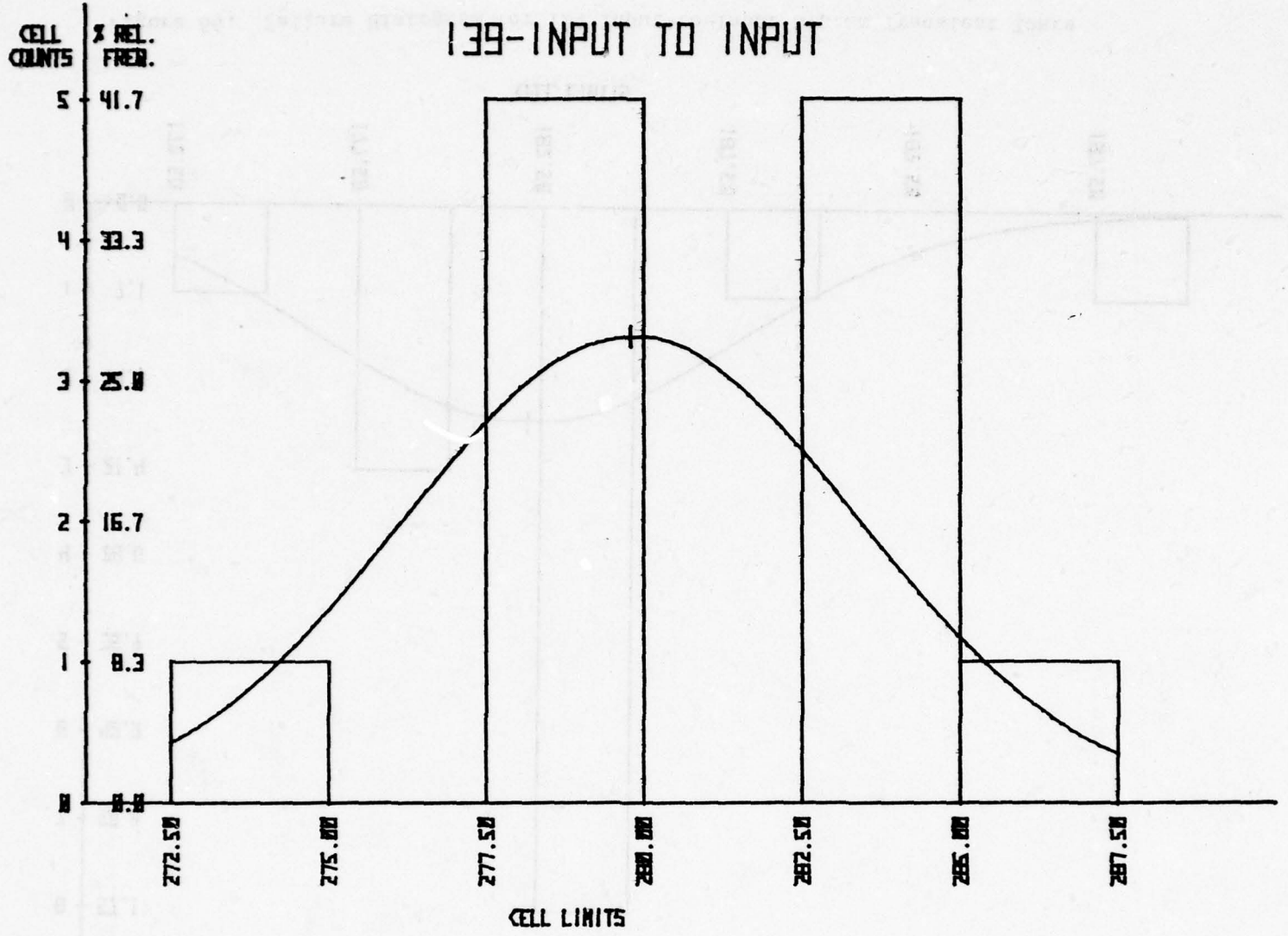


Figure 67. Failure Histogram for 139 Input-to-Input System Transient Tests

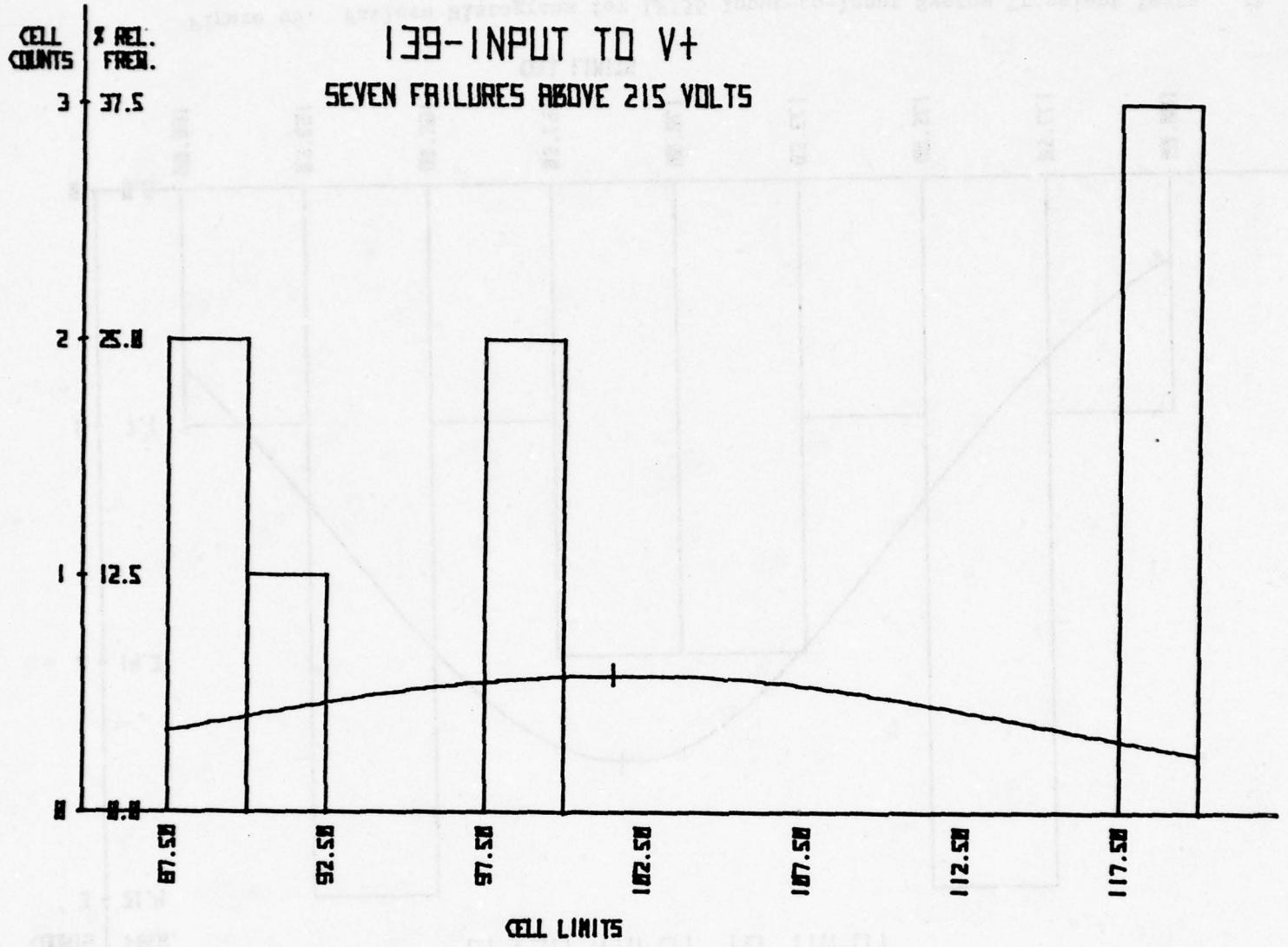


Figure 68. Failure Histogram for 139 Input to V+ System Transient Tests

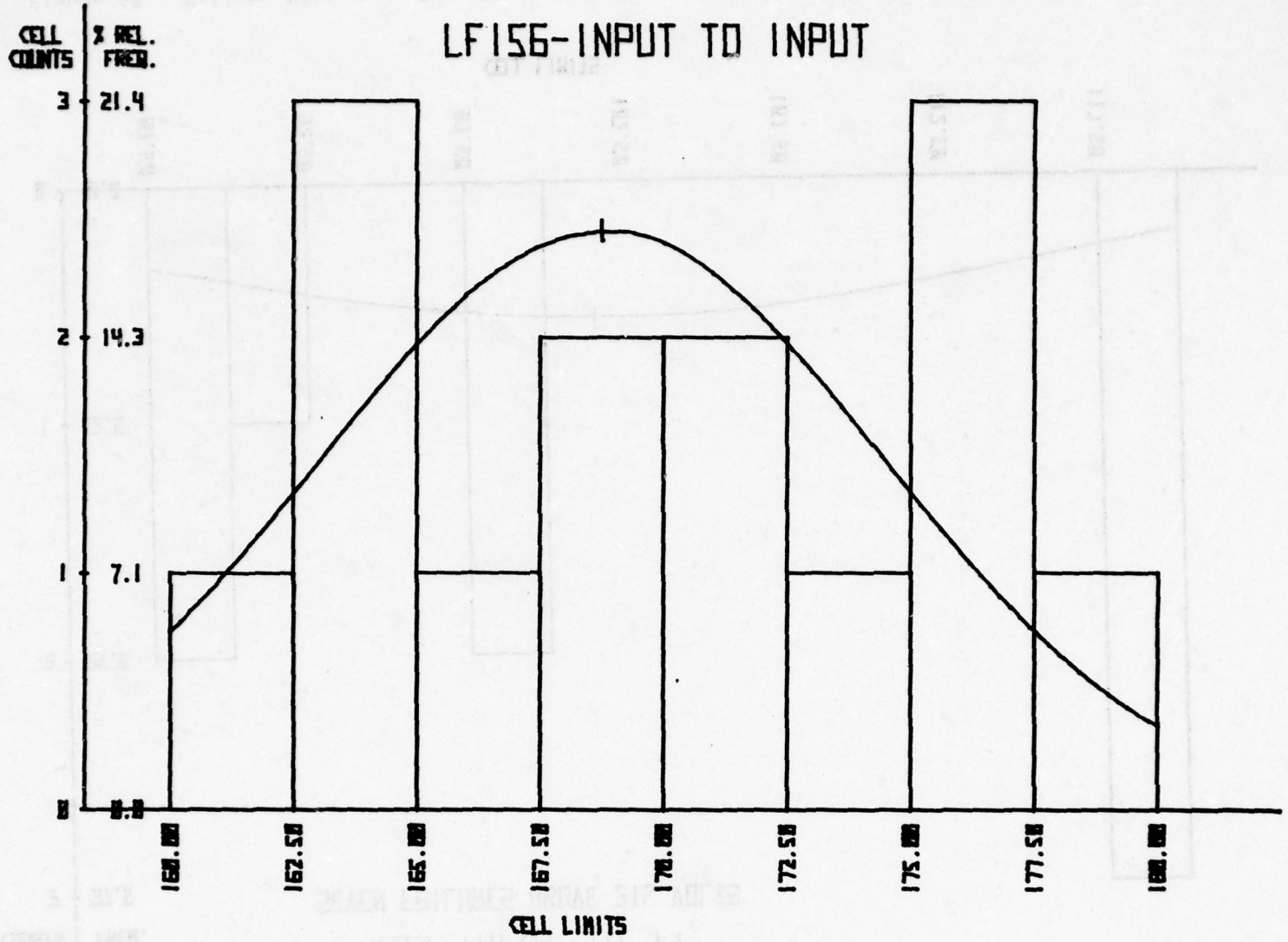


Figure 69. Failure Histograms for LF156 Input-to-Input System Transient Tests

Two three-terminal fixed regulators were tested, the 109 five volt positive regulator and the 120 eight-volt negative regulator. It was not possible to fail these devices with the maximum system transient pulse of 300 volts in any configuration. Thus, they were tested using a Velonex 350 pulse generator with a 100-ohm source resistance and a 10-microsecond rectangular pulse. The failure histograms are shown in Figures 70 through 72. Both devices failed by not regulating within specifications. The 109 exhibited a burnout of part of the ground distribution system, leading to a high ground resistance and failure to regulate. The 120 exhibited an emitter-base short on one of the output power transistors.

The three terminal regulators should be considered insensitive and are probably not worth screening. A minimum screening level of 300 volts should be adequate. Input to ground is generally the weakest configuration.

The 723 was the only variable regulator tested. The failure histogram for the differental sense inputs is shown in Figure 73. These inputs are very much weaker than the 3-terminal regulators. Note the one failure which occurred between 17.5 and 20 volts. This was a maverick device which failed due to a metallization burnout at an oxide step. All other devices failed due to a resistive filament across the reverse biased emitter-base junction.

Variable regulators should be tested so as to reverse bias emitter-base junctions of the sense circuit. The charging level should be 40 volts. These devices should be considered extremely sensitive to electrical overstress and handled accordingly.

5. Interface Devices

Interface devices make use of analog techniques to transmit digital data in the presence of noise. They are typically known as line drivers and receivers.

Two line drivers were tested, the 9616 and the 55109. The outputs of these devices are quite hard, and only the digital inputs appear to be sensitive. The failure histogram for these inputs is shown in Figures 74 and 75. These devices exhibit failure levels similar to TTL/DTL inputs. They should be screened at the same input level as TTL devices and in the same configurations.

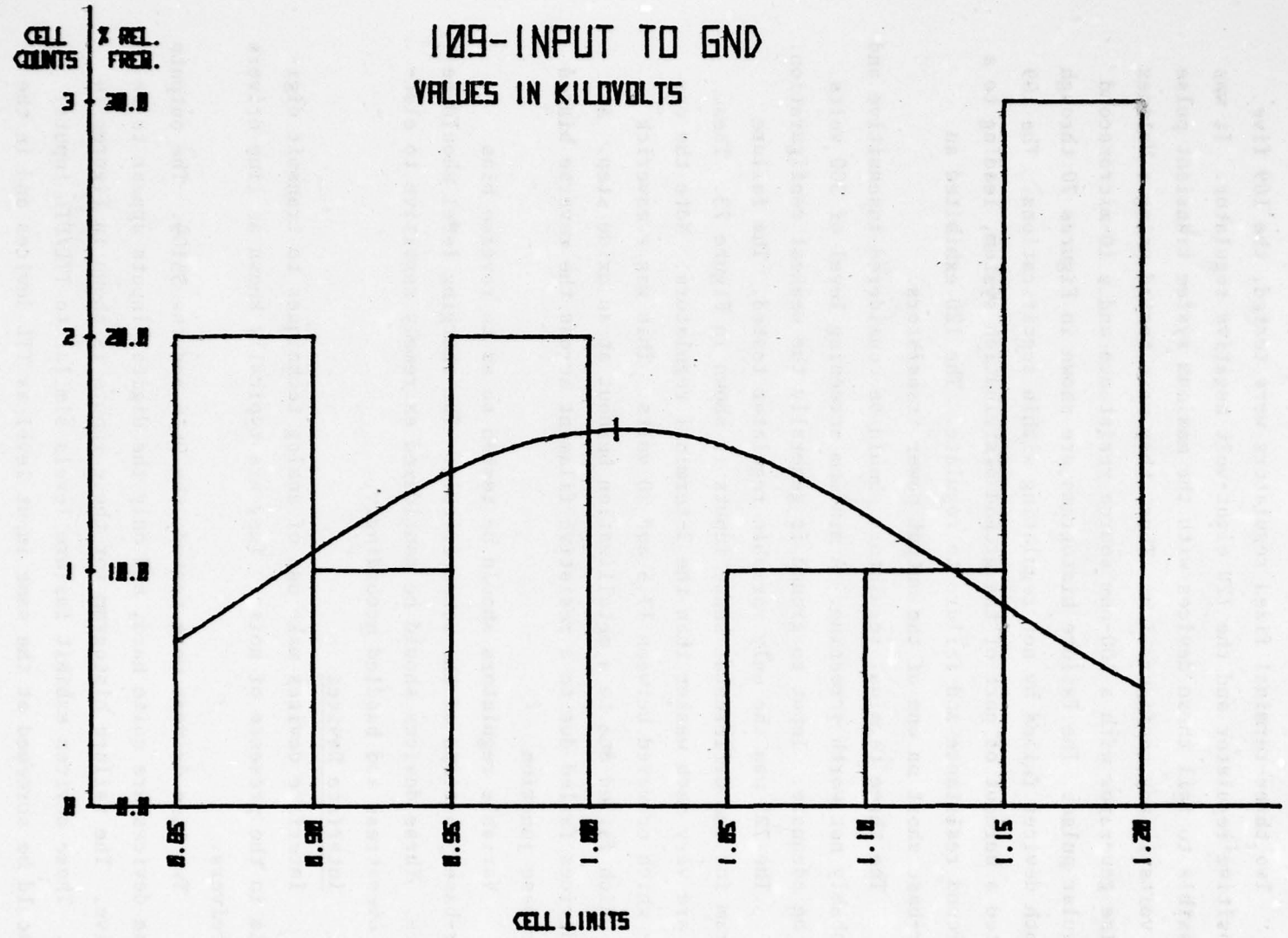


Figure 70. Failure Histogram for 109 Input-to-Ground 10 μsecond Rectangular Pulse Tests

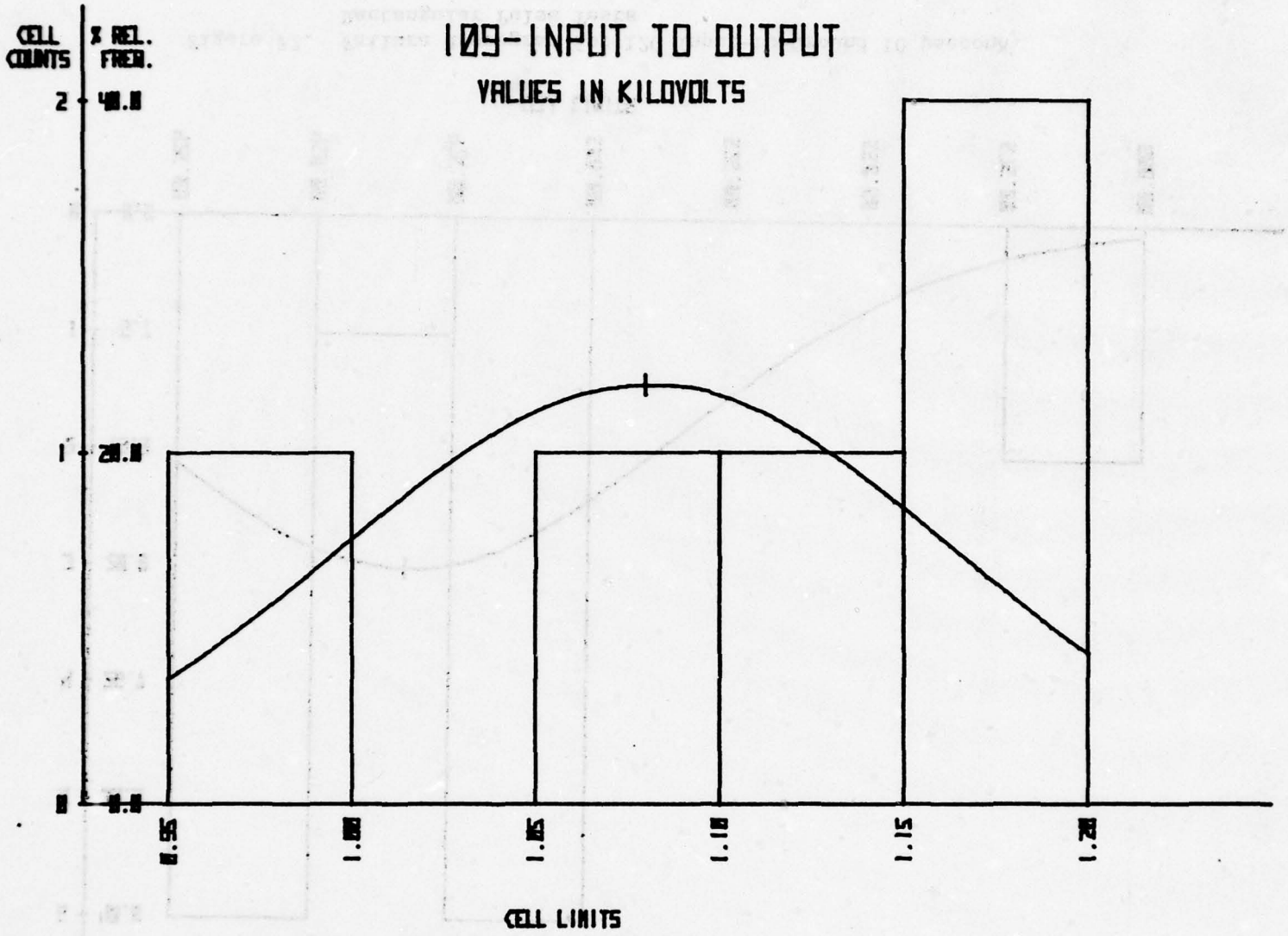


Figure 71. Failure Histogram for 109 Input-to-Output 10 μsecond Rectangular Pulse Tests

Figure 72. Failure Histogram for 120 Input-to-Ground 10 μsecond Rectangular Pulse Tests

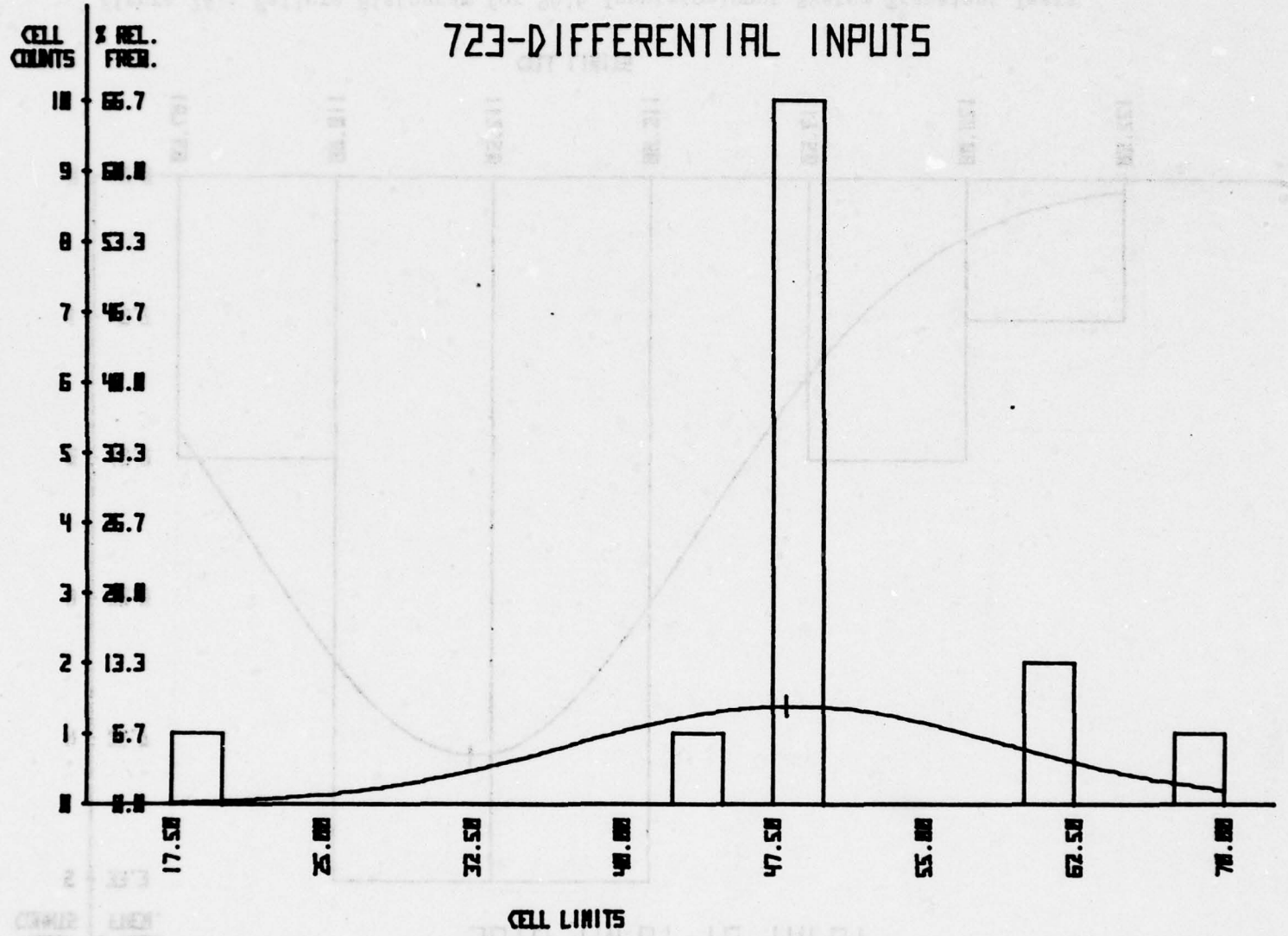


Figure 73. Failure Histogram for 723 Differential Input System Transient Tests

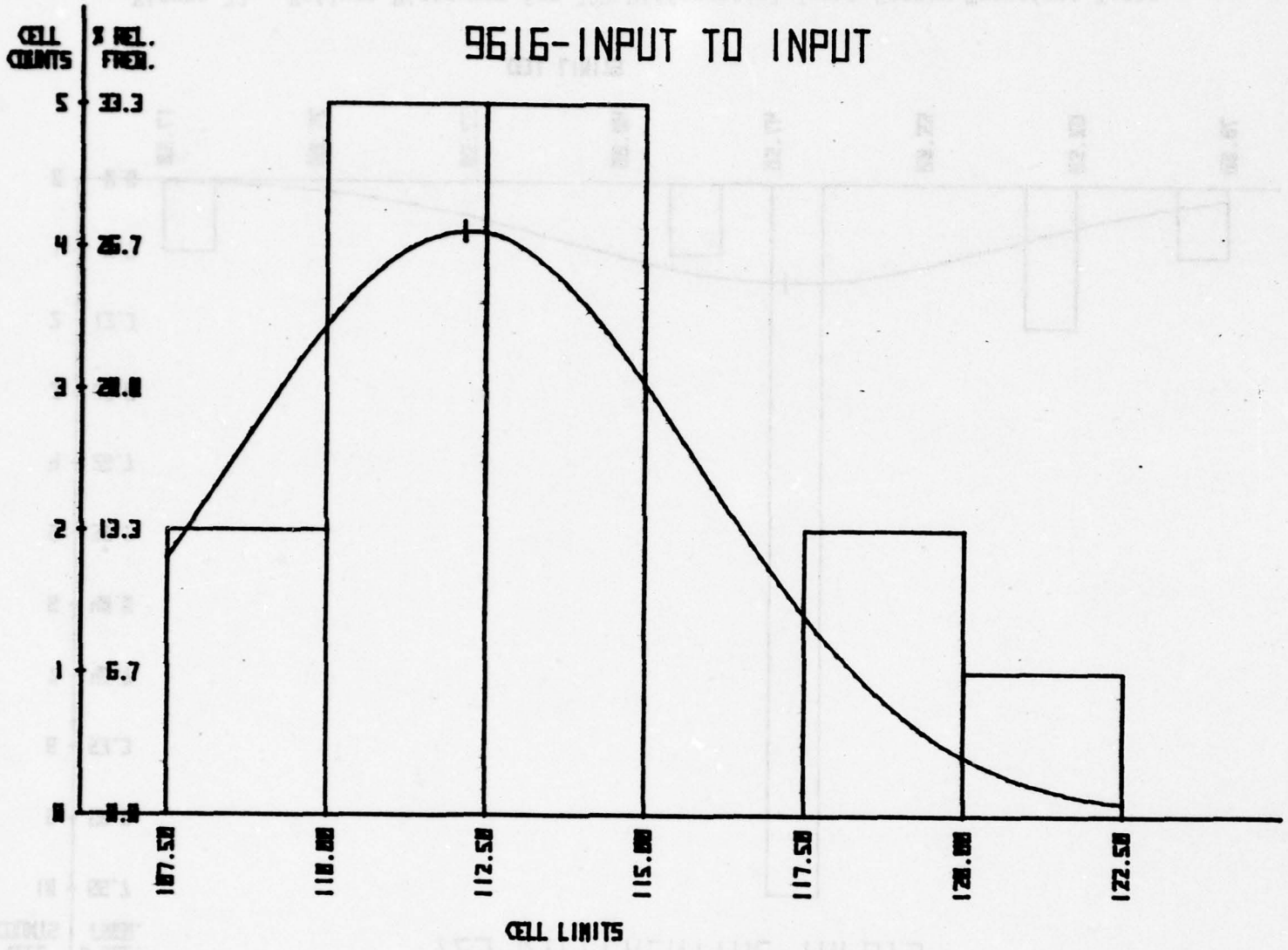


Figure 74. Failure Histogram for 9616 Input-to-Input System Transient Tests

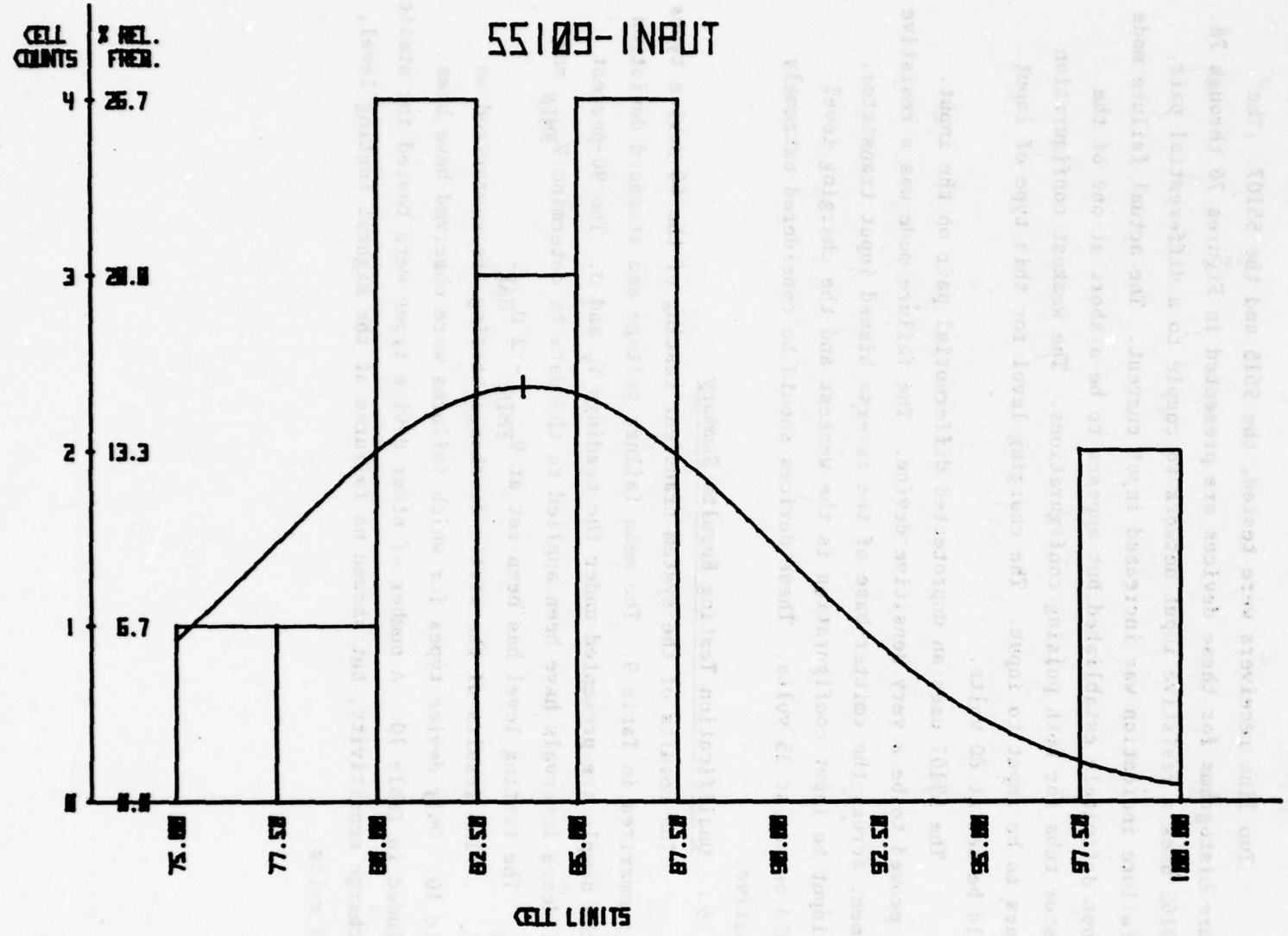


Figure 75. Failure Histogram for 55109 Input System Transient Tests

Two line receivers were tested, the 9615 and the 55107. The failure histograms for these devices are presented in Figures 76 through 78. The 9165 uses a resistive input network to couple to a differential pair. Its failure indication was increased input current. The actual failure mode was not definitely established but appears to be a short at one of the resistor tubs for both pulsing configurations. The weakest configuration appears to be input to input. The charging level for this type of input should be set at 80 volts.

The 55107 uses an unprotected differential pair on the input. This proved to be a very sensitive device. The failure mode was a resistive filament across the emitter-base of the reverse biased input transistor. The input to input configuration is the weakest and the charging level should be set at 35 volts. These devices should be considered extremely sensitive.

6. Qualification Testing Results Summary

The results of the system transient testing of the 40 device types are summarized in Table 9. The mean failure voltage and standard deviation of the sample are presented under the headings V_F and σ. The 90-percent confidence intervals have been applied to the data to determine V_{FMIN} and σ_{MAX}. The testing level has been set at $V_{FMIN} - 2\,\sigma_{MAX}$.

The results of the static discharge testing are summarized in Table 10. Only device types for which failures were observed have been included in Table 10. A number of other device types were tested for static discharge sensitivity, but showed no failures at the highest testing level, 1000 volts.

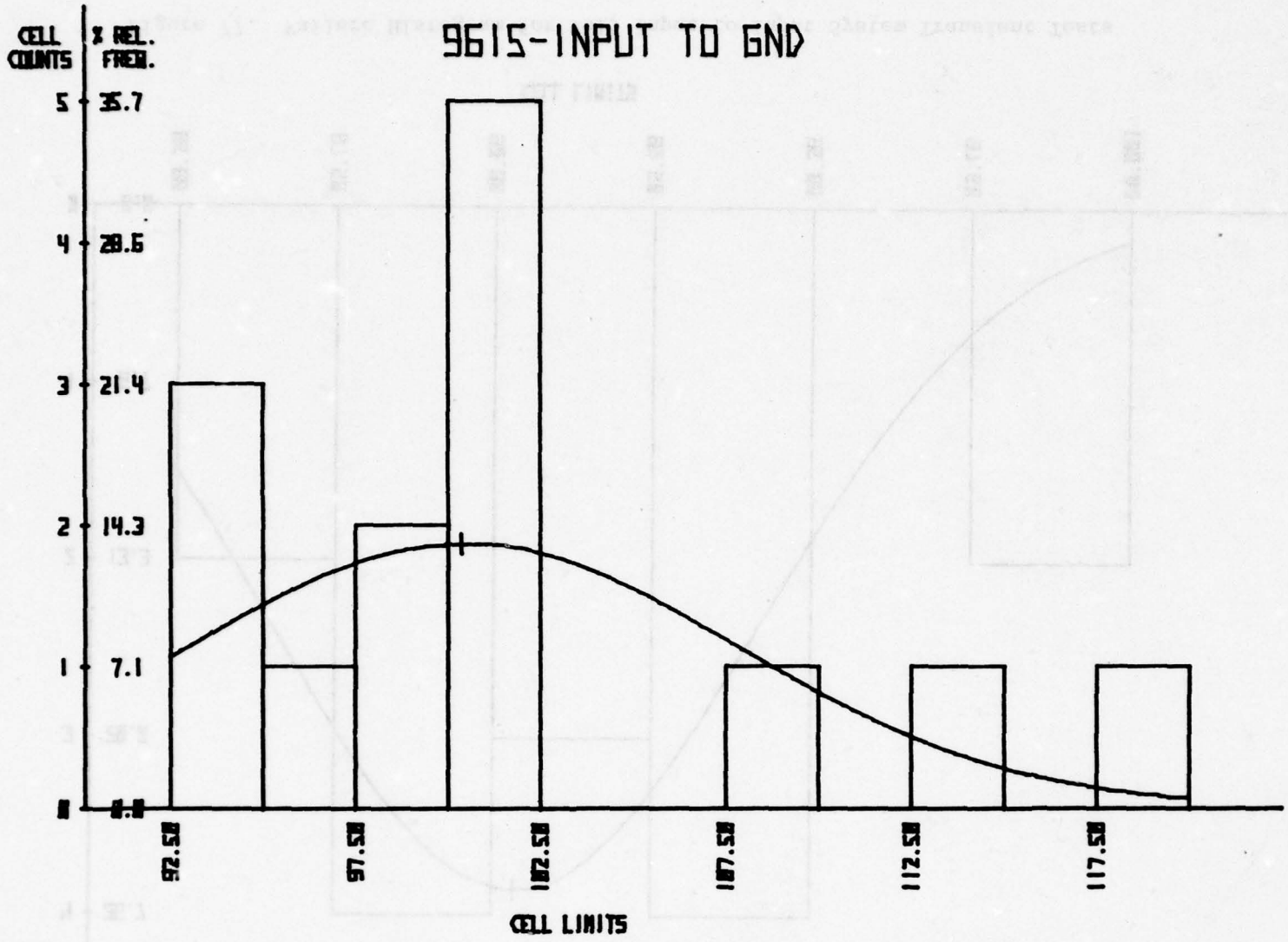


Figure 76. Failure Histogram for 9615 Input to Ground System Transient Tests

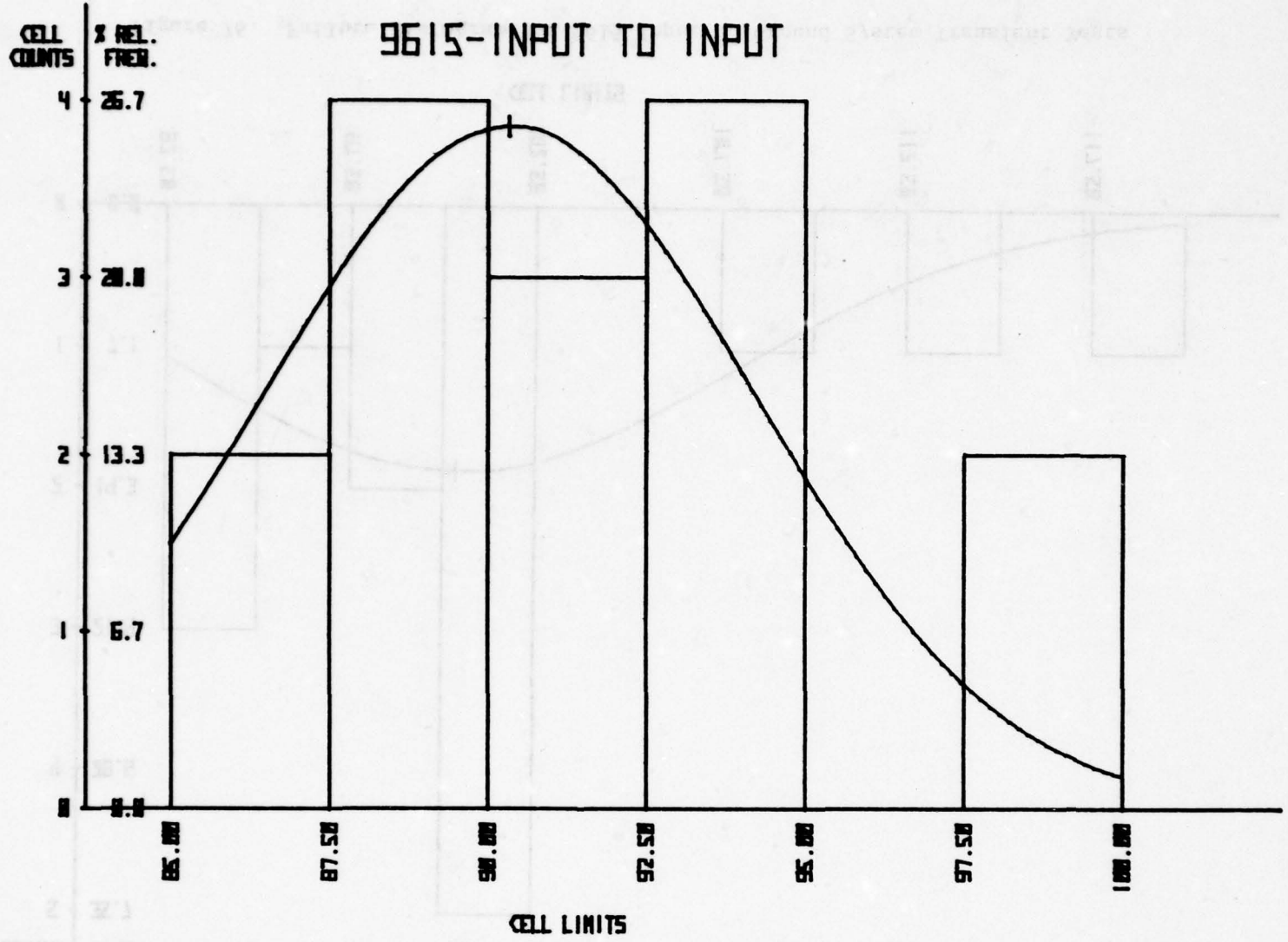


Figure 77. Failure Histogram for 9615 Input-to-Input System Transient Tests

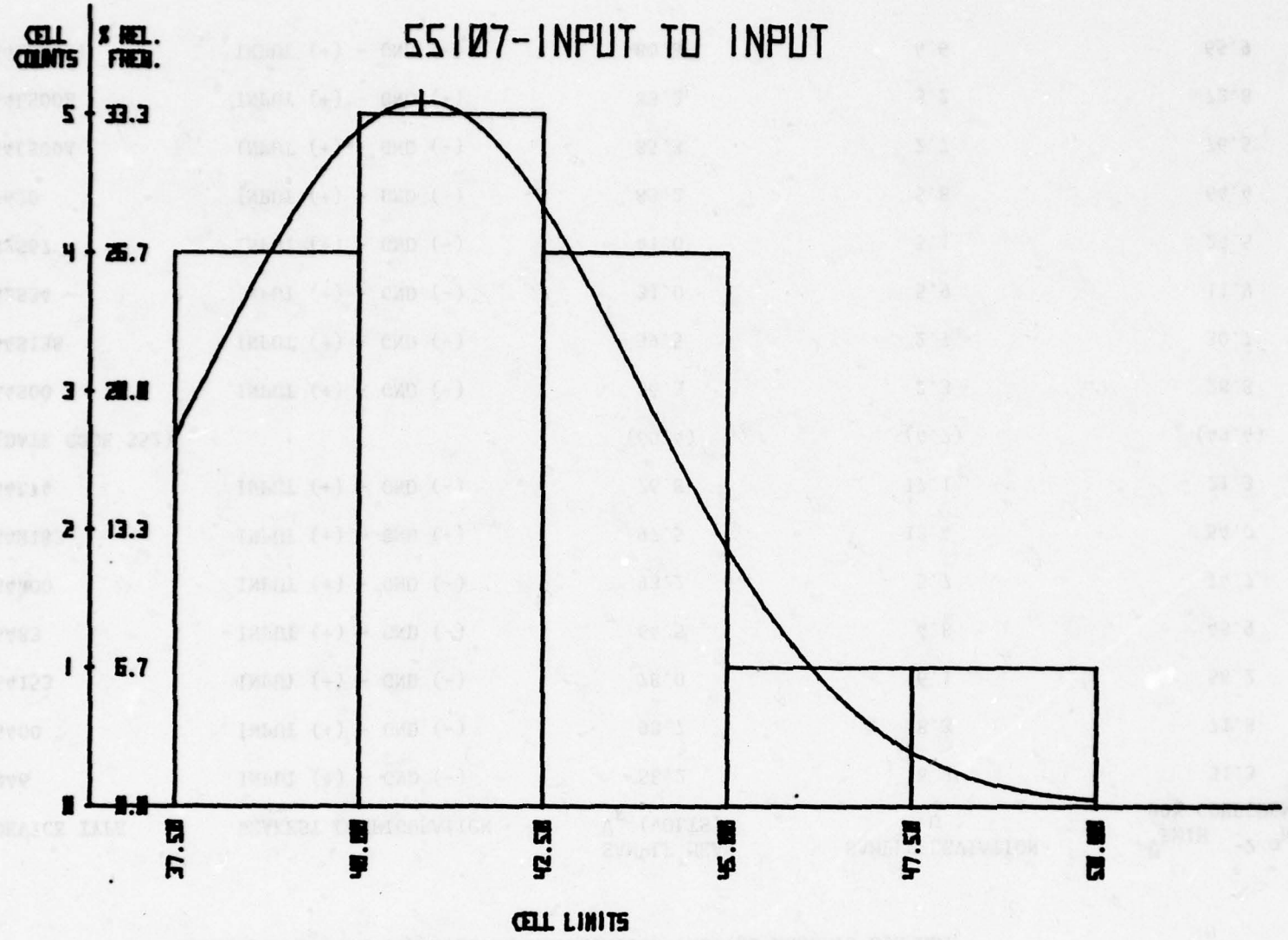


Figure 78. Failure Histogram for 55107 Input-to-Input System Transient Tests

TABLE 9. SYSTEM TRANSIENT QUALIFICATION TESTING RESULTS SUMMARY

	DEVICE TYPE	WEAKEST CONFIGURATION	SAMPLE MEAN $\bar{V}_F$ (VOLTS)	SAMPLE DEVIATION σ	$\bar{V}_{FMIN} - 2\sigma_{MAX}$ 90% CONFIDENCE
1.	946	INPUT (+) - GND (-)	58.2	8.3	31.3
2.	5400	INPUT (+) - GND (-)	98.7	8.3	71.8
3.	54153	INPUT (+) - GND (-)	78.0	6.1	58.2
4.	5483	INPUT (+) - GND (-)	64.5	4.8	48.9
5.	54H00	INPUT (+) - GND (-)	93.2	5.7	74.7
6.	54H183	INPUT (+) - GND (-)	97.5	13.4	54.0
7.	54L74	INPUT (+) - GND (-)	76.8	17.1	21.3
	(DATE CODE 352)		(60.4)	(4.7)	(49.4)
8.	54S00	INPUT (+) - GND (-)	36.3	2.3	28.8
9.	54S138	INPUT (+) - GND (-)	39.5	2.7	30.7
10.	82S34	INPUT (+) - GND (-)	31.0	5.9	11.9
11.	82S67	INPUT (+) - GND (-)	41.0	5.1	24.5
12.	7620	INPUT (+) - GND (-)	83.2	5.8	64.4
13.	54LS00A	INPUT (+) - GND (-)	85.3	2.7	76.5
14.	54LS00B	INPUT (+) - GND (-)	83.2	3.2	72.8
15.	54LS00C1	INPUT (+) - GND (-)	80.8	4.6	65.9

TABLE 9. SYSTEM TRANSIENT QUALIFICATION TESTING RESULTS SUMMARY (Continued)

	DEVICE TYPE	WEAKEST CONFIGURATION	SAMPLE MEAN $\bar{V}_F$ (VOLTS)	SAMPLE DEVIATION σ	$\bar{V}_{FMIN} - 2\sigma_{MAX}$ 90% CONFIDENCE
16.	54LS00C2	INPUT (+) - GND (-)	-	-	-
17.	54LS153	INPUT (+) - GND (-)	94.8	8.1	68.5
18.	54LS192	INPUT (+) - GND (-)	59.2	4.1	45.9
19.	10102	INPUT (-) - OUTPUT (+)	59.3	3.6	47.6
20.	10130	INPUT (-) - OUTPUT (+)	130.7	10.8	95.6
21.	XC401	OUTPUT (+) - GND (-)	52.0	4.6	37.1
22.	XC402	INJECTOR (+) - INPUT (-)	62.0	4.1	48.7
23.	XC404	INJECTOR (+) - INPUT (-)	48.8	4.5	34.2
24.	4001	INPUT (-) - V_{SS} (+)	65.8	2.6	57.4
25.	4066	INPUT (-) - V_{SS} (+)	76.2	2.5	68.1
26.	4023A	INPUT (-) - V_{SS} (+)	202.5	20.7	135.3
27.	4023B	INPUT (-) - V_{SS} (+)	231.5	6.5	210.4
28.	4023D	INPUT (-) - V_{SS} (+)	61.3	2.3	53.8
29.	2102	INPUT (+) - GND (-)	45.4	6.5	24.3
30.	LF156	INPUT - INPUT	168.8	5.7	150.3

TABLE 9. SYSTEM TRANSIENT QUALIFICATION TESTING RESULTS SUMMARY (Concluded)

	DEVICE TYPE	WEAKEST CONFIGURATION	SAMPLE MEAN $\bar{V}_F$ (VOLTS)	SAMPLE DEVIATION σ	$\bar{V}_{FMIN} - 2\sigma_{MAX}$ 90% CONFIDENCE
31.	LM108	INPUT - INPUT	213.7	7.0	191.0
32.	LM124	INPUT (+) - GND (-)	163.5	11.9	124.9
33.	LM139	INPUT (-) - V + (+)	101.5	13.8	50.0
34.	723	ACROSS DIFFERENTIAL INPUTS	50.4	6.9	28.0
35.	LM120	INPUT (+) - GND (-)	466.7	49.7	305.4
36.	LM109	INPUT (-) - GND (+)	1010.0	124.0	607.5
37.	9615	INPUT - INPUT	90.3	3.9	77.6
38.	9616	INPUT - INPUT	112.2	3.6	100.4
39.	55107	INPUT - INPUT	40.8	2.9	31.4
40.	55109	INPUT (+) - GND (-)	83.7	6.3	63.3

TABLE 10. STATIC DISCHARGE QUALIFICATION TESTING RESULTS SUMMARY

DEVICE TYPE	CONFIGURATION	NUMBER FAILED	LOWEST FAILURE VOLTAGE
4001	INPUT (+) - OUTPUT (-)	1 OF 14	950
4023A	INPUT (-) - OUTPUT (+)	2 OF 14	975
4023D	INPUT (-) - V_{SS} (+)	3 OF 14	1000
4023D	INPUT (-) - OUTPUT (+)	2 OF 14	950

SECTION IV
RECOMMENDATIONS

It appears that it is possible to define a practical electrical overstress tolerance specification which will separate microcircuits into sensitive and nonsensitive categories as well as screen out lots which do not meet normal standards for that technology. RADC should implement this specification on a trial basis, gather the appropriate information, and revise the specification as required.

There are several weaknesses which limit the usefulness of the specification at present. One is the fact that the testing levels are based on small sample sizes, typically only 15. Larger samples, 25 as a minimum, should be obtained from various manufacturers to better set the testing level for the various technologies.

A second limitation is the lack of information on the emerging technologies, I^2L in particular. Various forms of I^2L should be studied in detail to better set the testing levels and understand the failure modes. Samples should be obtained from all principal manufacturers of I^2L. The same should be done for some of the NMOS technologies.

Yet another limitation is the lack of information on the effect of screening on reliability. At present, it would be unwise to institute a 100 percent screen since this might degrade reliability. The results of the tests on the CMOS 4023B reported in Section III indicate reliability might be degraded for that device type. On the other hand, the results of the tests on the 723 voltage regulator indicate that such a screen might help eliminate weak devices. Only a thorough study can answer these questions.

Contact should be maintained with the EMP community. The waveform conversion techniques developed in this program can be used to translate EMP failure data into a form which can increase the available data base.

Ultimately, RADC should study design and processing factors which lead to high sensitivity and establish the trade-offs involved in reducing that sensitivity. The result would be improved microcircuit reliability.

APPENDIX A

ENVIRONMENT GENERATOR DESCRIPTION

A. GENERAL

The SPG-300 environment generator is designed to provide simulation waveforms for qualification testing of microcircuits. A photograph of the generator is shown in Figure A-1. The generator has two switch selected outputs, one for static discharge simulation, and one for system transient simulation. Figure A-2 shows oscilloscope photographs of the short circuit current waveforms of these two simulation pulses. The microcircuit to be tested is mounted in a zero insertion force socket with connections to the pulser output made by way of small 24-gauge jumper wires.

B. FRONT PANEL CONTROL AND INDICATORS

AC INDICATOR. Red neon lamp to indicate when ac power is turned on.

POWER ON switch. Push-on push-off switch to apply primary ac power.

FUSES. Primary power fuses, 2 amps each.

PULSE SELECT. Two-position switch to select static discharge or system transient simulation.

VOLTAGE ADJUST. Potentiometer to adjust the output pulser voltage.

PULSE SIMULATION lamps. Two lamps which indicate which section of the pulser is active. These lamps also indicate the meter range.

PULSER OUTPUT. Two sets of banana jacks into which the device fixture board is connected. Only the upper row of these jacks is active. The lower row is for mechanical strength only.

TRIGGER SWITCH. Pushbutton switch to generate the output pulse.

TRIGGER LAMP. Lamp to indicate that the trigger switch is depressed.

MONITOR. Banana jack for connecting external DVM.

METER. Analog meter to indicate pulser output amplitude. The pulse simulation lights indicate the meter range.

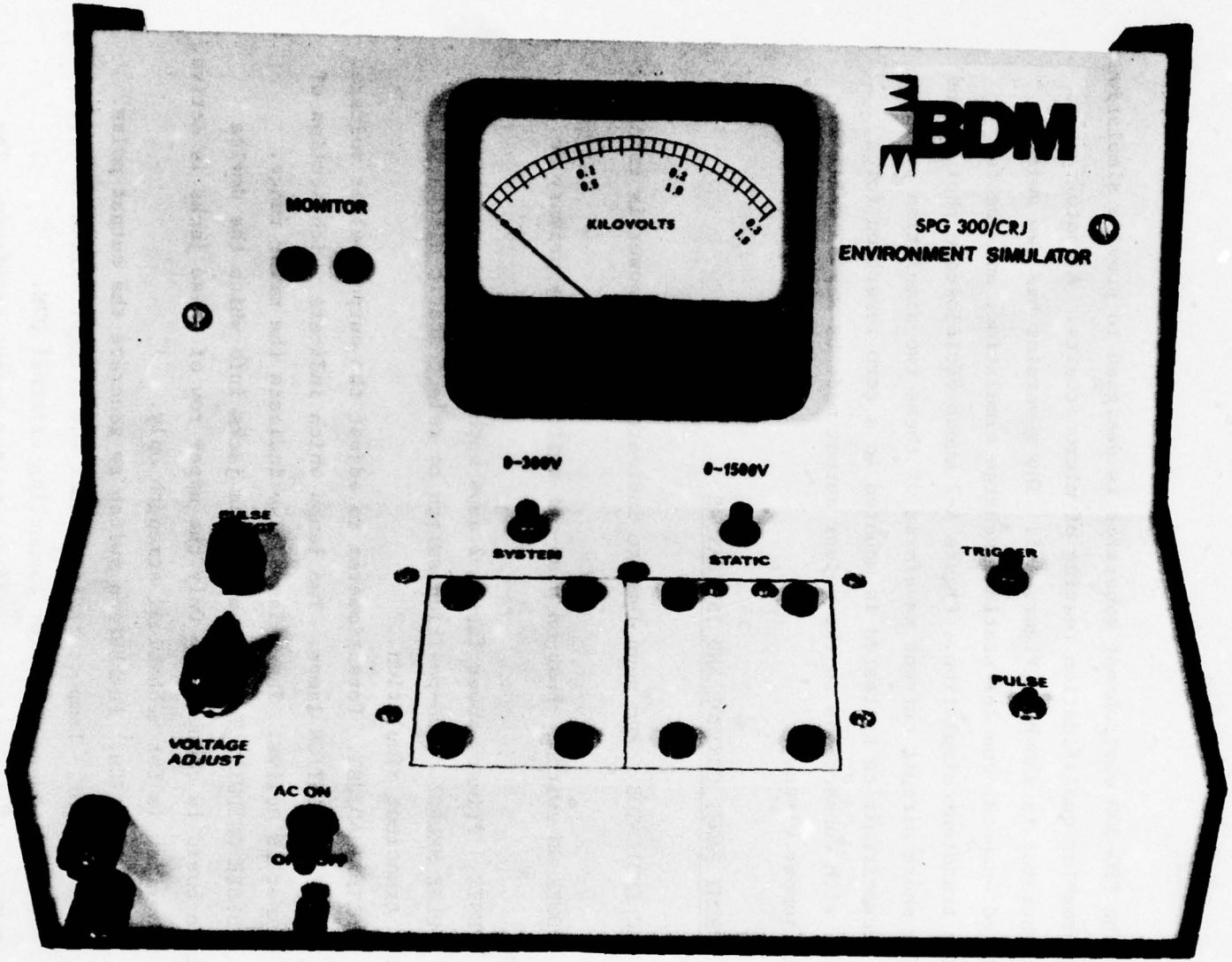
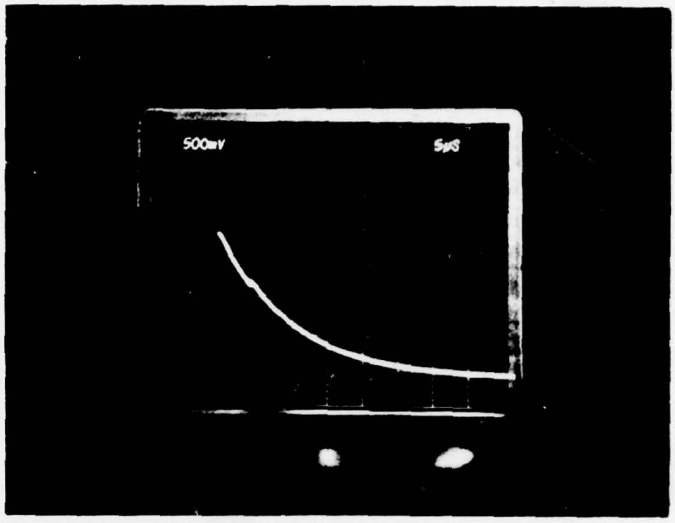
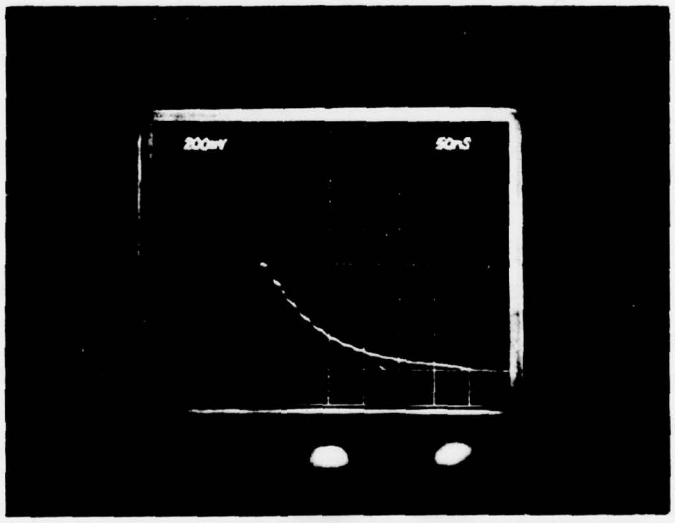


Figure A-1. SPG-300 Environment Generator



a) System Transient Current Waveform



b) Static Discharge Current Waveform

Figure A-2. Pulser Short Circuit Current Waveforms

C. OPERATING PROCEDURES

Before operating the simulator, the operator should be thoroughly familiar with the front panel controls described in the previous section.

WARNING

Voltages at the output terminal of the simulator and on the device fixture board may be as high as 1000 volts and can be dangerous. Extreme caution must be exercised when operating this instrument.

Prior to turning the simulator on, set the voltage adjust control to its minimum value (fully counterclockwise). It is recommended that this control be kept in the counterclockwise position when the simulator is not in use. Prewire the device fixture board to give the desired test pin combination using short pieces of #24-gauge tinned copper wire as jumpers. Insert the device fixture board into the appropriate test section, system or static, with the handle of the zero insertion force socket facing the operator. If an external DVM is to be used as a monitor, connect the DVM to the monitor jack. Turn on the ac power.

Select the test to be run with the pulse select switch. The green pulse select lamps will indicate which section of the simulator is active and which meter range to use. Adjust the output of the pulser using the voltage adjust control. The front panel meter is calibrated in kilovolts. The external monitor has a built-in 100:1 divider so that 1000 volts is read at 10.00 volts and 300 volts is read at 3.00 volts. The microcircuit to be tested can now be inserted into the zero insertion force socket.

To fire the pulser, depress and momentarily hold the pulser switch. During the time the pulse switch is held, the trigger lamp will be lit. This is also the time that the capacitor in the wave shaping circuit is charged. A momentary dip in the meter may be seen when the pulse switch is depressed. This is normal since the voltage at the power supply output momentarily drops to zero as the capacitor is connected. The simulation pulse is generated when the pulse switch is released.

D. THEORY OF OPERATION

The following paragraphs describe in detail the electronic operation of the SPG-300 Environment Simulator. Reference designations cited during this description are those shown in the schematic diagram of Figure A-3.

1. Low Voltage Supplies

Primary power is applied to the simulator through the ac plug, P1, and the single pole single throw pushbutton on-off switch, S1. The ac power input line is double fused and leads directly to the primary windings of transformer, T3. Transformer T3 supplies low voltage ac to the four-way bridge, CR2 through CR5.

Transistor Q7 and its associated components form a regulator whose output is 24 Vdc. The zener diode CR1 and resistor R42 are used to obtain a 5 volt regulated voltage for the logic portion of the simulator. Transistor Q8, resistor R18, and their associated components are used to develop a variable dc voltage to drive the converter transformers.

2. System Transient Section

The LM555, U1, is used as an astable multivibrator with a period of 1.5 milliseconds and a 50 percent duty cycle. The output of U1 provides base drive for the Darlington connected converter transistors Q1 and Q2. Collector voltage for Q1 and Q2 is provided from the variable supply through the pulse select switch S3-C when the simulator is operated in the system mode. The load for Q1 and Q2 is the primary of transformer T1. The secondary of T1 is connected to a voltage doubler consisting of CR8, CR9, C14, and C15. The output of the doubler is filtered by R19 and C16.

When the pulse switch, S2, is depressed, relay K1 is energized and the pulse forming capacitor is connected to the output of the doubler supply through the current limiting resistor R30. When S2 is released, K1 is deenergized and capacitor C25 is discharged through resistor R31 and the microcircuit under test. Resistor R35 is used to discharge capacitor C25 in the event a device is not connected or the device fails in an open circuit mode during a test.

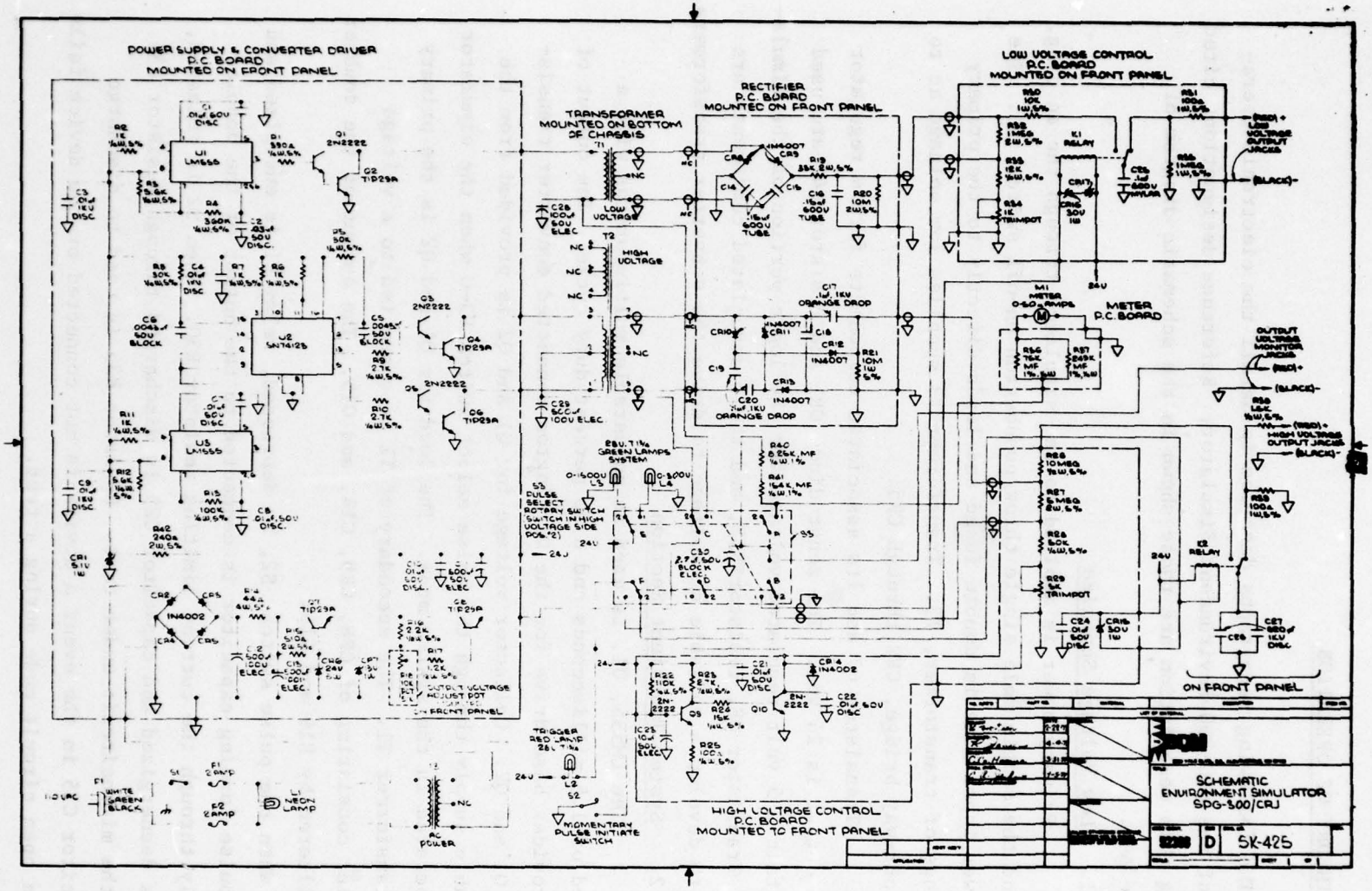


Figure A-3. Schematic Diagram of Environment Simulator SPG-300.

The meter circuit pickoff for the doubler power supply is via the 100:1 divider consisting of R32, R33, and potentiometer R34. Potentiometer R34 provides adjustment of the divider over approximately a 10 percent range. The output of the divider is connected directly to the monitor output through the pulse select switch S3-B and to the meter through S3-A.

3. Static Discharge Section

The LM555, U3, is used as an astable multivibrator having a pulse width of 1.4 milliseconds and a duty cycle of 50 percent. The output of U3 is used to trigger the monostable multivibrator U2. The pulse width at the output of U2 is 40 microseconds. Alternate pulses are generated at the output of U2 and are used as base drives for the two Darlington connected drivers Q3, Q4, and Q5, Q6. Collector voltage for these transistors is supplied from the variable supply through S3-C. The load for these transistors is the primary of transformer T2. The secondary of transformer T2 is connected to a voltage quadrupler consisting of diodes CR10 through CR12 and capacitors C17 through C20.

When pulse switch S2 is depressed, relay K2 is energized and the pulse forming capacitors C26 and C27 are connected to the output of the quadrupler supply through the current limiting resistor R26. When S2 is released, K2 is deenergized and C26 and C27 are discharged through resistors R39, R38, and the microcircuit under test. In the event of no load, the capacitors are discharged through resistor R39.

The meter circuit pickoff from the quadrupler supply is via the 100:1 divider consisting of R27, R28, and potentiometer R29. Potentiometer R29 provides adjustment of the divider over approximately a 10 percent range. The output of the divider is connected directly to the monitor output through the pulse select switch, S3-B, and to the meter through current limiting resistors R40 and R41.

APPENDIX B

WAVEFORM CONVERSION

Most of the integrated circuit failure threshold data available are in terms of a rectangular pulse. In order to utilize these data, a conversion between the square pulse and expotential pulse is required. A conversion has been developed and is presented below.

The power required to fail an integrated circuit is given as

$$P_F = At^{-B} \qquad \text{(Eq. B-1)}$$

where t is the pulse width and A and B are empirically determined constants. This is a more general form of the familiar Wunsch formulation for single junction failures which is

$$P_F = Kt^{-1/2} \qquad \text{(Eq. B-2)}$$

For an exponential pulse, assuming the voltage across the device clamps at a given level, the instantaneous power is given as

$$P_i = P_o e^{-t/\tau} \qquad \text{(Eq. B-3)}$$

and the average power is

$$\overline{P} = \frac{\tau P_o}{t}\left(1-e^{-t/\tau}\right) \qquad \text{(Eq. B-4}$$

Figure B-1 shows a log-log plot of the general shape of Equations B-1 and B-4. Figure B-1 shows that for a given square pulse width, t, there is one value of τ and P_o which will produce the same average power from the exponential pulse for time t, without exceeding the device failure power at some other time. This point can be found by letting

$$\overline{P} = P_F \qquad \text{(Eq. B-5)}$$

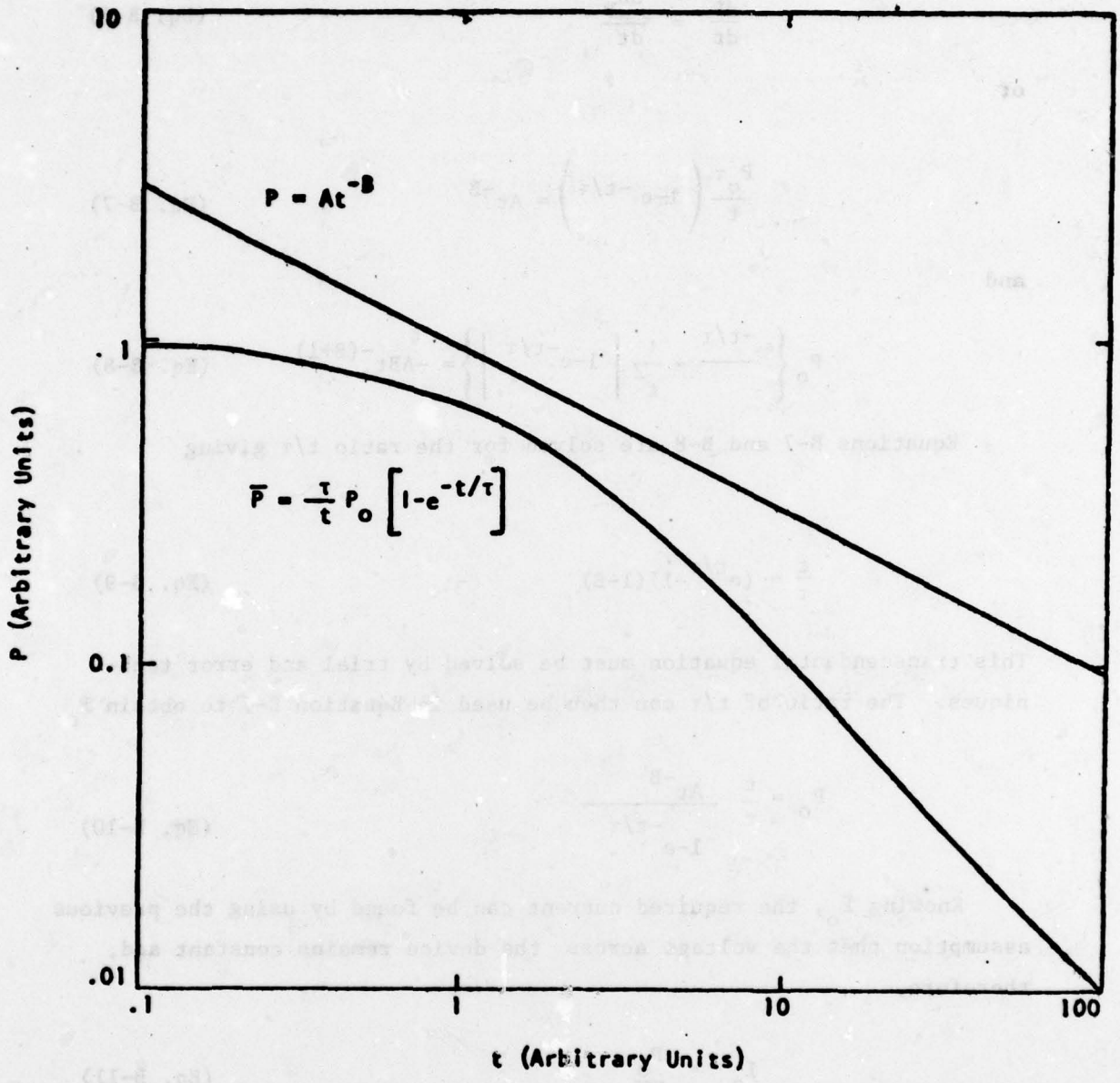


Figure B-1. Plots of $P_F = At^{-B}$ and $\bar{P} = \frac{\tau P_o}{t}\left[1-e^{-t/\tau}\right]$ in Arbitrary Units

and

$$\frac{d\bar{P}}{dt} = \frac{dP_F}{dt} \qquad \text{(Eq. B-6)}$$

or

$$\frac{P_o\tau}{t}\left(1-e^{-t/\tau}\right) = At^{-B} \qquad \text{(Eq. B-7)}$$

and

$$P_o\left\{\frac{e^{-t/\tau}}{} - \frac{\tau}{t^2}\left[1-e^{-t/\tau}\right]\right\} = -ABt^{-(B+1)} \qquad \text{(Eq. B-8)}$$

Equations B-7 and B-8 are solved for the ratio t/τ giving

$$\frac{t}{\tau} = (e^{t/\tau}-1)(1-B) \qquad \text{(Eq. B-9)}$$

This transcendental equation must be solved by trial and error techniques. The ratio of t/τ can then be used in Equation B-7 to obtain P_o

$$P_o = \frac{t}{\tau}\,\frac{At^{-B}}{1-e^{-t/\tau}} \qquad \text{(Eq. B-10)}$$

Knowing P_o, the required current can be found by using the previous assumption that the voltage across the device remains constant and, therefore,

$$I_o = \frac{P_o}{V_D} \qquad \text{(Eq. B-11)}$$

where V_D is the device voltage, I_o is the peak current, and P_o is the peak power. The open circuit peak voltage for a given source resistance is therefore given as

$$V_{oc} = V_D + I_o R_s \qquad \text{(Eq. B-12)}$$

where R_s is the source resistance.

The above expression have been used to convert in-house failure data to equivalent open circuit pulser voltages as shown in Table B-1. The device bulk resistance has been neglected in these calculations because the source resistance of 100 ohms is much larger than the device bulk resistance.

TABLE B-1. CONVERSION PARAMETERS (DATA FROM REFERENCE 11-13)

TECHNOLOGY	A	B	t/τ	V_{BD}	V_F
DTL	.0137	.580	1.540	18 VOLTS	108
TTL	.00126	.689	2.01	7 VOLTS	79
LINEAR	.0235	.509	1.286	7 VOLTS	191

APPENDIX C
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