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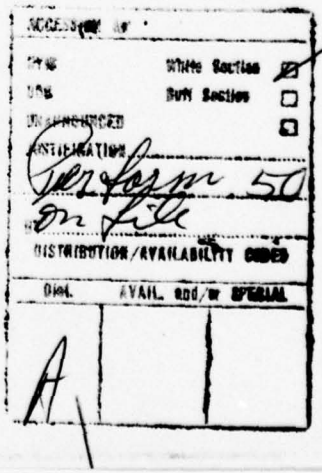

1ST QUARTERLY INTERIM TECHNICAL REPORT

B&K

DYNAMICS, INC.

I. INTRODUCTION

B-K Dynamics activities during the first quarter (28 October 1974 to 15 January 1975) have been focused on two major areas: STINGER simulation preparation and ~~PADDIOS~~ PDDAIOS installation. This report summarizes the work performed by BKD during the above period and outlines accomplishments and plans for the next quarter. No attempt has been made to document software generated during the period since all programs described are being continually upgraded. Current listings, flow charts and program decks are stored in the ACS's 9300 room.

II. STINGER SIMULATION ACTIVITIES

The interim STINGER simulation system is shown in Figure II-1. During the past quarter BKD activities have centered around completing installation of the 3010 interface, the AD-4 interface and the Simulation Interface Buffer Unit (SIBU). In addition an investigation of the requirements for converting the simulation to the ASC's 6600 system has been started. Each of these activities is discussed below.

A. Interim IRSS 3010 Interface

The interim 3010 interface installation has been completed. During the report period a remote clear button and manual clock switch were installed on the 9300 console. These enable the 9300 operator to ready the interface from the console and to make block transfers manually when the IRSS's clock signal is not on.

The IRSS/9300 system was tested using the IRSS real-time software. Problems were encountered with starting the software at the end of a 9300 write/read sequence following the IRSS's clock pulse. The problem was traced to the 3010 selector channel (SELCH) which was not lowering

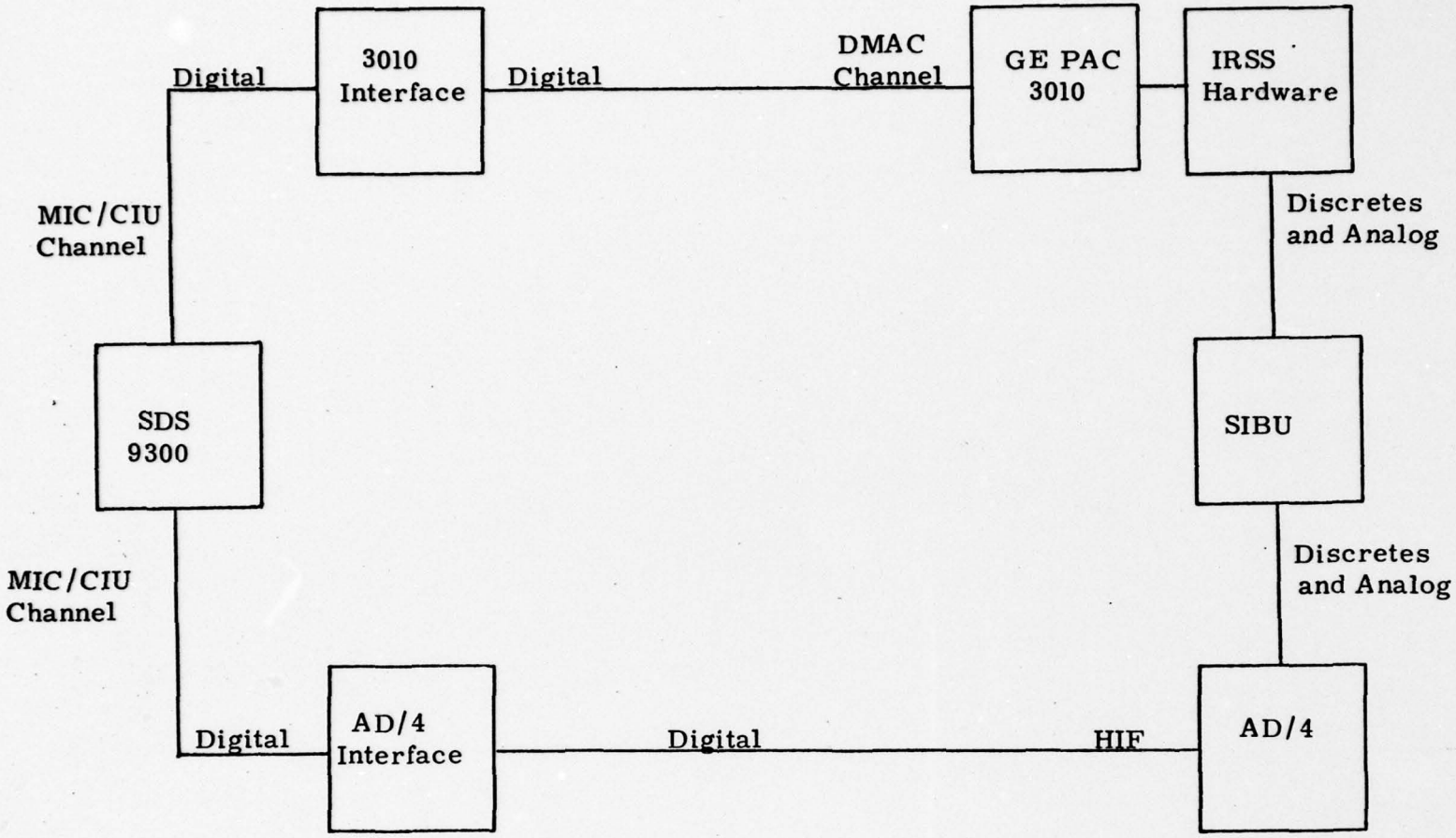

Figure II-1 Interim Simulation System

the memory bus request quickly enough. To fix this a hardware mod was made to release the request sooner and circuitry was added to generate an interrupt which would start the IRSS software at the end of the read sequence.

Subsequent tests were made using the 9300 to generate data and transfer it to the IRSS with the real-time software running. These tests were successful. Additional tests were later made where data was read from the AD-4, ADC channels and transferred to the IRSS where it was recorded on a strip chart. These tests were also successful

A program was generated to test the IRSS by writing all bit patterns from 0 to 2^{15} in 3010 memory locations $FOOO_{16}$ to $FFEO_{16}$. Documentation of this routine will be completed in the 2nd quarter. The program has been used periodically to check the interface and it has operated reliably during all tests.

B. AD-4 Checkout

The STINGER simulation is being transferred to a newly acquired AD-4 analog computer. BKD, using the interim AD-4 interface, checked out the AD-4's hybrid interface (HIF) and verified that necessary op codes were working. Two bad data bits were found in the HIF but otherwise the system seemed to be working properly. The ADC system, however, operates differently than the original AD-4's ADC system. With the old system, when a sequential MUX scan was performed the first ADC value read was garbage. It was followed, however, by 16 valid conversions. On the new system the first value read is the correct one. The observed difference is currently being examined. It has minor impact on the interim STINGER simulation requiring a simple software modification.

Two hardware additions were made to the AD-4 interface during the 1st quarter. A remote clear button was installed at the 9300 console and

a set of display lights was installed at the interface for trouble shooting and verification of system operation. Key interface signals displayed are:

- o $\not{Z}$0 - denotes 9300 input or output
- o WR - AD-4 write ready
- o EXECUTE - AD-4 op code execute signal
- o ACCESS - AD-4 op code load signal
- o T0
- o T1 AD-4 interface control bits
- o T2
- o PHASE - internal control
- o READY - AD-4 data ready
- o EREQ - interface request to 9300

The AD-4 check routines used by BKD should be upgraded to include functions which are not used in the STINGER simulation so that the software can be used in checkout of the other new analog machines providing a more comprehensive check. Currently the program exercises the following op-codes:

- o 002 Write DAC group register
- o 021 Write IRC
- o 022 Write IRA
- o 225 Read IRC
- o 026 Read IRA
- o 031 Set a DAC
- o 047 Do a sequential mode ADC read
- o 050 Write DGC's
- o 060 Read DGS's

To make the program generally applicable to AD-4 checkout the following op-code routines should be added:

000 Disable Hybrid on Condition and Read Status Bus

001 Read Out Status Bus

003 Read Out DAC Update Register

010 Set the Voltage Source

011 Generate a "Logic Step" Pulse

012 Set I Amplifier Scaling to X1

013 Generate a Simulatenous DAC Update Signal

033 Set DAC or POT and Increment Address

C. Simulator Interface Buffer Unit Checkout

Figure II-2 is a functional block diagram of the simulator interface Buffer Unit (SIBU). This hardware was installed and checked out during the report period. In addition a discrete display was added which will indicate the status of discrete signals used in the interim STINGER simulation. They are:

RECEIVED FROM IRSS

- o Initial Field Requested
- o Start Simulation
- o Emergency Shutdown
- o End of Problem
- o IRSS Ready

TRANSMITTED TO IRSS

- o Discrete #5
- o Target Acquired
- o Simulation Running
- o Normal Termination
- o Shutter Command #2
- o Shutter Command #6
- o Shutter Command #7

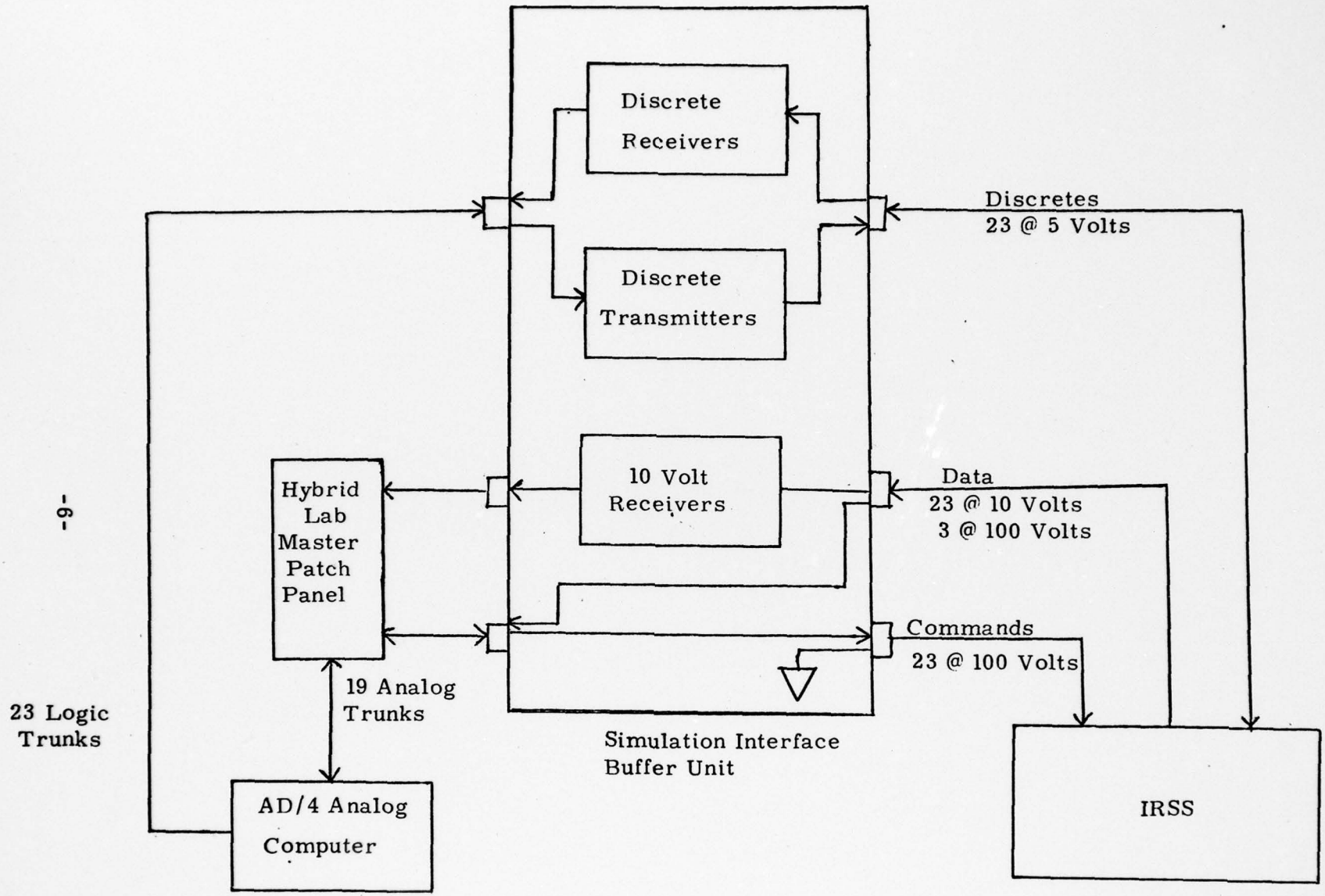

Figure II-2 SIBU Functional Block Diagram

D. STINGER Simulation Conversion

The interim STINGER simulation uses the IBM 7094 computer along with the XDS 9300 and interim interfaces to perform a closed loop simulation with the IRSS. Because all of this requipment is being replaced by the ASC's central hybrid facility using the CDC 6600, BKD is investigating the requirements for conversion to the new system.

A time phased approach is anticipated with replacement of the 7094 functions deemed most critical since that machine is due to be removed before the end of Fiscal Year 75. The next logical step is to remove the 9300 and interim interfaces from the simulation using the CDC 6600 direct cell link and AD-4 controller. Finally recompilation of the analog/hybrid program using the ASC's advanced software will complete the changeover.

III. PDDAIOS INSTALLATION

BKD efforts on the PDDAIOS installation have centered on two areas: IRSS direct cell installation and installation of the AD-4 controller. In the IRSS direct cell installation activity BKD is providing assistance in the localization of hardware problems associated with connecting the 3010 interface to the direct cell channel. Problems have included data path delays causing clocked strobes to load bad data and intermittent connections due to faulty connector pins. As of this writing the problems encountered have been solved and software testing is underway.

During the direct cell/3010 installation process BKD has assembled a set of simplified drawings of the 3010 interface hardware. These drawings are presented with discussion in Appendix A. This material will form the nucleus of a design/maintenance guide to be developed later in the contract.

BKD has provided trouble-shooting assistance in check out of the AD-4 controller. Primarily this effort has been associated with repair of logic faults in the AD-4 HIF. In several instances the interim AD-4 interface has been used to verify AD-4 performance by making comparative measurements on the interim system hardware. Check out of the AD-4 controller hardware will continue into the 2nd quarter.

APPENDIX A

APPENDIX A

The IRSS's 3010 Interface Design

The IRSS's interface to the CDC 6600 central computer makes use of a standard interdata 70 (i.e. GE PAC 3010) selector channel (SELCH) and universal interface module (UIM) both of which have been modified extensively. Documentation of the modification is limited to a set of corrected schematic diagrams.

During the process of trouble shooting the interface, an attempt has been made to generate a set of simplified schematics which will aid in understanding the hardware's operation. The following paragraphs present a "First Pass" at describing the system.

Figure A-1 in a block diagram of the hardware components showing their interconnection. The driver/receiver cards shown are 75107 and 75110 differential receivers and transmitters which are used to send signals over the 160 foot cable between the IRSS and the central computer. The UIM is used as local receiver/transmitter card for communicating with the SELCH. In a typical INTERDATA application the UIM would be used by the CPU to set up a selector channel for acessing memory. In this application the UIM has no connection to the CPU and serves only to route data and control signals to the appropriate selector channel connection. The SELCH provides an address register, a data register and circuity for generating control signals for accessing the computer system's memory bus directly. The interface hardware (i.e. diver/receiver card, UIM and SELCH) is activated only by the external device, in this case the CDC 6600 direct cell channel. The interface's SELCH channel has priority over the 3010 CPU so that a request for memory access from the 6600 would be serviced before a request from the CPU.

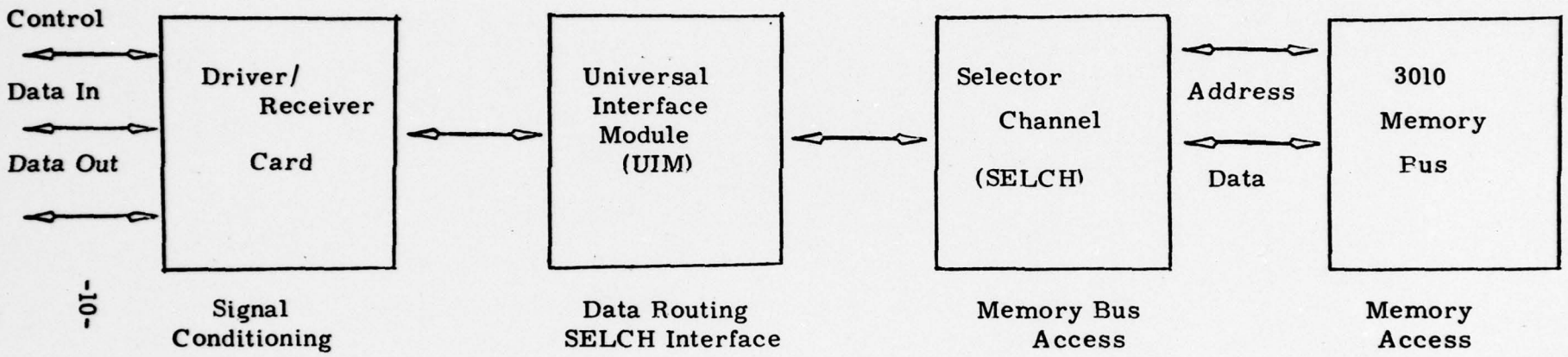

Figure A-1 Functional Block Diagram of IRSS 3010 Interface

1. Control signals. Six control signals are communicated between the 6600 and the 3010 interface; they are WRITE, ADDRESS, DATA VALID, ADDRESS VALID sent from the 6600 to the 3010 and SYNCH 1 and SYNCH 2 sent from the 3010 to the 6600.

The interface operates in one of two modes, write or read. In both modes the external device sends over a 3010 memory address to be read or written and tells the 3010 interface that the address is there by raising ADDRESS VALID.

If the mode selected is write mode the 6600 raises WRITE along with ADDRESS VALID and receives a SYNCH 1 from the 3010 when the address has been strobed into the SELCH's address register. The 6600 then places the 16 data bits to be written on the data lines and raises DATA VALID. The 3010 interface uses DATA VALID to request a memory access cycle and returns a SYNCH 2 signal to the 6600 indicating that the data has been accepted (i. e. strobed into the SELCH channel data register.) Note that no signal is generated to tell the external device that the data has been put into memory rather the interface requires that the data lines be held up long enough to assure memory service is acquired before another access is requested by the 6600.

If the read mode is selected the 6600 raises READ along with ADDRESS VALID. These signals are used to make a memory request. At the conclusion of the memory cycle in which the data requested is read out, the SELCH channel generates a SYNCH 2 indicating the data can be read by the 6600.

Figure A-2 shows the paths of the external control signals and how SYNCH 1 and SYNCH 2 are generated by the SELCH.

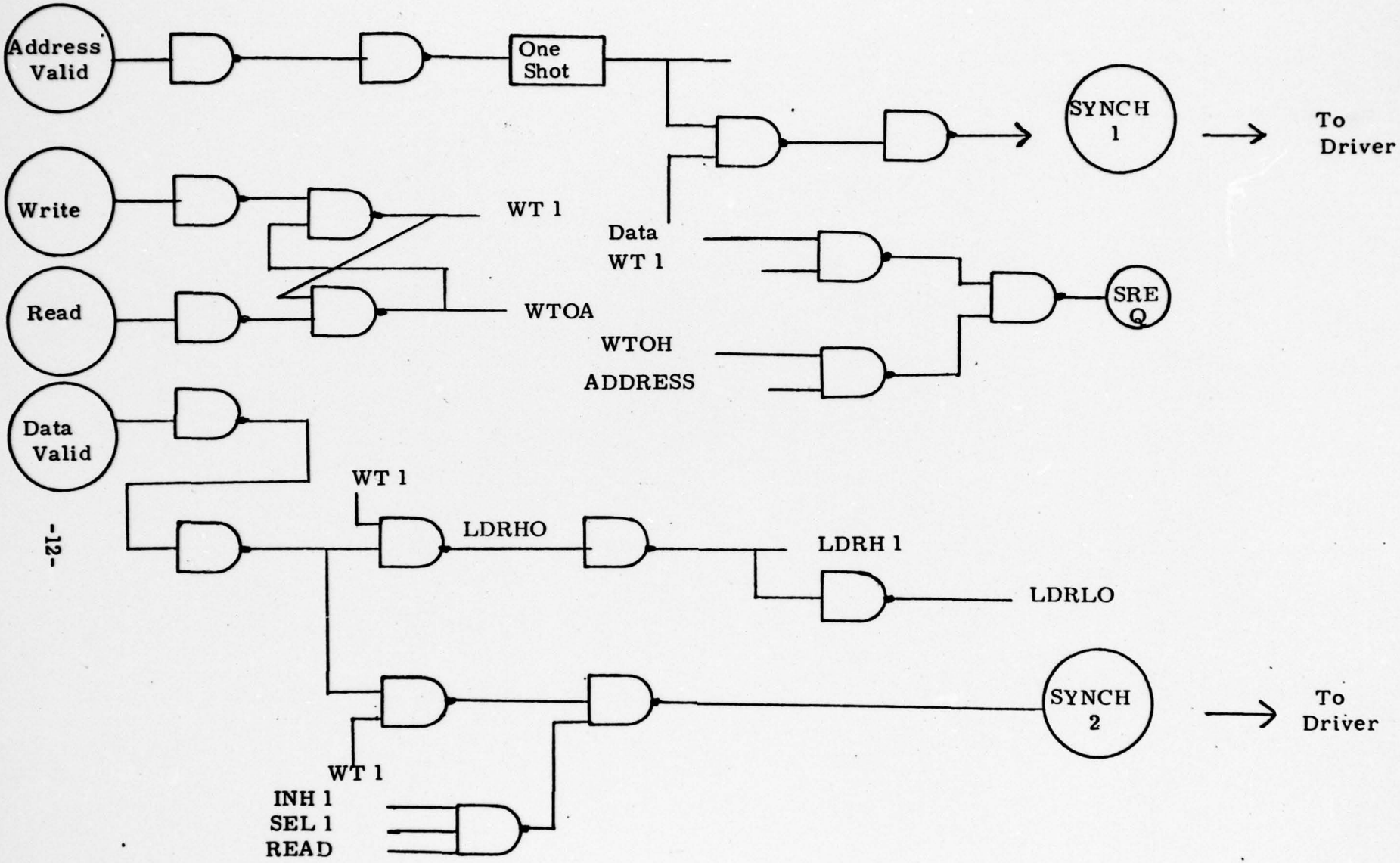

Figure A-2 3010 Interface Control Signals

2. Memory Bus Control Signals. (Figure A-3). The SELCH channel requests a memory cycle by raising REQ. The memory responds by sending over an enabling signal ENO which sets SEL 1 in the SELCH to indicate that the SELCH has been selected. The trailing edge of Inhibit (INHO), from the Processor, indicates the end of the memory cycle. This edge, unless the SELCH has dropped REQ in time to remain selected during the next cycle, will cause the SEL flip-flop to reset. Two pulses, End of Memory Transfer (EMXO) and Inhibit (INHOP), are generated by the leading and trailing edges of INHO respectively. EMXO is used to indicate the end of the memory transfer.

In the Memory Read Mode, the Memory Data Register (MDR) is cleared by Clear Data Register (CDRO) which is generated by the trailing edge of REQ1. Write Not (WTOA) is added with SEL 1 to form Enable Memory Data Read (ENMDR1), which gates the contents of the MDR onto the Memory Data Lines for the restore portion of the memory cycle. The contents of the memory location accessed is gated to the direct set inputs of the MDR by Enable Memory Strobe (ENMS1).

When writing to memory, the contents of the DATA Buffer are gated onto the Memory Data Lines by Enable Memory Data Write (ENMDW1), when selected. A memory Write operation is indicated to the Processor by activating WRTOA.

3. Data I/O Path. Figure A-4 depicts the path into the SELCH's data register. The path consists of nine gates including the differential receiver and one gate on the UIM. The data register is loaded by two signals, LDRHO and LDRLO, (Load data register high order bits and load data register low order bits) which are generated by DATA VALID

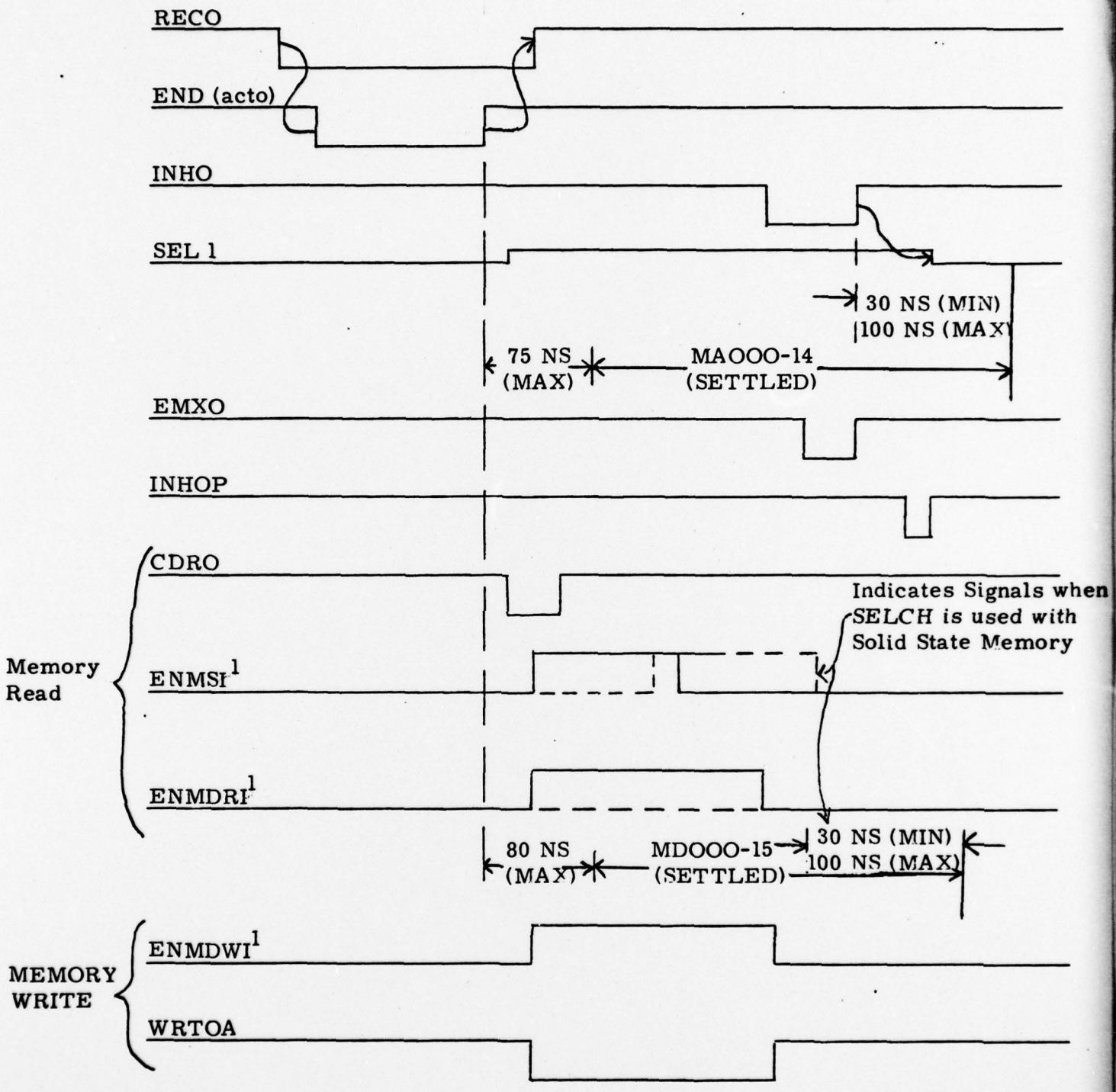

Figure A-3 3010 Memory Bus Timing Diagram

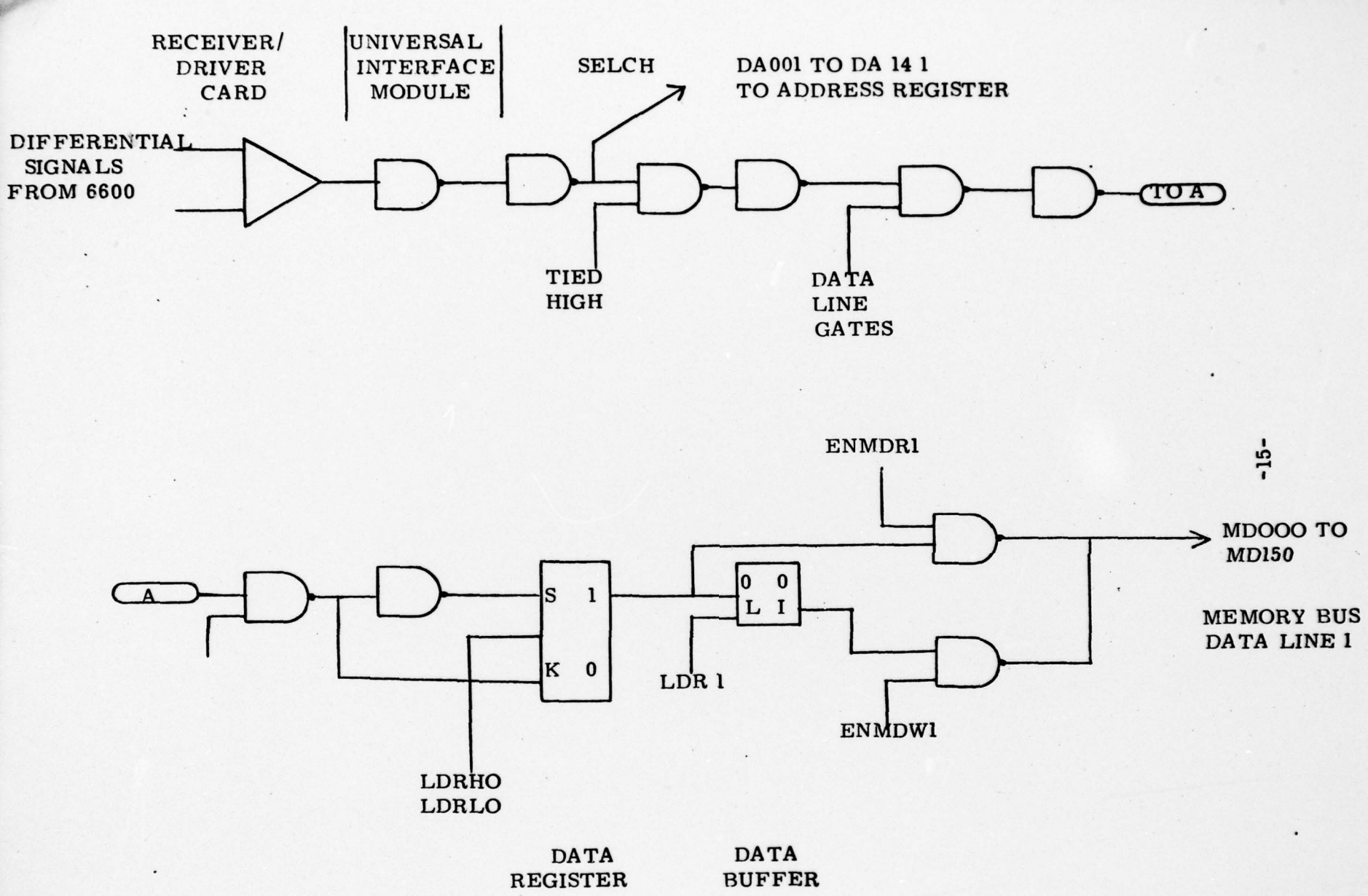

Figure A-4 Input Data Path Through 3010 Interface

and WRITE. When the SELCH's memory request is serviced the data register is enabled onto the memory bus by ENMDW1 which is generated by WT1, essentially WRITE and SEL 1.

Figure A-5 shows the path followed by data being read from the 3010 memory. The data is gated from the memory bus into the SELCH data register by ENMS 1 which is generated by WTOA (essentially READ), SEL 1, and INHO (memory bus signals indicating the SELCH is selected and that the data can be read now). The data is gated into the same flip-flop register that is used for writing data into memory and during the second half of the memory cycle the data read from memory is re-written, being strobed onto the memory bus by ENMDR 1. The data read is subsequently gated through nine logic stages including a data buffer in the UIM before being sent to the 6600.

4. Address Path. Figure A-6 shows the path followed by data destined for the SELCH's address register. The register is loaded by LARHO and LARLO which are enabling signals generated essentially by the ADDRESS VALID signal. The address register lines are gated onto the memory bus address lines by SEL 1, the memory bus signal indicating that the SELCH has been selected for the read memory cycle.

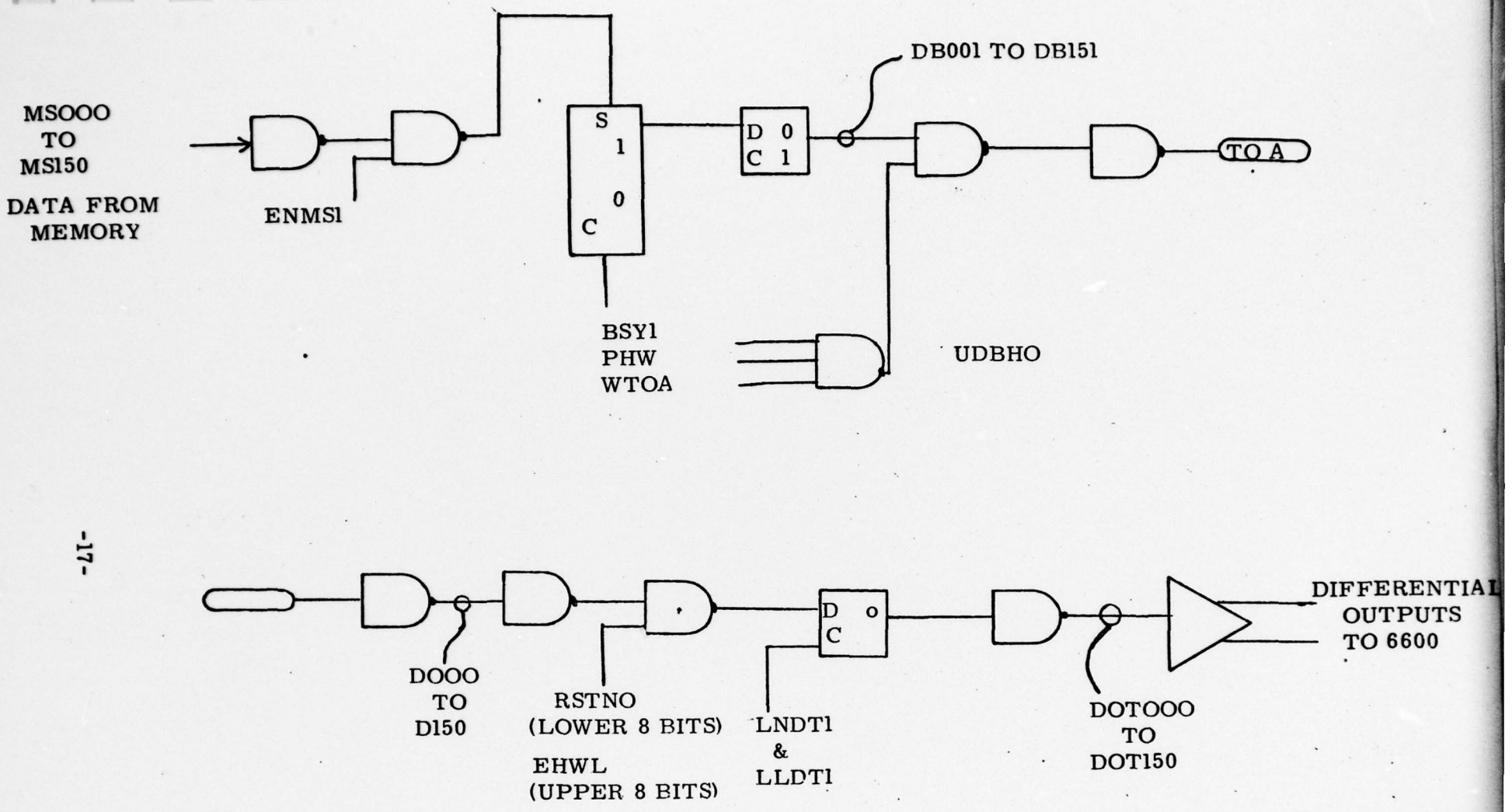

Figure A-5 Output Data Path Trough 3010 Interface

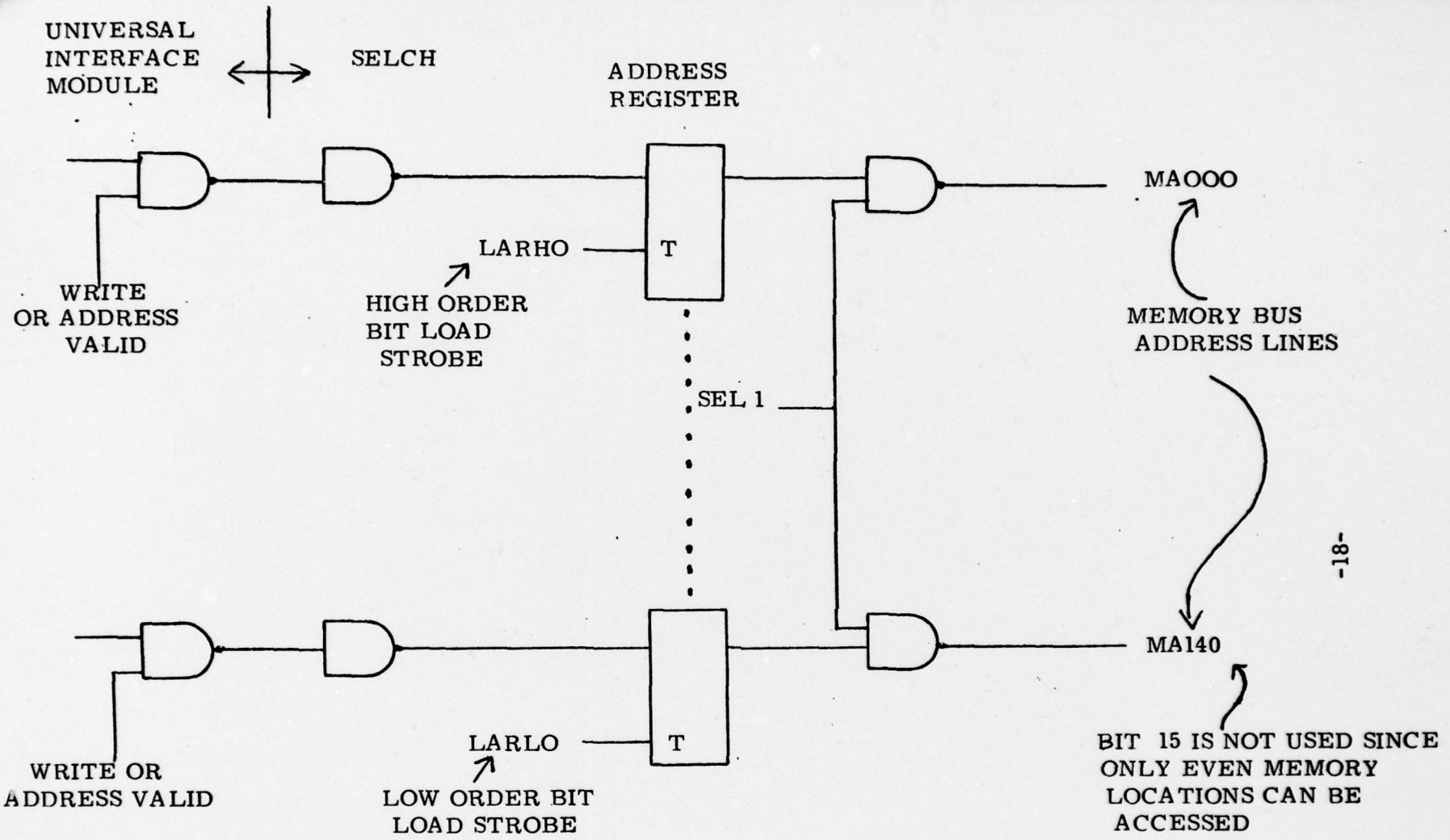

Figure A-6 Address Path in 3010 Interface