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PROFILING OF GAAS USING A DISTRIBUTED RC STRUCTURE.(U)
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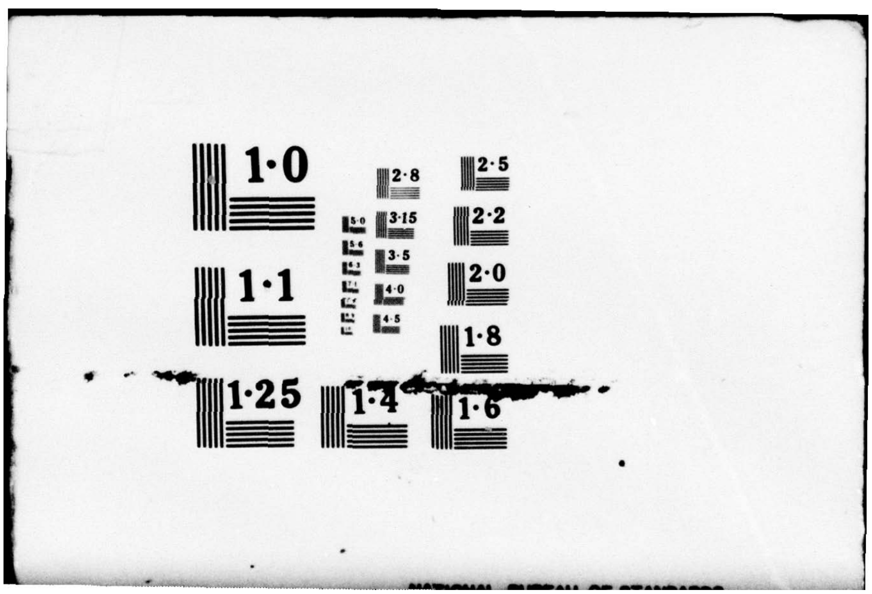
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FINAL REPORT

PROFILING OF GaAs USING A DISTRIBUTED RC STRUCTURE

By

Roy A. Colclaser

The University of New Mexico

Department of Electrical Engineering
and Computer Science
and
Bureau of Engineering Research
Albuquerque, New Mexico 87131

Final Report No. EE-251(78)AFOSR-550-1

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Research Objectives

The objective of this research was to compare the results of an experiment using a distributed RC structure to evaluate both the impurity profile and mobility of ion-implanted layers in GaAs with the results of the differential Hall-effect technique for the same type of samples. The distributed RC structure experiments were to be performed at The University of New Mexico (UNM) and the differential Hall-effect experiments were to be performed at AFAL-DHR at WPAFB. The theory of the distributed RC technique is presented in the Appendix.

Significant Accomplishments

The major accomplishment of this project was to develop a processing technique for fabricating the distributed RC structure. Processing difficulties were encountered at both AFAL-DHR and UNM. Only one set of useable samples were received from AFAL-DHR. These were received in late September, and were subsequently rendered useless due to processing at UNM.

The process failure was involved with the definition of the Au-Ge ohmic contact pattern. The process, which had been developed during the summer of 1976 while the principal investigator was working at AFAL-DHR as part of the USAF-ASEE Summer Faculty Research Program, involved the use of a Film Microelectronics C-35^R standard gold etch (based on KI) to delineate the pattern, followed by a germanium etch (H_2O_2 (30%): HF (49%):H_2O in the ratio 1:1:4). The C-35 etchant produced a slow GaAs etch which was not observed during the processing at AFAL-DHR. This effect was sufficient to remove the implanted layer in the regions between the contacts, leaving isolated contact regions. For this reason, it was necessary to use a photoresist lift-off technique to define the ohmic contact regions, and this was subsequently demonstrated on another set of samples in November. Unfortunately, this alternate set of samples was alloyed at too high a temperature, resulting in non-ohmic contacts.

A major difficulty in the experiments was due to the mask set which was supplied from AFAL-DHR. A composite drawing of this mask set is shown in Figure 1. A significant portion of the mask is used to define a Van Der Pauws pattern for Hall-effect measurements, and a number of distributed structures too small for the intended experiments, resulting in only three to six useable structures per sample. Also, the mesa etch removed approximately 75 percent of the surface. It was desirable to use the mesa etch only for the isolation of the individual structures by providing moats around the devices, and to fabricate a high density of useable structures. For this reason, a new mask set was designed and fabricated at UNM. A composite drawing of the new mask set is shown in Figure 2. Unfortunately, AFAL-DHR was unable to supply any additional samples during December, so that these masks have not yet been employed.

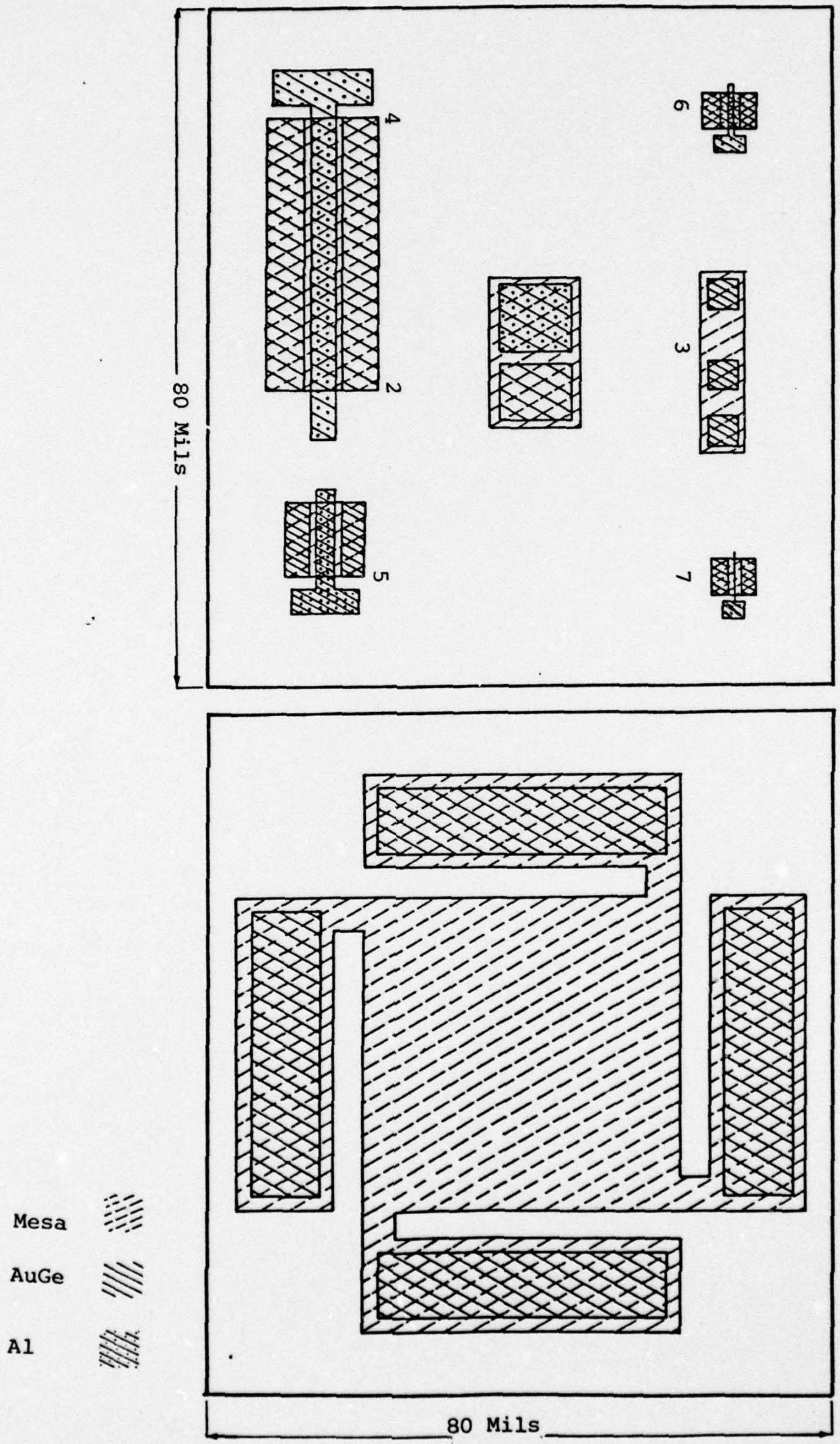


Figure 1. Composite Mask Set, AFAL-DHR

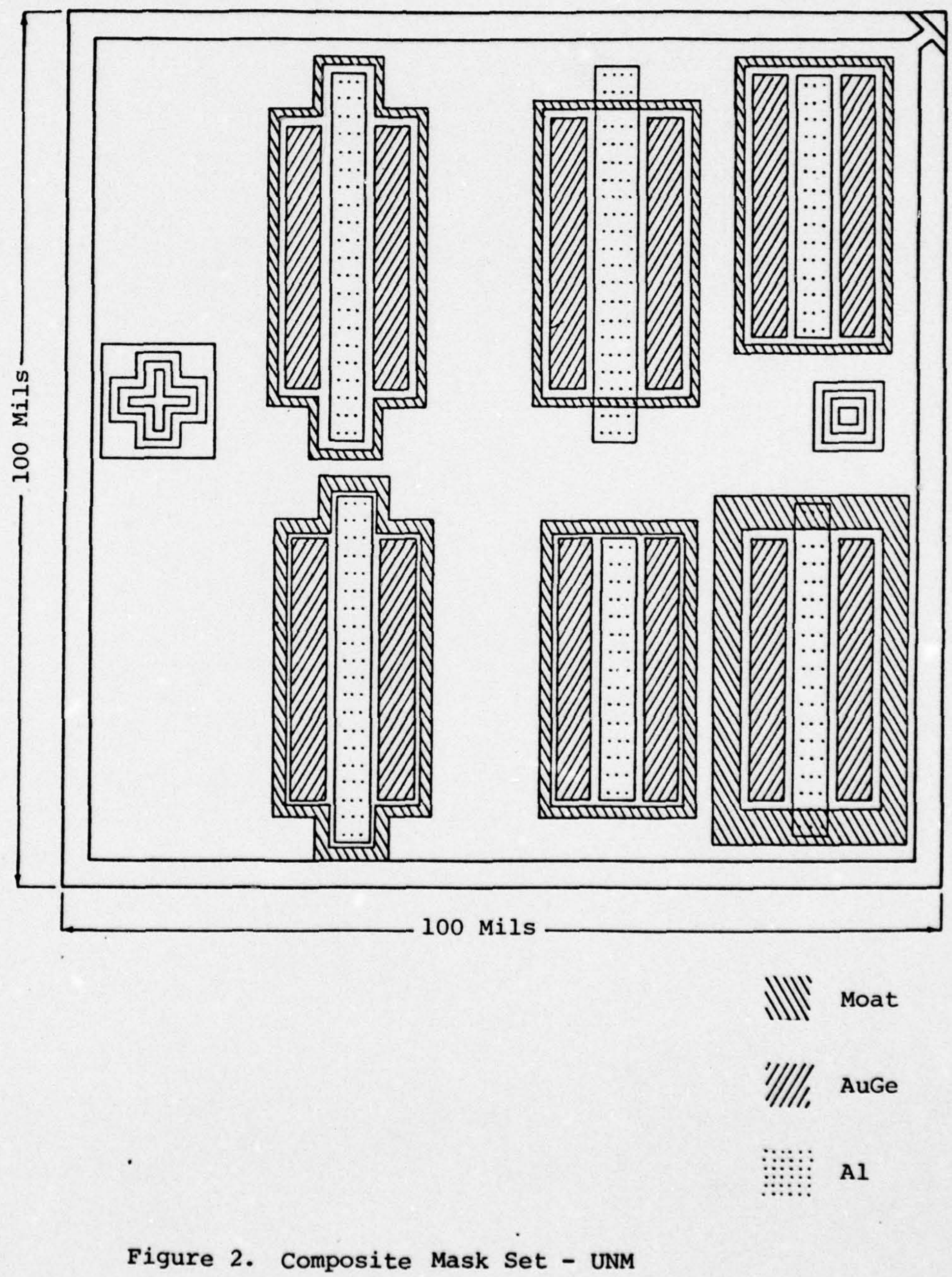


Figure 2. Composite Mask Set - UNM

In order to eliminate the over-temperature alloy problem encountered with the alternate sample set, a new alloy fixture was made at UNM. This was also not used, since samples were not available.

The basic process has now been developed for fabricating the RC distributed structures. This consists of:

1. Definition of moat pattern
2. Moat etch ($H_2SO_4:H_2O_2:H_2O$,1:1:5)
3. Definition of contact pattern
4. Deposition of Au-Ge
5. Lift-off process
6. Alloy of contacts (425°C in H_2)
7. Definition of gate pattern
8. Deposition of Al
9. Lift-off process

Personnel

Principal Investigator:

Dr. Roy A. Colclaser - 2 man-months

Graduate Student:

Robert A. Pezzano - 1/4 man-month

Undergraduate Student:

Mark W. McDermott - 1/4 man-month

Relevant Information

In the original proposal for this work, it was intended that most of the device fabrication would be performed in July and August. The first samples supplied by AFAL-DHR were not available until 1 August, and these samples had been annealed at too high a temperature (950°C) resulting in a breakdown of the encapsulating layer. The result of this is a highly damaged surface. Since such a large surface area was exposed to the mesa etch, and the damaged areas were preferentially attacked, these samples were useless, even for process evaluation. The principal investigator requested two sets of samples by 1 October. Only one set was available, and these were rendered useless by the contact delineation etch. An alternate set of samples was made available on 25 November. These samples were alloyed at too high a temperature and also provided no measureable devices. The new mask set and improved alloy fixture were prepared, but AFAL-DHR was unable to supply additional samples during the grant period.

APPENDIX

INTRODUCTION

Several techniques have been developed for the determination of impurity concentration profiles in semiconductors [1]. The most accurate of these methods use radioactive tracer elements and controlled layer removal (such as anodic oxidation) to determine the total impurity profile. Of more interest in device applications are evaluation techniques which determine the electrically active impurity profile.

In addition to the impurity profile, it is of great interest to determine the mobility of the majority carriers, and its dependence on position within the material. One highly successful technique for measuring both quantities is the differential Hall effect measurement. This is performed by measuring the conductivity and Hall effect on a sample in a series of measurements, with layer removal performed after each set of measurements. The result is an accurate determination of the electrically active impurity concentration and Hall mobility as a function of the distance from the original surface of the material. The Hall mobility is related to the drift mobility by a factor (between 1 and 2) which depends upon the scattering mechanisms experienced by the majority carriers within the crystal.

The method discussed in this report consists of fabricating a device structure on the surface of the sample and measuring the electrical impedance of this structure. Proper interpretation of the data yields a method for estimating the electrically active impurity concentration and the drift mobility as a function of the position relative to the surface. This method has been used previously to evaulate epitaxial GaAs layers [2] [3]. The objective of this project is to determine if this technique may also be applied to ion-implanted regions in GaAs, and to determine limitations of the technique.

THE C-V, D-V METHOD

The method to be considered in this report consists of fabricating an RC distributed structure on the surface of the GaAs through which the ions have been implanted, measuring both the capacitance (C) and dissipation factor (D) as a function of DC bias voltage at room temperature, and calculating the electrically active impurity concentration (N) and the mobility (μ) from the measured data. The structure consists of making ohmic contacts to the implanted layer to form the resistance, and a Schottky barrier in an area between the ohmic contacts to form the capacitance. The measurements were made using a Hewlett-Packard Model 427A Automatic Capacitance Bridge. The calculations are based on the equations derived in the following paragraphs.

There are two sets of boundary conditions which can be established for the measurements applicable to this method. The structure is shown schematically in Figure A. The first possible boundary condition is to make v_{13} the sum of the DC bias voltage V and the AC measuring signal $\overline{V}_1(j\omega)$, and leave terminal 2 open ($i_2 = 0$). The second possible boundary condition is to make $v_{13} = v_{23}$ where v_{13} is the same as under the first situation. The measurements under the second boundary condition gave more consistent results, and this will be the situation considered in the remainder of the report.

Under the condition that $v_{13} = v_{23}$, $\overline{I}_1(j\omega) = \overline{I}_2(j\omega)$. Therefore, the AC impedance measured under this situation is

$$\overline{Z}(j\omega) = \frac{\overline{V}_1(j\omega)}{2\overline{I}_1(j\omega)}$$

From transmission line theory,

$$\overline{Z}(j\omega) = \frac{r}{2z\sqrt{j\omega rc}} \coth \frac{L}{2}\sqrt{j\omega rc}$$

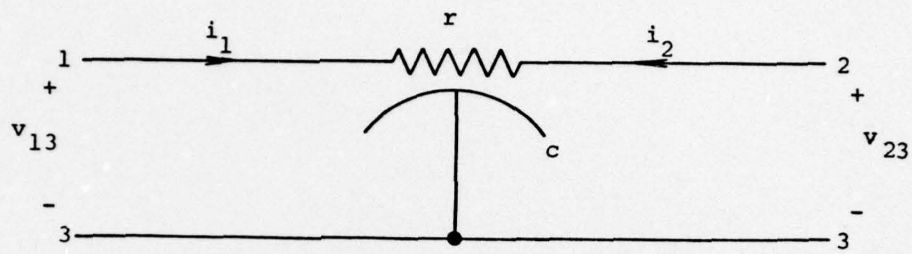
where: r is the sheet resistance in ohms per square

z is the width of the structure

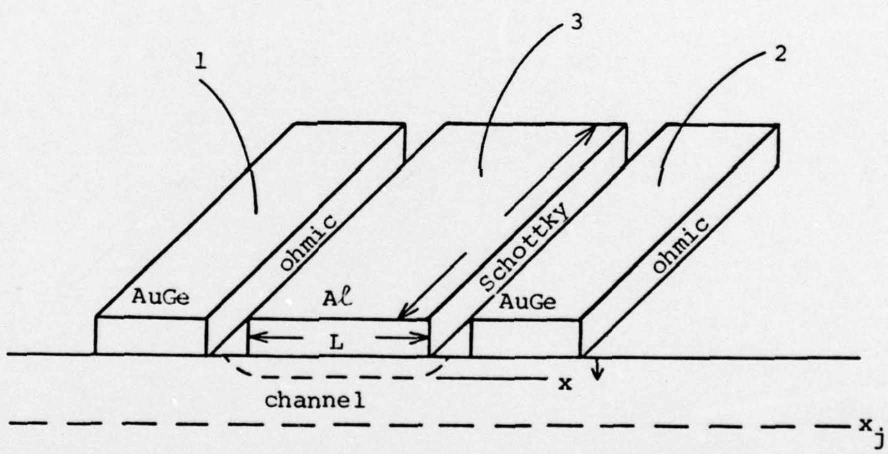
c is the capacitance per unit area

L is the length of the structure

ω is the angular frequency



a) Schematic



b) Pictorial

Figure A. The Basic RC Distributed Structure.

z and L are in centimeters, and c is in farads per square centimeter. It can be shown that

$$\overline{Z}(j\omega) = \frac{r}{2\sqrt{2}z\sqrt{\omega rc}} \left[\frac{\left(\cosh \frac{L}{2}\sqrt{\frac{\omega rc}{2}} \sinh \frac{L}{2}\sqrt{\frac{\omega rc}{2}}\right)}{\left(\sinh^2 \frac{L}{2}\sqrt{\frac{\omega rc}{2}} + \sin^2 \frac{L}{2}\sqrt{\frac{\omega rc}{2}}\right)} - \frac{\left(\cos \frac{L}{2}\sqrt{\frac{\omega rc}{2}} \sin \frac{L}{2}\sqrt{\frac{\omega rc}{2}}\right)}{\left(\sinh^2 \frac{L}{2}\sqrt{\frac{\omega rc}{2}} + \sin^2 \frac{L}{2}\sqrt{\frac{\omega rc}{2}}\right)} - j \frac{\left(\cosh \frac{L}{2}\sqrt{\frac{\omega rc}{2}} \sinh \frac{L}{2}\sqrt{\frac{\omega rc}{2}}\right)}{\left(\sinh^2 \frac{L}{2}\sqrt{\frac{\omega rc}{2}} + \sin^2 \frac{L}{2}\sqrt{\frac{\omega rc}{2}}\right)} - j \frac{\left(\cos \frac{L}{2}\sqrt{\frac{\omega rc}{2}} \sin \frac{L}{2}\sqrt{\frac{\omega rc}{2}}\right)}{\left(\sinh^2 \frac{L}{2}\sqrt{\frac{\omega rc}{2}} + \sin^2 \frac{L}{2}\sqrt{\frac{\omega rc}{2}}\right)} \right]$$

for $\omega << \frac{1}{rc}$

$$\overline{Z}(j\omega) \simeq \frac{rL}{12z} - j\,\frac{1}{\omega zLc}$$

Therefore, for the proper frequency range, the measured impedance appears to be a frequency independent resistance, designated

$$R_S = \frac{rL}{12z} \qquad (1)$$

connected in series with a frequency independent capacitance, designated

$$C_S = zLc \qquad (2)$$

The condition on ω is met when the dissipation factor,

$$D = \omega R_S C_S \qquad (3)$$

is less than 0.333.

The quantities measured are D and the shunt capacitance, C_{SH}, at a given frequency. A small parasitic capacitance, C_{PAR}, due partly to the diode structure and partly to the measuring apparatus is included in C_{SH}. The value of C_{PAR} can be determined by increasing the reverse bias until no change is observed in the capacitance. The value of C_S can be determined from

$$CS = (C_{SH} - C_{PAR})(1 + D^2) \tag{4}$$

The effects of a parasitic resistance R_{PAR} are included in D. R_{PAR} represents the resistance between the ohmic contacts and the edge of the diode. This effect can be removed by using two structures which are identical except that the distance from the ohmic contacts to the diode edges in structure 2 are twice as large as those distances in structure 1. A first order correction in D is given by

$$D = 2D_1 - D_2 \tag{5}$$

Another parasitic effect, which can alter the measurement of D, is the leakage current of the diode. Corrections for diode leakage were not made in the measurements reported below.

Both c and r are functions of DC bias voltage. The r is the sheet resistance of the channel between the junction, formed by the ion-implanted impurities and the substrate, and the depletion region due to the reverse biased Schottky barrier. The width of this depletion region depends on the magnitude of the reverse bias. The capacitance also depends upon the width of the depletion region, as well as the carrier concentration.

The capacitance per unit area of a reverse biased Schottky barrier diode is given by

$$c = \frac{\varepsilon_o \varepsilon_r}{x} = \frac{\delta Q_C}{\delta v} \tag{6}$$

where:

ε_o is the permittivity of free space

ε_r is the relative permittivity of the material

x is the distance between the surface and the edge of the depletion region

Q_C is the charge per unit area in the channel

V is the magnitude of the reverse bias voltage.

For an n-type semiconductor with slowly varying N with x,

$$Q_C = -eN(x_j - x) \tag{7}$$

where:

e is the magnitude of the charge on an electron

xj is the distance from the surface to the junction formed between the substrate and the ion-implanted layer.

From Gauss' Law,

$$\delta Q_C = \varepsilon_o \varepsilon_r \delta E$$

where E is the electric field intensity and

$$\delta V \approx x \delta E$$

then

$$\delta V \approx \frac{x}{\varepsilon_o \varepsilon_r} \delta Q_C = \frac{xeN}{\varepsilon_o \varepsilon_r} \delta x$$

$$\delta V \approx \frac{eN}{2\varepsilon_o \varepsilon_r} \delta (x^2)$$

from (5)

$$N \approx \frac{2\varepsilon_o \varepsilon_r}{e} \frac{\delta V}{\delta \left(\frac{\varepsilon_o^2 \varepsilon_r^2}{C^2} \right)}$$

$$N \approx \frac{2}{e\varepsilon_o \varepsilon_r} \frac{\delta V}{\delta \left(\frac{1}{C^2} \right)}$$

$$N \approx - \frac{C^3}{e\varepsilon_o \varepsilon_r} \left(\frac{\delta c}{\delta V} \right)^{-1} \tag{8}$$

The sheet resistance of the channel is given by

$$r = \frac{1}{eN\mu (x_j - x)} = \frac{-1}{\mu Q_C}$$

from (6)

where μ is the drift mobility of the electrons

Then $\delta \left(\frac{1}{r} \right) = -\mu \delta Q_C$ if μ is assumed to vary slowly with x.

$$\frac{\delta \left(\frac{1}{r} \right)}{\delta V} = -\mu \frac{\delta O_C}{\delta V} = -\mu c$$

or

$$\mu = -\frac{1}{C}\frac{\delta\left(\frac{1}{r}\right)}{\delta V} \tag{9}$$

N and μ, as functions of x, can be related to the measured and corrected quantities, V, ω, C_S, and D by combining equations (1), (2), (3), (6), (8), and (9). Resulting in

$$x = \frac{\varepsilon_o \varepsilon_r zL}{C_S} \tag{10}$$

$$N = -\frac{C_S^{\,3}}{e\varepsilon_o \varepsilon_r z^2 L^2}\left(\frac{\delta C_S}{\delta V}\right)^{-1} \tag{11}$$

$$\mu = -\frac{L^2 \omega}{3C_S}\;\frac{\delta\left(\frac{C_S}{D}\right)}{\delta V} \tag{12}$$

Note that these relationships are approximations, and will yield more accurate information if N and μ are slowly varying functions of x.

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The objective of this research was to compare the results of an experiment using a distributed RC structure to evaluate both the impurity profile and mobility of ion-implanted layers in GaAs with the results of the differential Hall-effect technique for the same type of samples. The basic process has been developed for fabricating the RC distributed structures. This consists of: Definition of moat pattern; Moat etch ($H_2SO_4:H_2O_2:H_2O$, 1:1:5); Definition of contact pattern; Deposition of Au-Ge; Lift-off process; Alloy of contacts

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(425°C in H_2); Definition of gate pattern; Deposition of Al, and Lift-Off Process. The C-V, D-V method involves an RC distributed structure on the surface of the GaAs through which the ions have been implanted, measuring both the capacitance (C) and dissipation factor (D) as a function of DC bias voltage at room temperature, and calculating the electrically active impurity concentration and the mobility from the measured data. The structure consists of making ohmic contacts to the implanted layer to form the resistance, and a Schottky barrier in an area between the ohmic contacts to form the capacitance.