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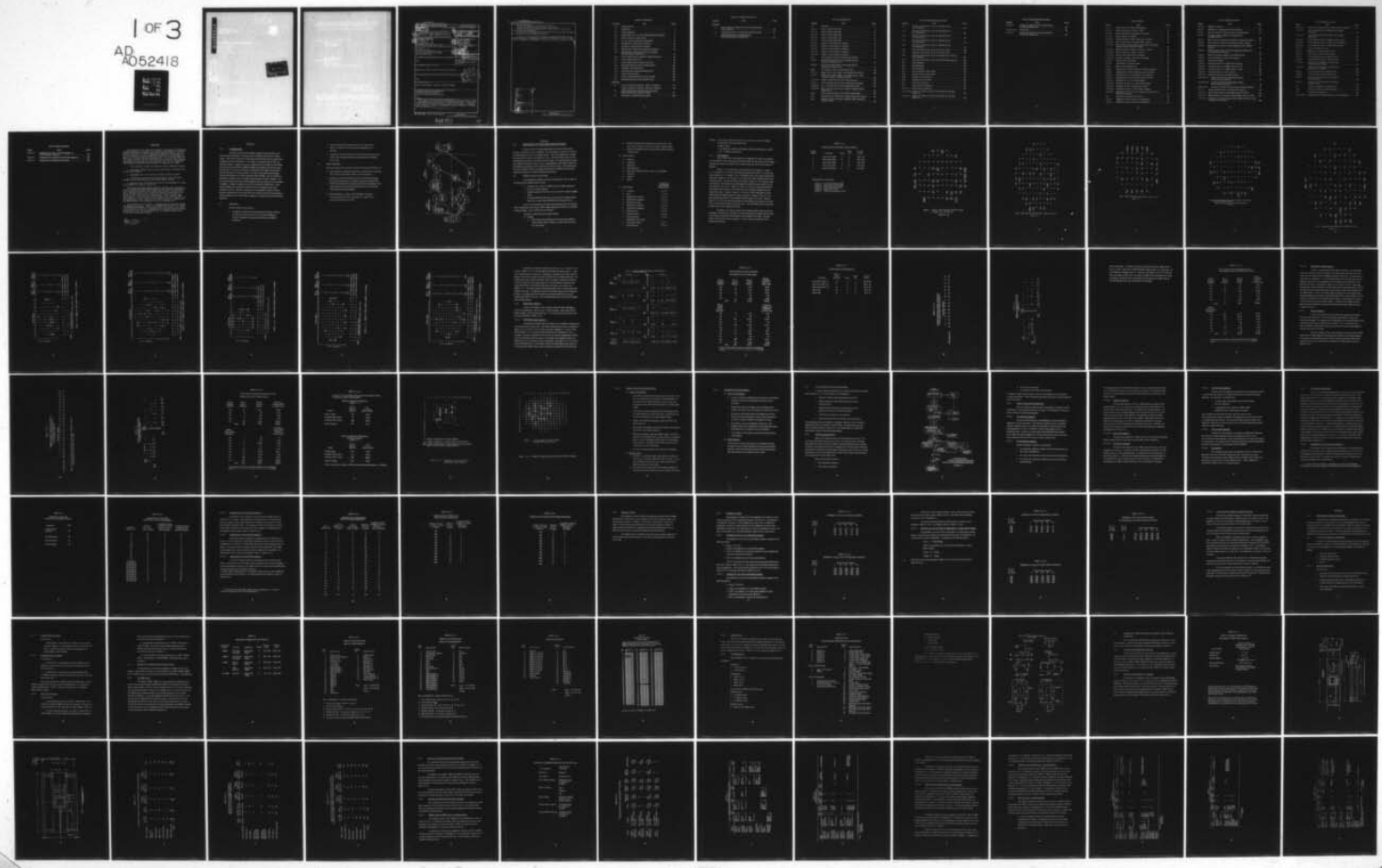

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Complex Microcircuit Screening Tests
LSI Wafer Fabrication Controls
LSI Control and Screening Techniques

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The purpose of this study was to establish an alternate procedure in lieu of High Magnification preseal visual for complex microcircuits. In-line wafer process controls were developed which provide effective control of the wafer visual conditions. Changes to MIL-STD-883 have been recommended to implement this process control.

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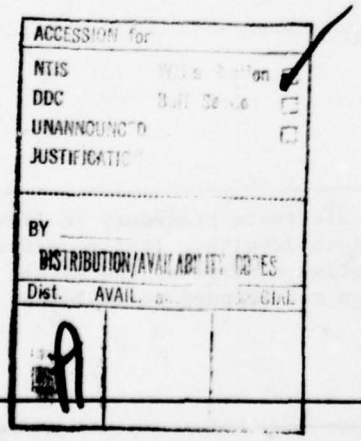
The study approach was to:

Perform wafer mapping of visual defect locations,
Develop in-line wafer process controls from this data,
Perform preliminary testing with known visual defects on LSI chips to verify alternate test methods, and
Perform final verification testing on complex LSI wafer product processed in accordance with the recommended procedures.

In addition, it was found that a package problem generated numerous bond failures which were not adequately detected by 10 temperature cycles. A change has been recommended to MIL-STD-883 to perform 100 cycles of temperature cycling.



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EVALUATION

The objective of this study was to evaluate existing MIL-STD-883 Quality Assurance Procedures and establish, if necessary, new methods for screening complex microcircuits. Specific emphasis was placed on preseal visual inspection, because of the difficulties being encountered in performing this test on microcircuits having layered metallization or for devices where the complexity is greater than 250 equivalent gates. This study considered the risk associated with relaxing or eliminating certain device visual screening requirements and replacing them with in-process wafer and lot inspections. The following investigations were performed in conducting this study:

a. Visual mapping of wafers to locate and classify defective circuits.

b. Preliminary testing of devices with known defects to develop alternate testing procedures.

c. Development of in-line controls to identify defective wafers.

d. Verification testing of devices fabricated on wafers that were subjected to the newly developed in-line wafer control screens.

e. Analysis of the verification test results and development of screening procedures for complex microcircuits.

This study successfully demonstrated that alternate test procedures in lieu of the 100% high magnification internal visual inspection are feasible. In the verification testing, the proposed wafer controls, in conjunction with a low magnification visual inspection, proved to be effective in minimizing failures resulting from visual defects, while at the same time, increasing the initial electrical probe yields. These alternate tests, which consist of a specific wafer control procedure and minor changes in the low magnification visual inspection, will make it possible to require the high magnification visual inspection, only as an optional test.

The end product of this study is a proposed new test method for screening complex microcircuits. RADC, as the Preparing Activity for MIL-STD-883 "Test Methods and Procedures for Microelectronics" will utilize the results of this study as the basis for recommending, to Government/Industry sources, the adoption of this new test method for use in screening complex microcircuits for military applications.

Edward P. O'Connell

EDWARD P. O'CONNELL
Project Engineer

SECTION 1

1.0 INTRODUCTION

Problems are resulting from attempts to employ existing screening, and quality assurance procedures in the procurement of complex microcircuits for military systems. This is due to advances in device processing technology that have significantly changed device physical dimensions. For example, in the period 1968 to 1974, the following changes in complexity occurred: components/chip increased from 50 to 3000; chip area (sq mils) increased from 2000 to 20,000; area/component (sq mils) decreased from 10 to 0.2. This trend is continuing as evidenced by the usage of microprocessors and other LSI devices in military systems. As a result of this advancing technology, Precap Visual Inspection as currently specified in MIL-STD-883, cannot be effectively performed on LSI devices due to the larger chips and smaller area per component. Yet the use of LSI devices has increased the probability of the occurrence of visual anomalies. In addition, a number of complex microcircuits use multilevel metallization, or have unique processes which preclude the performance of any reasonable Precap Visual Inspection of the die. Therefore, procedures must be developed to identify Visual Inspection requirements that can be most effectively performed during in-line processing as sampling inspection tests on each wafer as opposed to the present end-of-the-line Precap inspections.

1.1 OBJECTIVES

The basic objective of this study is:

- to establish an effective screening and quality assurance procedure for complex microcircuits by use of in-line wafer sampling inspection as opposed to the present end-of-the-line acceptance inspections,

- to develop alternate testing procedures that will detect known defects in complex microcircuits as part of packaged device screening,
- to perform a final verification test to evaluate the effectiveness of the in-line wafer sampling and alternate testing procedures developed by this study.

1.2 STUDY APPROACH

This study consists of four activities as shown in the study plan of Figure 1.2.

- Wafer mapping of completed complex device wafer defects and development of in-line wafer process controls by Visual Inspection.
- Preliminary verification testing consisting of screening of packaged devices with known defects to develop an alternate testing procedure.
- Verification testing of devices produced utilizing the developed in-line wafer process controls to evaluate the effectiveness of those controls and the alternate testing procedure.
- Recommendation for changes to MIL-STD-883 to incorporate screening and quality assurance procedures for complex microcircuits as developed by this study.

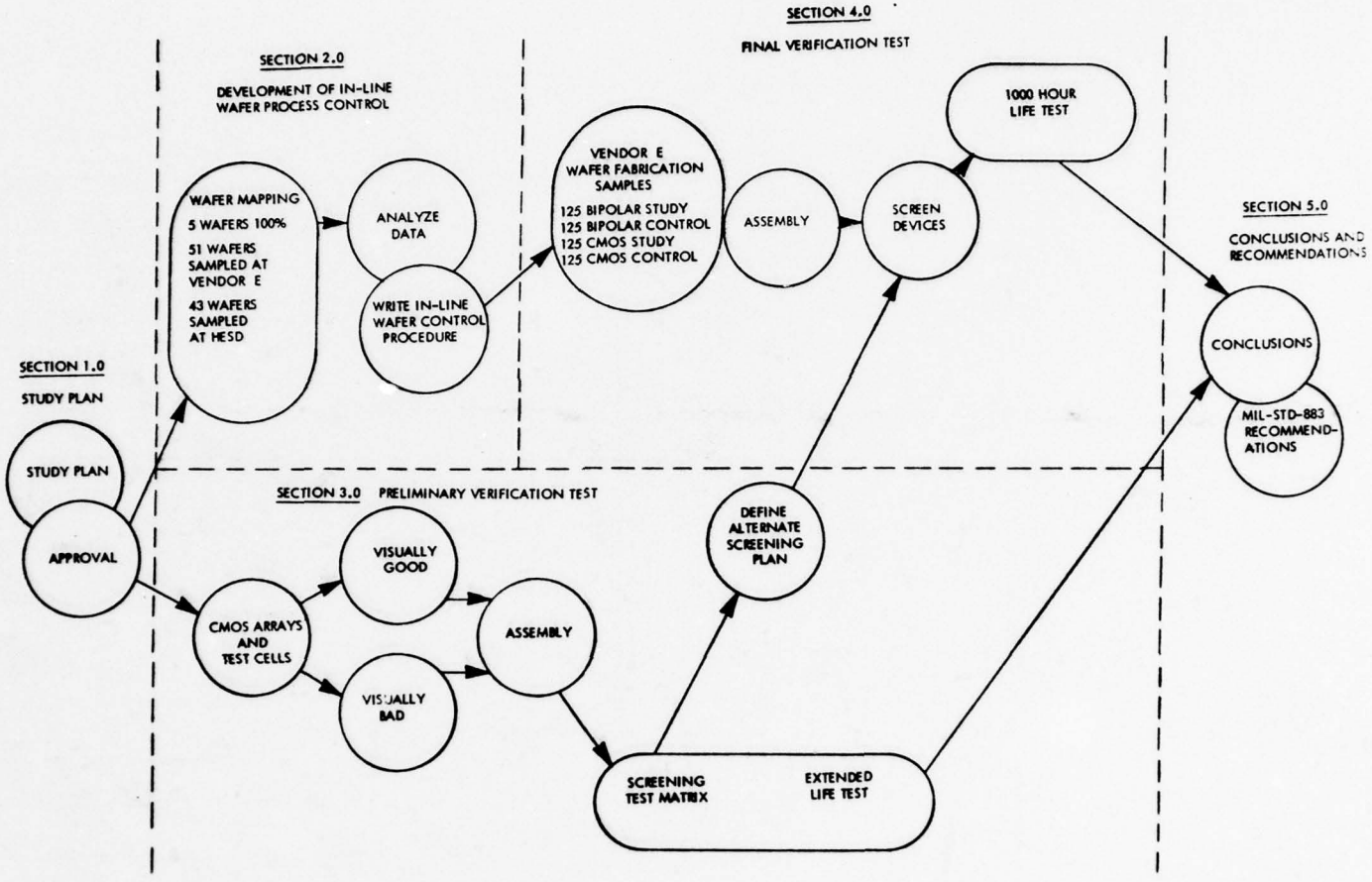


FIGURE 1.2 STUDY PLAN

SECTION 2

2.0 DEVELOPMENT OF IN-LINE WAFER PROCESS CONTROLS

In order to select the wafer sampling plans and required wafer process controls, two parameters were investigated. The first parameter studied was the location of visually defective circuits on completed wafers. This was accomplished by recording the location on the wafer of each defective circuit. This data formed a series of wafer maps showing the frequencies of defects across the wafers. The second parameter studied was the defect itself and its cause. This was accomplished by identifying the defect and then making an assessment as to the process step at which it occurs. Once these parameters were recorded, the data was assessed and analyzed to establish the in-line wafer inspection procedures for the final verification test devices.

2.1 DEFECT LOCATION AND CAUSE

To investigate the location and cause of visual defects, data was taken on the following three separate sampling groups.

- o A sample of five custom LSI CMOS wafers with 100% inspection of each circuit (wafer mapping).
- o A sample inspection of the center row on each of 41 custom LSI CMOS wafers.
- o A sample inspection of the center row on each of 51 complex bipolar wafers from a vendor's MIL-M-38510 certified production line.

Every circuit inspected in each of the three sampling groups was inspected under a metallurgical microscope at 150X to 200X magnification minimum and classified by defect category, cause of defect and type of defect.

The defect classifications were coded as follows:

A. Category

a. Batch defects such as alignment or etching process problems which normally affect all wafers in a given lot or all circuits on a given wafer.

b. Repetitive/random circuit defects such as missing metal in the same location on each circuit which are mask or design related.

c. Random circuit defects such as missing metal caused by handling or process faults.

B. Cause of Defect

a. Handling

b. Oxide etch

c. Metal etch

d. Metal deposition

e. Mask tear or foreign particles on mask or in photoresist

f. Alignment

g. Diffusion

h. Others

C. Type of Defect		Paragraph of MIL-STD-883 Method 2010.2
a.	Scratches	3.1.1.1
b.	Voids	3.1.1.2
c.	Metallization corrosion	3.1.1.3
d.	Metallization adherence	3.1.1.4
e.	Metallization probe	3.1.1.5
f.	Metallization bridging	3.1.1.6
g.	Metallization alignment	3.1.1.7
h.	Diffusion faults	3.1.2.1
i.	Passivation faults	3.1.2.2
j.	Foreign material (Paragraphs b and c only)	3.1.6.1
k.	Glassivation defects	3.1.7
l.	Metal blistering	3.1.1.4

NOTES: If more than one defect was found in any one circuit, each of the defects are indicated in the grid for that circuit.

Example of code;

- o caa represents a random circuit defect caused by handling seen as a scratch.
- o OK - indicates a good circuit.

2.1.1 Wafer Mapping

For the 100% wafer Visual Inspection and mapping, five wafers were selected from four different vendors representing metal gate CMOS and silicon gate SOS technology. All wafers selected for the mapping were residual devices from one of Harris' custom LSI programs.

Table 2.1.1-1 summarizes the wafers selected for the inspection. Figures 2.1.1-1 through 2.1.1-5 are the wafer maps generated from each wafer. From the wafer maps of Figures 2.1.1-1 through 2.1.1-5, an additional set of wafer maps were generated. These maps, Figures 2.1.1-6 through 2.1.1-10, show the number of defects found in each individual circuit. Analysis of the data from Sample 1, Figure 2.1.1-6, revealed a high concentration of visual defects around the edge of the wafer and one row below and one row to the left of the center. Sample 2, Figure 2.1.1-7, shows a high concentration of visual defects near the bottom of the wafer and a band of defects scattered across the center of the wafer. Sample 3, Figure 2.1.1-8, shows a high concentration of visual defects around the edges and near the center of the wafer. Sample 4, Figure 2.1.1-9, shows a high concentration of visual defects around the edge of the wafer. Sample 5, Figure 2.1.1-10, shows a high concentration of visual defects around edges of the wafers and in a band across the bottom third of the wafer. The visual defect patterns as observed on these wafers can be explained as follows:

The edges of the wafers are where the manufacturer picks up the wafer during processing. This edge loss is expected. The high concentration of defects near the bottom of some wafers was caused by the scribing of the lot numbers on the wafer. The high defect counts near the centers of Samples 1, 2, and 3, are due to anomalies in the manufacturer's tooling.

TABLE 2.1.1-1

WAFERS SELECTED FOR 100% VISUAL MAPPING

Sample Number	Technology	Vendor	Wafer Size	Die Size in Mils
1	Metal Gate CMOS	A	2"	149X 187
2	Metal Gate CMOS	B	3"	196 X 203
3	Metal Gate CMOS	C	2"	181 X 184
4	Silicon Gate SOS	D	2"	126 X 157
5	Metal Gate CMOS	B	3"	216 X 204

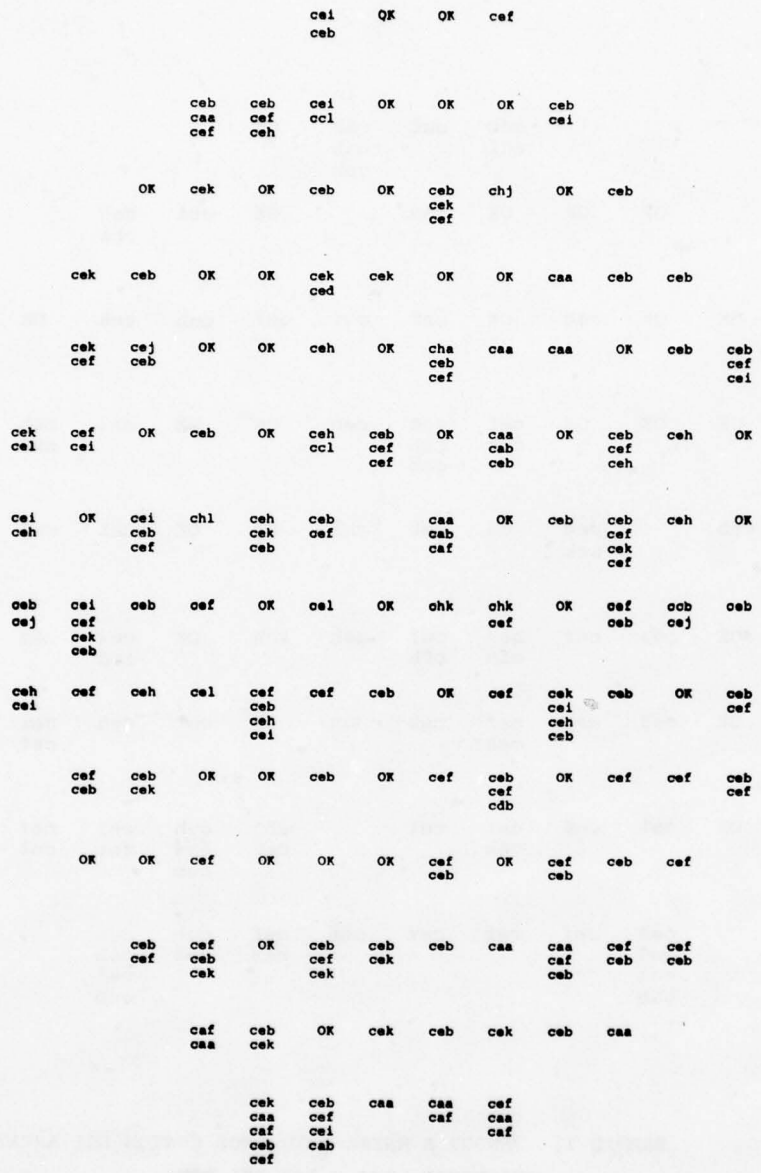
Identification of vendor code:

Vendor A: Harris Semiconductor (HSD)
Vendor B: Solid State Scientific (SSSI)
Vendor C: RCA Semiconductor (RCA)
Vendor D: Hughes (SOS wafer)
Vendor E: National Semiconductor (NSC)

				cdb ecf	caf	cek cab ceh	OK				
			OK	OK	OK	caa		OK	cbi	ceh cbi		
		OK	OK	ceb	OK	caf	cef	cef	ceb	ceh	OK	
cai cek	OK	OK	OK	cef ceb	cef ceh ceb	ceb	OK	OK	chl	ceb cef	ceb caf cab cef
ceh cei	ceb		ceb cek	OK	ceb	chl	OK	OK	chl	cel	ceh cei ceb cal
cei ceh caa	OK	ceb	cef	ceh cfh	cef cfh	aeh	aeh	OK	cek ced	ceb	caa cei
caa cei ceh	OK	cef	ceh	cef cek	ceb	OK	OK	cef	cgh	cei cef	cei caf
	OK	cei	cef	cef ceb	cel		chj cef	ceh caa ceb	cef cei	caf cei	
		ceh ced cef ceb	cef	cef	cef	cef	cef ceb	cgh caa	caa ceh cei ceb		

SAMPLE 1. VENDOR A METAL GATE CMOS CUSTOM LSI ARRAY
2" WAFER 149 X 187 MIL DIE

FIGURE 2.1.1-1



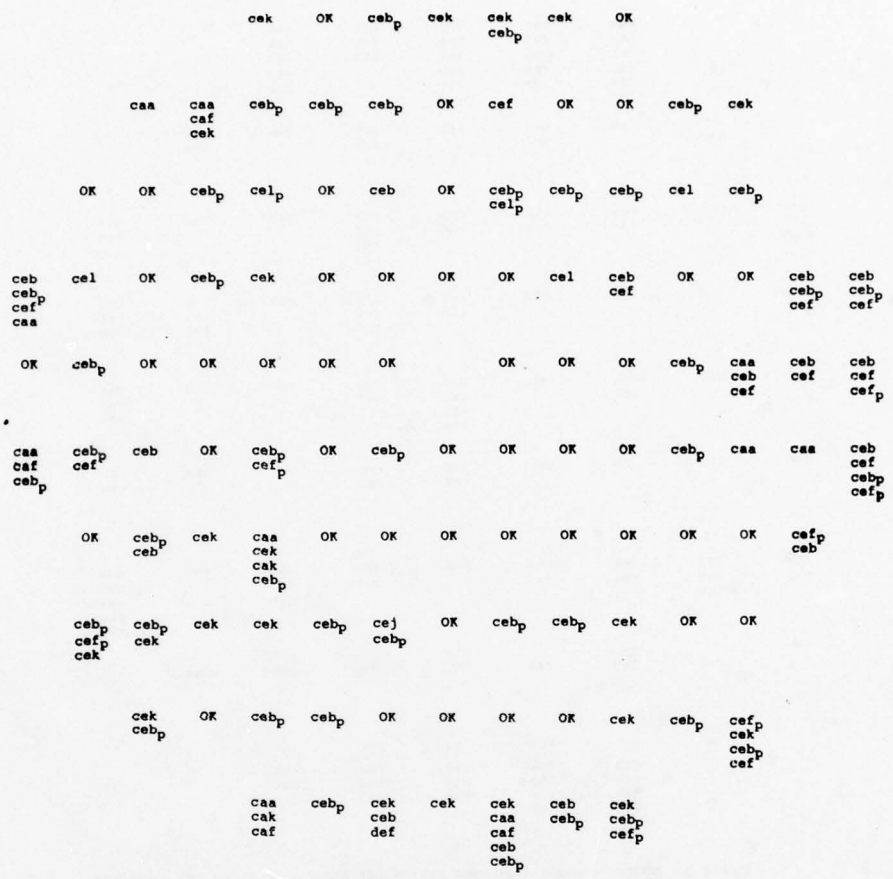
SAMPLE 2. VENDOR B METAL GATE CMOS CUSTOM LSI ARRAY - 3" WAFER 196 X 203 MIL DIE

FIGURE 2.1.1-2

		ceb cdb cel ceh caa caf	ceh cei ceb cek caa	ceb caa caf cab chc cdd	ceb ccc chk	ceb cek cef caa cab		
	cfh ceb	ceb	cek cef	ceb	ceh cek	ceb	ceb caa	
caa cfh ceb	ceb cef	ceb cef	ceh ceb	ceb cef	ceb cbj ccj	ceb	caa	cef cek
caa cek	OK	cek	cfh	ceh cfh	ceb cef ccd	ceb	ceb caa caf	cdb caf caa
cek	cfg	ceb cef	ceb	ceb cef cfh cek	ceb cef	cek	cfg	caa caf cab
ceb	ceb	OK	ceb	ceb cef	ceb caa	ceb	ceb	ceb ceh
caf	chj caa ceb	ceb cei	cek caa	ceb	ceb cek	caa caf ceb	ceb	caa ceb cei ceg cek
	ceg	ceb	ceb	cfg	OK	ceb	caa	
		ceh ceh cek cei	ceb chj caa caf	ceb chj chh	caa cab ceb	ceb caa		

SAMPLE 3. VENDOR C METAL GATE CMOS CUSTOM LSI ARRAY - 2" WAFER 181 X 184 DIE

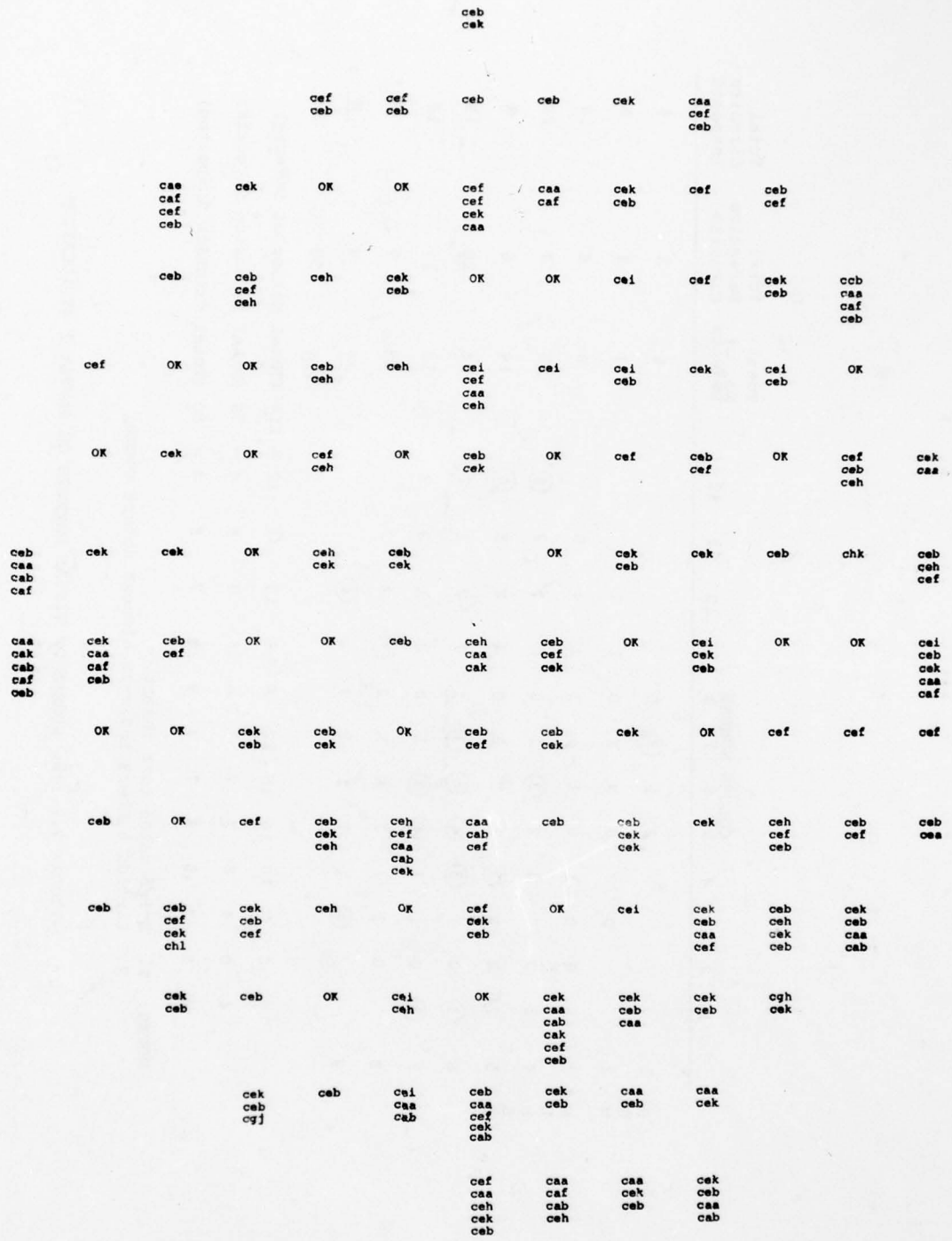
FIGURE 2.1.1-3



NOTE: p after the type of defect indicates a metallization type defect in the polysilicon. Polysilicon defects are not presently covered by method 2010.2 of MIL-STD-883.

SAMPLE 4. VENDOR D SILICON GATE CMOS TEST CELL 2" WAFER 126 X 157 MIL DIE

FIGURE 2.1.1-4



SAMPLE 5. VENDOR B METAL GATE CMOS CUSTOM LSI ARRAY - 3" WAFER 216 X 204 MIL DIE

FIGURE 2.1.1-5

ROW NUMBER	COLUMN NUMBER 1	2	3	4	5	6	7	8	9	10	11	12	Total No. of Defects	Total Defective Circuits	Total Circuits Inspectd
1					2	1	(3)	0					6	3	4
2			0	0	0	X	X	0	1	2			3	2	6
3		0	0	1	0	1	1	1	1	1	0		6	6	10
4	2	0	0	0	2	(3)	1	0	0	1	2	(4)	15	7	12
5	2	X	X	(3)	1	2	2	0	0	X	X	(4)	14	6	8
6	(3)	0	1	(3)	(4)	(4)	(3)	1	0	2	1	2	24	10	12
7	(3)	0	1	1	(4)	(3)	1	0	1	1	2	2	19	10	12
8		0	1	1	2	X	X	2	(3)	2	2		13	7	8
9			(4)	1	1	1	1	2	2	(4)			14	8	8
													116	59	80
	10	0	7	10	16	15	12	6	8	13	7	12 = 116 (Total Number of Defects)			
	4	0	4	6	7	7	7	4	5	7	4	4 = 59 (Total Defective Circuits)			
	4	5	7	8	9	7	7	9	8	7	5	4 = 80 (Total Circuits Inspected)			

NOTES: 1. X indicates test insert.
2. Circled numbers indicate highest defect count.

FIGURE 2.1.1-6. NUMBER OF VISUAL DEFECTS ON SAMPLE 1 BY LOCATION

ROW NUMBER	COLUMN NUMBER 1	2	3	4	5	6	7	8	9	10	11	12	13	14	Total No. of Defects	Total Defective Circuits	Total Circuits Inspected
1						2	0	0	1						3	2	4
2				(3)	(3)	2	0	0	0	2					10	4	7
3			0	1	0	1	0	(3)	1	0	1				7	5	9
4		1	1	0	0	2	1	0	0	1	1	1			7	6	11
5		2	2	0	0	1	0	(3)	1	1	0	1	(3)		14	8	12
6	2	2	0	1	0	2	(3)	0	(3)	0	(3)	1	0		17	8	13
7	2	0	(3)	1	(3)	2	0	(3)	0	1	(4)	1	0		20	9	13
8	2	(4)	1	1	0	1	0	1	2	0	2	2	1		17	10	13
9	2	1	1	1	(4)	1	1	0	1	(4)	1	0	2		19	11	13
10		2	2	0	0	1	0	1	(3)	0	1	1	2		13	8	12
11		0	0	1	0	0	0	2	0	2	1	1			7	5	11
12			2	(3)	0	(3)	2	1	1	(3)	2	2			19	9	10
13				2	2	0	1	1	1	1	1				9	7	8
14					(5)	(4)	1	2	(3)						15	5	5
															178	98	141
	8	12	12	14	17	22	9	17	17	15	17	10	8	= 178	(Total Number of Defects)		
	4	6	7	9	5	12	6	9	10	8	10	8	4	= 98	(Total Defective Circuits)		
	4	8	10	12	13	14	14	14	14	12	11	9	6	= 141	(Total Circuits Inspected)		

NOTE: Circled numbers indicate highest defect count.

FIGURE 2.1.1-7. NUMBER OF VISUAL DEFECTS ON SAMPLE 2 BY LOCATION

ROW NUMBER	COLUMN NUMBER 1	2	3	4	5	6	7	8	9	Total No. of Defects	Total Defective Circuits	Total Circuits Inspected
1			(3)	(4)	(5)	(3)	(5)			20	5	5
2		2	1	2	X	2	1	2		10	6	6
3	1	2	2	2	2	(3)	1	1	2	16	9	9
4	2	0	1	1	2	(3)	1	(3)	(3)	16	8	9
5	1	X	2	1	(4)	2	1	X	(3)	14	7	7
6	1	1	0	1	2	2	1	1	2	11	8	9
7	1	(3)	2	2	1	2	(3)	1	(5)	20	9	9
8		1	1	1	X	0	1	1		5	5	6
9			(4)	(4)	(3)	(3)	2			16	5	5
										128	62	65
	6	9	16	18	19	20	16	9	15 = 128 (Total Number of Defects)			
	5	5	8	9	7	8	9	6	5 = 62 (Total Defective Circuits)			
	5	6	9	9	7	9	9	6	5 = 65 (Total Circuits Inspected)			

NOTES: 1. X indicates test insert.

2. Circled numbers indicate highest defect count.

FIGURE 2.1.1-8. NUMBER OF VISUAL DEFECTS ON SAMPLE 3 BY LOCATION

ROW NUMBER	COLUMN NUMBER 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Total No. of Defects	Total Defective Circuits	Total Circuits Inspected
1																		
2					1	0	1	1	2	1	0					6	5	7
3			1	(3)	1	1	1	0	1	0	0	1	1			10	8	11
4		0	0	1	1	0	1	0	2	1	1	0	1	1		9	8	13
5	(4)	1	0	1	1	0	0	0	0	1	2	0	0	(3)	(3)	16	8	15
6	0	1	0	0	0	0	0	X	0	0	0	1	(3)	2	(3)	10	5	14
7	(3)	2	1	0	2	0	1	0	0	0	0	1	1	1	(4)	16	9	15
8		0	2	1	(4)	0	0	0	0	0	0	0	0	2		9	4	13
9		(3)	2	1	1	1	2	0	1	1	1	0	0			13	9	12
10			2	0	1	1	0	0	0	0	1	1	(4)			10	6	11
11					(3)	1	(3)	1	(5)	2	(3)					18	7	7
																117	69	118
	7	7	8	7	15	4	9	2	11	6	8	4	10	9	10	= 117 (Total Number of Defects)		
	2	4	5	5	9	4	6	2	5	5	5	4	5	5	3	= 69 (Total Defective Circuits)		
	3	6	8	8	10	10	10	9	10	10	10	8	8	5	3	= 118 (Total Circuits Inspected)		

NOTES: 1. X indicates test insert.
2. Circled numbers indicate highest defect count.

FIGURE 2.1.1-9. NUMBER OF VISUAL DEFECTS ON SAMPLE 4 BY LOCATION

ROW NUMBER	COLUMN NUMBER 1	2	3	4	5	6	7	8	9	10	11	12	13	Total No. of Defects	Total Defective Circuits	Total Circuits Inspected
1							1							1	1	1
2					2	2	1	1	1	3				10	6	6
3			(4)	1	0	0	(4)	2	2	1	2			16	7	9
4			1	3	1	2	0	0	1	1	2	(4)		15	8	10
5		1	0	0	2	1	(4)	1	2	1	2	0		14	8	11
6		0	1	0	2	0	2	0	1	2	0	3	2	13	7	12
7	(4)	1	1	0	2	2	X	0	2	1	1	1	3	18	10	12
8	(5)	(4)	2	0	0	1	3	3	0	3	0	0	(5)	26	8	13
9		0	0	2	2	0	2	2	1	0	1	1	1	12	8	12
10		1	0	1	3	(5)	3	1	3	1	3	2	3	26	11	12
11		1	(4)	3	1	0	3	0	1	(4)	(4)	(4)		25	9	11
12			2	1	0	2	0	(6)	3	2	2			18	7	9
13				3	1	3	(5)	2	2	2				18	7	7
14						(5)	(4)	3	(4)					16	4	4
														228	101	129
	9	8	15	14	16	23	32	21	23	21	17	15	14 = 228	(Total Number of Defects)		
	2	5	7	7	9	9	11	9	12	11	8	6	5 = 101	(Total Defective Circuits)		
	2	7	10	11	12	13	13	13	13	12	10	8	5 = 129	(Total Circuits Inspected)		

NOTES: 1. X indicates test insert.
2. Circled numbers indicate highest defect count.

FIGURE 2.1.1-10. NUMBER OF VISUAL DEFECTS ON SAMPLE 5 BY LOCATION

An additional breakdown of the data from Figures 2.1.1-1 through 2.1.1-5 is shown in Table 2.1.1-2. From the Table it can be seen that defect cause, e, mask tears or foreign particles on mask or in photoresist, accounted for the largest number of defects on each wafer ranging from 65.6% to 86.3% of the total defects observed. The second largest cause of defects was defect cause a, handling, accounting for between 12.7% to 21.8% of the total defects observed. The total of these two defect causes represent 94.14% of the total defects observed on all wafers as can be seen from Table 2.1.1-3. The largest number of the handling defects were scratches representing 55.03% of the total. An additional 24.85% of the handling defects were metallization bridging. The largest percent of the defects caused during photoresist were voids representing 39.49% of the total. The next largest defect type was the 21.51% metallization bridging defects.

2.1.2 Sample Wafer Inspection

In order to investigate a larger sample of wafers and other technologies, circuits were inspected on wafer just prior to electrical probe. These wafers like the previous samples, all had a glassivation layer. The wafers selected for this part of the study are summarized in Table 2.1.2-1.

2.1.2.1 CMOS Wafer Sample Inspection

An additional 43 CMOS wafers from Vendor B were sampled by inspecting one row across the center of each wafer. The wafers selected for the study are summarized in Tables 2.1.2.1-1 and 2.1.2.1-2, with the raw data in Appendix A. A review of the data of Table 2.1.2.1-1 indicates a high concentration of visual defects in rows 1 through 6. The high concentration in the first two rows could be explained by handling since the manufacturer picks the wafer up on the edge during handling; however, the defect count on rows 3 through 6 cannot be explained. From Table 2.1.2.1-2 it can be seen that handling (code -a-) and defects caused by the photoresist process (code -e-) are once again the highest defect cause accounting for 16.8% and 77.4% of the total

TABLE 2.1.1-2 MATRIX OF TOTAL NUMBER OF DEFECTS BY DEFECT CLASSIFICATION OBSERVED ON FIVE (5) WAFERS INSPECTED 100%

Sample Number	Defect Category	Cause of Defect a	b	c	d	e	f	g	h
	A		7			12			
	B								
1	C	15	2	1	1	75	1	2	2
Total		15	9	1	1	87	1	2	2
Percent		13.7	7.6	0.8	0.8	73.7	0.8	1.6	1.6
Total Defects - 118									

Defect Category & Cause	Type of Defect a	b	c	d	e	f	g	h	i	j	k	l
Ab								7				
Ae								12				
Ca	6	2				5			2			
Cb									2			
Cc						1						
Cd		1										
Ce		19		2		22		14	12		5	1
Cf								1				
Cg								2				
Ch										1		1
Total	6	22		2		28		36	16	1	5	2
Percent	5.1	18.6		1.6		23.7		30.5	13.5	0.8	4.2	1.6

		a	b	c	d	e	f	g	h
2	A								
	B								
	C	23		2	1	149			5
Percent		12.7		1.1	0.5	82.7			2.7
Total Defects - 180									

Defect Category & Cause	Type of Defect a	b	c	d	e	f	g	h	i	j	k	l
Ca	14	2				7						
Cb												
Cc												2
Cd		1										
Ce	1	54		2		42		12	11	3	21	3
Cf												
Cg												
Ch	1									1	2	1
Total	16	57		2		49		12	11	4	23	6
Percent	8.9	31.7		1.1		27.2		6.7	6.1	2.2	12.8	3.3

		a	b	c	d	e	f	g	h
	A								
3	B								
	C	28	1	3	3	84	5		4
Percent		21.8	0.8	2.3	2.3	65.6	3.9		3.1
Total Defects - 128									

Defect Category & Cause	Type of Defect a	b	c	d	e	f	g	h	i	j	k	l
Ca	17	4				7						
Cb												
Cc			1	1						1		
Cd		2		1								
Ce		44				11	2	8	4		14	1
Cf								5				
Cg												
Ch			1							3		
Total	17	50	2	2		18	2	13	4	5	14	1
Percent	13.3	39.1	1.5	1.5		14.1	1.5	10.2	3.1	3.9	10.9	0.8

		a	b	c	d	e	f	g	h
	A								
4	B								
	C	16				101			
Percent		13.7				86.3			
Total Defects - 117									

Defect Category & Cause	Type of Defect a	b	c	d	e	f	g	h	i	j	k	l
Ca	10					4					2	
Cb												
Cc												
Cd												
Ce		55				19				1	21	5
Cg												
Ch												
Total	10	55				23				1	23	5
Percent	8.5	47.0				19.7				0.8	19.7	4.2

		a	b	c	d	e	f	g	h
	A								
5	B								
	C	47		1		174		2	2
Percent		20.8		0.4		77.0		0.9	0.9
Total Defects - 226									

Defect Category & Cause	Type of Defect a	b	c	d	e	f	g	h	i	j	k	l
Ca	24	11				9					3	
Cb												
Cc		1										
Cd												
Ce	1	63				34		19	10		47	
Cf												
Cg								2				
Ch											1	1
Total	25	75				43		21	10		51	1
Percent	11.1	33.2				19.0		9	4.4		22.6	0.4

Total All Wafers		12	10	7	5	595	6	4	13
Total All Wafers		129	10	7	5	595	6	4	13
Percent		16.8	1.3	0.9	0.6	77.4	0.8	0.5	1.7
Total Defects - 769									

Total All Wafers	79	259	2	6	0	161	2	82	41	11	116	15
Percent	9.6	33.7	0.2	0.8		20.1	0.2	10.7	5.3	1.4	15.1	2.0

TABLE 2.1.1-3

Percent defective caused by photoresist and handling in the five wafer sample.

Defects Caused by Handling	No. of Defects Observed	Percent of Total Defects	Percent of Handling Defects by Defect Type
caa	71	9.23	55.03
cab	19	2.47	14.72
caf	32	4.16	24.81
cai	2	.26	1.55
cak	5	.65	3.88
Total	129	16.78	100.00

Defects Caused During Photoresist			Percent of Caused during Photoresist by Defect Type
aeh	12	1.56	2.02
cea	2	.26	.33
ceb	235	30.56	39.49
ced	4	.52	.67
cef	128	16.64	21.51
ceg	2	.26	.33
ceh	53	6.89	8.91
cei	37	4.81	6.22
cej	4	.52	.67
cek	108	14.04	18.15
cel	10	1.30	1.68
Total	595	77.37	100.00

Total % visual defects caused by handling and by photoresist process ----------94.14%

TABLE 2.1.2-1

WAFERS SELECTED FOR SAMPLING

Technology	No. of Wafers Inspected	Vendor	Wafer Size	Die Size in Mils
Metal Gate CMOS LSI	24	B	3"	205 X 168
Metal Gate CMOS LSI	9	B	3"	204 X 216
Metal Gate CMOS LSI	10	B	3"	186 X 183
Bipolar MSI	38	E	3"	87 X 113
Bipolar MSI	13	E	3"	83 X 92

TABLE 2.1.2.1-1

NUMBER OF DEFECTS ACROSS CENTER ROW
OF 43 CMOS WAFERS FROM VENDOR B

	COLUMN NUMBER															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Total Defects/Row	63	54	47	53	55	53	39	35	41	45	34	34	39	21	33	45

TABLE 2.1.2.1-2

MATRIX OF TOTAL NUMBER OF DEFECTS BY DEFECT CLASSIFICATION OBSERVED ON 43 CMOS WAFERS FROM VENDOR B

Defect Category	a	b	c	d	e	f	g	h
A		3		6				
B								
C	75	1	2	22	577	1		4
Total	75	4	2	28	577	1	0	4
Percent	10.8	0.6	0.3	4.1	83.5		-	0.6

Total Defects - 691

Defect Category and Cause	a	b	c	d	e	f	g	h	i	j	k	l
Ab						3					3	
Ad												3
Ca	4	19				42			1	7	2	
Cb									1			
Cc		1				1						
Cd		8		1		13						
Ce		148				195		81	11	6	133	3
Cf								1				
Cg												
Ch				1						3		
Total	4	176	0	2	0	254	0	82	13	16	138	6
Percent	0.6	25.5	-	0.3	-	36.8	-	11.9	1.9	2.3	20.0	0.9

defects respectively. The defect types did vary slightly between this sample and the previous 5 wafer sample with variations between scratches (code --a), voids (code --b), and metallization bridging (code --f). However, from Table 2.1.2.1-3 it can be seen that even though the defects did vary slightly, 94.36% of the total defects were caused by handling or the photo resist process problems which positively correlates with the 94.14% detected for the same causes in the 5 wafer sample.

TABLE 2.1.2.1-3

Percent defects caused by photoresist process and handling observed on 43 CMOS wafer sample

Defects Caused by Handling	No. of Defects Observed	Percent of Total Defects	Percent of Handling Defects by Defect Type
caa	4	.58	5.33
cab	19	2.74	25.33
caf	42	6.08	69.33
cai	1	.14	1.33
caj	7	1.01	9.33
cak	2	.29	2.67
Total	75	10.85	100.00
Defects *Caused During* Photoresist			
ceb	148	21.41	25.65
cef	195	28.22	33.80
ceh	81	11.72	14.04
cei	11	1.59	1.91
cej	6	.87	1.04
cek	133	19.25	23.05
cel	3	.43	.52
Total	577	83.50	100.00

Total percent visual defects caused by handling and by photoresist process.----------94.36%

2.1.2.2 Bipolar Wafer Sample Inspection

In order to investigate other than CMOS technology, a 51 wafer bipolar sample was inspected at Vendor E's facility. The sample wafers selected for the study were from a well established MIL-M-38510 certified production line. The data taken on these wafers is in Appendix A. As on the CMOS sample, one row across each wafer was inspected. Each circuit was inspected in the row just above the test cell insert. The data from this sample is summarized in Tables 2.1.2.2-1 and 2.1.2.2-2. Once again, the data shows a high concentration of visual defects near the edge (see Table 2.1.2.2-1). The defects are more equally distributed across the wafer in other areas than observed in the CMOS samples. Similar to the other samples the largest cause of the defects were handling and photoresist problems representing 79.76% of the total (see Table 2.1.2.2-3). However, this sample had 17.2% foreign material (code --j) as compared to 1.4% and 2.3% in the other two previous CMOS samples. A summary of the comparison of the defects caused by handling and by photoresist operation on all three samles are shown in Table 2.1.2.2-4.

2.1.3 Electrical Mapping

In order to more fully assess the location of the samples to be selected during the wafer inspection, 97 electrically probed custom CMOS LSI wafers from Vendor B were mapped. This mapping was accomplished by indicating the location of each electrically good circuit on a grid as shown in Table 2.1.3-1. As indicated in the Table, the highest concentration of electrically good circuits were clustered slightly to the left of the center of the wafer.

Plotting a composite of the visually defective circuit from the five CMOS wafers that were 100% mapped and superimposing the locations of the highest frequency of occurrence of electrically good circuit reveals a high concentration of electrically good devices occurring in areas of high concentration of visually defective die (see Table 2.1.3-2).

TABLE 2.1.2.2-1

NUMBER OF DEFECTS ACROSS CENTER ROW
OF 51 BIPOLAR WAFERS INSPECTED
AT VENDOR E's FACILITY

	COLUMN NUMBER																								*
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
Total Defects/Row	68	45	23	22	19	21	19	22	15	19	15	14	24	21	26	18	24	25	18	18	20	20	17	19	19

*Note: rows past 25 were not inspected on some wafers; therefore, results of rows 26 through 29 are not shown in this table.

TABLE 2.1.2.2-2

MATRIX OF TOTAL NUMBER OF DEFECTS OF DEFECT CLASSIFICATION OBSERVED ON 51 BIPOLAR WAFERS INSPECTED AT VENDOR E's FACILITY

Defect Category	Cause of Defects a	b	c	d	e	f	g	h
A		4	3					
B			6		8			
C	88	13	37	57	381		1	
Total	88	17	46	57	389	0	1	0
Percent	14.7	2.8	7.7	9.5	65.1	-	0.2	-

Defect Category and Cause	a	b	c	d	e	f	g	h	i	j	k	l
Ab											4	
Ac		1		1		1						
Bc		4				2		3				
Be						5		3				
Ca	62	2				3		8		13		
Cb									13			
Cc		13				22				2		
Cd		2		8		47						
Ce		61		1		37		81	12	88	101	
Cf												
Cg								1				
Ch												
Total	62	83	0	10	0	117	0	93	25	103	105	0
Percent	10.4	13.9	-	1.7	-	19.6	-	15.6	4.2	17.2	17.6	-

TABLE 2.1.2.2-3

Percent defects caused by photoresist process and handling observed on 51 bipolar wafers.

Defects Caused by Handling	No. of Defects Observed	Percent of Total Defects	Percent of Handling Defects by Defect Type
caa	62	10.4	70.45
cab	2	.33	2.27
caf	3	.50	3.40
cah	8	1.33	9.09
caj	13	2.17	14.77
Total	88	14.71	100.00

Defects Caused during Photoresist			% of Defects Caused during Photoresist by Defect Type
beh	3	.50	.77
bef	5	.83	1.28
ceb	61	10.20	15.68
ced	1	.16	.25
cef	37	6.19	9.51
ceh	81	13.55	20.8
cel	12	2.00	3.08
cej	88	14.71	22.62
cek	101	16.89	25.96
Total	389	65.05	100.00

Total percent visual defects caused by handling and by photoresist process ----------79.76%

TABLE 2.1.2.2-4

Summary of all three samples showing percent visual defects caused by photoresist operations and handling.

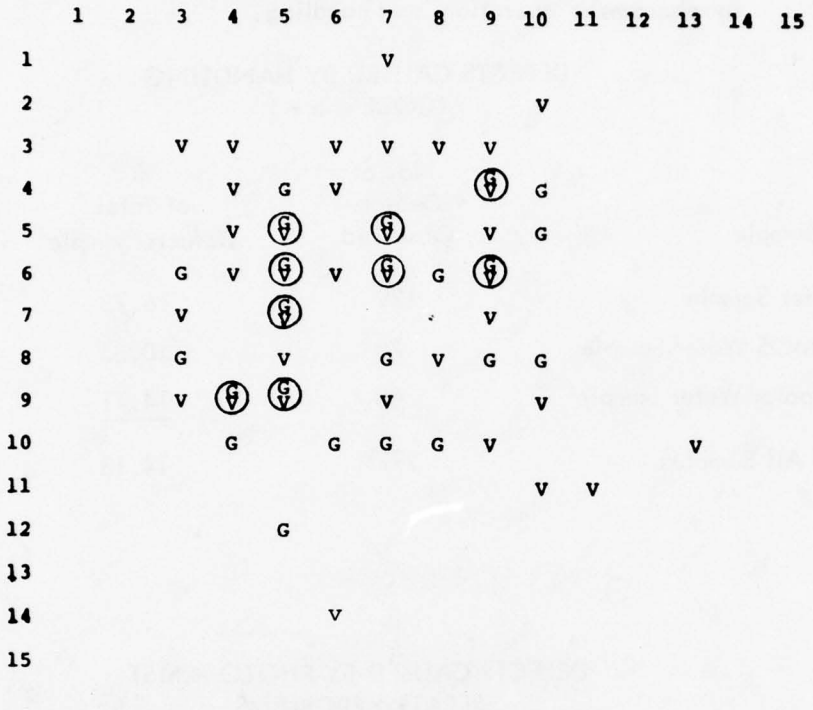
DEFECTS CAUSED BY HANDLING
(CODE - a -)

Sample	No. of Defects Observed	% of Total Defects/Sample
5 Wafer Sample	129	16.78
43 CMOS Wafer Sample	75	10.85
51 Bipolar Wafer Sample	88	14.71
Total All Samples	292	14.18

DEFECTS CAUSED BY PHOTO RESIST
RELATED PROBLEMS
(CODE - e -)

Sample	No. of Defects Observed	% of Total Defects/Sample
5 Wafer Sample	595	77.37
43 CMOS Wafer Sample	577	83.50
51 Bipolar Wafer Sample	389	65.05
Total All Samples	1561	75.85

Total % visual defects caused by handling and by photo resist operations-----90.03%.



V = Highest Probability of Visual Defects

G = Highest Probability of Electrically Good Circuits.

(G/V) - Highest Probability of Visual Defect and Electrically Good Circuits Occurs in Same Location.

TABLE 2.1.3-1. LOCATION OF VISUAL DEFECTS VS. ELECTRICALLY GOOD CIRCUITS.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1							11	7	3	2						
2				3	10	7	13	17	13	14	1	11				
3			5	15	17	24	21	24	24	23	15	9	7	1		
4		5	19	24	(30)	27	26	27	(29)	(30)	13	12	16	2	7	
5		18	17	22	(29)	27	(31)	25	19	(29)	23	21	8	9	5	
6		10	(30)	25	(32)	17	(30)	(30)	(29)	16	21	20	17	11	9	
7	3	9	16	20	(34)	26	20	12	23	24	24	13	15	9	2	
8	9	25	(29)	27	22	23	(30)	26	(35)	(31)	22	20	10	16	5	
9	3	25	25	(37)	(31)	18	16	25	15	25	17	18	12	11	8	
10	2	13	15	(31)	17	(34)	(34)	(29)	25	22	25	15	16	6	4	
11		15	7	19	19	24	27	19	20	16	16	9	11	7	4	
12		3	9	14	(30)	19	27	20	16	10	14	8	8	3	1	
13				5	11	18	13	14	9	8	9	3	4			
14				2	7	4	8	4	3	7	5	1				
15						1	1	1	1							

NOTE: Circled numbers indicate highest locations of good circuits.

TABLE 2.1.3-2. NUMBER OF ELECTRICAL GOOD CIRCUITS BY WAFER LOCATION

2.1.4 Summary of Results from Visual Inspection

A. Cause of Visual Defects

- Visual defects caused during the photoresist process due to mask tears or foreign particles on the mask or in the photoresist are the largest cause of visually defective circuits in wafer form accounting for over 75% of the total defects in the three samples studied.
- Visual defects caused by handling are the second largest cause of visually defective circuits in wafer form, accounting for over 14% of the total defects in the three samples studied.
- Random circuit defects accounted for greater than 95% of the defects observed.
- Batch defects and repetitive random circuit defects accounted for less than 4% of the defects observed.
- Different technologies; metal gate CMOS, bipolar, and silicon gate SOS, revealed differences in percent defective, and types of defects, however, photoresist defects (code -e-) and handling defects (code -a-) accounted for over 79% of the cause of the visual defects for each technologies.
- Less than 1% alignment defects were observed in all samples.

B. Defect Location

- All wafers inspected show higher concentration of visually defective circuits around the edge of the wafer, however, on some of the CMOS devices there was also a high concentration of defects near the center of the wafer.
- The locations on the wafer that have the highest probability of finding an electrically good die are near the center of the wafer.

2.1.5 Conclusions from Visual Inspection

A. Cause of Visual Defects

- In order to control the wafer process and reduce the visual defects the photo resist process and handling of the wafers must be controlled.
- Although the type of visual defect varies for different technologies, the causes of the visual defects are relatively the same.
- The present visual process controls self-imposed by the manufacturer during wafer fabrication controls the batch defects but does allow a number of random circuit defects to escape.
- Some defects, such as mis-alignment of oxide cuts, were probably hidden by the metallization and the glassivation levels and therefore were not detected in the study samples.
- If the number of visual defects is reduced the electrical yield should improve.

B. Defect Locations

Circuits near the center of the wafer should be sampled for wafer acceptance since the highest probability of finding an electrically good die is near the center and since some of the samples showed a high concentration of visual defects near the center.

2.2 IN-LINE WAFER INSPECTION PROCEDURE

In order to develop the specification to control and eliminate the defects found in Section 2.1, the following tasks were accomplished:

- o Effective in-process wafer inspection points selected.
- o Effective process controls implemented at the selected inspection points.
- o Sampling plans developed which systematically remove defects by wafer worst case location sampling.
- o Comprehensive inspection criteria defined.
- o Escape probability determined based on the sampling plans.

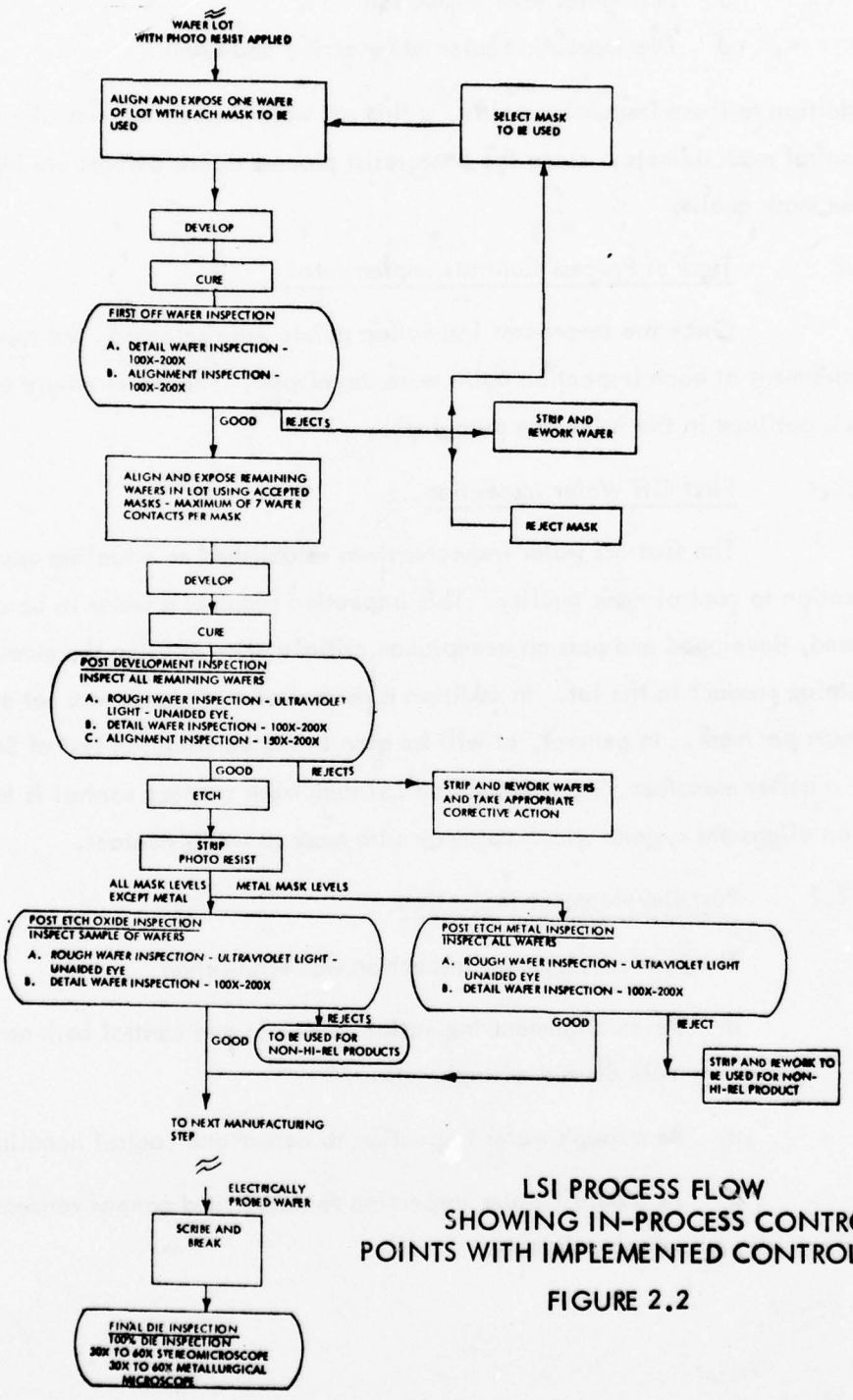
The resulting specification developed is diagramed in Figure 2.2 and is included in Appendix B as Harris Specification Number 131252. This specification was used in the verification testing of Section 4.0. The rationale used to accomplish the above tasks is outlined in the following paragraphs.

2.2.1 In-Process Inspection Points

Based on the inspection results and conclusions from Section 2.1, the in-process wafer inspection points were selected. The main objective in selecting these points was to reduce and control defects caused during the photoresist processes. The points in the process selected for the inspections were the same steps at which most semiconductor manufacturers normally inspect the product as part of their own in-house process control. This allows implementation of these wafer controls without disruption of the manufacturer's normal product flow.

These inspection points consist of:

- o Post development inspection
- o Post oxide etch inspection



LSI PROCESS FLOW
SHOWING IN-PROCESS CONTROL
POINTS WITH IMPLEMENTED CONTROLS

FIGURE 2.2

- o Post metal etch inspection
- o Die inspection after wafer scribe and break.

In addition to these inspection points, a first off wafer inspection was also selected to control mask defects, since the photoresist process orient defects are highly dependent on the mask quality

2.2.2 Type of Process Controls Implemented

Once the in-process inspection points were selected, the types of control to implement at each inspection point were developed. The development of these controls is outlined in the following paragraphs.

2.2.2.1 First Off Wafer Inspection

The first off wafer inspection was established as a tooling acceptance inspection to control mask quality. This inspection requires a wafer to be aligned, exposed, developed and pass an acceptance criteria prior to using the mask on the remaining product in the lot. In addition a control of mask usage was set at 7 contacts per mask. In general, as will be seen in the verification test of Section 4.0, a better manufacturing approach on LSI than mask contact control is to use projection alignment systems which do away with mask to wafer contact.

2.2.2.2 Post Development Inspection

The post development inspection was established

- o As an alignment inspection to detect and control both operator and mask caused misregistration.
- o As a rough wafer inspection to detect and control handling defects.
- o As a detail wafer inspection to detect and control random process oriented defects.

This inspection point, like the first mask inspection, acts as a control gate since wafers can be reworked at this point (prior to etch) without any impact on final product quality. Therefore, the most thoroughly economically feasible inspection was established at this inspection point.

2.2.2.2.1 Alignment Inspection

The alignment inspection, which is a 100% screen since wafers are individually aligned, is set up to control worst case operator error by inspecting the first whole circuit on either side of the wafer. (Flat edge of wafer being the bottom.) As a check on the worst case rotational alignment of the mask the first whole circuit on the wafer at the top and bottom is also inspected. The inspection of these four circuits guarantees that all circuits on the wafer will be aligned. Most manufacturers do not inspect to the outside edge of the wafer for alignment as required here, since they assume the outer circuits to be the poorest yielding part of the wafer. Therefore, any devices which may pass the electrical testing from the outside edge may be misaligned creating potential field failures.

2.2.2.2.2 Rough Wafer Inspection

The rough wafer inspection is a 100% screen set up as a control on handling defects by inspecting each wafer under ultraviolet light with the unaided eye.

2.2.2.2.3 Detail Wafer Inspection

The detail wafer inspection is also a 100% screen of the wafers, with a lot acceptance on each wafer. A sample of circuits is selected near the center of the wafer, thereby giving a worst case inspection point. The sample at the center is based on the result from Section 2.1, showing that the highest concentration of electrically good and visually defective circuits is located near the center of the wafer. The inspection is accomplished under 100X to 200X magnification with a metallurgical microscope.

2.2.2.3 Post Etch Oxide Inspection

The post etch oxide inspection was selected as a lot acceptance inspection to control batch and random circuit defects introduced at the etching and stripping operations. This inspection is accomplished by:

- o A sample rough wafer inspection under ultraviolet light with the unaided eye.
- o A sample detail wafer inspection at 100X to 200X magnification with a metallurgical microscope.

Since reworking the wafer after oxide etch could have impact on final product quality and is usually not feasible, the inspection is set up as an etch control by sampling wafers from each lot. The rough wafer inspection and the detail wafer inspection is performed in the same manner here as at the post development inspection except on a sample wafer basis.

2.2.2.4 Post Etch Metal Inspection

The post etch metal inspection was selected as a 100% wafer inspection point (screen) to select acceptable wafers for processing into military circuits. As in the post etch oxide inspection, a rough wafer inspection and a detail wafer inspection is performed. This inspection point is designed to replace the 100% high magnification preseal die inspection currently required by MIL-STD-883.

2.2.2.5 Die Inspection

The die inspection after scribe and breaking of the die is a 100% screen performed at low power only (30X to 60X) under both a metallurgical and stereo microscope and is designed to remove defects caused by handling, probe, scribe, and breaking occurring after the last wafer inspection point. Refer to Appendix B, Specification 131252, Sheet 2, for inspection details.

2.2.3 In-Line Wafer Sampling Plans

To arrive at the required sampling plans the results from the wafer inspections of Section 2.1 were analyzed. A statistical expectation of the process outputs of the three samples of Section 2.1 was computed using the classical process capability study approach; however, since the process capability (% defective) was much higher than in non-batch processed manufacturing processes and since the sample size would have to be small to make the inspection economical, the classical determination of sampling based on process capability was abandoned as not being feasible for wafer process control. Therefore, the only realistic way to arrive at the required sampling plans would be to have them based on a process improvement objective rather than on the process capability as found by the samples inspected in Section 2.1. In addition, for a reasonable yield to be achieved on an LSI circuit, the visual defect count should be less than what was observed in the study samples of Section 2.1. Based on these premises, we selected what we considered a maximum economical sample size and a maximum LTPD for the post development inspection and derived a set of sampling plans that would give a systematic defect elimination procedure to control defects as the wafer moved through the process. The rationale used to arrive at these sampling plans is given below. A summary of the LTPD's of the sampling plans is outlined in Table 2.2.3 with the Operating Characteristic Curves for each plan shown in Appendix C.

2.2.3.1 Sampling Plan for Post Development Inspection.

For the detail circuit inspection at post development, a sampling plan with a LTPD of 40 [1] was chosen with the sampling plan developed as shown in Table 2.2.3.1. The sampling plan has acceptance criteria for individual wafers based on the number of defective circuits per wafer. In addition lots for which the number of rejected wafers exceeds the inspection plan are also rejected.

[1] In order to keep the sample to a reasonable size a number of the operating characteristic curves chosen actually had a LTPD between 32 and 44 (see Appendix C).

TABLE 2.2.3

SUMMARY OF LTPD's OF
WAFER IN-LINE SAMPLING PLANS

Inspection	LTPD
First Off Wafer Inspection	32
Post Development	40
Post Etch Oxide	34
Post Etch Metal	45

TABLE 2.2.3.1

SAMPLING PLAN FOR DETAIL
INSPECTION AT POST DEVELOPMENT

Number of Wafers in Lot	Number of Circuits per Wafer to Inspect	Acceptable Number of Defective Circuits Allowed for Each Wafer Inspected	Acceptable Number of Rejected Wafer Allowed in Sample
4	15	2	0
5	12	2	0
6	10	1	0
7	9	1	1
8	8	1	1
9	7	1	1
10	7	1	1
11	7	1	1
12	7	1	2
13	6	0	2
14	6	0	2
15	6	0	3
16	6	0	3
17	6	0	3
18	6	0	3
19 through 21	6	0	4
22 through 24	6	0	5
25 through 28	6	0	6
29 through 32	6	0	7
33 through 34	6	0	8
35 through 38	6	0	9
39 through 42	6	0	10
43 through 44	6	0	11
45 through 46	6	0	12
47 through 48	6	0	13
48 through 50	6	0	14

2.2.3.2 Sampling Plan for Post Etch Oxide Inspection

For the detail circuit inspection at post etch oxide a sample plan with a LTPD of 34 [2] was chosen. From experience we have found that due to the batch processing, the defects observed after oxide etch are normally across the entire lot rather than oriented to individual wafers. The acceptance criteria for this inspection is based on the number of defective circuits found in the entire sample. The sampling plan for this inspection was developed as shown in Table 2.2.3.2.

2.2.3.3 Sampling Plan for Post Etch Metal Inspection

For the post metal etch inspection a sampling plan with a LTPD of 45 was chosen. Since this inspection is a 100% wafer inspection to select the wafers which are acceptable for hi-rel products, a LTPD slightly looser than the other inspection points was chosen. As can be seen from reviewing the post etch metal sampling plan, the sample sizes have been held as small as possible to make the inspection time reasonable. The sampling plan for this inspection is developed as shown in Table 2.2.3.3.

2.2.3.4 Sampling Plan for First Off Wafer Inspection

For the first off wafer inspection a sampling plan with a LTPD of 32 was chosen. Since the mask must be capable of producing product which will be acceptable at the post development inspection, this LTPD was chosen to enable meeting the 40% LTPD value required at the post development inspection.
To choose a tighter sampling plan for this inspection would require too large a sample size to be economical for this inspection. The sampling plan for this inspection is shown in Table 2.2.3.4.

[2] Once again the LTPD varied slightly between sampling plans. In this case the LTPD's were between 27 and 34 (see Appendix C).

TABLE 2.2.3.2

SAMPLING PLAN FOR DETAILED
POST ETCH OXIDE INSPECTION

No. of Wafers in Lot	No. of Wafers per Lot to Inspect	No. of Circuits per Wafer to Inspect	Total No. of Circuits to Inspect	Acceptable Number of Defective Circuits Allowed for Circuits Inspected
1	1	6	6	0
2	2	6	12	1
3	3	6	18	2
4	4	6	24	4
5	5	6	30	6
6	5	6	30	6
7	5	6	30	6
8	5	6	30	6
9	5	6	30	6
10	5	6	30	6
11	5	6	30	6
12	5	6	30	6
13	6	6	36	8
14	6	6	36	8
15	6	6	36	8
16	8	6	48	11
17	8	6	48	11
18	8	6	48	11
19	8	6	48	11
20	8	6	48	11
21 to 50	10	6	60	14

TABLE 2.2.3.3

SAMPLING PLAN FOR POST ETCH METALLIZATION INSPECTION

Number of Circuits per Wafer Less Than or Equal to	Number of Circuits to Inspect	Acceptable Number of Defective Circuits Allowed for Each Wafer
100	7	1
200	7	1
300	10	2
400	10	2
500	10	2
600	10	2
700	13	3
800	13	3
900	13	3
1000	13	3
1100	13	3
1200	13	3

TABLE 2.2.3.4

SAMPLING PLAN FOR FIRST OFF WAFER INSPECTION

Number of Circuits per Wafer Less Than or Equal to	Number of Circuits to Inspect	Acceptable Number of Defective Circuits Allowed for the Wafer
100	6	0
200	6	0
300	10	1
400	10	1
500	10	1
600	10	1
700	13	2
800	13	2
900	13	2
1000	13	2
1100	13	2
1200	13	2

2.2.4 Inspection Criteria

The inspection criteria was derived by modifying the present MIL-STD-883B, Method 2010.2, Condition B, criteria at Preseal Visual so that it properly applies to the wafer fabrication process. In addition, normal process oriented defect criteria were added. In order to allow the specification to cover as many processes as possible, a statement has been included in the specification to allow the manufacturer to use any additional reject criteria not specifically called out by the specification.

This inspection plan is outlined in Figure 2.2 and is included in Appendix B as HESD Specification Number 131252 as it was written and implemented in the verification study.

2.2.5 Probability of Escape

The probability of escape P (E) is the probability that a defective circuit will get through the In Process Inspection Procedure of Section 2.2. This probability is considered in three parts: (a) the probability of a device with an oxide defect escaping any one post etch oxide inspection, (b) the probability of a device with a metal defect escaping post etch metal inspection, and (c) the probability of device with either an oxide defect or a metal defect getting through the entire wafer process.

2.2.5.1 Probability of a Die with an Oxide Defect Escaping

The probability of a die with an oxide defect escaping is computed by the following equation:

- $P(E_O) = P(L)\ P(P)$
- $P(E_O)$ is the probability of an oxide defect escaping
- P (L) is the probability of a lot being accepted for a given sampling plan and given process percent defective.
- P (P) is the probability of a given die being defective.

The P (L)'s for typical lot sizes and typical process percent defectives for LSI circuits, shown in Table 2.2.5.1-1, were taken from the Operating Characteristic Curves of Appendix C. For the process percent defectives and the lot sizes indicated in Table 2.2.5.1-1 the $P(E_O)$'s are shown in Table 2.2.5.1-2.

2.2.5.2 Probability of a Die with a Metal Defect Escaping

The probability of a die with a metal defect escaping is computed by the following equation:

- $P(E_M) = P(W)\ P(P)$
- $P(E_M)$ is the probability of a metal defect escaping.
- P (W) is the probability of a wafer being accepted for a given sampling plan and process percent defective.
- P (P) is the probability of a given die being defective.

TABLE 2.2.5.1-1

PROBABILITY (P (L)) OF LOT BEING ACCEPTED

No. of Wafers per Lot	Process Percent Defective 5	10	20	30	40
5	.98	.93	.44	.15	.05
10	.98	.93	.44	.15	.05
20	.99	.95	.50	.14	.07
40	.98	.94	.65	.15	.05

TABLE 2.2.5.1-2

PROBABILITY (P (E_O)) OF AN OXIDE DEFECT ESCAPING

No. of Wafers Per Lot	Process Percent Defective 5	10	20	30	40
5	.049	.093	.088	.045	.020
10	.049	.093	.088	.045	.020
20	.049	.095	.100	.042	.028
40	.049	.095	.130	.042	.020

The P (W)'s for typical numbers of die per wafer and typical process percent defectives for LSI circuits, shown in Table 2.2.5.2-1, were taken from the operating characteristic curves of Appendix C.

For the process percent defectives and the number of circuits per wafer indicated in Table 2.2.5.2-1, the P (E_M) are shown in Table 2.2.5.2-2.

2.2.5.3 Probability of a Die with Either an Oxide Defect or a Metal Defect Escaping

The probability of a circuit with an oxide defect or a metal defect escaping based on a typical process requiring four oxide etches and one level of metallization, and considering each inspection independent, is computed by the following equation:

$$P(E_T) = 1 - Q(E_O)^4 Q(E_M)$$

$P(E_T)$ is the probability of a circuit with an oxide defect or a metal defect escaping

$$Q(E_O) = (1 - P(E_O))$$

$$Q(E_M) = (1 - P(E_M))$$

The P (E_T)'s for the cases considered in Tables 2.2.5.1-2 and 2.2.5.2-2 are shown in Table 2.2.5.3-1.

TABLE 2.2.5.2-1

PROBABILITY (P (W)) OF WAFER BEING ACCEPTED

No. of Circuits per Wafer	Process Percent Defective 5	10	20	30	40
100	.93	.83	.52	.30	.17
200	.93	.83	.52	.30	.17
300	.97	.90	.65	.36	.16
400	.97	.90	.65	.36	.16

TABLE 2.2.5.2-2

PROBABILITY (P (E_M)) OF A METAL DEFECT ESCAPING

No. of Circuits per Wafer	Process Percent Defective 5	10	20	30	40
100	.046	.083	.104	.090	.068
200	.046	.083	.104	.090	.068
300	.048	.081	.130	.108	.064
400	.048	.081	.130	.108	.064

TABLE 2.2.5.3-1

PROBABILITY P (E_T) OF A DIE WITH EITHER
AN OXIDE DEFECT OR A METAL DEFECT ESCAPING

No. of Circuits per Wafer	No. of Wafers per Lot	Process Percent Defective 5	10	20	30	40
100	5	.219	.379	.380	.243	.140
200	10	.219	.379	.380	.243	.140
300	20	.221	.383	.429	.249	.164
400	40	.221	.383	.502	.249	.137

2.2.5.4 Conclusions from Probability of Escape Calculations

Reviewing the probability (P_{EM}) of a metal defect escaping indicates that the wafer inspection for metal defects is reasonably tight, only yielding a 4.6% to 13% probability of a die with a metal defect escaping depending on the number of circuit/ wafers and the process percent defective of the incoming wafers.

The probability (P_{ED}) of an oxide defect escaping through one level is also reasonably tight with a probability of escape between 4.2% and 13% depending on the lot size and process percent defective of the incoming wafers.

Where the probability of escape becomes high, as would be expected, is when a number of oxide levels are considered independently. These probabilities (P_{ET}) (for a typical 4 oxide level and one metal level process) are between 13.7% and 48.9%, depending on the lot parameter as indicated in Paragraph 2.2.5.3. The probability analysis considers each oxide level inspection as an independent variable, not accounting for the interrelated defects in an actual case. This simplification is certainly a worst case assumption.

The escape probabilities derived herein are a considerable improvement, considering that the present method of visual inspection as required by MIL-STD-883, only looks at the product after the metal and glassivation levels are completed.

The actual probability of a latent defect escaping is very minimal since some of the underlaying oxide and visual defects will be screened out by electrical and environmental tests, and the alternate screening tests derived in Paragraph 3.0. The proof of this statement is shown by the final verification test of Section 4.0.

SECTION 3

3.0 PRELIMINARY VERIFICATION TESTING

The preliminary verification testing consisted of two phases. The first phase developed the alternate screening tests to be run on the packaged LSI devices to be employed to detect uninspectable known visual defects. Phase two consisted of selecting and assembling a group of LSI devices with known visual defects and subjecting them to the alternate screening tests of phase 1. The results of phase 2 were then analyzed to establish the alternate screening procedure to be utilized for the final verification testing.

3.1 ALTERNATE SCREENING PROCEDURES

In order to evaluate alternate screening techniques to use on packaged LSI devices, as alternatives to the high magnification preseal visual inspection, the following screening tests were developed to use in screening the preliminary verification test samples.

- o Electrical measurements
- o Extended stabilization bake
- o Extended temperature cycling
- o Burn-in

3.1.1 Electrical Measurements

Test Condition:

- o High speed functional testing with test vectors with a probability of detection of greater than 95% on random logic devices.
- o Complete parametric testing with stimulus applied to the device for 500 milliseconds on leakage test prior to test measurement.
- o Measurement to be made at maximum rated voltages or currents where applicable.

3.1.2 Extended Stabilization Bake

Test Condition:

Method 1008.1, Test Condition C (+150°C), with test duration extended to 168 hours. The extended test time is an alternate to the 24 hour, +150°C test presently called out by Paragraph 3.1.2, Method 5004.3 of MIL-STD-883.

3.1.3 Extended Temperature Cycling

Test Conditions:

1. Method 1010.1, Test Condition D of MIL-STD-883 (-65°C to +200°C), extended to 100 cycles with electrical end points at 10, 20, 50 and 100 cycles.

2. Method 1010.1, Test Condition C of MIL-STD-883 (-65°C to +150°C), extended to 100 cycles with electrical end points at 10, 20, 50 and 100 cycles.

The Extended temperature of +200°C and the extended number of cycles (100) are alternates to the 10 cycles required by Method 1010.1, Test Condition C of MIL-STD-883 (-65°C to +150°C), called out by Paragraph 3.1.3 of Method 5004.3 of MIL-STD-883.

3.1.4 Burn-in Test Procedures

Test Conditions:

1. Steady State Power Burn-in at +125°C - Method 1015.1, Test Condition B of MIL-STD-883, with test time extended to 1176 hours and electrical end points at 168, 336, 504, 672, 840, 1008 and 1176 hours.

2. Dynamic Clock Driving Burn-in at +125°C - Method 1015.1 of MIL-STD-883, with 125 KHz, 250 KHz and 500 KHz clocks applied at

device inputs and output load of 22 pF to ground - test time and electrical end points the same as test condition 1.

3. Dynamic Pattern Generator Burn-in at +125°C - Method 1015.1 of MIL-STD-883, with the test vector clocked through the inputs at 500 KHz and output load of 22 pF to ground - test time and electrical end points the same as test condition 1.

4. Steady State Power and Reverse Bias Burn-in at +125°C - Method 1015.1, Test Condition C of MIL-STD-883 - test times the same as test condition 1.

3.2 PRELIMINARY VERIFICATION DEVICE SELECTION

For the preliminary verification test samples five different devices were selected. These devices were three custom LSI CMOS arrays, 128239, 128240, 128243, and two CMOS test cells, the Harris test cell and the SCL 5999 test cell. (See Table 3.2)

3.2.1 The CMOS Arrays

The 128239, 128240, 128243, are custom random logic CMOS arrays designed for the Space Shuttle Pulse Code Modulation Master Unit utilizing the Harris ESD Computer Aided Design cell library. The pin functions and the burn-in circuits used during device screening are shown in Tables 3.2.1-1 through 3.2.1-4. The burn-in circuits for the 128239 and the 128240 are dynamic clock driving configuration with 125 KHz, 250 KHz and 500 KHz, 12 volt pulses applied at the device inputs during burn-in. The outputs were all loaded through a 22 pF load to ground. These burn-in circuits were developed by Harris ESD as a worst case burn-in for these custom devices. In order to compare the clock driving configuration to another configuration, the 128243 is arranged in a pattern generator burn-in configuration where the actual test pattern (test vector) is pulsed through the inputs at 500 KHz during burn-in.

TABLE 3.2

PRELIMINARY VERIFICATION TEST DEVICES

Specification Number	Function	Technology	Vendor	Die Size in Mils	Package Used
128239	First Stage I/O Buffer	Metal Gate CMOS	B	216 X 204	48 pin DIP
128240	Second Stage I/O Buffer	Metal Gate CMOS	B	186 X 183	48 pin DIP
128243	Decoder Logic	Metal Gate CMOS	B	205 X 168	40 pin DIP
---	Harris Test Cell	Metal Gate CMOS	B	212 X 212	40 pin DIP
SCL 5999	Test Cell	Metal Gate CMOS	B	67 X 66	40 pin DIP

TABLE 3.2.1-1

128239 PIN FUNCTIONS AND
BURN-IN CONFIGURATION

Input No.	Input Function	Output No.	Output Function
1	All Zero Load	1	Inhibit Priority
2	CMD WD RDY-RAM STR	2	AR BIT 0
3	Load I/O Not	3	RAM Input 2
4	Load Ram Input	4	Op Code A'3
5	I/O Clock	5	RAM Input 1
6	Comp/MDM	6	Op Code A'4
7	Load Counters	7	RAM Input 3
8	ROM 36/RAM 3	8	Op Code A'5
9	ROM 37/RAM 2	9	Op Code A'6
10	ROM 38/RAM 1	10	NRZ Out
11	ROM 39	11	End of Msg Not
12	ROM 40	12	Correct Add Not
13	ROM 41	13	I/O Bit 10 Comp I/O
14	ROM 42	14	Add No Resp
15	ROM 43		
16	ROM 14		
17	ROM 13	Power	V_{DD1} - 12.0 volts DC
18	BIT 1		V_{DD2} - 5.25 volts DC
19	BIT 2		Ground
20	BIT 3		
21	I/O BIT 12		

Burn-in Configuration - Dynamic Clock Driving

1. 12 volts DC at V_{DD1}, Inputs No. 1 and 3.
2. 5.25 volts DC at V_{DD2}.
3. Ground at Inputs No. 2, 9, 10, 12, 13, 14, 15, 16, 18, 19, 20.
4. 125 KHz ±12 KHz, 12 volt pulse at Inputs No. 8, 11, 17, 21.
5. 500 KHz ±50 KHz, 5 volt pulse at Inputs No. 4, 5, 7.
6. All output functions connected through a 22 pF load to ground.

TABLE 3.2.1-2

128240 PIN FUNCTIONS AND

BURN-IN CONFIGURATION

Input No.	Input Function	Output No.	Output Function
1	All Zero Load	1	R14
2	Cmd Wd Rdy - RAM Str	2	I/O Bit 12
3	Load I/O Not	3	RI 5
4	I/O Bit 20	4	RI 6
5	I/O Clock	5	RI 7
6	WR 3	6	RI 8
7	WR 4	7	RI 9
8	WR 5	8	RI 10
9	Load Pulse	9	RI 11
10	Priority Req Clk	10	I/O 19
11	WR 2	11	I/O 18
12	WR 1	12	I/O 17
13	ROM 28/RAM 11	13	I/O 13
14	ROM 29/RAM 10	14	I/O 16
15	ROM 30/RAM 9	15	I/O 14
16	ROM 31/RAM 8	16	I/O 15
17	ROM 32/RAM 7	17	All 1's
18	ROM 33/RAM 6		
19	ROM 34/RAM 5	Power	V_{DD1} - 12.0 volts DC
20	ROM 35/RAM 4		V_{DD2} - 5.25 volts DC
21	Load RAM Input		Ground

Burn-in Configuration - Dynamic Clock Driving

1. 12 volts DC at V_{DD1}, Input No. 3, 6, 7, 8, 11, 12.
2. 5.25 volts DC at V_{DD2}.
3. Ground at Input No. 1, 20, 19, 18, 17, 16, 15, 14, 13, 9.
4. 125 KHz ±12 KHz, 12 volt pulse at Input 21.
5. 250 KHz ±25 KHz, 12 volt pulse at Inputs 2, 4.
6. 500 KHz ±50 KHz, 12 volt pulse at Inputs 5, 10.
7. All output functions connected through a 22 pF load to Ground.

TABLE 3.2.1-3

128243 PIN FUNCTIONS

Input No.	Input Function	Output No.	Output Function
1	AR Bit 0	1	Bit 1
2	ROM 12 or I/O 13	2	Bit 2
3	ROM 11 or I/O 14	3	Bit 3
4	ROM 10 or I/O 15	4	Bit 4
5	ROM 9 or I/O 16	5	Bit 5
6	ROM 8 or I/O 17	6	Bit 6
7	ROM 7 or I/O 18	7	Bit 7
8	ROM 6 or I/O 19	8	Bit 8
9	ROM 5 or I/O 20	9	Bit 9
10	ROM 4 or I/O 21	10	Bit 10
11	ROM 3 or I/O 22	11	Bit 11
12	Address Clock	12	Decode 29
13	Load Counters	13	Decode 26
14	500 KHz	14	Decode 22
15	Clear Counters	15	Decode 17
		16	Decode 15
		17	Decode 0
		18	Load Pulse

Power	V_{DD1} - 12.0 volts DC
	V_{DD2} - 5.25 volts DC
	Ground

TABLE 3.2.1-4

128243 BURN-IN CONFIGURATION

PATTERN GENERATOR

The following Test Vector Pattern, which is the same as that used for the high speed functional testing, was applied to the inputs of the device during Burn-in with a 500 KHz clock. Rated power of V_{DD1} = 12 VDC and V_{DD2} = 5.25 VDC was applied. In addition, all output functions connected through a 22 pF load to ground.

Test No.	Device Inputs 12345 15	Test No.	Device Inputs 12345 15	Test No.	Device Inputs 12345 15
1	00000 00000 00111	46	00000 00000 00010	91	00000 00000 00000
2	00000 00000 00010	47	00000 00000 01010	92	00000 00000 00010
3	11111 11111 10010	48	00000 00000 00010	93	00000 00000 00000
4	11111 11111 10110	49	00000 00000 01010	94	00000 00000 00010
5	11111 11111 10010	50	00000 00000 00010	95	00000 00000 00000
6	00000 00000 00010	51	00000 00000 01010	96	00000 00000 00010
7	00000 00000 00110	52	00000 00000 00010	97	00000 00000 00000
8	00000 00000 00010	53	00000 00000 01010	98	00000 00000 00010
9	00000 00000 01010	54	00000 00000 00010	99	00000 00000 00000
10	00000 00000 00010	55	00000 00000 01010	100	00000 00000 00010
11	00000 00000 01010	56	00000 00000 00010	101	00000 00000 00000
12	00000 00000 00010	57	00000 00000 01010	102	00000 00000 00010
13	00000 00000 01010	58	00000 00000 00010	103	00000 00000 00000
14	00000 00000 00010	59	00000 00000 01010	104	00000 00000 00010
15	00000 00000 01010	60	00000 00000 00010	105	00000 00000 00000
16	00000 00000 00010	61	00000 00000 01010	106	00000 00000 00010
17	00000 00000 01010	62	00000 00000 00010	107	00000 00000 00000
18	00000 00000 00010	63	00000 00000 01010	108	00000 00000 00010
19	00000 00000 01010	64	00000 00000 00010	109	00000 00000 00000
20	00000 00000 00010	65	00000 00000 01010	110	00000 00000 00010
21	00000 00000 01010	66	00000 00000 00010	111	00000 00000 00010
22	00000 00000 00010	67	00000 00000 01010	112	00000 00000 00010
23	00000 00000 01010	68	00000 00000 00010	113	00000 00000 00000
24	00000 00000 00010	69	00000 00000 01010	114	00000 00000 00010
25	00000 00000 01010	70	00000 00000 00010	115	00000 00000 00000
26	00000 00000 00010	71	00000 00000 01010	116	00000 00000 00010
27	00000 00000 01010	72	00000 00000 00010	117	00000 00000 00000
28	00000 00000 00010		[1]	118	00000 00000 00010
29	00000 00000 01010	73	00000 00000 00000	119	00000 00000 00000
30	00000 00000 00010	74	00000 00000 00010	120	00000 00000 00010
31	00000 00000 01010	75	00000 00000 00000	121	00000 00000 00000
32	00000 00000 00010	76	00000 00000 00010	122	00000 00000 00010
33	00000 00000 01010	77	00000 00000 00000	123	00000 00000 00000
34	00000 00000 00010	78	00000 00000 00010	124	00000 00000 00010
35	00000 00000 01010	79	00000 00000 00000	125	00000 00000 00000
36	00000 00000 00010	80	00000 00000 00010	126	00000 00000 00010
37	00000 00000 01010	81	00000 00000 00000	127	00000 00000 00000
38	00000 00000 00010	82	00000 00000 00010	128	00000 00000 00010
39	00000 00000 01010	83	00000 00000 00000	129	00000 00000 00000
40	00000 00000 00010	84	00000 00000 00010	130	00000 00000 00010
41	00000 00000 01010	85	00000 00000 00000	131	00000 00000 00000
42	00000 00000 00010	86	00000 00000 00010	132	00000 00000 00010
43	00000 00000 01010	87	00000 00000 00000	133	00000 00000 00000
44	00000 00000 00010	88	00000 00000 00010	134	00000 00000 00010
45	00000 00000 01010	89	00000 00000 00000	135	00000 00000 00000
		90	00000 00000 00010	136	00000 00000 00010

[1] At the end of Test No. 72, 1984 toggles (0, 1) are added to Input 12.

3.2.2 Harris Test Cell

The Harris Test Cell is a representation of a CMOS computer aided cell family. This test cell was used by Harris ESD as a design verification tool in developing a cell library. The test cell is made up of a number of individual logic cell sets. As can be seen from the Pin Functions of Table 3.2.2-1, each cell set has a separate output. The burn-in configuration also shown in Table 3.2.2-1 was a steady state power burn-in.

3.2.3 SCL 5999 Test Cell

The SCL 5999 test cell is a CMOS test cell made up of the following test components:

Step Matrix

- o 0.3 mil metal run
- o 0.4 mil metal run

Oxide Matrix

- o Metal over N+
- o Metal over N-
- o Metal over P+
- o Metal over P-

2 X 2 Transistors (CMOS complementary pair)

Diffused Resistors

- o P- diffused resistor
- o P+ diffused resistor
- o N+ diffused resistor

Multiple Contact

- o Metal run with 1200 contacts

TABLE 3.2.2-1

HARRIS TEST CELL

PIN FUNCTIONS AND BURN-IN CONFIGURATION

Input No.	Input Function
1	Stimulus A
2	Stimulus B
3	Stimulus C
4	Stimulus D
5	Stimulus E
6	Stimulus F
7	Stimulus G
Power (nominal rating)	
1	V_{DD1} +5.5 volts DC
2	Ground
Burn-in Configuration	
1	Input Stimulus and ground Grounded (Input No. 1 thru 7)
2	+7 volts DC at V_{DD1} (absolute maximum rating)

Output No.	Output Function
1	Output Buffer Pad 2
2	Output Buffer Pad 2
3	2-Input AND, 4-Input AND
4	2-Input AND, 3-Input NAND
5	3-Input NOR, 3-Input OR
6	2-Input NOR, $\overline{AB}$ Decode
7	Inverter, 3 Bit and MPX, Full Adder, 2, 2, and 2 NOR MPX Register
8	SS Inverter, 3 Bit and MPX Full Adder - ΣO
9	2 Bit and MPX
10	HS 2-Input NAND HS NI Buffer
11	HS 4-Input NAND
12	HS Inverter HS EX-OR
13	2-Input OR delay, 4-Input OR Delay
14	2-Input NOR
15	Divide by 8 Ripple Counter
16	Divide by 8 Up/Down Counter
17	Divide by 8 Johnson Counter
18	Hi-Z Inverter
19	Inverter String Oscillator
20	NAND Pair Delay
21	NAND Pair Delay Reference
22	NOR Pair Delay Reference
23	Hi Speed 2-Input NOR
24	4-Input NOR
25	High Speed Inverter Pair Delay Reference
26	High Speed Inverter Pair Delay
27	STD Speed Inverter Pair Delay Reference
28	STD Speed Inverter Pair Delay

Bipolar Combination

- o Bipolar transistor
- o Zener diode
- o Bipolar diode

Quad 4 P MOS transistors

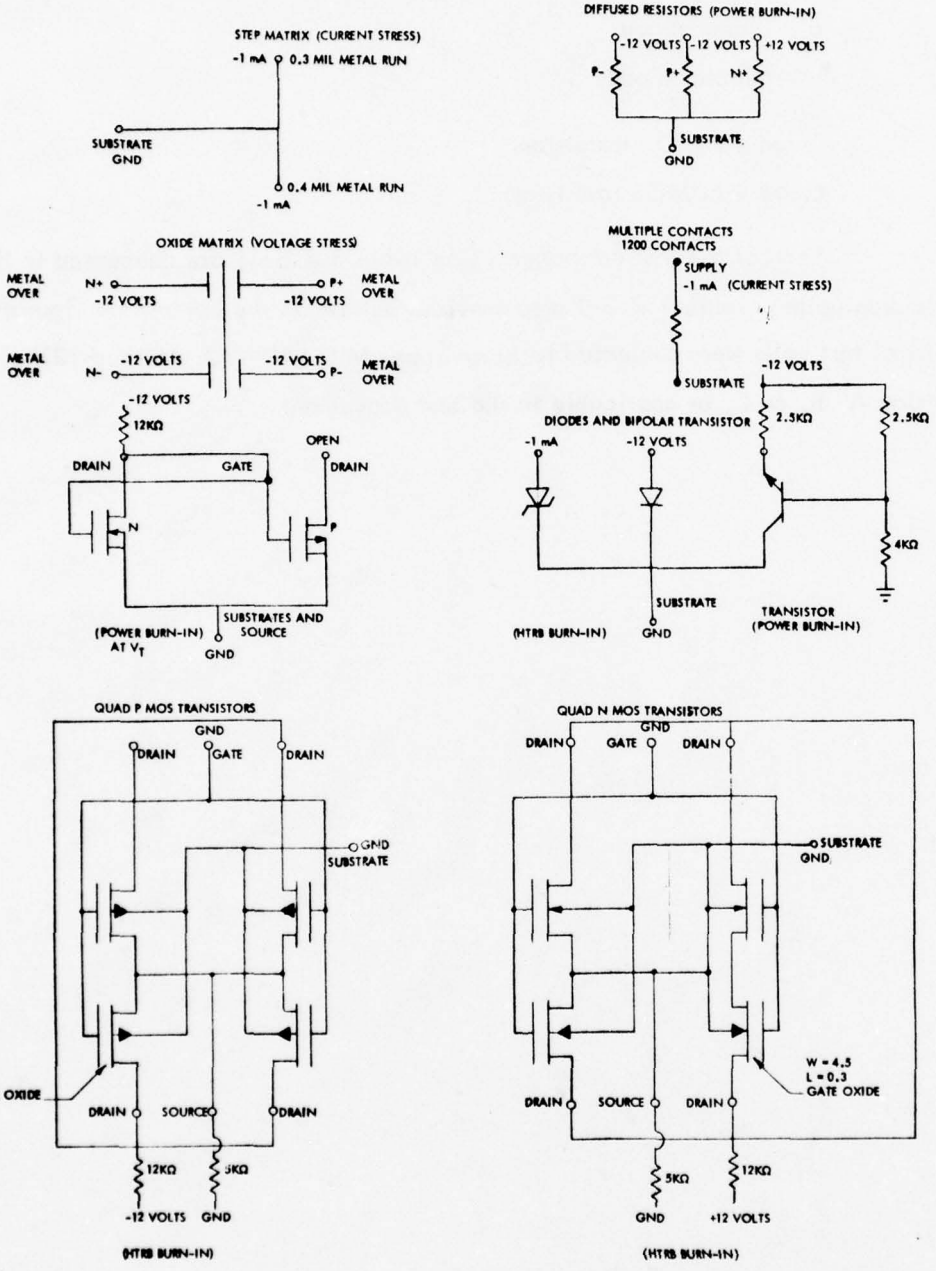
Quad 4 N MOS transistors

Each of the test components (see Table 3.2.3-1) are connected to the outside package pins. Table 3.2.3-1 also provides details on the burn-in configuration. The individual test cells were subjected to burn-in per MIL-STD-883, Method 1015.1, Condition A, B, or C, as applicable to the test component.

TABLE 3.2.3-1

SCHEMATIC DIAGRAM AND BURN-IN CONFIGURATION FOR SCL 5999 TEST CELL

( ) = BURN-IN CONDITIONS



3.3 PRELIMINARY VERIFICATION DEVICE ASSEMBLY AND ALTERNATE SCREENING

The five preliminary verification device types were separated into visual defect categories, assembled into 40 pin and 48 pin DIP packages, electrically tested and screened to a matrix of the alternate screening tests developed in Section 3.1.

3.3.1 Preliminary Verification Device Die Sort

The die from the five device types selected for the preliminary verification study were visual inspected under the high magnification requirements of Method 2010 of MIL-STD-883 and sorted into the defect categories as indicated in Table 3.3.1-1. All the array dice (128239, 128240, 128243) were previously rejected by Vendor B to MIL-STD-883, Method 2010 , Test Condition B. The visual defects were formed into a matrix by defect category and device type as shown in Table 3.3.1-2 prior to being started into assembly.

3.3.2 Preliminary Verification Device Assembly

The devices were assembled into 40 pin and 48 pin ceramic DIP packages as shown in Figures 3.3.2-1 and 3.3.2-2. The die attach was accomplished with Dupont 5504 epoxy. The die wire bonding was with 1.25 mil aluminum wire. The packages were braze sealed at +300°C under vacuum. The matrix showing the assembly steps with the number of devices rejected at each assembly operation is included as Table 3.3.2-3. Once the devices completed the assembly sequence, the number of devices by defective category were once again tabulated. These results are shown in Table 3.3.2-4.

TABLE 3.3.1-1

DEFECT CATEGORIES OBSERVED IN
PRELIMINARY VERIFICATION SAMPLES

Type of Defect	Inspection Criteria or Paragraph of MIL-STD-883 Method 2010.2, Used for Die Inspection
Bridging Metal	3.1.1.6[1]
Metal Voids	3.2.1.2
Foreign Material	3.1.6.1[2] Paragraphs b and c only
Photoresist/Diffusion	3.2.2 and 3.2.7
Questionable	Other foreign material or contamination not rejectable by Method 2010.2

1 The criteria of Test Condition A was used here since 50% separation between metal interconnection is easier for an inspector to judge rather than the 0.1 mil criteria of Condition B. In general, there are wide variations between manufacturers on the implementation and interpretation of this criteria.

2 The criteria of Test Condition A was used here since it is difficult to determine if an unattached particle is only attached at the top surface of the glassivation. In general, there are wide variations between manufacturers on the implementation and interpretation of this criteria.

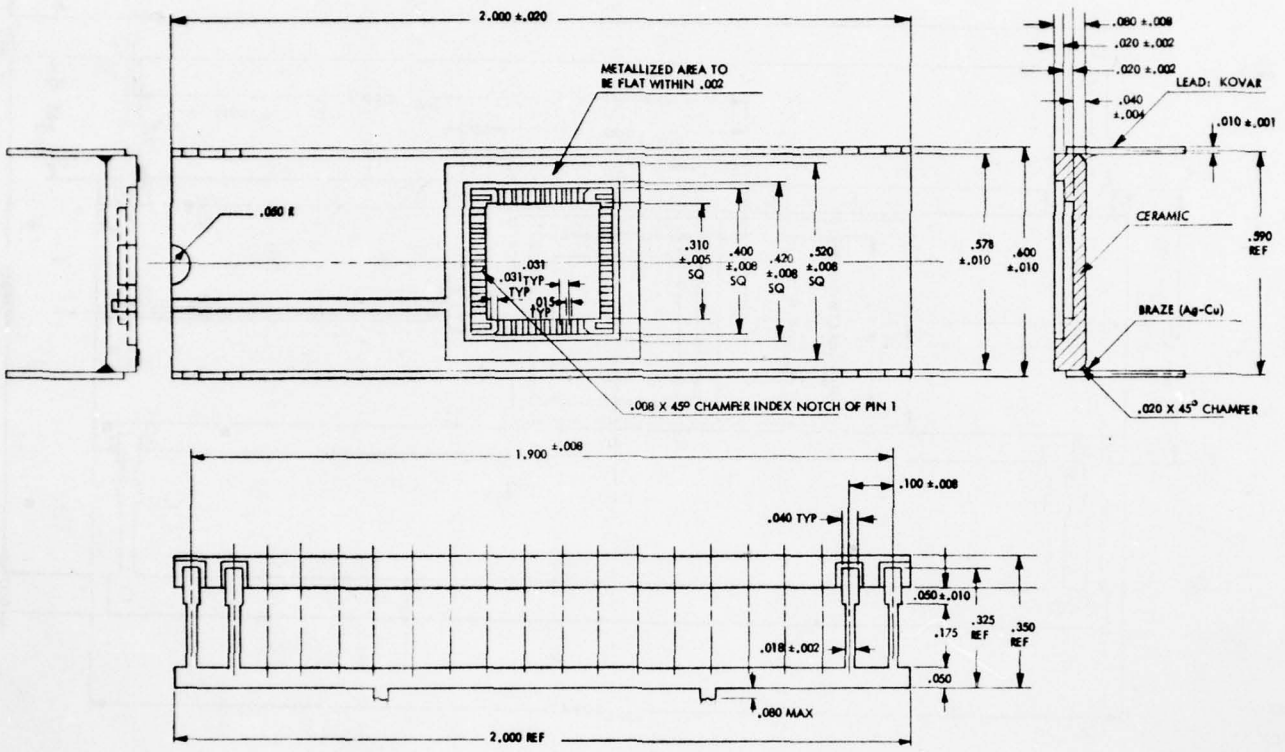


FIGURE 3.3.2-1 40 LEAD SIDE BRAZED CERAMIC DIP PACKAGE USED FOR PRELIMINARY VERIFICATION TEST

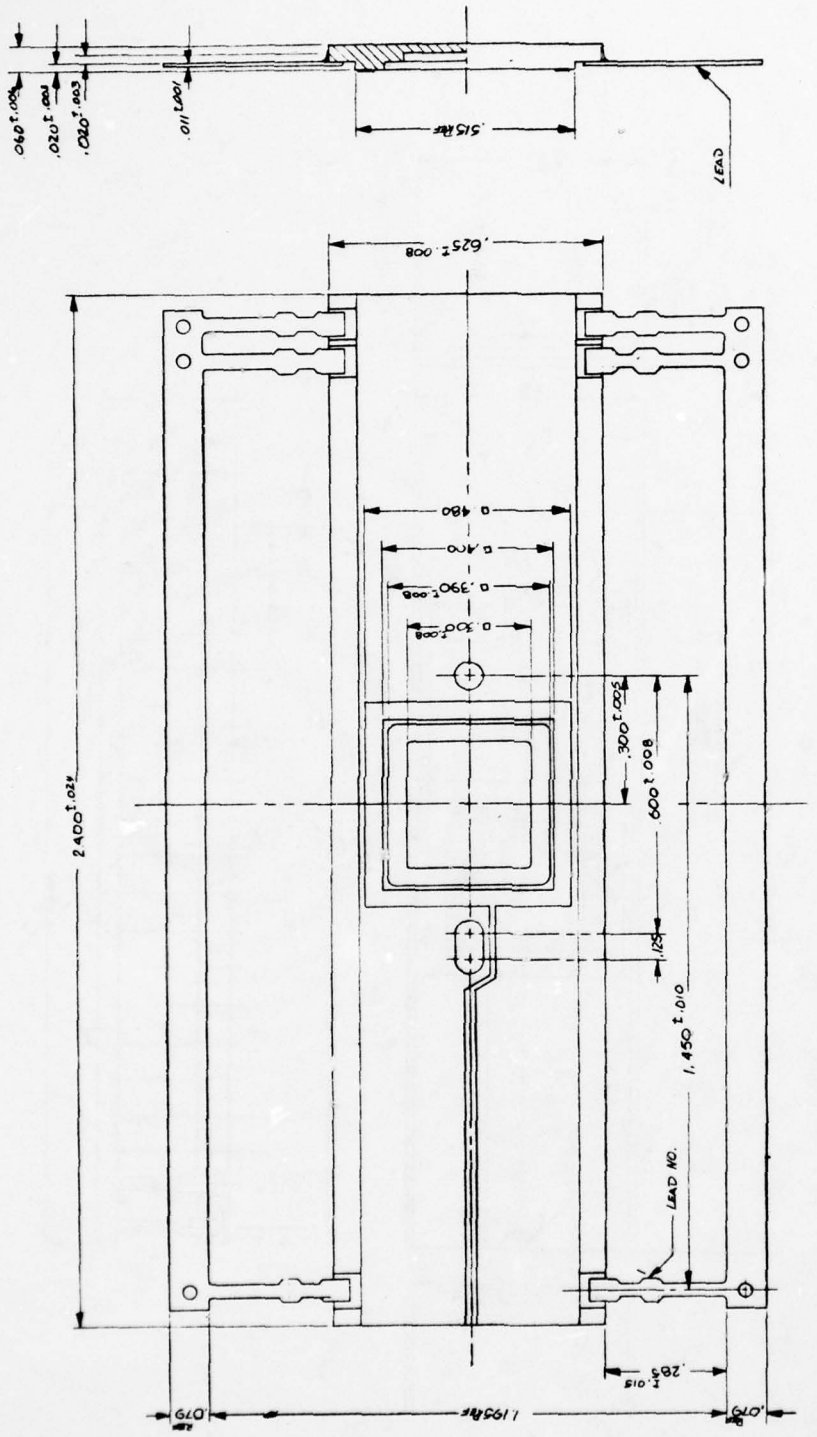


FIGURE 3.1.2-2 48 LEAD TOP BRAZED CERAMIC DIP PACKAGE USED FOR PRELIMINARY VERIFICATION TEST

TABLE 3.3.1-2

MATRIX OF DEVICES STARTED INTO ASSEMBLY BY DEFECT CATEGORY

Defect Category	SCL 5999 Test Cell	Harris Test Cell	128243 Custom LSI CMOS Array	128240 Custom LSI CMOS Array	128239 Custom LSI CMOS Array	Total
Photoresist/ Diffusion	19	58	18	13	10	118
Bridging Metal	12	18	16	15	17	78
Metal Voids	4	36	15	22	21	98
Foreign Material	30	1	27	0	15	83
Questionable	53	0	13	3	12	81
Good (control units)	20	20	9	8	13	70
TOTAL	138	133	108	61	88	528

TABLE 3.3.2-3

MATRIX SHOWING NUMBER OF DEVICES
REJECTED AT EACH ASSEMBLY OPERATION

Assembly Operation	Device Type / Package	SCL 5999 Test Cell 40 Lead	Harris Test Cell 40 Lead	128243 Custom LSI CMOS Array 40 Lead	128240 Custom LSI CMOS Array 48 Lead	128239 Custom LSI CMOS Array 48 Lead	Total Rejects
Die Mounting		5	0	2	0	0	7
Die Bonding		5	13	5	3	3	29
Fine Leak MIL-STD-883, Method 1014		4	2	3	0	2	11
Gross Leak MIL-STD-883 Method 1014		2	15	2	1	7	27
Lead Clipping		0	1	0	0	1	2
Total Rejects		16	31	12	4	13	76
Total Remaining Devices		122	103	96	57	75	

TABLE 3.3.2-4

MATRIX SHOWING NUMBER OF DEVICES BY VISUAL DEFECT
COMPLETING ASSEMBLY PRIOR TO INITIAL ELECTRICAL TESTING

Defect Category	SCL 5999 Test Cell	Harris Test Cell	128243 Custom LSI CMOS Array	128240 Custom LSI CMOS Array	128239 Custom LSI CMOS Array	Total Rejects
Photoresist/Diffusion	19	45	17	12	10	103
Bridging Metal	9	12	14	14	17	66
Metal Voids	2	29	14	20	19	84
Foreign Material	29	1	32	0	10	72
Questionable	46	0	11	3	12	72
Good (control units)	17	16	8	8	7	56
TOTAL	122	103	96	57	75	453

3.3.3 Preliminary Verification Device Electrical Testing

As a potential alternate screening method the electrical test times were extended and maximum voltages applied on all devices as indicated in Paragraph 3.1.1. This was the only change between the electrical testing at probe and the initial electrical testing after packaging.

The CMOS arrays (128243, 128240 and 128239) and the Harris test cell were also comprehensively functionally tested at 500 KHz as the main mode of testing with DC parametric data read and recorded on leakage currents. The SCL 5999 test cell had DC parametric testing performed on the key electrical parameters as shown in Table 3.3.3-1.

The electrical defects by visual defect category are shown in Table 3.3.3-2. Since the SCL 5999 test cell had a probe criteria to pass the device based on any element being good, the initial electrical test results are not included in the summary.

3.3.4 Preliminary Verification Device Matrix Screening

After completion of electrical testing, the devices were separated by visual defect category into the test matrix as shown in Table 3.3.4-1. The results from this matrix are summarized and analyzed in the following paragraphs and utilized to develop the alternate screening procedure.

3.3.4.1 128243 Custom LSI CMOS Array - Screening Summary

The screening summary for the 128243 Custom LSI CMOS Array is shown in Table 3.3.4.1-1. As indicated in the Table, 23 devices categorized by various visual die defects were temperature cycled from -65°C to +150°C for 100 cycles per Test Condition 2 of Paragraph 3.1.3 without any failures occurring.

An additional ten devices were temperature cycled from -65°C to +200°C for 100 cycles per Test Condition 1 of Paragraph 3.1.3. As indicated in Table 3.3.4.1-1 one device failed functional testing after 100 cycles. Failure analysis of this device revealed a lifted post bond.

TABLE 3.3.3-1

ELECTRICAL PARAMETERS TESTED ON SCL 5999 TEST CELL

Test Component	Electrical Tests Performed
Step Matrix	Resistance
Oxide Matrix	Leakage Current
2 X 2 CMOS Transistor	Threshold Voltage On Resistance Leakages
Bipolar Transistor	I_{CEO} $V_{CE(sat)}$ h_{FE}
Bipolar Diodes	Breakdown Voltages Reverse Currents Forward Currents
Quad P-MOS Transistors	Threshold Voltage On Resistance Leakages
Quad N-MOS Transistors	Threshold Voltage On Resistance Leakages

TABLE 3.3.3-2

ELECTRICAL REJECTS BY VISUAL DEFECT CATEGORY

Device	Category	Good	Photoresist/ Diffusion	Bridging Metal	Metal Voids	Foreign Material	Questionable
128243	No. of Rejects	3	3	2	3	4	3
Custom LSI	% of defect category	37.5%	17.6%	14.2%	17.6%	12.5%	27.2%
CMOS Array	% of total	3.2%	3.2%	2.1%	3.2%	4.1%	3.2%
128240	No. of Rejects	0	0	2	3	0	1
Custom LSI	% of defect category	--	--	14.2%	15%	--	33%
CMOS Array	% of total	--	--	3.5%	5.2%	--	1.8%
128239	No. of Rejects	4	4	7	3	8	7
Custom LSI	% of defect category	57.1%	40%	41.2%	15.8%	80%	58.3%
CMOS Array	% of total	5.3%	5.3%	9.3%	4%	10.7%	9.3%
Harris Test Cell	No. of Rejects	2	6	5	7	0	0
	% of defect category	12.5%	13.3%	41.6%	24.1%	--	--
	% of total	1.9%	5.8%	4.8%	6.8%	--	--

TABLE 3.3.4-1

SCREENING TEST MATRIX

Showing Number of Visual Defects by Defect Category Submitted to Each Alternate Screening Test

Candidate for Alternate Screening Procedure	128243 Custom LSI CMOS Array		128240 Custom LSI CMOS Array		128239 Custom LSI CMOS Array		Harris Test Cell		SCL 5999 Test Cell	
	Defect Category	Number of Devices Tested	Defect Category	Number of Devices Tested	Defect Category	Number of Devices Tested	Defect Category	Number of Devices Tested	Defect Category	Number of Devices Tested
Temperature Cycle Extended cycles (-65°C to +150°C, 100 cycles) Paragraph 3.1.3 Test Condition 2	Metal voids	6	Metal voids	10			Metal voids	6		
	Foreign material	7	Metal bridging	1			Photoresist/diffusion	13		
	Photoresist/diffusion	9	Good	2			Good	2		
	Good	1								
	Total Devices Tested	23	Total Devices Tested	13			Total Devices Tested	21		
Temperature Cycle Extended extremes and Extended cycles (-65°C to +200°C, 100 cycles) Paragraph 3.1.2 Test Condition 1	Foreign material	3	Photoresist/diffusion	6	Metal bridging	9	Metal bridging	5	Metal voids	2
	Questionable	6	Good	2	Metal voids	1	Photoresist/diffusion	10	Foreign material	10
	Good	1					Good	3	Questionable	17
									Good	7
	Total Devices Tested	10	Total Devices Tested	8	Total Devices Tested	10	Total Devices Tested	18	Total Devices Tested	36
Stabilization Bake Extended Time (+150°C for 168 hr) Paragraph 3.1.2	Metal bridging	7					Metal voids	7	Metal bridging	9
	Questionable	3					Good	5	Photoresist/diffusion	9
	Good	1							Foreign material	7
									Questionable	18
									Good	9
	Total Devices Tested	11					Total Devices Tested	12	Total Devices Tested	52
Burn-in - Steady State Power (1176HR at +125°C) Paragraph 3.1.4 Test Condition 1 or 4							Metal voids	10	Photoresist/diffusion	10
							Metal bridging	3	Good	2
							Good	2	Foreign material	8
							Photoresist/diffusion	15	Questionable	10
							Total Devices Tested	30	Total Devices Tested	30
Burn-in Dynamic Clock Driving (1176 hr at +125°C) Paragraph 3.1.4 Test Condition 2			Photoresist/diffusion	6	Foreign material	3				
			Metal voids	7	Metal voids	15				
			Metal bridging	12	Photoresist/diffusion	5				
			Questionable	2	Questionable	5				
			Good	3	Good	2				
			Total Devices Tested	30	Total Devices Tested	30				
Burn-in Dynamic Pattern Generator (1176 hr at +125°C) Paragraph 3.1.4 Test Condition 3	Metal bridging	0								
	Photoresist/diffusion	4								
	Metal voids	5								
	Foreign material	14								
	Total Devices Tested	29								

TABLE 3.3.4.1-1

SCREENING SUMMARY
FOR 128243 CUSTOM LSI ARRAY

Screening Procedure	Defect Category	No. of Devices Tested	Electrical Read & Record End Points	Accumulative Functional Failures	Accumulative Parametric Failures	Serial Number of Failures	Visual Defect Category of Failure	Failure Analysis Results
Temperature Cycle Extended Cycles (-65°C to +150°C, 100 cycles) Paragraph 3.1.3 Test Condition 2	Metal voids	6	10 cycles	0	0			
	Foreign material	7	20 cycles	0	0			
	Photoresist/diffusion	9	50 cycles	0	0			
	Good	1	100 cycles	0	0			
	Total Devices Tested -	23						
Temperature Cycle Extended Extremes and Extended Cycles (-65°C to +200°C, 100 cycles) Paragraph 3.1.3 Test Condition 1	Foreign material	3	10 cycles	0	0			
	Questionable	6	20 cycles	0 *	0			
	Good	1	50 cycles	0	0			
			100 cycles	1	0	25	Foreign material	Lifted post bond
	Total Devices Tested -	10						
Stabiliation Bake Extended Time (+150°C for 168 hr) Paragraph 3.1.2	Metal bridging	7	168 hours	0	0			
	Questionable	3						
	Good	1						
	Total Devices Tested -	11						
Burn-In dynamic pattern generator (1176 hr at +125°C) Paragraph 3.1.4 Test Condition 3 and Table 3.2.1-4	Metal bridging	6	168 hours	0	1	74	Bridging metal	Original die defect not cause of failure. Cause of failure not determined.
	Photoresist/diffusion	4	336 hours	0	1			
	Metal voids	5	504 hours	0	1			
	Foreign material	14	672 hours	0	1			
	Total Devices Tested-	29	840 hours	0	1			
			1008 hours	0	1			
			1176 hours	0	1			

* One device dropped and broken during testing.

TOTALS: 73 devices tested
1 functional failure
1 parametric failure

Eleven devices from the sample were stabilization baked at +150°C for 168 hours per Paragraph 3.1.2. None of these devices failed electrically after completion of the testing.

The final test for this device type was a pattern generator dynamic burn-in of 29 devices for 1176 hours at +125°C as described in Paragraph 3.1.4, Test Condition 3 and Table 3.2.1-4. Of the 29 devices subjected to the burn-in one device failed parametric testing due to an increase in input leakage current after the 168 hour end point. The failure analysis on this device was inconclusive; however, it did conclude that the failure was not caused by the initial die defect. (bridging metal)

3.3.4.2 128240 Custom LSI CMOS Array Screening Summary

The screening summary for the 128240 custom LSI CMOS array is shown in Table 3.3.4.2-1. As indicated in the Table, 13 devices categorized by various visual die defects were temperature cycled from -65°C to +150°C for 100 cycles per Test Condition 2 of Paragraph 3.1.3. One device exhibited an input leakage parametric failure after 20 cycles. Failure analysis of this device found the bonding wires were laying across edge of the die. As with most parametric failures, this condition could only be indicated as a possible cause of failure. However, the failure analysis did conclude that the metal void which was the original die defect was not the cause of failure.

An additional eight devices were temperature cycled from -65°C to +200°C for 100 cycles per Test Condition 1 of Paragraph 3.1.3. One device exhibited an input leakage parametric failure after 50 cycles of temperature cycling. Again the exact cause of failure was not determined but the analysis did determine that the original die defect was not related to the failure mechanism.

A separate sample of 30 devices was dynamically burned-in with a clock driving configuration at +125°C to Paragraph 3.1.4, Test Condition 2 and Table 3.2.1-3 followed by 100 cycles of temperature cycling from -65°C to +200°C per Paragraph 3.1.3,

Test Condition 1, as indicated in Table 3.3.4.2-1. One device failed functional testing during burn-in. Failure analysis of this device indicated that the original defect, a void in a metallization path, had completely opened after 1008 hours of burn-in.

3.3.4.3 128239 Custom LSI CMOS Array - Screening Summary

The screening summary for the 128239 custom LSI CMOS array is shown in Table 3.3.4.3-1. As indicated in the Table, 10 devices categorized by various visual die defects were temperature cycled from -65°C to +150°C for 100 cycles per Test Condition 1 of Paragraph 3.1.3. None of the devices failed electrically after completion of the testing. A separate sample of 30 devices was dynamically burned-in with a clock driving configuration for 1176 hours at +125°C to Paragraph 3.1.4, Test Condition 2 and Table 3.2.1-1. This test was followed by 100 cycles of temperature cycling from -65°C to +200°C per Paragraph 3.1.3, Test Condition 1, as indicated in Table 3.3.4.3-1. One device failed functional testing after 336 hours of burn-in. The failure analysis indicated the failure was due to a scratch on the die caused during assembly.

3.3.4.4 Harris Test Cell - Screening Summary

The screening summary for the Harris test cell is shown in Table 3.3.4.4-1. As indicated in the Table, 21 devices were temperature cycled from -65°C to +150°C for 100 cycles per Test Condition 2 of Paragraph 3.1.3. Four devices failed functional testing and one device failed parametric testing during various end points. Summarization of the test results and the failure analysis of these devices indicated the following:

1) The device that failed after 10 cycles of testing was an input leakage parametric failure. Although the exact cause of the increase in leakage was not determined the failure analysis on this device concluded that the original die defect, a metal void, was not the cause of the failure.

TABLE 3.3.4.2-1
SCREENING SUMMARY FOR 128240 CUSTOM LSI ARRAY

Screening Procedure	Defect Category		Electrical Read and Record End Points	Accumulative Functional Failures	Accumulative Parametric Failures	Serial Number of Failures	Visual Defect Category of Failure	Failure Analysis Results
Temperature Cycle Extended Cycles (-65°C to +150°C 100 cycles) Paragraph 3.1.3 Test Condition 2	Metal voids	10	10 cycles	0	0			
	Metal bridging	1	20 cycles	0	1			Original die defect not cause of failure. Possible cause of failure was bonding wires laying on edge of chip
	Good	2	50 cycles	0	1	240	Metal Void	
	Total Devices Tested - 13		100 cycles	0	1			
Temperature Cycle Extended Extremes and Extended Cycles (-65°C to +200°C 100 cycles) Paragraph 3.1.3 Test Condition 1	Photoresist/ Diffusion	6	10 cycles	0	0	220	Photoresist/Diffusion	Initial die defect not cause of failure. Cause of failure not determined.
	Good	2	20 cycles	0	0			
	Total Devices Tested - 8		50 cycles	0	1			
			100 cycles	0	1			
Burn-In - Dynamic Clock Driving (1176 Hrs. at +125°C) Paragraph 3.1.4 Test Condition 2 and Table 3.2.1-2 Followed by Temperature Cycling Extended Extremes and Extended Cycles (-65°C to +200°C 100 cycles) Paragraph 3.1.3 Test Condition 1	Photoresist/ Diffusion	6	168 hours	0	0		Metal void - Failure analysis performed after 1176 hour end point	Metallization opened - Failure caused by original metallization void on chip.
	Metal voids	7	336 hours	0	0			
	Metal bridging	12	504 hours	0	0			
	Questionable	2	672 hours	0	0	223		
	Good	3	840 hours	0	0			
			1008 hours	1	0			
	Total Devices Tested - 30		1176 hours	1	0			
			10 cycles	0	0			
			20 cycles	0	0			
			50 cycles	0	0			
			100 cycles	0	0			

TOTALS: 51 devices tested
1 functional failure
2 parametric failures

TABLE 3.3.4.3-1

SCREENING SUMMARY FOR 128239 CUSTOM LSI ARRAY

Screening Procedure	Defect Category		Electrical Read and Record End Points	Accumulative Functional Failures	Accumulative Parametric Failures	Serial Number of Failures	Visual Defect Category of Failure	Failure Analysis Results
Temperature Cycle	Metal Bridging	9	10 cycles	0	0			
Extended Extremes	Metal voids	1	20 cycles	0	0			
and Extended Cycles			50 cycles	0	0			
(-65°C to +200°C			100 cycles	0	0			
100 cycles)								
Paragraph 3.1.3	Total Devices							
Test Condition 1	Tested	10						
Burn-in	Foreign material	3	168 hours	0	0			
Dynamic Clock	Metal voids	15	336 hours	1	0	18	Metal void	Metallization opened - Failure caused by tool mark on die made during assembly. Failure analysis performed after 1176 hour end point
Driving (1176	Photoresist/							
Hrs. at +125°C)	Diffusion	5	504 hours	1	0			
Paragraph 3.1.4	Questionable	5	672 hours	1	0			
Test Condition 2	Good	2	840 hours	1	0			
and Table 3.2.1-1			1008 hours	1	0			
Followed by	Total Devices		1176 hours	1	0			
Temperature Cycling	Tested	30	10 cycles	0	0			
Extended Extremes			20 cycles	0	0			
and Extended Cycles			50 cycles	0	0			
(-65°C to +200°C			100 cycles	0	0			
100 cycles)								
Paragraph 3.1.3								
Test Condition 1								

TOTALS: 40 devices tested
1 functional failure

TABLE 3.3.4.4-1

SCREENING SUMMARY FOR HARRIS TEST CELL

Screening Procedure	Defect Category	Electrical Read and Record End Points	Accumulative Functional Failures	Accumulative Parametric Failures	Serial Number of Failures	Visual Defect Category of Failure	Failure Analysis Results
Temperature Cycle Extended Cycles (-65°C to +150°C 100 cycles) Paragraph 3.1.3 Test Condition 2	Metal voids 6 Photoresist/ Diffusion 13 Good 2 Total Devices Tested - 21	10 cycles 20 cycles 50 cycles 100 cycles	0 0 4 4	1 2* 1 1	435 481 442, 481, 511, 507	Photoresist/Diffusion - Serial # 481, 511, 507 Metal void - Serial # 442, 435	#435 - Initial die defect not cause of failure. Exact cause of failure not determined. #481 - Shorted metallization, possible undetected initial visual die defect. #442 - Initial die defect not cause of failure. Exact cause of failure not determined. #511 - Metal bridge caused during assembly. #507 - Lifted post bond
Temperature Cycle Extended Extremes and Extended Cycles (-65°C to +200°C 100 cycles) Paragraph 3.1.3 Test Condition 1	Metal Bridging 5 Photoresist/ Diffusion 10 Good 3 Total Devices Tested - 18	10 cycles 20 cycles 50 cycles 100 cycles	0 1 1 1	1 0** 1 1	417 529	Metal Bridging Photoresist/Diffusion	#417 - Initial die defect not cause of failure. Exact cause of problem not determined. #529 - Metallization opened due to scratch caused during assembly.
Stabilization Bake Extended Time (150°C for 168 Hr.) Paragraph 3.1.2	Metal voids 7 Good 5 Total Devices Tested - 12	168 Hours	0	0			
Burn-in - Steady State Power Burn-in (1176 Hours at +125°C) Paragraph 3.1.4 Test Condition 1 and Table 3.2.2 Followed by Temperature Cycling Extended Extremes and Extended Cycles (-65°C to +200°C 100 cycles) Paragraph 3.1.3 Test Condition 1	Metal voids 10 Metal Bridging 3 Good 2 Photoresist/ Diffusion 15 Total Devices Tested - 30	168 Hours 336 Hours 504 Hours 672 Hours 840 Hours 1008 Hours 1176 Hours	1 1 2 2 2 2 2	0 0 0 0 0 0 0	515 419	Photoresist/Diffusion Metal void	#515 - Metallization opened due to scratch caused during assembly. #419 - Metallization short due to scratch caused during assembly.
		100 cycles***	3	0	476	Photoresist/Diffusion	#476 - Lifted post bond

*Serial #481 changed from a parametric failure to a functional failure after 50 cycles.
**Serial #417 failed at all end points except 20 cycles.
***End points read after 100 cycles only.

TOTALS: 71 devices tested
8 functional failures
2 parametric failures

AD-A052 418 HARRIS CORP MELBOURNE FLA ELECTRONIC SYSTEMS DIV F/G 9/5
QA PROCEDURES FOR COMPLEX MICROCIRCUITS.(U)
DEC 77 L R PARADISO, J L WOLCOTT F30602-76-C-0328
UNCLASSIFIED RADC-TR-77-418 NL

2 OF 3
AD A052418

2) After 20 cycles an additional input leakage failure occurred. At 50 cycles of temperature cycling the failure mode of this device changed to a functional failure. Failure analysis of this device indicated two smeared metallization runs were shorted. Although the original die defect category was a metal void, it is believed that the bridged metal defect was originally in the die.

3) Three additional devices failed functional testing after 50 cycles. Two of the devices, serial numbers 511 and 507, had assembly and/or package oriented defects. Serial number 511 failed due to a metal bridge caused during assembly, and serial number 507 failed due to a lifted post bond. The exact cause of failure of the third device, serial number 442, was not determined, but the analysis concluded that the original die defect was not the cause of failure.

A separate sample of 18 devices was temperature cycled from -65°C to +200°C for 100 cycles per Test Condition 1 of Paragraph 3.1.3. As indicated in Table 3.3.4.4-1 one device failed input leakage after 10 cycles. Analysis of this part indicated the original bridging metal was not the cause of the failure. One additional device failed after 20 cycles which was analyzed to be a scratch caused during assembly.

A separate sample of 30 devices was burned-in under steady state power conditions for 1176 hours at +125°C to Paragraph 3.1.4, Test Condition 1 and Table 3.2.2-1 followed by 100 cycles of temperature cycling from -65°C to +200°C per Paragraph 3.1.3, Test Condition 1. As indicated in Table 3.3.4.4-1 three devices failed for assembly and/or package oriented defects. One device failed at the 168 hour end point and another at the 504 hour end point both due to metallization scratches. The third device failed after 100 temperature cycles due to a lifted post bond.

3.3.4.5 SCL 5999 Test Cell - Screening Summary

The screening summary for the SCL 5999 test cell is shown in Table 3.3.4.5-1. As indicated in the Table, 36 devices categorized by various visual die defects were

TABLE 3.3.4.5-1
SCREENING SUMMARY FOR SCL 5999 TEST CELL

Screening Procedure	Defect Category	Electrical Read & Record End Points	Accumulative Catastrophic Failures	Serial No. of Failures	Visual Defect Category of Failure	Failure Analysis Results: Lifted Post Bonds	Failure Analysis Results: Open or Shorted Metallization Caused Assembly Process	Failure Analysis Results: Capacitor Shorts Possibly Caused by Static	Failure Analysis Results: Open Metallization Resulting from Screening
Temperature Cycle Extended Extremes and Extended Cycles (-65°C to +200°C) Paragraph 3.1.3 Test Condition 1	Metal voids: 2 Foreign material: 10 Questionable: 17 Good: 7 Total devices tested: 36	10 cycles 20 cycles 50 cycles 100 cycles	0 1 6 17	242 258,268,318, 319,246 267,270,271, 324,244,314, 321,322,326, 328,320	Good: 242,246, 244 Foreign Material: 258,268,270, 267,271 Questionable: 324,314,318, 319,321,322, 326,328,320	242 258,268,318 267,270,271, 324	319 shorted 244 shorted	246 314,320,321,322, 326,328	
Stabilization Bake Extended Time (+150°C for 168 hours) Paragraph 3.1.2	Metal bridging: Photoresist/diffusion: 9 Foreign material: 7 Questionable: 18 Good: 9 Total devices tested: 52	168 hours	9	278,221,215, 218,230,239, 251,303,311	Photoresist/ diffusion: 215,218 Metal bridging: 221,230 Foreign Material: 278 Good: 251,239 Questionable: 303,311	278,221		215,218,230,239, 251,303,311	
Burn-in - Steady State (1176 hours at +125°C) Paragraph 3.1.4 Test Condition 1 and 4	Photoresist/diffusion: 10 Good: 2 Foreign material: 8 Questionable: 10 Total devices tested: 30	168 hours 336 hours 504 hours 672 hours 840 hours 1008 hours 1176 hours	1 3 4 8 10 11 12	262 260,302 280 217,306,284, 210 288,290 323 208	Photoresist/ diffusion: 208, 210,217 Foreign Material: 260,262,284,280 Questionable: 288,290,302, 306,323	260 217 288,290	302 open 284 open 208 open		262 - 0.3 mil step matrix opened 280 - open zener diode 306 - open gnd 210 - 0.3 mil step matrix opened 323 - 0.3 mil step matrix opened

Totals: 118 devices tested
38 catastrophic failures

temperature cycled from -65°C to +200°C for 100 cycles per Test Condition 1 of Paragraph 3.1.3. A total of 17 devices exhibited catastrophic failures at various end points during the 100 cycles of test (see Table 3.3.4.5-1). Failure analysis of these devices indicated the following:

1) The device that failed after 20 cycles had a lifted post bond.

2) Of the five devices that failed after 50 cycles three had lifted post bonds, one had shorted metallization caused by assembly processing and one was a shorted capacitor (see oxide matrix of Table 3.2.3-1).

3) After 100 cycles an additional 11 devices failed. Of these failures, four had lifted post bonds, one had shorted metallization caused by assembly processing, and six had shorted capacitors.

An additional 52 devices were stabilization baked at +150°C for 168 hours per Paragraph 3.1.2. As indicated in Table 3.3.4.5-1, nine devices were catastrophic failures after screening. Failure analysis of these devices indicated two lifted post bonds and seven shorted capacitors.

A separate sample of 30 devices were burned-in for 1176 hours at +125°C as indicated in Table 3.2.3-1. A total of 12 devices exhibited catastrophic failures at various end points during the life test (see Table 3.3.4.5-1). Failure analysis of these devices indicated the following:

1) The device that failed after 168 hours of testing had an open metal path in the 0.3 mil step matrix.

2) Two devices failed after 336 hours of testing. One had a lifted post bond and one had an open metallization path caused during assembly.

3) At the 504 hour end point one device had an open metallization path in the zener diode.

4) After 672 hours one device failed for a lifted post bond. A second device had the ground metallization run open. A third device had open metallization caused during the assembly process. The fourth device failed for open metallization in the 0.3 mil step matrix.

5) Both failures after the 840 hour end point were caused by lifted post bonds.

6) The failure after the 1008 hour end point was caused by an open metallization run in the 0.3 mil step matrix.

7) The failure after the 1176 hour end point was due to an open metallization path caused during assembly.

3.3.5 Analysis of Alternate Screening

The results of the alternate screening tests on all devices are summarized and analyzed from two main points of views:

1) The effectiveness of the screening procedure and,
2) The cause of the induced failure.

3.3.5.1 Effectiveness of the Alternate Screening Test

Each of the alternate screening tests, electrical measurements, extended temperature cycling, extended stabilization bake, and burn-in, are analyzed in regard to the end points at which the failure occurred and type of defect screened.

3.3.5.1.1 Electrical Measurements

The extended test times and use of maximum voltages during electrical measurement were programmed into the automatic test tapes and used for all end point measurements. After the initially defective devices were screened out in the initial electrical test, all failures on subsequent end points were analyzed to ascertain whether the extended electrical measurements were of benefit in detecting visual failures. None of the failures were shown to be related to the extended electrical measurements. Of the six failures whose cause was not specifically identified, no link between the visual defect category and the failure symptoms could be found.

3.3.5.1.2 Temperature Cycling

The results from the two different conditions used for temperature cycling are summarized in Table 3.3.5.1.2-1 and Table 3.3.5.1.2-2. In total, four devices failed the -65°C to +150°C test and 12 devices failed the -65°C to +200°C test as functional rejects. Five additional devices failed parametrically. Analyzing the functional/catastrophic/failures (see Table 3.3.5.1.2-1A) reveals that none of the devices failed after 10 cycles of temperature cycling for any of the test conditions. At the 20 cycle end point two devices failed the extended temperature extreme test (-65°C to

TABLE 3.3.5.1.2-1A

SUMMARY OF FUNCTIONAL/CATASTROPHIC FAILURES DURING ALTERNATE SCREENING

Alternate Screening Procedure	Device Type: / Package Size:	128243 Custom LSI CMOS Array 40 Pin	128240 Custom LSI CMOS Array 48 Pin	128239 Custom LSI CMOS Array 40 Pin	Harris Test Cell 40 Pin	SGL 5999 Test Cell 40 Pin	Totals
Temperature Cycle Extended Cycles (-65°C to +150°C, 100 cycles)	Number of Devices Screened:	23	13	0	21	0	57
	End Points	Accumulative Functional Failures	Accumulative Functional Failures	Accumulative Functional Failures	Accumulative Functional Failures	Accumulative Catastrophic Failures	Accumulative Failures
	10 cycles	0	0	N/A	0	N/A	0
	20 cycles	0	0		0		0
	50 cycles	0	0		$4\left(1^1+1^2+1^3+1^4\right)$		$4\left(1^1+1^2+1^3+1^4\right)$
	100 cycles	0	0		4		4
Temperature Cycle Extended Extremes and Extended Cycles (-65°C to +200°C, 100 cycles)	Number of Devices Screened:	10	8	10	18	36	82
		Accumulative Functional Failures	Accumulative Functional Failures	Accumulative Functional Failures	Accumulative Functional Failures	Accumulative Catastrophic Failures	Accumulative Failures
	10 cycles	0	0	0	0	0	0
	20 cycles	0	0	0	1^2	1^1	$2\left(1^2+1^1\right)$
	50 cycles	0	0	0	1	$*5\left(3^1+1^2\right)$	$6\left(3^1+1^2\right)$
	100 cycles	1^1	0	0	1	$*10\left(4^1+1^2\right)$	$12\left(5^1+1^2\right)$
Stabilization Bake Extended Time (+150°C for 168 hours	Number of Devices Screened:	11	0	0	12	52	75
		Accumulative Functional Failures	Accumulative Functional Failures	Accumulative Functional Failures	Accumulative Functional Failures	Accumulative Catastrophic Failures	Accumulative Failures
		0	N/A	N/A	0	2^1	2^1

Note	Defect Cause	Total Defects Found by Cause in Temperature Cycle and Stabilization Bake
1	Lifted Post Bond	12
2	Open or shorted metallization caused during assembly (tool marks or misplaced bonds)	4
3	Cause of failure undetermined	1
4	Original visual die defect caused failure	1

* Shorted capacitors not shown in Summary.

TABLE 3.3.5.1.2-1B

SUMMARY OF FUNCTIONAL/CATASTROPHIC FAILURES DURING ALTERNATE SCREENING

Alternate Screening Procedure	Device Type:	128243 Custom LSI CMOS Array	128240 Custom LSI CMOS Array	128239 Custom LSI CMOS Array	Harris Test Cell	SCL 5999 Test Cell	Totals
	Package Size:	40 Pin	48 Pin	40 Pin	40 Pin	40 Pin	
	Number of Devices Screened:	29	30	30	30	30	149
	End Points	Accumulative Functional Failures	Accumulative Functional Failures	Accumulative Functional Failures	Accumulative Functional Failures	Accumulative Catastrophic Failures	Accumulative Failures
Burn-In (1176 hours at +125°C)	168 hours	0	0	0	1^{2}	1^{5}	$2(1^{2}+1^{5})$
	336 hours	0	0	1^{2}	1	$3(1^{1}+1^{2})$	$5(1^{1}+2^{2})$
	504 hours	0	0	1	2^{2}	4^{5}	$7(1^{2}+1^{5})$
	672 hours	0	0	1	2	$8(1^{1}+1^{2}+2^{5})$	$11(1^{1}+1^{2}+2^{5})$
	840 hours	0	0	1	2	$10(2^{1})$	$13(2^{1})$
	1008 hours	0	1^{4}	1	2	11^{5}	$15(1^{4}+1^{5})$
	1176 hours	0	1	1	2	12^{2}	$16(1^{2})$
Temperature Cycle Extended Extremes and Extended Cycles (-65°C to +200°C, 100 cycles)	10 cycles		1	1	N/A		-
	20 cycles		1	1	N/A		-
	50 cycles		1	1	N/A		-
	100 cycles		1	1	3^{1}		$17(1^{1})$

Note	Defect Cause	Total Defects Found by Cause in Burn-in and Burn-in followed by Temperature Cycle
1	Lifted post bond	5
2	Open or shorted metallization caused during assembly (tool marks or misplaced bonds)	6
4	Original visual die defect cause of failure	1
5	Open metallization resulting from screening (open metal over oxide step)	5

TABLE 3.3.5.1.2-2
SUMMARY OF PARAMETRIC FAILURES DURING ALTERNATE SCREENING

Alternate Screening Procedure	Device Type	128243 Custom LSI Array	128240 Custom LSI Array	Harris Test Cell	128239 Custom LSI Array	TOTALS
	Number of Devices Screened	23	13	21	0	57
	End Points	Accumulative Parametric Failures	Accumulative Parametric Failures	Accumulative Parametric Failures	Accumulative Parametric Failures	Accumulative Parametric Failures
Temperature Cycles Extended Cycles (-65°C to +150°C, 100 cycles)	10 cycles	0	0	1	N/A	1
	20 cycles	0	1	2*		3
	50 cycles	0	1	2		3
	100 cycles	0	1	2		3
	Number of Devices Screened	0	8	18	10	36
	End Points	Accumulative Parametric Failures	Accumulative Parametric Failures	Accumulative Parametric Failures	Accumulative Parametric Failures	Accumulative Parametric Failures
Temperature Cycles Extended Extremes and Extended Cycles (-65°C to +200°C, 100 cycles)	10 cycles	N/A	0	1	0	1
	20 cycles		0	0**	0	0
	50 cycles		1	1	0	2
	100 cycles		1	1	0	2
	Number of Devices Screened	29	30	30	30	89
	End Points	Accumulative Parametric Failures	Accumulative Parametric Failures	Accumulative Parametric Failures	Accumulative Parametric Failures	Accumulative Parametric Failures
Burn-in (1176 hours at +125°C)	168 hours	1	0	0	0	1
	336 hours	1	0	0	0	1
	504 hours	1	0	0	0	1
	672 hours	1	0	0	0	1
	840 hours	1	0	0	0	1
	1008 hours	1	0	0	0	1
	1176 hours	1	0	0	0	1

*Changed to a functional failure of 50 cycles.

**Same device failed all end points except after 20 cycles.

+200°C). At 50 cycles a total of 10 devices failed both temperature cycling tests. The 100 cycle end point revealed six additional failures in the -65°C to +200°C test.

Analyzing the parametric failures (see Table 3.3.5.1.2-2) indicates two devices failed after 10 cycles, one for each test condition. At the 20 cycle end point, two devices failed on the -65°C to +150°C test. This same device failed functionally at the 50 cycle end point. One additional device also failed the -65°C to +200°C test after 50 cycles.

3.3.5.1.3 Stabilization Bake

The results from the extended stabilization bake are shown in Table 3.3.5.1.2-1A. Only one device failed out of 75 screened.

3.3.5.1.4 Burn-in

The results from the burn-ins are summarized in Tables 3.3.5.1.2-1B and 3.3.5.1.2-2. The dynamic burn-ins produced a total of two defects in 89 devices. The power burn-in produced two failures in 30 devices. Twelve failures were produced in the 30 SCL 5999's which were on a combination of power and reverse bias burn-in.

As can be seen from Table 3.3.5.1.2-2, the dynamic pattern generator burn-in run on the 128243's did not produce any failures through the 1176 hours of testing. The dynamic clock driving burn-in performed on the 128240's and 128239's did, however, produce one failure on each device type. The 128240 failed after 1008 hours of burn-in while the 128239 failed at the 336 hour end point. The twelve failures on the SCL 5999 burn-in occurred throughout the test.

3.3.5.1.5 Burn-in Followed by Temperature Cycling

The results of this test sequence are shown in Table 3.3.5.1.2-1B. Only one failure, of 90 devices tested, occurred after 100 cycles of -65°C to +200°C temperature cycling.

3.3.5.2 Cause of the Induced Failures

Analysis of the failures shows that the causes can be related to a specific fabrication or screening process and corrective action may be taken.

3.3.5.2.1 Seventeen Failures - Lifted Post Bonds

These failures were on the 40 lead package only. (see Appendix E) Ten occurred in the -65°C to +200°C temperature cycle at greater than 10 cycles, one in the -65°C to +150°C temperature cycle, four in life test and two in stabilization bake.

3.3.5.2.2 Ten Failures - Tool Marks and Misplaced Bonds

Six occurred in life test, three in the -65°C to +200°C temperature cycle and one in the -65°C to +150°C temperature cycle test. The misplaced bond problem was primarily due to the fact that the SCL 5999 bonding pads were extremely small.

3.3.5.2.3 Five Failures - Open Metallization in Screening

This grouping of failures is due to open metal runs generally over an oxide step, and all were detected in life test.

3.3.5.2.4 Two Failures - Original Die Defect

One was detected at 50 cycles of temperature cycling from -65°C to +150°C, one was found at 1008 hours of life test.

3.3.5.2.5 Seven Failures - Cause Undetermined

This group includes one functional and six parametric failures. Four occurred in the -65°C to +150°C and two in the -65°C to +200°C temperature cycles and one in burn-in.

3.3.5.2.6 Fourteen Failures - Static Damage

Fourteen of the SCL 5999 devices failed due to shorted capacitors; seven after temperature cycling, seven after stabilization bake, and none in burn-in. The failure analysis revealed damage from static discharge. Being a test cell, this device has no provision for input protection.

3.4 CONCLUSIONS AND ALTERNATE SCREENING PLAN

3.4.1 Conclusions

- o 100 cycles of -65°C to +200°C temperature cycling is the most effective screen for both package and assembly defects. Ten cycles was proven to be ineffective in detecting the lifted post bond problem which was encountered. This test should be included in the Final Verification Screening.
- o Burn-in - Comparing the dynamic burn-in with the power burn-in showed no significant difference in test results. No failures occurred on the pattern generator burn-in. Burn-in followed by temperature cycling was less effective than extended temperature cycling. 336 hours of burn-in should be evaluated in the Final Verification Test.
- o Visually undetectable metallization defects such as opens over oxide steps must be controlled by a process control, such as SEM and should be included in the Final Verification Screen.
- o Stabilization Bake was not effective as a screen. This is a very low cost test to perform and should be included in the Final Verification test plan for further evaluation.
- o Extended Electrical Measurements were not determined to be of value in screening out visual defects.

- Original Die Visual Defects were not easily detected in any of the alternate screening tests. In addition, a large percentage of these potentially defective devices reliably operated throughout the life test, indicating that die defects surviving screening are not necessarily latent defects.

3.4.2 Alternate Screening Plan

The following tests are recommended for the Final Verification Alternate Screening Plan.

- Process wafers to Specification 131252.
- Perform SEM.
- Perform mechanical screens per MIL-STD-883, Method 5004, Class B.
- Stabilization Bake, reference Paragraph 3.1.2.
- Change Temperature Cycling to 100 cycles, -65°C to +200°C. Reference Paragraph 3.1.2, Test Condition 1.
- Change Burn-in to 336 hours. Reference Paragraph 3.1.2, Test Condition 2.
- Evaluate the alternate screening results with a 1000 hour life test. Reference Paragraph 3.1.2, Test Condition 2.

SECTION 4

4.0 FINAL VERIFICATION TEST

The purpose of the Final Verification Test was 1) to verify that the control of wafer processing by means of Specification 131252 developed in Paragraph 2.0, and the alternate screening methods developed in Paragraph 3.0, is a viable and effective means to insure die integrity of LSI devices and; 2) to compare the results with those obtained with devices screened using existing MIL-STD-883, Level B criteria.

This Final Verification Test as shown in Figure 4.0-1 was performed on both bipolar and CMOS devices by selecting 125 die of each technology from wafers processed to Specification 131252 and screened to the alternate screening methods of Paragraph 3.0. The results of these sampies were compared with 125 die of each technology processes in the same time frame to existing MIL-STD-883, Level B criteria.

4.1 FINAL VERIFICATION SAMPLE SELECTION

Two large, complex circuits were selected to represent the bipolar and CMOS process techniques. These devices are described in the following paragraphs.

4.1.1 Bipolar Device Description

The bipolar device selected was a random access memory (RAM) with a chip size of 110 X 113 mils. Selection of this device was based on the fact that it was the largest chip size the manufacturer produced on his MIL-M-38510 certified production line. Refer to Table 4.1.1-1 for details. The memory organization, logic diagram, and pin assignments is given in Figure 4.1.1-1. The devices were produced on a production line which was certified to MIL-M-38510.

4.1.2 Metal Gate CMOS Device Description

The CMOS device selected was a four digit counter, latch, seven segment decoder and multiplex display driver. The output drivers are bipolar transistors. Chip size was 107 X 133 mils. This device was selected because it was the largest chip size

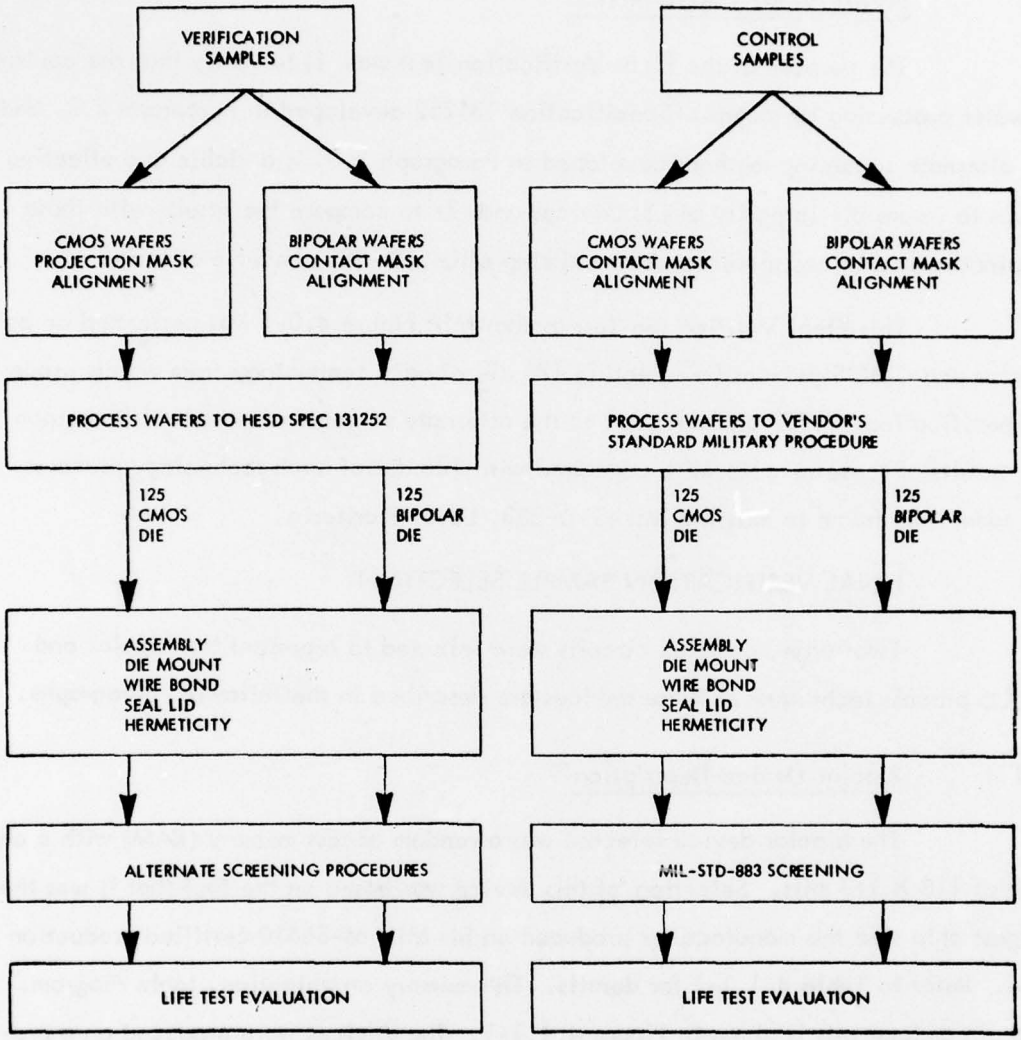


FIGURE 4.0-1 FLOW DIAGRAM OF FINAL VERIFICATION TEST PLAN

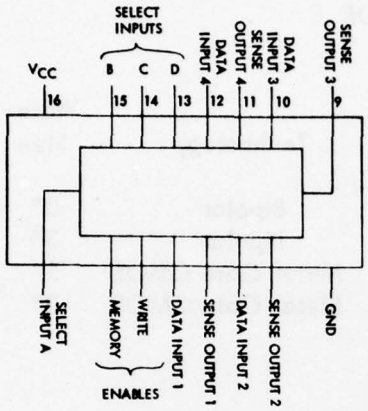
TABLE 4.1.1-1

WAFERS SELECTED FOR
FINAL VERIFICATION TEST

VENDOR E

Sample	Quantity	Processed	Technology	Wafer Size	Die Size in Mils
1	125	131252	Bipolar	3"	110 X 113
2	125	MIL-STD-883	Bipolar	3"	110 X 113
3	125	131252	Metal Gate CMOS	3"	107 X 133
4	125	MIL-STD-883	Metal Gate CMOS	3"	107 X 133

CONNECTION DIAGRAM



TRUTH TABLE

MEMORY ENABLE	WRITE ENABLE	OPERATION	OUTPUTS
0	0	WRITE	LOGICAL "1" STATE
0	1	READ	COMPLEMENT OF DATA STORED IN MEMORY
1	X	HOLD	LOGICAL "1" STATE

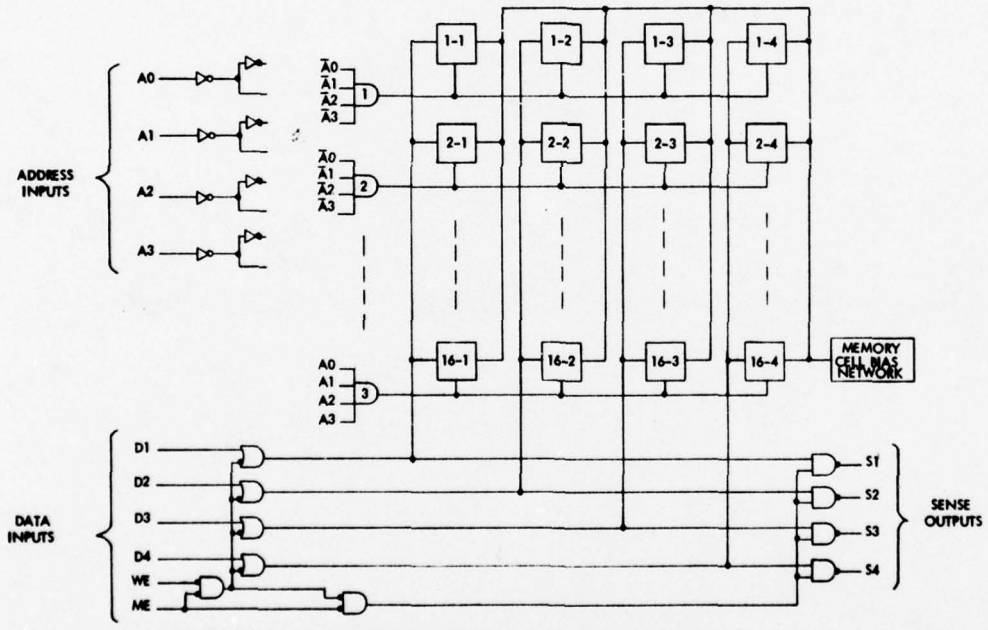


FIGURE 4.1.1-1 BIPOLAR DEVICE LOGIC DIAGRAM , 64 BIT READ/WRITE MEMORY

currently being run on the CMOS line exclusive of microprocessors and custom devices. Refer to Table 4.1.1-1 for details. The logic diagram and pinout for this device is given in Figure 4.1.2-1.

4.2 WAFER PROCESSING AND DIE PREPARATION

Both the bipolar and CMOS final verification test wafer processing and die preparation were subcontracted to Vendor E. Vendor E was selected in part on the basis of his willingness to implement Specification 131252 and his capability to process wafers in parallel to existing MIL-M-38510 process controls.

The selected wafers were processed by Vendor E to Specification 131252, with critical inspection points monitored by HESD. The control devices were processed in parallel to the vendor's existing controls as used to fabricate wafers for Military products.

4.2.1 Wafer Processing

4.2.1.1 Wafer Processing - Bipolar Study Samples

Two runs, one of 24 wafers, Lot 6915, and one of 23 wafers, Lot 6916, of the bipolar device were selected for the verification study test samples. The equipment used to process the bipolar devices was standard contact mask alignment equipment. (Cobilt 400 with vacuum clamping) The application of photoresist, curing and the developing was done as a single operation on an automated station, thereby limiting individual wafer handling to alignment and the required inspection steps.

Due to problems of production through-put times and disruption of the line, the inspection of the two verification test lots was started at the emitter photoresist step instead of at the first masking operation. This change ultimately resulted in the rejection of some wafers which were due to defects introduced in earlier stages of the process. These earlier process defects were still inspectable at the first inspection performed by HESD and therefore in no way impacted the results of this study.

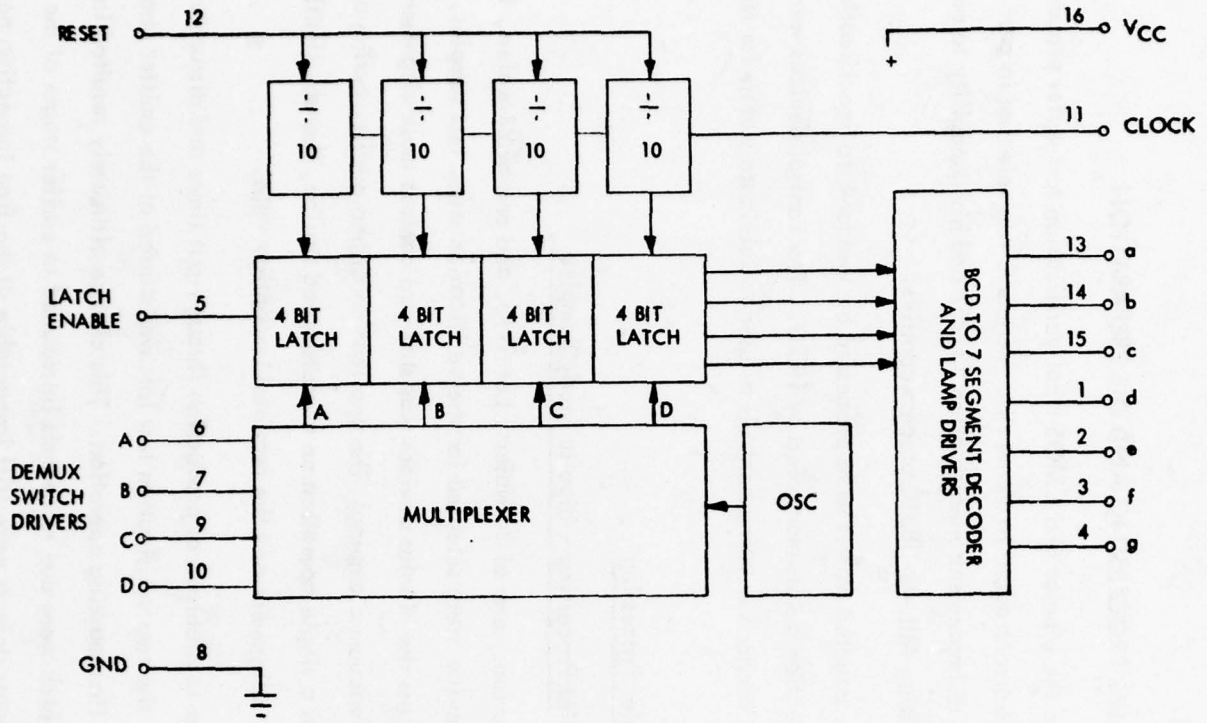


FIGURE 4.1.2-1 CMOS DEVICE LOGIC DIAGRAM - FOUR DIGIT COUNTER, LATCH, 7 SEGMENT DECODER, AND MULTIPLEX DRIVER

A review of the inspection data performed by the vendor showed only one defect was found, a pinhole; however, at that time the vendor did not consider anything which was damaged at any previous masking operation as defective.

HESD's first source inspection was performed on the contact aperture mask, at post development and post oxide etch. The first wafers inspected were the first off samples for the mask acceptance criteria of Paragraph 2.2.1 of Specification 131252. As a result of the first off wafer inspection, all wafers of Lot 6916 were rejected for misalignments of the base mask and tears in the isolation diffusion. These defects were all from previous photoresist steps and should have been removed or reworked at the second photoresist operation. This run was discontinued as part of the study. Refer to Table 4.2.1.1-1 for a summary of results.

The second lot, Number 6915, had 17 acceptable wafers for the study after completion of the source inspection. A summary of the inspection results are shown in Table 4.2.1.1-2.

After etching the contacts, a sample of six circuits were inspected on each of eight wafers. No defective circuits were found. See data summary in Table 4.2.1.1-2.

HESD source inspection was performed on the metallization mask at post development and at post etch. The inspection results from the post development metallization inspection are summarized in Table 4.2.1.1-2. At this inspection only one defective wafer was found.

After metal etching a sample of ten circuits on each wafer was inspected. One wafer was removed from the lot for epitaxial spikes. The remaining fifteen wafers were accepted.

The following observations were made during the bipolar wafer source inspection.

TABLE 4.2.1.1-1

WAFER PROCESS INSPECTION RESULTS

BIPOLAR DEVICE LOT 6916

	Rework	In	Out	Reject
Emitter Mask (Mask accepted)				
First Off Wafer Inspection		23	0*	23

* Entire wafer lot rejected due to base mask misalignment and tears in isolation diffusion.

TABLE 4.2.1.1-2

BIPOLAR WAFER PROCESS INSPECTION RESULTS

BIPOLAR DEVICE LOT 6915

	Rework	In	Out	Reject
Emitter Mask (Mask Accepted)				
Post Development		24	24	
Post Etch		24	24	
Contact Aperature Mask (Mask Accepted)				
Post Development	7(1)	24	12	5 (2)
Post Development Rework		7	5	2 (3)
Post Etch		17	17	
Metal Mask (Mask Accepted)				
Post Development		17	16	1 (4)
Post Etch		16	15	1 (5)
Total Accepted Wafers through Wafer Fabrication:			15	

(1) Six rejected at rough wafer inspection, one rejected at alignment inspection.

(2) Two rejected for defects in prior steps; three rejected for epitaxial spikes.

(3) Two rejected for mask misalignment.

(4) One rejected for metal bubble.

(5) One rejected for epitaxial spike.

a. Mask runout on the second base mask caused the three or four outside circuits to be misaligned on most of the rejected wafers. The vendor was using two different mask lots. One of the lots had excessive runout and seems to be the cause of the alignment problem. With a closer control of the incoming masks for runout, the alignment criteria could have been met on all wafers.

b. Of the 14 wafers rejected during the post development inspection from Lot 6915, six were found by the rough inspection simply by placing the wafer under a microscope illuminator. An additional three rejected wafers were caused by epitaxial spikes in the starting material.

c. During the detailed inspection, it was difficult to determine the defect categories into which the defective circuits should be assigned, since void, epitaxial spikes, and contamination all look similar.

d. Early rejection of wafers, documentation of defect causes, and identification of these problems will, in itself, effect a pressure to correct the causes of the defects and thereby improve the wafer quality.

e. Early elimination of batch related defects greatly reduces the defects surviving through the process to wafer completion as most of these defects originate in wafers with a high defect count. In this case, a small number of wafers in a lot with epitaxial spikes can cause a large number of repeating defects as the lot moves through the photo-resist steps. Therefore, removal of wafers with epitaxial spikes prior to the isolation masking operation would improve the visual yield.

f. The visual inspection criteria for wafer fabrication, as set up by HESD Specification 131252, can be met once the incoming masks are controlled and the wafers with epitaxial spikes are removed.

g. To be effective, a visual inspection during wafer fabrication requires source inspection.

Table 4.2.1.1-3 is a comparison of the verification study wafer inspection versus the vendor's standard inspection as observed during source inspection. The significance of this comparison is that the vendor's acknowledged criteria is very close to being sufficient, the primary additional requirement being that the inspection be well controlled with reject provisions clearly called out and enforced.

Upon completion of the metallization process, wafer run number 6915 was submitted to SEM inspection per Specification S-311-P-12A and was accepted.

The vendor performed electrical probe on this lot to his standard electrical probe and his standard electrical test criteria for this device. The probe yield was 38%.

4.2.1.2 Wafer Processing - Bipolar Control Samples

In parallel with the study sample of bipolar devices, a control sample lot of the same device type was run on the same certified MIL-M-38510 production line as the study wafers. The procedures and visual inspection normally used by the vendor for MIL-M-38510 candidate wafers was employed for this lot.

The vendor performed electrical probe on this lot to his standard electrical test criteria for this device. The probe yield was not provided on this lot, but the vendor indicated that his average yields on this device type are 22%.

4.2.1.3 Wafer Processing - CMOS Study Sample

One lot of 15 wafers was run on the CMOS device selected. This run, identified as CRE 195, was processed to Wafer Inspection for RADC Verification Test Vehicles, HESD Specification 131252.

The wafers were fabricated on a well controlled production line. The mask alignment equipment used was a Perkin-Elmer Micralign projection mask alignment system.

TABLE 4.2.1.1-3

COMPARISON OF VENDOR'S STANDARD WAFER INSPECTION CRITERIA TO THE VERIFICATION STUDY CRITERIA

	VENDOR'S INSPECTION	VERIFICATION STUDY INSPECTION
a.	Mask Acceptance Inspection	
	None performed One mask used for each wafer run (12-24 wafers)	Detail first inspection of first wafer aligned to assure acceptable masks. One mask used on every 5 wafers.
b.	Rough Wafer Inspection	
	The vendor's specification is very similar to study requirements.	Scratch criteria Slightly tighter
c.	Alignment Inspection	
	No separate alignment inspection.	Separate inspection of four worst case location circuits.
d.	Detail Wafer Inspection	
	Operator only scans wafer in 3 or 4 points and does not look at any whole circuits. No counting of defects is done.	Detail inspection of whole circuits with count of defective circuits.
e.	Post Etch Inspection	
	100% inspection of wafer.	Sample wafer inspection except after metal etch.

The application of photoresist, curing and developing was done as a single operation on an automated station, thereby limiting individual wafer handling to alignment and the required inspection steps. The use of the projection mask projection system eliminated mask to wafer contact.

The vendor reduced HESD Specification 131252 to a detailed working data sheet which provides both instructions to the operator and a process results log. A sample of this data sheet is reproduced as Figure 4.2.1.3-1.

HESD performed source inspection at the contact aperature etch step prior to metallization. Vendor inspection steps were performed for mask acceptance and for wafer acceptance at each mask step. Refer to Table 4.2.1.3-1 for a summary of results.

Comments on the results of the CMOS wafer processing are listed below:

a. Primary cause of the rejects was bridging metal which was a lot processing problem. This problem was detected as a marginal reject criteria on 8 wafers and was probably due to under-etch on those wafers. Accepted wafers showed no sign of the problem. Without the wafer control criteria, an assumed 20% to 30% of the resulting die would be visual rejects.

b. The foreign material embedded in the oxide and broken wafer were the result of handling problems. These problems can be expected in normal processing, but improvement in handling procedures may result if the problems are identified.

Upon completion of the metallization, the CMOS wafer lot number CRE 195 was subjected to SEM inspection per Specification S-311-P-12A and was accepted. Refer to Appendix D for detail SEM reports.

The vendor performed electrical probe on this lot to his standard electrical test criteria for this device. The probe yield was approximately 53%.

Post Development Inspection

Device _____

Mask _____

A. First Wafer Inspection - Inspect first aligned and exposed wafer.

1. Damaged photoresist inspection at 100X or greater.

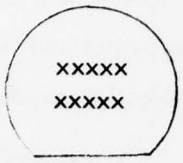
Inspect locations shown (10) for:

a. Scratches

b. Lifting

c. Pinholes

d. Voids



# of circuits failing = _____

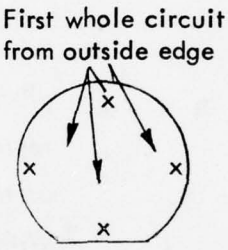
Reject mask for two or more failures.

2. Alignment Inspection 150X or greater

Inspect alignment keys in four locations shown for proper alignment.

# of sites rejected = _____

Reject mask if one or more sites are rejected.



B. All Wafers

1. Rough inspection - under U. V. Illuminator.

Reject wafers with any of the following defects:

a. No photoresist

b. double image

c. Partial coverage (pattern not covering to within 1/8" of edge)

d. Voids (Rips or tears covering more than one circuit)

VENDOR E SAMPLE DATA SHEET FOR WAFER PROCESSING
FIGURE 4.2.1.3-1

e. Lifting photoresist

f. Irregularities in photoresist (such as cloudiness, smudges, crushed resist, strain on surface, drops of resist, uneven coverage)

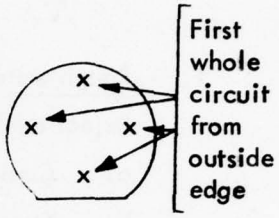
# of wafers passing = _____; # of wafers failing = _____

2. Alignment Inspection

Inspect keys in locations shown for proper alignment.

# of sites rejected = _____

Reject wafer if one or more sites are rejected.

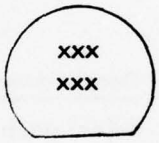


3. Detailed wafer inspection - inspect at 100X or greater.

# of wafers in Lot = _____

# of circuits/wafer to inspect = _____

Location of inspected circuits



Causes for rejection:

a. Over exposed patterns

b. Under exposed patterns

c. Under developed patterns

d. Spiking in photoresist

e. Poorly developed patterns

f. Damaged photoresist (scratches, lifting, pinholes, voids)

Wafer #	1	2	3	4	5	6	7	8	9	10	11	
# of Reject Ckts												Total Lot Rejects= _____
Wafer #	12	13	14	15	16	17	18	19	20			
# of Reject Ckts												

Reject wafer if reject ckts = _____ or more

Reject Lot if rejects (including rejected wafers) = _____ or more.

Operator _____ Date _____

FIGURE 4.2.1.3-1 continued

Post Oxide Etch Inspection

Device _____

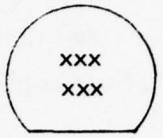
Mask _____

Lot Size = _____ wafers

Inspection sample size = _____ wafers

# of circuits per wafer to inspect = _____

Total # of circuits to inspect = _____



1. Rough wafer inspection - under ultraviolet illuminator.

   Reject each wafer for the following on any part of the wafer:

   a. Contamination

   b. Streaks and clouds

   c. Oxide in openings

   # of rejected wafers = _____

   * If any wafer is rejected perform this inspection on all wafers in lot.

2. Detailed wafer inspection - inspect at 100X or greater.

   Reject each circuit in inspection sample for:

   a. Contamination

   b. Oxide in openings

   c. Over-etching

   d. Pinholes

   e. Oxide faults

Wafer #	1	2	3	4	5	6
# of reject ckts						

Total Reject Circuits

_____

Reject Lot if total of reject circuits is _____ or more.

Operator _____ Date _____

FIGURE 4.2.1.3-1 continued

Post Metal Etch Inspection

Inspect every wafer in lot.

1. Rough wafer inspection - under dark field illuminator.

   Reject wafer for:

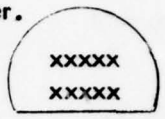
   a. Unremoved photoresist

   b. Foreign material on wafer

   # of reject wafers = _____

2. Detailed wafer inspection - inspect at 150X or greater.

   Inspect 10 circuits on every wafer in locations shown.



   Reject circuits exhibiting:

   a. Metallization scratches

   b. Metallization voids

   c. Metallization corrosion

   d. Metallization adherence

   e. Metallization bridging

   f. Metallization alignment

   g. Foreign material

Wafer #	1	2	3	4	5	6	7	8	9	10
# of Reject Cks										
Wafer #	11	12	13	14	15	16	17	18	19	20
# of Reject Ckts										

Reject wafers having _____ or more reject circuits.

Operator _____ Date _____

FIGURE 4.2.1.3-1 continued

TABLE 4.2.1.3-1

WAFER PROCESS INSPECTION RESULTS

CMOS DEVICE LOT CRE 195

		Rework	In	Out	Reject
P -Well MASK 1	(Accepted)				
Post Development		-	15	15	-
Post Etch		-	15	14	1
P +Well MASK 2	(Accepted)				
Post Development		-	14	14	-
Post Etch		-	14	14	-
N+ MASK 3	(Accepted)				
Post Development		-	14	14	-
Post Etch		-	14	14	-
Oxide MASK 4	(Accepted)				
Post Development		-	14	14	-
Post Etch		-	14	14	-
Contact Aperature MASK 5	(Accepted)				
Post Development		-	14	11	3 (1)
Post Etch					
Metal MASK 6	(Accepted)				
Post Development		-	11	11	-
Post Etch		-	11	3	8 (2)
Glassivation MASK 7	(Accepted)				
Post Development		-	3	2	1 (3)
Post Etch		-	2	2	

NOTES

(1) Three wafers rejected due to foreign matter embedded in oxide.
(2) Eight wafers were rejected with exactly three circuits rejected on each wafer for bridging metal. Reject criteria is reject on three of 10 circuits inspected. Accepted circuits had 0 rejects.
(3) One wafer broken.

4.2.1.4 Wafer Processing - CMOS Control Sample

In parallel with the study sample of CMOS devices, a control sample lot of the same device type was run on the MIL-M-38510 certified production line, using standard contact mask alignment equipment. The procedures and visual inspection normally used by the vendor for MIL-M-38510 candidate wafers was employed for this lot.

The vendor performed electrical probe on this lot to his standard electrical test criteria for this device. The probe yield was approximately 43%.

4.2.2 Dice Inspection

4.2.2.1 Dice Inspection - Bipolar Study Samples

The dice from the accepted wafers were subjected to a 100% visual inspection. The vendor performed both a high power magnification and a low power magnification inspection to MIL-STD-883, Method 2010.2, Test Condition B. The specification, 131252, requires only the low power inspection. As a result of this inspection, the vendor removed 41 pieces. These 41 vendor removals were subsequently replaced in the lot to maintain the data validity and therefore the inspection lot consisted of 125 pieces plus the 41 pieces for a total of 166 pieces. This inadvertant error did allow these marginal devices to be identified separately such that the results of screening could be evaluated.

All 166 devices were inspected by HESD to the low magnification die inspection requirements of 131252. During this inspection four devices were rejected, two from the 41 pieces for cracked chips and two from the 125 piece sample, one for bridging metal, and one for foreign material. (See Table 4.2.2.1-1) An additional high magnification inspection was done on all with the results shown in Table 4.2.2.1-2. These results indicate that although the 41 devices were rejected by the vendor as not meeting MIL-STD-883, Method 2010.2, Test Condition B, six were good, and 14 were marginally acceptable. Sixteen had foreign material in the form of ink splatter.

TABLE 4.2.2.1-1

VISUAL INSPECTION RESULTS OF BIPOLAR STUDY SAMPLES

(LOW POWER)

Low Power Visual Inspection to HESD Specification 131252

		125 Piece Sample	Vendor Removals
Die Received		125	41
Reject Cause:	Cracked chip		2
	Bridged Metal	1	
	Foreign Material	1	
	Removed from lot	2	2
Sent to assembly		123	39

TABLE 4.2.2.1-2

VISUAL INSPECTION RESULTS OF BIPOLAR STUDY SAMPLES
(HIGH POWER)

125 piece sample - no defects found to MIL-STD-883, Method 2010.2, Test Condition B High Power Inspection

Results of high power inspection of vendor removals:

Criteria	Results	MIL-STD-883 Method 2010.2 Test Condition B Results	Qty
Ink Splatters (foreign material)	Visually acceptable	Acceptable	16
Glassivation	Two adjacent metallization paths not covered	Rejectable	3
Bridging Metal	$\geq$ 50% and $\leq$ 0.1 mil	Marginally Acceptable	5
Voided Metal	$\geq$ 25% and $\leq$ 50%	Marginally Acceptable	2
Cracked Chips	Not in active area	Marginally Acceptable	7
Visually Good			6
			39

4.2.2.2 Dice Inspection - Bipolar Control Samples

The dice from the bipolar control sample wafers were subjected to a 100% visual inspection to MIL-STD-883, Method 2010.2, Test Condition B. From this group, 125 die were received. For comparison, these die were subjected to both a high magnification and a low power magnification inspection at HESD. The results of this inspection are shown in Table 4.2.2.2-1.

4.2.2.3 Dice Inspection - CMOS Study Samples

The vendor performed a 100% low power inspection on the CMOS lot per HESD Specification 131252. A summary of the results is given below:

Accepted Die from one Wafer			229
Reject cause:	Cracked chip	5	
	Scribe defects	7	
	Metallization coverage	6	
	Total Rejects	18	
Accepted die to low power			211
Quantity shipped			125

The above rejects are primarily due to the scribe and break operation and represent an 8% defect rate. From this group, 125 good die were submitted to HESD and a visual inspection was performed. These results are given in Table 4.2.2.3-1.

4.2.2.4 Dice Inspection, CMOS Control Sample

The dice from the CMOS control sample wafers were subjected to a 100% visual inspection to MIL-STD-883, Method 2010.2, Test Condition B. From this group, 125 die were received. For comparison, these die were subjected to both a high power magnification and a low power magnification inspection at HESD. The results of this inspection are shown in Table 4.2.2.4-1.

TABLE 4.2.2.2-1

VISUAL INSPECTION RESULTS OF BIPOLAR CONTROL SAMPLE

Die received		125
Low Power Visual (30X)		
Reject cause: Foreign material	3	
High Power Visual (175X)		
Reject cause: Photoresist	2	
Glassivation	2	
Diffusion	3	
Metallization void	4	
Total Defects	14	
Sent to Assembly		125

TABLE 4.2.2.3-1

VISUAL INSPECTION RESULTS OF CMOS DIE STUDY SAMPLES

Quantity Received		125
Low Power Inspection		
Rejected	0	
High Power Inspection		
Glassivation Defects	6	
Metal Voids	1	
Diffusion Flaw	1	
	8	
Accepted		125
Sent to Assembly		125

TABLE 4.2.2.4-1

VISUAL INSPECTION RESULTS OF CMOS CONTROL SAMPLE

Quantity Received		125
Low Power Inspection		
Rejected	0	
High Power Inspection		
Metal void	1	
Cracked chip	2	
Diffusion flaw	1	
	4	
Accepted		125
Sent to Assembly		125

4.2.3 Analysis of Wafer Processing and Dice Inspection

The most significant factors derived from the Final Verification Test are shown in the yields given in Table 4.2.3-1. Review of this chart shows that the study lots had measurably higher electrical probe yields than the control lots with equivalent die visual inspection yields.

In addition to the yield improvements, a number of specific observations were made.

- Some wafer defects were identified which could be reworked. If processing had continued rework may not have been possible.
- Epitaxial spikes on a few bipolar wafers caused damage to the masks, thereby propagating the effects. Early removal of these wafers significantly improved yields.
- A mask runout problem was found rejecting one wafer and the mask rather than the entire lot.
- The vendor is generally not being asked to tighten his inspection criteria, only change the sampling plans and control points. Reference Table 4.2.1.1-3.
- The wafer inspection procedure improved visual yields by rejecting wafers with 20% to 30% rejectable die to the bridged metal criteria.

4.2.4 Conclusions from Wafer Processing and Die Inspection

- Wafer process controls revealled process problems, affecting visual yields, that can be easily corrected.
- The wafer inspection control procedures consistently produced significantly higher electrical probe yields.

TABLE 4.2.3-1

ANALYSIS OF INSPECTION RESULTS

ELECTRICAL PROBE

	Bipolar Study Lot	Bipolar Control Lot	CMOS Study Lot	CMOS Control Lot
Yield	38%	22%	53%	43%

DICE INSPECTION

Inspection Flow	Bipolar Study Lot	Bipolar Control Lot	CMOS Study Lot	CMOS Control Lot
Vendor Low Power Inspection	Performed	Performed	Performed	Performed
Vendor High Power Inspection	N/A	Performed	N/A	Performed
HESD Low Power Inspection % Defective	2.4% *	2.4%	0	0
HESD High Power Inspection % Defective	1.8%	11%	6.4%	3.2%

* Rejects from high power inspection counted as being in lot for analysis.

- Die fabricated with wafer processed controls obtain the same visual quality without high magnification inspection as those produced with MIL-STD-883 visual inspection imposed.
- For wafer process controls to be effective source inspection must be imposed at the last oxide etch inspection and at the wafer metallization inspection.

4.3 ASSEMBLY AND SCREENING

The four groups of final verification test vehicles were assembled using standard production procedures. The two study sample groups were then screened to the alternate screening procedure developed in Section 3.0. The two control sample groups were screened in parallel to the present MIL-STD-883 techniques. The results of both groups were then compared and analyzed.

4.3.1 Assembly

The four groups of final verification test vehicles were packaged in a 16-lead dual-in-line (DIP) package (see Figure 4.3.1-1) and assembled on the same assembly line to minimize variations which could affect the study results. Die mount was by eutectic bonding. Leads were ultrasonically bonded with 1.25 mil aluminum wire. The packages were braze sealed at +300°C under vacuum.

A summary of the quantities in and out of each assembly operation is given for each lot in Tables 4.3.1-1 and 4.3.1-2.

4.3.2 Screening Tests

The final verification test samples were subjected to the screening sequence derived in the Preliminary Verification Test. Details of this modified screening test are given in Paragraphs 3.1 and 3.4.2. The control samples were subjected to the screening procedure of MIL-STD-883, Method 5004, Class B. The results of the screening tests are shown in Tables 4.3.2-1 and 4.3.2-2 and discussed in the following paragraphs.

4.3.2.1 Mechanical Screening Tests

In performance of both the study sample screening (modified MIL-STD-883 screen) and the control sample screening (MIL-STD-883, Class B) the constant acceleration and hermetic seal tests were more readily accomplished in the device packaging and assembly area (Vendor A) rather than in the screening test area (HESD). Tables 4.3.2-1 and 4.3.2-2 summarize the results of these tests.

TABLE 4.3.1-1

BIPOLAR DEVICE

ASSEMBLY DATA SUMMARY

	Study Sample (1)				Control Sample	
	125 Study Samples		41 Vendor Removals			
Operation	Qty In	Qty Out	Qty In	Qty Out	Qty In	Qty Out
Die Mount	123	103	39	35	125	120
Lead Bond	103	103	35	35	120	120
Preseal Inspection	103	100	35	29	120	109
Preseal Bake	100	100	29	29	109	109
Seal	100	100	29	29	109	109

(1) 162 devices; 123 devices from the vendor's initial shipment plus 39 devices initially from the lot. See Paragraph 4.2.2.1.

TABLE 4.3.1-2

CMOS DEVICE

ASSEMBLY DATA SUMMARY

Operation	Study Sample		Control Sample	
	Qty In	Qty Out	Qty In	Qty Out
Die Mount	125	125	125	122
Lead Bond	125	122	122	120
Preseal Inspection	122	118	120	115
Preseal Bake	118	118	115	115
Seal	118	118	115	115

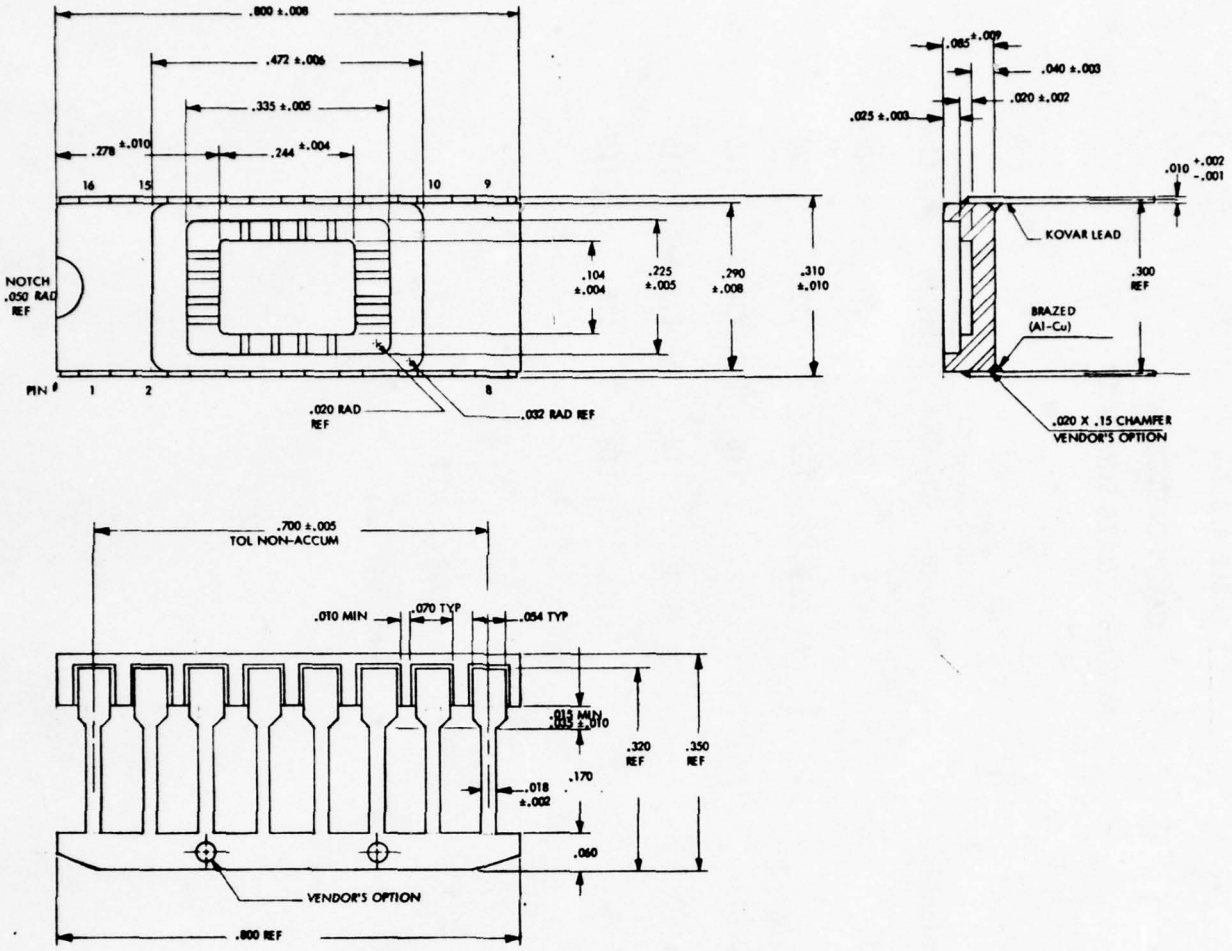


FIGURE 4.3.1-1 16 PIN PACKAGED USED FOR FINAL VERIFICATION TEST SAMPLES

TABLE 4.3.2-1

SCREENING RESULTS SUMMARY

BIPOLAR DEVICES

Operation	Study Samples: 125 Piece Sample Qty In	Study Samples: 125 Piece Sample Qty Out	Study Samples: 41 Piece Vendor Removals Qty In	Study Samples: 41 Piece Vendor Removals Qty Out	Control Samples Qty In	Control Samples Qty Out
Preseal Inspection	103	100	35	29	120	109
Centrifuge	100	100	29	29	109	109
Fine Leak	100	99	29	29	109	109
Gross Leak	99	99	29	28	109	105
Load in Carriers	99	99	28	28	105	105
Initial Electrical	99	73	28	23	105	64
Stabilization Bake	73	73	23	23	64	64
Electrical End Points	73	73	23	23	64	64
Temp Cycle, 10 cycles	73	73	23	23	64	64
Electrical End Points	73	71	23	23	64	63
Temp Cycle, 50 cycles	71	71	23	23	N/A	N/A
Electrical End Points	71	60	23	23	N/A	N/A
Temp Cycle, 100 cycles	60	60	23	23	N/A	N/A
Electrical End Points	60	54	23	23	N/A	N/A
Burn-in, 168 hr	54	54	23	23	63	63
Electrical End Points	54	52	23	23	63	63
Burn-in, 336 hr	52	52	23	23	N/A	N/A
Electrical End Points	52	44	23	23	N/A	N/A
Accepted Quantity	---	44	---	23	---	63

TABLE 4.3.2-2

SCREENING RESULTS SUMMARY

CMOS DEVICES

Operation	Study Sample Qty In	Study Sample Qty Out	Control Samples Qty In	Control Samples Qty Out
Preseal Inspection	118	118	120	115
Centrifuge	118	118	115	115
Fine Leak	118	113	115	112
Gross Leak	113	105	112	106
Load in Carriers	105	103	106	105
Initial Electrical	103	89	105	92
Stabilization Bake	89	89	92	92
Electrical End Points	89	89	92	92
Temperature Cycle, 10 cycles	89	87	92	92
Electrical End Points	87	87	N/A	N/A
Temperature Cycle, 50 cycles	87	84	N/A	N/A
Electrical End Points	84	84	N/A	N/A
Temperature Cycle, 100 cycles	84	84	N/A	N/A
Electrical End Points	84	82	N/A	N/A
Burn-in, 168 hr	82	82	90	90
Electrical End Points	82	82	90	90
Burn-in, 336 hr	78	78	N/A	N/A
Electrical End Points	78	76	N/A	N/A
Accepted Quantity	---	76	---	90

4.3.2.2 Electrical Screening Tests

Test programs were prepared for both the bipolar device and the CMOS device to utilize automatic test equipment. Emphasis was placed on providing a thorough functional and parametric test to detect failures. No attempt was made to characterize the devices over temperature limits as such data was not pertinent to the control of visual criteria. Table 4.3.2.2-1 gives a summary of the electrical tests for the bipolar devices. Table 4.3.2.2-2 gives a similar summary for the CMOS devices.

The initial electrical defects for both device types fell between 12% and 39% (see Table 4.3.2-1 and 4.3.2-2). Failure analysis of these parts indicates the primary cause of failure to be tool marks on the metallization surface and open post bonds. On the bipolar control samples, 26 failures occurred due to low breakdown voltage on output pins. No similar electrical failures occurred on the study samples.

4.3.2.3 Environmental Screening Tests

The environmental screening consisted of high temperature stabilization bake, temperature cycling and burn-in as defined in Paragraph 3.1. Electrical measurements were made between each screening test. Refer to Table 4.3.2-1 and 4.3.2-2 for the test sequence and results.

TABLE 4.3.2.2-1

ELECTRICAL TEST DESCRIPTION

FOR BIPOLAR FINAL VERIFICATION TEST SAMPLES

Test No.	Test Description
01	I_{DD} Static, $V_{DD} = 5.0V$, $I_{DD} \leq 20mA$
02	Functional test checkerboard pattern of "1"'s and "0"'s written into memory and readout verified. The test is then repeated with the complement of the first checkerboard. Each output threshold voltage is checked. $V_{OL} \leq 0.4V$ at $I_{OL} = 3.6mA$, $I_{OH} \leq 50\ \mu A$ at $V_{OH} = 5.5V$.
05	Input clamp (-V) to input - check for clamp diode action $\leq 1.5V$.
07	Current at maximum input voltage $V_{IN} = 5.5V$, $I_{IN} \leq 100\ \mu A$
08	High Level Input Leakage $V_{IN} = 5.0V$, $I_{IN} \leq 1\ \mu A$
09	Low Level Input Leakage $V_{IN} = 0V$, $I_{IN} \leq 0.18\ mA$
12	I_{DD} Static, $V_{DD} = 5.0V$, $I_{DD} \leq 20\ mA$
17	Functional - same as Test 02 to verify active device

TABLE 4.3.2.2-2

ELECTRICAL TEST DESCRIPTION FOR

CMOS FINAL VERIFICATION TEST SAMPLES

Test No.	Test Description
01	Static $I_{DD} \leq 1$ mA, V_{CC} = 5V, inputs low
02	Static $I_{DD} \leq 1$ mA, V_{CC} = 5V, inputs high
03 thru 08	Input leakage, clock, latch, and reset, at 0 and +15V ≤ 1 µA
10 thru 16	Functional Tests at V_{CC} = +5V 1. Clock, latch sequence to count of 1111 (decimal) verify 7 segment output. 2. Clock to 7777 (decimal) latch - verify 3. Clock to 2222 (decimal) latch - verify 4. Clock to 5555 (decimal) latch - verify 5. Reset - latch - verify 0000 6. Clock to 9999 (decimal) - latch - verify 7. Clock to 8888 (decimal) - latch - verify Functional verification consists of verifying the 7 segment display driver outputs with specified source or sink current loads applied as applicable for each of the applied counts.
25 thru 31	Output current on display drivers, V_{OL} V_{CC} = +5V, Drivers = +5V, current limited to 10 µA $V_{OL} \leq 0.5$V
32 thru 39	Output current on digit switch drivers, I_{OH} and V_{OL} V_{CC} = +5V, $V_{OL} \leq 1.$ volts, $I_{OH} \geq 1$ mA

- Stabilization Bake

  Stabilization bake caused no failures in the screening tests.

- Temperature Cycling

  The study samples were subjected to a total of 100 temperature cycles with electrical end points measured at 10, 50 and 100 cycles at the extended temperature (+200°C). The control samples were only tested to a total of 10 cycles.

  Temperature cycling caused two failures in each of three of the four sample groups at 10 cycles. By 100 cycles the study groups had accumulated a total of 26 failures. The control groups were not subjected to the additional temperature cycling. Analysis revealed all failures were lifted post bonds.

- Burn-in

  Burn-in on both the bipolar and CMOS devices was accomplished at their rated temperature, under load and with dynamic drive conditions applied. The burn-in circuits are described in Figures 4.3.2.3-1 and 4.3.2.3-2. Rated temperature for the bipolar devices is +125°C and for the CMOS devices is +85°C.

  The burn-in results continued to display failures on the study groups which had been subjected to 100 temperature cycles.

  A total of 13 lifted bond failures and one cracked chip was detected.

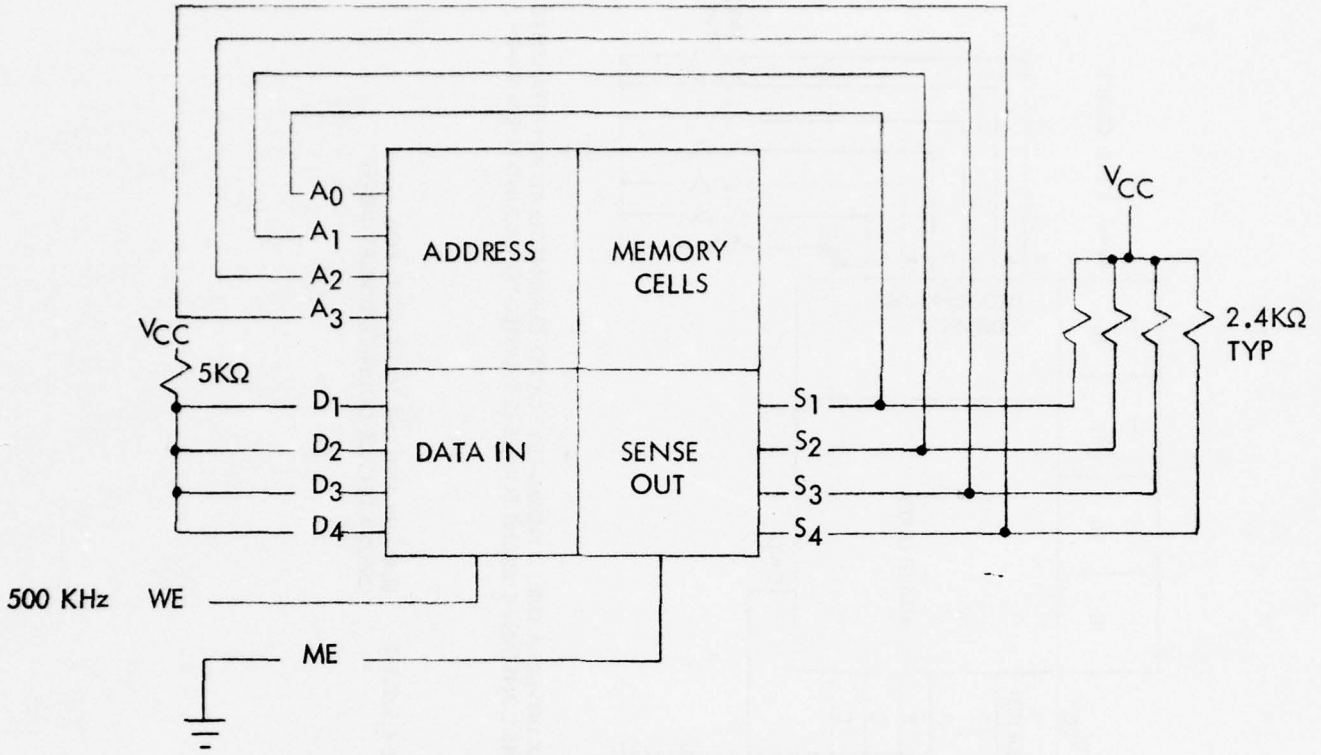
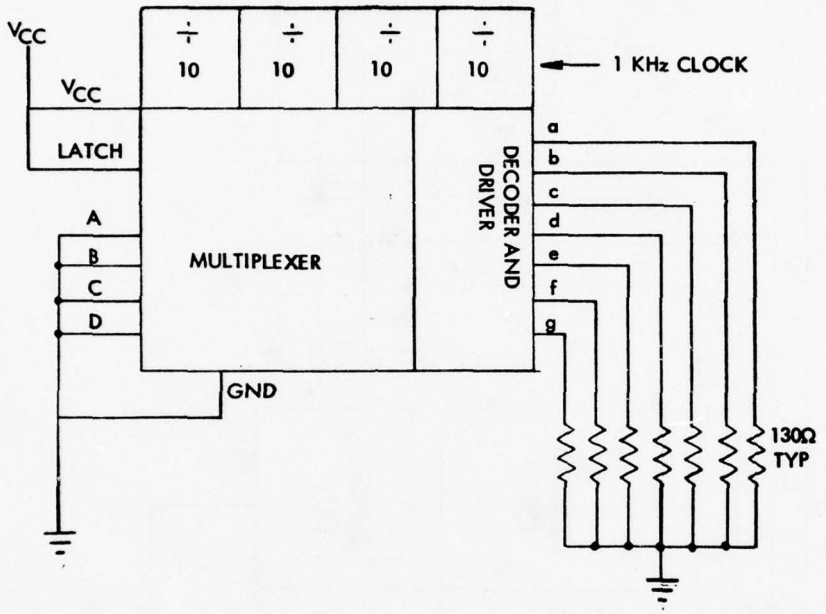


FIGURE 4.3.2.3-1 BURN-IN AND LIFE TEST CIRCUIT FOR BIPOLAR 64-BIT RAM



NOTE: MULTIPLEX DRIVERS A THRU D NORMALLY SOURCE CURRENT TO AN NPN TRANSISTOR BASE. THIS CONSTANT CURRENT SOURCE IS SHUNTED TO GROUND FOR BURN-IN.

FIGURE 4.3.2.3-2 BURN-IN AND LIFE TEST CIRCUIT FOR CMOS 4 DECADE COUNTER/DISPLAY DRIVER

4.3.3 Life Test

Following burn-in, samples from each of the groups were subjected to a life test of 1000 hours duration at rated temperature and dynamic test conditions. The life test circuit used was the same as that used for burn-in. Reference Figure 4.3.2.3-1 and 4.3.2.3-2. Measurements were made at one week intervals throughout the life test. Tables 4.3.3-1 and 4.3.3-2 provide a summary report.

Four failures occurred on the bipolar study sample group. All were analyzed and found to have lifted post bonds.

One failure occurred on the CMOS study sample due to a lifted post bond.

4.3.4 Analysis of Final Verification Test Results

The Final Verification Test was analyzed to determine whether the study met its objectives. The results of the Final Verification Tests are summarized by

1) screening test effectiveness
2) cause of the failure, and
3) comparison of the study samples to the control samples

Screening Test Effectiveness

Table 4.3.4-1 summarizes the Final Verification Test failures by screening test end points. From this table it is seen that

1) 100 temperature cycles are far more effective than 10 cycles, in detecting bond failures;
2) one cracked chip escaped the low power visual inspection and failed burn-in. This type of escape could occur at random in any lot.

Cause of Failure

The cause of each failure is further summarized in Table 4.3.4-2. This table depicts the severity of the lifted post bond problem and the lack of any other failures after initial electrical test except for the one cracked chip already discussed. (See Appendix E, Failure Analysis of Lifted Post Bond Failures, for further details).

TABLE 4.3.3-1

LIFE TEST RESULTS SUMMARY

BIPOLAR DEVICES

Hours at End Point	Study Samples				Control Samples	
	Qty	Failures	Qty	Failures	Qty	Failures
0	22	0	22	0	46	0
136	22	0	22	0	46	0
336	22	1	22	0	46	0
504	21	1	22	0	46	0
672	20	1	22	0	46	0
840	19	1	22	0	46	0
1000	18		22	0	46	0

TABLE 4.3.3-2

LIFE TEST RESULTS SUMMARY

CMOS DEVICES

Hours at End Point	Study Samples		Control Samples	
	Qty	Failures	Qty	Failures
0	45	0	45	0
168	45	0	45	0
336	45	0	45	0
504	45	0	45	0
672	45	1	45	0
840	44	0	45	0
1000	44	0	45	0

TABLE 4.3.4-1

SUMMARY OF FINAL VERIFICATION TEST FAILURES
BY TEST END POINT

(NON-ACCUMULATIVE TOTALS)

Test End Point	Bipolar Study Sample	Bipolar Control Sample	CMOS Study Sample	CMOS Control Sample
Initial Electrical	14 of 28 failures analyzed $10^{(1)}, 2^{(2)}, 2^{(3)}$	32 of 41 failures analyzed $3^{(2)}, 26^{(5)}, 2^{(3)}, 1^{(4)}$	5 of 12 failures analyzed $4^{(2)}, 1^{(1)}$	7 of 13 failures analyzed $3^{(2)}, 3^{(1)}, 1^{(3)}$
Initial Electrical Yield	76%	61%	86%	88%
10 cycles	$2^{(1)}$	$1^{(1)}$	$2^{(1)}$	0
50 cycles	$8^{(1)}$	N/A	$3^{(1)}$	N/A
100 cycles	$9^{(1)}$	N/A	$2^{(1)}$	N/A
168 hours burn-in	$1^{(4)}, 1^{(1)}$	0	$2^{(1)}$	0
336 hours burn-in	$8^{(1)}$	N/A	$2^{(1)}$	N/A
168 hours Life	0	0	0	0
336 hours Life	$1^{(1)}$	0	0	0
504 hours Life	$1^{(1)}$	0	0	0
672 hours Life	$1^{(1)}$	0	$1^{(1)}$	0
840 hours Life	$1^{(1)}$	0	0	0
1000 hours Life	0	0	0	0
Total Failures	61	42	24	13

NOTE Defect Cause
(1) - Lifted post bond.
(2) - Open or shorted metallization caused during assembly (tool scratch).
(3) - Cause of failure not determined.
(4) - Cracked chip.
(5) - Low breakdown voltage on output.

TABLE 4.3.4-2

SUMMARY OF FINAL VERIFICATION TEST FAILURES
BY FAILURE CAUSE

Failure Cause	Initial Electrical	Temperature Cycling	Burn-in	Life	Total
Lifted post bonds	14	27	13	5	59
Tool scratch	12	0	0	0	12
Not determined	5	0	0	0	5
Cracked chip	1	0	1	0	2
Low BV	26	0	0	0	26
Not analyzed	36	0	0	0	36
Total Failures	94	27	14	5	140

Comparison of the Study Samples to the Control Samples

At Initial Electrical Test, the lowest yield, 61% versus 76% on the study samples, was on the bipolar control samples, caused by 26 low breakdown electrical failures. This data indicates a difference in electrical yield related to process control.

The differences in temperature cycling failures between both groups of study and control samples points out the effect of temperature cycling on bond failures. A total of 26 failures occurred on the study samples versus one on the control samples.

Five additional bond failures were found during life test on the study samples, while only one failure occurred on the control sample life test.

No die defects related to visual quality other than the assembly/packaging workmanship problems were found in the Final Verification Test.

4.3.5 Screening and Life Test Conclusions

From the Final Verification Test screening and life tests, the following conclusions are evident.

- o The proposed wafer process control procedure has been proven effective using only a low magnification inspection.
- o Electrical yields were improved using the wafer process control procedures on the bipolar samples.
- o A control mechanism is needed for assembly/package related defects.
  a. lifted post bonds (10 cycles of T.C. is not sufficient)
  b. cracked chips
  c. assembly tool damage

SECTION 5

5.0 CONCLUSIONS AND RECOMMENDATIONS

The results of this study are summarized as:

- o Study conclusions
- o MIL-STD-883 recommendations
- o Recommendations for further study

5.1 STUDY CONCLUSIONS

This study has successfully demonstrated that an alternate method is feasible to replace the tedious, 100%, high magnification internal visual inspection. Specific action requires the addition of a wafer control procedure to MIL-STD-883 as an optional procedure with simultaneous deletion of high power 100% internal visual. Strengthening of the low power visual to detect cracked chips is also recommended to control assembly and packaging defects.

It has also been demonstrated that wire bond problems can escape the present 10 cycles of temperature cycling, and that 100 cycles with a percent defective allowable is more effective.

Changes to electrical test, stabilization bake and burn-in were investigated and were found to have little effect. No changes are recommended in these areas.

5.2 CHANGES RECOMMENDED TO MIL-STD-883

A new method as an optional replacement for Paragraph 3.1.1 of Method 5004, screening procedures, is recommended for use on complex microcircuits. Necessary changes to implement this recommendation are given in Figure 5.2-1 and Appendix F. Figure 5.2-1 describes the recommended changes to MIL-STD-883, Method 5005 and Appendix F describes the proposed Method 5XXX, Wafer Process Control and Preseal Visual.

1. Change Paragraph 3.1.1, Internal Visual, Method 5004.3, to the following:

Screen	Class A		Class B		Class C	
	Method	Reqmt	Method	Reqmt	Method	Reqmt
3.1.1 Internal Visual	2010, Test Condition A	100%	2010, Test Condition B	100%	2010, Test Condition B	100%
Option, see 3.3.1	5XXX	100%	5XXX	100%	5XXX	100%

2. Change Paragraph 3.1.3, Temperature Cycling, to the following:

Screen	Class A		Class B		Class C	
	Method	Reqmt	Method	Reqmt	Method	Reqmt
3.1.3 Temperature Cycling ①	1010, Test Condition D except 100 cycles 5% PDA	100%	1010, Test Condition D except 100 cycles 10% PDA	100%	1010 Test Condition D except 100 cycles	100%

3. Delete present Paragraph 3.3.1 and substitute the following:

3.3.1 Alternate Screens for Complex Microcircuits. For complex microcircuits, the procedure of Method 5XXX may be substituted for Paragraph 3.1.1, Internal Visual.

① Percent Defective Allowable (PDA) determined by percentage of shorts or opens from before to after temperature cycling. Additional tests and sequence of electrical testing is optional.

FIGURE 5.2-1 RECOMMENDED CHANGES TO MIL-STD-883, METHOD 5004

5.3 RECOMMENDATIONS FOR FURTHER STUDY

During the course of this study, several areas requiring further study have been identified. These areas are listed below:

- o A time/cost study should be performed to compare the implementation cost of the proposed wafer control process to the cost of 100% high magnification internal visual inspection. The crossover point versus circuit complexity where the proposed optional procedure becomes less expensive than 100% preseal inspection should be defined.
- o In order to prepare source inspection personnel for the additional technological areas involved in the recommended procedure, a "Source Inspector's Manual" should be prepared.
- o The recommended procedure should be implemented on a chosen group of parts from several vendors to provide a qualification of the procedure and generate definitive cost data.
- o A study is needed to define controls for packages and assembly operations including all incoming materials used.

APPENDIX A

VISUAL INSPECTION RESULTS
ON
CMOS DEVICES FROM VENDOR B

TABLE A-1

SUMMARY OF INSPECTION
OF CMOS DEVICES

Device Type	Run No.	No. of Wafers Inspected	No. of Die Inspected
8243	3	19	304
8243	2	5	72
8239	1	1	10
8239	2	5	50
8239	5	3	35
8240	2	10	130
		43	601

Wafer No.	Row Number 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Device Type	Run No.
1.	ceb cef cek	cek	cef cek	ceh	ceh cek	cek ceb	ceb	cef	ceb	OK	OK	ceb	OK	OK	OK	caf cef	8243	3
2.	OK	ceh ceb cef	cef	OK	caf cef	OK	ceb	cef	cek	cek	cef	OK	cef	OK	ceb	cek	8243	3
3.	caf cef ceb	cef ceb	OK	ceb	ceb	OK	cef	cef	cek	cef	cef	cef	cek	OK	ceb	cek	8243	3
4.	caf	cef cek	ceb	ceb cek cef	cek ceb cef	cek ceh cef	cef ceb	cef cek	caf ceh cef	caf cab cef cek	cef	cek ceb cef	cef	cef ceh ceb	cef	ceh cek ceb	8243	3
5.	ceh ceb cef	cef	ceh cek	OK	cek ceb	cek cef	OK	ceh	cef ceb cek	cek	cef cek	ceh	ceb	cef ceh	ceb	cef	8243	3
6.	cek ceb cef caf	cek caf ceh cef	cek	cek cef	cek cef	cek caf	cek	ceb cef	OK	cek cef	cek	cek ceh	ceb	OK	cek	cei cef	8243	3
7.	ceb ceh	ceh cek ceb	ceh cef	ceh cek	ceh cef	cef	cef	cef	OK	ceb cef ceh	cef ech	ceh	ceh	ceh	ceh cef	cef ceb	8243	3
8.	cek ceb ceh	cef	cek	ceb cej	cef cek	cek ceb	cek ceb cef	cef	cek cef	cef ceh	cef	cef ceh	ceh cef	cef	cei ceh	caf cef ceb	8243	3
9.	ceb caf cek	cek ceb ceh cef	cef	cef cek cab caf	OK	cef	cek	cef	cef	cef	cef	OK	cef ceb	OK	ceb cek cef	cef ceb	8243	3

FIGURE A-1. INSPECTION DATA ON CENTER ROW OF CUSTOM CMOS DEVICES FOR VENDOR B

Wafer No.	Row Number 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Device Type	Run No.
10.	ceb cek ceh cei cak ceb	ceb cef ceh	OK	ceb	ceb	cef	OK	cef	cef	cef	ceb	ceb	cef	OK	cek	OK	8243	3
11.	cef ceb	OK	cef ceh cek	cef cei	ceh cek cef	cek	cek	ceb	cek cef	OK	cef	cef ceb	ceb cef	cef	OK	cek ceb	8243	3
12.	cef	cek ceh ceb	cek cef	ceh cef	ceh cef	cek cef ceb	cef ceb cek	OK	cef cek	cef cek	cef	ceh cef	ceb	ceb cef	cef cek	cef cek	8243	3
13.	cef	cef	cef ceb	ceb cef ceh cek	ceh cek	OK	ceb	OK	cek cef	cef	cab	cef	OK	cef	cef ceb	ceb	8243	3
14.	cef ceb	cek cei	cek cef	cef caf	cek	cek cef	cef	cef	cef	cef	cef cek	cef	OK	cef ceh	cef	cef cek ceh	8243	3
15.	ceb cef ceh	cek	ceb cef cek	ceh ceb	ceh cef cek	cek ceb	ceb	OK	cek	cek ceb	cek	OK	cef cek ccb	cek	chj cek	ceb cef cdd	8243	3
16.	ceb cef	ceh cef	cek cef ceh	OK	cek ceb	cek ceb	OK	cab	OK	cef	caf cab	cef	cek ceb cef ceh	OK	cek	cef ceb	8243	3
17.	ceb cef	cbi ccf	OK	OK	OK	caf	caf caj cek cab	caj cek	ceb cef	ceb cef	ceh	OK	cef ceb	cek	OK	ceb	8243	2
18.	caf ceb	ceh	ceh cef	ceh caj	caj	OK	OK	ceh	ceh	ceh	OK	ceh	ceh	OK	ceb cef	ceh cek	8243	2

FIGURE A-1 (CONTINUED). INSPECTION DATA ON CENTER ROW OF CUSTOM CMOS DEVICES FOR VENDOR B

Wafer No.	Row Number 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Device Type	Run No.
19.	← Missing →					OK	OK	ceb	cef	OK	OK	ceh cef	ceb cef	OK	ceh caf	caf ceb	8243	2
20.	ceb cef	cef	OK	OK	cef	OK	ceb	cef	cef	OK	cef	caf	caf caa	← Missing →			8243	2
21.	OK	ceb cef	ceb cek ceh cef	OK	cef	ceb	ceb cek cef	OK	ceb cek cef	cef ceb cek caf	← Missing						8239	1
22.	cef	OK	cej	cek	OK	ceh	OK	cek	OK	ceh	OK	OK	OK	ceh	ceb ceh	ceh ceb caf	8243	2
23.	ceb cef	caf ceb cek	ceb	OK	cef cek	cek cab caf cef	cef cek ceb	OK	OK	ceb cek	OK	OK	ceb	cek ceh	chj	OK	8243	3
24.	cek ceb	ceh	cek ceh ceb	cek cei	ceb	cek ceb cef	cek cef	cek cei ceb	cek cef	cef cel	cef	cef cel	caf ceb cel cab	cef	ceh cef	ceh cek ceb	8243	3
25.	cek ceb	OK	cef chd cek	cek	ceb cek cef	cek ceb	ceb	OK	ceh	cek	ceb	OK	cek	cek ceb	ceh cek ceb	ceb cei caf cef	8243	3
26.	ceh caf	OK	ceb	cek ceb	OK	cek	OK	ceh caf	caf	OK	ceh	ceb					8239	2
27.	Missing →			ceb cef	cef ceb	cab caf	cab	cab caf	ceh cab	ceh cab cef	Missing						8239	2
28.	ceb	cef cab	ceb	cef cek	ceh cef	ceh	ceb	ceb	OK	ceb	OK	caf cei					8239	2
29.	Missing →			cef cek caf	cab caf	caf chj cab ceb ceh cek	cab ceb	cek caf cab ceb	cab caf	caf cab	Missing						8239	2

FIGURE A-1 (CONTINUED). INSPECTION DATA ON CENTER ROW OF CUSTOM CMOS DEVICES FOR VENDOR B

Wafer No.	Row Number 1	2	3	4	5	6	7	8	9	10	11	12	13	Device Type	Run No.
30.	OK	cei ceb	OK	OK	cei	OK	ceb	OK	ceb	OK	ceb	caf cfh		8239	2
31.	OK	caf	cak cdf cdf	cdf cdf cdf	cdf	cdf	OK	OK	cdb	caj	cek	cek	cdf	8240	2
32.	cdf cdb	OK	OK	ceb	ceb	cek	OK	ceb	OK	OK	OK	adf	adf	8240	2
33.	OK	OK	OK	cef	OK	OK	cef	OK	OK	OK	OK	OK	caa	8240	2
34.	abk	abk	abk	cef	cef ceb	OK	OK	cef	OK	OK	cef	cek	OK	8240	2
35.	OK	OK	OK	cef	OK	cef	OK	OK	OK	OK	cek	OK	caj	8240	2
36.	cek	ceb	ceb	OK	OK	OK	OK	OK	OK	OK	cef	OK	cef	8240	2
37.	OK	caj	OK	cef	ceb	ceb ceb ceb	cef	OK	ceb	OK	OK	OK	OK	8240	2
38.	OK	OK	OK	cek	OK	OK	OK	OK	OK	cdf cdf	cdb cdf cdf	OK	OK	8240	2
39.	ceb	cej	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	8240	2
40.	caa	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	8240	2
41.	OK	cdb	OK	adl	adl	adl	OK	OK	OK	OK	OK	OK		8239	5
42.	cdb	cdb	OK	OK	cdb cdb	OK	OK	OK	OK	OK	ceb	cef		8239	5
43.	cek	OK	OK	OK	adf	OK	OK	OK	cef	OK	caa			8239	5

FIGURE A-1 (CONTINUED). INSPECTION DATA ON CENTER ROW OF CUSTOM CMOS DEVICES FOR VENDOR B

VISUAL INSPECTION RESULTS

ON

BIPOLAR DEVICES FROM VENDOR E

TABLE A-2

SUMMARY OF INSPECTION

OF BIPOLAR DEVICES

Device Types	Run Number	Number of Wafers Inspected	Number of Die Inspected
1643	5979	10	296
1643	5369	3	75
8212	5821	6	116
8212	5902	12	317
8212	5822	3	84
8212	5810	11	334
8212	5819	6	162
		51	1382

DEVICE TYPE 1643 RUN NUMBER 5979 INSPECTOR - L. Paradiso DIE SIZE - 83 MILS X 92 MILS

Wafer No.	Row Number 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
1.	OK	bef	OK	OK	OK	OK	OK	OK	OK	OK	cdf	cdf	cdf cdf	cdf	cdf	OK	cdf cdf cdf	cdf cdf	cdf cdf	cdf cdf	cdf	cdf	OK	cdf	OK	OK			
2.	OK	bef	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	cdf	OK	OK	cdf	OK	OK	OK	OK	cdf	OK	OK	OK	OK				
3.	acb	cdf cdf	OK	OK	caj	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	cdf	OK	OK	QK	OK	OK	OK	OK	OK		
4.	ceh	bef cej	caf	OK	OK	OK	OK	OK	ceb	OK	OK	OK	OK	cdf cdf	cdf cdf	ceh	OK	OK	OK	cdf cah	cdf	OK	OK	caj	OK	caj	OK	OK	OK
5.	caa	cdf cdf ceb	OK	cab	OK	OK	OK	cdf	OK	OK	OK	ceh	cdf	cdf ceb	ceb	ceb	OK	cdb cdb	ceb	cef	ceh cef	OK	OK	OK	OK	OK	OK	OK	cdf
6.	OK	cdf	OK	OK	OK	OK	OK	OK	OK	ceb	OK	cef cdf	cek	ceb	OK	OK	cef	OK	OK	OK	OK	OK							
7.	OK	OK	cek	OK	cdf	OK	OK	OK	OK	OK	OK	OK	caj	OK	ceh	OK	cef cek cek	ceh ceb	OK	OK	OK	OK	OK	OK					
8.	OK	caj	caj	ceh	OK	caj	caj	OK	OK	OK	OK	OK	OK	OK	cek cef	cek	OK	cdf	cdf	OK	OK	cdf	OK	cef	OK				
9.	OK	OK	OK	OK	OK	OK	cek	OK	caj	OK	OK	OK	ceb	OK	OK	OK	OK	OK	cgh cef	cej cdf	OK	OK	OK						
10.	OK	OK	OK	OK	OK	OK	OK	cef	OK	OK	OK	OK	OK	OK	cdf	OK	ceb	OK	OK	OK	OK	OK	OK	cek	cek				

FIGURE A-2. INSPECTION DATA ON CENTER ROW OF BIPOLAR WAFERS INSPECTED AT VENDOR'S FACILITY

DEVICE TYPE 1643 RUN NUMBER 5369 INSPECTOR - L. Paradiso DIE SIZE - 83 MILS X 92 MILS

11. caj caj OK OK OK OK OK OK OK OK OK OK OK OK OK OK OK caa caa caa OK OK OK

12. ceb cek OK OK OK OK OK OK caa caa OK OK OK OK cef OK OK cek OK OK OK OK cek OK OK
ceb bef
caa
cek

13. caa bef OK OK OK OK OK OK OK OK OK OK OK OK OK OK OK OK OK OK OK OK OK OK OK OK
ceb caa
ceb

DEVICE TYPE 8212 RUN NUMBER 5821 INSPECTOR - L. Paradiso DIE SIZE - 87 MILS X 113 MILS

14. Vapox problem on this wafer not etched though bonding pads. This wafer has some foreign material across the wafer. Probably could be cleaned.

abk abk abk cej cej cej cef cei OK cej cej cej cej cej ccj ccj OK OK abk cej cej
cej caa cej

15. cei OK cej cej OK ccb ceh ceh cdf ceh ccb OK OK OK ceh OK OK OK OK OK OK OK OK ceh
caa cah caj cej

16. ceh ceh OK OK OK acb OK ceh cef cek ccb ccb cbi cbi ceh ceh OK cbi ceh OK OK OK OK caa ceh
acf caa cek

17. OK OK OK ccf ccb cdd ceh cek OK cek OK caa cek OK cbi cdd cbi
cbi cek caa cej ceh cek ccf

18. caa cej OK cbi OK bcb cbi ceh cek cek cek OK cej cej OK cek OK cek ccf OK OK OK OK ccb cej
cek cek cek cdd ccb cek cej cej cdd

19. OK OK caa OK OK bcb ccf ceh OK ccf ccb OK ceh OK cek cek cej cek OK ccf OK ceh OK ceh ceh
ceh ccf ccf cdd cek ceh

DEVICE TYPE DP8212 RUN NUMBER 5902 INSPECTOR - Vendor's Inspector DIE SIZE - 87 MILS X 113 MILS

20. ceh ccb OK OK beh OK OK OK ccb OK OK OK ccf OK OK ccb OK ccb ceh ccf ccf
cek

21. ccb ccf OK ccf beh OK OK ccb ccf OK OK ccf ccf OK ccf ccf bcb ccf ccf OK ceh ccf ccf ceh
ceh ceh bcf cek
cbi
cej

FIGURE A-2 (CONTINUED) INSPECTION DATA ON CENTER ROW OF BIPOLAR WAFERS INSPECTED AT VENDOR'S FACILITY

DEVICE TYPE DP8212 RUN NUMBER 5902 INSPECTOR - Vendor's Inspector DIE SIZE - 87 MILS X 113 MILS

22. cbi cej caa cbi beh OK OK ceh OK OK OK ceh OK ceh OK OK bcb OK OK OK ccb ccf OK ceh caa
ceh bcf ceh

23. caa ceh cek caa cej OK OK OK ceh OK cek OK ceh OK ceh OK OK ceb OK OK cek cek ceb cei
cek cek ceh caa cek cei cef cek
ceh cej
cej

24. ceb ceb OK OK OK cek OK OK OK OK OK ceb OK ceh cek OK OK ceb OK cei OK cek OK cei caa
caa cek ceh ceb cek
cef

25. cek cek OK OK ceh OK OK ceb OK ceb cei OK OK OK OK OK ceb OK OK OK cek cek ceh OK
ceb

26. cek OK OK cef cef OK OK ceb OK OK cei OK OK OK OK OK ceb OK OK OK cek cek OK

27. caa caa OK OK cei OK OK OK caa caa OK OK ceb ceb OK cek cei ceb OK cef OK cek ceb OK OK
cek cek cef cek

28. ceb cek OK ceb OK cdf OK OK OK OK OK OK OK OK OK OK ceb OK OK OK cek cef cek cek
cek ceh cek
caa

29. cek caa cej OK ceb OK caa cej cej OK OK ceb OK OK OK OK OK ceb OK OK caa cek caa OK caa
caa cef cek

30. caa cek OK OK OK cek OK cei OK cef OK OK OK OK OK OK caa ceb OK OK OK cek OK caa caa
cef cei

31. cef cek cej OK OK OK OK OK cek OK OK OK OK OK OK OK OK OK ceb OK OK OK cek ceb caj ceh
cek caa
cej

FIGURE A-2 (CONTINUED) INSPECTION DATA ON CENTER ROW OF BIPOLAR WAFERS INSPECTED AT VENDOR'S FACILITY

DEVICE TYPE 8212 RUN NUMBER 5822 INSPECTOR - L. Paradiso DIE SIZE - 87 MILS X 113 MILS

32. caa OK cej cej cej cek ceh cef OK OK OK OK cah cah caa cah cej OK OK OK OK cej OK ceh OK cej OK OK cej OK cej
cab cah caa caf

33. cej cej OK OK OK OK OK OK OK OK OK OK cek ceh cef cej ceb OK OK ceh caa OK OK

34. cek cah cah ceh ceh OK ceb OK OK cek cef OK OK OK OK OK OK OK OK OK ceb cek OK OK OK OK OK OK OK

DEVICE TYPE 8212 RUN NUMBER 3810 INSPECTOR - L. Paradiso DIE SIZE - 87 MILS X 113 MILS

35. cej caf OK OK OK ceb OK OK OK OK OK OK OK OK OK OK OK OK OK OK OK OK OK OK caa caa caa

36. ceb OK OK OK OK OK cek OK OK caa OK ceh OK OK OK OK OK OK OK OK OK OK OK
ceh

37. cek OK cej OK OK OK OK OK OK cek OK OK OK OK OK OK OK OK OK OK OK OK OK OK cek OK OK OK

38. caa cef OK caa OK OK OK cej OK OK OK OK OK caa caa OK OK OK OK caa ceb OK cef OK OK caa OK
ceh cej

39. ceb cek OK OK OK OK OK cek ceb OK OK OK caa OK OK OK OK cdd OK OK OK cek OK OK
ceb cek
ceb

40. caa OK caa OK OK OK OK OK cej OK OK OK OK OK OK OK ceb OK OK OK OK cek OK OK OK OK ceh
cej
caa
cek

41. OK OK OK OK OK OK OK OK OK OK OK OK OK OK OK OK OK ceh OK OK OK OK OK OK OK OK OK OK ceh ceh

42. caa OK OK OK OK OK OK OK OK OK OK OK OK OK OK OK OK OK OK cej OK OK OK OK OK OK cej OK

43. cej OK cef ceh OK OK OK OK OK OK OK OK OK OK OK OK cej OK OK OK OK OK OK ceb OK OK OK OK OK cej OK cek OK caf

44. OK OK OK OK OK OK OK OK OK OK OK OK OK OK OK OK ceh OK OK OK OK ceb ceb cef OK OK OK OK cej OK OK OK

45. OK OK OK ceh OK cej cek OK OK OK OK cej ceh OK OK OK OK OK OK ceb OK OK OK OK OK OK OK OK cdf

FIGURE A-2 (CONTINUED). INSPECTION DATA ON CENTER ROW OF BIPOLAR WAFERS INSPECTED AT VENDOR'S FACILITY

DEVICE TYPE 8212 RUN NUMBER 5819 INSPECTOR - L. Paradiso DIE SIZE - 87 MILS X 113 MILS

46. OK OK cek cdd cef OK cbi OK OK OK cej OK OK OK cek OK OK cej OK OK cef OK OK cej ceh cej OK OK
cek cbi

47. caa ceb cek ceh OK ceh cei ceh OK OK ceh OK OK OK OK OK OK OK OK OK OK ceh OK OK OK
caa ceh cej
cek ceb

48. OK cej ceh cef OK OK OK OK OK OK OK OK OK cek cek OK OK cej OK OK OK OK OK OK cef OK OK cej cej OK cej OK
cek

49. cef OK OK OK OK OK OK cdd OK OK OK OK OK OK OK OK OK OK OK OK OK cej OK OK cej OK OK
ceb

50. ced OK OK OK cek OK OK OK OK cek cej cek cek OK OK OK OK OK OK OK OK OK OK OK OK OK OK
ceh

51. ceh cej cej OK OK ceh cej OK OK OK OK OK OK OK OK cek cej OK cej cej OK cej cej OK OK OK cej OK
cej

159/160

FIGURE A-2 (CONTINUED) INSPECTION DATA ON CENTER ROW OF BIPOLAR WAFERS INSPECTED AT VENDOR'S FACILITY

APPENDIX B

WAFER INSPECTION SPECIFICATION FOR RADC VERIFICATION TEST VEHICLES (131252)

APPLICATION			REVISIONS					
DASH NO.	NEXT ASSY	USED ON	LTR	DESCRIPTION			DATE	APPROVED
			A	CHG BY SGS	CHK BY	ECO NO.	7/19/72	
				Revised shs 2,5,6,11,12,16,18,23,25 Sheets 12,18 redrawn				

REVISION INDEX																									
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
	REV	A	A			A	A					A	A				A		A					A		A	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE APPLIED FINISH TOLERANCES

2 PLACE ± 3 PLACE ± ANGLES ±

CONTRACT NO.

DR BY | CHK BY

ENGINEER

PROJECT ENGINEER

APPROVAL

APPROVAL

HARRIS ELECTRONIC SYSTEMS DIVISION MELBOURNE, FLORIDA 32901

TITLE

WAFER INSPECTION FOR
RADC VERIFICATION TEST VEHICLES

SIZE	CODE IDENT NO.		REV
A	91417	131252	A

SCALE | SHEET 1 of 26

DoD FORM 000000-1- M

1.0 INTRODUCTION

This procedure consists of three (3) separate inspection procedures:

Section 2 - Post Development Inspection

Section 3 - Post Etch Oxide Inspection

Section 4 - Post Etch Metalization Inspection

These inspections will be performed in place of the manufacturer's normal inspections at these points, however, any reject criteria used by the manufacturer that is not specifically called out by this procedure due to unique process requirements should be performed in the usual manner.

In addition to the three wafer inspection plans the following will apply:

1. No wafer with reworked metalization will be acceptable for this study.
2. All inspection data for each lot processed shall be recorded and sent to Harris ESD. This data shall consist of the number of defects found at each inspection by defect category.
3. The die from the wafers will be inspected [under low magnification (30X to 60X)] to MIL-STD-883B Method 2010.2 Condition B for probe damage (Para. 3.2.1.5), scribing and die defects (Para. 3.2.3), foreign material (Para. 3.2.6.1 Part C), and scratches (Para. 3.2.1.1). This inspection will be performed at low magnification (30X to 60X) using both a stereo microscope per MIL-STD-883, Method 2010.7, Paragraph 3 (d) and a metallurgical microscope perpendicular to the die surface with illumination normal to the die surface.

HARRIS CORPORATION ELECTRONIC SYSTEMS DIVISION MELBOURNE, FLORIDA 32901	SIZE A	CODE IDENT NO. 91417	131252	REV A
	SCALE			SHEET 2

400958-9 K

SECTION 2

POST DEVELOPMENT

INSPECTION

HARRIS CORPORATION ELECTRONIC SYSTEMS DIVISION MELBOURNE, FLORIDA 32901	SIZE A	CODE IDENT NO. 91417	131252	REV
	SCALE		SHEET 3	

2.0 POST DEVELOPMENT INSPECTION

2.1 Purpose

The purpose of this inspection is:

A. To screen the wafers for gross batch defects and misalignments introduced during application of resist, alignment, exposure, or developing.

B. To assure the mask integrity by a first wafer inspection.

C. To lot accept each run for batch and random circuit defects introduced during application of resist, alignment exposure or developing.

This purpose is accomplished by the following inspections:

A. Inspection of the first wafer aligned and exposed prior to exposing the entire lot.

B. Rough wafer inspection under ultraviolet illuminator.

C. Alignment inspection of four worst case location circuits.

D. Detailed circuit inspection in select wafer locations with metalurgical microscope.

HARRIS CORPORATION ELECTRONIC SYSTEMS DIVISION MELBOURNE, FLORIDA 32901	SIZE A	CODE IDENT NO. 91417	131252	REV
	SCALE		SHEET 4	

2.2 Procedure

2.2.1 First Off Wafer Inspection

A maximum of seven masks to wafer contacts will be allowed with each mask.

The first wafer aligned and exposed each time a new mask is used will be developed and inspected prior to using the mask. Based on the number of circuits on the wafer, select the number of circuits to be inspected from Table 1. For the sample selected, refer to Table 2 to determine the location of the circuits to be inspected on the wafer.

Inspect each circuit in the sample with a metalurgical microscope at 100X to 200X magnification for damaged photoresist as indicated in Paragraph 2.3.2. In addition, perform the alignment inspection of Paragraph 2.2.3.

If the number of defects found in the sample exceeds the accept number in Table 1 or if the alignment acceptance criteria of Paragraph 2.2.3 is not met, reject the mask and repeat this procedure until an acceptable mask is found. (Accept mask if defects found are considered workmanship related.)

SAMPLING PLAN FOR

FIRST OFF WAFER INSPECTION

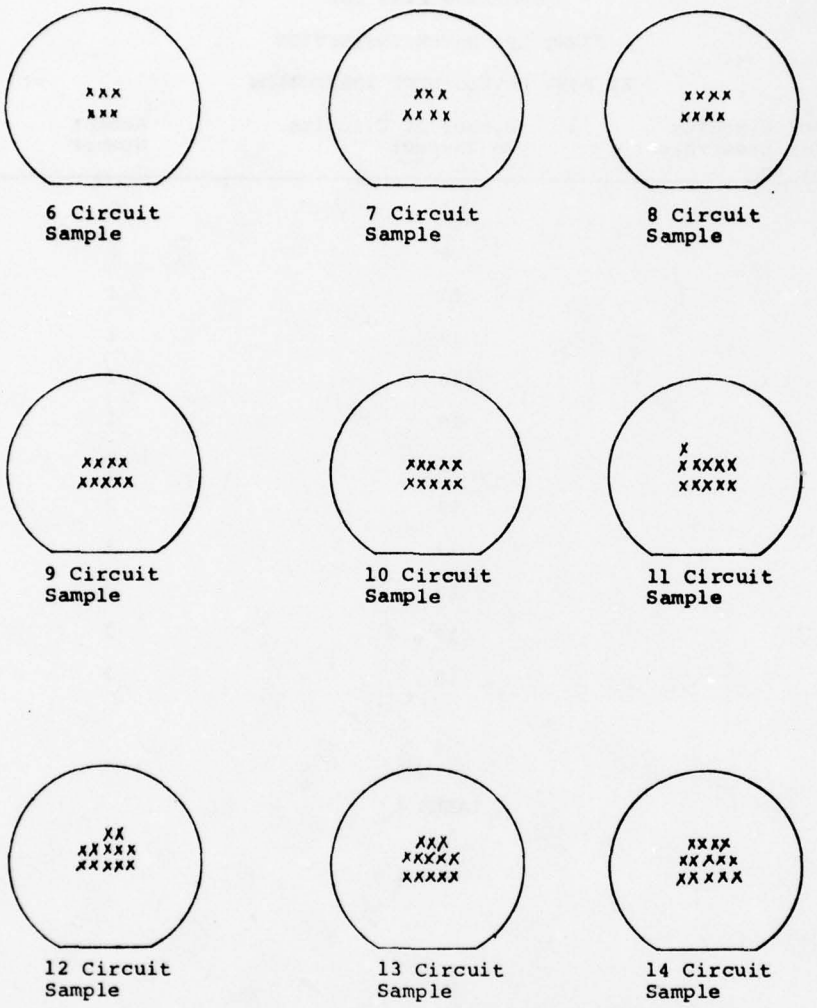
AT POST DEVELOPMENT INSPECTION

Number of Circuits Per Wafer Less Than Or Equal to	Number of Circuits To Inspect	Accept Number
100	6	0
200	6	0
300	10	1
400	10	1
500	10	1
600	10	1
700	13	2
800	13	2
900	13	2
1000	13	2
1100	13	2
1200	13	2

TABLE 1

HARRIS CORPORATION ELECTRONIC SYSTEMS DIVISION MELBOURNE, FLORIDA 32901	SIZE	CODE IDENT NO.		REV
	A	91417	131252	A
	SCALE			SHEET 6

400833-9 K



LOCATION ON WAFER OF CIRCUITS
TO BE SELECTED FOR INDICATED SAMPLE SIZE

TABLE 2

HARRIS CORPORATION ELECTRONIC SYSTEMS DIVISION MELBOURNE, FLORIDA 32901	SIZE A	CODE IDENT NO. 91417	131252	REV
	SCALE			SHEET 7

400925-8 K

15 Circuit
Sample

16 Circuit
Sample

ALL WAFERS TO BE INSPECTED

WITH FLAT TOWARD OPERATOR

TABLE 2 (Continued)

HARRIS CORPORATION ELECTRONIC SYSTEMS DIVISION MELBOURNE, FLORIDA 32901	SIZE A	CODE IDENT NO. 91417	131252	REV
	SCALE			SHEET 8

2.2.2 Rough Wafer Inspection

After the entire run is developed inspect all wafers under a dark field illuminator to reveal gross defects. Reject any wafers that exhibit the following defects:

a. No film

Any wafer without photoresist.

b. Double Image

Any wafer having the pattern exposed twice.

c. Partial Coverage

Any wafer where pattern is not covering the wafer to within (appearance of 1/8 moons) a 1/8" of the edge.

d. Voids

Any rips or tears in the photoresist covering more than one circuit (caused by scratches, contamination or mask contact problems).

e. Lifting Resist

Any photoresist peeling from the wafer surface.

f. Photoresist Quality

Any irregularities in the resist such as cloudiness, smudges, crushed photoresist, strain on surface, drops of photo resist or uneven photoresist coverage (comets).

2.2.3 Alignment Inspection

Inspect four (4) circuits as shown in Figure 1 on each wafer for alignment with a metalurgical microscope at 150X - 200X magnification.

FIGURE 1

Reject Criteria

Reject wafer if any one of the four (4) circuits inspected does not meet the manufacturer's accept/reject alignment criteria (if alignment marks are used only the alignment masks need to be inspected). For the metalization mask the wafers must meet the metalization alignment criteria of Paragraph 3.1.1.7 of Method 2010.2 in MIL-STD-883A.

HARRIS CORPORATION ELECTRONIC SYSTEMS DIVISION MELBOURNE, FLORIDA 32901	SIZE A	CODE IDENT NO. 91417	131252	REV
	SCALE		SHEET 10	

2.2.4 Detailed Wafer Inspection

Based on the number of wafers in the lot, select the number of circuits to inspect on each wafer from Table 3. For the sample selected, refer to Table 2 to determine the location of the circuits to sample on the wafer. Inspect each circuit in the sample with a metalurgical microscope at 100X to 200X magnification to the post development defect criteria of Paragraph 2.3.0.

If the number of defective circuits found on any one wafer exceeds the accept number in Table 3 for individual wafer, reject that wafer. If the number of rejected wafers exceeds the accept number for the lot, reject the lot.

HARRIS CORPORATION ELECTRONIC SYSTEMS DIVISION MELBOURNE, FLORIDA 32901	SIZE A	CODE IDENT NO. 91417	131252	REV A
	SCALE		SHEET 11	

2.3.0 Post Development Defect Criteria

2.3.1 Pattern Definition

Patterns must be clear of photo resist of designed size with edges of undeveloped areas sharp and clearly defined.

Patterns exhibiting the following conditions will be counted as defective:

a. Over Exposed Patterns

Developed areas smaller than designed size. Pattern edges will appear unclear and rounded.

b. Under Exposed Patterns

Developed areas larger than designed size pattern. Photoresist will usually be puckered.

c. Under Developed Patterns

Patterns with photoresist still remaining in opening. Patterns will have the appearance of cobwebs running through or along the edges of openings.

d. Spiking in Photoresist

Spikes of developed areas extending from designed openings to form undesigned open patterns.

e. Poorly Developed Patterns

Irregularities in the resist such as swelling making opening smaller than design value, puckered resist showing a rippled effect, or cloudy or smudged resist.

HARRIS CORPORATION ELECTRONIC SYSTEMS DIVISION MELBOURNE, FLORIDA 32901	SIZE A	CODE IDENT NO. 91417	131252	REV
	SCALE		SHEET 13	

400928-2 K

TABLE 3

SAMPLING PLAN FOR DETAIL
INSPECTION AT POST DEVELOPMENT

Number of Wafers in Lot	Number of Wafers in Lot	Number of Circuits per Wafer to Inspect	Accept No. for Individual Wafers	Accept No. for the Lot
	4	15	2	0
	5	12	2	0
	6	10	1	0
	7	9	1	1
	8	8	1	1
	9	7	1	1
	10	7	1	1
	11	7	1	1
	12	7	1	2
	13	6	0	2
	14	6	0	2
	15	6	0	3
	16	6	0	3
	17	6	0	3
	18	6	0	3
	19 through 21	6	0	4
	22 through 24	6	0	5
	25 through 28	6	0	6
	29 through 32	6	0	7
	33 through 34	6	0	8
	35 through 38	6	0	9
	39 through 42	6	0	10
	43 through 44	6	0	11
	45 through 46	6	0	12
	47 through 48	6	0	13
	48 through 50	6	0	14

HARRIS CORPORATION ELECTRONIC SYSTEMS DIVISION MELBOURNE, FLORIDA 32901	SIZE A	CODE IDENT NO. 91417	131252	REV A
	SCALE		SHEET 12	

400825-6 K

2.3.0 Post Development Defect Criteria

2.3.1 Pattern Definition

Patterns must be clear of photo resist of designed size with edges of undeveloped areas sharp and clearly defined.

Patterns exhibiting the following conditions will be counted as defective:

a. Over Exposed Patterns

Developed areas smaller than designed size. Pattern edges will appear unclear and rounded.

b. Under Exposed Patterns

Developed areas larger than designed size pattern. Photoresist will usually be puckered.

c. Under Developed Patterns

Patterns with photoresist still remaining in opening. Patterns will have the appearance of cobwebs running through or along the edges of openings.

d. Spiking in Photoresist

Spikes of developed areas extending from designed openings to form undesigned open patterns.

e. Poorly Developed Patterns

Irregularities in the resist such as swelling making opening smaller than design value, puckered resist showing a rippled effect, or cloudy or smudged resist.

HARRIS CORPORATION ELECTRONIC SYSTEMS DIVISION MELBOURNE, FLORIDA 32901	SIZE A	CODE IDENT NO. 91417	131252	REV
	SCALE		SHEET 13	

400F28-8 K

2.3.2 Damaged Photo Resist

Photo resist with voids or contamination in the form of tears or scrapes in the photoresist.

Patterns exhibiting the following conditions will be counted as defective:

a. Scratches

Any scratches in the surface of photoresist.

b. Lifting Photo Resist

Any lifting or peeling photoresist.

c. Pinholes

Any pinholes in the photoresist.

d. Voids

Any voids in photoresist (this includes voids due to contamination of mask or photoresist).

HARRIS CORPORATION ELECTRONIC SYSTEMS DIVISION MELBOURNE, FLORIDA 32901	SIZE A	CODE IDENT NO. 91417	131252	REV
	SCALE		SHEET 14	

400825-SK

SECTION 3

POST ETCH OXIDE INSPECTION

HARRIS CORPORATION ELECTRONIC SYSTEMS DIVISION MELBOURNE, FLORIDA 32901	SIZE A	CODE IDENT NO. 91417	131252	REV
	SCALE		SHEET 15	

400823-8 K

3.0 POST ETCH OXIDE INSPECTION

Inspection to be performed after post etch photoresist stripping.

3.1.0 Purpose

The purpose of this inspection is to lot accept each run for batch and random circuit defects introduced at the etching and cleaning operation. This will be accomplished by the following inspections:

a. A rough wafer inspection under ultraviolet illuminator.

b. A detail wafer inspection under a metalurgical microscope at 100X to 200X magnification.

HARRIS CORPORATION ELECTRONIC SYSTEMS DIVISION MELBOURNE, FLORIDA 32901	SIZE A	CODE IDENT NO. 91417	131252	REV A
	SCALE		SHEET 16	

3.2.0 Procedure

3.2.1 Sample Selection

Refer to Table 4 to determine the number of wafers to be inspected. For the sample selected, refer to Table 2 to determine the location of the circuits on the wafer to be sampled for the detail wafer inspection of Paragraph 3.2.3. Randomly select the wafers from the lot for inspection.

3.2.2 Rough Wafer Inspection

Inspect each wafer from the sample selected in Paragraph 3.2.1 under a dark field illuminate for the following defects as described in Paragraph 3.3.0.

a. Contamination

b. Streaks and clouds

c. Oxide in openings

If any part of any wafer does not meet this criteria, reject the wafer and inspect all remaining wafers in the sample and in the lot.

TABLE 4

SAMPLING PLAN FOR DETAILED
POST ETCH OXIDE INSPECTION

No. of Wafers in Lot	No. of Wafers per Lot to Inspect	No. of Circuits per Wafer to Inspect	Total No. of Circuits to Inspect	Accept. No. for Lot
1	1	6	6	0
2	2	6	12	1
3	3	6	18	2
4	4	6	24	4
5	5	6	30	6
6	5	6	30	6
7	5	6	30	6
8	5	6	30	6
9	5	6	30	6
10	5	6	30	6
11	5	6	30	6
12	5	6	30	6
13	6	6	36	8
14	6	6	36	8
15	6	6	36	8
16	8	6	48	11
17	8	6	48	11
18	8	6	48	11
19	8	6	48	11
20	8	6	48	11
21	10	6	60	14
to				
50	10	6	60	14

HARRIS CORPORATION ELECTRONIC SYSTEMS DIVISION MELBOURNE, FLORIDA 32901	SIZE A	CODE IDENT NO. 91417	131252	REV A
	SCALE		SHEET 18	

400930-8 M

3.2.3 Detail Wafer Inspection

Inspect each circuit in the sample selected in Paragraph 3.2.1 with a metalurgical microscope at 100X to 200X magnification for the following defects as described in Paragraph 3.0.*

a. contamination

b. oxide in openings

c. overetching

d. pinholes

e. oxide faults

If the number of defects found in the sample exceeds the accept number as indicated in Table 4, reject the lot.

* The detect criteria for inspection of the glassivation layer (Vapox) will be substituted with Paragraph 3.1.7 of method 2010.2 of MIL-STD-883A.

HARRIS CORPORATION ELECTRONIC SYSTEMS DIVISION MELBOURNE, FLORIDA 32901	SIZE A	CODE IDENT NO. 91417	131252	REV
	SCALE		SHEET 19	

3.3.0 Defect Criteria

a. Contamination

1. Residue of photoresist not fully removed from the wafers.

2. Foreign material on the wafers.

b. Streaks and Clouds

c. Oxide in Openings

No oxide shall be visible in oxide opening.

d. Overetching (Undercutting)

The openings must not be overetched to the extent that triple lines can be seen at the edge of the oxide opening. Other tighter criteria due to design constraints are to be imposed by the manufacturer at each masking level as required.

e. Pinholes

Any pinholes in oxide visible when viewed with a metalurgical microscope at 200X magnification minimum.

HARRIS CORPORATION ELECTRONIC SYSTEMS DIVISION MELBOURNE, FLORIDA 32901	SIZE A	CODE IDENT NO. 91417	131252	REV
	SCALE		SHEET 20	

AD-A052 418 HARRIS CORP MELBOURNE FLA ELECTRONIC SYSTEMS DIV F/G 9/5
QA PROCEDURES FOR COMPLEX MICROCIRCUITS.(U)
DEC 77 L R PARADISO, J L WOLCOTT F30602-76-C-0328
UNCLASSIFIED RADC-TR-77-418 NL

3 OF 3
AD A052418

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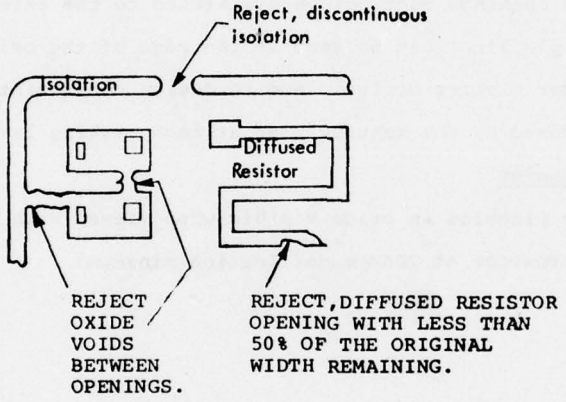
DATE FILMED
5-78
DDC

f. Oxide Faults

1. Any oxide voids that allow bridging between oxide opening (see figure 2).

2. Any isolation opening that is discontinuous or any other opening with less than 25 percent (50 percent for resistors) of the original designed width that remains (see figure 2).



OXIDE FAULTS

FIGURE 2

HARRIS CORPORATION ELECTRONIC SYSTEMS DIVISION MELBOURNE, FLORIDA 32901	SIZE A	CODE IDENT NO. 91417	131252	REV
	SCALE			SHEET 21

400923-2 K

SECTION 4

POST ETCH METALIZATION

INSPECTION

HARRIS CORPORATION ELECTRONIC SYSTEMS DIVISION MELBOURNE, FLORIDA 32901	SIZE A	CODE IDENT NO. 91417	131252	REV
	SCALE		SHEET 22	

400823-2 K

4.0 POST ETCH METALIZATION INSPECTION

4.1 Purpose

The purpose of this inspection is to screen each lot for batch and random circuit defects introduced at metal deposition, metal etching photoresist stripping. This will be accomplished by the following inspections:

a. A rough wafer inspection under ultraviolet illuminator.

b. A detail wafer inspection under a metalurgical microscope at 100X to 200X magnification.

HARRIS CORPORATION ELECTRONIC SYSTEMS DIVISION MELBOURNE, FLORIDA 32901	SIZE A	CODE IDENT NO. 91417	131252	REV A
	SCALE		SHEET 23	

400850-8 K

4.2 Procedure

4.2.1 Sample Selection

Refer to the Table 5 to determine the number of circuits on each wafer to be inspected. For the sample selected, refer to Table 2 to determine the location of the circuits on the wafer to be sampled for the detail wafer inspection of Paragraph 4.2.3.

4.2.2 Rough Wafer Inspection

Inspect each wafer under an ultraviolet illuminator for contamination (residue of photoresist not fully removed from wafers or foreign material on wafers). If any part of any wafer does not meet this criteria, reject the wafer.

SAMPLING PLAN FOR

METALIZATION INSPECTION

Number of Circuits Per Wafer Less Than or Equal To	Number of Circuits To Inspect	Accept Number
100	7	1
200	7	1
300	10	2
400	10	2
500	10	2
600	10	2
700	13	3
800	13	3
900	13	3
1000	13	3
1100	13	3
1200	13	3

TABLE 5

HARRIS CORPORATION ELECTRONIC SYSTEMS DIVISION MELBOURNE, FLORIDA 32901	SIZE A	CODE IDENT NO. 91417	131252	REV A
	SCALE		SHEET 25	

400828-8 K

4.2.3 Detail Wafer Inspection

Inspect each circuit in the sample selected in Paragraph 4.2.1 with a metalurgical microscope at 100X to 200X magnification for the following defects as defined in Paragraphs 3.1.1.1, 3.1.1.2, 3.1.1.3, 3.1.1.4, 3.1.1.6, 3.1.1.7 and 3.1.6.1 (Post (b) and (c) only) of Method 2010.2 of MIL-STD-883A.

a. Metalization scratches
b. Metalization voids
c. Metalization corrosion
d. Metalization adherence
e. Metalization Bridging
f. Metalization alignment
g. Foreign material

If the number of defects found in the sample exceeds the accept number as indicated in Table 5, reject the wafer.

HARRIS CORPORATION ELECTRONIC SYSTEMS DIVISION MELBOURNE, FLORIDA 32901	SIZE A	CODE IDENT NO. 91417	131252	REV
	SCALE		SHEET 26	

400923-2K

APPENDIX C

OPERATING CHARACTERISTIC CURVES FOR IN-LINE INSPECTION PLANS

OPERATING CHARACTERISTIC CURVES FOR IN-LINE INSPECTION PLANS

Operating Characteristic Curves for Post Development Inspection

Operating Characteristic Curves for Post Etch Oxide Inspection

Operating Characteristic Curves for Post Etch Metal Inspection

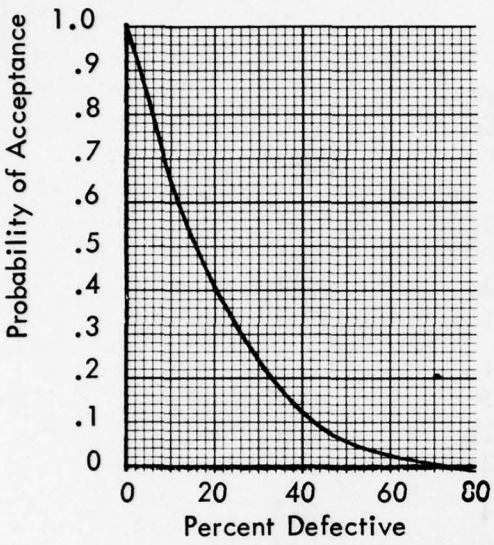
Operating Characteristic Curves for First Off Wafer Inspection

OPERATING CHARACTERISTIC CURVES FOR POST DEVELOPMENT INSPECTION *

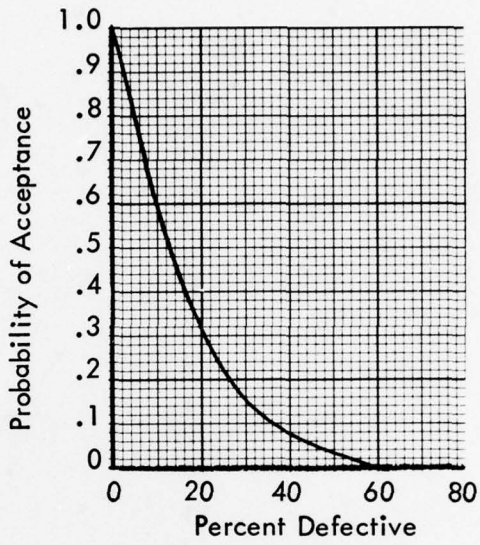
Sample Size (N)	Accept Number (C)	Figure
4	0	C-1
5	0	C-1
6	0	C-1
7	1	C-1
9	1	C-2
11	1	C-2
12	2	C-2
15	3	C-2
21	4	C-3
23	5	C-3
25	6	C-3
29	7	C-3
33	8	C-4
35	9	C-4
39	10	C-4
43	11	C-4
45	12	C-5
47	13	C-5
49	14	C-5

* Since a number of the operating curves are very similar only representative curves are shown. To approximate a curve not given, use the proper value of C with the nearest value of N.

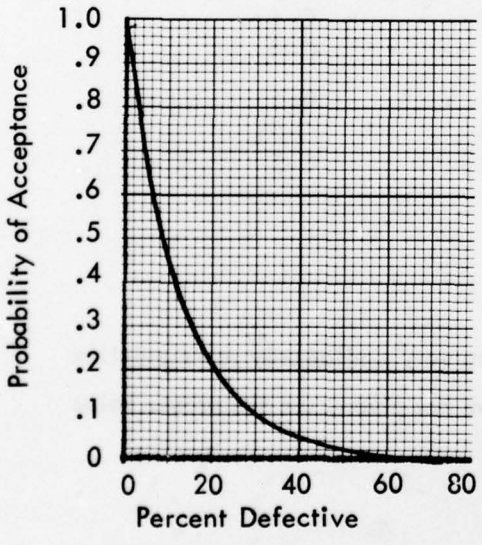
OPERATING CHARACTERISTIC CURVES
FOR SAMPLING PLAN FOR POST DEVELOPMENT



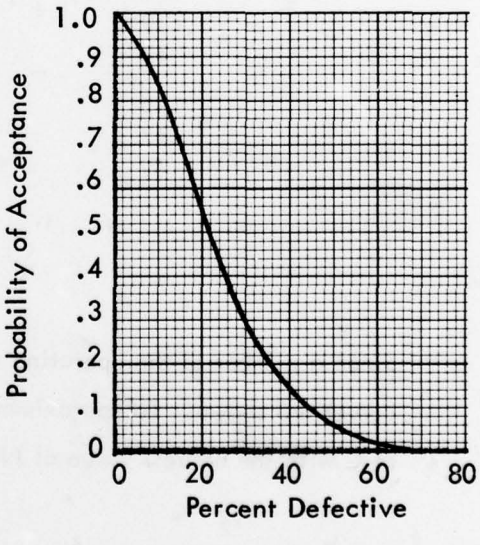
N = 4, C = 0, LTPD = 44



N = 5, C = 0, LTPD = 36



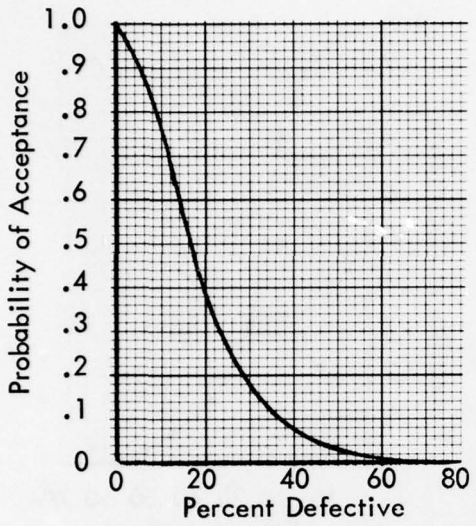
N = 6, C = 0, LTPD = 32



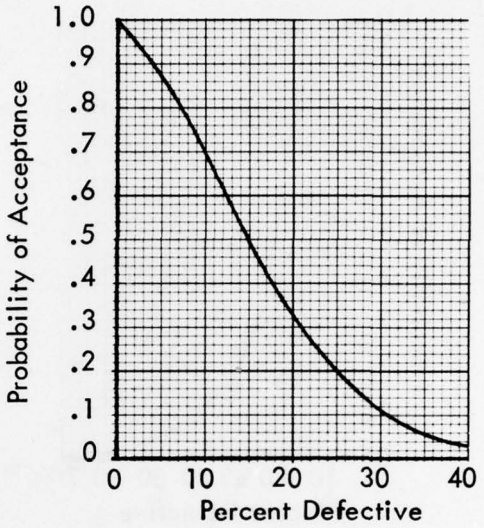
N = 7, C = 1, LTPD = 44

FIGURE C-1

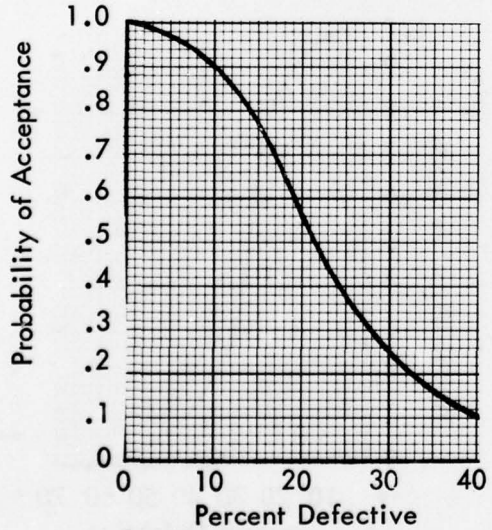
OPERATING CHARACTERISTIC CURVES
FOR SAMPLING PLAN FOR POST DEVELOPMENT



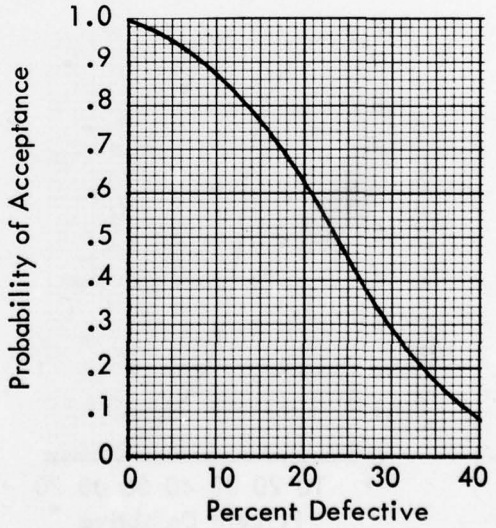
N = 9, C = 1, LTPD = 36



N = 11, C = 1, LTPD = 32



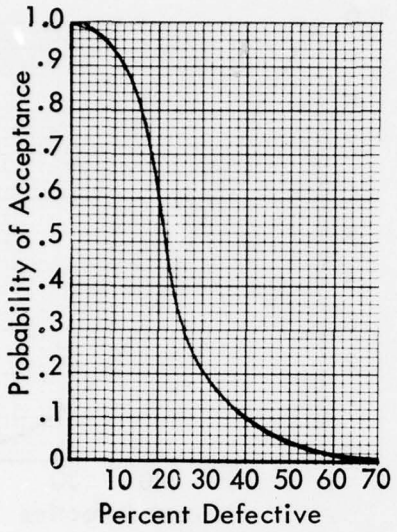
N = 12, C = 2, LTPD = 38



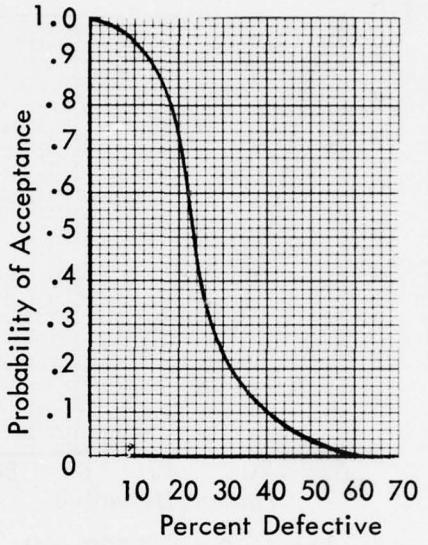
N = 15, C = 3, LTPD = 34

FIGURE C-2

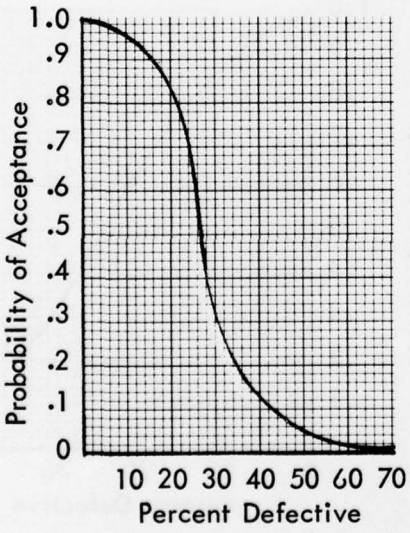
OPERATING CHARACTERISTIC CURVES
FOR SAMPLING PLAN FOR POST DEVELOPMENT



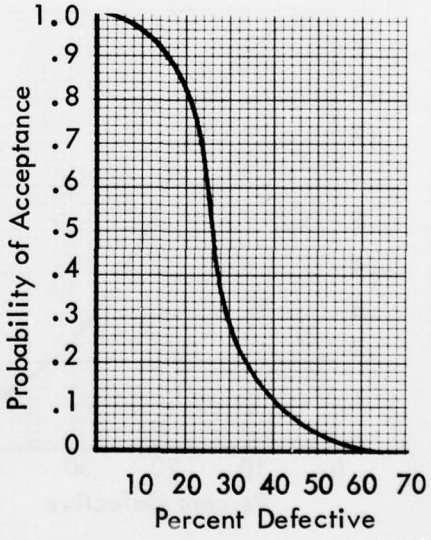
N =21, C = 4, LTPD = 38



N = 23, C = 5, LTPD - 40



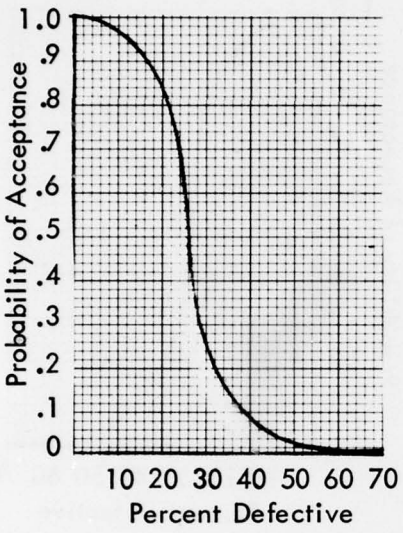
N =25, C = 6, LTPD = 42



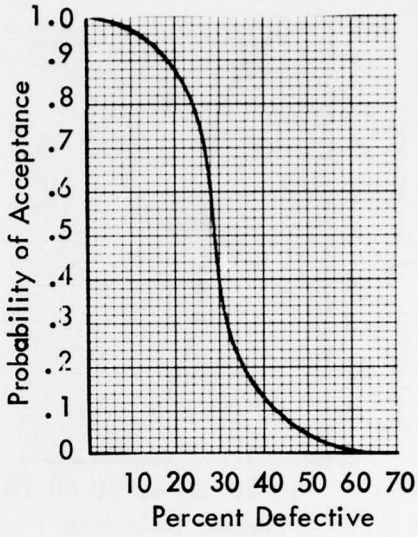
N = 29, C = 7, LTPD = 41

FIGURE C-3

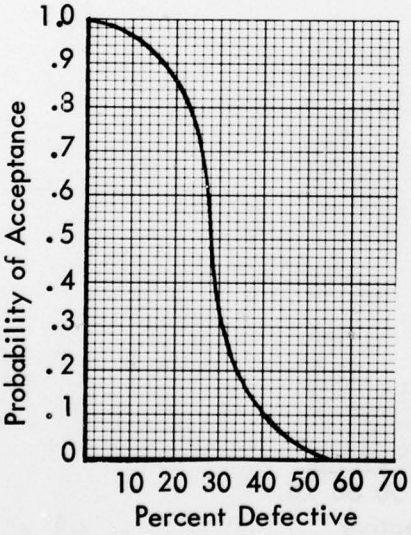
OPERATING CHARACTERISTIC CURVES
FOR SAMPLING PLAN FOR POST DEVELOPMENT



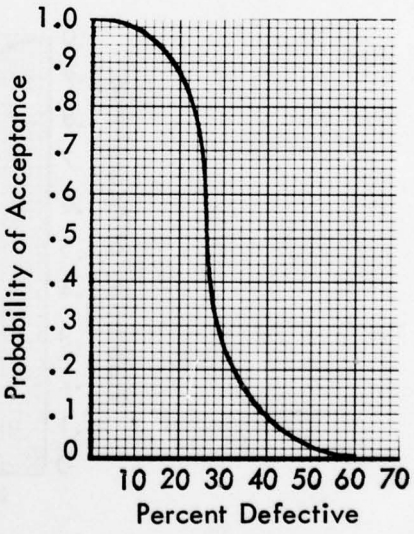
N = 33, C = 8, LTPD =39



N = 35, C = 9, LTPD = 40



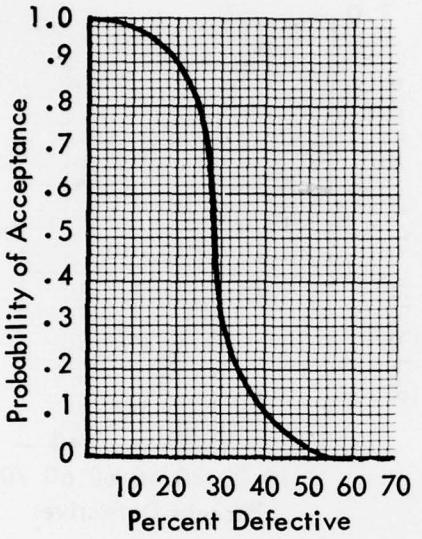
N =39, C = 10, LTPD = 41



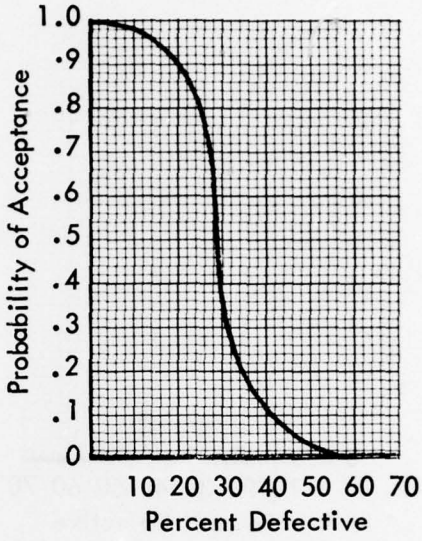
N = 43, C = 11, LTPD = 39

FIGURE C-4

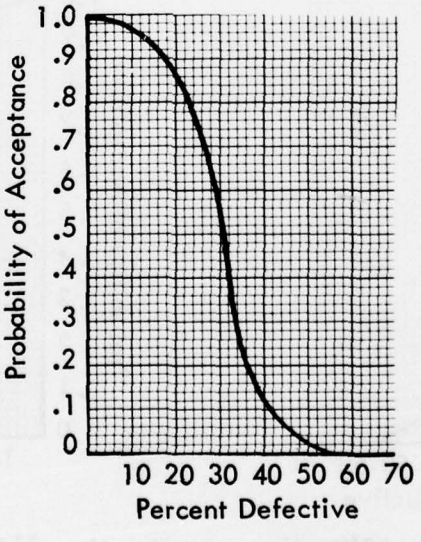
OPERATING CHARACTERISTIC CURVES
FOR SAMPLING PLAN FOR POST DEVELOPMENT



N = 45, C = 12, LTPD = 40



N = 47, C = 13, LTPD = 40



N = 49, C = 14, LTPD = 41

FIGURE C-5

OPERATING CHARACTERISTIC CURVES FOR POST OXIDE ETCH INSPECTION

Sample Size (N)	Accept Number (C)	Figure
6	0	C-6
12	1	C-6
18	2	C-6
24	4	C-6
30	6	C-7
36	8	C-7
48	11	C-7
60	14	C-7

OPERATING CHARACTERISTIC CURVES
POST ETCH OXIDE

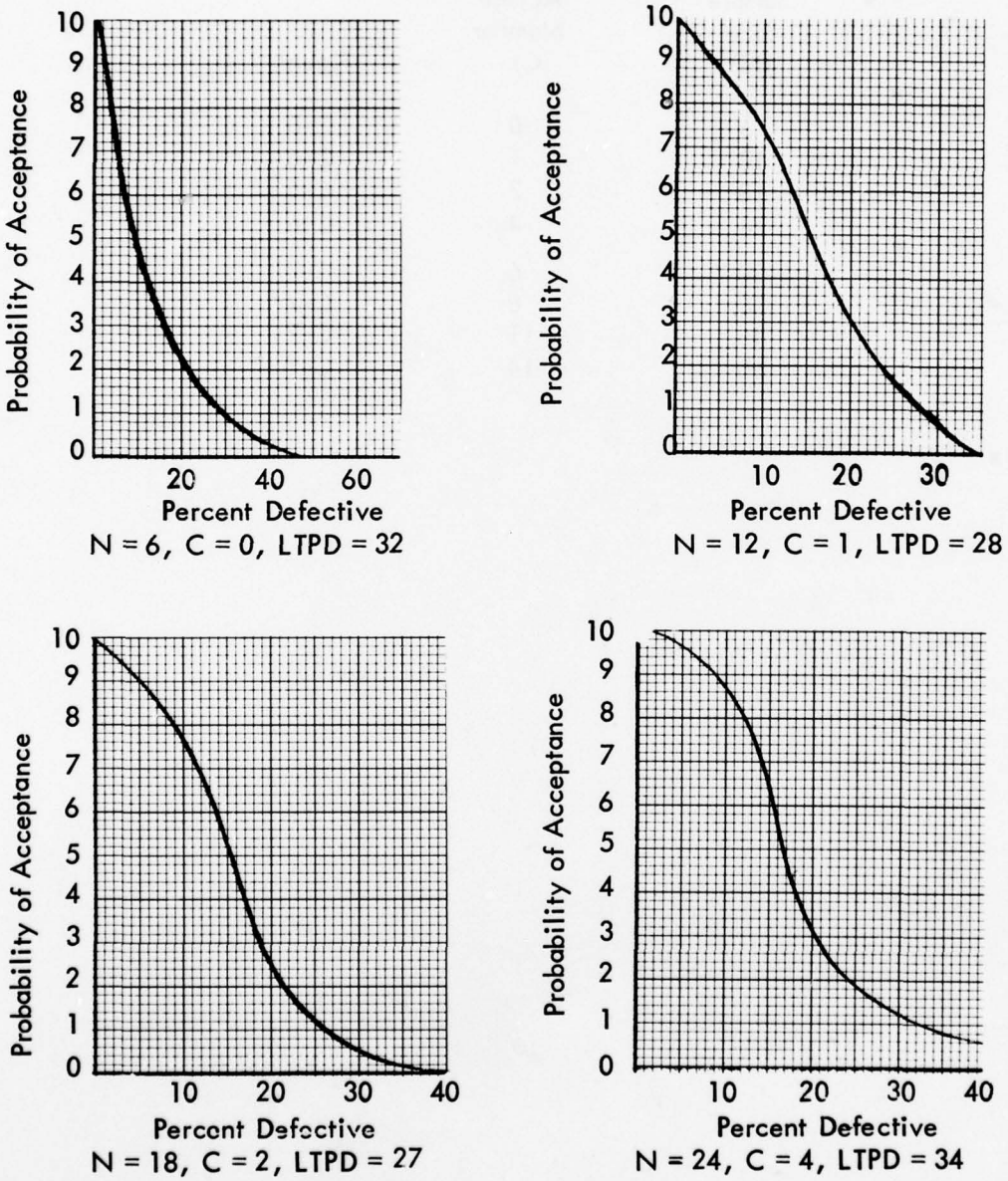
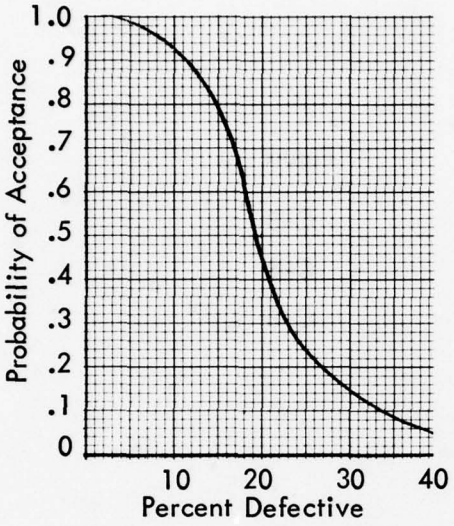
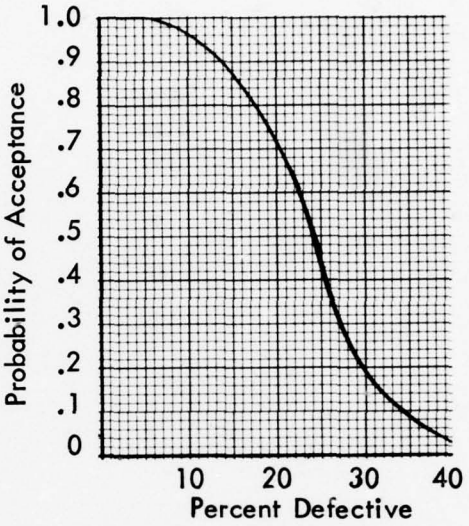


FIGURE C-6

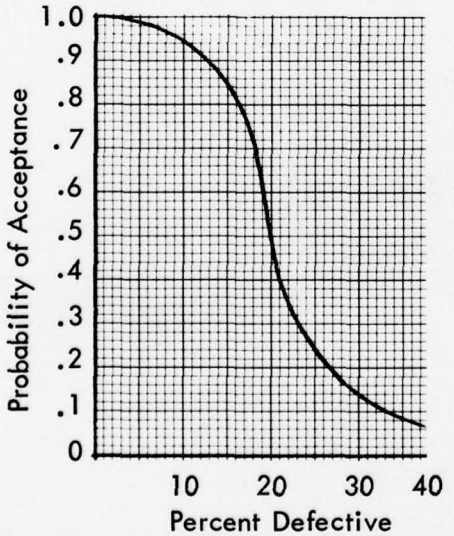
OPERATING CHARACTERISTIC CURVES
POST ETCH OXIDE



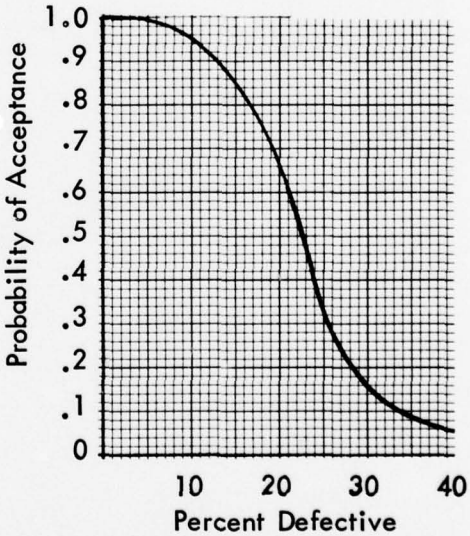
N =30, C = 6, LTPD = 34



N = 36, C = **8**, LTPD = 34



N =48, C = 11, LTPD = 34



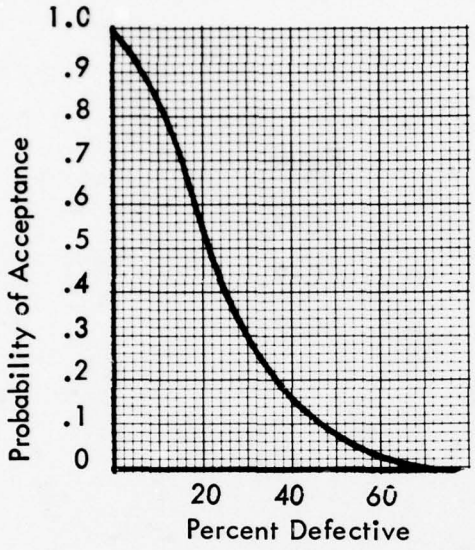
N = 60, C = 14, LTPD = 34

FIGURE C-7

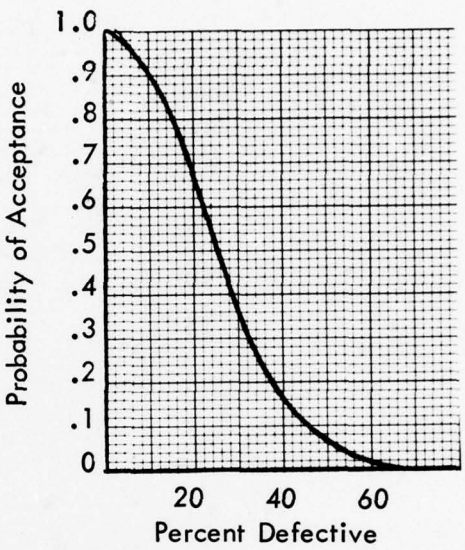
OPERATING CHARACTERISTIC CURVES
FOR POST ETCH METAL INSPECTION

Sample Size (N)	Accept Number (C)	Figure
7	1	C-8
10	2	C-8
13	3	C-8

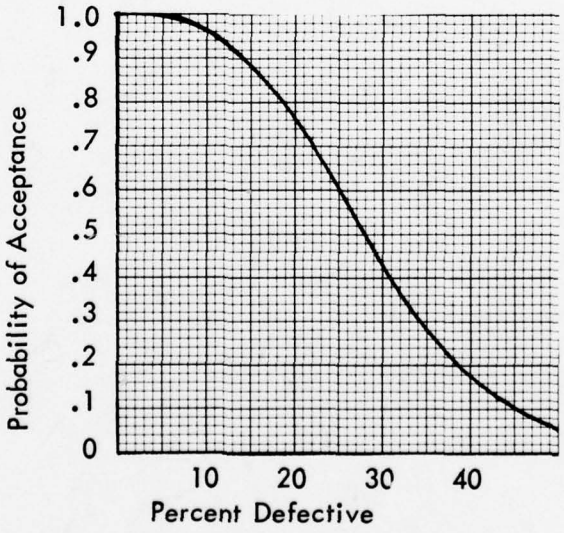
OPERATING CHARACTERISTIC CURVES
FOR SAMPLING PLAN AT POST ETCH METAL INSPECTION



N = 7, C = 1, LTPD = 44



N = 10, C = 2, LTPD = 44



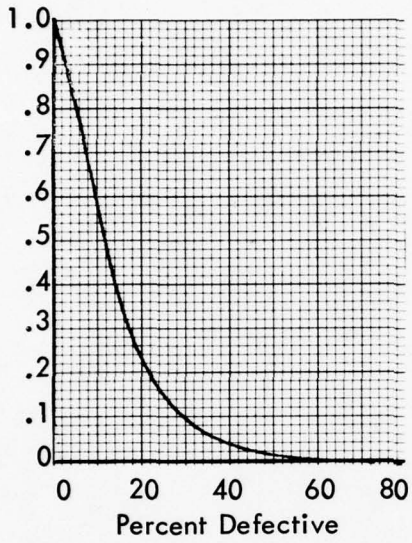
N = 13, C = 3, LTPD = 45

FIGURE C-8

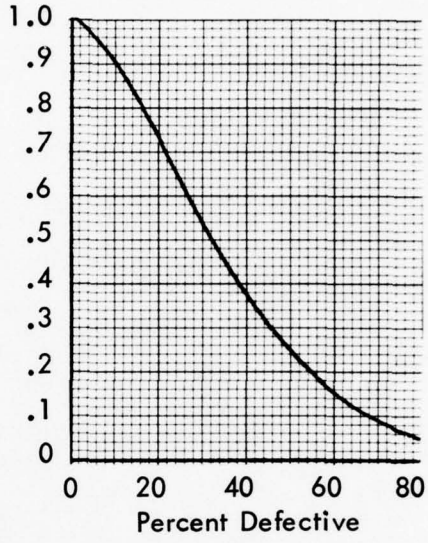
OPERATING CHARACTERISTIC CURVES FOR FIRST OFF WAFER INSPECTION

Sample Size (N)	Accept Number (C)	Figure
6	0	C-9
10	1	C-9
15	2	C-9

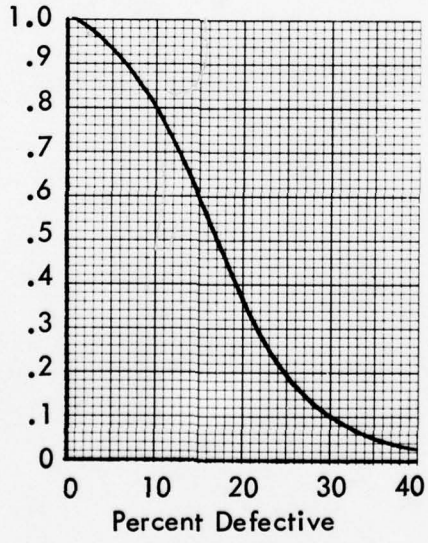
OPERATING CHARACTERISTIC CURVES
FOR FIRST OFF WAFER INSPECTION



N = 6, C = 0, LTPD = 32



N = 10, C = 1, LTPD = 32



N = 15, C = 2, LTPD = 33

FIGURE C-9

APPENDIX D

SEM INSPECTION REPORTS ON FINAL VERIFICATION STUDY SAMPLES

1. Bipolar Devices, Vendor E
2. CMOS Devices, Vendor E

SEM ACCEPTANCE REPORT

CUSTOMER: Harris Electronics Systems

PURCHASE ORDER: 215944

CUSTOMER PART NUMBER: 131252-001

VENDOR E PART NUMBER:

BASIC DEVICE TYPE: Bipolar study sample

SALES ORDER: 542419

SP NUMBER: D0006

SEM SPECIFICATION: S-311-P-12A

SEM ACCEPTANCE LOT NUMBER: 2507

WAFER RUN NUMBER: 6915

DATE ACCEPTED: 1-15-77

ACCEPTANCE VERIFIED BY: (original signed)

NOTE: Vendor references replaced with "VENDOR E".

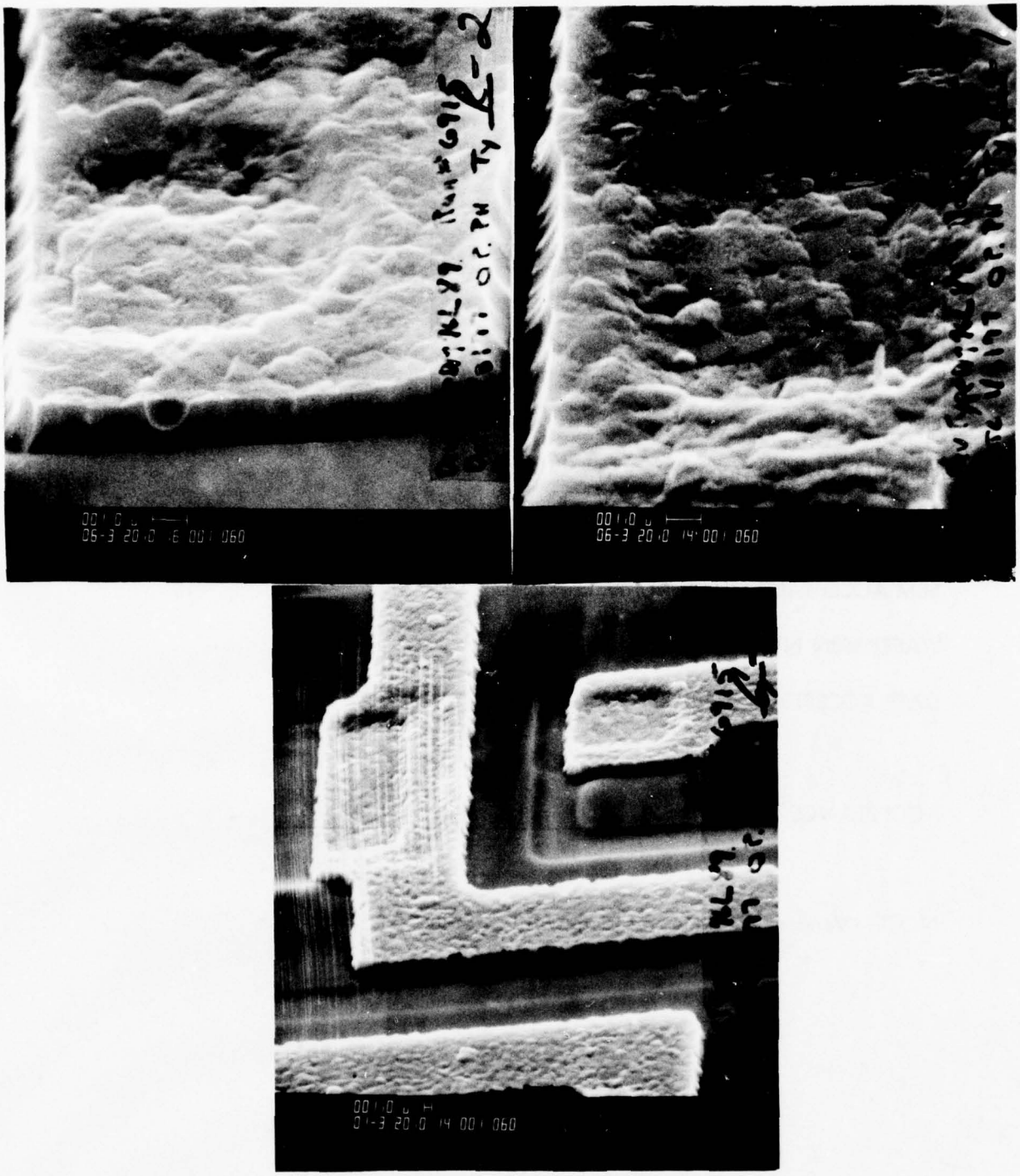


FIGURE D-1 SEM PHOTOGRAPHS

SEM ACCEPTANCE REPORT

CUSTOMER: Harris

PURCHASE ORDER: 215944

CUSTOMER PART NUMBER: 131252-002

VENDOR E PART NUMBER: -

BASIC DEVICE TYPE: CMOS study sample

SALES ORDER: ----

SP NUMBER: SPD0007

SEM SPECIFICATION: S-311-P-12A

SEM ACCEPTANCE LOT NUMBER: 2603

WAFER RUN NUMBER: CRE195

DATE ACCEPTED: 3-8-77

ACCEPTANCE VERIFIED BY (original signed)

NOTE: Vendor references replaced with "VENDOR E".

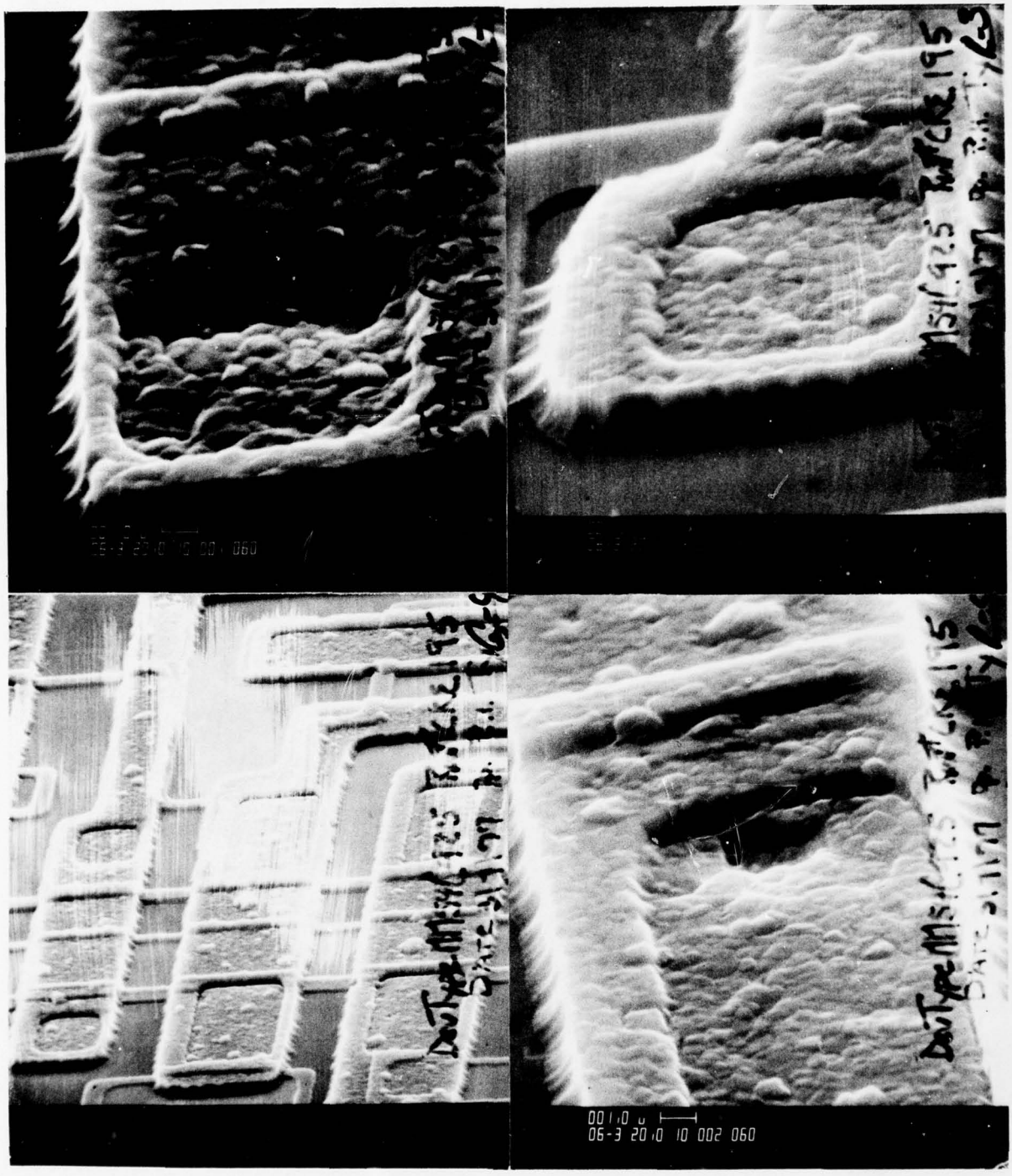


FIGURE D-2 SEM PHOTOGRAPHS

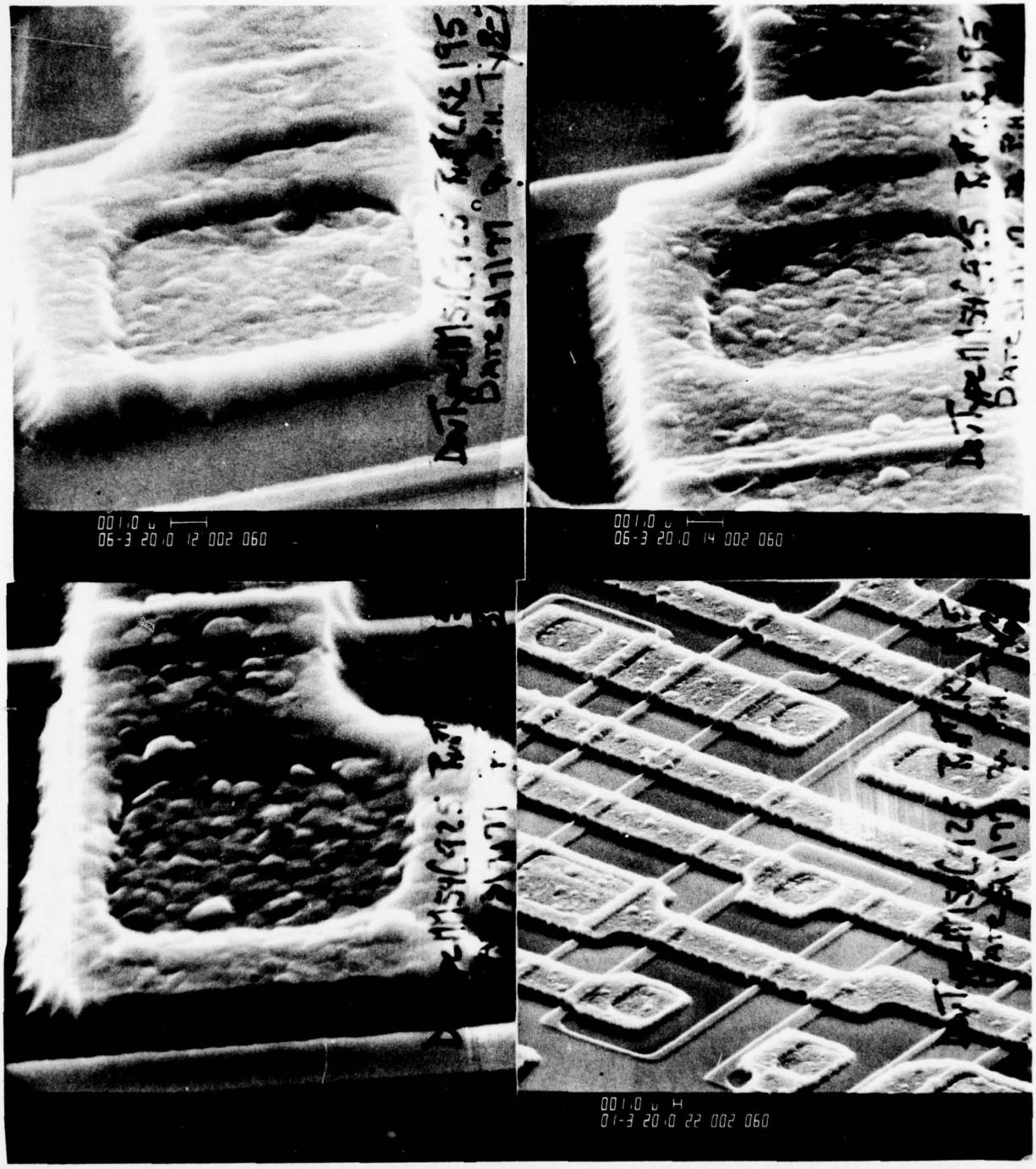


FIGURE D-3 SEM PHOTOGRAPHS

APPENDIX E

FAILURE ANALYSIS
OF
LIFTED POST BOND FAILURES

APPENDIX E

FAILURE ANALYSIS OF LIFTED POST BOND FAILURES

This Appendix discusses the lifted bond failure mechanism observed during the verification testing. Resolution of this failure mechanism was not considered to be a goal of this study. Therefore, this analysis has been dealt with as a separate section in this Appendix.

1. Analysis Summary

Prior to autopsy of the units each device was electrically tested utilizing a curve tracer (limited current). Each unit classified as an open bond failure, was confirmed by electrical probing. In some cases the opens were intermittant making it necessary to test at temperature extremes of -55°C and +125°C to detect the failures.

Autopsy was conducted subsequent to confirming the failure electrically. Observation of the post bond areas revealed that the gold had separated from the nickel plating indicating a lack of adhesion.

Figure E - 1a and 1b, are photographs of an initial defect from the study sample of the Final Verification Test.

Figure 1a shows a well formed lead bond with proper necking and bond size. Figure 1b shows the post from which the bond lifted and the bond mark is of the proper size; however, it can be seen that the gold plating has separated from the base nickel.

Figure E - 2a, depicts a 10 temperature cycle failure and Figure 2b a 100 temperature cycle failure with the same characteristics as found in the initially defective units.

Figure E-3 depicts a typical burn-in failure with the same symptoms as the initially defective units.

Figure E-4 is typical of the life test failures.

The lifted post bond failures were related to both the package and to the assembly run. For purposes of clear display in the analysis, failures were regrouped by package type.

Package	Assembly Run	No. of Bond Failures	Remarks
48 pin	1	0	One lot of packages
	2	0	
40 pin	1	1	
	2	15	One lot of packages
	3	1	
16 pin	1	42	
	2	1	Packages drawn from stock
	3	15	separately for each assembly
	4	3	run - Not traceable to lot.

The bond problem affects the 40-pin and 16-pin packages only as can be seen by the above data. Also, those lots with only 10 cycles of temperature cycling (16-pin, Run 2 and 4) had fewer failures than those lots with 100 cycles of temperature cycling (16-pin, Run 1 and 3).

2. Investigation

From the package manufacturer, it was determined that the 16-pin and 40-pin packages are made in one plant while the 48-pin package is made in another. In addition, at least two semiconductor users were identified who had the same problem with these packages. The defective production may span up to a six month time period. Both indicated a sporadic problem had been experienced but details of the exact cause of the lack of plating adhesion was not identified. One semiconductor vendor did reveal

that they had recently instituted a package lot qualification test which consisted of a wire bond pull test after the bond wires had been aged at +390°C for one hour.

The problem has been pinpointed to a plating adhesion difficulty, due to either gold plating thickness or contamination.

Further investigation of this problem was not within the scope of this study; therefore, it was not pursued nor corrective action taken.

INITIALLY DEFECTIVE STUDY SAMPLE

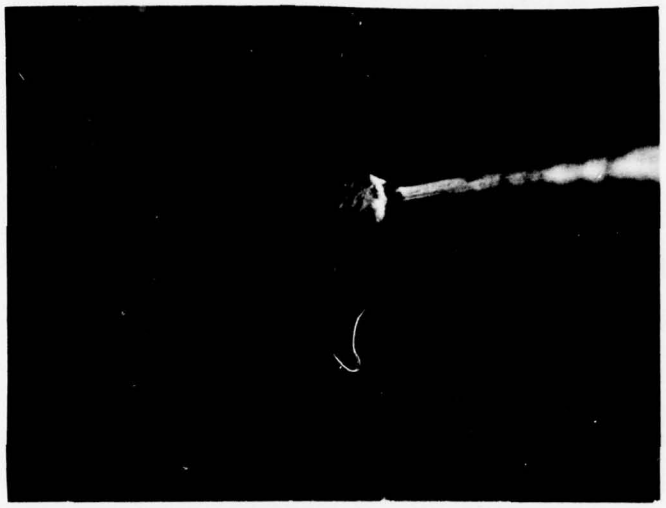


FIGURE E-1a

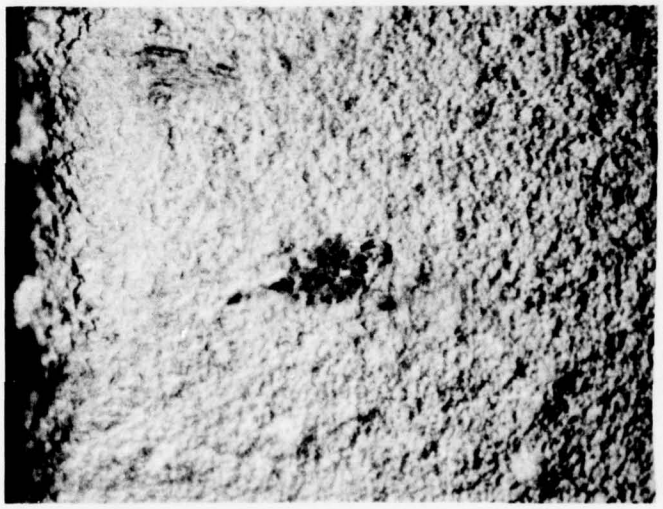


FIGURE E-1b

TEMPERATURE CYCLE FAILURES

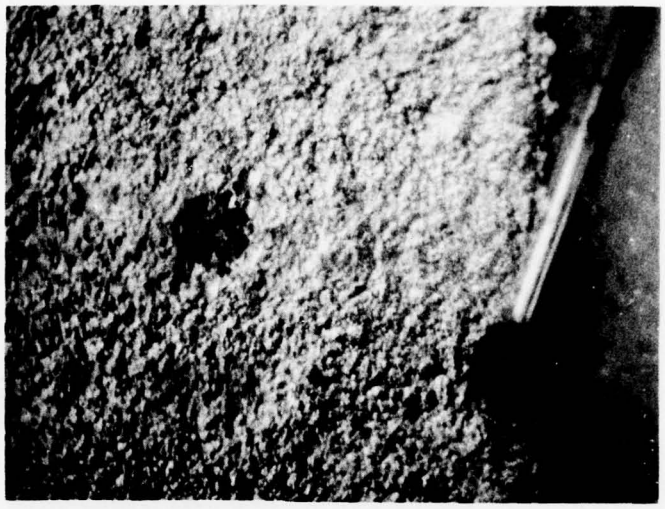


FIGURE E-2a

FIGURE E-2b

TYPICAL BURN-IN FAILURE

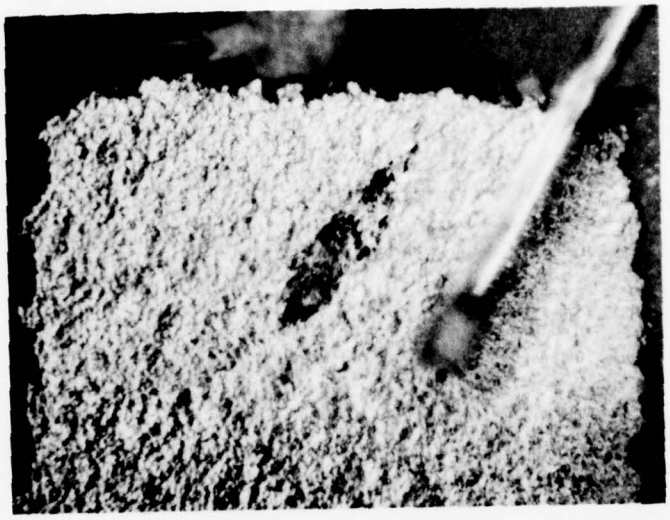


FIGURE E-3

TYPICAL OF THE LIFE TEST FAILURES

FIGURE E-4

APPENDIX F

RECOMMENDED MIL-STD-883 METHOD
FOR
WAFER PROCESS ACCEPTANCE

METHOD 5XXX

WAFER PROCESS ACCEPTANCE

1. PURPOSE

This method establishes the requirements for wafer process control and low power internal visual inspection to be performed in lieu of high power internal inspection on complex microcircuits.

2. APPARATUS

The apparatus for this test shall include optical equipment capable of the specified magnification(s) and ultra-violet illuminator and any visual standards (gages, drawings, photographs, etc.) necessary to perform an effective examination and enable the operator to make objective decisions as to the acceptability of the device being examined. Adequate fixturing shall be provided for handling devices during examination to promote efficient operation without inflicting damage to the units.

When referenced, additional apparatus used shall be in accordance with the apparatus requirements of the methods specified in Table I conditions.

3. PROCEDURE

The performance of the wafer process acceptance tests shall be in accordance with the conditions specified in Table F-1.

a) Magnification. High magnification inspection shall be performed perpendicular to the die surface with the device under illumination normal to the die surface. Rough wafer inspection shall be performed with the unaided eye under an ultra-violet illuminator at an angle of 30° to the wafer surface.

TABLE F-1
WAFER PROCESS ACCEPTANCE

Inspection	Condition	Inspect	Acceptance
1. All Photo Masking Steps			
First Off Wafer	Para 3.2	1- wafer	Mask acceptance
Post Development	Para 3.1	100% of lot	Wafer acceptance
Post Etch			
Oxide inspection as applicable	Para 3.3	sample	Lot acceptance
Metal inspection as applicable	Para 3.4	100% of lot	Wafer acceptance
2. Source Inspection Post contact aperature etch prior to 1st metal			Lot acceptance
3. Source Inspection Post metal etch prior to each glassivation			Wafer acceptance
4. SEM	Method 2018		Lot acceptance
5. Internal Visual	Method 2010.2 Cond B		
30X to 60X metallurgical microscope	Para 3.2.1 Para 3.2.3	100%	
30X to 60X stereo microscope	Para 3.2.1 Para 3.2.3 Para 3.2.4 Para 3.2.5 Para 3.2.6	100%	

b) Sequence of Inspection. The order in which the criteria are present is not a required order of examination and may be varied at the discretion of the manufacturer.

c) Interpretation. Only defects in the photoresist, oxide, or metal at the level being processed will be considered during inspection. Oxide and metal defects from previous levels will not be considered rejectable.

d) All wafers successfully passing the test shall be considered the lot for the remainder of the tests. All wafers failing the inspection shall be removed from the lot. Data obtained from all inspections shall be recorded. The sequence of the tests in Table F-1 does not have to be adhered to, however, the tests must be performed at the point in the processing (if specified) required in the conditions column of Table F-1. Rework on wafers is allowed, except for metal. No metal etch rework is allowed.

3.1 POST DEVELOPMENT WAFER INSPECTION

The purpose of this inspection is to 100% inspect wafers after photoresist development prior to all oxide and all metal etching steps for gross batch defects and misalignments introduced during application of resist, alignment, exposure, and developing.

3.1.1 Procedure

The inspection is a three-part inspection:

- o rough wafer inspection per Paragraph 3.1.1.1
- o alignment inspection per Paragraph 3.1.1.2
- o detail wafer inspection per Paragraph 3.1.1.3

The inspections are performed on 100% of the wafers.

3.1.1.1 Rough Wafer Inspection

The rough wafer inspection shall be conducted on each wafer under an ultra-violet illuminator. The rejection criteria for any wafer shall be as defined.

No Film - Any wafer without photoresist.

Double Image - Any wafer having the pattern exposed twice.

Partial Coverage - Any wafer where pattern is not covering the wafer to within (appearance of 1/8 moons) a 1/8-inch of the edge.

Voids - Any rips or tears in the photoresist covering more than one circuit (caused by scratches, contamination or mask contact problems).

Lifting Resist - Any photoresist peeling from the wafer surface.

Photoresist Quality - Any irregularities in the resist such as cloudiness, smudges, crushed photoresist, strain on surface, drops of photoresist or uneven photoresist coverage (comets).

3.1.1.2 Alignment Inspection

Inspect four circuits as shown in Figure F 3.1.1.2 on each wafer for alignment with a metallurgical microscope at 150X to 200X magnification.

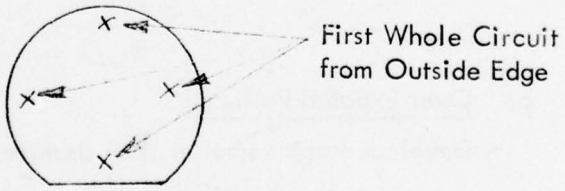


FIGURE F 3.1.1.2
WAFER ALIGNMENT INSPECTION

Reject wafer if any one of the four circuits inspected does not meet the requirements of Paragraphs a) or b).

a) Photoresist Oxide Inspection - The manufacturer's accept/reject alignment criteria (if alignment marks are used only the alignment marks need to be inspected).

b) Photoresist Metal Inspection - MIL-STD-883, Method 2010, Paragraph 3.1.1.7.

3.1.1.3 Detailed Wafer Inspection

Based on the number of wafers in the lot, select the number of circuits to inspect on each wafer from Table F 3.1.1.3-1. For the sample selected, refer to Figure F 3.1.1.3-2 to determine the location of the circuits to sample on the wafer. Inspect each circuit in the sample with a metallurgical microscope at 100X to 200X magnification to the post development defect criteria of Paragraphs 3.1.1.3.1 and 3.1.1.3.2.

If the number of defective circuits found on any one wafer exceeds the accept number in Table F 3.1.1.3-1 for individual wafer, reject that wafer. If the number of rejected wafers exceeds the accept number for the lot, reject the lot.

3.1.1.3.1 Pattern Definition

Patterns must be clear of photoresist of designed size with edges of undeveloped areas sharp and clearly defined.

No patterns exhibiting the following conditions shall be acceptable that exhibits:

a) Over Exposed Patterns

Developed areas smaller than designed size. Pattern edges will appear unclear and rounded.

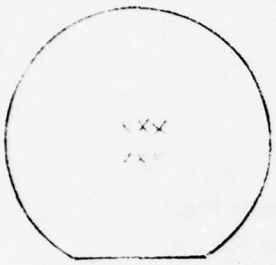
b) Under Exposed Patterns

Developed areas larger than designed size pattern. Photoresist will usually be puckered.

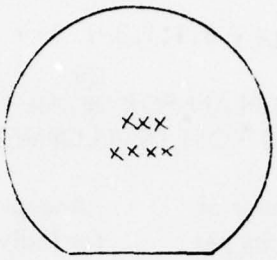
TABLE F 3.1.1.3-1

SAMPLING PLAN FOR DETAIL
INSPECTION AT POST DEVELOPMENT

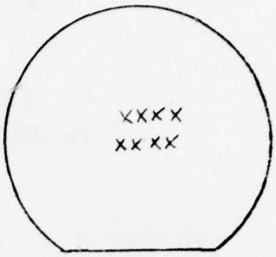
Number of Wafers in Lot	Number of Circuits per Wafer to Inspect	Accept No. for Individual Wafers	Accept No. for the Lot
4	15	2	0
5	12	2	0
6	10	1	0
7	9	1	1
8	8	1	1
9	7	1	1
10	7	1	1
11	7	1	1
12	7	1	2
13	6	0	2
14	6	0	2
15	6	0	3
16	6	0	3
17	6	0	3
18	6	0	3
19 through 21	6	0	4
22 through 24	6	0	5
25 through 28	6	0	6
29 through 32	6	0	7
33 through 34	6	0	8
35 through 38	6	0	9
39 through 42	6	0	10
43 through 44	6	0	11
45 through 46	6	0	12
47 through 48	6	0	13
48 through 50	6	0	14



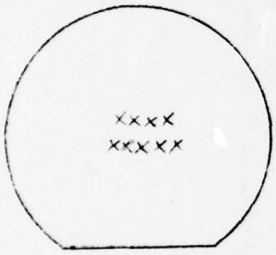
6 Circuit
Sample



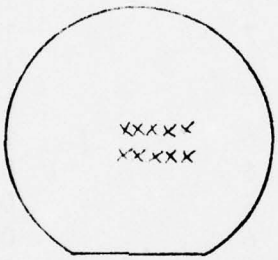
7 Circuit
Sample



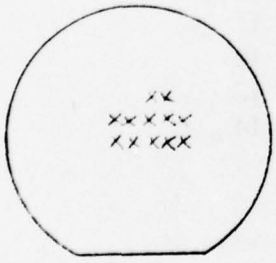
8 Circuit
Sample



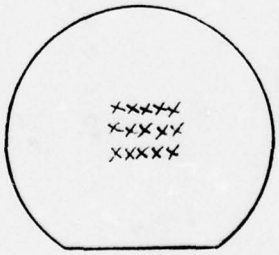
9 Circuit
Sample



10 Circuit
Sample



12 Circuit
Sample



15 Circuit
Sample

FIGURE F 3.1.1.3-2
LOCATION ON WAFER OF CIRCUITS TO BE SELECTED
FOR INDICATED SAMPLE SIZE

c) Under Developed Patterns

Patterns with photoresist still remaining in opening. Patterns will have the appearance of cobwebs running through or along the edges of openings.

d) Spiking in Photoresist

Spikes of developed areas extending from designed openings to form undesigned open patterns.

e) Poorly Developed Patterns

Irregularities in the resist such as swelling making opening smaller than design value, puckered resist showing a rippled effect, or cloudy or smudged resist.

3.1.1.3.2 Damaged Photoresist

Photoresist with voids or contamination in the form of tears or scrapes in the photoresist.

Patterns exhibiting the following conditions will be counted as defective:

a) Scratches

Any scratches in the surface of photoresist.

b) Lifting Photoresist

Any lifting or peeling photoresist.

c) Pinholes

Any pinholes in the photoresist.

d) Voids

Any voids in photoresist (this includes voids due to contamination of mask or photoresist).

3.2 FIRST OFF WAFER INSPECTION

Purpose: The purpose of this inspection is to determine mask acceptability by inspecting the first wafer aligned and exposed each time a new mask is used. This inspection is performed to the post development criteria at the post development inspection point.

3.2.1 Procedure

The first wafer aligned and exposed each time a new mask is used will be developed and inspected prior to using the mask. Based on the number of circuits on the wafer, select the number of circuits to be inspected from Table F 3.2.1-1. For the sample selected, refer to Figure F 3.2.1-2 to determine the location of the circuits to be inspected on the wafer.

Inspect each circuit in the sample with a metallurgical microscope at 100X to 200X magnification for damaged photoresist as indicated in Paragraph 3.1.1.3.2 of the post development wafer inspection. In addition, perform the alignment inspection of Paragraph 3.1.1.2 of the post development wafer inspection.

If the number of defects found in the sample exceeds the accept number in Table F 3.2.1-1 or if the alignment acceptance criteria of Paragraph 3.1.1.2 is not met, reject the mask and repeat this procedure until an acceptable mask is found. (Accept mask if defects found are considered workmanship related.)

A maximum of seven masks to wafer contacts will be allowed with each mask when contact alignment is used.

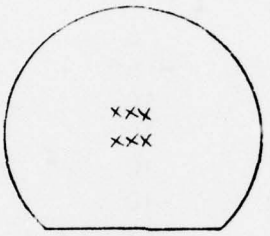
TABLE F 3.2.1-1

SAMPLING PLAN FOR FIRST OFF WAFER INSPECTION
AT POST DEVELOPMENT INSPECTION

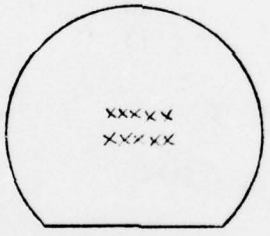
Number of Circuits per Wafer less than or equal to	Number of Circuits to Inspect	Accept Number
100	6	0
200	6	0
300	10	1
400	10	1
500	10	1
600	10	1
700	13	2
800	13	2
900	13	2
1000	13	2
1100	13	2
1200	13	2

FIGURE F 3.2.1-2

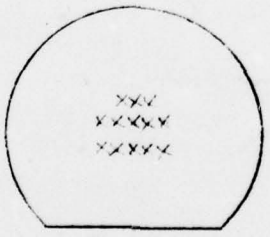
LOCATION ON WAFER OF CIRCUITS TO BE SELECTED
FOR INDICATED SAMPLE SIZE



6 Circuit
Sample



10 Circuit
Sample



13 Circuit
Sample

3.3 POST ETCH OXIDE WAFER INSPECTION

The purpose of this inspection is to lot accept each wafer run after oxide etching and photoresist stripping for batch and random circuit defects introduced at the etching and photoresist stripping operations.

3.3.1 Procedure

The inspection is a two part inspection.

- o A rough wafer inspection per Paragraph 3.3.1.1.
- o A detail wafer inspection per Paragraph 3.3.1.2.

The rough wafer inspection is a 100% wafer inspection. The detail wafer inspection is a sample lot acceptance wafer inspection.

Refer to Table F 3.3.1-1 to determine the number of wafers to be inspected. For the sample selected, refer to Figure F 3.3.1-1 to determine the location of the circuits on the wafer to be sampled for the detail wafer inspection of Paragraph 3.3.1.2. Randomly select the wafers from the lot for inspection.

3.3.1.1 Rough Wafer Inspection

Inspect each wafer from the sample selected in Paragraph 3.3.1 under an ultraviolet illuminator for the defects as described in Paragraphs 3.3.1.1.1 through 3.3.1.1.5.

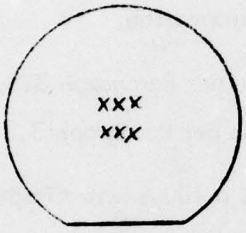
If any part of any wafer does not meet this criteria, reject the wafer and inspect all remaining wafers in the sample and in the lot.

3.3.1.1.1 Contamination

a. Residue of photoresist not fully removed from the wafers.

b. Foreign material on the wafers.

3.3.1.1.2 Streaks and Clouds



6 Circuit
Sample

FIGURE F 3.3.1-1 LOCATION ON WAFER OF CIRCUITS TO BE SELECTED FOR INDICATED SAMPLE SIZE

TABLE F 3.3.1-1

SAMPLING PLAN FOR DETAILED
POST ETCH OXIDE INSPECTION

No. of Wafers in Lot	No. of Wafers per Lot to Inspect	No. of Circuits per Wafer to Inspect	Total No. of Circuits to Inspect	Accept No. for Lot
1	1	6	6	0
2	2	6	12	1
3	3	6	18	2
4	4	6	24	4
5	5	6	30	6
6	5	6	30	6
7	5	6	30	6
8	5	6	30	6
9	5	6	30	6
10	5	6	30	6
11	5	6	30	6
12	5	6	30	6
13	6	6	36	8
14	6	6	36	8
15	6	6	36	8
16	8	6	48	11
17	8	6	48	11
18	8	6	48	11
19	8	6	48	11
20	8	6	48	11
21 to 50	10	6	60	14

3.3.1.1.3 Oxide in Openings

No oxide shall be visible in oxide opening.

3.3.1.1.4 Overetching (undercutting)

The openings must not be overetched to the extent that triple lines can be seen at the edge of the oxide opening. Other tighter criteria due to design constraints are to be imposed by the manufacturer at each masking level as required.

3.3.1.1.5 Pinholes

Any pinholes in oxide visible when viewed with a metallurgical microscope at 200X magnification minimum.

3.3.1.2 Detail Wafer Inspection

Inspect each circuit in the sample selected in Paragraph 3.3.1 with a metallurgical microscope at 100X to 200X magnification for the following defects as described in Paragraph 3.3.1.2.1 and 3.3.1.2.2.

If the number of defects found in the sample exceeds the accept number as indicated in Table F 3.3.1-1, reject the lot.

3.3.1.2.1 Oxide Inspections

(a) Contamination

1. Residue of photoresist not fully removed from the wafers.
2. Foreign material on the wafers.

(b) Streaks and Clouds

(c) Oxide in Openings - No oxide shall be visible in oxide opening.

(d) Overetching (undercutting) - The openings must not be overetched to the extent that triple lines can be seen at the edge of the oxide opening. Other tighter criteria due to design constraints are to be imposed by the manufacturer at each masking level as required.

(e) Pinholes - Any pinholes in oxide visible when viewed with a metallurgical microscope at 200X magnification minimum.

(f) Oxide Faults

1. Any oxide voids that allow bridging between oxide opening (see Figure F 3.3.1.2.1-1).
2. Any isolation opening that is discontinuous or any other opening with less than 25 percent (50 percent for resistors) of the original designed width that remains (see Figure F 3.3.1.2.1-1).

3.3.1.2.2 Glassivation Inspections

MIL-STD-883, Method 2010, Paragraph 3.1.7.

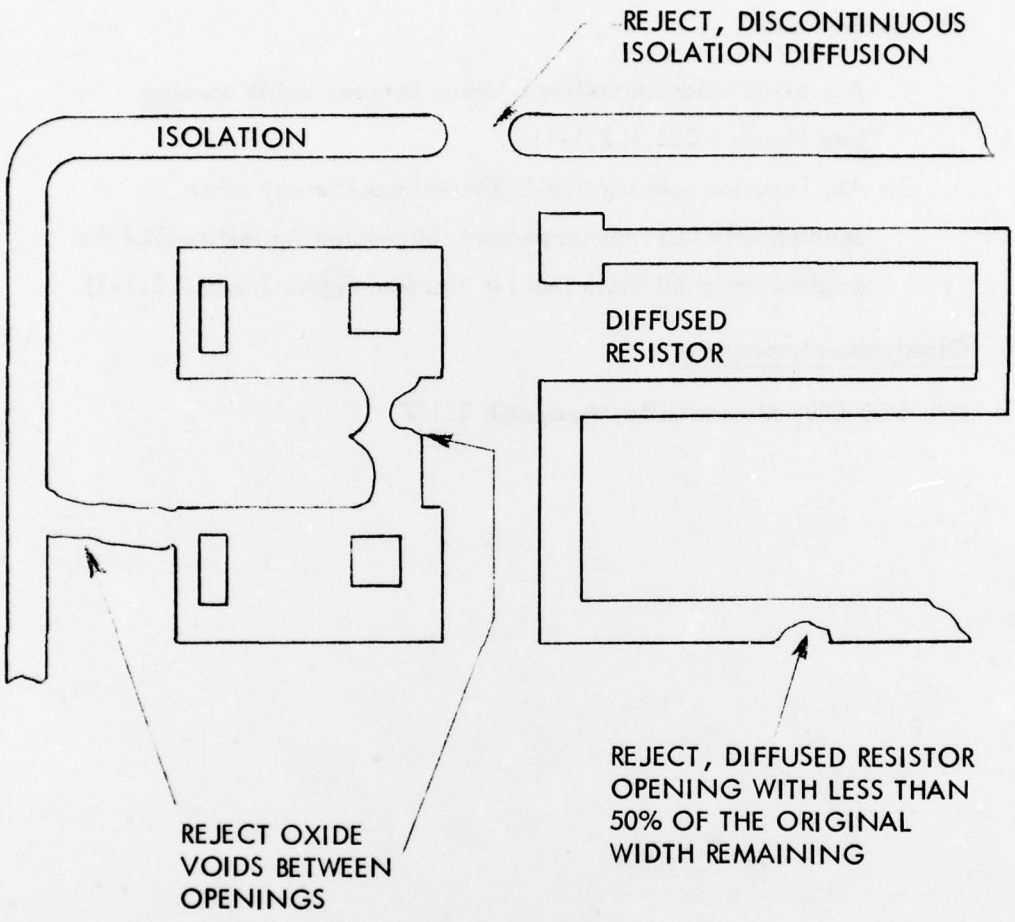


FIGURE F 3.3.1.2.1-1 OXIDE FAULTS

3.4 POST ETCH METALLIZATION WAFER INSPECTION

The purpose of this inspection is to perform wafer acceptance after metal etching and photoresist stripping for batch and random circuit defects introduced at metal deposition, metal etching and photoresist stripping operations.

3.4.1 Procedure

The inspection is a two part inspection.

- o A rough wafer inspection per Paragraph 3.4.1.1.
- o A detail wafer inspection per Paragraph 3.4.1.2.

The inspections are performed on 100% of the wafers.

Refer to Table F 3.4.1-1 to determine the number of circuits on each wafer to be inspected. For the sample selected, refer to Figure F 3.4.1-1 to determine the location of the circuits on the wafer to be sampled for the detail wafer inspection of Paragraph 3.4.1.2.

3.4.1.1 Rough Wafer Inspection

Inspect each wafer under an ultraviolet illuminator for contamination (residue of photoresist not fully removed from wafers or foreign material on wafers). If any part of any wafer does not meet this criteria, reject the wafer.

3.4.1.2 Detail Wafer Inspection

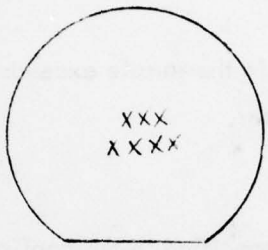
Inspect each circuit in the sample selected in Paragraph 3.4.1 with a metallurgical microscope at 100X to 200X magnification for the following defects as defined in Paragraphs 3.1.1.1, 3.1.1.2, 3.1.1.3, 3.1.1.4, 3.1.1.6, 3.1.1.7 and 3.1.6.1 (Para (b) and (c) only) of Method 2010 of MIL-STD-883A.

a. Metallization scratches
b. Metallization voids
c. Metallization corrosion
d. Metallization adherence

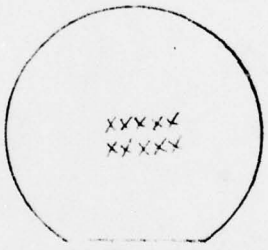
TABLE F 3.4.1-1

SAMPLING PLAN FOR
METALLIZATION INSPECTION

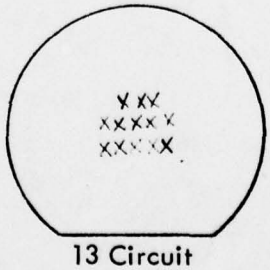
Number of Circuits per Wafer Less Than or Equal To	Number of Circuits to Inspect	Accept Number
100	7	1
200	7	1
300	10	2
400	10	2
500	10	2
600	10	2
700	13	3
800	13	3
900	13	3
1000	13	3
1100	13	3
1200	13	3



7 Circuit
Sample



10 Circuit
Sample



13 Circuit
Sample

FIGURE F 3.4.1-1 LOCATION ON WAFER OF CIRCUITS TO BE SELECTED FOR INDICATED SAMPLE SIZE

e. Metallization bridging

f. Metallization alignment

g. Foreign material

If the number of defects found in the sample exceeds the accept number as indicated in Table F 3.4.1-1, reject the wafer.

4.0 SUMMARY

The following details shall be specified in the applicable device specification.

(a) Requirements or limits if other than those in Table I.

(b) Source inspection