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FINAL REPORT

THE INFLUENCE OF CONTACT CONDITONS AND CIRCUIT ON SHORT NEGATIVE DIFFERENTIAL MOBILITY SEMICONDUCTING DEVICES.

By
H.L. GRUBIN

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The Influence of Contact Conditions and the Circuit

On Short Negative Differential Mobility Semiconducting Devices

TABLE OF CONTENTS

R78-921818-9

The Influence of Contact Conditions and the Circuit On Short Negative Differential Mobility Semiconducting Devices

SECTION I

INTRODUCTION AND PROGRAM HIGHLIGHTS

This report contains a summary of results under the U.S. Navy, Office of Naval Research Contract N00014-74-C-0237 and a proposal for additional work. We propose to continue the theoretical study of the space charge dependent and time dependent properties of nonlinear semiconducting field effect transistors (FET).

During 1977 under Contract N00014-74-C-0237 we examined theoretically the space charge dependent properties of nonlinear semiconducting FETs with particular attention given to gallium arsenide devices. Emphasis was given to determining: (1) the role of the nonlinear velocity electric field relation on the output characteristics of the FET; (2) the influence of sample dimensions on the electrical stability of the FET; and (3) the influence of the substrate on the operation of the device.

There have been many accomplishments at United Technologies Research Center under Contract N00014-74-C-0237. These accomplishments have been summarized in seven papers presented at major semiconductor device meetings; and in eight papers already published or accepted for publication. The results of two terminal devices will also appear in a monograph on the Gunn-Hilsum effect to be published by Academic Press, and in a review article, also to be published by Academic Press. A summary of these accomplishments follows.

(1) In 1974 we confirmed numerically that X-band transferred electron devices were able to sustain a permanent time dependent anode adjacent dipole layer while undergoing large signal self-excited oscillations. The anode adjacent dipole eliminated circuit control of the oscillation, placed an upper limit on the oscillation frequency, and held the minimum oscillating voltage to a value in excess of the instability threshold voltage. This type of oscillation appears to be peculiar to thin negative differential mobility devices. Thick devices do not sustain self-excited oscillations when the minimum device voltage exceeds the instability threshold voltage. Our results were reported in the paper: "Bias Dependent Oscillations in Ten Micron Long Transferred Electron Oscillators", Electronics Letters, Volume 10 (1974). The results were also discussed at the Third European Specialist Workshop on Microwave Active Semiconductor Devices, Ronneby, Sweden, (1975).

(2) Because of the interest generated by the observation that select indium phosphide two terminal devices could yield anomalously high output powers and efficiencies while exhibiting dc properties characteristic of low efficiency devices, we began a detailed study of the contact dependence of the output characteristics of short transferred electron oscillators. We used a time independent cathode field model and showed that n^+ contacts would not necessarily yield the highest output power. Rather, devices which sustained a moderate pre-instability cathode voltage drop, corresponding to an estimated cathode field slightly in excess of the NDM threshold field, were shown to yield the best performance. The results of our study were presented at the Second Annual Conference on the Physics of Compound Semiconductor Interfaces, Los Angeles, California (1975). Our results are part of the Conference Proceedings under the title: "Transferred Electron Devices with Emphasis on the Role of the Contacts - A Review," (CRC Critical Reviews in Solid State Sciences Volume 5 (1975)).

(3) Our time independent cathode field studies have demonstrated that while a fixed cathode model is able to account for a broad spectrum of GaAs device behavior and a more narrow range of InP device behavior, it is not able to explain the high efficiency InP oscillations. Investigators in Great Britain proposed that an explanation of the high efficiency InP results would emerge if instead of a fixed cathode field a fixed cathode conduction current density was assumed. In an attempt to reconcile the arbitrary features of both models we introduced a phenomenological time dependent cathode field model that included both cathode conduction current and cathode displacement current contributions. The cathode conduction current was represented analytically by the current voltage relation of an unalloyed metal-semiconductor contact and implied that the alloyed contact submits to the same description. With this more general model we were able to account for the broad spectrum of both GaAs and InP device behavior and to correlate device current voltage curves and threshold conditions with the oscillation properties. In terms of the analytical cathode conduction relation, the InP results required a thermionic emission dominated alloyed contact, whereas the GaAs devices required a tunneling dominated contact. In either case both contacts required very low barrier heights of the order of 0.2 ev. There is some evidence that the alloyed metal-semiconductor contact may be described in terms of a barrier height that is less than 0.4 ev. Our results were presented at the Third Annual Conference on the Physics of Compound Semiconductor Interfaces, San Diego, California (1976). They also appeared in the Conference Proceedings under the title: "Dynamic Cathode Contacts and Transferred Electron Semiconductors," J. Vac. Sci. & Tech., Volume 13 (1976). Another paper on this topic: "Dynamic Cathode Boundary Field and Transferred Electron Oscillators," was published in IEEE Transactions on Electron Devices Volume ED-23 (1976). A detailed study, comparing the time independent and time dependent cathode field models will appear in the IEEE Transactions on Electron Devices during 1978.

(4) In 1975 we initiated programming to determine the device physics and device circuit interaction of nonlinear field effect transistors. This program was

designed to allow numerical experiments to be performed so that the dependence of the device on the contact configuration, doping profile, sample dimensions, material properties (e.g., the velocity field relation) could be determined. The program was initially developed on a PDP-6 computer and then transferred to the faster UNIVAC 1110 computer. The program can treat two dimensional rectangular three terminal devices with almost any contact configuration. It is capable of examining substrate effects, variable doping profiles under the gate contact and between contacts, various velocity-field and diffusion-field relations, circuit effects, inductive effects, and time dependent voltages on the contacts. A portion of the program was discussed at the 1976 Summer Computer Simulation Conference, Washington, D. C. (1976). The paper appears in the Conference Proceedings under the title: "Two Dimensional Numerical Simulation of Negative Differential Mobility Semiconducting Devices."

(5) During 1977 we began a detailed study of the role the carrier dynamics, as reflected in the shape of the field dependent carrier velocity curve, has on the space charge distribution and hence the operation of the FET. We were interested in several features. For one thing, we were looking for a determination of whether the current instability that appeared in the FET simulations was a universal feature of negative differential mobility devices or whether conditions could be attained which would inhibit the appearance of the instability. We demonstrated that devices with sufficiently thin conducting channels would not support an instability; and have developed an empirically accessible criteria for classifying a device as 'thin': If the pinchoff voltage at the gate contact is approximately equal to the drain voltage at the onset of current saturation (under zero gate bias conditions) the device is 'thin'. The pinchoff voltage is the amount of gate bias necessary to reduce the drain current to negligible values. For FET devices, of the type analyzed in our simulations, pinchoff is determined mainly by geometric constraints, and current saturation by the fact that the carrier velocity has a peak value. Thus, in contrast, a 'thick' device is one whose pinchoff voltage may be considerably larger than the drain voltage at the onset of current saturation. It appears that many currently available three terminal devices fall into the category of being 'thick' devices. Also thick devices can sustain high current density levels and are capable of supporting a current instability arising from a region of negative differential mobility.

Our classification of GaAs FETs into either thick or thin channel devices draws attention to the fact that in thick devices and at high drain bias levels the electrons in the gate to drain region may be traveling at significantly different values of velocity than carriers in the source to gate region. In the former and at high values of drain potential the carriers are traveling at their saturated drift velocity value. Now generally the electron dynamics in the gate to drain region of the FET control the operation of the device. Therefore, the value of the saturated drift velocity is an extremely important parameter in the design of an FET. To corroborate this result we have begun a collaborative study with

workers at the Naval Research Laboratory. Initially the temperature dependence of the drain current will be measured, at NRL, to see if its variation is the same as the temperature dependence of the saturated drift velocity. Interpretation of the results unfortunately will not be direct as there is also evidence for the appearance of stationary dipole layers in the region between the gate and drain contacts. This evidence first made its appearance in our calculations and was summarized in Section III, Fig. 18 of last years' proposal. It was also discussed at the 'Hot Electron' Conference, the results of which will appear on its proceedings. The first substantial evidence for this dipole layer was reported experimentally in the September issue of the Proceedings of the IEEE, by workers from Fujitsu Laboratories.

The temperature dependent measurements are expected to place the saturated drift velocity as the main parameter determining the value of the saturated drain current in thick devices. If this is the case what is the role of the peak velocity? It is our conclusion that in both thick and thin devices saturation begins when at some point along the conducting path the carriers reach their peak velocity. Generally the carriers reach their peak velocity at the drain-side of the gate contact. Upon reaching their peak velocity there is usually an increase in potential under the gate contact because of the inherent instability associated with the region of negative differential mobility. In thin devices this increase in potential results in rapid saturation of the current level but no instability because the current level is too low. In thick devices if the potential drop under the gate region is within a certain range and the current level is greater than that associated with the saturated drift velocity an instability will occur. The importance of the value of the outside current level is consistent with results we have obtained with two terminal devices. On the basis of these instability conclusions for thick devices, we would like to corroborate experimentally that a current instability is an essential feature of the device itself. Now for a variety of reasons other than device thickness some FETs do not sustain a current instability. Some of the reasons include the fact that at high doping levels associated with current FETs the peak-to-valley velocity ratio is depressed. Another reason may be the placement of the gate contact - it may be too close to the drain contact. We can overcome some of the effects of the former by doing measurements at below room temperatures, where the peak-to-valley velocity ratio increases. These types of measurements will also be carried out by workers at NRL in collaboration with me.

The above set of temperature dependent measurements should be able to isolate some essential differences between the peak and saturated drift velocity values and its importance for device operation. They should also be able to confirm a number of predictions we have made under the present Navy Contract.

Because many of the features of our calculations are dependent on the fact that we are dealing with a semiconductor with a region of negative differentail mobility, we have performed calculations with nonlinear elements whose velocity saturates

but does not exhibit the NDM region. The results of this study provide an important comparison to gallium arsenide but are also of interest in themselves in that they are applicable to such semiconductor FETs as silicon. The calculations provide a significant advance over other studies with saturated drift velocity relations in that transient effects are included and the calculations are performed self-consistently. We have found that for these types of devices dipole layers form under the gate contact; but of course these layers are stable. Because of the absence of a current instability the richness of solutions available to the gallium arsenide FET is absent here. In particular, the presence of a dipole layer extending from the gate to the drain contact in gallium arsenide devices does not appear at comparable bias levels in the element without the region of negative differential mobility. Also the division of devices into categories of thick and thin is less important for devices without a region of negative differential mobility.

Most of our calculations have been performed on devices with doping levels of $10^{15}/cm^3$. This level was chosen because of computing costs. Most FETs have a nominal doping level of $10^{17}/cm^3$. We have begun a systematic effort to scale the results and have found that for the space charge equations the contribution of the diffusion current is the only term that does not scale with doping level. Indeed the effect of diffusion increases at the higher doping level. Nevertheless, in those circumstances where we have performed higher doping level calculations we find behavior qualitatively similar to the lower doping level calculations. The study has not yet been completed.

We have also begun to examine in detail the role of the substrate on the performance of the device and have found that there is a substantial amount of charge injected into the substrate. This has been reported earlier. We have sought ways to avoid this charge injection including the introduction of semi-insulating non-gallium arsenide substrates. In each case we were still left with a substantial amount of space charge injection. We have recently begun to include effects due to a heterojunction at the interface between the active region and the substrate. The heterojunction is being modeled phenomenologically rather than from first principles. Our preliminary calculations reveal the possibility through the use of the heterojunction to minimize the injection of charge into the substrate.

Some of the results discussed above were presented at four meetings: (1) "Large Signal, Bias, Circuit and Space Charge Dependent Properties of GaAs FETs" 1977 WOCSEMMAD (February 1977, New Orleans), (2) Fourth European Specialist Workshop on Active Microwave Semiconductor Devices (April 1977, Baden, Austria), (3) "Hot Electron Transport Effects in Field Effect Transistors", Hot Electron Conference (July 1977, Denton, Texas), (4) "Large Signal Numerical Simulation of Field Effect Transistors", Sixth Biennial Conference on Active Microwave Semiconductor Devices and Circuits (August 1977, Ithaca, N.Y.).

The papers presented at the Hot Electron Conference and the Sixth Biennial Conference at Cornell University will be published in the conference proceedings. These papers are incorporated as Appendix A and B of this report.

A detailed technical discussion of the current FET program and the proposed program for future work is summarized in Section II of this report.

The proposed statement of work is contained in Appendix C.

SECTION II

FIELD EFFECT TRANSISTORS: DETAILED TECHNICAL DISCUSSION AND PROPOSED PROGRAM GOALS

Introduction

The nonlinear semiconducting gallium arsenide metal-semiconductor field effect transistor has been described at the recent Cornell University Electrical Engineering Conference as "the most active area of research in the microwave device field for the past five years". The reason given for this activity is that as a low noise device over the frequency range of 4-20 GHz it demonstrates higher gain and lower noise than any other device. Secondly, as a power device the GaAs FET is similar in power but with higher gain when compared to silicon bipolar transistors over the frequency range of 4-6 GHz. It exceeds that of silicon at higher frequencies. Thirdly, it is a broadband device. In this important area of microwave device research, we have developed, under ONR sponsorship, a reliable time dependent transient simulation of nonlinear semiconducting FETs. An important aspect of the study is that the solutions are self-consistent and include the crucial influence of the external circuit.

During the present term of the ONR Contract we have emphasized three broad areas of study:

1. How does the velocity electric field relation influence the output characteristics of the device. Under which conditions may we expect an instability to occur?

2. How do sample dimensions influence the output of the device. Do the results scale with channel height, or are there qualitative differences in the time and space dependence of the space charge distribution within thick and thin channel devices. Is there a usable empirical distinction between thick and thin channel devices?

3. What effect does the substrate have on the operation of the device. Is there a significant amount of charge injection into the substrate; and if so, is there significant current flow accompanying this injected charge? How is the influence of the substrate modified when its properties are altered?

In addition to the above topics we also began a study of large signal amplification. Inductive contributions were examined and programming to study effects due to finite charge densities on the free surfaces was completed. However, from the available number of research areas associated with the FET we emphasized the three enumerated topics listed above. These we felt contained the important device physics areas that needed most current attention. In addition, because our studies have involved numerical computations at doping levels of $10^{15}/cm^3$, which is below that currently used in the fabrication of present FETs we began a study to determine if any qualitative differences in device performance occurred at the higher doping levels. This latter topic will also be discussed.

The Role of the Velocity Electric Field Relation and The Effect Of Sample Dimensions

We have grouped the first two topics, discussed in the previous paragraph, together because they are interrelated. In the past we have determined that the presence of negative differential mobility leads to nonuniform space charge distributions within the conducting channel and that these nonuniform space charge distributions could lead to a current instability. This was summarized (Ref. 1) in P76-278 submitted last year to ONR. In addition to examining the instability more carefully this year, we also determined that if the thickness of the channel height was reduced the instability could be suppressed. Some of the nomenclature to be used in the discussion below is illustrated in Fig. 1.

The first set of calculations we discuss show the interplay between the velocity-electric field curve, device operation and channel thickness. These calculations are displayed in Fig. 2 which shows steady-state and averaged drain current versus drain voltage with gate bias as a parameter. The drain voltage shown is for potential on the drain contact. All calculations in Fig. 2 are for devices with 10 micron long channel lengths and doping levels of $10^{15}/cm^3$. L_G = 1.95 microns. The channel thickness for each calculation is indicated and the gallium arsenide velocity electric field relation - scaled to current and voltage - is also shown. Closed circles correspond to steady-state time independent space charge configurations. X's denote averaged current when an instability is present. (The calculations for H_C = 3.19 microns are as yet incomplete.)

The most apparent difference between the calculations within each frame of Fig. 2 is that the drain current level for V_{GO} = 0 gets progressively bigger as the channel thickness increases. This can be explained using classical FET concepts and is based on the fact that the relative size of the depletion layer decreases as H_C

increases. The second feature that should be noticed is the absence of X's from the drain current characteristic of the thinnest device. Very simply, this means that the thinnest device does not sustain a current instability. The absence of a current instability from the thin device is consistent with two terminal results obtained by us, and others, which demonstrate that one criteria for the appearance of an instability is that the current density exceed the current associated with the saturated drift velocity values for the negative differential mobility semiconductor. This holds approximately true for the GaAs FET. Thus the absence of the instability for the thin device and its presence in thicker devices.

One may conclude from the above discussion that devices that sustain a current instability may be regarded as thick devices and those that do not are thin devices. While this is true, it is sometimes difficult to detect an instability and so another criteria must be established. If we look at the computations on Fig. 2a for the thin device we see that as the gate bias is made increasingly more negative the drain current decreases and that the gate bias needed to reduce the drain current to negligible values is approximately equal to the drain potential at the onset of saturation for zero gate bias. Indeed we have adopted this condition as one to be used for empirically classifying a device as thin or thick. It should be noted that all of the devices that fall into the gradual channel approximation of Shockley (Ref. 2) can be regarded as thin devices. However, very early (Ref. 3) in the study of gallium arsenide FETs it was determined that there was a class of devices that did not satisfy the "thin" criteria but had pinchoff voltage in significant excess of the drain voltage required for saturation. Indeed, these thick devices which are represented by Figs. 2b and 2c also have pinchoff voltages in excess of the drain voltage required for saturation.

It should be noted that the empirical determination of the difference between thick and thin devices appears to yield the same conclusion as the concept of 'thick' and 'thin' determined from the 'thickness-doping concentration' criteria (Ref. 4). The origin of the constraints obtained from our calculations and the analysis of Ref. 4 appears to be different. Ours seems to rely heavily on the fact that if the current density levels are below that associated with the saturated drift velocity of the carriers there will not be a current instability. More work should be done to reconcile the two concepts.

The calculations of Figs. 2b and 2c indicate that the instability may be suppressed at sufficiently high drain bias levels. In Ref. 1 we demonstrated that the suppression of the current instability was accompanied by the appearance of an accumulation of charge extending from the gate to the drain contact and that there was a large potential drop within the gate to drain region accompanying the charge accumulation. The first experimental observation of a time independent state following a current instability is that of Ref. 3. The first theoretical discussion of this is in a study by us to be published shortly (Ref. 5). A copy of this paper is contained in Appendix A. The properties of a high field region at

the drain contact in three terminal devices should be similar to that for two terminal devices and one manifestation should be the presence of radiation at the contact region. This has been recently reported (Ref. 6). In Ref. 6 it was also reported that the emission decreased as the gate bias was made more negative. This would tend to imply a decreasing amount of accumulated charge in the gate to drain region and an accompanying decrease in electric field across the gate to drain region. Our numerical results are consistent with these experiments.

On the basis of our numerical studies (Ref. 5) and on the experiments reported in Refs. 3 and 6, I believe we can state confidently that we are on the right track for determining the distribution of space charge within the nonlinear FET and its effect on device operation.

In connection with the unstable and stable states associated with the GaAs FET there are several additional matters to discuss. First, with regard to the instability, I would like to indicate why there are difficulties in detecting its presence. The instability in the FET, as in two terminal devices is generally characterized by a drop in current and a consequent oscillation. The drop in current in two terminal devices is determined mainly by conditions at the cathode contact and in some cases may be so small as to by insignificant. Further, in two terminal devices the latter is generally accompanied by very high values of cathode field. Typically in two terminal devices a measure of a good Gunn diode is that the average current after the current oscillation begins is significantly lower than the current level just prior to the oscillation. The latter point is also the key to simple detection in FETs. In the first place the instability generally is a result of an initial rearrangement of charge under the gate contact and a resulting transient drop in current. This is reported in Refs. 1 and 5. But the resulting average current level associated with the instability may not be significantly different than that prior to the instability. Thus curve tracer measurements of the current voltage characteristics are not likely to guarantee the detection of an instability when it occurs. But generally if we are interested in determining whether the instability is a universal occurrance in thick FETs we must look for ways to enhance its appearance. One way is to do the curve-tracer voltage measurements at a decreased temperature where the 'peak to valley' velocity ration of the carriers increases. Other techniques for direct evaluation of the transient instability in the FET is to employ directly the use of sampling scope techniques.

The second matter of interest has to do with the value of the current level at values of drain bias sufficiently high to result in the suppression of a current instability and the appearance of a gate to drain accumulation of charge. Our calculations reveal that under zero gate bias conditions there is a large potential drop in the gate to the drain region. The potential drop is sufficient to cause the carriers to be traveling at their saturated drift velocity values. Thus any current level in excess of the saturated drift velocity value would be expected to reflect the presence of a region of charge accumulation or a consequent dipole.

The question of course, is how high can the drain current level be. First, the drain current level will not exceed I_p the threshold current level for negative differential mobility. For at these current levels an instability will be expected to occur either at the source contact or again under the gate. But the current level may be expected to exceed by a significant amount the saturated drain current level. Thus, in thick channel devices the current levels under zero gate bias conditions may be expected to vary from the current level associated with the saturated drift velocity to the peak velocity current level, and that the value of the current level is a measure of the amount of charge accumulated in the gate to drain region. It is significant to point out that for thin devices in this case H_c = 1.22 microns the high drain bias current levels are not accompanied by a dipole layer in the gate to drain region.

The above discussion has emphasized some of the important results associated with the gallium arsenide FET. In discussing these results, we have displayed the stationary current and voltage points and the steady state averaged current and voltage points associated with a propagating dipole layer. We are also able to calculate the transient current voltage characteristics. This is a new calculation and is obtained by eliminating time between the current time profiles and the voltage time profiles. Figure 3 illustrates.

In Fig. 3a we plot transient drain current versus transient drain voltage for four different values of drain bias V_{DO}. The drain bias is expressed in multiples of V_p the voltage at the onset of a current instability in uniform field devices. For the ten micron long FET, V_p = 3.2 volts. The drain current and drain voltage are related by the load line equation $V_{DO}(t) = I_D R_O + V_D$. Each region of Fig. 3a is identified by the steady state value of the drain bias; but it should be pointed out that this steady state value of bias is only gradually reached. Indeed, as the bias is increased both the drain current and the drain voltage, V_D, also increase. But after the drain bias has reached its constant value the drain current and voltage still undergo time dependent changes until a steady state is reached. The steady state load lines are identified by the arrows in Fig. 3. The situation in Fig. 3 for $V_{DO} = 1.4\ V_p$ is a steady state one and corresponds to a depletion region under the gate contact. The situation for $V_{DO} = 1.5\ V_p$ results in a small damped instability and represents a small dipole layer under the gate contact. A large signal instability begins to occur at $V_{DO} = 1.6\ V_p$. Here the end points of the load line equation indicate the maxima and minima of the drain current. Increasing the drain bias results in a retention of the instability with the current minima decreasing and the current maxima increasing. In order to place these results in proper perspective we have also sketched the dc characteristics corresponding to the stationary time independent values of current and the average current associated with the instability.

Now if the semiconducting device under consideration were a two terminal device, the source current would be expected to follow the same time dependence as the drain current and the source current-drain voltage relation would be exactly the same as the drain current-drain voltage relation. The presence of the gate contact precludes this and there is consequent looping in the relationship between the source current and the drain voltage. This is also displayed in Fig. 3b. A comparison of Figs. 3a and 3b emphasizes the importance of the circuit on the measurement. In the common source configuration, which defines the circuit used in our simulations, there is no circuit originated looping in the drain branch of the circuit. There is dynamic looping in the source branch of the circuit.

More calculations of the type illustrated in Fig. 3 are anticipated in order to further characterize the transient behavior of the FET.

The above calculations have been performed on FETs whose characteristics are similar to that of gallium arsenide. We have also done calculations on devices whose velocity electric field relation indicates velocity limitation but which does not exhibit any region of negative differential mobility. The velocity electric field relation is therefore quite similar to that of the semiconductor silicon. These materials do not exhibit any current instability. And while these devices submit to a thick or thin classification the thick devices do not sustain dipole layers in the gate to drain region at bias levels comparable to that for which they first appeared in the gallium arsenide simulations. Some of the results of the zero differential mobility materials, as we refer to them, are summarized in a paper to be published shortly. This paper is contained in Appendix B of this report.

The Role of the Substrate and the Inclusion of A Simulated Heterojunction

During the past year we have begun a more earnest effort to determine the role of the substrate on the operation of the device. In our discussion last year we demonstrated that a $10^{15}/cm^3$ device sitting on an abruptly altered $10^{12}/cm^3$ substrate allowed for the presence of substantial charge injection into the substrate. We have continued some of these calculations and intend to pursue them vigorously in the future. Some of our present results are summarized below.

The substrate calculations are performed for the device geometry shown in Fig. 4, in which the source, gate and drain contacts are coplanar. The thickness of the substrate region is denoted by H_s and that of the conducting channel by H_c. For these calculations both are equal to 0.88 microns. For this active region depth the FET may be regarded as a thin device. The current voltage characteristics for this device are represented by the dashed lines in Fig. 5. The closed circles are actual stationary state computed points. The dotted lines represent the current voltage characteristic for a two terminal device with the same source and drain contacts as the three terminal device. For the two terminal device the gate contact is

absent. There are several features to be noted in the figure: (1) the resistance of the two-terminal device at drain potentials below $0.6V_p$ is less than that of the three terminal device. This is to be expected; the three terminal device introduces additional resistance due to the presence of the gate region. Also for the two terminal device there is a drop back in current at a drain potential in excess of $0.6V_p$. This drop back occurs because of the formation of a high field domain at the source contact. The high field domain forms at the edge of the source contact where the lines of current density are high. We did not examine the properties of the resulting domain, but very likely because of the thickness of the active region the carriers would redistribute themselves such that there would not be a sustained current instability. Thus for the two terminal device the transition to a high bias stationary state takes place through an unstable state. A similar situation occurs for the three terminal FET. Indeed, the first point shown in Fig. 5 for the FET is a stationary one, but takes place through a damped current instability.

It is useful at this point to illustrate the distribution of carriers, potential and current within both the active and substrate regions for the device whose current voltage characteristic is displayed in Fig. 5. The distribution is shown in Fig. 6 and is for a drain potential of $0.75V_p$. The carrier density contours are in multiples of N_0 ($=10^{15}/cm^3$); the potential contours are in multiples of V_p ($=3.2V_p$). The vector current displays lines whose value is proportional to the current density at the point in question. The direction of current flow is indicated. Also, the horizontal line on both the carrier density and the vector current density displays denotes the separation of the active region from the substrate. The inset to the figure is a sketch of the velocity electric field curve for the substrate. For the calculation of Figs. 5 and 6 the velocity relation is identical to that of the active region.

The results of the calculation indicate a substantial charge injection into the substrate and an accompanying significant current flow into the substrate. Indeed the current density under the gate is approximately equally shared by the active region and the substrate. Also we note that most of the potential drop occurs under the gate contact, where it is large enough to cause the electric field to exceed the threshold field for negative differential mobility.

It is useful at this point to digress and compare the substrate calculations for the planar FET with the thin device of Fig. 2a. First, with regard to the current voltage characteristics there is not a substantial difference between that of Fig. 2a and that of Fig. 5. The current levels are about the same and they both do not sustain a current instability. The presence of charge injection for the substrated 'thin' device does not seem to offer any advantages or disadvantages. There may however be differences in the space charge distribution, and these may affect the details of the time dependent operation. To illustrate, Fig. 7 shows the charge, potential and current distribution for the parallel contact device of

Fig. 2a at a level of drain potential comparable to that of Fig. 6. For Fig. 7 the drain potential is equal to $0.72V_p$. At the bottom of the conducting channel there is a region of charge accumulation. For the substrated device there is no apparent charge accumulation at this drain potential level. It is as though the presence of the substrate allows for a smearing of the total charge and a reduction in its value.

But the presence of a dipole layer is not precluded by the presence of a substrate. This is displayed in Fig. 8 for the device configuration of Fig. 4. In this case the drain potential is $2.7V_p$ and there is a dipole layer at the interface between the active region and the substrate. There is also a considerable amount of current flowing into the substrate under the gate region.

Figure 9 illustrates the situation when a negative bias equal to $-0.3V_p$ is applied to the gate. The potential on the drain contact is equal to $2.9V_p$. We see the presence of charge injected into the substrate. In fact the amount of charge injected into the substrate exceeds the amount of charge within the active region of the element. One also notes that there is very little current flowing in the n-region, most of it is in the substrate.

Another important point to note from the above is that the large potential drop under the gate region, forces the carriers to travel at their saturated drift velocity values.

The above substrate discussion has been for the case where the carrier velocity versus electric field relation for the substrate was the same as that of the higher doped region. We have also done calculations for the situation where the carrier velocity electric field relation is different. Figure 10 illustrates the situation where the carrier velocity does not exhibit any negative differential mobility, but instead saturates. We have taken the saturated drift velocity to be approximately one-half of that of gallium arsenide. The situation this might represent is that of a gallium arsenide material sitting on top of a gallium aluminum arsenide substrate. Majerfeld, at the recent Cornell meeting (Ref. 6) indicated, on the basis of band structure calculations, the amounts of gallium, aluminum and arsenic that would be necessary for such a velocity field relation to occur. Interest in this material as a substrate material is high because of reduced difficulties associated with lattice matching.

In Fig. 10 we display the carrier density, potential and current density distribution for a drain potential of $3.9V_p$ and a gate potential of $-0.3V_p$. While there is still charge injection into the substrate a greater fraction of current is flowing in the higher doped region that we would expect if the substrate had a higher value for the saturated drift velocity.

The above calculations have shown that the presence of a lower doped substrate allows for charge injection into the substrate. Since in the design of a given device we would like the option of deciding whether or not we want charge

injection we ask about the possibilities of minimizing it. We have displayed results in which there is no charge injection, as in Figs. 2 and 3. This situation is physically realizable in a variety of ways. In one case the results are directly applicable to a four terminal device in which the gate contact is symmetrically placed on the top and bottom of the device. This type of device was first discussed by Shockley (Ref. 2). One might also envision the situation in which a three terminal device is sitting on top of a reverse bias p-type substrate so that a PN junction forms at the bottom of the device. We have attempted to simulate the effect of a junction at the interface between the high and low doped regions of the three terminal device, by providing the junction with a well defined current voltage relationship. The current voltage at the interface may be that of a reverse bias PN junction or heterojunction. We have performed only one type of simulation to see if the program was capable of handling the presence of such a voltage dependent junction. It is, and Fig. 11 illustrates. For this calculation the gate potential is $-0.3V_p$ and the drain potential is $1.9V_p$.

The junction calculation of Fig. 11 is for a substrate whose doping level is $10^{12}/cm^3$ and before. The velocity electric field relation is approximately that of gallium arsenide and is indicated in the inset to the figure. At the interface between the higher doped and lower doped region the current voltage relation is arbitrarily specified. We require that the normal component of current into the substrate be zero.

Once the calculations of Fig. 11 are compared to the other substrate calculations it becomes clear that a dramatic change has occurred. There appears to be no injected charge into the substrate. Actually there is some, but it is just below the 25 percent level associated with the first carrier density contour. More significantly there is virtually no current flow through the substrate. Any current flow through the substrate would be expected to result from the motion of carriers that diffused across the interface between the low and high doped materials.

The above discussion summarizes where we stand with regard to determining the effect of the substrate on the operation of the device. At this point with the absence of the junction, the gross features of thin devices do not seem to be altered by the presence of the substrate, although it is clear that the space charge distribution is considerably different for the two. But we emphasize, these calculations are for devices whose active region must fall into the classification of being thin. For the case of thick devices sitting on top of a substrate the presence of the substrate is expected to have a more dramatic effect. For one thing, instabilities initiated within the active region may propagate into the substrate, and thereby alter the property of the device. These matters must be investigated.

The Role of Doping Level on the Operation of the Device

The calculations we have performed on FETs have been for a background doping level of $10^{15}/cm^3$. While three terminal structures have doping levels varying from 10^{15} to values somewhat greater than $2x10^{17}/cm^3$, most current device grade

microwave FETs have active region levels at the higher end. Our choice of $10^{15}/cm^3$ as the background doping level was predicated on cost. But our confidence in the qualitative applicability of the calculations with respect to the higher doping levels lies in the qualitative agreement of our results with published experimental data. It should be noted that most higher doping level calculations are based upon analytical models that neglect the influence of diffusion. As we will demonstrate the relative contribution of the diffusion current increases at the higher doping and so its neglect must be regarded cautiously. Further the higher doped calculations do not include large signal time dependence.

One of the first questions that one should ask is do we lose negative differential mobility at the higher doping level devices. According to the calculations of Ruch and Fawcett, shown in Fig. 12, there is a reduction in the amount of negative differential mobility, but it is still present. More recent calculations by others tend to confirm this result. Thus if negative differential mobility is still present what is the affect of a change in the background doping level? To examine this we have subjected the governing space charge dependent equations to a normalization.

The normalized variables are displayed in Table 1 and the resulting normalized equations are displayed in Table 2. One important result is expressed in the right hand column of Table 2. Here in terms of the normalized units, Poissons equation, the equation of continuity and the equation of total current are <u>all independent of carrier density</u>. Thus as far as these equations are concerned, the equations can be scaled. The equation of carrier transport however, depends <u>explicitly</u> on carrier concentration through the dielectric relaxation time. Indeed the contribution of diffusion increases at the higher levels.

The second point to note is that all of the differential equations on Table 2 require specification of <u>boundary conditions</u> and these boundary conditions are at the ends of the device. But since we have normalized the distance variable x, we must also normalize the length of the device. The normalized length of the device depends on the background carrier concentration, and effectively increases linearly with N_0. <u>Thus the normalized two-dimensional area of the FET increases</u> as N_0^2. This is illustrated in Fig. 13.

What, therefore, are some of the effects we might expect from going to higher doping levels. <u>First</u>, if we had two devices of different doping level but comparable device dimensions, the effective size of the domain would be smaller in the higher doped device at similar bias levels. <u>Second</u>, a device that was considered to be a stable 'thin' device at the lower doping level, might be regarded as a 'thick' device at a higher doping level. Also, we have been able to show that at both 10^{16} and 10^{17} a dipole layer forms and is capable of propagating. The result for $10^{16}/cm^3$ is displayed in Fig. 14. The effect of diffusion we have found is to smear out the dipole layer, but as the calculations indicate it is not sufficient to eliminate the dipole layer.

The propagating dipole layer at higher doping levels will illustrate the effect of doping level on computer costs. The normalization we use is a natural one in that the resulting differential equations, with the exception of the carrier transport equation, are independent of N_0. For the most part, we use this normalization scheme in our numerical computations. The principle cost factor lies in analyzing the details of the recycling dipole layer and this is because time is normalized to the dielectric relaxation time of the semiconductor. Thus, if we imagine that a dipole layer will propagate a distance of ten microns in 100 ps; in normalized units @$10^{15}/cm^3$, it will take approximately 100 normalized seconds. At $10^{16}/cm^3$, it will take approximately 1000 normalized seconds. One may tend to look upon this normalization as inefficient, but it is not; for it recognizes that the response of the carriers is dependent on the doping level and allows for an efficient resolution of the response. We should point out, that with regard to cost, if we are going from one steady state distribution to a second one, without any intermediate current instability (as manifested in a propagating dipole) we have not found any substantial increase in computer costs.

Summary and Future Programs

Some of the results discussed above were briefly discussed in a proposal submitted in 1976. The brief 1976 discussion was intended to provide an indication of the direction of the program. During 1977 we have begun to fill in the details of the results, and as they have appeared we have reported them. In this manner we have reported our current results at four international meetings and they will appear in two publications. The future programs we would like to maintain are extensions of the present one. We intend to:

1. Continue to detail the difference between the operation of thick and thin three terminal devices. It is necessary here to map out the properties of the stable high drain bias dipole layer in the gate to drain region of the thick device.

2. Our substrate studies are beginning to become fruitful in that we are beginning to understand the influence of the substrate on the operation of the device. We will continue this study in the coming year. Also, we intend to pursue the effects of a junction at the interface between the high and low doped regions to see if it is desirable to prevent charge from being injected into the substrate. In this connection the study of junctions at the interface will include the presence of a heterojunction which will be modeled phenomenologically. Also a variety of different semiconductor substrate materials will be simulated.

3. The scaling problems will be pursued vigorously. While our studies indicate that instabilities will occur in materials doped to 10^{17} it is as yet not clear what the full range of the instability will be.

4. In all of these studies we will compare the results obtained for gallium arsenide with other materials that either do, or do not possess a region of negative differential mobility. This comparison will highlight the role of negative differential mobility on device operation. Materials to be considered are InP and GaAlAs.

5. Our program has incorporated the effects of the external circuit. However, because of a revised set of priorities in the study of the three terminal device we have not throughly explored the realm of possibility of device operation afforded by varying the circuit parameters. Also, we have not examined in detail the effects of large signal operation of the amplication characteristics of the device. Some studies will be performed which will begin to map out these effects.

The above topics of discussion fall naturally within the framework of our present program and only an incidental amount of new programming is required to achieve the above objectives. This programming is essentially coupled to the examination of the junction at the substrate interface on the operation of the device. However, we would like to initiate a major extension to our program that would enable us to study the device physics of metal-oxide-semiconductor-field-effect-transistors. These devices are generally referred to as MOSFETs and the oxide, in this acronym, is generally placed under the gate contact. There are a variety of MOSFET configurations, two of which are shown in Figs. 15 and 16. A specific discussion of each configuration will provide an understanding of why the MOSFET device may be an important electronic tool.

Figure 15 shows a classical MOSFET often referred to as a p-type MOSFET. Generally, this type of device usually employs silicon as the principal semiconductor. The figure shows the presence of an oxide film sitting on top of a p-type doped region. There are also two n-type diffused regions. Now initially with no bias applied at any of the terminals we have two back to back pn junctions. If a bias is applied to the gate, but one that is positive with respect to the p-region, an electric field will point into the substrate causing holes to migrate toward the bottom of the device resulting in a p-type depletion region near the oxide interface. Minority carriers, (electrons) being of opposite sign move toward the interface creating an inversion layer. These mobile carriers are now available for conduction and, when a bias is applied to the drain contact, will result in the flow of current. Thus the migration of minority carriers to the region near the oxide opens up a conduction channel. Unlike most currently fabricated MESFETs this p-type MOSFET normally does not have any current flowing under zero gate bias conditions. Because of its low current levels it is a strong candidate for digital integrated circuits.

Now what are some of the interesting features associated with this device? For one thing, the application of a gate bias does not automatically result in current flowing between the source and drain contact. Generally, there are surface states at the oxide interface and the minority carriers may be expected to fill the surface states before a conducting channel is formed. In our existing program for unipolar conduction we have completed programming for the incorporation of surface

state contributions to device operation. This would have to be expanded to incorporate p-type material. The second interesting feature of a MOSFET program has to do with the fact that most p-type devices are fabricated from the material silicon. Very little is done with the material gallium arsenide. So a natural question is what does the role of negative differential mobility have to do with the operation of MOSFETs?

The programming for p-type MOSFETs, because it involves hole conduction is more ambitious than that for unipolar conduction, the type associated with MESFETs. Poissons equations must now be expanded to include electrons and holes; to the equation of carrier transport for electrons, we must add one for holes. Also the equation of current continuity must include that for holes. Expressions for generation and recombination must also be included. A typical set of MOSFET equations is shown in Table 3.

Because of the possibility of a native oxide to gallium arsenide there is also under study so-called n-type MOSFETs. Figure 16 depicts this device. Essentially this is an n-type device and could well be simulated within the confines of our present program in that the oxide has the effect of behaving as a semi-insulating region. We have already done calculations with this configuration. n-type MOSFETs have the advantage of low leakage currents.

In proceeding with the new program to include holes as well as electrons our first goal will be to see if it can be done. On the basis of our success with unipolar conduction and with the fact that bipolar conduction has been simulated in IMPATT diodels we are confident of success in this matter. Upon completion of the program and demonstrating its feasibility we will have a transient simulation available for the modeling of MOSFETs. We do not intend to get into fundamental problems associated with the limit of intervalley transfer, nor would we be seeking fundamental limitations on device size. Rather our intention will be to develop physical insight into the operation of minority carrier devices. Also upon completion of the program, we would have obtained a far more realistic semiconductor device modeling program; which in fact, would allow us to examine more realistically junction field effect transitors as well as breakdown contributions.

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FIGURE CAPTIONS

1. Device and circuit configuration for an FET with parallel source and drain contacts. The drain potential V_D and the gate potential V_G are related to the drain and gate bias values V_{DO} and V_{GO} through a load line equation.

2. Drain current versus drain potential for the device circuit configuration of Fig. 2. Device dimensions differ only in the value of the channel thickness H_C. Also L_G = 1.95 microns. Drain current is in multiples of I_P, the peak conduction current of the carriers. Drain potential is in units of V_p, the potential at I_P for a uniform space charge device. For a 10 micron long device V_p = 3.2 volts. Drain current versus drain potential are parameterized by the value of gate bias V_{GO}, expressed in multiples of V_p. Also shown is the drift velocity versus electric field curve, scaled to current and voltage, used in the calculation.

3. Transient current versus voltage for different values of drain bias, V_{DO}. L_G = 0.98 microns, H_C = 3.19 microns, and L = 10 microns. (a) Drain current versus drain voltage. Dashed curve connects stationary time independent points (closed circles) and average time dependent points (X's). (b) Source current versus drain voltage.

4. Device circuit configuration for a coplanar FET. Substrate calculations are performed for this geometry. H_C denotes the thickness of the active region and H_S the thickness of the substrate. The channel length is 10 microns. The doping within H_C is uniform and equal to $10^{15}/cm^3$. The doping within H_S is uniform and equal to $10^{12}/cm^3$.

5. Drain current versus drain potential for the configuration of Fig. 4. Closed circles denote stationary time independent points; X's denote unstable points. Dots connect current versus voltage points for a <u>two terminal</u> device in which there is no gate contact (i.e., L_G = 0.0). Dashes connect current versus voltage for a <u>three terminal</u> device. The three terminal curves are parameterized by the value of the gate bias V_{GO}, expressed in multiples of V_p. Device parameters for the three terminal device are as for Fig. 4 with L_G = 1.6 microns.

6. Contours of constant carrier density (in multiples of $N_O = 10^{15}/cm^3$); contours of constant potential (in multiples of V_p = 3.2 volts); vector current density distribution. Vector lines are proportional to current density and the distance between centers of points is equal to $N_O e v_p$, where v_p is the peak carrier velocity. Dashed horizontal lines denote separation of the active region from the substrate. Inset displays the substrate v(E) relation. For this calculation $V_{DO} = V_p$ and V_{GO} = 0.0.

FIGURE CAPTIONS (Cont'd)

7. As in Fig. 6 but for the configuration of Fig. 1 with the parameters of Fig. 2a. For this calculation $V_{DO} = V_p$ and $V_{GO} = 0.0$.

8. As in Fig. 6 but with $V_{DO} = 3V_p$.

9. As in Fig. 8 but with $V_{GO} = -0.3V_p$.

10. As in Fig. 6 but with $V_{DO} = 4V_p$ and $V_{GO} = -0.3V_p$. There is a new substrate whose properties are identified by the v(E) curve in the inset.

11. As in Fig. 6 but with $V_{DO} = 3V_p$ and $V_{GO} = -0.3V_p$. Also there is a new substrate identified by a new v(E) curve and a junction, discussed in the text. L_G = 1.95 microns and $H_C = H_S$ = 1.12 microns.

12. GaAs drift velocity versus electric field as a function of N_0. From Ref. 9.

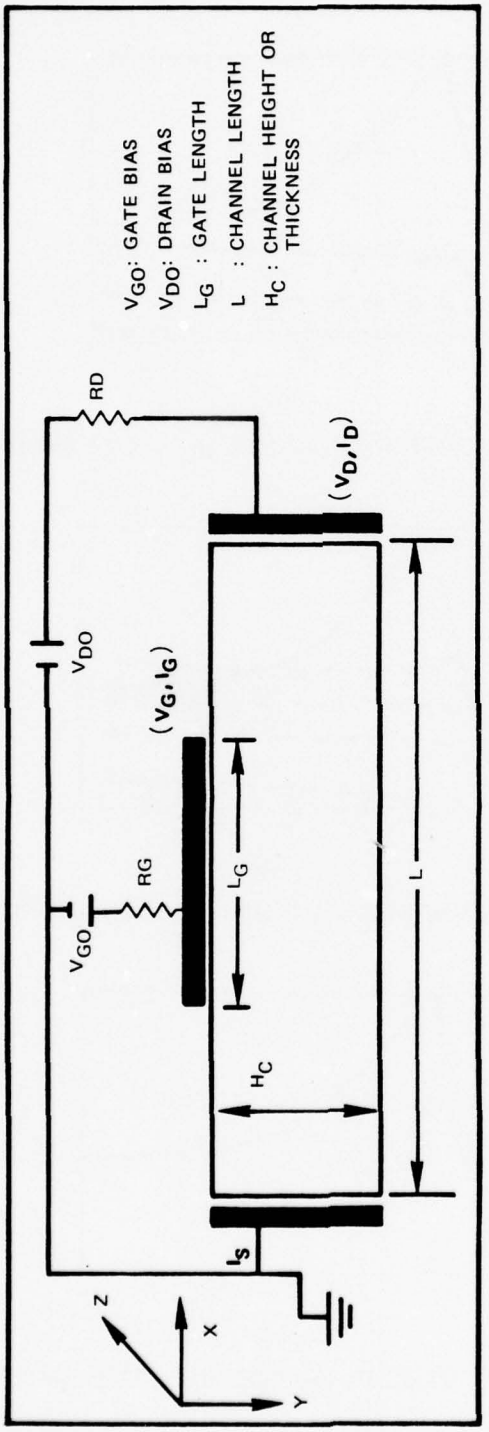
13. Scaling and device dimension for two different values of N_0 with $N_{0_2} > N_{0_1}$.

14. Dipole propagation for $N_0 = 10^{16}/cm^3$.

15. p-type MOSFET.

16. n-type MOSFET.

FIG. 1



DEVICE AND CIRCUIT CONFIGURATION

3

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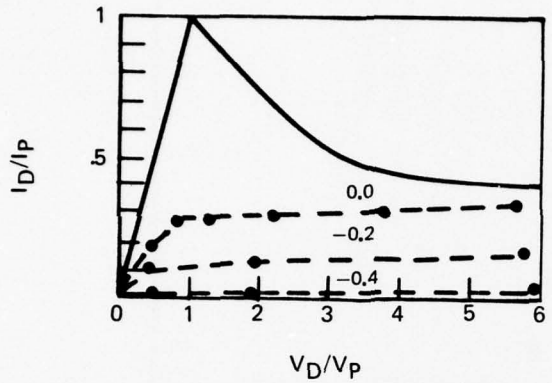
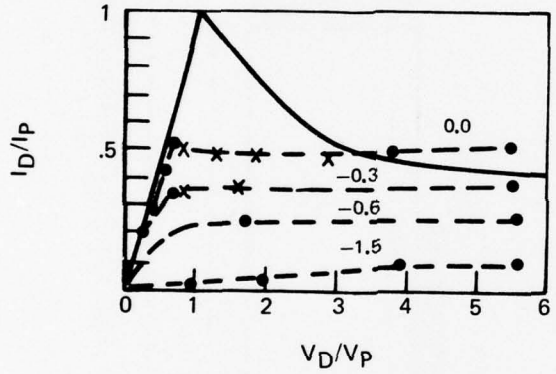
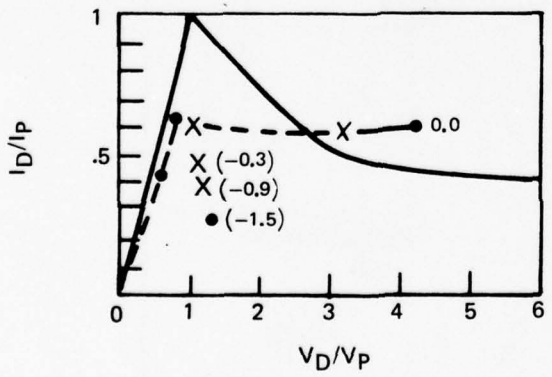


2a. I_D VERSUS V_D FOR H_C = 1.22 MICRONS



2b. I_D VERSUS V_D FOR H_C = 2.24 MICRONS



2c. I_D VERSUS V_D FOR H_C = 3.19 MICRONS

FIG. 3

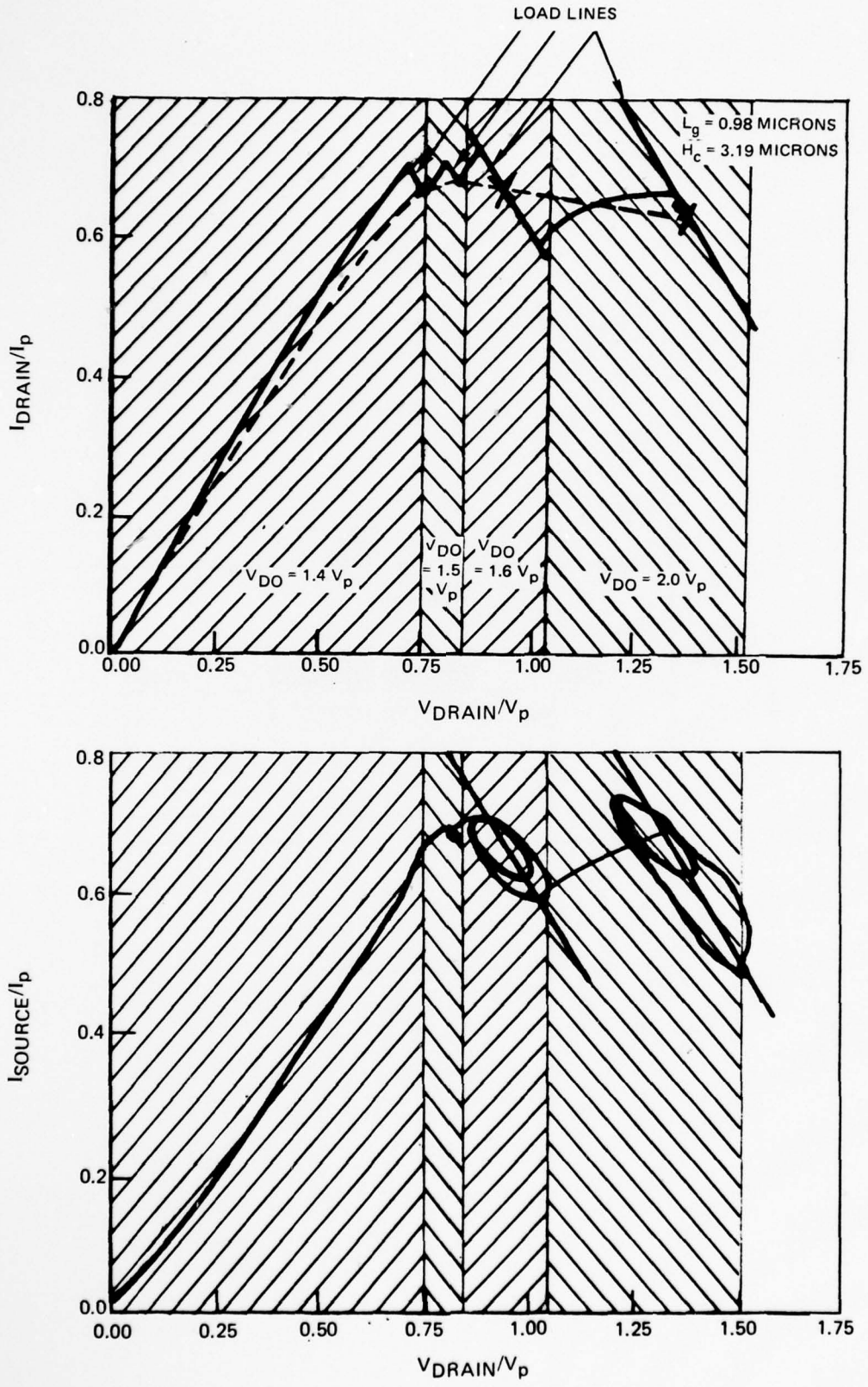


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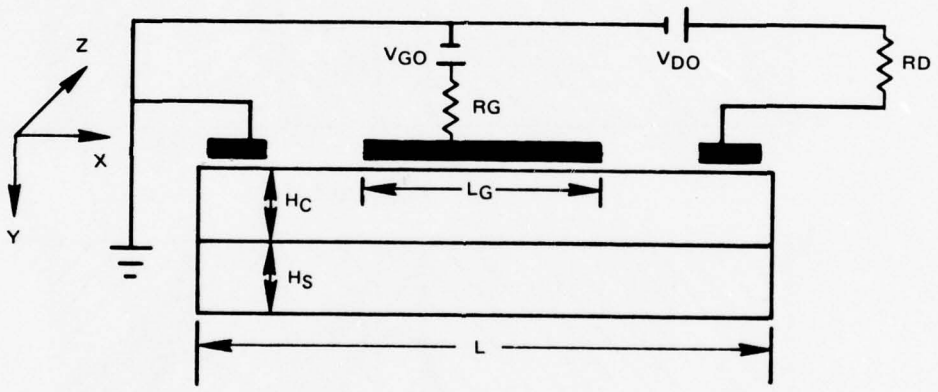
FIG. 4



$H_S = H_C = 0.88$ microns

$L_G = 1.6$ microns

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FIG. 5

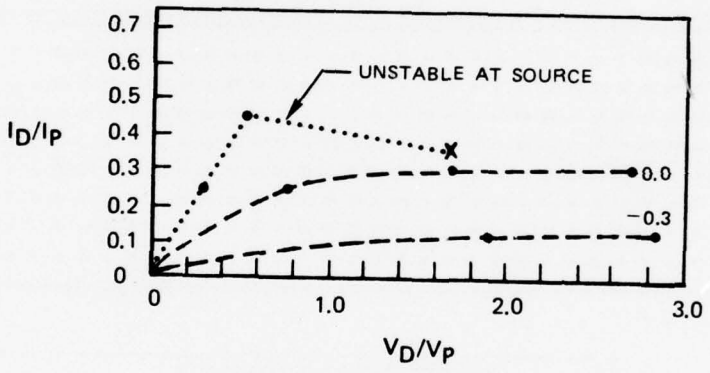

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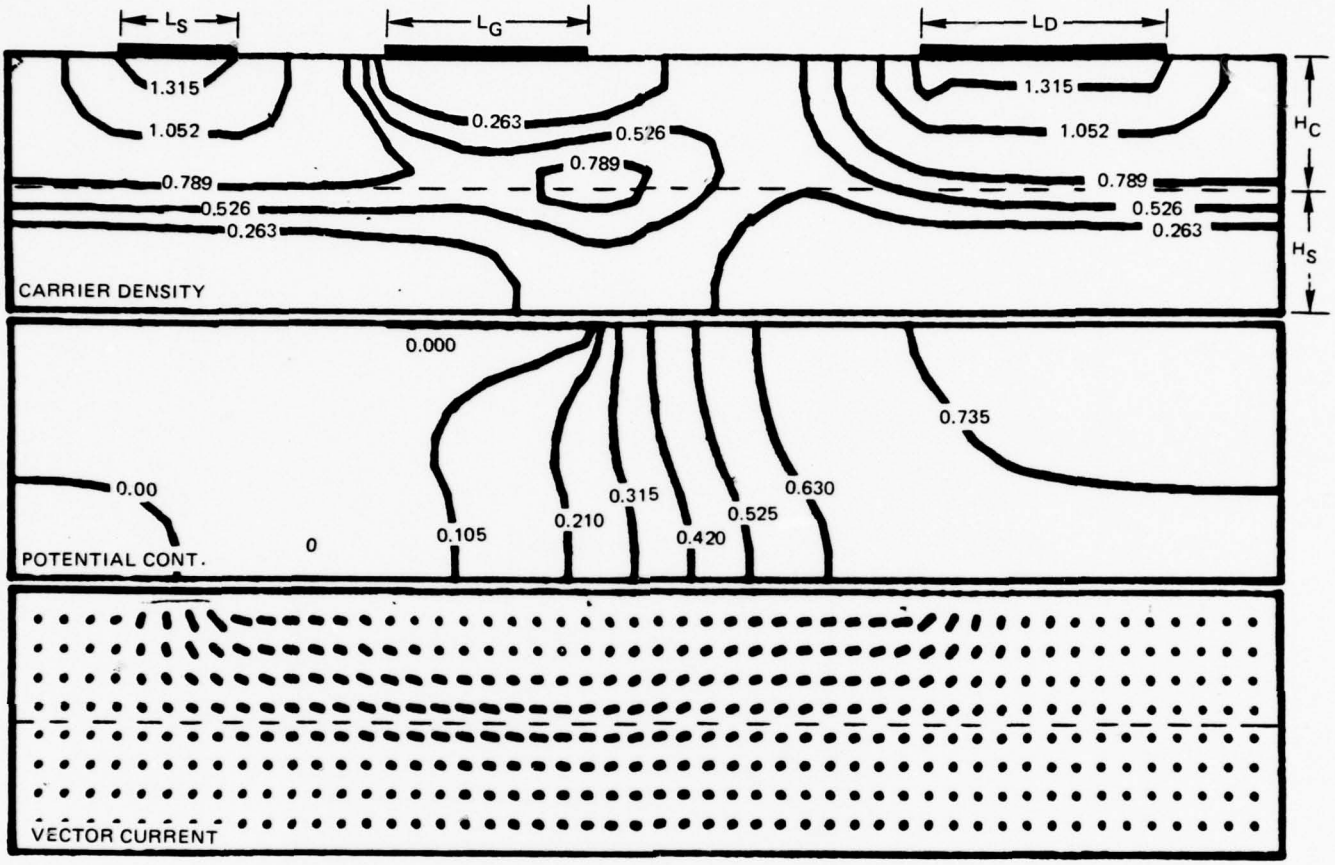
FIG. 6



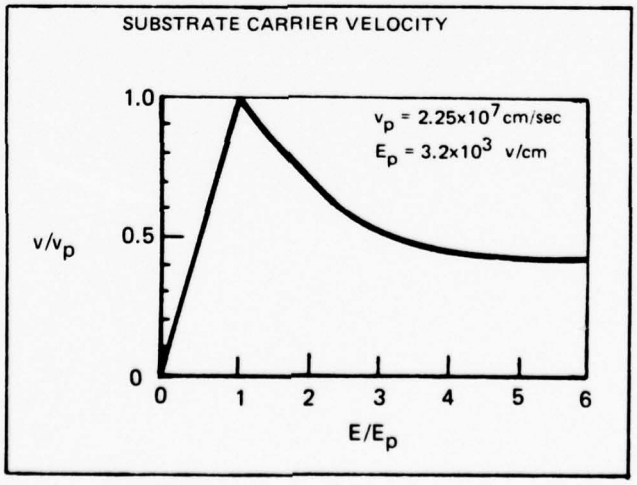


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FIG. 7

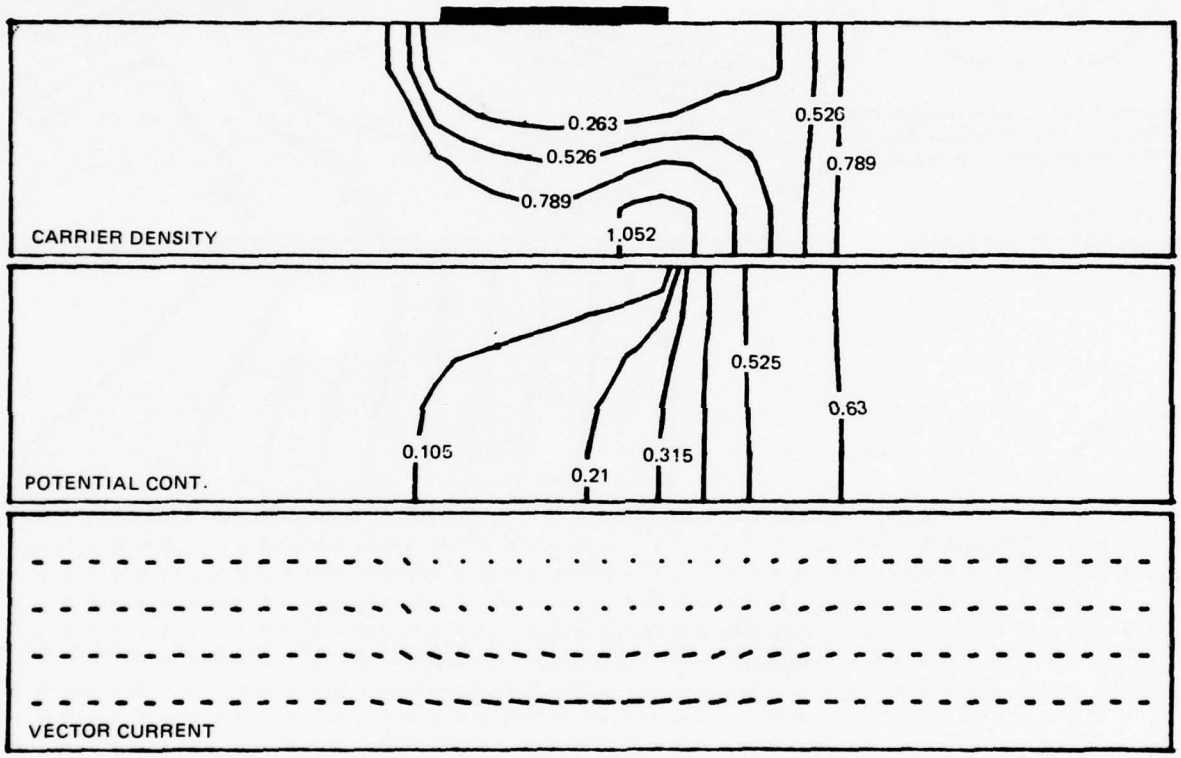

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FIG. 8

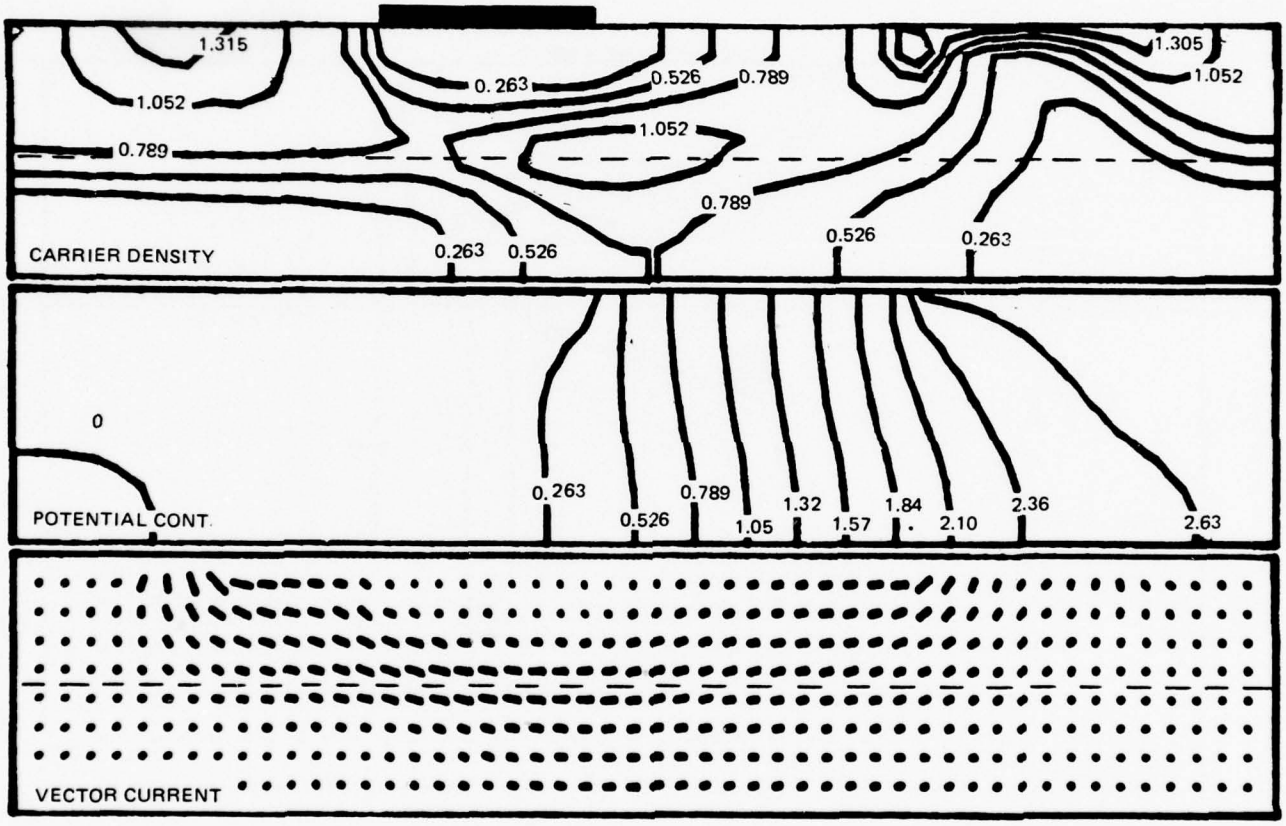

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FIG. 9

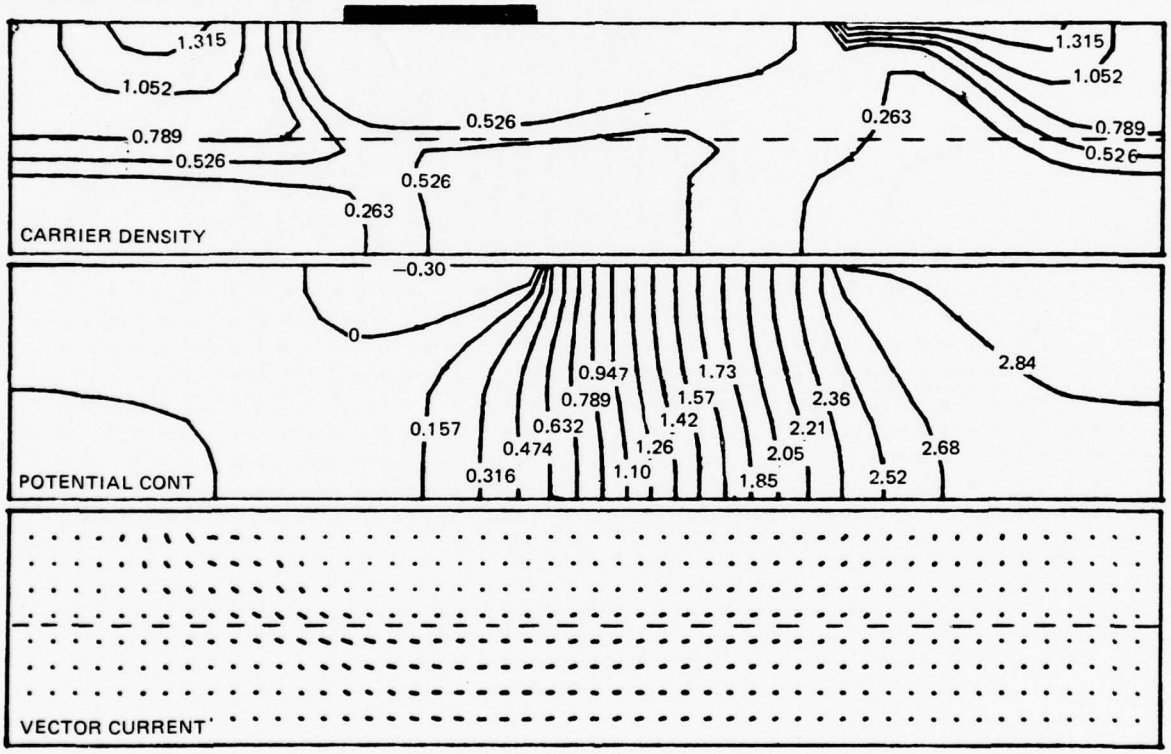

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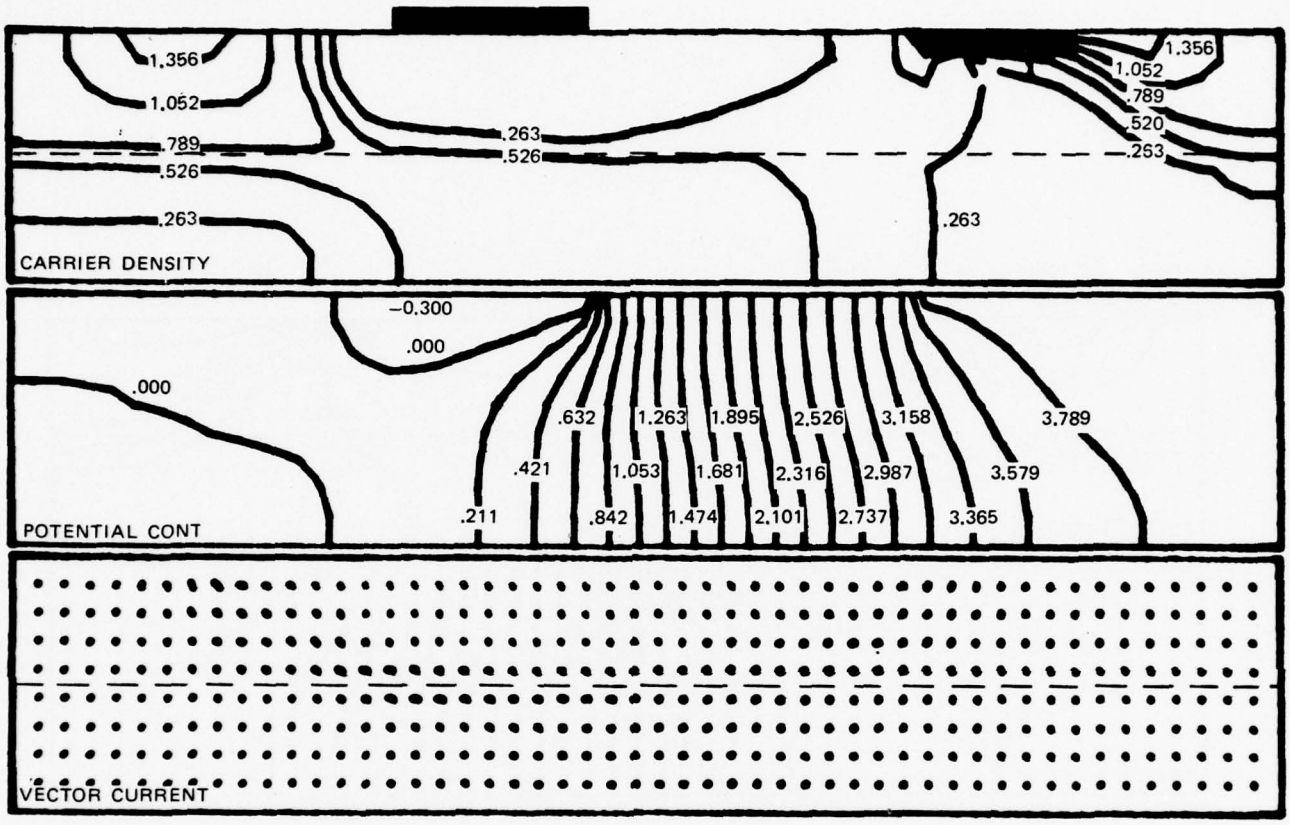
FIG. 10



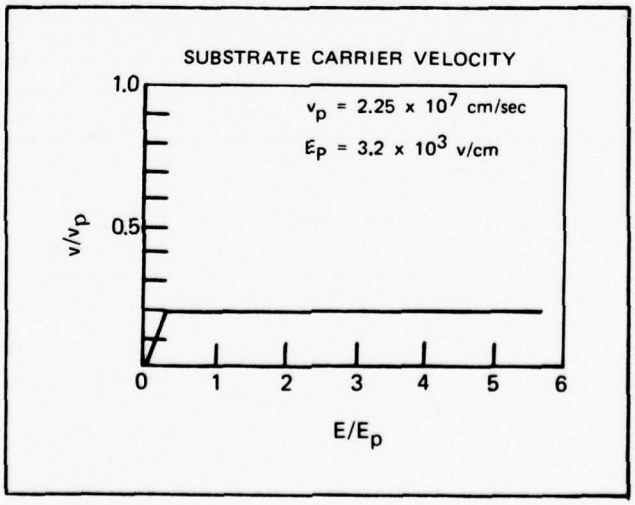


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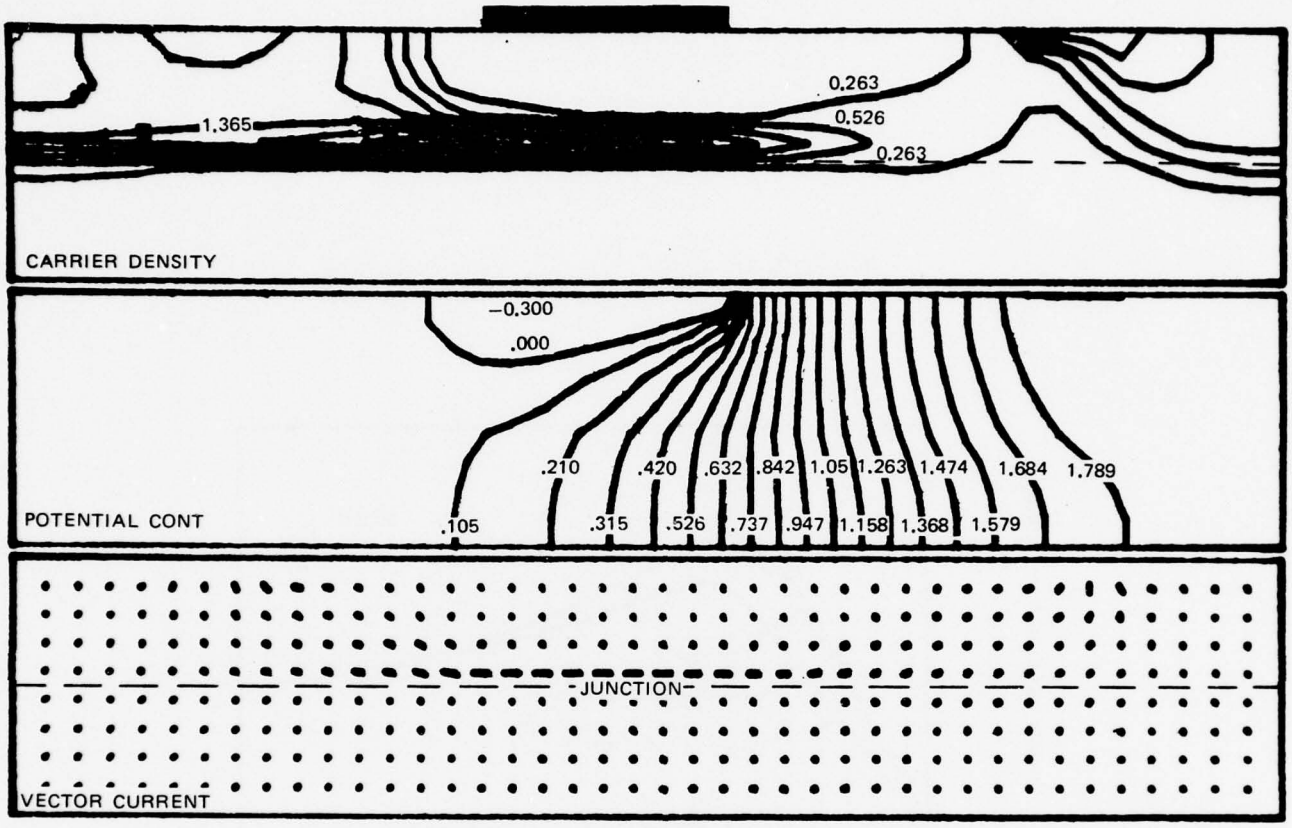
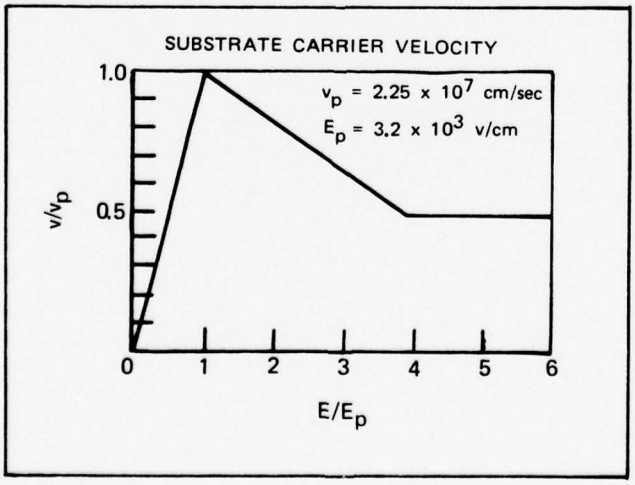
FIG. 11





13

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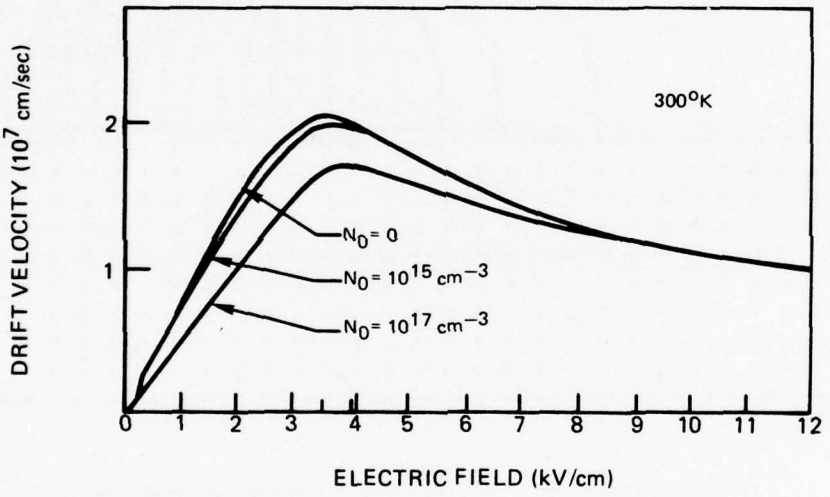
FIG. 12



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SCALING AND DEVICE DIMENSIONS

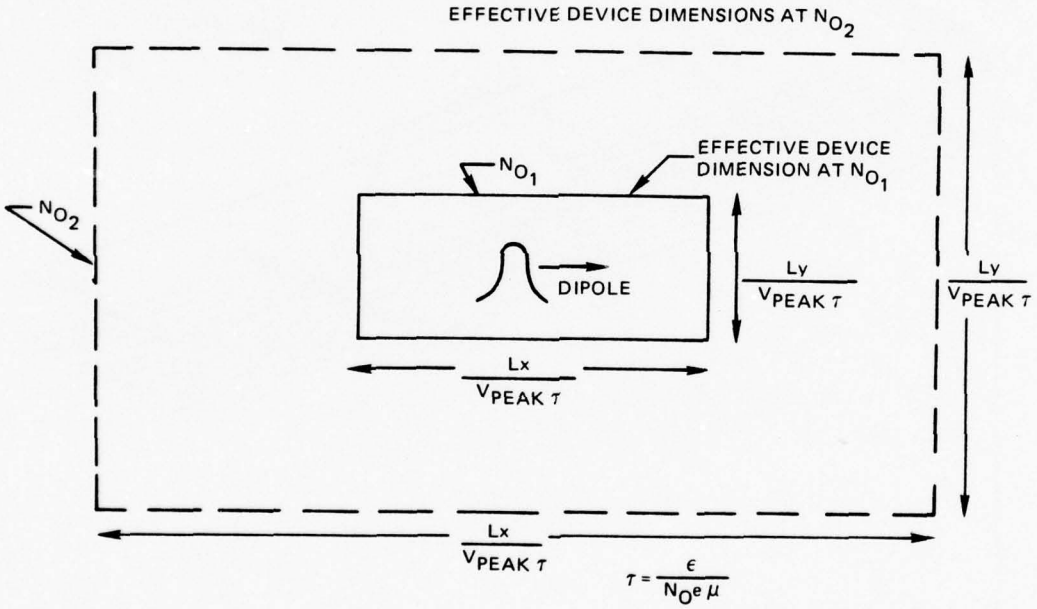

FIG. 14

DIPOLE PROPAGATION

CARRIER DENSITY

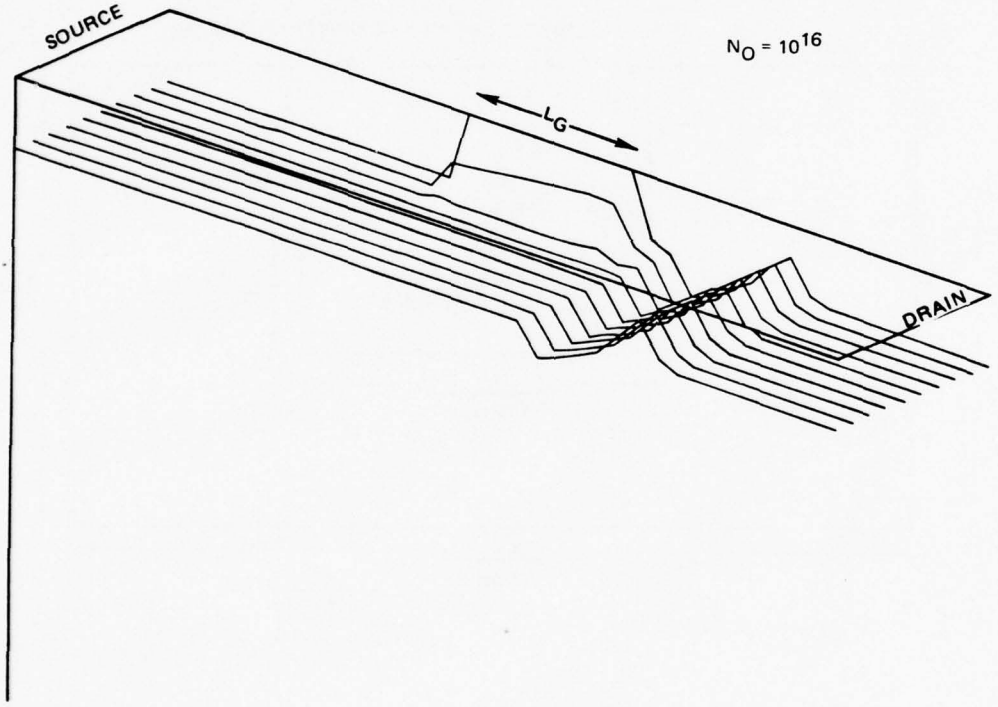

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FIG. 15

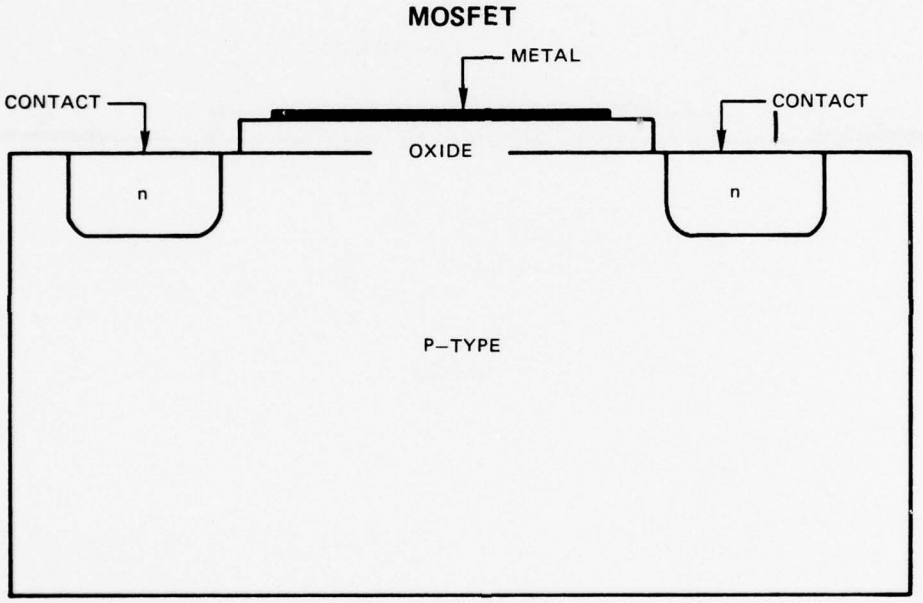

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FIG. 16

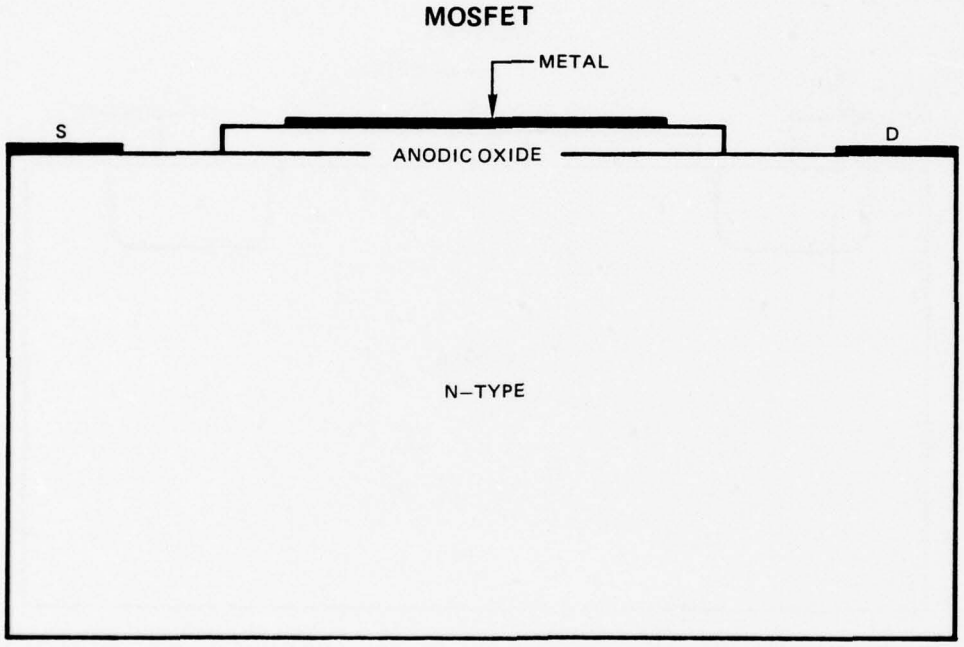

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TABLE I
SCALED FET VARIABLES

Variable	Ordinary units	Normalized units
Distance	x (cm.)	$x' = x/v_p\tau$ **
Time	t (sec.)	$t' = t/\tau$
Potential	V (volts)	$\phi = V/(E_p v_p \tau)$ **
Carrier density	N (particles/cm^3)	$n = N/N_0$ **
Electric field	E (volts/cm)	$\mathcal{E} = E/E_p$
Current density	J (amps/cm^2)	$j = J/N_0 e v_p$
Velocity	v (cm/sec)	$\vartheta = v/v_p$

** v_p is the peak carrier velocity of the electrons, typically 2.2×10^7cm/sec at $10^{15}/cm^3$ doping. E_p is the electric field at v_p and is equal to 3.2kv/cm at $10^{15}/cm^3$. τ is the low field dielectric relaxation time and is equal to 0.9ps at $10^{15}/cm^3$. N_0 is the background doping level.

TABLE II
SCALED FET EQUATIONS

Equation	Ordinary units	Normalized units
Poissons	$\nabla_x^2 V = e(N-N_O)/\epsilon$	$\nabla_{x'}^2 \phi = n - l$
Continuity	$\mathrm{div}_x J = \frac{e\partial(N-N_O)}{\partial t}$	$\mathrm{div}_{x'} j = \frac{\partial(n-l)}{\partial t'}$
Total current	$-I = J + \epsilon \frac{\partial E}{\partial t}$	$-i = j + \frac{\partial \mathcal{E}}{\partial t'}$
Carrier transport	$J = -Nev + eD\,\mathrm{grad}_x N$	$j = -n\vartheta + \left(\frac{D}{v_p^2 \tau}\right) \mathrm{grad}_{x'} n$

TABLE III
MOSFET EQUATIONS

Poissons equation:

$$\nabla^2 V = \frac{-e}{\epsilon}\left[(P-N) + (N_O - P_O)\right]$$

(Donors: N_O; Acceptors: P_O)

Carrier transport

$$J_N = -Nev_N + eD_N \text{grad} N \qquad \text{(Electrons)}$$

$$J_P = Pev_P - eD_P \text{grad} P \qquad \text{(Holes)}$$

Current continuity

$$-(1/e)\text{div}J_N + (R_N - G_N) = -\frac{\partial}{\partial t}(N-N_O) \qquad \text{(Electrons)}$$

$$(1/e)\text{div}J_P + (R_P - G_P) = -\frac{\partial}{\partial t}(P-P_O) \qquad \text{(Holes)}$$

(Recombination: R_N, R_P; Generation: G_N, G_P)

Total current

$$-I = J_N + J_P + \epsilon\frac{\partial E}{\partial T}$$

Circuit equations

APPENDIX A

HOT ELECTRON TRANSPORT EFFECTS IN FIELD EFFECT TRANSISTORS

Hot Electron Transport Effects in Field Effect Transistors

H. L. Grubin and T. M. McHugh
United Technologies Research Center
East Hartford, Connecticut 06108 USA

Abstract

Present semiconductor devices may be placed in one of several groups according to whether hot electron effects are or are not responsible for their operation. Gunn diodes fall into the former category whereas field effect transistors are in the latter. Currently used field effect transistor materials such as gallium arsenide are however subject to electron transfer with significant negative differential mobility and device operation may be expected to reflect this contribution. We have developed a program that numerically simulates the space and time dependent effects of negative differential mobility on field effect transistor operation. We have also included the effects of the external circuit which we represent by lumped elements. We will illustrate the transient formation of high field domains within the conducting channel and conditions necessary for propagation and recycling between the gate and drain contacts. We will also display stationary space charge configurations specific to the presence of negative differential mobility.

Hot Electron Transport in Field Effect Transistors

H. L. Grubin and T. M. McHugh
United Technologies Research Center
East Hartford, Connecticut 06108 USA

I. Introduction

Present semiconductor devices may be conveniently classified according to whether their operation depends on 1) the properties of a metallurgical junction, 2) nonequilibrium hot carrier effects in homogeneous materials, or 3) neither. Often the choice of semiconductor material introduces effects common to these categories, as in the case of the field effect transistor (FET) when gallium arsenide or indium phosphide are the active region material. In this paper we present some results of a new computer simulation of hot electron contributions to FET operation. The simulation is for the semiconductor GaAs and is unique in that it is the first to examine transient and steady state contributions of a region of negative differential mobility to the large signal operation of the FET. The results of the study are presented in section II. Section III outlines the numerical techniques used.

II. Space Charge Effects in Three Terminal Devices

The FET in its simplest form is a semiconductor slab with three terminals. Two of these are usually low resistance contacts, while the third is either a Schottky contact or a PN junction with an accompanying region of charge depletion. For unipolar conduction device operation is based on modulation of the depletion region which is usually accomplished by changes in the gate bias. Small and large signal gain are possible. Figure 1 is a sketch of the device

and connecting lumped element circuit parameters, whose operation we have simulated. For our discussion the source and drain contacts are parallel so that specific geometrical edge effects do not arise. The gate contact is symmetrically placed and all three contacts extend to infinity in both direction, indicating that the z-dependence of the space charge distribution is ignored. All three contacts are equipotentials and the drain bias is positive. The device dimensions and bias levels chosen for specific illustrations allow easily recognizable hot electron contributions. The y-dimension of the source and drain contact is 2.19microns and the x-dimension of the gate contact is 1.95microns. The source and drain separation is 10 microns. The doping concentration in this study is taken as $10^{15}/cm^3$, which is high enough to illustrate high field domain formation and propagation and low enough to assure reasonable computational speeds. The results are expected to be at least qualitatively applicable to the higher doped devices; a matter to be taken up at a later time. The electrons are assumed to follow the steady state velocity electric field curve[1]. Velocity overshoot[2] contributions are not considered.

The output of the simulation is illustrated in figures 2 and 3. Figure 2 shows the time evolution of the current at the three contacts and the potential at the gate and drain contacts for the situation where the gate bias is decreased, relative to ground, to the value $-0.3V_p$. The drain bias is increased to 0.5 and $1.0V_p$ in two steps. All bias changes are at a finite rate with the values listed in the figure captions. V_p=3.2volts. The sign conventions

are: positive source current means current flow into the device through the source contact; positive gate current means current flow out of the device through the gate contact; positive drain current means current flow out of the device through the drain contact. Thus, from figure 2, initially an increase in drain and a decrease in gate bias results in displacement current contributions with carriers leaving through the drain and source contacts and building up on the gate contact. After the initial transient there is significant conduction current contributions associated with physical movement of the gate depletion region until a steady state has been reached. The subsequent increase in drain bias with its associated charge buildup on the gate results in further movement of the depletion region.

The internal distribution of charge and current associated with the current and potential levels of figure 2 is shown in figure 3 where we begin to see the effects of nonlinearity associated with the velocity electric field curve. Figure 3a shows a set of current density streamlines through the device. The lengths of each streamline is proportional to the magnitude of the vector current density at the point in question. The maximum lengths of the individual x- and y- components before overlap is $J_P = N_0 e v_P$, where N_0 is the doping level and v_P the peak carrier velocity. For the parameters of this problem $v_P = 2.25 \times 10^7$ cm/sec. For the stationary states at t=45ps amd 81ps we see the current density to be greatest under the gate contact as required by current continutiy. For the 81ps frame the current density under the gate region is at least as great as J_P and velocity limitation introduces charge accumulation. The density of charge particles within the device is generally nonuniform and figure 3b is a projection of this distribution. We point out that particle

density increases in the downward direction. The first two frames of figure 3b show motion of the depletion layer toward the bottom of the conducting channel (increasing y). The second pairs show formation of a weak dipole layer. The initial formation of an accumulation layer is a consequence of velocity limitation and current continuity and materials like silicon also exhibit this[3]. Quantitative estimates of the particle density are displayed in the contour plots of figure 3c where adjacent contours enclose the regions $0.263r < N/N_0 < 0.263(r+1)$ where r=0,1,2,... . The presence of carrier accumulation is commensurate with high values of electric field. These values are obtained from the potential distribution, figure 4d, which demonstrates that at higher bias levels most of the potential drop is under the gate contact. The regions between the source and gate, and between the gate and drain are at low potential levels and act as linear resistors. The potential contours enclose the regions $0.105r < V/V_P + 0.5 < 0.105(r+1)$. Lines A,B,C,... represent r=10,11,12,... . While figure 3 illustrates the type of information available from our simulation the signature of the FET is its source-to-drain current-voltage (I-V) characteristic.

The FET I-V relation for the parameters listed above is shown in figure 4. We have also drawn for reference the velocity electric field curve for GaAs scaled to the current and voltage parameters. The first point to note is that the current levels nowhere approach the peak current associated with GaAs. This is, in part, a consequence of the additional resistance supplied by the gate region. We recall that in two terminal devices sublinearity in the GaAs I-V characteristic is often accompanied by a current instability. For wide channel three terminal GaAs devices similar behavior occurs. The instability is repre-

sented by the dashed part of the I-V curves of figure 4. The x's in the diagram represent average current and voltage values for the instability. We see that at drain bias levels somewhat above that of the parameters associated with figure 3 an instability has occured. In two terminal devices instabilities occur at cathode determined values of current density.[4] These values are somewhere between $\frac{1}{2}J_P$ and J_P, and as a consequence threshold current densities are generally polarity dependent. In three terminal devices the initiation of a domain instability generally occurs within that portion of the conducting channel under the gate contact. The instability occurs at a value of current density approximately equal to J_P. Then so long at the current density at the source and drain contacts is sufficiently low the source-drain I-V characteristics to the instability threshold should not experience significant polarity dependence.

Figures 5 and 6 provide a dramatic representation of an FET instability. With reference to the time scale of these figures, our calculations are performed sequentially and do not necessarily start at time t=0. Figure 5 shows the nucleation, propagation and recycling of a high field domain. Figure 6 shows the drain current and potential for this oscillation. The sequence of events associated with the instability is as follows: Domain growth under the gate is accompanied by an increase in potential. A corresponding decrease in current occurs throughout the device and circuit, as constrained by the dc load line. As the current decreases, carriers with velocities below that of v_P enter the accumulation layer region which subsequently begins to detach. The domain spreads as it leaves the gate region and it settles into a value of current density somewhat in excess of that associated with the saturated

drift velocity of the electrons. Prior to reaching the drain contact the domain dynamics appear to be one dimensional.

Among the earliest evidence for current instabilities in three terminal GaAs devices was that of Winteler et al[5]. In what they refer to as high current density devices they observed a current instability at zero gate bias and a drain bias just beyond the onset of saturation in I-V. At still higher drain bias levels the oscillation ceased. Their results are also not sensitive to polarity.

The numerical situation at high drain bias levels and zero gate bias levels is consistent with that of Winteler et al[5] and suggests that the cessation of current instabilities is accompanied by the presence of an accumulation layer extending from the gate to the drain contact. This is illustrated in figure 7 where at time t=594ps the drain bias is increased from $3.3V_P$ to $4.3V_P$ volts. Space charge accumulation in the gate-drain region is accompanied by a large nonuniform potential drop in this region with resulting high values of electric field and electrons travelling at their saturated drift values. Space charge accumulation is a consequence of current continuity. We note that this three terminal behavior where an unstable region is sandwiched between two stable regions has also appeared in two terminal devices[6]. In the two terminal case the high bias stationary state is accompanied by an anode adjacent domain.

Studies with two terminal devices teach that cathodes yielding large potential drops limit the downstream current densities to values below $N_0 e v_S$[4] where v_S is the high field saturated drift velocity of the carriers. Instabilites if present are damped. An analogous situation occurs with three term-

inal devices when a large negative bias is applied to the gate For this case the depletion layer moves toward the bottom of the channel and the source drain current is low. A large potential drop is present under the gate contact resulting in the formation of a high field domain. As seen in figure 8 the accumulation region is now surrounded on all sides by a depletion zone. The computations indicate that the highest velocity particles are in the upstream depletion region adjacent to the accumulation layer.

The above discussion demonstrates that in wide channel devices, hot electron effects common to two terminal devices also appear in three terminal devices. A simple intuitive picture of the two and three terminal commonality arises after making a one-to-one correspondence between the potential drop in that portion of the conducting channel that is under the gate contact and a phenomenological cathode field[4]. Moderate values for the gate potential yield drain bias dependent stationary and time dependent states. Cathode fields in two terminal devices with values somewhat in excess of the threshold field for negative differential mobility yield similar behavior[7]. Large negative gate potentials yield low current levels and an absence of a dc instability. High cathode field values in two terminal devices are generally accompanied by low current levels and the absence of an instability.[4]

The situation with narrow channel devices is less interesting from the view point of domain instabilities. For the symmetry of figure 1 and a source contact with a y-dimension approximately equal to one micron time dependent instabilities do not occur for 10^{15} doping levels.

III. Numerical Methods

The computations are carried out on a uniform mesh with MxN nodes. Boundary conditions are specified on surrounding nodes with the total number of nodes equal to (M+2)x(N+2). Potential and particle density are defined at nodal points, derived quantities are defined elsewhere. Poissons equation and the equation of continuity are

$$V_{i+1,j,k} + V_{i-i,j,k} + V_{i,j+1,k} + V_{i,j-1,k} - 4V_{i,j,k} = X^2 e\left(N_{i,j,k} - N_{O\ i,j,k}\right)/\epsilon \tag{1}$$

$$N_{i,j,k+1} - N_{i,j,k} = T\left(Jx_{i+1,j,k} - Jx_{i,j,k} + Jy_{i,j+1,k} - Jy_{i,j,k}\right)/eX \tag{2}$$

where i,j,k denote the x,y and t indicies and X and T denote the spatial and temporal increment. ϵ is the permittivity. The boundary potentials $V_{0,j,k}$, $V_{M+1,j,k}$, $V_{i,0,k}$ and $V_{i,N+1,k}$ are determined from Dirichlet conditions on the the contacts and Neumann conditions on the free surfaces. The potential on the contact is computed from the circuit equations and the normal component of electric field is zero on the free surfaces. The normal derivative of the particle density is taken to be zero on the free surfaces. On the source and drain contacts it is equal to N_0, on the gate contact it is equal to $10^{-7}N_0$.

The current densities in equation 2 are obtained from the equations

$$Jx_{i,j,k} = e\left(N_{i,j,k} + N_{i-1,j,k}\right)\left(\mu(\tilde{E}_{i,j,k})\bar{E}x_{i,j,k} + \mu(\tilde{E}_{i,j+1,k})\bar{E}x_{i,j+1,k}\right)/4 + e\left(D(\tilde{E}_{i,j,k}) + D(\tilde{E}_{i,j+1,k})\right)\left(N_{i,j,k} - N_{i-1,j,k}\right)/2X \tag{3}$$

and

$$Jy_{i,j,k} = e\left(N_{i,j,k} + N_{i,j-1,k}\right)\left(\mu(\tilde{E}_{i,j,k})\bar{E}y_{i,j,k} + \mu(\tilde{E}_{i+1,j,k})\bar{E}y_{i+1,j,k}\right)/4 + e\left(D(\tilde{E}_{i,j,k}) + D(\tilde{E}_{i+1,j,k})\right)\left(N_{i,j,k} - N_{i,j-1,k}\right)/2X \quad (4)$$

In the above $\bar{E}x_{i,j,k} = 0.5(Ex_{i,j,k} + Ex_{i,j-1,k})$ and $\bar{E}y_{i,j,k} = 0.5(Ey_{i,j,k} + Ey_{i-1,j,k})$. The vector $\vec{E}_{i,j,k}$ with components $\bar{E}x_{i,j,k}$ and $\bar{E}y_{i,j,k}$ is located in the center of a square with corners identified by the nodes (i,j), (i-1,j), (i,j-1), (i-1,j-1). The quantity $\tilde{E}_{i,j,k}$ represents the magnitude of the vector $\vec{E}_{i,j,k}$. The electric field in the above equations in obtained from the equations

$$Ex_{i,j,k} = -\left(V_{i,j,k} - V_{i-1,j,k}\right)/X \quad (5)$$

$$Ey_{i,j,k} = -\left(V_{i,j,k} - V_{i,j-1,k}\right)/X \quad (6)$$

The quantities $\mu(\tilde{E}_{i,j,k})$ and $D(\tilde{E}_{i,j,k})$, the mobility and diffusion coefficient respectively have values that are included in the numerical simulation. Thus the current density $Jx_{i,j,k}$ is located midway between the nodes (i,j) and (i-1,j) and the current density $Jy_{i,j,k}$ is located midway between the nodes (i,j) and (i,j-1). The above procedure involving the position of the current densities and electric field values is the result of computer experiments . This particular formulation we found leads to efficient numerical algorithms.

The total current density is calculated so that its components are in the same location as J. Thus

$$Jx_{i,j,k} + \epsilon\left(Ex_{i,j,k+1} - Ex_{i,j,k}\right)/T \equiv -Ix_{i,j,k} \quad (7)$$

$$Jy_{i,j,k} + \epsilon\left(Ey_{i,j,k+1} - Ey_{i,j,k}\right)/T \equiv -Iy_{i,j,k} \quad (8)$$

The total current on each contact is found by integrating the normal component of total current density over all nodes associated with the contact.

The external circuit equations for the simulations discussed here are for real impedances and Z_S=0.0. Then V_S=0,

$$V_{BD_k} = I_{D_k} xR_D + V_{D_k} \quad (9)$$

$$V_{BG_k} = I_{G_k} xR_G + V_{G_k} \quad (10)$$

$$I_{S_k} = I_{G_k} + I_{D_k} \quad (11)$$

where V_S , V_G, V_D are the source , gate and drain contact potential values; and I_S,I_G,I_D are the respective currents. The external circuit equations demand an iterative solution and for the three terminal device two levels of iteration are required. For a fixed estimate of I_G an estimate of I_D is made and improved, using a gradient technique, until the difference $\left|V_{BD_K} - I_{D_k} xR_D - V_{D_K}\right|$ is less than a specified small number. For a fixed estimate of I_D the estimate of I_G is improved similarly. . The presence of the external circuit introduces difficulties in the solutions.. If the potential on the contacts is constant the above procedure produces divergence free solutions. However the form of the difference equation 2 assumes that there is no change in the boundary conditions over the integration interval. If ΔT is the

largest time step for which solutions exist, we find it necessary to solve equations 2,7 and 8 over a much smaller interval $\Delta T'$ over which we may assume the boundary conditions to be approximately constant. If $N_{i,j,k'}$ is the electron concentration propagated by the time step $\Delta T'$, then propagation to the next full time step is performed as follows:

$$N_{i,j,k+1} = N_{i,j,k} + \Delta T\left(N_{i,j,k'} - N_{i,j,k}\right)/\Delta T' \qquad (12)$$

The completed solution requires the following procedures. Initial conditions on the gate and drain currents , electron concentration, and boundary conditions on the potential and electron concentration are required. At each time step, given $N_{i,j,k}$, $I_{G_{k-1}}$, $I_{D_{k-1}}$, and estimates of I_{G_K} and I_{D_K} : (1) Find $V_{i,j,k'}$, $Jx_{i,j,k}$ and $Jy_{i,j,k}$; (2) Find $N_{i,j,k'}$, $V_{i,j,k'}$, $Jx_{i,j,k'}$, $Jy_{i,j,k'}$; (3) Find $Ix_{i,j,k'}$ and $Iy_{i,j,k'}$; (4) Update estimates of I_{G_K}, I_{D_K}. A gradient technique is used to update the estimates of the total currents I_{D_k} and I_{G_k}. When the iterations have converged the mobile charge density is propagated to the next time step using equation (12).

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Figure Captions

1. An FET configuration with the source and drain contacts at the ends of the device. The device is modelledin the x-y plane and the circuit is represented by lumped elements. For all calculations $Z_S=0.0$, $Z_G=0.1R_0$ and $Z_D=R_0$. $R_0=V_P/J_PA$ where A is the cross sectional area of the source contact, and is arbitrary.

2. Time evolution of the current and potential at the three contacts. $I_P=J_PA$. The drain bias is increased linearly from zero to the value $0.5V_P$ in 4.5 ps. The gate bias is decreased linearly from zero to the value $-0.3V_P$ in 2.7ps. In the second step the drain bias is increased at 45ps to the value V_P. The increase is linear and in 4.5ps.

3. The internal distribution of current,charge and potential for the parameters of figure 2.Note that the particle density surrounding the nonuniform distribution is uniformly distributed within the source gate region and the gate-drain region. The uniform distribution is at the value $N/N_0=1.0$.

4. Drain current-drain voltage relation. Circles denote computed points.

5. Projection of the time dependent particle density when a instability occurs. For this oscillation the drain bias is increased linearly from 1.3 to $1.8V_P$ in 4.5ps, beginning at time t=144ps. The gate bias for this calculation is zero.

6. The time dependent potential and current at the drain contact for the instability of figure 5.

7. Distribution of current, particle density and potential for the case when the drain potential is increased from $3.3V_P$ to $4.3V_P$ volts in 9ps. Also shown is the drain potential and current. The gate bias is zero for this calculation. The particle density contours have the same labelling as figure 3. The potential contours are as follows: $0.21r< V/V_P\leq 0.21(r+1)$.

8. Particle density, current density and potential distribution for a time independent configuration with a drain bias of $2.0V_P$ and a gate bias of $-0.9V_P$. Particle density contours are as in figure 3. Potential contours are $0.158r < V/V_P + 1.0< 0.158(r+1)$.

Acknowledgement

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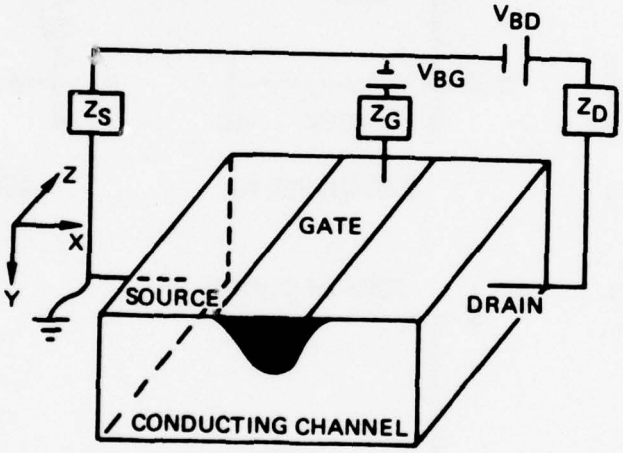
FIG. 1



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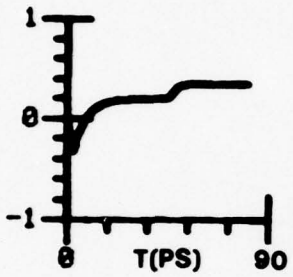

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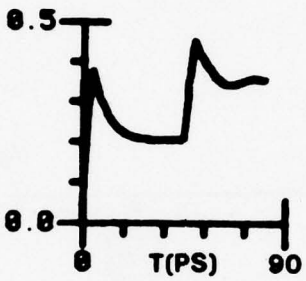

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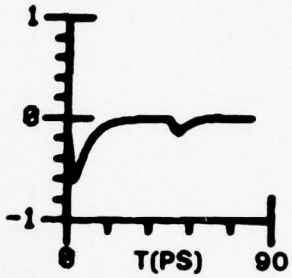

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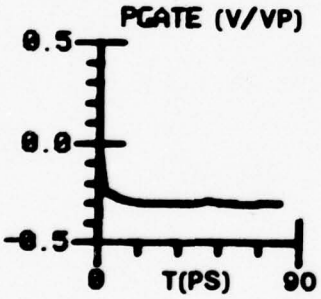

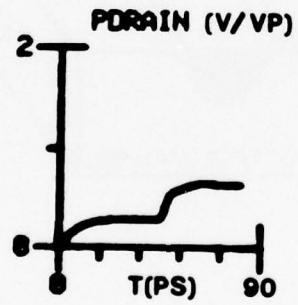

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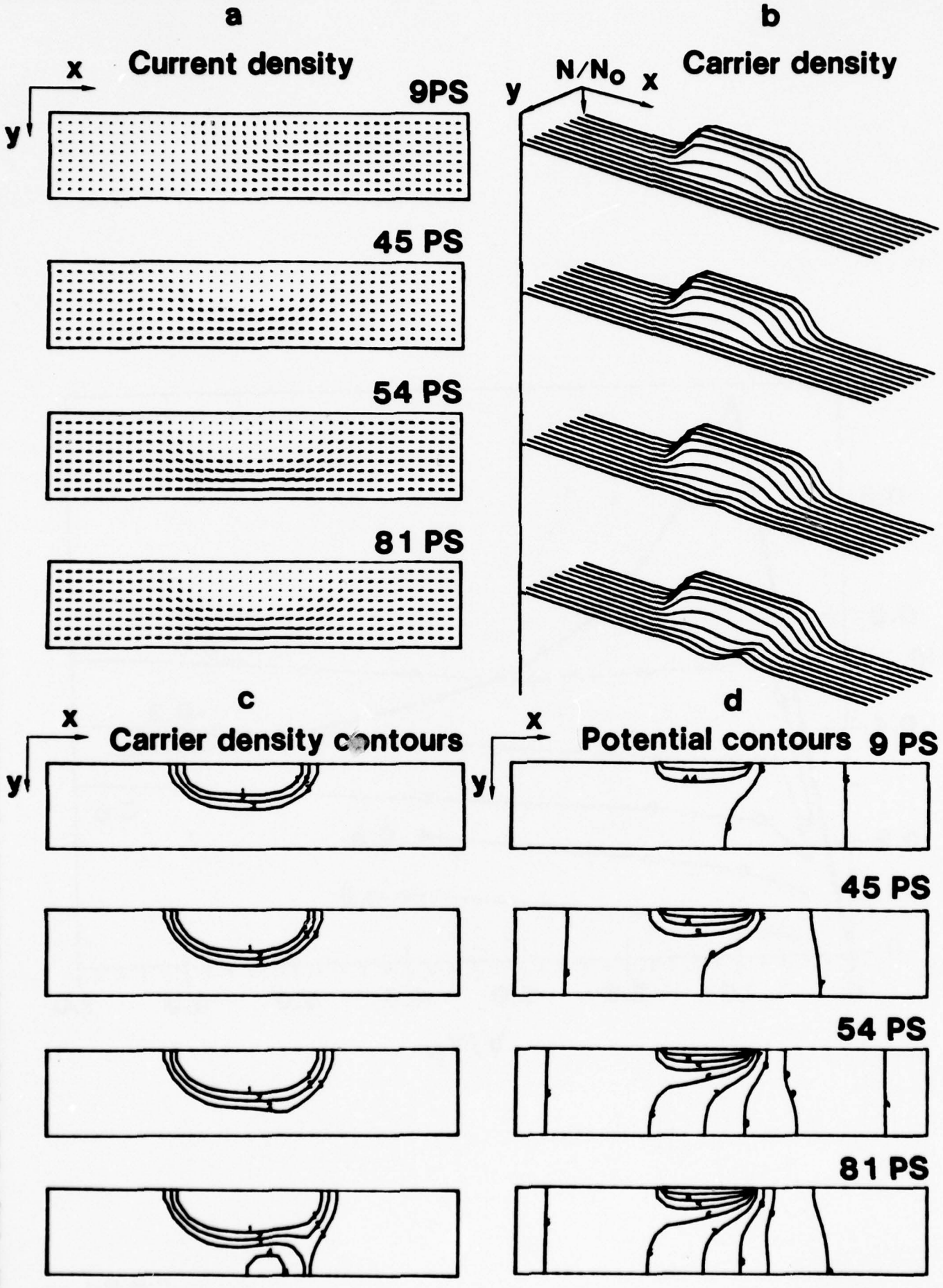
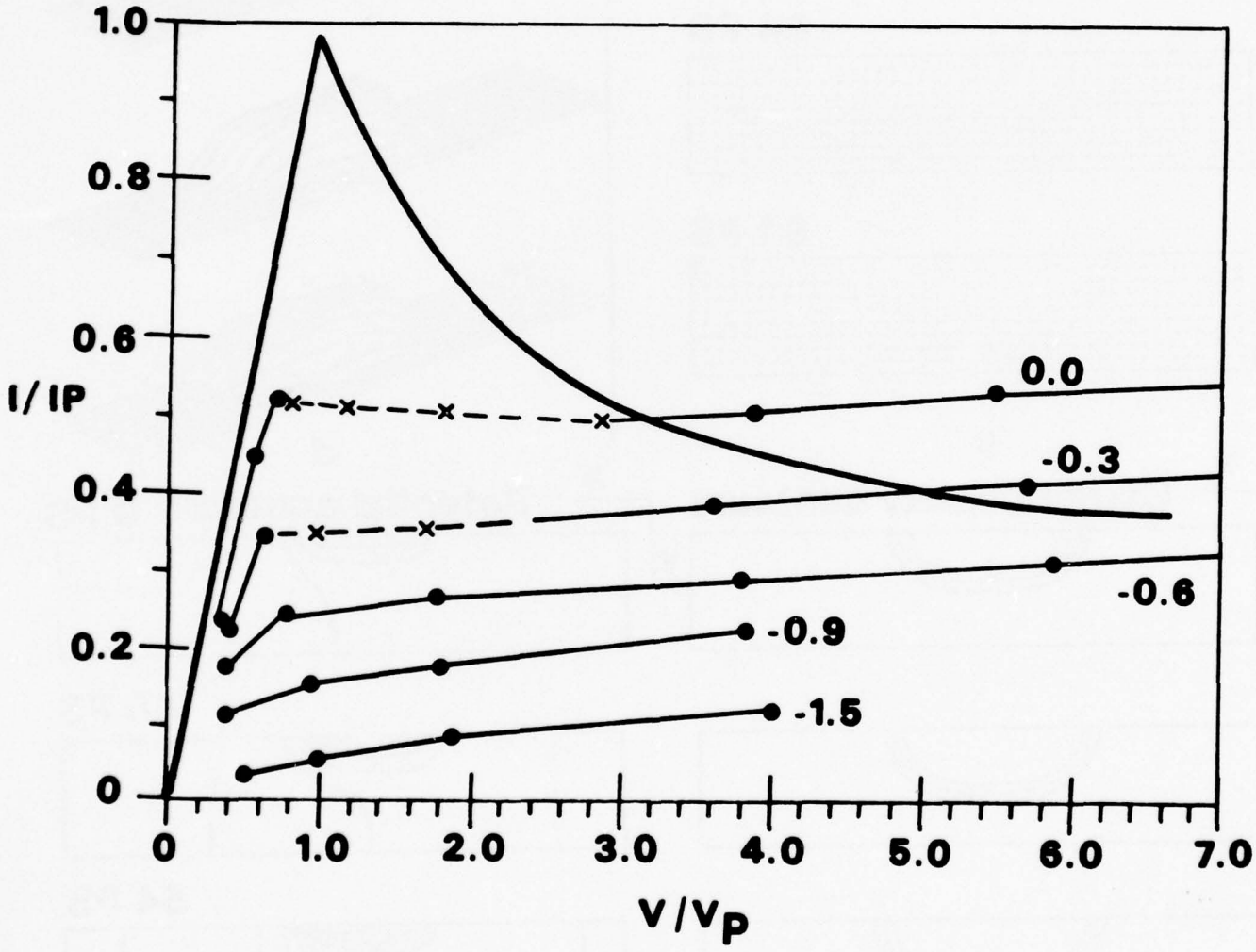

a
Current density
x
y
9PS
45 PS
54 PS
81 PS
b
Carrier density
N/No
x
y
c
Carrier density contours
x
y
d
Potential contours
x
y
9 PS
45 PS
54 PS
81 PS

77-08-28-1



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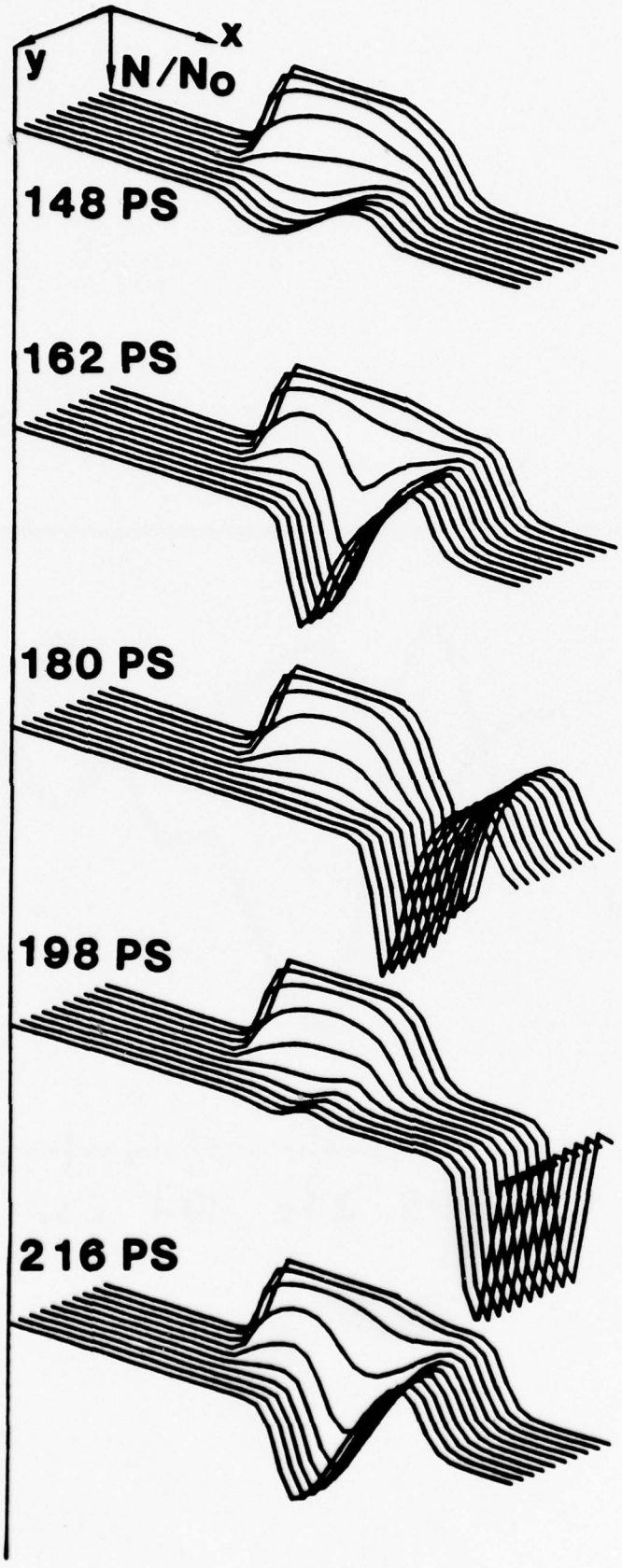

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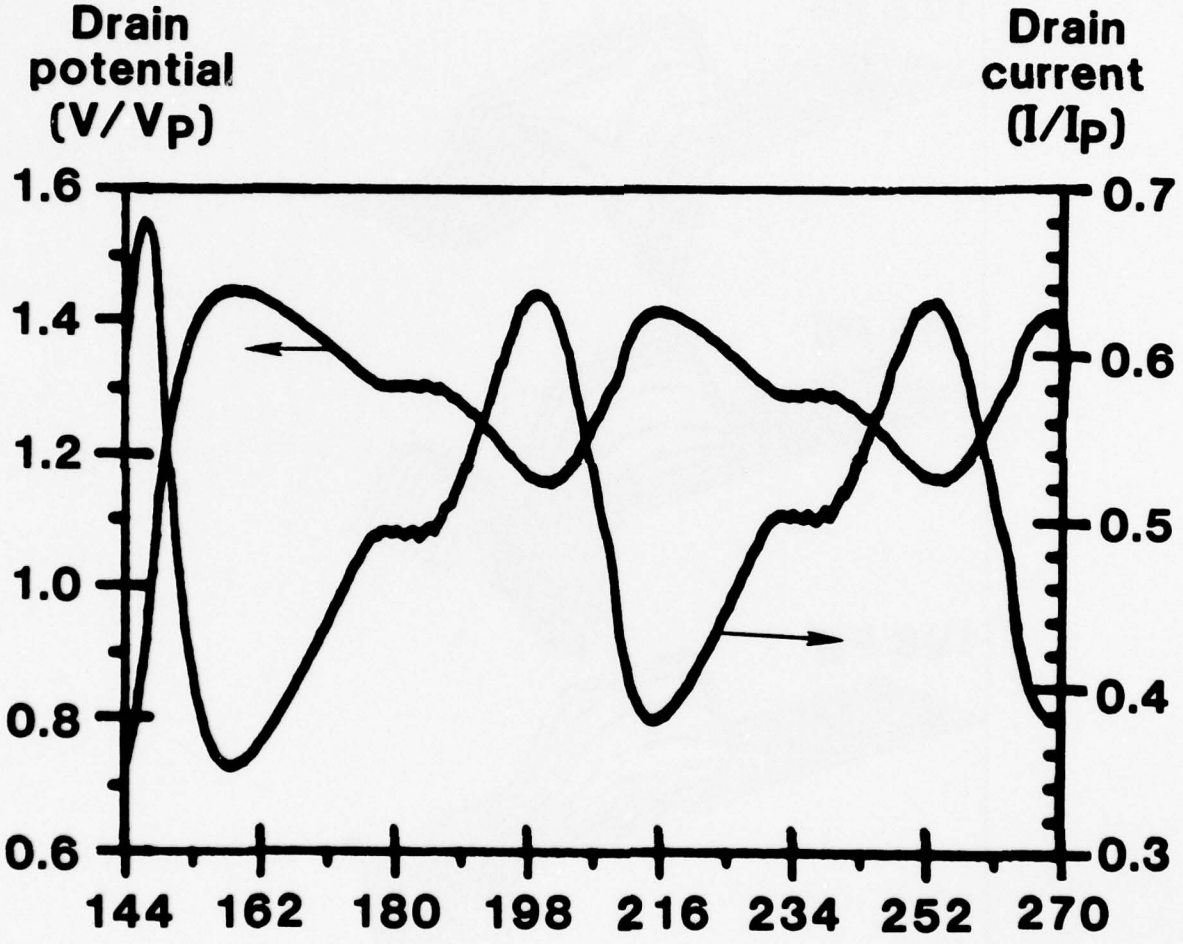
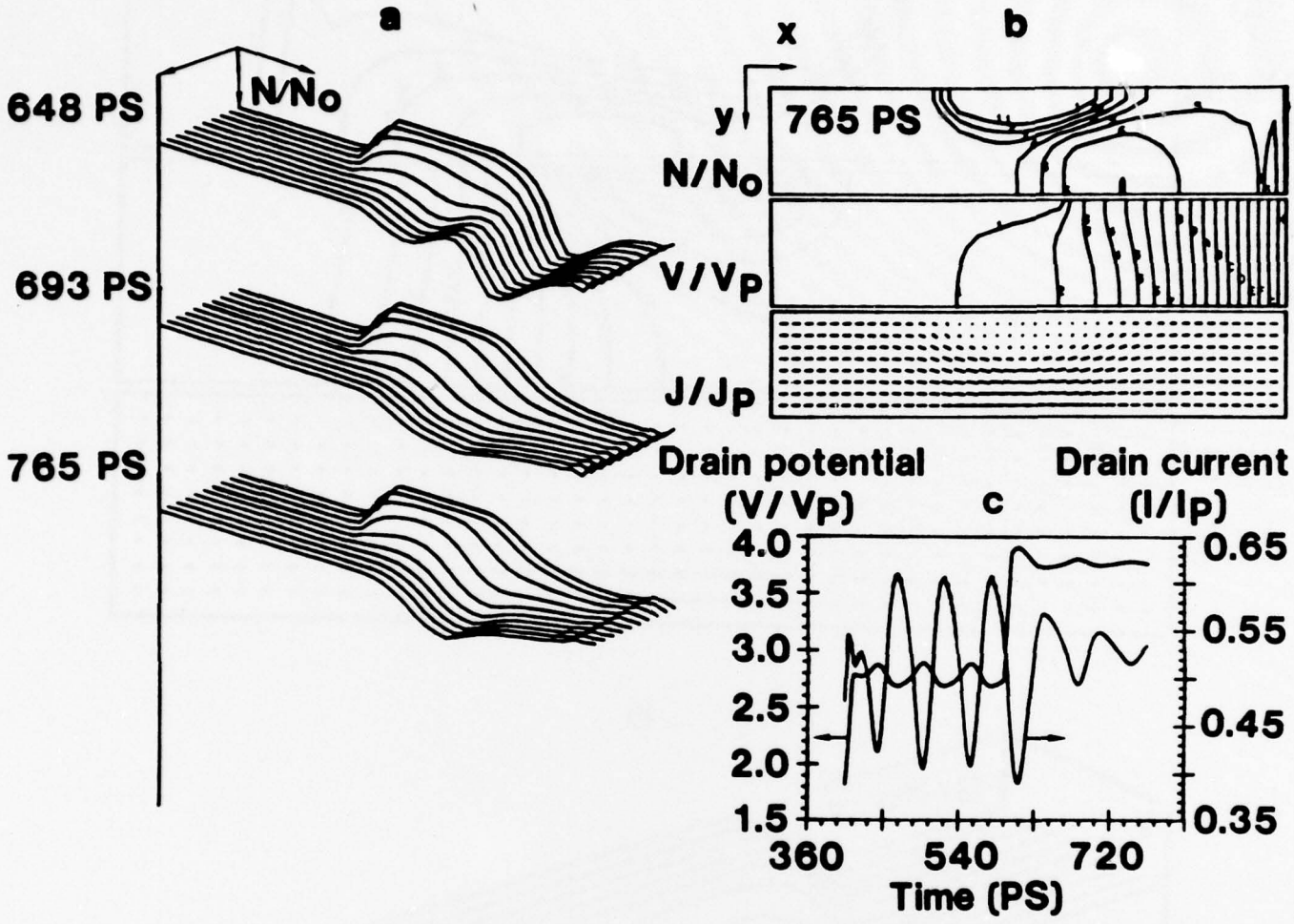
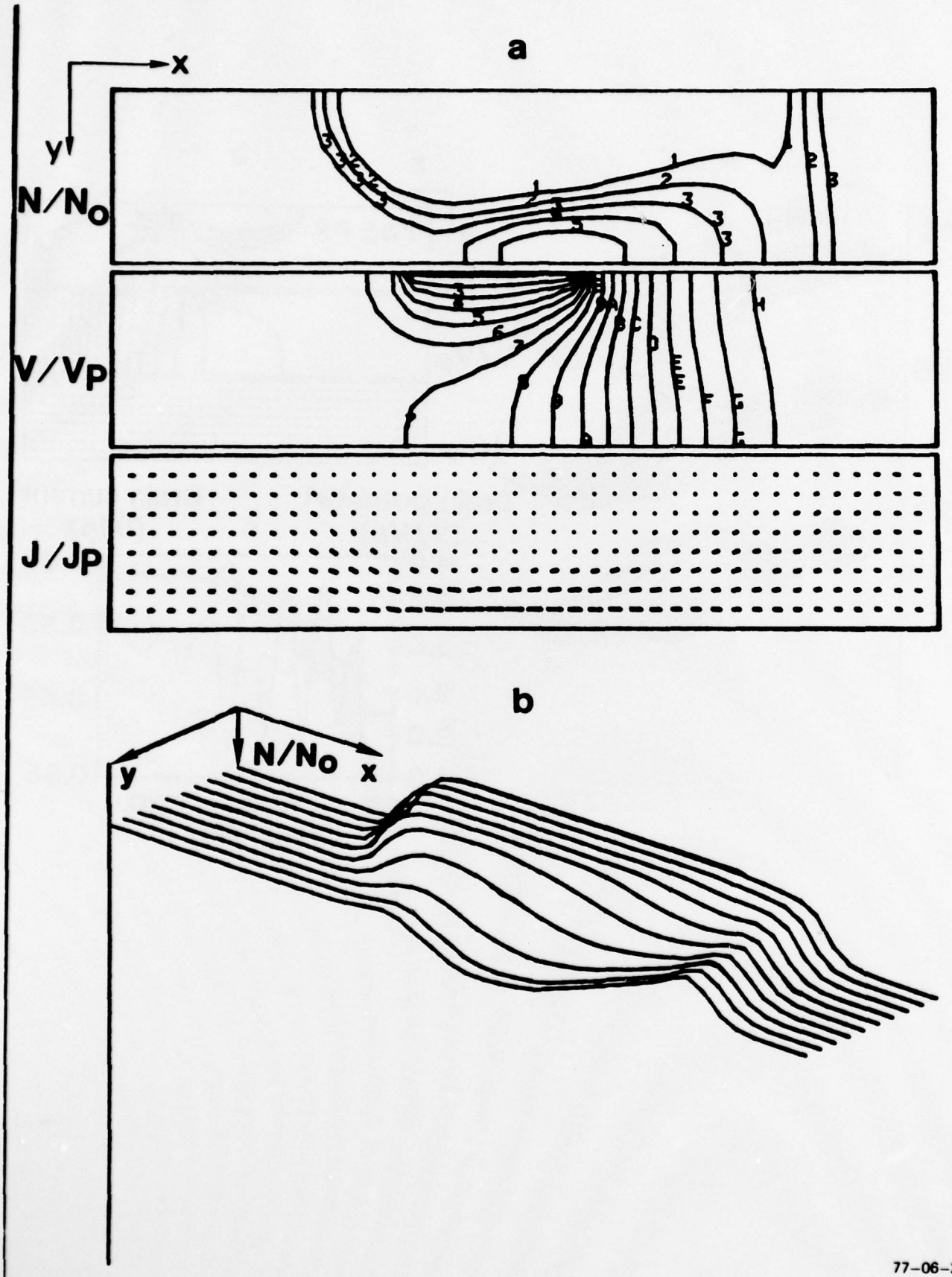

Drain potential (V/Vp)
Drain current (I/Ip)
1.6
1.4
1.2
1.0
0.8
0.6
0.7
0.6
0.5
0.4
0.3
144
162
180
198
216
234
252
270

77-06-29-5


a
N/No
648 PS
693 PS
765 PS
x
b
y
765 PS
N/No
V/Vp
J/Jp
Drain potential
(V/ Vp)
c
Drain current
(I/Ip)
4.0
3.5
3.0
2.5
2.0
1.5
0.65
0.55
0.45
0.35
360
540
720
Time (PS)

77-08-29-2



77-06-29-6

APPENDIX B

LARGE SIGNAL NUMERICAL SIMULATION OF FIELD EFFECT TRANSISTORS

LARGE SIGNAL NUMERICAL SIMULATION OF FIELD EFFECT TRANSISTORS

H.L.Grubin
United Technologies Research Center
East Hartford, Connecticut 06108

A large signal time dependent numerical code has been developed for simulating the space charge and circuit dependence of nonlinear single gate unipolar field effect transistors (FET). One goal of the simulation is to determine the ways the nonuniform space charge distribution is affected by the form of the velocity electric field relation, v(E), and the material properties of the device (e.g., substrate); and how it in turn affects such things as the source-drain current voltage characteristic. Another goal is to obtain design parameters for the large and small signal behavior of the FET. In the discussion that follows we will concentrate on the former goal and restrict ourselves to effects common to GaAs FETs possessing either Schottky[1] or junction[2] gates.

The FETs of interest fall into two groups according to whether under zero gate bias conditions they are or are not capable of sustaining a current instability arising from the propagation of a dipole layer. It is known that for sufficiently wide channel structures the devices exhibit, above a critical drain bias, microwave frequency oscillations[2,3]. The oscillation properties are dependent on the values of the drain and gate bias, and may be suppressed at sufficiently high negative gate[3] or positive drain[2] bias levels. Upon suppression of the oscillation normal FET operation appears possible. The oscillations do not appear to be significantly dependent upon the level of the active region doping, as the results of references 2 and 3 in which instabilities were observed were for significantly different doping values. The second group of FETs of interest are narrow channel devices and in these devices large signal instabilities do not occur.

Numerical simulation of the time dependent properties of wide channel GaAs FET in which the effects of the external circuit was included and the oscillation detected by variations in current and voltage across an external impedance was recently reported[4]. These results will be summarized below and used as a point of comparison with the more recent narrow channel studies and with studies that include a substrate.

The numerical simulation is for the device/circuit configuration of figure 1. The simulation is for two space dimensions plus time. The x-dependence is along the length of the channel, the y-dependence along the channel height. All variations along the z-direction are ignored. The calculations are performed for two cases: one in which the source and drain contacts are parallel (bold lines in figure 1) and the second in which all three contacts are coplanar (dashed lines). In all cases

the contacts are equipotentials. The active region height of the FET is denoted by H_c and that of the substrate by H_s. For the present study the doping within the active region and substrate are uniform and time independent. The doping of the active region is $10^{15}cm^{-3}$, that of the substrate is $10^{12}cm^{-3}$. The numerical results are not qualitatively dependent on the value of the doping within the active region, and the low value was chosen to reduce computing costs. The specific semiconductor properties are represented by a field dependent velocity and diffusion relation. We assume an'instantaneous' velocity response to changes in electric field. This neglect of velocity 'overshoot' contributions means that the fundamental frequency limitation of the FET cannot be ascertained within the present program. Rather the frequency response obtained herein must be regarded as a lower limit to the true frequency response. Details of the parameters used in the calculation, references for the v(E) and diffusion curves, and a discussion of the numerical methods is contained in reference 4. The results are summarized next.

The static and dynamic properties of a Schottky gate GaAs FET with H_c=2.20 microns, L_g=1.95 microns and L=10 microns are summarized in figure 2a[4]. For this case the gate is centrally placed, the source and drain contacts are parallel and H_s=0. The results are essentially symmetrical about the bottom of the device; and it is as though a fictitious 'reflecting' substrate were present. Figure 2a displays drain current versus drain voltage for the device. Closed circles denote time independent computed points; crosses denote average current and voltage when the device is sustaining a self-excited transit time oscillation. The v(E) curve is also included in the diagram and scaled to the current and voltage parameters. The current is in multiples of $I_p=N_0ev_pA$, where N_0 is the active region doping level, v_p the peak carrier velocity, and A the cross sectional area in the y-z plane. The drain potential, which is the potential on the drain contact is in multiples of $V_p=E_pL$, where E_p is the electric field at peak velocity. Here E_p= 3.2kV/cm and $v_p=2.2x10^7$cm/sec. The curves are further labelled by the value of gate bias, which is also expressed as a multiple of V_p.

The results associated with figure 2a teach that for each curve, and below saturation,that a depletion region exists under the gate contact and that the regions between the source and gate, and gate and drain may be regarded as electric-field-independent resistors. For V_{GO}=0 saturation begins at a value of drain potential significantly below that value of gate bias needed to reduce the drain current to negligibly small values. For the parameters associated with figure 2a the gate bias needed to pinchoff the drain current is approximately $-3.0V_p$(see also reference 3). Saturation for V_{GO}=0 is accompanied by the presence of an accumulation layer that forms within the conducting channel at the drain side of the gate contact. The accumulation layer is preceeded downstream by a depletion layer and dipole formation results. It should be noted that dipole formation for FETs is not a consequence of a region of negative differential mobility (NDM); it is

a consequence of velocity limitation[5] and channel widening downstream from the gate contact. The effects of dipole formation should also manifest itself in FETs fabricated from silicon. The presence of a region of NDM affects the stability of the dipole layer and for sufficiently high values of drain bias an instability occurs in the form of a propagating and recycling high field domain. The oscillation frequency is determined by the nucleation time under the gate, propagation time and drain time. For an average drain potential of $1.3V_p$ the frequency of oscillation is approximately 18GHz. The transit time oscillation is bias dependent and at sufficiently high values of drain bias the oscillation ceases and the space charge distribution within the FET now includes the presence of an accumulation layer that extends, within the conducting channel,from the drain side of the gate contact to the drain contact. One important consequence of this is that the region between the gate and drain contacts can no longer be modelled by a field independent resistance. The presence of charge accumulation between the gate and drain contacts is a consequence of a potential drop sufficiently great for the electrons to be travelling at their saturated drift velocity value v_s which is approximately equal to $0.4v_p$. Then,any significant value of drain current in excess of $0.4I_p$ would be expected to be accompanied by carrier accumulation. (Similar high bias space charge distributions are thought to be responsible for the amplification properties of two terminal super-critical amplifiers[6].) The situation at moderately increased negative values of gate bias is similar to that for $V_{GO}=0$, but at sufficiently high values the oscillations again cease. For this case the low value of drain current implies that most of the potential drop must fall under the gate contact, and the regions between the source and gate and gate and drain can again be regarded a electric field independent resistors. But an increased drain potential under large negative values of gate bias causes the depletion layer to migrate toward the drain contact with the result that the gate to drain parasitic resistance although no longer field dependent is dependent on bias. We point out that the gate dependence of the oscillation for the FET is a feature essential to the operation of transferred electron logic devices[7].

Parallel calculations to those for GaAs were performed on a fictitious element whose high field velocity is constant and equal to v_p for values of electric field greater than E_p. This zero differential mobility (ZDM) element has characteristics similar to that of silicon, although among other things its saturated velocity is greater than twice that of silicon. The ZDM calculations were performed to determine the extent to which NDM affects saturation; and also because the ZDM calculations are easily scaled, they can provide modelling assistance. For the ZDM calculations the diffusion was taken as constant and equal to 200 cm^2/sec. The ZDM current voltage curves are displayed in fig. 2b, where we have also drawn the v(E) curve. We note again that saturation begins, for the $V_{GO}=0$ case, at drain potential values below that necessary to pinch the drain current to negligible values. For this

case pinchoff occurs for a value of gate bias equal to $-2.5V_p$. Qualitatively similar results were obtained in reference 5. We also point out that the value of drain current, for $V_{GO}=0$, at high values of drain potential (exceeding those of the scale of figure 2b) approaches unity. This suggests that the device dimensions are not limiting the current values in the figure 2a GaAs calculations; rather it is the value of the high electric field saturated drift velocity. Additional calculations have been performed in which the saturated drift velocity values in NDM elements bracketed the GaAs value. For the case where the saturated drift velocity exceeded the GaAs value the high drain potential current level exceeded that for GaAs; the reverse occured for NDM elements with saturated drift velocities values less than the GaAs one.

One necessary requirement for the presence of large signal domain instabilities is that the current density be high enough to sustain a propagating domain. By decreasing the channel height the relative contribution of the depletion region under the gate increases and the current density throughout the device decreases. The elimination of domain instabilities is then possible . The question is: how much of a decrease is necessary. For the gate length of figure 2a the peak current, prior to saturation and the subsequent current instability, is very close to the minimum current necessary for supporting a traveling domain. This suggest that a device with with a somewhat smaller channel height would be sufficient for eliminating the instability. We did not do a systematic study of channel height versus stability. Instead for a channel height of 1.22 microns numerical simulations did not yield any large signal instability. The drain current versus drain voltage relation for this narrower device, with parallel source and drain contacts is displayed in figure 3a. In figure 3b we show computed results for a ZDM element with the same dimensions. We note for the figure 3 calculations that the voltage at the onset of saturation is approximately equal to the gate voltage necessary to pinchoff the drain current. For the GaAs element pinchoff occurs at a gate bias of $-0.6V_p$; for the ZDM element it occurs at $-0.6V_p$.

A cursory examination of the results of figures 2 and 3 suggests that if the presence of current instabilities is ignored in the three terminal device then the drain current versus drain voltage relation and perhaps the small signal parameters for a GaAs FET can be modelled by assuming a two piece velocity electric field relation of the type used in figures 2b and 3b. Indeed if the peak velocity for the ZDM element was chosen from a best fit with experiment then satisfactory agreement with the GaAs drain current versus drain voltage relation can be obtained. We have found that the current voltage relation in saturation and for time independent conditions submits to the relation $I_D=I_{DO}(V_D)(1 - V_{GO}/V_{GP})^n$, where $I_{DO}(V_D)$ is the drain current for $V_{GO}=0$, and V_{GP} is the value of gate bias necessary for pinchoff. n is a dimensionless parameter. The values of the pinchoff voltages have been given in the above paragraphs. The values of n for the GaAs elements in fig-

ures 2a and 3a are respectively 2.3 and 1.7 . The values of n for the ZDM elements in figures 2b and 3b are respectively 1.5 and 1.8 .

There are,however, limitations in the extent to which a GaAs FET can be adequately modelled by a two piece ZDM element. In particular difficulties arise in representing the voltage dependence of the gate to drain resistance for the situation when there is significant charge accumulating within this region. In this case the distribution of charge within a wide channel GaAs FET (see figure 8 of reference 4) is not necessarily the same as that within a wide channel ZDM element. The situation is somewhat brighter for narrow channel devices where the drain current is significantly below the current associated with the saturated drift velocity. In this case for both the GaAs element and the ZDM element saturation is accompanied by a large potential drop under the gate region, where most of the charge nonuniformities reside. We illustrate this charge distribution for the narrow channel GaAs FET in figure 4.

In figure 4 we display, for three combinations of drain potential and gate bias, the projection of the carrier density within the FET. We note that carrier density increases in the downward direction. In figure 4a the gate bias is zero and the drain potential is $0.28V_p$. We point out that the rate of increase of mobile carrier density under the gate contact is greatest near the source side of the gate region. In figure 4b the results for a drain potential of $0.72V_p$ show the rate of increase to be greatest at the drain side of the gate region where an accumulation of charge has formed. We note the region of partial carrier depletion downstream from the accumulation layer and the presence of the resulting dipole layer. Figure 4c shows the carrier density projection for a gate bias of $-0.3V_p$ and a drain potential of $1.93V_p$. Here the increase in negative gate bias results in a decrease in current density between the source and gate contacts, and between the gate and drain contacts. The region surrounding the gate is essentially swept free of mobile carriers.For the calculation of figure 4c, the low drain current and high drain potential values require that most of the potential drop be across the depletion region. This is illustrated in figure 5a which shows the large potential drop across the depleted region; the latter extending itself downstream from the gate contact region. The display in figure 5a is a contour plot of equipotential lines. Each line separates the regions $0.105r < V/V_p < 0.105(r+1)$, where r=0,1,2,...,9,A,B,... Lines A,B,C,.. represent r=10,11,12,.. We point out that the potential drop across the depletion zone results in an average electric field sufficiently high for the carriers to be traveling at their saturated drift velocity value. We indicated above that the potential and charge distribution for a narrow channel ZDM element was qualitatively similar to that for GaAs. Figure 5b displays a contour plot of potential for the ZDM element with a gate bias of $-0.2V_p$ and a drain potential of $1.34V_p$.

The calculations we have performed are time domain transient cal-

culations and so far have not revealed a region of static negative differential conductivity. Instead a low voltage high current state may switch to a lower current higher voltage state through an unstable region. The time dependent calculations in addition to allowing us to explore the transit-time dependent properties of the three terminal device,also allow us to explore the large signal amplification properties of the device, and to obtain realistic estimates of the response of the system to changes in gate and drain bias. In figure 6 we display a large signal gate current versus time profile, where time is in multiples of the low field dielectric relaxation time, 0.9×10^{-12}sec for 10^{15} doping. We show in a sequence of steps the time it takes the carriers to settle into a time-independent distribution after responding to changes in bias. At time t=0 the device is turned on with the gate bias decreasing at a finite rate to the value $-0.2V_p$ and the drain bias increasing at a finite rate to the value $0.5V_p$. There is initially a transient displacement current contribution due to these bias changes which results primarily in charge buildup on the gate contact. Conduction current contributions are always present but they dominate after the bias has reached its assigned value. In this case the conduction current contributions correspond to charge rearrangement within the device as determined by the amount of charge residing on the gate contact. Charge rearrangement is represented in figure 6 by the apparent exponential relaxation of the gate current to a zero value. The relaxation to steady state is dependent upon the speed of the carriers, the width of the depletion region and parasitic contributions. Going to higher drain bias values results in an increase in carrier velocity for situations below saturation. The result is a decrease in the time of relaxation. This is displayed in figure 6 where at the normalized times of 80 and 120 the drain bias is increased at a finite rate to the values $1.0V_p$ and $1.5V_p$,respectively. An increase in the value of the gate potential to a higher negative value results in an increase in the resistance of the device. The result is an increase in the time the system takes to settle into a steady state configuration. This is illustrated in figure 6, where at the normalized time of 160 the gate bias is decreased from the value $-0.2V_p$ to the value $-0.4V_p$. In this case the drain bias was held fixed at $1.5V_p$. We note that the calculations of figure 6 were for the narrow channel ZDM element.

The above discussion has ignored all substrate effects, except isofar as the bottom of the device may be regarded as the boundary line to a 'reflecting' substrate . Below, we briefly discuss some aspects associated with the presence of a substrate, and for this situation the numerical calculations are for the FET in the planar configuration. With respect to figure 1, L =10 microns and the height of the FET is 1.76 microns. H_c=0.98 microns, H_s=0.59 microns with the doping transition occuring over the distance of 0.19 microns. The source, gate and drain contact lengths are respectively 0.59, 1.59 and 1.76 microns. The calculations are displayed in figure 7 and are intended to draw attention to the presence of space charge injection into the substrate. The place-

ment of the contacts is indicated on the diagram. In figure 7 we display carrier density contours where the contours separate the regions $0.263< N/N_0< 0.263(r+1)$ for $N_0=10^{15}/cm^3$. We also show potential contours, which for figure 7a separate the regions $0.263r< V/V_p< 0.263(r+1)$; for figure 7b they separate the regions $1.05< V/V_p< 1.05(r+1)$. We also display a set of current density streamlines through the device. The streamlines represent the vector current density, with the length of individual streamlines proportional to the magnitude of the current density. The maximum length of the individual x- and y- components before overlap is equal to J_p in figure 7a and $\frac{1}{2}J_p$ in figure 7b, where $J_p=N_0ev_p$. The computation in figure 7a is for a zero gate bias and a drain potential of $2.68V_p$. Here we see the presence of charge accumulation under the gate region near the n-region/substrate boundary. There is also some current transport from the n-region into the substrate at the source end of the FET. But under the gate region all current is parallel to the bottom of the device; i e., the y- component of current is approximately zero. There is however enough structure in the potential at the n-region/substrate boundary to yield a finite y-component of electric field and consequent injection of carriers into the substrate. Once in the substrate they may contribute to the conduction current. Conduction in the substrate is also illustrated in figure 7b where the gate bias is equal to $-0.2V_p$ and the drain potential $1.87V_p$. For this case there is almost no current flow through the n-region; instead most of it is within the substrate.

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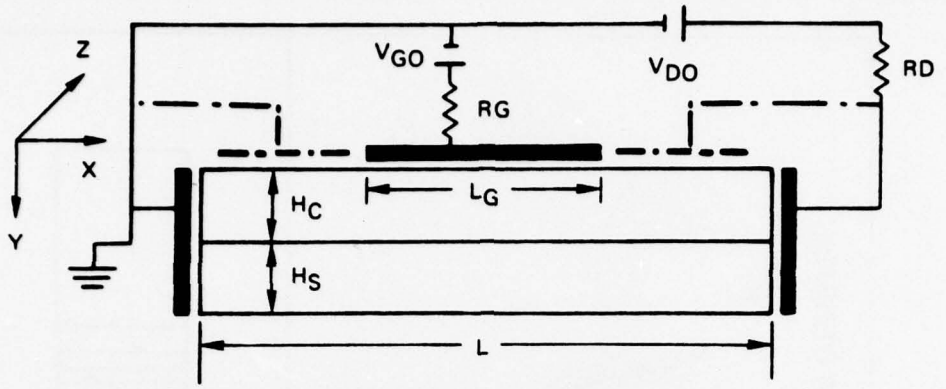

FIGURE 1. DEVICE AND CIRCUIT CONFIGURATION

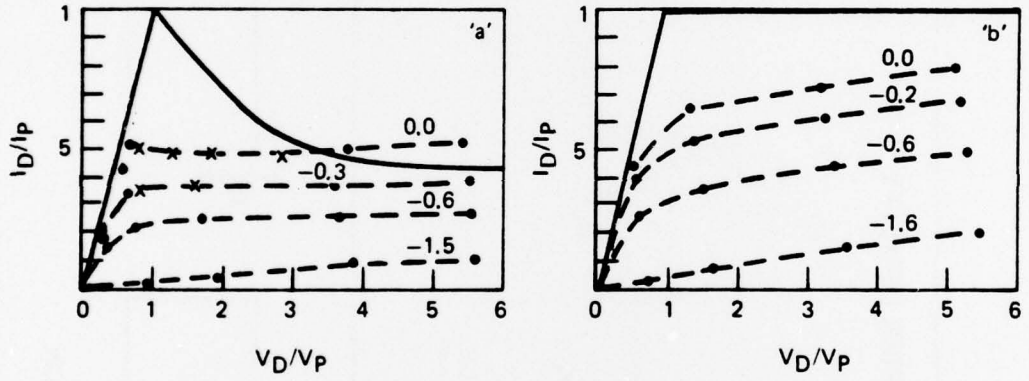

FIGURE 2. I_D VERSUS V_D FOR H_C = 2.24 MICRONS

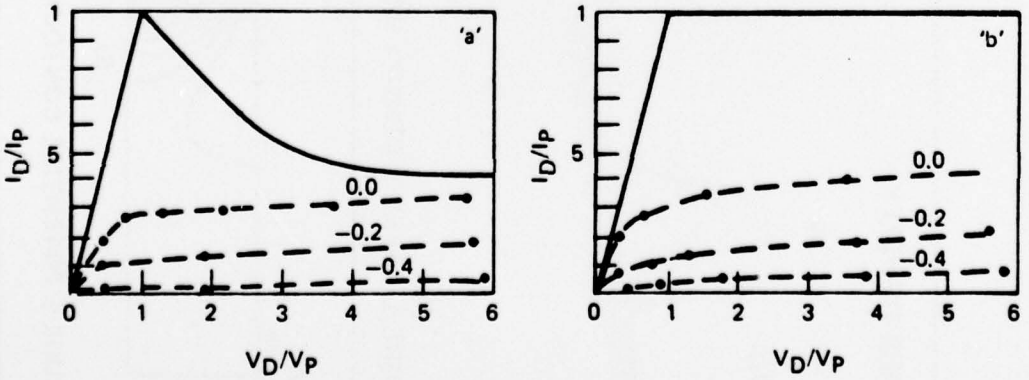

FIGURE 3. I_D VERSUS V_D FOR H_C = 1.22 MICRONS

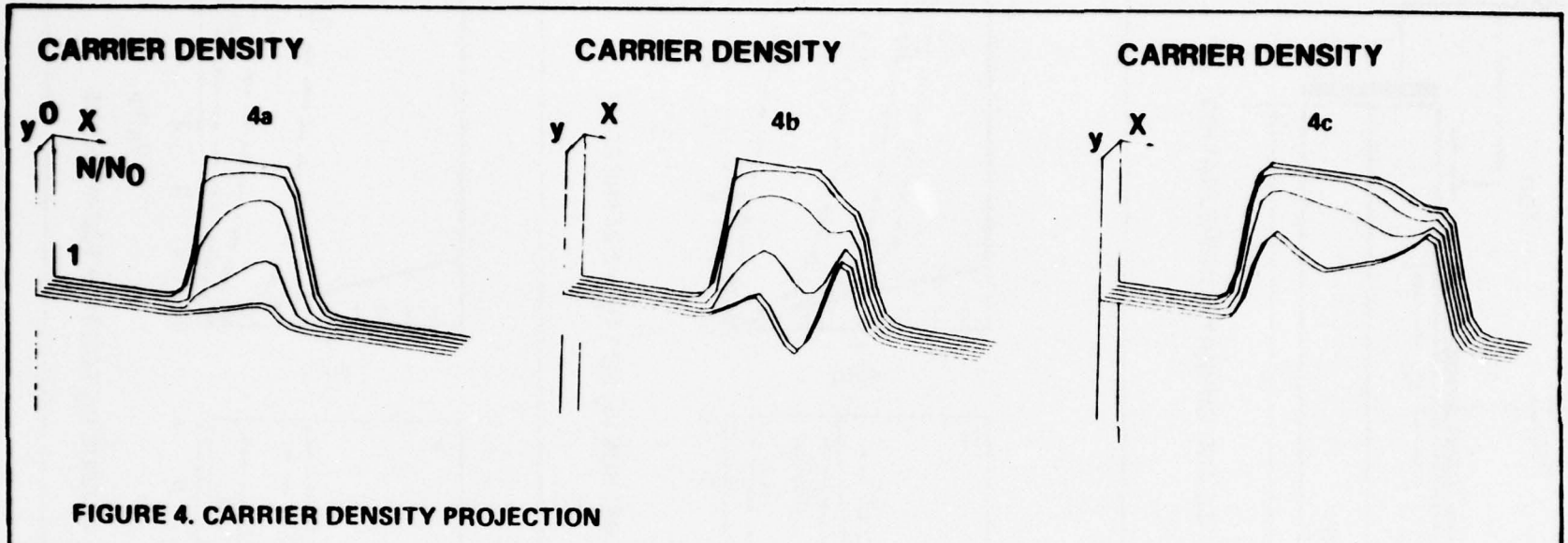

FIGURE 4. CARRIER DENSITY PROJECTION

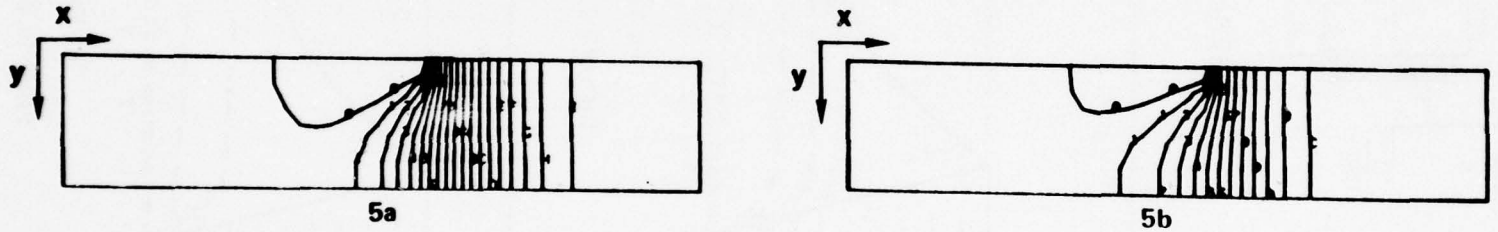

FIGURE 5. POTENTIAL CONTOUR DISTRIBUTION

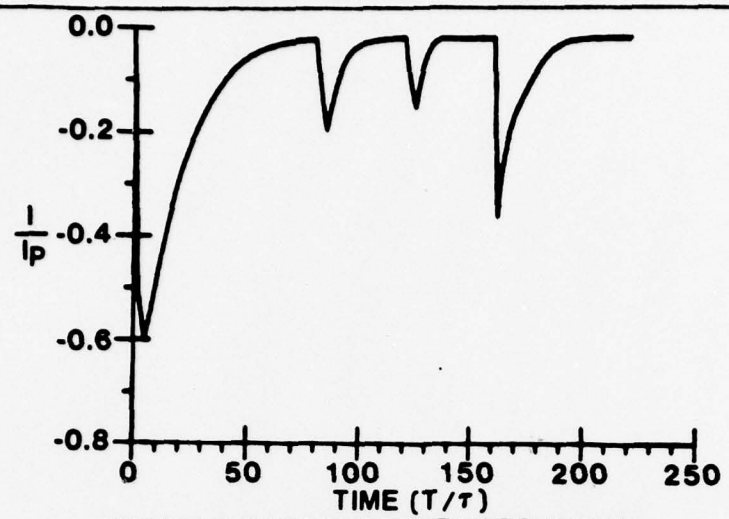

FIGURE 6. GATE CURRENT VERSUS TIME

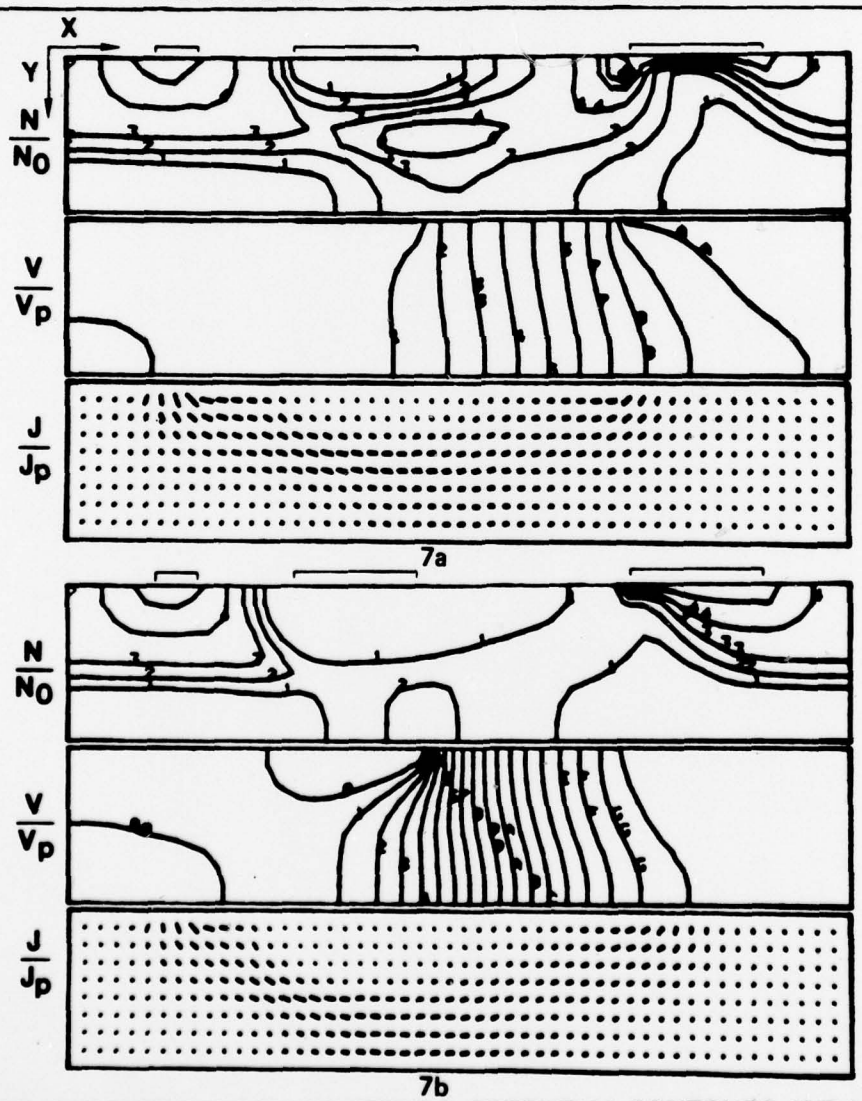

FIGURE 7. CARRIER DENSITY CONTOURS, POTENTIAL CONTOURS AND VECTOR CURRENT DENSITY

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