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AN AUTOMATIC RECYCLING MULTIPLE SAMPLER.(U)
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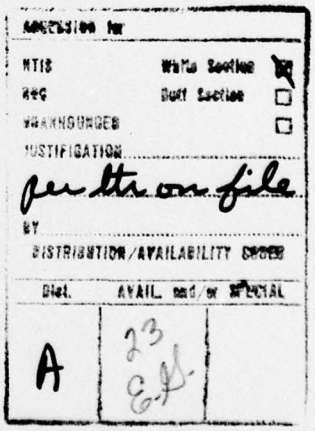
Foreword

This memorandum covers only a small phase of the problem of instrumentation for signal enhancement research and has been prepared primarily for internal distribution to aid others at NEL who may be interested in related problems. Only a limited distribution outside of the Laboratory is contemplated. Work to June 1955 is covered.



AN AUTOMATIC RECYCLING MULTIPLE SAMPLER

by

E. C. Westerfield

Introduction

In many problems in communication or data analysis some type of speed-up of signal processing is desirable. This speed-up may be accomplished by multiple-processing devices where several processing units are operated in parallel or by signal speed-up devices in which the information bearing signal is sped-up so that the multiple-processing operations can be carried out serially by a single processing unit. The speed-up might also be accomplished by a combination of signal speed-up and multiple-processing devices. A delay line memory using a quartz ultrasonic delay line provides one means of accomplishing the signal speed-up.[1] In this device, known as the DELTIC (Delay Line Time Compressor), successive samples of the signal are fed into the delay line after the previous sample has passed through and been recycled into the delay line a second time. The samples in the output of the delay line are thus in correct sequential order but are compressed in time by a factor depending on the relation between the sampling period and the delay time of the memory unit. The purpose of the present paper is to describe a similar device in which a binary shift register is used for the memory unit.

1. MIT Progress Report, Jan-March 1954, pp. 17-22.

Description of the Automatic Recycling Multiple Sampler

As may be seen from the block diagram, Figure 1, the circuitry of the Automatic Recycling Multiple Sampler is relatively simple.

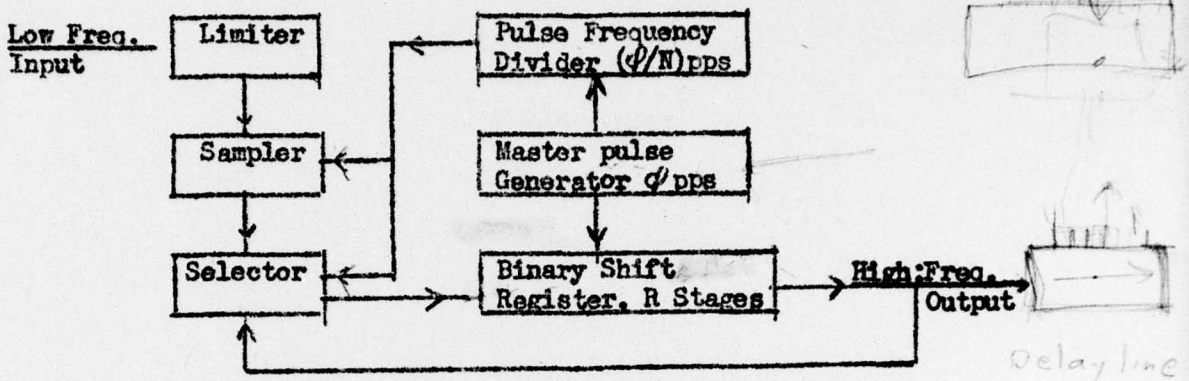


Figure 1. Block Diagram of Automatic Recycling Multiple Sampler.

The functions of the limiter, sampler and selector may be combined into a single unit. They are separated in the block diagram to simplify the discussion of the operation. The pulse frequency divider may be any unit, such as a preset counter for example, which will recycle and emit a pulse after receiving a predetermined number N of pulses from the master pulse generator. The binary shift register for example may have R = N - 1 stages for one mode of operation. The sampler and selector are driven by the pulse frequency divider at the rate (φ/N)pps, while the binary shift register is driven by the master pulse generator at the rate of φ pps. Additional pulse shaping, impedance matching, and power amplifier units may be necessary to make the pulses from the pulse generator operate the sampler, selector and shift register

reliably but these may be considered as incorporated in either the driving or the driven units, so no special blocks are required for these functions in the block diagram.

Operation of the Automatic Recycling Multiple Sampler

With R = N - 1 stages in the binary shift register the Automatic Recycling Multiple Sampler operates in a manner similar to that described for the DELTIC. A limiter is indicated on the input to the sampler to insure binary type samples. With the pulse frequency divider set to recycle and emit a pulse on the Nth count from the master pulse generator each time, the selector will accept N - 1 samples from the output of the binary shift register and recycle them into the shift register. The Nth sample from the output of the shift register will be rejected however and a sample from the sampler will be substituted. N - 1 counts later this sample will be recycled into the shift register and on the next count a new sample from the sampler will be fed into the shift register, etc. After NR = N(N - 1) counts the shift register will be filled with consecutive samples from the input signal but the interval between successive samples on the output of the shift register will be less than that on the original signal by a factor of 1/N. It follows that all frequencies less than $\varphi/2N$ will have been increased by a factor N. This sped-up output of the shift register is repeated each time the shift register recycles, the only change being that the oldest sample is dropped each time and a new sample added so that during any recycling period the output of the shift register consists of the N - 1 most recently received samples

of the incoming signal.

Other modes of operation are possible with the Automatic Recycling Multiple Sampler. For example, if $R = N + 1$ stages are used in the shift register the output will be sped-up in the ratio N to 1 but the samples will be inverted in order so that the signal will be effectively reversed in time. Or, as another mode of operation the shift register could contain $R = 2N - 1$ stages. This mode of operation would separate the odd from the even numbered samples so that the latest $N - 1$ odd numbered samples would appear on the output followed by the latest $N - 1$ even numbered samples, etc. One might also take $R = (N - 1)/M$, that is $N = MR + 1$, where R as before is the number of stages in the shift register and M is an integer. For this last mode of operation the shift register would recycle repeating its output (a sequence of the R latest samples) M times before the selector dropped the oldest sample and added a new one. It would then repeat the new sequence M times, etc. With $N = MR - 1$ the samples would be recycled through the shift register in inverse order M times before the selector dropped the oldest sample and added a new one.

Discussion

The chief advantage of the ARMS over the DELTIC unit is perhaps the absolute lock in synchronization which is possible in the shift register type of time delay unit. With the pulse frequency divider set to recycle on a count of N, φ may be varied over a fairly wide range without upsetting the operation of the ARMS unit. There is also the possibility of utilizing this feature to lock the ARMS unit in synchronization with

the other associated equipment. With the units operating properly, fairly wide variations in power supply voltages may occur also without affecting the synchronization.