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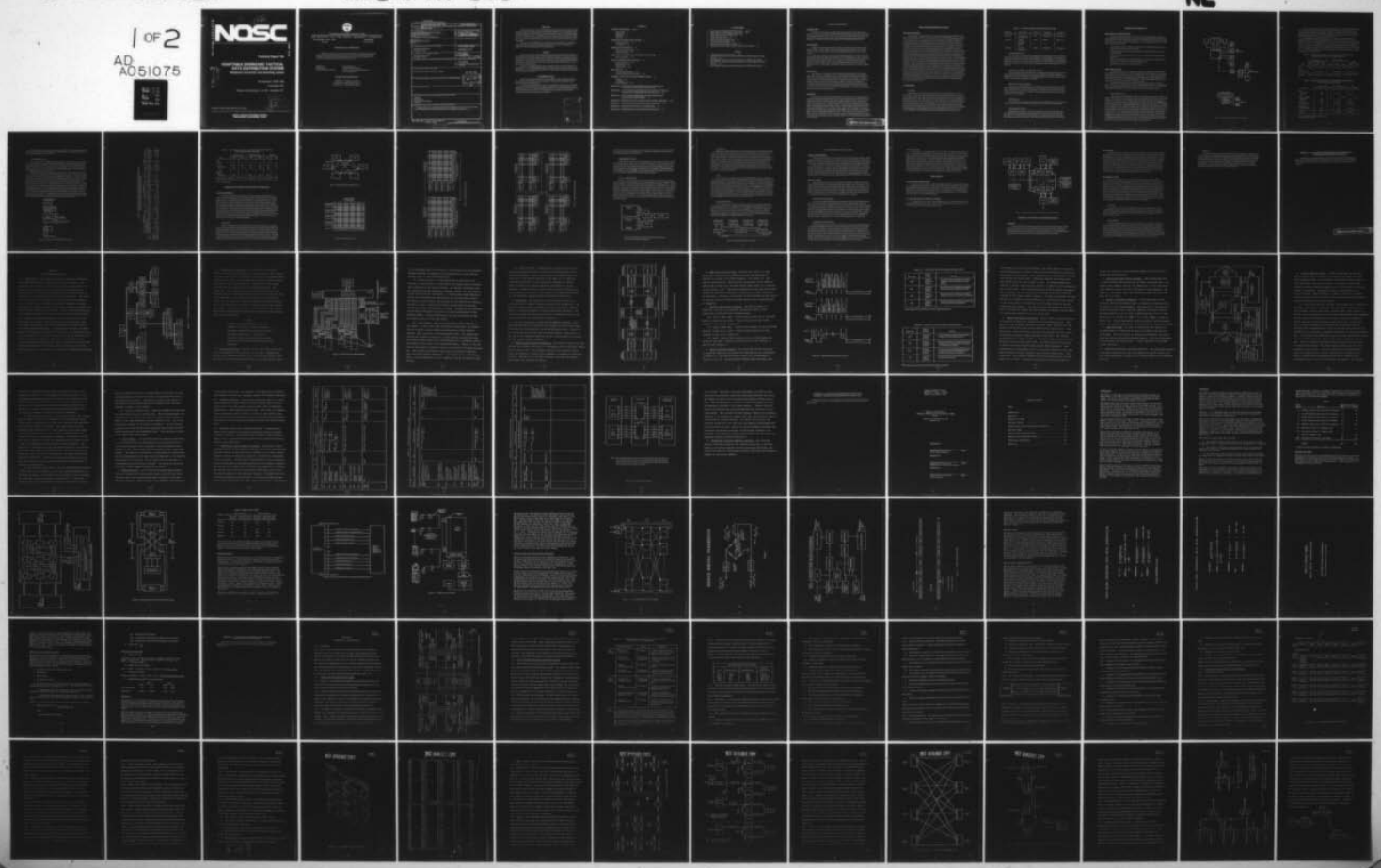

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Technical Report 183

ADAPTABLE SHIPBOARD TACTICAL DATA DISTRIBUTION SYSTEM

Shipboard conversion and switching system

HC Schleicher, LCDR, USN

16 December 1977

Research and Development: July 1976 — September 1977

Approved for public release; distribution is unlimited

NAVAL OCEAN SYSTEMS CENTER
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Design and fabrication of a Shipboard Conversion and Switching System is discussed. Concepts have been proven for this system by a demonstration model which uses a modified shore-based system.

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OBJECTIVE

The interconnection of computer components using bulky, expensive, parallel cabling and manual switches has been improved in shore-based complexes by use of parallel-to-serial converters, solid-state matrix switches, and serial-to-parallel converters. The added versatility realized in the matrix switch is as desirable as are the savings in material, weight, and installation costs. Virtually any channel of any equipment can be connected to any channel of any other equipment. Automatic fault detection and correction in distributed switching systems are feasible.

The objective of this NOSC task was to determine the requirements of a shipboard combat computer/peripheral switching and distribution system and to demonstrate an expandable converter-switching system for shipboard use.

RESULTS

An advanced model of the Shipboard Conversion and Switching System (SCSS) has been designed and fabricated. Much of the demonstration model uses a modified shore-based system to prove the recommended concepts. This does not endorse any particular system as the desired one. Indeed, none of the present shore-based systems satisfies all of the shipboard requirements. Additional work has been done in the areas where shortcomings exist. The entire concept has been proven.

The need for a shipboard system has been shown in detail for two combatants, USS RANGER (CV 61) and USS TARAWA (LHA 1). Savings in tons of hardware, thousands of dollars in labor costs, and additional availability for combat missions could have been realized if the SCSS had been installed.

RECOMMENDATIONS

Future Tactical Data Systems which will be installed in Navy complexes, shipboard and shore-based, will be impacted by the necessity to conduct serial interchange of data through a versatile switching system.

The switching conversion system must be such that the tactical system is expandable, compartmentized, fault-compensating, reliable, and standardized. These attributes are discussed in the text as are the means of implementing them. An engineering development model of the SCSS should be created now. The applications of this system extend from Fleet modernized carriers to new construction combatants.

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ILLUSTRATIONS

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GENERAL INFORMATION

INTRODUCTION

This report is the result of an NOSC exploratory development task. Work was conducted by members of the Information Transfer Division (Code 834) during the period 1 July 1976 through 30 September 1977. This report provides the baseline information and recommended action to guide the development of an engineering developmental model and to demonstrate a laboratory prototype of a shipboard switching and distribution system.

BACKGROUND

Solid-state conversion and switching systems are employed in three Navy computer support facilities. System usage in one of these facilities has increased from 55 percent to 95 percent because of the improved versatility and reliability introduced by the switching system.

The present technique of interconnecting shipboard computer complexes with dedicated parallel cabling is proving to be inadequate for the following reasons: there is no pooling nor sharing of backup equipments; recovery from a computer failure is slow; interconnecting cables are large and heavy; a large space is required for the SB-1299 manual switches which have limited capability; there is no real configuration management; and there is no realistic way to use a lower priority computer in a critical system in case of a prime computer failure.

OBJECTIVES

The objectives of this project were to determine the requirements, to develop the operational scenarios of a shipboard combat computer/peripheral switching and distribution system, and to demonstrate a baseline system in the laboratory. This modular expandable system provides: (a) standard interfaces for the computer equipment groups; (b) a means to monitor distribution system status and rapidly reconfigure computers and peripherals; (c) reduced distribution system size and weight; (d) on line, noninterfering, monitoring and recording of any system part; and (e) on-line training capabilities. This system is to include control, monitor, test, display, record-keeping and decision functions to provide total management for the interconnected ADP systems.

APPROACH

The initial phase of this project addressed two tasks. One was to investigate computer switching systems and techniques which now exist or are being developed. In this effort, an analysis of the benefits or shortcomings of the switching systems was to be conducted and a summary of how the systems compare when applied to shipboard configurations was to be made. The second task was to compile a listing of current and future shipboard ADP systems, their related equipment, and their interconnection. The investigation addressed several classes of ships including DD 963, CG 26, CGN 36, CVA 59, LHA 1, LCC 19 and CV 61. Systems which were to be addressed included NTDS, ATDS, MPDS, CDPS, ASIS, MIS, ACLS, TADIXS, ADT, CV-TSC, ITAWS, IADT, DTPEW, and TFCC. The second phase of this project was to analyze the data accumulated in phase one and to outline the baseline switching system which best satisfies present and future needs. A baseline system was to be demonstrated and evaluated in the laboratory.

SHORE-BASED DISTRIBUTION SYSTEMS

SYSTEM DESCRIPTION

The solid-state switching system is a computer-controlled, high-speed digital switch, used to automatically interconnect Naval Tactical Data System (NTDS) equipment channels. The system is designed for use at Fleet Combat Direction Systems Training Centers to facilitate the simulation of actual shipboard Combat Information Center (CIC) installations for the training of personnel. Unwieldy connectors and cabling at the switch/patchpanel are eliminated by converting parallel NTDS data channels to serial data channels. Reconversion to parallel data is required after channel I/O interconnection is accomplished at the switch. The system requires three types of parallel-to-serial (P/S) and serial-to-parallel (S/P) converters to permit interface to the different MIL-STD-1397 parallel interfaces. Since all NTDS computers do not have the same I/O control-word repertoire, a simulator is provided to compensate for this difference and also to permit the computers to interface on peripheral designated channels. An operator controls the automatic switching process by entering switch I/O interconnect data on the CRT/printer keyboard at the control console. The CRT DISPLAY permits the operator to monitor entered commands and also data responses from the Control Computer. A particular switch I/O path is established within milliseconds after data entry by an operator. Rapid configuration of multi-switch I/O paths, to reflect a particular installation, can be accomplished by calling for stored configurations. The operator, by use of various operational and maintenance test commands, can check any and all paths through the switch matrix. A medium-speed printer provides a hard copy of all test results and faults, for analysis. If the control console should fail, the switch paths can be controlled locally via pushbuttons. If both the automatic and local control modes should fail, switching can be accomplished by manually patching around the switch matrix. The system's high-speed, automatic verification of interconnect and software test diagnostics permit rapid configuration and verification of a given system. The solid-state switching systems have replaced the slow cumbersome fault-prone manual patching systems.

A COMPARISON

GENERAL

Three solid-state switching systems are installed in Naval shore facilities. They are listed in table 1. These systems are similar in that they perform parallel-to-serial conversion, pass the signal through three-stage space-division switching networks, and then perform serial-to-parallel conversion. The conversion units provide interfacing for the various NTDS MIL-STD-1397 parallel interfaces. The differences in these systems are in the conversion methods, synchronizing techniques, and in the technologies used to implement the matrix network. In-depth functional descriptions of these systems can be found in Appendixes A through C. The brief description included herein addresses the major attributes which must be considered for shipboard use. Recommendations based on this comparison are included in the final section (SUMMARY, CONCLUSIONS, AND RECOMMENDATIONS) of this report.

TABLE 1. EXISTING SOLID-STATE SWITCHING SYSTEMS

Nomenclature	System Name	Acronym	Command	Location
AN/USQ-62	Conversion and Switching System	CSS	FCDSSALANT	Dam Neck, VA
AN/USQ-67	Centrally Controlled Information System	CCIS	CSMTF	Vallejo, CA
AN/USQ-68	High-Speed Digital System	HSDS	FCDSSAPAC	San Diego, CA

SYNCHRONIZATION

The AN/USQ-67 and AN/USQ-68 equipments are asynchronous systems. Synchronization at the receiving end of a channel is accomplished in the AN/USQ-67 by synchronizing a triggerable clock to the serial data. Synchronization in the AN/USQ-68 is accomplished by using phase-lock loops to synchronize the receiver clock. The AN/USQ-62 is a bit-synchronous system wherein pulses from a central clock are distributed to the transmitting and receiving converters.

BLOCKING (INABILITY TO PROVIDE A PATH)

The AN/USQ-62 and the AN/USQ-67 are functionally nonblocking switching systems. A functionally nonblocking system is one which uses software to guarantee a signal path through the switch. The AN/USQ-68 is physically nonblocking. This requires a larger switch with more internal paths to guarantee a signal path.

PHYSICAL CHARACTERISTICS

The converters in the AN/USQ-62 and AN/USQ-68 are multichannel converters with similar cabinets of various shapes which either fit onto equipments or stand alone as remote units. The AN/USQ-67 converters are packaged as extensions of the connectors for the particular equipments on which they are placed. A power supply for these connector/converters is located near each equipment.

TECHNOLOGY

The AN/USQ-62 uses transistor-transistor logic; the AN/USQ-67 uses hybrid transistor-transistor logic; and the AN/USQ-68 uses transistor-transistor and electron-coupled logic.

TRANSMISSION MEDIA

The transmission media for these systems are RG-59 coaxial or RG-8 triaxial cable. The AN/USQ-62 and AN/USQ-68 pass digital signals in one direction per cable while the AN/USQ-67 uses a duplex-digital-transceiver (DDT) to pass edge information in both directions simultaneously over triaxial cable. Paths through all of the switches are unidirectional.

SHIPBOARD REQUIREMENTS

OPERATIONAL CONSIDERATIONS

The necessity for a combatant to be resistant to battle damage limits the degree to which individual weapons systems can be interdependent. Ideally, each system should stand alone and include a totally redundant backup system. Realistically, communications between these systems is essential. They cannot stand alone nor is total redundancy practical. A shipboard combat system should be:

Expandable so that new systems can be added to the communications link with no apparent effect upon the rest of the system;

Compartmentalized as stand-alone weapon systems which communicate via a communications link;

Fault-compensating, having the ability to sense a system failure and automatically compensate;

Reliable having redundancy in that the primary system could use equipment from a lesser system to perform a function of the primary; and

Standardized to make use of standard interfaces.

SHIPBOARD SYSTEMS

Several classes of ships were studied in this project. In general, the systems aboard these combatants can be grouped according to computing power. One group is a large system having three or more large computers such as NTDS systems. The second group is a smaller system having one or two large computers, and a third group uses a single computer system of the minicomputer type. The USS RANGER (CV 61) and USS TARAWA (LHA 1) have a cross section of systems which fall into these various groups.

The systems in both ships are extremely limited, in terms of the given definition. These systems are not expandable nor are they fault compensating, reliable, nor standardized. There is very little capability for using equipment within the same system for backup much less using that equipment for backup of another system. Some examples are given.

USS RANGER (CV 61)

The combat system in RANGER consists of several small systems which interface with NTDS. The NTDS system functions as the display and decision element of the combat system. Smaller systems which are tied to NTDS include Carrier Approach Traffic Control Center (CATCC), Tactical Support Center (TSC), NATO Sea Sparrow Missile System (NSSMS), Ships Inertial Navigation System (SINS), Intelligence Center (IOIC), and other sensor and electronic warfare equipments such as AN/SPN-43A, AN/SPS-37, AN/SPS-10, AN/SPS-48, and AN/ULQ-6. New systems which will be added to RANGER include Integrated Automatic Detection and Tracking (IADT), Design-to-Price Electronic Warfare (DTPEW), and Task Force Command and Control (TFCC). The combat system on RANGER used over 4008 yards of parallel cable weighing over four tons to transfer digital information between the various computers and peripherals. Limited reconfiguration of the NTDS system is accommodated by a manual switching system weighing one and one-half tons. A block diagram of the interconnections in the RANGER system is shown in figure 1. (Note that neither the peripherals nor the computers of one system can be used as a backup for any other system.)

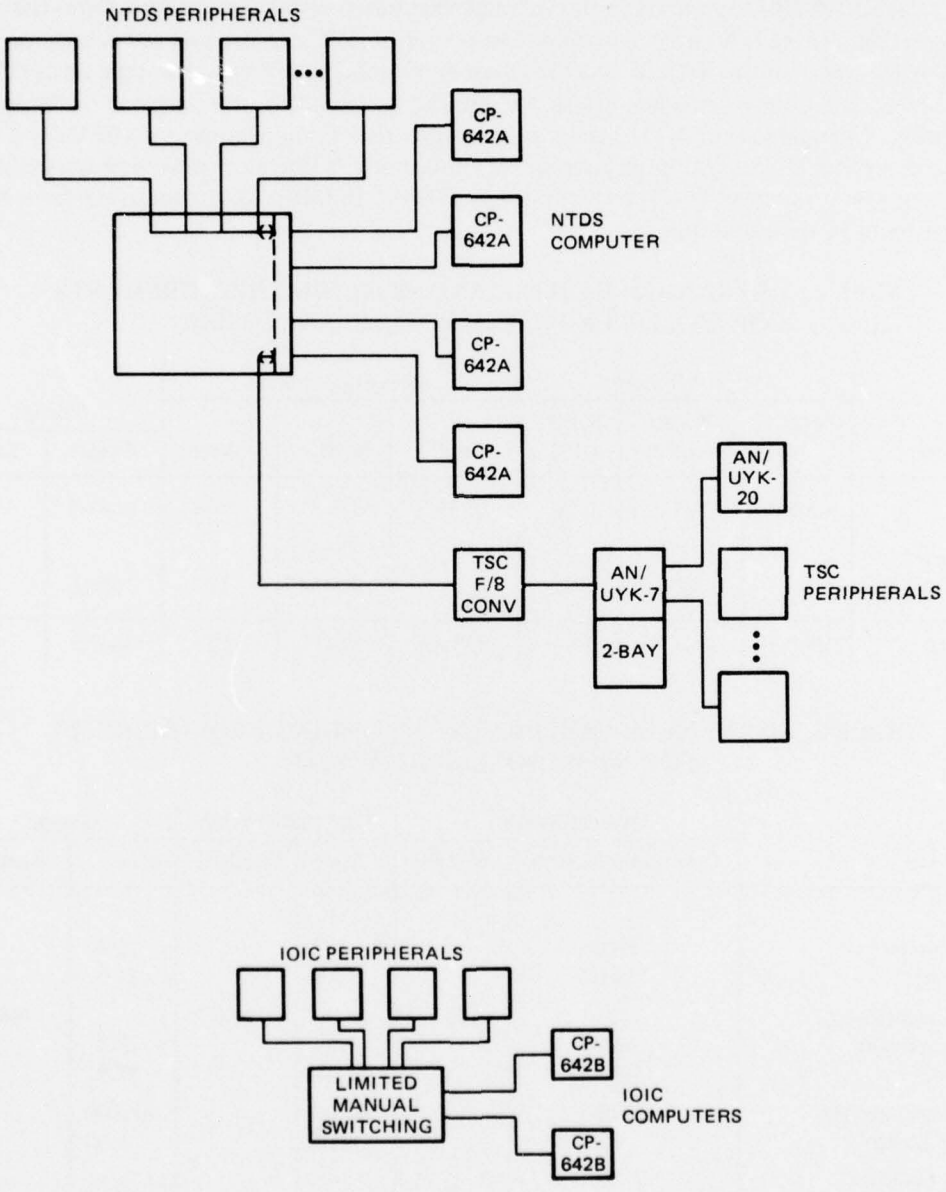


Figure 1. Block diagram of USS RANGER combat system.

Tables 2 and 3 summarize the cabling and switching used in the NTDS system (volume, weight, and dollar analysis). A comparison is made in the table for a similar system using solid-state digital conversion and switching techniques. As will be seen from the two tables, the solid-state system costs some 355 thousand dollars more than the present system but its installation would result in weight savings of almost 5 tons.

On RANGER, computers in the Intelligence Center system are isolated from the NTDS system. There is no way the computing power of IOIC can be used as backup for NTDS or for TSC. In the RANGER NTDS system, two 2-channel magnetic tape units (MTUs) are used. Channel one of either MTU can be selected for connection to any one of the system computers. Channel two of MTU-1 goes only to computer C and channel two of MTU-2 goes only to computer D. Special interfaces for NTDS fast and NTDS slow must be inserted whenever a new system such as TSC is to be joined to NTDS. In this case, the interface for a single channel costs 30 thousand dollars.

TABLE 2. USS RANGER CABLING AND SWITCHING REQUIREMENTS FOR NTDS (WEIGHT AND VOLUME ANALYSIS)

Item	Present System			Solid-State System			Savings	
	Length (yards)	Weight (pounds)	Space (ft^2)	Length	Weight	Space	Weight	Space
Cable	4008.3	8417.5	N/A	3333.3	370.0	N/A	8047.5	
Switches/ Converters (85)		3000.0	96		1400.0	12	1600.0	84
TOTALS	4008.3	11417.5	96	3333.3	1770.0	12	9647.5	84

TABLE 3. USS RANGER CABLING AND SWITCHING REQUIREMENTS FOR NTDS (DOLLAR ANALYSIS)

Item	Present System		Solid-State System		Savings	
	Cost (dollar $\times 10^3$)	Number	Cost	Number	Cost	Number
Cable						
Procurement	28.0		0.7		27.3	
Labor*	24.0		3.0		21.0	
Connectors (80-pin)		612		224.0		388.0
Procurement	36.7		13.4		23.3	
Labor**	48.9		21.1		27.8	
Switches/Converters	120.0		605.0		-485.00	
TTY Switch	1.0		0.0		1.00	
Special Interface						
TSC (fast/slow)	30.0		0.0		30.0	
TOTALS	288.6		643.20		-354.60	

*0.1 to 0.2 manhour per foot (1 manhour = $20)
**4.0 manhour per connector

Reconfiguration to accommodate a reduced capability program is accomplished using eight banks of switches having 15 switches per bank. The time to accomplish this is far in excess of acceptable limits for combatants.

USS TARAWA (LHA 1)

The combat system on TARAWA is being expanded. The initial system consisted of an AN/UYK-7 (3-bay) computer and associated peripherals. This system was also used for processing supply data and other secondary uses. The modification to TARAWA plans to add an AN/UYK-7 (2-bay). The intent is to add on equipment to perform the supply and other functions and to act as a backup for the original combat system. A block diagram of the TARAWA system is shown in figure 2.

The magnetic tape units are hardwired to the AN/UYK-7s with the exception of one channel which can be switched to an external communications system. Loading of cabinets one and two of the three-bay computer is accomplished by cabinet zero. A failure in cabinet zero will cause the entire three-bay system to be inoperable and a reduced two-bay program could not be loaded into the three-bay system. The backup system could, however, be loaded with a two-bay program. A unique feature of the LHA operational program is the ability to change the purpose of an input/output (I/O) port. If an I/O port fails, or if a cable or connector fails, it is possible to change the port address allowing communication through an alternate port and cable. The configuration management and configuration versatility of the TARAWA system are extremely limited and do not allow use of this ability. Tables 4 and 5 summarize the cabling and switching used on TARAWA combat systems before and after the system is expanded. A comparison is made in the tables for a similar system using solid-state digital conversion and switching techniques. The advantages which can be realized using the newer techniques are contained in a later paragraph of this report.

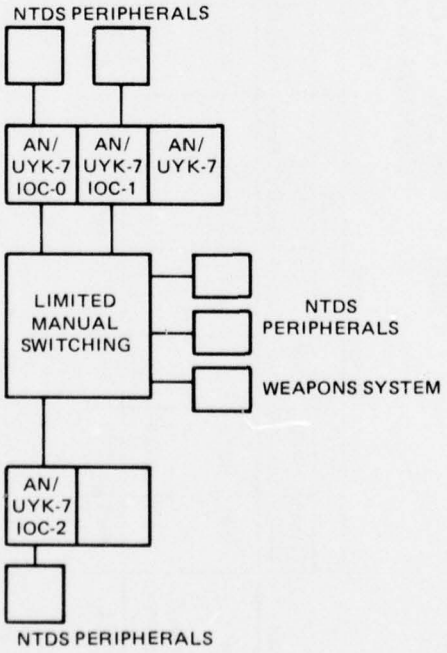


Figure 2. Block diagram of USS TARAWA combat system.

TABLE 4. USS TARAWA CABLING AND SWITCHING REQUIREMENTS FOR NTDS (WEIGHT AND VOLUME ANALYSIS)

	Present System						Solid-State System						Savings					
	1 CPU			2 CPU			1 CPU			2 CPU			Old			New		
Item	Length (yards)	Weight (pounds)	Space (ft^2)	Length	Weight	Space	Length	Weight	Space	Length	Weight	Space	Length	Weight	Space	Length	Weight	Space
Cable	4405	3127.5		1750	1242.5		4360	161.0		1066	59		45	2966.5		150	1183.50	
Switches/ Converters		1200.0	18		300.0	6.0		1000	12.0		120	0.0		200.0	6.0		180.00	6.0
TOTALS	4405	4327.5	18	1750	1542.5	6.0	4360	1161.0	12.0	1066	179.0			3166.6	6.0		1363.50	6.0

TABLE 5. USS TARAWA CABLING AND SWITCHING REQUIREMENTS FOR NTDS (DOLLAR ANALYSIS)

Item	Present System		Solid-State System		Savings	
	1 CPU	2 CPU	1 CPU	2 CPU	Old	New
Cable						
*Labor	66.1	26.2	8.2	3.0	57.9	23.2
Connectors	(182)	(46)	(49)	(8)	(133)	(38)
Procurement	9.0	2.3	2.5	0.4	6.5	1.9
Labor	14.6	3.7	3.9	0.6	10.7	3.1
Switches/ Converters						
Procurement	40.0	13.3	605.0	20.0	-565.0	-6.7
TOTALS (dollars $\times 10^3$)	129.7	45.5	619.60	24.0	-489.9	21.5

*0.1 to 0.2 manhour/foot

SHIPBOARD CONVERSION AND SWITCHING SYSTEMS (SCSS)

SYSTEM DESCRIPTION

The purpose of SCSS is to interconnect all tactical computers, peripherals, and weapons systems on the ship, thereby allowing any channel of any equipment to be electrically connected to any channel of any other equipment. Certain interconnects can be prohibited if desired. SCSS provides electrical ports with a common interface for new systems when expansion is required. Individual systems stand alone as compartmentalized units at remote locations throughout the ship, communicating via coaxial cable and the computer-controlled switch. SCSS communicates with all tactical computers, performing fault isolation and compensation. The reliability of the entire tactical weapons system is improved because the compartmentalized, fault-compensating, SCSS also provides redundant signal paths for all equipments. The cost of a tactical weapons system with SCSS is initially greater than one without. However, the costs of adding new systems or modifying old ones are greatly reduced because of the serial signal standardization which SCSS provides. These attributes are discussed in greater detail in the following paragraphs.

EXPANSION

The hub of the SCSS is the crosspoint matrix. The size of the matrix, ie, number of inputs and outputs, depends upon the complexity of the tactical weapons system which is to be interconnected. If the system is small, such as in a DLG, one crosspoint matrix associated with the NTDS suite is adequate to allow the interconnection of all tactical computers and equipments. If the system is more complicated, several crosspoint matrices may be required. System expansion is accommodated by trunking the matrices as shown in figure 3. The nodes of this expandable system are actually the crosspoint matrices. Note that alternate routes are available from one node to another. Figures 4, 5, and 6 reflect the concept of expandability.

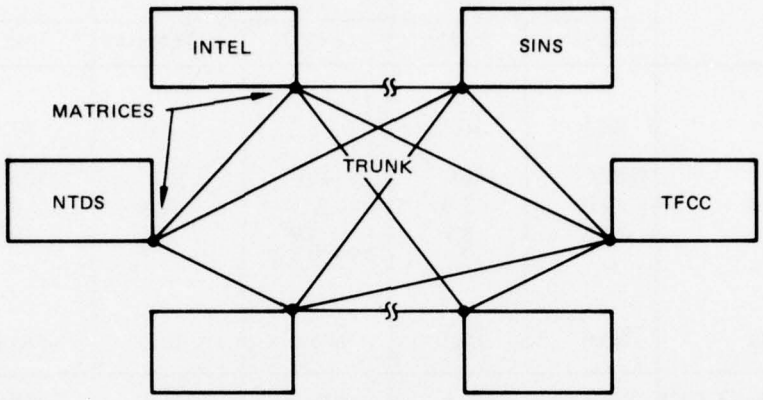


Figure 3. SCSS compartmental expandable system.

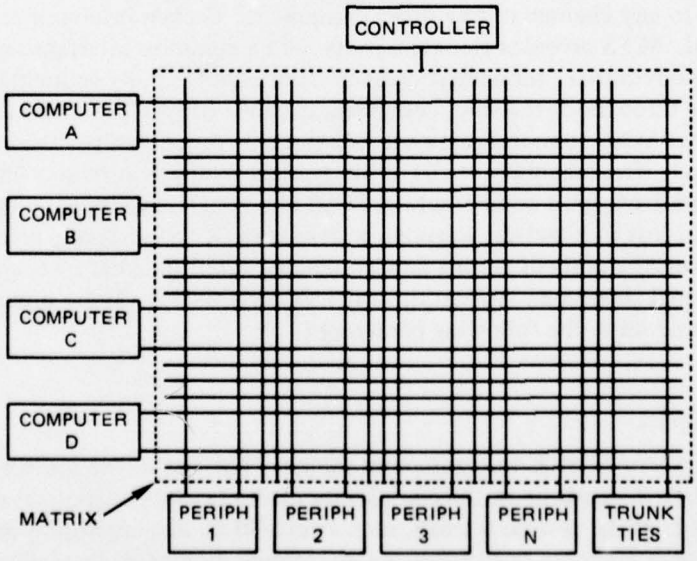


Figure 4. SCSS stand-alone system.

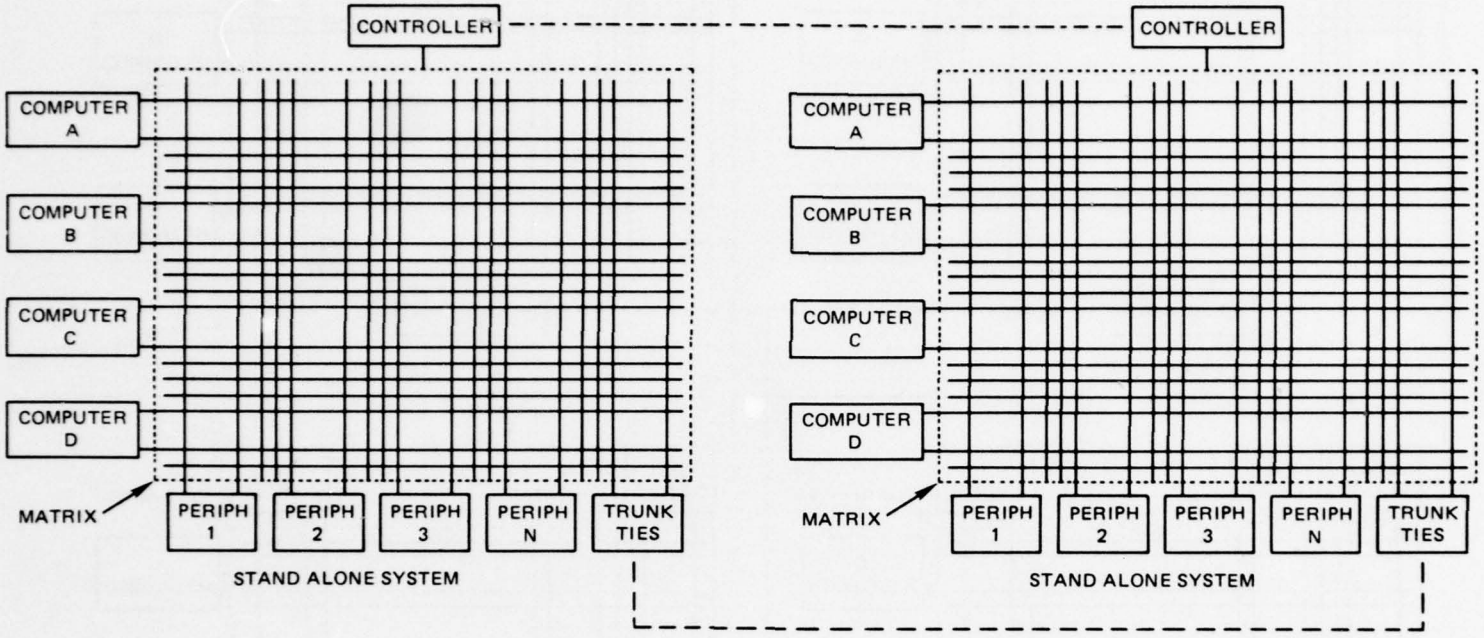


Figure 5. SCSS expandable (dual) system.

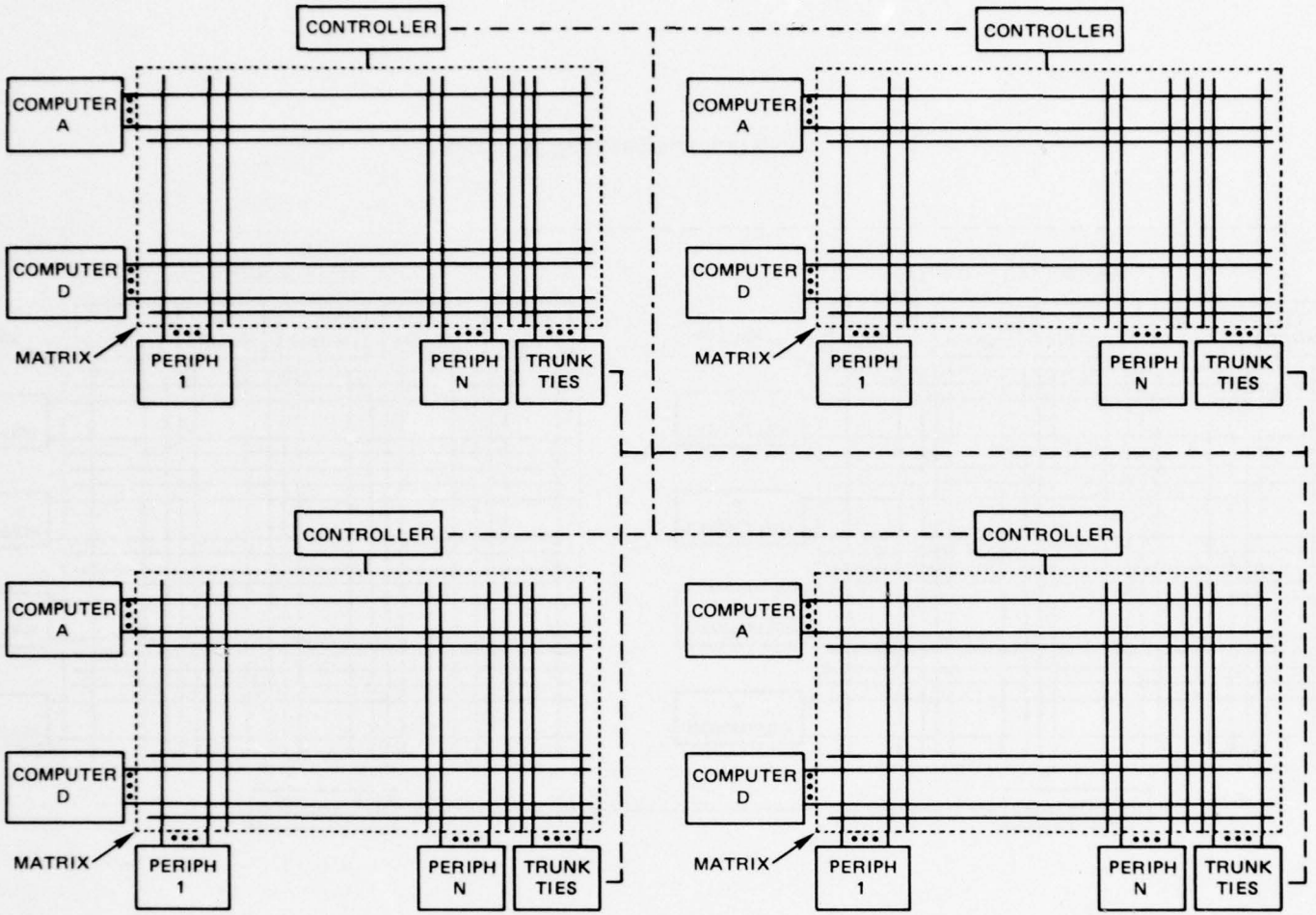


Figure 6. SCSS expandable (multiple) system.

Note that the matrix controllers are interconnected. This allows for local configuration control, such as is desired in an intelligence suite, and global configuration control, such as is desired from display and decision in CIC.

COMPARTMENTATION

SCSS links the various systems which comprise the tactical weapons system. Each of the individual systems stands alone, performing its function in a remote compartment best suited for the function. The interconnection is accomplished by redundant coaxial cables carrying serial data. Compartmentation of this type reduces the likelihood that the entire system will fail as a result of a single catastrophe, eg, battle damage. Compartmentation is also conducive to the "SEAMOD" modular approach which is desirable in new construction. The modular, compartmental concept is shown in figure 3.

FAULT COMPENSATION

SCSS uses a control computer (Data General NOVA or equivalent) to control the tactical weapons-system configuration. The control computer carries on a dialogue with the tactical computers, continuously inquiring into the "health" of the various systems. As shown in figure 7, when a system has a fault such as an I/O port failure or CPU failure, the control computer compensates for the fault by instructing the tactical computer to use an unused I/O port or by substituting a predesignated backup computer for the faulty one. All channels of the entire tactical weapons system are available in SCSS. This means that a computer in a lesser system, such as Intelligence, can be substituted for a primary computer, such as in Weapons Control, if the need arises. The beauty of SCSS is that the fault compensation is automatic and does not wait for a human decision. Of course, the option to go automatic or manual is available.

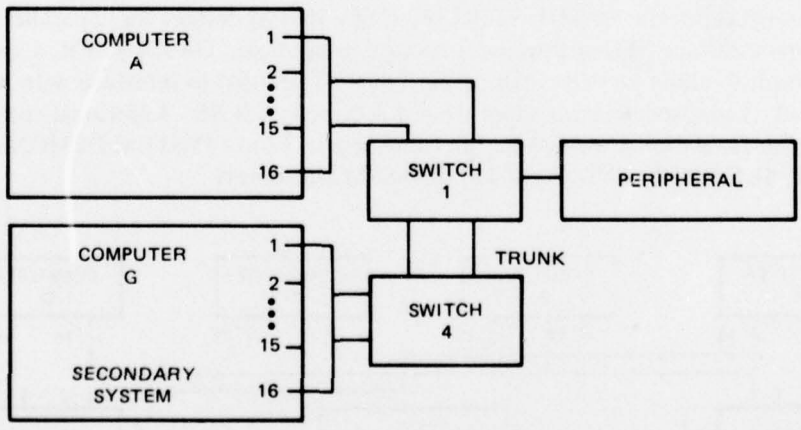


Figure 7. Fault compensation in SCSS accommodating a faulty I/O port or computer by substituting a functioning one.

RELIABILITY

SCSS improves the reliability of the tactical weapons system by reducing the number of cable drivers and receivers for each input or output port from 36 to two. Each of the two cables carries identical, redundant signals which are routed through different cable ways. Dual, redundant matrices, controllers, and trunk ties are also provided in SCSS. In addition to the system redundancy, the fault compensation mentioned in the previous paragraph greatly enhances the tactical weapons-system reliability. Figure 8 shows how the computers and peripherals are interfaced using the redundant SCSS. Duplicate signals leave from a port (eg, computer A) on identical cables via redundant switch matrices to the destination (eg, peripheral). At the receiver, the hardware searches for either signal and locks onto the first one it detects. If the signal being tracked drops out, the hardware again searches for a signal and locks onto the first one it detects.

COST

A cost analysis of the NTDS system aboard USS RANGER indicates an additional cost of $354.9K would have been realized in RANGER if SCSS had been installed when NTDS was originally put aboard. This figure does not include the saving which would be realized because the original installation as well as the additions of new components to the system would take less time and the ship would become operational sooner. A similar analysis for USS TARAWA was conducted. An NTDS modification has been proposed for TARAWA. Two analyses have been performed for this purpose; one for the system as it now exists and one to reflect the proposed modification. Installation of SCSS on TARAWA would have originally cost an additional 490 thousand dollars while a saving of 25.5 thousand dollars would have been realized in the intended modification of the system. On RANGER, the total weight saving is 4.8 tons and on TARAWA, 1.6 and 0.7 tons are saved for the two cases.

STANDARDIZATION

One of the advantages of SCSS is its ability to interconnect equipments which have differing electrical interfaces. MIL-STD-1397 (NAVSHIPS) defines three parallel interfaces and one serial interface. These interfaces are not compatible. On RANGER, a special converter was built to allow two channels of the TSC (NTDS fast) to interface with NTDS (NTDS slow). These special converters are not required in SCSS. Additional comments regarding standardization are contained in following sections (SYSTEM DEMONSTRATION AND TEST, SUMMARY AND CONCLUSIONS) of this report.

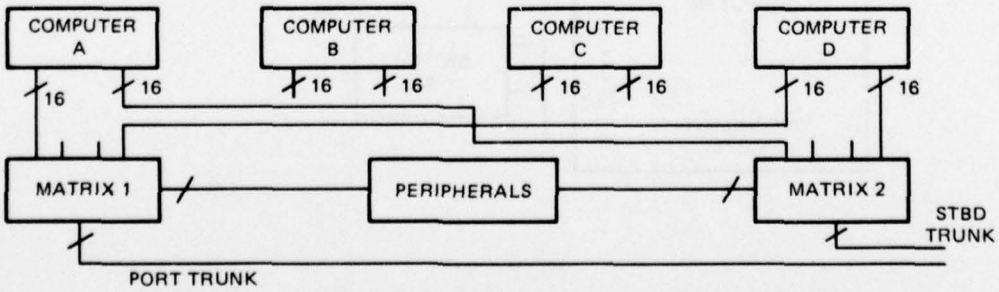


Figure 8. Redundant paths and matrices in SCSS.

SYSTEM DEMONSTRATION AND TEST

GENERAL INFORMATION

Three shorebased activities are employing conversion and switching techniques. These systems, of themselves, demonstrate the techniques and some benefits which are applicable to shipboard use. (Functional descriptions of these systems are included in Appendixes A, B, and C.) All of the attributes cited in the previous section are planned for an SCSS demonstration.

Some additional comments concerning standardization need to be made. In each of the shore-based systems, a conversion from NTDS parallel to some nonstandard serial format and back to parallel is accomplished. Since the serial formats are nonstandard, it is necessary to show, in a separate demonstration, that the MIL-STD-1397 definition for serial interface could be applied to SCSS as well. An alternate switch matrix has been designed and tested which is capable of handling bidirectional analog signals such as the MIL-STD-1397 serial signal.

DIGITAL SYSTEM

The digital system to be used to demonstrate the attributes of SCSS is the AN/USQ-62(X). The AN/USQ-62(X) is augmented by hardware designed as part of this project. The system demonstration has not been accomplished at this writing because of interference from construction in the facility where the system is located. A discussion of the demonstration, hardware, and software developed for the demonstration, and related facts in existing, functioning switching systems are presented here. A supplement to this report will be submitted as an appendix under separate cover when the demonstration is completed.

SOFTWARE DEVELOPMENT

There are two software packages which have been developed for the SCSS demonstration. One software package is for the Data General NOVA computer which controls the switch matrix and carries on dialogue with the tactical computers. The other software package is for the tactical computers. Initially, the intent was to use an unaltered tactical, operational program in which the dialogue allows for the changing of the I/O port usage. Such a program exists for USS TARAWA; however, it is written for use on a three-bay AN/UYK-7 computer. For this demonstration, only one-bay AN/UYK-7s are available. Therefore, a program has been written which will allow the inter-computer dialogue, provide for the changing of the I/O port, and drive a display so that the effects of inducing failures can be monitored.

HARDWARE DEVELOPMENT

Hardware which has been developed to demonstrate the concepts of SCSS is designed to augment the AN/USQ-62(X) system. Each of the fabricated elements performs a unique function which contributes to the implementation of SCSS. Each is described briefly here and in detail in Appendixes D thru F. The Data General NOVA control computer has been redesigned to accommodate a special I/O structure which will allow it to communicate with the tactical computers and to perform the control function required for start-up, loading, and the like. A special converter card for the tactical computer converters has been designed which allows the control computer to perform the SMP functions. New converter cards, both transmit and receive, which provide redundant signal paths, have been fabricated.

ANALOG SYSTEM

It is desirable to use the MIL-STD-1397 serial format as the standard serial format for SCSS. This format requires half-duplex operation over a single coaxial line. Inserting a solid-state switching matrix in a half-duplex path requires that the solid-state devices pass signals in both directions. A new device has been procured which can be cascaded to form a large bidirectional switching matrix. The device, a Signetics SD3501 D-MOS switch, has been cascaded to form a 16-by-16 bidirectional analog matrix. Tests have been conducted on the analog matrix to determine whether it can be used in the SCSS application. The test results are contained in Appendix G. The results indicate that the device tested is not adequate to perform the SCSS function. It is very close, however, and a similar device designed for high-frequency application is feasible. In lieu of this alternative, a much simpler solution would be to change the standard to one which can be handled by the existing switching system.

APPLICATIONS

ANALOG VIDEO DISTRIBUTION

The Signetics device, SD5301, while not adequate for SCSS is useful in applications at lower frequencies. One such use is currently being addressed in the Integrated Combat Systems Test Facility (ICSTF) at San Diego. In this facility, it is desirable to switch the analog video signals which are distributed to many display units. In this application, the analog signals are unidirectional and receivers and transmitters buffer the switching devices. The switch will be under the control of the AN/USQ-62(X) system.

ANALOG AND DIGITAL TECHNICAL CONTROL

Technical control of an entire communications suite can be achieved by use of analog and digital switching matrices. Figure 9 shows how strings of devices can be created for use in a command-post, communications-support facility.

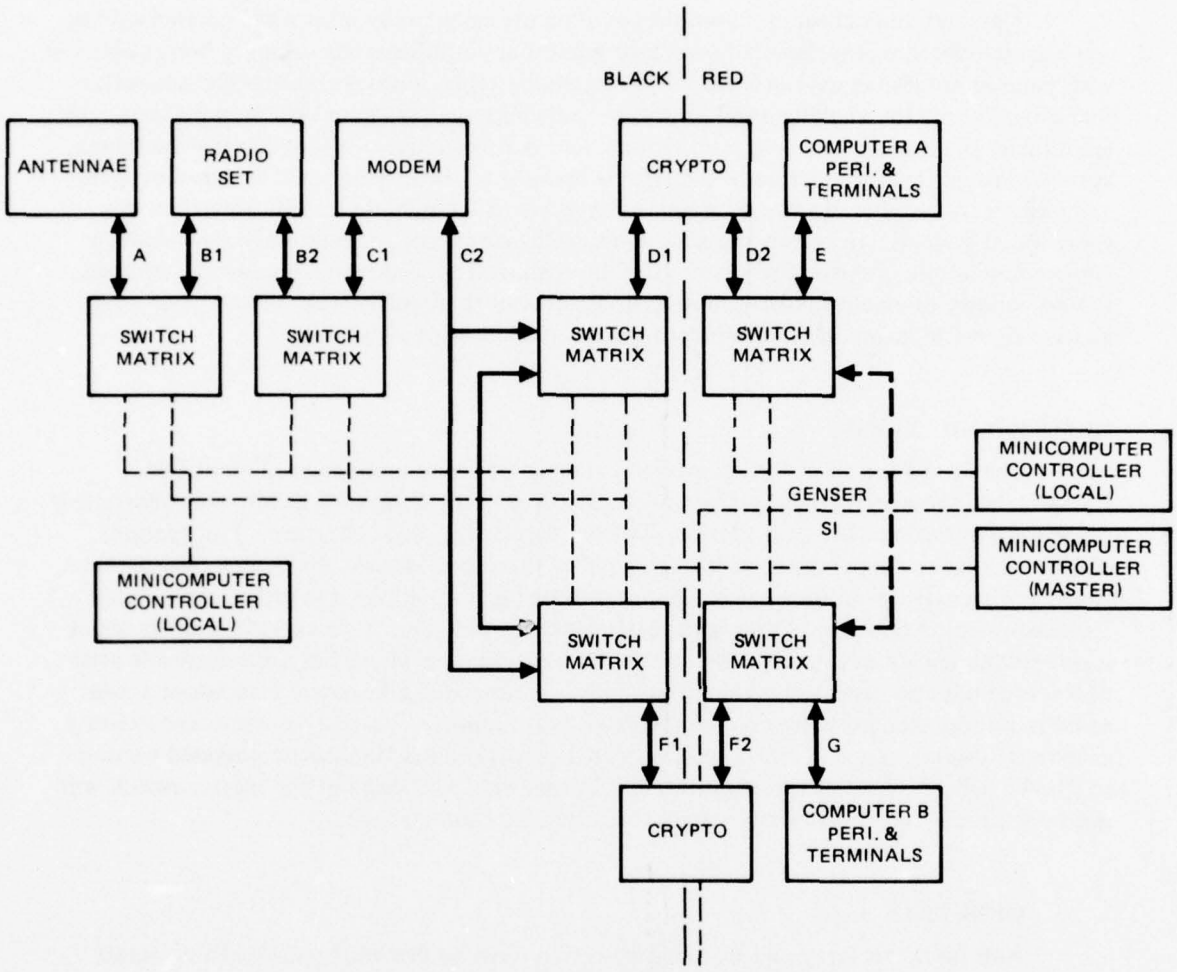


Figure 9. Implementation with a master technical control and local controls.

SUMMARY, CONCLUSIONS, AND RECOMMENDATIONS

SUMMARY

Shore-based solid-state switching systems have been examined and compared. Shipboard requirements for a solid-state switching system have been identified. A model of a solid-state switching system for shipboard use has been assembled. An alternate analog switching model has also been designed, fabricated, and tested for use with the MIL-STD-1397 serial interface. Other applications for the analog switch have been identified.

CONCLUSIONS

The interconnection of computer components using bulky, expensive parallel cabling and manual switches is archaic. Shore-based computer complexes have already been improved with parallel-to-serial converters, solid-state matrix switches, and serial-to-parallel converters. The driving force for implementing solid-state switching systems has been the need to rapidly reconfigure the shore-based computer complexes. A by-product of the solid-state switching system is a significant reduction in the size and weight of the interconnect system (ie, cables and switches). Shipboard systems are considerably smaller and less complicated than the shore-based systems. However, the need for a rapid, automatic reconfiguration mechanism is more crucial. In combat, there is no time for technical decisions to be made. In combat, the probability of an equipment failure is much greater than normal, eg, a hit or near miss, and the need for automatic fault-detecting and -compensating is critical.

RECOMMENDATIONS

The need for a shipboard conversion and switching system has been identified. Research has shown that there are several alternatives in the design for SCSS. One alternative centers around using the current MIL-STD-1397 format for serial interface. This requires additional research and design work since none of the shore-based systems uses this standard. Another alternative would be to change the standard and militarize one of the shore-based systems for shipboard use. Although this alternative would be the quickest to implement, it is not recommended because, while each of the shore-based systems has some desirable attributes, each has also certain shortcomings. The recommended alternative is to adopt a new serial interface standard which is compatible with an improved version of one of the existing switching systems. Specifically, a unidirectional asynchronous Manchester encoded version of the AN/USQ-62 format is recommended. In this way, a redesign of the matrix switch will not be required. The SCSS should meet the following characteristics.

GENERAL

Automatic recovery and/or reconfiguration must be provided along with universal configuration management and sharing of backup equipment. As compared to existing systems size and weight must be greatly reduced and costs must be held to current installation levels. The SCSS must be designed with redundant capabilities, be expandable, and use a standard interface format.

CONVERTERS

Converter clocking shall use asynchronous techniques (ie, no separate clock cables). Converter timing shall be maximized to permit the use of existing diagnostic or operational software without the need for timing modifications to that software. Converters shall be mounted in easily maintained racks (with provision for future installation within equipment). Loss of synchronization or lack of synchronization between transmitting and receiving converters shall disable all control signals and generate a system alert. Converters shall be capable of interfacing with equipment using all MIL-STD-1397 interface signals. (Existing equipment now meeting current MIL-STD-1397 specifications will be treated as special cases.)

SWITCH

The switch shall have a module size of 64 by 64 and be capable of expansion to 256 by 256. It shall be functionally nonblocking and shall be asynchronous (ie, data clock from converters shall not be required). The switch shall contain Built-In-Test Equipment (BITE) for data-path variation, incorporate redundant power supplies, and be computer-controlled for path selection. Pulse width distortion shall not exceed MIL-STD-1397 or equivalent specifications. Failed cards shall be capable of being removed from the switch without removal of power and the Mean Time to Repair (MTTR) must incorporate a minimal time specification. Manual bypass of the switch shall be provided.

APPENDIX A: A FUNCTIONAL DESCRIPTION OF THE AN/USQ-62(XG-2) CONVERSION AND SWITCHING SYSTEM (CSS)

Appendix A is an excerpt, Chapter 5, from the Technical Manual for Operation and Maintenance of AN/USQ-62(XG-2). Note that the term "high speed data switch" (HSDS) may be used throughout to mean either the CSS system in general or, specifically, the switching matrix.

CHAPTER 5

FUNCTIONAL DESCRIPTION

5-1. INTRODUCTION. This chapter provides a functional description of the AN/USQ-62(XG-2)(V) Conversion and Switching System. The description is presented at two levels; overall, and detailed. The purpose of this discussion is to provide the technician with an understanding of the functional capabilities of the HSDS system as an adjunct to troubleshooting and corrective maintenance. The level of the description is consistent with the maintenance philosophy, i.e., troubles will be isolated to a specific equipment whereupon the respective equipment manual is consulted to identify the defective card or major component to be replaced. Hence, detailed descriptions of individual equipments or circuit elements are not included herein.

5-2. OVERALL FUNCTIONAL DESCRIPTION. The primary function of the HSDS system is to permit rapid interconnection of equipment input and output data channels and also to permit rapid reconfiguration of existing switch connections. In addition to switching, the HSDS system also provides the function of simulation. The simulation function is ancillary. It need not be operational for the HSDS system to perform its primary function. Figure 5-1 is a breakdown of the various functions performed by the system. A description of how each function contributes to the overall system function, and also the ancillary function of simulation, is described in subsequent paragraphs.

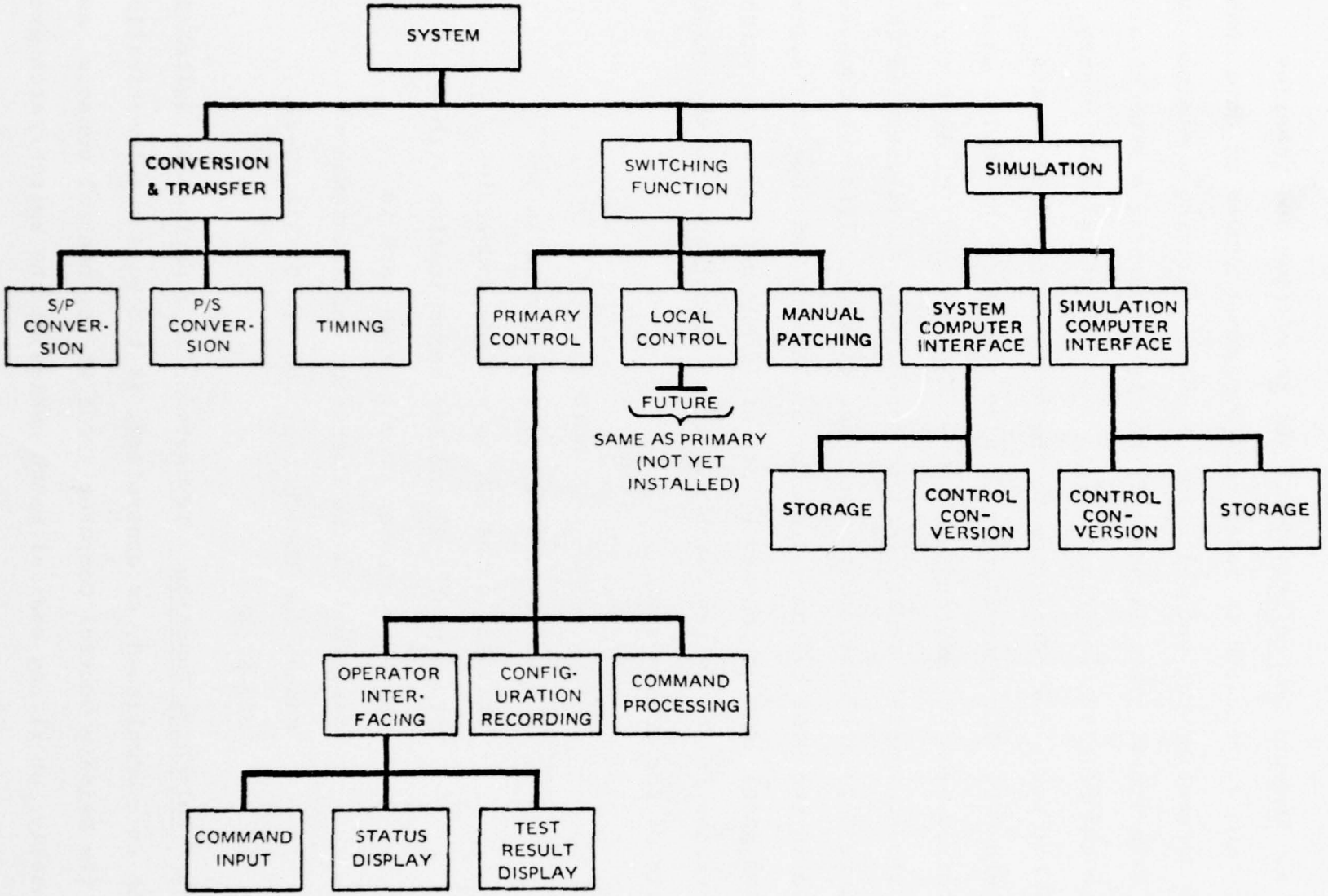


Figure 5-1. Breakdown of System Functions

a. Conversion and Transfer. The conversion and transfer function is required to facilitate a maximum number of data channel I/O connections at the switch/patch panel utilizing a minimum number of data lines. This is accomplished by converting a NTDS parallel data channel (40 lines/channel) to a single serial line channel (40 bit word) for connection to the switch/patch panel. See figure 5-2. The converters must also reconvert the serial data received from the switch/patch panel back to parallel data for input to the equipment. Three types of converters, as illustrated in figure 5-2, are required to interface with the different computers used in the NTDS system. Transfer of data to and from the switch/patch panel is synchronized by use of 10 MHz central clock which is generated in the switch/patch panel and distributed to the various units of the HSDS system.

NOTE

A special parallel-to-serial card is installed in the PCC to provide conversion of control commands for communication with the switch/patch panel. This card is described in the Operation and Maintenance Manual for the Control Console OJ-332(XG-2)/USQ-62(V).

b. Switching Function. The setting of a particular switch I/O path is accomplished, or controlled, in two ways: automatically by the Primary Control Computer (PCC) at the control console, and manually, utilizing coaxial patch cables at the switch/patch panel.

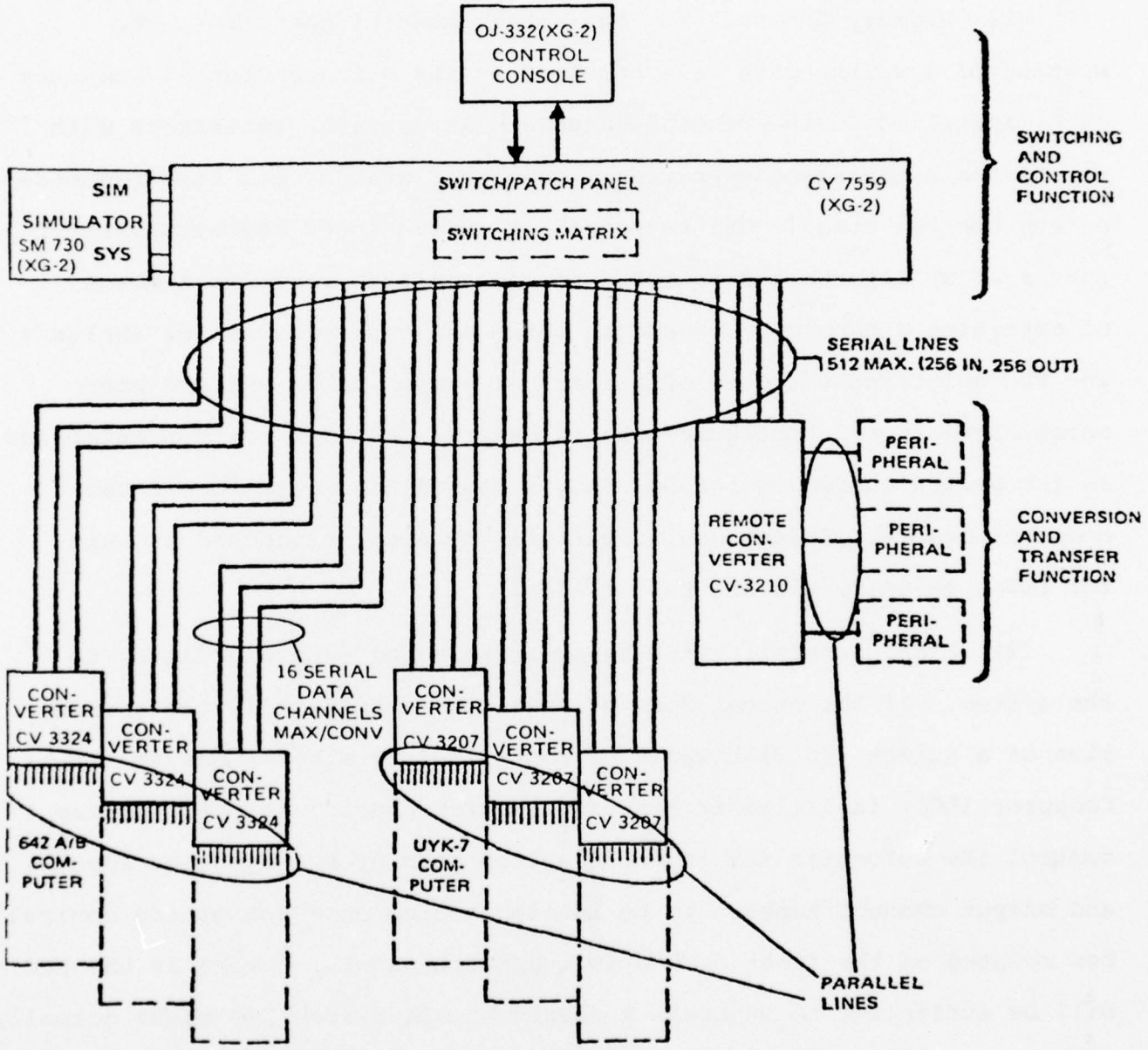


Figure 5-2. System Functional Block Diagram

It is anticipated that in the future, a third method will be available whereby switching is automatically accomplished by a Local Control Computer (LCC) at the switch/patch panel.

(1) Primary Control. In the normal mode of operation, the setting of a switch path is controlled by the Primary Control Computer (PCC) installed in the control console. An operator interfaces with the system by entering cperational commands, status, and test requests on the control console CRT keyboard. A medium speed keyboard/printer serves as an alternate data entry device and also provides a means of obtaining a hard copy of switch paths and test results for analysis. The PCC maintains a record of all actual switch paths set and pre-established stored configurations in memory. An operator can establish an I/O switch configuration by using a stored configuration in the computer memory. Switch configurations can also be punched on tape for later re-entry via the tape reader.

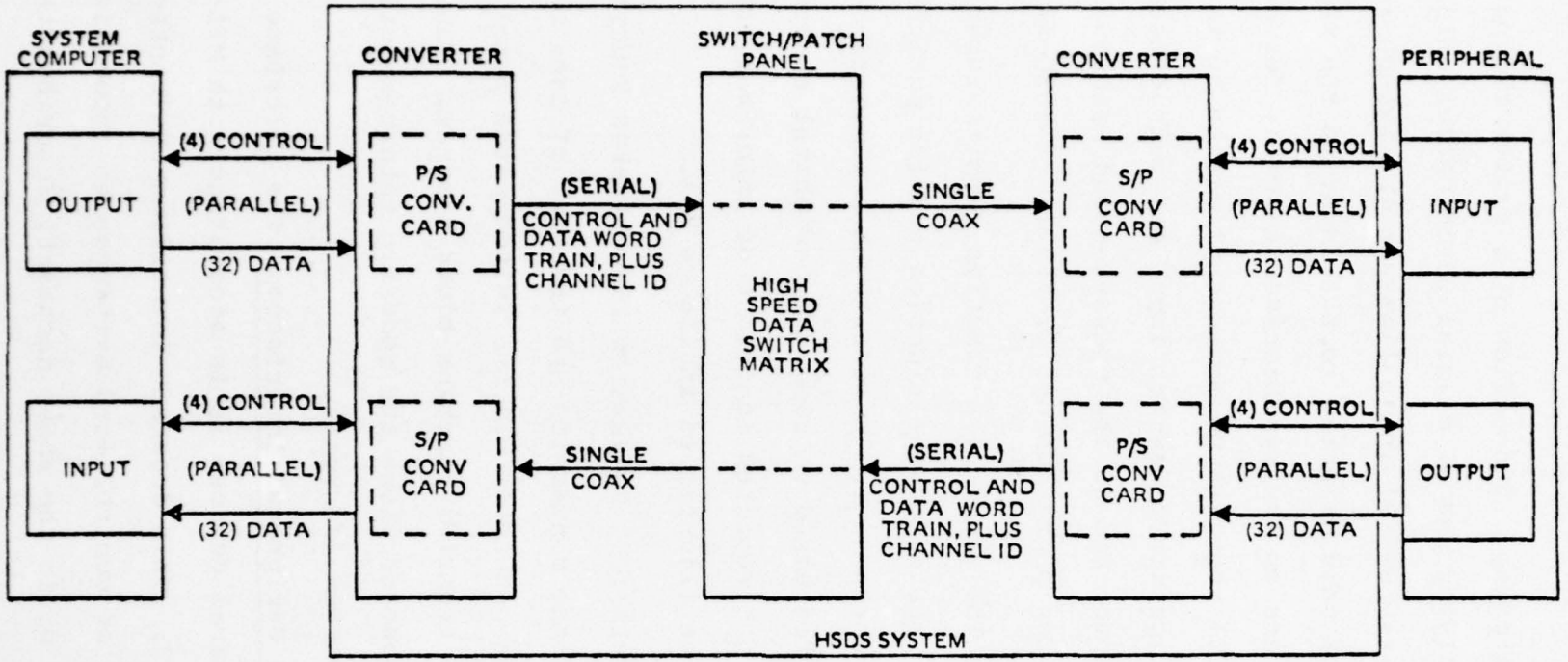
(2) Local Control. This is an anticipated future addition to the system. If the normal mode of operation should fail, the connection of a switch I/O path would be controlled by a Local Control Computer (LCC) installed in the switch/patch panel. An operator may control the automatic setting of a switch path by entering the input and output channel numbers to be interconnected on a pushbotton control box mounted on the front of the switch/patch panel. Memory in the LCC will be sufficient to maintain a record of all switch I/O paths actually set. This feature would permit rapid return of control to the PCC when the latter becomes operational. LCC control of the switch/patch panel, with the exception of a few commands, will be equivalent to PCC control.

(3) Manual Patching. Connection of a switch I/O path can be accomplished manually by use of coaxial patch cables which bypass the switching matrix. Serial input lines at the switch input connector matrix are patched directly to the input of the repeater/distributor amplifiers on the synchronizer assembly for output. Manual patching still requires DC power application to the synchronizer. Identification of switch input and output terminals for manual patching is provided in the Operation and Maintenance manual for the Electrical Equipment Cabinet CY-7559(XG-2)/USQ-62(V).

c. Simulation. The simulation function permits interface of NTDS computers on computer channels designated for peripherals. The simulator normally works in conjunction with a simulation computer which is software programmed to simulate peripheral equipment. The simulator provides the required functions of interface, storage, and control conversion as illustrated in figure 5-1.

5-3. DETAILED DESCRIPTION, CONVERSION AND TRANSFER FUNCTION. This paragraph describes the conversion and transfer of data between equipments which are interconnected via the switch/patch panel. Figure 5-3 is a conversion and transfer function block diagram. Figure FO-1, at the rear of this document shows the specific interconnection of control and data signals between I/O ports.

a. Computer and Peripheral Interfaces. The inferface between an NTDS computer and peripheral devices is in accordance with MIL-STD-1397 (SHIPS) dated 30 August 1973. This document identifies the control signals, timing and sequence of control word exchanges to accomplish a data word transfer. Appendix B, in the above document, describes the special requirements for computers CP-642A/B.



NOTE: THE INPUT AND OUTPUT PORTS SHOWN ON THE PERIPHERALS ABOVE REPRESENT DATA FLOW, RATHER THEN SOME COMPUTER/PERIPHERAL INTERCONNECTION CONVENTION.

Figure 5-3. Conversion and Transfer Block Diagram

b. HSDS Data Conversion Rate. Parallel data input to a HSDS system must necessarily be converted to serial and then back to parallel for output to the NTDS equipment. See figure 5-3. The time to accomplish this conversion and reconversion in the HSDS converters may in some cases introduce delays which result in a reduction of data transfer rate. The delays encountered in the transfer of data through the switch are negligible in comparison to those introduced in conversion. Therefore, the transfer of data through the HSDS system is limited primarily by the conversion function and is approximately 6.5 megabaud.

c. Parallel Data Levels and Rates. The HSDS interface is compatible with and can accommodate the parallel NTDS or ANEW channel data levels and rates indicated below.

(1) Type A (NTDS slow). Parallel data transfer of up to 41,667 words per second on one cable. Binary voltage levels are 0 Vdc (logical 1) and -15 Vdc (logical 0).

(2) Type B (NTDS fast). Parallel data transfer of up to 125,000 words per second on one cable. Binary voltage levels are 0 Vdc (logical 1) and -3 Vdc (logical 0).

(3) ANEW. Parallel data transfer of up to 125,000 words per second on one cable. Binary voltage levels are 0 Vdc (logical 1) and +3.5 Vdc (logical 0).

d. Control and Data Formats. The serialized control bits used to establish communications between two NTDS devices are illustrated in figure 5-4. The meaning of each control bit is described in tables 5-1 and 5-2. See MIL-STD-1397 (SHIPS) dated 30 August 1973

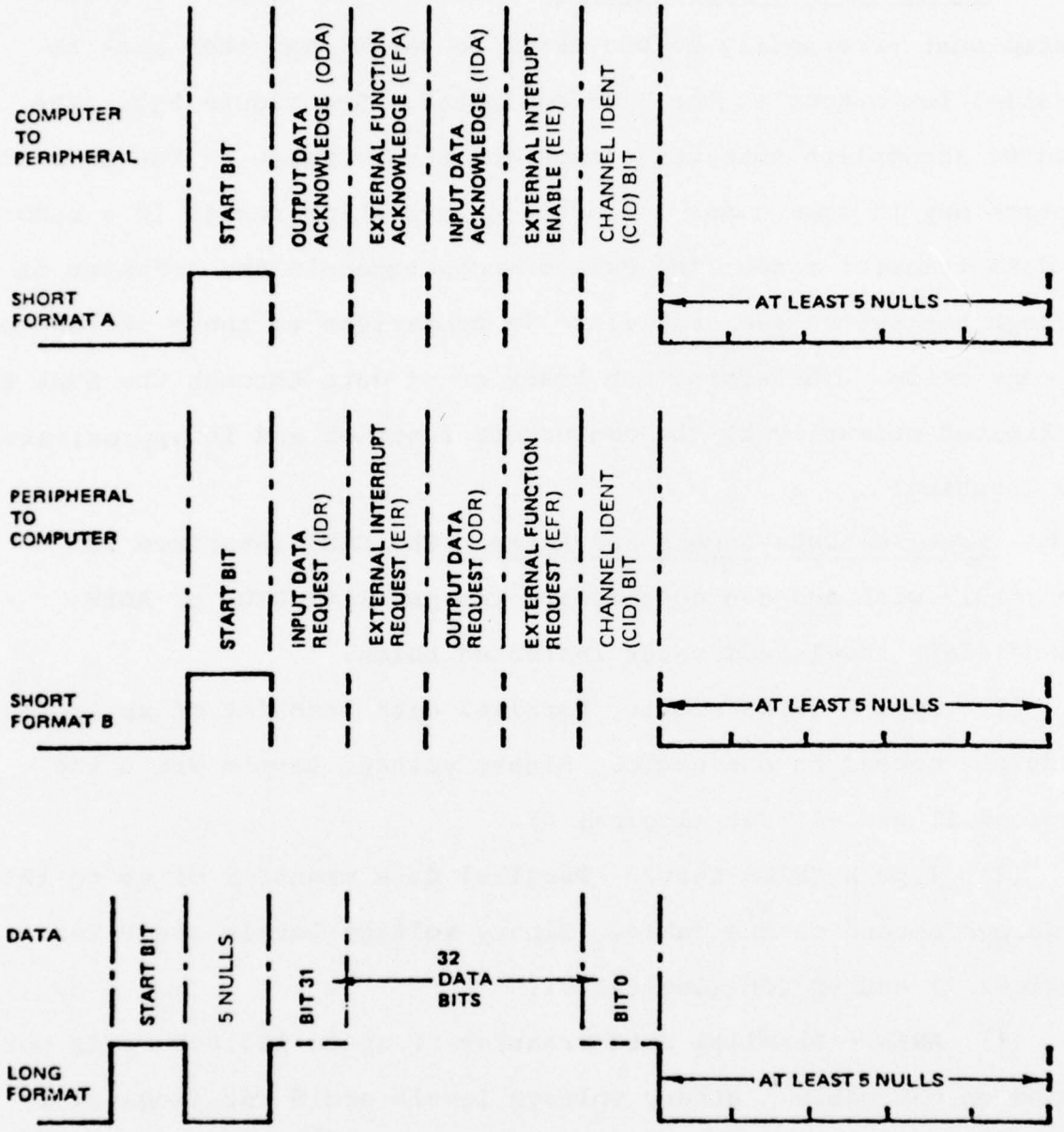


Figure 5-4. Short and Long Transmission Formats

TABLE 5-1. FUNCTION OF OUTPUT CHANNEL CONTROL LINES

Name of line	Direction of signal	Function
EFR[1/]	Peripheral equipment to computer	Set condition indicates readiness of the peripheral equipment to accept an EF code word on that channel.
EFA	Computer to peripheral equipment	Set condition indicates the computer has placed an EF code word on the OD lines of that channel.
ODR	Peripheral equipment to computer	Set condition indicates readiness of the peripheral equipment to accept a word of data on that channel.
ODA	Computer to peripheral equipment	Set condition indicates the computer has placed a word of data on the OD lines of that channel.

1/ Not all computers have the EFR line; see individual equipment specification.

TABLE 5-2. FUNCTION OF INPUT CHANNEL CONTROL LINES

Name of line	Direction of signal	Function
EIE[1/]	Computer to peripheral equipment	Set condition indicates readiness of the computer to accept an EI code word on that channel.
IDR	Peripheral equipment to computer	Set condition indicates that the peripheral equipment has placed a word of data available to the computer on the ID lines of that channel.
EIR	Peripheral equipment to computer	Set condition indicates the peripheral equipmeat has placed an Interrupt Code Word available to the computer on the ID lines of that channel.
IDA	Computer to peripheral equipment	Set condition indicates that the computer has sampled the ID lines of that channel.

1/ Not all computers have the EIE lines, see individual equipment specification.

for sequence of control word exchange. The serial control bit stream and interconnection of control lines are also illustrated in figure FO-1 at the rear of this manual. Once communication is established, the data word follows the control word. Separation between the control word and the data word must be at least 5 nulls. To uniquely identify a channel, a channel identification (CID) bit is added to each transmission of a control word. After 10 transmissions, circuitry within the switch matrix assembles the 10 CID bits into a 10-bit serial chain word for transfer to the primary control computer. A comparison between the input CID bits of a channel and those appearing at the desired output channel of the switch permits verification of an I/O path connection by the primary control computer. The results of the CID comparison test are sent to the CRT for display and also retained in computer control memory as a switch path completion or as a faulty path.

e. Parallel-to-Serial Conversion. Parallel data from NTDS equipment is converted to serial for transfer to the switch/patch panel. This section of the converter, parallel-to-serial (P/S), converts the four parallel control bits into a short format serial control word. (See figure 5-4). Each P/S circuit card also has switches that are preset to identify the channel number assigned to that card. The channel identification bit (CID) is added to the short format control word and appears as bit 5 in the control word. The short format control word is used to establish communications between NTDS equipments. Once communication is established, the 32 bit parallel data word, which has been converted to serial, follows a short format control word. (See figure 5-4). All converter outputs to the switch/patch panel are TTL level (0 to 3.5 Vdc). Details of the parallel to serial conversion

process are contained in the applicable operation and maintenance manuals for the converters.

f. Switch/Patch Panel Serial Transfer. The switch/patch panel is unidirectional switch which does not alter the serial data. The switch, under computer control, can connect any 1 or all 256 serial input channels to any 1 or all of 256 serial output channels. All inputs to, and outputs from, the switch/patch panel are at the TTL level (0 to 3.5 Vdc).

g. Serial to Parallel Conversion. Serial data input to the converter from the switch/patch panel is converted to parallel data for transfer to the NTDS equipment. See figure 5-3. The serial-to-parallel converter circuit card also converts the signal level of the data from TTL (0 to +3.5 Vdc) to NTDS level fast (0 to -3 Vdc), NTDS slow (0 to -15 Vdc), or ANEW (0 to +3 Vdc), depending upon the channel use. See the applicable converter operation and maintenance manuals for details regarding the serial-to-parallel conversion process.

h. Converter Clock. In order to synchronize data transfer in the HSDS system, a 10 MHz central clock is located in the switch/patch panel. The clock signal is distributed throughout the system which can contain multiple switch/patch panels. Only one switch/patch panel generates the central clock. A clock adjustment is provided in each converter.

5-4. DETAILED DESCRIPTION, SWITCHING FUNCTION. This paragraph provides a functional description of the three methods of switch control; primary, local and manual. Figure 5-5 is a block diagram of the switching function.

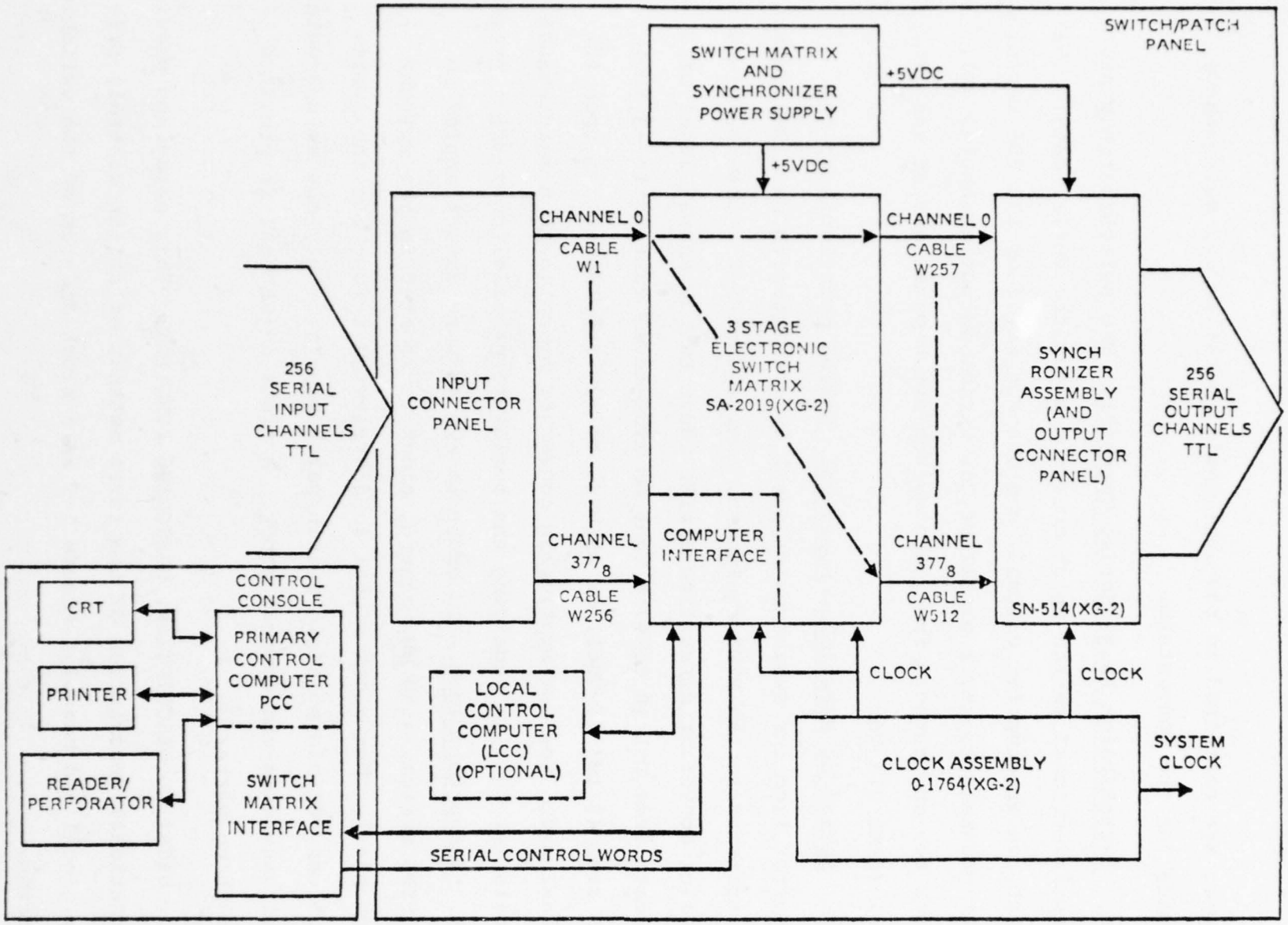


Figure 5-5. Switching Function Block Diagram

a. Primary Computer Control. In the primary mode of operation, switch setting, path verification, recording of set paths and testing of defective paths is controlled by the primary control computer (PCC) installed in the control console. An operator controls the automatic process by entering command data to the PCC via the control console CRT keyboard. An alternate control entry device is the printer keyboard. Rapid setting of a complete switch I/O configuration can be accomplished by entering the configuration data via memory-stored configuration or the tape reader.

(1) Switch Path Setting. The PCC, upon receipt of the instruction word LINK, will connect identified input and output terminals to provide a duplex, simplex, end-around, or plural path. (See chapter 4, section II for a description of switch path types and operation commands.) The PCC executes the command by first checking memory to determine whether the switch input and output ports are in use. If they are, the PCC causes a message to be displayed on the CRT informing the operator that the requested port is in use and the path cannot be set. The operator can designate a different switch path or break the existing path. If the input and output ports are not in use, the PCC will search for an available mid-stage module in the switch to complete the I/O path. When an available mid-stage module is located, the PCC issues a 3-word switch command. The switch command output from the PCC is converted to serial form. (The P/S conversion is accomplished by means of a modification of the PCC consisting of an added circuit board.) Control bits are generated by the PCC to identify which switch/patch panel (1 of 4) is to execute the command. The computer

interface, in each switch/patch panel, receives the serial switch command and converts it to three parallel instruction words. Only the addressed switch/patch panel will process the instruction words. Details of how the switch/patch panel electrically connects the I/O terminals in accordance with the instruction words received from the PCC are contained in the Operation and Maintenance Manual for the Electrical Equipment Cabinet CY-7559(XG-2)/USQ-62(V).

(2) Switch Path Verification. As each path is set, the computer program enables a test signal generator in the switch/patch panel, which injects a coded signal into the input interface card previously selected by the switch I/O command. The output signal from the selected output interface card is then compared to the input signal in the test signal generator card, and the comparison result is issued to the PCC via the computer interface. In addition, the CID bits used to identify a channel are assembled and are output as part of the serial word sent to the PCC switch matrix interface. See Figure 5-5. The serial word from switch/patch panel #1 is converted to parallel for output to the PCC data bus. The PCC evaluates the comparison result and the CID to determine if a switch I/O path has been set successfully. A message is issued for display on the CRT that the switch path is set, or that setting of the path cannot be verified or accomplished.

(3) Recording of Switch Paths. The PCC, upon evaluating whether a switch path is set correctly or not, will cause the information to be stored in memory. If the path is set correctly it is so recorded, as in the type of path set (duplex, simplex, etc). If the path cannot be set, it is recorded and is placed in the table of faults.

Operator command entries are available which will display all used and unused switch I/O ports on the CRT, or will cause the list to be printed on the printer. The PCC will refuse to set a path if the I/O ports on the switch matrix are already in use, and will generate a display to that effect.

(4) Testing of Switch Paths. Operation commands are available for maintenance testing of switch paths. These commands permit the connection of any input to any output via any mid-stage (stage 1) module if the required modules are not already in use. Use of the maintenance commands are described in chapter 6. All maintenance commands can be used during normal operating hours except the TEST SWITCH subcommand in the MAINTENANCE mode. This subcommand injects a test signal into switch paths.

b. Local Control. If the primary mode of operation should fail, it is anticipated that the HSDS system will be controllable by a local control computer (LCC) installed in the switch/patch panel. Commands to set a switch path will be entered via front panel push-buttons. The setting, verification, and recording of a switch path will be accomplished in the same manner as described in the previous paragraphs for PCC control. The LCC should also be valuable in troubleshooting switch control problems. (It should be noted that this local control capability does not yet exist.)

c. Manual Patching. An I/O path can be established manually by use of coaxial patch cables which connect a port on the input connector panel to a repeater/distributor amplifier on the synchronizer assembly. Identification of I/O channels, and procedures

to manually connect them, are provided in the Operation and Maintenance Manual for Electrical Equipment Cabinet CY-7559(XG-2)/USQ-62(V).

5-5. FUNCTION DIRECTORY. The function directory, table 5-3, lists and describes the various control and data signals used to set a switch path in the HSDS system, and also those used to establish a communication channel between NTDS devices. This table is a summary of the information given in tables 5-1 and 5-2, and contains some additional functions discussed in detail in the Operation and Maintenance manual for the Electrical Equipment Cabinet CY-7559(XG-2)/USQ-62(V).

5-6. DETAILED DESCRIPTION, SIMULATION FUNCTION. Communications between NTDS computers on peripheral-designated channels requires a special interface. The simulator may be used as that interface. Figure 5-6 is a simplified block diagram of the simulation function showing normal data flow.

a. Simulation, System Computer Interface. The system computer interface section of the simulator converts the control word received from one computer (called the system computer) to one which another computer (called the simulation computer) interprets as originating from a peripheral. In this manner communications between computers can be accomplished on channels normally used as peripheral channels. The top portion of figure 5-6 illustrates the conversion of control bits as they enter and leave the simulator when data flow is from the system computer to the simulation computer. Although figure 5-6 illustrates several I/O control bits, it should be remembered that only a single serial line for input, and one for output, (full duplex)

Table 5-3. System Function Directory

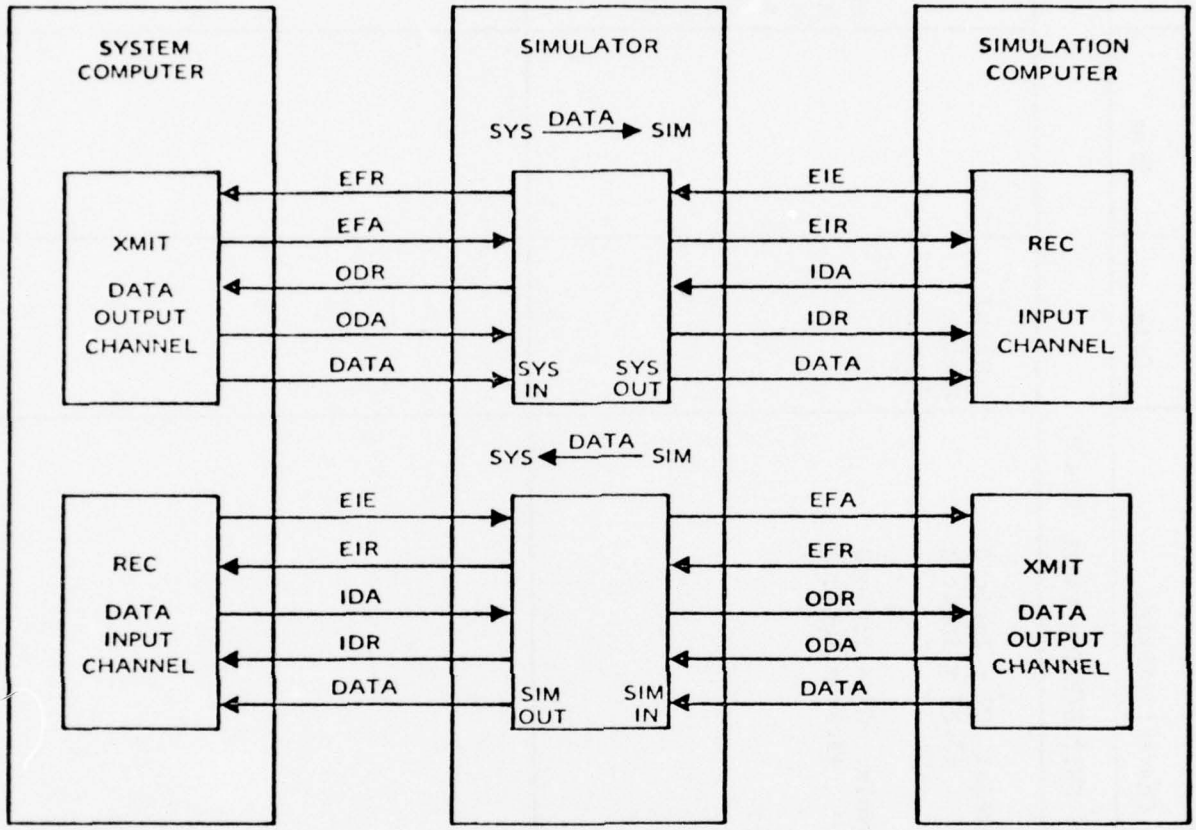
Name	Description	Type	Characteristics	Orig	Term	Reference
NTDS I/O CHANNEL COMMUNICATION						
ODA EFA IDA EIA	Output Data Acknowledge External Function Acknowledge Input Data Acknowledge External Interrupt Enable	Control	NTDS Fast: 0V = logic 1 -3V = logic 0 NTDS Slow: 0V = logic 1 -15V = logic 0 or ANEW: 0V = logic 1 +3.5V = logic 0	NTDS Computer	NTDS Peripheral	Tables 5-1 and 5-2 Figures 5-4 and FO-1
IDR ODR EFR EIE	Input Data Request Output Data Request External Function Request External Interrupt Enable	Control	NTDS Fast, NTDS Slow, or ANEW	NTDS Peripheral	NTDS Computer	Tables 5-1 and 5-2 Figures 5-4 and FO-1
DATA (32 bits)	Data	Data	NTDS Fast, NTDS Slow, or ANEW	Computer/ Peripheral	Peripheral/ Computer	Tables 5-1 and 5-2 Figure 5-4.

Table 5-3. System Function Directory (Contd)

Name	Description	Type	Characteristics	Orig	Term	Reference
			HSDS SWITCH/PATCH PANEL			
$\overline{DS0}$ through $\overline{DS5}$	Selects 1 of 4 switch/patch panels to execute I/O switch connection command	Control	TTL levels: 0V = logic 0 +3.5V = logic 1	PCC	Switch/ Patch Panel	Operation and Maintenance manual for Electrical Equipment Cabinet CY-7559 (XG-2)/USQ-62(V)
DOA	Control timing bit for DOA instruction word					
DOB	Control timing bit for DOB instruction word					
DOC	Control timing bit for DOC instruction word					
START	Timing to indicate control words have been set					
CLR	Used to enable test signal generator					
DATA (16 bits)	Instruction words (DOA, DOB and DOC)	Data	TTL levels: 0V = logic 0 +3.5V = logic 1	PCC	Switch/Patch Panel	

Table 5-3. System Function Directory (Contd)

Name	Description	Type	Characteristics	Orig	Term	Reference
HSDS SWITCH/PATCH PANEL (Contd)						
BUSY	Test Signal Generator Compare	Indicating	TTL levels: 0V = logic 0 +3.5V = logic 1	Switch/ Patch Panel	PCC	
DONE	Data Present	Indicating	TTL levels: 0V = logic 0 +3.5V = logic 1			Operation and Maintenance Manual for Electrical Equipment Cabinet CY-7559(XG-2)/ USQ-62(V)
CID (10 bits)	Channel Identification Bits	Indicating				



NOTE: THIS DIAGRAM SHOWS INDIVIDUAL LINES FOR CONTROL BITS AND DATA TO PORTRAY FUNCTIONAL FLOW. ACTUAL INTERCONNECTION BETWEEN THE SIMULATOR AND A COMPUTER IS VIA TWO SERIAL COAXIAL LINES; ONE FOR INPUT AND ONE FOR THE OUTPUT CHANNEL.

Figure 5-6. Simulation Block Diagram

are utilized. Therefore, the figure represents I/O control words which exist at different times when processing different data words. See tables 5-1 and 5-2 for correlation and meaning of data control bits. The bottom portion of figure 5-6 illustrates data flow from the simulation computer to the system computer. Observe that the control bits between the top and bottom portions of figure 5-6 are interchanged. When transferring data between computers on peripheral channels, it is possible to transfer data when the receiving computer is not ready to receive the data. To prevent loss of data, the simulator stores data until the receiving computer acknowledges that it has received the data. Details on how the simulator performs the conversion and storage functions, including data transfers, are described in the Operation and Maintenance Manual for the Electronic Equipment Simulator SM730(XG-1)USQ-62(V).

b. Simulation, Simulator Computer Interface. The simulator computer interface section of the simulator functions in the same manner as the system computer interface previously described, when control data bits are interchanged and data flows from the simulation computer to the system computer.

APPENDIX B: A FUNCTIONAL DESCRIPTION OF THE AN/USQ-67 CENTRALLY CONTROLLED INTERCONNECTION SYSTEM (CCIS)

Appendix B is reprint of a document prepared for Naval Electronic Systems Engineering Center, Vallejo, CA titled "Technical Highlights of Centrally Controlled Interconnection System (CCIS)."

NAVAL ELECTRONIC SYSTEMS
ENGINEERING CENTER, VALLEJO
VALLEJO, CALIFORNIA 94592

TECHNICAL HIGHLIGHTS OF CENTRALLY CONTROLLED INTERCONNECTION SYSTEM (CCIS)

Contract No. N66314-74-C-7195
October 1974

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TABLE OF CONTENTS

INTRODUCTION

The purpose of this paper is to describe the principles of design and development of the CSMTF Centrally Controlled Interconnection System (CCIS). The CCIS is the backbone of the CSMTF and performs the major portion of training schedule rearrangement functions.

This Engineering Report provides a general description of the Centrally Controlled Interconnection System (CCIS) and its design criteria. The interconnection system to be employed will satisfy only the digital data network of the CSMTF program. Since many of the digital data equipments (e.g., central processors and peripheral equipment) have application in several training systems, the ability to interconnect them into the various systems increases equipment utilization, and reduces equipment quantities and, consequently, cost.

The interconnection method selected for CSMTF use is a serial data transmission 3-stage (A,B,C) array. (See Fig. 1). This method allows a total access system (i.e., any input to this system may be connected to any output) while significantly reducing its size and cost over conventional single stage arrays. This system will be controlled from a central control station located in the same room with it.

The CCIS will initially interconnect the digital data channels of 23 digital computers and 240 peripheral equipments (which equates to an array having 594 digital input cables and 586 digital output cables) with the capability of being expanded to 640 x 640 array. The CCIS is non-blocking (in the wide sense), meaning any one of the 594 inputs may connect to any one of the 586 outputs not already assigned. However, care must be exercised in loading the array so as to prevent blocking before total access (i.e., 594 x 586) is achieved. The same statement holds true when the CCIS increases to a 640 x 640 array.

In order to provide computer-to-computer (inter-computer) interconnection in the same manner as computer-to-peripheral, the scheme for connecting digital data channels to the switching matrix is different than that of usual conventions. In the CCIS, all data input cables will be connected to the A-stages and all data output cables will be connected to the C-stages. Then, since the CCIS will interconnect any A-stage input to any C-stage output, computer-to-computer and computer-to-peripheral are handled in an identical manner.

Also considered part of the CCIS are a series of Underdeck Interconnect Panels. These panels are to be located on each of the four decks under the raised floor. They will be plugged and jacked for coaxial digital data cables. These devices will be permanently mounted to the deck and will provide a junction point for the digital data cables of each peripheral or computer requiring connection to the CCIS switching matrix. Provision for approximately 120 peripheral data cables per deck will be provided.

BACKGROUND

The Combat Systems Maintenance Training Facility (CSMTF) will consist of multiple general-purpose digital computers of several types and over 200 pieces of supporting peripheral equipment. To effect the most efficient and economical use of all this equipment, the various pieces of hardware will be electrically reconfigured at appropriate times to provide operational systems configurations corresponding to the maintenance training courses being taught. This equipment sharing concept, which has already been employed at other Naval training facilities, will result in decreased initial capitalization costs and more efficient utilization of the various types of equipment.

Therefore, it is imperative that the CSMTF switching system incorporate automatic or semi-automatic techniques to the extent that these methods fall within the programmed funding limits.

The overall CSMTF system switching complex must be capable of configuring the various equipments into predetermined training course configurations which will allow simultaneous independent training, when required, on different functional systems. The digital data switching complex will configure the equipment into system segments where each system segment is specifically related to one or more training courses. The design of such a switching complex, is specified in the performance, design, test, qualification requirements, installation and checkout for the "CENTRALLY CONTROLLED INTERCONNECTION SYSTEM (CCIS)" procurement package contract N66314-74-C-7195 with Univac.

The following criteria have been specified:

a. The designed complex must be modular in nature in order to accommodate either small or large incremental increases in quantities of equipment.

b. The complex is basically a support system and, as such, must have appropriate reliability, safety and convenience to enhance usage of the training course hardware.

c. The complex must provide rapid, convenient and compatible equipment reconfiguration at a frequency commensurate with course support requirements.

The development and design of the final switching scheme utilized by the CCIS must be guided by high performance in the form of minimal degradation of all defined signals, easy control and maintainability (high MTFB, low MTTR).

The large size and expandability requirements impose strict modular considerations or the equivalent, a means by which the monumental number of switchpoints is reduced. In addition, it is desirable to implement a system such that documentation is minimal, and downtime is obviated during

system expansion. Therefore, a graphic clarification of tradeoff constraints (viz., the weighting of cost, size, MTTR, MTBF, reliability, expandability, installation ease, etc.) was necessary so that the switching technique would be optimum for the CSMTF requirements.

TABLE 1

Req'd. Amount	Devices	Digital Data Channels Input	Output
3	CP-642A computers each with 14 I/O channels	42	42
2	CP-642B computers each with 16 I/O channels	32	32
4	CP-789 computers each with 8 I/O channels	32	32
3	U-1616 computers each with 16 I/O channels	48	48
11	AN/UYK-7 computers ea. with 16 I/O channels	176	176
* 2	SMP control cables @ 3 channels each	6	-
* 1	SMP control cables @ 2 channels each	2	-
4	KCMX @ 4 channels each	16	16
240	Peripheral I/O channel requirements	240	240
	TOTALS	594	586

* Direct computer interface in parallel transmission

PARALLEL DATA RATES

The parallel data rates and corresponding pulse (bit) transition times were considered in determining transmission-line requirements for computer I/O distribution. The transmission-line band width is governed by pulse transition time (rise/fall time) rather than data rate. Table 2 summarizes the aforementioned characteristics.

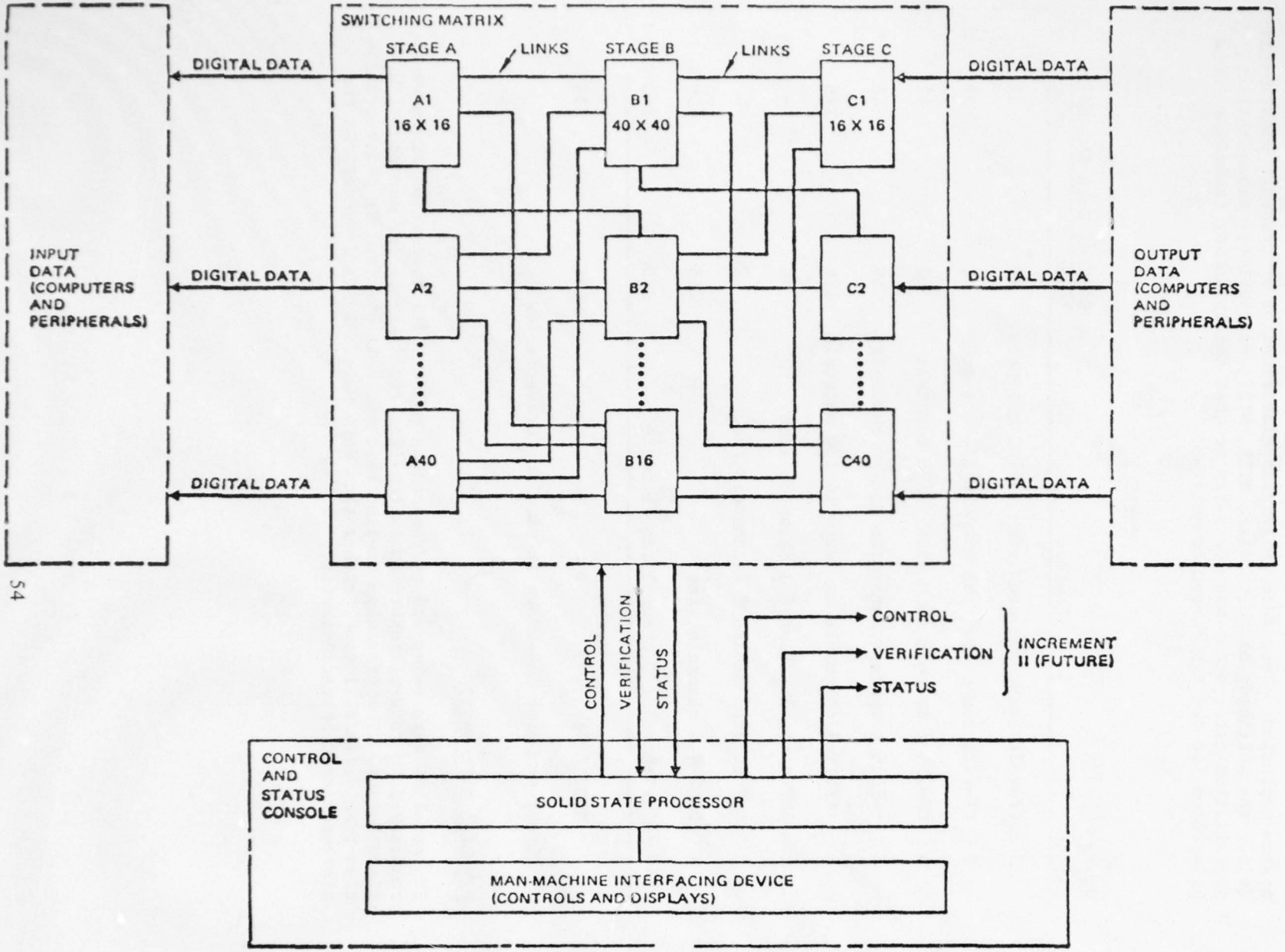


FIGURE 1. CCIS FUNCTIONAL FLOW DIAGRAM

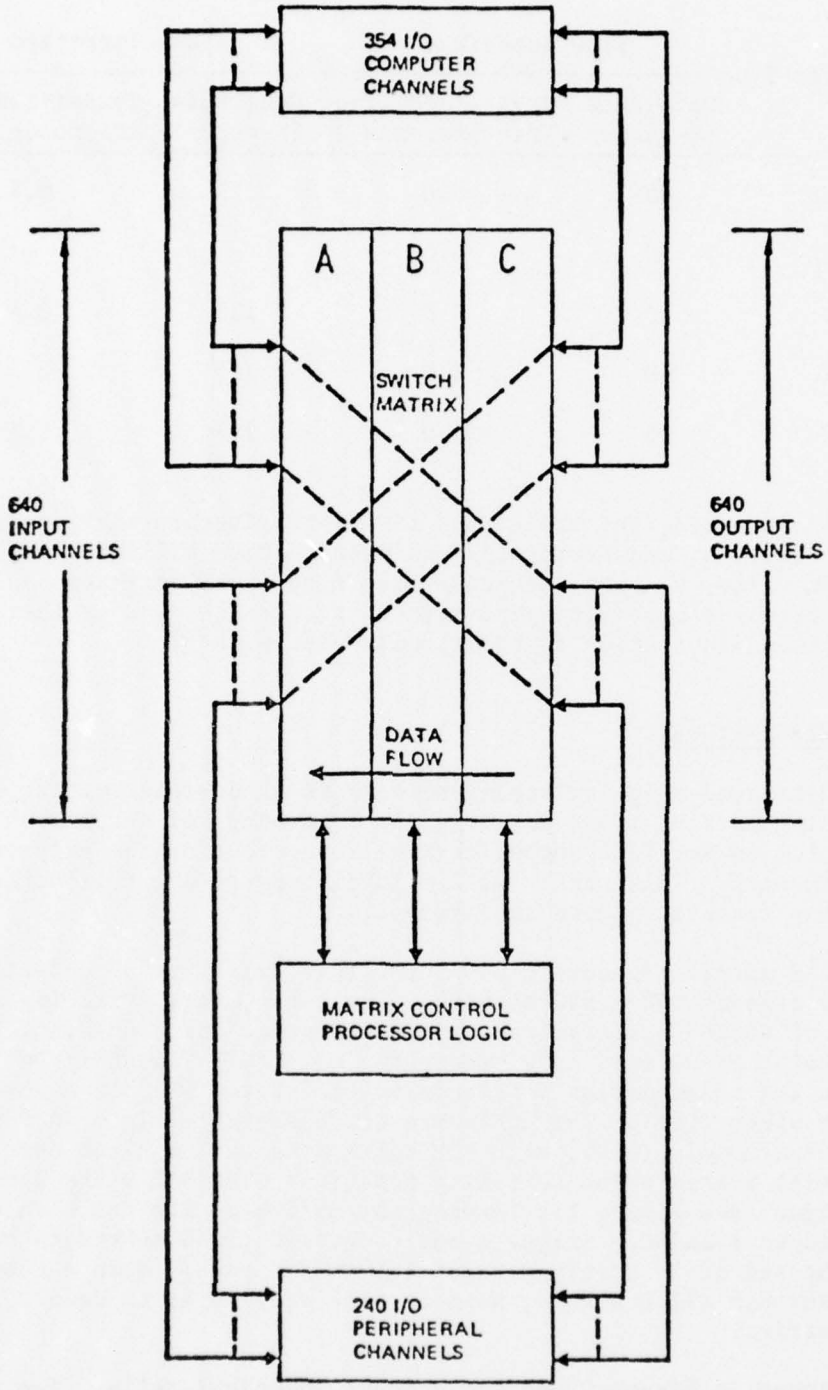


FIGURE 2. CCIS 604 X 640 I/O CHANNEL INTERFACE NETWORK

TABLE 2 PARALLEL DATA RATES

Computer Type	Slow Interface		Fast Interface	
	Data Rate (K-words)	Transition Time (Microsec max.)	Data Rate (K-words)	Transition Time (Microsec max.)
CP-642B	40	6.0	125	0.4
CP-642A	30	6.0	-	-
CP-789	40	6.0	125	0.4
CP-967	40	6.0	125	0.4
AN/UYK-7	33	6.0	167	0.4

As will be noted, the transition times are given at their maximum time. It is felt that manufacturer's equipment design will be close to this maximum value, since to decrease rise time is to increase bandwidth, which requires more stringent circuit tolerances, and an increased bandwidth is an invitation to additional noise pickup.

SWITCHING NETWORK

The CCIS three-stage switching network is a non-interrupting, re-arrangeable switching matrix; i.e., any idle input terminal of matrix can always be connected to any idle output terminal by rerouting the existing connections, if necessary. This matrix will maintain one-to-one full access with non-blocking features, shown in Figure 1.

The CCIS matrix connecting 640 input terminals and 640 output terminals abbreviates as 640 x 640 network. The three-stage switching matrix consists of 46,080 basic switching cable crosspoints elements (CCE's). The crosspoint is defined as a two-state (ON or OFF) switching device possessing a low transmission impedance in one state (ON) and a very high impedance in the other (OFF). The CCE's are to be assembled into an 8 x 8 basic switching module (BSM), each BSM containing 64 CCE's and each CCE capable of serial transmission switching function. The BSM's are assembled into substages (see Figure 1), forming assemblies of 256 CCE's on each substage for stages A and C. Stages A and C consist of 40 substages each. Stage B is composed of 16 substages with 1600 CCE's each. Each A substage shall have through all B stages, sixteen (16) data paths to each C substage of the matrix.

The stages in Figure 2 are composed of identical CCE's. Two adjacent stages are connected by a pattern of links. Along with the CCE's, the

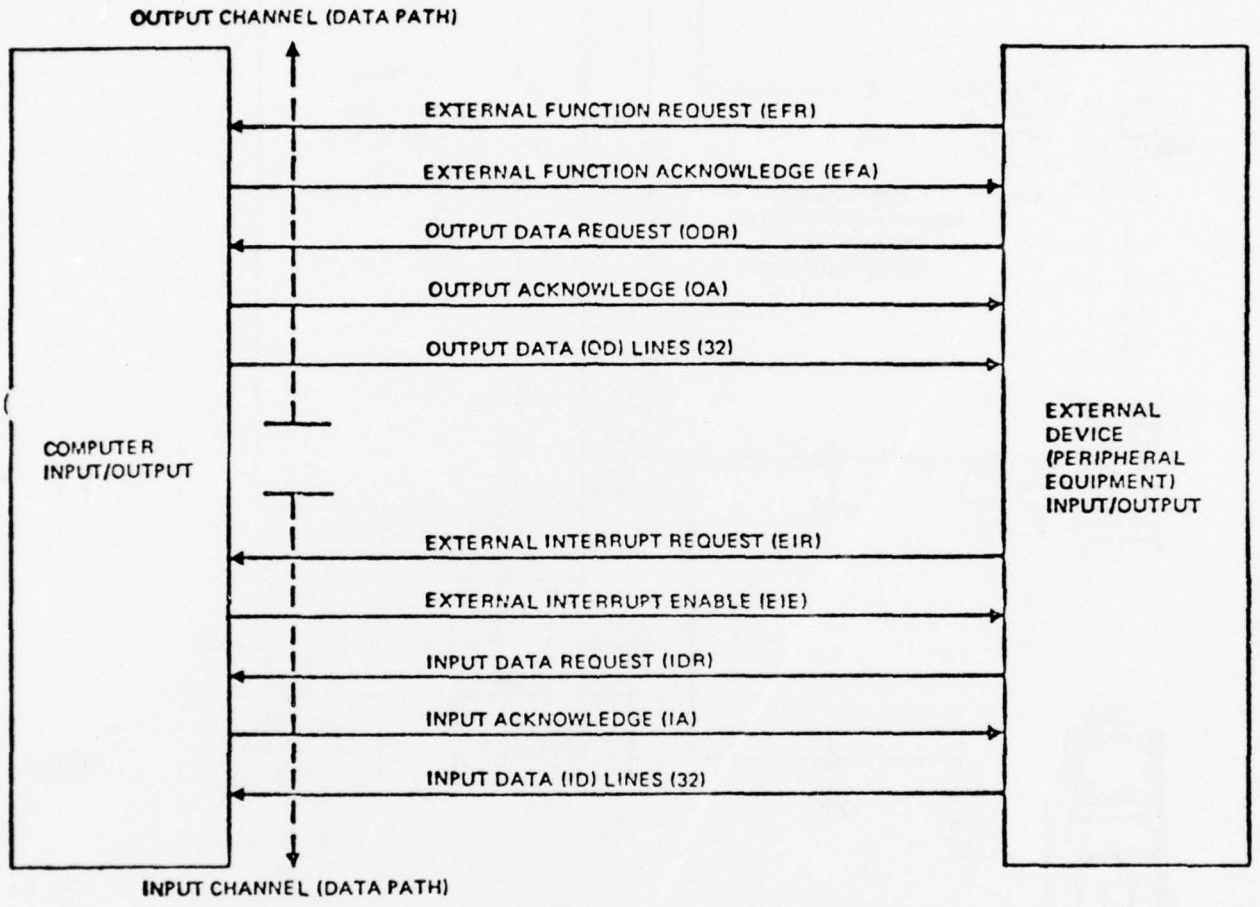


FIGURE 3. COMPUTER-PERIPHERAL INPUT/OUTPUT COMMUNICATION

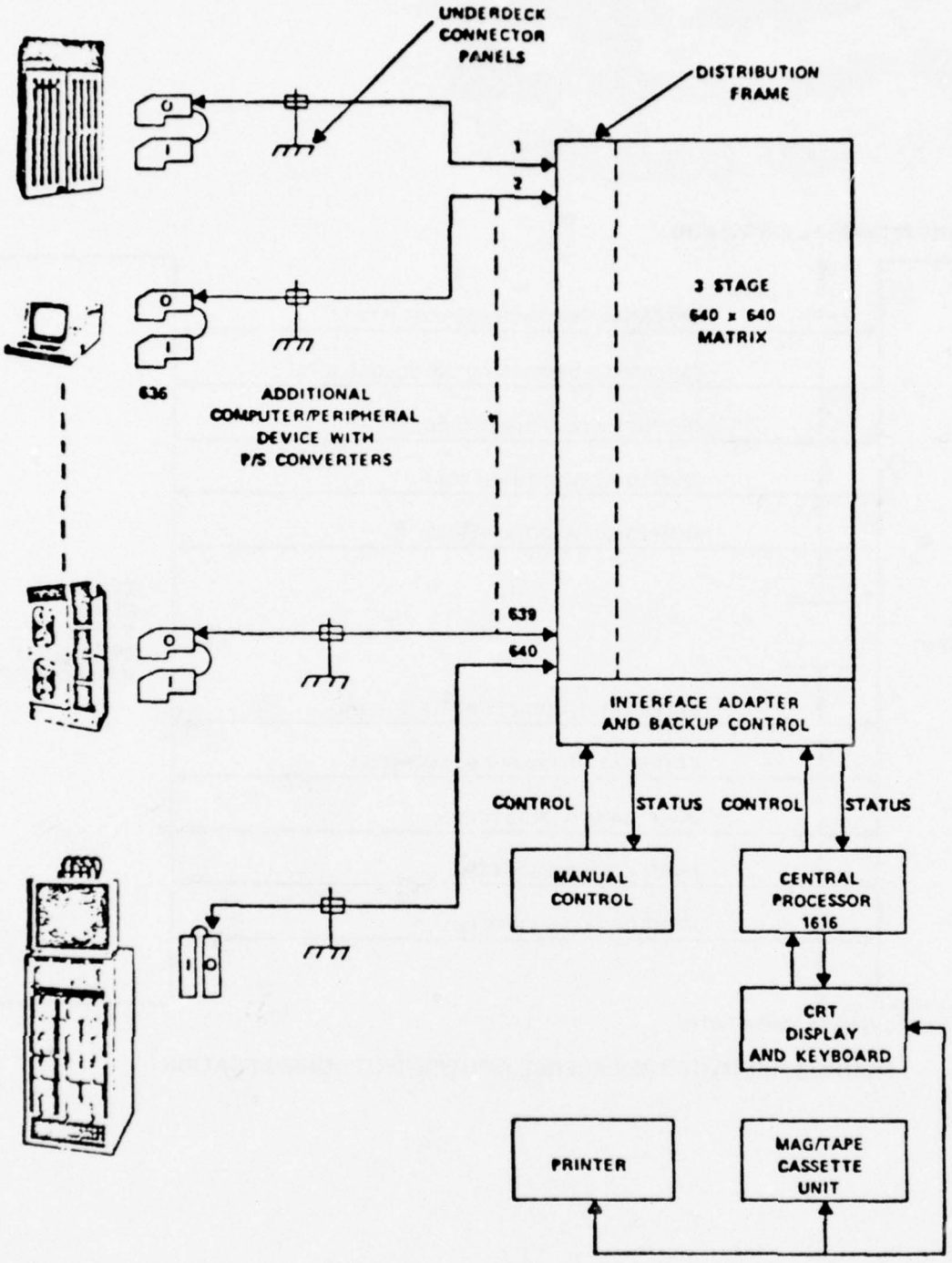


Figure 4 CCIS Switch and Control

link patterns are responsible for the distributive characteristics of the CCIS network. They afford an inlet (data input) ways of reaching many outlets (data outputs) (Figure 3). Obviously, each output on the CCE in a given stage is some input of the next stage for the chosen path. The switch matrix input 640 ports on the stage A are numbered in a sequential order, and that the 640 output ports on the stage C are also numbered in a sequential order (i.e., from 1 through 640). This makes it clear that each link pattern, and each permitted way of closing the largest possible number of crosspoints in a stage are interrelated signal paths throughout the matrix. Henceforth, 640 port arrangement of A and C stages can be viewed abstractly as a permutation on (1, ..., 640). The network in Figure 1 has the property that all maximal stages have the same number of 640 data paths in progress, and any such maximal state (i.e., states in which no additional data paths can be transmitted) realizes a permutation which is a product of certain of the permutations represented by the link patterns and the stages A, B and C. A matrix of this structure can always achieve any arbitrary permutation controlled by algorithm that consist of decomposing a given permutation into 16 (where 16 x 16 is the base of the network) permutation for the 16 (40 x 40) subnetworks, thus determining the connections for the 40 (16 x 16) networks in the input and output stages.

PARALLEL/SERIAL AND SERIAL/PARALLEL CONVERSION

Figure 4 illustrates the CCIS serial transmission configuration. Each I/O channel has Parallel/Serial (P/S) conversion logic at the channel source. Communication with the switch matrix is via bidirectional coaxial cable. The matrix is not sensitive to the data patterns or data rates of the serialized data transmission flow, therefore, an instantaneous passage of fast and slow rated data in a simultaneous mode will be operated without interference (see Figure (5).

All P/S converters are designed to operate with data words up to 36 bits or less. When a converter is operating with a data word less than 36 bits, the remaining bits are disregarded. Each data word is synchronized by appearance on the channel of a transition which has been preceded by a minimum 832 nanoseconds of no transition (quiet period). This "quiet period" signifies an end of data word. The first transition after the 832 nanoseconds period, starts the 36-bit (or less) data word in which the four control bits are interleaved (see Figure 3). Control line status is transmitted more frequently than the data bits to preserve the "handshaking" requirements described in Specification DS-4772.

One data bit is transmitted during each 104 nanoseconds clock period. During this time frame, one or two transitions take place. The first transition always occurs and is called a CLOCK transition. The second one is conditional and indicates the data bit. The clock transition for the data bit occurs 104 nanoseconds after the last clock transition, therefore, the stream of "1" and "0" bits is generated within the 104

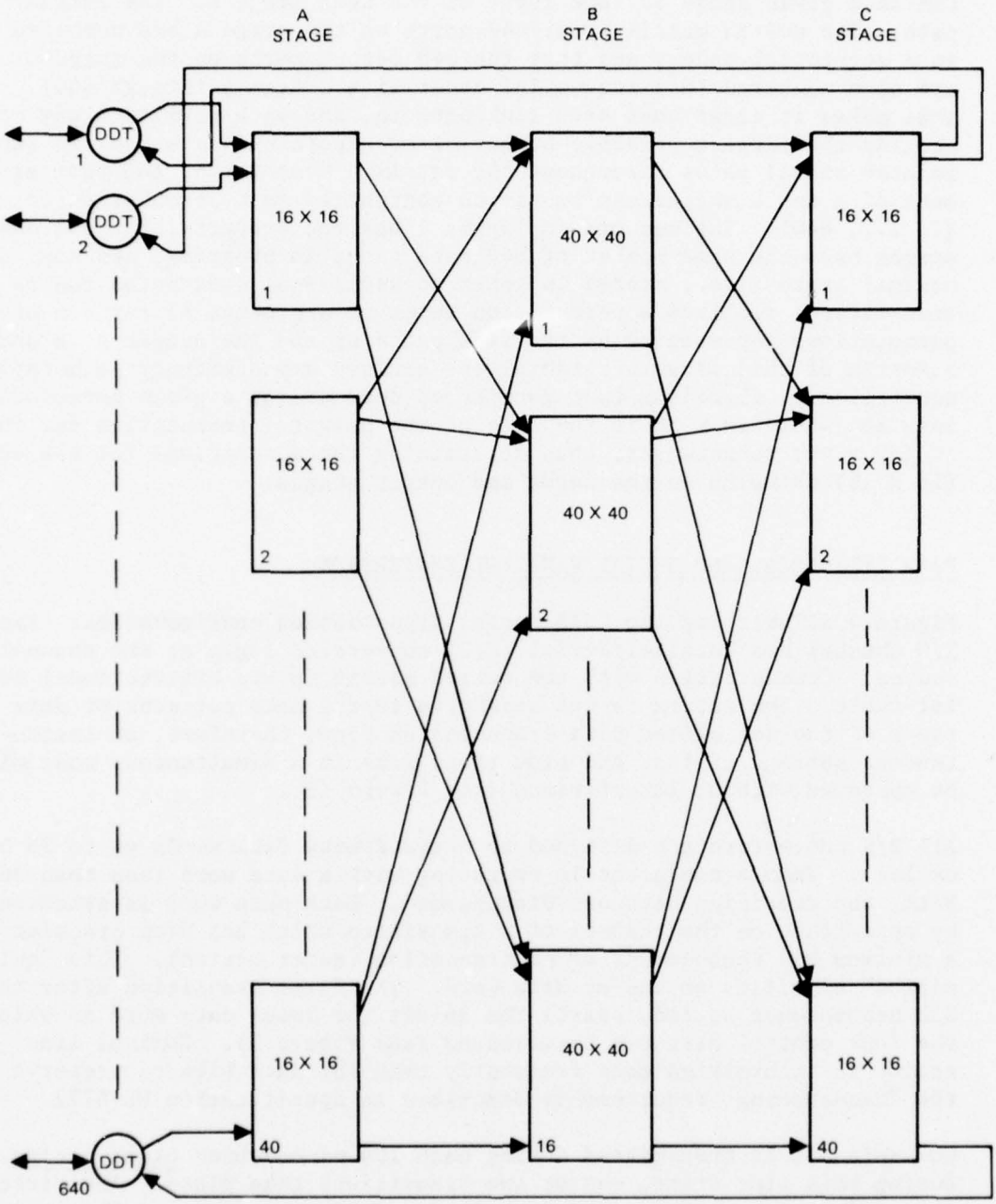


Figure 5. SWITCHING MATRIX BLOCK DIAGRAM

DUPLEX DIGITAL TRANSCEIVER

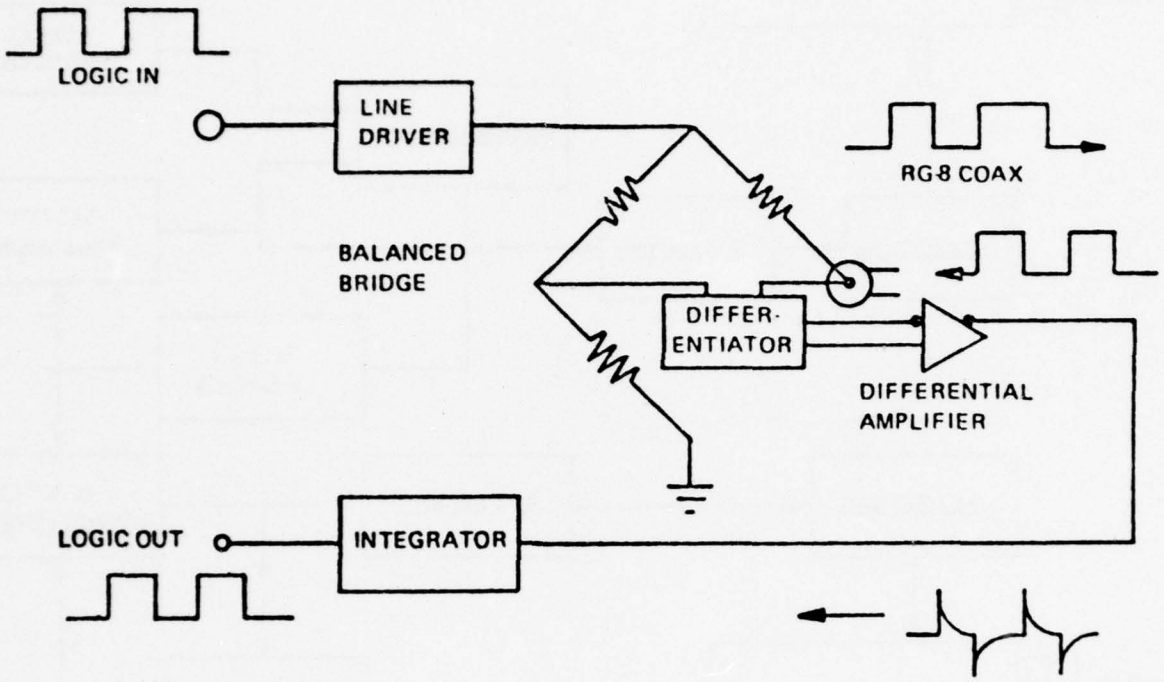
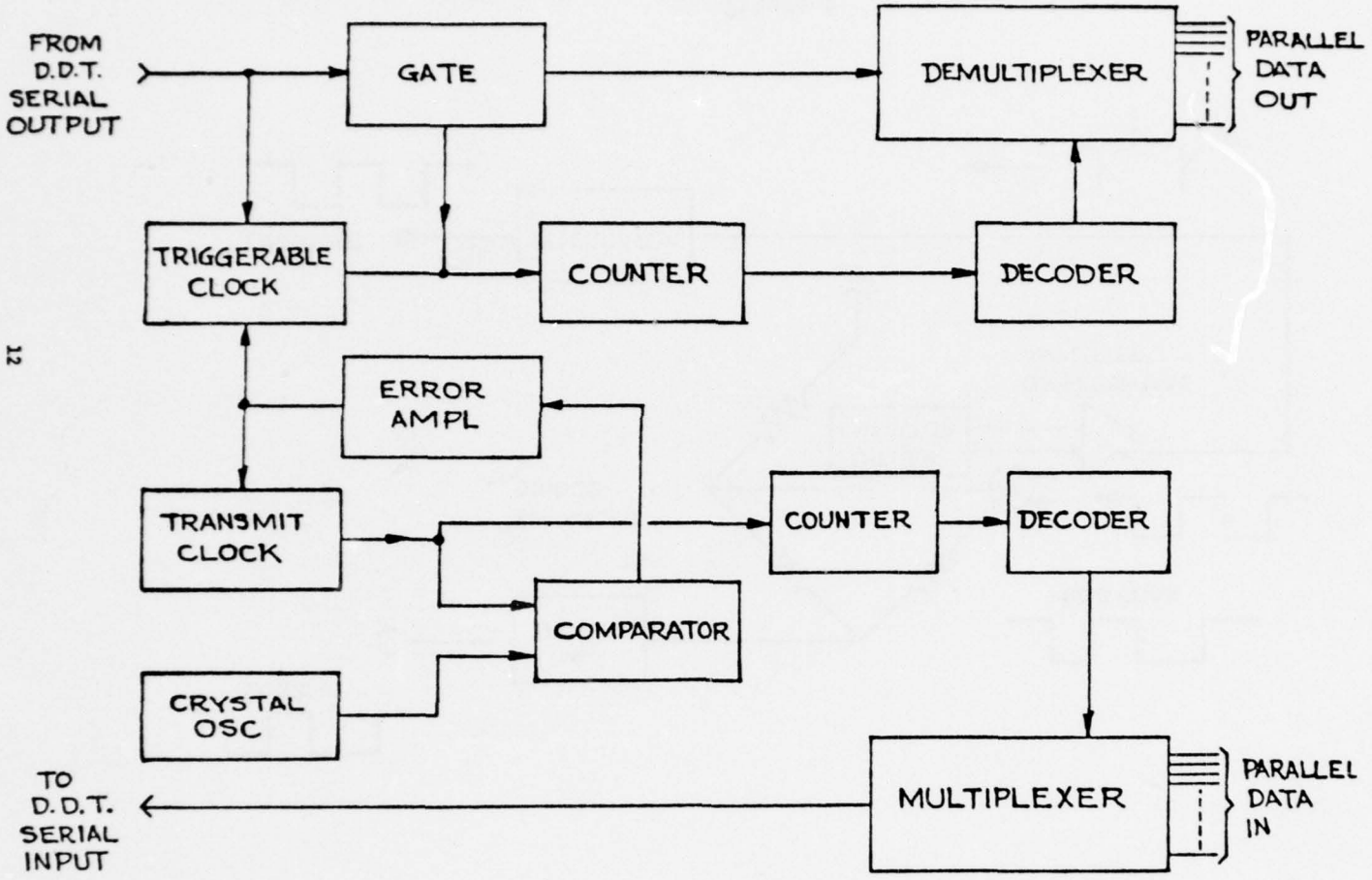


Figure 6

I/O CONVERTER BLOCK DIAGRAM



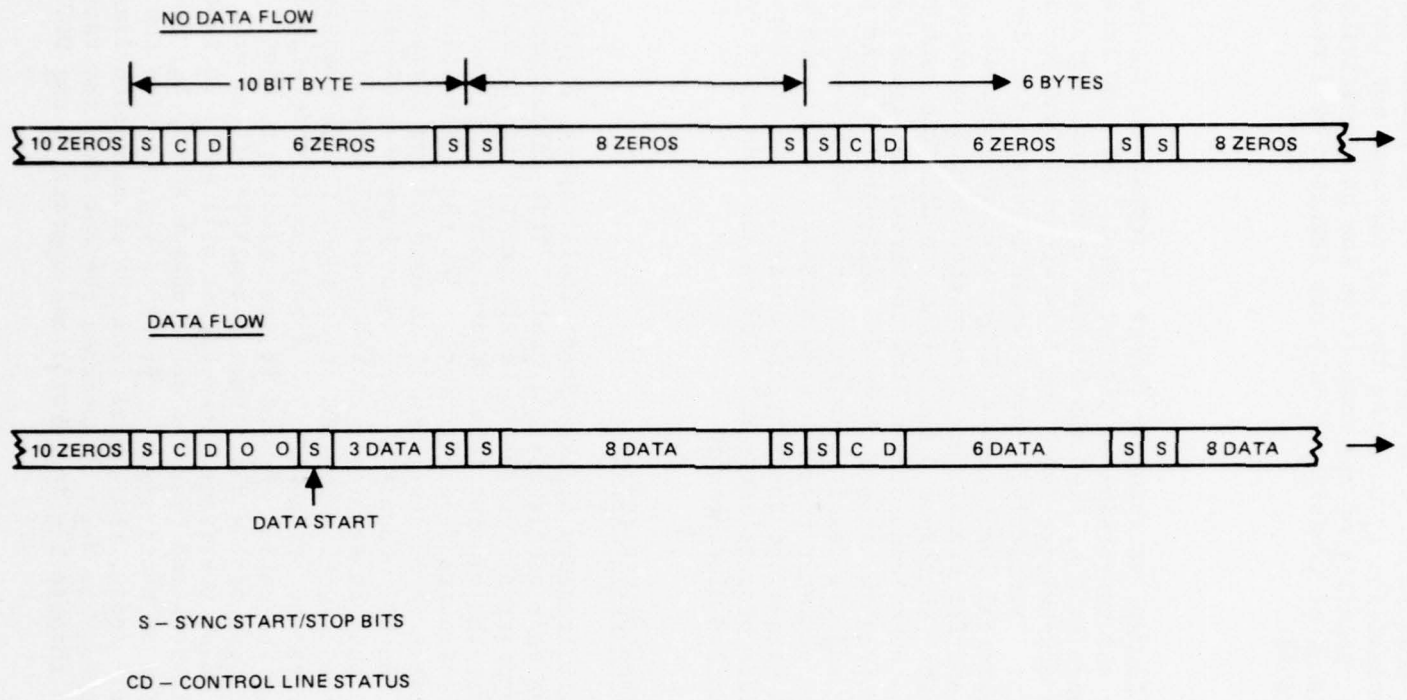


Figure 8. SERIAL INTERFACE FRAME

nanoseconds time span by the occurrence or absence of 42 nanoseconds transition. The serial data stream is then routed to the duplex digital transceiver (DDT) as shown in Figure 6, where it is differentiated for transmission via coaxial cable to another DDT at the matrix interface. The process of transition is carrying the information, not the logic level; therefore, polarity of the transition has no significance whatever. Thus, the occurrence of transitions only are detected at a receiving converter (Figure 7).

DATA WORD FORMAT

The serial word format, as shown in Figure 8, represents the basic art of serialization and conversion of digital data. The slow interface -- serialization where bits A, B, C and D refer to control signals; i.e., A is output data acknowledge (ODA) and B is external function acknowledge (EFA) control bits. Similarly, C and D would correspond to input acknowledge (IA) and external input enable (EIE) bits, respectively, from the peripheral. IA and EIE signals are transmitted in the opposite direction from all other bits, therefore C and D lines to and from each connector are routed to the other connector of the converter set (pair) as shown in Figure 7. Operationally, this enables all multiplexing to be performed in one connector and all demultiplexing in the other connector. The fast interface differs somewhat from the slow interface, where the word transfer rate is much higher and the sampling delay is much shorter. To transmit three data bits it takes only 168 nanoseconds and total 36 bits is transferred in 2.8 microseconds.

DUPLEX DIGITAL TRANSCEIVER (DDT)

The DDT allows simultaneous bidirectional (full duplex) digital serial mode transmission on a single coaxial cable. This allows two-bit streams travelling in opposite directions to be transmitted on the same cable. The DDT interfaces the bidirectional transmission cable with unidirectional TTL logic circuits (see Figure 6). The characteristic impedance of the coaxial cable is 50 ohms, and it is used as one element of a Wheatstone bridge of the DDT schematic. The input impedance of each bridge is also 50 ohms, thus it ensures that the cable is properly terminated on each end of the network. The DDT logic input is differentiated and then appears across the bridge (V_{AB}). A portion of that signal appears as V_{CB} and drives the cable. R_6 and R_7 are selected so that $V_{CB}=V_{DB}$, therefore, the output of the differential amplifier (V_{EB}) will always equal to zero. Thus, the transmitted signal will never be received locally. Signals received from the cable appear across R_5, R_6, and R_7 as V_{CB}. A portion of these signals appear as V_{CD}, driving the differential amplifier. Again, the signal from the transmission line is amplified and appears as V_{EB}. It becomes obvious that the received signal is routed through the integrator and appears as the DDT logic

CCIS SLOW INTERFACE DATA RATE COMPARISION

$$\text{DATA RATE} = \frac{1}{C_D + P_D + TD_1 + TD_2}$$

ASSUME C_D = 25 uSEC (i.e. DATA RATE = 40 KW/S

P_D = 0 uSEC

$$\text{CONVERTERS} = \frac{1}{25 + 12.06/14.26} = 27/25.4 \text{ KW/S}$$

$$\text{R/A} = \frac{1}{25 + 17.86/20.06} = 23.4/22.4 \text{ KW/S}$$

$$\text{*PARALLEL} = \frac{1}{25 + 9.780} = 28.8 \text{ KW/S}$$

includes DVRS/RCVRS at Matrix

CCIS FAST INTERFACE DATA RATE COMPARISION

$$\text{DATA RATE} = \frac{1}{C_D + P_D + TD_1 + TD_2}$$

ASSUME $C_D = 6$ uSEC (i.e. DATA RATE = 167 KW/S)

$P_D = 0$ uSEC

$$\text{CONVERTERS} = \frac{1}{6 + 4.1/5.5} = 99/87 \text{ KW/S}$$

$$\text{R/A} = \frac{1}{6 + 4.76/6.160} = 93/82.4 \text{ KW/S}$$

$$\text{PARALLEL} = \frac{1}{6 + 2.280} = 121 \text{ KW/S}$$

CCIS FORCED MODE
DATA RATE COMPARISION

CCIS SYSTEM IS CAPABLE OF TRANSFERRING

DATA AT COMPUTER RATE UP TO 310 KW/S

output. Because the bridge is a linear element of the DDT network, the incoming and outgoing signals cause no interference between same, nor do they tend to cancel each other out. Even though a positive input pulse and a negative output pulse may produce a net zero voltage at the cable interface, the superposition of both signals at the amplifier input still produce a net differential voltage. In the event of balancing the bridge for dc, the baseband signals are always differentiated for transmission. There are four DDT's for each full duplex I/O passage in the CCIS network; i.e., 320 x 4 = 1280 DDT's.

SERIALIZED DATA TRANSMISSION RATES

By definition, the data transfers are measured by pulse time limits of the highest frequency component of the response which the digital computer program can faithfully reproduce. Reaction time (delay) represents a transfer lag in the signal loop through the digital computer. Both the pulse time and the delay time are determined by the execution time of the digital computer program. In the CCIS full duplex I/O transmission link, the following delays are involved.

a. Transmission delays (in microseconds typ.)

b. Cable delays

c. Matrix delays

d. Serialization delays

e. Driver-Receiver delays (All these delays contributing impedance to the systems data words transmission rates. There are two modes of data transmission involved in the NTDS use:

1. Handshaking mode with elements of computer reaction time (C_R), peripheral reaction time (P_R) and transmission delay (TD).

2. Forced mode with elements of computer reaction time (C_R) only; i.e., in this mode data words are transmitted at computer I/O transmission rate.

Therefore, one should derive "Transmission Rate Equations" as follows:

a. Handshaking work rate = $\dfrac{1}{C_R + P_R + TD_1 + TD_2}$

Where:

C_R - Computer Reaction Time

P_R - Peripheral Reaction Time

TD_1 - Transmission Delay between computer and peripheral

TD_2 - Transmission Delay between peripheral and computer

b. Forced Mode = $\frac{1}{C_R}$

SYSTEM DELAY CALCULATIONS

a. CABLE DELAY (CD)

Assuming distance 200 feet from computer to matrix and 200 feet from matrix to peripheral. Therefore, 400' x 1.5NS/FT = 600 nsec. and 600 x 2 = 1200 nsec. delay.

b. MATRIX DELAY (See Figure)

Wire + 2 DDT's + 3 stages = 90 nsec. and 90 x 2 = 180 nsec. delay.

c. SERIALIZATION DELAY

Where serialization = 2.48 + 0/2.48 + 1.40 = 2.48/3.88 microseconds delay.

d. DRIVER-RECEIVER DELAYS (in microseconds)

	SLOW		FAST	
	CONV.	R/A	CONV.	R/A
Driver/Receiver	4.6	8.4	0.24	0.90
Reset/Misc.	3.6/4.4	5.6/6.4	0.20	0.20

CONCLUSION

The decision to acquire CCIS and associated maintenance support equipment primarily based very largely on a dollar and cents matter. Both reduction of large operational and maintenance personnel costs in the switching network, and the value of better state-of-the-art technology evolvement were used to estimate the net dollar effect of CCIS network utilization in CSMTF complex.

CCIS and allied equipments represent just one area in which NTDS management may have opportunity in receiving technological assurance for investment. While switching networks may undergo substantial revision after operational experience is gained with the CCIS network, the CCIS itself will have relatively long operational life. It would not matter if less expensive, more powerful, or otherwise more enticing switchers are developed, the CCIS will provide productive service over an extended period (projected 25 years).

APPENDIX C: A FUNCTIONAL DESCRIPTION OF THE AN/USQ-68 HIGH SPEED DIGITAL SWITCH (HSDS)

Appendix C is an excerpt, section 3, from the Technical Manual for the High Speed Digital Switch System prepared by Fleet Combat Direction Systems Support Activity, San Diego, CA.

SECTION 3

FUNCTIONAL DESCRIPTION

3-1. GENERAL.

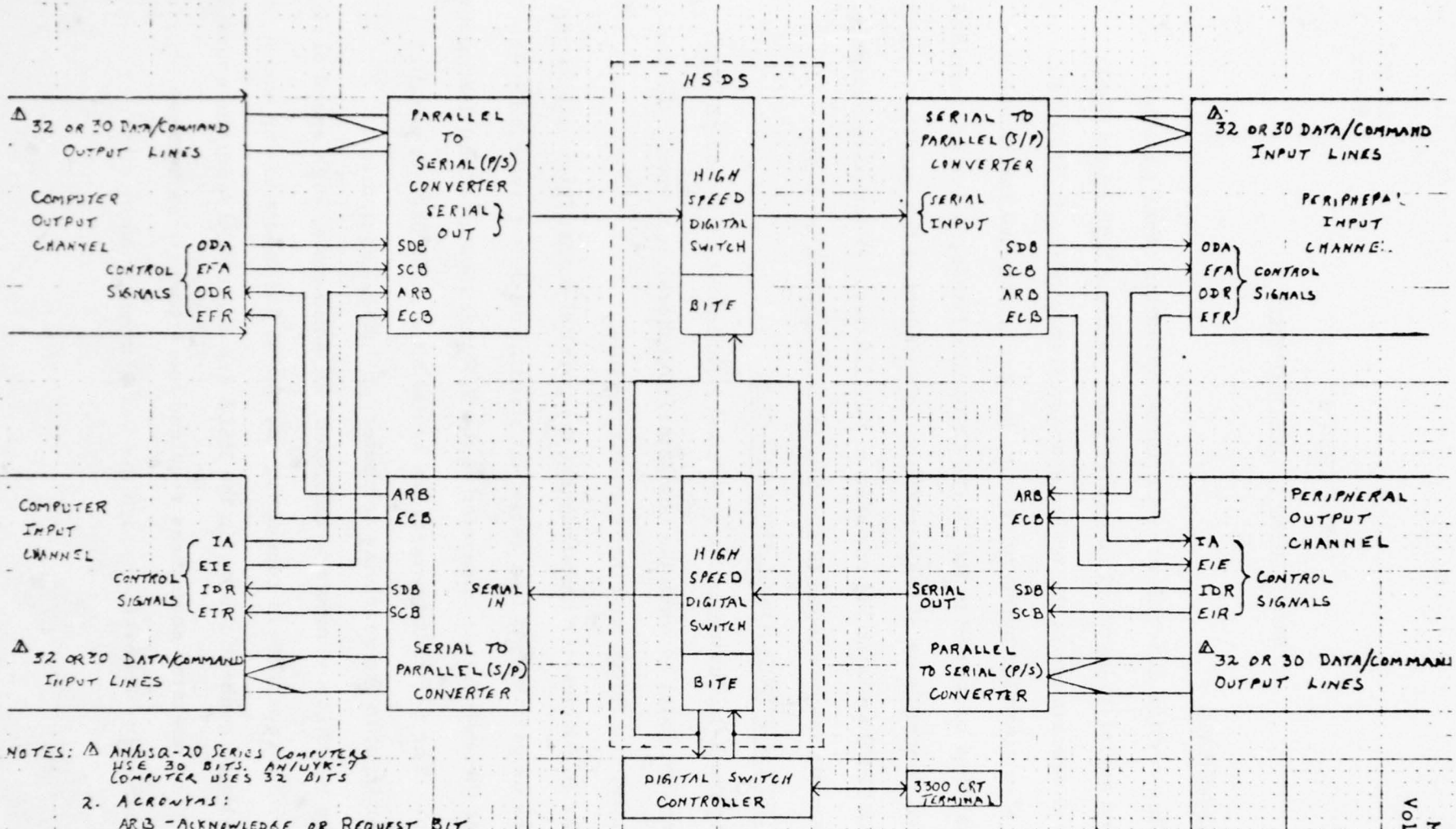
3-2. This section describes the functional operation of the parallel-to-serial and serial-to-parallel converter units, and the high speed digital switch. A description of the major characteristics of the D-116 minicomputer is also given for quick reference, however, detailed functional data and signal flow contained in the D-116 Computer Handbook are not included. Functional descriptions of the remaining components of the operator console and of the SPES are also not included in this section. Detailed information for these units may be found in existing manuals (see table 1-3).

3-3. SYSTEM FUNCTIONAL INTERFACES.

3-4. Figure 3-1 illustrates the functional interconnectivity and physical interfaces that exist between the computer/peripheral equipment, the converter units, the HSDS, and the operator console.

3-5. The P/S converter units convert the parallel output from originating computers or peripherals to a serial bit stream which is forwarded to the HSDS. At the switch it is connected to the S/P unit located at the destination equipment. The S/P unit converts the serial bit stream back to parallel format for input to the receiving computer/peripheral equipment.

3-6. The HSDS is a computer-controlled, all solid state, high speed serial switch, with a capability of connecting any one of 512 inputs to any one of 512 outputs. Patch connections within the HSDS are controlled from the operator's console. The operator configures required interconnections between terminated computers/peripherals through the D-116 minicomputer either by using



NOTES: 1. ANΔSQ-20 SERIES COMPUTERS USE 30 BITS. AN/UYK-7 COMPUTER USES 32 BITS

2. ACRONYMS:
   - ARB - ACKNOWLEDGE OR REQUEST BIT
   - ECB - ENABLE OR REQUEST COMMAND BIT
   - SCB - SEND COMMAND BIT
   - SDB - SEND DATA BIT
   - BITE - BUILT IN TEST EQUIPMENT
   - CRT - CATHODE RAY TUBE

FIGURE 3-1. TYPICAL COMPUTER, HSDS AND PERIPHERAL INTERFACE

stored configurations on tapes, or by using the Model 3300 CRT terminal to manually insert desired links. Each configuration selected is always available to the operator and he may determine from his remote position, on a channel-by-channel basis, the exact paths of data that have been interconnected. Individual paths can be added or broken without disturbing the remainder of the data interchange paths between computers/peripherals.

3-7. NTDS CHANNEL CONTROL COMMUNICATIONS.

3-8. The P/S and S/P converter units are designed to interface with equipment using standard NTDS input/output channels. The standard NTDS channel provides for parallel transfer of up to 32 data bits plus four control signals at data rates of up to a nominal 40K words per channel ("slow" interface), or at rates of up to 167K words per channel ("fast" interface). These maximum rates are reduced to some extent by the P/S and S/P converters and by the switching networks at the high speed digital switch (HSDS). The P/S and S/P converter PC boards are equipped to handle either interface by changing a reference voltage from -15 vdc (slow interface) to -5 vdc (fast interface).

3-9. NTDS Channel Control Signals. The NTDS channel uses a d-c level input/output system. The d-c level signals may change upon the interchange of control information and may exist for microseconds or for days, depending on the nature of the particular exchange involved. The control signals used for peripheral-to-computer input/output and their meaning are listed in table 3-1. Control signals used for intercomputer input/output are described below in paragraph 3-16. The control lines that carry the control signals are given the same names and are carried in the same cables as the data lines.

Table 3-1. CONTROL SIGNALS USED IN INPUT/OUTPUT - COMPUTER-TO-PERIPHERAL

	SIGNAL NAME	ORIGIN	MEANING
Input Channel	Interrupt Enable (EIE)	Computer	"I have enabled my input section to honor an interrupt on your channel."
	Input Data Request (IDR)	Peripheral Equipment	"I have a data word on my output lines ready for you to accept."
	Input Acknowledge (IA)	Computer	"I have sampled your data lines."
	External Interrupt (EIR)	Peripheral Equipment	"I have an interrupt code word on my output lines ready for you to accept."
Output Channel	Output Data Request (ODR)	Peripheral Equipment	"I am in a condition to accept a word of data from you."
	Output Acknowledge (ODA)	Computer	"I have put a data word for you on the data lines; sample them now."
	External Function Request (EFR)	Peripheral Equipment	"I am in a condition to accept an External Function message on my data lines."
	External Function (EFA)	Computer	"I have put an External Function message for you on the data lines; sample them now."

Note: In computer-peripheral communications, the control signals from the computer are always pulses, i.e., the computer control signal only has to be "set" for some minimum time, depending on the type of interface and equipment to which connected. The peripheral must be able to act on the computer control signal within this minimum time.

The control signals from the peripherals are levels, i.e., once the peripheral sets a control signal, that signal remains set until it is acknowledged by the computer.

3-10. At the S/P and P/S interfaces the NTDS control signals are assigned acronyms that are unique to the converters. These acronyms serve as integral references for converter unit logic and provide clarity and ease in following the detailed logic flow descriptions contained in Section 5. Figure 3-1 and the following table show the interrelationship between these acronyms and the NTDS control signals to which they equate.

P/S INPUT CONTROL SIGNALS			
P/S	COMPUTER	PERIPHERAL	INTER-COMPUTER
SDB	ODA	IDR	READY
SCB	EFA	EIR	EFA Line
ARB	IA	ODR	RESUME
ECB	EIE	EFR	EIE Line

3-11. Computer-Peripheral Input/Output. The sequence of events for each of the four cases of communication described in table 3-1 (i.e., data output, data input, external function commands and external interrupts) are detailed in the following paragraphs.

3-12. Data Output. A normal output sequence for data transfer from computer to peripheral is as follows (it is to be understood that the transfer for each sequence of events in this and the following descriptions is via the converter units and the HSDS):

a. The computer program control initiates the output buffer for the given channel.

b. Peripheral equipment sets its Output Data Request (ODR) line when it is in a condition to accept data.

c. The computer, at its convenience, detects the ODR and clears the information lines if any data exist.

d. The computer places data on the output information lines.

e. The computer sets the Output Data Acknowledge (ODA) line, indicating that data are ready for sampling.

f. Peripheral equipment detects the Output Acknowledge.

g. Peripheral equipment may drop the ODR any time after detecting the Output Acknowledge.

h. Peripheral equipment samples the data on the output lines.

i. Computer drops Output Acknowledge and the data lines.

Steps b through i of this sequence are repeated for every data word until the number of words specified in the output buffer have been transferred.

3-13. Data Input. A normal input sequence for data transfer to the computer from peripheral equipment is as follows:

a. The program control initiates input buffer for a given channel.

b. Peripheral equipment places data word on information lines.

c. Peripheral equipment sets the Input Data Request (IDR) line to indicate that it has data ready for transmission.

d. The computer detects the IDR at its convenience.

e. The computer samples the information lines.

f. The computer sets the Input Acknowledge (IA) line, indicating that it has sampled the data.

g. Peripheral equipment senses the Input Acknowledge line.

h. Peripheral equipment drops the IDR line.

Steps b through h of this sequence are repeated for every word until the

number of words specified in the input buffer have been transferred.

3-14. External Function Messages. The following sequence of events occurs when the computer is transmitting External Function messages to external equipment.

a. The computer initiates the External Function buffer for given channel.

b. Peripheral equipment sets the External Function Request (EFR) line indicating that it is in a condition to accept External Function messages.

c. The computer (at its convenience) detects the EFR and clears the data lines if any data exist.

d. The computer places the External Function message on the data lines.

e. The computer sets the External Function (EFA) line indicating that an External Function message is ready for sampling.

f. Peripheral equipment detects the External Function.

g. Peripheral equipment may drop the EFR at any time after detecting the External Function.

h. Peripheral equipment samples the External Function message on the data lines.

i. Computer drops the External Function line and the External Function code.

Steps b through i of this sequence are repeated for every External Function message until the number of words specified in the External Function buffer have been transferred.

3-15. External Interrupt. The sequence for transmitting an interrupt from peripheral equipment to the computer is as follows:

a. The computer sets the Interrupt Enable (EIE) line when it is ready to

accept an External Interrupt Request (EIR)[1].

b. Peripheral equipment detects the Interrupt Enable.

c. Peripheral equipment status requires the computer to be interrupted.

d. Peripheral equipment places the interrupt word on the data lines.

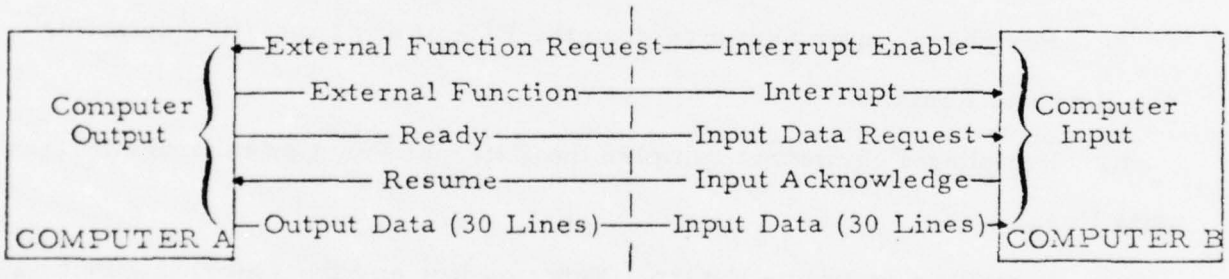
e. Peripheral equipment sets the interrupt line to indicate that the interrupt word is on the data lines.

f. The computer detects the interrupt signal and, at its convenience, accepts the interrupt word and sets the Input Acknowledge (IA).

g. The computer drops the Interrupt Enable.

h. Peripheral equipment detects the IA and clears the interrupt line and the data lines.

3-16. Intercomputer Input/Output. The control signals and lines governing intercomputer communication are shown in the following diagram.



When a computer is sending data or external function messages to a given peripheral equipment, it holds the data in its output registers for a fixed minimum time period, after which any other output or EFR on any channel can cause the data to be changed. When, however, the computer is sending

[1] Peripheral equipment not equipped with interrupt enable logic may interrupt the program using sequence steps c, d, e, f, and h.

data or external function messages to another computer, it must hold the information in its output registers until the receiving computer acknowledges receipt of those data. This acknowledge signal is received on what is known as the Resume line. When the computer is ready to transfer data, it sets what is known as the Ready line. The sequence of events for each of the two cases of intercomputer communication appears below.

3-17. Command Word Transfer. Intercomputer command word transfer from Computer A to Computer B is as follows:

a. Computer B sets the Interrupt Enable when it is ready to accept a command word from Computer A.

b. Computer A recognizes the Interrupt Enable as an External Function Request and places the External Function code on the information lines.

c. Computer A sets the External Function to indicate that the External Function code is on the information lines.

d. Computer B recognizes the External Function as an interrupt and accepts the command word at its convenience.

e. Computer B clears the Interrupt Enable line and sets the Input Acknowledge line.

f. Computer A recognizes the Input Acknowledge as a Resume and clears the External Function line.

3-18. Intercomputer Data Transfer. Intercomputer data transfer from Computer A to Computer B is as follows:

a. Computer B initiates an input buffer and Computer A initiates an output buffer for the required channel.

b. Computer A places data on the information lines.

c. Computer A sets the Ready line to indicate that the data are on the lines.

d. Computer B recognizes the Ready signal as an Input Data Request signal and, at its convenience, accepts the data word.

e. Computer B sets the Input Acknowledge.

f. Computer A recognizes the Input Acknowledge as a Resume signal and clears the Ready line and the data lines.

Steps b through f of this sequence are repeated for every data word until the number of words specified in the output buffer have been transferred.

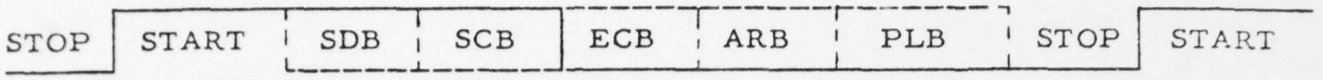
3-19. HSDS SYSTEM FUNCTIONAL DESCRIPTION.

3-20. CONVERTER UNITS.

3-21. Output Formats. The Parallel-To-Serial (P/S) converter generates a series of 7-bit frames, formatted either as the control format (one frame) or the data format (seven frames) (refer to figure 3-2). The first bit of each frame, the START bit, is always a logic high, and the last bit of each frame, the STOP bit, is always low. The transition between the STOP and START bit provides synchronization for the Phase Locked Loop (PLL) section of the receiving Serial-To-Parallel (S/P converter.

3-22. Control Format. This format contains the five bits that comprise the control information. The Output Data Acknowledge (ODA) bit, the Input Acknowledge (IA) bit, the External Function Acknowledge (EFA) bit, the External Interrupt Enable (EIE) bit, and a timing bit (PLB - Pulse Length Bit) are transmitted within this frame. The P/S converter remains in this control format mode until an input request or an output acknowledge control signal is generated by the transmitting computer (or peripheral). The P/S converter then shifts into the data format mode.

CONTROL FORMAT



DATA FORMAT

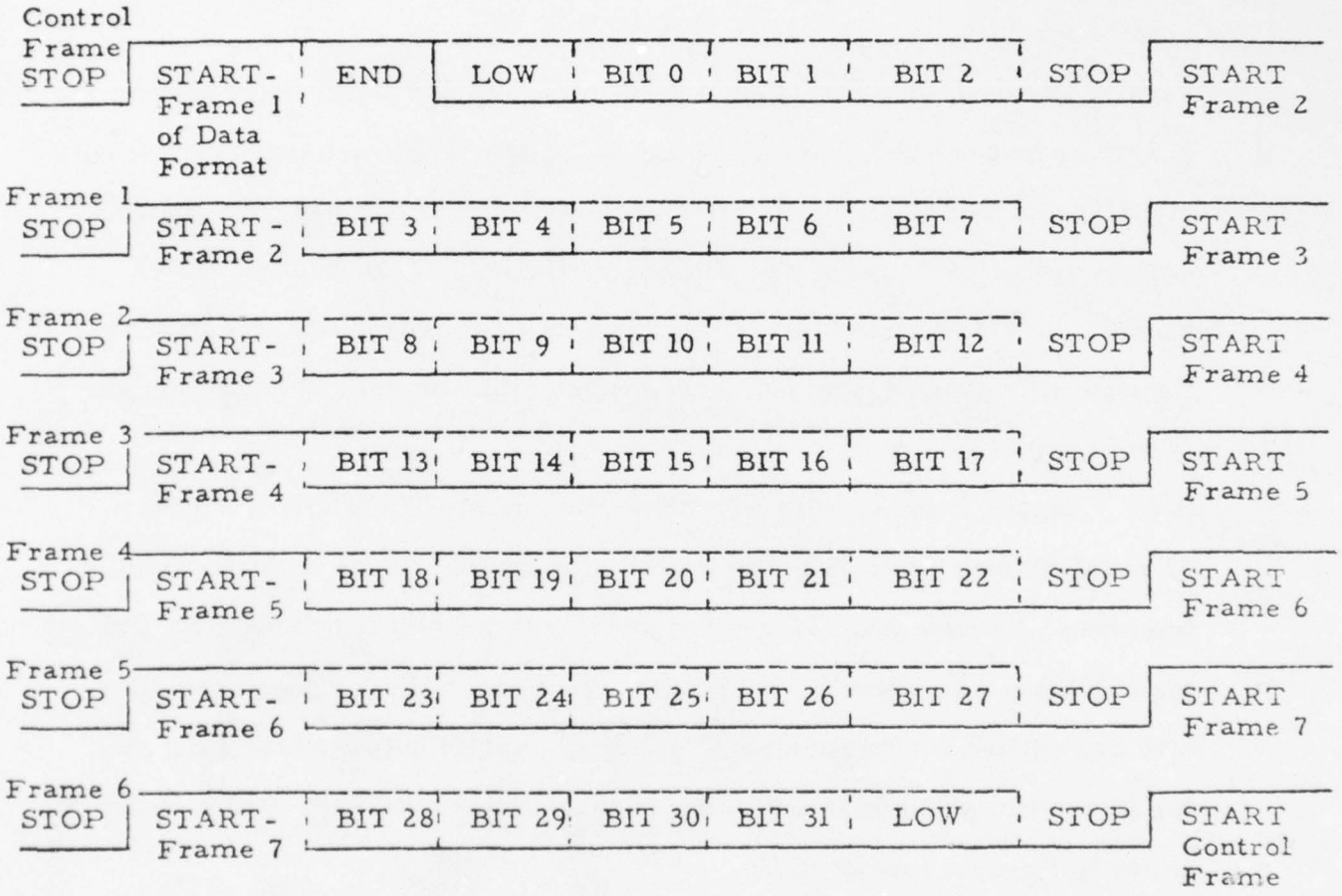


Figure 3-2. CONTROL AND DATA FORMATS

3-23. Data Format. The data format mode consists of seven frames, each of which is seven bits wide with the first bit being the start bit of each frame and the seventh being the stop bit of each frame. The data format contains 32 bits of data (maximum) plus two filler (LOW) bits and an END bit. The END bit is sent to the receiving S/P converter to indicate a shift back to the control format.

3-24. Parallel-To-Serial Converter. The P/S converter unit converts the computer or peripheral parallel outputs (data or command bits and control signals) to a serial string in which each bit represents one of the parallel outputs (refer to figure 3-1). The logic elements of the P/S converter include the clocking and formatting circuits (see figure 5-4), the parallel input circuits (see figure 5-2, Sheet 1), and the control and output circuitry (see figure 5-5).

3-25. Input Circuits. The P/S converter units provide for reception of 32 parallel input bits. The input section includes "NTDS receiver" type integrated circuits that are used to convert the external line volatages to the voltage levels used by the P/S TTL circuits. The incoming parallel bits are shifted out through parallel-input - serial output shift registers for formatting and inclusion as the data bit outputs when the P/S converter shifts to the data format mode.

3-26. Clocking And Formatting Circuits. The 16 MHz clock signal is used to generate the various framing clock (FR CLK) signals (ϕ2, ϕ4, ϕ5, and ϕ6) that load and clock the parallel input bits through the input circuit shift registers. The ϕ5 and ϕ6 FR CLK signals are also used, in conjunction with the PLD control signal, to switch the P/S converter output from the

control format to the data format mode.

3-27. Control and Output Circuits. The output logic control elements continually generate the control output format until either (a) A computer sets its ODA (SDB) signal or its EFA (SCB), or (b) A peripheral sets its IDR (SDB) line or its EIR line (SCB). Receipt of either of these two signals generates a logic high PLB (see figure 5-5) which causes the converter to shift into the data format.

3-28. SERIAL-TO-PARALLEL CONVERTER. The two components of the S/P converter are the Phase Locked Loop (PLL) section, which derives its clock from the input data stream, and the control logic, which strips the data and control bits from the input frames and provides them as parallel data to the receiving computer. The PLL section generates a stable clock for the operation of the rest of the logic in the unit.

3-29. Phase Locked Loop Section. The phase locked loop section of the S/P converter uses the frequency of the serial bit stream to extract and generate a clock signal which is used by the remaining logic. The PLL section makes use of the concept that the data rate or frequency of the serial bit stream will be a constant for some period of time and that this frequency can be recovered at the S/P converter and converted to a clock signal. To accomplish this, the PLL synchronizes the oscillator in the S/P converter to the frequency of the incoming serial bit stream. The PLL consists of an oscillator and a phase detector (see figure 5-13, Sheet 1). The phase detector compares the frequency of the incoming bit rate to the oscillator in the S/P converter. The oscillator is a voltage controlled oscillator (VCO) which means the oscillator frequency is controlled

by a dc voltage applied to a control terminal. Thus, the phase detector portion of the PLL generates a dc correction voltage to the VCO portion of the PLL. This adjusts the frequency of the VCO to that of the serial bit stream.

3-30. Control Logic. The design of the remaining logic of the S/P converter is based on the format of the serial bit stream. This logic strips the data and control bits from the input frames and provides them as parallel data to the receiving computer/peripheral. It includes circuits for clocking the serial bit stream (SB CLK) into shift registers, and for clocking the control bits (SFF CLK) and data format (LFF CLK) through shift registers and output circuits. Selectable delay circuits provide synchronization of timing with external devices.

3-31. HIGH SPEED DIGITAL SWITCH. The HSDS functional switching elements, termination, control, buffer, and built-in test equipment (BITE) circuits are contained on a total of 337 PC cards, mounted in eight card cages, A through G (see figure 3-3). The PC card assemblies are grouped in functional elements as follows (refer to figure 3-4):

a. Input circuits - These are located in card cages A and B.

b. Basic Matrix Module (BMM) PC cards - A total of 256 BMM PC cards are installed in the eight card cages.

c. Output circuits - These are located in card cages G and H.

d. Termination and control - These two PC cards are located in slots 42 and 43 of card cage C.

e. BITE transmit, receive and delay PC cards - These are located as follows slots 41, 42, and 43 of card cage E, and in slot 41 of card cage F.

(1) BITE Tx - C41
(2) BITE Control - E42
(3) " Rcv - E41
(4) " Delay E43

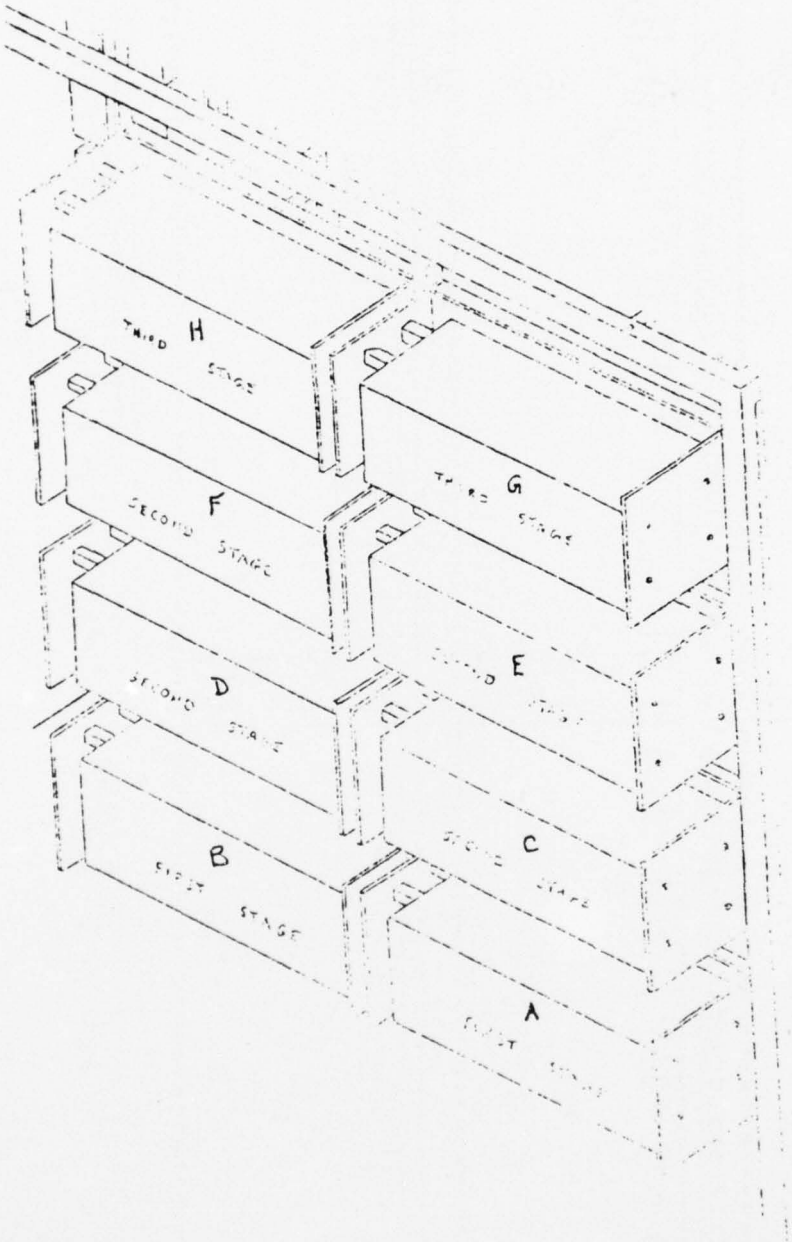


Figure 3-3. HSDS Card Cages - Front View

3-15

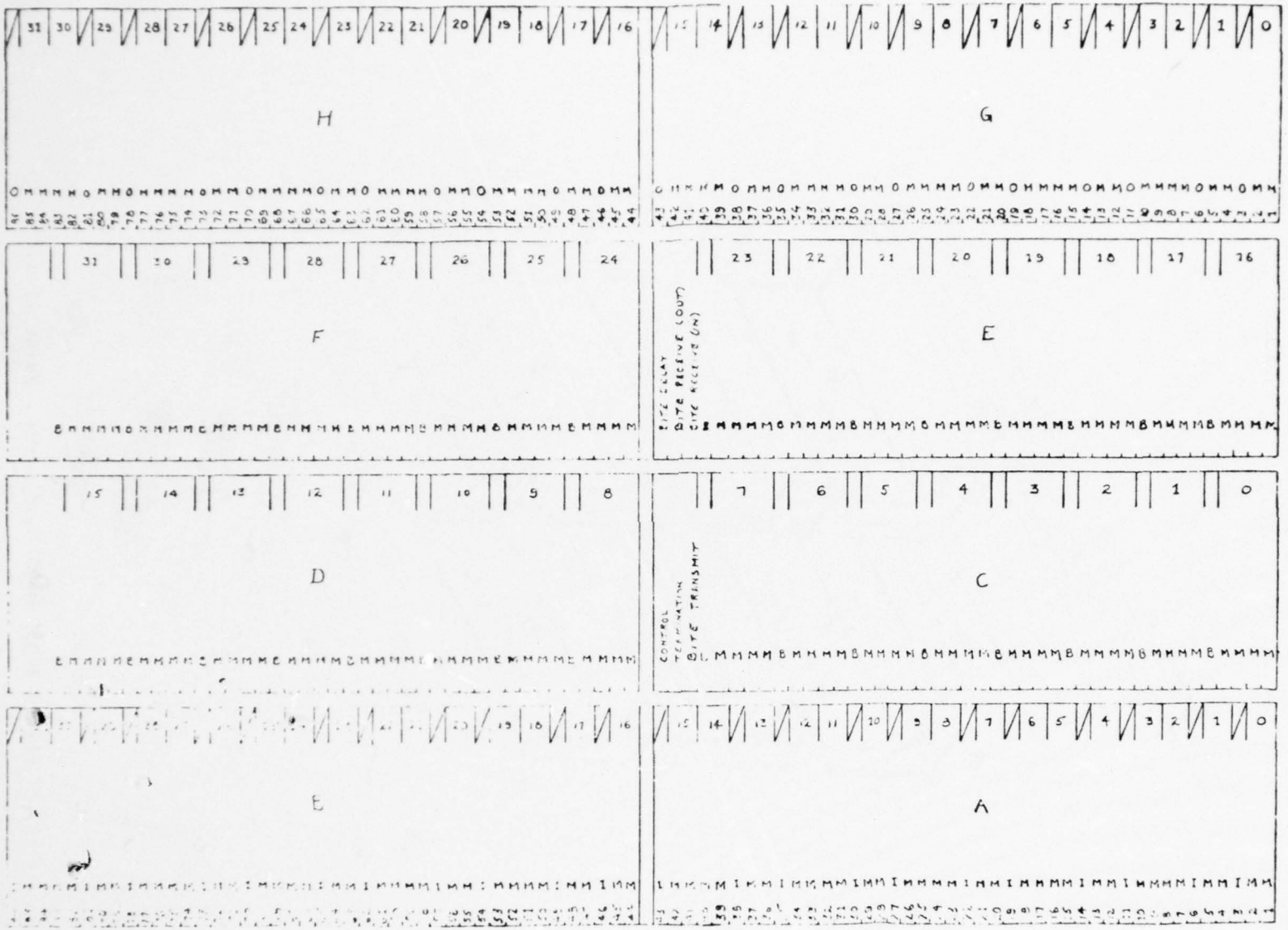


FIGURE 3-4 - NICES PC CARD/MODULE ASSIGNMENTS

1/27/76

f. Buffer circuits - Eight buffer circuit PC cards are used in each of the card cages C, D, E, and F.

3-32. Input Circuits. There are a total of 22 input circuit PC cards in card cages A and B. Twenty of these terminate 24 input channels (480 channels) while the 11th card in each cage (see figure 3-4) is used to terminate 16 channels (i.e., 8 of the 24 inputs are not used). Twisted wire pairs are used to connect the outputs of the input circuit PC cards to the BMM cards in cages A and B.

3-33. Matrix Switching. Any one of the 512 input channels to the HSDS may be switched to any one of the 512 output channels via groups of modules in each of three stages. A "module," as defined for the HSDS, is a grouping of two BMM PC cards for stages 1 and 3, and four BMM PC cards for stage 2. The allocation and distribution of the BMM PC cards is such that each stage contains 32 "modules" (refer to figures 3-4 and 3-5). Each Stage 1 module is wired to accept 16 inputs and to provide 32 outputs; each Stage 2 module provides for 32 inputs and 32 outputs; and each Stage 3 module accepts 32 inputs and is wired to output to 16 channels.

3-34. Stage 1. Since each input circuit card contains 24 inputs and each Stage 1 module is interconnected to provide for only 16 inputs, two input circuit PC cards are used with three Stage 1 modules to enable input of the eight additional channels on each of the two input cards (see figure 3-6/A). A series of five of these groups in each of the card cages A and B provides for 480 input channels (10 x 48). The last three cards of each card cage, A and B, are connected as shown in figure 3-6/B to provide for input/output of the remaining 32 channels. Any one of the 16 inputs to a module can be connected to any one of the 32 outputs (see figure 3-6), i.e., any one input

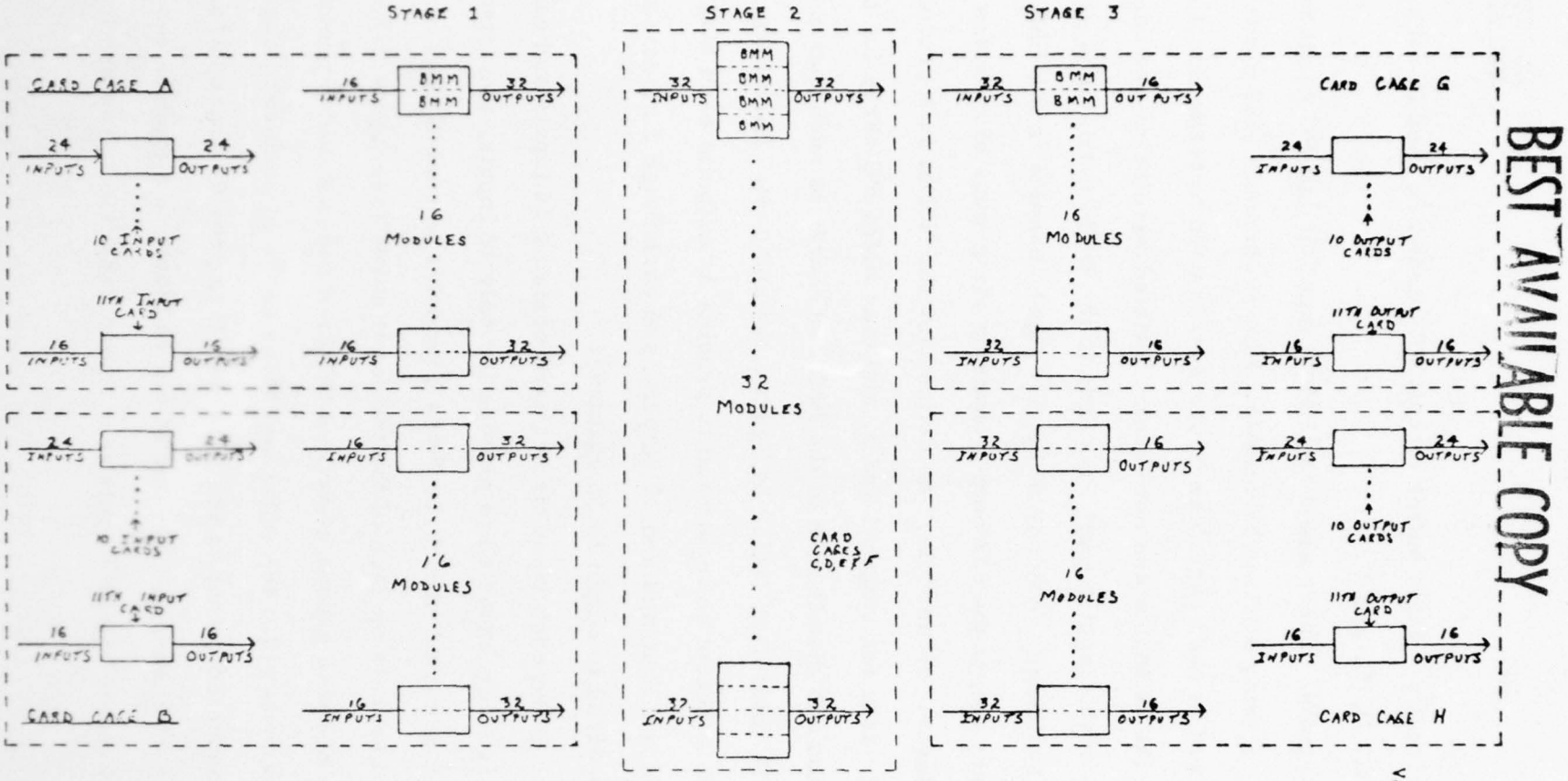
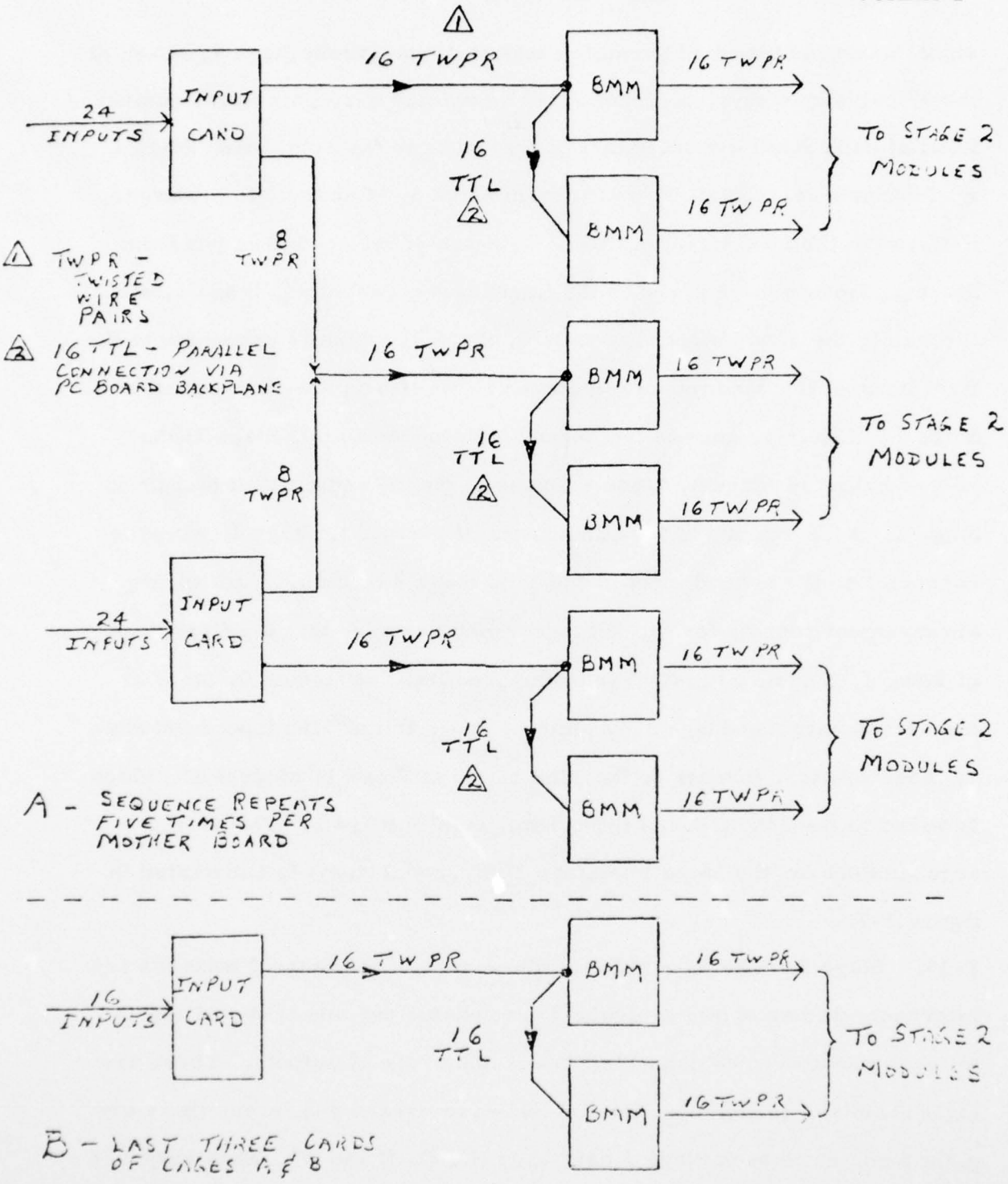


FIGURE 3-5. HSDS INPUT/OUTPUT BY STAGES



Pages 3-6, Unit - Stage 1 [illegible]

1.

signal has a choice of 32 possible paths for output from Stage 1. Each of the 32 outputs is physically connected by twisted wire pair to the numbered input of each Stage 2 module that corresponds to the originating Stage 1 module number. The first output from Stage 1, Module 0, for example, is wired to the first input of Module 0, Stage 2; the second output from Stage 1, Module 0, is wired to the first input of Module 1, Stage 2, etc., through to the 32nd output of Module 0, Stage 1, which is connected to the first input of the 32nd module in Stage 2. Similarly, the first output of Stage 1, Module 1, goes to the second input of Module 0, Stage 2; the second output of Stage 1, Module 1 goes to the second input of Module 1, Stage 2, etc., through to the 32nd output of Module 1, Stage 1, which is connected to the second input of the 32nd Stage 2 module. This wiring arrangement repeats for all 32 Stage 1 modules such that the first output of Stage 1, Module 31, is wired to the 32nd input of Module 0, Stage 2; the second output of Stage 1, Module 31, goes to the 32nd input of Module 1, Stage 2, etc., through to the 32nd output of Stage 1, Module 31, which is wired to the 32nd input of the 32nd module in Stage 2. The wiring arrangement for the Stage 1 to Stage 2 interconnections is illustrated in figure 3-7.

3-35. Stage 2. The four BMM cards in each of the Stage 2 modules are interconnected as shown in figure 3-8 to enable any one of the 32 inputs (of each module) to be connected to any one of its 32 outputs. There are eight groups of interconnections as shown in figure 3-8, i.e., there are eight modules in each Stage 2 card cage (C, D, E and F). Each output of the 32 modules is connected by twisted wire pair to the Stage 3 modules,

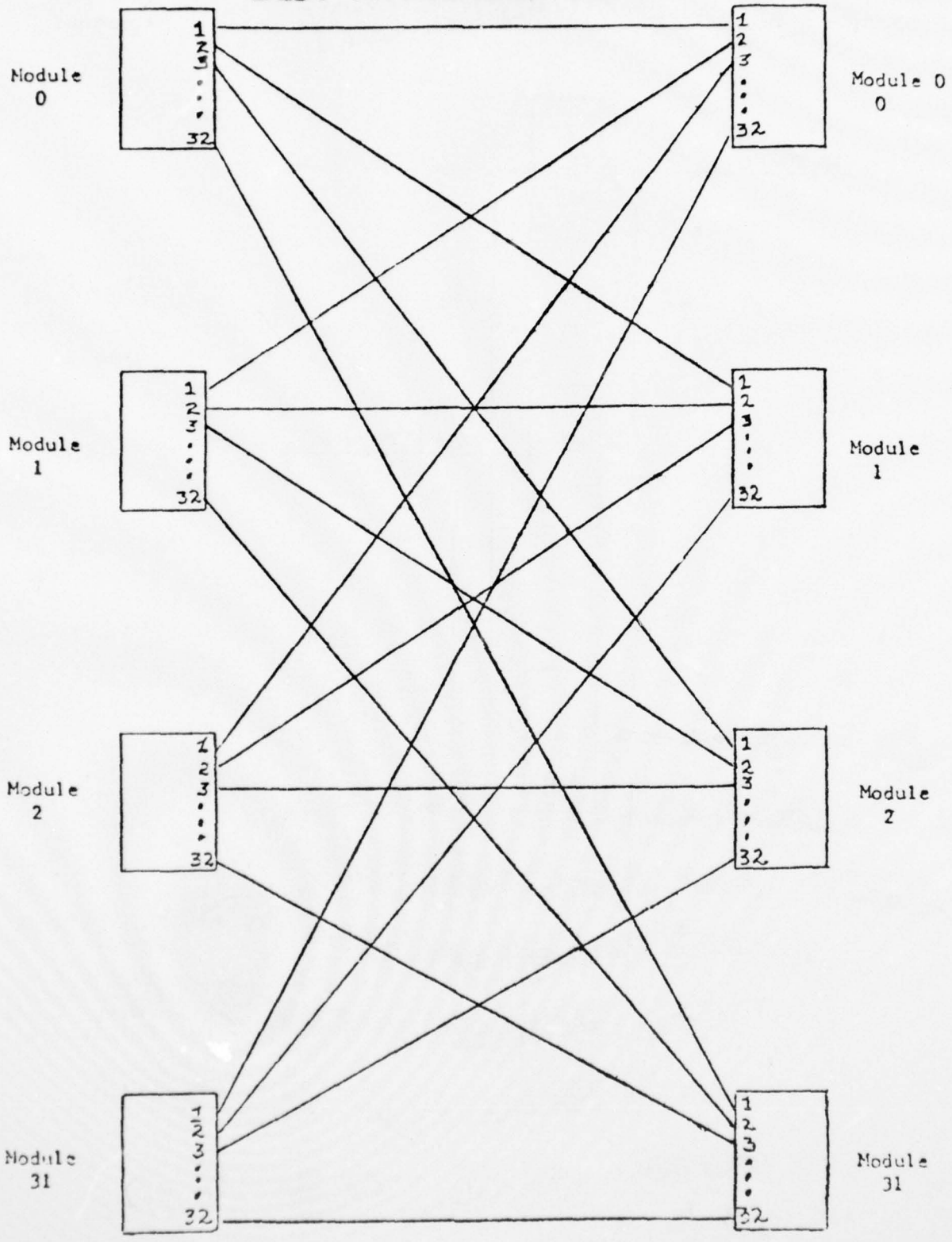
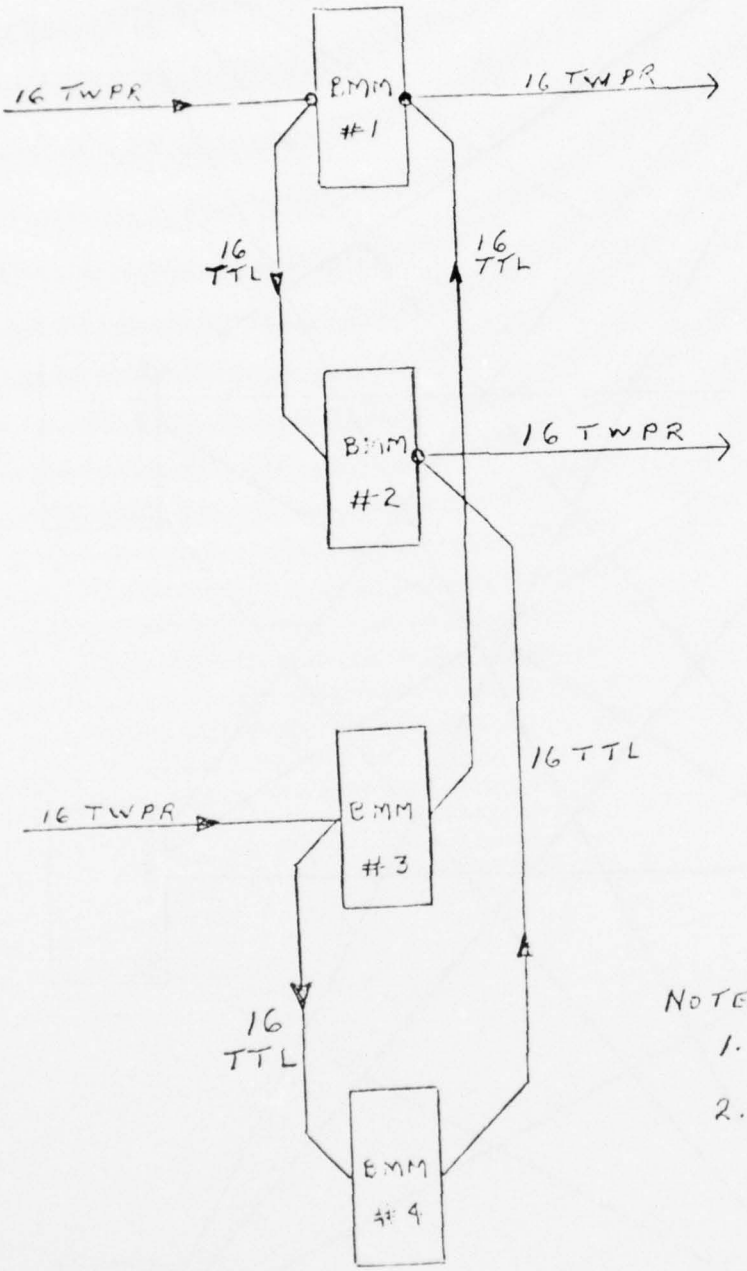


Figure 3-7. Stage 1 - Stage 2 Interconnectivity



NOTES:

1. TWPR - TWISTED WIRE PAIRS
2. 16 TTL - PARALLEL CONNECTIONS VIA PC BOARD BACKPLANE

FIGURE 3-8. STAGE 2 MODULE INTERCONNECTS

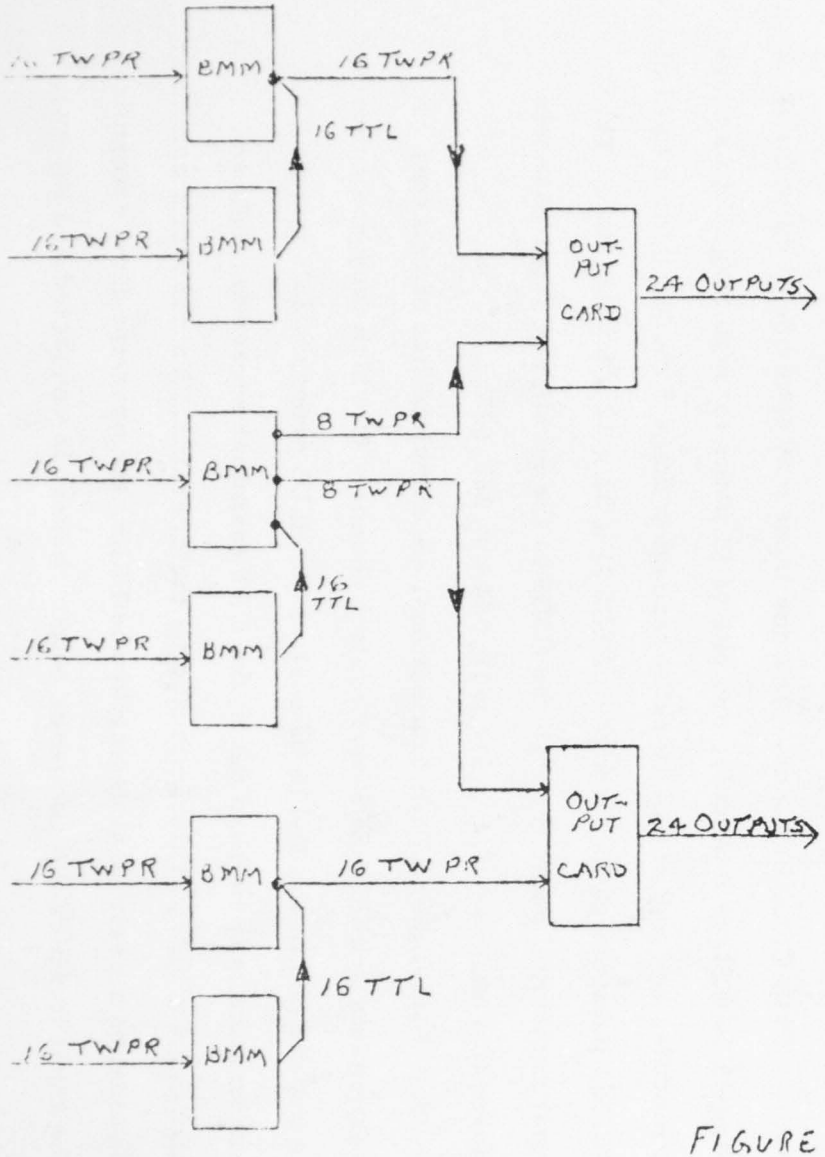
3-22

following the same pattern as those between Stage 1 and Stage 2 modules.

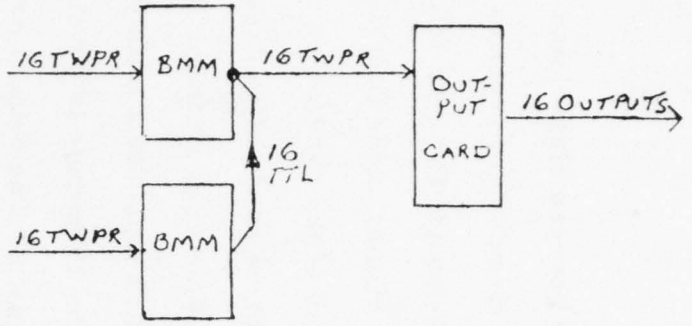
3-36. Stage 3. Since each output circuit card contains 24 outputs and each Stage 3 module is interconnected to provide for only 16 outputs, three Stage 3 modules are used with two output circuit cards (see figure 3-9/A). A series of five of these groups in each of the card cages G and H provides for 480 output channels. The last three cards of each card cage, G and H, are connected as shown in figure 3-9/B) to provide for input/output of the remaining 32 channels. Any one of 32 inputs to a module can be connected to any one of 16 outputs. Each of the 16 outputs is physically connected to an output circuit card by twisted wire pair. The outputs are connected by RG179B/U coaxial cable from jack-pin terminations on the output cards to matrix locations on the HSDS coaxial cable connector panel.

3-37. Path Configurations. Any one input may take one of 32 paths through Stage 1 to a Stage 2 module, any one of 32 paths through Stage 2 to a Stage 3 module, and any one of 16 paths through a Stage 3 module, for a total of 16,384 possible paths through th HSDS (1 x 32 x 32 x 6 = 16,384). The total number of paths through the HSDS is the number of input channels times this number, i.e., 512 x 16,384 = 8,388,608.

3-38. Establishing Path Connections. A complete list of external equipments and the HSDS input/output channels to which they are connected, is maintained in the D-116 as part of the HSDS program data base. This information may be read out to the CRT terminal screen through an appropriate entry at the keyboard by the operator. To connect a computer channel to a peripheral device by the HSDS, the operator first determines the input to which the computer output channel is connected and the switch



A - SEQUENCE REPEATS FIVE TIMES PER MOTHER BOARD



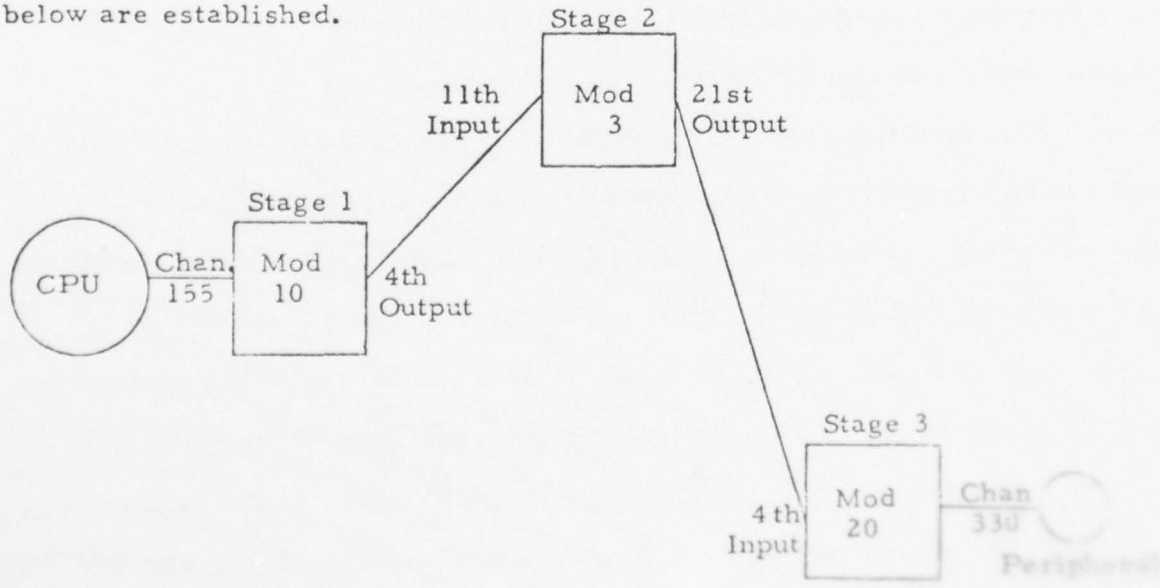
B - LAST THREE CARDS OF CAGES G & H

NOTES:

1. TWPR - TWISTED WIRE PAIR
2. 16 TTL - PARALLEL CONNECTIONS VIA PC BOARD BACKPLANE.

FIGURE 3-9. STAGE 2 MODULE - OUTPUT CIRCUIT INTERCONNECTS

output to which the peripheral equipment is connected. When these have been determined and have been entered by the operator, the program determines whether the input and/or output is in use, i.e., if either the computer or the peripheral equipment is already connected to some other piece of equipment. If neither is in use, the program then searches for a Stage 2 module that has both a free inpuj from the Stage 1 module to which the computer is connected and an unused output to the Stage 3 module to which the peripheral is connected. The program progresses numerically from the lowest numbered module in Stage 2. If, for example, it is desired to connect the Channel 155 input from Module 10 in Stage 1 to the Channel 330 output of Module 20 in Stage 3, the program first determines which of the Stage 2 modules that have a free 11th input from Module 10 in Stage 1, also have a free output path (th 21st) to Module 20 in Stage 3. Assuming an available path is found via Stage 2, Module 3, the links as diagrammed below are established.



AD-A051 075 NAVAL OCEAN SYSTEMS CENTER SAN DIEGO CA F/G 17/2
ADAPTABLE SHIPBOARD TACTICAL DATA DISTRIBUTION SYSTEM. (U)
DEC 77 H C SCHLEICHER
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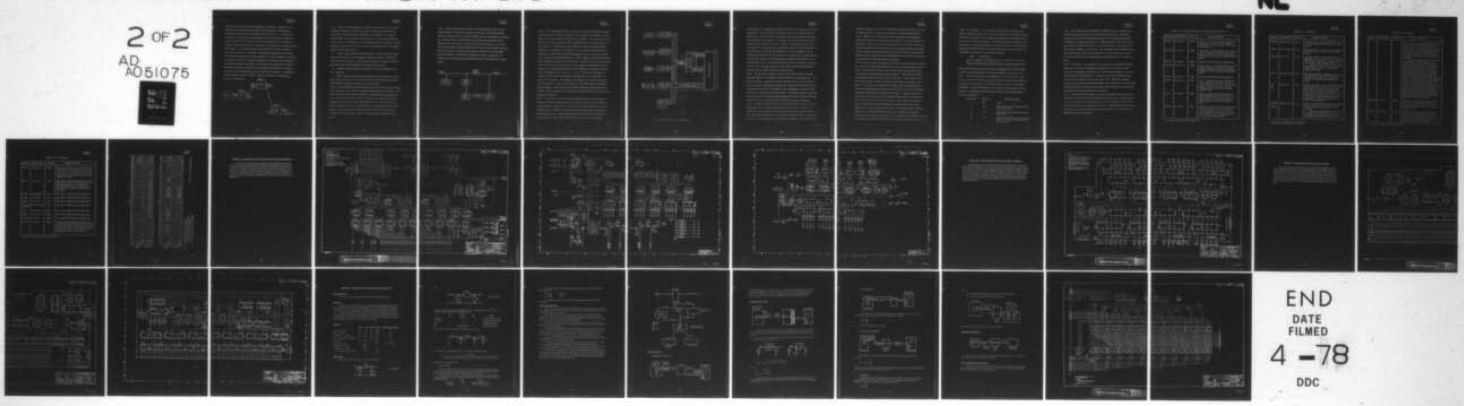

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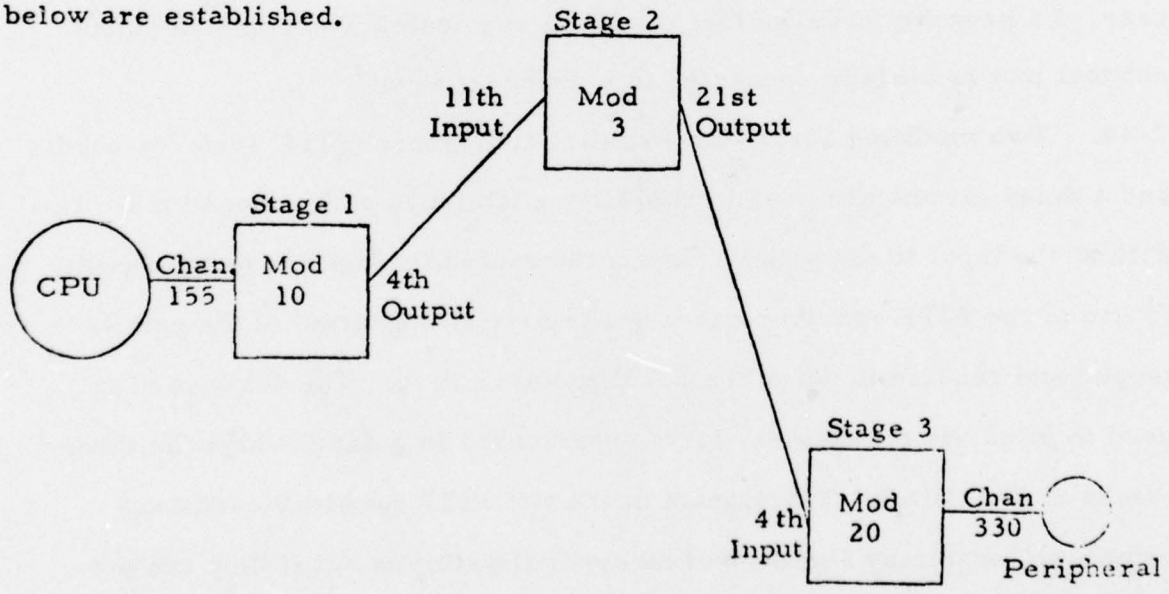
DDC

output to which the peripheral equipment is connected. When these have been determined and have been entered by the operator, the program determines whether the input and/or output is in use, i.e., if either the computer or the peripheral equipment is already connected to some other piece of equipment. If neither is in use, the program then searches for a Stage 2 module that has both a free inpuj from the Stage 1 module to which the computer is connected and an unused output to the Stage 3 module to which the peripheral is connected. The program progresses numerically from the lowest numbered module in Stage 2. If, for example, it is desired to connect the Channel 155 input from Module 10 in Stage 1 to the Channel 330 output of Module 20 in Stage 3, the program first determines which of the Stage 2 modules that have a free 11th input from Module 10 in Stage 1, also have a free output path (th 21st) to Module 20 in Stage 3. Assuming an available path is found via Stage 2, Module 3, the links as diagrammed below are established.



3-25

3-39. Built-In Test Equipment. The basic function of the Built-In Test Equipment (BITE) is to check the possible paths through the switch to ensure that valid throughput connections are available, i.e., that the output signals on a given path are the same as, or match, the input data for that path. The HSDS control program provides for continuous checking of paths by the BITE subsystem, on a non-interference basis. The types paths the BITE checks are:

a. Paths being established by the operator. In the event data input/output mis-matches, or "no compares" are discovered on a path just established by the operator, the program searches for another available path and the faulty path notation is entered in an error log.

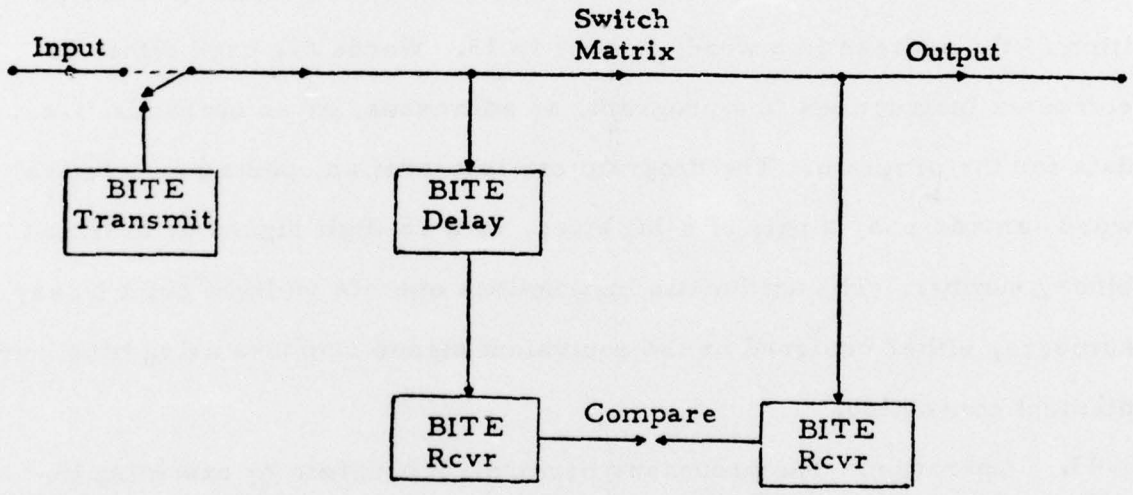
b. Already established path connections, to ensure continued error-free operation.

c. Input channels that are not connected to any switch output. In this case, the program ensures that the BITE el minates checking any output channel that is already connected to a different input .

3-40. Two modified Serial-To-Parallel converters (BITE receiver cards) and a delay circuit are used in checking established path connections. The data at the input to the path is tapped and routed through the delay circuit to one of the BITE receiver cards. The data at the output of the path is tapped and reouted to the other BITE receiver card. The delay card is used to simulate the delay a signal experiences in going through the three stages of the switch. The signals at the two BITR receiver cards are compared, frame by frame, and an error flip-flop is set if they are not equal.

3-26

3-41. To check inputs that do not have established path connections to switch outputs, a special test signal is injected by a BITE transmitter card into the path prior to where the BITE receiver/delay cards are tapped in. The input path is switched from the normal input path flow to the BITE transmit connection as shown in the following diagram. The BITE test signal is then received by both the first and the second BITE receivers and the two outputs compared as is done for serial data on established path connections. The BITE test signal has a unique configuration to ensure non-recognation by equipment that may be connected to the switch outputs.



3-27

3-42. D-116 MINICOMPUTER. The D-116 is a general purpose computer system utilizing a 16-bit word length. The computer includes four accumulators, two of which may be used as index registers. The central processor governs all peripheral input/output equipment and the operation of the interface modules. It performs all the arithmetic, logical and data handling operations and sequences the program. It is connected to the memory by a memory bus and to the peripheral equipment by an in-out bus (see figure 3-9). The processor handles words of 16 bits, which are stored in memory with a maximum capacity of 64,336 words. The bits of a word are numbered 0 to 15, left to right, as are the bits in the registers that handle the words. Registers that hold addresses are 15 bits, numbered according to the position of the address in a word, i.e., 1 to 15. Words are used either as computer instructions in a program, as addresses, or as operands, i.e., data for the program. The program can interpret an operand as a logical word, an address, a pair of 8-bit bytes, or a 16-digit signed or unsigned binary number. The arithmetic instructions operate on fixed point binary numbers, either unsigned or the equivalent signed numbers using twos complement convention.

3-43. Operation. The processor performs a program by executing instructions retrieved from consecutive memory locations as counted by the 15-bit program counter (PC). At the end of each instruction, PC is incremented by one so that the next instruction is normally taken from the next consecutive location. Sequential program flow is altered by changing the contents of PC, either by incrementing it an extra time in a test skip

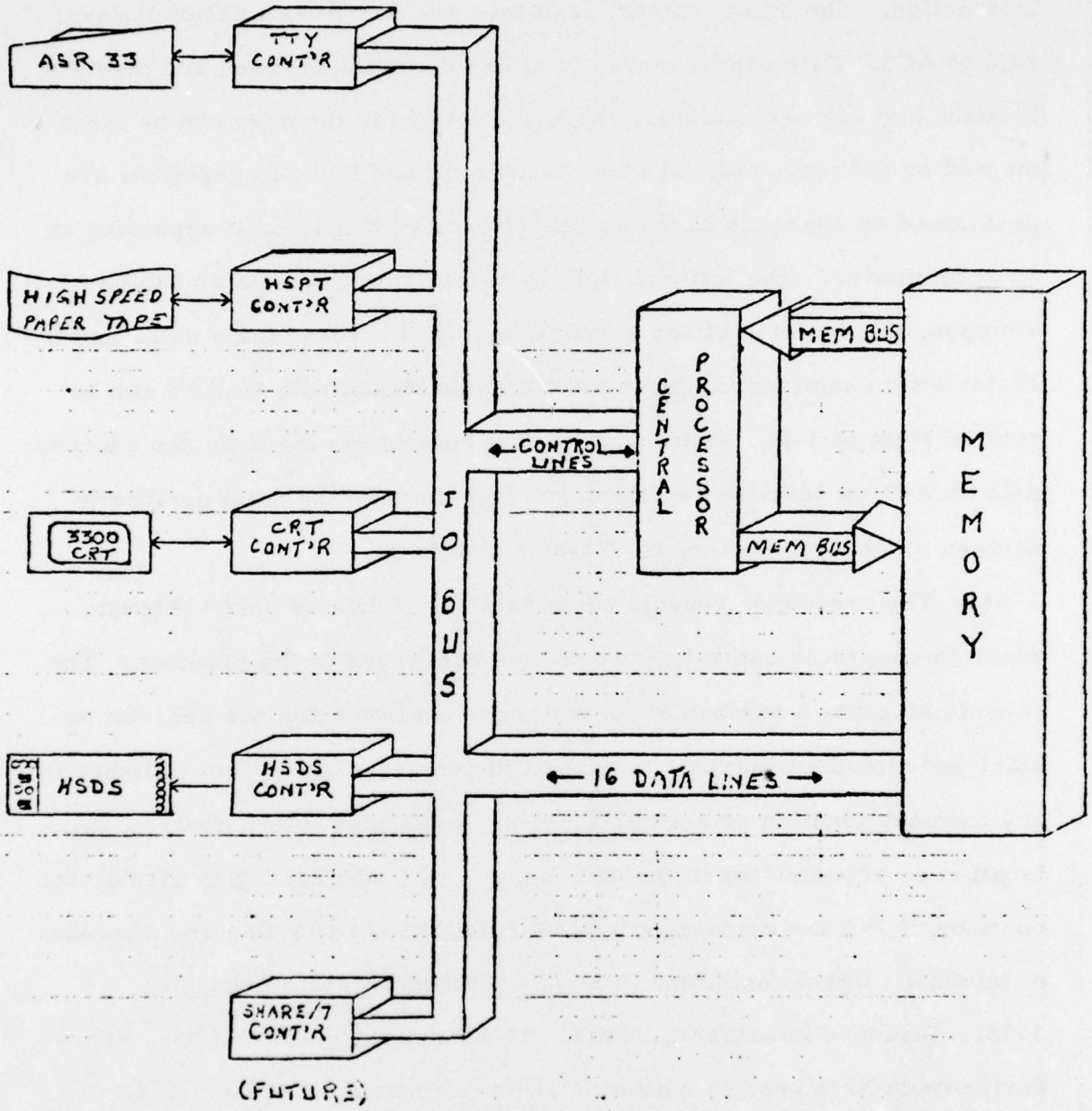


FIGURE 3-10. D-16 ORGANIZATION

3-29

instruction or by replacing its contents with the value specified by a jump instruction. The other internal registers are four 16-bit accumulators, AC0 to AC3. Data can be moved in either direction between any memory location and any accumulator. Although a word in memory can be incremented or decremented, all other arithmetic and logical operations are performed on operands in the accumulators, with the result appearing in an accumulator. The left and right halves of any accumulator can be swapped, the contents of any accumulator can be tested for a skip, and the 17-bit word contained in any accumulator combined with CARRY can be rotated right or left. An instruction that references memory can address AC2 or AC3 as an index register, and transfers to and from peripheral devices are also made through the accumulators.

3-44. The processor console contains a set of data switches through which the operator can supply words and addresses to the program. The console also has a number of control switches that allow the operator to start and stop the program, to deposit the contents of the data switches in any memory location or accumulator, and to display the contents of any location or accumulator in the data lights. The address lights display the contents of PC; the remaining lights display the CARRY flag and a number of internal control conditions that are useful in program debugging.

3-45. Standard Interface Circuits. To connect to the in-out bus, every device must have certain fundamental circuit networks. Each device must have a 6-bit selection net to guarantee that the device will respond when and only when its device code is given by the program; a "busy-done" net to specify the device state and request interrupts; a net to determine

the interrupt priority in terms of the device position on the bus; and a net to supply the device code when an interrupt is acknowledged (INTA).

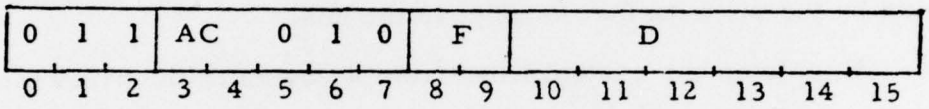
3-46. Signals on the control lines from the processor to peripheral devices synchronize all transfers on the data lines, start and stop device operations, and control the program interrupts. In addition, signals on the control lines from the processor not only specify particular functions but also supply all timing information needed for execution of those functions as well as supply all other timing functions that may need to be performed by the cirucits that connect to the bus.

3-47. Signals on the control lines from a device to the processor indicate the states of its BUSY and DONE flags, or may request a program interrupt. A given device needs to connect only to those control lines that correspond to the functions the device requires. The BUSY and DONE flags together denote the basic state of the device. When both are clear, the device is idle. To place the device in operation, the program sets BUSY. If the device is to be used for output, the program must give a data-out instruction that sends the first unit of data, a word or character, depending on how the device handles information. When the device has processed a unit of data, it clears BUSY and sets DONE to indicate that it is ready to receive new data for output, or that is has data ready for input. In the former case, the program responds with a data-out instruction to bring in the data that is ready. If the INTERRUPT DISABLE flag is clear, setting the DONE flip-flop (FF) signals the program by requesting an interrupt; if the program has set INTERRUPT DISABLE, then it must keep testing DONE or BUSY to determine when the device is ready.

3-31

3-48. Data Transfer. For in-out data transfer the program senses BUSY or DONE or allows the device to interrupt when it requires service. The transfer of data to or from peripheral equipment is governed by the in-out class of instruction words. These instructions also cause various operations to be performed within the central processor. The following diagram illustrates an instruction word used for data output as well as requesting performance of a processor function.

DOA DATA OUT A



(This instruction directs the contents of accumulator AC to the A buffer in device D and performance of function specified by F in device D.)

3-49. An in-out instruction is designated by "011" in bits 0-2. Bits 10-15 are used to encode the 2-digit octal address of the device that is to respond to the instruction. Bits 8 and 9 either control or sense BUSY and DONE. In those instructions in which bits 8 and 9 specify a control function, the mnemonics and bit configurations and the functions they select are as follows:

Mnemonic	Bits 8-9	Control function
	00	None
S	01	Start the device by clearing Done and setting Busy
C	10	Clear both Busy and Done, idling the device
P	11	Pulse the special in-out bus control line - the effect, if any, depends on the device

3-50. The overall sequence of BUSY and DONE states is determined by both the program and the internal operation of the device. The data-in or data-out instriction that the program gives in response to the setting of DONE can also restart the device. When all data has been transferred, the program usually clears DONE so the device neither requests further interrupts nor appears to be in use. Bits 5-9 specify the complete function to be performed. If there is no transfer (bits 5-7 all alike) bits 3 and 4 are ignored and bits 8 and 9 may specify a control function or a skip condition.

3-51. In-Out Bus. The central processor governs all peripheral equipment and is connected to peripheral equipment by an in-out bus which contains 16 bidirectional data lines, six device selection lines, 19 control lines from the central processor to devices, and six control lines from devices to the central processor (see table 3-2). Within the computer chassis the in-out bus consists of printed circuit connections on a vertically mounted PC board. These circuits connect like-numbered A and B receptacle pins of the PC board slots to one another.

3-52. For each slot that requires external connection, the in-out bus is extended to the chassis jacks by means of 52-wire cables. The pins for the in-out bus signals are as shown in figure 3-10. (Viewed from the rear of the PC board, the A connector is on the left.) Shaded positions are used by the memory bus and blank positions have been used for the interface and HSDS data and control signals.

Table 3-2. IN-OUT BUS DATA AND CONTROL SIGNALS

SIGNAL	DIRECTION	LEVEL	EXPLANATION
DATIA	To device	High	Data in A. Generated by the processor during a DIA to place the A buffer in the device selected by DS0 - DS5 on the data lines.
DATOB	To device	High	Data out B. Generated by the processor after AC has been placed on the data lines in a DOB to load the data into the B buffer in the device selected by DS0-DS5.
DATIB	To device	High	Not used in HSDS System application.
DATOC	To device	High	Data out C. Generated by the processor after AC has been placed on the data lines in a DOC to load the data into the C buffer in the device selected by DS0 - DS5.
DATIC	To device	High	Not used in HSDS System application.
STRT*	To device	High	Start. Generated by the processor in any nonskip IO instruction with an S control function (bits 8-9 = 01) to clear Done, set Busy, and clear the INT REQ flip-flop in the device selected by DS0 - DS5.
CLR*	To device	High	Clear. Generated by the processor in any nonskip IO instruction with a C control function (bits 8-9 = 01) to clear Busy, Done, and the INT REQ flip-flop in the device selected by DS0 - DS5.
IOPLS*	To device	High	IO Pulse. Generated by the processor in any nonskip IO instruction with a P control function (bits 8-9 = 11) to perform some special function in the device selected by DS0 - DS5 (this signal is for custom applications).

* Not used in HSDS System application

3-34

Table 3-2. (Continued)

SIGNAL	DIRECTION	LEVEL	EXPLANATION
SELB*	To processor	Low	Selected Busy. Generated by the device selected by DS0 - DS5 if its Busy flag is set.
SELD*	To processor	Low	Selected Done. Generated by the device selected by DS0 - DS5 if its Done flag is set.
RQENB*	To device	Low	Request Enable. Generated at the beginning of every memory cycle to allow all devices on the bus to request program interrupts or data channel access. In any device RQENB sets the INT REQ flip-flop if Done is set and Interrupt Disable is clear. Otherwise it clears INT REQ.
INTR*	To processor	Low	Interrupt Request. Generated by any device when its INT REQ flip-flop is set. This informs the processor that the device is waiting for an interrupt to start.
DS0 to DS5	To device	Low	Device Selection. The processor places the device code (bits 10 - 15 of the instruction word) on these lines during the execution of an in-out instruction. The lines select one of 59 devices (codes $_{8}$ 04 - 76) that may be connected to the bus. Only the selected device responds to control signals generated during the instruction.
DATA0 ** to DATA15	Bidirectional	Low	Data. All data and addresses are transferred between the processor and the devices attached to the bus via these 16 lines. For programmed output, the processor places the AC specified by the instruction on the data lines into the corresponding buffer in the device selected

* Not used in HSDS System application.
** DATA0 through DATA3 not used.

3-35

Table 3-2. (Continued)

SIGNAL	DIRECTION	LEVEL	EXPLANATION
			by DS0 - DS5, or generates MSKO to set up the Interrupt Disable flags in all of the devices according to the mask on the data lines. For data channel output, the processor places the memory buffer on the data lines and generates DCHO to load the contents of the lines into the data buffer in the device that is being serviced. For programmed input, the processor generates DATIA, DATIB, or DATIC to place information from the corresponding buffer in the device selected by DS0-DS5 on the data lines, or generates INTA to place the code of the nearest device that is requesting an interrupt on lines 10-15. The processor then loads the data from the lines into the AC selected by the instruction. To get an address for data channel access, the processor generates DCHA to place a memory address from the nearest device that is requesting access on lines 1-15 and then loads the address into the memory address register. For data channel input, the processor generates DCHI to place the data buffer of the device being serviced on the data lines and then loads the contents of the lines into the memory buffer.
DATOA	To device	High	Data Out A. Generated by the processor after AC has been placed on the data lines in a DOA to load the data into the A buffer in the device selected by DS0 - DS5.
INTP*	To device	Low	Interrupt Priority. Generated by the processor for transmission serially to the devices on the bus. If the INT REQ flip-flop in a device is clear when the device receives INTP, the signal is transmitted to the next device.

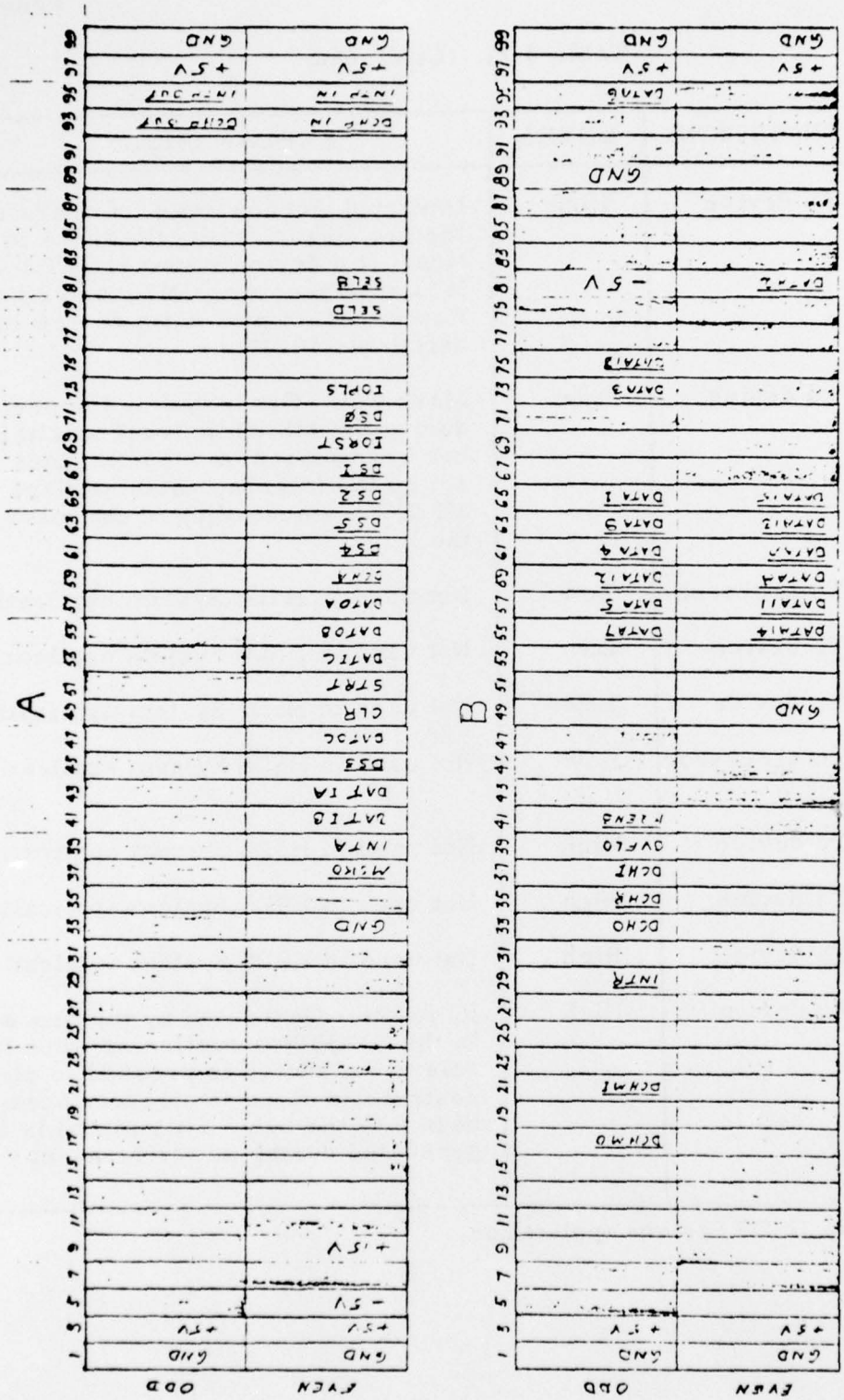
* Not used in HSDS System application.

3-36

Table 3-2. (Continued)

SIGNAL	DIRECTION	LEVEL	EXPLANATION
INTA*	To device	High	Interrupt Acknowledge. Generated by the processor during the INTA instruction. If a device receives INTA while it is also receiving INTP and its flip-flop is set, it places its device code on data lines 10-15.
MSKO	To device	Low	Mask Out. Generated by the processor during the MSKO instruction after AC has been placed on the data lines to set up the Interrupt Disable flags in all devices according to the mask on the lines.
DCHR	To processor	Low	Not used in HSDS System application.
DCHP	To device	Low	Not used in HSDS System application.
DCHA	To device	Low	Not used in HSDS System application.
DCHM0 DCHM1	To processor	Low	Not used in HSDS System application.
DCHI	To device	High	Not used in HSDS System application.
DCHO	To device	High	Not used in HSDS System application.
OVFLO	To device	High	Not used in HSDS System application.
IORST*	To device	High	IO Reset. Generated by the processor in the IORST instruction or when the console reset switch is pressed to clear the control flip-flops in all interfaces connected to the bus. This signal is also generated during power turn-on.

* Not used in HSDS System application.



Notes: 1. Two connectors (A and B) for each slot.
2. Shaded portions are used by memory bus.
3. Blank positions indicate pins available for use on interface and multiplex boards.
4. Cabling from back panel to external equipment is made via connectors at back of processors.

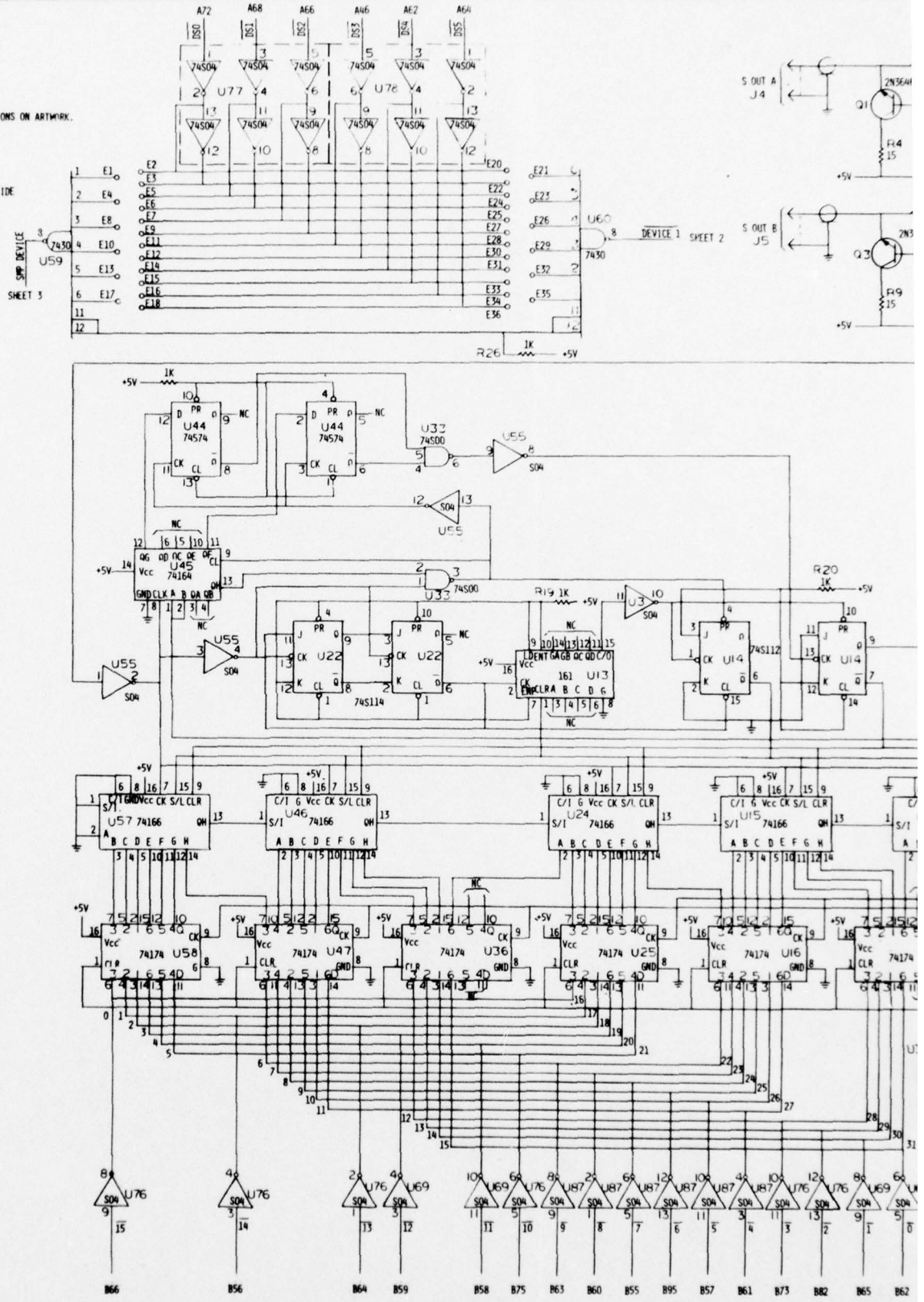
Figure 3-11. D-116 Back Panel Connectors

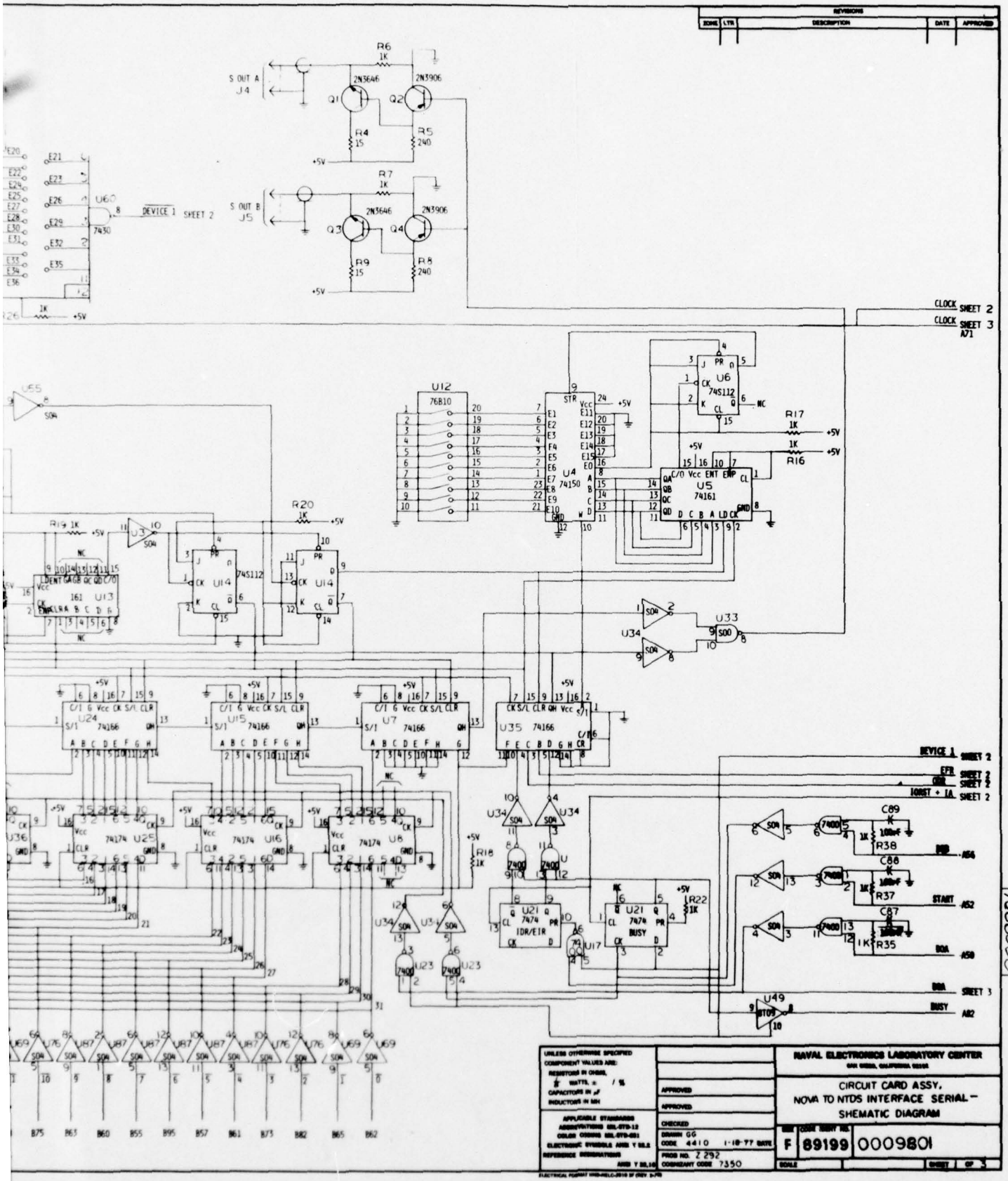
APPENDIX D: REDESIGN OF DATA GENERAL NOVA CONTROL COMPUTER

The Data General NOVA Control computer is a 16-bit machine which normally exchanges data on 16 bidirectional data lines using six device selection lines and nineteen control lines. A redesign of the NOVA board provides a serial interface with the tactical computers. The timing and functions for this interface are described in Appendix A. In addition, circuitry has been added which allows the NOVA to interface with the SMP converter card. This allows the NOVA to perform the SMP function. Drawing 0009801 is a schematic of the redesigned NOVA to NTDS interface. Sheet three of the schematic is the SMP interface.

NOTES:

1. INTERPRET DRAWING PER MIL-STD-100.
2. REFERENCE DRAWINGS:
   CIRCUIT CARD ASSEMBLY 89199-0009799
   PRINTED WIRING BOARD 89199-0009800
3. REFERENCE DESIGNATIONS E1 - E54 ARE JUMPER TERMINATIONS ON ARTWORK.
4. ALL CAPACITORS ARE CKO5 TYPE
5. THERE IS A .022μF CAPACITOR LOCATED NEAR EACH IC.
6. J1-J6 ARE SELECTRO 51-1 3-0109 LOCATED ON OPPOSITE SIDE OF BOARD FROM CONNECTOR A & B 1.5" FROM EDGE.

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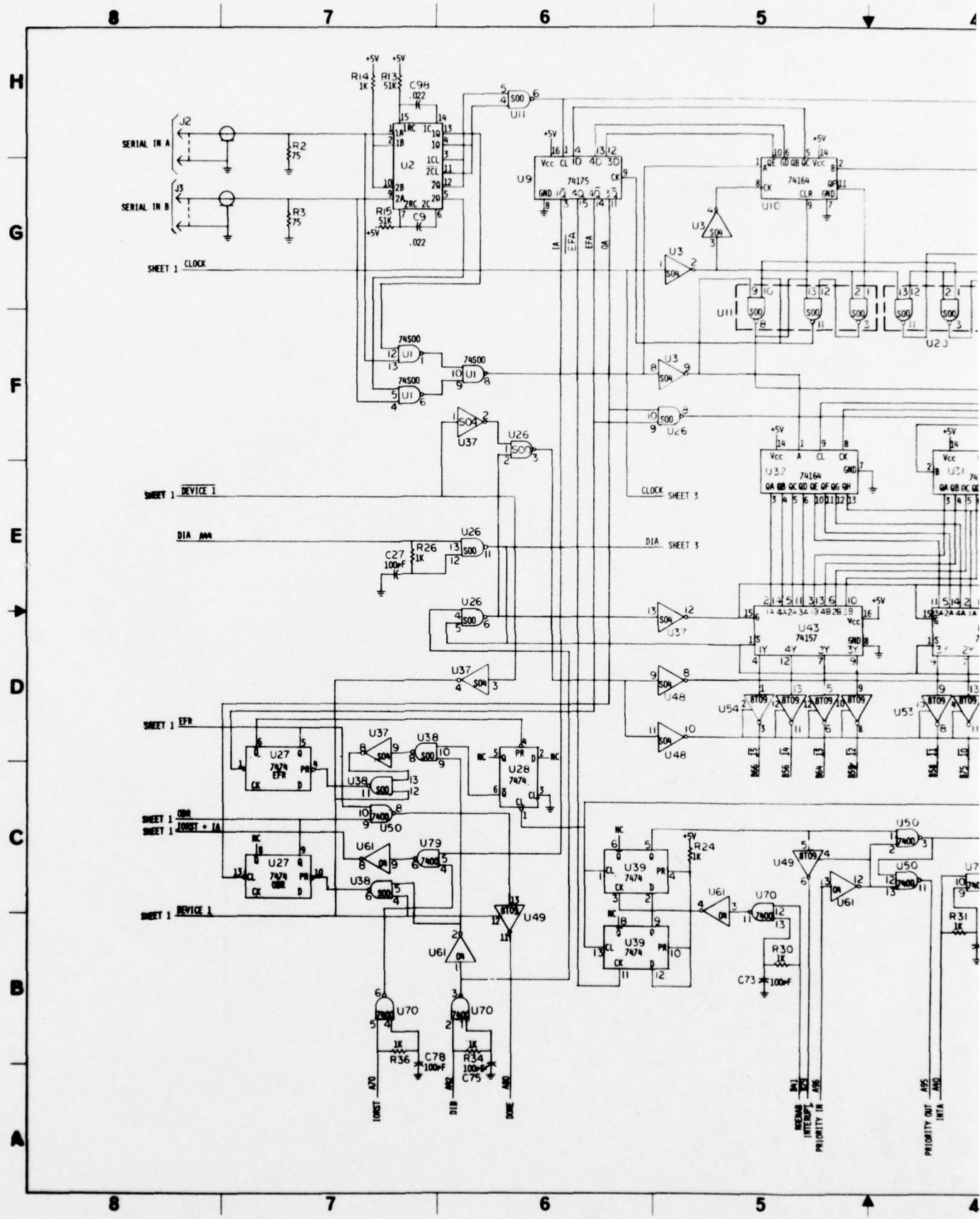
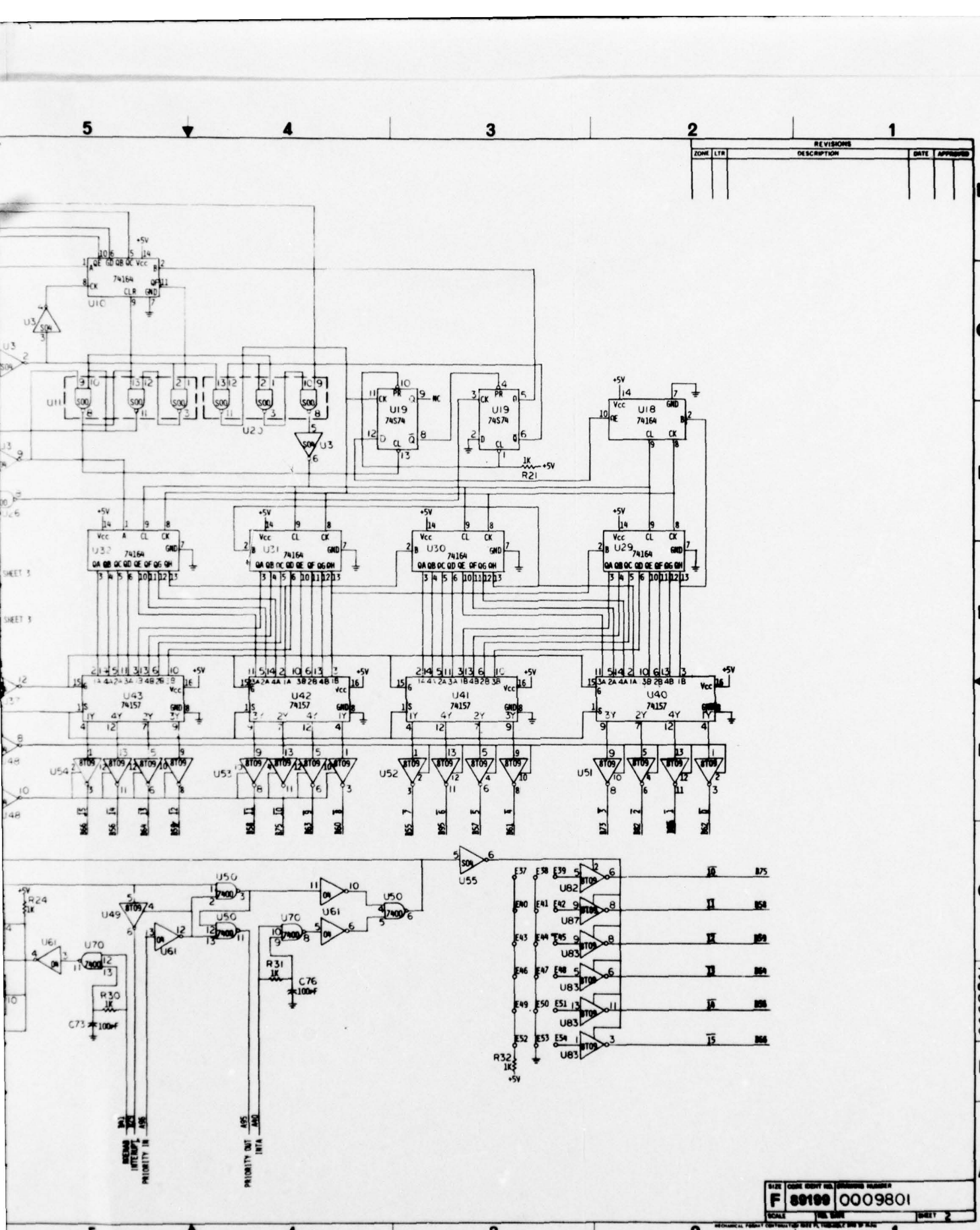
ZONE | LTR | DESCRIPTION | DATE | APPROVED
R6 1K
S OUT A J4
2N3646
2N3906
Q1
Q2
R4 15
R5 240
+5V
R7 1K
S OUT B J5
Q3
Q4
R9 15
R8 240
U60
7430
DEVICE 1 SHEET 2
CLOCK SHEET 2
CLOCK SHEET 3 A71
U12
76B10
U4
74150
STR
U6
74S112
U5
74161
R17 1K
R16 1K
R20 1K
U3
U14
74S112
U13
161
U24
74166
U15
U7
U35
DEVICE 1 SHEET 2
EFR SHEET 2
CDR SHEET 2
IORST + IA SHEET 2
U34
U36
U25
74174
U16
U8
R18 1K
U21
7474
IDR/EIR
BUSY
R22 1K
C89
C88
C87
R38
R37
R35
BSD A54
START A52
BOA A50
BOA SHEET 3
BUSY A82
U49
8T09
B75 B63 B60 B55 B95 B57 B61 B73 B82 B65 B62
UNLESS OTHERWISE SPECIFIED
COMPONENT VALUES ARE:
RESISTORS IN OHMS,
CAPACITORS IN μF
INDUCTORS IN MH
APPLICABLE STANDARDS
APPROVED
APPROVED
CHECKED
DRAWN GG
CODE 4410 1-10-77 DATE
PROG NO. Z 292
CODE/ENTRY CODE 7350
NAVAL ELECTRONICS LABORATORY CENTER
CIRCUIT CARD ASSY,
NOVA TO NTDS INTERFACE SERIAL -
SHEMATIC DIAGRAM
SIZE F
CODE IDENT NO. 89199
DRAWING NO. 0009801
SCALE
SHEET OF

1086000

2


SERIAL IN A
SERIAL IN B
SHEET 1 CLOCK
SHEET 1 DEVICE 1
DIA AAA
SHEET 1 EFR
SHEET 1 ODR
SHEET 1 IORST + IA
SHEET 1 DEVICE 1
CLOCK SHEET 3
DIA SHEET 3
IORST
DIB
DONE
INTERRUPT
PRIORITY IN
PRIORITY OUT
INTA


REVISIONS
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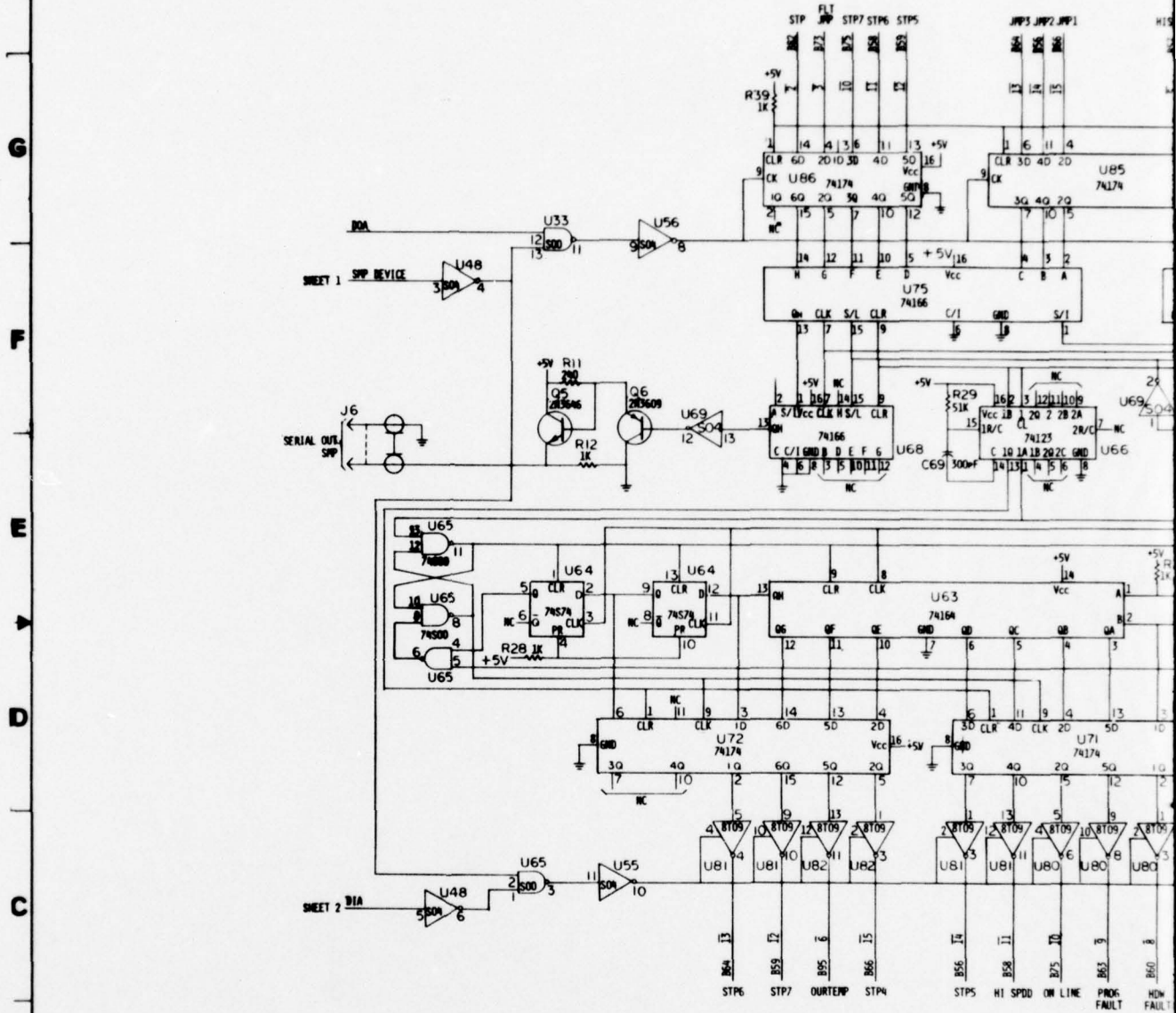
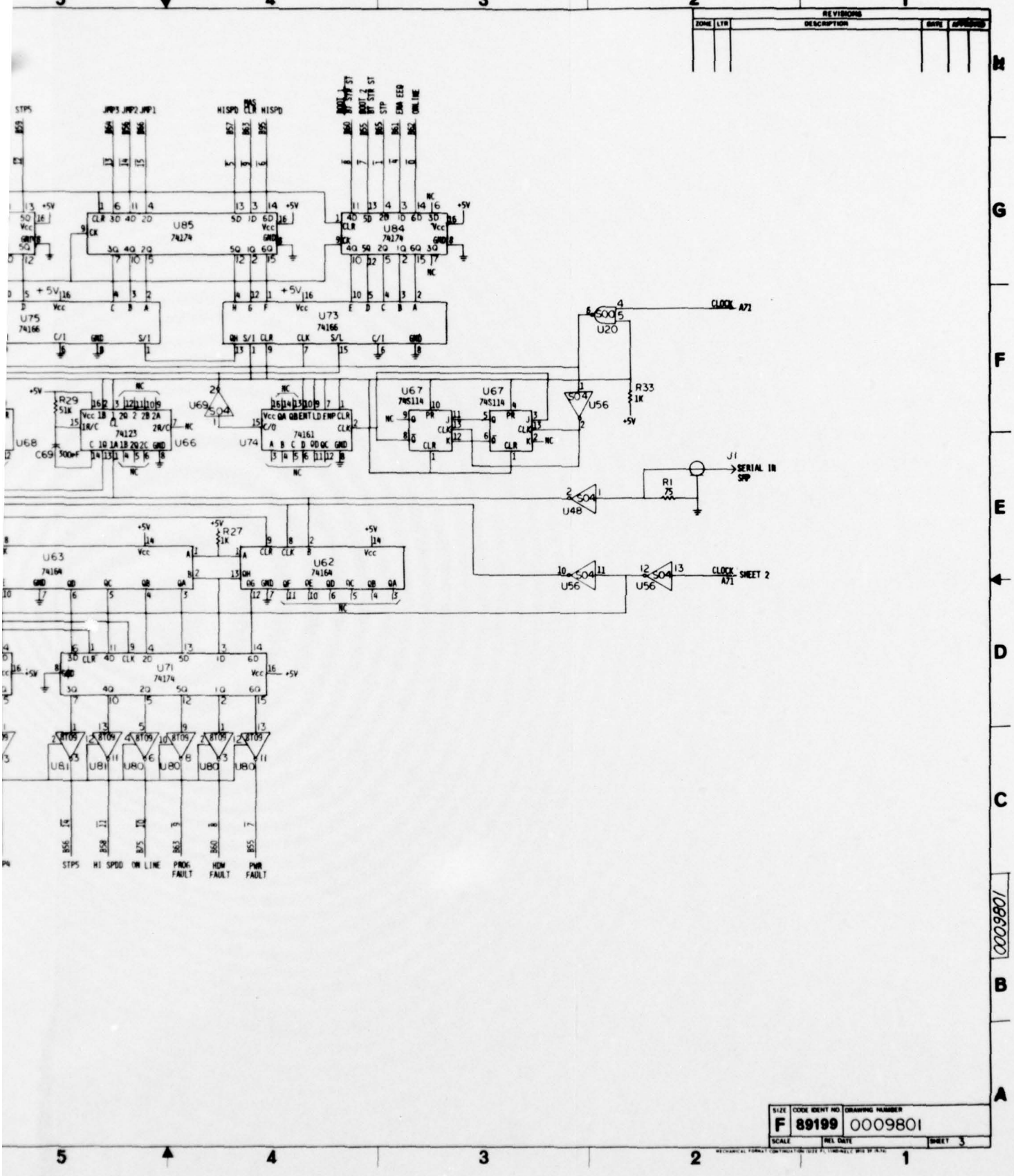
LTR
DESCRIPTION
DATE
APPROVED
U10
U11
U20
U19
74S74
U18
74164
U33
U32
U31
U30
U29
U43
U42
U41
U40
74157
U54
U53
U52
U51
U55
U50
U49
U61
U70
U82
U87
U83
R21
1K
R24
R31
R30
C76
100pF
C73
R32
+5V
SHEET 3
SHEET 3
PRIORITY IN
PRIORITY OUT
INTA
SIZE
F
CODE IDENT NO.
89199
DRAWING NUMBER
0009801
SCALE
SHEET 2
0009801


STP
FLT JMP
STP7 STP6 STP5
JMP3 JMP2 JMP1
R39 1K
U86 74174
U85 74174
U75 74166
U33
U56
U48
SHEET 1 SMP DEVICE
Q5 2N3646
Q6 2N3609
R11 200
R12 1K
J6
SERIAL OUT SMP
U69
U68 74166
U66 74123
R29 51K
C69 300pf
U65 74S00
U64 74S74
R28 1K
U63 74164
U72 74174
U71 74174
U81 8T09
U82 8T09
U80 8T09
U55
SHEET 2 DIA
STP6
STP7
OUTERMP
STP4
STP5
HI SPDD
ON LINE
PROG FAULT
HDW FAULT


REVISIONS
ZONE
LTR
DESCRIPTION
DATE
APPROVED
STP5
HISPD
U85
74174
U84
74174
U75
74166
U73
74166
U20
CLOCK A71
R29
51K
U68
C69
500pF
U66
74123
U69
U74
74161
U67
74S114
U56
R33
1K
+5V
J1
SERIAL IN
SHP
R1
75
U48
R27
1K
U63
7416A
U62
7416A
CLOCK
SHEET 2
U71
74174
U81
U80
8T09
STP5
HI SPDD
ON LINE
PROG. FAULT
HDW FAULT
PWR FAULT
SIZE
CODE IDENT NO
DRAWING NUMBER
F
89199
0009801
SCALE
REL DATE
SHEET 3

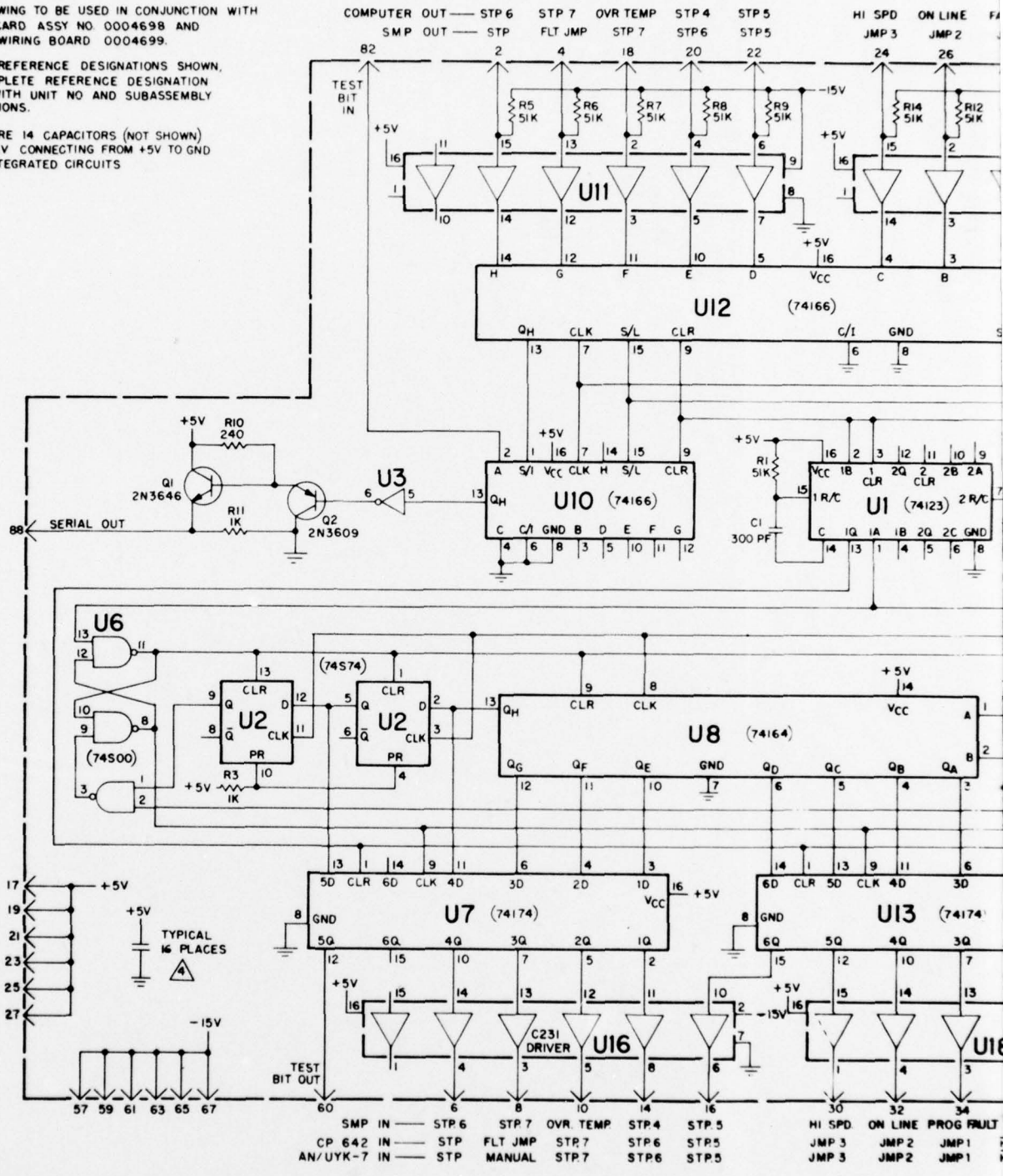
APPENDIX E: SYSTEM MAINTENANCE PANEL (SMP) CONVERTER

The SMP converter is a parallel-to-serial and serial-to-parallel converter. It is used in SCSS to allow a serial interface of the SCSS control console with the tactical computers in the system. All functions which are normally performed at the SMP panel can be performed at the SCSS control console. Drawing 0004700 is a schematic diagram of the SMP converter. Thirty-two bits of data are exchanged between the SMP converter and the control computer. Data from the SMP card is latched into the control computer and is treated as a priority interrupt. Data from the control computer is latched into the SMP card where the standard parallel signals are generated. Note that the SMP card is used for either the AN/UYK-7 or the CP-642 computer.

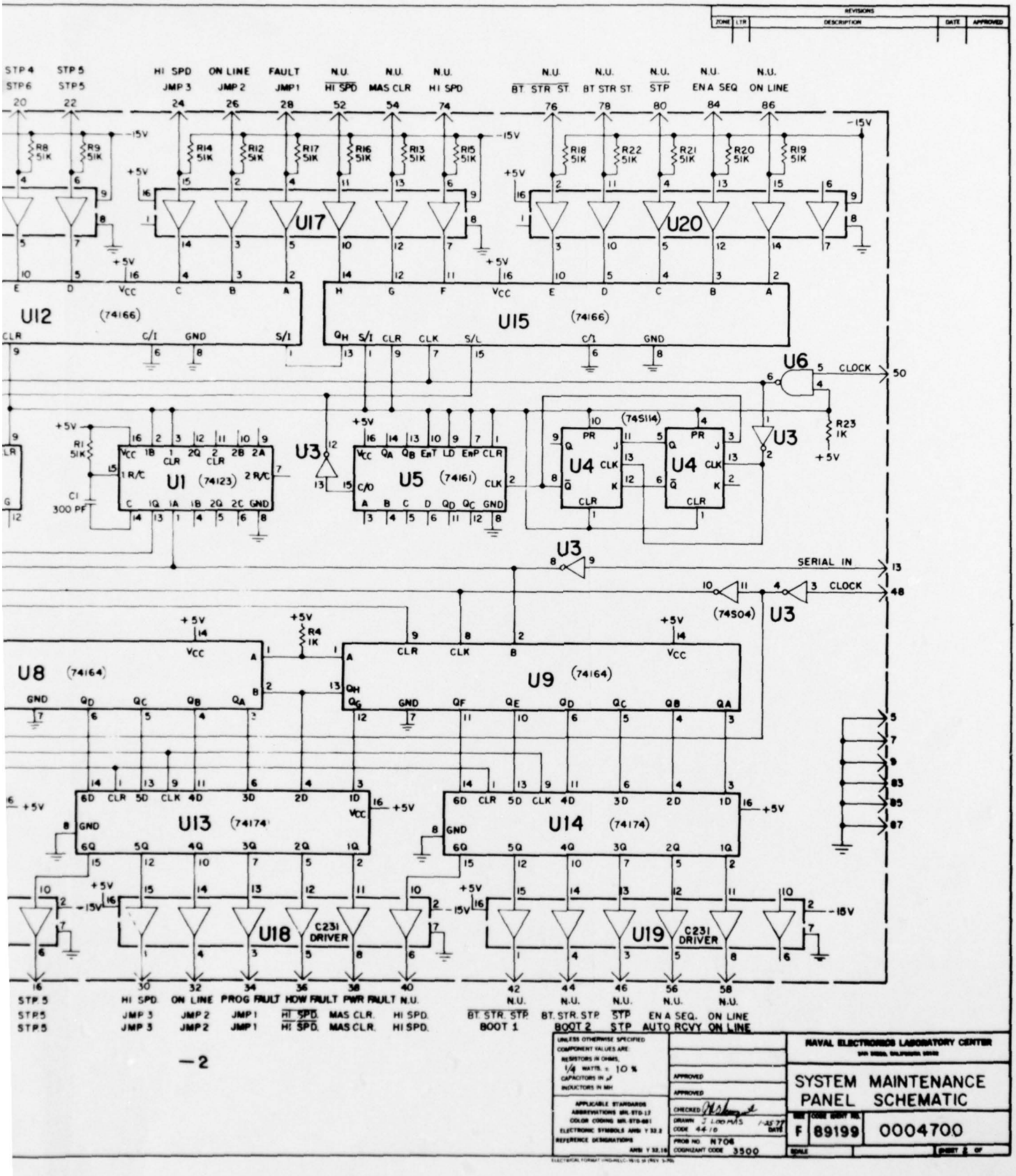
NOTES:

1. INTERPRET DRAWING PER MIL-STD-100.
2. THIS DRAWING TO BE USED IN CONJUNCTION WITH CIRCUIT CARD ASSY NO. 0004698 AND PRINTED WIRING BOARD 0004699.
3. PARTIAL REFERENCE DESIGNATIONS SHOWN, FOR COMPLETE REFERENCE DESIGNATION PREFIX WITH UNIT NO AND SUBASSEMBLY DESIGNATIONS.

(4) THERE ARE 14 CAPACITORS (NOT SHOWN) .022 μf, 16V CONNECTING FROM +5V TO GND NEAR INTEGRATED CIRCUITS

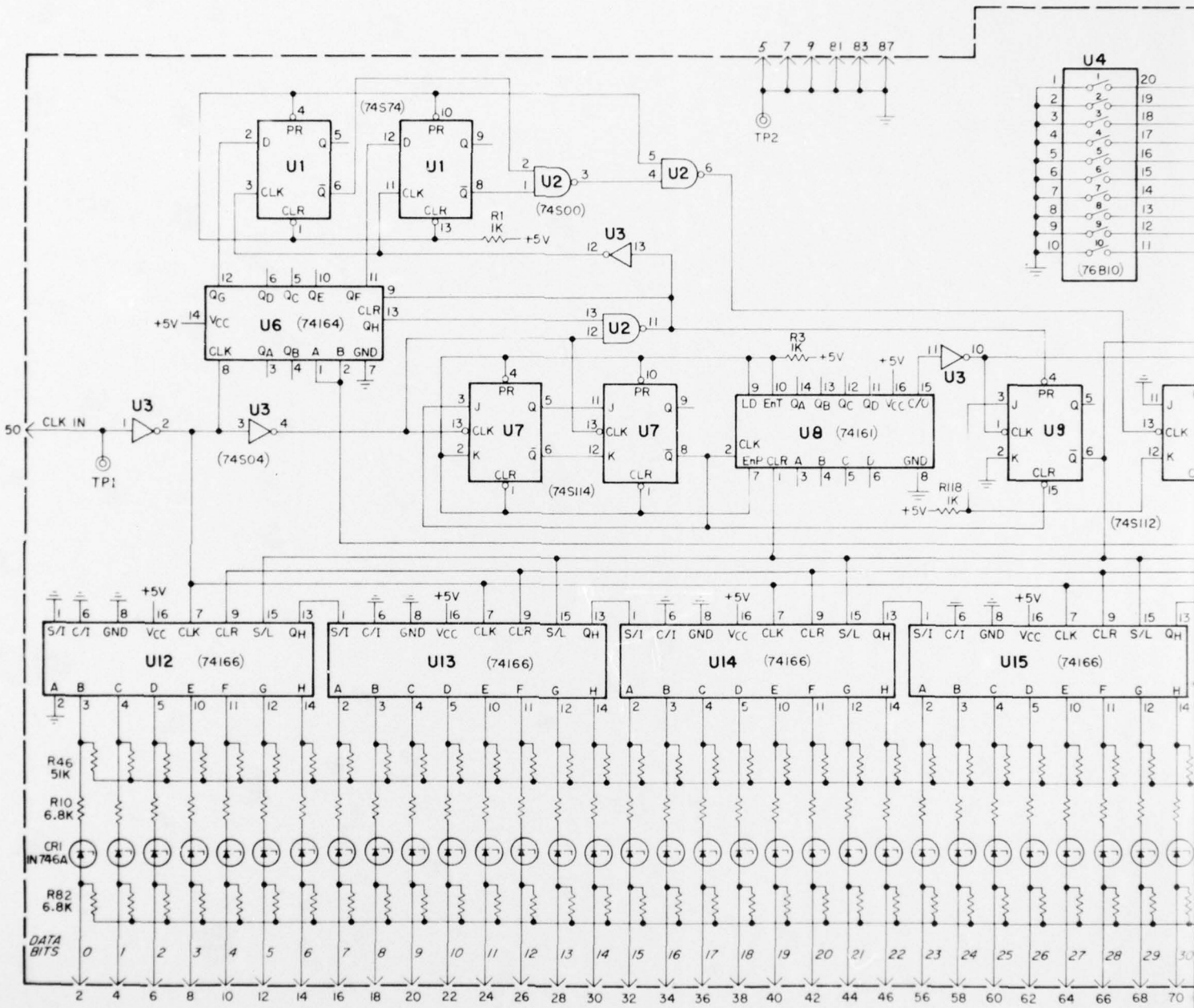


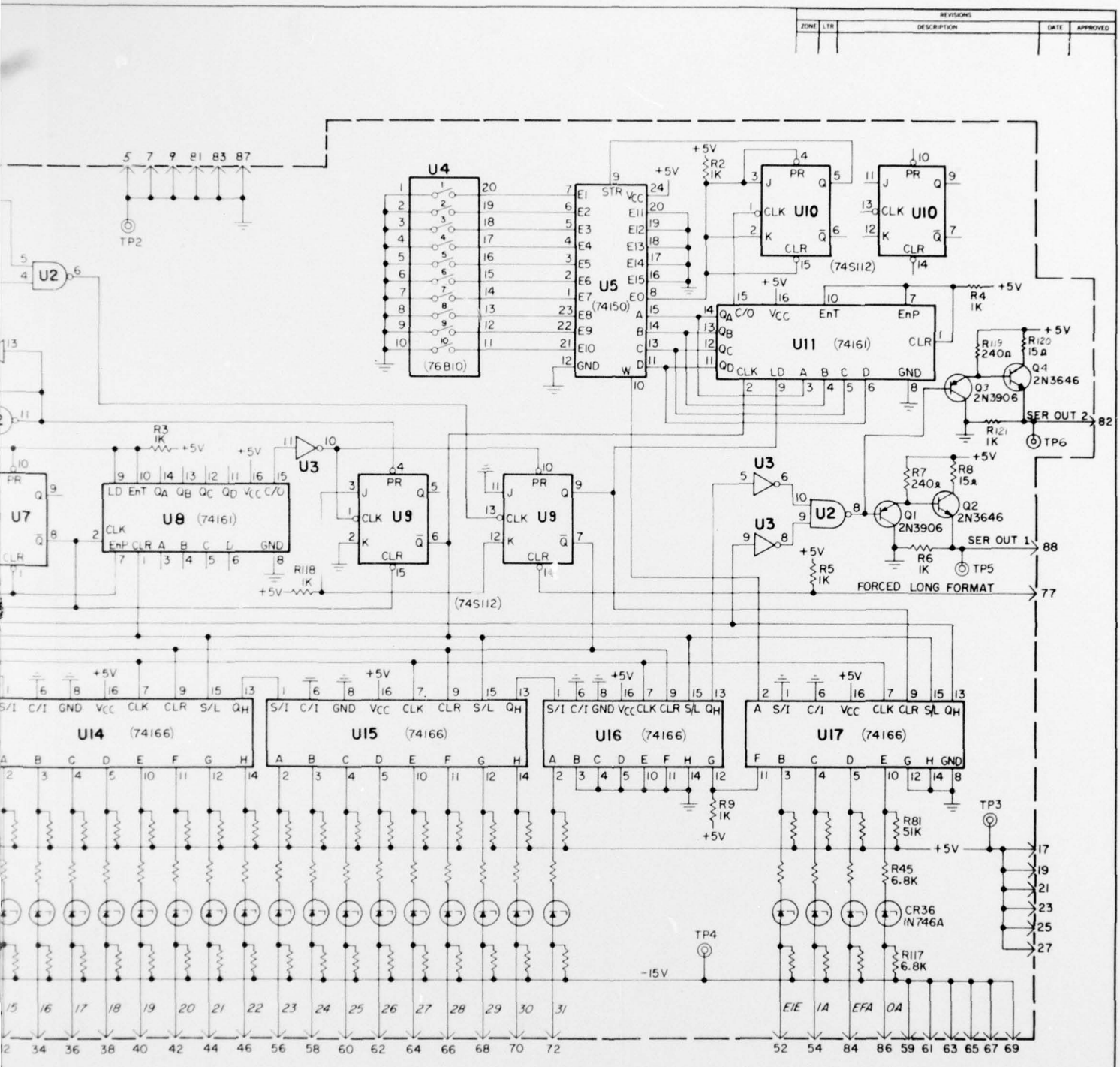
PRECEDING PAGE BLANK-NOT FILMED


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
STP 4 STP 5 STP 6 STP 5
HI SPD JMP 3
ON LINE JMP 2
FAULT JMP 1
N.U. HI SPD
N.U. MAS CLR
N.U. HI SPD
N.U. BT STR ST
N.U. BT STR ST
N.U. STP
N.U. ENA SEQ
N.U. ON LINE
-15V
+5V
R8 5IK
R9 5IK
R14 5IK
R12 5IK
R17 5IK
R16 5IK
R13 5IK
R15 5IK
R18 5IK
R22 5IK
R21 5IK
R20 5IK
R19 5IK
U17
U20
U12 (74166)
U15 (74166)
CLR C/I GND S/I
QH S/I CLR CLK S/L C/I GND
U6
CLOCK 50
R23 1K
U3
(74S114)
U4 CLK
U4 CLK
PR
CLR
R1 5IK
C1 300 PF
U1 (74123)
U5 (74161)
SERIAL IN 13
CLOCK 48
(74S04)
U8 (74164)
U9 (74164)
R4 1K
U13 (74174)
U14 (74174)
U18 C231 DRIVER
U19 C231 DRIVER
-15V
STP 5 STP 5 STP 5
HI SPD JMP 3 JMP 3
ON LINE JMP 2 JMP 2
PROG FAULT JMP 1 JMP 1
HDW FAULT HI SPD HI SPD
PWR FAULT MAS CLR MAS CLR
N.U. HI SPD HI SPD
N.U. BT STR STP BOOT 1
N.U. BT STR STP BOOT 2
N.U. STP STP
N.U. ENA SEQ AUTO RCVY
N.U. ON LINE ON LINE
-2
UNLESS OTHERWISE SPECIFIED
COMPONENT VALUES ARE:
RESISTORS IN OHMS
1/4 WATTS ± 10 %
CAPACITORS IN μF
INDUCTORS IN MH
APPLICABLE STANDARDS
ABBREVIATIONS MIL STD-12
COLOR CODING MIL STD-681
ELECTRONIC SYMBOLS ANSI Y 32.2
REFERENCE DESIGNATIONS ANSI Y 32.16
APPROVED
APPROVED
CHECKED
DRAWN J. LOOMIS
CODE 44 10
PROG NO. N706
COGNIZANT CODE 3500
NAVAL ELECTRONICS LABORATORY CENTER
SYSTEM MAINTENANCE PANEL SCHEMATIC
SIZE F
CODE IDENT NO. 89199
0004700
SCALE
SHEET 2 OF

APPENDIX F: REDUNDANT-PATH DUAL I/O CONVERTERS

Two converter devices are required for each serial channel; a parallel-to-serial transmitter and a serial-to-parallel receiver. The parallel-to-serial converter diagram shown in drawing 0004682 shows the dual serial drivers which feed two coaxial cables. The timing functions of this device are the same as those of the parallel-to-serial converter described in Appendix A. The serial-to-parallel converter diagram shown in drawing 0004685 shows the dual serial input ports. Integrated circuit one-shot devices are fed by these ports. When a signal arrives at one of the ports, the one-shot devices lock out the alternate port and allow only the incoming signal to pass. If the signal ceases, both ports are again opened for a new signal.





-3

UNLESS OTHERWISE SPECIFIED
COMPONENT VALUES ARE:
RESISTORS IN OHMS,
WATTS, ±
CAPACITORS IN μF
INDUCTORS IN MH

APPLICABLE STANDARDS
ABBREVIATIONS MIL STD 12
COLOR CODING MIL STD 681
ELECTRONIC SYMBOLS ANSI Y 32.2
REFERENCE DESIGNATIONS
ANSI Y 32.16

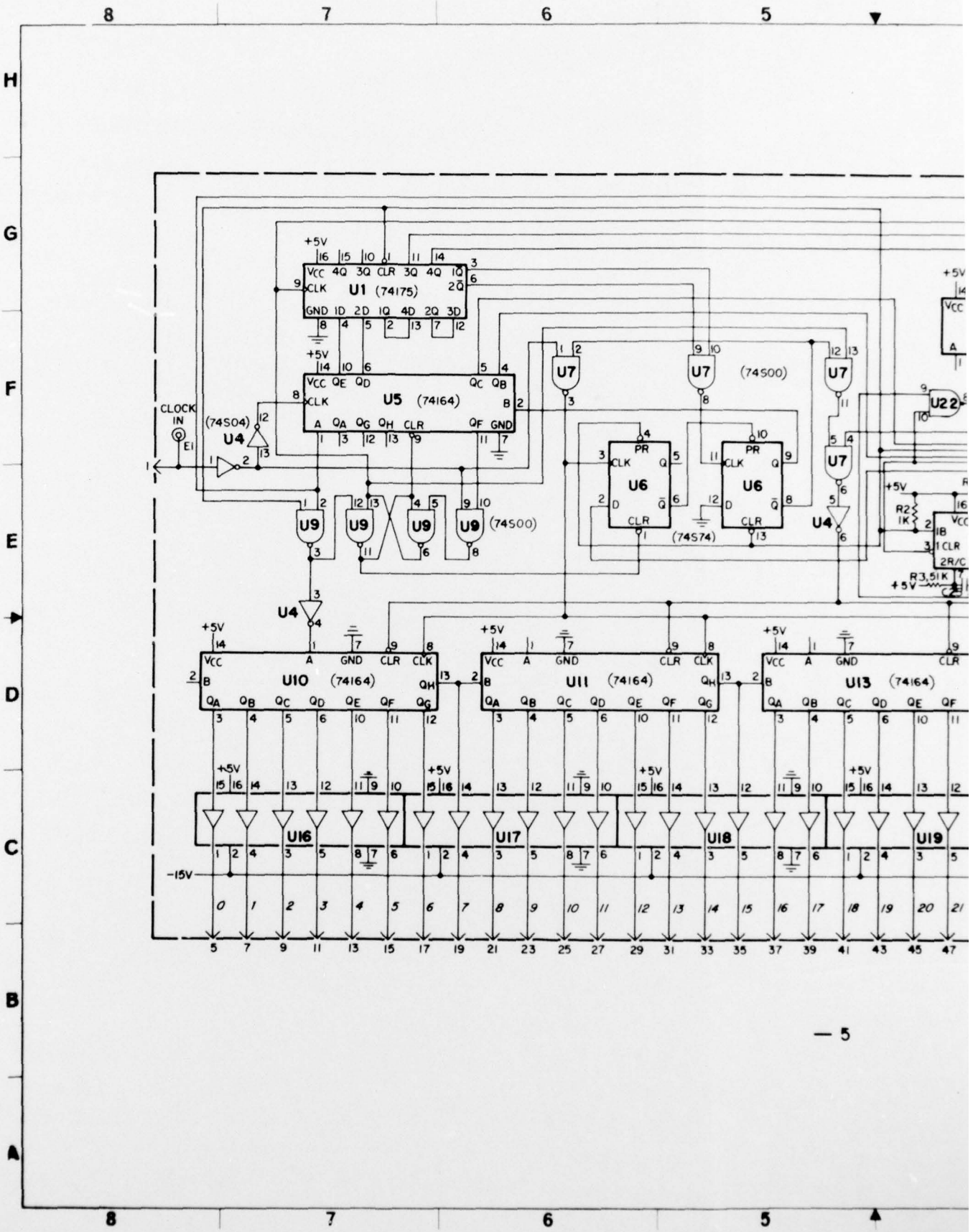
APPROVED
APPROVED
CHECKED
DRAWN
CODE
DATE
PROB NO. N706
COGNIZANT CODE 3500

NAVAL ELECTRONICS LABORATORY CENTER
SAN DIEGO, CALIFORNIA 92152

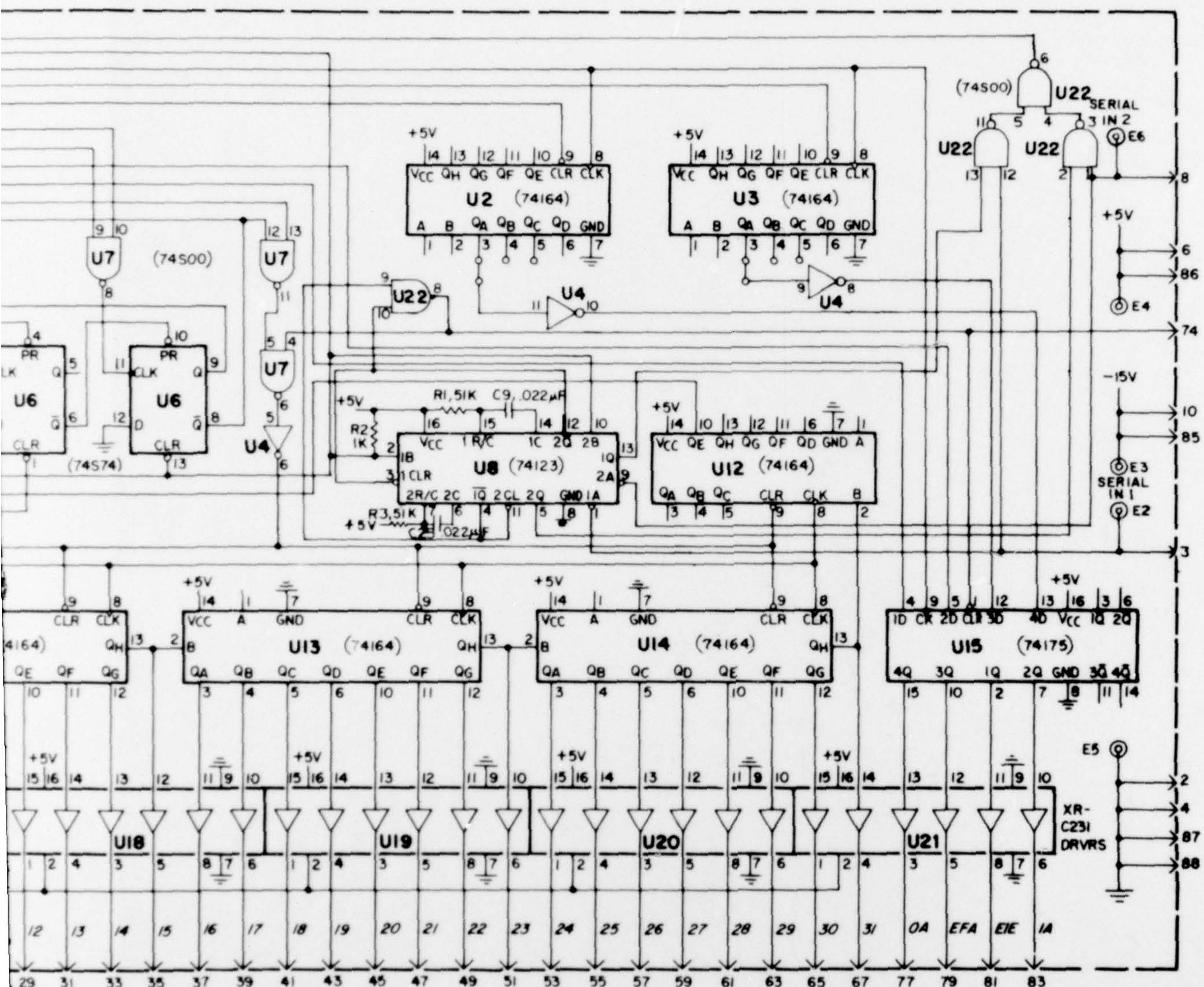
PARALLEL TO SERIAL
SCHEMATIC DIAGRAM

SIZE F | CODE IDENT NO. 89199 | 0004682 | 3
SCALE — | SHEET 7 OF

2


8
7
6
5
H
G
F
E
D
C
B
A
+5V
U1 (74175)
U5 (74164)
CLOCK IN
(74S04)
U4
U7
(74S00)
U6
(74S74)
U9
(74S00)
U4
U10 (74164)
U11 (74164)
U13 (74164)
U16
U17
U18
U19
-15V
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21
5 7 9 11 13 15 17 19 21 23 25 27 29 31 33 35 37 39 41 43 45 47

— 5



NAVAL ELECTRONICS LABORATORY CENTER

SERIAL TO PARALLEL CONVERTER SCHEMATIC

SIZE	CODE IDENT NO.	DRAWING NUMBER
F	89199	0004685

APPENDIX G: BIDIRECTIONAL ANALOG SWITCH TEST RESULTS

INTRODUCTION

The results of several tests on analog switching matrix are presented here.

PROBLEM

A signal switching matrix that can route analog signals in a bidirectional fashion has been constructed and tested (see drawing 0010065). The basic switch point is a Signetics 5301 integrated circuit containing a 2 by 8 switch array. This 2 by 8 format is expanded by connecting specific inputs and outputs to build an array having 16 inputs and 16 outputs.

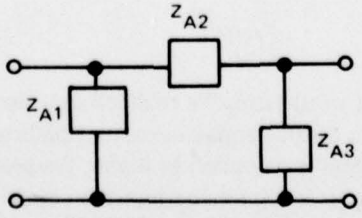
An output or input in the "off" state on the 5301 circuit can be modeled as a capacitance. As a result, the frequency response of an "on" channel is a function of the number of paralleled inputs and outputs. The actual frequency response is also affected by stray capacitance, and therefore this parameter, and others, were measured.

RESULTS

	MIN	AVG	MAX	UNITS	# OF PATHS TESTED
Frequency Response	8.5	9.9	13	MHz	31
Max. Input Swing	3.9	4.65	4.8	Volts	16
Off Isolation @ 3 dB Freq.	33	36.3	43	dB	29
Loss through Switch @ 3 dB Freq.	2	3.7	4	dB	30
Cross Talk	33	36.3	43	dB	29
Distortion Products		-40		dB	@ 5^V Swing
1 KHz Measurements		Typical			
Off Isolation @ 1 KHz		90		dB	
Loss through Switch @ 1 KHz		0.75		dB	

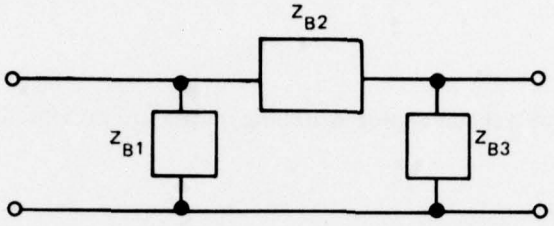
DISCUSSION

The switch can be modeled in its two states as shown below.



"ON" STATE

and

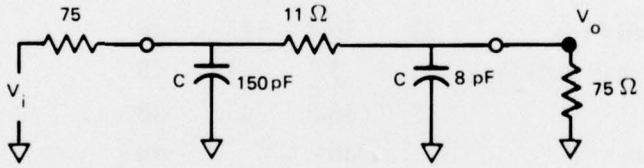


"OFF" STATE

At these frequencies Z_{A1}, Z_{A3}, Z_{B1}, Z_{B3} are capacitive elements defined by the circuit geometry. The data sheet lists the following values.

	Min.	Typical	Max.	Units
Z_{A1}, Z_{B1}	–	150	–	Input Capacitance (pF)
Z_{A3}, Z_{B3}	–	8	–	Output Capacitance (pF)
Z_{A2}	7	11	15	ON Resistance (Ω)
Z_{B2}		No Specification		OFF Resistance (Ω)

In a 75 ohm system the complete circuit model in the on state is:



In this circuit, the output 3 dB frequency can be found from the equation

$$V_o = \frac{(V_1)(R_3)}{(R_1 + R_2 + R_3 - \omega^2 R_1 R_2 R_3 C_1 C_2) + jw(R_1 C_1 (R_2 + R_3) + R_3 C_2 (R_1 + R_2))}$$

With the above parameters, this is:

$$f_{3dB} = 25 \text{ MHz}$$

This potential bandwidth would only be realized in a simple on-off switching application since only one input and one output capacitance are loading the signal path. An additional factor is that the off isolation is degraded at higher frequencies.

For the basic 16 by 16 array, each analog input is connected to two 5301 inputs, and each analog output is connected to outputs from eight 5301 circuits. This raises the switch model parameters to:

	Typ.	Units
Z_{A1},Z_{B1}	300	Input Capacitance (pF)
Z_{A3},Z_{B3}	64	Output Capacitance (pF)

The actual values of input and output capacitance measured with a Time-Domain Reflectometer are:

Z_{A1}, Z_{B1}	436 pF
Z_{A3}, Z_{B3}	230 pF

These measured values show an accumulated wiring capacitance of about 300 picofarads.

CIRCUIT DESCRIPTION

When power is first applied to the 5301 switch array, the switches assume random on and off states. For this reason, the prototype matrix includes an automatic mode that is used to set all the switches open or closed.

In the automatic mode, 16 address bits are generated by four 4-bit synchronous counters. The least significant 4 bits are routed to a shift register where they are parallel loaded with a fifth bit that comes from a simple toggle switch. This fifth bit is the command bit to open or close one of 16 switches in the 5301 circuit.

The five bits are clocked out of the shift register and sent to every 5301 circuit on every card. Only the 5301 circuit that has been enabled by the remaining 12 address bits will respond to the 5-bit data word.

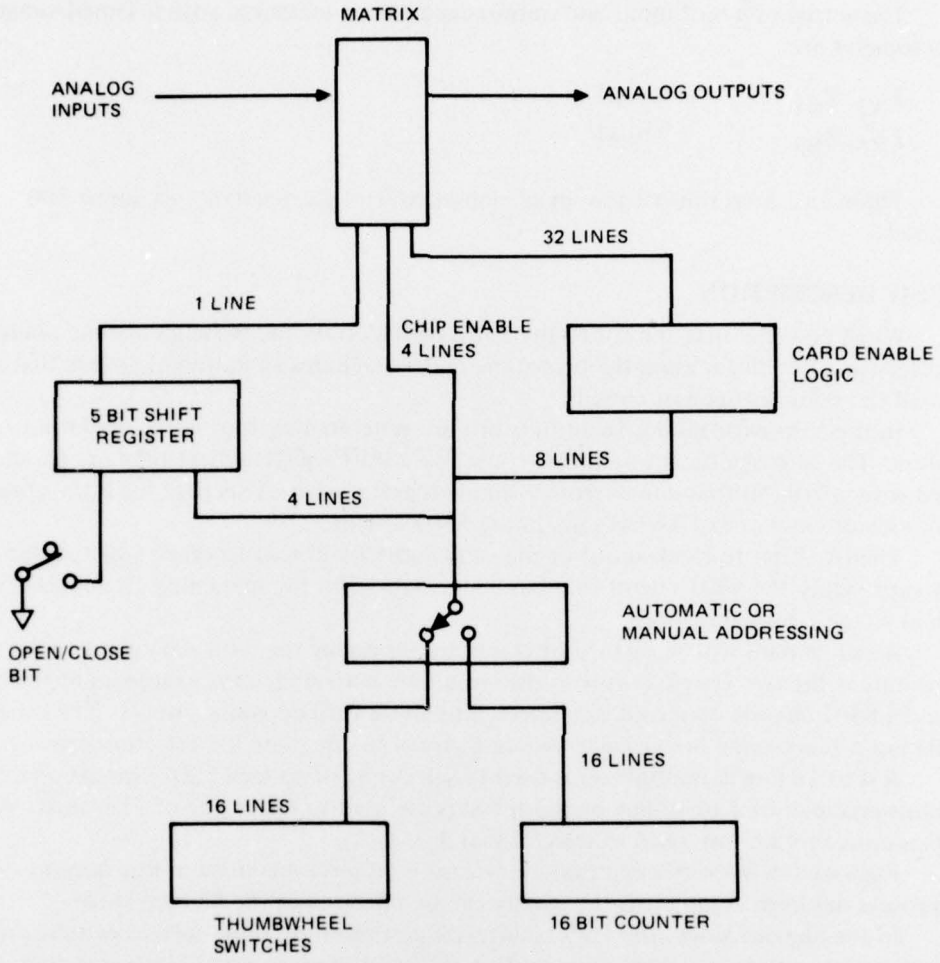
A switch path will be opened or closed by supplying the 5-bit data word to the 5301 circuit only if the two enable inputs to the circuit are activated. One enable input from each of the 16-5301 circuits on a card is connected to an on-card decoding circuit. The other enable input is activated just prior to the data arrival to complete the selection process.

A 4 to 16 line demultiplexer is used to select one of sixteen 5301 circuits on a card. An additional pair of 4 to 16 line demultiplexers are used to select one of 256 cards. A total of 16 address bits are thus used to select a switch.

Each switch in every circuit on every card is addressed and set in this fashion. After this process has been completed, the matrix can be operated in the Manual Mode.

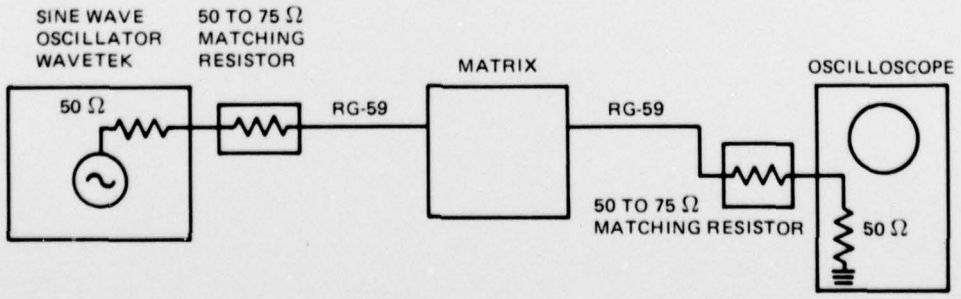
In the Manual Mode, the 16-bit address is generated by thumbwheel switches, and the execution of a command is done on a contact closure of a momentary contact switch.

The best way to operate the 5301 circuit for analog signals that swing plus and minus is to power the circuit from split power supplies. Since the switching in the circuit is done by FET's that have been biased on or off, the off isolation is not retained if the analog voltage is too close to the circuit supply voltages. Operating from split supplies assures proper switch operation with the largest permissible bipolar range.



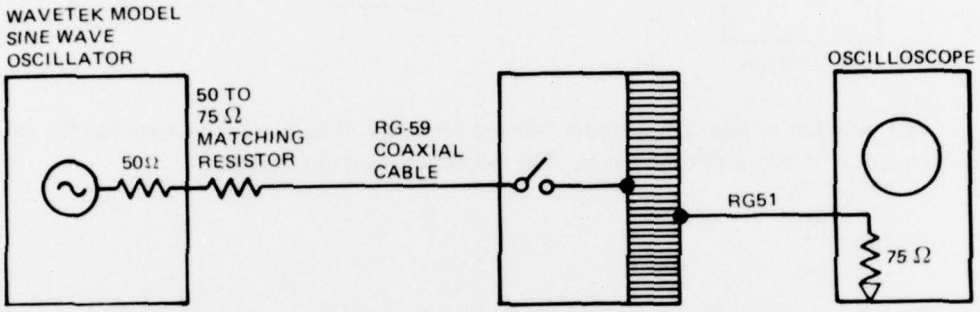
TEST CONDITIONS

FREQUENCY RESPONSE



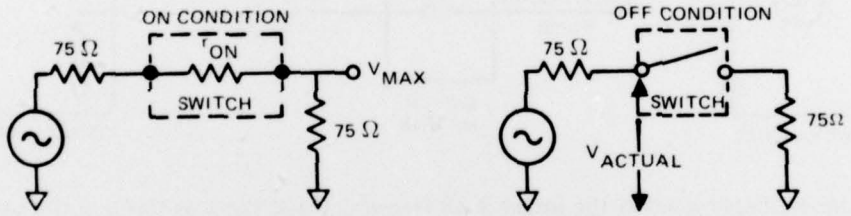
The OUTPUT voltage is set to some level V_1 at 1 kilohertz. The frequency is increased until the output voltage drops to 0.707 V_1. The frequency is recorded as the half-power frequency, even though the actual power dissipated in the load is slightly less than half the power delivered by the source. About 0.75 dB is lost in the finite switch resistance.

MAXIMUM INPUT SWING



A signal at 1 KHz is applied to one input. All switches are in the off state. All outputs are monitored, and the input signal is increased until 1 mV of feed through is observed. This level is fixed, the switch is closed, and the voltage appearing across the 75-ohm load is recorded.

Since the source is unterminated when the switch is opened, the actual voltage swing at the input is greater by a factor of 2.15.



$$V_{actual} = V_{max} \frac{75 + 75 + r_{on}}{75} = \frac{150 + r_{on}}{75}$$

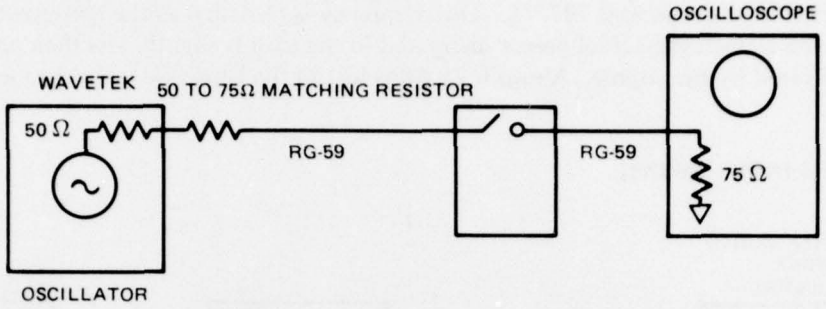
with

r_{on} = 11Ω typical

V_{actual} = 2.15 V_{max}

This means that if the source could be terminated when the switch is opened, the maximum input swing figures measured could be easily doubled if the 5301 circuit dissipation is not exceeded.

OFF ISOLATION

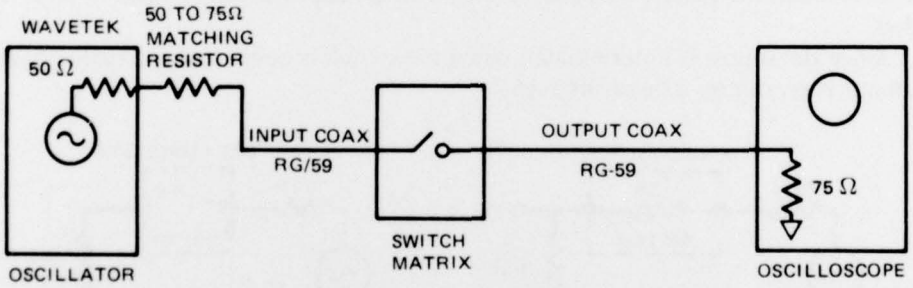


All switches in the circuit under test are set open. The oscillator is set for the upper 3 dB frequency of the path under test. The off isolation is defined as

$$20 \log \frac{V_{off}}{V_{on}}$$

See also the discussion on crosstalk.

LOSS THROUGH SWITCH



The oscillator is set at the upper 3 dB frequency and the loss through the switch defined as

$$\text{loss} = -20 \log \frac{V_1}{V_2}$$

where V_1 = voltage appearing across 75-ohm load with switch in path, and V_2 = voltage appearing across load with the switch removed from the path.

CROSSTALK

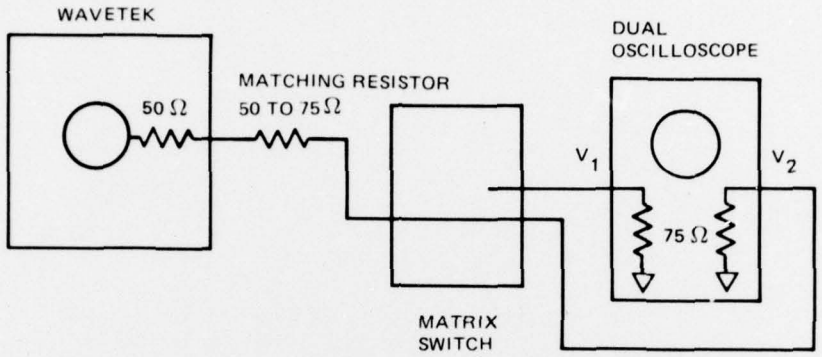
Crosstalk is the level of signal coupling to an adjacent channel. The worst case coupling occurs when the adjacent channel is in the off state since the voltage swing at the input is doubled. For this reason, crosstalk for this switch is defined as:

$$-20 \log \frac{V_1}{V_2}$$

where

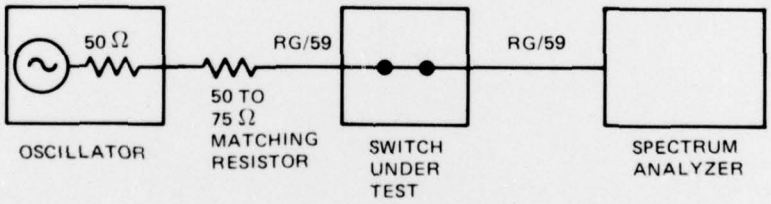
V_1 = adjacent channel voltage across 75-ohm load with switch open

V_2 = voltage across 75-ohm load with switch closed.



This measurement is done at the upper 3 dB of the switch.

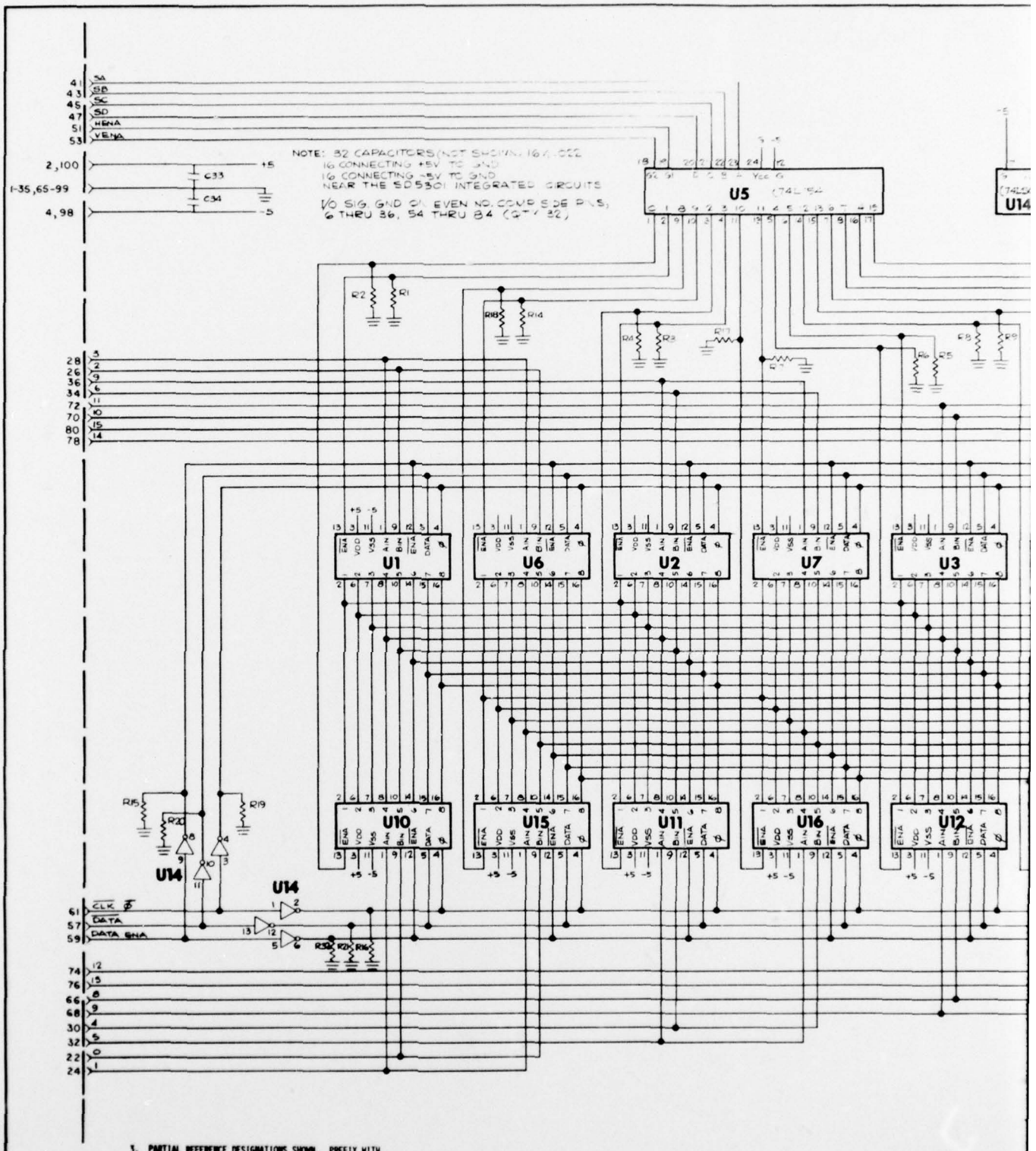
DISTORTION PRODUCTS



The oscillator is set to produce a 5V peak-to-peak sine wave output at 2 megahertz. A photograph of the spectrum analyzer is taken.

ONE-KILOHERTZ MEASUREMENTS

Two measurements identical to those described earlier are made of the off isolation and loss through the switch, at a frequency of 1 kilohertz. These measurements give an indication of the resistive leakage through the switch.



3. PARTIAL REFERENCE DESIGNATIONS SHOWN. PREFIX WITH UNIT AND SUBASSY DESIGNATION.

2. REFERENCE DWG:
CIRCUIT CARD ASSY 89199-0010063
PRINTED WIRING BOARD 89199-0010064

1. INTERPRET DWG. PER MIL-STD-100

NOTES:

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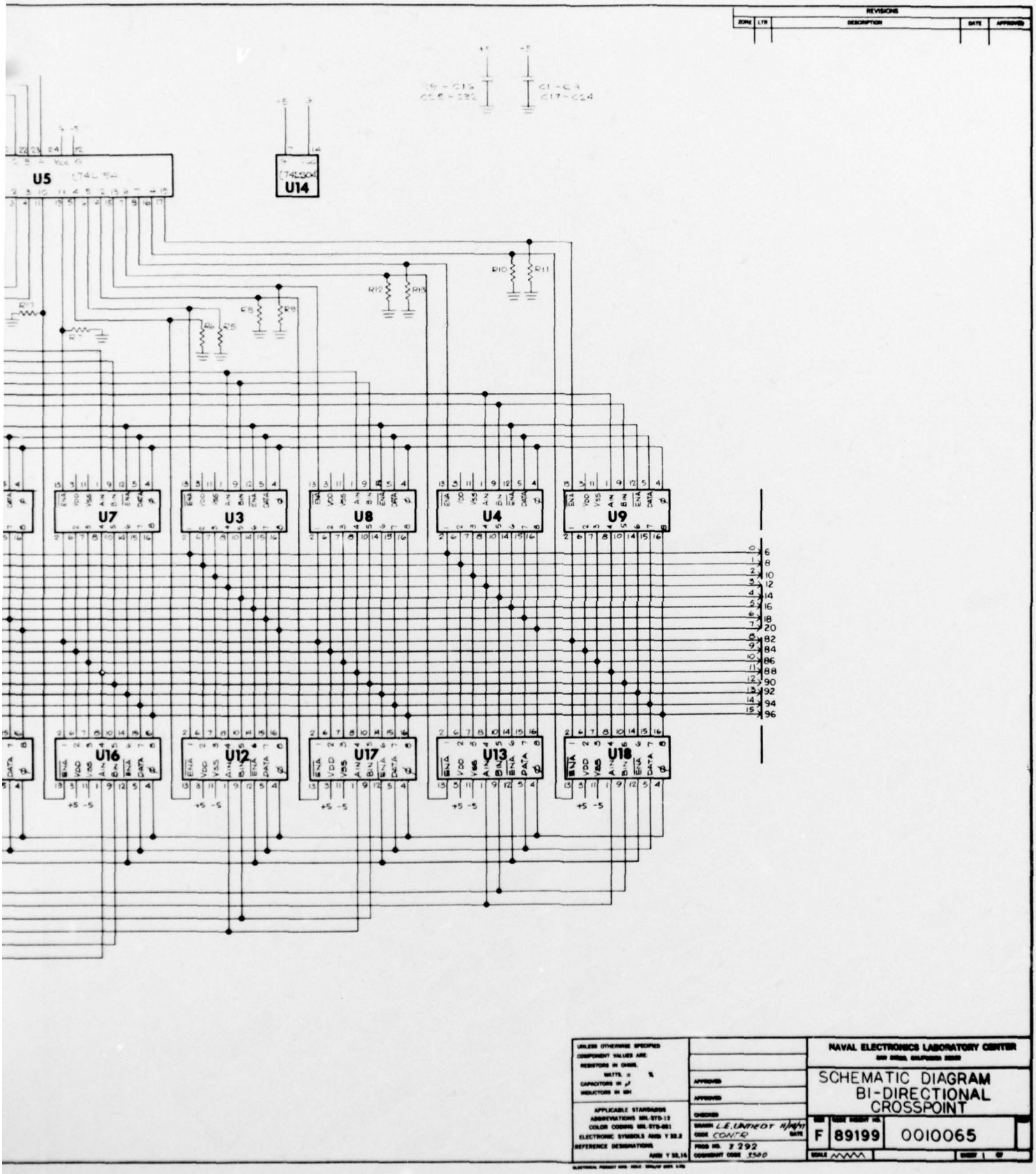
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