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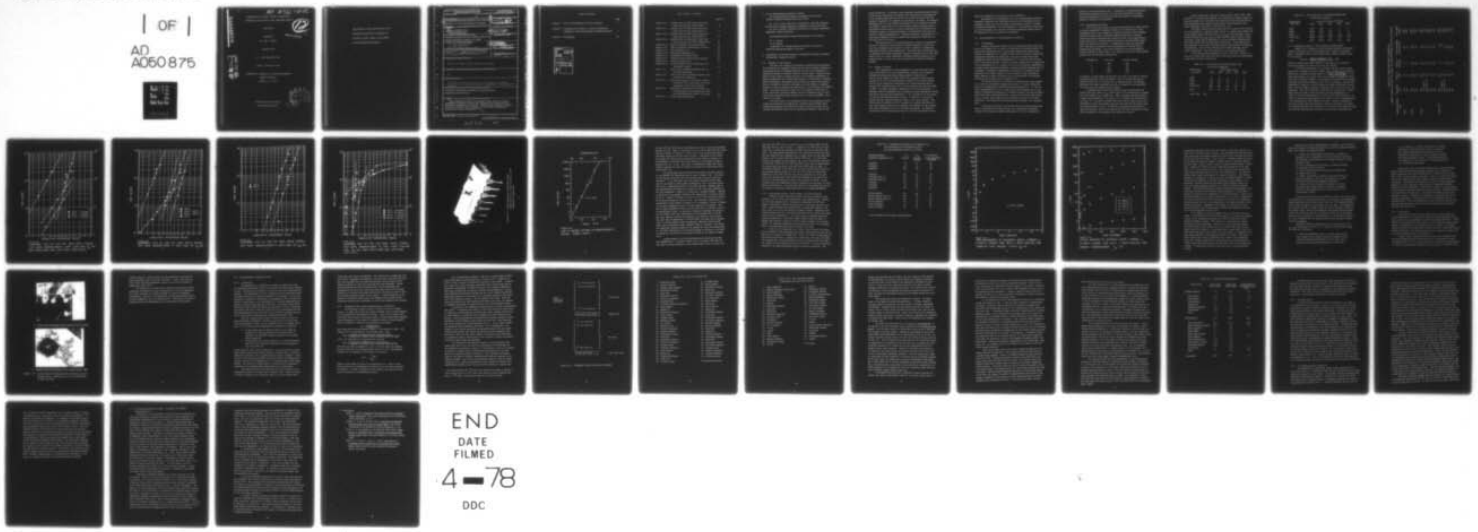

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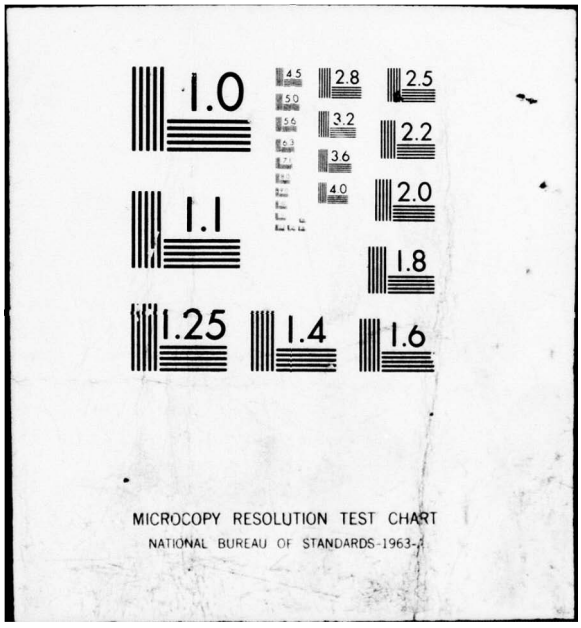
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INVESTIGATION OF FACTORS INVOLVED IN RELIABILITY ASSURANCE OF PLASTIC-ENCAPSULATED INTEGRATED CIRCUITS

(12)

FINAL REPORT

PREPARED BY

DR. JOHN L. PRINCE

FEBRUARY 1978

U. S. ARMY RESEARCH OFFICE

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CLEMSON UNIVERSITY

CLEMSON, S. C. 29631

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Upper temperature limits to accelerated stress testing of plastic-encapsulated integrated circuits were determined and evidence of chip-encapsulant interaction was obtained. Possible yield-reliability correlations were considered and alternatives to MIL-M-38510 screening were discussed for plastic-encapsulated IC's.

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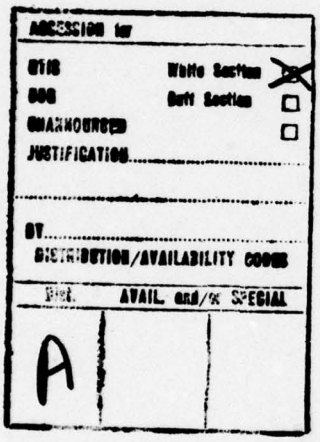

List of Figures and Tables

1. List of Participating Scientific Personnel

The following faculty members participated in the project covered by Research Agreement DAAG29-77-G-0039:

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The following graduate students participated in the project:

Mr. D. Bullard

Mr. R. Hartman

In addition, Mr. Bullard received the Master of Science in Electrical Engineering degree in May 1977.

2. Investigation of Factors Involved in Reliability Assurance of Plastic-Encapsulated Integrated Circuits

2.1. Statement of the Problem

The cost, both tangible and intangible, associated with enhancing the reliability of integrated circuits (IC's) used in military equipment to levels beyond those of standard commercial IC's has been recognized as a significant problem by elements in DOD for several years. Steps have been taken in recent years to improve the built-in or inherent reliability of plastic-encapsulated IC's through improvements in IC fabrication techniques. These technological improvements must eventually be coupled with improvements in reliability assurance techniques, and particularly in screening methods, in order to maximize the improvement in IC reliability cost-benefit ratio. Two factors which are likely to be of fundamental importance in future reliability assurance schedules are high temperature ($T_{AMB} > 125^{o}$) burn-in and accelerated stress testing, and an IC yield-reliability correlation if it exists.

The first factor is of importance because high temperature burn-in offers the possibility of screening out incipient early failures under accelerated operating conditions rather than by techniques which are of somewhat questionable value, and are undoubtedly expensive, such as 100%

visual inspection. In addition, high-temperature accelerated stress testing allows for the possibility of evaluating the reliability of purchased lots by lot sampling techniques such as are used by the Bell System for semiconductor components, in reasonable and economical time spans. The question addressed here is at what ambient temperature does the interaction between the "plastic" matrix and the IC chip introduce anomalous failure modes in accelerated stress testing, or at what temperature does this plastic-chip interaction result in anomalous decrease in the potential total life of a burned-in plastic encapsulated IC. Phrased another way, the question is at what (high) temperature does the plastic-chip interaction become the controlling factor in IC "life".

The second factor is of interest because if there is a correlation between IC yield and IC reliability attributes subsequent to final test, then this correlation can be used by IC users to predict IC reliability performance based on manufacturing data. This means that IC yield data may be integrated with other reliability assurance techniques such as high temperature burn-in, or high temperature accelerated stress testing on a lot-sampling basis, to form a new, more cost-effective reliability assurance program.

2.2. Summary of Results

The investigation of high temperature IC chip-encapsulant interaction involving IC's from two manufacturers subjected to an extensive accelerated temperature-voltage stress schedule, showed that an apparent upper temperature limit (150°C) for accelerated stress testing existed for IC's from one manufacturer (manufacturer B) whereas devices from the other manufacturer (manufacturer A) showed anomalous time-to-failure (TTF) characteristics over the entire temperature range from 125°C to 200°C. The epoxy encapsulant differed for the two manufacturers. A phenomenon which is apparently room temperature storage degradation was also observed for devices from manufacturer A. The implications of this effect for Life-of-Type procurements are obvious. In addition, a unique new failure mode was observed during the course of the stress testing. This failure mode is insidious in that it appears as a pattern sensitivity of logic gate leakage current and is strongly time dependent at room temperature, after stressing of the IC at elevated temperature. The failures associated with this failure mode would not have been identified if auto-

mated test equipment has been used in the investigation.

Examination of the proposition that the IC manufacturing yield and subsequent reliability are correlated resulted in the conclusion that the correlation exists but that the degree of correlation is still not clear. An experiment designed to test the hypothesis of the existence of the correlation was designed, and a possible reliability assurance program based on the existence of such a correlation was designed.

2.3. High Temperature IC Chip-Encapsulant Interaction

2.3.1. Introduction

Feasible temperature limits for both accelerated stress testing and burn-in are normally set by assembly or fabrication technology factors, for hermetically encapsulated IC's. Accelerated temperature-voltage stress testing at temperatures up to 300°C has been used for discrete, hermetically encapsulated semiconductor components. Much less is known about upper temperature limits for plastic-encapsulated IC's, and still less is available in the open literature. There is a general feeling that at temperatures in the neighborhood of, or in excess of, the glass transition temperature T_g of common epoxy encapsulant materials, extraneous failure mechanisms may be introduced. Occurrence or enhancement of extraneous or abnormal failure mechanisms is of course contrary to the principle on which accelerated stress testing is based, and gives rise to the possibility of inordinate shortening of the useful life of burned-in IC's.

The section reports on work aimed at determining the upper temperature limits for accelerated temperature-voltage (T-V) stress testing and burn-in for commercially available plastic-encapsulated IC's. It was initially hypothesized that if T-V stress testing were performed over a wide range of temperatures bracketing T_g a definite change in the time-to-failure (TTF) distribution characteristics or a change in the failure mode distribution, or both, would enable the upper temperature limit to be clearly identified. This hypothesis was only partially confirmed, as is discussed later.

Publications entitled "A New Failure Mode for Plastic Encapsulated CMOS IC's Stressed at High Temperatures" and "Accelerated Temperature-Voltage Stress Testing of Plastic Encapsulated IC's" are in preparation.

Reprints of these publications will be transmitted to monitoring agencies. The following description of the work therefore concentrates on major points and conclusions rather than detailed descriptions of experimental results or rationale for conclusions.

2.3.2. Experimental Procedures

One of the prime concerns in applying accelerated T-V stress testing to plastic-encapsulated integrated circuits is the possibility of chip contamination due to the transport of impurities from the plastic package. Since MOS devices display a generally greater sensitivity to surface instability failure mechanisms than bipolar devices, and an approximately equal sensitivity to corrosion failure mechanisms, the CMOS digital logic family was selected for testing. In particular the quad two input NAND gate, type 4011, was picked as being representative of current mature manufacturing technology. The circuit complexity is also low enough to simplify analysis of failed units. The following device lots were purchased directly from two different manufacturers:

Manufacturer	Date Code	Lot Size (units)
A	640	1000
A	715	500
B	7716	550
B	7723	450

In addition, a small sample (50 with date code 514) of the type "A" devices were purchased from a local distributor. The "A" devices were the non-buffered series; the "B" devices were the buffered series. The buffered NAND gates have eight transistors per gate as opposed to four transistors per gate in the non-buffered series circuits.

Accelerated stress test bias conditions were two NAND gates per package with both inputs at V_{ss} (output high) and two NAND gates per package with both inputs at V_{DD} (output low). Supply voltages used during stress testing were generally V_{DD} = 12V and V_{ss} = 0 V although some tests were run with V_{DD} = 5V. In order to simplify the stress test pc boards, which were fabricated in house, the outputs were left open circuited and current limiting resistors were not used. The omission of limiting resistors did not cause any problems. None of the observed failures were attributed to excess power dissipation or overstressed input protection circuits.

Stress temperatures used were generally 125°C, 150°C, 175°C, 190°C and 200°C. All tests were conducted using mechanical convection ovens, and bias was applied at all times when the boards were above room temperature. Device parameters were measured at period down times during each test. These measurements were made at 23°C using V_{DD} = 5V.

Initially, failures were defined as any one or more of the following at room temperature: quiescent supply current, I_L, greater than 500nA; open circuit output levels differing from V_{DD} or V_{ss} by more than 10mV; output levels differing from V_{DD} or V_{ss} by more than 500mV while sinking or sourcing 120μA; or more than a 500mV shift in the gate transfer characteristic. Gate input current was also monitored in some cases. As the testing program proceeded, it was discovered that failures could generally be detected by measuring I_L (for all four combinations of inputs) and open circuit output voltage only. Gate input current was also normally measured.

The following tables summarize the major life tests. Tables 2.3.1 and 2.3.2 include test devices and device test hours from minor experimental stress tests as well as major tests.

Table 2.3.1. Test Devices by Manufacturer/Date Code, At Each Test Temperature

Manufacturer/ Date Code	Units Stress Tested 125°C	150°C	175°C	190°C	200°C
A/514	17	17	0	0	0
A/640	136	153	171	0	0
A/715	136	170	35	33	34
B/7716-7723	144	170	36	34	33
Total	433	510	242	67	67

Grand Total 1319

Table 2.3.2. Device Test Hours by Manufacturer/Date Code, At Each Test Temperature

Manufacturer/ Date Code	Device Test Hours (10^3 Hours)				
	125°C	150°C	175°C	190°C	200°C
A/514	32.0	16.4	0	0	0
A/640	246.8	59.8	10.4	0	0
A/715	366.3	86.7	39.6	1.6	5.0
B/7716-7723	429.3	201.9	67.7	8.8	7.2
Total	1074.4	364.8	117.7	10.4	12.2

2.3.3. Experimental Results: Time-to-Failure Characteristics

Figures 2.3.1. through 2.3.4 show observed cumulative failure percentages versus time for all major stress tests, plotted on log-normal paper. Percentages shown are the statistically unbiased estimator given by the equation

$$\% \text{ failure} = \frac{\text{Number of failures} - 0.5}{\text{Number of devices on test}} \times 100\%$$

Results of stress tests which resulted in very small final cumulative failure percentages (see Table 2.3.3) were not plotted.

If the TTF distributions are log-normal, the data points should approximate a straight line with a median time to failure at 50 cumulative percent and a standard deviation equal to $\ln \frac{\text{time to 50\% failures}}{\text{time to 16\% failures}}$. It is clear from Figures 2.3.1 through 2.3.4 that a simple log-normal TTF distribution was not always observed. The deviations of the data from the simple log-normal distribution apparently fell into two categories. Devices from manufacturer A appeared to show a bimodal log-normal distribution in some cases, with the "weaker" population comprising 30% to 50% of the total test population. This type of behavior is most evident in Figure 2.3.1, which shows results of tests on date code 640 units from manufacturer A. A "break" in the TTF characteristic is obvious for the 175°C test data. The 150°C test data shows what appears to be a break in the TTF characteristic, in the neighborhood of 50% cumulative failures. However, truncation of that test at 1500 hours does not allow a positive conclusion to be drawn. It is significant that the dispersions (σ's) of all the date code 640 stress test data were approximately the same at lower failure percentages and,

Table 2.3.3. Major Stress Tests by Temperature,
Number of Devices per Test, Test Length, and Final Percentage of Test Device Failures

Manufacturer/Date Code	Temperature (°C)	Number on Test	Number of Failures	Total Percentage of Failures (%)	Test Length (hours)
A/514	125	17	3	18	2000
	150	17	9	53	1500
A/640	125	136	34	25	2000
	150	68	42	62	1500
	175	34	26	76	390
A/715	125	136	28	21	3000
	150 (test I)	85	44	52	800
	150 (test II)	85	71	84	1700
	175	35	26	74	3000
	190	33	31	94	350
	200	34	29	85	500
B/7716-7723	125	144	2	1.4	3000
	150 (test I)	85	3	3.5	800
	150 (test II)	85	7	8	1700
	175	36	36	100	3000
	190	34	34	100	350
	200	33	33	100	300

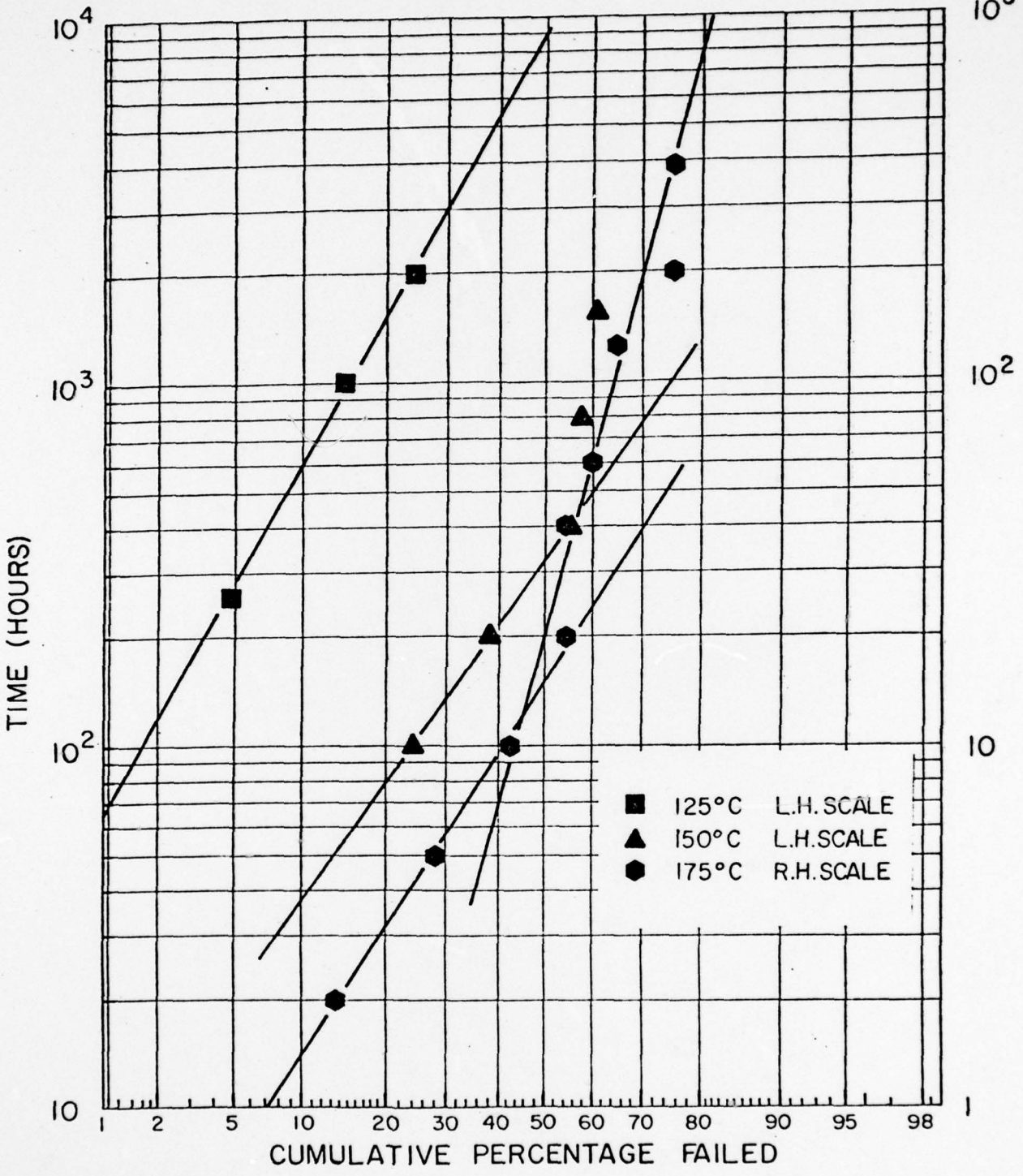


Figure 2.3.1

LOGNORMAL PLOT OF TYPE 4011 CMOS STATIC STRESS TEST DATA. MANUFACTURER A, DATA CODE 640, V_{DD} = 12V. NOTE RIGHT-HAND AND LEFT-HAND TIME SCALES.

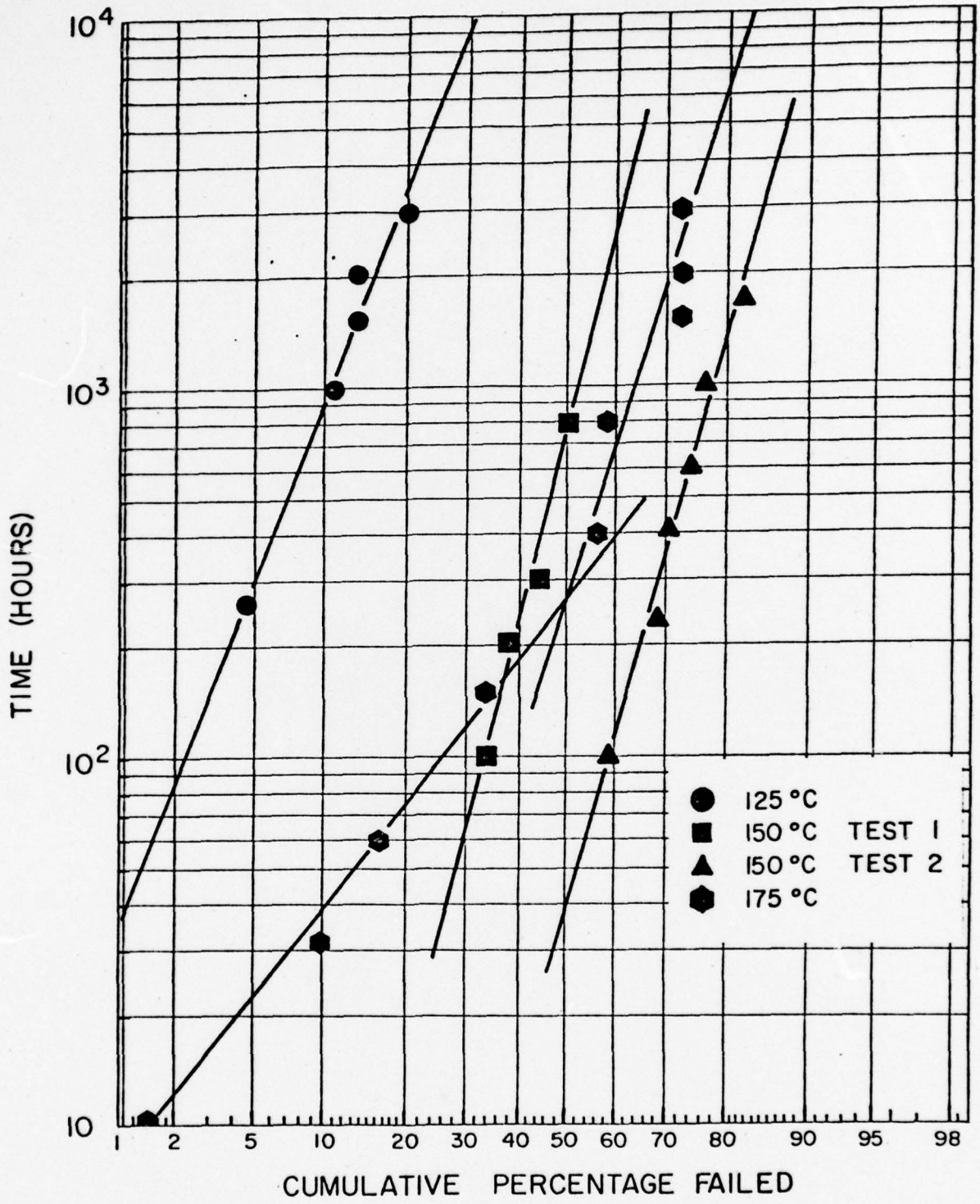


Figure 2.3.2
LOGNORMAL PLOT OF TYPE 4011 CMOS STATIC STRESS TEST DATA. MANUFACTURER A, DATE CODE 715, V_{DD}=12V.

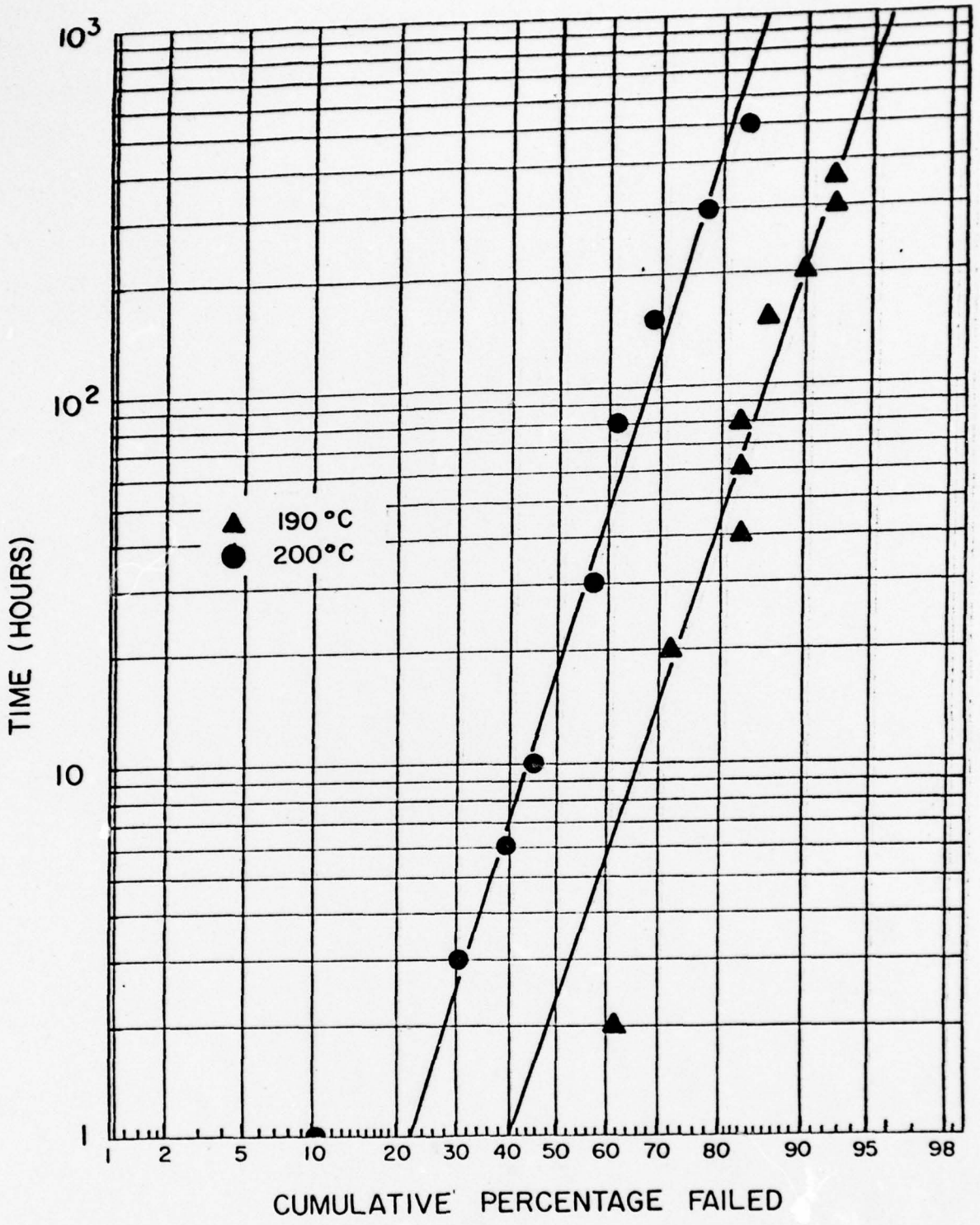


Figure 2.3.3
LOGNORMAL PLOT OF TYPE 4011 CMOS STATIC STRESS TEST DATA. MANUFACTURER A, DATE CODE 715, V_{DD} = 12V.

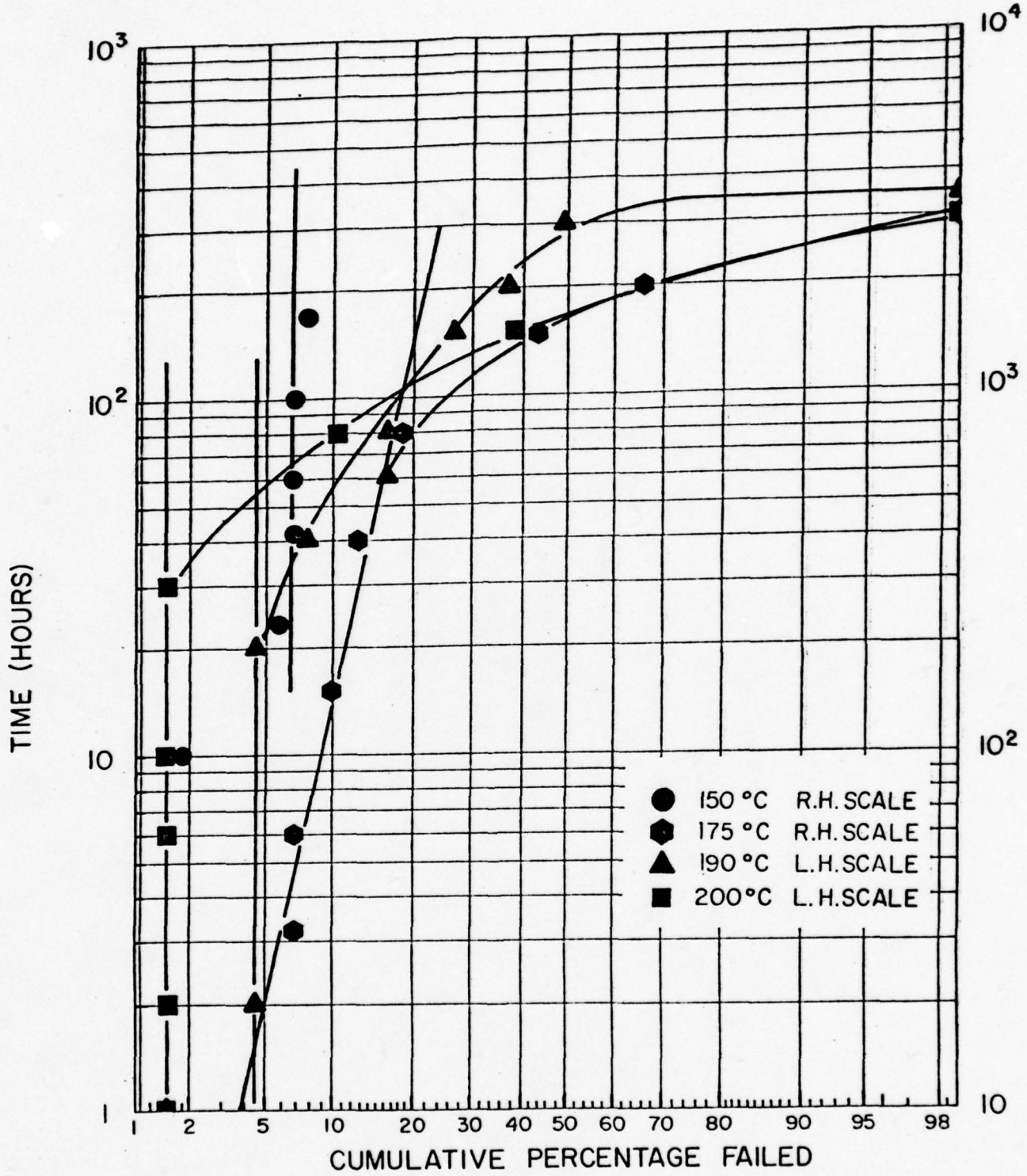


Figure 2.3.4

LOGNORMAL PLOT OF TYPE 4011 CMOS STATIC STRESS TEST DATA. MANUFACTURER B, DATE CODE 7716 AND 7723, V_{DD} = 12V. NOTE RIGHT-HAND AND LEFT-HAND TIME SCALES

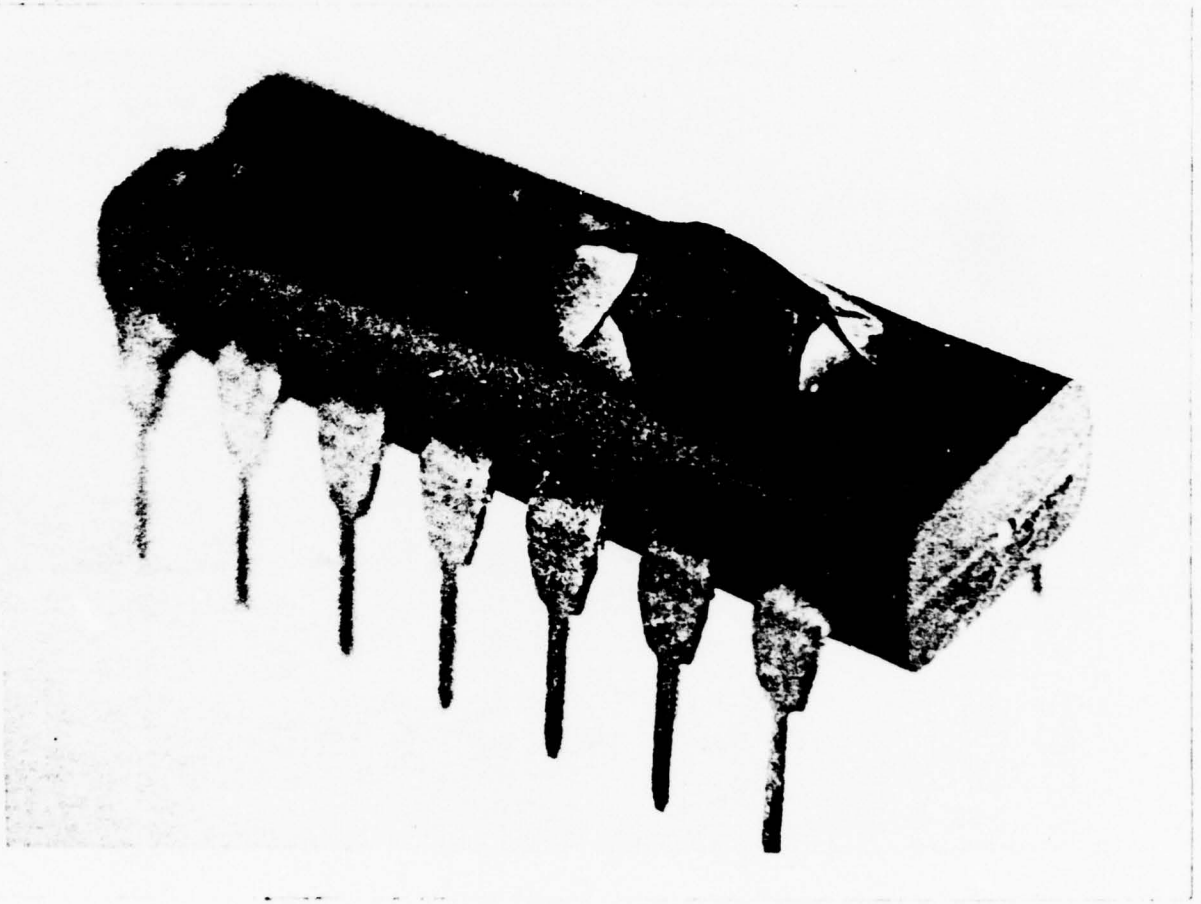


Figure 2.3.5. Typical Appearance of Ruptured Package, Manufacturer B Unit, After 300 Hours of 200°C Temperature-Voltage Stress

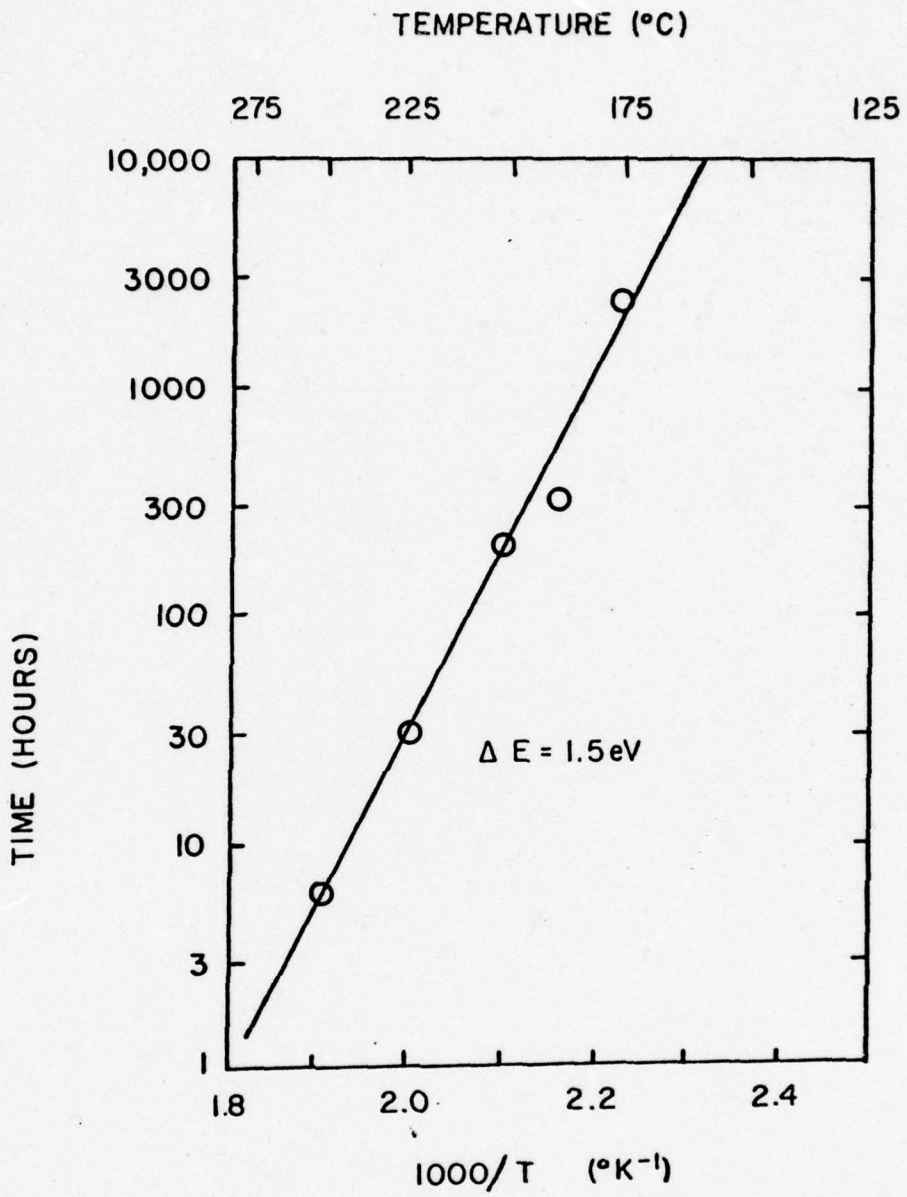


Figure 2.3.6
TIME TO PACKAGE RUPTURE FOR MANUFACTURER B DEVICES, VERSUS 1000/T.

for the 150°C and 175°C tests, approximately the same at failure percentages greater than 50%. These σ's are close to the σ's of the date code 715 stress test data plotted in Figures 2.3.2 and 2.3.3, in the low and high failure percentage regions of the date code 715 plots. Calculation of the activation energy for failure using the portions of the curves in Figure 2.3.1 corresponding to less than 20% failure results in an activation energy of approximately 1.9 - 2.0eV. This value is considerably larger than values normally reported for surface instability failures for hermetically encapsulated CMOS IC's.

The second major type of deviation from simple log-normal behavior of the observed TTF distributions can be seen in Figure 2.3.4. Data shown in this figure is for date code 7716 and date code 7723 units from manufacturer B. It is clear that, with one possible exception (175°C test), none of the results of these tests satisfactorily fits a log-normal distribution over a significant portion of the data spectrum. Packages made by this manufacturer were observed to rupture at test times which depended on the test temperature. Figure 2.3.5 shows such a ruptured package. Rupture, or swelling, of the package correlated with catastrophic electrical failure of the IC. Figure 2.3.6 shows an Arrhenius plot of time to package rupture. The activation energy for this is 1.5eV. The increase of failure rate of manufacturer B units evident in Figure 2.3.4 is assumed to be due to changes in the epoxy encapsulation prior to actual rupture of the package. This sets an upper temperature limit of no more than 150°C to testing or burn-in of manufacturer B units. No swelling or rupture of packages was observed for the longest 150°C test (1700 hours) and no abnormalities of the TTF plot were observed for this test population for times out to 1700 hours. The epoxy used by manufacturer B is Morton 410B; the epoxy used by manufacturer A is Morton 410B-21 which is ostensibly identical to Morton 410B except that an additional flame retardant (SbO_3) is included. This difference apparently prevents rupture of the package for units from manufacturer A. Note that calculation of an activation energy for failure is not possible except for the end-of-life (rupture) portions of the curves in Figure 2.3.4.

Another anomaly in the TTF distributions was found for the units from manufacturer A. As seen in Figure 2.3.2, the second 150°C test for date code 715 units resulted in a much smaller median time to failure (t_m)

than the first 150°C test. In fact the t_m for the second 150°C test was less than that for the 175°C test. In addition, the 190°C test for these units had a t_m which was less than the 200°C test for the same date code units. The only apparent difference in test conditions was that the units had been stored at room temperature for a longer period of time since manufacture, for the second 150°C test and the 190°C test. The time after assembly date-coding was approximately two to four months before the start of the 125°C, 150°C (test I), 175°C and 200°C tests, and was approximately six months before the start of the 190°C and 150°C (test II) tests. A truncated repetition of the 150°C test for date code 640 units showed the same general behavior relative to the first 150°C test for these units. Repetition of the 150°C test for units from manufacturer B at the same time as the manufacturer A test repetitions resulted in the same TTF behavior for this manufacturer's units as was observed initially. It was concluded that room-temperature storage degradation was occurring for units made by manufacturer A. Note that the behavior of the failure rate can not be fitted to an Arrhenius relationship due to this storage degradation.

2.3.4. Experimental Results: Failure Modes and Failure Analysis

Observed failure modes were primarily excessive quiescent supply current I_L for IC's from both manufacturer A and manufacturer B. However, for units from manufacturer B, stressed at temperatures of 175°C and higher, functionality failures were observed at times near the end of the tests. These failures were undoubtedly due to mechanical changes in the epoxy prior to or during the process of package rupture. Neglecting these clearly abnormal failures, the observed failures for all devices were essentially all due to excessive I_L. No simple corrosion failures were found although manufacturer B units which showed package rupture or signs of package swelling did in some cases exhibit anodic corrosion of the metalization. No verifiable bonding or wire failures were found. No verifiable cases of over-stressed input protect circuits were found.

Observed I_L failures were of two types, stable leakage and leakage which increased at room temperature for certain combinations of logic levels applied to the inputs of the NAND gate. Table 2.3.4 shows the percentage of the failures which were I_L failures (by manufacturer, date code, and stress test temperature), and the percentage of the I_L failures which were stable and unstable at room temperature for each stress test. The room temperature instability was always associated with the n-channel transistors. The

Table 2.3.4. Percentage of Failures Due to Excessive I_L, And Percentage of Room-Temperature Stable And Room-Temperature Unstable I_L Failures

Manufacturer/Date Code/Test Temperature (°C)	% I_L Failures	% I_L Failures (Stable)	% I_L Failures (Room-temperature Unstable)
A/640/125	97	52	45
A/640/150	96	52	48
A/640/175	100	62	38
A/715/125	100	21	79
A/715/150 (test I)	100	52	48
A/715/150 (test II)	97	86	11
A/715/175	100	30	70
A/715/190	94	87	7
A/715/200	100	36	64
B/7716-7723/125	100	100	0
B/7716-7723/150 (test I)	100	33	67
B/7716-7723/150 (test II)	100	71	29
B/7716-7723/175 *	44	31	13
B/7716-7723/190 *	53	24	29
B/7716-7723/200 *	39	30	9

* many failures due to package rupture/swelling

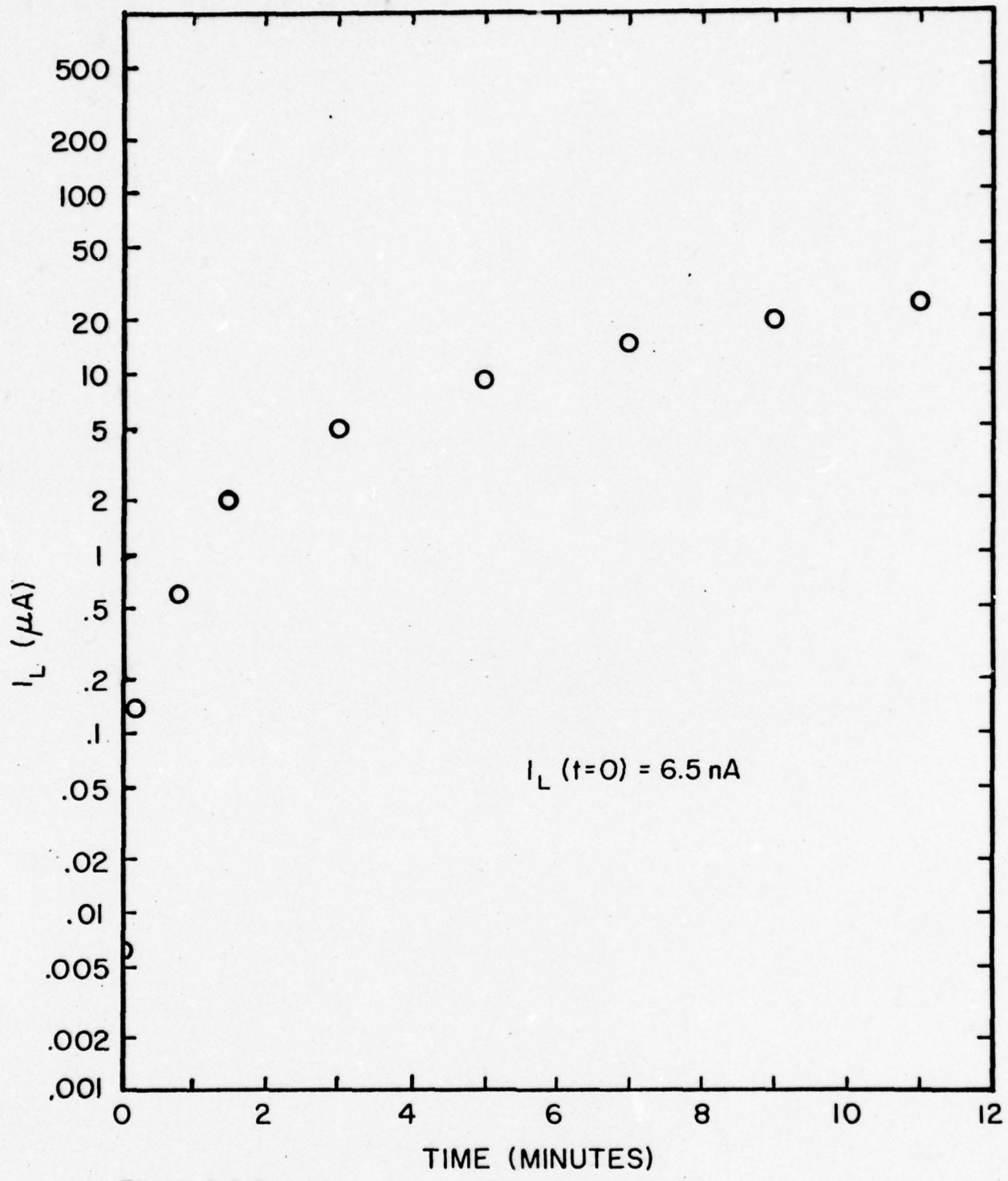


Figure 2.3.7
TIME DEPENDENCE OF QUIESCENT SUPPLY CURRENT I_L (01 INPUT) VERSUS TIME WITH 11 INPUT APPLIED, FOR "PUMP-UP" TYPE FAILURE. T= 25°C, V_{DD}= 5V.

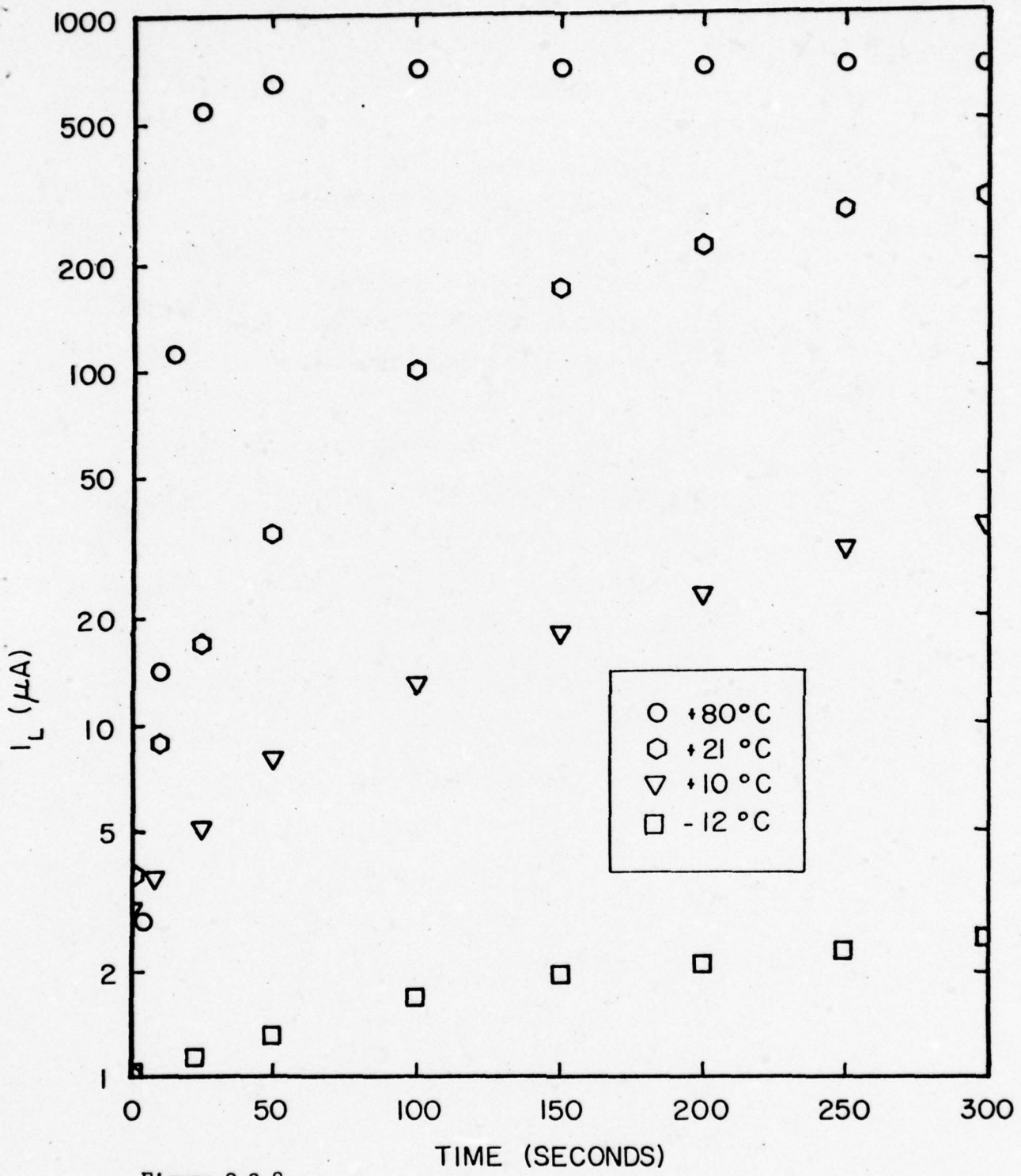


Figure 2.3.8

TYPICAL BEHAVIOR OF QUIESCENT SUPPLY CURRENT I_L (01 INPUT) VERSUS TIME WITH 11 INPUT APPLIED, FOR VARIOUS TEMPERATURES. V_{DD} = 5V.

instability manifested itself when both inputs of some gates were set to a logic 1 for a period of time, and then I_L was remeasured for the other three input conditions; the leakage current was found to have increased for one or all of the other input states. This "pump-up" of leakage current was found to take from less than one second to several minutes to reach the failure level of 500nA. Often I_L could be made to increase several orders of magnitude. Figure 2.3.7 shows I_L at room temperature measured with one input high (V_i = 5V) and one input low (V_i = 0V), versus the time for which the inputs were both held high, for a unit from manufacturer A. The behavior shown in this figure was typical of the "pump-up" failures. The "pump-up" phenomenon is assumed to be unique to plastic encapsulated CMOS IC's, since it has not been reported in the open literature by other workers. It is definitely a surface instability phenomenon which manifests itself as a time- and voltage-dependent decrease in n-channel transistor threshold voltage. This was established by transfer characteristic measurement. The time scale involved in the threshold voltage decrease is on the order of seconds or minutes at room temperature, as mentioned earlier. Figure 2.3.8 shows the behavior of the "pump-up" phenomenon as a function of temperature. It should be noted that for this failure mode the hazard of not detecting failures exists, due to the time dependence of the pump-up behavior and its pattern sensitivity. Depending on the sequence of testing or the time interval involved, many failures could go undetected especially when automatic testing equipment is being used.

In an effort to locate the leakage paths, several tests were conducted. Units exhibiting both stable and "pump-up" I_L failure were annealed without bias at temperatures greater than 125°C and were found to have greatly decreased I_L levels. This behavior is consistent with surface instability failure mechanisms. Units left at room temperature without bias also tended to show improved I_L levels although many weeks were required before this happened. The failures which "became good" by either of these means were found to fail again, and more quickly, if subjected to the same stress conditions which originally caused the failure. Some units which "became good" at room temperature were biased at room temperature along with a control population of virgin units; the units which had previously failed again failed after less than 1000 hours of room temperature testing. No virgin units failed in over 2000 hours of room temperature testing.

During the electrical failure analysis procedure, over 100 failed units were selected at random and analyzed by pin-to-pin electrical measurements. The results are summarized below.

1. Failures were classifiable as excessive I_L (stable or "pump-up"), out of specification output voltage, or absolutely non-functional (catastrophic, due to package rupture), or combinations of these.
2. Most I_L failures were not caused by leakage associated with the input protect circuitry.
3. Output voltage failures were usually associated with very large values of I_L.
4. Stable, single gate I_L failures could occur for any or all input conditions. This was not dependent on how the inputs were biased during temperature stressing.
5. Either of the two n-channel transistors in a single logic gate could exhibit pump-up I_L failure, but only if the gate of the transistor was at a logic low (V_i = 0V), during stress testing.

Physical failure analysis was performed on many of the above units. It consisted of (1) cleaning the exterior of the package, (2) stripping the epoxy encapsulant locally, above the IC chip, and, (3) stripping the protective oxide overcoat from the surface of the IC chip. The stripping of the overcoat was done in several stages to prevent inordinate etching of the thermal oxide. Electrical measurements performed during the process lead to the conclusion that the I_L failures were not due to conduction, mobile charge, or dipoles in the encapsulant, in the protective overcoat, or at any interfaces from the thermal oxide-overcoat interface outward into the encapsulant.

Additional electrical measurements such as measurement of the I_L - V_{DD} characteristic and the V_D - V_i transfer characteristic allowed the following conclusions:

1. The room-temperature stable I_L failures were caused by mobile charge in the thermal oxide which resulted in soft junction breakdown characteristics in some cases, and in channelling conduction characteristics in other cases.

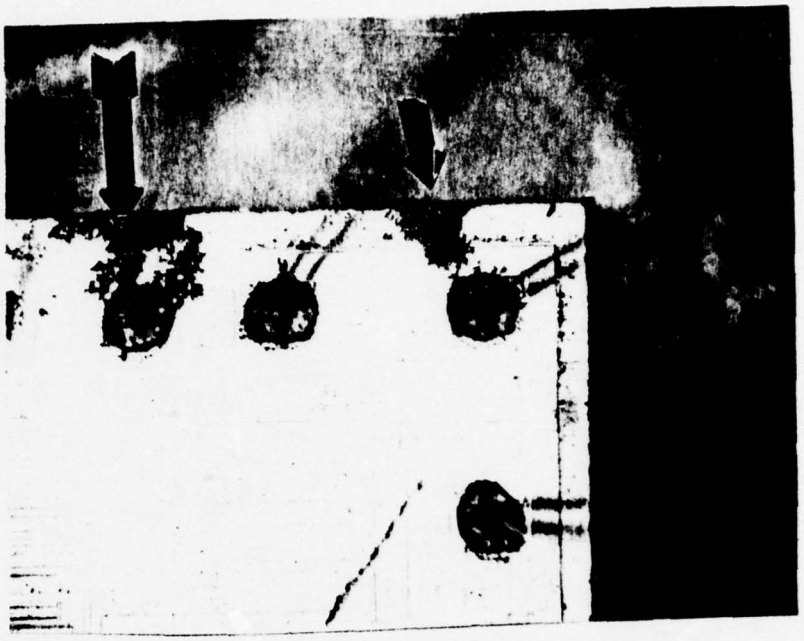
2. The "pump-up" I_L failures were caused by a charge instability in the gate oxide of one or the other of the n-channel transistors which resulted in a room temperature instability of n-channel threshold voltage after high temperature failure. The charge instability is believed to be due to movement of charged species and not a polarization phenomenon.

Observations made on non-failed manufacturer A units after 3000 hours of 175°C testing showed incipient failures due to migration of silver, apparently from the die attach epoxy, to the top of the IC chip particularly in the vicinity of bond pads. Figure 2.3.9 shows the appearance of the migrated silver under visible light and scanning electron microscopes. The material was identified as silver by energy dispersive analysis of x-rays, conducted by manufacturer A laboratory personnel. Material similar in appearance to that shown in Figure 2.3.9 was observed on the surface of 2000 hour failures from the same test. The material did not cause failure of these units. The reliability hazard posed by this mechanism is clear. Presumably the mechanism is correlated with the use of epoxy encapsulation. The occurrence of the mechanism has not been reported before. Note that migrated silver was not found on earlier failures from the same stress test, nor was such material found on failures from any other stress test.

2.3.5. Conclusions

From observed time-to-failure distributions, failure modes and failure mechanisms it is clear that substantial IC chip encapsulant interaction occurs at high temperature for epoxy encapsulated CMOS IC's. Several effects of this interaction were observed. Room temperature storage degradation, extraordinarily high activation energy for failure, and package rupture were some of the gross effects which were noted. Other less obvious effects found were a new pattern-sensitive charge instability failure mode and silver migration on the IC chip surface.

Taken in total, results of the study lead to the conclusion that the upper temperature limit for accelerated T-V stress testing of epoxy encapsulated CMOS IC's is no higher than 150°C for devices from manufacturer B. Data on stress testing of devices from manufacturer A indicates a very



a. Visible light micrograph showing migrated silver (arrows)

b. Scanning electron microscope view of migrated silver, 300X

Figure 2.3.9. Visible Light and Scanning Electron Microscope Views of Migrated Silver. Manufacturer A Unit, Post-3000 Hours at 175°C (Non-Fail)

complex situation. From this work it seems reasonable to say that the upper temperature limit is no more than 125°C. In fact, the limit may even be less than this temperature; however, data was not obtained at temperatures below 125°C.

The results of this work show the complex nature of the IC chip-encapsulant interaction for epoxy encapsulated IC's at high temperature. The results indicated the serious problems, and lack of fundamental understanding, involved in the application of accelerated stress testing and high temperature burn-in to these devices. Considerably more work is required before real understanding of the mechanisms involved exists.

2.4. Yield-Reliability Correlation Study

2.4.1. Introduction

The possibility of a significant correlation between the yield and reliability attributes of an IC lot has been for years tacitly accepted by many. The idea has its origins in the early years of the semiconductor inductry. The justification for the correlation revolves partially around the general feeling that high yield requires high "quality", and that the attributes of "quality", particularly in workmanship, result in high reliability. Another part of the justification is the gross experimental correlation between failure modes and yield loss. For example, using information from Prince (1973) and Wilson and Long (1973), it can be concluded that 50% of yield loss of MOS LSI circuits is due to patterning (41%) and oxidation/passivation (9%), and that 50% of reliability failures are also due to these factors (patterning 14%, oxidation/passivation 36%).

There is a serious lack of data on which to base an analysis of yield-reliability correlation. The data cited above is the best yield loss data available to date, but it is sketchy and is now somewhat out of date. In this section will be addressed the following two questions:

a. To what degree are the relative number of IC's which are rejected at a yield inspection point correlated with, or indicative of, incipient failures remaining in the yielded device population?

b. To what extent are incipient failures in a device population after final test caused by mechanisms which are <u>not</u> associated with yield loss.

Another question which could be addressed is "to what degree are certain human related yield losses (such as broken or dropped slices, mistakes in reading lot travelers, etc.) correlated with incipient failures?". These types of yield losses are randomly distributed through the manufacturing process, and are not considered here to be a necessary part of the normal process. The loss due to these factors is currently being decreased by automation of the manufacturing process and will be ignored here.

The approach taken in this analysis was first to examine the IC manufacturing process for three major IC families (TTL, linear, and CMOS) in order to determine yield inspection points and yield criteria used.

Toward this end a major IC manufacturer was consulted and a production line was visited. Management and disposition of yield data (both slice and final test) was discussed with two major manufacturers, and the amount of and analysis conducted on final test yield data was also discussed. Failure mode distribution and failure mechanism data from the literature was assembled and the yield loss distribution data which exists was evaluated. Projections of future failure mode distributions were made in order to take into account technology trends in the industry. A gross estimation of the degree of correlation between yield loss mechanisms and failure-causing mechanisms was made and an experiment to verify the correlation was outlined.

2.4.2. Integrated Circuit Yield and Manufacturing Process Flow

Far from being a simple concept, IC yield is in fact a complex subject. To begin with, there are several different types of yield commomly in use throughout the semiconductor industry. There is the overall yield (OAY) which is the ratio of the actual number of electrically good integrated circuits produced, to the number of integrated circuits it would theoretically be possible to produce if the processing were perfect:

$$\text{OAY} = \frac{\text{\# actual IC's}}{\text{\# possible IC's}} .$$

This yield must be further defined, however, by stipulating a limit. For example, Eq. (1) could refer to a particular slice. Then,

$$\text{SOAY} = \frac{\text{\# actual IC's produced from a particular slice}}{\text{\# possible IC's which could be produced from this slice}}$$

or Eq. (1) could refer to a particular lot of slices

$$\text{LOAY} = \frac{\text{\# actual IC's produced from a particular lot}}{\text{\# possible IC's which could be produced from this lot}}$$

Both SOAY and LOAY are dependent on time. Since the number of possible IC's per slice will not vary appreciably from lot to lot, being affected primarily by the placement of the pattern on the slice,

$$\text{LOAY} = \frac{\sum_{i=0}^{N} \text{SOAY}}{N}$$

where N is the number of slices in the particular lot. However, while SOAY and LOAY can be experimentally determined they are rarely documented in practice. In order to discuss the more commonly used yields we first need to discuss the IC manufacturing process.

The IC manufacturing process is made up of a large number of fabrication operations as shown schematically in Figure 2.4.1. Figures 2.4.2 and 2.4.3 show a linear IC manufacturing process in some detail. In Figure 2.4.1 there are j slice processing operations which involve steps such as diffusion, photomasking, and metal deposition, and k assembly operations which involve steps such as mounting, bonding, and encapsulation. Present batch fabrication technology dictates that the slices progress through the fabrication sequence in lots whose size is generally dictated by the capacity of the diffusion furnaces. This is typically 100 slices. After the slices are scribed into bars following electrical slice probe, lot identity is generally lost except in special cases (e.g. Hi-Rel production lines).

In addition to the fabrication steps there are at least two electrical test points -- electrical slice probe, in which each circuit on every slice is tested for dc functionality, and final test, which includes both ac and dc functionality, but which may not be applied with equal severity to all devices. Thus the generalized IC manufacturing operation consists of slice processing, circuit assembly, slice probe and final test. Each operation within the sequence has a yield associated with it. Let us first consider the sequential slice processing operations. The IC manufacturer, in an attempt to both control processing and optimize material flow, has established Quality Control (QC) points associated with each processing step. The yield at each step fluctuates randomly and detailed slice yield data* is collected at each of these points by lot, and daily, weekly, and monthly composite average yields are generated.

The criteria for acceptance or rejection, which determines each operational yield, will vary both from manufacturer to manufacturer and from operation to operation. However, in practically no case is it possible to examine in-process slices for electrical functionality, or for that matter, even positive physical attributes. Slice evaluation is largely based on the number of negative characteristics observed--pinholes in the oxide for example. Thus most slice processing yields are based on visual inspection only. Based on predetermined visual inspection criteria and a predetermined sampling plan, slices are either accepted or rejected even

* The slice yield for the i^{th} step is the ratio of the number of slices in the lot sent to the $(i + 1)^{th}$ step to the number of slices received from the $(i - 1)^{th}$ step. Note that the yield is in terms of slices.

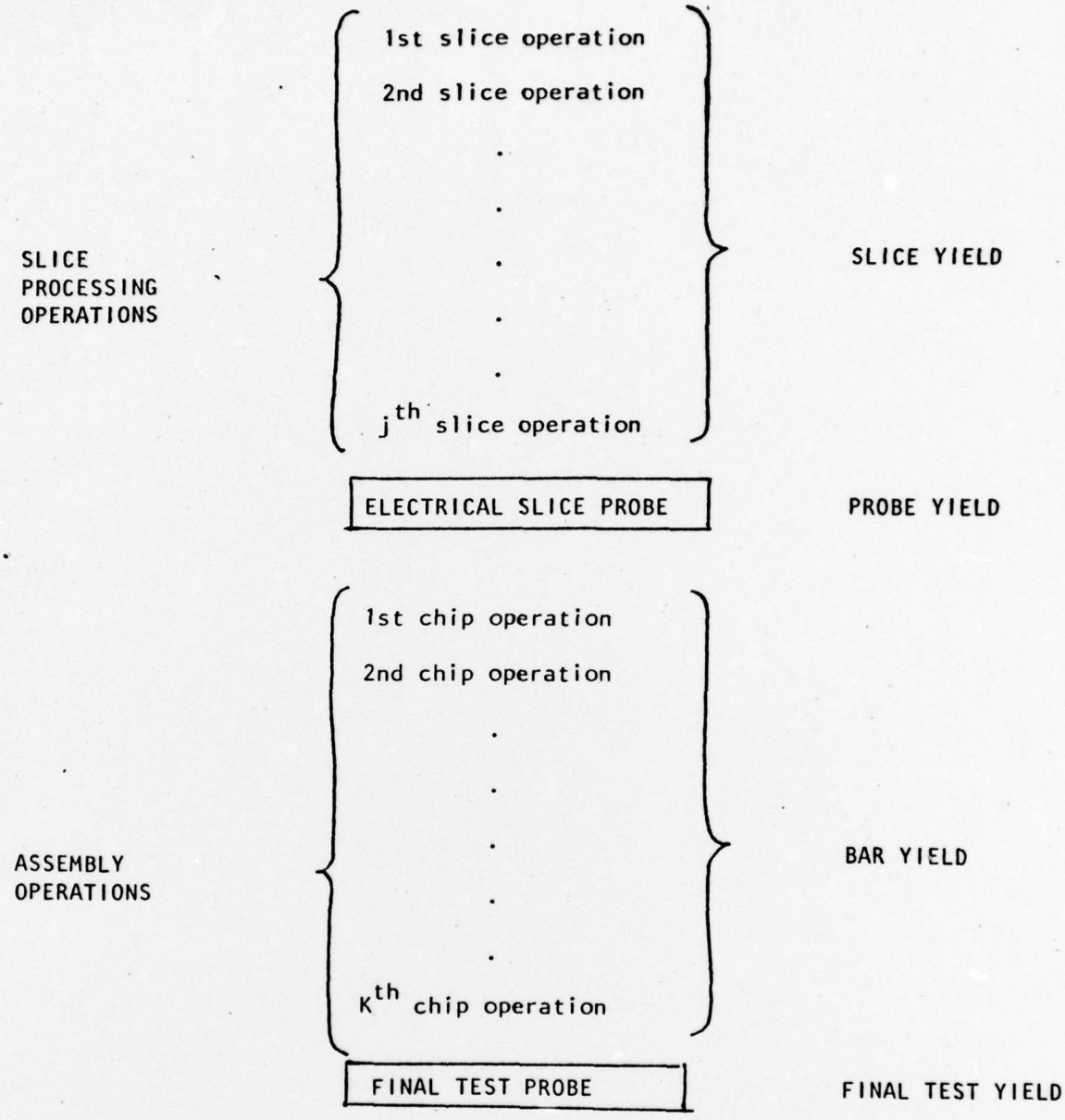


Figure 2.4.1. INTEGRATED CIRCUIT MANUFACTURING SEQUENCE

Figure 2.4.2. Linear IC Process Flow

1. Substrated Clean
2. Initial Oxidation
3. Measure Oxide Thickness
4. Photoresist Process
5. Oxide Etch
6. Photoresist Removal
7. Post Etch Inspection
8. Standard Clean
9. N^+ Buried Collector Deposition
10. Glass Removal
11. Measure R_S
12. Definition Oxidation
13. Oxide Removal
14. Standard Clean
15. Epitaxial Growth
16. Epi Inspect
17. Standard Clean
18. Isolation Oxidation
19. Measure Thickness
20. Photoresist Process
21. Oxide Etch
22. Photoresist Removal
23. Post Etch Inspection
24. Standard Clean
25. Isolation Deposition
26. Glass Removal
27. Measure R_S
28. Isolation Diffusion
29. Oxide Etch
30. Isolation Probe
31. Standard Clean
32. Base Oxidation
33. Photoresist Process
34. Oxide Etch
35. Photoresist Removal
36. Post Etch Inspection
37. Base Deposition
38. Glass Removal
39. Measure R_S
40. Base Diffusion
41. Measure R_S
42. Photoresist Process
43. Oxide Etch
44. Photoresist Removal
45. Post Etch Inspection
46. Emitter Cleaning
47. Emitter Diffusion
48. Glass Etch
49. Measure R_S
50. Thermal Oxidation
51. Photoresist Process
52. Oxide Etch
53. Photoresist Removal
54. Post Etch Inspection
55. Standard Clean
56. Capacitor Oxidation
57. Measure Thickness
58. Pre-Nitride Etch

To Metalization Process

Figure 2.4.3. Trimetal/Sealed Junction
Metalization and Passivation Process

1. Si_3N_4 Deposition
2. Measure Thickness and Etch Rate
3. Oxide Deposition
4. Measure Thickness
5. Photoresist Process
6. Oxide Etch
7. Inspect
8. Photoresist Removal
9. Si_3N_4 Etch
10. Oxide Etch
11. Post Etch Inspection
12. Pre-Metal Clean
13. PT Sputter
14. Measure Thickness
15. Pt Si Formation
16. Pt Etch
17. Inspect
18. Clean
19. Ti/Pt Sputter
20. Measure Thickness
21. Photoresist Process
22. Pt Etch
23. Inspect
24. Photoresist Removal
25. Photoresist Process
26. Au Plate (Interconnects)
27. Measure Thickness
28. Photoresist Removal
29. Post Plate Inspect
30. Photoresist Process
31. Au Plate (Bumps)
32. Measure Thickness
33. Photoresist Removal
34. Post Plate Inspect
35. Ti Etch
36. Inspect
37. Si_3N_4 Overcoat Deposition
38. Photoresist Process
39. Si_3N_4 Etch
40. Inspect
41. Photoresist Removal
42. Inspect

To DC Probe

though some good bars may be discarded and some defective bars accepted. The determination of yield for some diffusion and oxidation operations, on the other hand, may be based on the destructive evaluation of pilot slices. On the basis of a pilot slice the entire lot will be either accepted (100% yield) or rejected (0% yield). Many factors both technical and economic, go into determining the particular process acceptance criteria, and they are continually refined as the process evolves and situations change.

Some fabrication steps lend themselves to rework. An example would be the forming of metal interconnections. If visual inspection revealed excessive overetching the metal could be stripped, redeposited and reetched. Reworked slices are then brought back into the system as "bonus" lots or "bonus" slices inserted into existing lots, with the processing history of the slices lost. Bonus lots or slices will momentarily inprove process yields for the affected operation, sometimes even resulting in greater than 100% yields. Bonus slices also compromise the integrity of ordinary lots.

The slice yield of Figure 2.4.1, as used in IC manufacturing, is the product of all the individual process operation yields during the same period. Thus the slice yield for a particular lot may never be tabulated even though the raw data exists. Instead the manufacturer's daily slice yield might involve the product of the metalization yield of lot #75, the contact oxidation removal yield of lot #74, the emitter diffusion yield of lot #73, etc. Thus, the daily slice yield refers to the yield which would be experienced by a hypothetical lot which was able to complete all slice processing operations in a single day and which experienced that day's average yield at each operation. Because of statistical fluctuations in the number of lots going through each process step the daily slice yield is not a particularly meaningful parameter. For this reason daily yields are maintained for each operation, but usually are not multiplied together. On the other hand, the monthly slice yield has considerable significance and is used effectively in monthly management reviews and pricing meetings. Thus, the monthly slice yield would be the yield which a hypothetical lot would experience if it completed all the slice processing steps experiencing the monthly average yield at each step.

Unfortunately the yield for an individual process step does not reflect that step's technological impact on the overall yield because of

two factors, the sampling character of determining process yields and the non-functional nature of the process acceptance criteria. The first functional test which the individual circuits undergo is slice probe. Defective units at slice probe will be due to faults which occurred at one or more of the preceeding process operations. However, unless the probe yield is abnormally low little or no defect analysis is performed to related electrical test defects to particular processing steps.

In the analysis thus far we have assumed the slices to be travelling through the process in lots. It has long been a dream of IC manufacturers to develop a continuous process similar to an automobile assembly line. Much effort has already been devoted to this concept and it will undoubtedly occur with time. A continuous process will also be characterized by process operation yields, but the yields will be gathered either on the basis of a time period or an arbitrary number of slices rather than some initial quantity of slices started into the process. From a process control standpoint, the important consideration in determining either the time period or the number of slices to be used in yield calculations is that it be sufficiently small that the yield can be considered constant during the time of processing. Continuous slice processing is somewhat akin to the present assembly process, where lot identification is generally not maintained. Acceptance criteria are primarily visual in the assembly process, but involve 100% inspection. Quite often the inspection is done by the operators themselves rather than QC personnel. Defects are generally catastrophic such as broken bars, open bonds, etc. The assembly yield is the product of the yields of each individual assembly operation.

Final test yields involve faults which occurred during slice processing and were not detected at slice probe and electrical faults which occurred during assembly. There is a tradeoff between dc probe yield and final test yield. Tightened electrical criteria at dc probe tend to decrease probe yield but raise final test yield. The inverse is also true. Typically final test involves 100% dc, sample ac, and sample temperature extreme testing. The overall yield for the IC involves the product of the slice process yield, the assembly yield, the slice probe yield and the final test yield. Thus the overall manufacturing yield for a particular period is the ratio (in percent) of good IC's produced during that period to the number of possible IC's that could have been produced during that period assuming that the material experienced the average yield which occurred

during that period at each step in the process.

The above discussion of IC yield illustrates the complexity of the yield data gathering and date management problem. Meetings were arranged with personnel from two major IC manufacturers to discuss yield loss criteria, details of the manufacturing process flow, yield loss allocation at dc probe and final test, and yield data management. As mentioned earlier, inspection criteria in the manufacturing process are almost entirely based on visual inspection at photolithographic steps, and slice rework and "bonusing" of slices is common. The overall picture that emerged from the discussions was that no effort was generally made to allocate yield loss at electrical test to workmanship problems at individual process steps. No effort had been made by these manufacturers to correlate yield and reliability. One manufacturer categorically stated that there was no such correlation and that if there were, the company would not sell IC's based on the correlation as a matter of policy.

Some records are kept of dc probe and final test yields. The management and accessibility of this data, and perhaps its accuracy, varies widely between manufacturers. As mentioned previously, after dc probe, lot identity is lost in the (offshore) assembly process. The only correlation between assembled units and LOAY is a tenuous one based on the average assembly process cycle time and the time of shipment of assembled units from offshore locations. Thus with current practice units received back from offshore locations can be associated with a certain time span of manufacturing, but not with individual manufacturing lots. Even if assembled units could be tracked back to a certain process lot, the practice of reworking slices or lots clouds the uniqueness of an individual lot. Any lot may have inserted into it reworked slices from previous lots. This practice exists even in the most modern, automated manufacturing lines.

The conclusion drawn from the investigation of real manufacturing processes is that the problems of qualitative yield criteria, maintenance of lot identification, and maintenance of lot integrity provide substantial barriers to the usefulness of a lot yield-reliability correlation for any manufacturing step before dc probe. There are problems in maintaining lot identity and integrity after dc probe; however these problems are relatively small compared to the problems before dc probe. The usefulness of slice yield data thus seems small for any practical yield-reliability correlation. The usefulness of dc probe yield and final test yield data is not necessarily small, however.

Table 2.4.1. Failure Mode Distributions

Failure Mode	MOS MSI/LSI Prince (1973)	Bipolar SSI Prince (1973)	Bipolar/MOS SSI Johnson and Stitch (1977)
Assembly-Related	9.2	37.8	1.5
Wire-Related	1.3	6.2	0.5
Bond-Related	2.8	9.7	0.3
Alloy-Related	0	1.7	
Cracked die	0	6.2	
Package hermeticity	0.8	5.3	0.7
Particulates	0.4	4.9	
Other	3.9	3.8	
Slice-Related	61.6	42.8	96.8
Oxide instability	19.0	12.1	92.3
Oxide dielectric defects	17.0	7.6	1.0
Metal migration	0	0.4	
Metal damage	1.1	1.2	
Metal step coverage	0	1.7	2.4
Metal adhesion	0	1.8	
Metal decomposition	8.3	5.3	
Metal-Silicon contact	2.4	2.1	
Patterning defects	13.8	3.8	
Bulk-related	0	2.8	1.1
Other	0	4.0	0.3
"Overstress"	29.2	19.4	1.4

An attempt was made to obtain yield loss allocation data from the manufacturers consulted for SOAY and LOAY. This attempt was not successful. The only yield loss data available is therefore that previously cited. This data shows primary yield loss categories of patterning and oxidation/passivation. The total of these two categories was (1973) 50% of total yield loss. No more recent data exists in the open literature.

2.4.3. IC Failure Modes

IC failure mode distributions must be considered in the light of the technology of the IC families. TTL IC's, for example, show a reduced sensitivity to surface instability failures; CMOS and linear IC's are generally quite sensitive to such failure mechanisms. The most recent and complete data on IC failure modes is due to Johnson and Stitch (1977), although relatively complete data was reported earlier by Prince (1973). The data reported by these workers pertains to standard Al technology IC's. The more recent data shows a preponderance of surface instability failures, with essentially no failures due to bond/wire problems. Although there are complications in extrapolation of the data presented due to variations in level of screening and packaging technology, weighting of the data by current technology trends (e.g., TAB assembly) results in the conclusion that future failure mode distributions will have essentially no bond/wire problems and will have a preponderance of surface instability failures. Table 2.4.1 shows failure mode distribution data which appears to show this trend. Note that the data shown in Table 2.4.1 originated in quite different circumstances [failure analysis laboratory (Prince) versus controlled reliability testing program (Johnson and Stitch)]. The future failure mode distributions will be heavily oriented toward surface instability mechanisms and possibly random defects (e.g., contact pitting, patterning defects in oxides or metalization, etc.). This last category may become even more important as IC packing densities and therefore metalization current densities increase.

2.4.4. IC Yield-Reliability Correlation

The probability of correlation between certain categories of IC slice yield loss (e.g., patterning losses) and the occurrence of some failure modes can be argued to be quite high. For example, take the patterning step associated with base oxide removal. Anomalies in the process can derive from many sources, including photoresist breakdown, mask defects, under and over-etching, and operator error. Photoresist breakdown, and thus loss of

etch-masking ability of the photoresist film, can itself occur due to several causes, including substandard photoresist material, improper baking cycle, photoresist developing problems, and contaminated or improper etch solutions. Mechanical abrasion of the film before the final bake could also be added to this list. It is likely that the effect of photoresist breakdown, no matter what the root cause, will not be uniformly severe across a slice or from slice to slice. Thus, at the post-etch inspection step shown in Figure 2.4.2 some slices in the lot will be rejected for severe anomalies (pinholes or worse) while others will be passed on to the next step even though some pinholes exist. If slices in a lot are rejected at this point in the process, due to photoresist breakdown, it is fairly certain that other slices in the lot which passed process control inspection are affected by the same problems, due to the same causes, except that the severity of the "problem" is less. Of the bars with pinholes which are passed on to dc probe, a large percentage will probably not be functional due to the existence of the pinholes. However, not all pinholes are of equal size or depth, so some IC's with dielectric defects will be passed through final test as properly functioning devices. These devices constitute potential reliability problems.

In spite of the above plausibility statement favoring some slice yield-reliability correlation, the usefulness of any such correlation would seem small. This is so because of the practical difficulties caused by qualitative yield inspection criteria and lot integrity. However, some of the latent catastrophic defects from the slice processing operation will certainly result in low yield at dc probe. Also, marginal media electrical parameters at dc probe almost certainly mean increased yield loss due to the gaussian distribution of electrical parameters. Thus it is plausible that low dc probe yield is indicative of both incipient failure, due to the sort of catastrophic slice processing problems discussed earlier and incipient degradational failures due to poor electrical parameter distributions. The importance of the distribution of electrical parameters comes about because of the predominance of surface instability failures in the present and projected future failure mode distributions. Thus dc probe yield appears to be a yield that can be (theoretically) correlated with incipient failures and a yield that can be obtained and used for yield-reliability correlation.

The above conclusion suggests that the existence of a yield-reliability correlation can be proven or disproven by a series of experiments based on the dc probe yield of slices. In order to do this the probe yield losses

must be allocated between catastrophic (e.g., electrical opens or shorts) and parametric (e.g., marginally out-of-spec electrical parameters). Two parallel experiments are suggested. One experiment would require identifying slices which are low yield due to catastrophic problems, assembling surviving units from the slices and comparing their reliability performance under accelerated stress test to units from "average" slices. The other experiment would involve taking units from slices which had average or superior yields due to catastrophic problems, but relatively poor parametric distributions and comparing the reliability performance of these units to the performance of units from slices having equally good "catastrophic" yields and superior parametric distributions. The experiments suggested are not simple in that substantial yield loss analysis would be required at dc probe, and the selection of candidate lots would be critical because few lots would fit the above criteria. In addition, the reliability verification testing would be extensive, probably involving several thousand units. However, demonstration of yield-reliability correlation, or the lack of it, would pay benefits in reliability assurance programs.

2.5. Alternative Reliability Assurance Techniques for Plastic-Encapsulated IC's

Alternatives to MIL-M-28510/MIL-STD-883 screening techniques for reliability assurance of plastic-encapsulated (or, more generally, non-hermetically encapsulated) IC's are required to preserve advantages of availability and cost of these devices. Potential alternatives must be evaluated in terms of both current technology and present technology trends. For example, Al-metalized devices are known to corrode (at least at the bond pads) in moist ambient more rapidly if gross paths exist for ingress of moisture down the leads. Corrosion will always occur sooner or later for Al-metalized, epoxy encapsulated IC's due to the water-permeable nature of the encapsulant and the relative chemical impurity of the encapsulant. Technology trends indicate that gold-metalized devices with plasma-deposited silicon nitride do not corrode or electroplate even if exposed as a bare chip to high humidity, high temperature environments. Thus it may be necessary to determine the lead-plastic "seal" integrity, perhaps on a lot-sample basis, for current technology IC's. Such a screen could be biased temperature-humidity testing on a lot sample or on a 100% screen basis. For future IC's it would not appear to be necessary to screen for this since, with adequate process controls at the slice fabrication level, the corrosion failure mode would not exist. In a real sense, a built-in failure mechanism (for current IC's) will have been eliminated. Similar consideration exist when manual wire bonding is compared to the present technology trend of beam tape assembly.

Reliability assurance techniques for future technology IC's will be proposed. These IC's are defined as having (1) a gold-based metalization system, (2) a sealed-junction technology, (3) a continuous, conformal, crack-free overcoat such as plasma-deposited silicon nitride, (4) assembly by beam tape gang-bonding techniques, and (5) a silicone encapsulant. IC's using all of these techniques are being developed by RCA under Navy contract. For these IC's the limitations on temperature of accelerated stress testing and burn-in discussed in Section 2.3 do not exist because the silicone encapsulation compounds are chemically relatively pure and do not exhibit a glass transition below 300°C. Thus no chip-encapsulant interaction should occur for reasonable temperatures (e.g., temperatures below 300°C). No Al-Au interactions need be considered for these IC's; the Cu-Au interaction which occurs proceeds slowly at temperatures below 300°C, and for beam tape

assembled units the bond-beam strength is considerably in excess of the conventional bond-wire strength. Considering the five technology factors cited above it is clear that most screens currently used will be unnecessary. What will be required is a method to screen out infant mortality failures. Two techniques immediately come to mind, high-temperature burn-in and correlating lot yield with reliability. The high temperature burn-in time and temperature required depends on the TTF characteristics of the main and freak device populations and on the activation energies for failure of the two populations. If the infant mortality population fails with the same activation energy as the main population then the burn-in time required is reduced; if the activation energy is much less then the burn-in time may be quite long even at high temperature. Firm data on the characteristics of the freak population must be obtained before time and temperature of an optimized burn-in screen can be calculated.

An alternative to high temperature burn-in, or an auxiliary technique for use in conjunction with high temperature burn-in, is the use of yield-reliability correlation. This allows the possibility of using "free" data (yield) as a way of inferring reliability attributes. The correlation may be a powerful tool if experimental work is done to prove both its existence and the degree of correlation. Thus at the present time its usefulness as a screen is speculative. Substantial work will be required in order to demonstrate its value. As mentioned in previous sections, there is some doubt on the part of IC industry reliability workers that the correlation even exists.

To the two techniques discussed above could be added other developing techniques such as the dc probe-voltage overstress method described by Hirsch (1977). This technique is finding some acceptance for LSI bipolar IC's which can not practically be inspected visually according to MIL-STD-883. This method described by Hirsch has the advantage of being inexpensive, and the disadvantage of having as yet unknown effects on the TTF characteristics of the main device population.

A possible improved reliability assurance schedule for future IC's would be a combination of high-temperature burn-in (e.g., $T > 200^{\circ}C$) and dc probe yield data. Addition of a dc probe voltage overstress step may also be effective, at little cost. The need for all other screens in the MIL-M-38510 schedule would then be negligible. The details of a technique such as described above will depend on the results of extensive development work as discussed earlier.

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