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This report describes the progress during the second six-month period of an 18-month research program to develop amplifier modules suitable for airborne, active array radar applications. Using GaAs FETs as the active device, the design goal of these amplifier modules is an output power of 5 W with 25-dB gain over the 9- to 10-GHz frequency band. Extensive characterization of the amplifiers during pulsed operation is also part of this program.

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It is projected that the amplifier module will be configured as a cascade of five balanced stages. To achieve high overall amplifier efficiency, the output power of the FETs will be tailored to each of the amplifier stages.

In this report period, three new vapor-phase epitaxial reactors have been constructed under RCA support. Measurements show that excellent well-defined channel layers can be grown on buffer layers which are 1.0 μm or less in thickness using Reactor C.

AuGe ohmic contact technology has been developed to the point of being compatible with the self-aligned gate process. The AuGe contacts have lower resistance, are truly ohmic compared to Ti/Pt/Au contacts, and should result in FETs with improved rf performance.

A new 8G type FET (8G means eight gate stripes per cell) has been developed which has outstanding rf performance. Although it was designed for an output of 0.5 W, close to 0.7 W with 4.8-dB gain and 32% power-added efficiency has been achieved at 10 GHz.

Amplifiers have been designed, fabricated, and tested for the first four stages of the module. The first two stages, using DXL-3501 and 4G FET pellets, have sufficient power and gain. The power output of the third stage using 8G FETs exceeds the stage power requirement, but the gain is low. The fourth stage, utilizing 16G FETs peaks at 8.5 GHz rather than the desired 9.5 GHz, although the power and gain levels are close to the requirements of that stage.

Interdigitated couplers are being developed to permit pairs of amplifiers to be combined into balanced amplifier stages. Final adjustments of the amplifier responses will be made at that time.

New measurements of AM/PM conversion show that FET amplifiers are less susceptible to this error than originally reported. In particular, a multistage amplifier with a 500-mW output has a maximum AM/PM conversion of 3.5°/dB.

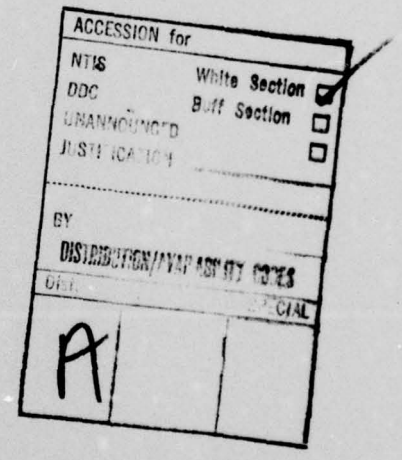
The high breakdown voltage required of the FET when using gate pulsing is difficult to achieve simultaneously with good rf performance. Drain pulsing should therefore be considered as an alternative.

Twenty FETs have been delivered to the contracting agency during this period.

PREFACE

This Semiannual Report describes the progress of the research performed for the period 1 April 1977 to 30 September 1977, under Contract N00173-76-C-0383 at RCA Laboratories, Princeton, N.J., in the Microwave Technology Center, F. Sterzer, Director. The Project Supervisor is S. Y. Narayan and the Project Scientists are R. L. Ernst and H. C. Huang.

The Navy Project Engineer is E. Cohen of Naval Research Laboratory. This program is funded by Naval Air Systems Command.



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SECTION I

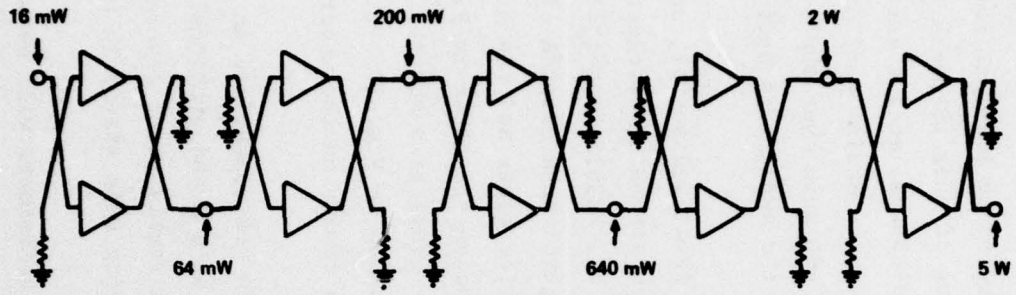
INTRODUCTION

The progress during the second six-month period of an 18-month research program is summarized in this report. The objective of this 18-month research program is to develop amplifier modules suited to airborne, active array radar applications. Using GaAs FETs as the active device, the design goal of these amplifier modules is an output power of 5 W with 25-dB gain over the 9- to 10-GHz frequency band. Extensive characterization of the amplifiers during pulsed operation is also part of this program.

Based upon the current performance of devices developed so far, and upon the predicted performance of higher power FETs which are being developed in this program and in a concurrent program (Contract No. F33615-76-C-1144), it is projected that the amplifier module would be configured as a cascade of five balanced amplifier stages. The anticipated FET device types and the stage-by-stage budget of gain, power levels, and efficiencies are shown in Fig. 1. A mock-up of the amplifier module which shows the overall size and the anticipated layout of the component rf subassemblies is shown in Fig. 2. Pulse modulation and bias circuitry would be located in a cavity on the underside of the module.

The dimensions of the various types of RCA FETs are summarized in Table 1. The four-gate (4G) device uses designs established by RCA and previously reported in the literature. The other devices are currently under development, and the performance obtained from these devices during this six-month period will be given in Section II of this report.

It is projected that the output power stage requirements will be satisfied by using two 32G devices. These devices are designed to operate at higher bias voltages, permitting the attainment of 3 W per device. A 48G device under development should be able to develop 4 W at 10 GHz with a drain to source voltage equal to the 8-V level which is anticipated for the four lower level amplifier stages. Since it is expected that due to its greater complexity, the 48G device will not reach a sufficient performance level during the time frame of this contract, the 32G device is the prime candidate for this amplifier stage.



DEVICE TYPE	3501A	4G	8G	16G	32G
GAIN	6 dB	5 dB	5 dB	5 dB	4 dB
ADDED POWER	48 mW	136 mW	440 mW	1.36 W	3.0 W
DC POWER	267 mW	680 mW	2.2 W	5.44 W	12.0 W
P.A. EFFICIENCY	18%	20%	20%	25%	25%

Total Gain : 25 dB

DC Power : 20.6 W

P.A. Efficiency: 24.3%

Figure 1. Overall amplifier approach.

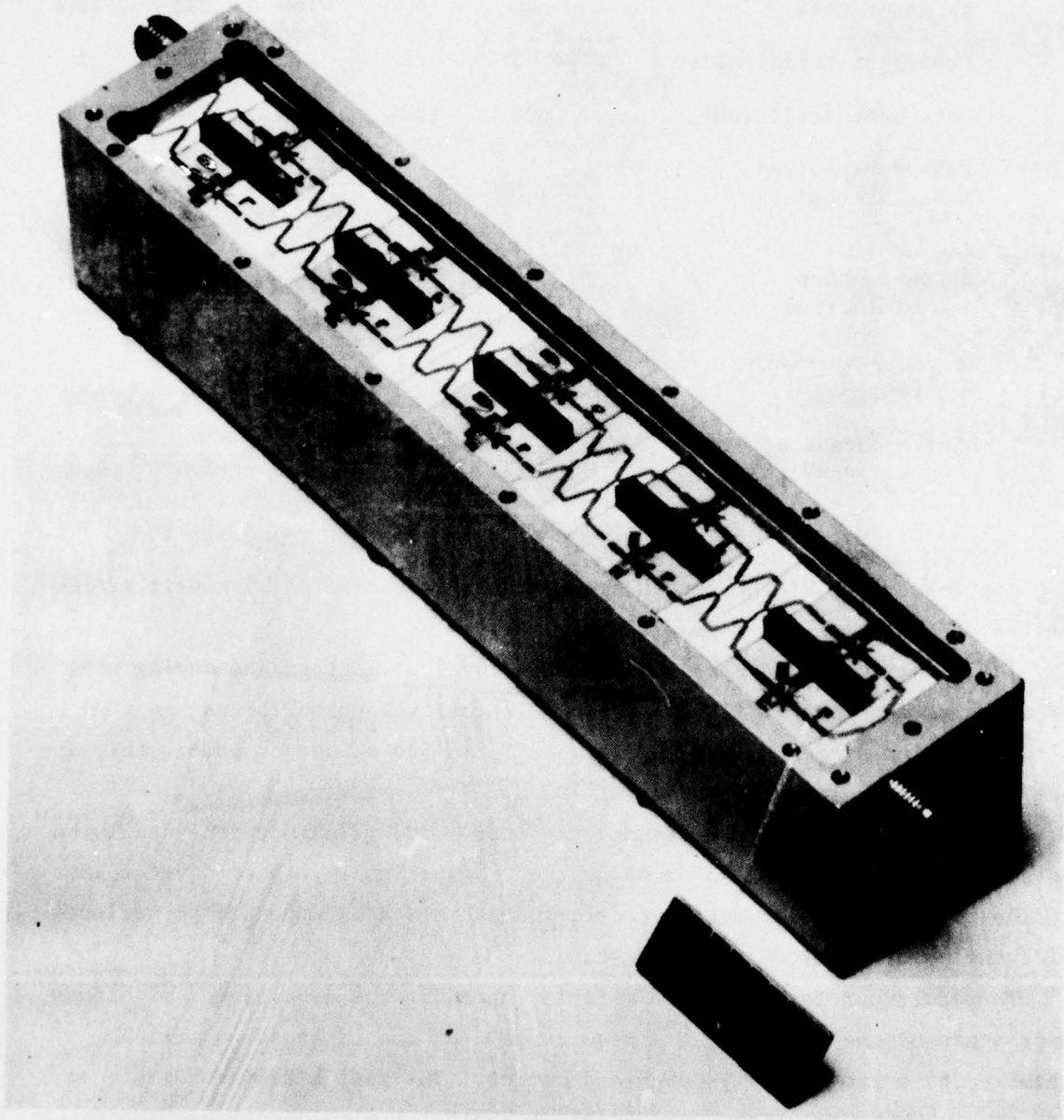


Figure 2. Model of the amplifier module.

TABLE 1. COMPARISON OF FET GEOMETRIES

Designation (number of gates/cell	4G	8G	16G	32G	48G
Number of cells/pellet	5	1	1	1	1
Gate width/cell (μm)	600	1200	2400	4800	9600
Gate length (μm) (mask dimension)	1.0	1.0	0.8, 1.0	0.8, 1.0	1.0, 1.5
Drain contact width (μm)	25	25	12	12	12
Source post width (μm)	50	50	30	30	30
Design output power at V_{DS} = 8V (W)	0.25	0.5	1.0	2.0	4.0

The 2-W output of the fourth stage should be satisfied by a pair of 16G devices designed for a 1-W power level.

The 8G device has reached such a high level of performance during this six-month period that it is now the most logical selection for use in the third amplifier stage. Although designed for a 500-mW output power, this device has achieved levels approaching 700 mW.

The requirements of the second stage for a 200-mW output can ideally be satisfied by a single cell of a 4G device. Historically, these devices have had the greatest developmental effort, and can often be expected to achieve twice the power required for this stage.

To permit our facilities to be fully used for the development of higher power state-of-the-art FETs, the requirements of the first stage will be satisfied by a commercially purchased device. The most likely candidate at this time appears to be the Dexcel (DXL-) 3501A. A single chip has a rated output of 50 mW with 8-dB gain at 10 GHz.

Besides requiring development of new FET types and new amplifier modules, extensive efforts are needed to determine the pulse characteristics of the amplifiers with special efforts and attention to the intrapulse and interpulse

phase properties. The amplifier rf and bias circuitry must then be configured to have optimal pulse characteristics for pulse widths between 0.2 and 20 μs and for duty factors as great as 50%.

During this six-month period, it was realized that a measurement technique error had caused the AM/PM data reported in the first Semiannual Report to be too high. When these measurements are done correctly, it is found that the AM/PM conversion of a complete five-stage amplifier having an output capability of 500 mW is a maximum of 3.5°/dB. This is considerably lower than what would have been expected from the data previously reported for single stages.

This semiannual report will summarize the efforts for the last six months in the following areas:

-Material processing and characterization.

-Device development and fabrication.

-Device evaluation for amplifier design parameters.

-Amplifier design techniques and measured circuit performance.

-Pulsed-phase considerations for FET amplifiers.

Both the progress made in these areas and the problems which have been encountered will be detailed. The program plan for the next six months to alleviate these problem areas will also be given.

SECTION II

MATERIAL AND DEVICE DEVELOPMENT

A. INTRODUCTION

During this report period, under RCA's sponsorship, we have set up additional GaAs reactors. Consequently, part of the device effort was directed toward the evaluation of material characteristics from the new reactor and toward the development of AuGe ohmic contact technology for the new reactor wafers. In order to obtain a consistent evaluation of the new wafers and the AuGe contact technology, we used mainly the 8G FET pattern (designed for 0.5-W output power) to have a uniform base for comparison. At 10 GHz, 8G FETs, with AuGe ohmic contact yield about 540 mW with a power-added efficiency of 26%.

B. MATERIAL DEVELOPMENT

The major effort in the material effort is to devise a technology for consistent growth of 4- to 6-μm buffer layers. Two approaches have been taken. The first approach is to grow undoped buffer layers, and the second is to grow Cr-doped semi-insulating buffer layers. Three additional reactors were constructed during this period. At the end of this report period, one is operational and the other two are under evaluation. Table II shows the designation of our reactors. The old Reactor A, with wafers numbered in the 3000 series, has been completely modified and it is now called Reactor A+ which was completed recently and is being evaluated. No FET wafers have been grown from this reactor yet. Reactor B was constructed prior to the start of this program, and it went through some minor modification in this period to improve the reproducibility. The n+ carrier concentration of the Reactor B wafer is, in general, lower than that of the old Reactor A wafers. Thus, the Ti/Pt/Au ohmic contact, which was developed for the old Reactor A wafers, exhibited rectifying characteristics for Reactor B wafers.

Most of the FET wafers evaluated in this period were from Reactor C, which was constructed and became operational in this period. This reactor has a silane doping time in addition to the usual H_2S time. Hence, we can study the different n and n^+ layer characteristics with Si and S doping.

TABLE 2. RCA's REACTORS (OCTOBER 1977)

Reactor #	Type	Bore Diameter (cm)	Dopant	Remark
A+	AsH_3	2.5	S, Cr	for Cr buffer layer
B	AsH_3	5.0	S	for undoped buffer
C	AsH_3	2.5	S, Si	1. for undoped buffer 2. for Si-doped n+ layer
D	$AsCl_3$	4.0	S	for undoped buffer
A	AsH_3	2.5	S, Se	completely rebuilt to be A+

A series of experiments was formulated for the evaluation of the material characteristics. Wafers of n/buffer/SI substrate were grown. The carrier concentration of n-layer was fixed at about $5x10^{16}$ cm^{-3}, and the thickness (t) fixed at about 0.3 μm. This nt product will permit a carrier concentration profile measurement extending into the buffer layer region. The carrier concentration of the buffer layer is the reactor background concentration. The thickness of the buffer layer was the parameter of the experiment. A series of wafers with buffer layer thickness of 0-, 1-, 2-, 4-, and 6-μm were grown. The carrier concentration profile of each wafer was measured with the use of the C-V technique to determine the carrier concentration of the buffer layer. In addition, van der Pauw measurements were carried out on each wafer to determine the average Hall mobility and average carrier concentration both at 300 and 77 K. A comparison of carrier profile and van der Pauw data reveals the mobility, compensation ratio, and quality of the buffer layer.

Figure 3 shows the carrier density and 77 K mobility (μ_{77}) as a function of depth in a test wafer with n-layer carrier concentration of $5x10^{15}$ cm^{-3}. The carrier density plot was generated using Al Schottky barriers and an automatic profiler, while the μ_{77} profile was generated by an etch-and-test van der Pauw measurement. The Debye length at several carrier density values is indicated on the profile. The spatial resolution of the profiling technique is between 1 and 2 Debye lengths. Note the abrupt n-buffer interface

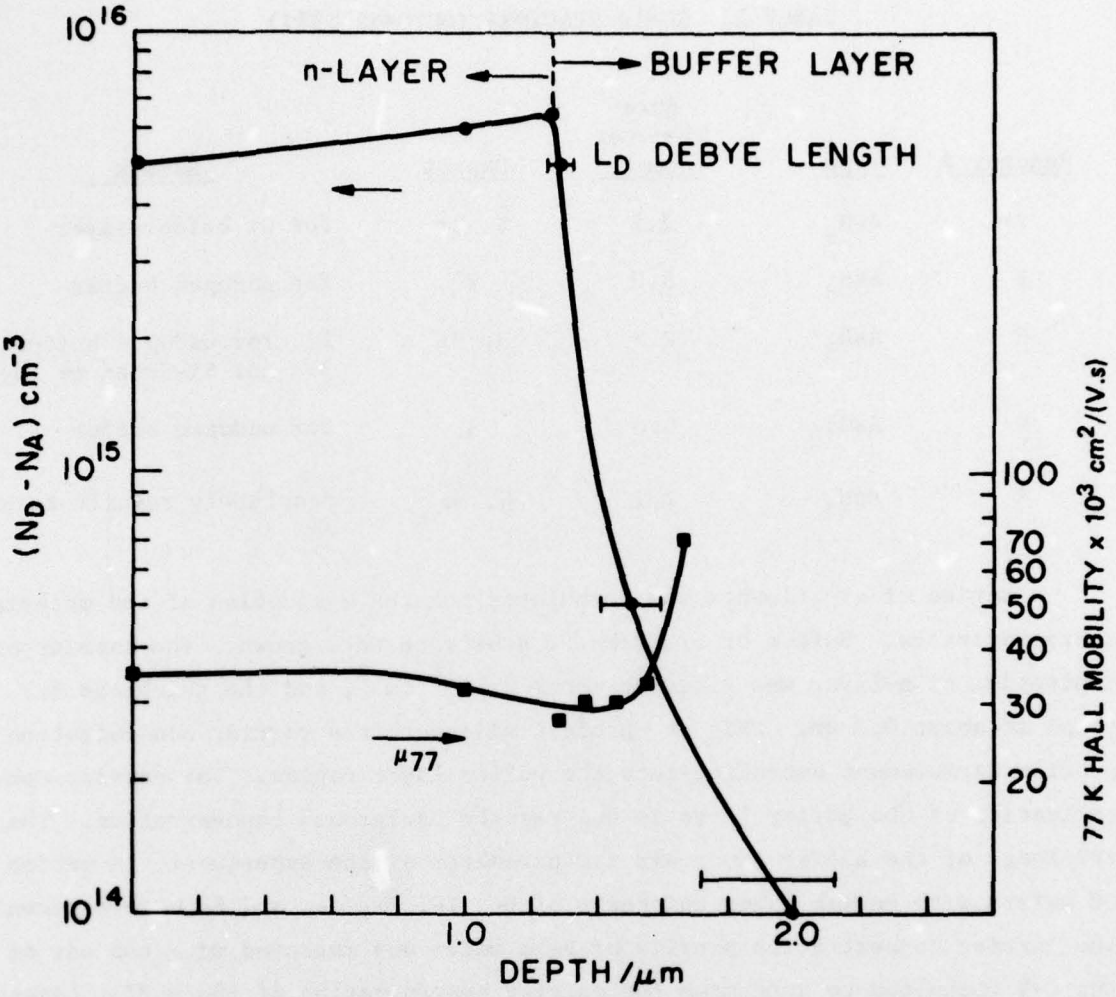


Figure 3. Carrier profile of a Reactor C wafer with buffer layer. The n-layer carrier concentration is 5×10^{15} cm^{-3}.

and that the mobility increases as we penetrate into the buffer layer. This is a very encouraging result.

Figure 4 shows the results of similar measurements made on two wafers both with a 0.2-μm-thick n-layer doped to 6.5×10^{16} cm^{-3}. These wafers were grown one after the other; one with a 1-μm buffer layer and the other without a buffer layer. Note the fairly good wafer without the buffer layer;

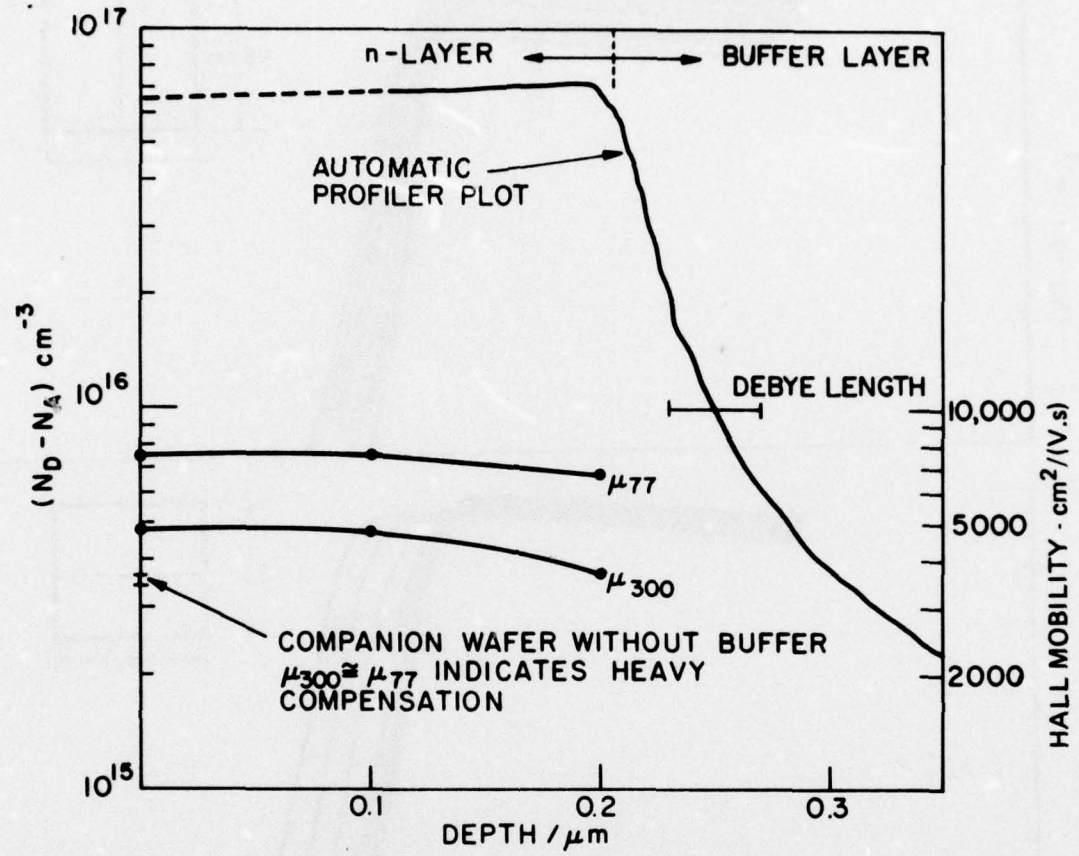


Figure 4. Carrier and mobility profile of a Reactor C wafer with a 1-μm buffer layer for an n-layer carrier concentration of 6.5×10^{16} cm^{-3}.

the value of μ is lower, and more significantly, $\mu_{300} \simeq \mu_{77}$ indicates heavy compensation. This experiment clearly shows the beneficial effect of using a buffer layer.

A series of experiments was carried out with BN mixing baffles upstream of the substrate in Reactor C. Figure 5 shows n vs x plots taken every 1 mm with 0.25-mm diameter Al Schottky barrier in two perpendicular directions across the wafer. Note that the thickness is uniform to within a Debye length. The uniformity from left-to-right is excellent if the three dots about 2 mm from the edges are neglected. The top-to-bottom uniformity is not as good. The substrate was held almost perpendicular to the gas stream. In Fig. 5, the direction of gas flow is into the paper.

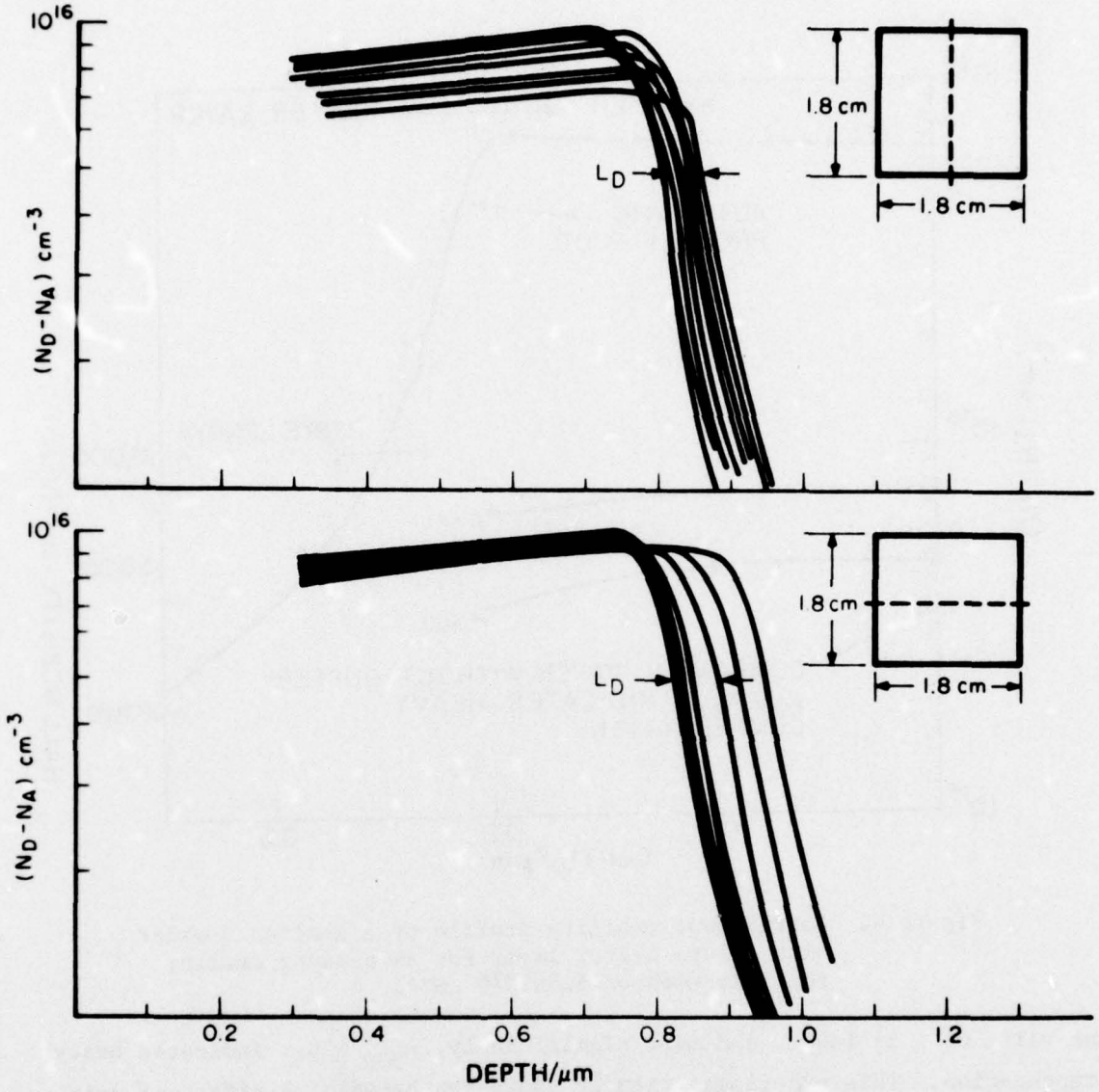


Figure 5. Doping uniformity across the wafer.

Table 3 summarizes the results of the test wafers with buffer layer thicknesses of 1, 2, 4 and 6 μm. These results indicate that when a buffer layer of more than 1 or 2 μm is grown, part of the buffer layer is conducting. This is indicated by the anomalously high electron mobility. Observe that increasing the buffer layer thickness from 1 to 2 μm increases the average mobility from 4165 $cm^2/V \cdot s$ to 4410 $cm^2/V \cdot s$.

TABLE 3. RESULTS OF TEST WAFERS

Wafer No.	$T(n^+)$ μm	T(n) μm	T(buffer) μm	n(300 K) cm^{-3}	n(77 K) cm^{-3}	μ(300 K) $cm^2/(V.s)$	μ(77 K) $cm^2/(V.s)$
C171	0	0.3	1	$5.36x10^{16}$	$4.48x10^{16}$	4165	7793
C172	0	0.3	2	$5.0x10^{16}$	$3.44x10^{16}$	4410	13750
C173	0	0.3	4	$5.0x10^{16}$	$3.57x10^{16}$	5209	31205
C174	0	0.3	6	$5.26x10^{16}$	$3.84x10^{16}$	5799	38750
C175	0.1	0.4 (1.0)	2	$1.8x10^{17}$	$3.43x10^{16}$	4415	37142

Figure 6 shows the n(x) profile for C171 (1-μm buffer layer) measured using a JAC profiler. The n-values agree reasonably with the van der Pauw measurement as shown in Table 3. Figure 7 shows the n(x) profile for C173 (4-μm buffer). Note that the buffer layer close to the active layer is doped to $2x10^{15}$ cm^{-3}.

The n^+ layer carrier concentration of the Reactor C wafer is somewhere between that of the old Reactor A and the Reactor B. When Ti/Pt/Au is deposited on the n^+ layer, the contact is somewhat rectifying and it is nonohmic.

The construction of the Reactor D ($AsCl_3$ system) was completed near the end of this report period. No wafer has been grown yet from the Reactor D.

C. DEVICE DEVELOPMENT

During this six-month period, a new FET type, which was specifically designed for the 0.5-W power level, has been successfully developed. This new device design incorporates 8 parallel gates, each being 150 μm wide and approximately 1.0 μm long, in a configuration as shown in Fig. 8. At 10 GHz, some 8G FETs tested to date have achieved power output levels greater than the 0.5-W level design goal. For example, one unit has generated 0.68 W with an associated gain of 4.8 dB and a power-added efficiency of 31.8%.

The device development effort in this report was concentrated on the development of AuGe ohmic contact technology compatible to self-aligned gate technique and in the evaluation of the Reactor C wafers.

In order to obtain low resistance ohmic contacts from the Ti/Pt/Au metallization, the doping level of the n^+ layers have to be in the $4-6x10^{18}$ cm^{-3} range. This high doping density is very close to the upper limit that can be

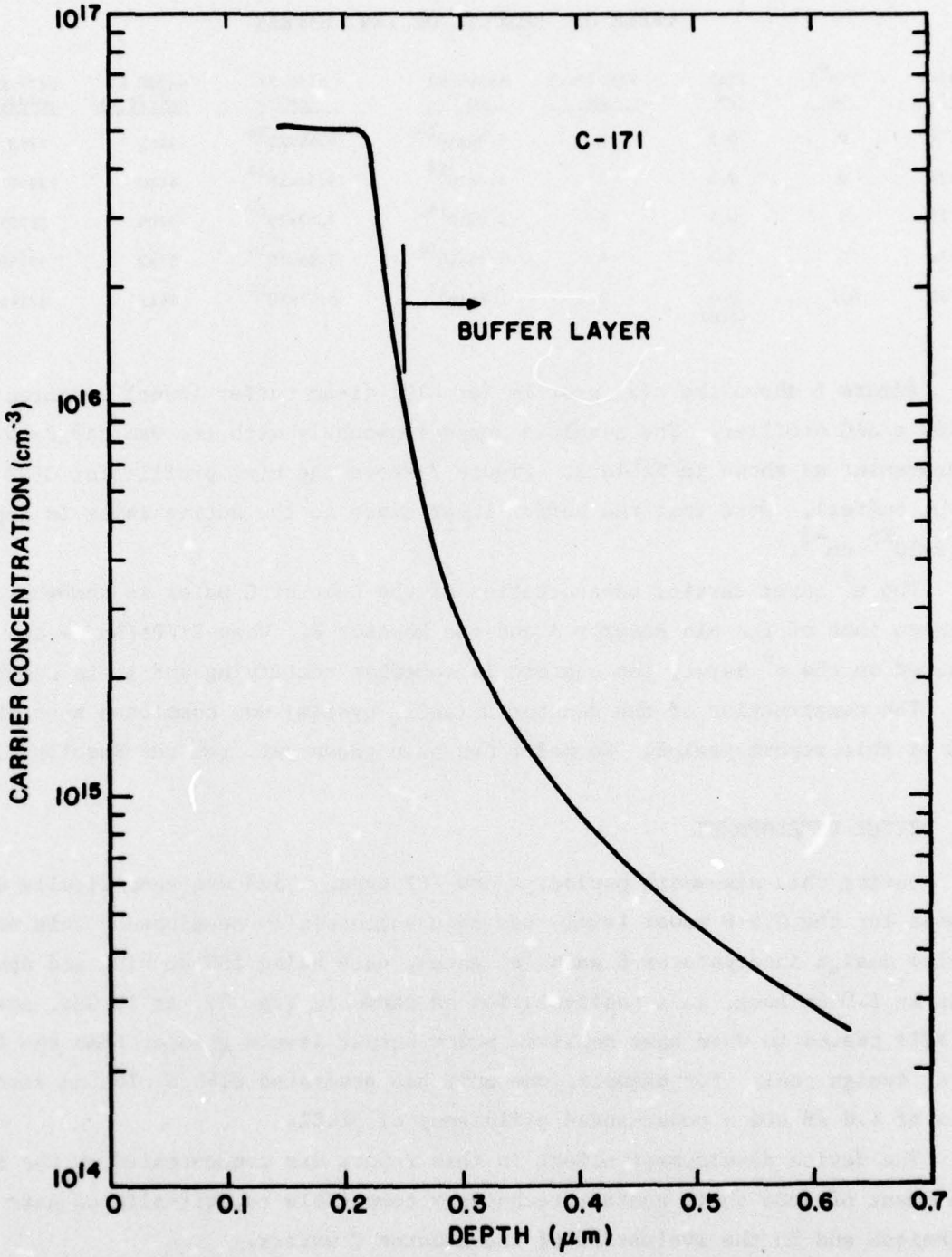


Figure 6. Growth adjusted for 1-μm buffer and 0.3-μm n-layer with no anomaly.

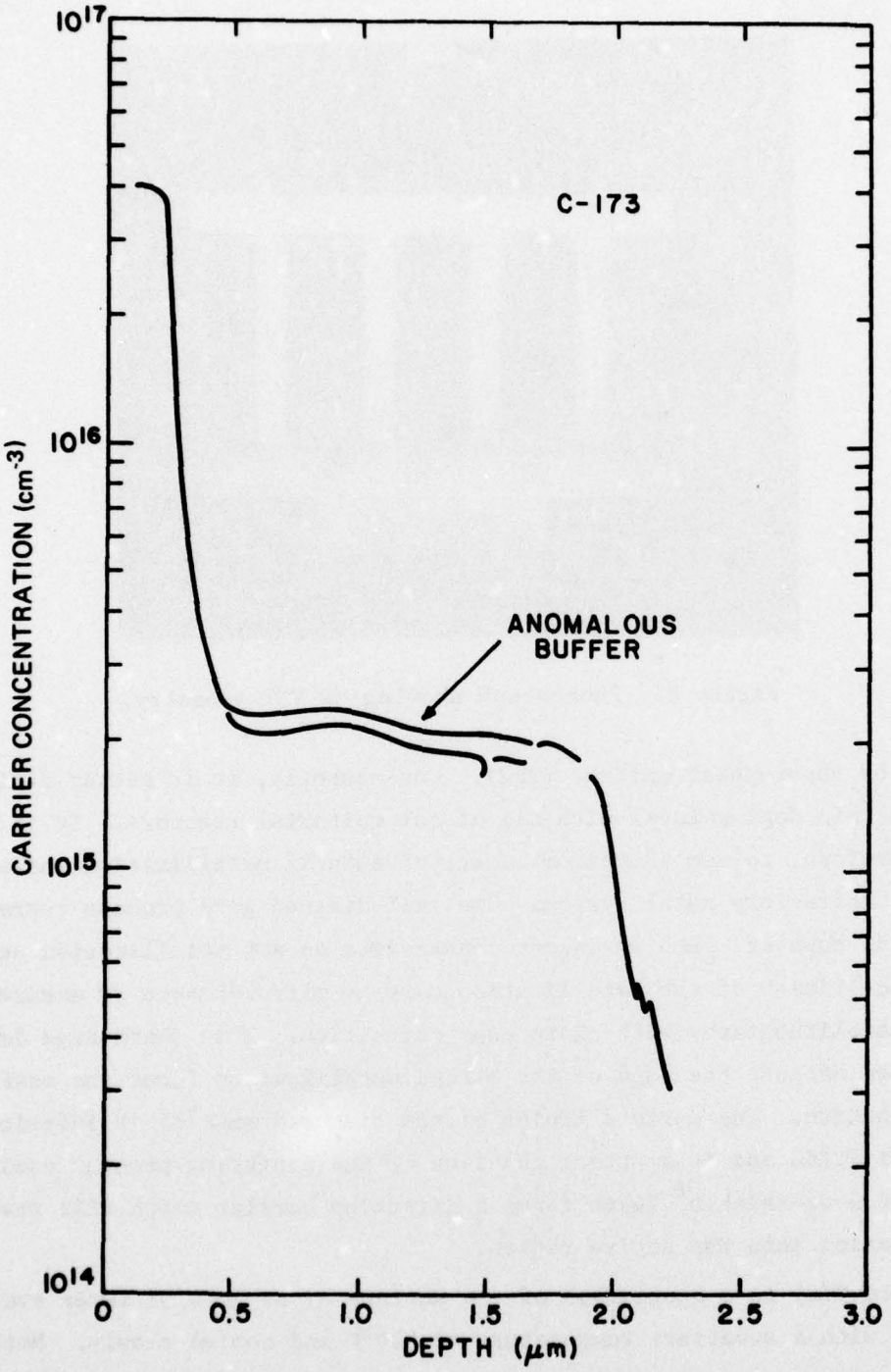


Figure 7. Growth adjusted for 4-μm buffer and 0.3-μm active layer. Note anomalous 2×10^{15} cm^{-3} doped layer.

Figure 8. Photograph showing 8G FET geometry.

achieved by vapor-phase epitaxy (VPE). Consequently, it is rather difficult to obtain this doping level with all of our epitaxial reactors. It is desirable, therefore, to use a minimum amount of AuGe/Ni metallization and overlay it with a refractory metal system. The self-aligned gate process currently being used, however, puts stringent constraints on any metallization used. The surface finish of the metallization must be mirror-smooth to ensure submicron photolithography with sharp edge definition. This sharp edge definition is required because the edge of the etched metallization forms the mask for gate definition. The surface finish of the sintered AuGe/Ni is inferior to that of Ti/Pt/Au and is a strong function of the sintering process used. Note that the 0.5-μm-thick n^+ layer forms a diffusion barrier which will prevent Au penetration into the active region.

Figure 9(a) is a photograph of the surface of an AuGe/Ni layer evaporated in vacuum with a substrate temperature of 450°C and cooled slowly. Note large grain structures several micrometers in size. This surface finish is obviously unsuitable. Figure 9(b) shows an AuGe/Ni film deposited at 90°C and sintered in H_2 followed by rapid cooling. The surface finish is much better and is compatible to the requirement for the gate definition.

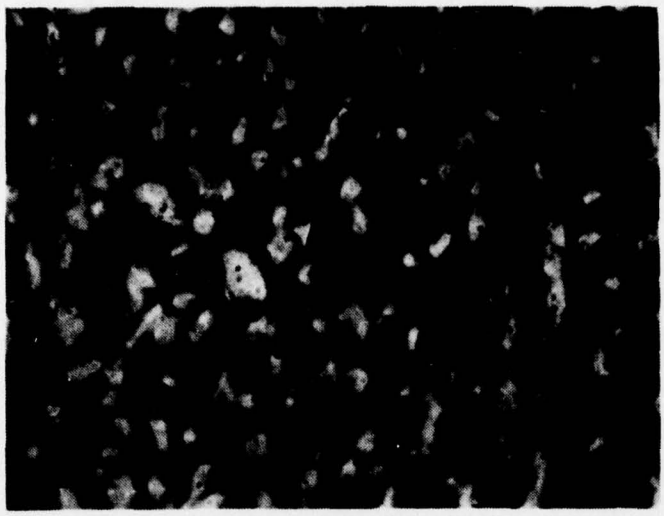


Figure 9(a). Surface finish of AuGe/Ni ohmic contact, evaporated at 450°C, and slow cooling in the vacuum system. Magnification: 1000X.

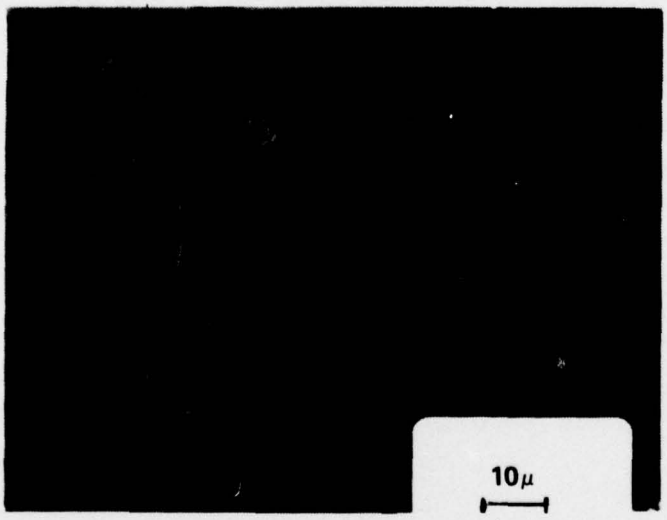


Figure 9(b). Surface finish of AuGe/Ni ohmic contact, evaporated at 90°C, sintered in a separate furnace, and fast cooling. Magnification: 1000X.

The AuGe/Ni ohmic contact is now being gradually incorporated in the normal FET processing. Although we will still process a few wafers using Ti/Pt/Au ohmic contact for comparison purposes, most of the subsequent wafers will have Ni/AuGe/Ni/Ti/Pt/Au ohmic contact. Figure 10 indicates the I-V characteristics of a wafer B787. One half of the wafer had AuGe/Ni ohmic contact. The other half had Ti/Pt/Au ohmic contact. The low field resistance of the Ti/Pt/Au contact is almost twice that of the AuGe/Ni contact for this particular case.

Two wafers left over from the original Reactor A were processed for 8G FETs. Wafer 3149 had Au-Ge ohmic contact and wafer 3191 had Ti/Pt/Au ohmic contact. The reason we chose both wafers from the original Reactor A was to establish a base line for AuGe/Ni ohmic contact. The n^+ layers grown in Reactor A have consistently yielded better ohmic contact than wafers from other reactors when Ti/Pt/Au was used. Thus, the above experiment would reveal possible problems associated with AuGe/Ni ohmic contact.

The small signal gain of 3149 was about 6 dB with 540 mW at the 1-dB compression point with 26% power-added efficiency at 10 GHz. The small-signal gain of 3191 FETs was about 5.5 dB with 500 mW output power at the 4-dB gain point and about 10 to 20% power-added efficiency at 10 GHz. Thus, the rf performance of both wafers is nearly comparable.

Performance of 8G FETs from Reactor C wafers is about 4- to 5-dB gain at 10 GHz with 0.5-W output power. Table 4 shows the current status of RCA power FETs to provide a bench mark.

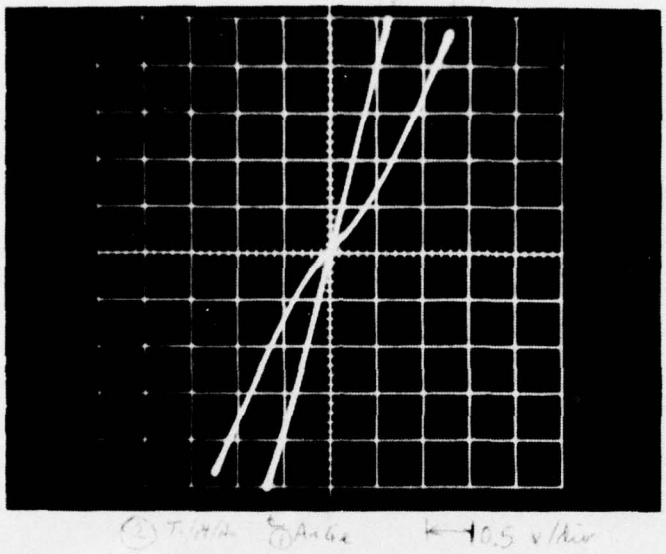


Figure 10. I-V characteristic of AuGe contact vs Ti/Pt/Au contact on Wafer B787. Curve 1 is AuGe contact.

TABLE 4. CURRENT STATUS OF RCA's GaAs POWER FET

Frequency (GHz)	Linear Gain (dB)	Output Power (W)	Gain at P_{out} (dB)	Power-Added Efficiency (%)	Source Periphery
4	5.3	4.1	3.4	12.6	48G (9.6 mm)
4	6.5	3.0	4.7	32	48G (9.6 mm)
8	5.0	1.8	3.3	14	32G (4.8 mm)
8	7.0	0.7	6.0	33	8G (1.2 mm)
10	6.0	0.68	4.8	31.8	8G (1.2 mm)
10	6.6	1.2	5.3	22.2	16G (2.4 mm)
15	4.6	0.77	3.7	9.6	16G (2.4 mm)
15	4.0	0.50	3.0	25	Two 4G (1.2 mm)

SECTION III

AMPLIFIER DEVELOPMENT

A. OVERALL AMPLIFIER APPROACH

The overall amplifier configuration proposed to satisfy the program design goals consists of a cascade of five balanced amplifier stages as discussed in Section I and shown in Fig. 1. The RCA device types which have been available for amplifier circuits during this six-month period are the 4G, 8G, and 16G varieties.

B. DEVICE CHARACTERIZATION

Once a FET has been fabricated, mounted, and has passed dc testing, it is given two different rf tests. The FET, which is flip-chip mounted onto an open carrier as shown in Fig. 11, is assembled between two 50-ohm microstrip lines and two SMA connectors on an open block. Tuning chips are then placed on the microstrip lines, and the locations of these chips are changed to achieve a maximum power output for a given input power. This test gives the small-

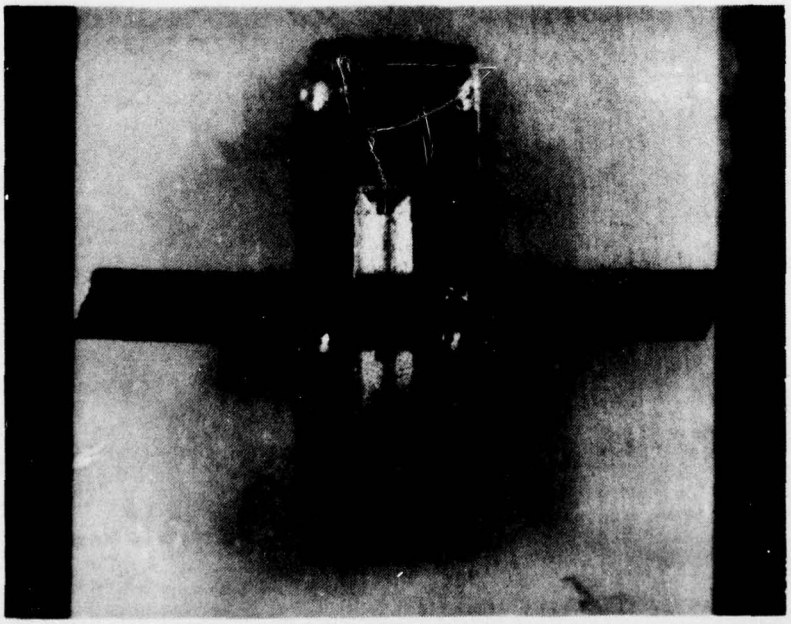


Figure 11. Flip-chip mounted FET on a carrier.

signal gain, the saturated power output, the associated gain and power-added efficiency, and the drain current at the frequency of operation. Table 5 shows data typical of that taken during this test.

The S-parameters of the FET are then measured by remounting the device into a microstrip structure, which, when covered, is in a waveguide below cutoff configuration. This configuration uses very short lengths (5.33 mm long) of microstrip line, and minimizes the effects of dispersion, radiation, and unwanted waveguide modes of propagation. S-parameter data taken in this fixture are very uniform and free of resonant loops up to frequencies greater than 10 GHz when using 0.64-mm-thick alumina substrates. Representative data for the various devices used during the past six months will be shown in the following subsections.

Presently, the open fixture used for the chip-tuned power evaluation test uses rather long microstrip lines, about 12.5 mm long, without any mode suppression packaging. S-parameters measured with this package are not uniform,

TABLE 5. RCA MESFET EVALUATION SHEET

DEVICE: 3172A-9 8G CG

V_D = 10 V, I_{DSSO} = 442 mA, V_G = -2 V, f = 10 GHz

V_{SAT} = 2.5 V, G_M = 62 mmho, V_B = _____ V at 1 mA

P_i	P_{in}(mW)	P_o	P_{out}(mW)	G(dB)	I_D(mA)	$P_{out}-P_{in}$(mW)	η_{PA}(%)
50	45	160	214.4	6.78	329	169.4	5.1
100	90	295	395.3	6.427	334	305.3	9.1
200	180	520	696.8	5.878	338	516.8	15.2
300	270	610	817.4	4.810	322	547.4	17.0
400	360	655	877.7	3.870	309	517.7	16.75
500	450	670	897.8	2.99	303	447.8	14.77
600	540	680	911.2	2.272	301	371.2	12.37

show resonant loops, and as such cannot be used for accurate circuit design. These S-parameters are useful for comparative rough evaluations of devices.

The shorter waveguide below cutoff fixture used for accurate S-parameter measurement, is not suited to power testing. The chips used in power testing are conductive, and cannot be permitted to contact grounded metal. Even a momentary short-circuiting to ground of either drain or gate will destroy the FET. The side walls of the waveguide below cutoff test fixture present such a hazard. The shorter length of these fixtures do not always allow tuning chips to be placed at the optimum locations.

An attempt has been made to develop a single test fixture which will permit both rf tests to be done, thereby eliminating the need to transfer the FET between fixtures. This new fixture has a U-shaped cover designed so the that when the cover is attached to the fixture, a waveguide below cutoff enclosure is established which is suitable for accurate S-parameter measurements; and when the cover is removed, an open configuration suitable for safe power chip tuning of the FET exists. So far it has been found that although more accurate S-parameters are obtained with this structure than the open structure, resonant loops occur which limit the value of the measured parameters for circuit design.

When S-parameters are measured on a computer-controlled automatic network analyzer, the computer can also print out the calculated values of the small-signal maximum available gain (MAG) and the Rollet stability factor (K). With the Dexcel, 4G, and 8G devices, good correlation between the maximum available gain and the small-signal gain measured during power testing usually occurs. When testing the higher power 16G devices, the predicted gain is sometimes several dB lower than the measured gain. Two approaches are being pursued to determine the causes of this discrepancy. It is presently felt that either the measured S-parameters are not accurate enough for these devices, or some type of feedback occurs during chip testing which enhances the gain of the FET.

The S_{11} of a typical 16G FET is about 0.85, which corresponds to a mismatch loss of about 5.7 dB. Such high values of S_{11} are difficult to measure accurately. If an error of $\pm$ 0.05 occurs in the measurement of the input reflection coefficient, the value of the input mismatch loss and, hence, the calculated device gain can be in error by about $\pm$ 1.5 dB. One possible way of achieving more accurate S-parameter measurements is to incorporate a

simple impedance transformer into the characterization test fixture. This will transform the reflection coefficients to lower values which can be more accurately measured on the network analyzer. Because MAG and stability factors are not changed by lossless matching networks these parameters can be calculated at the time of measurement. Subsequent computer calculations can then be used to remove the transformation caused by these networks and generate the S-parameters of the FET which need to be known for accurate circuit design.

The effects of single in-line transformer sections on the values of S_{11} and S_{22} are illustrated on the Smith chart plots in Fig. 12. For this example, a typical 8G device has been selected and its S-parameters shown by the single points in Fig. 12. The value of S_{22} is close enough to the real axis that a quarter wavelength transformer will result in transformed impedances which are also close to the real axis. S_{11} is inductive, so that a transformer which is about one-sixth of a wavelength long, is needed to transform to impedances near the real axis. Figure 12 shows the effects of the impedance transformers when the characteristic impedance of each is allowed to vary. It can be seen that as lower impedance lines are used, both reflection coefficients are closer to the origin of the Smith chart. It is felt that with 25-mil-thick alumina substrates, the lowest practical characteristic impedance for the transformer sections is about 25 ohms. When lower impedance levels are used, the transformers would become greater than one-quarter wavelength wide in the 9-to 10-GHz frequency range, and would likely radiate or support other than the desired quasi-TEM mode of microstrip line. The use of partial impedance matching during device characterization will be investigated in the next six-month period.

When a power FET is characterized by chip tuning, it is conceivable that the chips are introducing effects other than that of transmission-line type matching network elements. The very close proximity of the chips to the FET pellet in the case of the 16G devices suggests that coupling effects might possibly exist between the output and input matching networks, and between each matching network and the FET pellet itself. As first approximation, it can be assumed that a feedback capacitance exists between the output and input matching networks. A 16G FET has been selected for an example in a

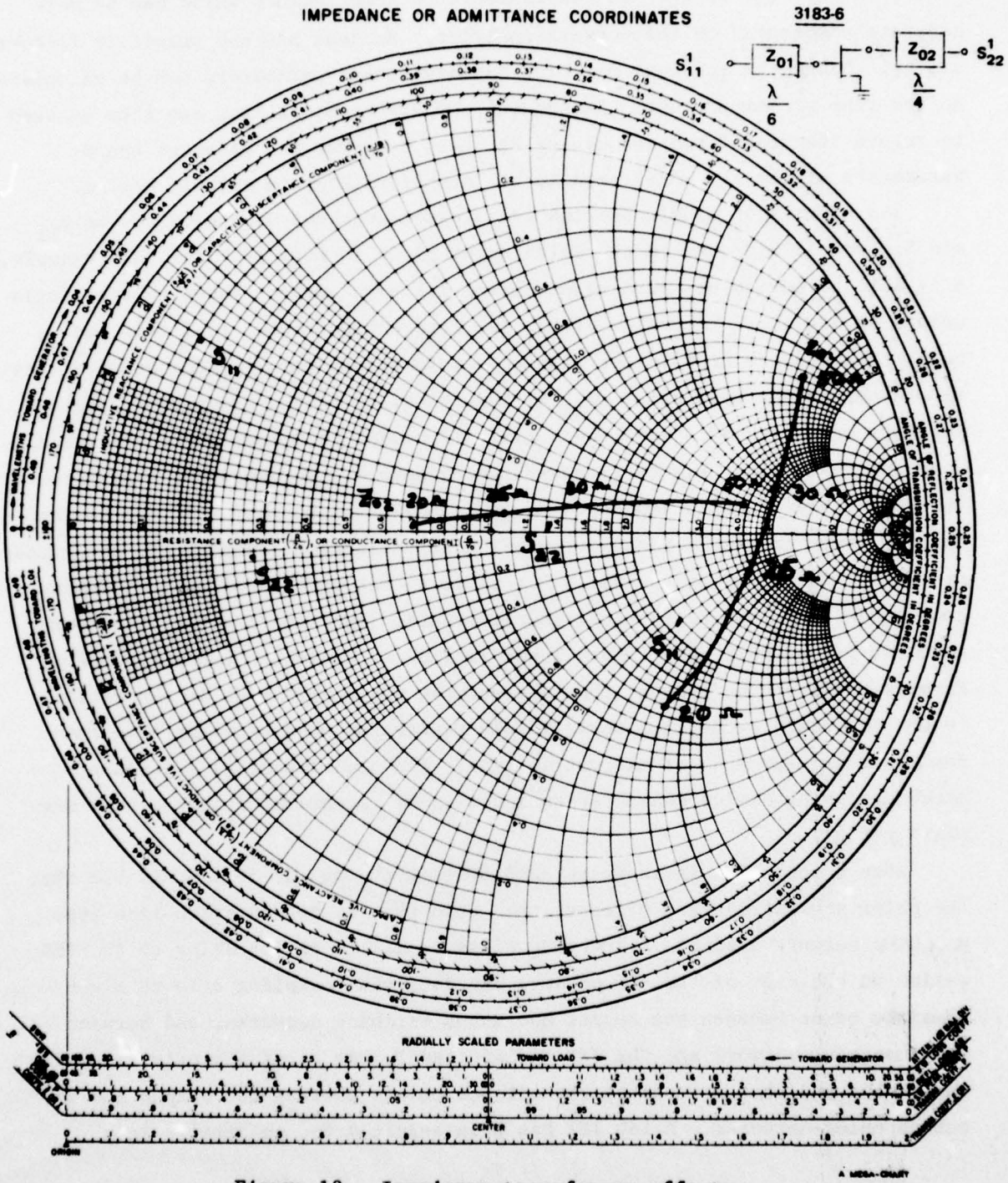


Figure 12. Impedance transformer effects.

computer circuit which places a capacitor between drain and gate. The calculated values of stability factor (K) and maximum available gain (MAG) are shown in Fig. 13. It can be seen that as the feedback capacitance increases to about 0.23 pF in this example, the value of K decreases, and the MAG increases by about 3 dB. Additional increases to feedback capacity cause K to become less than unity causing the MAG to become undefined. During these calculations, it has been noticed that the only S-parameter to be strongly influenced by the feedback capacity is S_{11}. Unfortunately, as this feedback is increased, the magnitude of S_{11} also increases, as shown in the lower portion of Fig. 13. This would make the achievement of a broadband matching network more difficult.

The results of further analytical studies of the possible effects of capacitive feedback will be given in the subsection describing the amplifier performance achieved with 16G devices.

C. AMPLIFIER LAYOUT AND MECHANICAL CONSIDERATIONS

The projected layout of the completed amplifier module is shown in Fig. 2. A cross section of the proposed layout is given in Fig. 14. The prime criterion in designing this layout is to minimize wasted areas in the rf circuitry so that the resulting amplifier will be small. Each amplifier stage and coupler is on a separate carrier permitting each unit to be separately measured and trimmed, as needed. Repair and replacement of defective components is facilitated by this arrangement. Each carrier is then bolted into the main chassis and placed in a small recess at the top. A larger recess on the lower portion of the chassis is reserved for bias and pulse modulation circuitry. When two amplifiers are used in a balanced amplifier stage, a shielding partition is placed between them to minimize extraneous coupling between amplifiers and to establish a waveguide below cutoff enclosure for each amplifier stage. Wires carrying the bias and pulse modulation voltages from the larger recess to the smaller recess with the rf components will pass through holes provided on either side of the mounted FET carrier. New interdigitated couplers are being designed on a small substrate of 1.78 cm x 0.51 cm area with a 1.02-cm spacing between inputs. It is anticipated that the dimensions of the overall module, excluding connectors and heat sinks, will be 14 x 3.2 x 3.3 cm.

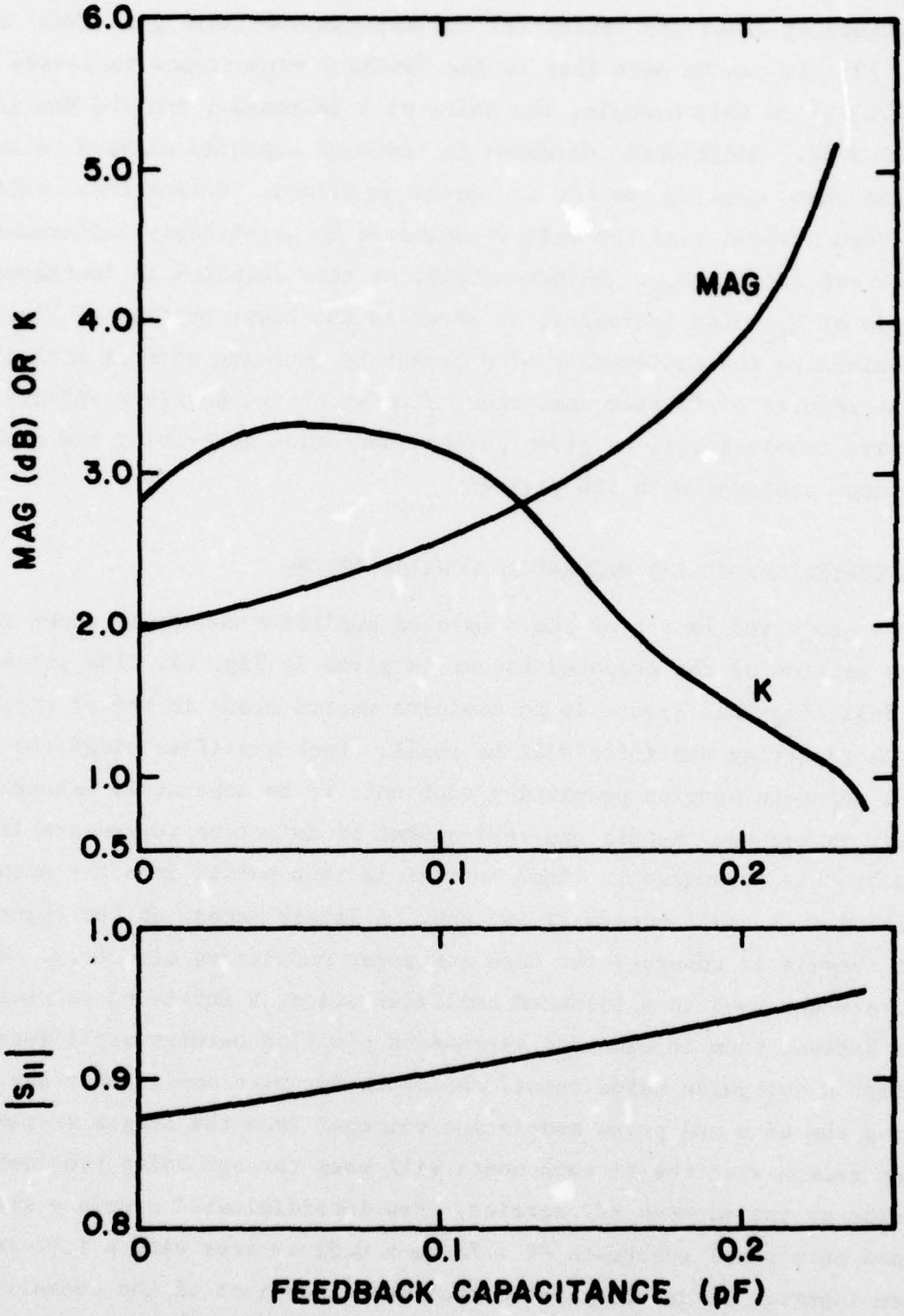


Figure 13. Effects of feedback capacitance.

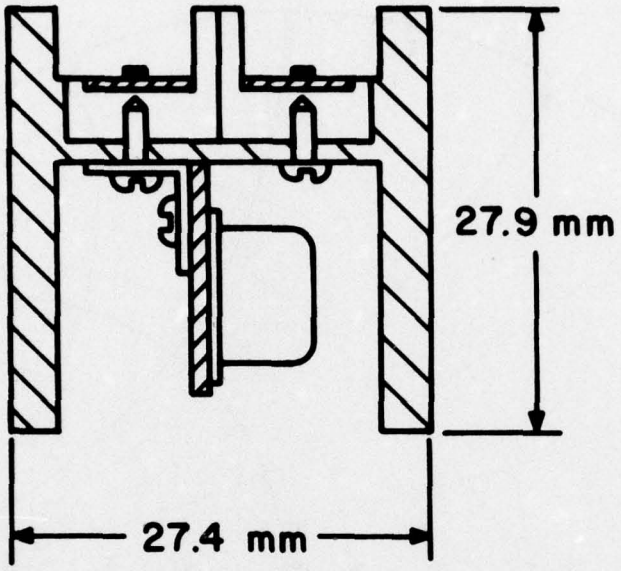


Figure 14. Cross-sectional view of complete amplifier assembly.

D. MEASURED FET PARAMETERS

The design of a FET amplifier stage begins with a measurement of the small-signal S-parameters on an automatic network analyzer using the waveguide below the cutoff test fixture described previously in Section III.B.

The measured values of S_{11} and S_{22} can now be plotted by an in-house computer program directly onto a Smith Chart. This type of plot is shown in Figs. 15(a) and 15(b) for the DXL-3501A FET chip. Such plots show the input and output impedance values which are used to determine the initial circuit designs.

When the network analyzer computer prints the S-parameters of the FET, it can also calculate and print various amplifier parameters. Among these parameters are the stability factor (K) and the maximum available gain (MAG) for those cases in which K is greater than unity. The initial circuit designs are optimized by computer to try to achieve a gain equal to the MAG.

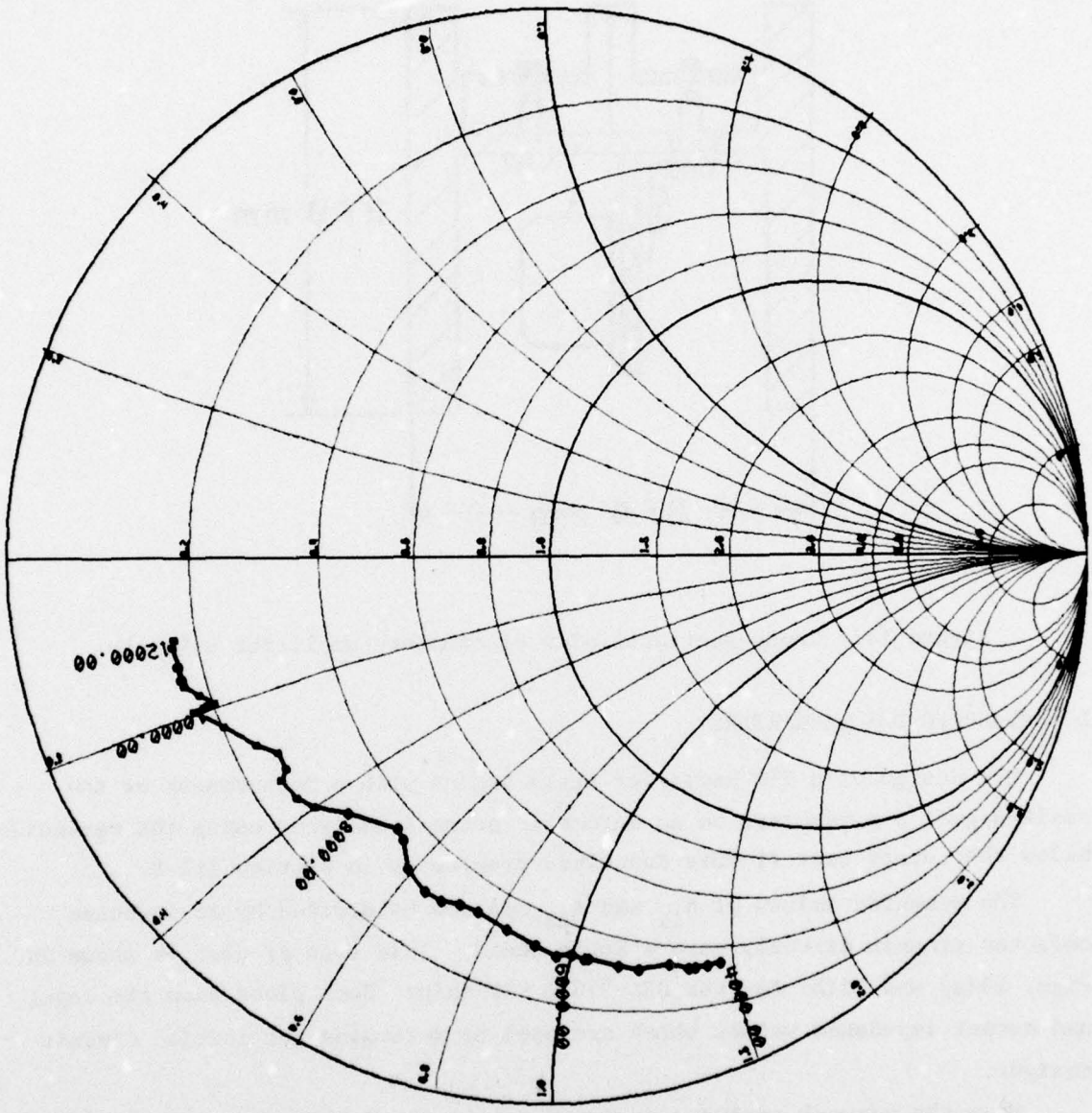


Figure 15. (a) S_{11} of DXL-3501A FET chip.

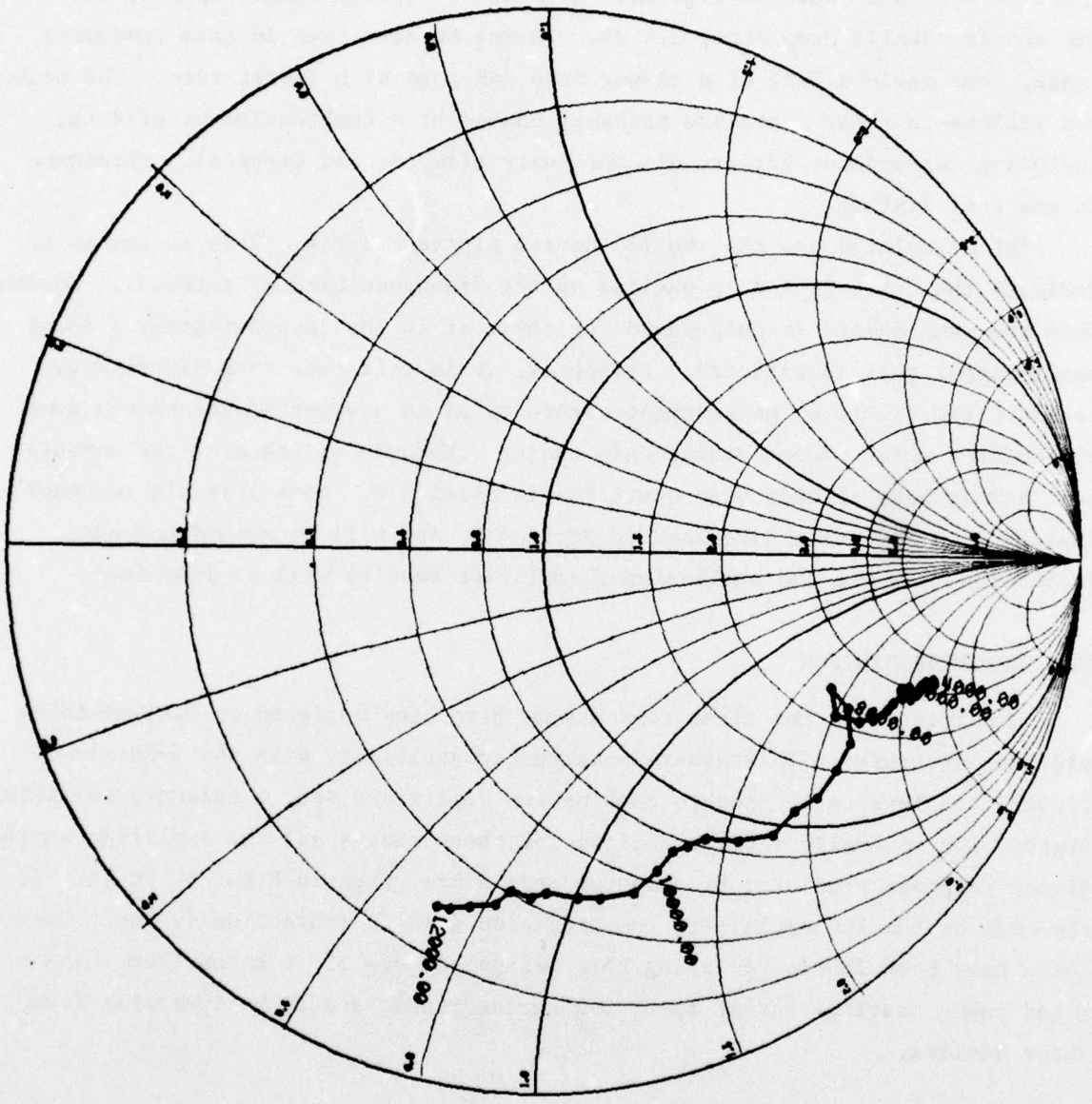


Figure 15. (b) S_{22} of DXL-3501A FET chip.

The input and output reflection coefficients for the various FET types tested during this six-month program are plotted in Figs. 15 to 18. The respective MAGs are shown in Fig. 19. Over the frequency range plotted, the MAG should ideally drop about 2.4 dB. It can be seen that in this frequency range, some devices fall at a slower rate and some at a faster rate. The peaks and valleys in these plots are probably caused by a combination of effects, including measurement errors, discontinuity effects, and dispersion phenomena in the test fixture.

The calculated MAG for the 16G device plotted in Fig. 19 is so low as to indicate that this device is useless in the frequency band of interest. However, when the same device is chip-tuned for power at 10 GHz, approximately 4 dB of small-signal gain is achieved. Presently, it is felt that this discrepancy could be the result of measurement errors or of an unexpected phenomenon such as feedback which occurs during chip tuning. Methods of reducing the measurement errors have already been described in Section B. Some possible feedback explanations have been discussed in Section B, and will be considered again in Section F, where the small-signal amplifier results will be discussed.

E. AMPLIFIER DESIGNS

Amplifiers for the first four stages have been designed on 0.64-mm-thick alumina substrates. This assures maximum compatibility with the 3-dB directional couplers to be used to combine two amplifiers into a balanced amplifier stage. The schematic representations for these stages and the amplifier small-signal response predicted by computer models are given in Figs. 20 to 23. In the case of the 16G amplifier, the predicted gain is impractically low. Circuits have been fabricated using this design because it is known from chip-tuned power testing that at least 3-dB greater gain should be available from these devices.

F. SMALL-SIGNAL RESULTS

The circuits required for the first four stages have been fabricated and tested. A minimum number of wire bonds have been used. These bonds are required for attachment to the DXL-3501A chip, and are also used to provide

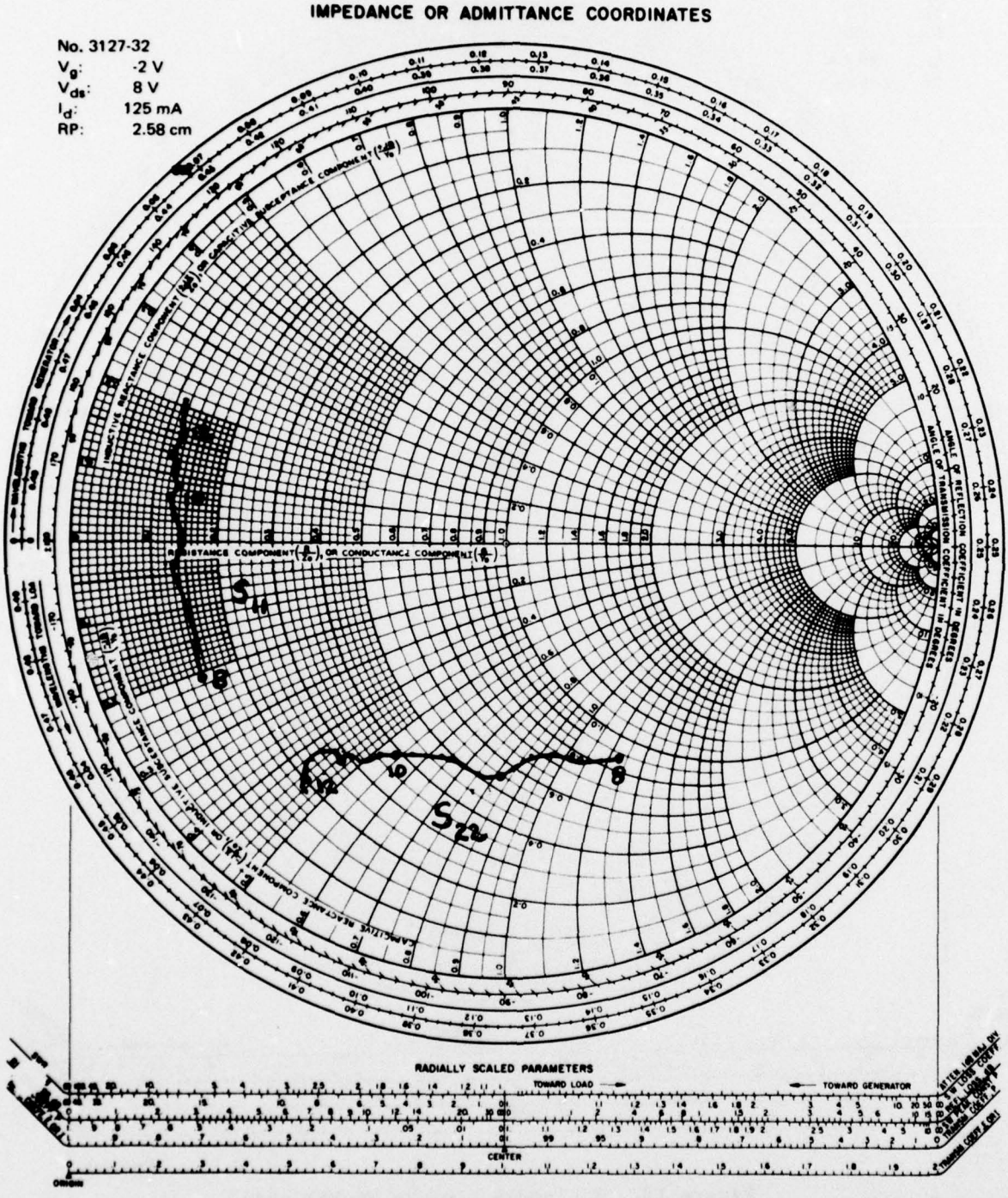


Figure 16. S_{11} and S_{22} of a 4G FET chip.

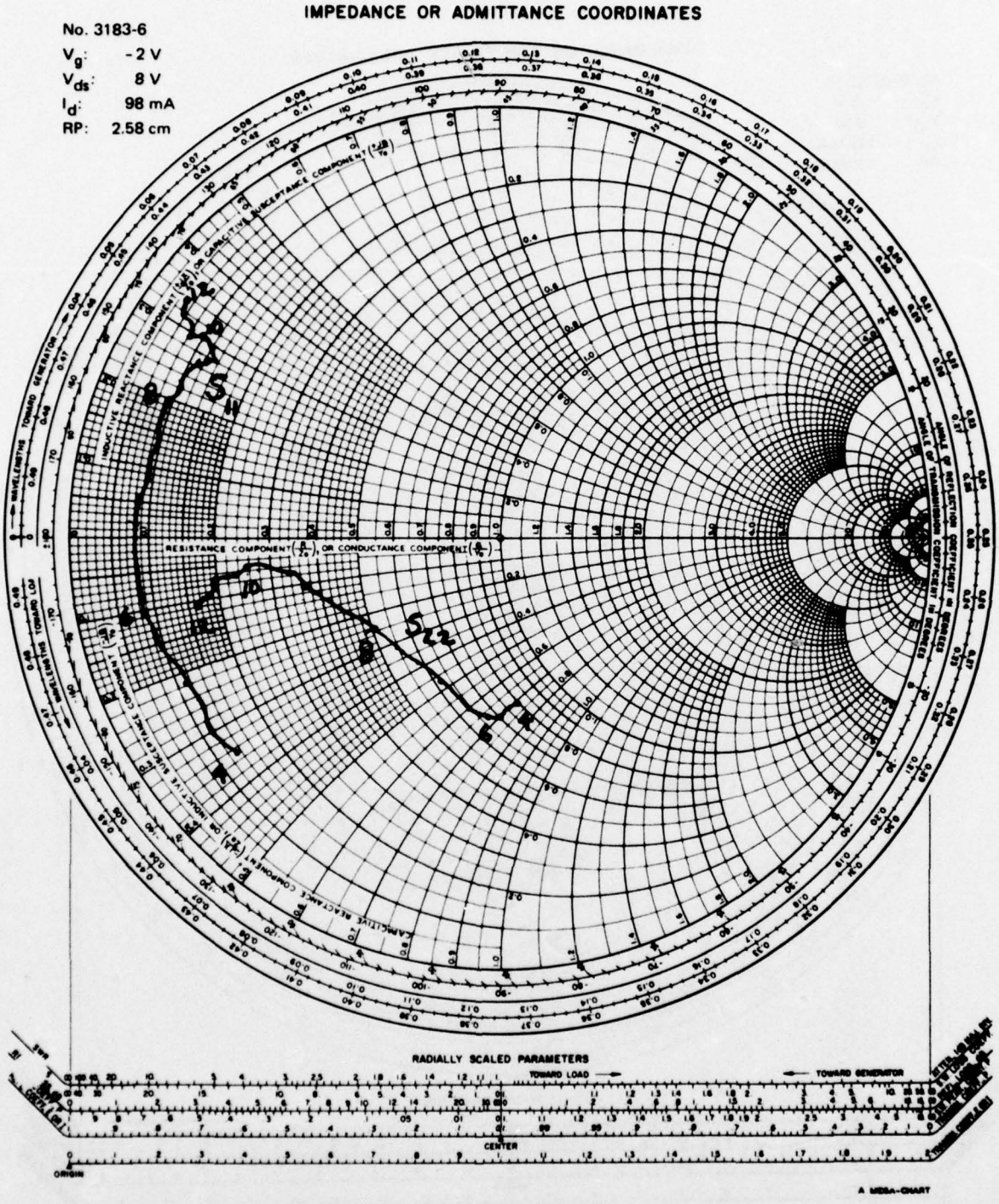


Figure 17. S_{11} and S_{22} of an 8G FET chip.

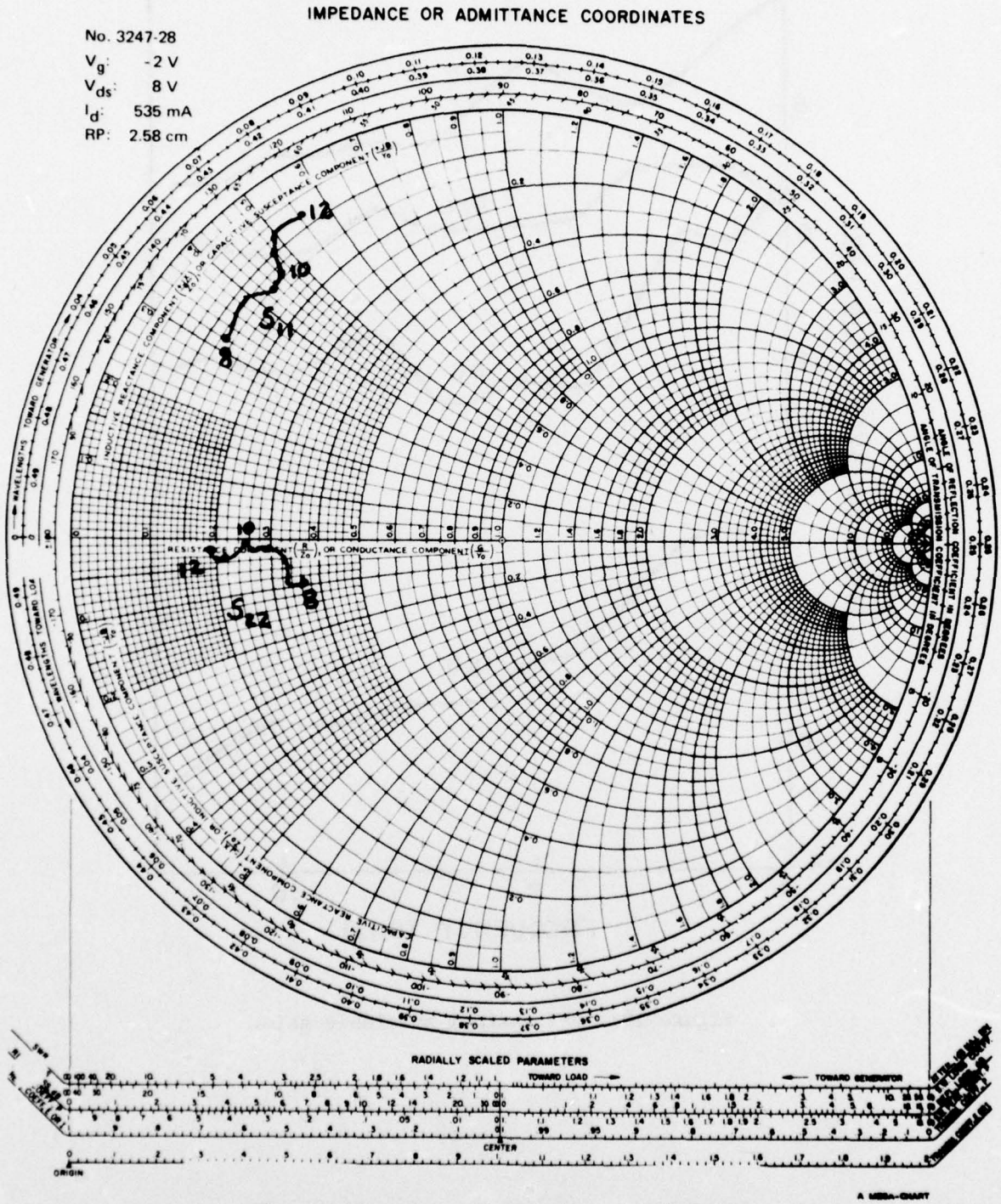


Figure 18. S_{11} and S_{22} of a 16G FET chip.

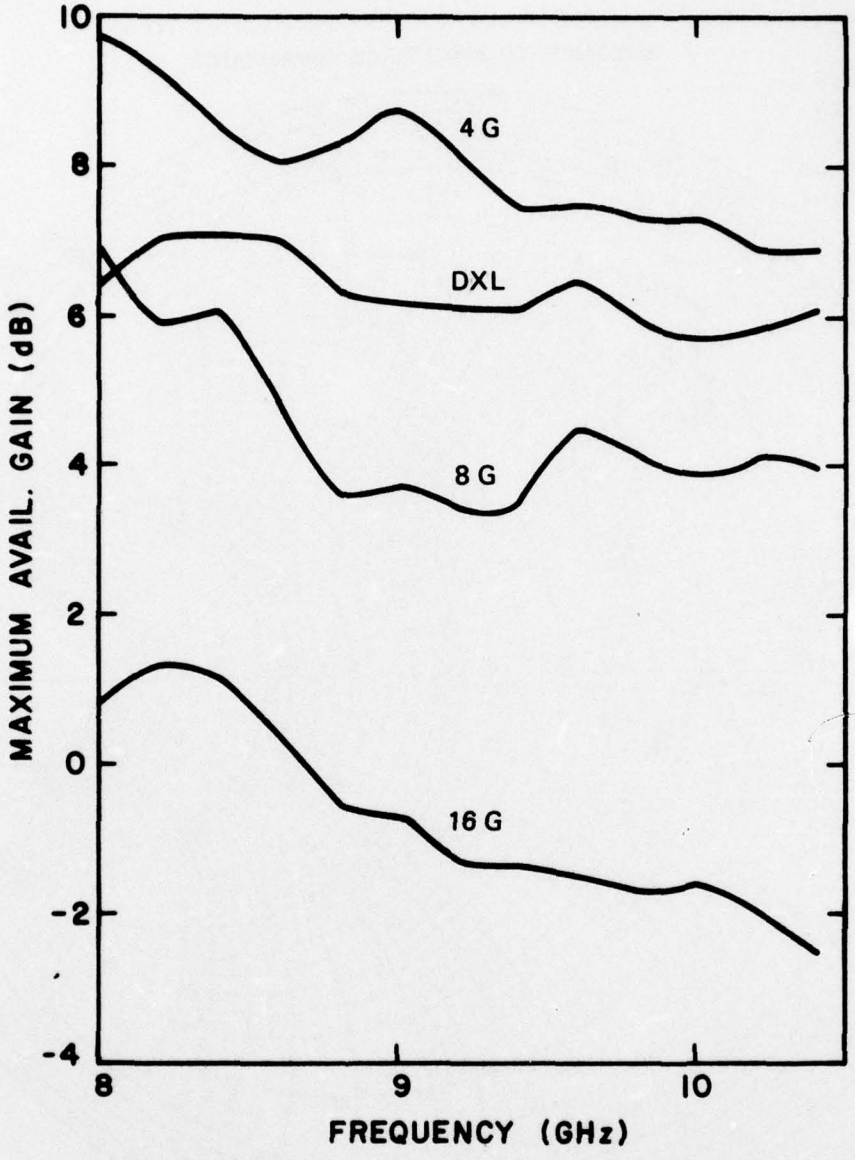
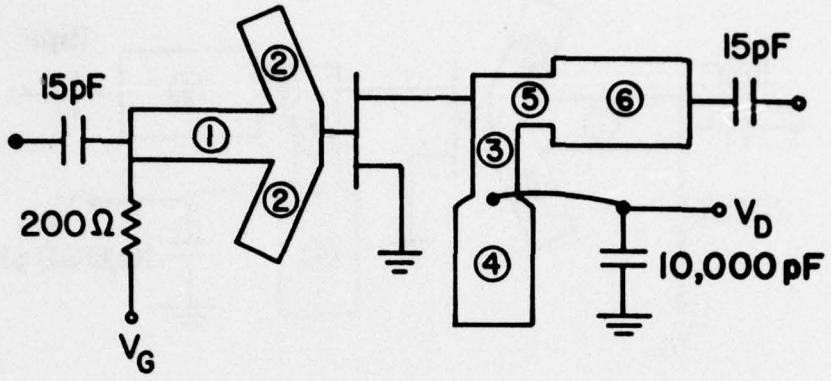


Figure 19. FET maximum available gain.

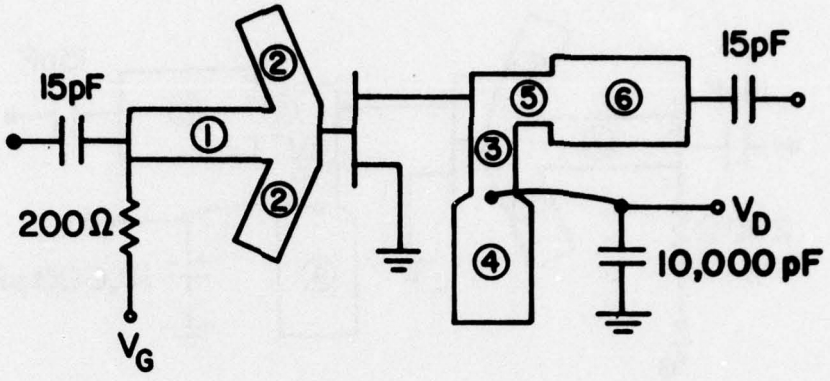


LINE #	LENGTH	WIDTH
1	145	75
2	86	16
3	76	5
4	117	50
5	90	10
6	53	23
Gate Induct.	0.44nH	

COSMIC(RTE) RUN: 8/22/77
DATA FILE: $.RLE4: DXL3501A, -1V, 42 MA @ 8V.
ANALYSIS ONLY!...

FREQ	FGAIN PH		FLATNESS		S11,I.RC		S22,0.RC	
	X	1.000DB	X	1.000DB	X	1.000*	X	1.000*
8.800	8.542	-159.63	0.000	0.00	0.326	-51.95	0.531	-137.93
9.000	8.706	-176.57	0.164	0.16	0.294	-79.14	0.458	-153.79
9.200	8.660	167.24	0.164	-0.05	0.253	-99.00	0.386	-172.89
9.400	8.506	150.54	0.201	-0.15	0.211	-122.69	0.319	163.84
9.600	9.025	133.36	0.519	0.52	0.254	-148.78	0.309	132.15
9.800	8.815	116.97	0.519	-0.21	0.213	-168.63	0.290	100.62
10.000	8.778	95.94	0.519	-0.04	0.205	150.24	0.323	67.76
10.200	8.145	76.32	0.880	-0.63	0.167	95.02	0.387	42.42

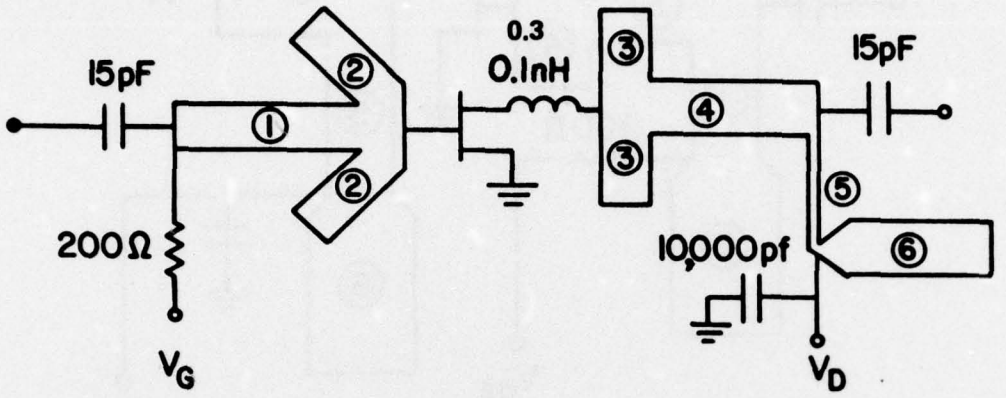
Figure 20. Amplifier design and predicted performance using a DXL-3501A FET.



LINE #	LENGTH	WIDTH
1	133	75
2	70	40
3	30	6
4	117	50
5	30	30
6	80	40

FREQ	FGAIN PH		FLATNESS		S11,I.RC		S22,0.RC	
	X	1.000DB	X	1.000DB	X	1.000*	X	1.000*
8.800	6.405	-126.72	0.000	0.00	0.308	-82.40	0.641	-85.33
9.000	6.651	-142.04	0.247	0.25	0.319	-104.44	0.582	-98.65
9.200	6.721	-156.61	0.316	0.07	0.320	-124.20	0.504	-113.22
9.400	6.951	-175.47	0.546	0.23	0.376	-153.39	0.418	-126.66
9.600	7.205	168.65	0.801	0.25	0.438	-173.61	0.361	-143.53
9.800	6.704	155.17	0.801	-0.50	0.379	166.78	0.303	-160.11
10.000	6.405	140.45	0.801	-0.30	0.360	147.29	0.255	-177.96
10.200	6.052	128.05	1.153	-0.35	0.336	125.76	0.234	161.08

Figure 21. Amplifier design and predicted performance using a 4G-single-cell FET.



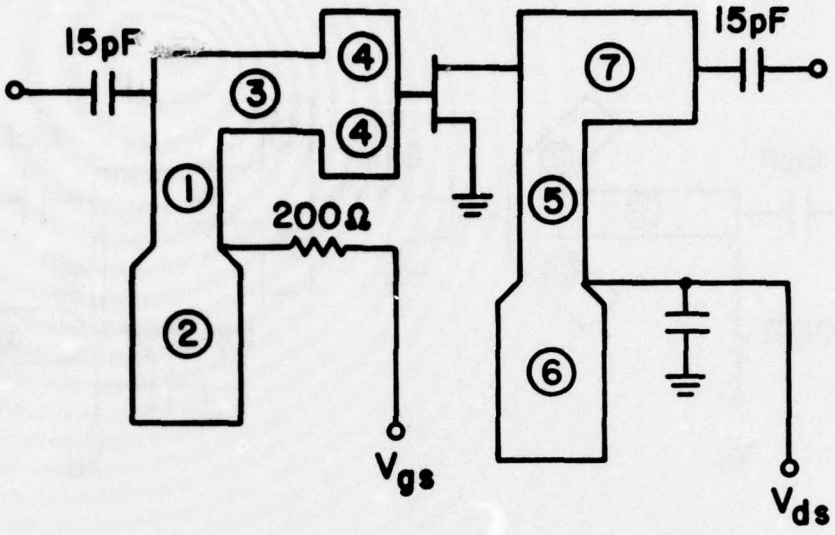
LINE #	LENGTH	WIDTH
1	-	50Ω
2	65	34
3	60	28
4	150	53
5	127	5
6	117	50

```
COSMIC(RTE) RUN:  9/14/77
DATA FILE:  $.RLE1, #3183-6,-2V,112 MA @ 8V
 ANALYSIS ONLY!...
```

FREQ	FGAIN PH		FLATNESS		S11,I.RC		S22,0.RC	
	X	1.000DB	X	1.000DB	X	1.000*	X	1.000*
8.800	5.988	172.36	0.000	0.00	0.680	103.65	0.141	-89.34
9.000	5.939	160.39	0.048	-0.05	0.585	94.25	0.193	-118.59
9.200	6.023	147.18	0.084	0.08	0.525	81.03	0.223	-143.16
9.400	6.297	133.78	0.357	0.27	0.533	63.63	0.255	-164.82
9.600	7.036	114.61	1.096	0.74	0.617	32.61	0.327	171.35
9.800	6.966	103.83	1.096	-0.07	0.586	19.89	0.347	162.83
10.000	5.698	84.17	1.338	-1.27	0.527	-15.68	0.286	140.10
10.200	4.956	73.44	2.079	-0.74	0.490	-32.07	0.253	126.77

```
NEXT?  (PAUSE):  *GO,??
```

Figure 22. Amplifier design and predicted performance using an 8G FET.



LINE #	LENGTH	WIDTH
1	50	5
2	117	50
3	159	20
4	65	35
5	95	13
6	117	50
7	120	75

```
COSMIC(RTE) RUN:  9/15/77
DATA FILE:  $.RLE2,#3147-27,-2V,545 MA @ 8V
 ANALYSIS ONLY!...
```

FREQ	FGAIN PH		I VSWR O		S11,I.RC		S22,O.RC	
	X	1.000DB	X	1.000	X	1.000*	X	1.000*
8.800	1.763	85.88	2.114	1.59	0.358	-142.05	0.228	80.50
9.000	2.013	71.25	1.766	1.32	0.277	-152.98	0.137	59.45
9.200	1.714	59.28	1.433	1.22	0.178	-158.70	0.098	42.33
9.400	1.828	48.80	1.412	1.13	0.171	-171.28	0.062	8.71
9.600	1.752	33.70	1.105	1.14	0.050	103.72	0.064	-13.41
9.800	1.488	18.53	1.265	1.17	0.117	15.29	0.078	-68.76
10.000	1.395	0.04	1.842	1.24	0.296	0.62	0.109	-102.37
10.200	0.375	-11.41	2.267	1.29	0.388	-23.77	0.126	-90.02

```
NEXT? (PAUSE):  *GO,??
```

Figure 23. Amplifier design and predicted performance using a 16G FET.

a tunable series inductance in the input matching network of the first-stage amplifier. DC blocks are provided by 15-pF beam lead capacitors commercially purchased. Chip capacitors of 10,000 pF are used for bypassing the drain supply circuit, although this would have to be changed if the drain supply is pulsed. Presently, the amplifiers are configured for pulsing at the gate using a 200-ohm chip resistor for dc and pulse injection into the gate matching network. The fabricated circuitry eliminated wire bonds and several standoff chips which had been used in earlier versions in the dc bias circuitry. The resulting circuits should therefore be more rugged and reliable, as well as being simpler to fabricate. When earlier versions of these circuits were fabricated as described in the first Semiannual Report, it was found found that extensive retuning with chips was required. The positions of these chips seem to indicate that the matching networks wanted to see wider lines for optimum performance. Therefore, when designing and fabricating these networks, the matching elements were allowed to become wider than would normally be allowed at these frequencies, and the placement of components during the artwork generation permitted larger metallized areas at the junctions of stubs with the main transmission line matching elements.

The small-signal gain and input and output vswr of each amplifier type measured with the automatic network analyzer are plotted in Figs. 24 to 31. These responses are obtained without any tuning or adjustments of the circuits. Trimming will be done when pairs of amplifiers are combined to give a balanced stage with high-power output. These measurements were done with coaxial connectors attached with silver paint to the matching networks. Soldered connections will be used only when the amplifiers are integrated with the directional couplers. As a result, the responses measured may vary slightly with time depending on the tightness and flexing of connections to the measurement setups.

It can be seen that the responses of the first two amplifier stages are close to what should be expected in terms of having high gain and low vswr within the frequency band of interest. The 8G amplifier stage has a lower gain than desired, but this may be attributed to the higher vswr. The 16G amplifier stage peaks at too low a frequency, but with a gain several dB higher than expected from the calculated value of MAG.

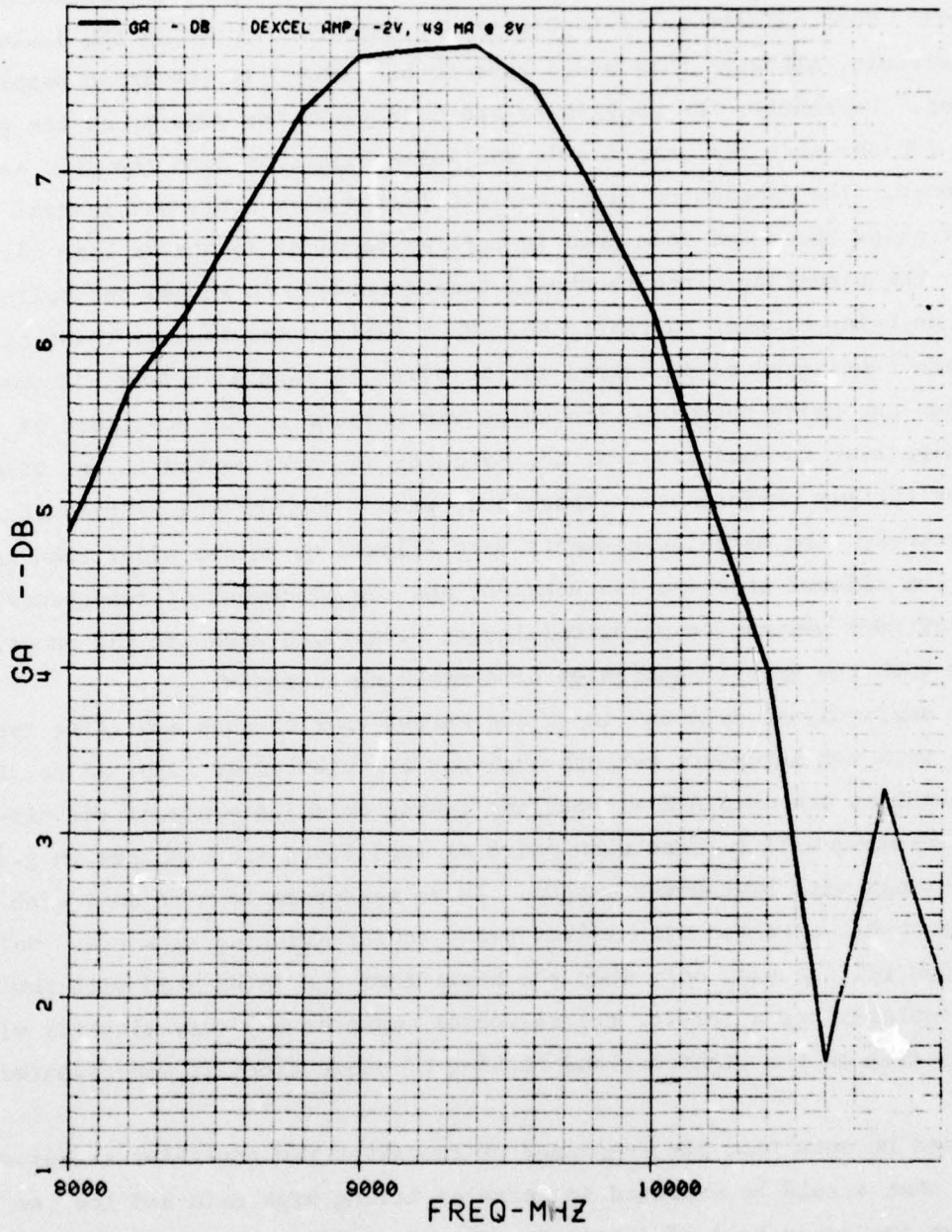


Figure 24. Measured small-signal gain of a DXL-3501A amplifier stage.

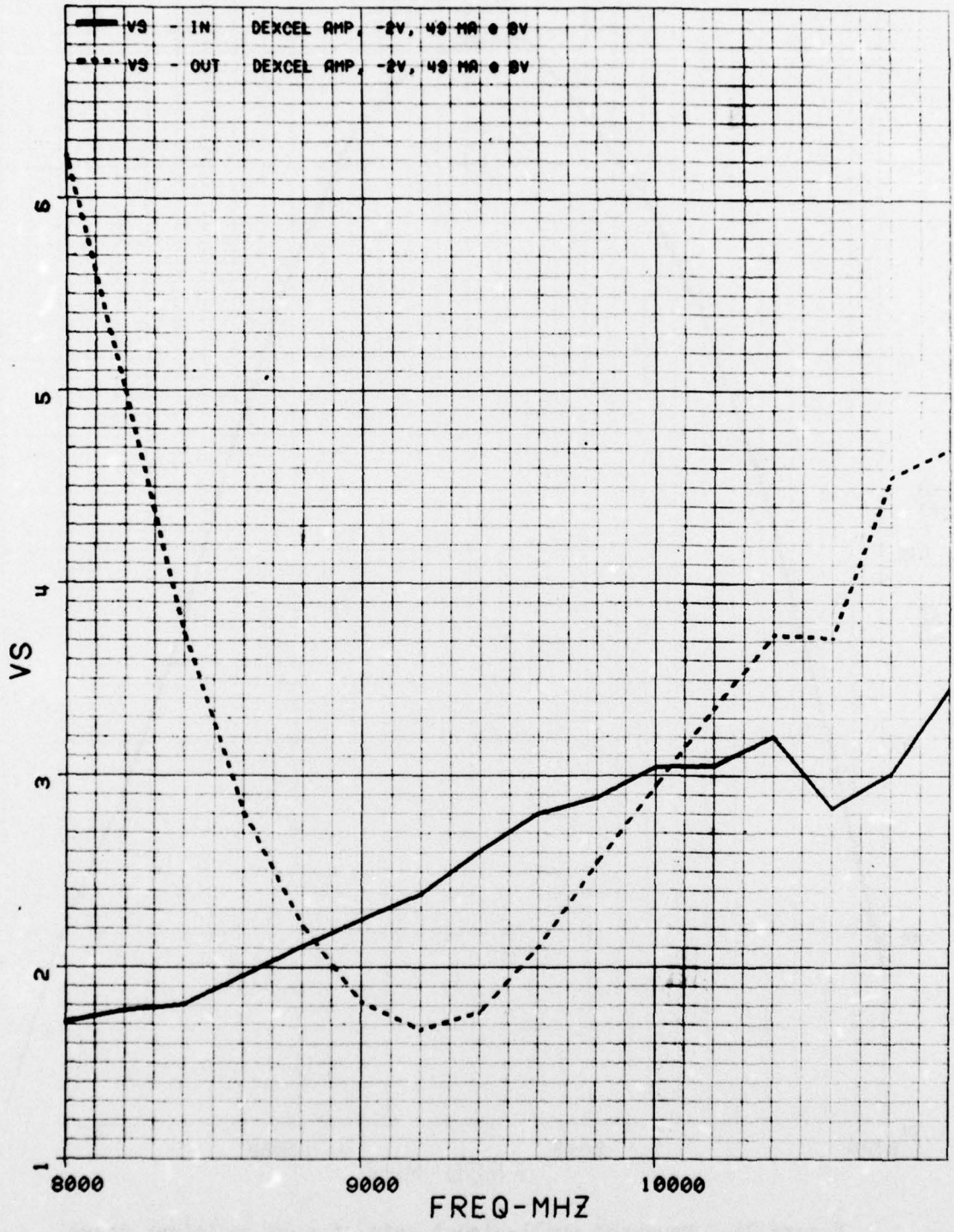


Figure 25. Measured small-signal vswr of a DXL-3501A amplifier stage.

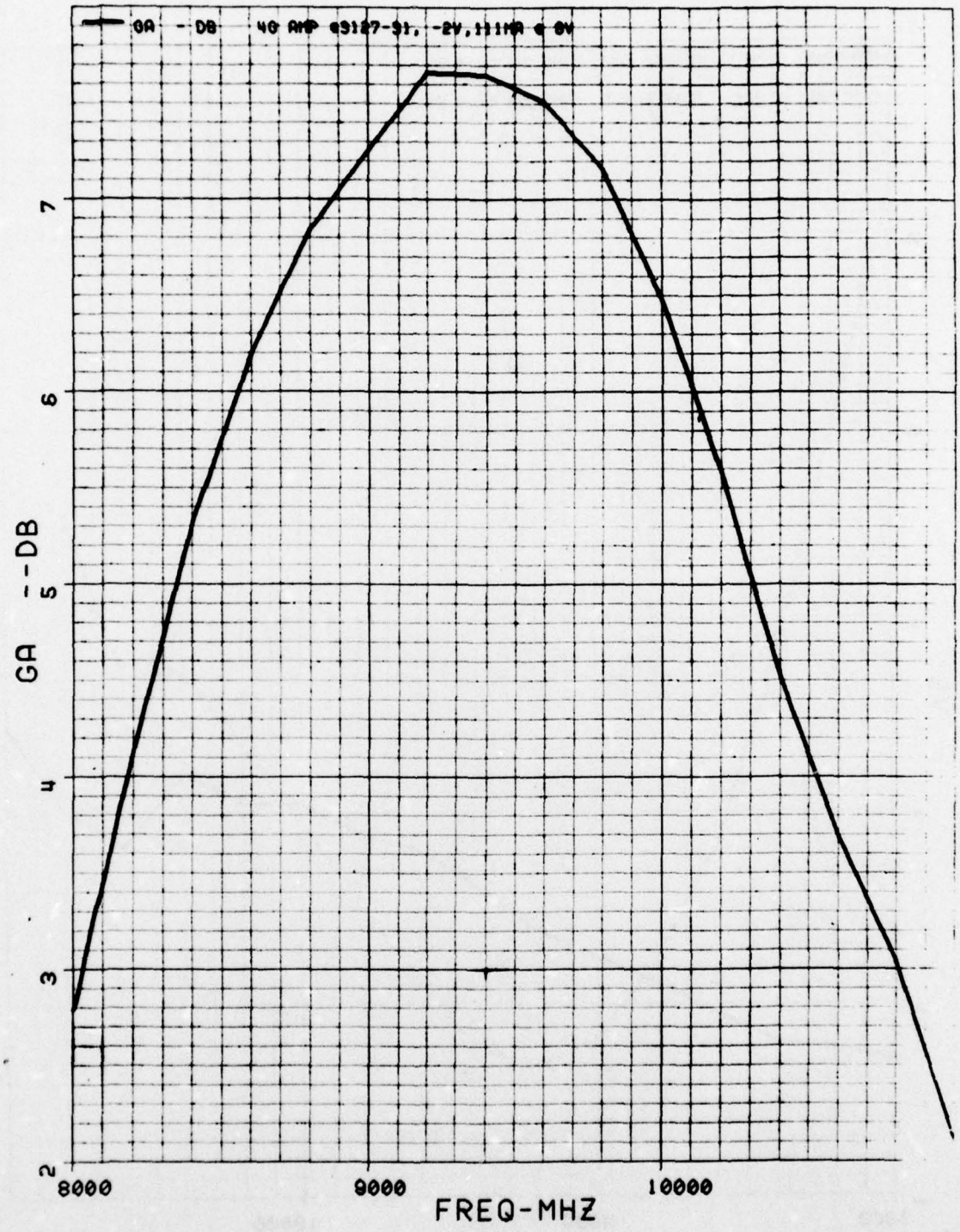


Figure 26. Measured small-signal gain of a 4G amplifier stage.

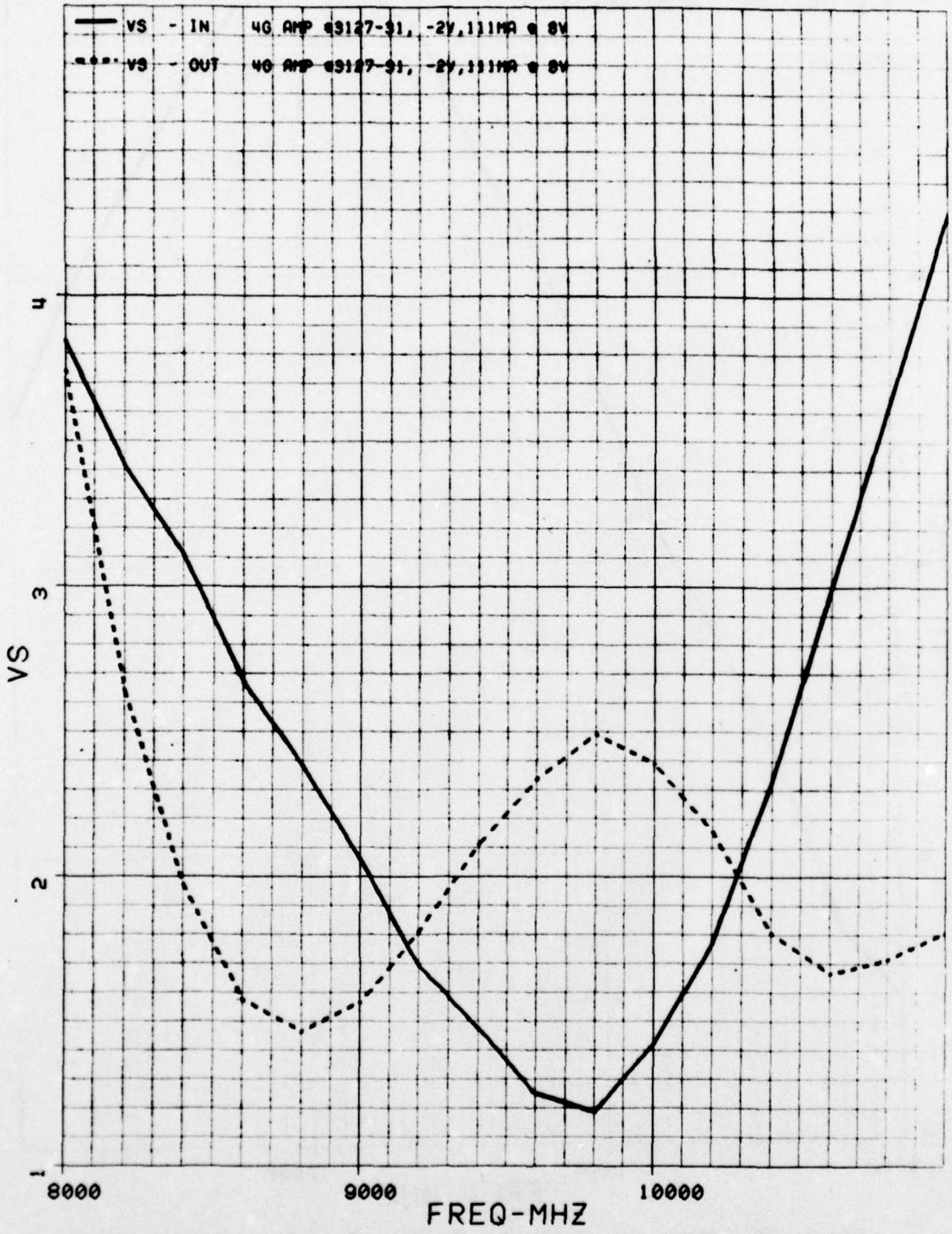


Figure 27. Measured small-signal vswr of a 4G amplifier stage.

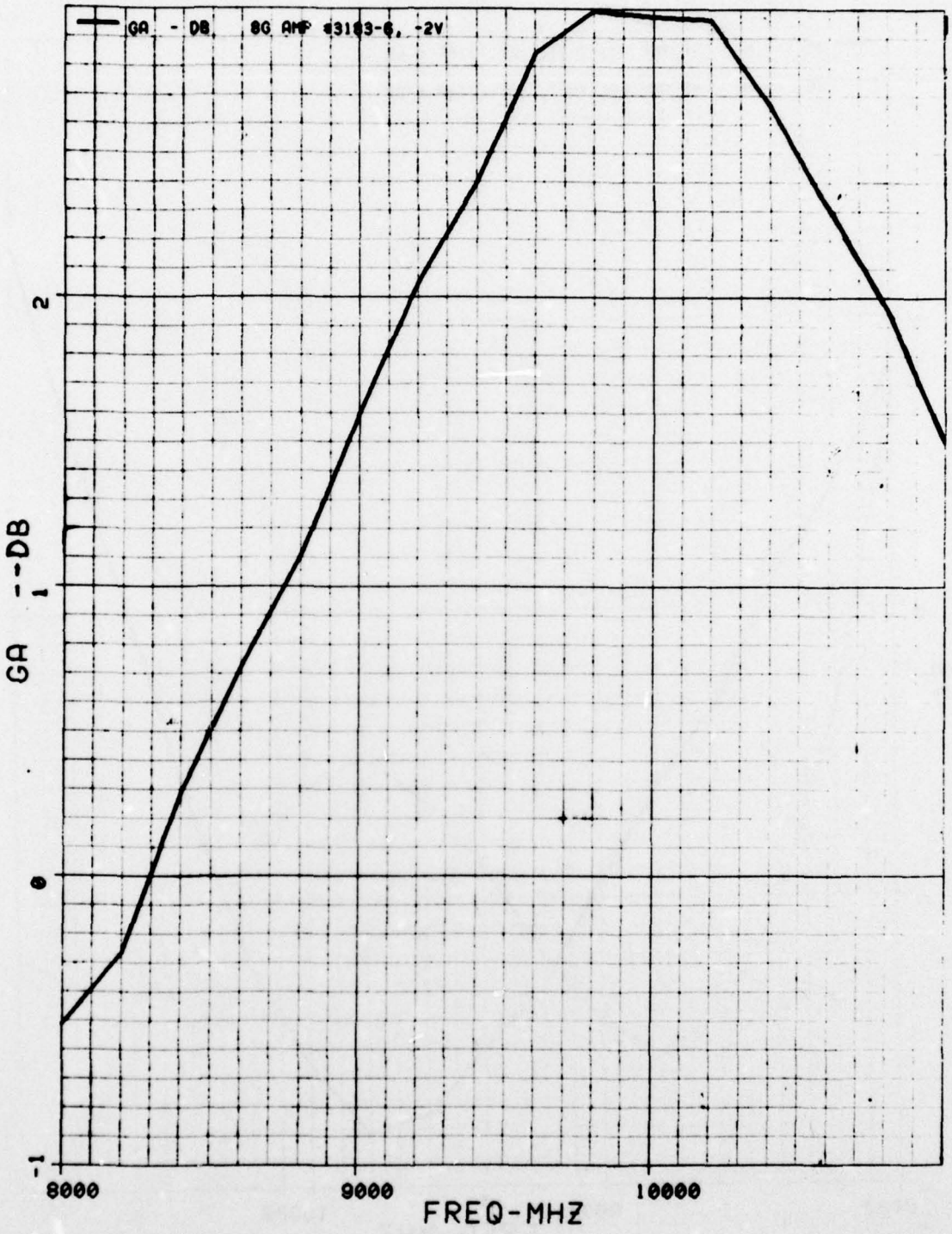


Figure 28. Measured small-signal gain of an 8G amplifier stage.

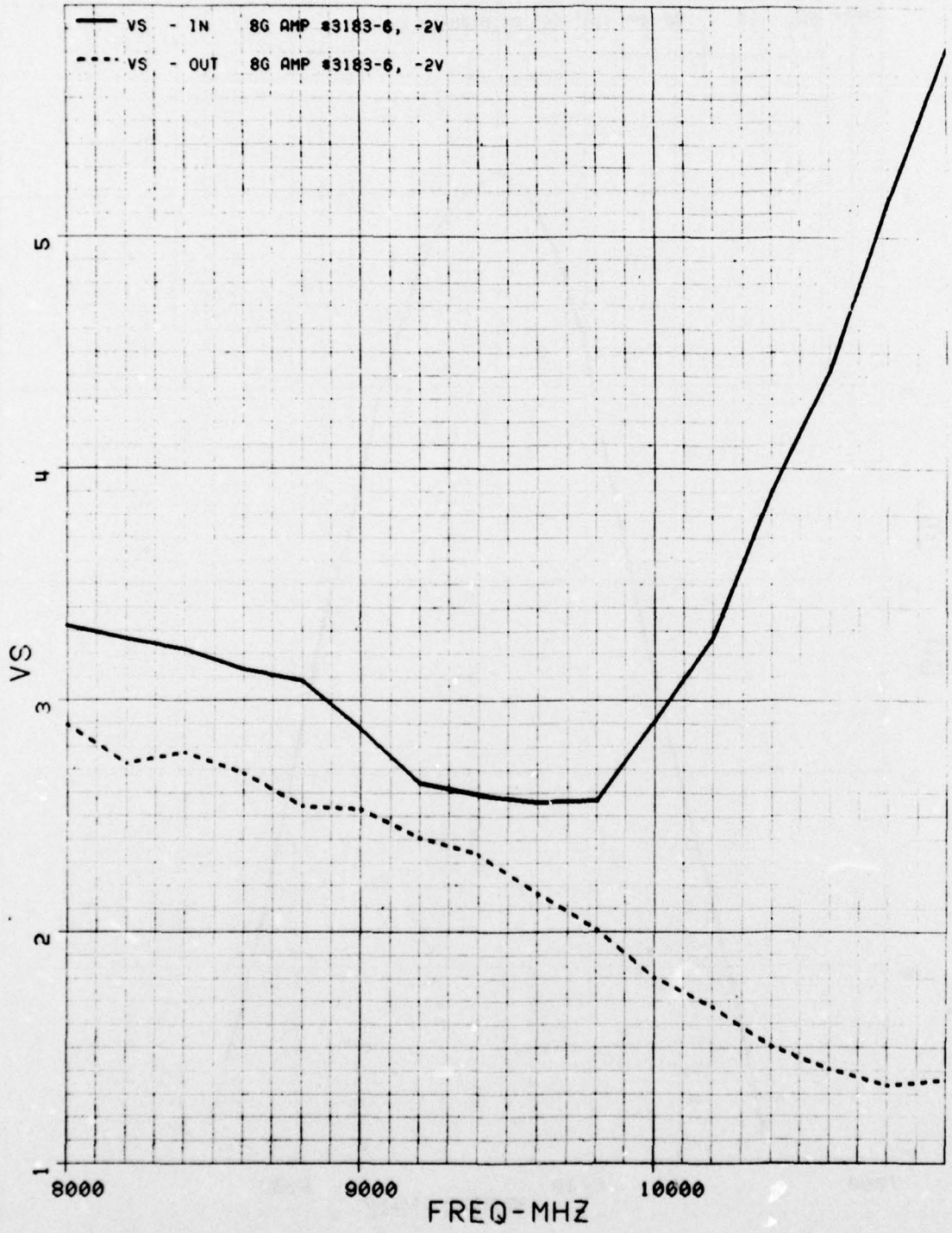


Figure 29. Measured small-signal vswr of an 8G amplifier stage.

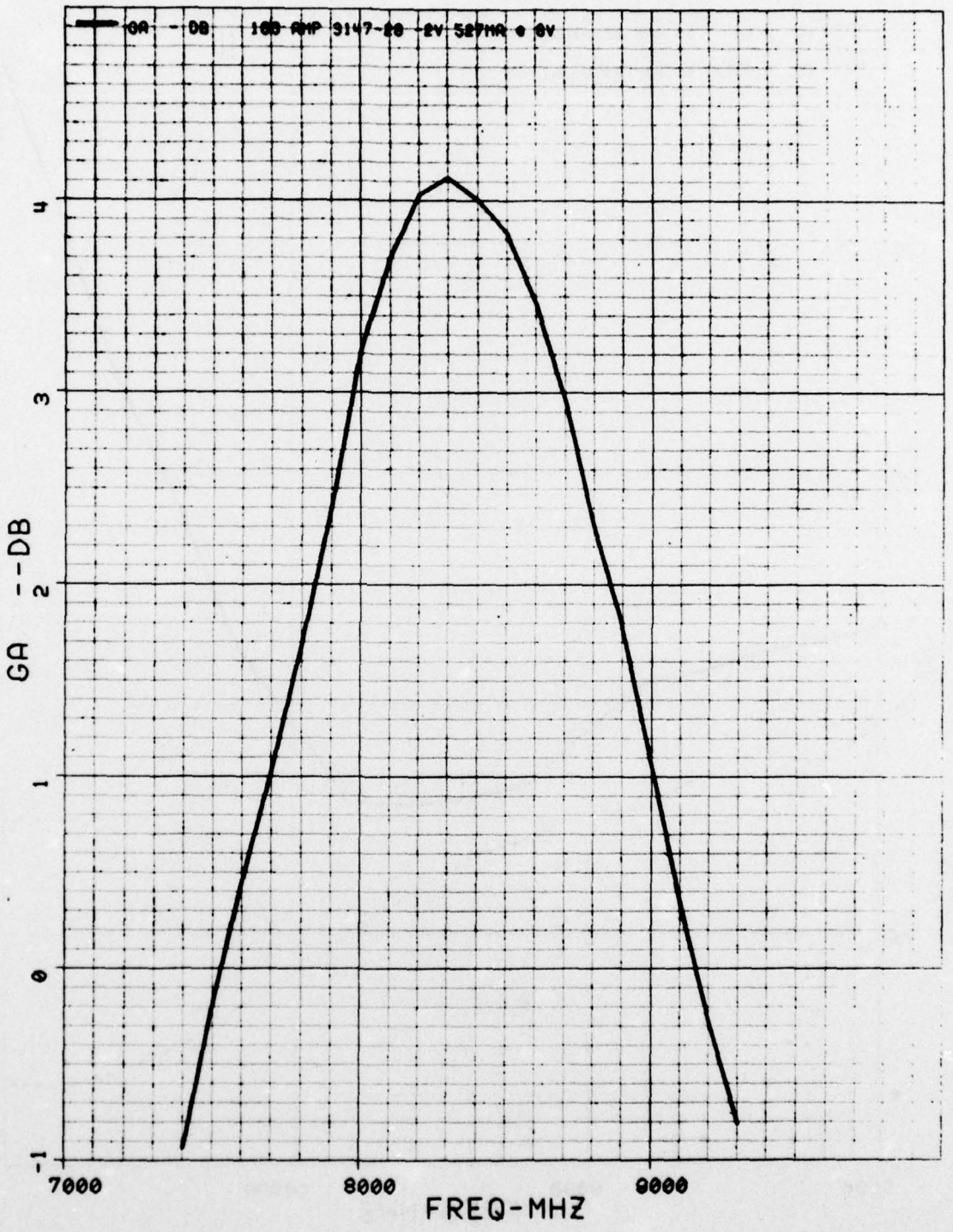


Figure 30. Measured small-signal gain of a 16G amplifier stage.

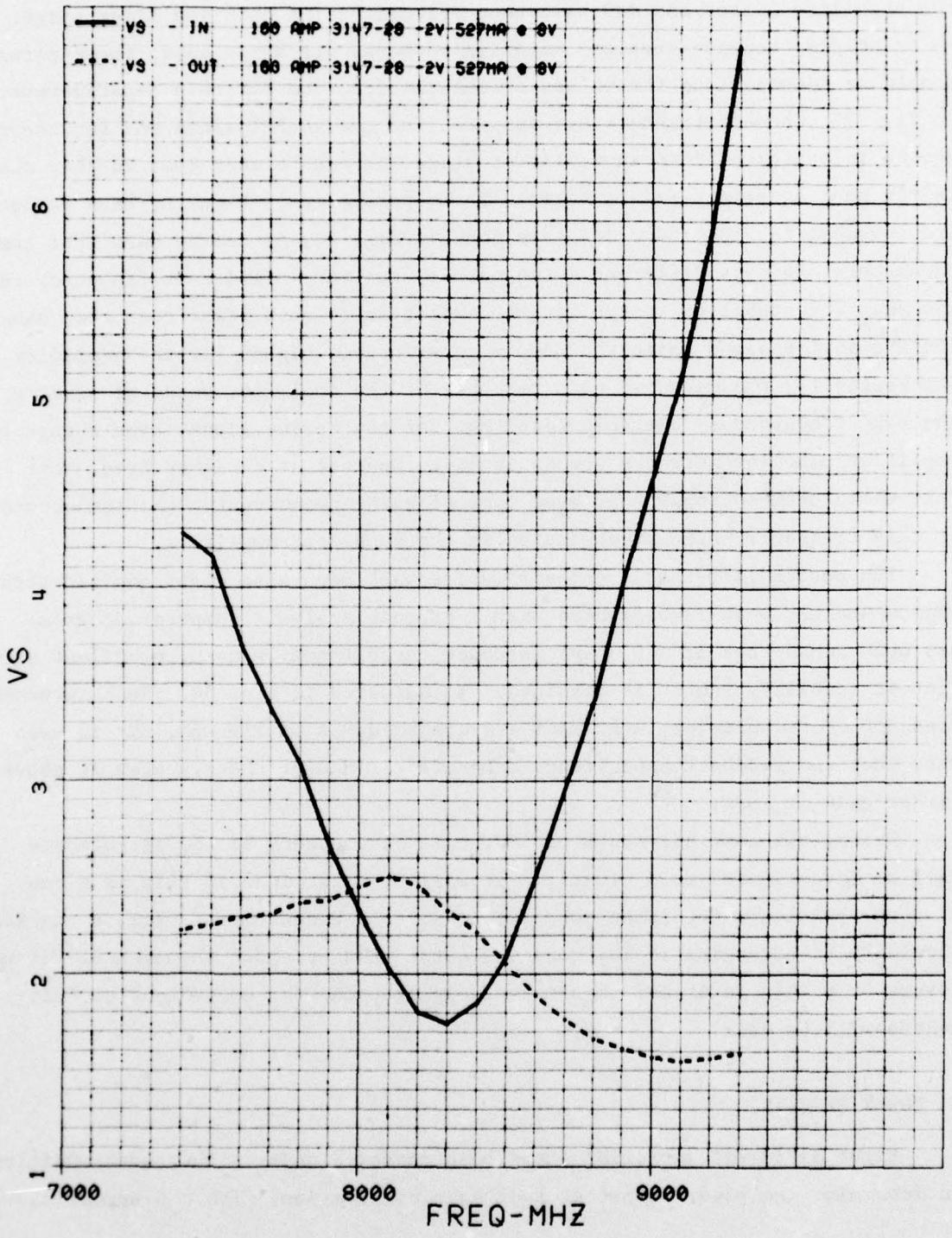


Figure 31. Measured small-signal vswr of a 16G amplifier stage.

In an attempt to gain an insight into the cause of this gain discrepancy, the stability factor and MAG have been calculated for each amplifier stage. In principle, because lossless matching networks are being used, these parameters should be identical to the values calculated from the FET chip S-parameters. In Fig. 32, these parameters are compared for the 4G FET alone and for the same device incorporated into an amplifier stage. It can be seen that in this case fairly good agreement exists between these parameters. When the same parameters are compared for the 16G case as is done in Fig. 33, it can be seen that these parameters are very different in magnitude, but very similar in frequency response. The stability factor for the amplifier is much lower than that measured for the device alone while the MAG is considerably higher for the amplifier. Interestingly, the measured gain response of the amplifier peaks at exactly the same frequency as the calculated MAG for the device alone, even though the amplifier matching networks are designed to operate at a higher frequency. This would seem to imply that some type of gain-enhancement mechanism occurs at this frequency which predominates in the completed amplifier.

The possibility that a capacitive feedback mechanism might explain this phenomenon has been investigated with a circuit analysis computer program. It has been found that if a 0.35-pF feedback capacitance is used, excellent agreement in stability factor is obtained, as indicated in Fig. 34. Such agreement does not occur, however, when MAGs are compared, as in Fig. 35. It is seen here that the feedback capacitance enhances the MAG of the FET when it shows either gain or loss.

During the next six-month period, this discrepancy in 16G performance will be investigated more closely. It will be determined if this is a consistent phenomenon for large power devices. All measurements will be checked carefully to determine if inaccuracies cause this apparent phenomenon. If we assume that this is a real phenomenon, explorations for equivalent circuit models will be done.

G. POWER RESULTS

Eight different amplifiers have been measured under high-power conditions to determine the power output at 1-dB gain compression. Table 6 summarizes

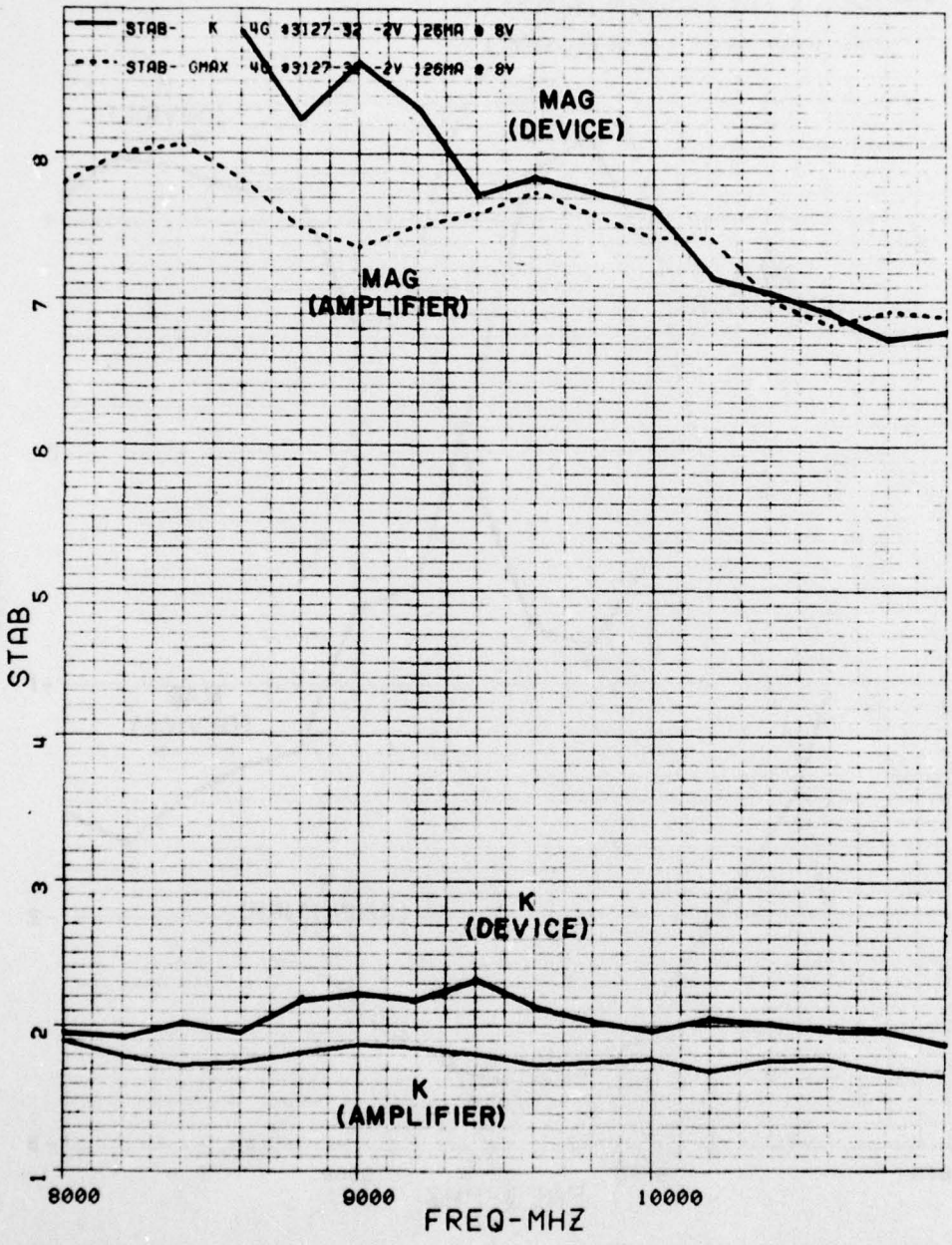


Figure 32. Comparisons of stability factors and maximum available gains for a 4G FET and amplifier stage.

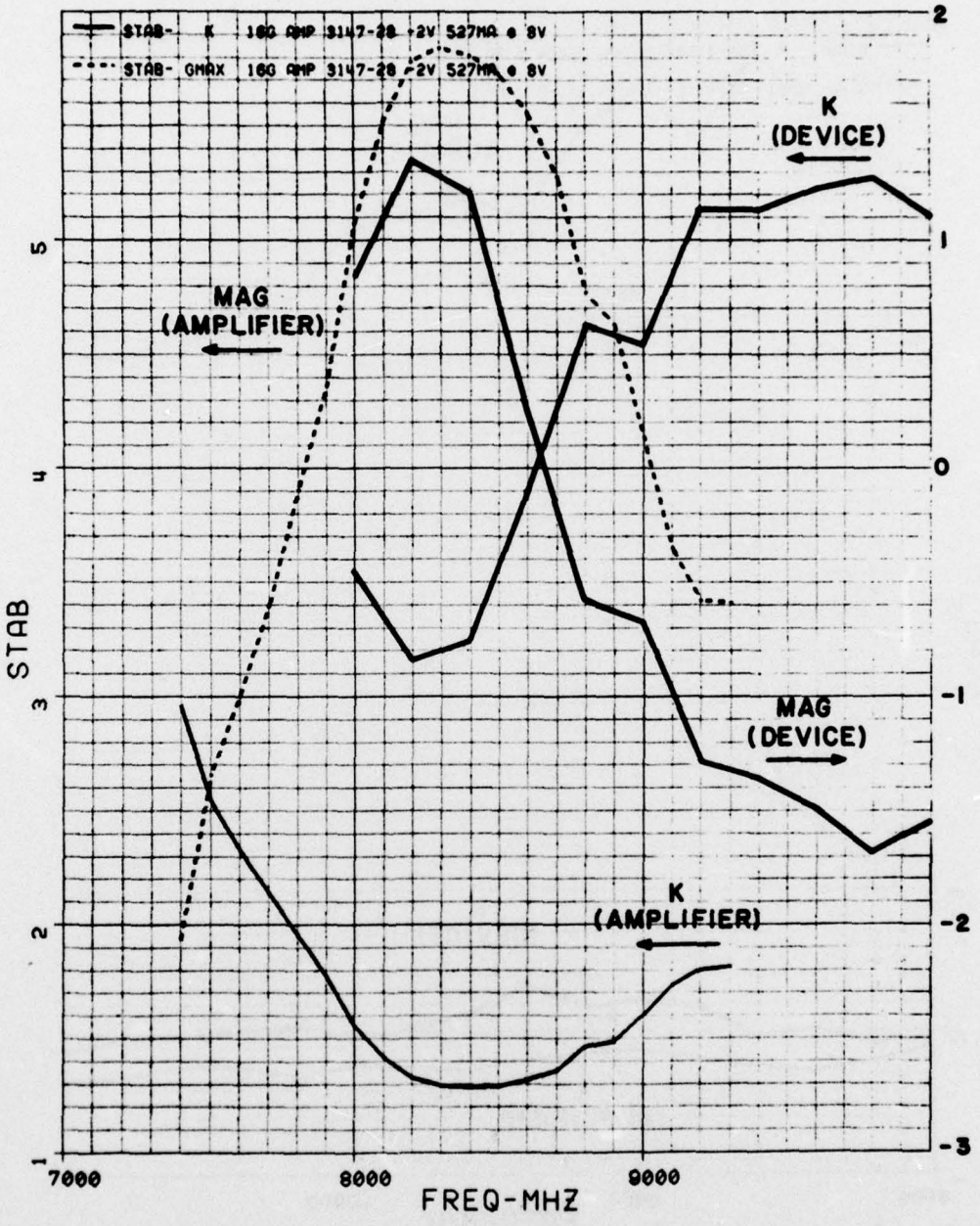


Figure 33. Comparisons of stability factors and maximum available gains for a 16G FET and amplifier stage.

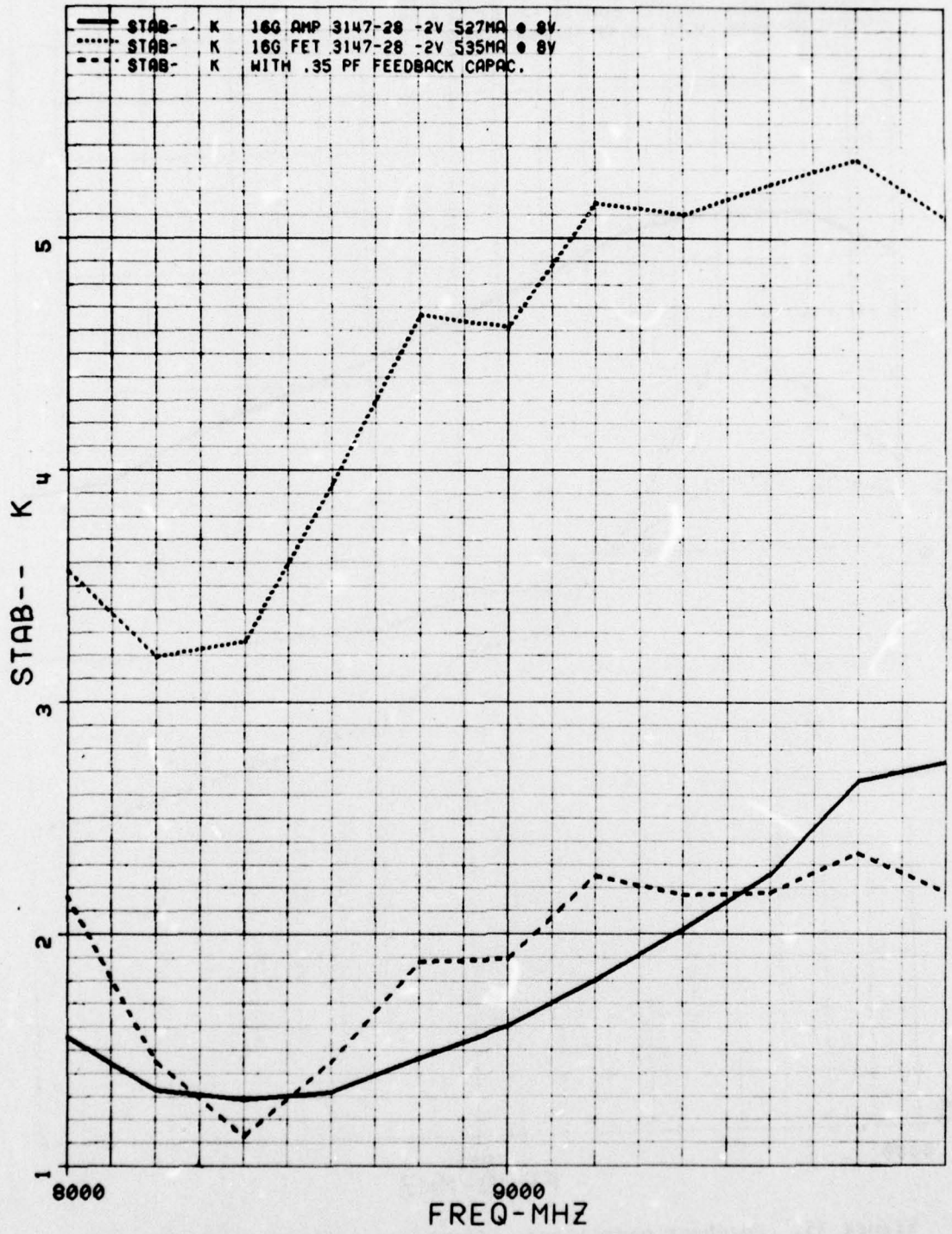


Figure 34. Feedback capacitance effects on stability.

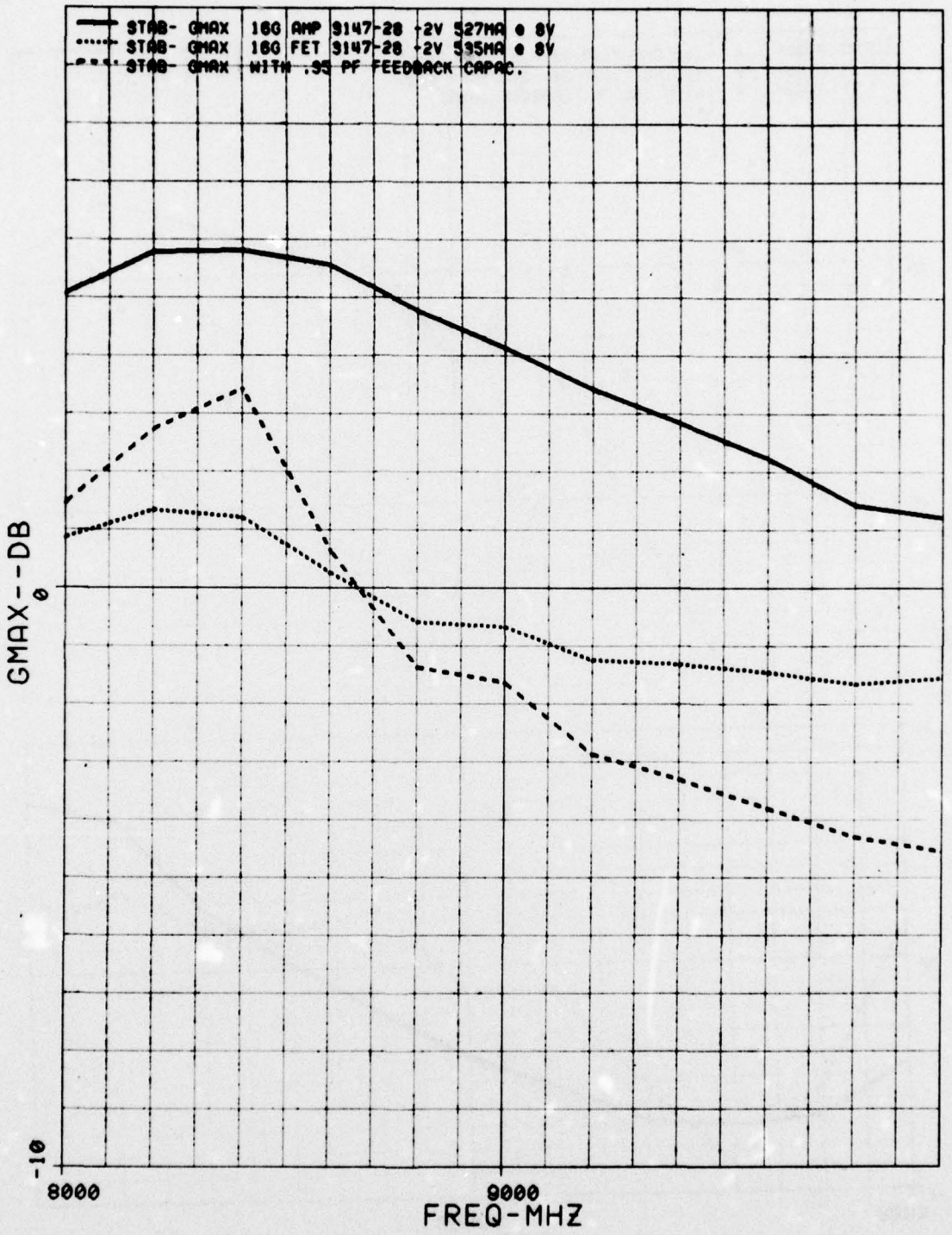


Figure 35. Feedback capacitance effects on maximum available gain.

TABLE 6. AMPLIFIER PERFORMANCE DATA

Stage	Device	Gain(ss) (dB)	P(-1 dB) (mW)	η_{PA}	9-10 GHz Swept Gain @ P(-1 dB point) (dB)
1	DXL-3501A	9.0	53	15.0%	-
	DXL-3501A	7.5	58	16.1%	7.6±0.6
2	3127-31	8.5	71	6.6%	-
	3127-32	7.5	55	4.3%	6.8±0.7
3	3183-6	3.3	550	19.6%	1.9±0.5
	3183-110	3.6	447	12.4%	-
4	*3147-27	4.7	851	10.4%	-
	*3147-28	4.2	1000	11.1%	-

* 8.5 GHz

these results at a frequency of 9.5 GHz (except for the 16G amplifiers which were tested at the frequency of maximum gain, namely 8.5 GHz). The saturation characteristic of each type of amplifier is plotted in Fig. 36. Also shown are points representing the performance required from each stage including coupler losses. These points are derived from the numbers given in Fig. 1 by dividing in half the power output from each balanced amplifier stage.

The Dexcel amplifier stage has sufficient gain and power for the system requirements. However, the vswr small-signal measurements show that some improved performance should be possible through tuning the matching networks.

The 4G amplifier stages have high gain, but disappointingly low output power. The small-signal measurements show that the vswr are very low. Under large-signal conditions, the output is expected to be mismatched. It is therefore conceivable that some improvement in output power is possible through tuning the output matching network. Otherwise, it will be necessary to select other devices for this stage.

The saturation characteristics of the 4G amplifiers are distinctly different from the other amplifiers in that they saturate in a "soft" way. Other amplifiers show constant gain with increasing drive level until very close to

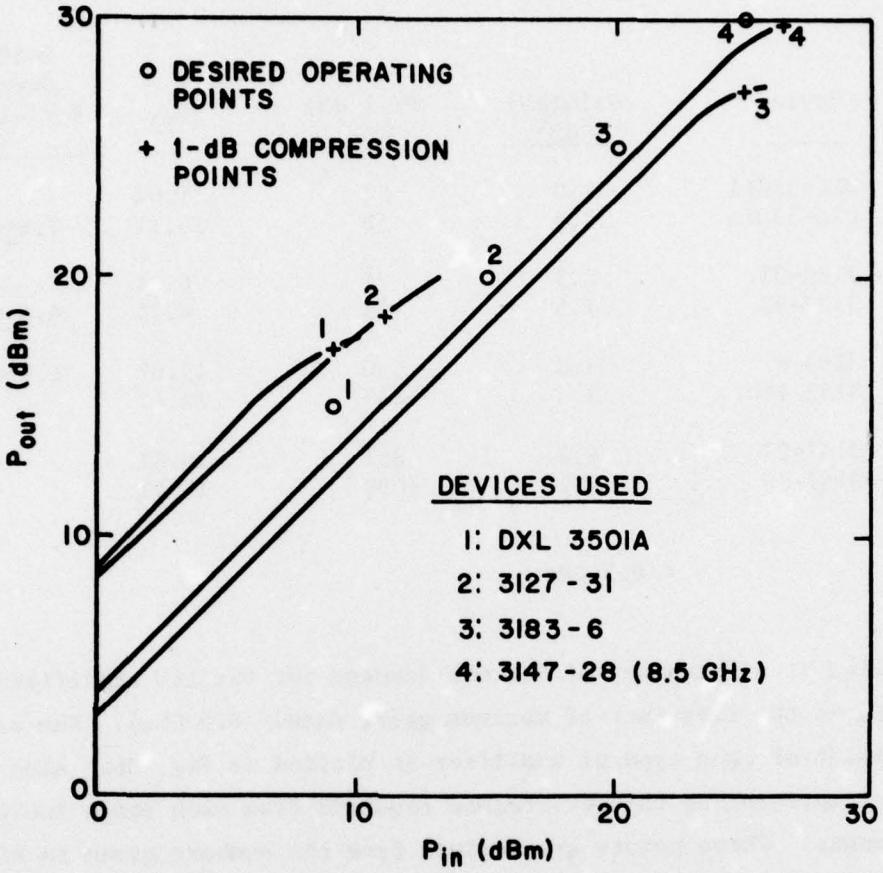


Figure 36. Saturation characteristics of fabricated amplifier stages.

saturation. The 4G amplifiers have gains which decrease very slowly as drive is increased. If overdriven beyond the 1-dB gain compression point, sufficient gain and power are available from these devices. If alternate devices are not found, it may be necessary to operate the existing 4G devices in this manner.

The 8G amplifiers have sufficient output power, but with low gain. Both the input and output vswr indicate that better gain can be achieved by improving the matching of the input and output networks. The substrates which are used to fabricate these particular amplifiers seem to have inferior metallization which causes soldering and bonding operations to be quite difficult. This defective metallization may also be causing the poor amplifier performance.

If higher gain cannot be realized by means of better substrates and by tuning of the input and output matching networks, then other devices will have to be selected for this stage. Note that close to 20% power-added efficiency was achieved in one of these amplifiers even at this low gain.

The 16G amplifier performance, although at a frequency which is 1-GHz too low, shows a gain and power level very close to that needed. Attempts will be made to achieve this performance at the desired frequency. As indicated earlier, this will involve careful measurement of device parameters, and a possible investigation to determine whether other than simple lossless matching networks are needed to achieve optimum performance.

H. PHASE CONSIDERATIONS

Extensive pulsed-phase characterization of FET amplifier stages was done in the beginning of this program and the data was presented in the first Semiannual Report. On a parallel program at that time, a five-stage 500-mW amplifier for the 9-to 10-GHz frequency range was developed (USAF Avionics Laboratory Contract F33615-76-C-1122). The completed module saturation characteristics were tested on a modified computer-controlled network analyzer which measures gain, phase, and output power as a function of input drive level. *These measurements showed that the AM/PM conversion of the complete five-stage amplifier is a maximum of 3.5°/dB, which is considerably lower than the numbers measured with the phase measurement bridge described in the first Semiannual Report.*

A careful evaluation of measurement techniques disclosed that erroneous data had been generated with the phase-measurement bridge. A schematic of the phase measurement bridge is repeated in Fig. 37. AM/PM measurements are done by varying the drive level to the amplifier under test with the HP X375A variable attenuator preceding the amplifier, and measuring the resulting change in phase for a given change in amplitude. The data taken during these measurements erroneously neglected the change in phase through the attenuator for different settings of attenuation. Table 7, repeated from the first Semiannual Report, shows the phase characteristics of this attenuator. Due to this procedural error, this phase change had been improperly attributed to the amplifier being tested.

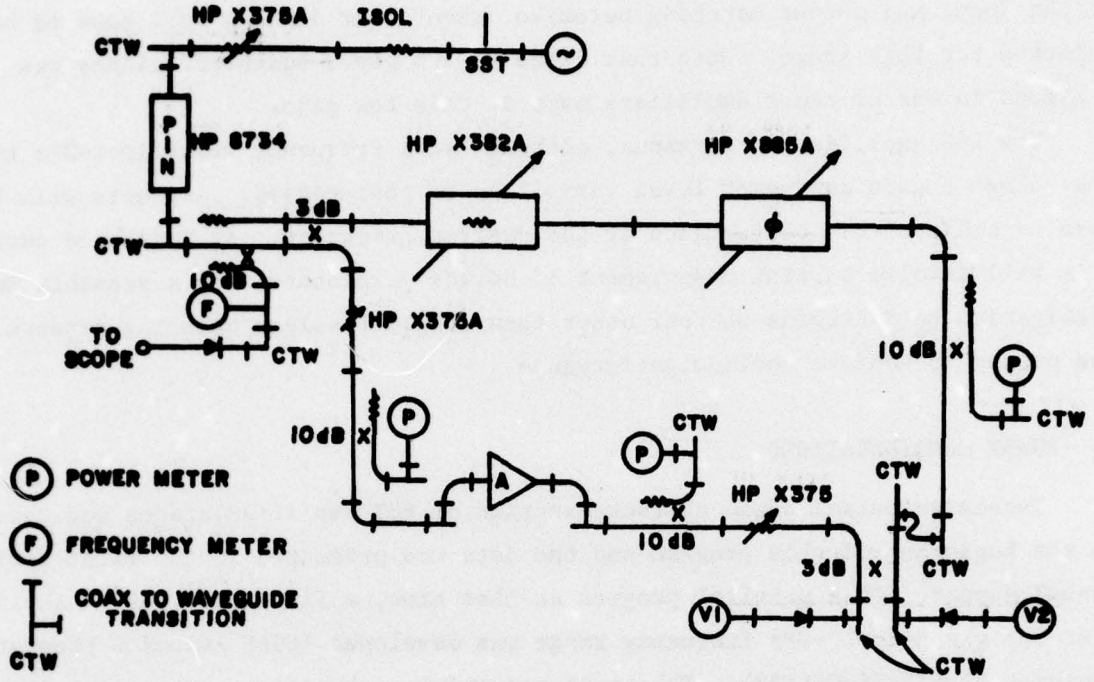


Figure 37. Pulsed-phase measurement bridge.

TABLE 7. COMPARATIVE PHASE-SHIFT MEASUREMENTS OF HP X375A (Inv. No. 3-5654) ATTENUATOR

Attenuator Setting (dB)	True Attenuation (dB)	$\Delta\phi$ Bridge (Degrees)	$\Delta\phi$ Analyzer (Degrees)
1	0.84	9.5	10.5
5	3.59	33.5	33.4
10	7.52	59.0	57.3
15	11.67	80.2	77.7
20	16.01	97.0	94.5

The proper measurement of AM/PM conversion with the phase bridge requires that the bridge be first calibrated at the same drive levels which will be used during the amplifier testing. The phase shifts measured during calibration must then be subtracted from the values measured with the amplifier in place. This corrected procedure will be done in all future testing.

To maintain maximum efficiency under pulsed rf conditions, the dc power to the module must also be pulsed. Either pulsing of the gate voltage to effectively turn the drain current on and off, or pulsing of the drain voltage may be used. Gate pulsing has the advantage of using simpler pulse modulation circuitry because the gate draws essentially no current. Drain modulation requires that large currents be controlled by the modulating circuitry, and losses in the drain modulation process will directly degrade the overall efficiency of the complete amplifier module.

In performing the various pulsed-phase measurements, it has become apparent that gate pulsing has the disadvantage of requiring large FET source-to-gate breakdown voltages. This breakdown voltage must be greater than the sum of the gate bias, drain bias, and the peak rf voltage. This sum is estimated to be about 15 V. The FETs should therefore have breakdown voltages of about 20 V to provide an adequate margin. Such high breakdown voltages would require the carrier density in the FET channel to be reduced to the mid-10^{16} cm^{-3} range. Unfortunately, this is incompatible with the density required for good amplifier performance at the frequencies of interest to this project.

At this time, it is not clear whether drain pulsing or gate pulsing is the preferred approach for a FET amplifier. Drain-pulsing techniques will be more closely evaluated during the next six months, which will permit more meaningful comparisons with gate pulsing.

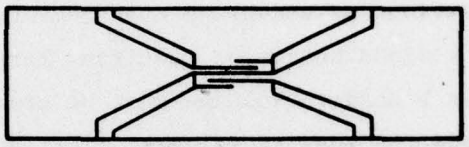
I. DIRECTIONAL COUPLERS

Interdigitated 3-dB directional couplers for 9- to 10-GHz had been developed before the award of the current contract. The electrical performance of these couplers is good, but the size of the coupler substrates, 20.3 mm x 12.7 mm x 0.64 mm, is large. As a result, the size of two couplers used to assemble a balanced amplifier stage would be larger than the amplifiers which are being combined. These couplers are being modified to fit on smaller substrates so that the resulting overall amplifier size will be minimal.

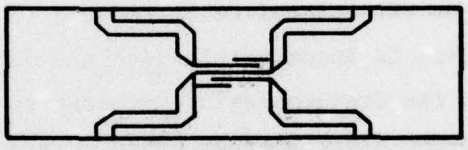
Initially, the modified couplers have been fabricated on substrates measuring 17.8 mm x 5.1 mm x 0.64 mm. Testing of these couplers has shown what fabrication parameters are critical to good coupler performance.

It has been found that the metallic crossovers required in an interdigitated coupler are not critical. Identical coupler performance has been achieved when using single wire bonds, double wire bonds, and small ribbons for the crossovers.

The geometry of the 50-ohm microstrip lines used to connect the coupler to the edge of the substrate has been found to be critical. Figure 38 shows several geometries which have been tried. In all cases, the lines are arranged perpendicular to the edge of the substrate to minimize discontinuities which might occur when the couplers are connected to other components.



PATTERN NO. 3034



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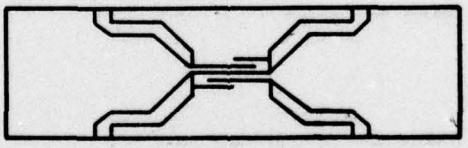

PATTERN NO. 3039

Figure 38. Directional coupler patterns.

The angle at which the microstrip lines leave the coupling section has been found to be important. If the angle is made too small, as it is for pattern 3034 shown in Fig. 38, extraneous coupling seems to occur along those portions of the lines close to the coupler section. As a result, the effective length of the coupler is longer than designed and the coupler response shifts to lower frequencies. The performance of coupler 3034C, shown in Fig. 39, seems to be optimum at about 7.5 GHz. The angle between 50-ohm lines is approximately 45°. Attempts have been made to raise the frequency response of the coupler by shortening the coupling length. However, this has a minimal effect on the center frequency, indicating that the extraneous coupling has a dominant influence.

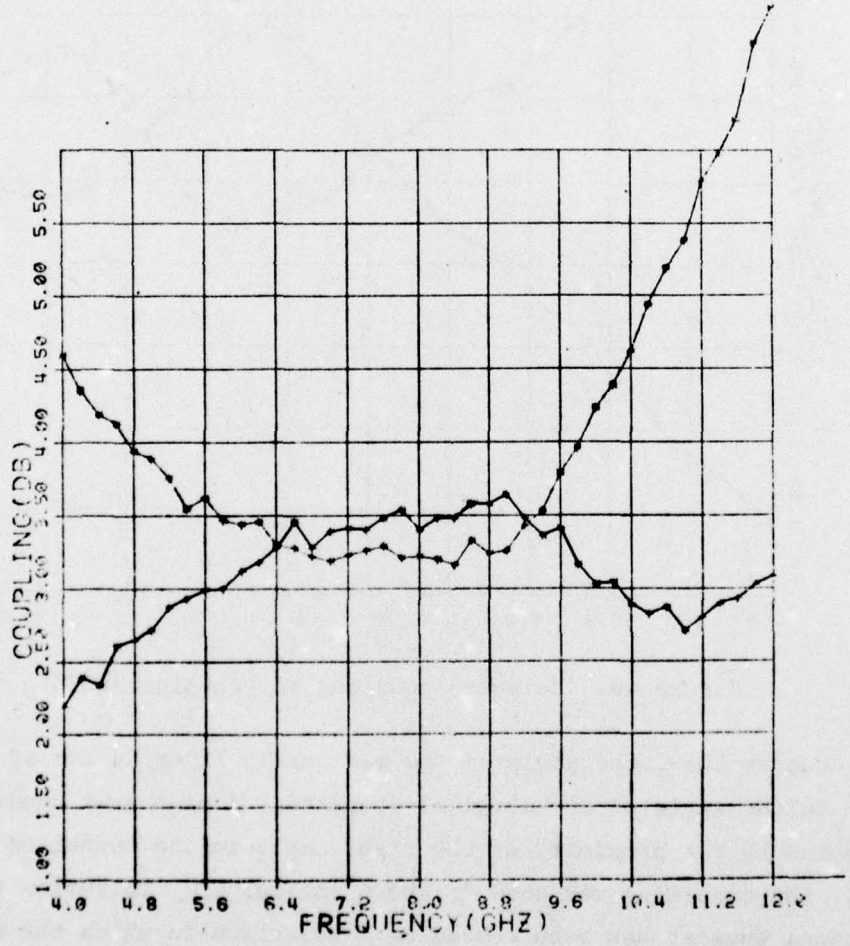

Figure 39. Measured coupling for coupler 3034C.

In coupler 3037, the angle between lines is increased to 180° to try to minimize this extraneous coupling. However, it is found that the right angle discontinuities in close proximity to the coupler adversely affect its performance. Figure 40 shows the type of response which is obtained.

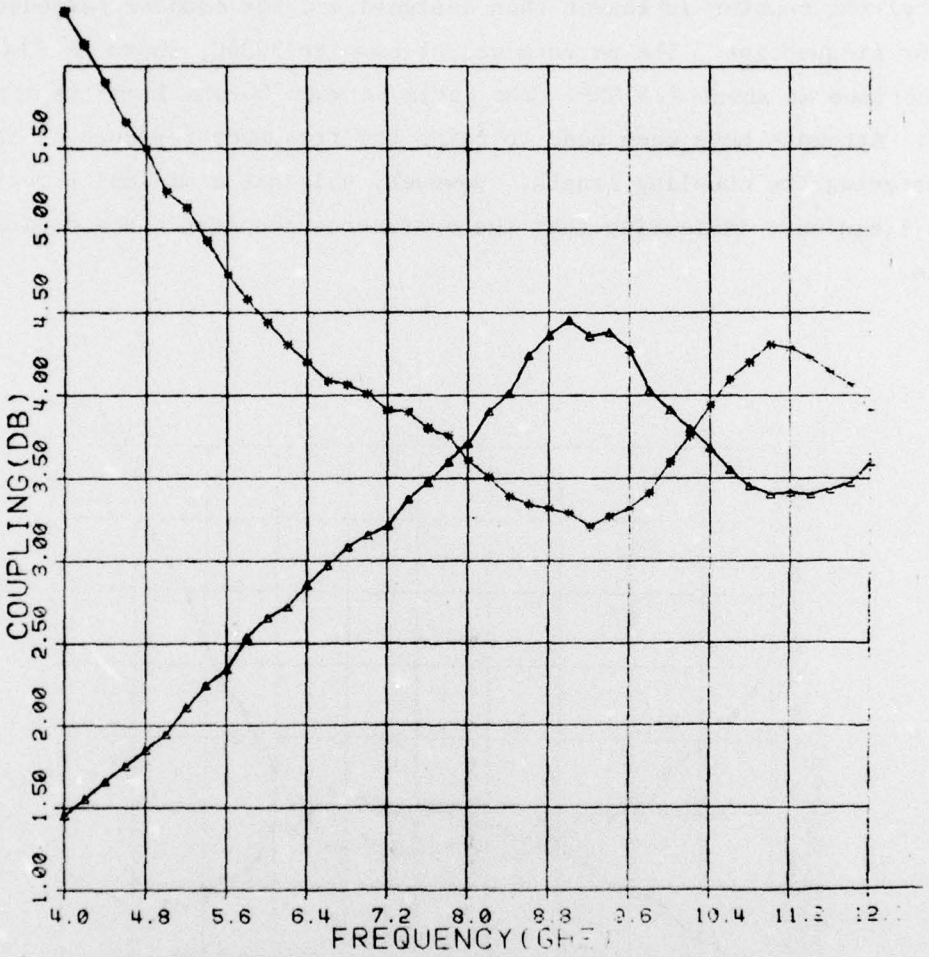

Figure 40. Measured coupling for coupler 3037A.

In coupler 3039, the angle of the microstrip lines is set at 105°, which is close to the angle of the original couplers. A high vswr condition seems to be caused by the proximity of the right angle to the connector used for testing. The resulting response is shown in Fig. 41. To verify this effect, an identical coupler has been tested on a substrate in which the width has been doubled to 10.2 mm, and the 50-ohm lines between the connectors and the right angles are increased by 2.6 mm. The resulting coupler indicates the good

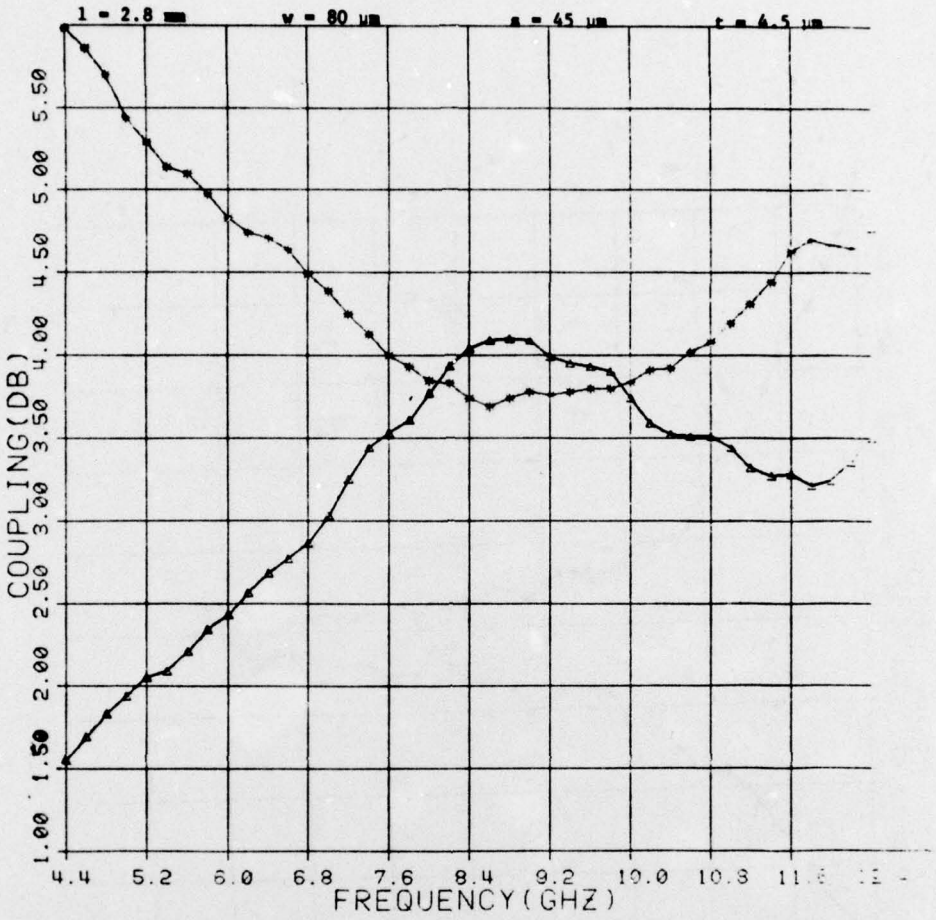

Figure 41. Measured coupling for coupler 3039-1.

performance shown in Fig. 42. Although this response is slightly undercoupled, overplating with gold can be used to achieve optimum coupling. The isolation, vswr, and insertion loss data associated with the coupler are shown in Figs. 43 and 44. From these plots, it can be seen that the frequency of best performance is approximately 11 GHz. Over the band from 7 to 12 GHz, the overall loss of this coupler, including connectors and the longer microstrip lines is 0.4 dB, the isolation is better than 18 dB, and the vswr is less than 1.35.

The next couplers will be fabricated on narrower substrates to determine the minimum size compatible with good performance. These couplers will then be integrated with the amplifiers to form balanced stages.

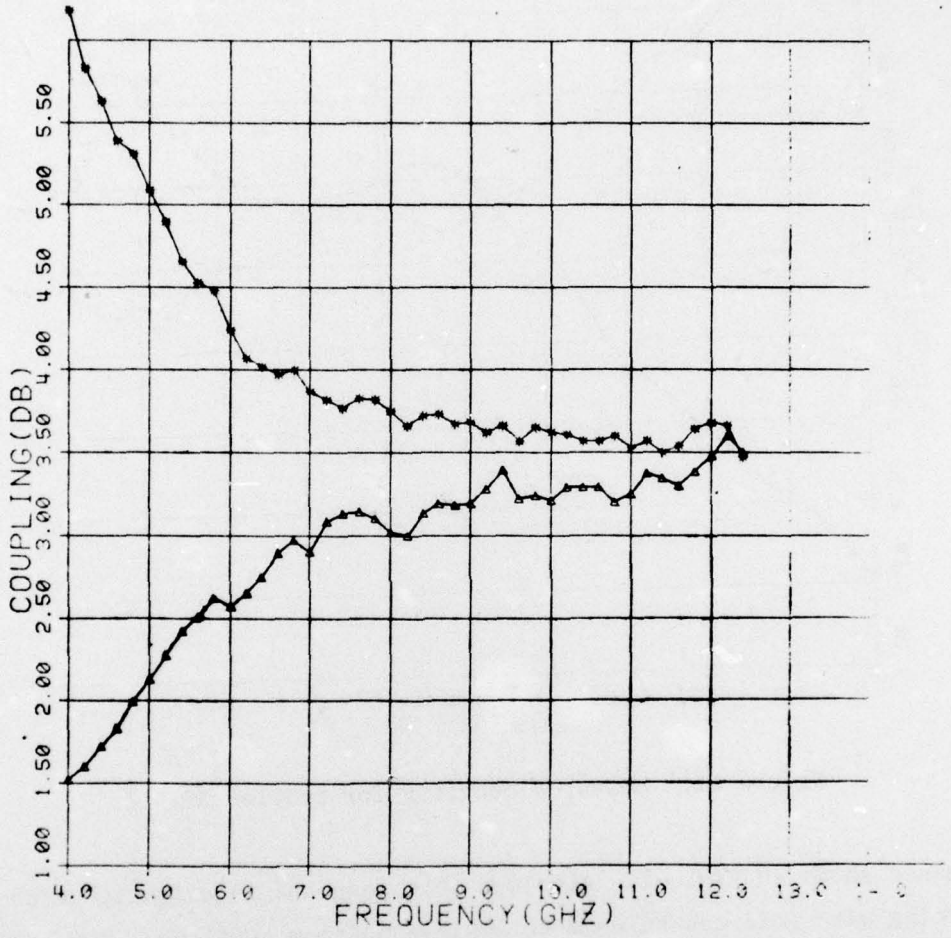

Figure 42. Measured coupling for coupler 3039-M1-1.

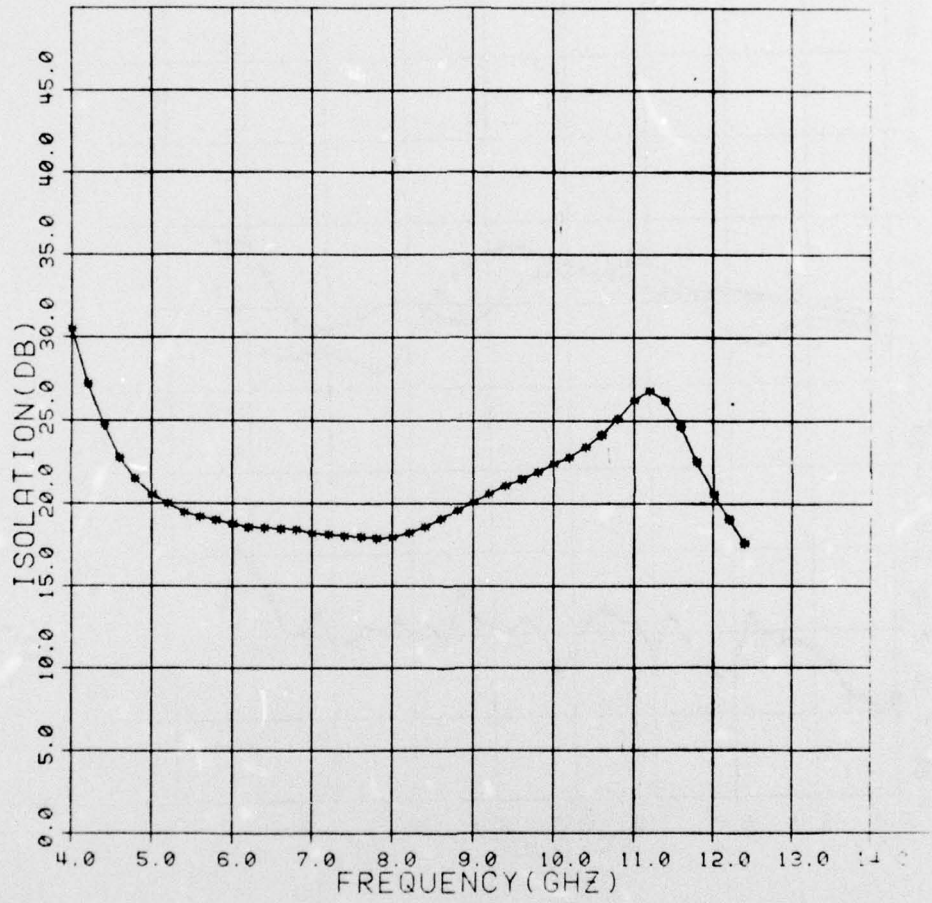

Figure 43. Measured isolation for coupler 3039-M1-1.

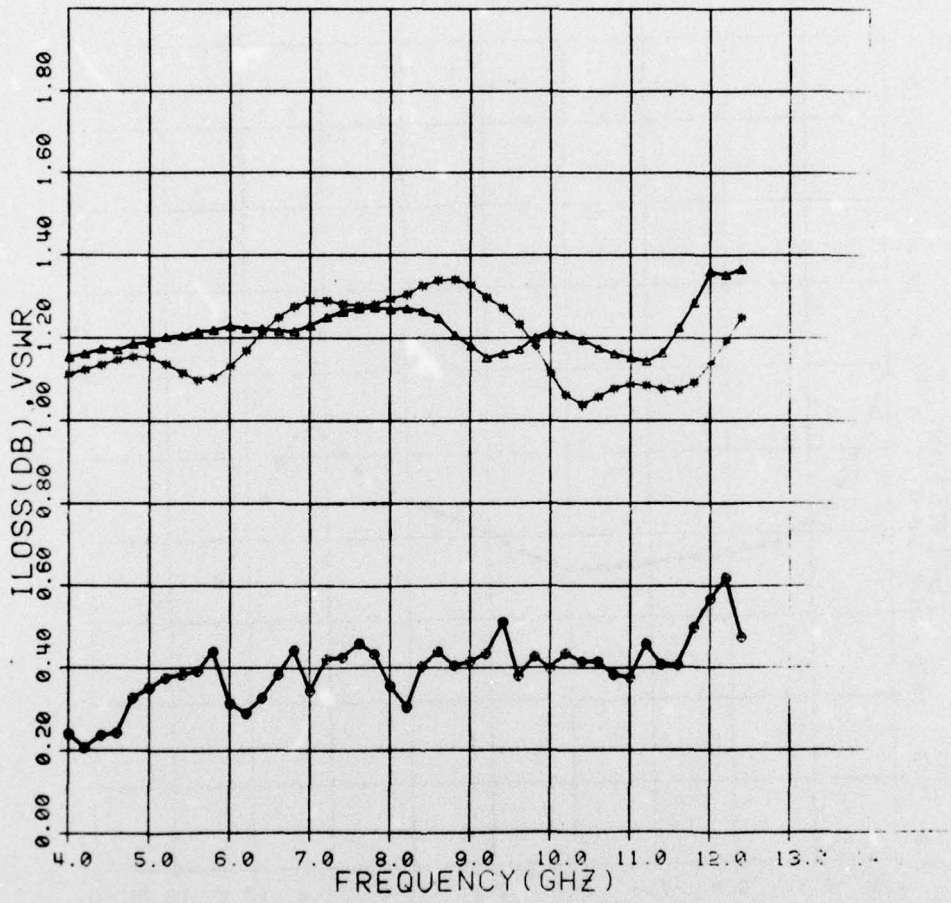

Figure 44. Measured vswr and loss for coupler 3039-M1-1.

SECTION IV

DEVICE DELIVERIES

During the second six-month period of this program, two deliveries of ten devices each were made. Complete data sheets showing the rf performance of the mounted devices as a function of drive level have been delivered with the devices. A summary of the device characteristics is tabulated in Table 8.

TABLE 8. CHARACTERISTICS OF DELIVERED FET DEVICES

Device No.	Power Out (mW)	Gain (dB)	η_{PA} (%)	Gain (Small Signal) (dB)
16G FETs tested at 8 GHz				
B642-20	540	3.26	7.9	6.32
-22	580.5	2.32	6.2	6.07
-23	621	2.62	7.5	6.40
-26	594	2.42	8.33	6.48
-30	600.75	2.47	9.16	6.48
3147-1	1490	3.4	14.6	4.6
-4	1282.5	2.8	12.05	5.0
-6	783.0	2.7	26.27	5.2
-7	1039.5	3.09	9.79	4.18
-8	1053	3.15	11.11	5.43
8G FETs tested at 10 GHz				
3172A- 8(CG)	670	2.69	10.0	4.28
-21(RG)	562.8	1.93	10.9	4.28
-23(CG)	549.4	1.81	8.9	5.35
-27(CG)	623.1	2.38	18.1	5.05
-42(RG)	589.6	2.12	10.6	3.6
-55(CG)	623.1	2.38	14.6	3.76
Unmounted FETs - Not Tested				
3172A-41				
-50				
-53				
-75				

The last ten items in this table show the devices delivered in the second shipment during this period. It can be seen that the power output of 16G FETs from wafer 3147 is almost double that from wafer B642, and that higher efficiencies are also obtained. Since this is a newer wafer, it shows the progress being made in device development.

SECTION V

PLANS FOR THE NEXT SIX MONTHS

Several tasks remain to be done during the final six months of this contract. These include:

- -Development of 32G FETs for use in the final stage of the amplifier module.
- -Continued development and investigation of ohmic contact metallization systems.
- -16G FETs and amplifiers to be evaluated more closely to determine reasons for apparent gain discrepancies.
- -Integration of existing amplifiers with directional couplers to form balanced amplifier stages. This includes a determination of the minimum size of the coupler substrate compatible with good rf performance.
- -Investigation of drain pulsing vs gate pulsing techniques.
- -Evaluation of the pulsed-phase characteristics of cascaded balanced amplifier stages.
- -Development of the output power stage using 32G FETs.

SECTION VI

SUMMARY

During the second six-month period of this program, device fabrication techniques and parameters have been carefully evaluated to achieve improved performance, and amplifiers for the first four stages of the five-stage module have been designed, fabricated, and tested.

Three new vapor phase epitaxial reactors have been constructed during this period with RCA support. The most intensive investigation of material parameters has been done on wafers grown in Reactor C, which is an AsH_3 type. It has been found that excellent well-defined channel layers can be grown on buffer layers which are 1.0 μm or less in thickness.

AuGe ohmic contacts are being grown and evaluated. It has been necessary to develop the sintering techniques to achieve surface smoothness which are compatible with the self-aligned gate process. The resulting contacts are more truly ohmic compared to the Ti/Pt/Au contacts evaporated onto wafers from the same reactor. The AuGe contacts also have lower resistance, and thus, should result in FETs with improved rf performance.

A new FET type using an 8G pattern has been developed during this period. Although designed for an output of 0.5 W, close to 0.7 W with 4.8-dB gain and 32% power-added efficiency has been achieved at 10 GHz. This new FET type is now the best choice for the third stage of the amplifier module.

Amplifiers fabricated for the first two stages have sufficient power and gain for the module requirements. However, the vswr of the first stage using Dexcel 3501A devices could be improved, and the efficiency and power output of the 4G devices used in the second stage should be higher. The power output of the 8G amplifiers needed for the third stage exceeds the stage requirements, but the gain is low. The 16G amplifier stages have shown gain and power capability close to what is required, but at a frequency of 8.5 GHz rather than the desired 9.5 GHz. The 16G devices are being carefully reevaluated to determine if the cause of the amplifier response being too low in frequency is caused by inaccurate measurements of the device S-parameters, or is the result of an unintentional circuit effect producing such feedback from drain to gate.

Interdigitated couplers of small size are being developed for the balanced amplifiers. It has been found that couplers having good rf performance can be fabricated on wide substrates, but the interactions of connector discontinuities with the coupler circuitry degrade performance when smaller substrates are used. Efforts are being made to determine the optimum size of the coupler substrate.

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