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MULTIMODE INFORMATION DISTRIBUTION SYSTEM (MIDS)

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The Multimode Information Distribution System (MIDS) is an advanced, local area communication system capable of simultaneously handling audio, video, and digital data traffic for a large number of subscribers. The MIDS configuration utilizes a broadband coaxial cable transmission medium such as that used by the CATV industry.

20. ABSTRACT (concluded)

The prototype MIDS serves to demonstrate proof of concepts for flag-for-service signaling and supervision as well as an adaptive data rate transmission scheme. This final report describes the MIDS prototype design implemented at The MITRE Corporation in Bedford, Massachusetts and discusses technical limitations for an operational system.

ACKNOWLEDGMENTS

The demonstration of proof of concepts for the Multimode Information Distribution System (MIDS) is the result of efforts by many individuals; only some of them are listed as authors of this document.

At the culmination of the MIDS Project 7040, we would like to acknowledge the original work of Richard P. Witt and his patent disclosure relating to the data modem. Also, we would like to acknowledge the contributions of both Gayle C. Dempsey and R.P. Witt relating to the architectural concepts of MIDS and their associated patent disclosure.

The work of Decio Stone on the CATV network amplifier distortion and temperature effects testing was vital to proving that low-cost commercial components could be used for local information distribution systems such as MIDS. We also acknowledge the support of David G. Willard in the cable/amplifier test program.

In the closing months of the project, the efforts of Paul B. Gill and Roger M. Robillard in completing the design and implementation of the data poller subsystem were much appreciated contributions.

Finally, we wish to recognize engineering technicians Francis Gomes and George E. Schertell for their assistance in assembling and debugging the MIDS prototype hardware. The software for the microprocessor controlling the signaling and supervision keypad unit was written by Valerie Lafleur.

The MIDS project was carried out under the cognizance of Major Neal J. Adams, Project Officer. His support and guidance was indeed helpful. The work was sponsored by the Electronics Systems Division, Air Force Systems Command, under Contract No. F19628-76-C-0001.

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EXECUTIVE SUMMARY

1.1 BACKGROUND

Today the thrust of military modernization programs is to maintain overall force superiority through advanced technology in the face of numerical inferiority. Since our qualitative lead is beginning to decline, however, numbers again become important, and more effective command, control and communication (C^3) systems are required. In the conduct of base and operational missions, improved C^3 systems will provide military commanders with the means to control their forces effectively and achieve real-time responses with reduced manpower. Such systems, in effect, multiply the forces available.

1.1.1 Air Force Technical Needs

To date, developments in communications have concentrated primarily on long-haul capabilities; the success of these developments is increasingly affected by deficiencies in local area information distribution capabilities. The process (and time) to get a message from the originating commander to an entry point, and from the receiving center to the destination, typically involves the

use of slow-speed terminal equipment, even slower human intervention, and is much the same today as it was in the 1940s (Reference 1).

Thus, the principal need in local area C^3 systems (e.g., on Air Force bases) is the ability to interconnect many subscribers within relatively short distances in flexible connectivity patterns and at minimal system cost. For very short distance systems (e.g., within a command center containing a limited number of subscribers), the main objectives are to maximize the flexibility and minimize the complexity, space, weight and power required. Furthermore, the interconnecting means must operate with existing terminal devices and computers, and in all situations reliability and maintainability are very important considerations.

1.1.2 Technical Challenges and Program Objectives

In 1973 a mission analysis of Air Force communications (Reference 2) concluded that the implementation of a fully integrated and multiplexed local distribution system, capable of carrying all types of information (voice, digital data, video), offered significant potential to improve performance and reduce cost at the earliest time. In view of this motivation, the Advanced Communications Technology Program (Project 7040) was established at The MITRE Corporation with the goal of providing a demonstrable

communications concept that would establish a basis for more effective Air Force C^3 systems. The resulting Multimode Information Distribution System (MIDS) had to be transparent in its transfer of information from source to sink with minimum delay, using recent technological advancements in the interests of economy, maintainability and interoperability with existing terminal equipment and computers.

The most crucial technological risk in this program was the achievement of a low-cost subscriber unit to provide an interface between the transmission medium and existing subscriber terminal devices. Among the problems encountered were the limitations imposed by the transmission plant on the ultimate range and quality of information transfer.

Security problems, susceptibility of the transmission plant to willful tampering (sabotage), and the effects of a nuclear electromagnetic pulse (EMP) are not within the scope of this program. However, the emerging fiber optic transmission medium offers much promise in these areas, and this technology will be explored more fully in follow-on programs.

1.2 SYSTEM REQUIREMENTS

The Multimode Information Distribution System, a telecommunication system, must simultaneously distribute voice, digital data, and video traffic to a large number of subscribers.

1.2.1 Operational Requirements

Operational requirements dictate that a multitude of subscribers (at least as many as are now served by airbase telephone equipment) will have to be connected over a geographical area of several square miles. In addition, it is desirable to have call connectivities established in approximately one second or less under worst-hour traffic conditions. Furthermore, in a multimode environment the need exists to allow call modifications (i.e., placing a telephone call in addition to a data or video connection) without disturbing the established connection.

In addition to the conventional point-to-point connections, several new classes of connectivities are required. There is a need to "broadcast" digital data to several subscribers; this is termed one-to-many connectivity. In contrast, there is also a need to allow several users to access a central data file or computer, as in a time-shared service; this is termed many-to-one connectivity.

1.2.2 Data Transfer Requirements

Characteristics of data communications depend in large measure on the end user. Although data rates between digital computers range up to many kilobits (kb) or even megabits (Mb) per second, data rates between human subscribers utilizing electromechanical typewriters are very low, in the range of 100 to perhaps 300 bits per second (b/s). Also, there are combinations of these data rates, for example, where a human user is interacting via a CRT terminal with a computer data base. In this situation, the data rate from the subscriber to the computer is very low; however, to avoid human irritation, the data rate from the machine to the subscriber needs to be very high in order to fill the viewing screen with information in one second or less. Such data traffic tends to be of "burst" form and must be accommodated in a viable distribution system.

1.2.3 Voice and Video Requirements

Design emphasis for the MIDS was directed toward network control (signaling and supervision), and the data transmission subsystem. Since telephone and video subsystems are available commercially, they were not redeveloped in this project, but the network control architecture was designed from the outset as an integrated facility capable of handling the signaling and

supervision (S&S) functions for voice and video as well as for data transmissions.

1.2.4 Interoperability Requirements

Implementation of new distribution systems in operating environments calls for an orderly, hence, evolutionary, changeover to next-generation equipment. It is an economic imperative that the majority of existing data terminals, digital sensors, and computer systems be usable in initial configurations. A MIDS must, therefore, interface a wide variety of devices and overcome a majority of interoperability problems, such as incompatible data rates, code sets, and control protocol. In other words, a MIDS must be totally transparent to the peculiarities of the subscriber's terminal device.

1.2.5 Economic Considerations

Above all, a MIDS must be economically attractive. Even though its features are far superior to conventional systems, the total subscriber life-cycle cost cannot be significantly greater than the existing means of establishing similar communication functions. In particular, the subscriber unit, which interfaces a terminal to the transmission medium, should not cost more than a few hundred dollars.

1.2.6 Technical Assessment

The design of new communication systems involves certain technological risks; therefore, it is necessary to construct a limited prototype system in order to uncover unforeseen practical difficulties. Additionally, it is necessary to perform a technical identification and assessment of possible limitations in order to probe, in depth, areas that cannot be fully implemented or tested in a prototype system. Problem areas so identified should be stressed in future recommendations and recognized in compiling specifications for a testbed application or advanced development program.

1.3 GENERAL APPROACH

To service each end user (subscriber) individually in a local communication system, an approach is employed that interleaves a multitude of information signals into a common medium for later separation and recovery (known as multiplexing and demultiplexing). Instead of using for this purpose a large number of twisted-pair wires emanating from the traditional local switch, a single high-capacity (broadband) coaxial cable pair is routed to all subscribers in a "tree" distribution network, shown in Figure 1-1. To simplify the distribution components used, and to avoid potential interference problems, one cable is dedicated to transmitting information, hereafter called the transmit cable, and the other

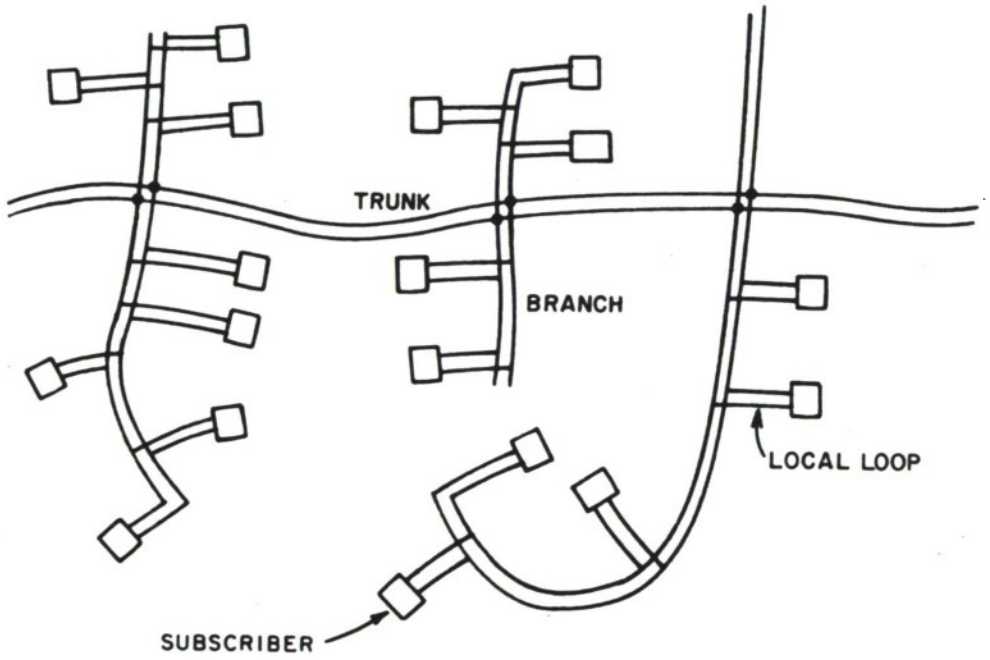

Figure 1-1. Tree Distribution Network

cable is dedicated to receiving information, called the receive cable (each cable is unidirectional).

Network control functions and the audio, video and digital information are controlled by an integrated set of subsystems. As shown in Figure 1-2, each subsystem is allocated a portion of the available frequency spectrum and integrated via the conventional frequency division multiplexing (FDM) technique. The audio and video information is further divided into a large number of FDM channels for individual assignments to subscribers desiring these services.

All of the digital data information is serialized and modulated for distribution on its own frequency channel. This serial data channel is then divided into a large number of message blocks or packets, each with a data channel address header. This technique is called time division multiple access (TDMA) multiplexing, which services all subscribers and conserves bandwidth. Likewise, the network control functions are assigned still different carrier frequencies and distributed via a similar TDMA technique.

Quick response to subscriber demand for service in such a multimode common-user system obviously requires efficient network control functions for proper network operation. For MIDS, the TDMA

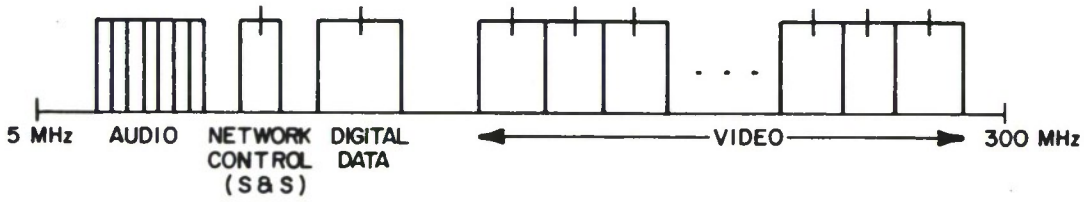

Figure 1-2. Typical Multimode Spectrum Allocation

technique was adopted to accomplish these crucial network control functions because it not only allows service requests to be processed through a centralized digital computer for quick response, but it also makes possible distribution of some of the control functions to the subscriber terminals employing low-cost microprocessors. This distribution of functions utilizing microprocessors provides much of the operational flexibility in the MIDS network.

1.3.1 Network Control - Signaling and Supervision

The network control function is called signaling and supervision (S&S). The subscriber signals a network control computer (NCC) by entering the desired connectivity on a keypad much the same as a conventional telephone user does. The NCC then supervises the establishment of the connection by sending various commands to the subscriber units involved.

The S&S network control was implemented with a unique noncontentious flag-for-service technique that will achieve a one-second average connect time for any one of up to 16,000 subscribers under worst-hour traffic conditions. In this technique, the subscriber gets the attention of the NCC by raising a flag pulse in a unique and dedicated time slot. Then, polling signals from the

NCC (interspaced in the flag-for-service fields) are sent to collect the keystrokes in a response message from the subscriber.

Predetermined keystroke combinations are "dialed" by the user to select the type of connectivity or modification desired. The NCC, on checking and finding a "go" status for the called party, supervises the establishment of the call by sending a transmit and receive channel address for the service required (i.e., data, voice or video frame) to the parties involved. An out-of-band frequency is utilized for these S&S functions so that call modifications (such as connecting a telephone service in addition to a data service) can be implemented without breaking down (disconnecting) the original call. Sometimes this is referred to as a "common channel" S&S technique.

1.3.2 Data Service

With respect to digital data service, it was apparent that to avoid user annoyance, a full page (full-screen video display) should be filled with information in about one second or less. Such service requires a data rate of approximately 19.2 kb/s. Because the user then typically views the information for several seconds, during which no data is transferred, the data flow to each subscriber is of "burst" form.

The approach needed, therefore, was to invent a data subsystem which automatically jumps (adapts) from a low idle rate of, say, 600 b/s to a burst rate of 19.2 kb/s on demand. Since the data subsystem must also be able to handle any intermediate rate to satisfy the specific data rate requirements of the user's terminal device, this subsystem was designed to both conserve bandwidth (everyone can't have a 19.2 kb channel all the time) and provide each user with a burst mode capability when needed.

1.3.3 Implementation Approach

It was anticipated that such a system could be implemented while achieving the prime objective of low subscriber cost. Thus, in looking at hardware implementation for the distribution system, the decision was made to utilize well-proven commercially available CATV (cable television) components such as coaxial cable, line repeater and extender amplifiers, and tap (mixer, splitter) hardware.

To implement complex functions economically in the subscriber unit (which interfaces the user's terminal to the cable), two microprocessors were employed, one for the S&S functions and one for the adaptive data subsystem. The use of microprocessors not only allows terminals of different data rates to be connected, but also allows for code conversions, special formatting, and adaptation to

line protocol requirements for existing terminal devices. Such requirements can be accomplished by changing or modularizing the microprocessor's stored program (firmware). This technique, to a large extent, solves with little extra cost the ever-present interoperability problem. Implementation of this communication concept with conventional hardwired logic would have been cost-prohibitive.

The MIDS implementation employs an integrated set of four units as shown in Figure 1-3. At the subscriber station, an S&S keypad control unit functions with the keypad, while the collocated data buffer unit forms an interface between the subscriber's terminal (via RS-232 conventions) and the distribution cable. At the network control computer, two additional units are required, the S&S poller and the data poller.

At the subscriber keypad control unit, a low-cost 4-bit microprocessor (the Intel 4040) was used to implement the S&S functions of interrogating the subscriber keypad, refreshing keypad displays, communicating with the NCC, and transferring assigned data channel addresses to the collocated data buffer unit.

At each subscriber data buffer unit a 16-bit microprocessor (National PACE) was programmed to handle data buffering, data rate control, and error control. The read/write buffer memory of this

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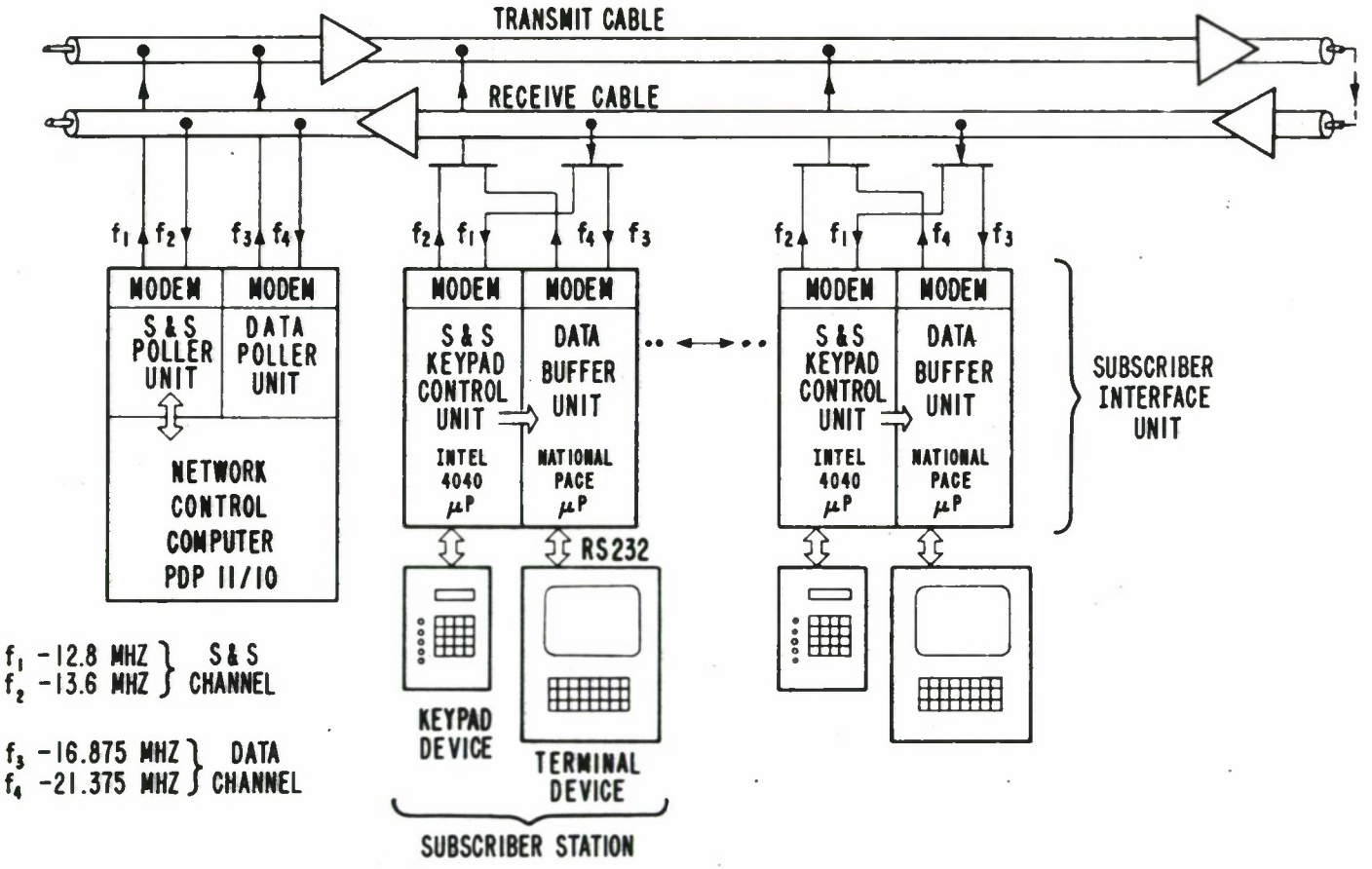

Figure 1-3. MIDS Architecture

microprocessor stores the data packets temporarily. When its buffer memory is almost filled with data from the terminal device, the microprocessor can request high-speed (burst) service to unload. If this transmitted rate is too fast for the connected subscriber's terminal, the mircoprocessor at the receiving station can slow down or halt the flow of information over the cable. The rolls are, of course, reversed for a two-way (duplex) data conversation. Since the subscriber data buffer microprocessor also controls the send and receive functions for the attached terminal, data overruns and resulting data losses are prevented. Thus, different data rate terminals are accommodated, with the slowest receiving device in any particlar connectivity controlling the maximum data rate. The details of how this adaptive data rate scheme works are contained in Appendix B.

In addition, if errors are detected in the transmission of data over the cable, retransmission of the applicable packets are initiated by the data buffer's microprocessor. The additional task of terminal code conversions to a "universal" code could also be accommodated through the power of this microprocessor.

The S&S poller unit, located at the network control computer, originates the flag-for-service time slots and interspaces polling and control messages for subscriber units. In addition, it receives service request flags and subscriber responses. A 16-bit PACE

microprocessor is utilized to interface the S&S poller to the PDP-11 network control computer.

The data poller unit, located near the NCC (but not connected to it), emanates a sequence of polls to allow subscribers (which have been assigned data channel addresses) to transmit their data messages in 64-bit data packets. On request, this poller inserts additional polls between the regularly sequenced polls to achieve the high-speed burst transfer service occasionally required. Again, a 16-bit PACE microprocessor is utilized for this unit.

In effect, the adaptive data subsystem thus implemented allows each MIDS subscriber to appear to be using a high-rate (19.2 kb/s) data communication channel. The MIDS was designed with a serial throughput rate of 2.25 Mb/s for the data channel providing for a maximum of 1,024 subscribers communicating simultaneously at an idle rate of 600 b/s; in addition, up to 32 subscribers may automatically jump to 19.2 kb/s for burst transfer. If more than 32 subscribers need burst service simultaneously, the adaptive data subsystem will proportion available capacity to all requestors.

In order to transmit and receive S&S signals and digital data information on the coaxial cable at specific frequencies, special modems for both the S&S and data subsystems had to be developed, because such modems were not available commercially to meet the

configuration and specifications required. The S&S modems employ the conventional modulation technique of amplitude shift keying (ASK) at a base rate of 25 kb/s. The digital data modems employ a novel three-phase modulation (TPM) differential phase shift keying (DPSK) technique. Data modems operate at a base rate of 2.25 Mb/s, which allows the carrier signal to simultaneously convey data, sync, and clock information.

1.4 ACHIEVEMENT

The primary objective of the project was achieved. MITRE demonstrated that a low-cost subscriber unit can be built to interface a local broadband distribution system with existing terminals. Such a unit is shown in Figure 1-4. High-volume production costs are estimated at $200 to $300 per unit. A typical subscriber station is shown in Figure 1-5. Performance of the CATV components allows such local distribution systems to be extended for distances up to at least 20 miles.

1.5 FUTURE PLANS

It is anticipated that the demonstration of this type of system will generate the necessary interest to consider a testbed or operational application.

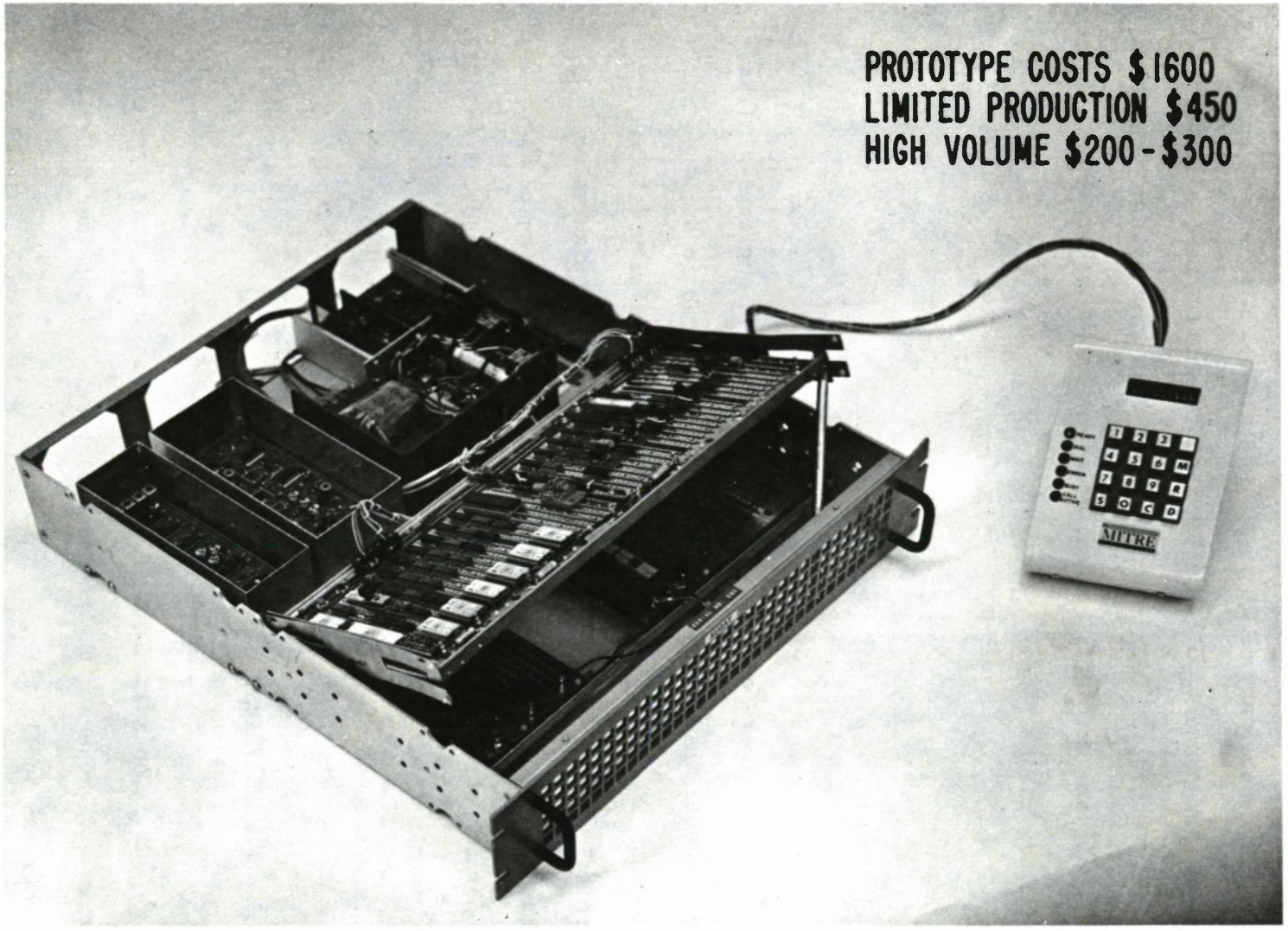

Figure 1-4. Subscriber Keypad and Data Buffer Unit

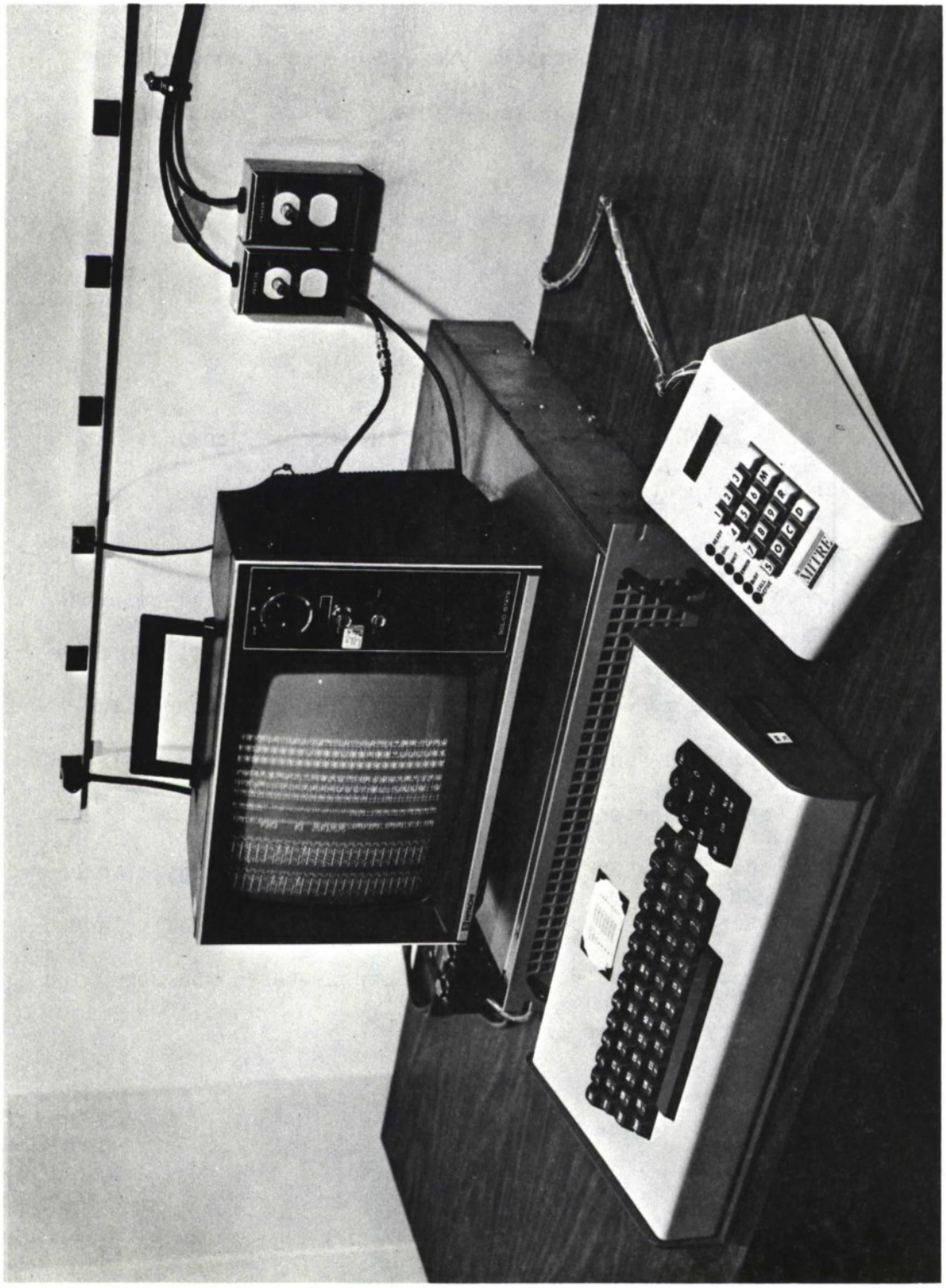

Figure 1-5. Typical MTDS Subscriber Station

Certain technical difficulties remain to be solved. A multiplexed system employing a common distribution scheme is subject to a security breach. Furthermore, the effects of a nuclear EMP could render terminal equipment inoperable. Future plans are directed toward employing a fiber optic transmission medium to overcome these potential problems.

1.6 PREDICTED IMPACT

The conversion to or provision for "softcopy" terminals at each subscriber's location will certainly improve response times. With access to key data base information directly from the computer files and remote information processor, the commander will be better informed as to the current status of his resources and will be able to deploy his forces more accurately and in a timely manner. The attendant reduction in "hardcopy" paperwork reduces considerably the support manpower now necessary with conventional systems. Connecting present computer facilities and existing terminals to an information distribution system such as MIDS will allow well-planned evolutionary C^3 concepts to reduce significantly the number and kind of interoperability problems existing today.

SECTION 2

MIDS DESIGN CONSIDERATIONS AND DESCRIPTION

2.1 GENERAL CONSIDERATIONS

The Multimode Information Distribution System provides an advanced local area communication facility capable of simultaneously handling audio, video and digital data traffic for a large number of subscribers in a variety of connectivity patterns. The user's desired connectivity is entered via a keypad much the same as in a modern Touchtone® telephone set. Since three modes would be available in a fully expanded system, the user not only "dials" the called party's number, but also specifies the type of service desired, i.e., audio, video or digital data.

The keypad device is shown in Figure 2-1. It utilizes visual indicators for human interaction to convey the call status and display the called number as entered. The detailed operational aspects of the keypad control unit are described in detail in Appendix A.

Signaling and supervision (S&S), which conveys keystroke and call connectivity information for a maximum of 16,384 subscribers, is provided via a separate out-of-band channel. The serial bit stream used to convey this information between the NCC and the

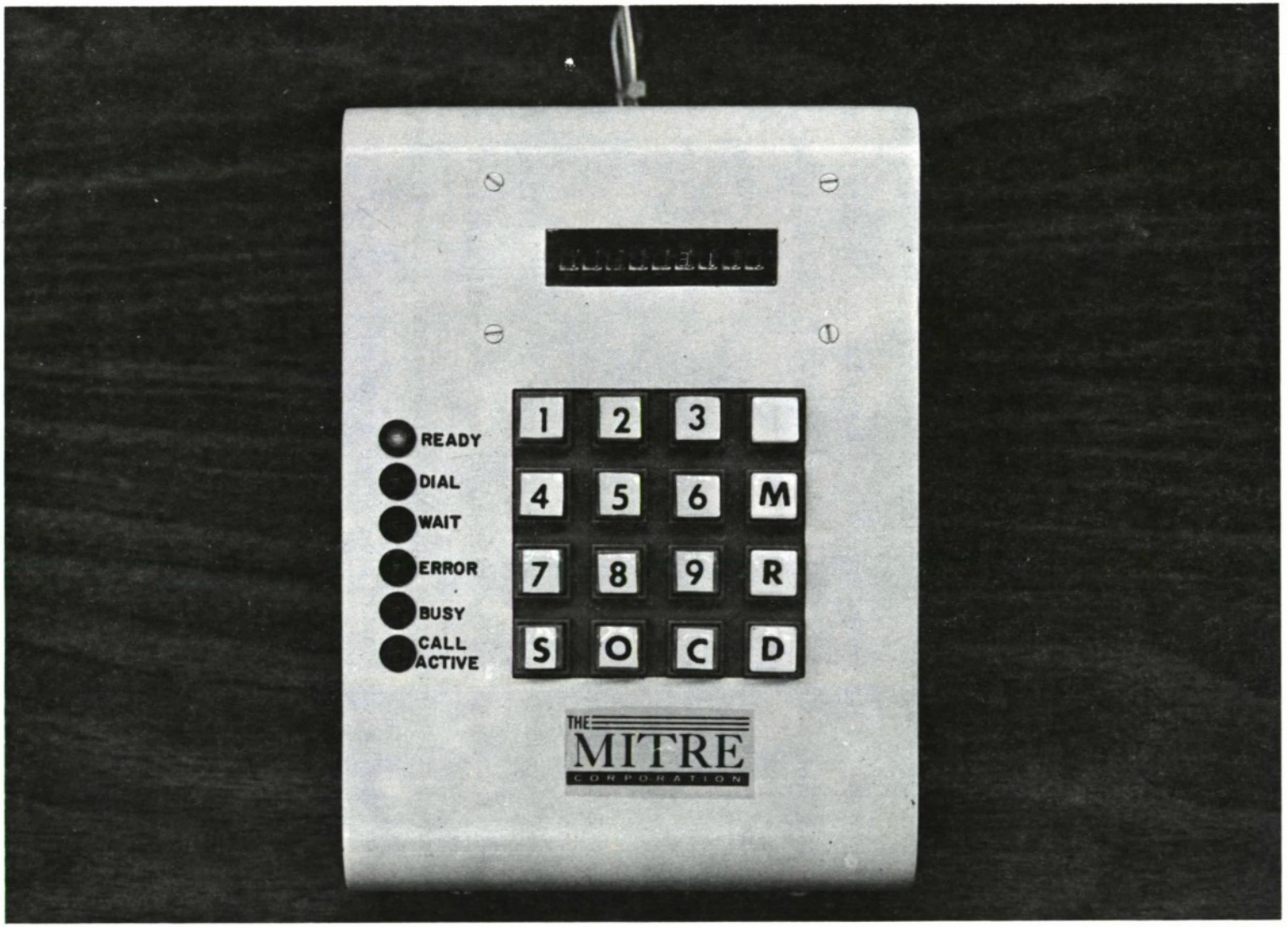

Figure 2-1. MIDS Keypad Unit

subscriber has a transmission rate high enough to attain a one-second response time. To accomplish this response under worst-case conditions, serveral general considerations apply.

Approximately two calls per hour placed by each subscriber is taken as a worst-hour traffic condition. Since there are over 16,000 possible subscribers, the S&S subsystem must handle well over 32,000 calls per hour, which for all practical purposes is equivalent to approximately 10 calls per second. In this subsystem, roughly 500 bits of information (not consecutive) are required to collect keystrokes and convey the data channel addresses for a single call; therefore, an average serial bit rate of approximately 5,000 b/s is required to establish connectivities under these conditions. To these requirements, however, 16,384 uniquely positioned bit times must be added to provide noncontentious "slots" for flag-for-service requests from the subscribers. The total rate required, then, is something over 21 kb/s, which is rounded up to 25 kb/s for the S&S subsystem bit rate specification. Bit formats and protocol for the S&S system are described further in Appendix A.

The adaptive data subsystem utilizes a serial bit stream with a polled TDMA protocol to transfer data packets between subscribers who have been assigned data channel addresses by the S&S subsystem. For the maximum size of systems under consideration, it was felt that 1,024 addresses would be sufficient to handle data-type

connectivities. Also, it was felt that an idle rate of 600 b/s would be more than sufficient for base rate service. The resulting serial bit rate required is, therefore, approximately 600 kb/s. In addition, it is desirable to allow a small number of users (up to 32) to transition to the higher rate of 19.2 kb/s for burst data transfer. This requires an additional capacity on the serial bit stream of 600 kb/s. Furthermore, each data packet must be burdened with the overhead of an address header and a polling field, which increases the rate by a factor of 104/64. Hence, the combined serial data rate required is slightly over 2 Mb/s and is rounded up to 2.25 Mb/s for the capacity of the MIDS data channel.

This adaptive data subsystem allows for graceful degradation of burst mode service. That is, if more than 32 subscribers need high-speed service simultaneously, everyone will be serviced but at a proportionately lower average rate. For example, if 64 subscribers simultaneously requested high-speed service, they would each be allowed to transmit at an average rate of 9.6 kb/s instead of at 19.2 kb/s.

The split of MIDS data service capacity that allocates one-half to base rate service (1,024 subscribers at 600 b/s) is arbitrary. A more judicious choice can be made once a better picture of traffic loads and demand factors is understood. Perhaps an even better solution is to extend the design of the adaptive data

system to automatically allocate the total capacity between low- and high-speed service between the ranges of 110 b/s to perhaps 50 kb/s.

Although audio and video service modes are not implemented in the prototype hardware, the fundamental design considerations include their requirements in the S&S subsystem architecture. For example, in the case of telephone service using a system like the Collins ATX-101, the FDM channel assignments may be conveyed via the MIDS S&S hardware. A modular addition to the keypad microprocessor firmware, implemented in its read-only memory (ROM), would handle this option. Likewise, for a static-frame video system, the channel and frame number would be handled in a similar fashion by the S&S subsystem.

The MIDS described here is intended for operation in the MITRE-Bedford building complex on an existing cable system known as the MICOM. Because of prior spectrum allocations on MICOM, operation of the MIDS is further constrained. Ramifications of these and other constraints are considered in the following subsections.

2.2 NETWORK CONFIGURATION AND SPECTRUM ALLOCATION

Connectivity among all subscribers and the network control elements in MIDS is realized by a dual coaxial cable configuration.

The total bandwidth available in the cable distribution facility is 295 MHz, limited by the passband of the cable amplifiers, which is between 5 and 300 MHz. The portion of this total frequency spectrum presently assigned to MIDS is from 12 to 24 MHz. Within this 12-MHz band on the MICOM cable system lie the MIDS channel assignments for signaling and supervision, and for digital data service.

The present MICOM frequency allocation is shown in Figure 2-2, referenced to the dual cables, transmit and receive. In addition to MIDS, allocation is provided for FDM telephony, the MITRIX system (an alternative information transfer system), several TV channels, and FM radio. This represents a typical multimode frequency allocation.

An enlarged view detailing the specific MIDS channel locations within the 12- to 24-MHz range is given in Figure 2-3. Transmission carrier frequencies and signal bandwidths for the various MIDS channels are shown in Table 2-1.

The S&S channels (f1, f2) support the information flow associated with subscriber signaling, NCC terminal status monitoring, and supervision of desired call connectivities. These channels employ amplitude shift keying (ASK) at a rate of 25 kb/s.

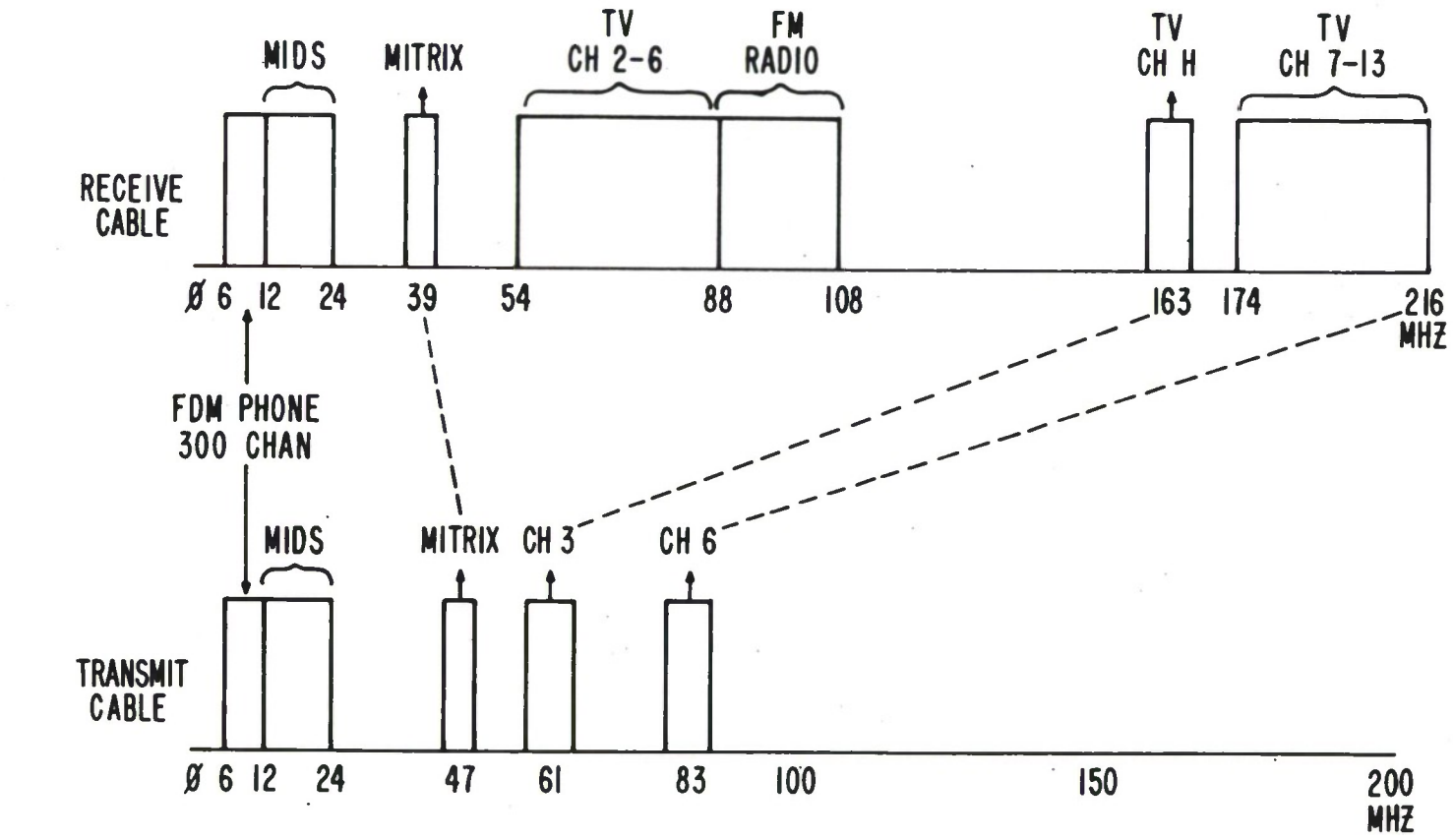

Figure 2-2. MICOM Frequency Spectra

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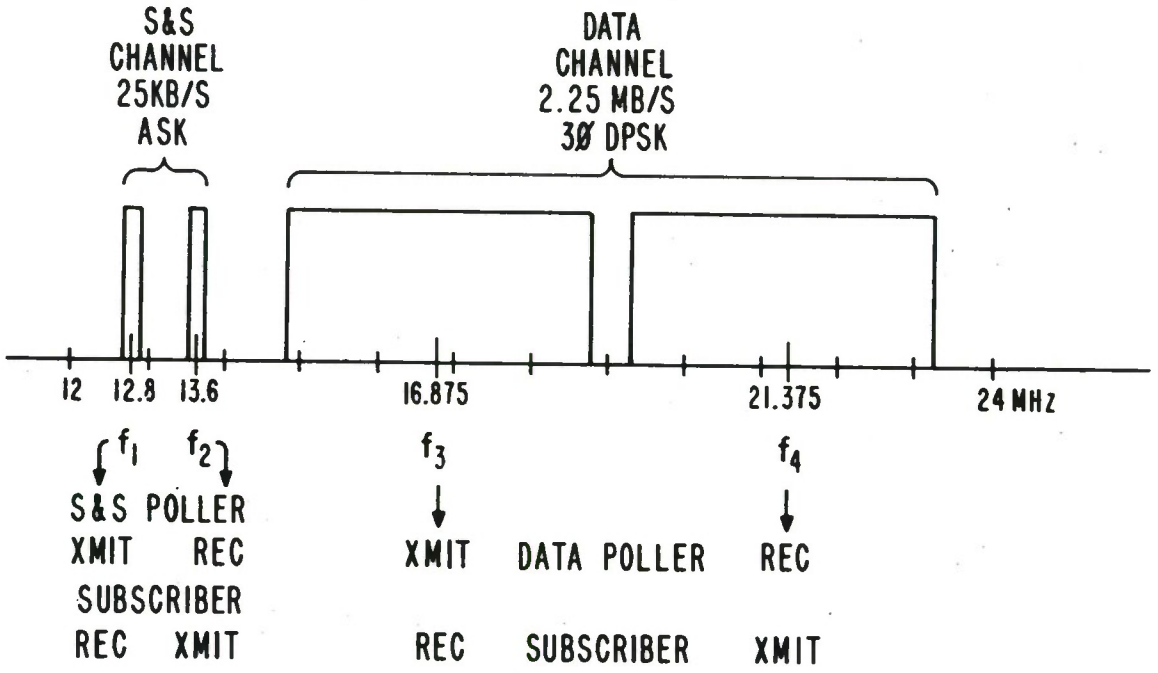

Figure 2-3. MIDS Frequency Spectrum

TABLE 2-1

MIDS CARRIER FREQUENCIES AND CHANNEL BANDWIDTHS

Channel	Transmission Frequency	Channel Bandwidth
S&S Poller	f1 = 12.8 MHz	100 kHz
S&S Subscriber	f2 = 13.6 MHz	100 kHz
Data Poller	f3 = 16.875 MHz	4 MHz
Data Subscriber	f4 = 21.375 MHz	4 MHz

The data channels (f3, f4) support the flow of TDMA high-speed data services at a total throughput rate of 2.25 Mb/s. This data service may be shared among subscribers in such a manner that each may transmit, on demand, at a maximum effective burst-mode data rate of 19.2 kb/s. When the burst transmission mode is not needed by a subscriber, the effective data rate automatically reverts to 600 b/s. Digital modulation for the MIDS data subsystem utilizes three-phase differential phase shift keying (DPSK).

Utilization of two S&S channel bands and two high-speed data channel bands in the MIDS spectrum allows the NCC to be located anywhere along the cable system. This utilization will also allow physical redundancy in the system control element to provide backup in the event that one NCC malfunctions or becomes inoperative in a

tactical environment. The physical connection, or interface, of the NCC to the cable distribution system is treated in the same manner as for any of the subscriber units. The requirement for such modularity was felt sufficient to warrant the attendant doubling of the number of channel bands within the MIDS spectrum.

A simplified alternative could be implemented if the NCC were placed at the head-end of the distribution cable. In this case only one S&S band and one data band would be required, and would therefore require only one-half of the present bandwidth for these functions. However, the vulnerability of a single controller location is unacceptable for most military applications.

The basic MIDS network configuration was shown in Figure 1-3. All units transmit on the transmit cable at the appropriate frequency and level of 200 mV rms. The signals traverse the transmit cable and are looped around onto the receive cable at the MIDS bandpass filter, where the physical connectivity of the transmit and receive cables is established. Desired signals are taken, by subscribers or the pollers, from the receive cable. The received signals are in the level range of 1 to 10 mV rms, which is within the dynamic range of the S&S and data receivers (demodulators).

Details on the S&S and data pollers, subscriber data buffer, S&S keypad control unit, and modems are given in the appendices of this document.

2.3 S&S SUBSYSTEM CONSIDERATIONS

2.3.1 Alternative S&S Techniques

A number of common channel S&S techniques were considered in the preliminary design phase of MIDS. Basic considerations on the choice of an S&S technique are documented elsewhere. Three alternatives considered were: roll-call polling, a contentious scheme such as used in the ALOHA system (Reference 3), and a flag-for-service technique.

As the MIDS facility is intended to support a large number of subscriber terminals, it was felt that roll-call polling would probably result in a monumental overhead inefficiency, and a contentious technique would be dangerous in peak-load situations because of the attendant increase in system response times. The flag-for-service technique, therefore, was elected as the S&S method for MIDS, and this technique is described in the following paragraphs.

2.3.2 Flag-for-Service Signaling and Supervision

The information format on the MIDS S&S channel is illustrated in Figure 2-4. Each time frame contains 64 S&S message blocks; each message block is divided into a flag-for-service field and a message field. The flag-for-service field contains 256 bit times, which, when repeated over 64 message blocks, yields 16,384 bit positions.

A flag-for-service technique is used to handle requests for service from any of a possible 16,384 subscribers. Each subscriber keypad is assigned a code (directory address) that corresponds to a unique bit position in the field of 16,384 bits in the time frame. Starting with the beginning of each time frame, the keypad control logic counts each bit received (in the flag-for-service field) on the receive cable until its assigned bit position is reached. At this point in time, the keypad control logic may send a flag-for-service pulse on the transmit cable if required. The subscriber, in entering a service request by depressing appropriate keys on the keypad unit, causes the flag-for-service pulse to be sent.

The S&S poller recognizes the flag-for-service pulse because of its time position and then polls that subscriber by sending the directory address of the subscriber keypad in the next available message field. When the keypad recognizes that it is being polled,

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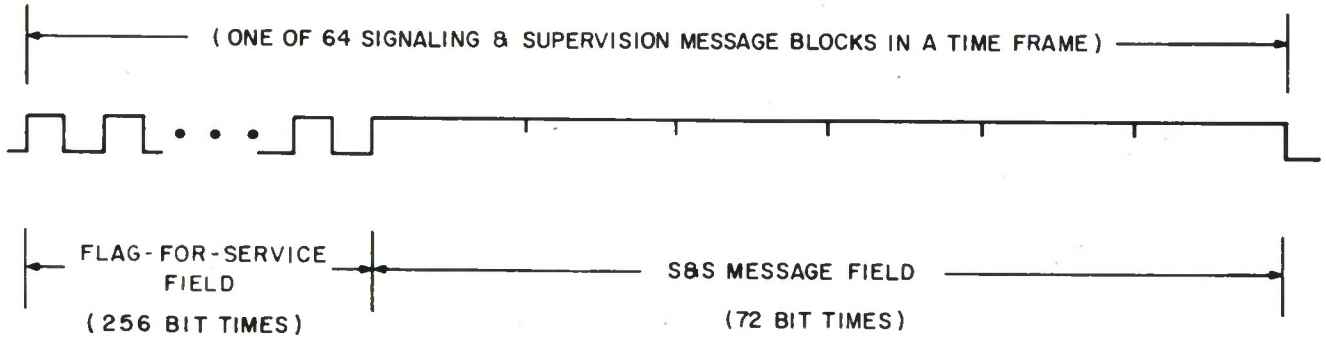

Figure 2-4. S&S Subsystem Message Fields

it responds by transmitting its stored keystrokes and status information on the transmit cable during the time occupied by the next message field. The S&S poller accepts the keystroke-status information, which conveys the subscriber's request, and forwards it to the NCC. (The remaining 63 message blocks in the same time frame are available for "simultaneous" servicing of other subscribers.)

The NCC then checks availability of equipment involved in the desired connection. Based on the availability, the network control computer sends the necessary data channel receive and transmit addresses (called indirect addresses) to the keypad control unit for transfer to the subscriber data buffer unit. Data transmission between subscribers may then begin on the data channel.

The message format for the S&S message field uses six 8-bit characters. Character transmission is performed on a conventional start-stop asynchronous basis and requires the overhead of a start, parity, and two stop bits. The total message field for the six characters is therefore 72 bits long.

2.3.3 S&S Modulation

Modulation of the binary information on the S&S channel is accomplished by amplitude shift keying the appropriate RF carrier signal. This type of modulation was chosen for its relative

simplicity and ease of implementation. Carrier frequencies for the S&S subsystem are 12.8 MHz and 13.6 MHz corresponding to the outputs of the S&S poller and subscriber stations respectively.

Design details of the S&S subsystem are described in Apppendix A.

2.4 ADAPTIVE DATA SUBSYSTEM CONSIDERATIONS

2.4.1 Message Block Format and Information Flow

The MIDS adaptive data subsystem is based on a form of polled, time division multiplexing and will accommodate up to 1,024 simultaneous data users. The data poller sequentially polls all 1,024 addresses in its polling table. These data channel addresses are not assigned permanently to any particular terminals and do not correspond to the fixed directory addresses of the terminal keypad units. For this reason, the addresses assigned by the NCC for data distribution in the adaptive data subsystem are called indirect addresses. This indirect addressing feature allows up to 1,024 end terminals to time-share the data channel, out of a maximum possible population of 16,384 subscribers.

The structure of the data poller message block used on the MIDS data channel is illustrated in Figure 2-5. During the polling

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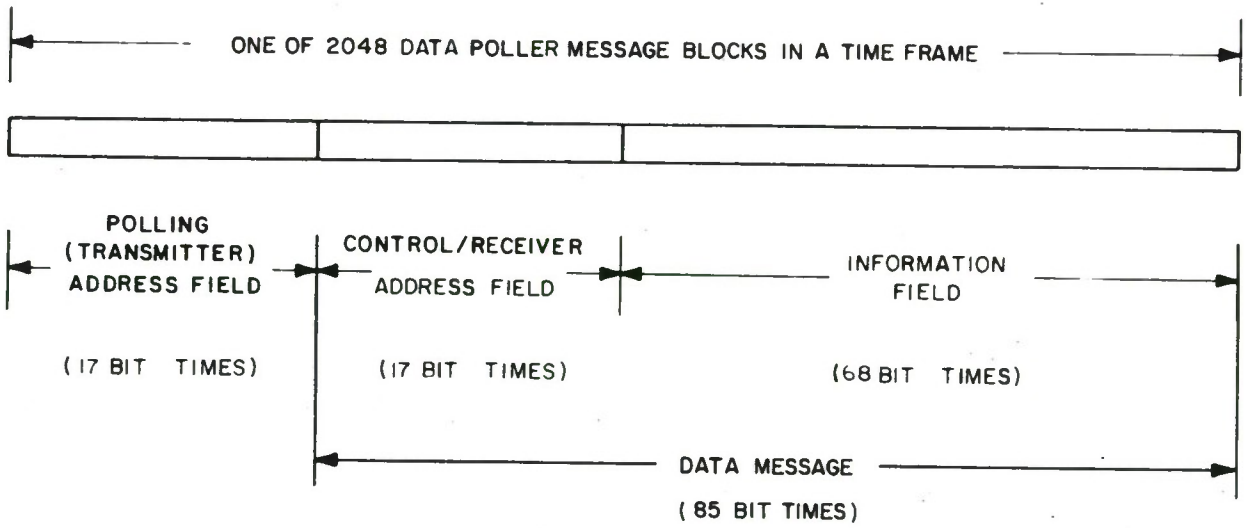


Figure 2-5. Data Poller Message Block Format

(transmitter) address field time the data poller sends the address of the terminal that is expected to transmit. When the polled terminal recognizes its address on the receive cable, it uses the remaining 85 bit times to send its data message on the transmit cable. The data message contains a control/receiver address field (17 bits) followed by an information field. The information field contains the remaining 68 bits, which consist of four 16-bit words with each word followed by a single parity bit. This message traverses the transmit cable, is looped onto the receive cable at the MIDS bandpass filter, and is received by the data poller, which retimes and inserts the message onto the transmit cable destined for the intended receiving subscriber, thus completing a typical transmit-to-receive cycle.

2.4.2 Adaptive Data Rate Concept

A unique feature of the adaptive data subsystem is the fact that the effective data rate to any particular terminal (governed by how often the terminal is polled by the data poller) is adapted automatically to fulfill the traffic activity demands of that terminal. This adaptive data rate permits the system to automatically switch a terminal from a basic 600-b/s data rate to a much higher speed of 19.2 kb/s as demanded by terminal traffic activity. Of the 1,024 simultaneous on-line terminals, any 16 pairs of terminals are permitted the higher data rate at any one time.

The interaction of the 600-b/s and 19.2-kb/s data rates can be visualized as operation of two circular polling queues shown in Figure 2-6. The poll address selectors within the circular queues rotate at different speeds. The 600-b/s data rate terminal devices are on the low-speed selector rotating at 10.56 revolutions per second (r/s); therefore, each subscriber is polled 10.56 times per second to send the four 16-bit words, which result in a data rate in excess of 600 b/s. Terminal devices requiring 19.2-kb/s data rate service are assigned temporarily to the high-speed selector rotating at 338 r/s. Alternate interleaving of poll addresses from the two queues provides the time division servicing of all terminals that may be active.

Automatic adaptive data rate service is provided by monitoring the output buffer in each subscriber data buffer unit, thereby permitting efficient dynamic allocation of capacity. As a subscriber output data buffer fills up, the polling rate to that subscriber data buffer is increased, providing the high data rate transfer and a rapid screen fill time required for visual display terminals. As the buffer is emptied, the polling rate reverts to the lower effective data rate. This lower data rate is more than sufficient to handle normal keyboard activity of 15 characters/second and yet maintain terminal connectivity so that rapid data transfer can take place without the need for re-

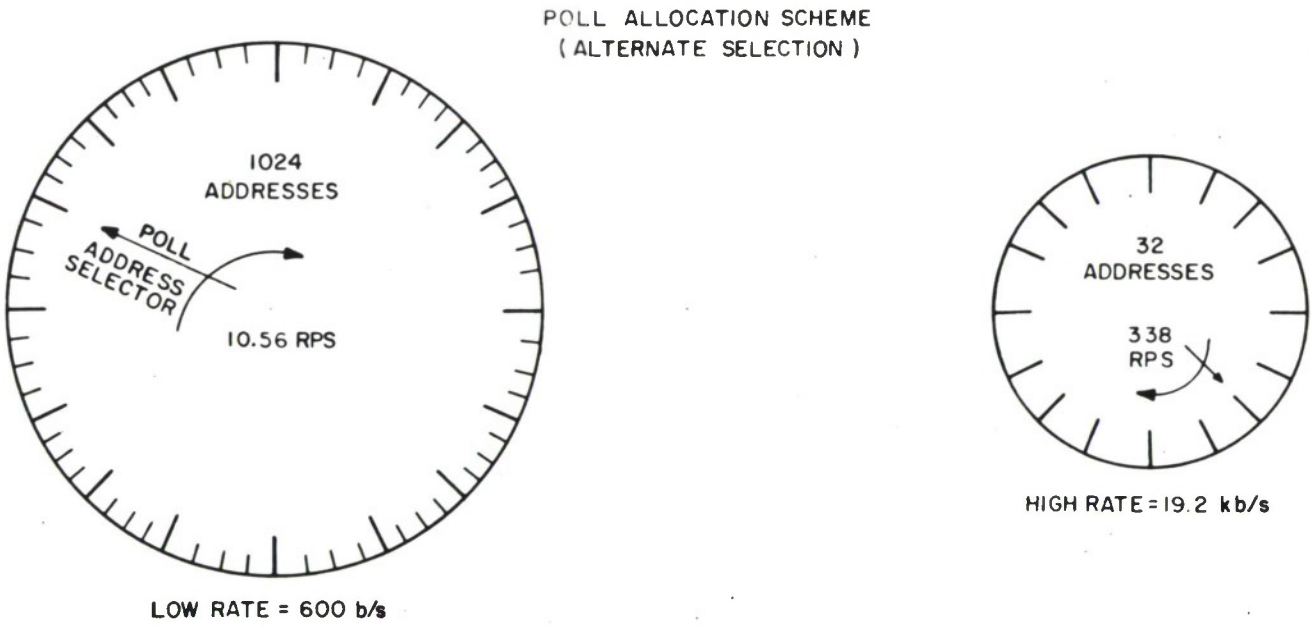


Figure 2-6. Self-Adaptive Data Rate Polling Analog

establishing a connection for each transmission. Design of the data channel is described in detail in Appendix B.

2.4.3 Data Modulation

Modulation of the binary information on the MIDS data channel utilizes a unique form of differential phase shift keying with three phases to encode the information. A number of considerations led to the choice of this three-phase DPSK technique; the major considerations are highlighted as follows:

a. The three-phase modem as designed can recover, at the receiving end, the timing information, data and synchronization from the RF carrier. The phase state of the carrier frequency is guaranteed by the encoding process (discussed in Appendix C) to change each and every bit interval, allowing clock recovery so that data can be clocked in at the proper instants. Obtaining synchronization from the RF signal, so that clocking begins at the correct instant, means less complexity in the logic circuitry of the modem. (There is no need to incorporate logic circuits whose sole function is to search constantly for a logically encrypted sync word.) Encoding the sync in the RF signal also gives good channel utilization efficiency, since only two bit intervals are used for a sync pulse.

b. With differential PSK, as opposed to coherent PSK, there is no need for a highly stable reference signal. With differential PSK, only short-term stability between consecutive phases is required.

c. Phase shift keying is known to have a relative noise immunity advantage over other methods of carrier modulation (References 4 and 5). This noise immunity in conjunction with simple single-bit parity checking will give good reliability for the received data.

d. The information and synchronization encoding could be accomplished by using four phases, but this would require more electronics in the transmitter generation and receiver detection of the extra phase state. Also, a three-phase system can withstand greater phase deviations than a four-phase system.

Details on the three-phase encoding scheme and the data modem are found in Appendix C.

2.5 INTEROPERABILITY CONSIDERATIONS

Data formats and transfer protocol on the cable establish a "universal" medium for connected users, and the MIDS subscriber data

buffer forms the interface between this cable and the user's terminal device. Since most existing terminals utilize the popular EIA RS-232 interface standard, the MIDS data buffer accommodates this connection. Other interface standards could be accommodated with minor alterations to the terminal interconnect cable and to the data buffer's microprocessor firmware.

Even though a specific interface standard was adopted, at least three parameters still impact the interoperability of existing terminals: data rate differences, character code incompatibilities, and peculiar operational requirements such as mechanical line feeds and carriage returns. However, the MIDS data buffer, through the power of its 16-bit microprocessor, can overcome these difficulties. Actually implemented is a technique to overcome the most difficult aspect of interoperability -- data rate incompatibility. The MIDS adaptive data rate scheme automatically paces the data transfer so as not to overrun the slowest receiver connected in any call. Furthermore, a transfer protocol was implemented which, if transmission errors are detected on the cable, automatically retransmits the same message. To overcome additional difficulties, the microprocessor can be programmed to handle code conversions and padding characters for electromechanical terminals.

One solution to terminal interoperability problems lies in modularizing a section of the microprocessor's program memory,

residing perhaps on a single, integrated-circuit ROM chip. This chip would tailor the MIDS data buffer to the correct personality for a specific terminal type, data rate, and code set. A further extention of this philosophy is to have all combinations reside within a larger ROM and select the characteristics of the terminal, via switches, to let the data buffer know what kind of terminal is connected to it. Perhaps the ultimate arrangement is to let the data buffer microprocessor interact with the connected terminal for the purpose of determining the appropriate parameters.

In any case, one of the many advantages of using microprocessors becomes apparent: A small cost increment in memory allows software to eliminate hardware differences found in existing terminal devices.

2.6 ECONOMIC CONSIDERATIONS

From the outset, economic factors were a prime consideration in the MIDS design. The physical distribution system is based entirely on economical and proven components utilized by the CATV industry. Included here are the rugged line and extender amplifiers, solid shielded coaxial cable, and conventional mixer/splitter hardware, all of which are designed for exterior use in an all-weather environment.

The subscriber interface unit was implemented with current microprocessor technology, which in effect can replace conventional integrated circuit logic designs by chip-count ratios of 50 to 1. In other words, a few additional chips associated with the microprocessors replace several hundred, with resultant reductions in numbers of circuit cards, chassis, and power supply requirements. Shown in Table 2-2 is an estimated cost analysis (including both material and labor) for the subscriber unit in the prototype version and limited-production version (which simply replaces wire-wrap boards with etched circuit boards, and development EPROMs with high-density masked ROMs).

For high-volume production of several thousand units, consideration would be given to implementing the S&S and data buffer microprocessors with single-chip microcomputers which cost approximately $5 to $15 each. The projected high-volume unit cost is in the neighborhood of $200 to $300 with the majority of the cost in the data modem, power supplies, and chassis hardware.

With such low-cost interface units and a distribution plant, a MIDS would be cost-competitive with conventional switched telephones equipped with data modems. In addition, a MIDS brings to each subscriber the many features and advantages of a truly multimode system in terms of high data bandwidth, video information, and flexible connectivities.

TABLE 2-2

ESTIMATED COST ANALYSIS FOR MIDS SUBSCRIBER UNIT

	Prototype	Limited Production
S&S Logic and Micoprocessor	$ 300	$ 70
Data Buffer and Microprocessor	450	100
Power Supply	150	115
S&S Modem	35	10
Data Modem	120	80
Mixer/Splitters	5	5
Chassis and Hardware	400	90
Keypad Unit	100	50
Total	$1,560	$420

Maintenance costs are minimized through the use of proven CATV components and simple microprocessor circuits with reduced chip counts. Internal test routines could be included within each microprocessor's program which would direct service efforts in pinpointing problems. Furthermore, subscriber locations may be changed easily by merely disconnecting the interface unit from a wall outlet and reconnecting it at a new location. Simple modifications to the subscriber unit may be handled through "firmware" (changing plug in ROMs) which will extend its useful life. All these factors aid in reducing the life-cycle cost of a MIDS.

SECTION 3

POTENTIAL TECHNICAL LIMITATIONS

3.1 GENERAL PERSPECTIVE

A fully operational MIDS can support a large number of communication channels, all on the same coaxial cable medium. The various channels can include signaling and supervision, high-speed TDMA data, and several channels of telephone and video communications. The technique used to interleave and separate all these signals on the common coaxial cable is frequency division multiplexing (FDM). Exploiting the available bandwidth of the distribution system means packing as many channels as possible into the spectrum without creating serious interference and degradation. This section examines a number of potential technical limitations that may exist in a communication system such as MIDS, and reports the results of certain measurements made on typical CATV system components (trunk amplifiers and the cable itself). This examination supports the conclusion that a fully operational MIDS is technically feasible.

3.2 CABLE CHARACTERISTICS

This subsection discusses the electrical characteristics and related transmission impairments of the coaxial cable used for

signal distribution in the MIDS. Two cable types, typically used in the CATV industry, have been considered for use in the MITRE experimental cable system. Both cables have a copper-clad aluminium center conductor and a seamless aluminum outer shielding with a black polyethylene jacketing. The cables differ in their dielectric insulating material. The cable characteristics discussed here are losses, attenuation uniformity, attenuation stability, shielding, propagation delay, and dispersion.

3.2.1 Losses

The resistance of a coaxial cable gives rise to energy dissipation in the form of heat and, hence, losses. Cable attenuation (usually expressed in dB/100 ft) should be known accurately so that appropriate spacing for the repeater amplifiers may be determined.

Attenuation of a coaxial cable is not constant over the frequency range of interest (5 to 300 MHz). The attenuation increases exponentially as the square root of frequency; thus the higher frequencies are attenuated more than the lower frequencies. Complex time domain signals are composed of a number of different components in the frequency domain. Nonuniform attenuation of these components across a particular channel gives rise to attenuation distortion. If, however, cable attenuation as a function of

frequency is known, then compensation for the nonuniformity usually is provided by the cable amplifier's slope gain control.

Cable attenuation versus frequency for the two cables considered is shown in Figure 3-1. It is seen that cable attenuation in dB/100 ft versus frequency is linear with logarithmic scaling on both axes. The highest attenuation, at 300 MHz, occurs for the JT1412J cable with a polyethylene dielectric. This worst case gives slightly less than 2 dB/100 ft. Figure 3-1 is valid at a nominal temperature of 68°F. Attenuation at other temperatures can be predicted from the fact that the attenuation changes by 1% of the nominal value for each 10°F deviation from the nominal temperature, with higher temperatures causing greater attenuation. The cable attenuation variation with temperature can be balanced by the use of thermal compensating circuits. These circuits, associated with the cable amplifiers, are designed to have the opposite temperature characteristics, namely less loss with higher temperature.

Since cable attenuation specifications and variation with temperature are well known and have been confirmed by laboratory measurement in an environmental chamber test setup at MITRE, it appears that attenuation distortion and signal level imbalance will not adversely affect the performance of a MIDS.

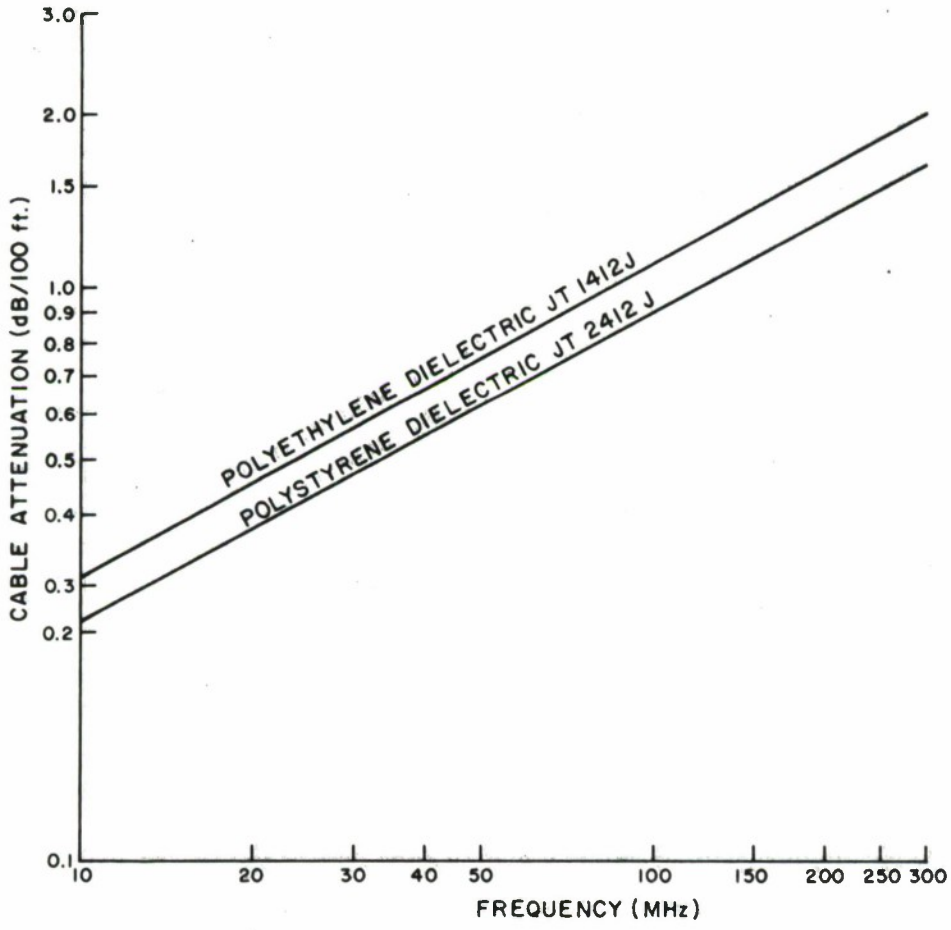


Figure 3-1. Cable Attenuation Versus Frequency at 68°F

3.2.2 Attenuation Uniformity

Much literature on CATV coaxial cable performance has been devoted to the subject of impedance irregularities in the cable. Such irregularities have been classified into two groups: discontinuities of random magnitude distributed randomly along the cable length, and a set of regularly spaced (periodic) discontinuities, each of which has a very small magnitude. The origin of these discontinuities occurs in the manufacturing, handling and installation of the cable, and each of these discontinuities represents a localized impedance variation in the cable.

When a propagating electromagnetic wave encounters such a local impedance irregularity, part of the wave is reflected backward. The periodically spaced discontinuities can cause a greater impairment compared to the random discontinuities because the reflections from regularly spaced discontinuities, although each one is small in amplitude, are phased precisely at certain frequencies. When the spacing between irregularities is equal to an electrical half-wave length, these precisely phased reflections arrive back at the input end of the cable and cause narrowband attenuation spikes at the frequencies involved. In one particularly severe case (Reference 6) a field engineer returned a reel of cable that would not pass TV Channel 6 (located between 82 to 88 MHz).

Laboratory testing of this particular reel of cable resulted in the discovery of an attenuation peak deviating 50 dB above the nominal loss curve at precisely 87 MHz.

It is felt that with proper return-loss testing a faulty cable section can easily be identified and rejected. If return-loss measurements are performed by the cable supplier, cable irregularities caused by the manufacturing process will be screened out. Careful handling and installation practices should be followed in order to prevent the creation of random irregularities as a result of tight bends (the minimum bending radius is recommended to be greater than 10 times the cable's outer diameter). If such testing and handling procedures are followed, problems with mechanical irregularities will be minimized.

3.2.3 Attenuation Stability

Attenuation stability refers to the ability of the cable to maintain its nominal frequency response characteristics when exposed to changing environmental and mechanical conditions. In addition to variations in attenuation due to temperature changes, the attenuation of a coaxial cable can increase with time and flexure. Cable manufacturers (Reference 7) indicate that this attenuation increase can be caused by:

a. Moisture penetration through the cable jacketing material,

b. Corrosion of the outer conductor shield, or

c. Contamination of the dielectric insulator due to jacket plasticizers (e.g., those used in PVC jackets).

These effects should not present a serious threat to system operation. According to manufacturers, the attenuation degradation caused by a small amount of moisture penetration is more pronounced at frequencies above 1 GHz; the system under consideration utilizes a frequency spectrum up to only 300 MHz (0.3 GHz). More important is the fact that the cable types under consideration, namely Times Wire's Dynafoam® and Alumifoam® , both utilize a seamless aluminum tubing for the outer conductor shield with an extruded black polyethylene jacket (not PVC). Cables constructed with the seamless aluminum tubing shield commonly are referred to as semiflexible. Moisture penetration and shield corrosion would present a problem for main trunks if the so-called flexible cable were used because this cable uses a braided (copper) outer shield. The braided structure of the shield, with small interstices between the braids, leaves open the possibility of moisture penetration, contamination impregnation, and corrosion. Subscriber drops, which normally utilize flexible cable, are usually of a short length and run

primarily within a sheltered environment, therefore contributing negligible impairment.

3.2.4 Shielding

Insufficient shielding of a coaxial cable leads to electromagnetic radiation leaking from the cable. This radiation can cause interference with noncable, over-the-air communications using the same frequencies allocated on the cable system.

Although the solid, outer conductor-type of cable has been shown to provide a good shielding, it should be mentioned that the total shielding efficiency may be limited by the shielding efficiency at the cable connectors and junction boxes. Another worst-case possibility for leakage could occur at a rupture just after an amplifier, where the signal levels in the cable are at their highest value. It is felt, however, that such an event would cause perceptible interference only to RF systems operating very near the cable, due to the fact that signal levels within the cable are not that large to begin with, and the resulting radiated field intensity drops off as the square of the distance from the leakage source. However, because of the seriousness of possible interference with, for example, air traffic control, this aspect needs further resolution if such a system will be located in the vicinity of airbase facilities.

Also related to electrical shielding of the cable system is the question of RF penetration into the distribution facility of signals from nearby high-power transmitters. Radio frequency interference from local amateur radio transmissions has been observed on the MITRE (MICOM) cable system. The output power of the MITRE amateur radio facility is approximately 0.5 kW. Of particular concern to MIDS operation are radio transmissions on the 20-meter (14 to 14.350 MHz) and 15-meter (21 to 21.450 MHz) bands. Both of these bands fall within the MIDS frequency allocation (12 to 24 MHz). For military base applications of MIDS such interference could result from on-base MARS transmitters, which typically operate at an output power of 1 kW.

The mechanism of this RF penetration is not clearly understood at present, but it is felt that seamless aluminum shielding of the coaxial cable is sufficient to rule out coupling through the cable itself. This leaves open the possibility of coupling through unshielded terminals, connectors and junction boxes, or possibly induction through ac power lines. Further investigation is needed to identify these entrance points so that methods may be devised to alleviate this type of interference.

3.2.5 Propagation Delay

The velocity at which electrical signals propagate along a coaxial cable is determined by the dielectric constant of the insulating material between the concentric conductors. This velocity usually is expressed as a percentage of the speed of light. The reciprocal of this velocity gives the propagation delay, which is usually expressed in nanoseconds per foot (ns/ft).

Because of the delicate timing requirements involved in high data rate TDMA transmissions from subscribers located at different positions along the cable, it is essential that the propagation velocity/delay be known accurately. The two cable types considered differ in their insulating dielectric material; one uses foam polyethylene and the other uses polystyrene. Their propagation characteristics are shown in Table 3-1 (Reference 7).

A potential problem could come about if the propagation delay changes as a result of a change in environmental conditions (e.g., ambient temperature variation). Such a change in the propagation characteristics could have a serious impact on system timing, resulting in intersymbol interference or interference between messages in adjacent time slots transmitted by different subscribers.

TABLE 3-1

CABLE PROPAGATION CHARACTERISTICS

Cable Dielectric	Time Delay (ns/ft)	Velocity (% of Speed of Light)
Foam Polyethylene	1.27	80.0
Foam Polystyrene	1.12	91.0

The operating temperature range for the foam insulators is given as -65° to +80°C (Reference 7). This temperature range would certainly seem to be sufficient for most applications; however, this range is based on acceptable attenuation properties (related to the "power factor" of the insulating material) and does not give consideration to changes in propagation velocity.

The possibility of propagation velocity variations presents a potential problem in a TDMA system, such as the MIDS data subsystem, because of the required timing that each subscriber must observe. These variations would not, however, present a problem in conventional CATV applications because in the broadcast mode operation employed in cable TV, precise timing synchronization is unnecessary. That is, in CATV operation all subscribers simply receive, and delay variations do not affect performance perceptibly.

The solution to the problem of velocity variations in a TDMA data system is to insert a guard interval between adjacent time slots. An analysis of the required guard interval resulted in a formula for the required guard interval T, which is

$$T = \frac{\delta}{1+\delta} \cdot \frac{2L}{v}$$

where v is the minimum propagation velocity on the cable, δ is the fractional variation in the velocity caused by temperature changes, and L is the longest length of cable that signals must traverse when the cable is in operation. The required guard interval is, therefore, directly proportional to the length of cable with a proportionality constant fixed by the velocity and its expected variation.

In the current design of MIDS, the guard interval T is 8.4 μs. Environmental chamber measurements of the propagation delay as a function of temperature over a range of -40° to +140°F have shown no significant change in the propagation velocity. The time reading accuracy of these measurements is estimated conservatively as ± 0.01 μs. Since the cable specimens examined were approximately 1,000 ft in length, the measured delays were on the order of 1 μs. This means that the fractional variation in velocity will be less than 0.02. Using this worst-case

variation, the nominal propagation velocities listed previously, and the 8.4- μs guard interval, the corresponding signal path lengths turn out to be:

L (polyethylene) = 32 miles

L (polystyrene) = 36 miles.

Under the worst-case configuration (NCC located at far end of trunk), a subscriber's signal would have to loop the cable length twice; therefore, the system length supported by the MIDS 8.4-μs guard interval will be half of the values listed above (16 and 18 miles respectively).

Summarizing, the results of environmental chamber testing of typical CATV-type coaxial cables indicate that under worst-case conditions the MIDS guard interval of 8.4 μs will accommodate operational system lengths of at least 16 miles using a cable with a foam polyethylene dielectric, and at least 18 miles with the polystyrene dielectric cable, over a temperature range of -40° to +140°F. These lengths are certainly sufficient for most C^3 or base applications.

3.2.6 Dispersion

The previous discussion of cable propagation velocity does not take into account the phenomenon of dispersion, which is a

dependence of propagation velocity on frequency. The degradation manifested by a dispersive medium is intersymbol interference as the individual pulses tend to spread out and overlap. Measurements on dispersion as a function of temperature also were performed by environmental chamber testing. The conclusions reached by these dispersion tests were:

a. The JT1412J (polyethylene dielectric) cable exhibits no measurable dispersion over the frequency range of 10 to 300 MHz and temperature range of -40° to +140°F; and

b. The JT2412J (polystyrene dielectric) cable exhibited a 0.02-μs delay difference between 10 and 150 MHz for all temperatures examined. This change amounts to the cable being electrically longer by 1.6% at 10 MHz than at 150 MHz.

Since relative frequency-dependent delays are important only over the bandwidth of a given channel, the widest of which are the 4-MHz high-speed MIDS data channels, the slight dispersion observed on the polystyrene cable (over a 140-MHz band) is not serious. We can therefore classify the tested coaxial cables as essentially nondispersive media.

3.3 AMPLIFIER CHARACTERISTICS

The major limiting factors in an amplifying device are the output power capacity, the internally generated noise power, and the linearity within the operating range. For broadband cable communications, the output power limitation generally does not arise because of the low signal levels required in providing various services.

The amplifier used in the MITRE cable system is the 300-series line extender manufactured by Jerrold Electronics and is representative of commercially available CATV equipment.

3.3.1 Internally Generated Noise

Internally generated noise levels of the line extender amplifier were measured, and details of the measurement procedure and equipment were documented. The results of these measurements are:

a. The amplifier internal noise level is -16 dBmV across a 4-MHz channel;

b. The operational amplifier output levels in the cable system are at 46 dBmV; and therefore,

c. A signal-to-noise ratio of 46 + 16 = 62 dB results from a clean signal passing through one amplifier.

Measurement was made of the noise accumulation through eight cascaded amplifiers. It was found that the average noise level, in a 4-MHz bandwidth, at the output of the last amplifier in cascade was approximately 8 dB higher than the noise level measured for the single amplifier. This result, within 1 dB, conforms to the general rule that doubling the number of amplifiers in cascade increases the noise level at the output of the last amplifier by 3 dB.

For C^3 or base applications it is felt that the noise accumulation from cascaded amplifiers will not cause serious degradation in received signal quality.

3.3.2 Nonlinear Distortion

Passing electrical signals through nonlinear components in a communication system can cause interference by the production of undesired frequencies in the passband of the system. The cable amplifiers are a source of such nonlinear distortion.

Because the input/output voltage characteristics of an amplifier are not perfectly linear, signals entering the amplifier are distorted at its output. If a pure sinusoidal signal is injected into an amplifier with nonlinear distortion, the output signal will not be a pure sine wave. Fourier analysis shows that

this distorted output signal is composed of a number of different frequency sinusoids of which only the fundamental frequency is desired. When many signals are passed through a cable amplifier, numerous undesired frequency components occur throughout the passband.

The input/output voltage characteristics of typical CATV amplifiers is approximated closely by the three-term series (Reference 6):

$$e_{out} = k_1 e_{in} + k_2 e^2_{in} + k_3 e^3_{in}$$

where e_{in} is the instantaneous input and e_{out} the instantaneous output voltage of the amplifier, and k_1, k_2, k_3 are real numbers. This representation essentially says that second-order (squared term) and third-order (cubed term) distortion is present, but it neglects higher-order distortion. Laboratory measurements of the distortion components indicate that this third-order approximation of cable amplifier characteristics is a valid assumption (Reference 8).

Based on this third-order approximation, an analysis was performed on distortion products generated by the interaction among carrier frequencies in the MIDS spectrum. The fundamental frequencies considered were the following MIDS carriers:

a. S&S poller output: 12.8 MHz,

b. S&S subscriber output: 13.6 MHz,

c. Data poller output: 16.875 MHz, and

d. Subscriber data output: 21.375 MHz.

The location of the amplifier distortion products is seen in Figure 3-2. Only third-order distortion is present in the MIDS band (12 to 24 MHz). This results from the MIDS band occupying precisely one octave of bandwidth (24 MHz = 2 X 12 MHz). In general it is true that an allocation falling within one octave or less will never generate in-band second-order distortion. Thus, only third-order triple beats, of the form $f_i \pm f_j \pm f_k$, and intermodulation products, of the form $2f_i \pm f_j$, where f_i, f_j and f_k represent carrier frequencies, occur within the band of interest. Note from Figure 3-2 that the narrowband S&S carrier channels are free from distortion products, but that both of the wide-band, high data rate channels contain four distortion products.

By rearrangment of the channel locations within the MIDS band and/or shifting the band elsewhere within the 5 to 300-MHz spectrum, it may be possible to obtain fewer distortion products falling in the MIDS channels. A total analysis should take into account all the carriers over the total spectrum (including possible video and audio channels in the system).

IA-49,243

C = TRIPLE BEAT
D = INTERMODULATION COMPONENT

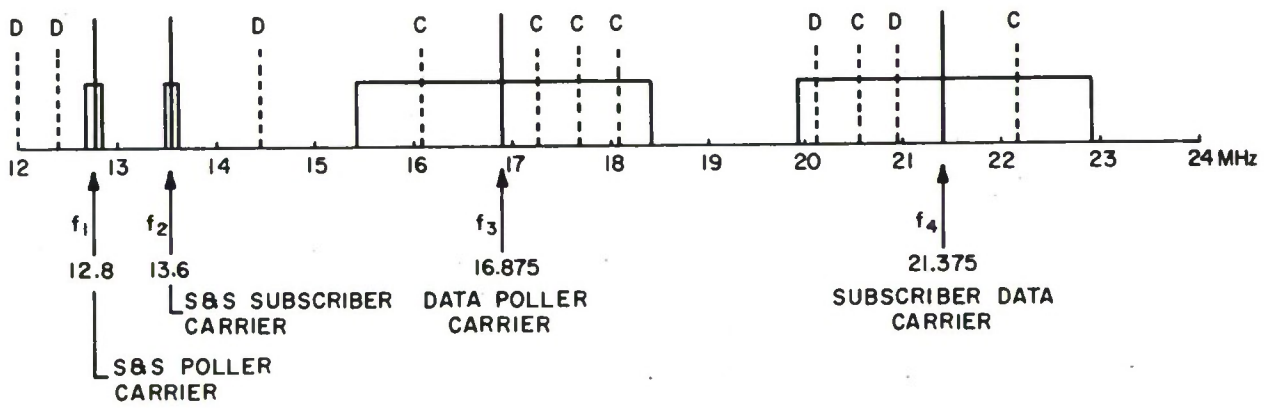
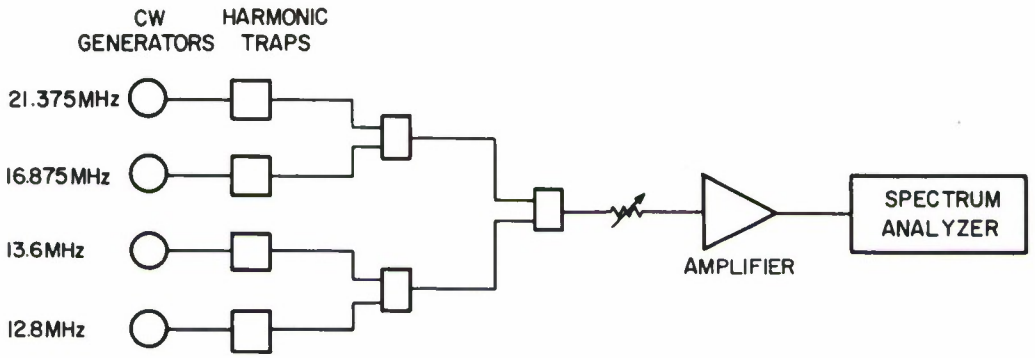


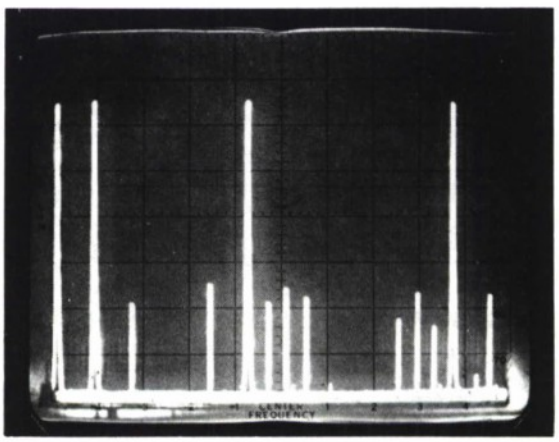
Figure 3-2. Predicted Distortion Components in MIDS Band

In an attempt to verify the amplifier modeling assumption of considering only second- and third-order distortion and neglecting higher-order terms, a Jerrold solid-state TV-FM amplifier (Model 3441) purposely was driven into overload. Four CW sinusoids at frequencies corresponding to MIDS carriers were injected into the amplifier. The levels of these four test tones were gradually increased until the major distortion components were observed clearly. The test setup is seen in Figure 3-3(a). Harmonic trap filters were placed at the output of each CW generator to assure that source harmonics would be suppressed. Figure 3-3(b) shows the spectrum of the overloaded amplifier as observed on a spectrum analyzer. The horizontal axis scans from 12.8 to 22.8 MHz with a scan width of 1 MHz/div. The scaling on the vertical axis is 10 dB/div. The four strong signals seen in Figure 3-3(b) are the MIDS carriers. The other components, greater than 40 dB below the output carrier levels, are the amplifier distortion products. Very good agreement is seen between the predicted (Figure 3-2) and measured (Figure 3-3) frequency location of the distortion components. The assumption of neglecting nonlinear terms higher than third order is, therefore, verified along with the distortion analysis (Reference 8).

The need for an accurate mathematical modeling of cable amplifiers is realized when one considers the problem of determining an optimum frequency allocation for the various channels in the



(a) DISTORTION COMPONENT MEASUREMENT CONFIGURATION



(b) ANALYZER DISPLAY OF OVERLOADED AMPLIFIER OUTPUT
(SCANNING FROM 12.8 TO 22.8 MHz AT 1 MHz/DIV)

IA-49,244

Figure 3-3. Measured Distortion Components in MIDS Band

system. If an accurate mathematical amplifier model is assumed, an iterative computer program may be employed to calculate optimum channel locations, based on a given number of channels and their respective bandwidths, to minimize interference from in-band nonlinear distortion products.

Measurements of the distortion component levels on the Jerrold SLE-300 line extender amplifier were made in MITRE laboratories. The main conclusion drawn from these measurements is that the manufacturer's distortion level specifications for the single amplifier, and also for eight amplifiers in cascade, were met only when the rules specified for cable operation were closely adhered to. In particular, the 3-dB block tilt (reduction in the low band levels by 3dB relative to the high band levels) must be observed, and all audio carriers, including frequencies in the FCC-allocated FM band (88 to 108 MHz), should be operated at least 15 dB below the design level of the video carriers.

This conclusion implies that the frequency range of 88 to 108 MHz cannot be used for video channels without exceeding the manfacturer's specifications on amplifier distortion product levels. This is, therefore, a constraint imposed on seeking a suitable frequency allocation for a fully operational MIDS carrying data, voice and video communications. On the present MICOM system, data

signals are operated at the same level as video carriers; however, it may be desirable to operate data signals at a level lower than the video carrier level. The lower data level would help to optimize amplifier operation by reducing statistical amplifier overload.

3.4 OTHER SPECTRUM-ALLOCATION-RELATED INTERFERENCES

Aside from the occurrence of amplifier nonlinear distortion products falling within allocated channels in a full spectrum utilization, there are other types of spectrum-allocation-related interferences that may arise (Reference 9). The majority of these problems stems from the heterodyne detection process used in subscriber TV receivers. Here a local oscillator signal is beat against the composite incoming RF signal to downshift the desired frequency level of interest to the IF range for further amplification and signal processing. These additional interferences -- local oscillator leakage, image interference, and IF beats -- are discussed briefly in the following paragraphs.

In general, the frequencies of the TV local oscillator may lie within the range of other communication channels. If the oscillator signal from a malfunctioning TV receiver is leaking back into the distribution cable, then interference in other channels may be observed. This interference, however, will affect only nearby

subscribers on the same feeder line, because the leaked signal will suffer a feeder line loss on its way back to the directional tap, and the directional tap will itself severly attenuate this leaked signal to keep it from entering the main cable.

Image interference arises when a second channel lies in the image band of a given channel. This "image band" is located symmetrically around the local oscillator frequency of the given channel. Interference can result from undesired mixing of the image band with the local oscillator of the given channel, and is observed in the IF range when the given channel is being received. Avoidance of image interference calls for good image frequency rejection (filtering) in the TV receiver before the mixing stage.

The IF beats arise when two channels are allocated in such a way that their carriers are separated by approximately the IF frequency. If these two signals should somehow interact in a nonlinear device to create difference beats at the input to an IF amplifier, then these beats will lie within the IF passband and will be amplified along with the desired signal.

Summarizing, nonlinear distortion is only one form of spectrum-allocation-related interference. In attempting to construct a total spectrum allocation for full service on MIDS

(data, video and voice), consideration must also be given to these other possible interference sources.

SECTION 4

CONCLUSIONS AND RECOMMENDATIONS

The impetus in the development of MIDS was the achievement of low-cost subscriber units to interface end terminals to the distribution system, proof-of-concept demonstrations of flag-for-service signaling and supervision, and an adaptive data rate scheme. The following subsections discuss the realization of the economic goal and the effectiveness of the technical concepts employed in MIDS.

4.1 LOW-COST SUBSCRIBER UNITS CAN BE IMPLEMENTED

To have accomplished, with conventional hardwired logic, the functional tasks of call connectivity, data buffering, variable rate control, and error correcting performed by the subscriber unit would have consumed several hundred integrated circuits, associated cards, chassis, and power supplies. The cost of such conventional hardware, even when acquired in volume, would have been well over one thousand dollars and would perhaps have exceeded the cost of the terminals themselves.

The evolution of large-scale integrated circuits into the microprocessor is the predominant factor which has opened the possibility of achieving low-cost subscriber units. In the MIDS

subscriber unit, two microprocessors were employed, one for the S&S keypad control unit and another for the data buffer unit.

As was shown in Table 2-2, a limited production version of the subscriber unit would cost $420. If the volume requirements for MIDS subscriber units were to run into the tens of thousands, and the remaining small-scale integrated circuits were collapsed into a few custom large-scale integrated circuits used in conjunction with the microprocessor, the projected costs for each unit would be in the range of two to three hundred dollars. The most expensive remaining items (included in the projected cost) are the data modem (the fixed delay line in particular) and the power supply. Advances in modem technology and the use of CMOS circuits would ease these remaining costs factors considerably.

With the subscriber units costing a few hundred dollars, the MIDS concept is economically viable and competitive with conventional telephone alternatives (Reference 10). In addition to the economic benefits, the MIDS provides all the advantages of modern communication concepts discussed in this report.

4.2 EFFICIENCY OF S&S SUBSYSTEM

Conceptually, the MIDS S&S subsystem may be used to provide user access to any of the service varieties (data, video and telephone) found on the multimode distribution facility. This common channel signaling consumes a rather minute portion (100 kHz) of the total available cable system bandwidth (295 MHz).

The flag-for-service scheme incorporated in the MIDS S&S subsystem allows subscriber service requests to be recognized and identified by the S&S poller in an efficient manner. Only one bit per subscriber is necessary for such identification. Other techniques for accomplishing this identification, such as roll-call polling, require excess overhead information leading to considerable S&S channel inefficiency when the subscriber population is large. The flag-for-service scheme therefore reduces the necessary overhead for accomplishing the poller's function of identifying service requestors, and still maintains simplicity in its implementation. Future growth in the subscriber population can be accommodated by allocating extra flag bits, initially unused, in the S&S channel format.

4.3 EFFECTIVENESS OF ADAPTIVE DATA RATE SCHEME

The adaptive data rate concept implemented in MIDS provides an efficient mechanism, in the use of both low-speed and high-speed data polling queues, for subscribers to access high data rate transfer capabilities. The efficiency is realized by the fact that the high-speed capacity is shared among all subscribers and used only when necessary rather than by dedicating separate high-speed channels to each subscriber. Those data transactions that do involve the use of the high-speed capability (for terminal rates between 600 b/s and 19.2 kb/s) result in an effective transmission rate of precisely the data rate of the terminal device, and the time-shared low-speed/high-speed polling is transparent to the peripherals.

Under heavy traffic loading, when the number of high-speed service requests exceed the maximum capacity of the high-speed queues (16 pairs of subscribers), a graceful degradation of transmission speed occurs. This means that even under heavy demand periods no subscriber will be barred from high-speed polling; instead, all the requesting subscribers will be passed cyclically in and out of the high-speed poller with an attendant drop in the high-speed rate from 19.2 kb/s down to some lower value (say, 9.6 kb/s). As traffic conditions reduce from the peak load, normal operation

resumes and the maximum transfer rate, available to subscribers in the high-speed queue, returns to 19.2 kb/s.

4.4 TECHNICAL LIMITATIONS ASSESSMENT

Consideration has been given to a number of potential technical limitations resulting from signal degradation and interferences on a CATV-like cable distribution facility supporting multimode communications. These considerations led to a series of test measurements on typical CATV system components such as the coaxial cable medium and line amplifiers.

The main conclusion reached from the amplifier testing was that distortion level specifications on the amplifier were met only when all audio carriers, including any carrier frequency in the FCC-allocated FM band (88 to 108 MHz), were operated at least 15 dB below the design level of the video carriers. This conclusion implies that the frequency range of 88 to 108 MHz cannot be used for video channels without exceeding the manufacturer's specification on amplifier distortion product levels.

The main conclusion drawn from environmental chamber testing of the coaxial cable was that, over a temperature range of -40° to +140°F, no measureable variation occurred in propagation velocity, a potential problem for a TDMA system identified and analyzed under

the MIDS effort. Also, the dispersion effects were very small. Unresolved problems, still in need of further analysis, include: 1) RF penetration onto the cable distribution system from high-power transmitters in close proximity, and 2) an optimum frequency spectrum allocation for FDM multimode communications in order to avoid, as much as possible, amplifier nonlinear distortion and TV-related interferences such as local oscillator leakage, IF beats, and image interference.

4.5 RECOMMENDED CONTINUATION OF MIDS EFFORT

There are four areas where further technical effort is needed. These are:

a. Objective measurement of system operational performance under simulated traffic loading,

b. Verification of multimode operation on the MICOM system,

c. Design considerations for the utilization of a fiber optics medium as a replacement for coaxial cable, and

d. Considerations of the interface between MIDS and the outside world.

Any continuation of the MIDS program should examine these areas as detailed in the following subsections.

4.5.1 Performance Measurements Under Simulated Traffic Loading

There is a need to test the MIDS S&S and data subsystem operation under conditions which simulate peak-load traffic demand in an actual application. The maximum traffic that can be offered by the small number of subscriber units developed for the prototype MIDS demonstration cannot represent the case of a fully loaded system. What is needed are artificial traffic simulators that can transmit service request flags to the S&S poller and high-speed request indications to the data poller. The traffic simulators should possess a selectable request rate (measured by the total number of requests per unit time) so that the measurements may be parametrized according to different demand levels. Under this influx of artificial traffic, the following variables may be measured:

a. S&S response time - measured as the time elapsed from the calling subscriber's last S&S keystroke entry until illumination of his call active lamp, and

b. Rates of high-speed degradation - measured as the subscriber's effective data transmission rate while in the high-speed queue when more than 16 (simulated) pairs of subscribers simultaneously demand high-speed service.

In addition to acquiring parametric curves giving response time and transmission rate degradation as a function of traffic load, these test procedures can serve to define ultimate traffic limits above which the system would operate inefficiently.

Measurements should also be made of the S&S and data modem bit error rates as a function of (simulated) noise levels, along with tests on data pattern sensitivity. These measurements can be used to substantiate the single-bit parity error detection utilized in MIDS, or to indicate the need for more sophisticated error detection schemes.

The ability of end terminals of different data rates to communicate with each other has been designed into the MIDS subscriber interface unit by a process of retransmissions. Tests on the valid operation and efficiency of this scheme should be performed with a two-terminal connection by increasing the rate of one transmitting terminal while holding the rate of the other receiving terminal constant.

4.5.2 Verification of Multimode Operation

The assessment of technical limitations, reported in Section 3, identifies a number of potential problems related to the spectrum allocation of FDM channels on a wideband communication system.

Since a number of different services (data, video and telephony) are carried on the MICOM system, the inclusion of MIDS signals on MICOM will further serve to verify multimode operation. The evaluation of such operation will serve to separate real problems from potential problems, and will also serve as a testbed for identifying unforeseen limitations if any exist.

4.5.3 Utilization of Fiber Optics

Recent advances in the technology of fiber optics are showing the feasibility of this new communication medium for near-term applications (References 11, 12, 13 and 14). As the MIDS system utilizes a CATV-type distribution, it is interesting to note that Teleprompter Manhattan Cable Television recently (July 1976) put into daily use a fiber optic cable system designed as a substitute for 3/4-in. coaxial cable (Reference 15). The reason for Teleprompter's choice of the fiber optic medium is the relative loss advantage (16 dB/mile compared to the coax loss of 62 dB/mile) leading to wider repeater spacing, and the fact that the optical fiber cable allows TV operators to increase channel capacity while decreasing costs of new construction.

Of particular interest for the application of MIDS are the optical fiber transmission advantages of electromagnetic pulse (EMP) and electromagnetic interference (EMI) immunity which result from

the dielectric nature of the fiber. The fibers exhibit low crosstalk and therefore enhance the privacy of the system. Optical fiber cables are presently being developed so that intruders may be detected when attempting to tap information from the cable. A continuation of the MIDS effort should certainly attempt to exploit the potential advantages of the fiber optic medium.

In developing a fiber optic distribution for MIDS, consideration must be given to the appropriate choice of light sources (light emitting diodes, semiconduction injection lasers, Nd: YAG lasers), fiber cables (low-, medium- or high-loss, step or graded index, single strand or bundle), and receivers (PIN or avalance photodiode). There are also design decisions to be made on the type of modulation and multiplexing techniques to be used in optical transmission.

4.5.4 Interface With External World

MIDS is a local distribution facility. Any such facility must provide user access to communication links external to the local area; thus, effort is needed on the interface between MIDS and the external world. Depending on the specific application, considerations on the MIDS interface to the public telephone network, AUTOVON, AUTODIN, radio links, and tactical data links are in order. The technical work involved in this endeavor should be

aimed at the design and specification of hardware interface modules to ensure compatibility of electrical characateristics, message formats, and protocols, and MIDS control software modifications to accommodate these interfaces.

APPENDIX A

SIGNALING AND SUPERVISION SUBSYSTEM

A.1 GENERAL

The signaling and supervision subsystem provides the control for the MIDS network. The subsystem's basic control functions are to:

a. Routinely monitor the status of all subscribers,

b. Handle subscriber request for connectivity,

c. Authenticate request and requestor,

d. Ascertain availability of equipment, and

e. Establish and disconnect connectivities.

As was shown in Figure 2.3, the S&S subsystem operates over a separate channel pair at frequencies f1 and f2. This feature is equivalent to out-of-band, common-channel signaling in the commercial telephone network. The S&S channel permits the MIDS subscriber to modify connections without disturbing any transaction already in progress. Similarly, changes in equipment status are monitored and reported automatically over the S&S channel, regardless of the state of the subscriber's connections.

The S&S subsystem is comprised of two major functional elements. One element is the network control computer and its associated S&S poller unit; the other is the keypad control unit, which is a part of each subscriber unit. The S&S subsystem is shown in Figure A-1.

This appendix describes the following aspects of the MIDS signaling and supervision subsystem:

a. User system control and information flow,

b. Network control computer and S&S poller unit, and

c. S&S keypad control unit.

A.2 USER SYSTEM CONTROL AND INFORMATION FLOW

The keypad, with its associated status lamps, is the primary interface between the user and the signaling and supervision subsystem. The layout and markings of the keypad are illustrated in Figure A-2. A conventional 10-button keypad with six additional function keys is utilized. The six status lamps indicate the progress of the dialing sequence. In addition to the ten numeric keys the following function keys are provided:

S: Service Code,

C: Clear Keystrokes,

D: Disconnect,

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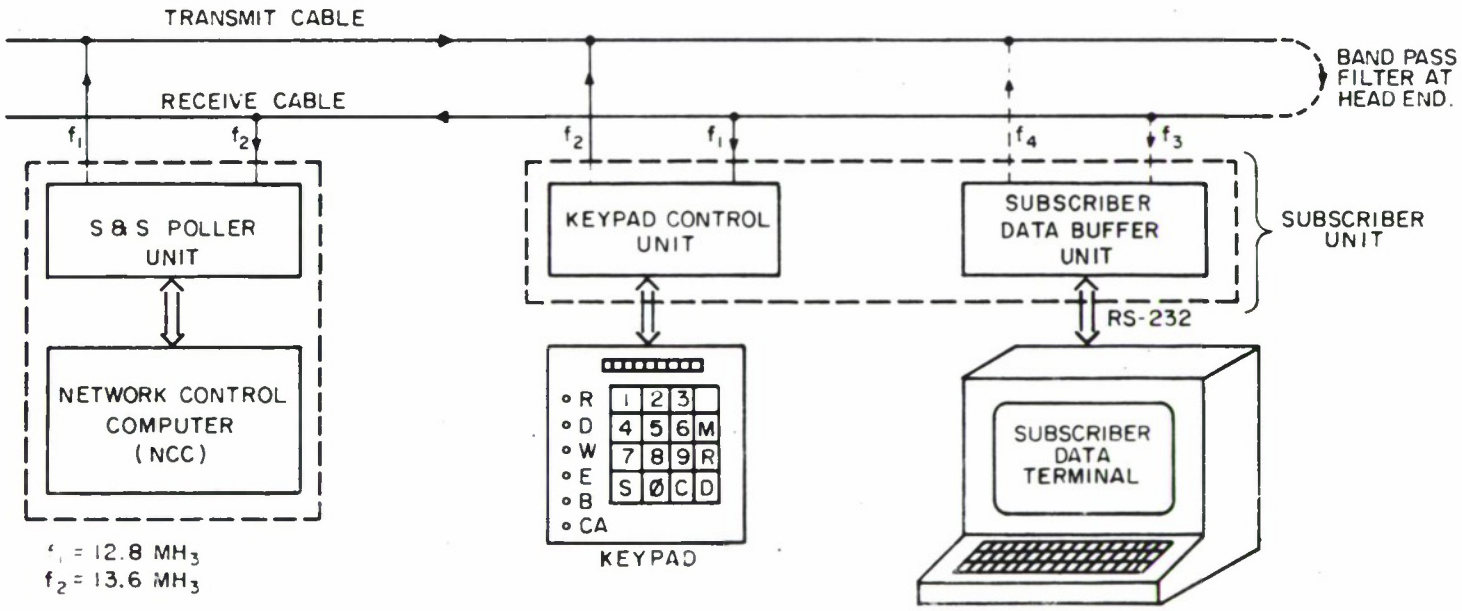

Figure A-1. S&S Subsystem

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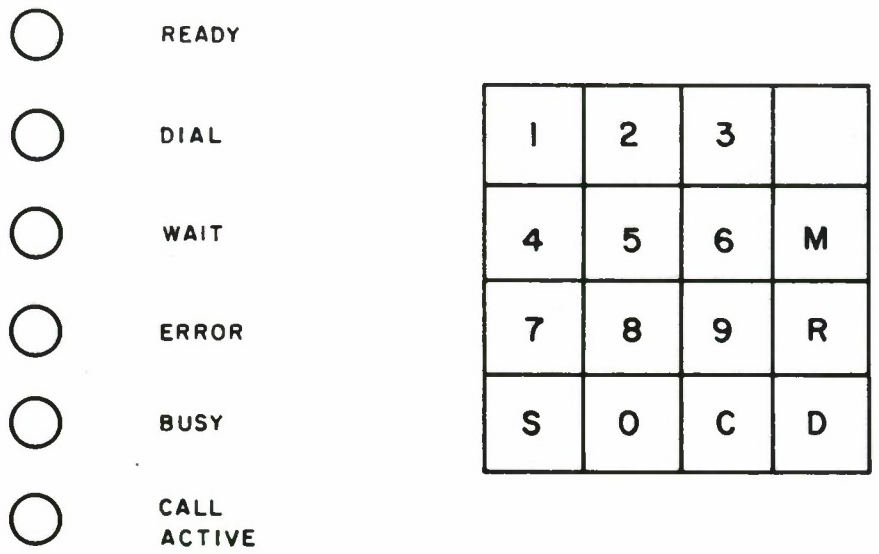

LEGEND

S: SERVICE CODE
C: CLEAR KEYSTROKES
M: MODIFY CALL
R: REDIAL CALL
D: DISCONNECT

Figure A-2. Keypad and Indicator Layout

R: Redial Call, and

M: Modify Call.

The sixth function key is unassigned and is available for future use.

The six indicators used to present status and guide user response are:

READY: S&S system ready for user input,

DIAL: User to continue to dial,

WAIT: Call being processed,

ERROR: Dialing error,

BUSY: Called party busy, and

CALL ACTIVE: Data connection complete and acknowledged.

The dialing sequence for the user at the keypad is illustrated in Figure A-3. When the S&S subsystem is initialized by the network control computer, the READY lamps at all of the keypads are turned on. When a user depresses a key, the resulting keystroke is collected by the S&S subsystem poll. The keypad control unit may store several keystrokes in its own buffer before transmitting to the S&S poller. The S&S subsystem checks first to see if the user has dialed either a CLEAR, a DISCONNECT, or a REDIAL. If a user has dialed a CLEAR, the S&S subsystem clears all prior keystrokes from memory and turns the READY lamp on. If a subscriber presses

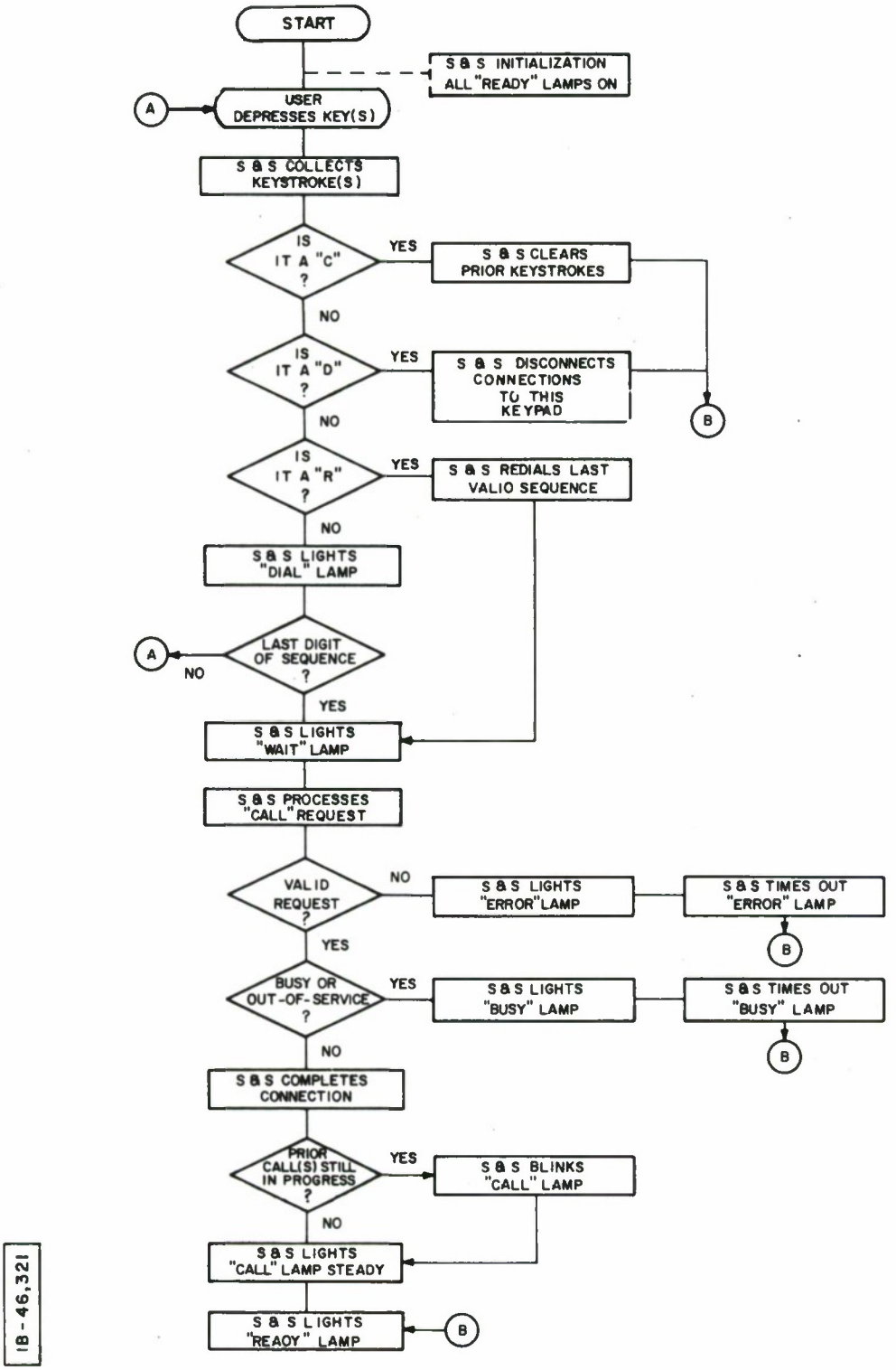

Figure A-3. Dialing Sequence

DISCONNECT, the S&S subsystem disconnects all prior connections and lights the READY Lamp. When a subscriber presses REDIAL, the S&S subsystem will attempt to make the connection previously requested by the user.

As each keystroke is received, the S&S subsystem checks to see if it is the last keystroke of a legitimate dialing sequence. When the last keystroke is so received, the S&S subsystem lights the WAIT lamp, which is an indication to the user that he is working into an active system. (It does not mean that the subscriber has to wait to do anything else.) The NCC then processes the call request. If a user has made an invalid request or a detectable error in dialing, the ERROR lamp is lit; however, the ERROR lamp is timed out by the system, so the READY lamp will illuminate after a predetermined time. If the called party is busy or out of service, the S&S subsystem will light the BUSY lamp on the calling party's keypad. It will then proceed to time out this busy lamp, and after a predetermined time, it will again light the READY lamp.

If, however, the necessary equipments are available, the S&S subsystem will complete the connection at both the calling and called party's keypads. If this connection is the initial call from the calling party's keypad, the CALL ACTIVE lamp is lit by the S&S subsystem. Before lighting the CALL ACTIVE lamp, however, the S&S subsystem checks to see whether a previous call from this keypad is

still in progress. If a previous connection has already been established for a different service package, then the CALL lamp would already be lit. If so, the S&S subsystem will cause the CALL lamp to blink before returning it to a steady state. The S&S subsystem also lights the READY lamp to indicate to the user that it is ready for another dialing sequence.

A.3 FUNCTIONAL DESCRIPTION OF NCC AND S&S POLLER UNIT

Communication between the keypad control unit (referred to in the remainder of this section as the keypad) and the NCC takes place on two channels dedicated to signaling and supervision. A transmit channel at frequency f1 is reserved for flag-for-service timing fields and messages from the NCC to the keypads. A receive channel at frequency f2 is reserved for flags-for-service and message responses from the keypads to the NCC. A time domain pictorial in Figure A-4 shows the relationships of these channels. Management of these channels is the function of the S&S poller unit (referred to in the remainder of this section as the S&S poller, or more simply, the poller), which is implemented with National Semiconductor's 16-bit PACE microprocessor and appropriate peripheral circuits.

The S&S poller is collocated with the NCC, as shown in Figure A-5, and provides the following functions:

a. Transmits the flag-for-service sequence,

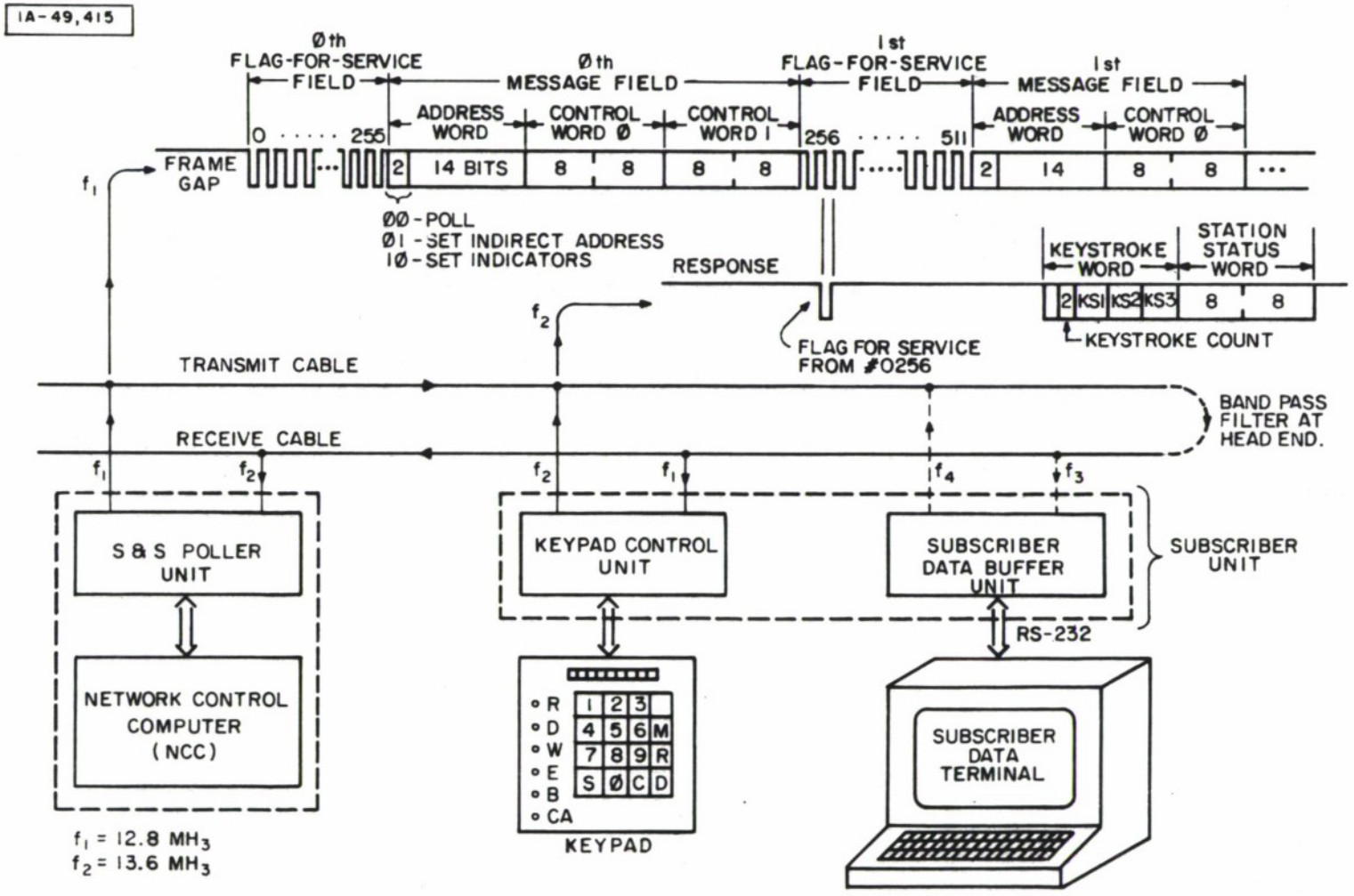

Figure A-4. S&S Communication

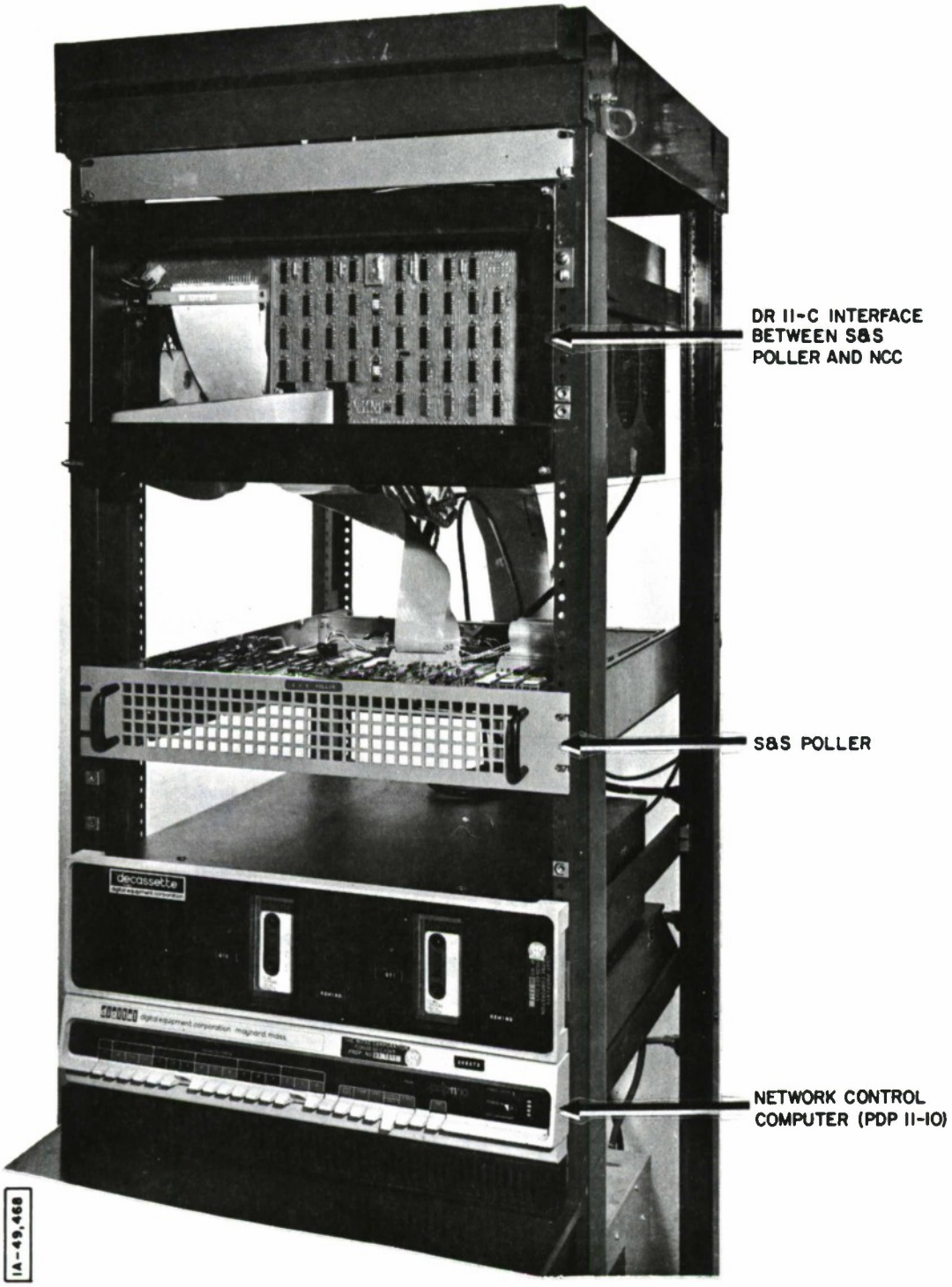

Figure A-5. Installation of S&S Poller and Network Control Computer

b. Establishes and updates a record of subscriber equipment status, and

c. Manages information transfer between the NCC and subscriber keypad control units.

Messages directed to the subscriber stations from the NCC go through the poller, as do messages sent from the subscriber to the NCC. The poller generates the flag-for-service pulse stream, which the keypad control units count to determine their unique time to flag for service. The poller also translates the incoming flags-for-service into user addresses, which the poller microprocessor uses to generate polling messages, which are transmitted in the message field.

The poller queues these polling messages and sends them out in order of priority. It receives responses from the keypad control units on the receive channel (at f2), matches each response (responses do not contain the keypad directory address) with the poll that generated it, and sends to the NCC only the messages containing new information. The poller also keeps a record of the status of all user equipment and polls the keypad control units for status regularly to insure that its records are up to date. All status changes are reported to the NCC.

A.3.1 Channel Organization

Each frame of the poller transmit channel (at carrier f1) begins with a frame gap followed by 64 S&S message blocks. Each of these message blocks consists of a flag-for-service field and an S&S message field. The message field contains a 6-byte message. Each byte consists of eight information bits, which will be detailed in the following subsections, along with overhead bits (start, parity, and two stop bits). The first two bytes contain a 14-bit address and two control bits that define the type of message (status poll, command to set indirect addresses, or command to set indicator lights). The remaining four bytes further define the command or indirect addresses and also provide a time slot in which the keypad control unit can send a response on the upstream channel, which is synchronized with the receive channel. This organization is shown in Figure A-4.

The poller receive channel (at carrier f2) contains flags-for-service from those subscribers requiring service and responses to polls. Responses consist of 4 bytes of information with no address. The origin of the response (the keypad directory address) is known to the poller by the timing of the response in relation to the poll that prompted it. The response to a poll message is delayed by one message block. The only type of response that is presently defined is the keystroke/status message. The first two

bytes contain keystroke data and the second two bytes contain station status. Figure A-6 is a functional diagram of the transmit and receive channel organization. For clarity, the start, parity, and stop bits are omitted from the diagram.

A.3.2 Types of Messages

Messages that are transmitted from the poller to the keypads can be categorized as 1) responses to flags for service, 2) messages relayed directly from the NCC, or 3) messages originated at the poller. A message is transmitted in each message field. Messages are directed to assigned user directory addresses, which are determined by the contents of the user data table in the NCC. The priority of messages is 1) responses to flags for service, 2) messages from the NCC, and 3) routine status polls.

A.3.2.1 Responses to Flags-for-Service

A keypad control unit generates a flag-for-service when it has keystroke data or a status change to report to the NCC. The poller responds to a flag-for-service with a status poll. The status poll sends no meaningful information to the keypad, but it addresses the subscriber and provides a time slot for the keypad to send the keystroke and status data to the poller. When the response message is received at the poller, the poller appends the user

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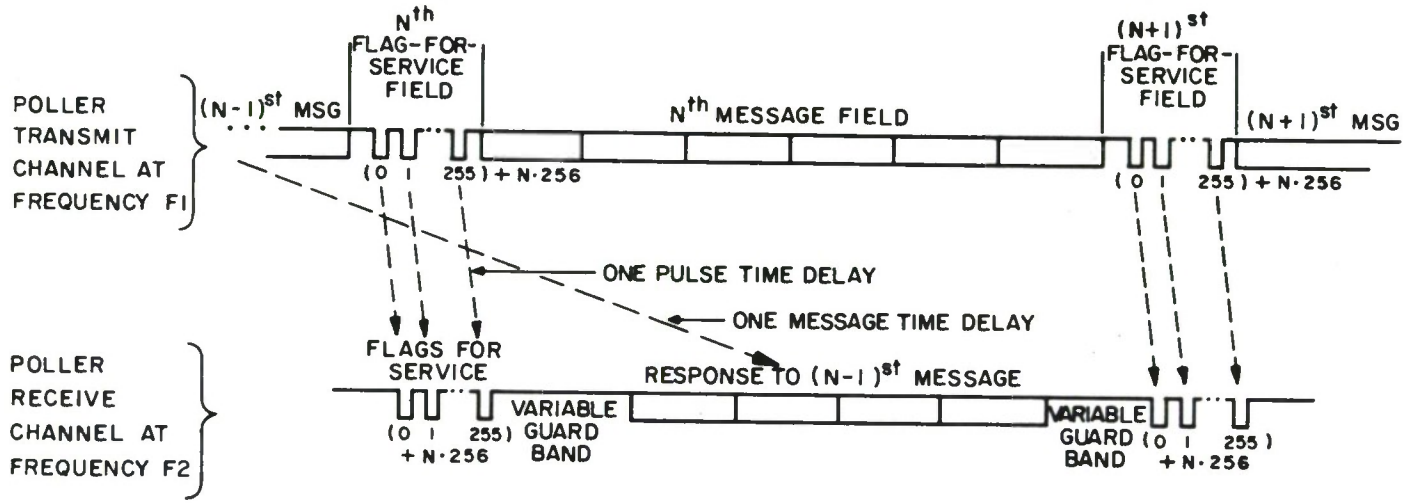


Figure A-6. S&S Channel Organization

directory address and sends it to the NCC. If there is a status change, the poller also updates its status table.

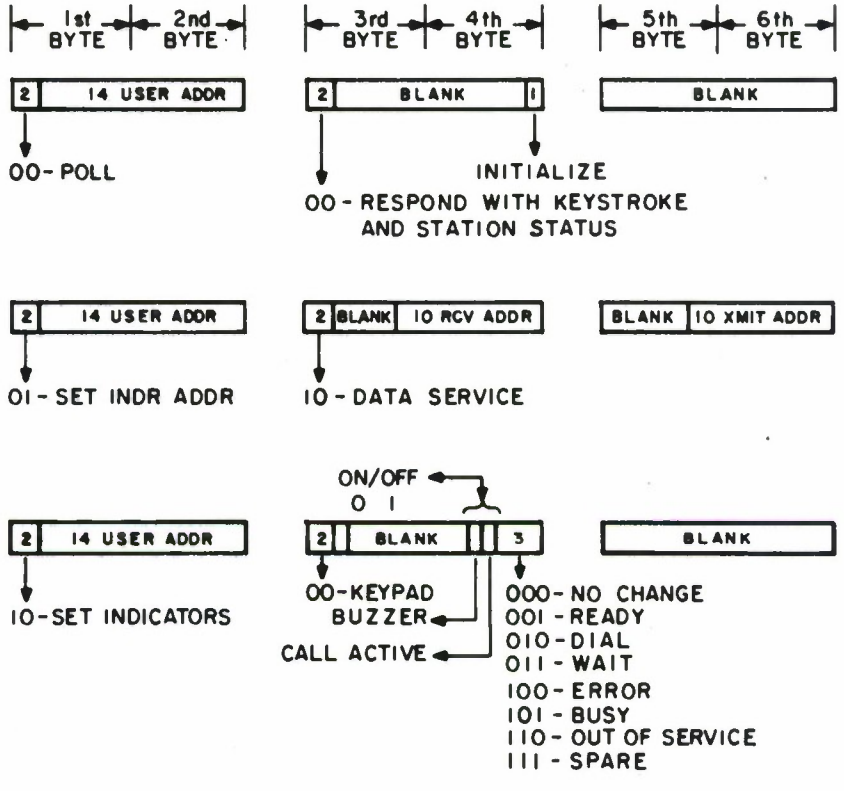
A.3.2.2 Messages from the Network Control Computer

Messages from the NCC to the keypad control units are sent to the poller, where they are queued up until they can be assigned to message blocks. These messages may or may not require a response from the keypad control unit. If the keypad control unit does respond, the response is sent, unaltered, to the NCC with the keypad directory address appended. In the present implementation, messages from the NCC to the subscriber keypad control unit are used to assign indirect addresses, to be used in the data buffer for data service, and to control indicator lights at the keypad. These messages from the NCC might be used to poll the keypad control unit for detailed status information, i.e., was the printer marked out of service because it was out of paper, off line, or powered down.

A.3.2.3 Poller-Generated Messages

There are two types of messages that originate at the poller itself: the initialization poll and the routine status poll. (Refer to Figure A-7 for the following discussion.) An initialization poll is addressed to each user during the period of initialization of the NCC and the poller. The initialization poll is the same as a status

TRANSMITTED S&S MESSAGE FORMATS



RECEIVED RESPONSE FORMAT

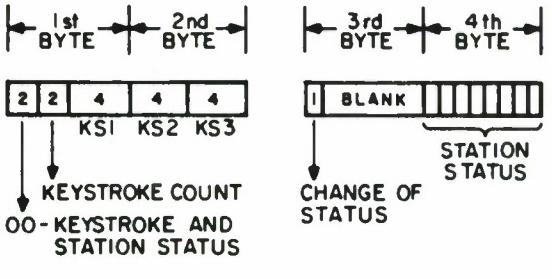


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Figure A-7. Message Formats

poll with the initialize bit set. On receipt of the initilization poll, the keypad control unit initializes itself and sets the indirect addresses of its data buffer to zero. It also responds to the poll with station status, which the poller uses to initialize its status table.

A routine status poll is generated whenever there are no other messages to be sent. This routine status poll is sent to keypad control units in order of their directory address numbers. The purpose of the routine status poll is to detect out-of-service keypad control units that are not able to flag for service to report their status. The format of a routine status poll is identical to that of the status poll which is sent in response to a flag for service. If a status change or keystroke is reported in response to a routine status poll, it will be processed as if the keypad control unit had flagged for service.

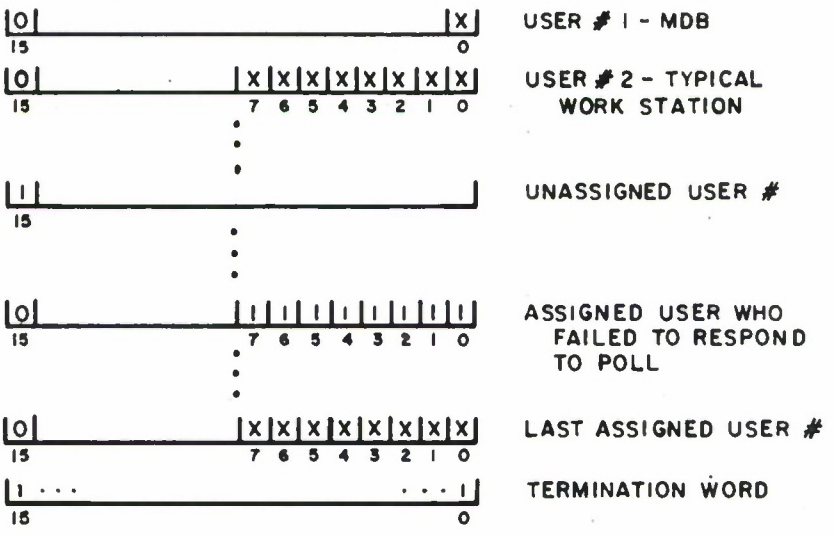
Figure A-7 is a diagram of the message formats. A "00" poll, a message containing zeros in the high-order two bits of the first address byte, is used for responses to flags for service, initialization polls, and routine status polls. Any of the three message types, 00, 01, or 10, may be used in a message sent by the NCC to a keypad control unit.

A.3.3 Status Polling

The poller keeps a record of the in-service or out-of-service status of the equipment at each subscriber station. Whenever the poller detects a change of status it notifies the network control computer, where status is also recorded. The duplication of the status table allows the NCC to have up-to-date status information for use in call setup and lets the poller assume the burden of routine status polling to detect out-of-service keypads.

The poller status table, shown in Figure A-8, is created during initialization. The size of the table is a function of the highest assigned user number (directory address). One word is allocated to each user number. Bits 0 through 7 indicate the status of equipment at the work station; bits 8 through 14 are unused; and bit 15 is set to 1 for unassigned user numbers.

The table is created from a series of one-word messages sent from the NCC to the poller based on the NCC's user data table. Each message contains the assumed status of a user's equipment. All equipment present at the subscriber station is assumed to be in service (power on, ready to be connected). This assumed status is also stored as the current status in the NCC. The NCC sends a word of 1's to signal the end of the table. The messages, as they are received, plus the word of 1's, form the original status table.



X = 0 - EQUIPMENT IN SERVICE
X = 1 - EQUIPMENT OUT OF SERVICE

BIT 0 OF USER #1 IS STATUS OF MULTIPORT DATA BUFFER

BITS 0-7 OF USER #S GREATER THAN 1 ARE THE STATUS OF EQUIPMENTS AT THE USER WORK STATION

BIT 15 IS SET TO 1 FOR UNASSIGNED USER NUMBERS.

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Figure A-8. Poller Status Table

After the entire table is created, the poller sends an initialization poll to each assigned user, who responds with his actual status. The actual status is compared with the assumed status, and where there is a discrepancy the NCC is notified. If a user fails to respond, all his equipment is marked "out of service". Flags-for-service are honored only after all keypads have been initialized and all responses processed.

Status changes at subscriber stations are normally reported automatically by the keypad control unit. A change of status of equipment at the station is detected by the keypad control unit, which flags for service. The poller sends the new status to the NCC, where it is transferred to the user data table. If equipment involved in a call goes out of service, the call will be disconnected by the NCC.

If the keypad control unit itself is out of service, it cannot flag for service and, therefore, cannot notify the poller of status changes; for this reason, the poller is designed to make a routine status poll of all keypad control units. The absence of a response causes the poller to mark all equipment at the subscriber station "out of service". The frequency of these polls depends on the number of assigned users. The poller cycles through the status table, sending out a routine status poll whenever there are no other messages to be sent.

A.3.4 Multiport Data Buffer Status

If common user equipment, such as a data processing computer, is included in a MIDS, it is accessed like any other subscriber in the system; however, instead of having just one data buffer, it has several in order to service several subscribers simultaneously. This interface device is referred to as a multiport data buffer (MDB). The basic architecture of the MID's network control software includes provisions for an MDB that has a capacity of 64 ports.

The first word of the status table contains the status of user #1, which is the directory address number assigned to the MDB. Only bit 0 is significant, representing the in- or out-of-service status of the entire MDB. Each of the 64 ports of the MDB has an individual on-hook/off-hook status that is recorded in the NCC. A status change of a single port in the MDB causes the MDB (user #1) to flag for service. The poller polls for status, and the MDB responds with a message containing the address of the port and its new status. The poller relays this message to the NCC.

The MDB is sent routine polls for status like any keypad control unit and it responds with the status of the MDB as a whole, including the front-end processor to the data processing computer. The absence of a response causes the MDB to be marked "out of

service" at the poller and at the NCC, which in turn causes calls involving the MDB to be disconnected.

A.4 SOFTWARE AND HARDWARE IMPLEMENTATION OF S&S POLLER

In normal operation (after the poller has begun transmitting to the cable), the poller software is synchronized with the poller/cable interface hardware. Most of the processing in the poller microprocessor is done while the hardware is outputting the 256 flag pulses. The 6-byte message, which is sandwiched between groups of flag pulses, is written as a combined effort of hardware and software. While this message is being written, the software task of first priority is to service the hardware. The microprocessor can be thought of as having a processing phase, when its operation is relatively independent of the hardware, and a message transmission phase, when it works closely with the hardware. Reference to the hardware functional diagram shown in Figure A-9 will be helpful to the reader in the following discussion. In addition, a photograph of the S&S poller hardware is shown in Figure A-10.

A.4.1 Message Transmission

A single 8-bit poller-to-cable (PC) hardware register used to store data to be written onto the cable is loaded by the software

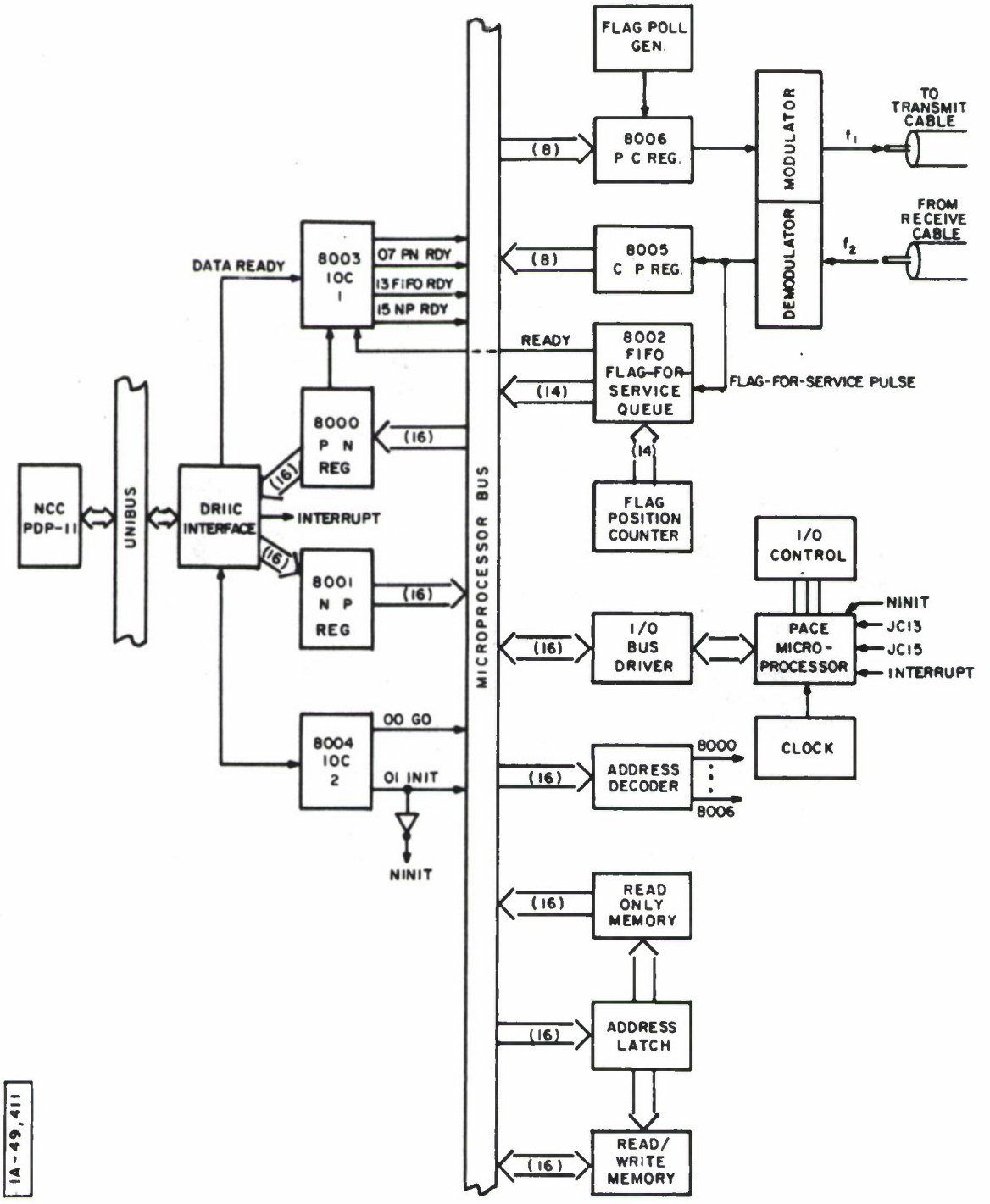

Figure A-9. Functional Block Diagram of NCC and S&S Poller

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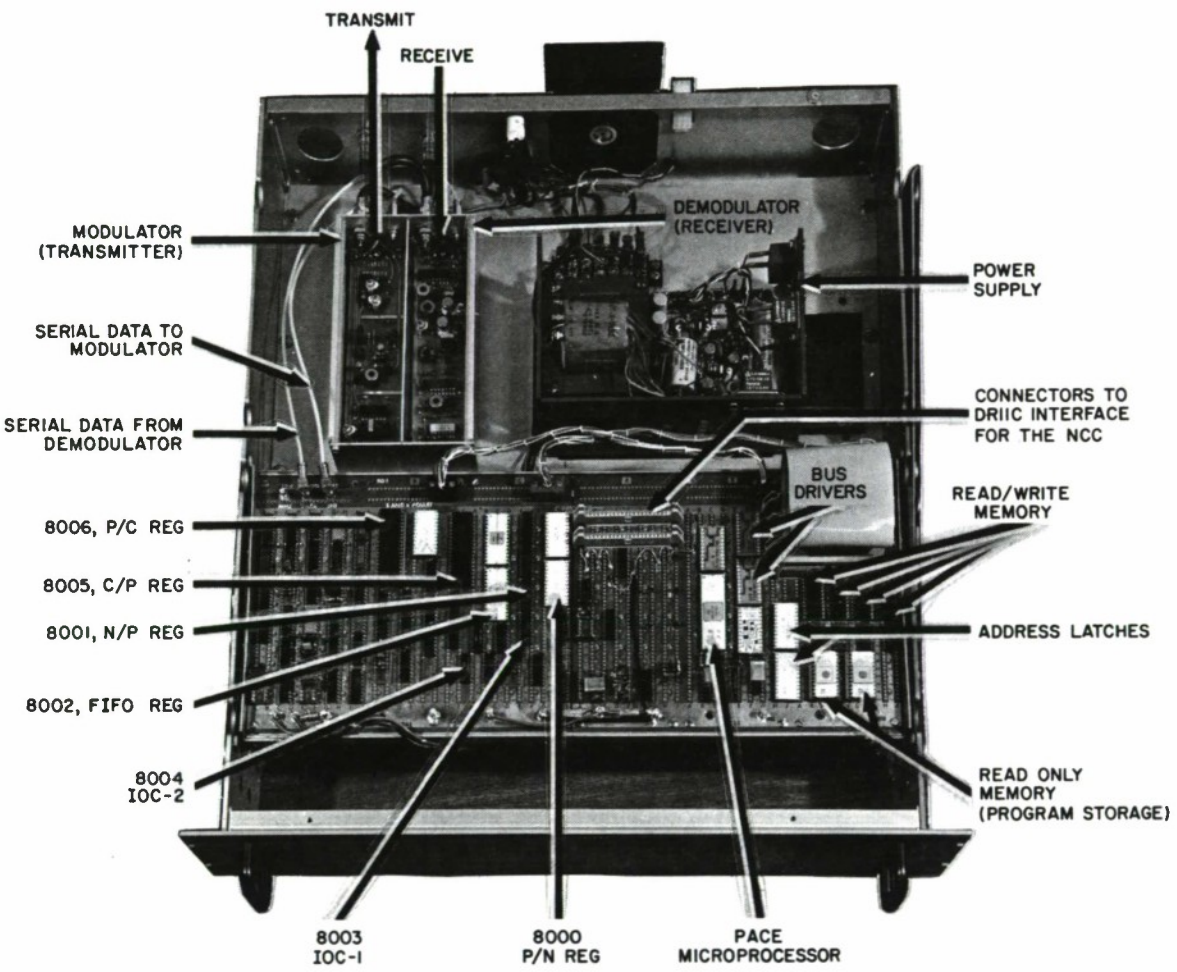

Figure A-10. S&S Poller

six times for each message written. Approximately 480 microseconds (μs) before a byte of data must be transferred to the cable, the hardware sets a flag (JC13) for the software. (See Reference 16 for a general description of all jump conditions, JC13, etc.) Within the 480 μs, the software fills the 8-bit register with one byte of the output message, causing the flag to be reset. The hardware empties the register onto the cable at the proper time and then sets the flag for the next byte. This sequence continues until all six bytes have been written. A message is sent downstream during each message time regardless of whether or not it contains meaningful information. Null messages are addressed to user #0, which is unassigned.

During the same period of time that the message is being written onto the transmit channel, the response to the preceding poll is read from the receive channel in a manner similar to the writing. Responses consist of four bytes spaced approximately 480 μs apart. An 8-bit input register (CP) is used to collect the data from the cable one byte at a time, and the hardware sets a flag JC15 when the register is full. The software has about 480 μs in which to read the data from the register, which causes the flag to be reset. The hardware sets it again when the next byte is ready.

The message transmission phase starts when the flag (JC13) is raised for the first byte of the output message. It ends when the

output message has been written and all four bytes of the response, if there is a response, have been read. The only additional processing done by the software during this phase is to allow an occasional interrupt by the network control computer. Only one interrupt is allowed between consecutive reads or writes, and the interrupt has been timed to insure proper servicing of the poller/cable interface hardware.

A.4.2 Message Processing

Message processing begins with evaluation of the incoming response. The response is first matched with the poll that prompted it (the poll that preceded the poll just sent). This poll contains the directory address of the keypad control unit and the type of information expected from the keypad. In the present implementation, the only polls that elicit responses are keystroke/status polls. The new status is compared with the status recorded at the poller; if there is a change of status or if the response contains keystroke data, the message is relayed to the network control computer. The failure of a keypad control unit to respond to a status poll causes all equipment at the subscriber station to be marked "out of service".

After the response is processed, a poll is prepared for the next cycle. The poll may be a status poll in answer to a flag-for-

service, a message from the NCC, or a routine status poll. The poll is first stored as three 16-bit words in the transmit message save area, where it will remain until the response is processed. It is also divided into six bytes and stored in the low-order eight bits of six consecutive words of memory, from which it will be fed to the hardware, one word at a time, during the message transmission phase. The routine software processing is finished when the message is ready for output.

The flag-for-service detection is a hardware function. The hardware translates the flags-for-service into keypad directory addresses and stores them in a hardware queue. The software accesses this queue through a single 14-bit, first-in/first-out (FIFO) register. The hardware indicates the presence of one or more directory addresses in the queue by setting the FIFO ready bit (bit 13 of IOC1). The bit is tested by the software when it is time to prepare an output message. If the bit is set, a directory address is read from FIFO and used to create a keystroke/status poll. The reading of the address causes another directory address to automatically enter the FIFO output register, and when the last directory address is read from the queue, the FIFO ready bit is reset by the hardware.

Messages from the NCC to the poller are sent through an NCC-to-poller (NP) 16-bit hardware register which is addressable by both

the NCC and the poller. The transfer of data to this register by the NCC causes the NP ready bit to be set (bit 15 of IOC1). This bit is used in two ways. If the poller's level-2 interrupt is enabled, the setting of the NP ready bit causes an interrupt. If the interrupt is not enabled, the bit can be tested by the poller software. In either case, reading of the NP register by the poller causes the bit to be reset.

During normal operation (after initialization is complete) all messages sent to the poller from the NCC are three words long. Each word contains two bytes of data exactly as it will be output to the cable. The poller interrupt is enabled throughout the processing phase and intermittently in the message transmission phase, as time allows. The first word of a message from the NCC causes an interrupt; the interrupt service routine disables the interrupt and reads the 3-word message through the NP register as each word is loaded by the NCC. The poller and the NCC test the NP ready bit. As the message is read, it is stored in the NCC queue, which is a list of messages to be output to the cable. After the third word, the interrupt is re-enabled and the interrupted processing is resumed.

Messages are sent from the poller to the NCC through another 16-bit register, called the poller-to-NCC (PN) register, addressable by both the poller and the NCC. Loading of this register by the

poller causes a PN ready bit to be set (bit 7 of IOC1). Reading of the register by the NCC causes it to be reset. When the NCC interrupt is enabled (bit 6 of IOC2), the transfer of data to the PN register causes an interrupt of the NCC. Messages to the NCC are three words long and are transferred in much the same way as those from the NCC to the poller.

A.4.3 Initialization

Initialization starts with the setting of the initialize bit (bit 1 of IOC2) by the network control computer, which causes the poller hardware to clear its buffers, reset flags, etc., and be prepared to start transmitting the first group of 256 flag pulses as soon as the go bit (bit 0 of IOC2) is set. It also triggers the NINIT (see Reference 16) signal in the microprocessor, which causes a microprogrammed initialization routine to be executed. This routine disables interrupts, clears flags, and transfers control to the poller initialization routine.

While the poller is in the initialization routine, it works closely with the network control computer. Interrupts are disabled in both the poller and the NCC, and data is passed back and forth through the PN and NP registers with both processors testing the ready bits in IOC1 for the presence of data.

The user data table in the NCC contains a record of all assigned user directory addresses and types of equipment at each station, as well as a record of the status of each equipment -- busy or not busy, in service or out of service. At initialization time, any pre-established connections are broken, all equipments are marked "not busy" in the NCC's user data table and, as an initial assumption, equipments are marked "in service". The major function of the poller initialization routine is to poll each keypad for the status of the equipment at the work station and send status information to the NCC to correct the assumptions made about the in- or out-of-service condition of user equipment.

The first step in the status initialization procedure is the creation of a status table in the poller. Figure A-8 showed the format of the table. User addresses are not included in the table. One word is allocated for each address, whether assigned or unassigned, from #1 to the maximum assigned user number. After setting the initialize bit in IOC2, the NCC sends the assumed status of user #1 (the multiport data buffer) to the poller through the NP register. The poller stores the word as the first entry in its status table. The NCC sends a 1-word status message for user #2, #3, etc., up to the highest assigned user number. The poller stores these words as consecutive entries in its table. For unassigned user numbers, the NCC sends a word with the high-order bit set to 1. A word of 1's is sent to terminate the table.

After the status table is complete, the poller software sets the go bit in IOC2 to activate the poller/cable interface hardware. This action causes the hardware to start transmitting flag pulses and signaling the software when it is time to send messages. An initialization poll is sent to each user; in response, a keypad control unit initializes itself and sends back its status. There is one message time delay in the response, so the order of processing is: 1) a poll is sent to user #1 (the MDB) while no response is received at the poller; 2) a poll is sent to the first user keypad while the response is read from the MDB; and 3) a poll is sent to the second keypad control unit while the response is read from the first, etc. When there is no response to an initialization poll or the status does not match the assumed status in the poller's status table, a 2-word message is sent to the NCC through the PN register. The first word contains the user directory address and the second contains the new status. The NCC detects the presence of a message by testing the PN ready bit.

Initialization is finished when the response to the last initialization poll has been processed. The poller resets the initialize bit in IOC2 as a signal to the NCC that the poller is starting normal operation. The poller then enables its level-2 interrupt, which allows the NCC to interrupt the poller with messages bound for the cable, and also enables the master interrupt,

which is reset throughout initialization. (See Reference 16 for a discussion of interrupt levels.)

A.4.4 Peripheral Registers

A detailed listing of the peripheral registers used in the S&S poller is given below. The hexadecimal address used by the poller software to address each register is indicated by the eight thousand series number.

PN - 8000 - Poller-to-NCC Register: A 16-bit register addressable by both the poller and the NCC used for sending data from the poller to the NCC. Writing into the PN causes the PN ready bit in IOC1 to set. Reading from the PN causes the bit to be cleared.

NP - 8001 - NCC-to-Poller Register: A 16-bit register addressable by both the poller and the NCC used for sending data from NCC to poller. Writing into the NP causes the NP ready bit in IOC1 to be set. Reading from the NP causes the bit to be cleared.

PC - 8006 - Poller-to-Cable Register: An 8-bit register used for outputting messages to the cable. JC13 is set when it is

time for the PC to be loaded by the software and is cleared after the PC is loaded.

CP - 8005 - Cable-to-Poller Register: An 8-bit register used for inputting messages from the cable. JC15 is set when the CP has been loaded by the hardware and is cleared after the CP has been read by the software.

FIFO - 8002 - Flag-for-Service Queue: A 14-bit register through which the software obtains the addresses of keypads that have flagged for service. The FIFO ready bit in IOC1 occurs whenever FIFO contains an address. The reading of FIFO by the software causes another address to enter the FIFO register if there has been another flag for service; otherwise, the FIFO ready bit is cleared. (Note: The addresses in FIFO are actually one greater than the keypad directory addresses that they represent. The software, after reading the register, must subtract one to obtain the correct address. See Figure A-6.)

IOC1 - 8003 - I/O Control Word: A 3-bit register containing flags that are controlled by hardware and that can be tested by the software of both the poller and the NCC. The bits are assigned as follows:

Bit 7 - PN Ready: A bit set when the PN register contains data for the NCC and reset when the PN register is read. If the NCC interrupt is enabled, the setting of this bit causes an interrupt.

Bit 13 - FIFO Ready: A bit that is set when the FIFO register contains a directory address and which remains set as long as the flag-for-service queue contains at least one address. The bit is cleared when the last directory address is read from the FIFO register by the poller software.

Bit 15 - NP Ready: a bit that is set when the NP register contains data for the poller and is reset when the data is read. If the poller's IEN2 (interrupt enable 2) flag is set, the setting of the NP ready bit causes an interrupt in the poller.

IOC2 - 8004 - I/O Control Word 2: A 3-bit register containing flags which are controlled by the software of the poller and the NCC. The bits are assigned as follows:

Bit 0 - Go bit: A bit used to control the operation of the poller-to-cable interface hardware that is cleared by the NCC at the same time the initialize bit is set by the

NCC. Clearing of the go bit stops transmission to the cable. The go bit is set by the poller software during the initialization routine. When the go bit is set the hardware starts transmitting the first set of 256 flag pulses.

Bit 1 - Initialize: A bit set by the NCC software during the NCC initialization routine which causes the poller to begin its own initialization procedure. The bit is reset by the poller software to indicate to the NCC that the poller initialization is complete.

Bit 6 - NCC Interrupt Enable: A bit controlled by the NCC software that enables the NCC to be interrupted by the poller when the PN ready bit is set.

A.5 SIGNALING AND SUPERVISION KEYPAD CONTROL UNIT

The keypad control unit provides a man/machine interface with the signaling and supervision subsystem via the keypad and its associated status lamps. It is subdivided into the five functional blocks shown in Figure A-11. These are:

a. Flag-for-service logic,

b. S&S message transmitter and receiver,

c. Operator interface,

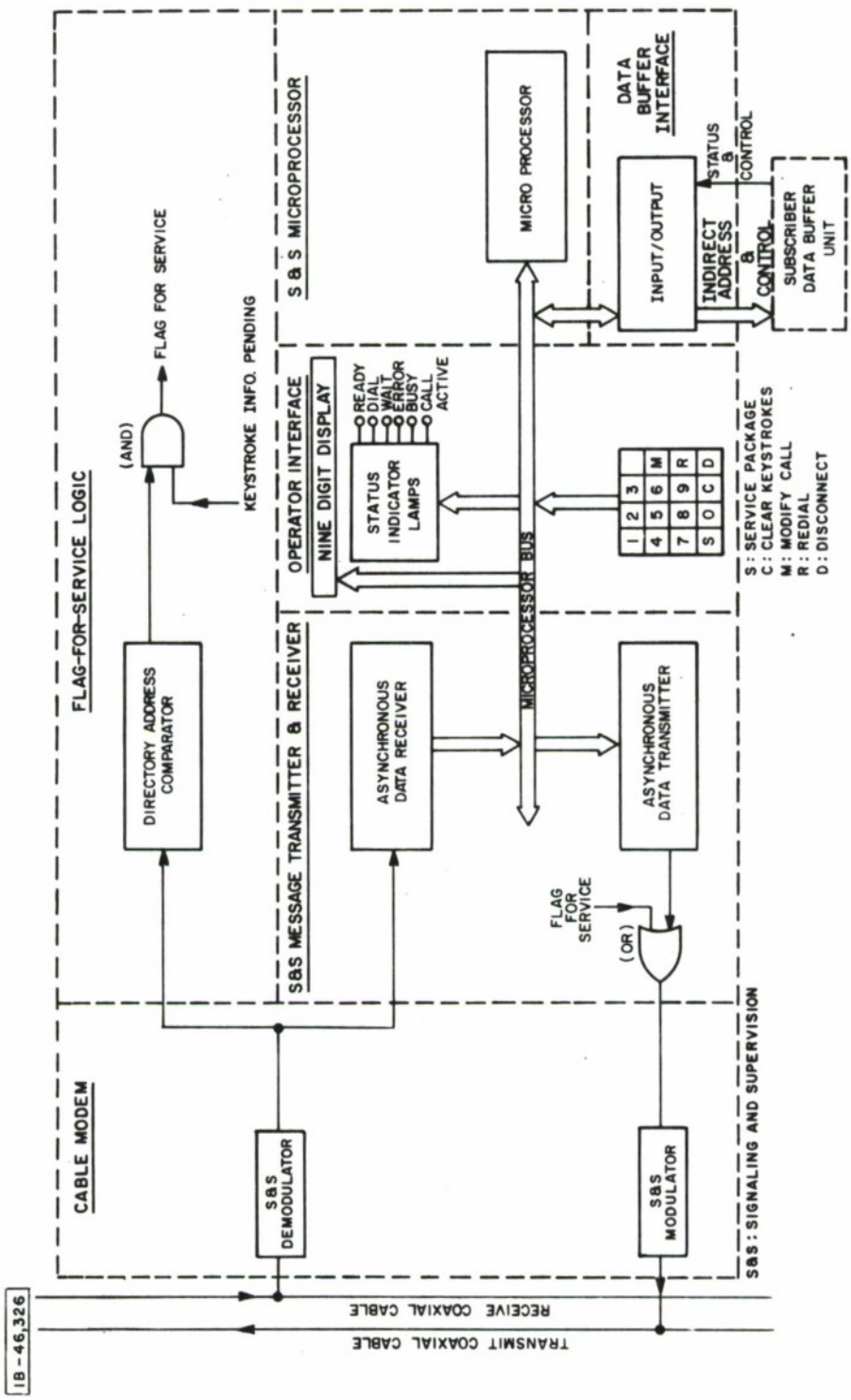

Figure A-11. Block Diagram of Keypad Control Unit

d. S&S microprocessor, and

e. Data buffer interface.

A photograph of the unit was shown in Figure 1-4; a detailed photograph in Figure A-12 shows the various functional units as discussed in the text of this subsection.

A.5.1 Flag-For-Service Logic and Cable Delay Compensator

The following discussion is based on Figure A-13. The output of the S&S demodulator is applied simultaneously to both the frame gap detector and the AND gate input of the bit counter (256). After detecting the frame gap at the start of the S&S message, the frame gap detector sends the frame sync (FS) signal to set the count/data steering flip-flop. This causes the count enable line to go high. If the power-is-up signal is also present, the AND gate of the bit counter (256) is enabled, and the counter will commence counting the pulses in the first flag-for-service field.

Either a frame sync signal or a power clear signal will cause a reset signal to be applied to the bit counter (256) and the block counter (64). Since there are 64 message blocks in one time frame, with each block containing 256 bits, a block counter is needed in addition to the bit counter to accumulate the total of 16,384 (2^{14}) flag-for-service pulses. When the flag-for-service field portion of

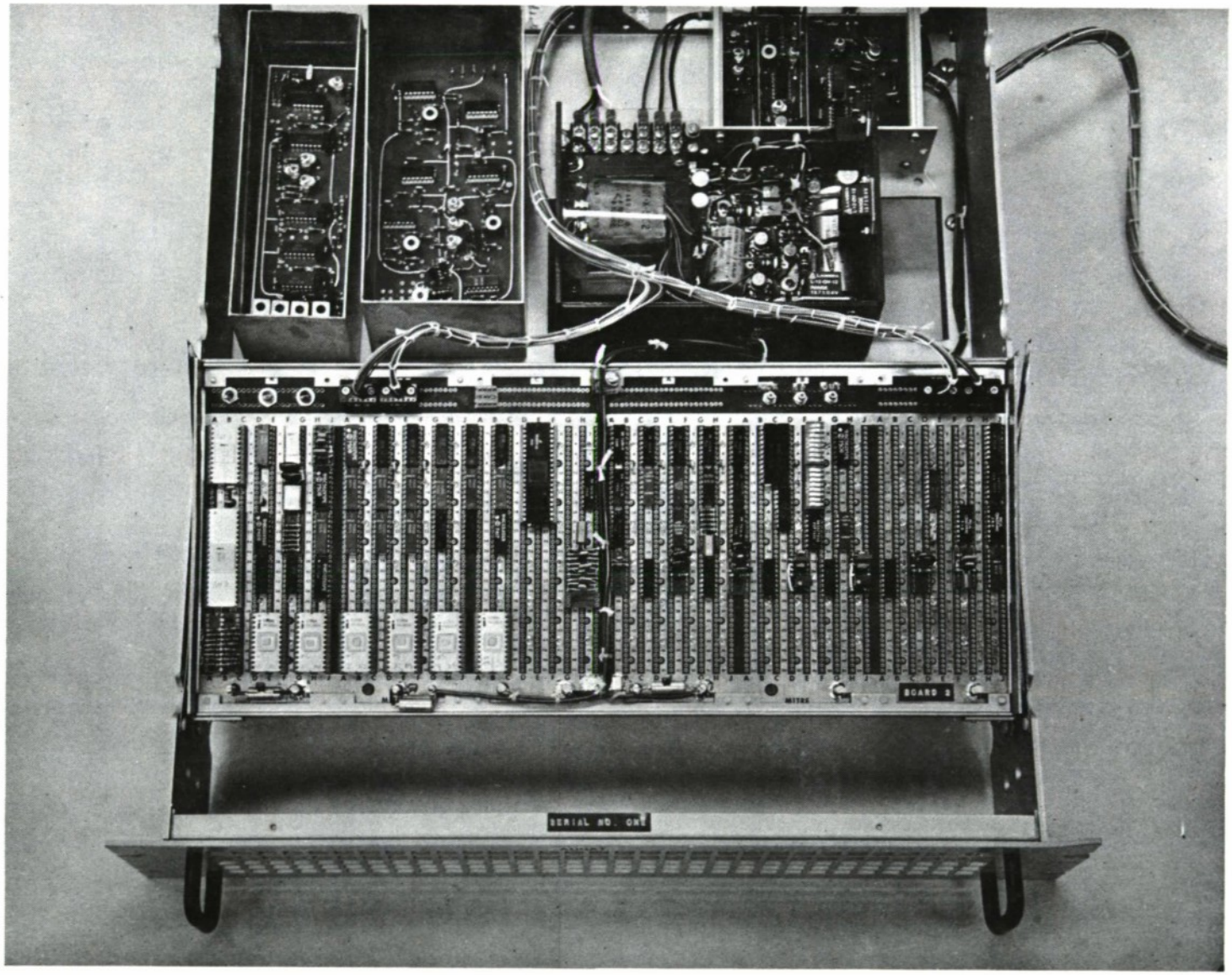

Figure A-12. Close-up View of Keypad Control Unit

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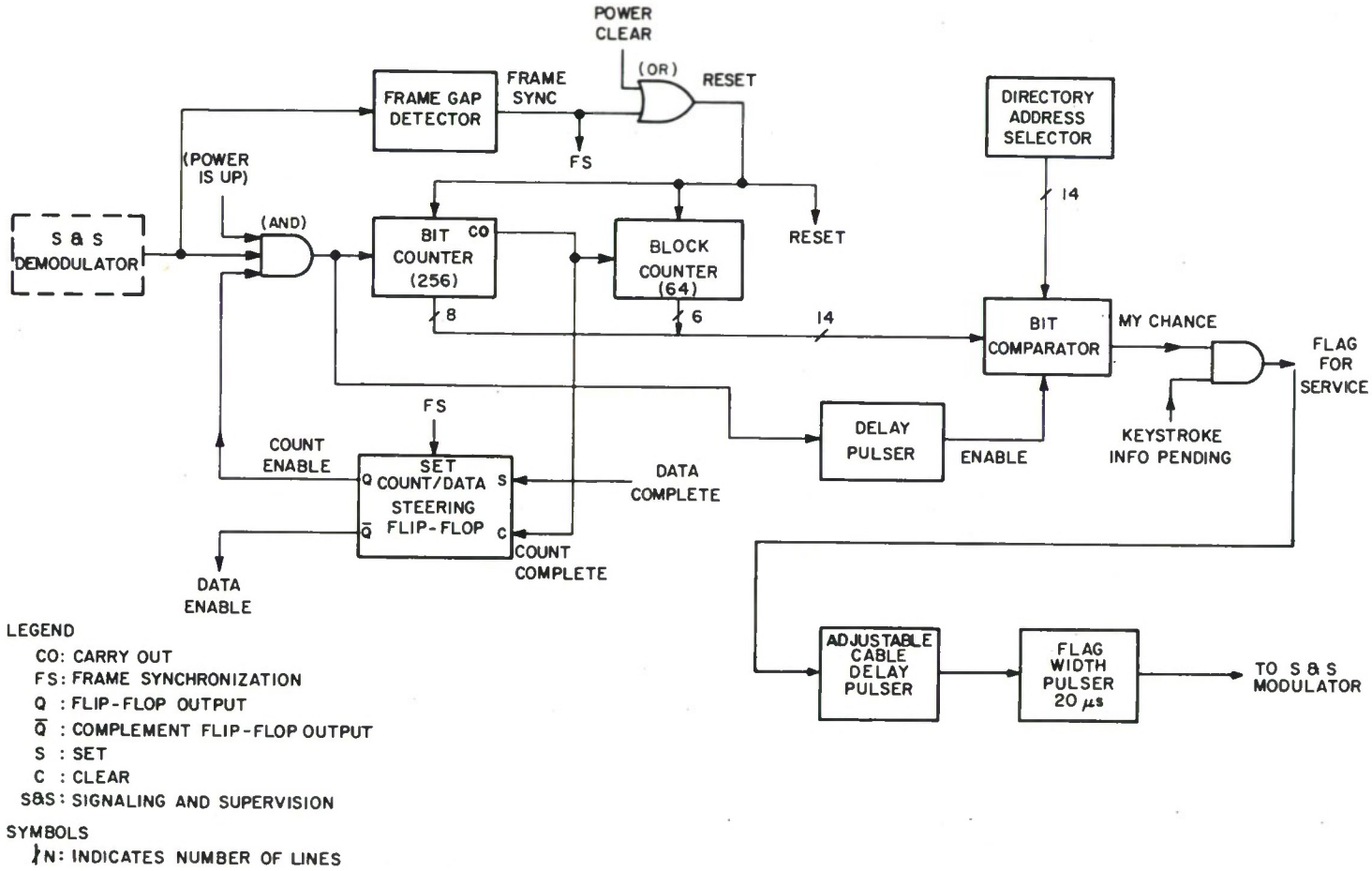

Figure A-13. Flag-for-Service Logic

the time group reaches the 256th bit count, the bit counter (256) enables the carry out signal, which sets the first count in the block counter and clears the count/data steering flip-flop. In effect, the steering flip-flop switches off the count enable signal, thus disabling the bit counter (256), and switches on the data enable signal. The data enable line is routed to the signaling and supervision data transmitter and receiver logic circuits.

During the preceeding process, the bit count and the block count are being constantly sent to the bit comparator. The total bit count during the entire time frame is compared to the output of the address selector which has been manually set to contain that subscriber's directory address. When the bit comparator finds a match, it causes the signal "My Chance" to occur. If the keystroke-information-pending signal is being received from the operator interface unit (as the result of an operator entering keystrokes), the flag-for-service line becomes active.

To compensate for a fixed cable delay between the subscriber's location and the S&S poller, a cable delay pulser is required, which is adjusted so that the flag-for-service pulse (which is 20 μs wide) arrives at the S&S poller in the middle of the next flag bit time as was shown in Figure A-6. Note that since each flag period is 40 μs wide, the generated flag pulse of 20 μs allows

a 10 μs guard zone on either side to allow for cable delay variations.

A.5.2 S&S Data Receiver and Transmitter

The following discussion is based on Figure A-14. When the bit counter of the flag-for-service logic reaches a count of 256, it sends a count complete signal to the count/data steering flip-flop. The $\overline{Q}$ output of the flip-flop sends a data enable signal to the AND gate preceding the asynchronous receiver in order to begin collecting the S&S message. The asynchronous receiver has an internal double-buffer register structure to allow overlap in holding a word for parallel output while at the same time inputting a second word. Assuming the power is up, the demodulated S&S signal is able to pass through the AND gate to the asynchronous receiver. The asynchronous receiver recognizes the first transition as a start bit and shifts the next eight bits into its receiver register. After the stop bit is detected, the contents of the shift register are transferred in bit-parallel form to the second register of the double buffer, that is, the receiver holding register. In addition, the parity bit is checked and, if parity is not valid, a signal is placed on its status line. After receipt of the entire 8-bit byte, a data ready signal is generated which performs the following functions:

a. Sends an interrupt signal to the microprocessor,

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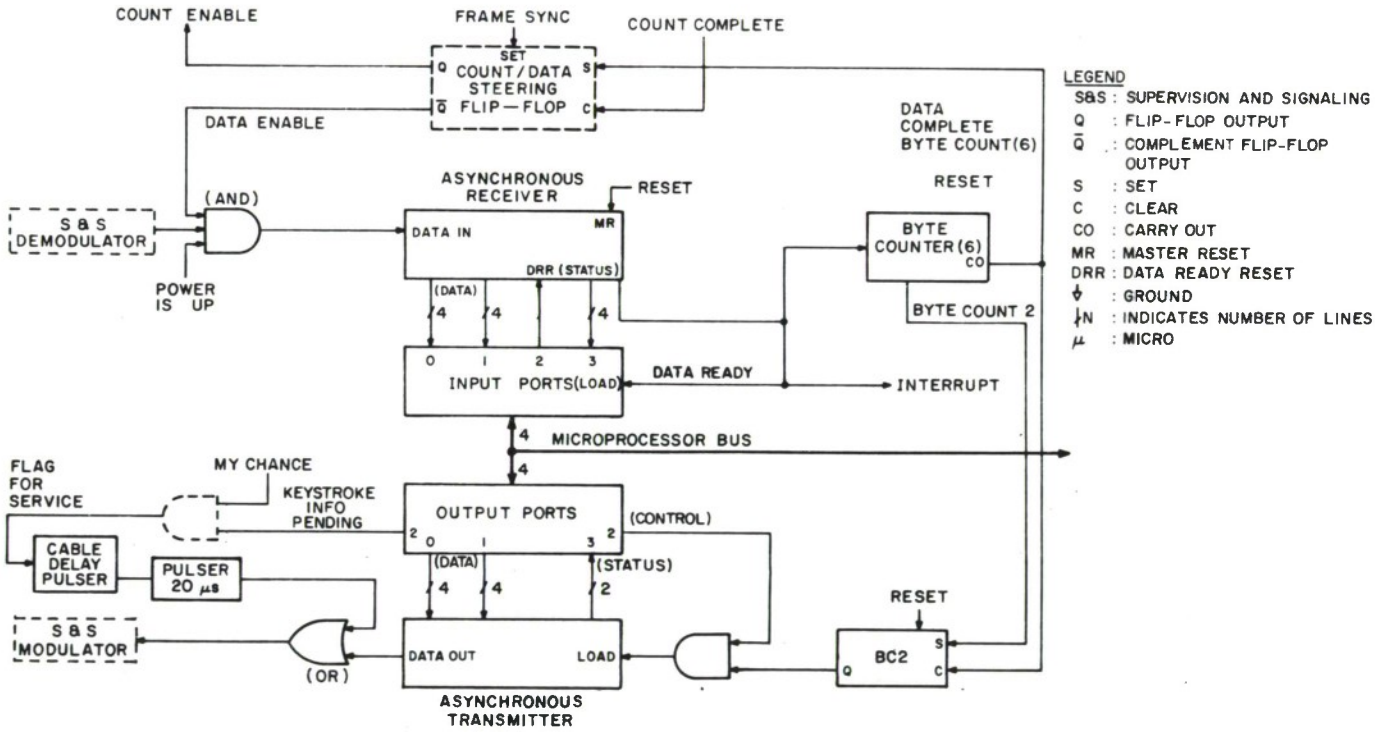


Figure A-14. Signaling and Supervision Data Receiver and Transmitter

b. Sends a load signal to the input port chip of the microprocessor, and

c. Sends a signal to the byte counter (6), which advances the byte counter by one.

Upon receipt of the load command from the asynchronous receiver the input port chip of the microprocessor accepts the eight bits in parallel over its incoming eight data lines. The incoming eight data lines are divided between Ports 0 and 1 with each port servicing four lines. The input port chip also reads in the parity and other status bits through Port 3. The microprocessor then sends a data ready reset (DRR) signal via Port 2 to the asynchronous receiver to indicate the completion of the byte transfer.

The interrupt signal received by the microprocessor causes an immediate branch to a special location in memory, which identifies the new program sequence (called an interrupt handler) to be followed. The microprocessor then sends three successive commands to the input port chip. On receipt of the first command, the input port chip loads the first data nibble (four bits) in Port 0 on the bus. On receipt of the second command, it loads the next nibble from Port 1. On receipt of the third command, it loads the status nibble from Port 3. Upon receipt of these three nibbles, the microprocessor branches back to its original program and continues

its background operations under control of its supervisor program until it is interrupted again.

Each time an incoming character byte is received, the byte counter (6) is advanced by a count of one. When the second character is received, the byte counter (6) sends a byte count 2 signal, which sets the BC2 flip-flop. The output of this flip-flop is sent to an AND gate, which is used as a control element for the asynchronous transmitter. If the microprocessor has sent a keystroke or status message over the microprocessor bus to its output port chip, the chip enables the other half of the AND gate through its control line. This control line is activated by the microprocessor in the next message block after receiving an interrogation poll at a point in time to leave a considerable guard band on either side of the transmitted message. This was shown in Figure A-6. The enabled AND gate activates a load signal to the asynchronous transmitter, which then reads the output data in bit-parallel from Ports 0 and 1 and begins serial transmission of keystroke and status information.

The asynchronous transmitter also has a double-buffer register structure similar to the asynchronous receiver. The register interface in the output port chip is called the transmitter-holding register, and the register interfacing the modulator is called the transmitter register. The asynchronous

transmitter transfers a character internally in bit-parallel mode from the transmitter-holding register to the transmitter register. This frees the transmitter-holding register to be available to accept the next character from the output port chip. In the meantime, the asynchronous transmitter sends the character in its transmitter register to the modulator in bit-serial mode.

This double-buffer feature of the transmitter and receiver allows the microprocessor almost one character transmission time to perform other background routines. If the double buffer were not present, the microprocessor would have to act within one bit time whenever characters were being transmitted or received.

The control cycle is complete when six incoming bytes have been received by the byte counter (6). The carry out signal is enabled and applied to the set lead of the count/data steering flip-flop, which in turn enables the flag-for-service counting logic to count the next flag-for-service field. In addition, the carry out signal is sent to clear the BC2 flip-flop, which disables the AND gate control line to the asynchronous transmitter.

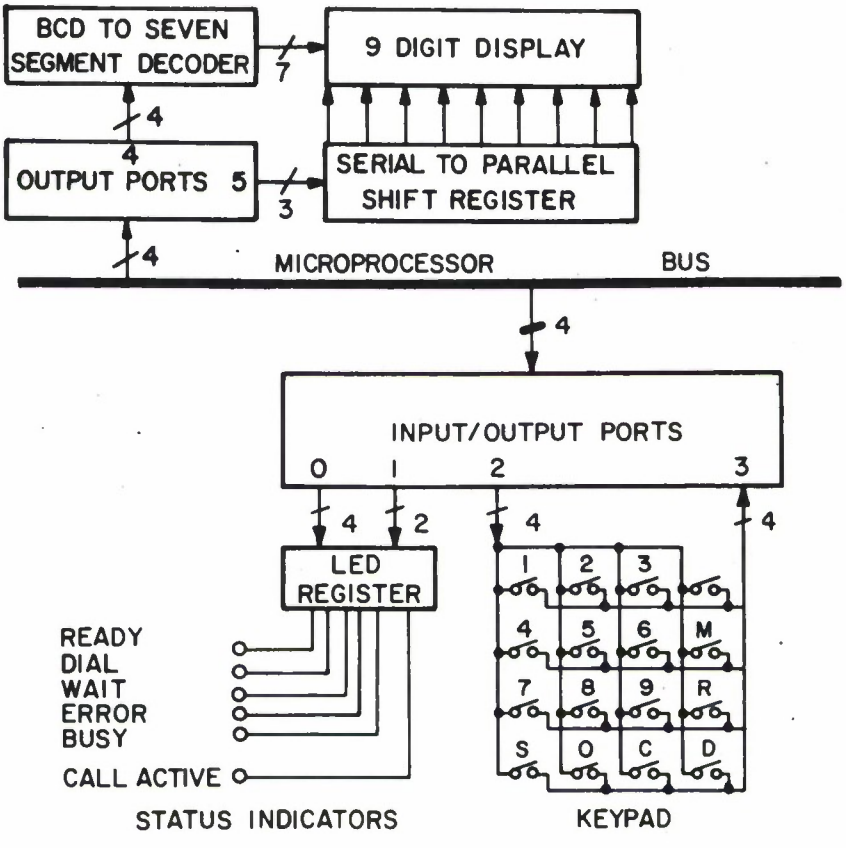
A.5.3 Operator Interface

The keypad device, status indicators, and keystroke display are connected to the microprocessor through other output port chips

as illustrated in Figure A-15. Each port services four lines, so Ports 0 and 1 are used to service the six indicator lamps, leaving two spare lines on Port 1. The keypad is connected via the four outgoing lines of Port 3 and the four incoming status lines of Port 4.

The microprocesor is programmed to scan the keypad as part of its background software routine. Thus the keypad need not send an interrupt signal to the microprocessor, as was the case with the asynchronous receiver. The keypad is arranged as a 4 X 4 matrix of key switches. Under program control, the first line of the output port is activated. All four input lines to the keypad are read and tested to see if a key has been pressed, and if so, which one it was. Then the next line is activated, and so on, until the entire keyboard has been scanned.

Keystroke characters are thus stored in the RAM (random access) memory and a flag-for-service is invoked. As keystrokes are collected, they are also displayed on the 9-digit display for operator convenience. Stored keystrokes are then transmitted to the S&S poller upon interrogation polling.



LEGEND

M : MODIFY CALL
R : REDIAL
S : SERVICE PACKAGE
C : CLEAR KEYSTROKES
D : DISCONNECT
LED: LIGHT EMITTING DIODE

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SYMBOL

/ N: INDICATES NUMBER OF LINES

Figure A-15. Operator Interface

A.5.4 S&S Microprocessor

The microprocessor for the keypad control unit consists of a central processing unit (CPU), a clock, and random access (RAM) and read-only (ROM) memory chips. This is illustrated in Figure A-16. The CPU receives four signals from the clock driver chip. The clock driver chip contains a crystal controlled oscillator, clock generation circuitry, and two phase clock driver circuits. The reset signal is generated whenever power is initially activated. Phase-1 and phase-2 signals provide the basic timing circuits for the entire microprocessor system. The stop signal allowed the CPU to execute instructions one at a time for initial design debugging.

The CPU is a single-chip, 4-bit parallel MOS (metal-oxide semiconductor) device, manufactured by the Intel Corporation. The CPU contains the necessary hardware to accept and process single level interrupts as from the asynchronous data receiver. It generates a synchronization signal, sent to the various RAM, ROM chips and other peripheral chips in the system, which indicates the beginning of an instruction cycle. The unit connects to a bidirectional data bus called the microprocessor bus. All transfer of address and data communications between the processor and the RAM, ROM, and peripheral chips is handled by way of these four lines.

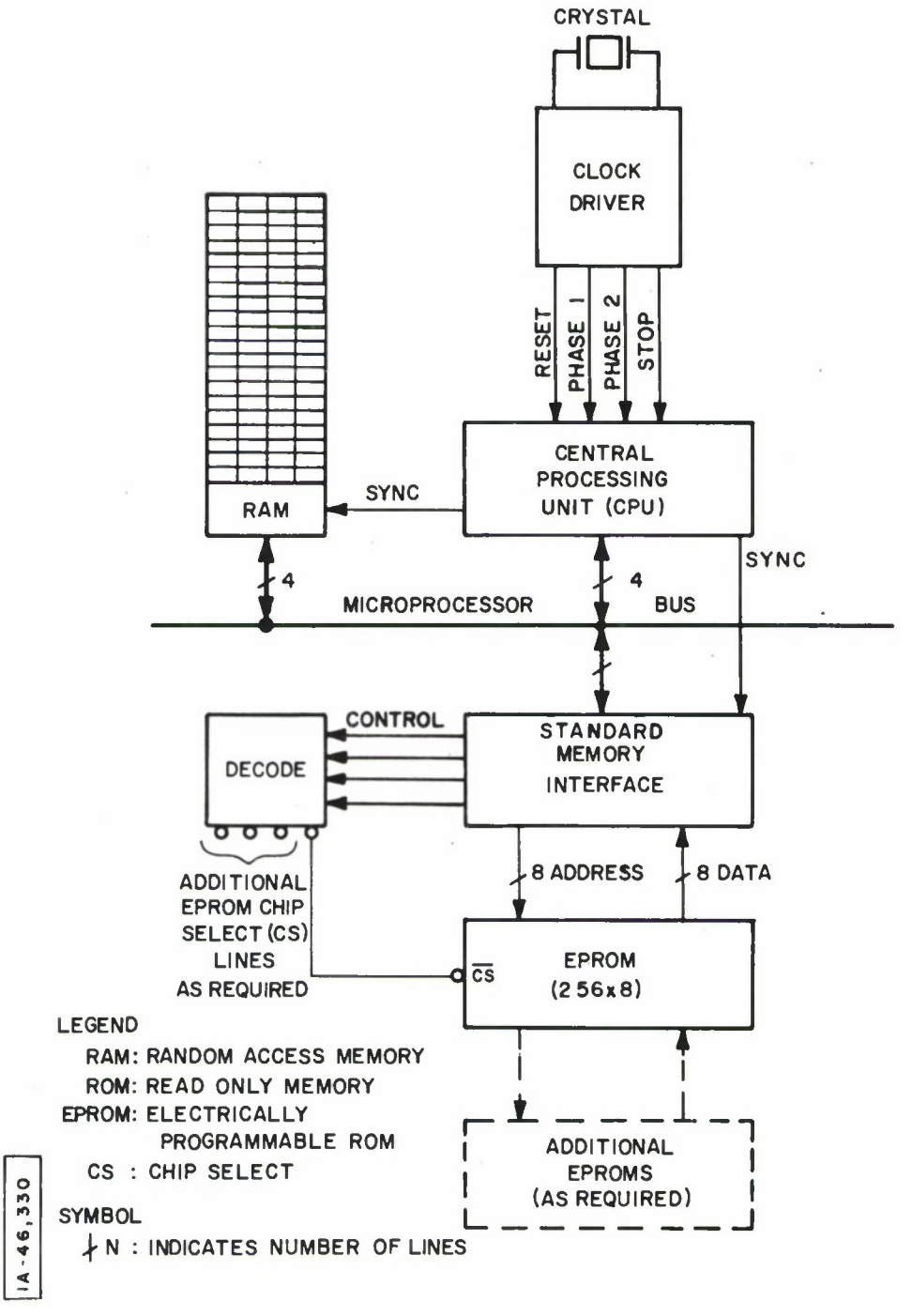


Figure A-16. Keypad Control Unit Microprocessor

A RAM memory chip can store 320 bits arranged in four registers of twenty 4-bit nibbles. The 80 nibbles of storage are so indicated in Figure A-16. The RAM memory is used in this application to store received information characters, keystrokes, indirect data buffer addresses, indicator status lamps, etc.

The ROM memory is of the erasable and programmable type and thus is sometimes called an EPROM. The EPROM is a 256-by-8 bit memory that is equivalent to 256 bytes of program instruction. Each instruction may consist of one or two bytes. The EPROM is packaged in a 24-pin, dual-in-line package with a transparent quartz lid, which allows the user to expose the chip to ultraviolet light to erase the memory pattern. A new pattern can then be written into the device by a piece of special programming equipment available from a number of manufacturers. This procedure may be repeated as many times as required during the development of the system.

A standard memory interface chip is used between the EPROMS and the CPU to accommodate up to 16 EPROMS for a total of 4K instruction bytes; slightly less than 2 K bytes were, however, required for this application. The standard memory interface is synchronized to the processor by the sync signal generated by the processor and sent out at the beginning of each instruction cycle. The memory interface chip receives three successive 4-bit nibbles from the CPU and presents these three nibbles in 12-bit parallel

form on the eight address lines and the four control lines. The four control lines are decoded by the decode block, and one of up to 16 EPROM chips is designated. The designated EPROM decodes the eight address leads to select one of the 256 8-bit bytes in its memory. The selected byte is then transferred to the standard memory interface via the eight bits to the CPU as two successive nibbles. It should be noted that the EPROM contains the operating software program as well as the fixed data used by the microprocessor. The RAMs contain the variable data that occur during the transactions processed by the CPU.

A.5.5 Subscriber Data Buffer Interface

The S&S microprocessor interfaces with the subscriber data buffer unit through an input/output port chip as illustrated in Figure A-17. When a subscriber requests data distribution service through his keypad, the network control computer sends two indirect addresses to the keypad control unit for use by the subscriber data buffer unit. These indirect addresses are not permanently assigned to any particular user, and therefore vary from connection to connection. One of the indirect addresses is used by the subscriber unit for receiving its data messages, while the other indirect address is used for transmitting its data to the destination terminal. The two addresses permit full- or half-duplex transmission. Ten of the lines between the input/output port chip

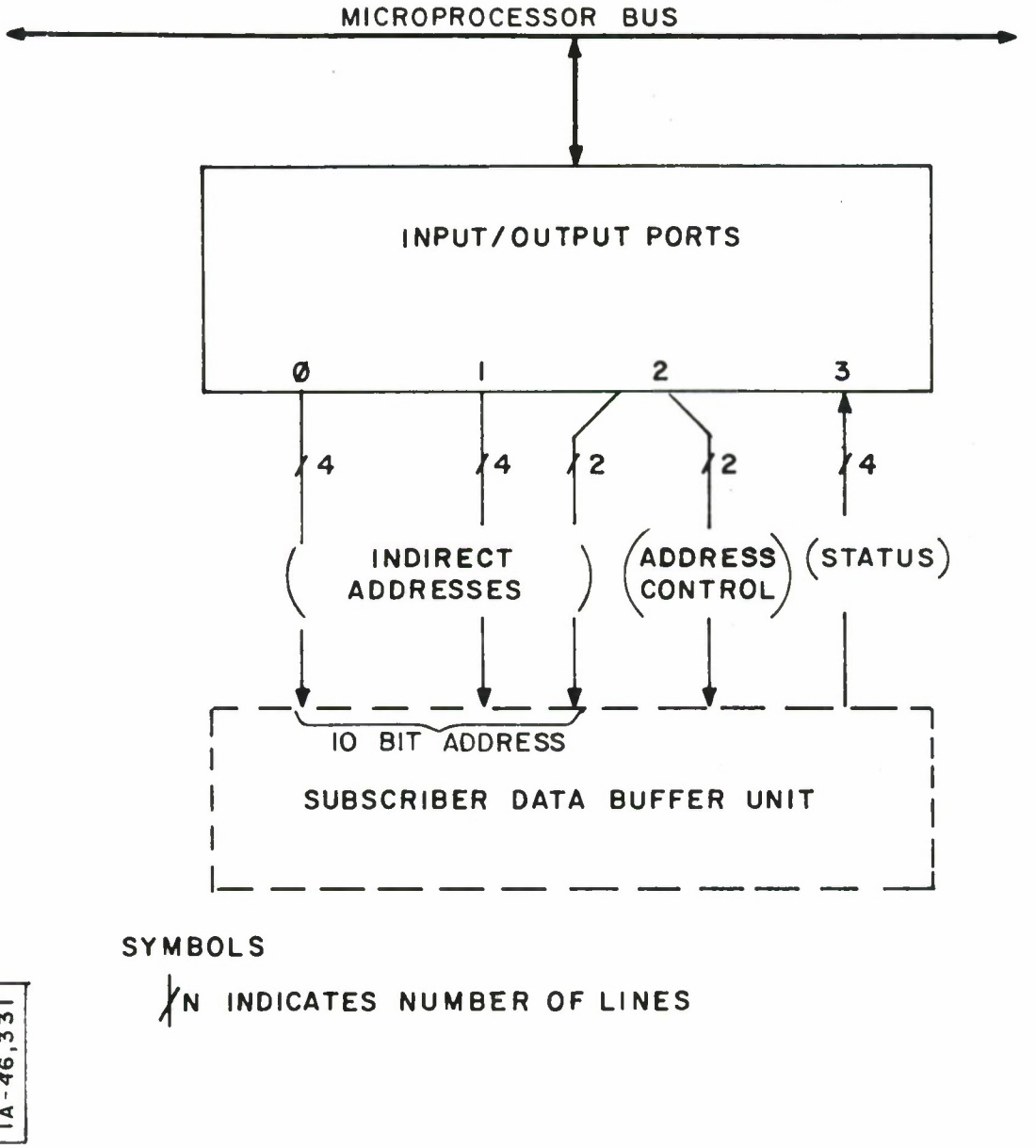


Figure A-17. Subscriber Data Buffer Interface

and the subscriber data buffer are assigned to transferring the indirect address information in bit-parallel form. The remaining lines are devoted to terminal status input.

APPENDIX B

MIDS ADAPTIVE DATA DISTRIBUTION SUBSYSTEM

B.1 GENERAL

The MIDS adaptive data subsystem performs the control and distribution of data messages between subscribers. It is termed adaptive because it will automatically jump from the idle rate of 600 b/s to 19.2 kb/s to handle burst transfers without intervention of the user.

The adaptive data subsystem consists of a data poller and the multiplicity of subscriber data buffer (SDB) units as shown in Figure B-1. The SDB unit is the interface between the cable bus and the subscriber's terminal. Common user equipment that could be time-shared simultaneously by several users is accessed through a multiport data buffer which is similar in concept to the subscriber data buffer.

A form of polled, time divison multiple access (TDMA) multiplexing is used for data transmission, at a rate of 2.25 Mb/s, over the data subsystem channels. With this capacity, up to 1024 terminals can be simultaneously serviced at 600 b/s. Terminals requiring speeds in excess of 600 b/s are automatically switched (by

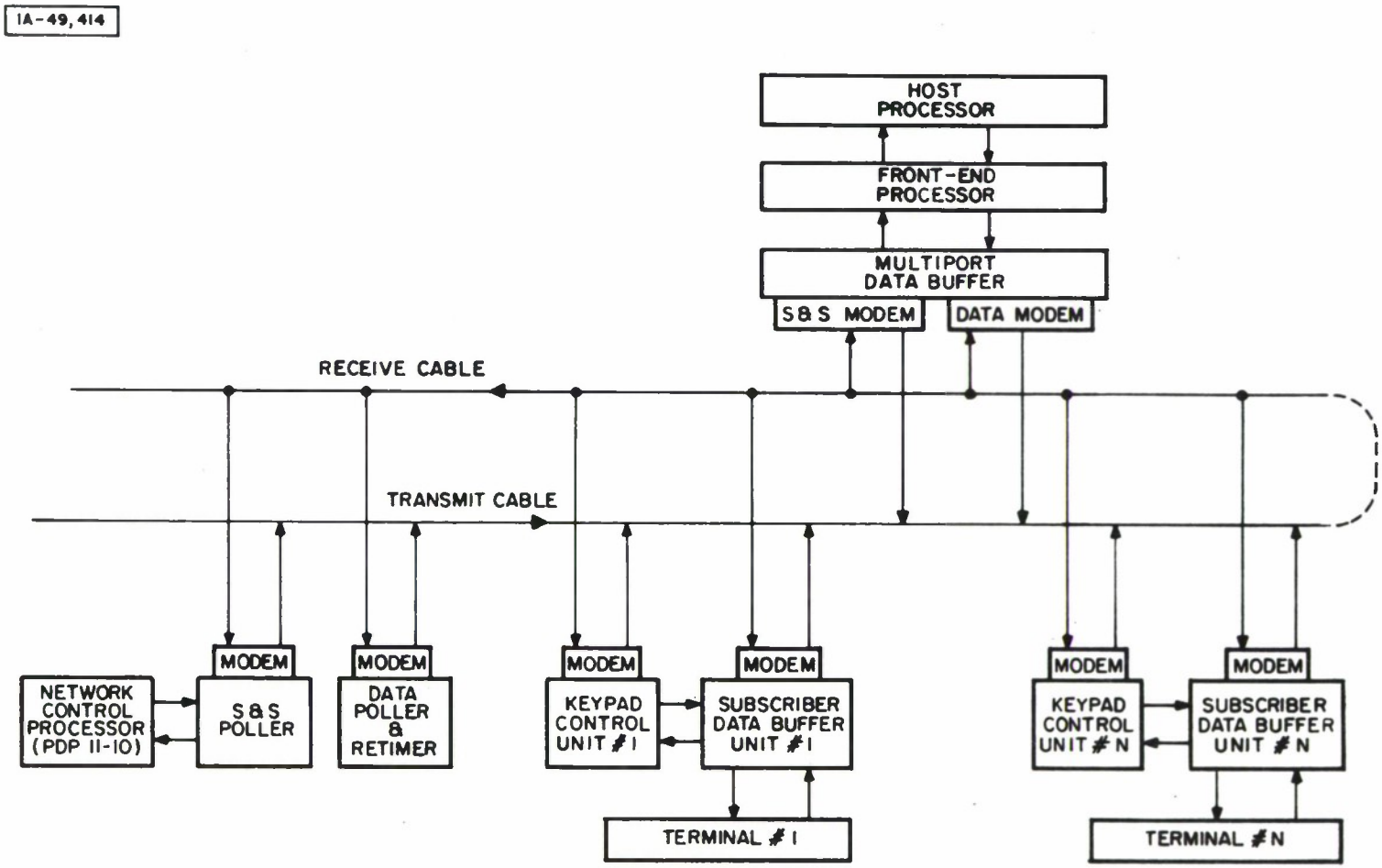


Figure B-1. MIDS Adaptive Data Subsystem and S&S Subsystem Configuration

the data poller) to a higher polling rate, allowing up to 32 subscribers to be serviced at the high-speed polling rate of 19.2 kb/s to adapt to the burst requirements. If more than 32 subscribers simultaneously require high-speed service, all will get higher-speed service but at a proportionately lower rate.

B.1.1 Indirect Address Assignment

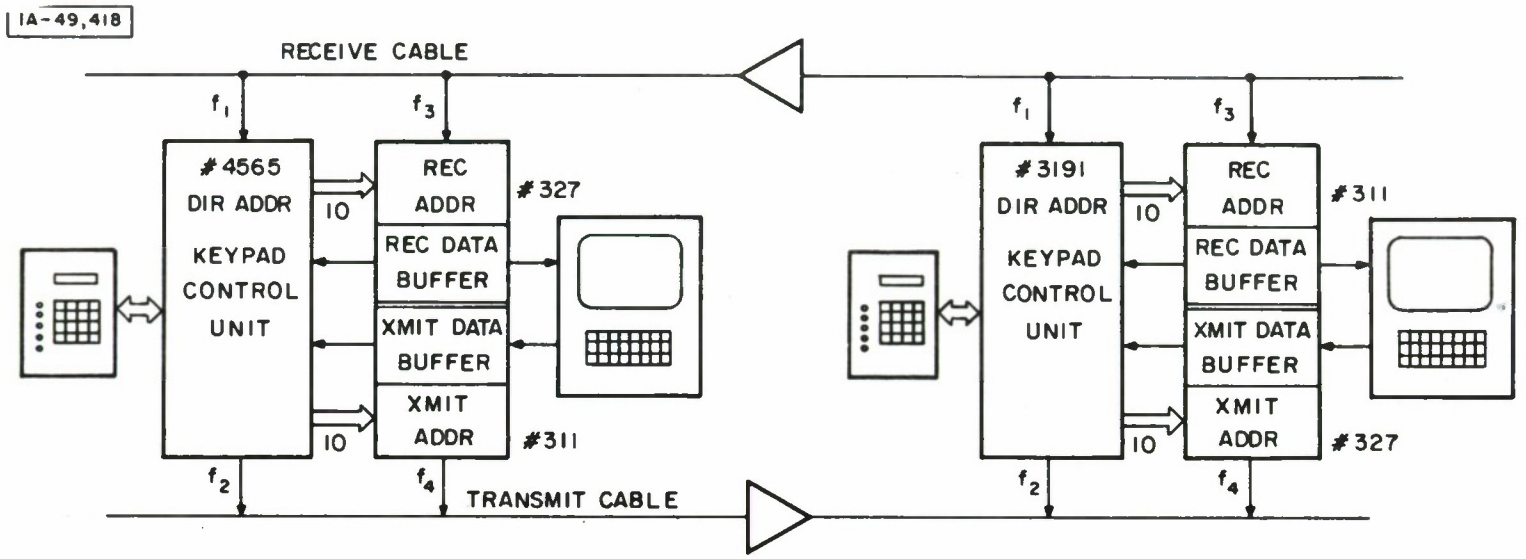
The subscriber initiates the desired data call by making a specific service request on his S&S keypad control unit that is transmitted over the S&S channel to the S&S poller. After the NCC determines that the request is valid (as described in Appendix A), it sends, via the S&S channel, a complementary set of indirect address pairs to the two keypad control units involved with this call connectivity. The keypad control unit, which is collocated with the subscriber data unit, passes the 10-bit indirect address pair to the receiver and transmitter of the data buffer. These indirect addresses are also used as address headers for data messages to be distributed in the data subsystem.

This concept is illustrated in Figure B-2(a), in which the subscribers involved have directory addresses (e.g., the number listed in a subscriber directory) of #4565 and #3191. These numbers are used by the S&S subsystem for keypad polling, etc., as explained in Appendix A.

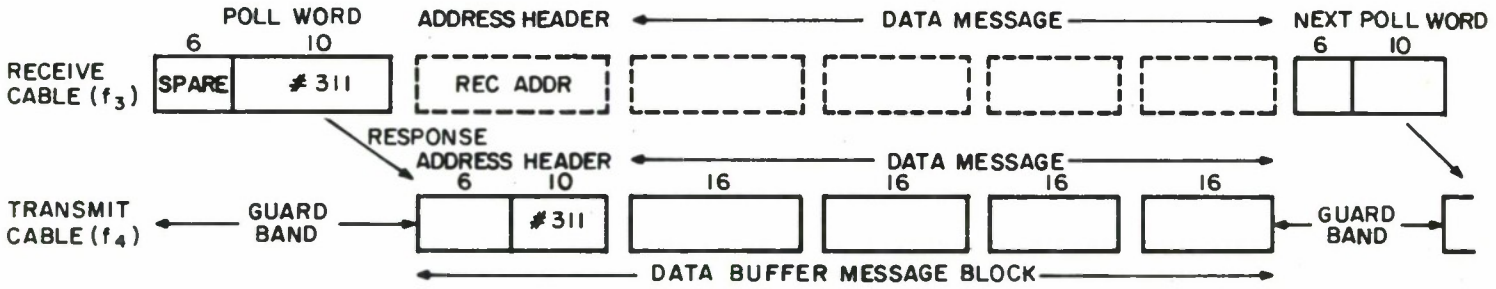
The indirect address pair for data transmission assigned by the S&S subsystem is #311 and #327. The assignment of the indirect address pair for a duplex connectivity is always modulo 16 e.g., they are separated by a numeric 16. This will be discussed further in Section B.2.1. Note that the first subscriber has the transmit address for the data buffer assigned #311 while the second subscriber has the receiver address assigned #311, implying that data can be transmitted from the first to the second. Also, the assignment for the second subscriber's transmitter is #327, which has also been assigned to the first subscriber's receiver. This allows a path in the opposite direction to make the data connectivity full-duplex in nature.

B.1.2 Data Distribution

The scheme for inserting messages in the high-capacity, 2.25 Mb/s TDMA data channel is illustrated in Figure B-2(b). It is the function of the data poller to generate and transmit poll words on a regular basis. All subscriber data buffers examine these poll words on the receive cable at frequency f3. When the address in the poll word compares with the indirect address in the data buffer's transmitter, the transmitter will respond. The response consists of a 64-bit data message preceeded by an address header consisting of six control bits and the transmitter's 10-bit indirect address. The total response is termed a data buffer message block.



(a) Indirect Address Assignments



(b) Data Distribution Scheme

Figure B-2. MIDS Data Distribution Subsystem

The data buffer message block is transmitted on frequency f4 to the data poller, which retimes the message block, inserts it behind the next poll with no alterations, and then retransmits it at frequency f3.

All data buffers examine the address header on the receive cable; when the address compares with the data buffer's indirect receiver address, the 64-bit message is received in that data buffer, which completes the transmission in one direction. A short time later, the transmitter of the second party will be polled, which allows data transmission in the opposite direction, thus accomplishing a full-duplex loop. The periodicity at which the polling occurs determines the average data rate. Control of the polling period and error correcting schemes is described in the following sections.

B.2 ADAPTIVE DATA RATE SUBSYSTEM

The purpose of the adaptive data rate scheme is to allow user terminals to automatically accommodate burst transfer modes. In addition, the scheme will allow terminals of different data rates to communicate with one another, i.e., a high-speed CRT device with a slow-speed teletype device.

At the heart of the adaptive data rate concept is a data poller that will vary the periodicity of polling of a particular subscriber depending upon how fast the subscriber wants to transmit messages. If the receiving party cannot accept data fast enough to keep up with the transmission, the receiving party will override the transmitters request and can in effect hold up transmission of new data until current data is digested (printed, displayed, etc). Thus, data loss is prevented in transmission between two terminals of different data rates.

B.2.1 Data Polling Scheme

The polling scheme used to accomplish the adaptive data rate information transfer is shown in Figure B-3. The poll selector can be thought of as a switch alternating between a low-speed queue and a high-speed queue. The poll selector picks a poll address first from the low-speed queue (which is nothing more than a sequential counter that starts at 0 and increments to 1023) and then picks the next poll address from the high-speed queue. The selector then increments to the next set of numbers and picks another pair, and so on. Since the high-speed queue has only 32 positions, any indirect address within it will be used as a poll and hence serviced 32 times more often than any address in the low-speed queue. The other function of the data poller is to insert received data buffer message blocks held in the retimer buffer immediately behind each

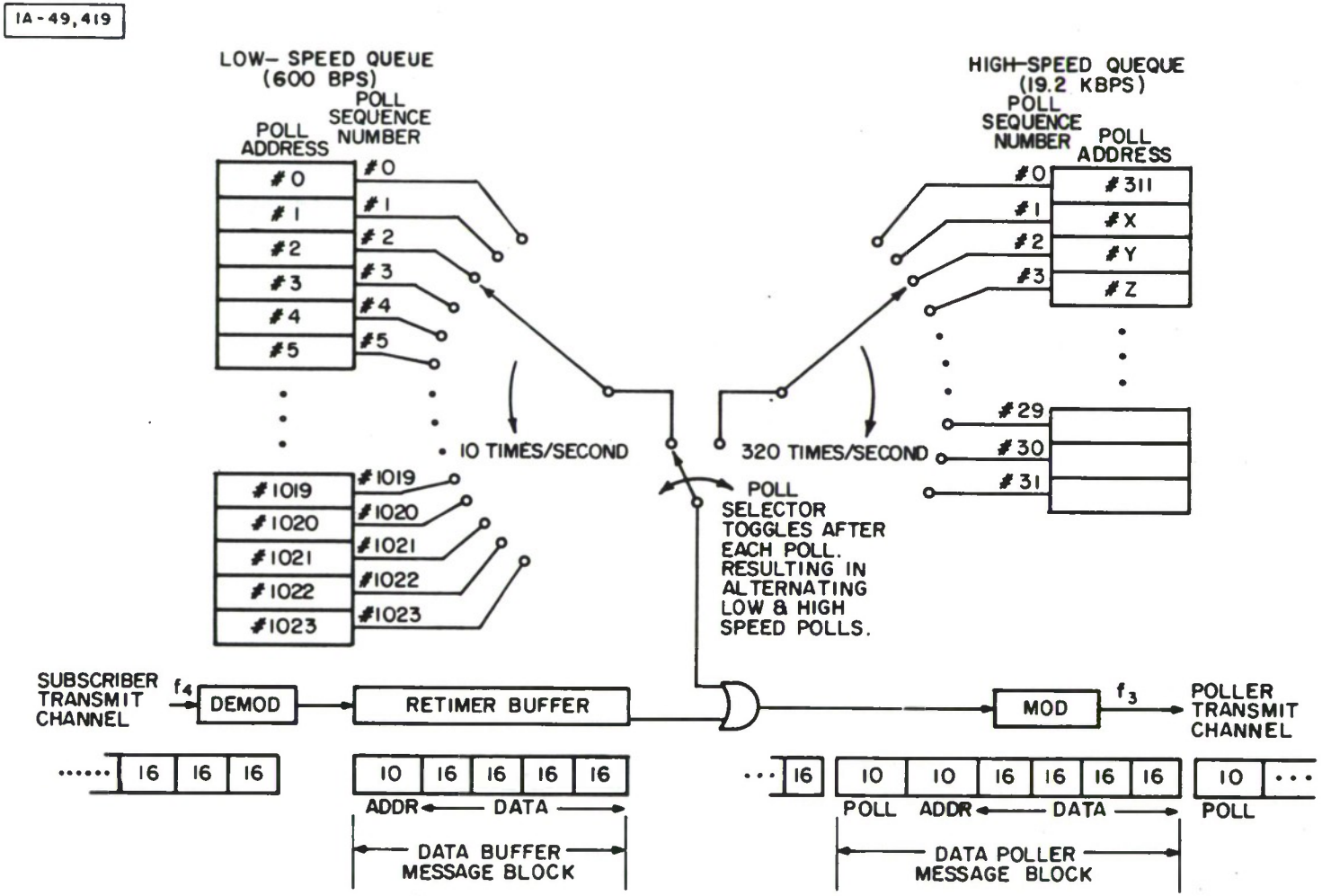


Figure B-3. Adaptive Data Rate Polling Scheme

poll. The transmitted poll along with the retimed data buffer message block form the data poller message block.

A data frame is defined in this subsystem as a sequence of 2048 polls, which is one "sweep" through the low-speed queue and 32 "sweeps" through the high-speed queue. There are approximately 10 data frames per second; therefore, if service has been granted to a subscriber via an assignment of an indirect address, he will be polled approximately 10 times per second, which results in a base data rate slightly over 600 b/s (10 X 64 bits). When burst transfer is required, the subscriber's indirect address is inserted into the high-speed queue; then the data rate is somewhat over 19.2 kb/s (320 X 64 bits = 20,480). The exact rates are inconsequential as the control algorithm will allow the subscriber terminals to communicate at an average rate which is adjusted to the rate of the slowest receiver in the connectivity.

A pictorial representation of the polling sequence is shown in Figure B-4(a). The data frame represents 2048 poll addresses. Low-speed addresses are shown as starting at L_0 and extending to L_{1023}. The high-speed addresss are represented from H_0 to H_{31}. In setting up the data paths, full-duplex links are usually established; therefore the 1,024 low-speed addresses permit 512 full-duplex low-speed links. Since the address pairs are related by the numeric 16, the first 16 addresses in the low-speed polling

sequence are duplex connected to the next 16 addresses. When a subscriber is switched to high-speed service, the duplex partner is also switched, which means that 16 pairs may exist in the high-speed queue. Note that there is equal time between polling the duplex partners on the high-speed queue, which allows reasonable time for the retransmission error correction scheme to operate.

A data polling cycle, shown in Figure B-4(b), consists of 32 low-speed data polls interspaced with 32 high-speed polls. In order to select all of the low-speed addresses (1,048), a total of 32 data polling cycles must occur, which make up the data frame.

When a subscriber data buffer requires high-speed service, a flag is raised in the control portion of the address header. The data poller microprocessor recognizes that request flag and determines which addresses are to be assigned high-speed service in the next data frame. The protocol that handles this assignment gives all requestors a turn at high-speed service, a feature which is central to the system's automatically adaptive data rate capability.

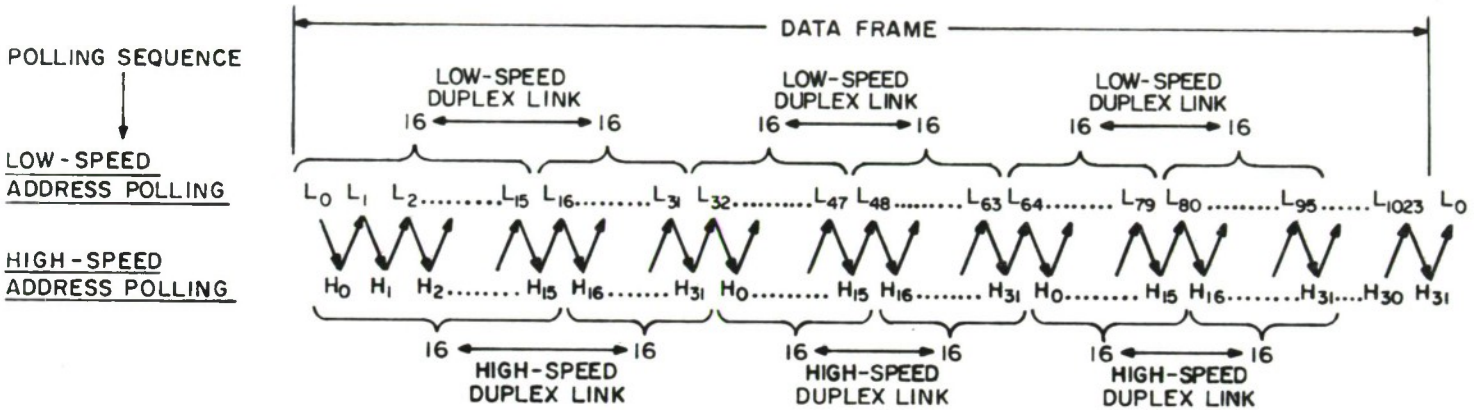


Figure B-4(a). MIDS Adaptive Data Subsystem — Data Frame

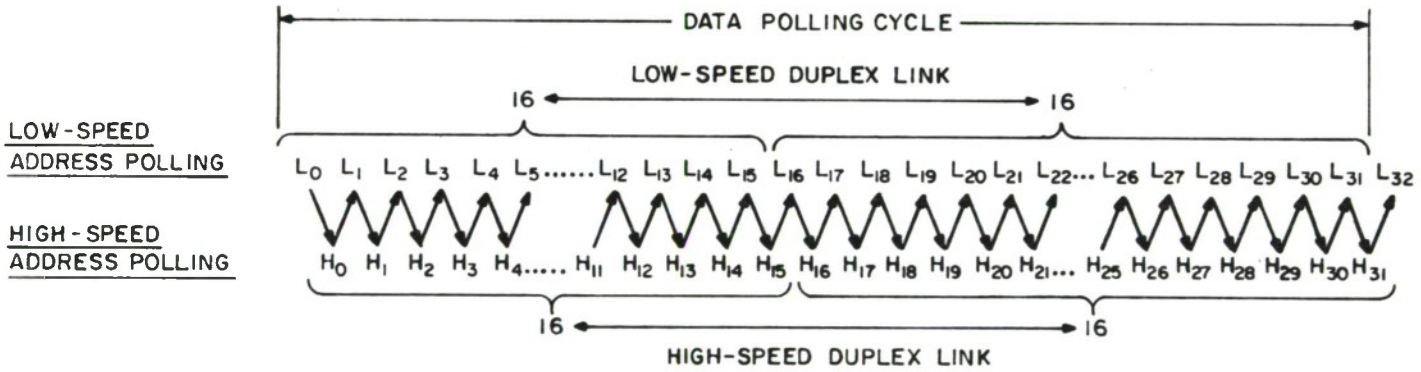


Figure B-4(b). MIDS Adaptive Data Subsystem — Data Polling Cycle

B.2.2 Message Formats

A portion of the 2,048 data poller message blocks data frame is indicated in Figure B-5. In the expanded view, the first data poller message block contains a high-speed polling address (H_1), followed by a low-speed polling address (L_2). The data poller sends a synchronization bit, followed by the H_1 address, which is followed, in turn, by a parity bit. The remainder of the block is used for a data message and associated parity bits.

The message format and bit assignments contained in a data poller message block are detailed in Figure B-6. The first word contains the polling address which is the indirect address of the terminal that is to transmit. The high-order ten bits of the word are assigned to represent one of the 1024 addresses. The low-order six bits of the word, that is 0 through 5, are unassigned. The second word and the remainder of the block is originated at the subscriber data buffer unit as a response to a previous poll. This second word contains an indirect address that each subscriber receiver will examine for correspondence. The high-order ten bits are assigned to this address.

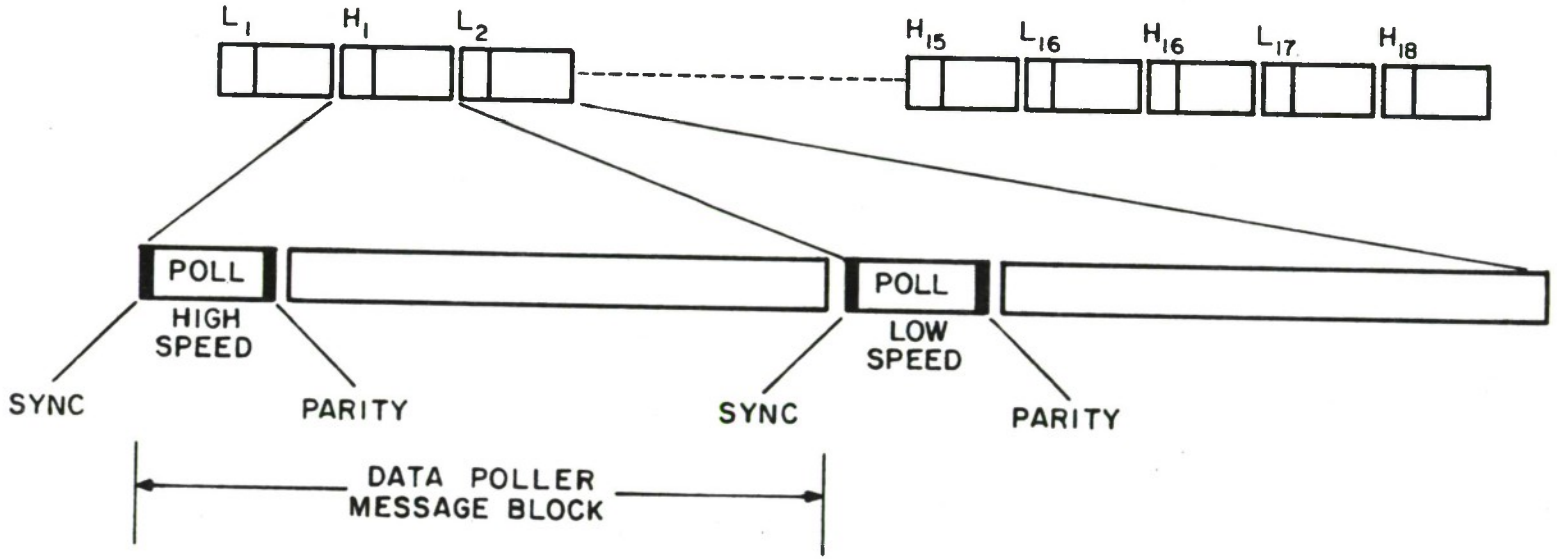


Figure B-5. MIDS Data Subsystem Polling and Timing

IA-46,334

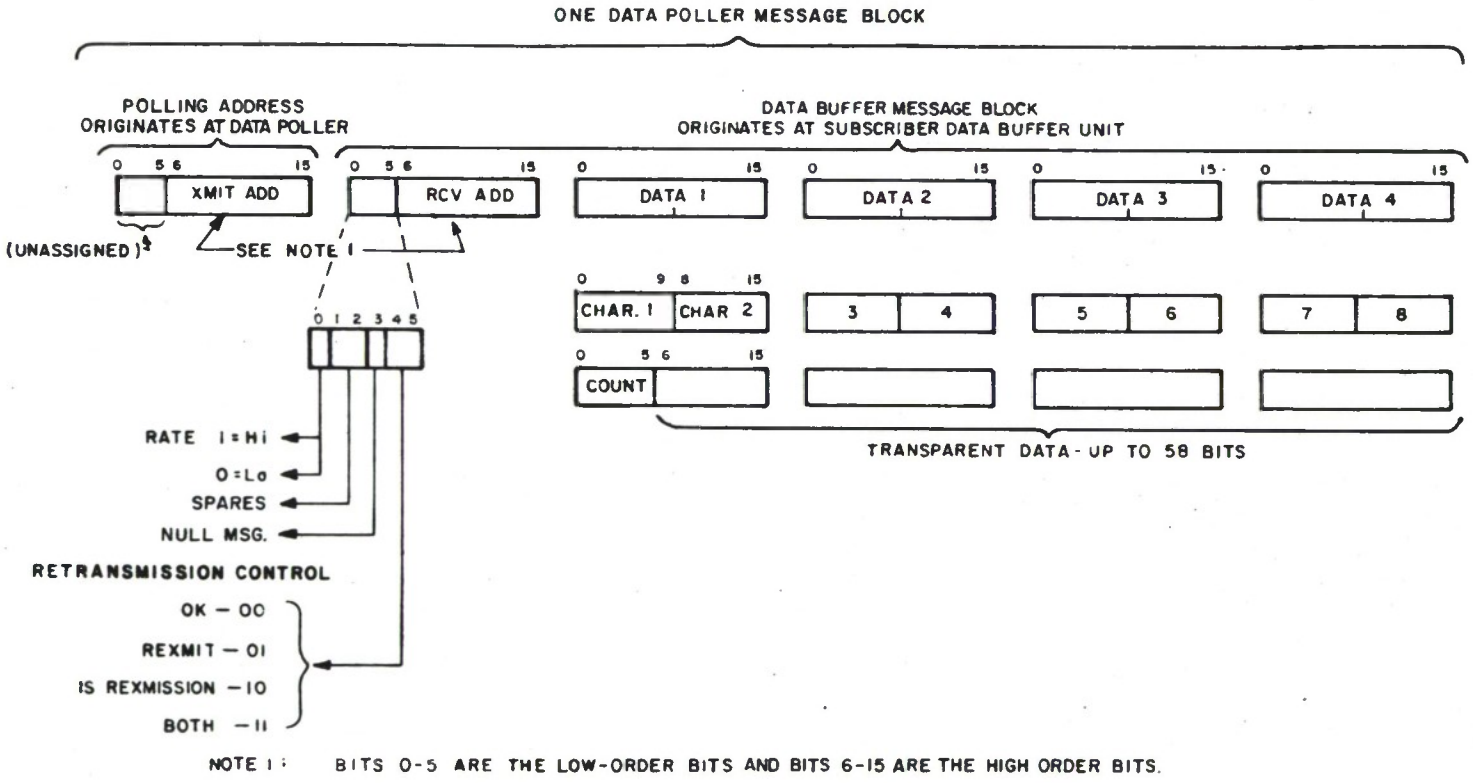


Figure B-6. Data Subsystem Message Format

B.2.3 Control Protocol

The low-order six bits (Figure B-6) of the second address word are control bits that originate at the subscriber data buffer unit. Bits 4 and 5 are for transmission control. If the receiving data buffer receives a message with a parity error, it can request a retransmission from the transmitting data buffer. This is accomplished by setting the control bits to a 01 combination in its next response to a poll. The receiving data buffer also uses this code to slow down the rate of incoming data if its buffer is temporarily full (primarily because the attached user terminal is a slow device like a mechanical printer). In this case, the receiving data buffer simply ignores the data message and continues to request retransmission of the same message until it can accept it. If no retransmission is required, the data buffer sets the control bits to a 00 code, which tells the sender he can send the next message (data packet).

When the data buffer is retransmitting a message, it sets the control bits to 10 when next polled, indicating that the data message is an exact retransmission of the previous message. This code condition is considered by the receiving buffer and confirms its previous request for retransmission. In some cases, a data buffer may want to both request a retransmission from the sending party and also retransmit its own data message to the other party

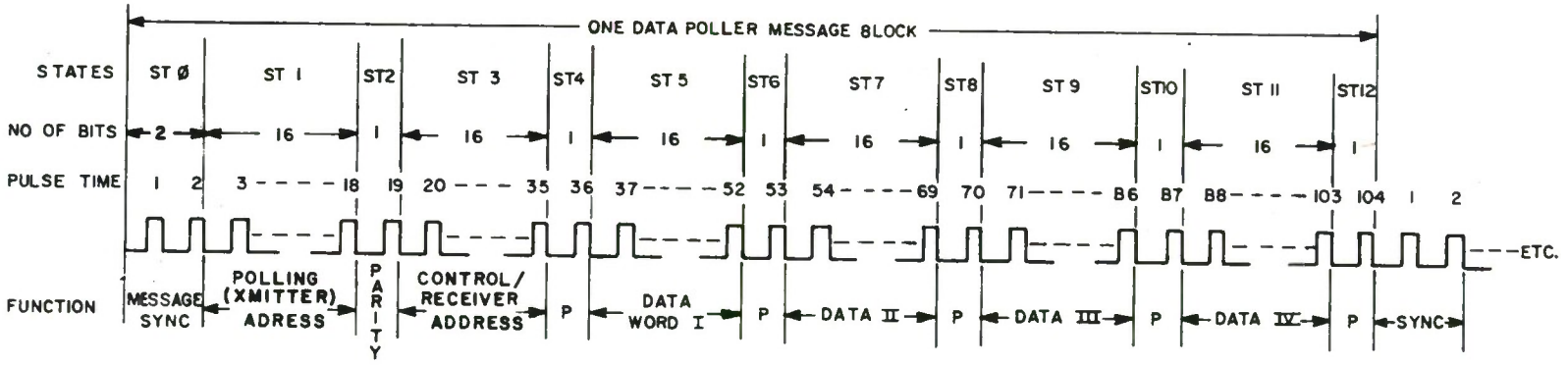
(because it had previously received a retransmission request). In this situation, it will set both control bits to 1 in its next response to a poll.

Bit 0 is used as a request for high-speed service indication. When bit 0 is set to 1, the data poller will store that terminal's address for insertion in the high-speed queue. Bits 1 and 2 of the control bits are not used. Bit 3 indicates a null message, i.e., the data words are filled with null characters. (See Subsection B.6.4). The remaining four words of the data message are used for transmitting the data information portion of the message. Since terminal transmission is usually character-oriented, each data word may contain two characters.

A second mode of transmission that is also available as a special service package corresponds to a "transparent data" operation. If a subscriber terminal device does not transmit in 8-bit character blocks, it may transmit any block length up to 58 bits. The number of valid data bits contained in the block is indicated by count bits 0-5 contained in the data word I. All 16 bit-words are followed by a simple parity bit.

Each data poller message block, therefore, contains a total of 104 bits. The bit count and pulse time corresponding to the various functions of the 104 bits is indicated in Figure B-7. The

IA – 46,335



ONE BIT DURATION = 444 NANOSECONDS

ONE BLOCK DURATION = 46.2 MICROSECONDS

STØ THROUGH ST12 ARE TIME SLOTS GENERATED BY POLLER TIMER

Figure B-7. Data Poller Message Block

states indicated by the state counter of the poller timer are also shown for each group of functional bit(s). The bit count is designated by pulse time 1 through 104. The quantity of bits assigned to a particular function appears above the pulse time in the diagram.

B.3 MIDS DATA POLLER UNIT

Figure B-8 is a block diagram that shows in simplified form the five basic parts that make up the data poller and retimer unit; its physical layout can be seen in Figure B-9. The unit's major sections are the:

a. Timer, which provides the 2.25 MHz clock signals and states 0 through 12 for transmitting the data poller message blocks. The timer logic works to produce a continuous bit stream consisting of the polling address from the high/low poller followed immediately by a repeated message from the retimer buffer.

b. High-speed/low-speed poller, which contains a high-speed address poller buffer and a low-speed address poller buffer. The polling address is the result of these two buffer outputs being alternated via control circuitry.

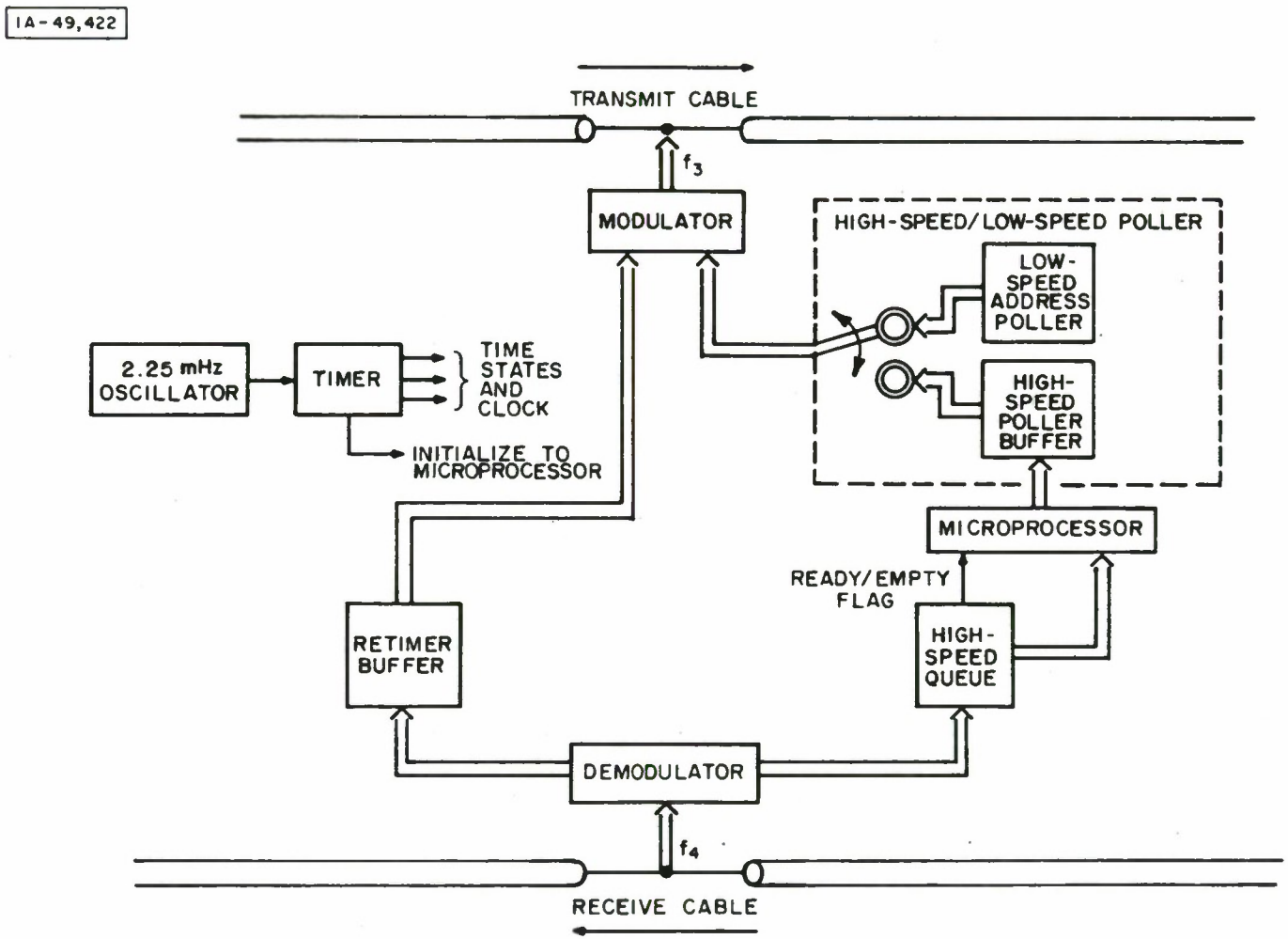


Figure B-8. MIDS Data Poller and Retimer

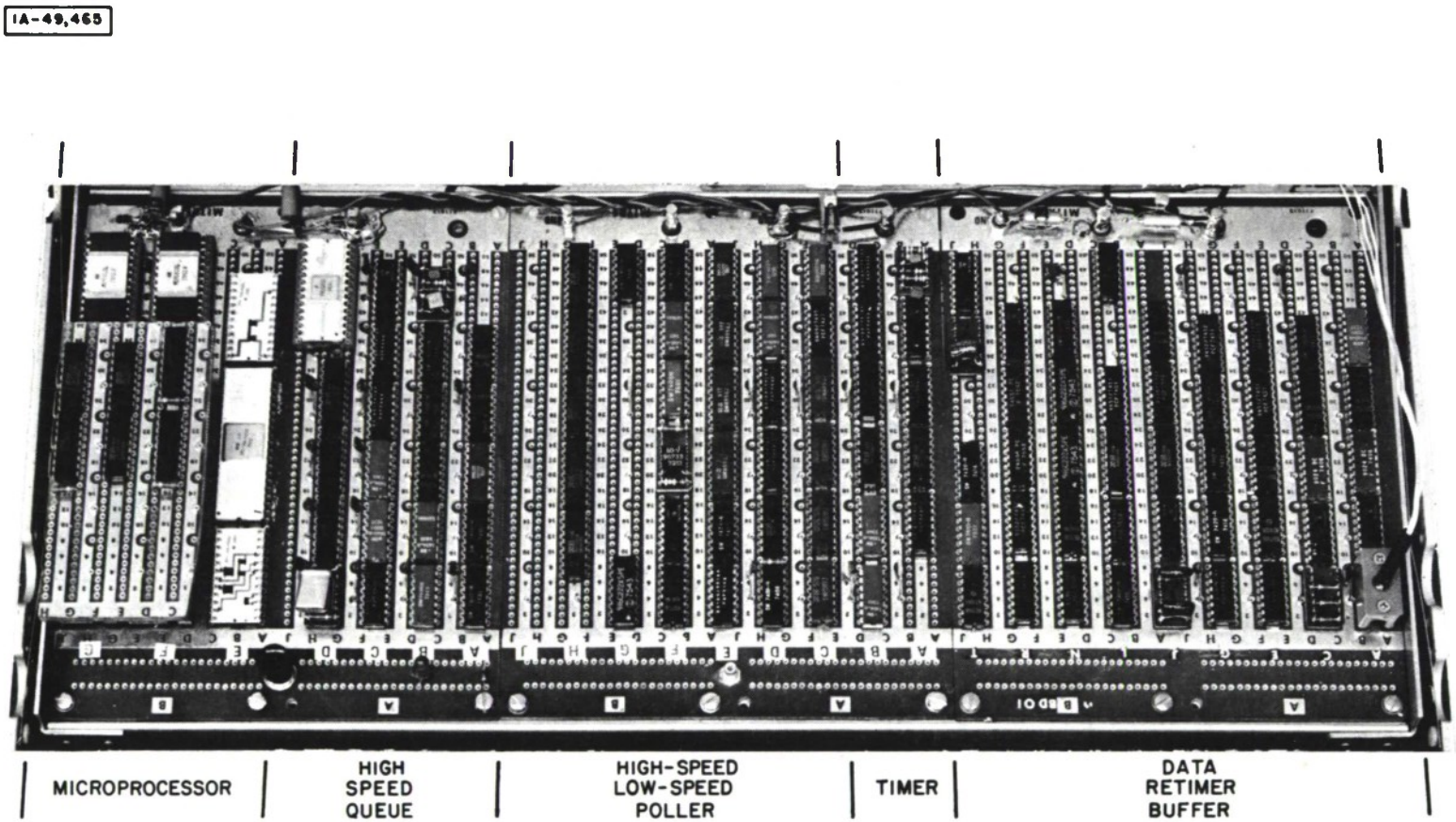


Figure B-9. Data Poller and Retimer Physical Layout

c. High-speed queue, which examines each data buffer message block received by the data poller demodulator. If the block contains a high-speed service control bit set to logic "1", the address attached to that block is stored for later insertion in the high-speed poller buffer.

d. Microprocessor, which is alerted by the high-speed queue (via the ready flag), is employed to retrieve addresses from the buffer. These addresses are stored in a high-speed address table within the microprocessor RAM memory. The microprocessor loads the 32-word high-speed address RAM into the high-speed address poller every data polling cycle.

e. Retimer buffer, which receives 87-bit data buffer message blocks from the subscriber terminals. It is the function of the retimer to temporarily store the 87-bit data buffer message blocks which are received somewhat asynchronously (due to cable delay variations) and insert them synchronously directly behind each poll word.

Together, these parts generate the polling addresses used for low- and high-speed service that are transmitted to all terminal devices via the poller transmit channel at frequency f3. The polls provide the synchronization and control necessary for transmission of digital data messages (data buffer message blocks) on the data buffer transmit channel (at frequency f4) from a large number of terminals. The data poller retimes these messages and then

retransmits them (data poller message blocks) on the data poller transmit channel.

B.3.1 Data Poller Timer

A series of 13 state pulses relating to the data poller message block is generated in the timer by moving a single bit through the state shift register. Figure B-10 shows the basic components that make up the data poller timer. Each state that is generated relates to a function in the message, as was shown in Figure B-7.

A crystal-controlled oscillator that is a support element of the processing and control element (PACE) microprocessor system produces TTL clock signals. Called the system timing element (STE), it employs an external series-resonant crystal at a frequency of 4.5 MHz. The oscillator output clocks a divide-by-two circuit, which in turn produces timing pulses that occur at one half the crystal resonant frequency. The data poller timer employs this 2.25 MHz clock as its timing reference.

The timer has a 4-bit data counter (datim) that counts clock pulses (CP) in order to time the 16-bit information portions of the six 17-bit data fields in each message. At the end of each 16-bit interval, or a count of 15, a carry-out pulse (datim) shifts the bit

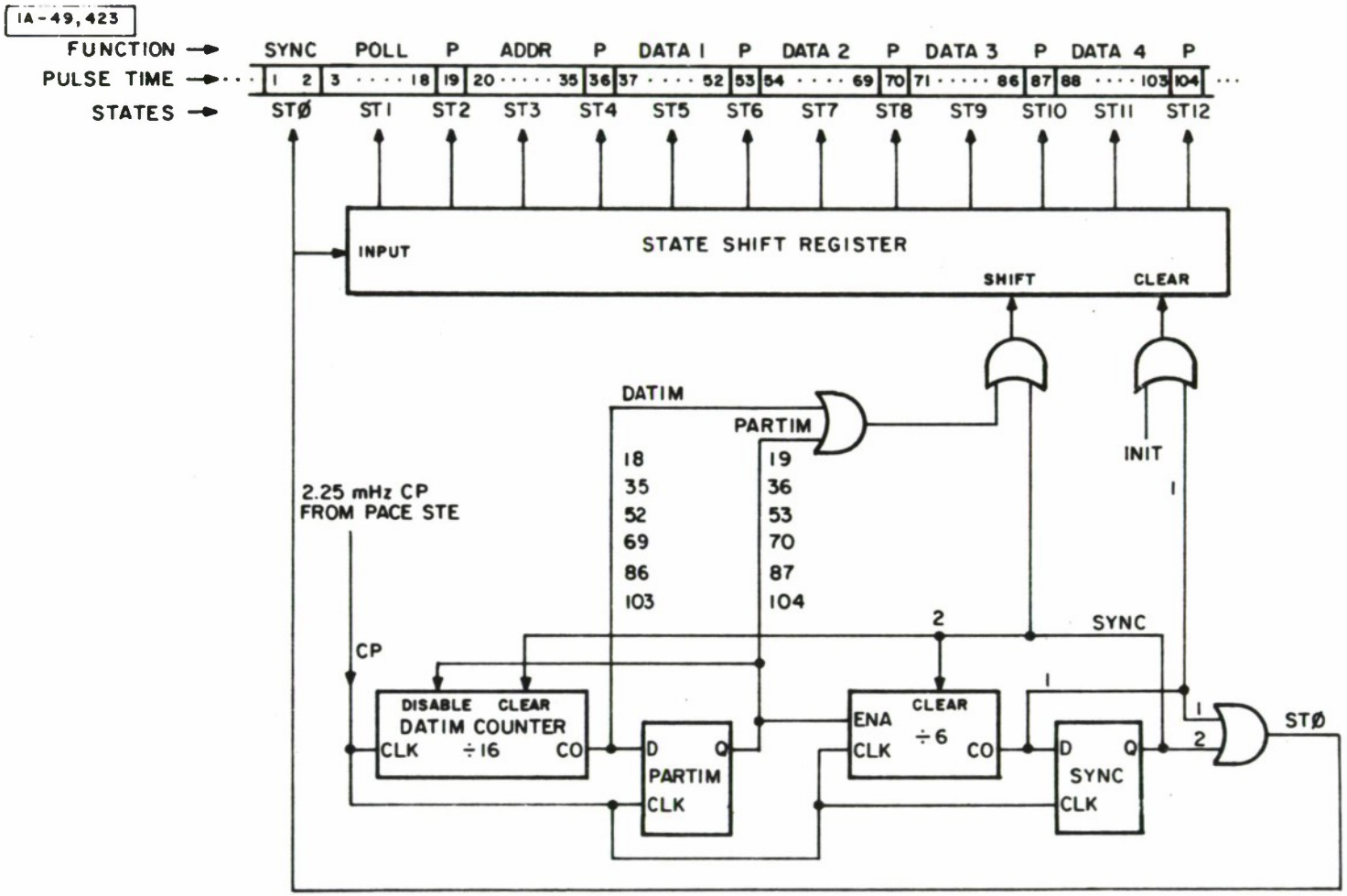


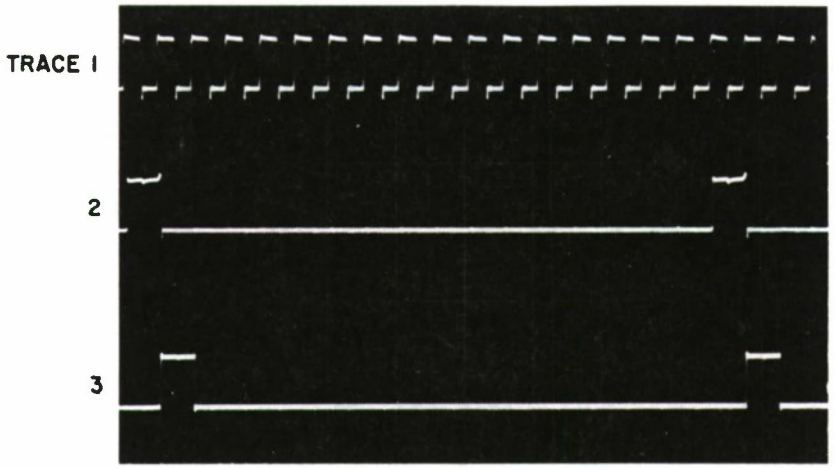
Figure B-10. Data Poller Timer Block Diagram

one stage to the right in the state shift register. The datim pulse is also applied to a parity time (partim) flip-flop. The resulting partim pulse performs a shift one bit-period later in the state shift register, which accounts for the associated parity bit. The oscilloscope display in Figure B-11 shows the clock input to the timer along with datim and partim pulses. In a complete cycle of 104 clock pulses, a datim pulse will occur during bits 18, 35, 52, 69, 86 and 103. The partim pulses will occur during bits 19, 36, 53, 70, 87, and 104. A counter which develops the sync interval (ST0) counts down starting from 6. At the count of 0, a carry-out pulse is used for combining with the output of the sync flip-flop to develop ST0. This state occurs every 102 clock pulses.

Figure B-12 shows the relationship of ST0 with datim and partim. Figure B-13 displays a typical portion of the complete data poller message block. The sync, datim or partim signals shift the state register generating the time slots for the sync data or parity time slots. The ST0 pre-sets the state shift register. The data poller timer is initilized by the microprocessor immediately after the power is applied to the system.

B.3.2 High-Speed/Low-Speed Poller

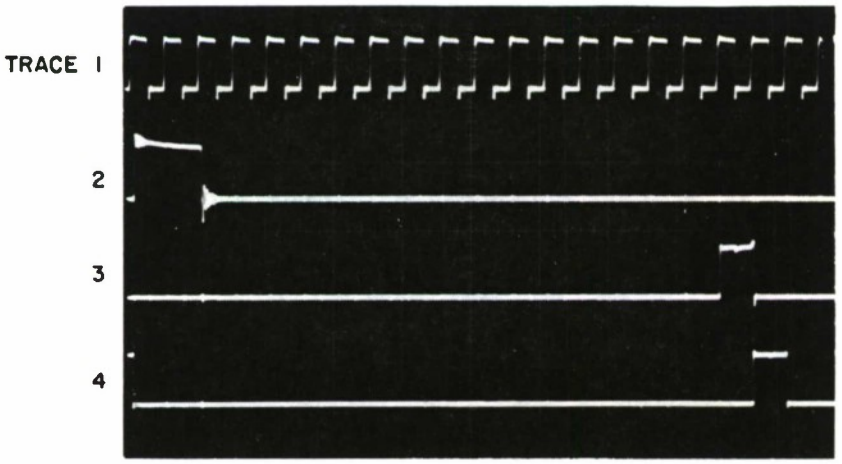
The high-speed/low-speed poller shown in Figure B-14 performs two major functions: it generates 10-bit low-speed addresses



1A-49,453

1. 2.25 mHz CLOCK INPUT FROM PACE STE
2. DATIM PULSES OCCURING DURING CLOCK TIMES 18,35,52,69,86 & 103
3. PARTIM PULSES OCCURING DURING CLOCK TIMES 19,36,53,70,87 & 104

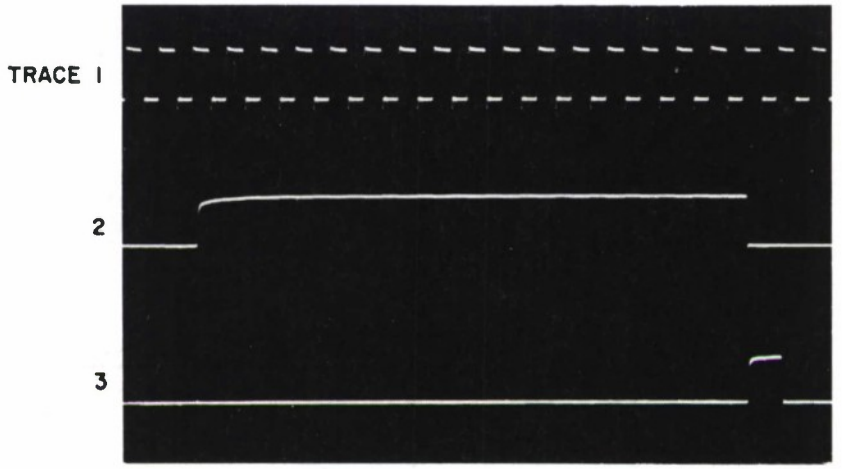
Figure B-11. Oscilloscope Display of Data Poller Timer Signals



1A-49,452

1. 2.25 mHz CLOCK
2. ST Ø PULSE (MESSAGE SYNC) OCCURING DURING CLOCK TIMES 1 & 2
3. DATIM PULSE
4. PARTIM PULSE

Figure B-12. Oscilloscope Display of Data Poller Timer Signals with Sync



1A-49,455

1. 2.25 mHz CLOCK
2. 16 BIT TIME SLOT REPRESENTING STATES 1,3,5,7,9,OR 11
3. 1 BIT TIME SLOT (PARITY SLOT) REPRESENTING STATES 2,4,6,8,10,OR 12

Figure B-13. Oscilloscope Display of Timer State Shift Register Signals

(numbering 0 to 1023) which are used to sequentially poll the subscriber terminals, and provides subscriber data buffer addresses requesting polling at a higher rate (high-speed polls). The bits generated by the poller during timer state 1 consist of six unused control bits and a 10-bit polling address. A 10-stage counter is sufficient to generate the low-speed addresses; however, an 11-stage counter is employed so that the first stage carry out (CO) may be used as a toggle for the lo/hi readout control circuit.

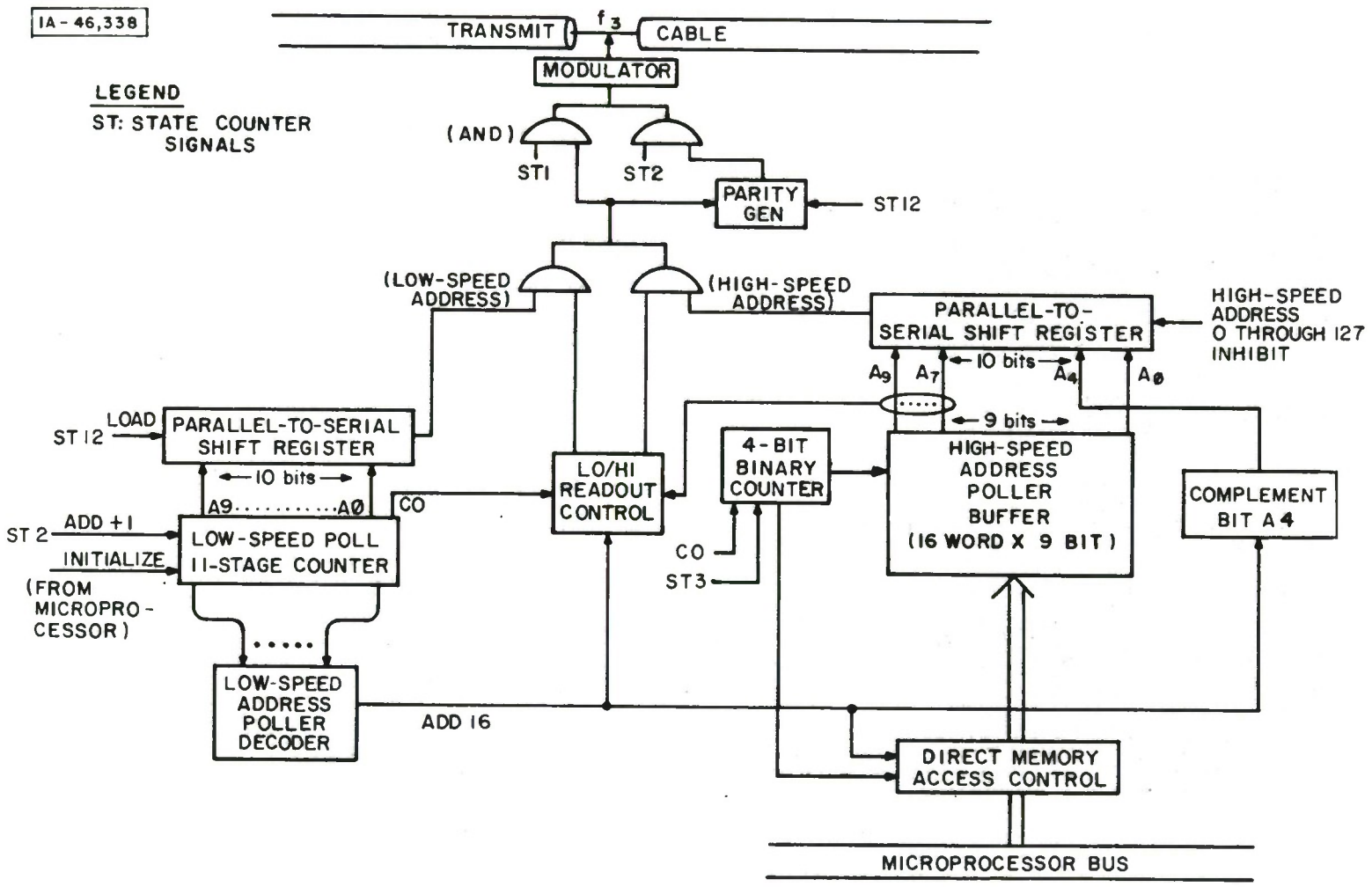


Figure B-14. Low-Speed and High-Speed Address Poller

The readout control circuit controls the alternate sending of low-speed and high-speed addresses by enabling the outputs of the low-speed address counter and the high-speed address memory. The 10-bit low-speed addresses are sequentially generated by the ten most significant bits of this 11-stage counter. These bits are transferred in a bit-parallel mode from the counter to a parallel-to-serial shift register. The shift register, which is loaded during ST12, applies the 10-bit address in a bit-serial mode through the gating circuits to the poller modulator for transmission on the data channel. This 10-bit address is gated through during ST1 and is clocked at a 2.25 MHz rate. The low-speed address counter increments the low-speed address count by one with the "ADD + 1" signal from the poller timer which occurs during ST2. The counter is reset (set to zero) by the initialize signal, which is generated by powering up or by depressing an external button to insure synchronism between the system hardware and the PACE microprocessor software.

The high-speed address poller stores 16 words in its high-speed buffer that have been received from the microprocessor via a direct memory access (DMA) control technique. Each word contains a high-speed address to be transmitted on the data channel. The high-speed polling address information is initially stored in the PACE random access memory, and the DMA output is the result of processing by the PACE microprocessor of high-speed polling requests received

from the subscriber terminals. The high-speed address poller sends a total of 32 addresses on the poller transmit channel consisting of two groups of 16 addresses. The second group of 16 addresses is offset from the first group by the numeric 16; therefore, the high-speed poller requires only a 16-word buffer.

The high-speed poller receives a logic control signal (ADD 16) from the low-speed address poller decoder indicating when to add the numeric 16 to the addresses. The poller performs this function by complementing the fifth bit (A4) in the output that is sent to the parallel-to-serial shift register. (It should be noted that the high-speed address poller buffer is organized as 16 words X 9 bits because only nine bits of each final 10-bit address is required; the poller logic inserts bit 4, which is complement bit A4 in Figure B-14.) The addressing of the poller buffer is controlled by a 4-bit binary counter that is stepped by the coincidence of a high-speed poll interval (CO control lead), a normal polling cycle and timer signal ST3. The counter indicates to the DMA control circuit that the high-speed address polling is complete. The signal, which is initiated by the detected 64th poll and ST3, is then gated with the low-speed address poller decoder control signal to set up the next DMA from the microprocessor.

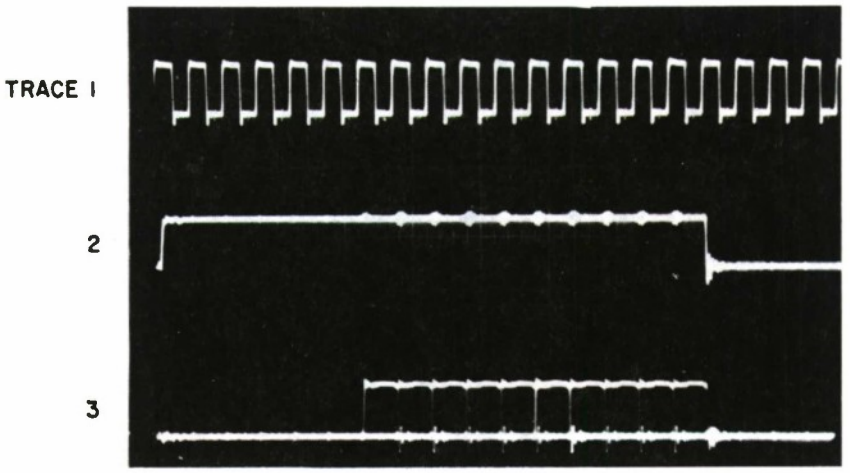
Each 16-bit poll transmission is accompanied by a 17th bit sent for parity-checking purposes. The 16 bits sent to the poller

modulator are also sent to a parity generator, and if an even number of 1's are detected in the 16 bits, the parity generator will place a 1 in the 17th bit position. If an odd number of 1's are detected, a 0 will be placed in these. The parity generator, which provides odd parity, is enabled during the ST2 1-bit interval. At ST12 time, the parity generator is "set" or conditioned for odd parity generation for the next poll.

Figure B-15(a) shows an oscilloscope display of the 10-bit polling address (Trace 3) as it is gated during ST1 (Trace 2) for transmission on the poller channel. Figure B-15(b) displays the 10-bit polling address (Trace 2) followed by parity in ST2 (Trace 4) into the poller modulator. Each bit (polling and parity) is shown in both 0 & 1 states demonstrating all possible address combinations followed by its proper parity bit. The data subsystem is designed such that high-speed addresses 0 through 127 are inhibited in transfer to the parallel-to-serial shift register. This is accomplished by using the low-speed counter (when at 0 through 127) to inhibit the shift register. These addresses are reserved for use in a multiport data buffer.

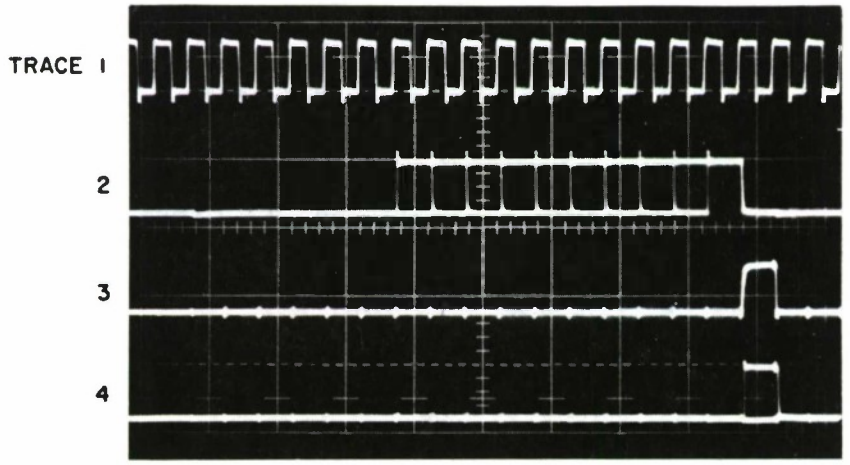
B.3.3 High-Speed Queue

The data poller high-speed queue (Figure B-16) examines the control bits and receiver address of a data buffer message block to



1. 2.25 mHz CLOCK
2. TIMER SLOT 1 (ST 1) USED FOR GATING POLLING ADDRESS
3. 10 BIT POLLING ADDRESSES

Figure B-15(a). Oscilloscope Display of Data Poller Signals



1. 2.25 mHz CLOCK
2. 10 BIT POLLING ADDRESSES
3. TIMER SLOT 2 (ST 2) USED FOR GATING PARITY BITS
4. PARITY BITS

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Figure B-15(b). Oscilloscope Display of Data Poller Signals with Parity

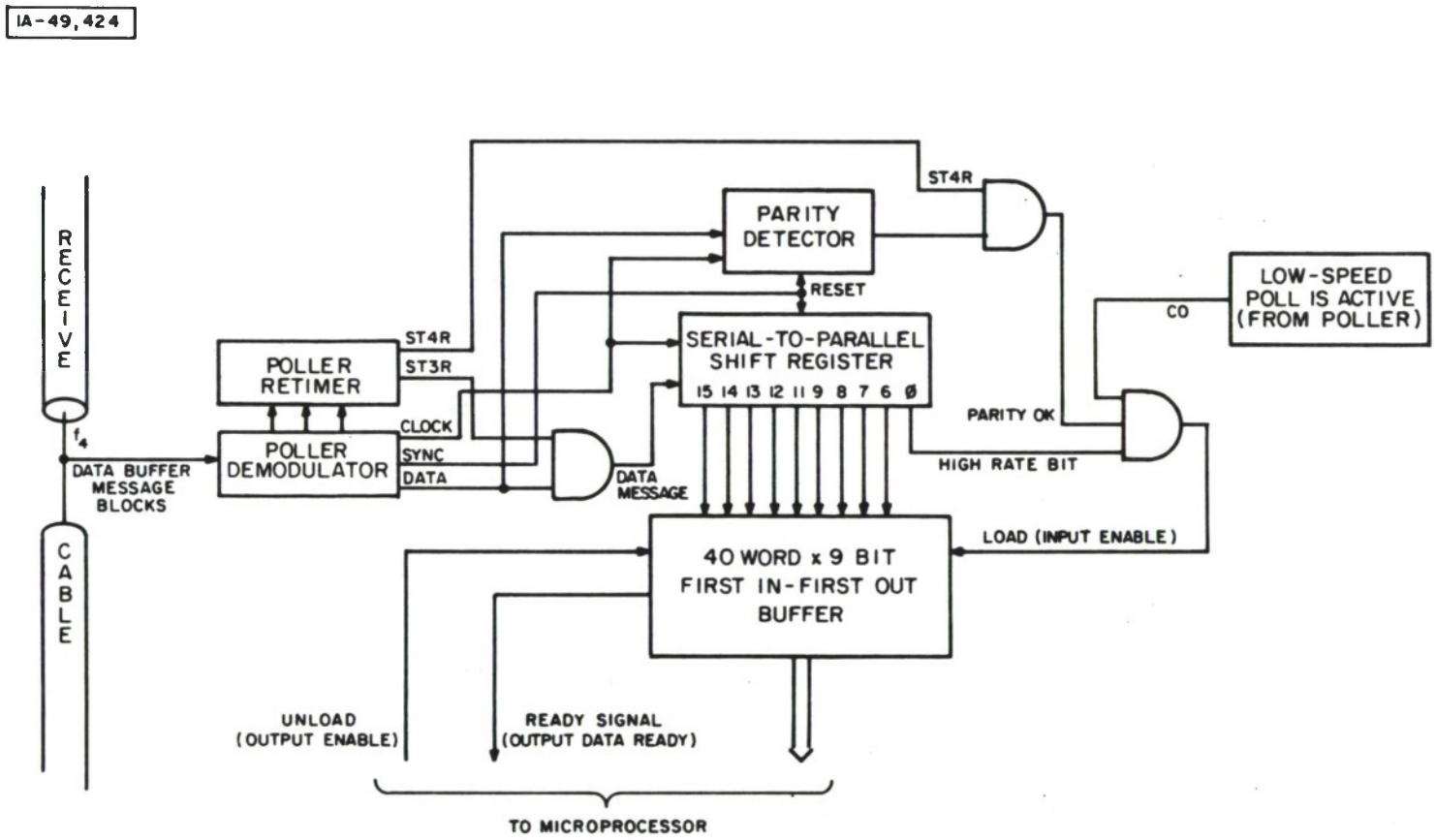

Figure B-16. Data Poller High-Speed Queue

determine if a high-speed polling request is being made by the subscriber data buffer. The high-speed queue provides the buffering required for the PACE microprocessor when high-speed requests are received. A valid high-speed request is interpreted when the first control bit (bit 0) is set to a logic 1. When a valid request is present, the logic interrupts the PACE and supplies the buffered address the control of the microprocessor.

A data buffer message block sync pulse, occurring with each message received by the data poller demodulator, is used to reset the shift register and parity detector in the high-speed queue. This is done in order to prepare for receiving the address portion of the message block (occurring during state ST3R from the the retimer) that contains the high-speed request bit along with the address of the requesting subscriber data buffer (bits 6 through 15). The recovered clock from the poller demodulator is used to shift the received data into the shift register during ST3R at the same time the parity generator is monitoring the state of the received bits. When a low-speed poll has been received, and provided the parity bit is correct and the high-speed request bit 0 is a logic 1, the nine address bits in the shift register will be transferred into the 40 word X 9 bit first-in/first-out (FIFO) buffer register. Whenever the FIFO buffer receives an address, it sends an output data ready signal to the microprocessor. The FIFO

will store addresses successively until the microprocessor has time to "unload" the addresses and process them.

B.3.4 Data Poller Microprocessor

The data poller microprocessor is employed to collect, collate, and generate a list of up to sixteen 9-bit high-speed polling addresses for the high-speed polling buffer in the high/low poller section. The software also determines which terminals are given high-speed service and for what duration. The microprocessor used is manufactured by the National Semiconductor Corporation and designated by the manufacturer as the Processing Arithmetic Control Element (PACE). The PACE operates under the control of two programs. The first is for initialization, which occurs at power-up or when the external reset button is depressed. The second program -- the principal one -- is executed every polling cycle. During the execution of this program, a list is created consisting of sixteen addresses to be polled during the high-speed address polling intervals of the following polling cycle. If no explicit high-speed address assignment is made, zero is assigned as a null value. The duplex partner addresses providing connectivity between subscriber data buffers are assigned by the S&S system and are formed by adding 16 to each address.

The PACE configuration and its associated memory and input/output elements are illustrated in Figure B-17. The microprocessor employs a 16-bit bus to provide parallel transfer of data or memory address information and contains the logic required to support the execution of the software residing in the PACE read-only memory (ROM). The system timing element (STE) produces the 2.25 MHz clock signals and provides bias voltages required by the PACE. The bidirectional transceiver elements (BTEs) are 8-bit transceivers that provide controlled voltage translation of signal levels between TTL buses and PACE MOS buses. The address latch elements (ALEs) are 8-bit units used to demultiplex and store the addressing information from the 16-bit data bus. The information stored is used to address the programmable read-only memory (PROM), RAM, or the FIFO. The PROM provides 512 16-bit words of ultraviolet-erasable memory and is used to store the programs for the PACE. The RAM storage provides a total of 128 16-bit words of static read/write memory used by the PACE. This memory includes the 16 9-bit high-speed addresses which are transferred to the high-speed poll buffer (in the data poller) during the DMA.

Flag and strobe control signals are used by the PACE to assure proper coordination and synchronization among all the PACE elements attached to the bus. The PACE input is supplied by the high-speed queue (FIFO) where the presence of requesting addresses

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LEGEND
PROM: PROGRAMMABLE READ ONLY MEMORY
RAM : RANDOM ACCESS MEMORY
DMA : DIRECT MEMORY ACCESS

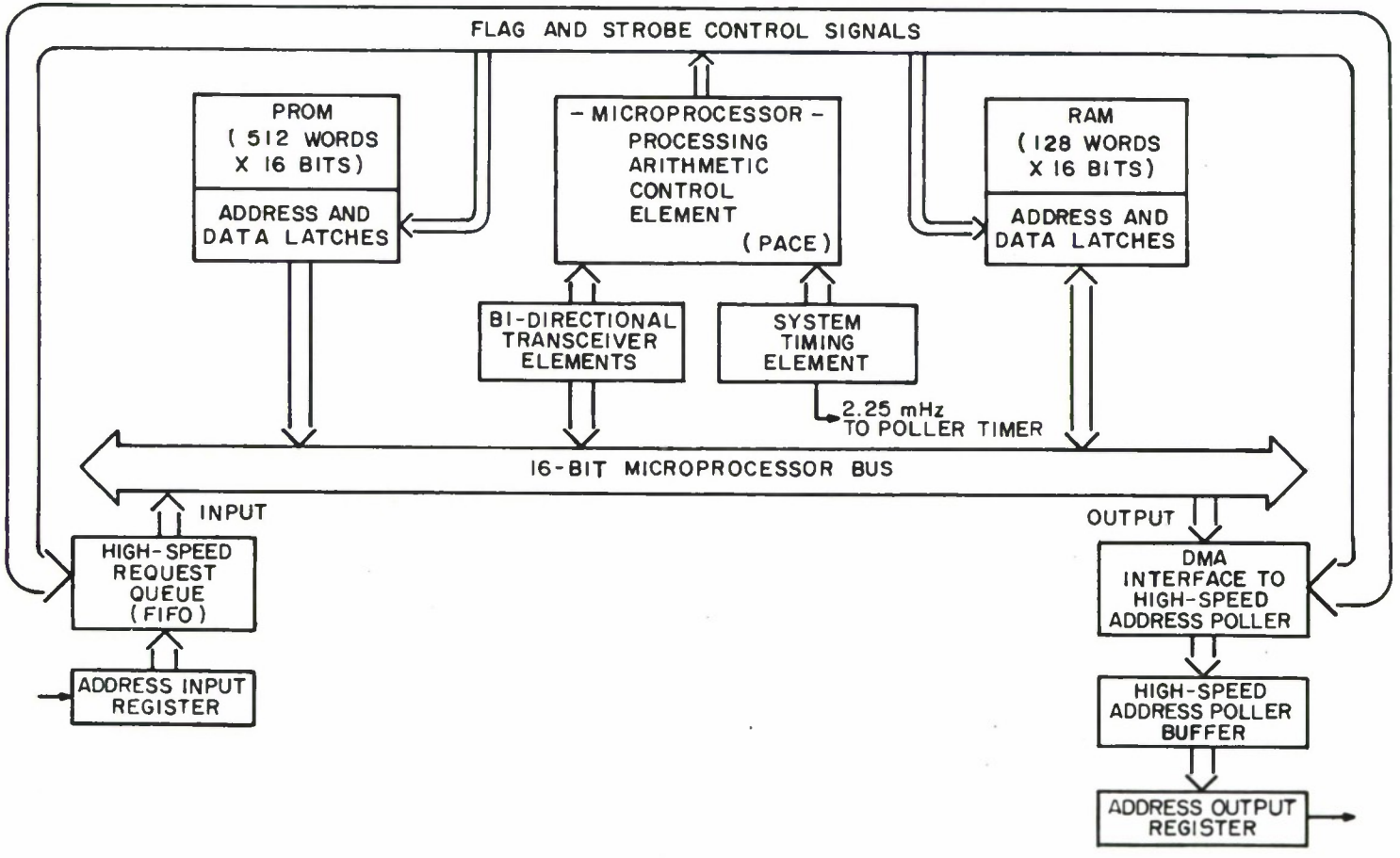


Figure B-17. Data Poller Microprocessor

are sensed by examining a ready bit (flag). The PACE microprocessor output is supplied via DMA to the high-speed poller.

B.3.5 Data Retimer Buffer

The function of the data retimer buffer is to accept demodulated data buffer message blocks from the receive cable, store them briefly, and repeat them onto the transmit cable via the poller modulator. The retimer is necessary because the arrival of data buffer message blocks is somewhat asynchronous in nature due to variations in propagation delay of the cable. The data buffer message blocks are repeated in such a manner that they are synchronously and contiguously interleaved with data poller high-speed/low-speed addresses when being retransmitted from the poller modulator.

Figure B-18 shows a simple block diagram of the retimer buffer. Demodulated data enters one of the four 85-bit shift registers (SR0 through SR3) and is stored in one of these four registers that make up a rotating buffer arrangement. The rotating storage arrangement can be thought of as a 4-barrel Gattling gun; messages are rather asynchronously loaded on a rotational basis into each buffer. The buffers are also discharged on a rotational basis but with precise timing, and exactly and contiguously following the insertion of the polling addresses. Messages are stored in this

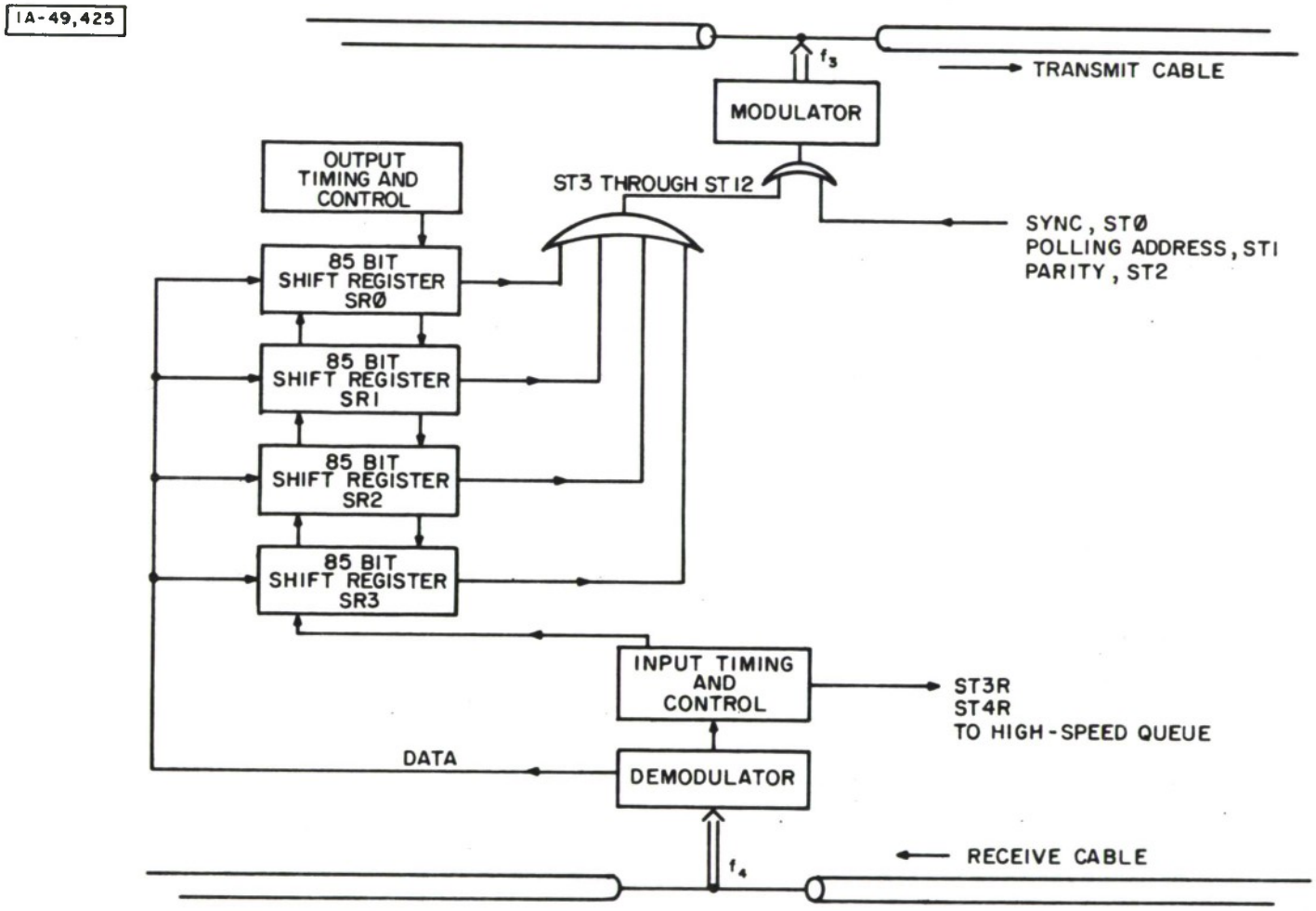


Figure B-18. Data Retimer Buffer

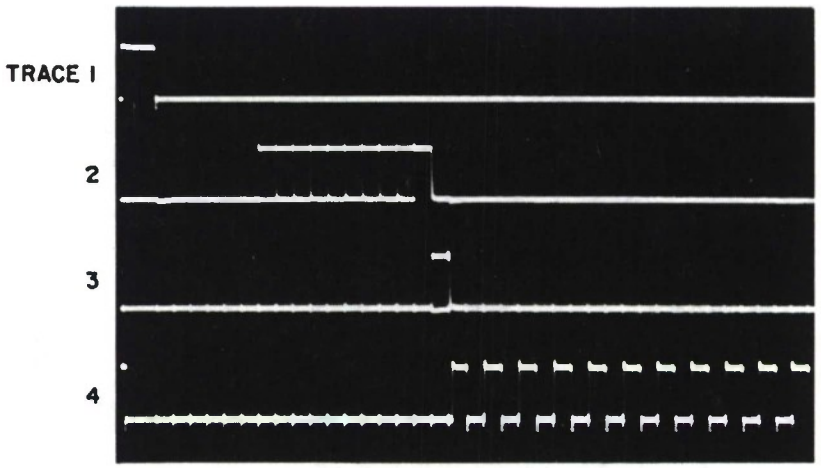
rotating buffer for approximately two message cycles, while SR2 is being loaded, SR0 is being discharged, etc.

The 85-bit shift register outputs (occurring during ST3 through ST12) are combined with the message sync (ST0), polling address (ST1), and parity (ST2) and then fed to the poller modulator for transmission of a 104-bit data poller message block. Figure B-19 shows these signals which are interleaved in their proper time slots to form the message block.

The received input timing and control signals of the retimer buffer are used to provide a ST3R and ST4R (received states) for the high-speed queue. These slots are used by the queue for extracting control signals from the address portion of the data buffer message block.

B.3.6 Microprocessor Software For The Data Poller

The microprocessor in the data poller is used to manage the high-speed address poller. The software determines which terminals are given high-speed service and how long they receive it before they are dropped back to low-speed service. As mentioned in Subsection B.3.4, the microprocessor contains two programs. The first is for initialization and is run when the data poller is first powered up. The initialization program clears software tables and



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1. MESSAGE SYNC (ST Ø)
2. POLLING ADDRESS (ST 1)
3. PARITY BIT (ST 2)
4. CONTROL/ADDRESS AND MESSAGE (ST 3···· ST 12) FROM RETIMER BUFFER

Figure B-19. Oscilloscope Display of MIDS Data Poller & Retimer Output Signals

signals the hardware to begin polling. The second program is the principal operating program and is flow-charted in Figure B-20. It is executed every 64 address polls (called a polling cycle) and creates a list of 16 addresses to be polled during the high-speed address polling time slots of the following polling cycle. The hardware will interleave these 16 addresses with 16 low-speed address polls. If no explicit address assignment is made to any of the 16 polling slots, zero is assigned as a default value. The hardware will then use the same table of addresses to poll the duplex partners of these addresses interleaved with the next 16 low-speed address polls.

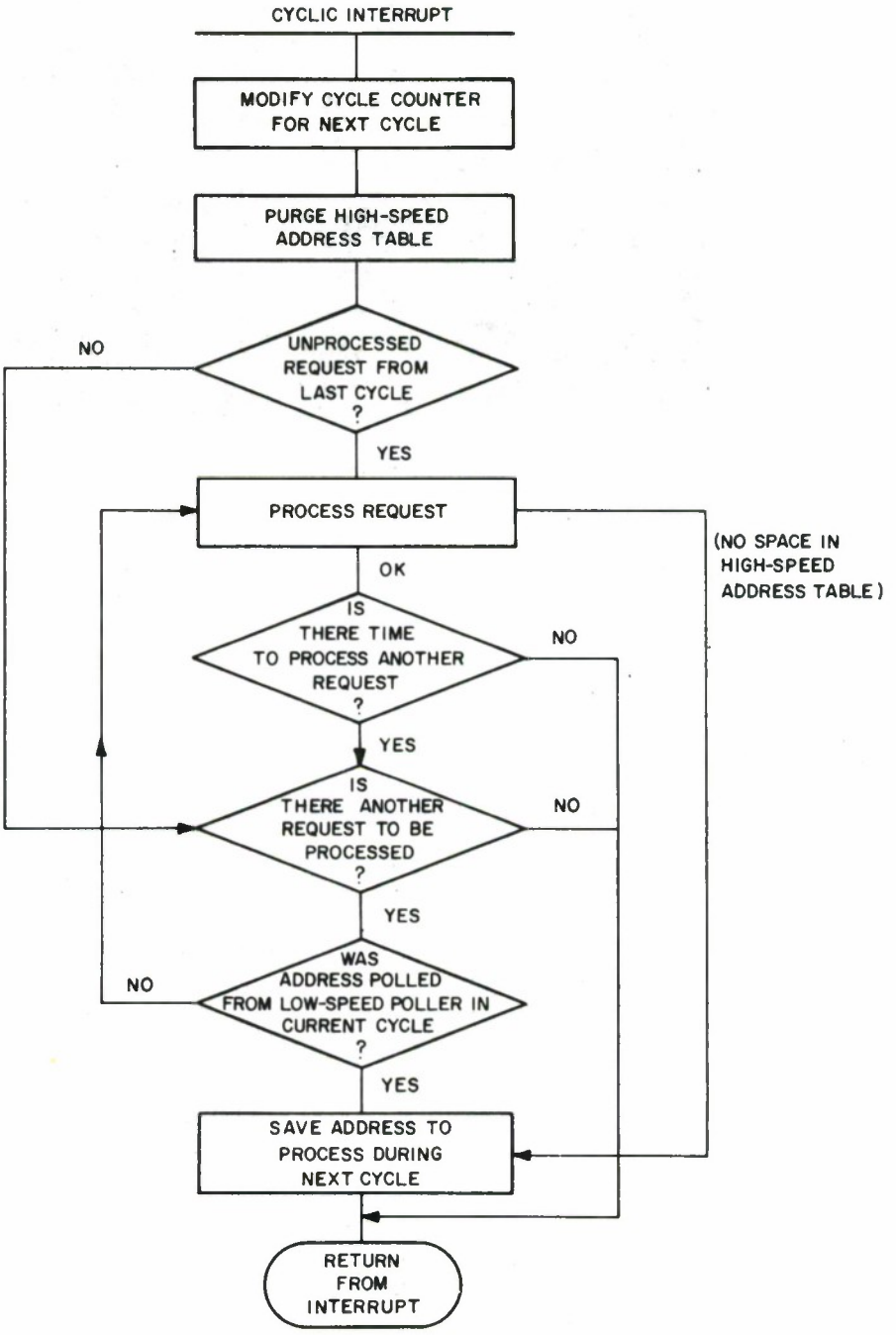


Figure B-20. Microprocessor Software for Data Channel Controller

The duplex partner addresses are formed by adding 16 to each of the table addresses. During the polling, this table is contained in the poller's high-speed address buffer. During each polling cycle, the software is preparing a new table within the microprocessor for the next polling cycle. The polling cycles are illustrated in Figure B-21. The polling sequence indicated in the diagram corresponds to the same polling sequence contained in Figures B-4(a) and B-4(b). The software timing that occurs during successive polling cycles is summarized in Figure B-22. The interaction between the software and hardware during each polling cycle is described in detail in the following paragraphs.

The only output of the microprocessor is the 16-word high-speed address polling table. This table is transferred to the hardware buffer at the very end of each cycle, without any action by the program, using the DMA hardware interface.

Requests for high-speed service are inputted to the microprocessor from the high-speed service queue (the FIFO), which is accessed one word at a time by the microprocessor. The FIFO sets a flag to indicate that the queue contains at least one address. When an address is removed from the queue for processing by the software, either the next address enters the microprocessor or the flag is reset, showing that the queue is empty. The software processes a request by putting the address in an empty word of the

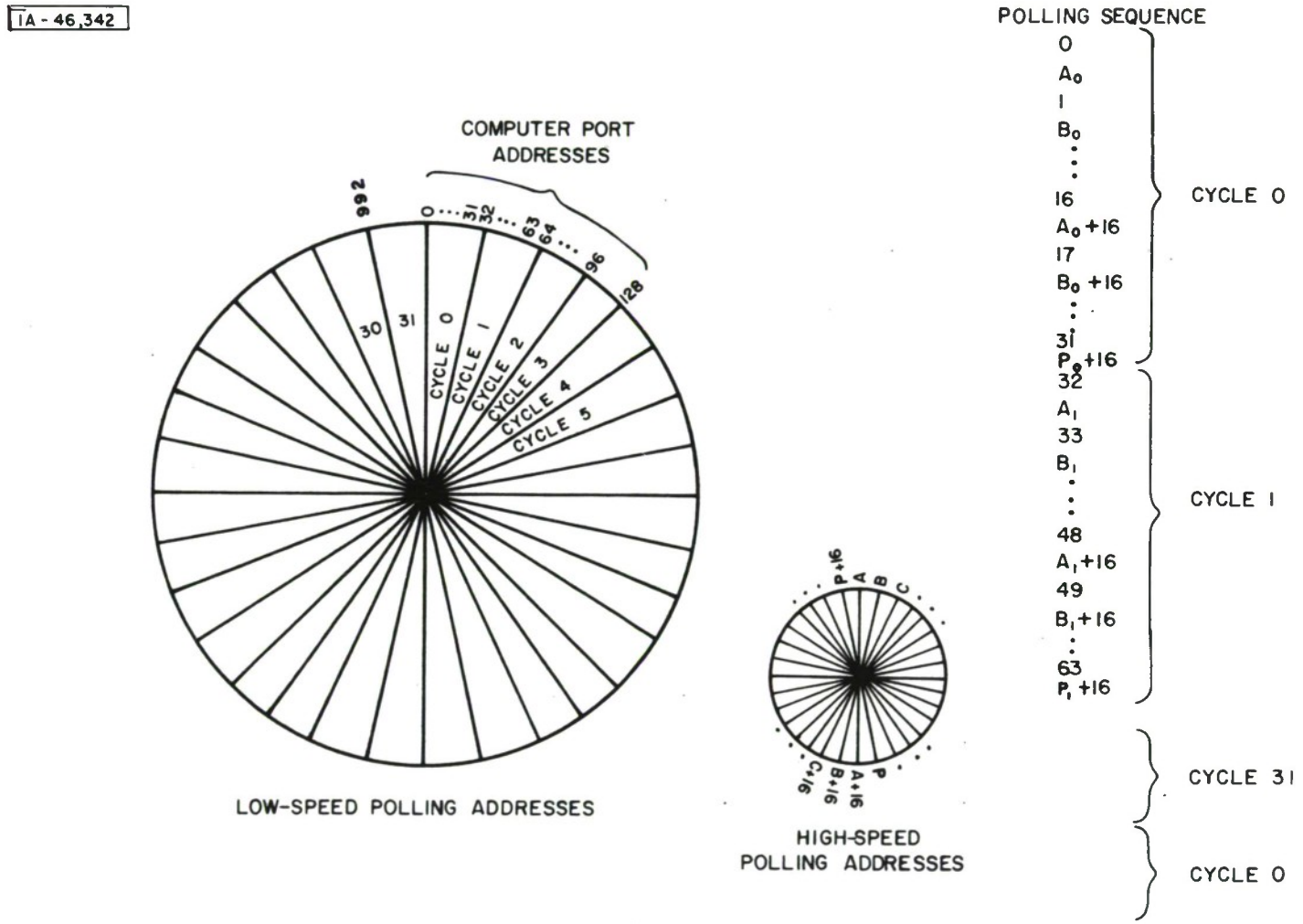


Figure B-21. Low-Speed and High-Speed Polling Sequences

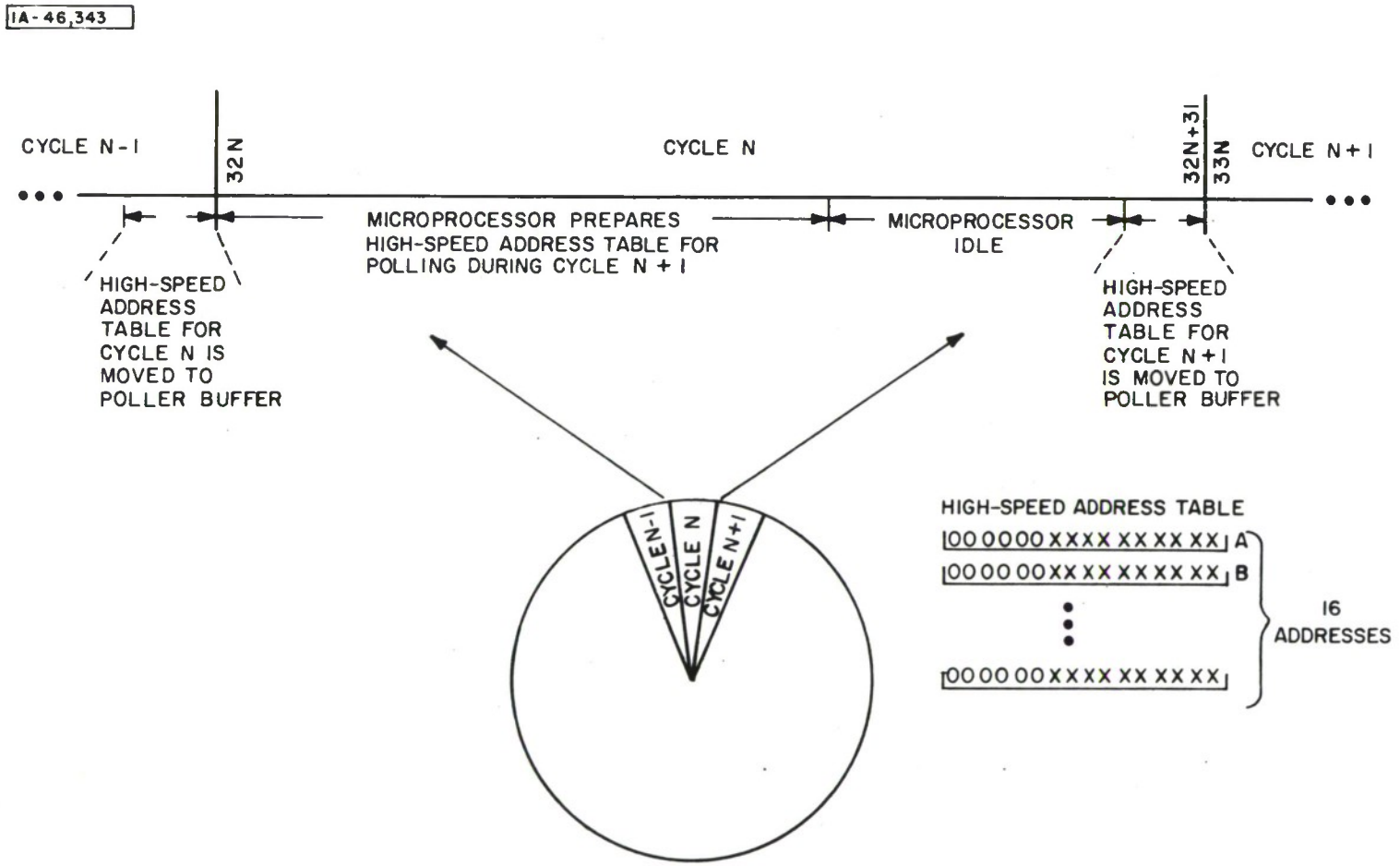


Figure B-22. Software Timing

16-word polling table. The address will stay in the table for approximately 29 cycles and will then be removed from the table by the software. The address and its duplex partner receive high-speed polling service as long as the address is in the table. After the address is removed, the service drops back to low-speed. A new speed-up request must be made by the subscriber data buffer unit to get high-speed service again.

Requests for high-speed polling are processed in the order they are received from the high-speed address request queue. If there is no space in the high-speed address table during one cycle, the address is saved for processing during the next cycle. The address will eventually be stored in the high-speed address table. Since the amount of processing time during each cycle is limited, the software is designed to process a fixed number of high-speed requests in order to be sure processing is complete before the high-speed address table is turned over to the hardware buffer (via DMA) for polling. Unprocessed requests are left in the request queue for the next cycle.

Each address is polled from the hardware's low-speed address poller once for every data frame, whether or not the address is in the high-speed address poller or an indirect address has been assigned to a terminal. There are 32 high-speed polling cycles during each data frame. Because indirect address assignments of

terminals conversing with each other are made to be modulo 16, the address and its duplex partner are polled from the low-speed address poller during the same cycle.

The software is designed so that an address will not be polled from the high-speed address poller during the cycles immediately preceding or following its low-speed address poller cycle. This is done to assure that there will be time for a response between the polling of an address and its partner. The cycle during which an address is polled from the low-speed address poller can be determined from the five high-order bits of the address. A cycle counter is maintained in the program to synchronize the software with the hardware that creates the low-speed address polls. By comparing an address with the cycle counter, the software determines when the address can be assigned to the high-speed address poller and when it should be taken off.

Whenever a subscriber data buffer unit is polled, it can request high-speed service. The subscriber data buffer unit does not differentiate between low-speed service polls and high-speed service polls; however, the request for high-speed service is recognized by the poller hardware only if it comes as a response to a low-speed service poll. Requests, therefore, are processed by the software within two or three cycles of the low-speed poll. If the request appears too soon, during the same cycle as the low-speed

poll, the processing is held up until the next cycle to assure that there is one cycle without polling before the address is put in the high-speed address poller. Addresses are removed from the high-speed poller by a purge of the address table at the beginning of each cycle of addresses within a certain range, which is a function of the cycle count.

B.4 FUNCTIONAL DESCRIPTION OF MIDS SUBSCRIBER DATA BUFFER

Every data subscriber in the MIDS has a subscriber data buffer unit (SDB or data buffer) between the data terminal and the cable. The SDB is designed for use with standard RS-232 compatible signals so that it can support several different types of terminals.

The primary function of the data buffer is to collect data from the terminal, reformat it, and send it out over the transmit cable, and to collect data from the receive cable and send it to the terminal. The secondary function is to control the flow of data so the terminal can operate at maximum speed with a minimum burden on the system. The data buffer also checks parity on incoming data and corrects errors either by requesting retransmission or responding to a retransmission request from another data buffer.

B.4.1 Data Transfer Through The SDB

Data moves from the terminal to the data buffer in a serial bit stream composed of a start bit, eight data bits, and one or two stop bits. The SDB terminal interface hardware receives the bit stream, strips the start and stop bits, and stores the remaining bits in an 8-bit character register. The character is then moved to a random access memory storage area of the data buffer, where it remains until it can be transmitted to the cable. There is also an 8-bit character register for data being sent from the SDB to the terminal. When the terminal signals that it is ready to accept data, one character is moved from random access memory to the character register; from there, the character is transmitted serially to the terminal.

Data moves between the SDB and the cable in 5-word messages, called data buffer message blocks, which contain an address for the intended receiver, some control information and up to eight (8-bit) characters of data. (See Figure B-6.) The timing of the message transmission is controlled by polls received from the data poller that are interspaced with other data buffer message blocks.

B.4.2 Communication Modes

Communication between DBs is primarily full-duplex. For every transmitting data buffer there is a receiving data buffer that, in turn, replies to each message. Data flow may be in either direction or both directions simultaneously. The one exception to the duplex service is receive-only simplex, where an SDB is listening to one side of a duplex conversation. The receive-only simplex mode allows a transmitting terminal to broadcast data to an unlimited number of other terminals.

During the entire time that two SDBs are connected to each other, they are polled alternately at frequent intervals by the data poller. On receipt of a poll, the SDB transmits a message containing from zero to eight characters of data. The message is received by the other SDB in time for the second SDB to prepare a reply before it is polled. The reply is in the same format as the message received. The two terminals send messages back and forth until they are disconnected. The time interval of the polls varies, but the alternation is strictly adhered to and there is always at least a 1.48 ms interval between polls to an SDB and his connectee. (This minimum time interval is equal to 32-2 or 30 polls.)

B.5 MIDS SUBSCRIBER DATA BUFFER HARDWARE

The subscriber data buffer hardware is the interface between a subscriber's terminal device and the digital data channel of the MIDS transmit and receive cables. The SDB hardware must interact with the S&S system in that it must accept and acknowledge the indirect addresses assigned to it by the S&S system. In order to properly interface with the system, an SDB must monitor all polling addresses from the data poller and transmit a data message to its duplex partner immediately after receiving the polling address that matches the indirect transmitter address assigned to it by the S&S system. Also, the SDB must monitor all receiver addresses in the data buffer message block and accept the data following the receive address that matches its own indirect receiver address. Additionally, the SDB must verify the parity on incoming data, in order to later recover if errors are present, and must generate the correct parity for outgoing data. Finally, on the cable side of the interface, the SDB must provide a means of delaying its output so that cable propagation delays may be accounted for.

On the terminal side of the interface, the SDB must convert data from the terminal into the MIDS data buffer message block format (as was shown in Figure B-6) and vice versa. The final function required of the SDB is that it be quickly adaptable to any RS-232 compatible terminal that a subscriber may desire to use.

B.5.1 Hardware Considerations

The SDB hardware consists of a modulator, demodulator, and integrated circits mounted on a wire wrap panel. This hardware is mounted, along with an S&S subscriber unit, a triple power supply, and the necessary control switches, in a 3 1/2 inch chassis. The logic devices and component holders are wired to create the various circuits named on the MIDS subscriber data buffer block diagram. How these circuits contribute to the fulfillment of the requirements of the SDB will be explained in the functional circuit descriptions that follow; reference to Figure B-23 will clarify the written descriptions. Figure B-24 shows a photograph of the circuit board and identifies the functional blocks.

B.5.2 Squaring Circuit

The squaring circuit insures proper alignment of the clock, sync, and data signals from the demodulator. The sync and data signals from the demodulator have rise times of approximately 50 ns; the clock has a fall time of approximately 100 ns and an amplitude of only two volts, peak to peak. The squaring circuit provides, besides alignment, equal amplitudes at TTL levels and rise and fall times of less than 25 ns, as shown in Figure B-25.

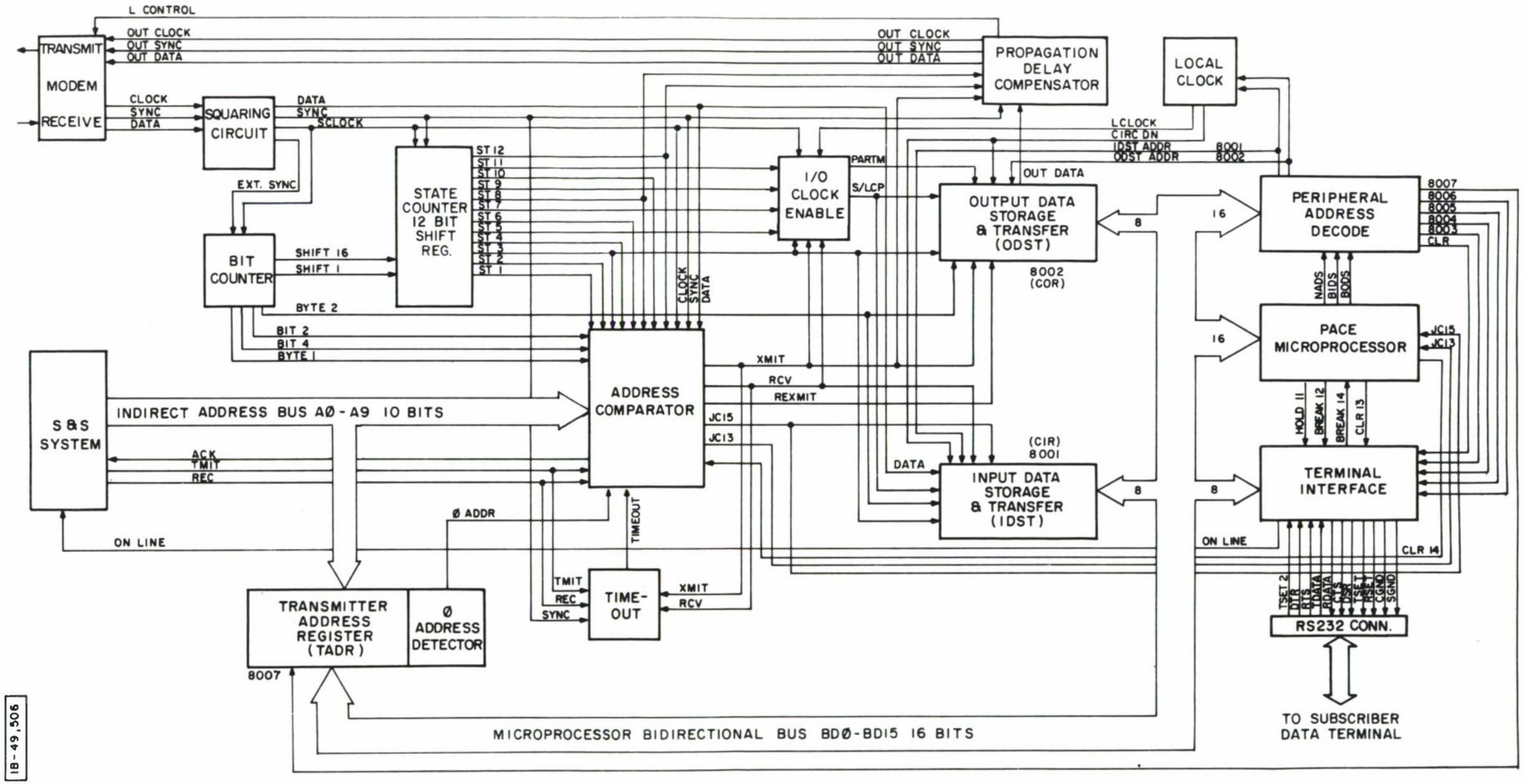


Figure B-23. MIDS Subscriber Data Buffer Unit Block Diagram

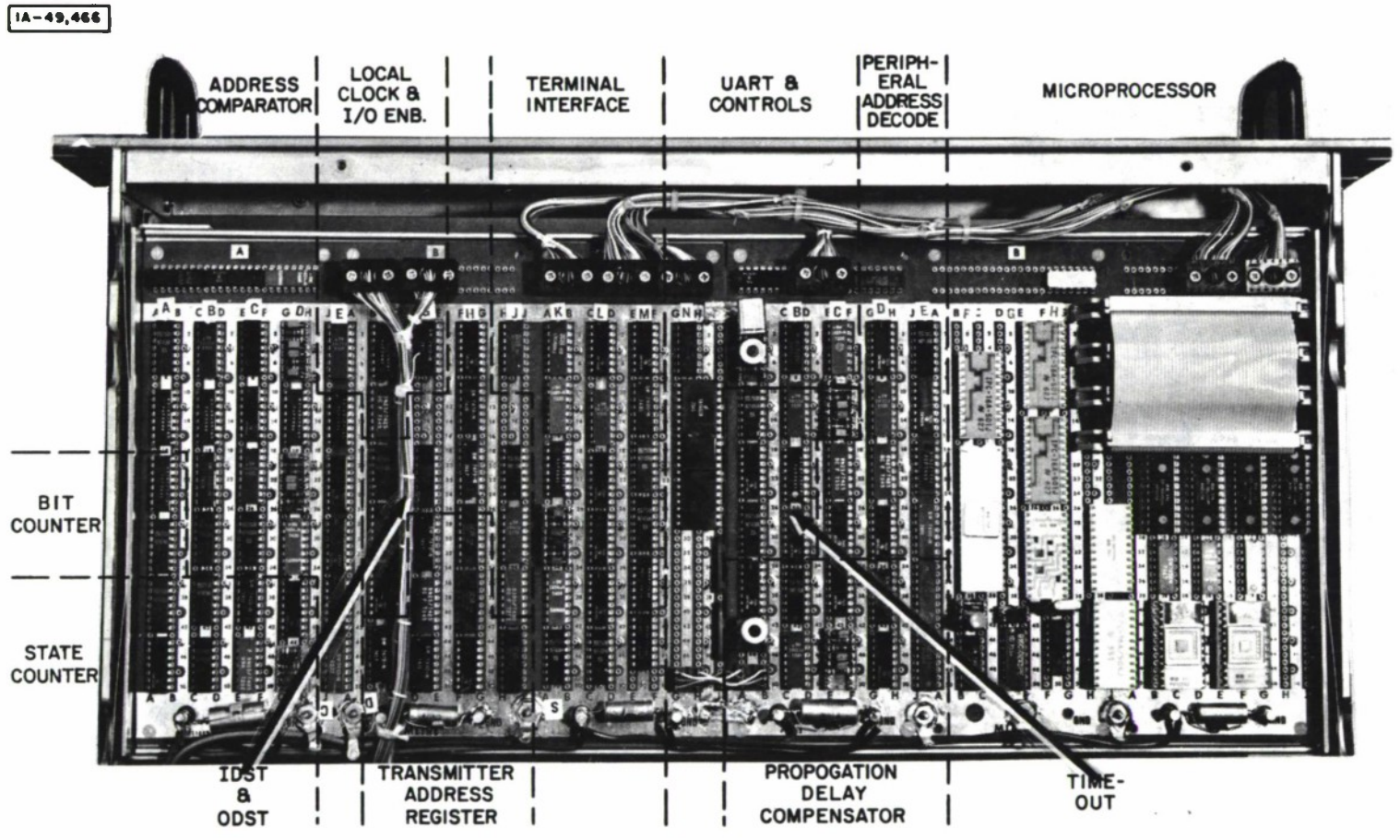
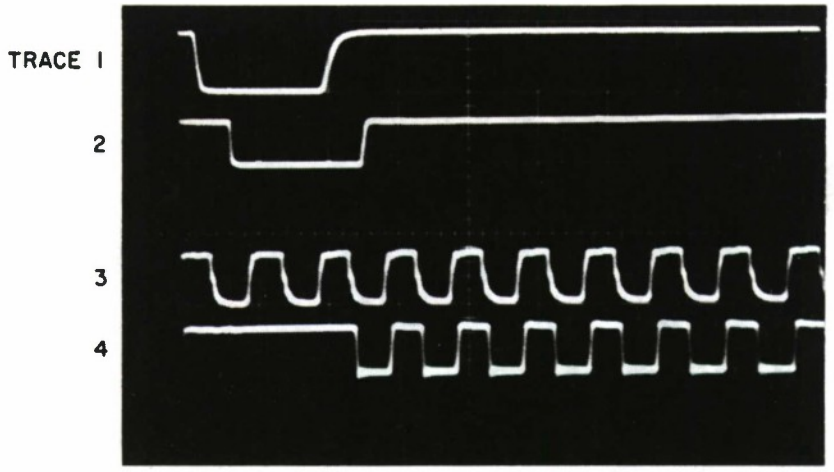


Figure B-24. MIDS Subscriber Data Buffer



SWEEP RATE, 0.5 μs/cm; AMPLITUDE 5 v/cm

1. SYNC PULSE FROM DEMODULATOR
2. SYNC PULSE AFTER SQUARING CIRCUIT
3. CLOCK PULSE FROM DEMODULATOR (AFTER VOLTAGE INCREASE)
4. CLOCK PULSE AFTER SQUARING CIRCUIT (WITH PULSE DURING SYNC REMOVED)

IA-49,451

Figure B-25. Squaring Circuit Input/Output Waveforms

Secondary functions of the squaring circuit are: providing adjustment of both edges of the sync pulse, removing clock pulses during the sync pulse, and generating an extended sync pulse that is one half clock period longer than the sync pulse from the demodulator, which is used to reset the bit counter.

B.5.3 Bit Counter and State Counter

The bit counter, after being reset by the extended sync pulse, counts clock periods. Combined with other logic elements, the bit counter shifts the state counter (a 12-bit parallel output

shift register) after counting 16 periods or one period, as is appropriate, to create state timing pulses.

The state timing pulses are called states 1 through 12 and are identical to the timing pulses used by the data poller to output information as was shown in Figure B-7. State 1 immediately follows the sync pulse, has a 16-period duration and is the time when a polling address should be on the serial bit stream from the data poller. State 2 is one period long and is the time slot for the polling address parity bit. States 3 & 4 are the receiver addresses and parity time slots. States 5, 7, 9 & 11 are the data word time slots. States 6, 8, 10 & 12 are the corresponding parity bit time slots. Figure B-26 shows the waveforms corresponding to all states. It should be noted here that detection of an incorrect parity bit on either address resets the state counter and therefore stops all activity until another sync pulse (data poller message block) is received.

B.5.4 Address Comparators and Transmitter Address Register

As stated earlier, the SDB receives an indirect transmitter address and receiver address from the S&S system as part of the call setup procedures. The SDB acknowledges receipt of each indirect address on the "ACK" line and forces the PACE microprocessor initialization after receiving the transmitter indirect address.

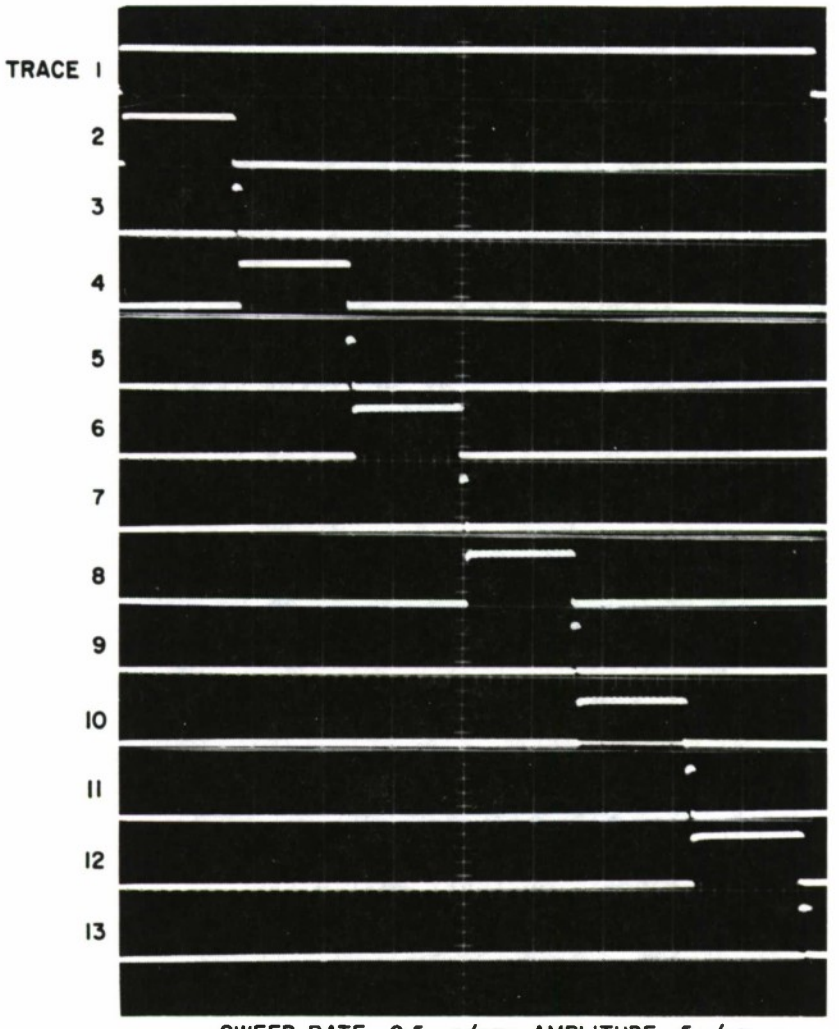


Figure B-26. State Counter Timing Waveforms

The indirect transmitter address, which according to system protocol is also the indirect receiver address of the duplex partner of a given call, is stored at the transmitter address register (TADR), where it can be read by the microprocessor. If the SDB is a receiver of a simplex connectivity, its indirect transmitter address will be a zero and will be decoded as such by the zero address detector circuit.

The SDB stores both indirect addresses, in separate recirculating shift registers within the address comparator (i.e. two, 16-bit, parallel in, serial in/out shift registers with their respective serial inputs and outputs connected). During state 1 the appropriate recirculating register is clocked and its contents are compared "on the fly" with the serial bit stream from the data poller. If the polling address matches the SDB's indirect transmitter address stored in the TADR, and the parity bit is correct, a signal called "XMIT" is set to a logic 1 for the remainder of that data poller message block, allowing a message to be transmitted from the output data storage hardware. This XMIT signal would be inhibited by the zero address detector if a transmitter address of zero (indicating a simplex connection) has been assigned by the S&S system.

During state 3, the other rotary shift register in the address comparator is clocked; if a match is found and the parity

bit is correct, a signal called RCV is set to a logic 1 for the rest of that data poller message block, allowing the input data storage hardware to gather and store the four relevant data words.

The SDB also stores the sixth header bit, which is the retransmit bit, of the receiver addresses from the poller. If the RCV signal goes high and the stored sixth bit is high, then a signal called "REXMIT" is set true, which indicates to the hardware that a request for retransmission has been received and the last message transmitted must be transmitted again when the next XMIT goes true.

B.5.5 Timeout Circuit

When either XMIT or RCV goes active, a timeout signal that is 28 data poller message blocks long, is initiated. The timeout disables the address comparators and guarantees that the microprocessor will have ample time to process either input or output data. The receipt of an indirect transmitter address from the S&S system also initiates a timeout in order to allow the microprocessor time to execute the initialize routine. Finally, the timeout circuit disables the parity checking circuit, thereby insuring that the state counter will free run and provide timing pulses throughout the timeout. This action is necessary because more than one data poller message block is required to transmit a message (as will be explained in Subsection B.5.10).

B.5.6 Output Data Storage and Transfer Buffer

Prior to the first transmission, the microprocessor outputs a dummy message to the cable output register (COR), which is internal to the output data storage and transfer (ODST) buffer. The COR register is comprised of both an 8-bit, parallel in, serial out shift register called the output transfer register and an 80-bit, serial in/out shift register called the output storage register. The dummy message consists of a header with the request for retransmission bit set to a logic 1, the duplex partner's address, and eight null characters.

The first time the XMIT signal goes high, this dummy message is clocked out of the output storage register, has parity added, and is sent to the propagation delay compensator circuit. The message is then transmitted on the cable by the modulator. Additionally, the message is clocked back into the storage register in case it is required later for a retransmission.

The SDB then sets jump condition #13 of the microprocessor true (meaning the message has just been sent) and sets REXMIT true in case an answer is not received from the duplex partner. The microprocessor resets the jump condition and issues a new header for the old message with both the request for retransmission (bit 5) and the retransmitted (bit 4) bits set. This new header stays in the

output transfer register until an answer is received from the duplex partner. If no answer is received and the XMIT signal goes high again, the new header is clocked out of the output transfer register overwriting the old header and is followed by the remainder of the old message.

This procedure prevents valid data from being transmitted until both duplex partners are connected to the system. When an answer is received, the microprocessor reads the header to determine if a retransmission has been requested. If so, an appropriate new header is issued (i.e., retransmission bit 5 is 0 and retransmitted bit 4 is 1). If not, the microprocessor issues a new message containing data from the terminal (with null characters to fill unused space if necessary).

B.5.7 Input Data Storage and Transfer Buffer

In order to have the incoming receiver address header available, the SDB stores the first byte of all data received during state 3 at the cable input register (CIR) internal to the input data storage and transfer (IDST) buffer. The CIR is comprised of both a 64-bit serial in/out shift register called the input storage register and an 8-bit, serial in, parallel out shift register called the input transfer register. If the RCV signal goes active (meaning the message is intended for this subscriber), the stored header byte

stays in the input transfer register, the rest of the address is not saved, and the four data words are stored in the input storage register. If no parity errors are encountered, jump condition #15 is set true (meaning a message has just been received) and any other data is prohibited from entering the CIR. The microprocessor reads the input header byte, prepares the necessary output message, then reads whatever portion of the data it requires before resetting jump condition #15. When the jump condition is reset, new data is allowed to enter the CIR in preparation for the next incoming message, whose address is examined, and the cycle repeats.

B.5.8 I/O Clock Enable

The IDST and the ODST are clocked by either the system clock from the demodulator or by the locally generated clock. The selection of the clock source, the duration of a given clock burst, and the destination of the burst are determined by the input/output I/O clock enable circuit. This circuit is comprised of a number of logic gates that form a steering network that applies the system clock to the IDST, ODST, or the propagation delay compensator in order to properly input or output message blocks. This circuit also applies the local clock to either the IDST when read by the microprocessor or the ODST when written into by the microprocessor.

B.5.9 Local Clock

The locally generated clock operates at approximately the same frequency as the system clock. Whenever the IDST or the ODST is addressed, the local clock generates a burst of eight clock pulses used to shift one byte of data into or out of the appropriate transfer register. Note that if a header byte is written into the ODST which is destined to be the new header of a retransmission, the I/O clock enable blocks the eight local clock pulses so that the header byte stays in the transfer register as stated in Subsection B.5.6. Finally, the local clock circuit generates an 850 ns negative pulse called "CIRCDN" at the end of each 8-pulse burst. This signal clears the latches that were set when the IDST or ODST was addressed.

B.5.10 Propagation Delay Compensator

In Subsection B.5.6 it was explained that the entire message was shifted to the propagation delay compensator (PDC) during the data poller message block in which the polling address match was detected. During the next data poller message block, the PDC assembles the 85-bit message in a temporary holding shift register. During state 12 of that message block, a pulser, which has been set between 0 and 20 μs is triggered by the PDC. The purpose of this pulser is to compensate for the predicted cable propagation delay to

the data poller. At the end of this pulse, the L control lead to the modulator goes high, which enables the transmitter. The system clock is then gated out to the modulator and a negative sync pulse (two clock periods long) is sent to the modulator, followed by the 85-bit message.

Now that the function of the PDC has been described, two facts mentioned earlier can be more readily understood. First, the reason that the state counter must be free running during the timeout is because it is required to operate the PDC at least two data poller message blocks after the XMIT signal goes active. Second, the reason why only 28 of 32 cycles are available for data processing is shown in Figure B-27. If the delay pulse were set to the maximum (20 μs), which is approximately one half a data poller message block (46 μs), the output message sync pulse would not reach the data poller until two and one-half data poller message blocks after the transmitter address match. The output message would then clear the data poller retimer circuit and reach the destination subscriber during the next message block (i.e., three message blocks after the transmitter address match). Because the subscriber's addresses of a duplex pair are numerically 16 apart, and high-speed and low-speed polls are interleaved, it becomes apparent that a given subscriber will be polled 32 data poller message blocks after the duplex partner is polled (if the pair are on the high-speed polling cycle). If the 3-message block delay introduced by the PDC

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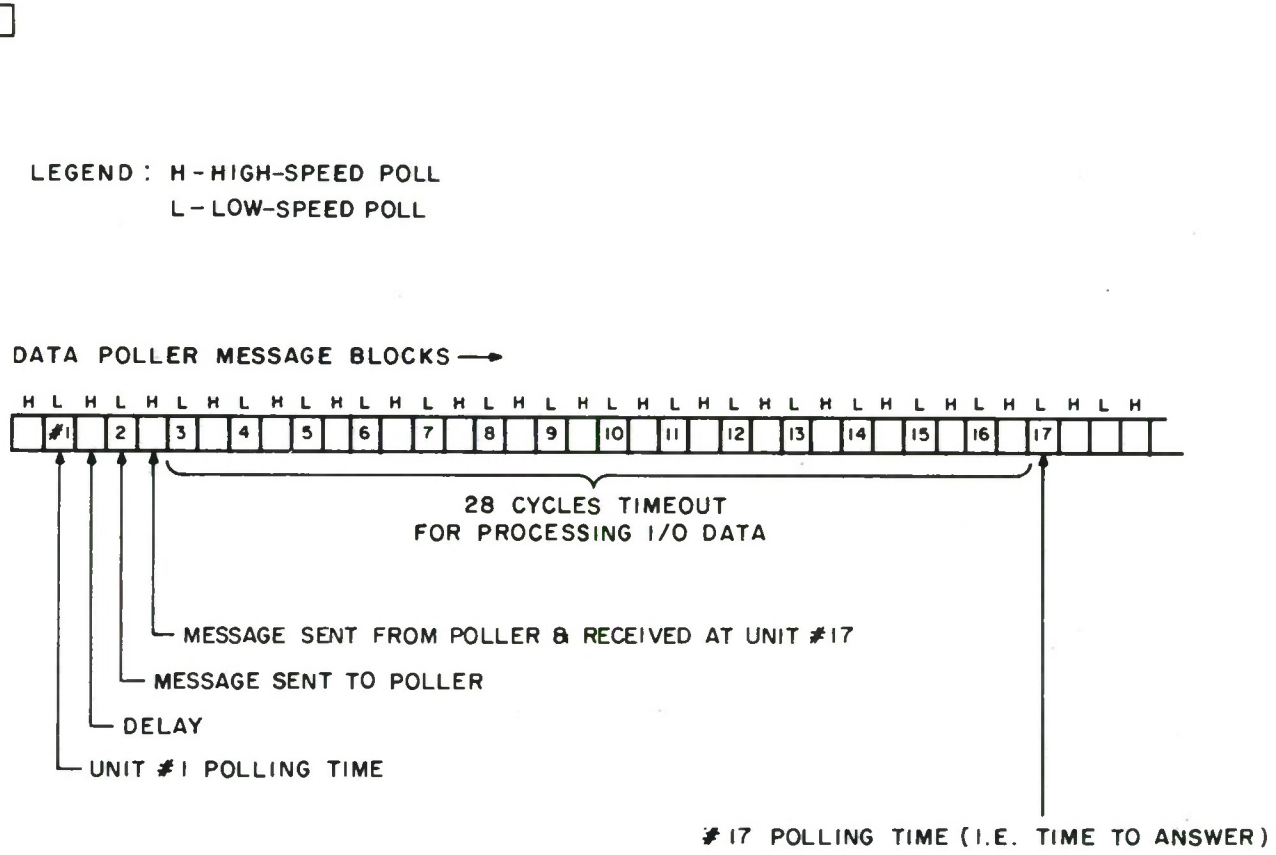

Figure B-27. Real-Time Diagram for Microprocessor Functions

is subtracted from the 32 available, the remainder (29) is the shortest amount of time available to a subscriber between receiving and transmitting; therefore, an SDB can be inactive (timeout) for a maximum of 28 data poller message blocks as discussed in Subsection B.5.5, allowing the microprocessor time to process input or output data.

B.5.11 Microprocessor

The microprocessor used for the subscriber data buffer is the same as was used in the data poller, i.e., the National PACE. The PACE features a 16-bit word size and a 2 μs microcycle. The PACE also employs a bidirectional, MOS level, address and data bus. This bus is readily interfaced by using National's bidirectional transceiver element, which provides I/O buffering between the MOS bus and the TTL devices used in the rest of the SDB.

Another support chip, the system timing element, is required to provide the single-phase true and complement MOS clocks, the corresponding TTL clocks, and a substrate bias voltage (8 volts) for the PACE. An address latch element is needed to provide address latching for the National #MM5204 erasable programable read-only memory. These devices are 4096 bit memories constructed in a 512 X 8-bit organization, and two devices are used in the SDB to provide space for a 512 X 16-bit word program. The read/write memory used

in the SDB is a National #1PC-16A/504 static random access memory (RAM), which is a 256 X 4 bit device. Four devices are used in the SDB, thus providing 256 X 16 bits of RAM. The interconnection and interaction of these devices is thoroughly described in the National Semiconductor's technical description of the PACE (Reference 17) and therefore, will not, be discussed here. The utilization of this microprocessor is presented in the software description following in Subsection B.6.

B.5.12 Peripheral Address Decode

The PACE interacts with the rest of the SDB hardware via the peripheral address decode circuit. This circuit monitors the bidirectional bus from the PACE during all address strobes (generated by the PACE) and latches the address that is on the bus if it is detected to be within the assigned range of 8000 through 8009 (hexidecimal numbers). The circuit then gates the next input or output strobe (PACE-generated) to the appropriate hardware register, allowing the PACE to read or write to the register. Within the range of available peripheral addresses, seven are used, one each for the IDST, ODST and TADR, and four for interaction with the terminal interface. See Table B-1.

TABLE B-1

MICROPROCESSOR PERIPHERAL ADDRESS ASSIGNMENTS

Address	Assignment
8000	Not Used
8001	CIR (IDST)
8002	COR (ODST)
8003	Terminal-to-Cable Character Load
8004	Terminal-to-Cable Character Ready
8005	Cable-to-Terminal Character Load
8006	Cable-to-Terminal Character Ready
8007	TADR
8008	Not Used
8009	Not Used

B.5.13 Terminal Interface

The terminal interface adheres to the signal definitions, electrical specifications, etc., that are defined in the Electrical Industries Association Standard called RS-232-C (Reference 18). The National Semiconductor's #LM1488 quad line drivers and #LM1489 quad line receivers are used to accomplish the conversions from TTL to MOS levels required by this standard. The most important device in this interface is a Western Digital TR1602 universal asynchronous receiver/transmitter (UART). The UART provides the parallel-to-serial and serial-to-parallel conversions between the RS-232-C data lines (serial) and the PACE (parallel). The word length, stop bit, and parity selection control lines to the UART are connected to rear panel switches on the SDB chassis and facilitate quick matching of the SDB to the data format of the user's terminal. The master clock to the UART is generated by a National #MM5307 baud rate generator/programmable divider that is also controlled by rear panel switches. This feature allows a user to select one of fifteen typical baud rates from 50 to 9600 baud. A derivative of the UART clock is used as the timing signal to the terminal interface and is, therefore, automatically kept in the proper relationship to the selected baud rate.

The last two parts of the terminal interface are the break detector and the break generator. The break detector circuit

monitors the data line from the terminal and sets the PACE jump condition #14 (Break 14) true if it detects a break signal. The microprocessor inserts a special character (see Subsection B.6.1) into the outgoing data software buffer and resets the jump condition. When the "break character" is received by the SDB, the microprocessor pulses flag #12 (Break 12). This action causes the break generator to take control of the data line to the terminal after waiting for any characters in the UART to clear, duplicates a break signal, and returns control to the UART.

B.6 MIDS SUBSCRIBER DATA BUFFER SOFTWARE

Executing the fixed program stored in its read-only memory, the SDB microprocessor controls the flow of information between the terminal and cable. The microprocessor read/write memory contains two wrap-around software buffers, one to hold data being transmitted from the terminal to the cable (the TC buffer), and one to hold data moving from the cable to the terminal (the CT buffer). The buffers are used to resolve timing differences between the terminal rate and the transmission rate. Data is stored in the buffers one character per word, indexed by pointers. The pointers indicate the location of the first and last characters in the buffer and are also used to compute the amount of data in the buffer. In normal operation, the number of characters stored in either the CT or the TC buffer is small.

The transmission rate is adequate to support the terminal; if, however, the terminal starts to transmit at a high rate, the TC buffer will approach capacity. At a certain threshold level the SDB will request a high-speed transmission rate from the data poller. The poller will poll both the SDB and his connectee more frequently and the buffer will empty out. Another higher threshold is used to cause the terminal to hold up in the event that high-speed service is unavailable. The two threshold levels can be adjusted according to the maximum transmission speed of the terminal and the time it takes for a terminal to react to the hold-up signal.

As long as the receiving terminal can accept data as fast as it is being transmitted, there will be no overflow of its CT buffer. If the receiving terminal operates slower than the transmitting terminal, or if it goes out of service during a call, the CT buffer of the receiving terminal will fill up. No attempt is made to slow down the polling rate when the receiving terminal cannot accept the data fast enough. However, to prevent loss of data when the CT buffer is full, the receiving SDB requests retransmission of the last message. The SDB of the transmitting terminal transmits the message as often as necessary, until it is accepted by the receiving terminal. This action,in effect, slows down the transmitting terminal. The same mechanism of retransmission request is used for the correction of parity errors.

B.6.1 Special Character Codes

There is no code conversion built into the SDB presently implemented. Only terminals with the same character code can converse. However, there are two special characters which are created in the SDB of the transmitting terminal and sent in messages to the SDB of the receiving terminal. The bit patterns of these characters were chosen from the characters unused by any of the terminals the SDB may be required to support.

The first of these characters (Code P1100100) is a termination code. It is used to fill in the unused portion of messages. Since messages are of fixed length, either a character count or some type of termination code must be used to define the end of the data transmitted by the terminal. A null code on one terminal was found to be significant data on another. A character was chosen to terminate short messages that is an illegal code on all terminals. The character does not appear in either the TC buffer or the CT buffer of the SDB and is never sent to the terminal.

The second special character is the break character (Code P0010100). On some terminals there is a key that causes a signal to be transmitted which simulates a break in the transmission medium. The key was designed as a way for a receiving terminal to interrupt

a long transmission in a half-duplex connection. The break is used as a control code in some text editing systems and must be accommodated in the messages transmitted by the SDBs; the break signal is sensed by the terminal interface hardware of the SDB. The hardware sets a flag for the software, which then inserts the special break character as the next character in the TC buffer. It is packed into an outgoing message like any legal character.

The SDB of the receiving terminal reads and stores the break character in its CT buffer like any other character. As characters are fed one by one from the CT buffer to the receiving terminal, they are tested for the break code. After detecting a break character, the software sets a flag for the terminal interface hardware, which then generates the break signal for the receiving terminal.

B.6.2 Message Format

Figure B-28 illustrates the message format received by SDB from the cable. The input from the cable, as seen by the SDB hardware, consists of polls alternated with messages. Polls are two bytes long and contain a 10-bit field for binary addresses up to 1023. The SDB hardware used the polls in the input data stream to determine the time to transmit a message to the other party. (This

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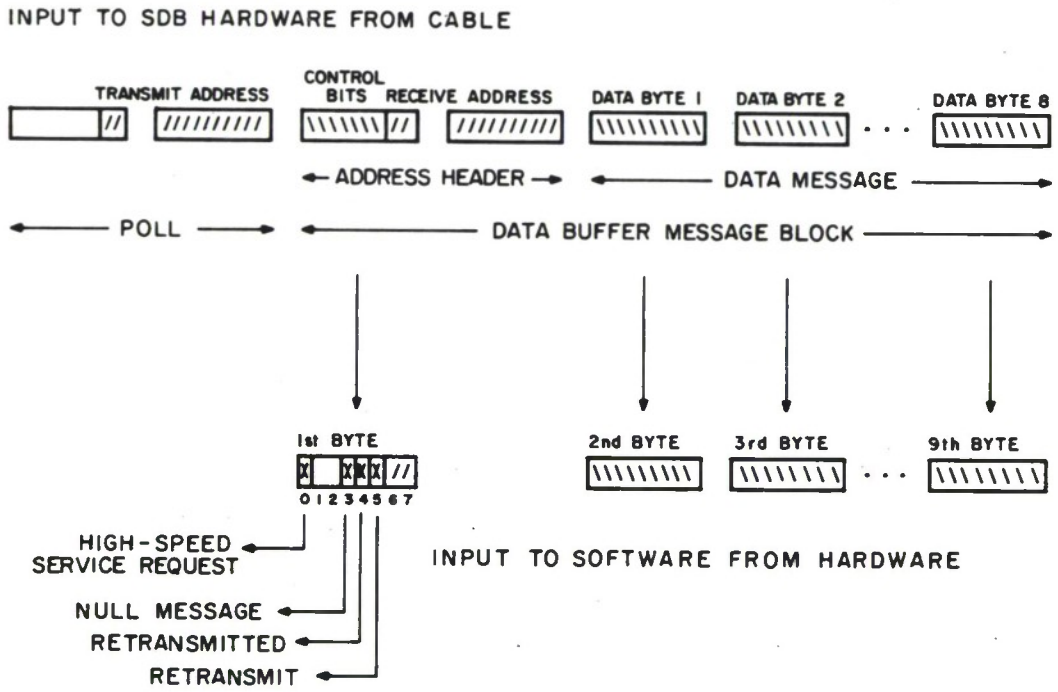

Figure B-28. Message Format

is explained in greater detail in Subsection B.6.6.) Polls are never passed on to the software.

Messages are ten bytes long. The first two bytes contain header information; the last eight contain data. A 10-bit address in the header is used by the SDB hardware to identify messages it is to receive, and the remaining six bits of the header are used for control information. The byte containing the control bits and all eight data bytes are made available for the software to read.

B.6.3 Software Input Message

The software sees the input message as nine bytes, accessed through the CIR by nine consecutive reads. The first byte read is the first header byte, which contains the control bits and the high-order two bits of the receive address. The remaining eight bytes contain data. (The second header byte is not passed on to the software.) Depending upon the contents of the message, either the entire message or only part of it may be read by the software.

B.6.4 Control Bits

Bit 0, the high-speed service request bit, is set to 1 by the transmitting terminal to flag the data poller for a higher polling rate. The bit is ignored by the receiving terminal.

Bits 1 and 2 are spare. (Bit 2 is used as internal control for SDB.)

Bit 3, the null bit, is set to 1 if the message is null. Null messages contain termination characters in all eight data bytes. The null bit was put in the header for the covenience of a front-end processor, which relays data from a multiport data buffer to a host processor.

Bit 4, the retransmitted bit, is set to 1 on retransmitted messages. Its primary function is to prevent SDBs operating, as add-on receive-only terminals to a full-duplex connection, from processing duplicated data messages.

Bit 5, the retransmit bit, is set to 1 to request retransmission. Retransmission is requested either because of a parity error or because the CT buffer of the receiving terminal is full.

Bits 6 and 7, the two-high order bits of the receive address, are ignored by the software.

B.6.5 Output Message

Each time an SDB is polled, it transmits a message consisting of two header bytes and eight data bytes in the same format as the input message. The message goes to the data poller where the high-speed request bit is checked. It is then inserted, unchanged, between two polls and transmitted so it can be identified and then received by the receiving data buffer.

The output message composed by the software is somewhat different from the input message. Normally all ten bytes are sent to the hardware through the same register (ODST-cable output register) in ten consecutive writes. The hardware saves the message in an output buffer to be transmitted when the SDB is polled. After transmission, the message remains in the hardware buffer to be used again if there is a retransmission request.

A retransmitted message is identical to the preceding output message except for the first header byte. If an output message is to be retransmitted, the software sends only the first header byte to the hardware. Bit 4 of this byte, the retransmitted bit, will be set to 1. Using bit 4 as a flag, the hardware recognizes this as the header of a retransmitted message, and composes a message with the new first header byte followed by the remaining nine bytes of the preceding message.

Bit 2 of the first header byte has a special use in the output message; in all transmitted messages, this bit is zero. If bit 2 of the first header byte is 1, the connection is simplex, where the SDB is receiving only. The output message is a dummy message written to simplify the SDB hardware and is not meant to be retransmitted. The hardware has other means of telling that the connection is simplex, but testing a bit is easiest.

B.6.6 Addressing

The addresses used in the data system are temporary indirect addresses, assigned to the subscriber data buffers by the S&S subsystem at call setup time. Each data buffer has two 10-bit hardware address registers, one to contain the receiver address, which is the address in the header of incoming messages, and one for the transmitter or polling address, which is the address that will be included in outgoing messages. When the data terminal is not in use, these registers will contain zeros. While the terminal is involved in a duplex connection, both registers will contain non-zero addresses differing numerically by 16. When the terminal is receiving in the simplex mode, the receiver address will be non-zero and the transmitter address zero.

Address assignments are made at the NCC through the S&S subsystem. At call setup time, the NCC sends a message to the

keypad control unit of each party involved in the data call. The message contains the receiver and transmitter indirect addresses to be used in the data buffer for the duration of the call. These addresses are transferred from the keypad control unit to the associated SDB through a special interface designed for this purpose. The receipt of the addresses by the SDB constitutes a connection. The connection is in effect until the keypad receives a message containing zero in both indirect addresses and uses these addresses to clear the SDB.

The SDB uses both indirect addresses to compare against addresses in the input data stream. It uses the receiver address to test the message headers. A match on a message header causes the SDB to read the remainder of the message and transfer the message, including the first header byte and eight data bytes, to the microprocessor. The transmitter address is used for testing polls. A match on a poll is the signal for the SDB to start transmission of the output message that is already prepared and waiting in a hardware buffer. Since the receiver address of one party in a duplex connection is the same as the transmitter address of the other, the output message will have in its header the same address that triggered the transmission. In a simplex connection, where the transmitter address of the SDB is zero, a match on a poll does not cause the SDB to transmit.

The microprocessor in the SDB is never given the receiver address. The transmitter address is sent to the microprocessor from the SDB hardware at call setup time and is used by the software to compose the header in output messages. It is also used to identify simplex connections for which the processing is slightly different than in duplex connections.

B.6.7 Polling

The data system is designed for adaptive service. The transmission service on the cable automatically adjusts to the transmission speed of a terminal. There is a low-speed service, which is provided for idle terminals and terminals transmitting at up to about 600 b/s, and there is a high-speed service for terminals transmitting faster than 600 b/s. High-speed service is provided only while the terminal is actively transmitting at a high rate. Service drops back to low-speed when the terminal stops or slows down.

The transmission service provided to a terminal is a function of the frequency of polls to the SDB. Normally, an SDB is polled about ten times a second. Each time it is polled, it can transmit up to eight characters from its TC buffer. If the polling rate is too slow to keep up with the terminal, the buffer will start to fill up. At a certain threshold level, the software sets the high-speed

service request bit in an outgoing message. The data poller intercepts the message, sees the high-speed request bit, and polls the SDB about 30 times as fast as normal for the next tenth of a second. In most cases, the extra polls allow the buffer to clear out, and low-speed service resumes. If the buffer is still over the threshold level after one-tenth of a second, the high-speed service request flag will again cause the poller to poll at the higher rate.

From the point of view of the SDB, the polling rate and the rate at which incoming messages arrive is unpredictable. The input data stream, which contains both the polls and the incoming messages, is controlled by the data poller. The poller allows at least 1.48 ms between the time it polls an SDB and the time it polls the other party in the duplex connection; however, this time interval may be as long as 93.18 ms, resulting from subscriber address assignments within the system timing interval.

B.6.8 Software Organization

The time interval of 1.48 ms between the polling of two connected SDBs is the product of the polling speed of the data poller (46.222 μs) and the minimum spacing of polls (32) between connected parties. At the beginning of this time interval, a message is transmitted from one of the data buffers (call it

Terminal B) to the data poller, where it is retimed and sent to the other data buffer (Terminal A). Because of such factors as propagation delay time and buffering at the data poller, the message from Terminal B will not appear in Terminal A's input data stream until three message times later. Terminal A must read the message, check it for validity, and test the retransmit bit before preparing its own output message. The delay of three message times, plus the normal time necessary to read a message, reduces the time available for composing the output message to twenty-eight message times, or 1.28 ms. See Figure B-29. Although this timing is based on the high-speed polling rate, the irregular spacing of the polls makes it necessary for the SDBs to process the message equally fast during periods of low-speed service.

The PACE microprocessor is slow for this data processing application. The first consideration in the design of the software was to minimize the number of executed instructions in the preparation of the output message so the message would be waiting in the hardware buffer when the SDB was polled. In order to compose output message, two things must be known about the input message: 1) whether or not a valid message was received since the last output message was transmitted, and 2) whether or not the input message contained a request for retransmission. The contents of the data portion of the input message have no relevance to the output message.

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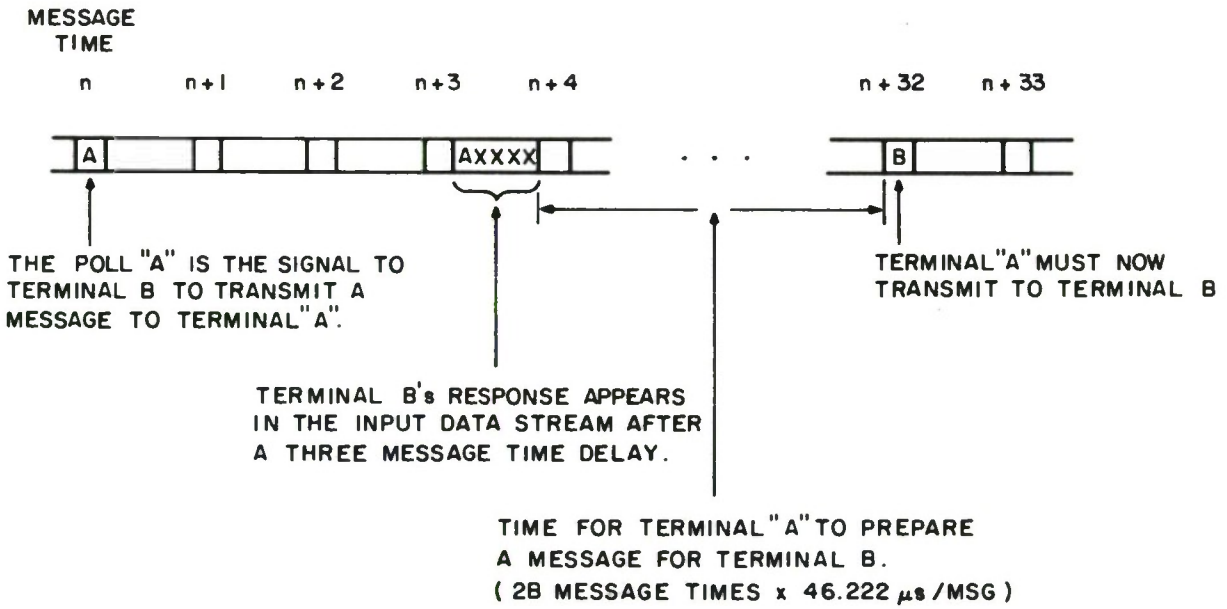


Figure B-29. Message Processing Time

When a message is received by the SDB hardware, the entire message, including both header and data, is checked for validity and stored in a hardware buffer. If valid, the message ready flag, JC15 (Reference 16), is set. The software tests the ready flag at intervals. When it sees the flag, it reads one byte of the message, the first header byte. Before reading the remainder of the input message, it prepares the output message and sends it, one byte at a time, to the output buffer.

The message that is transmitted from the data buffer is ten bytes long. Normally all ten bytes are created in the microprocessor and sent to the hardware buffer at each message time. An exception is made to this rule when retransmission is requested. In preparation for a retransmission request, each output message is retained in the hardware buffer until the following input message has been received. If the "retransmit" bit is set in the input message, only one byte of the output message is created in the microprocessor, the first header byte. Since the message is to be a retransmission, the "retransmitted" bit in the header byte is set. By testing the retransmitted bit, the hardware can tell that the message is to be retransmitted. The microprocessor forms the output message from the new header byte and nine bytes saved from the preceding transmission.

When the software has finished processing the output message, it reads and stores the data bytes of the input message. If the "null" bit is set in the input message header none of the data is read. Otherwise reading stops after the first termination character or after all eight bytes have been read.

After the input message is stored, the software services the terminal. It uses the terminal-to-cable character register (TCCR) ready flag, which is bit 15 of an addressable hardware register, to determine when a character can be read from this register. Each time a character is read from the TCCR and stored in the TC buffer, the TC buffer is checked against the holdup threshold. If the threshold is exceeded, the software notifies the hardware by setting flag 11 (Reference 16); the hardware then stops the terminal. If, after flag 11 has been set, the TCCR ready flag again comes true, the software reads the character and stores it in the buffer. The holdup threshold will be set at a level that prevents the CT buffer from overflowing if a few extra characters are transmitted before the terminal stops.

The cable-to-terminal character register (CTCR) ready flag, bit 15 of another addressable hardware register, is used to tell the software when the terminal is ready to receive a character. If the CT buffer has data in it when the CTCR ready flag is sensed, the software moves one character into this register. When the next

character in the CT buffer is a break character, flag 12 is pulsed to cause the hardware to simulate a break signal to the terminal.

B.6.9 Emergency Messages

The entire message processing is initiated by the setting of the message ready flag, which is done only on receipt of a valid input message. At call setup time, should one of the parties start transmitting before the other is connected, or at any time during the call should a parity error in an address occur, it is possible for a data buffer to be polled twice in succession without an intervening input message. Special provision has been made to cause the data buffer to respond to a poll with a valid output message despite the absence of an input message. The message that is output is a retransmitted message that also requests retransmission. If the problem resulted from a lost input message, the retransmission request will retrieve it. If the message was never sent because the transmitting data buffer was temporarily out of service, such as at call setup time, the retransmitted output message will prevent data loss in the other direction.

The implementation of this function is a combined hardware/software task. Immediately after transmitting a message, the hardware sets a flag for the software, JC13. Upon sensing the flag, the software sends a message header byte to the hardware. The

header byte is the same as the header byte in the preceding output message, except that the retransmit and retransmitted bits are set. The header is stored in the output buffer in front of the last nine bytes of the preceding output message. If the SDB is polled before it receives an input message, it responds to the poll by transmitting this emergency message. In the normal case, when an input message arrives before the SDB is polled a second time, the new header byte that the software creates replaces the emergency header byte in the hardware buffer.

The emergency message feature was designed to allow the data buffer to function properly in the absence of an input message. It is also used when an input message is received but found to be invalid. When the hardware detects a parity error in an incoming message, it bypasses the setting of the message ready flag. In the absence of the message ready flag, the software neither reads the input message nor prepares a new output message. Eventually the SDB is polled and the emergency message is transmitted.

B.6.10 Initialization

The SDB is initialized whenever the S&S keypad control unit sends it receiver and transmitter addresses, which is at call setup time, disconnect time, and at power-up. At disconnect and power-up time, the addresses will both be zero. At call-setup time, the

receiver address will be non-zero and the transmitter address may or may not be zero. When the SDB hardware receives the addresses, it stores them in the address registers, one of which (the transmitter address register) is readable by the software. The control of the microprocessor is transferred to the initialize routine.

In the microprocessor, flags are reset and buffers cleared. The transmitter address is read and checked for zero. A null message is sent to the output buffer, which provides the hardware with a valid message to transmit if it is polled for transmission before an input message is received. The program then enters a tight loop, testing JC13 for an indication that a message was transmitted and JC15 for a signal that a message was received. If JC13 comes true, an emergency messsage header is sent to the hardware (with retransmit and retransmitted bits set). Normal processing begins when a message is received from the other terminal.

If both the receiver and transmitter addresses are zero, the initialization routine is entered as it would be for a call setup, but in this case, the message ready flag will not be set and control of the microprocessor will remain in the initialization routine until another call is established.

B.6.11 Peripheral Registers

The following peripheral register addresses are used by the data buffer microprocessor. The functional descriptions are self explanatory. The 4-digit address are hexadecimal addresses used by SDB software to address the register.

CIR - 8001 - Cable Input Register: Used by the cable interface hardware to transfer data from the cable to the PACE. Data enters the PACE one byte at a time through the low-order eight bits of CIR. JC15 is used as a message ready flag. Successive reads by the software will obtain the first byte of the message, which contains the control bits, the third byte, etc. The second byte, containing the low-order eight bits of the address, is never transferred to the software.

COR - 8002 - Cable Output Register: Used by the cable interface hardware to transfer data from the PACE to a hardware buffer from which it will be transmitted onto the cable. Data is output one byte at a time through the low-order eight bits of COR. For every message to be transmitted, the software writes either the entire message consisting of two header bytes and eight data bytes, or it writes only the first header bytes and no data bytes. The

hardware tests bit 4 of the header byte, the retransmitted bit to determine whether or not the whole message will be sent. If bit 4 is set, no more information will be transferred by the software and the hardware will transmit a message composed of the new header byte and nine bytes saved from the preceding message. A "1" in bit 2 of the first header byte tells the hardware that the connection is simplex and the message that follows is a dummy message not to be transmitted.

TCCR - 8003 - Terminal To Cable Character Register: Used for transferring data from the terminal to the PACE. Data is sent to the microprocessor one character at a time through the low-order eight bits of TCCR. When the register is loaded, the terminal interface hardware sets the TCCR ready flag, which can be tested by the PACE software. Reading of the register by the software causes the ready flag to be reset.

TCCRRDY - 8004 - TCCR Ready Flag: Bit 15 of this register is used as a TCCR ready flag (see TCCR above). All other bits are unused.

CTCR - 8005 - Cable To Terminal Character Register: Used for transferring data from the microprocessor to the terminal.

Data is sent to the terminal one character at a time through the low-order eight bits of CTCR. When the terminal is ready to accept a character from the microprocessor, the terminal interface hardware sets the CTCR ready flag. Writing into the register by the PACE causes the ready flag to be reset.

CTCRRDY - 8006 - CTCR Ready Flag: Bit 15 of this register is used as a CTCR ready flag (see CTCR above). All other bits are unused.

TADR - 8007 - Transmitter Address Register: Used to provide the data buffer software with an indirect address to be used in the header of output messages. The register is loaded by the data buffer/S&S keypad interface hardware at call setup time. Zero in this register indicates a simplex (receive only) connection. The address is taken from the low-order ten bits of the third word of the S&S message, which sets up indirect addresses for data service.

B.6.12 Jump Conditions and Flags

The PACE microprocessor provides jump conditions and flags as a convenient means of relaying signals to and from external hardware. There are three jump conditions, JC13, JC14 and JC15, which can be used as needed to input signals to the microprocessor.

Jump conditions are controlled by the external hardware and can be tested by the software. Four flags, flags 11-14, are used by the software for sending signals out of the microprocessor. These are controlled by the software and tested by the external hardware. Jump conditions and flags are used in the data buffer as follows:

JC13 - Message Transmitted: Set by the cable interface hardware after a message has been transmitted. Sensing JC13, the software sends an emergency header byte to the output buffer. After receiving the expected header byte, the hardware resets JC13.

JC14 - TC Break: Set by the terminal interface hardware when the break key has been depressed at the terminal. Sensing JC14, the software inserts a break character into the TC buffer and pulses flag 13 as an acknowledgment that it has sensed JC14. JC14 is reset as a result of the pulsing of flag 13.

JC15 - Message Received: Set by the cable interface hardware when a message has been received by the hardware, tested for parity and is ready to be read by the software. JC15 is set only on receipt of a valid input message. Sensing JC15, the software reads as much as it needs of the message and

eventually pulses flag 14 as an acknowledgment that it has read the message. The pulsing of flag 14 causes JC15 to be reset.

Flag 11 - Terminal Hold-up Flag: Set by the software when the TC buffer reaches the hold-up threshold. It is reset after a message has been sent to the output buffer.

Flag 12 - CT Break Flag: Pulsed (turned on briefly, then turned off) when the next character in the CT buffer is a break character. Sensing flag 12, the terminal interface hardware inputs a break signal to the terminal.

Flag 13 - TC Break Acknowledgment: Pulsed as an acknowledgment that the software has acted on the TC break signal, JC14. The terminal interface hardware uses flag 13 to reset JC14.

Flag 14 - Message Received Acknowledgment: Pulsed after the software has finished reading what it needs of the input message. Flag 14 is used by the cable interface hardware to reset JC15.

B.6.13 Character Buffers

Figure B-30 illustrates various states of the wrap-around character buffers. Note that each buffer has four pointers, two of which are constant. The constant pointers (BOB and EOB for the TC buffer and BIB and EIB for the CT buffer) indicate the location of the beginning and end of the buffer. The variable pointers (BOD and EOD for the TC buffer and BID and EID for the CT buffer) locate the beginning and end of the data. When the buffer is empty, the two variable pointers are equal. The buffer is never allowed to fill completely because this condition would also result in the variable pointers being equal.

B.6.14 SDB General Flowchart Summary

The general flowchart in Figure B-31 shows the major steps involved in software for the data buffer microprocessor and summarizes the topics of previous subsections.

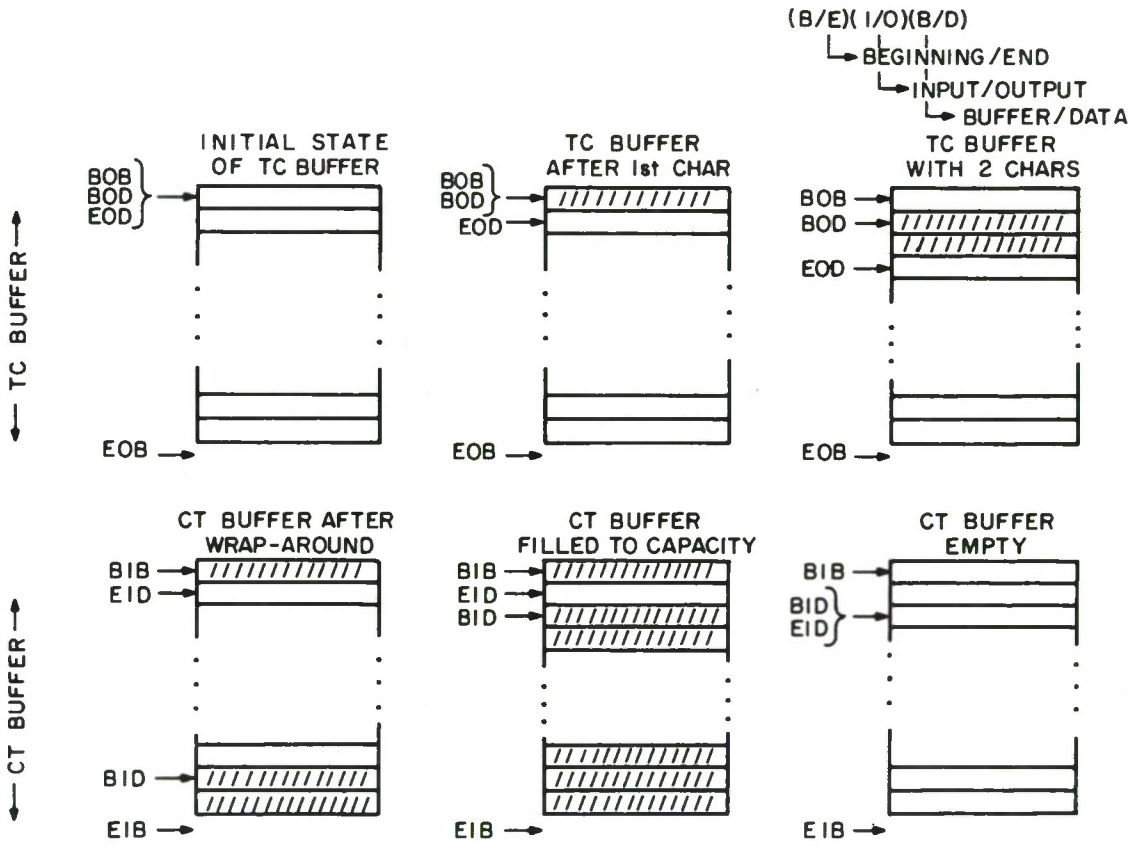


Figure B-30. Sample States of the Character Buffers

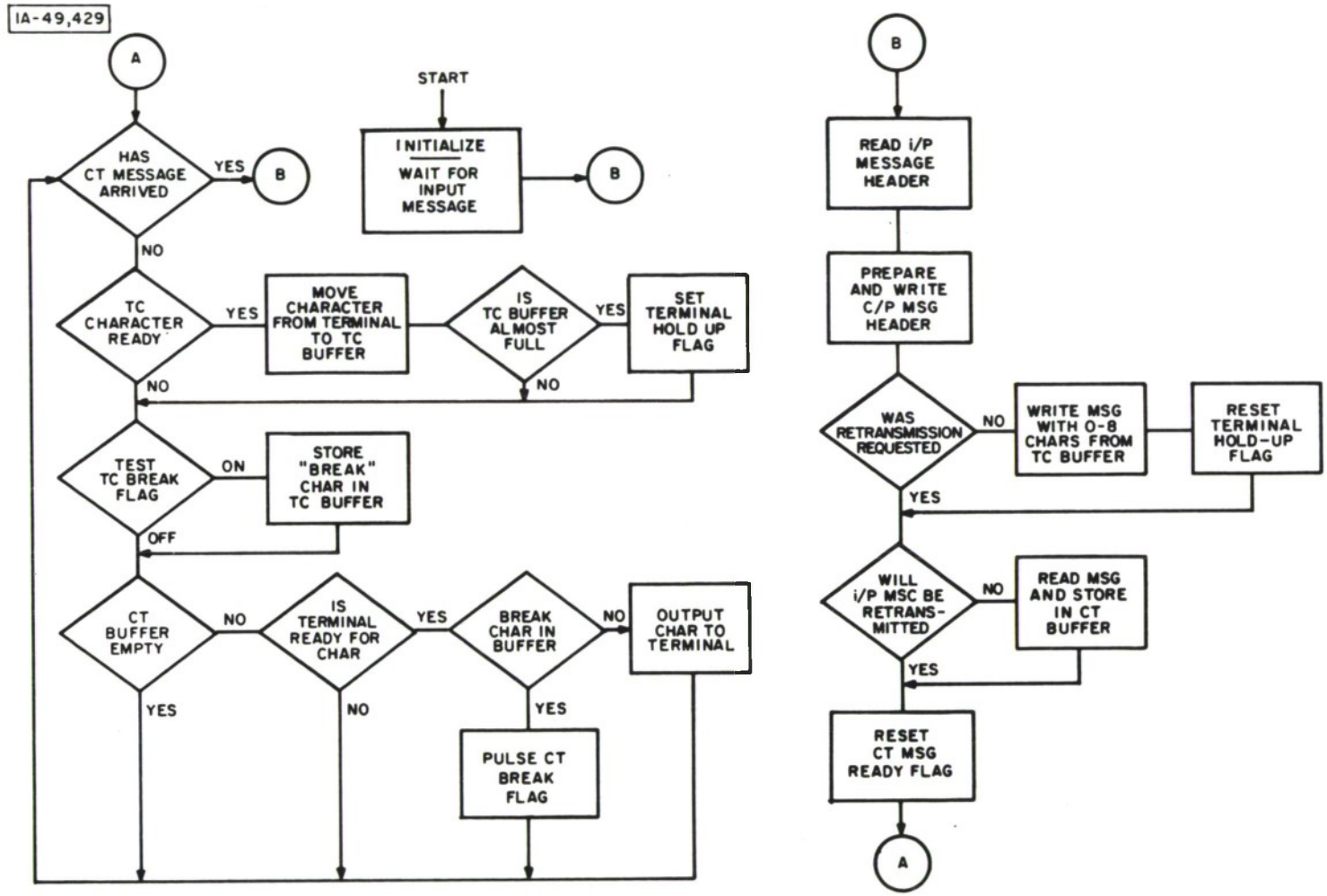


Figure B-31. Subscriber Data Buffer General Flowchart

APPENDIX C

MODEMS

The modem development effort under the MIDS operating environment achieved two main purposes:

a. It demonstrated the practical feasibility of three-phase differential phase shift keying modulation, and

b. Demonstrated the feasibility of accommodating simultaneously active multiple users on a common wideband media without undue mutual interference.

Since modems were not available commercially to meet the requirements of this application, they had to be developed specifically for MIDS at The MITRE Corporation.

As MIDS was designed to be implemented on the existing MICOM cable system, modem specifications were governed primarily by the consideration of potential intermodulation distortion resulting from amplification nonlinearity within the wideband cable amplifier.

In a cable system, the signal level unit is dBmV, with the reference 0 dBmV being equivalent to 1 mV rms measured across 75 ohms characteristic impedance. Signal level specifications adopted for the MICOM cable system are as follows:

a. In-Band Signal Levels at Cable Interface

(1) Transmit: 45-55 dBmV with modem keyed-on, less than 14 dBmV with modem keyed-off.

(2) Receive: 0-20 dBmV.

b. Out-of-Band Component Levels

(1) Transmit: At least 46 dB below normal transmit level with modem keyed-on, less than -16 dBmV with modem keyed-off.

(2) Receive: Modem shall be unresponsive to all out-of-band components at levels up to 20 dBmV.

Two types of modems are required for MIDS. The S&S modem handles only service request and network connectivity control traffic, and the data modem carries the high-speed digital data traffic up to 2.5 Mb/s. By virtue of the use of a much simplified flag-for-service signaling scheme, it was determined that a signaling rate of 25 kilobauds would be sufficient to meet all MIDS signaling and supervision requirements. For this reason, the approach for the S&S modem was to utilize straightforward amplitude shift (on-off) keying modulation.

On the other hand, in the transmission and reception of asynchronous digital data, sync and clock timing information must be conveyed in addition to the data itself. For the sake of bandwidth utilization efficiency, it was decided that a unique three-phase

modulation approach would be particularly suited to MIDS application. Thus, the novel TPM/DPSK (three-phase modulation/differential phase shift keying) data modem was developed.

During the early stages of the S&S modem development, serious problems were encountered in the design of detectors. Originally it was thought that a half-wave rectifier followed by a comparator would suffice for the on-off detection. It was found, however, that the pulse width of the detector output varied significantly over the operating range of the receive signal level. This problem was circumvented by adopting a combination of a square-law detector and a crystal filter followed by a comparator. The resulting S&S modem design is described in Section C.1.

The original data modem developed for MIDS employed several novel techniques, and initial problems were related to the filters as opposed to the detectors and phase generators.

For the data modem, the initial plan was to use two identical 4-pole Butterworth filters, one on each end of the transmit and receive modems, to provide sufficient protection against adjacent channel interference. Unfortunately it was discovered that the tuning and alignment of the filters were far too critical to maintain stable operation. Since the TPM scheme had never been

attempted in practice, there was some concern that the bandwidth requirements for proper TPM operation might exceed the 12 to 24 MHz limit allocated to MIDS. Consequently, a theoretical study was made to determine the spectral content of some representative TPM waveforms. In this manner it was established with confidence that a bandwidth allocation of 1.5 Hz/b/s would be adequate (References 19 and 20) and that the TPM modem problem was attributable mainly to the cumulative phase nonlinearity near the skirts of the Butterworth filters. The problem, once recognized, was rectified by using a 5-pole Bessel filter (maximal flat delay) in place of the 4-pole Butterworth filter in the receive modem. Operation of the data modem is described in Section C.2

C.1 S&S MODEMS

Two S&S modems provide interfaces between the RF signals on the coaxial cables and the S&S logic circuits: the S&S poller modem which transmits at a carrier frequency of 12.8 MHz and receives at 13.6 MHz, and the S&S subscriber modem which transmits at 13.6 MHz and receives at 12.8 MHz. The S&S poller modem interfaces with the PDP 11/10 network control computer (NCC) through the S&S poller unit, while the S&S subscriber modem interfaces with the keypad control unit at the subscriber location. Both modems are structured almost identically, and both operate on the principle of amplitude shift keying modulation at a nominal keying rate of 25 kilobauds.

Figure C-1 shows the physical layout of a typical S&S modem with the modulator and demodulator packaged in one box.

C.1.1 S&S Modulator

The S&S modulator consists of a crystal oscillator, a MOSFET (metal oxide semiconductor field-effect transistor) gated amplifier, and a harmonic trap filter. Figure C-2 shows a simplified block diagram of the S&S modulator.

The crystal oscillator is capable of delivering a sine wave carrier output at a signal level of 700 mV peak-to-peak. This output, combined with the potential 18-dB amplification in the MOSFET gated amplifier, provides a comfortable reserve of signal strength in the modulated RF output.

The MOSFET amplifier used in the S&S modulator is a silicon, depletion type, dual, insulated-gate, field-effect transistor (RCA 40673) that provides a wide dynamic range, fast switching response, and built-in back-to-back diode protection against handling damage. The gate control is driven by TTL (transistor-transistor logic) level data from the S&S logic circuits. When the data is low, the gate is open, letting the RF carrier out for transmission. When the data is high, the gate is closed, thus suppressing the RF carrier.

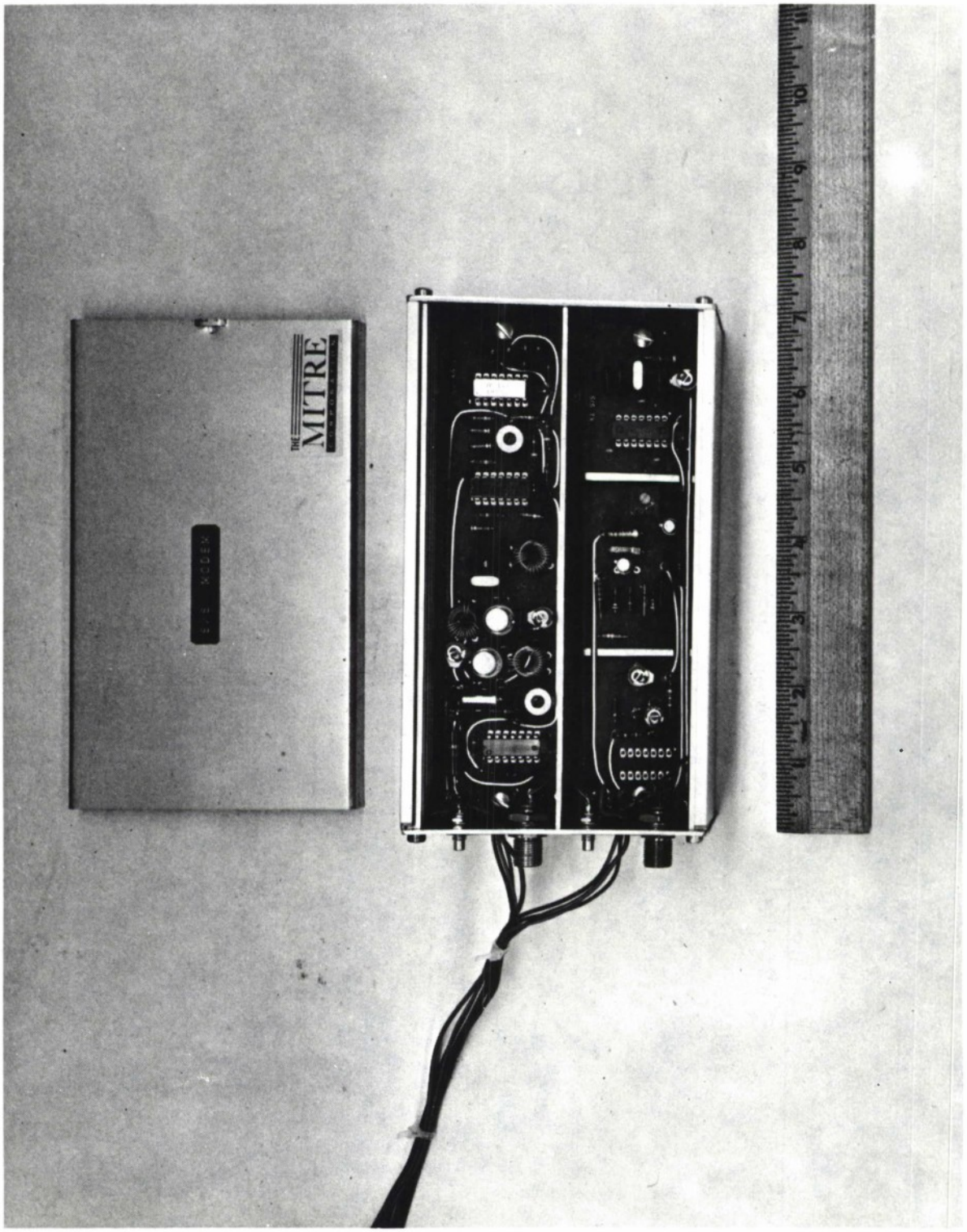


Figure C-1. S&S Modem

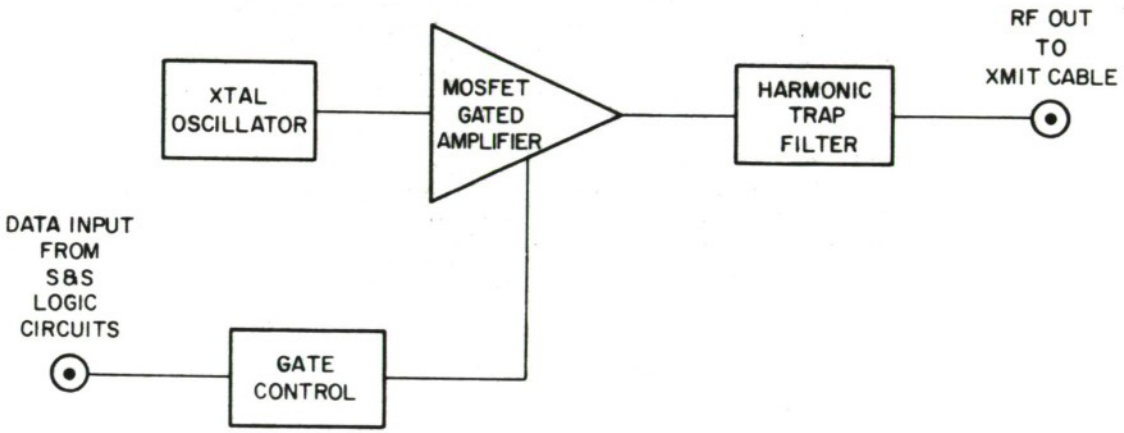


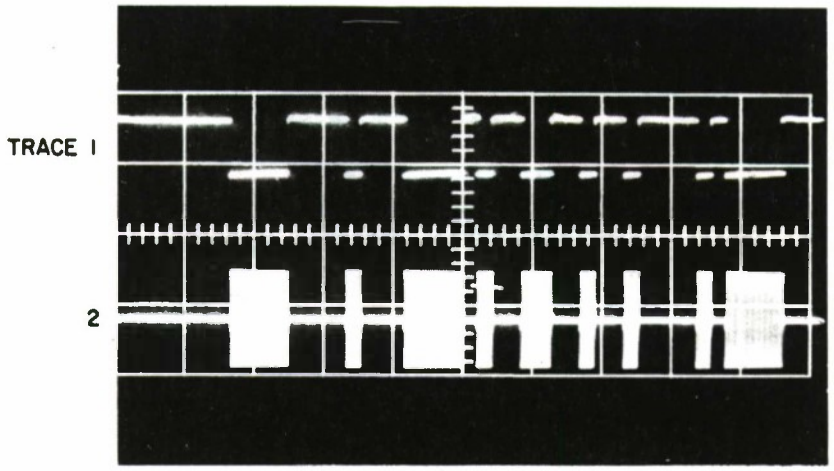
Figure C-2. S&S Modulator

To conform with modem specifications, the gated carrier is passed through a harmonic trap consisting of an LC π-network. By means of small trim capacitors, the π-network can be fine-tuned to provide a better than 30-dB supression of second- and third-order harmonics with reference to the fundamental carrier. Figure C-3 shows the RF output waveform of the S&S modulator.

C.1.2 S&S Demodulator

Figure C-4 is a simplified block diagram of the S&S demodulator, which consists of a preamplifier, a two-stage tuned amplifier, a crystal filter, a square-law detector, and a comparator.

The preamplifier has an adjustable gain of from 0 to 40 dB; in operation, generally it is set at a gain of around 20 dB. The two-stage tuned amplifier also has a gain of about 20 dB, but its primary purpose is to provide some predetection filtering. The LC tuned circuits used in this amplifier are designed for a 3-dB bandwidth of 600 kHz. Narrowband filtering is provided by the crystal filter, which has a 3-dB bandwidth of 100 kHz. The filtered and amplified RF signal is fed through a square law detector and comparator to generate a TTL-level data output for use in the S&S logic circuits. Figure C-5 shows examples of the demodulator output at different received RF signal levels.



1A-49,456

1. MODULATING WAVEFORM, 5 V/DIV
2. MODULATED RF, 0.5 V/DIV

Figure C-3. S&S Modulator Output Waveforms

S&S modem performance characteristics are presented in Section C.3 along with the data modem characteristics.

C.2 DATA MODEMS

Two TPM/DPSK modems provide interfaces between the coaxial cable transmission media and the data subsystem's data poller unit, and the subscriber data buffer unit. The modem associated with the data poller unit is called the data poller modem; the modem associated with the data buffer units is called the data buffer modem. Both versions of the data modem are structured almost identically except for their operating frequencies. The data poller

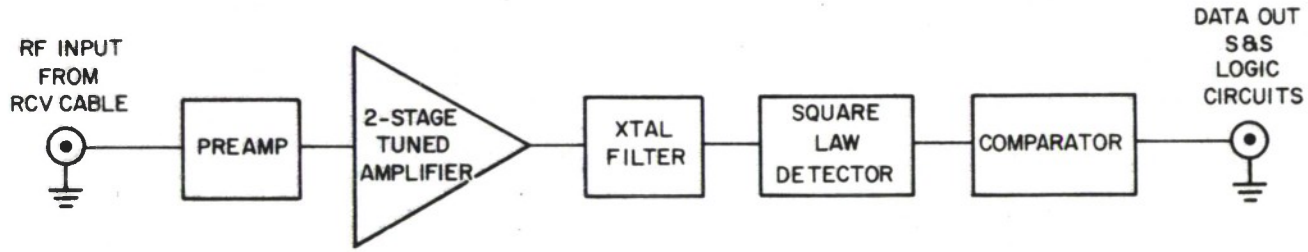
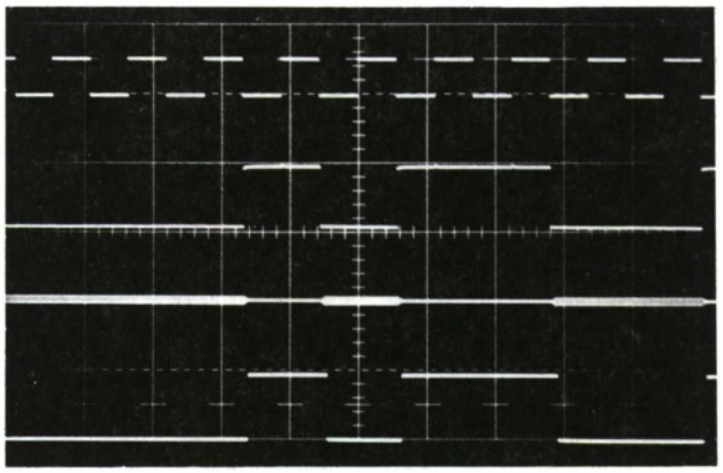


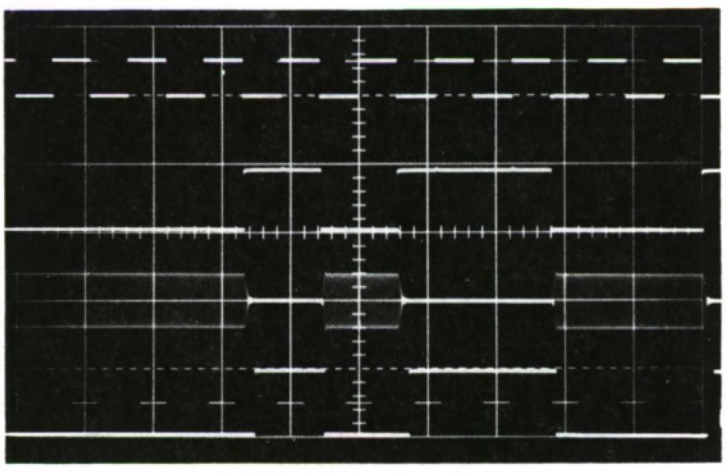
Figure C-4. S&S Demodulator



SWEEP RATE, 40 μs/cm

1. CLOCK PULSES, 10 V/cm
2. MODULATING DATA PATTERN, 5 V/cm
3. MODULATED RF AT RECEIVER INPUT, 0.1 V/cm
4. OUTPUT DATA FROM

IA-49,457



SWEEP RATE, 40 μs/cm

1. CLOCK PULSES, 10 V/cm
2. MODULATING DATA PATTERN, 5 V/cm
3. MODULATED RF AT RECEIVER INPUT, 0.1 V/cm
4. OUTPUT DATA FROM RECEIVER, 5 V/cm

IA-49,459

Figure C-5. S&S Demodulator Output Waveforms

modem transmits at a carrier frequency of 16.875 MHz and receives at 21.375 MHz (Figure 2-3); conversely, the data buffer modem transmits at 21.375 MHz and receives at 16.875 MHz. Both data modems operate at a data rate of 2.25 Mb/s. Figure C-6 shows the physical size of a finished TPM/DPSK modem. Since both modems have the same construction, only the data buffer modem is described in this report.

C.2.1 Data Buffer Modulator

Figure C-7 is a simplified block diagram of the 21.375-MHz data buffer TPM/DPSK modulator. In the modulator, the carrier frequency is generated from a crystal-controlled sine wave oscillator. Because data service is time-shared by all subscribers connected to the cable, the data buffer modulator can transmit only during its allocated time slot. For this reason, the carrier signal is fed first through a gate-controlled amplifier so that the signal can be switched on/off in accordance with a control command, called the L control, issued from the data buffer. In the data poller modem, L control is not used because this modem must transmit continuously.

First-amplifier differential outputs are applied to a phase splitter network consisting of three phase shifters. Three phases are derived from this network, each being separated from the other

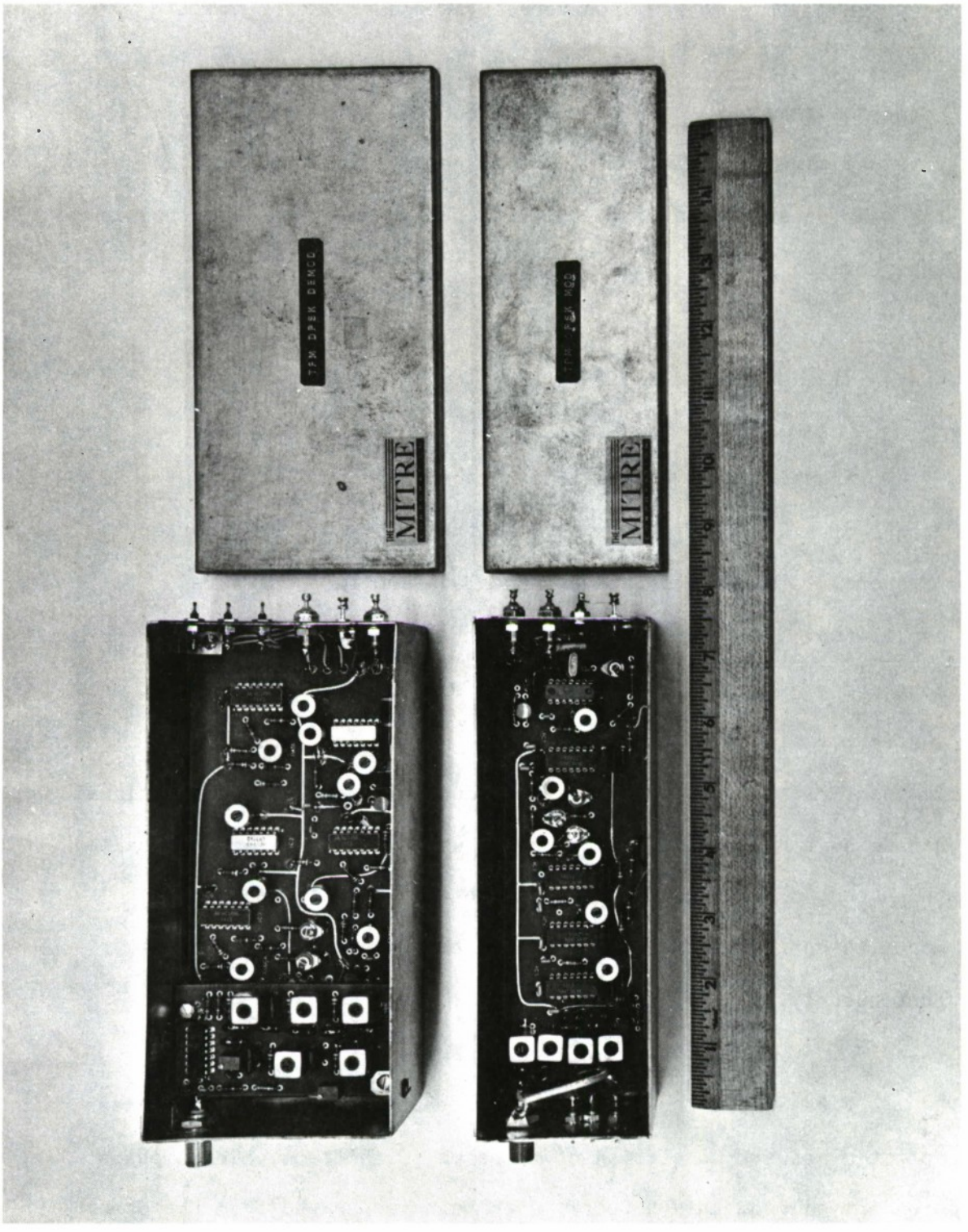


Figure C-6. TPM/DPSK Modem

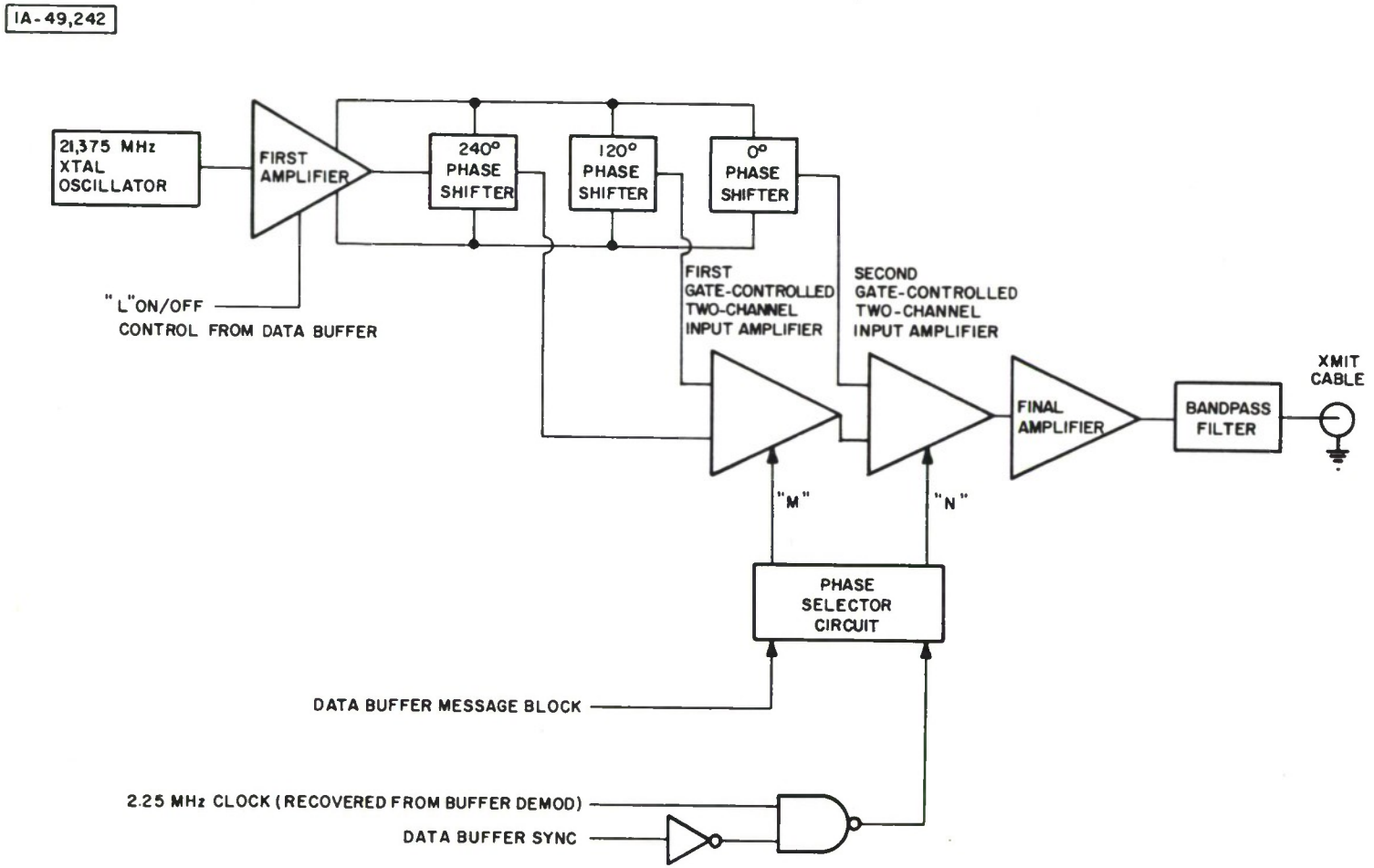


Figure C-7. Data Buffer TPM/DPSK Modulator (21.375 MHz)

by 120°. (Hereafter, these phases will be referred to as 0°,120° and 240°). Signals at 120° and 240° are supplied from the phase network to the first gate-controlled two-channel input wideband amplifier. The output of this amplifier (120° or 240°), and a 0° signal from the phase network are applied to a second gated amplifier, and the output of the second gated amplifier is applied to a final amplifier stage. The output of this final stage, after proper filtering, is connected to the tranmsit cable at an amplitude of 200 mV rms (46 dBmV). Phase selection is accomplished by operating the gates of the two-channel input amplifiers in a proper sequence as determined by the phase selector circuit (by two control leads called M and N) and its input clock, sync and data.

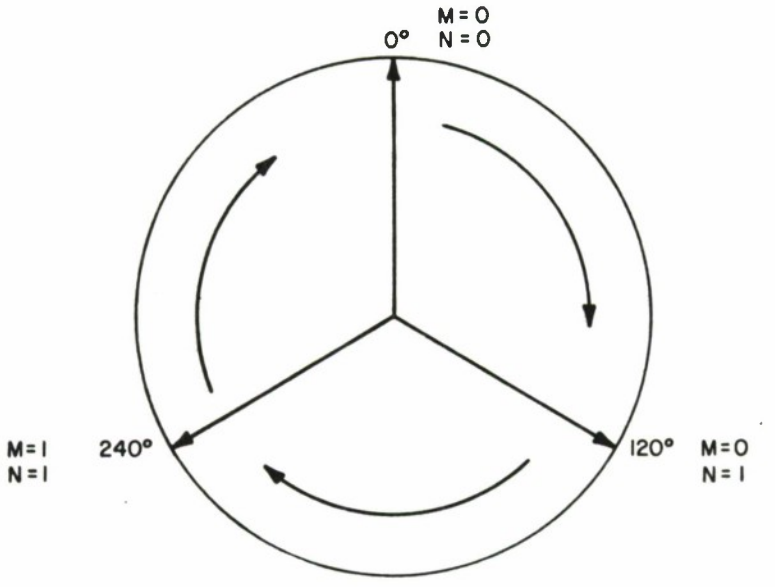
All phase selection is determined by the phase selector circuit and its two output control leads M and N. The M lead controls the selection of 120° or 240° at the first gate-controlled amplifier. The N lead controls the second gate-controlled amplifier and selects either 0° phase or the phase selected by the first gate-controlled amplifier. With the N lead low (TTL logic levels), the phase selected during the data bit period will always be 0° irrespective of the M lead level. With the N lead high, the phase selected will be 120° if M is low and 240° if M is high.

The M and N levels determined by the logic in the phase selector circuit are designed in such a way that whenever the data

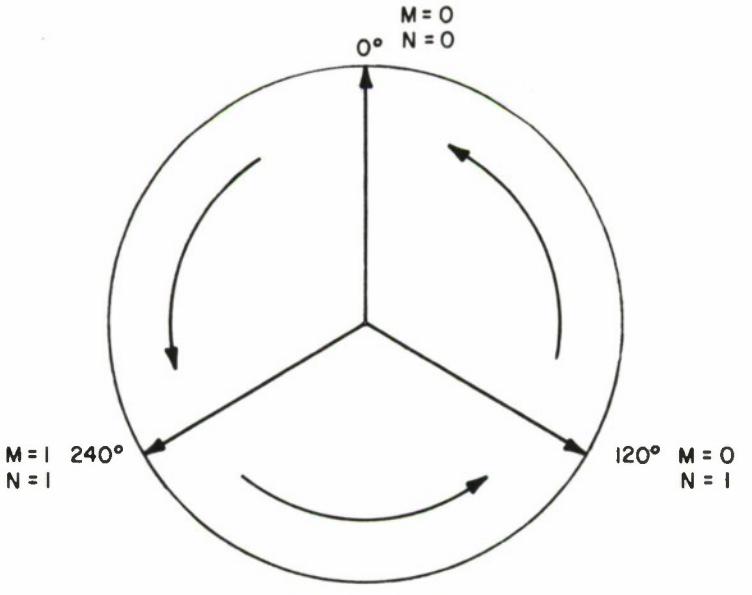
bit is low (or 0) the phase selection is advanced by 120°, and whenever the data bit is high (or 1) the phase selection is retarded by 120°. Thus, for a continuous data stream of all logic 0s, the phase selector will produce an M and N output sequence of 00, 01, 11, 00, 01, 11, etc. This corresponds to a clockwise rotation in the state transition of M and N levels as shown in Figure C-8(a). Similarly, for a data stream of all 1s, the output sequnce will be 00, 11, 01, 00, 11, 01, etc., corresponding to a counterclockwise rotation in the M and N state transition as shown in Figure C-8(b).

In the MIDS transmission format, each data message block is preceded by a synchronization period. During this sync time, the 2.25-MHz clock is inhibited from driving the phase selector circuit. This results in the input selection (via the M and N leads) to the first and second gate-controlled amplifiers remaining constant, causing the same phase selection for two or more consecutive clock periods.

Oscilloscope displays of phase selector circuit input/output signals are shown in Figures C-9 through C-11, which display the all logic low, all logic high, and random data conditions respectively. Note that where the clock is inhibited, the same MN combination will repeat until the clock is resumed. Repeated MN outputs will maintain the same phase for more than one clock period, allowing a sync pulse to be detected at the TPM/DPSK demodulator.



(a) Continuous Logic Zeros or All Low Data From Data Source Results in Phase Shifts in a Clockwise Rotation



(b) Continuous Logic Ones or All High Data From Data Source Results in Phase Shifts in a Counter Clockwise Rotation

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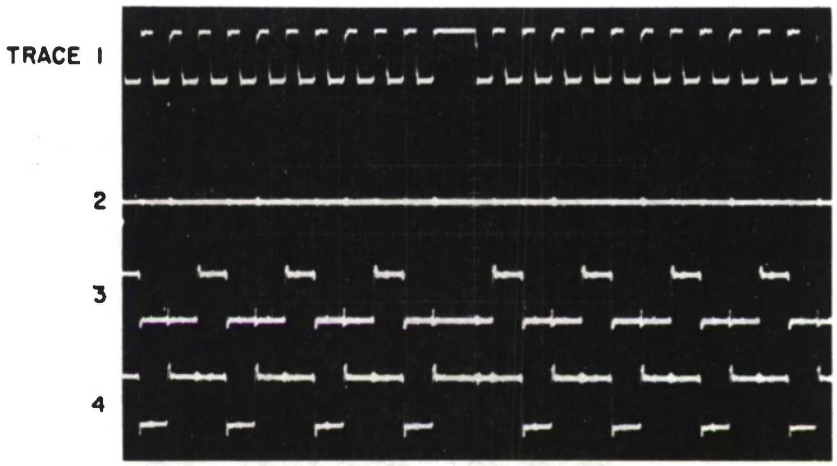
Figure C-8. State Transition in Phase Selector Circuit



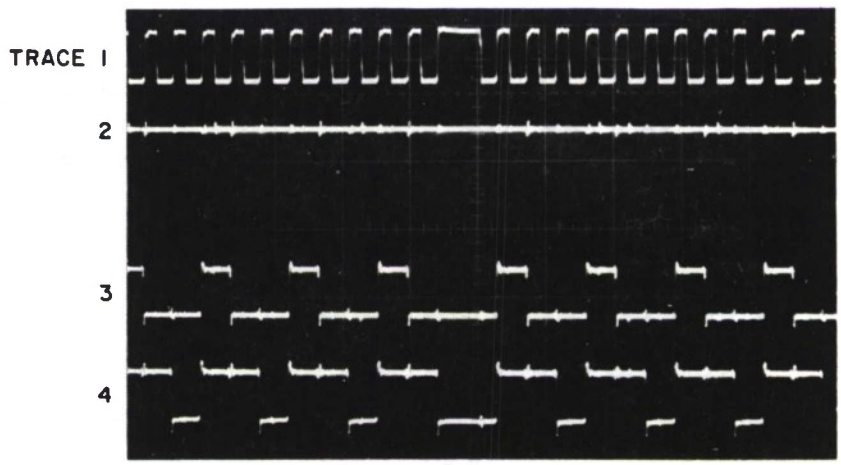
SWEEP RATE, 1.0μs/cm; AMPLITUDE, 5 v/cm

1. 2.25-MHz CLOCK INPUT TO PHASE SELECTOR
2. DATA INPUT (CONTINUOUS LOGIC LOW) TO PHASE SELECTOR
3. M OUTPUT OF PHASE SELECTOR
4. N OUTPUT OF PHASE SELECTOR

NOTE: MN REPEATS (01, 01) WHERE CLOCK IS INHIBITED.

IA-49,460

Figure C-9. Oscilloscope Display of Phase Selector Input/Output Signals with Input Data Continuous Logic Low

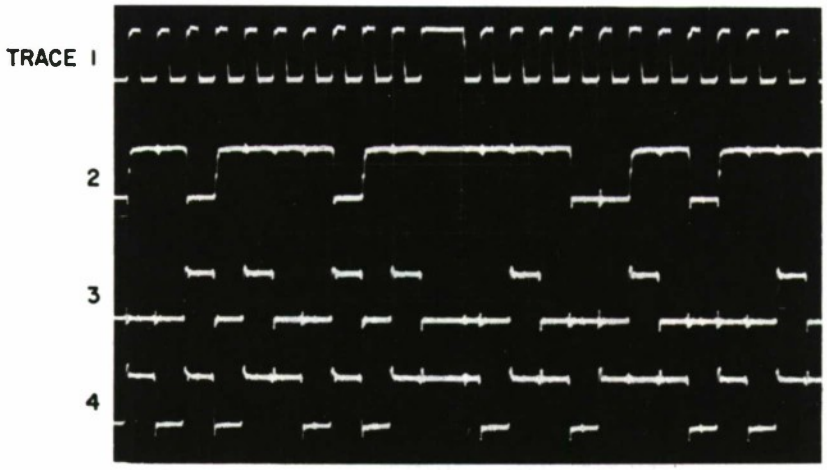


SWEEP RATE, 1.0 μs/cm; AMPLITUDE, 5 v/cm

1. 2.25-MHz CLOCK INPUT TO PHASE SELECTOR
2. DATA INPUT (CONTINUOUS LOGIC HIGH) TO PHASE SELECTOR
3. M OUTPUT OF PHASE SELECTOR
4. N OUTPUT OF PHASE SELECTOR

IA-49,461

Figure C-10. Oscilloscope Display of Phase Selector Input/Output Signals with Input Data Continuous Logic High



SWEEP RATE, 1.0 μs/cm; AMPLITUDE, 5 v/cm

1. 2.25-MHz CLOCK INPUT TO PHASE SELECTOR
2. DATA INPUT (RANDOM) TO PHASE SELECTOR
3. M OUTPUT OF PHASE SELECTOR
4. N OUTPUT OF PHASE SELECTOR

IA-49,462

Figure C-11. Oscilloscope Display of Phase Selector Input/Output Signals with Input Data Random

Finally, the gated RF signal is amplified and filtered through a 4-pole Butterworth filter with a 3-dB bandwidth of 4 MHz. Figures C-12 and C-13 show the TPM/DPSK modulator output before and after the bandpass filter.

C.2.2 Data Buffer Demodulator

Figure C-14 is a simplified block diagram of the 16.875-MHz data buffer TPM/DPSK demodulator. As shown, the demodulator input signal is amplified and then filtered through a 5-pole Bessel bandpass filter with a 3-dB bandwidth of 3 MHz. The filtered signal is amplified again and then fed into three almost identical series

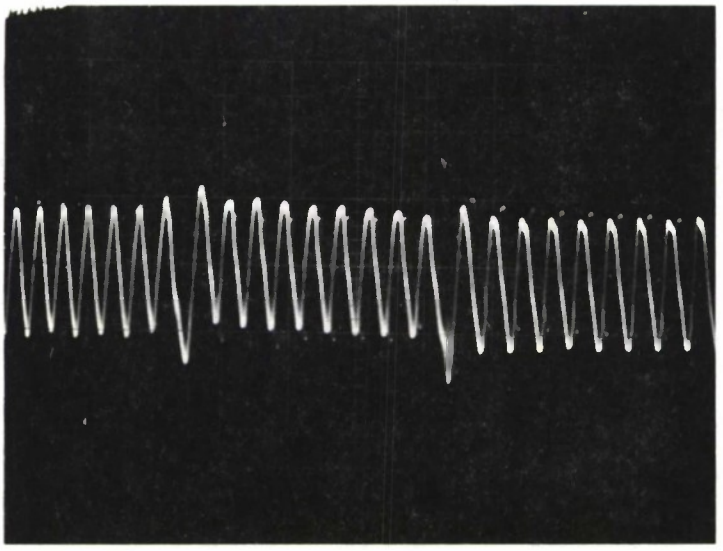


Figure C-12. Unfiltered TPM/DPSK Modulator Output (21.375-MHz Carrier Modulated at 2.25-Mb/s Rate)

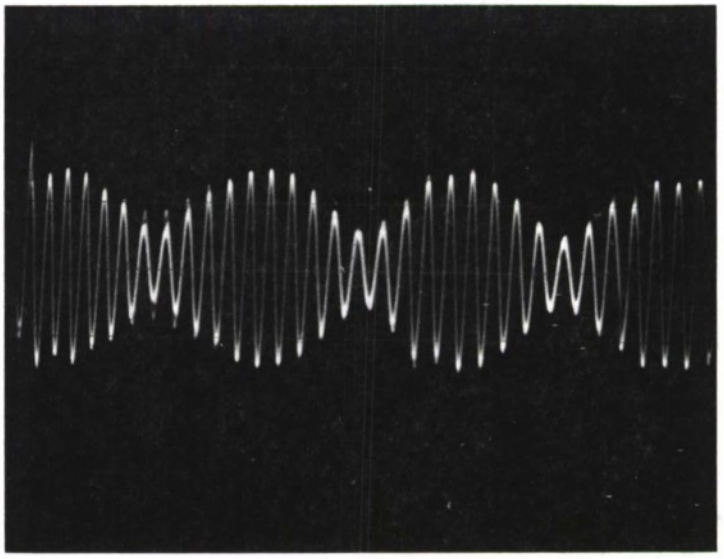


Figure C-13. Filtered TPM/DPSK Modulator Output (21.375-MHz Carrier Modulated at 2.25-Mb/s Rate)

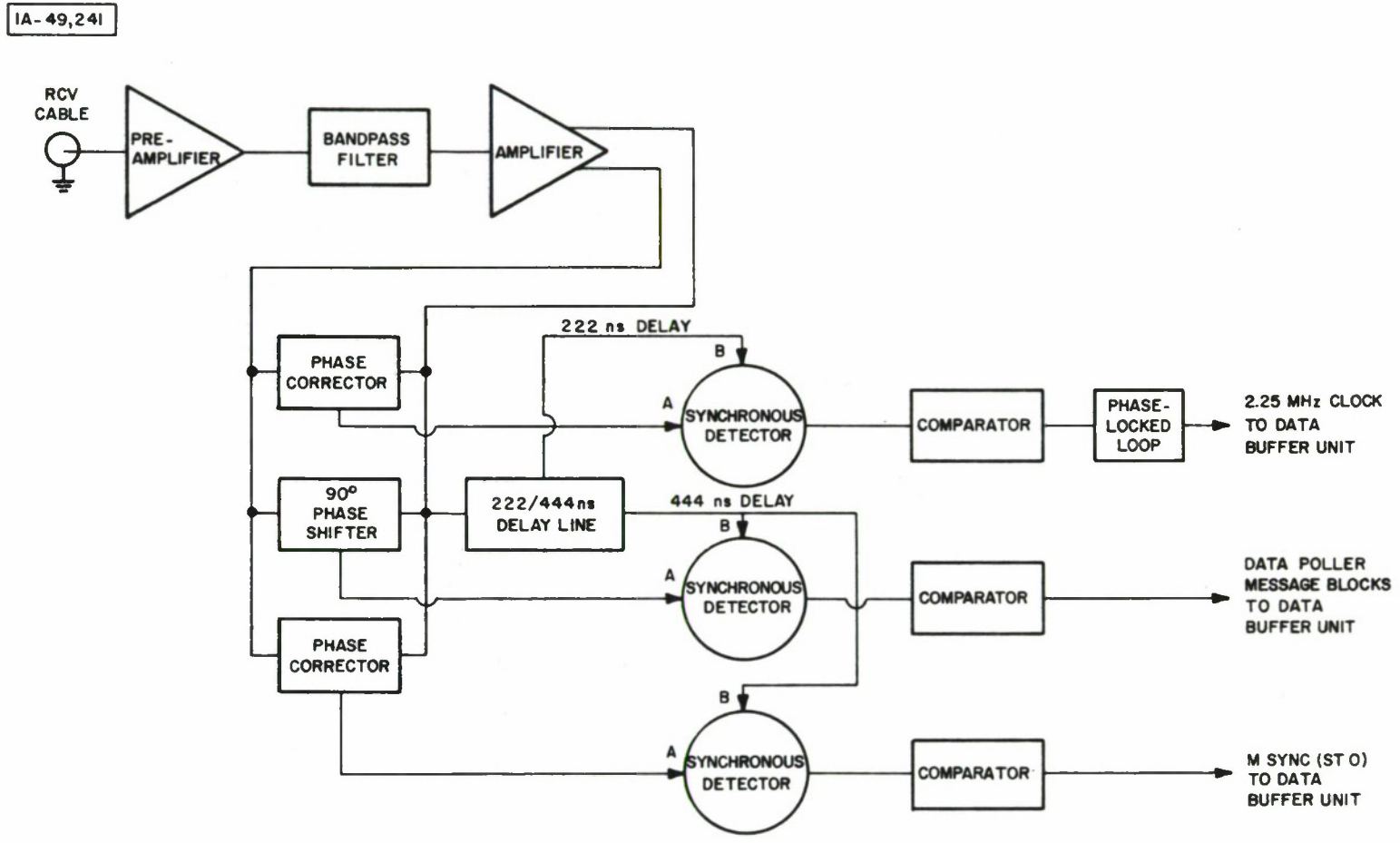


Figure C-14. Data Buffer TPM/DPSK Demodulator

of phase shifters, synchronous detectors, and comparators for the recovery of clock, data and sync.

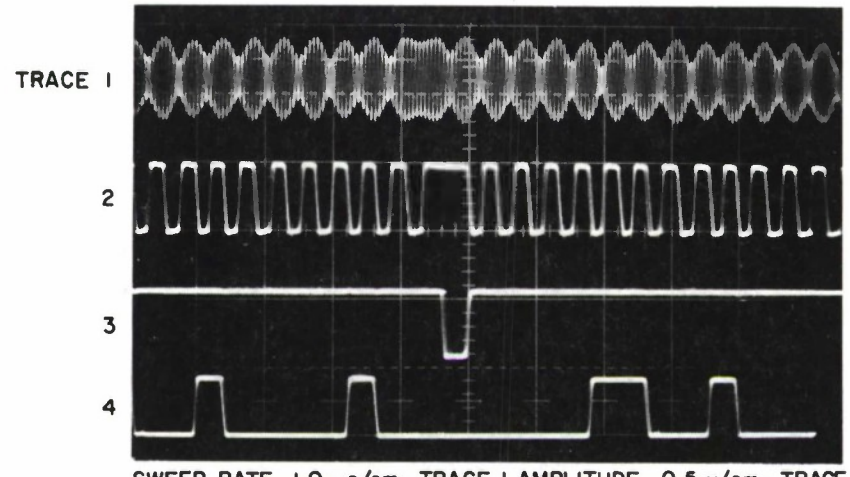
The synchronous detector operates on a mixing and filtering principle. If two signals of the same frequency applied on the A and B inputs to the synchronous detector are less than 90° apart, a positive output is produced, otherwise a negative output will result. The comparator circuit is used to adapt the detector output to TTL levels.

In the clock recovery circuit, one of the signals applied to the synchronous detector input is delayed by half of a data period or 222 nanoseconds (ns). This 1/2-bit delay is accomplished by employing a full period delay line (444-ns delay) that has a center tap. The phase difference between the two inputs to the detector will be 0° for one-half of the data period and 120° for the other half of the period, thus producing an alternating detector output at the data bit rate. The recovered clock output is connected to a phase-locked loop circuit to shape the clock waveform further and eliminate the timing jitter before it is sent to the data buffer unit. The phase-locked loop circuit is not used in the data poller demodulator because of possible timing incompatibility among the subscribers.

In the data and sync recovery circuits, one of the detector inputs is delayed by one full data period in order to allow phase comparison between two successive periods. For data recovery, because the phase difference between successive periods will be either plus or minus 120° depending on whether the data is low or high, one of the detector inputs is shifted further by 90° for proper detection.

Sync recovery is based on the fact that the same phase is maintained for more than one data period during the sync period preceding the data message block. Therefore, the phase difference in two successive periods will be zero only during the sync period, and the detector will produce a sync pulse output equivalent in duration to one less the total number of clock periods inhibited during the sync period.

Figures C-15 and C-16 show the waveforms at the demodulator outputs. Trace 1 shows the analog signal as it leaves the modulator. Its level is approximately 600 to 700 mV peak-to-peak. The analog signal at the demodulator input will be identical except that it will be attenuated to an amplitude of approximately 3.0 mV peak-to-peak. Demodulator outputs are identical in Figures C-15 and C-16, except that the clock signal in Figure C-16 has been connected to a phase-locked loop resulting in the elimination of all clock jitter along with the reinsertion of clock pulses originally

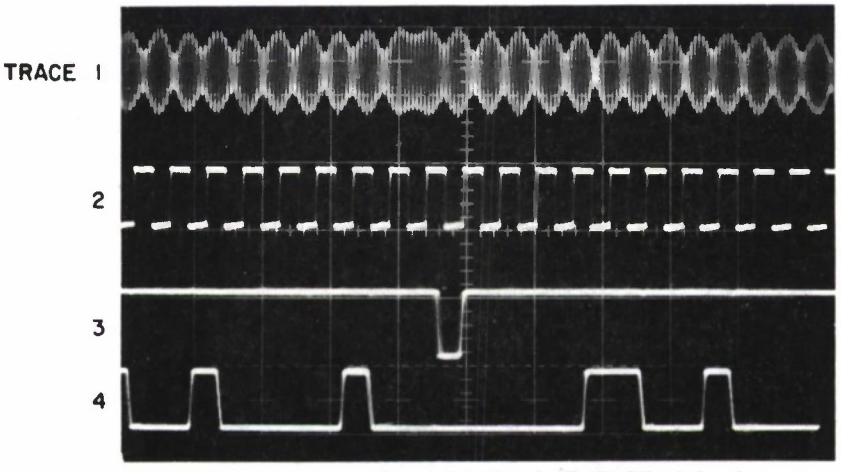


SWEEP RATE, 1.0 μs/cm; TRACE 1 AMPLITUDE, 0.5 v/cm; TRACE 2,3,4 AMPLITUDE, 5 v/cm

1A-49,463

1. MODULATOR OUTPUT SIGNAL CONNECTED TO TRANSMIT CABLE
2. 2.25-MHz CLOCK AT OUTPUT OF COMPARATOR
3. MESSAGE BLOCK SYNCHRONIZATION PULSE FROM DEMODULATOR OUTPUT
4. DATA RECOVERED FROM DEMODULATOR OUTPUT

Figure C-15. Oscilloscope Display of Data Modem Output Signals



SWEEP RATE, 1.0 μs/cm; TRACE 1 AMPLITUDE, 0.5 v/cm; TRACE 2,3,4 AMPLITUDE, 5 v/cm

1A-49,464

1. MODULATOR OUTPUT SIGNAL CONNECTED TO TRANSMIT CABLE
2. 2.25-MHz CLOCK AT OUTPUT OF PHASE-LOCKED LOOP
3. MESSAGE BLOCK SYNCHRONIZATION PULSE (1-BIT INTERVAL) FROM DEMODULATOR OUTPUT
4. DATA RECOVERED FROM DEMODULATOR OUTPUT

Figure C-16. Oscilloscope Display of Data Modem Output Signals (Clock Signal Connected to Phase-Locked Loop)

inhibited during the sync period. Both figures correspond to the random data pattern transmitted in Figure C-11.

C.3 PREDICTED AND MEASURED PERFORMANCE

The S&S and data modems were built and tested in a laboratory environment, and both types of modems operate well within the signal level specifications adopted for the MICOM cable system. Aside from signal level considerations, additional effort was made to examine in more detail the spectrum utilization of both modems for possible mutual interference in a multimode operation. The results of this examination are presented in the following subsections.

C.3.1 S&S Modem Performance

Measured S&S modem performance for the transmitter is:

a. Operating frequency: 12.8 MHz (poller)
   13.6 MHz (subscriber),
b. Output level: max. 1V peak-to-peak,
c. Modulation scheme: on-off keying,
d. Keying rate: max. 50 kilobauds,
e. Modulation control level: TTL compatible,
f. On/off ratio: Better than 56 dB, and
g. Output harmonic levels: All harmonics
   > 60 dB down from carrier;

and for the receiver is:

a. Operating frequency: 12.8 MHz (subscriber)
   13.6 MHz (poller),
b. Output level: max. 1V peak-to-peak,
c. Receive level range: min. 0.7 mV rms, max. 20 mV rms, and
d. Output data level: TTL compatible.

Note that the S&S modem transmitter output is relatively free from harmonics. (All harmonics are more than 60 dB below carrier level.) Spectral occupancy of the on-off keying modulation (for a repetitive 1010 data pattern) follows the classical sin x/x distribution (Reference 21). Figure C-17 shows the S&S modem transmitter output spectrum as recorded on a Hewlett-Packard 8553B Spectrum Analyzer. This agrees closely with the theoretical prediction summarized in Table C-1.

Error performance of the S&S modem also is predictable according to the principle of on-off keying. For example, at the E_b/No (energy-per-bit to noise spectral-density) ratio of 17 dB, the error rate would be 10^{-6} (Reference 22). However, in the present application thermal noise interference is much less severe than adjacent channel interference. For this reason, error performance of the S&S modem in the presence of thermal noise interference was not measured. Instead, the modem receiver bandwidth was determined by injecting a 20-dBmV CW (continuous wave) signal at the receiver

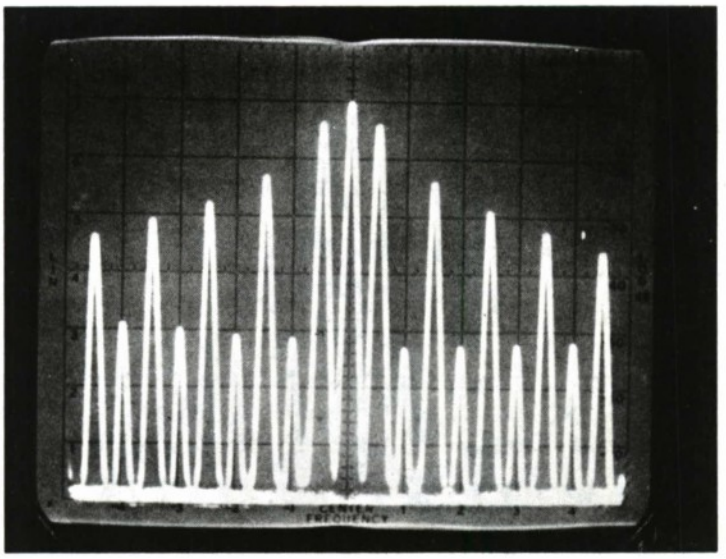


Figure C-17. S&S Modem Transmitter Output Spectrum (13.6-MHz Carrier Modulated by 1010 Data Pattern at 50-Kiloband Rate, Analyzer Scan Width = 50 kHz/div)

TABLE C-1

PREDICTED AND MEASURED SPECTRAL LEVELS FOR THE S&S MODEM TRANSMITTER

Side Band	dB Level Below Carrier	
	Predicted	Measured
0 (13.6 MHz Carrier)	-	-
1 (13.625 MHz)	3.9	4
3 (13.675 MHz)	13.5	14
5 (13.725 MHz)	17.9	18
7 (13.775 MHz)	20.8	22
9 (13.825 MHz)	23.0	24

input and noting the absence of receiver output at CW frequencies beyond a particular range. The receiver bandwidth for both the poller and subscriber S&S modems is about ±220 kHz around the carrier frequency. This indicates that S&S modems are relatively immune to adjacent channel interference within the present MIDS spectrum allocation scheme.

C.3.2 Data Modem Performance

Measured data modem performance for the transmitter is:

a. Operating frequency: 16.875 MHz (poller), 21.375 MHz (subscriber),
b. Output level: max. 1 V peak-to-peak,
c. Modulation scheme: TPM/DPSK,
d. Data rate: max. 2.5 Mb/s,
e. Modulation control level: TTL compatible,
f. On/off ratio: 20 dB, and
g. Output harmonic levels: > 50 dB below unmodulated carrier level;

and for the receiver is:

a. Operating frequency: 16.875 MHz (subscriber), 21.375 MHz (poller),
b. Receiver bandwidth: 4 MHz at 3-dB point,

c. Receiver sensitivity: min. 0.5 mV rms, max. 20 mV rms, and

d. Output levels: TTL compatible for data, clock and sync outputs.

Because of its novelty, the data modem's spectral characteristics were the subject of a documented theoretical study (References 19 and 20). As an example of the validity of this study, the spectral distribution of the TPM/DPSK modulator output prior to the 4-pole Butterworth filter as recorded by the spectrum analyzer is snown in Figure C-18. When this distribution is compared with the documented theoretical prediction summarized in Table C-2, it can be seen (within the accuracy of observation) that there is good agreement between the predicted and measured spectral levels.

The TPM/DPSK modem, like any other phase modulation modem, typically occupies a wide spectrum bandwidth. In order to avoid adjacent channel interferance, it is necessary to filter the modulated signal before transmission. Figures C-19(a) and C-19(b) show the TPM/DPSK modulated signal spectrum before and after the transmission filter. It can be seen that the filtering characteristics do correspond to the 4-MHz bandwidth and 24 dB per octave attenuation behavior designed for the 4-pole Butterworth filter.

TABLE C-2

PREDICTED AND MEASURED SPECTRAL LEVELS FOR THE DATA MODEM

Component Frequency (MHz)	dB Relative to Carrier Level	
	Predicted	Measured
12.9375	-12.0	-12.0
13.5000	-5.0	-0.8
14.0625	-9.4	-8.2
15.1875	-5.2	-8.6
15.7500	5.3	6.4
16.3125	4.0	3.8
16.8750	0	0
17.4375	3.7	3.8
18.0000	5.9	5.6
18.5625	-6.1	5.4
19.6875	-10.8	-8.8
20.2500	3.2	-4.4
20.8125	-14.0	12.4

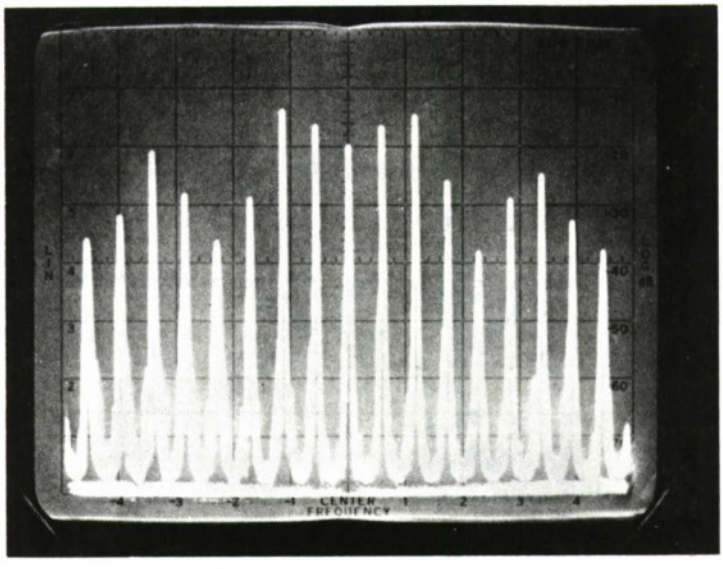
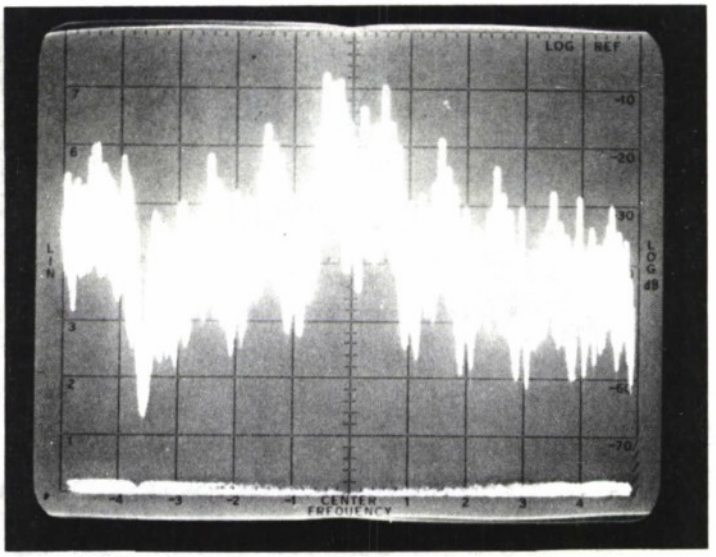


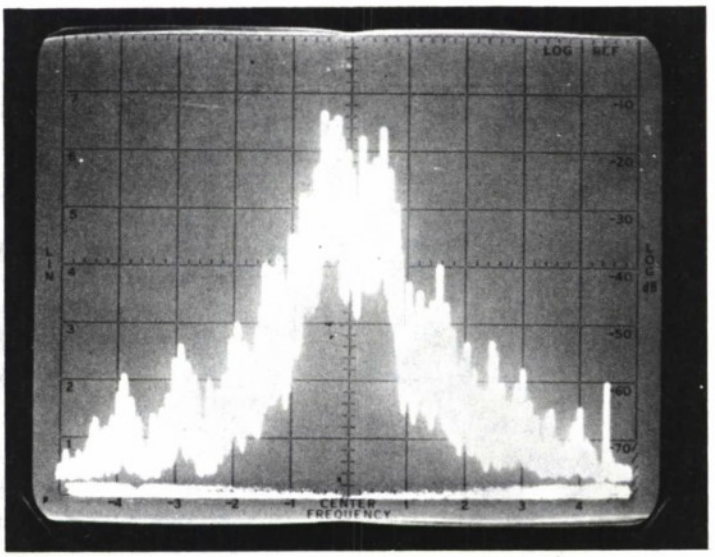
Figure C-18. TPM/DPSK Modulated Signal Spectrum Prior to Transmit Filter (16.875-MHz Carrier Modulated by 11001100 Data Pattern at 2-Mb/s Rate, Analyzer Scan Width = 1 MHz/div)

Error performance of the data modem has also been studied (Reference 19). According to the theoretical prediction, for a typical bit error rate specification of 10 the minimum required signal-to-noise ratio for the three-phase encoding is around 14 dB. Unfortunately, due to lack of adequate error measurement equipment, this error performance of the data modem has not been verified in the laboratory.

Finally, to provide a panoramic view of the spectrum occupancy of all MIDS modems, Figures C-20 and C-21 show the spectral distribution of all four transmitting modems (carrier frequencies at 12.8 MHz, 13.6 MHz, 16.875 MHZ and 21.375 MHz), fully



(a) Before Transmission Filter



(b) After Transmission Filter

Figure C-19. TPM/DPSK Modulated Signal Spectrum (16.875-MHz Carrier Modulated by 16-Bit Shift-Register-Generated Pattern at 2-Mb/s Rate, Analyzer Scan Width = 2 MHz/div)

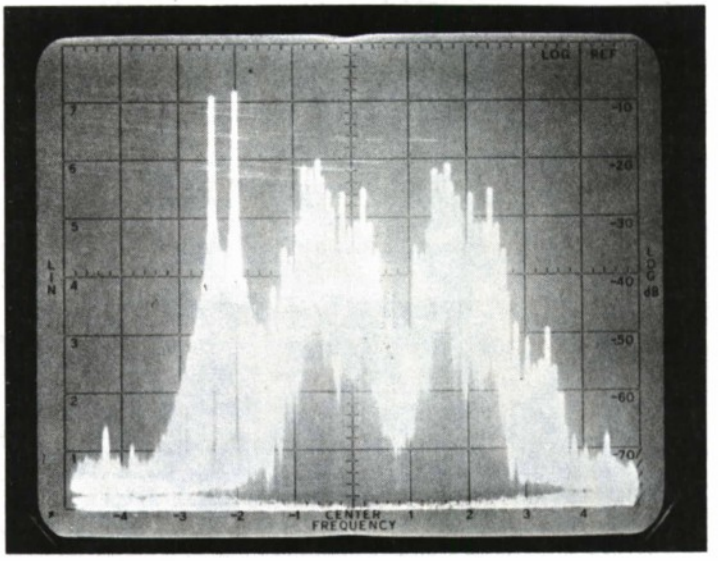


Figure C-20. Spectral Distribution of All Four MIDS Modems Fully Modulated (S&S Modems Modulated by 9-Bit Shift Register Sequence, Data Modems Modulated by 16-Bit Shift Register Sequence, Analyzer Scan Width = 2 MHz/div)

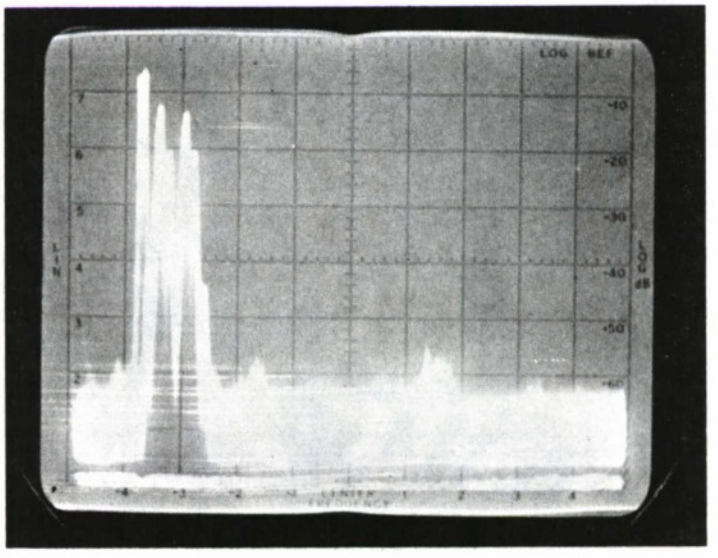


Figure C-21. Spectral Distribution of All Four MIDS Modems Fully Modulated (Analyzer Scan Range = 0-110 MHz to Show Harmonic Levels Outside MIDS 12-24 MHz Band, Log Scale = 10 dB/div)

modulated by pseudo-random sequences with unmodulated carrier levels all adjusted originally to the 46-dBmV level. The noticeable carrier dip in the data modems is a typical characteristic of TPM/DPSK modulation.

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GLOSSARY OF TERMS

AMPLITUDE SHIFT KEYING (ASK) - A modulation scheme in which changes in the amplitude of the carrier are used to convey digital information. On-off keying is a form of binary ASK where the carrier is switched on or off.

ADAPTIVE DATA SUBSYSTEM - A subsystem that implements a scheme to automatically jump (adapt) from a low idle rate to a burst rate upon demand from a subscriber's data buffer unit. It is thus a scheme to share total system capacity and is transparent to the subscriber's involvement. It consists of the data poller unit and the multiplicity of subscriber data buffer units.

CRT TERMINAL - A cathode ray tube terminal for reception and display of coded data in alphanumeric form, possibly with graphics and video information, and usually accompanied by a keyboard device for the transmission of information by the user.

DATA ADDRESSES - Same as DATA CHANNEL ADDRESSES

DATA BUFFER MESSAGE BLOCK - A group of 87 bits containing a synchronization pulse, receiver address, and 64-bit message with parity bits. The data buffer message block originates at the subscriber data buffer.

DATA BUFFER MESSAGE BLOCK SYNCHRONIZATION PULSE - First two bits of a data buffer message block.

DATA BUFFER TPM/DPSK MODEM - A modulator transmitting on a frequency of 21.375 MHz and a demodulator receiving on 16.875 MHz.

DATA BUFFER UNIT - Same as SUBSCRIBER DATA BUFFER UNIT

DATA CHANNEL - A pair of frequency bands, each 4-MHz wide, allocated for data transmission in the MIDS adaptive data subsystem. See Figure 2-3.

DATA CHANNEL ADDRESSES - An address pair assigned to the subscriber data buffer unit, wherein the transmitter responds to data polls coded with the transmit address and the receiver accepts messages preceded with the coded receive address. These addresses are assigned by the network control computer as the result of a subscriber request for connectivity. The data addresses are conveyed to the subscriber data buffer via the S&S system. These addresses are sometimes referred to as indirect addresses.

DATA FRAME - A sequence of 32 data polling cycles, each polling cycle consisting of 64 polls. See also DATA POLLING CYCLE. A data frame (for data polling) is not to be confused with a time frame, which is defined for S&S message transmission.

DATA PACKET - A group of contiguous bits (of fixed length) forming a portion of a digital message. The MIDS data packet consists of 64 bits.

DATA POLLER UNIT - A unit that emanates a sequence of polls to allow subscriber data buffers to transmit data buffer message blocks. It consists also of a retimer buffer, high-speed/low-speed poller, system timer, high-speed queue, and data poller microprocessor.

DATA POLLER MESSAGE BLOCK - A group of 104 bits containing a synchronization pulse, polling address, receiver address, and 64-bit message with parity bits.

DATA POLLER MESSAGE BLOCK SYNCHRONIZATION PULSE - First two bits of data poller message block preceding the polling address. Also referred to as state zero (0).

DATA POLLER TPM/DPSK MODEM - A modulator transmitting on a frequency of 16.875 MHz and a demodulator receiving on 21.375 MHz.

DATA POLLING CYCLE - A block of 32 low-speed data polls interspaced with 32 high-speed polls, i.e., a total of 64 polls.

DATA SUBSYSTEM - Same as ADAPTIVE DATA SUBSYSTEM

DEMODULATOR - See MODULATOR

DIRECTORY ADDRESS - A unique address code assigned to each subscriber keypad control unit. Up to 16,384 directory addresses may be accommodated in MIDS.

DIFFERENTIAL PHASE SHIFT KEYING (DPSK) - A modulation scheme in which consecutive phases of the carrier are compared to make logical decisions.

FIRMWARE - The instructions governing the operation of the processor, implemented or stored in a fixed memory, usually called read-only memory (ROM).

FLAG-FOR-SERVICE - A pulse raised in a unique time slot by the subscriber's action of depressing any key. This signals the network control computer (NCC) to poll that subscriber unit in order to collect keystroke "dialing" information.

FLAG-FOR-SERVICE FIELD - A contiguous sequence of 256 pulses, each defining a unique time slot dedicated to a single subscriber. Sixty-four such fields are contained within a time frame. This allows unique slot assignments for 16,384 subscribers in which each may raise a flag to signal the network control computer for service. See Figure 2-4.

FREQUENCY DIVISION MULTIPLEXING (FDM) - A multiplexing scheme in which modulated information signals are carried on a common medium, with each signal occupying a segment of the available frequency spectrum with enough separation to avoid undue interference.

INDIRECT ADDRESS - Same as DATA CHANNEL ADDRESS

KEYPAD CONTROL UNIT - Same as SUBSCRIBER KEYPAD CONTROL UNIT

L CONTROL - On-off control lead for data buffer modulator.

M&N LEADS - Phase-select control leads for data poller and data buffer modulators.

MICROPROCESSOR - A collection of large-scale integrated circuits capable of performing logical and arithmetic operations on a variety of input signals, thus controlling output signals. The operations of the processor are governed by an associated stored program.

MODEM - A contraction of MODULATOR and DEMODULATOR. A physical unit that contains both a modulator (transmitter) and a demodulator (receiver) to carry on a two-way information exchange.

MODULATOR - A device which changes some aspect of a carrier wave in accordance with an information signal and transmits the resulting

waveform into a distribution medium. In MIDS, modulators transmit S&S signals and digital data on a coaxial cable at specified frequencies. In order to carry on a two-way conversation, each subscriber unit is equipped with a modulator to transmit information and a demodulator to receive information. A demodulator works in the reverse of a modulator, i.e., it strips away the carrier frequency and recovers or reconstructs the original digital information.

NETWORK CONTROL COMPUTER (NCC) - A minicomputer employed to process connectivities as requested by subscribers, and also to continually interrogate all subscriber keypad control units to keep current subscriber information regarding their operational status.

ON-OFF KEYING - See AMPLITUDE SHIFT KEYING

POLL - A coded address which prompts a device with that specific address to respond with some type of information transmission.

POLLING CYCLE - Same as DATA POLLING CYCLE

RECEIVE CABLE - A unidirectional cable attached to receivers (demodulators) only. It is connected to the transmit cable only at one point, the headend.

S&S CHANNEL - A pair of frequency bands, each 100-KHz wide, allocated for S&S message transmission in the MIDS S&S subsystem. See Figure 2-3.

S&S KEYPAD CONTROL UNIT - Same as SUBSCRIBER KEYPAD CONTROL UNIT.

S&S MESSAGE BLOCK - The combination of one flag-for-service field (256 bits) and one S&S message field (72 bits). There are 64 such S&S message blocks in a time frame. See Figure 2-4.

S&S MESSAGE FIELD - A contiguous sequence of six 8-bit characters, each with start, parity, and two stop bits, totalling 72 bits. The network control computer uses this message field to poll subscribers for keystroke information and to convey information to the subscriber regarding call connectivity. See Figure 2-4.

SIGNALING AND SUPERVISION (S&S) - A network control scheme consisting of control signals from subscriber units to the network control computer, and vice-versa, that establish desired connectivity.

S&S POLLER MODEM - A modulator transmitting on a frequency of 12.800 MHz and a demodulator receiving on 13.600 MHz.

S&S SUBSCRIBER MODEM - A modulator transmitting on a frequency of 13.600 MHz and a demodulator receiving on 12.800 MHz.

S&S SUBSYSTEM - The S&S subsystem functions to establish desired connectivity of the many services desired by the subscribers. Comprised of the network control computer, with its associated S&S poller unit, and the multiplicity of subscriber keypad control units.

S&S POLLER UNIT - A unit which originates the flag-for-service bit stream and directs control messages between subscriber keypad control units and the network control computer. It is collocated with the NCC.

SUBSCRIBER DATA BUFFER (SDB) UNIT - Actually a subunit (contained within the subscriber unit) which handles the transfer of data between the subscriber's data terminal device and the communication medium.

SUBSCRIBER KEYPAD CONTROL UNIT - Actually a subunit (contained within the subscriber unit) which interrogates the keypad and communicates with the network control computer (NCC), and transfers data addresses (indirect addresses) to the collocated data buffer (sub)unit.

SUBSCRIBER TERMINAL - A device to allow the transmission or reception of information from and to a human operator. It includes such devices as teletypes, CRT terminals, line printers, audio and video devices.

SUBSCRIBER UNIT - An interface unit between the distribution medium (coaxial cable) and the subscriber's terminal device. It consists of the keypad control (sub)unit and data buffer (sub)unit. Sometimes referred to as the SUBSCRIBER INTERFACE UNIT.

TERMINAL - See SUBSCRIBER TERMINAL

TIME DIVISION MULTIPLE ACCESS (TDMA) - Interleaving several data messages, each with an address header, in a serial bit stream (which may be modulated) for later recovery by addressed receivers.

TIME FRAME - A contiguous sequence of 64 S&S message blocks. The time frame is delineated by a short frame gap of 960 microseconds.

THREE-PHASE MODULATION (TPM) - A variant of multiphase DPSK in which three phases are used to encode binary data. Binary states are distinguished by the advance or retardation of the carrier phase.

TRANSMIT CABLE - A unidirectional cable attached to all transmitters (modulators) only. It is connected to the receive cable at the headend.