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MANUFACTURING METHODS AND TECHNOLOGY ENGINEERING HIGH-EFFICIENCY, HIGH-POWER GALLIUM ARSENIDE READ-TYPE IMPATT DIODES

FINAL REPORT

30 June 1975 to 30 June 1977

VOLUME I

CONTRACT NO. DAAB07-75-C-0045

Prepared By

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A design review of Read profile IMPATT diodes is presented.

Work performed on this program to achieve the target specifications for high power X-band and Ku-band diodes is summarized. This includes development of specifications, processes, and characterization techniques for the Gallium Arsenide epitaxial wafer, as well as assembly and test procedures for the diode. Areas of investigation

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included epitaxial wafer growth processes, methods of controlling layer axial and radial uniformity, and techniques for testing the completed wafer. Schottky-barrier metallization and dimensional control techniques during plating, lapping and etching were the principal areas of investigation in the dice processing area.

Several novel techniques were applied to the manufacturing processes to improve the production rates of Read IMPATT diodes. This included spray dicing of the wafers, and new thermal resistance and noise measuring techniques.

Environmental test results are summarized, including storage and operating life test results during the program and on the final production units.

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MANUFACTURING METHODS AND TECHNOLOGY ENGINEERING
HIGH-EFFICIENCY, HIGH-POWER GALLIUM ARSENIDE
READ-TYPE IMPATT DIODES

FINAL REPORT

30 June 1975 to 30 June 1977

CONTRACT NO. DAAB07-75-C-0045

The object of this program was to develop a capability to manufacture High-Efficiency, High-Power Gallium Arsenide IMPATT Diodes meeting the description and specifications of Section F of the contract and the requirements of SCS-481.

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Waltham, Massachusetts 02154

PURPOSE

The objective of this program was to establish a capability to manufacture high-efficiency, high-power Gallium Arsenide IMPATT diodes at specified rates and yields. There are two diode types; one at X-band, and one at Ku-band which have the nominal characteristics listed below:

	X-Band	Ku-Band
Operating Frequency (GHz)	10.0 ±1.0	15.0 ±1.0
Power Output (Watts)	3.5 min.	2.5 min.
Conversion Efficiency (%)	20 min.	20 min.
Operating Junction Temperature (^{o}C)	200 max.	200 max.

Effort during the engineering phase was directed toward establishing production processes for both Gallium Arsenide epitaxial wafers and diode assembly and test. The wafers were designed to meet specifications which were dictated by the diode requirements and also for specific material characterization testing as specified in the contract. The diodes were designed to meet the detailed performance requirements outlined in SCS-481.

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SECTION I

DEVICE DESCRIPTION AND ANALYSIS - PROJECT HISTORY

1.0 DEVICE DESCRIPTION

1.1 Design Approach

The IMPATT diode is a two-terminal, solid-state negative resistance device used to convert applied DC electrical energy into microwave energy. The active zone of the usual IMPATT diode can be divided into two parts; the avalanche zone where bunches of current carriers are created by avalanche breakdown, and the drift zone where the carrier bunches interact with the DC and RF fields. If the thickness of the drift zone is properly chosen, the RF current in the external circuit will be 180°C out of phase with the RF voltage and the device will have a maximum negative resistance at the desired operating frequency.

The maximum conversion efficiency from DC to RF at the operating frequency then becomes approximately proportional to the ratio of the DC voltage across the drift zone to the total applied DC voltage. The larger the drift zone thickness relative to the total active zone thickness, the greater the available efficiency. For X or Ku-band devices having a uniform carrier concentration distribution (i.e., flat profile) throughout the active zone, the efficiency is limited because the avalanche zone occupies about one-quarter of the total active zone thickness. The drift zone width, therefore, cannot exceed three quarters of the total active zone thickness, and the drift voltage is limited to about one-half the breakdown voltage. The maximum achievable efficiency is, therefore, limited to considerably less than 20%.

In order to overcome this basic limitation, the relative width of the avalanche zone must be minimized. One method for accomplishing this is by shaping the doping profile following the basic prescription originally proposed by Read. Efficiencies and power output capabilities far exceeding those of conventional IMPATT diodes have been demonstrated using this approach.

The performance improvements which have been realized from the Read IMPATT diode are primarily due to the nature of the doping profile. Many of the characteristics of the diode are, therefore, built in during the growth of the epitaxial wafer from which it is manufactured. The natural frequency of oscillation and the maximum conversion efficiency are principally determined by the doping profile. The improved results are achieved with a more complex profile. Greater sophistication of processing competence is, therefore, required as well as a higher level of control relative to that required for simpler devices.

To utilize the performance potential from the wafer, new requirements are also imposed upon the diode manufacturing format, as well as upon the test and operating circuits. Because of the shallow doping spike, for example, new constraints have been imposed upon the metallization system which forms the Schottky barrier to prevent excessive consumption of surface Gallium Arsenide.

1.1.1 The Gallium-Arsenide Epitaxial Wafer

The process of growing gallium arsenide wafers with modified "Read" profiles was first developed at the Raytheon Research Division. The doping density distribution in Read profile wafers may have either a step or a narrow peak near the

surface barrier or junction. The former is known as the high-low (HL) profile, and the latter is known as the low-high-low (LHL) profile. Both are capable of yielding high-efficiency, high-power devices. Both serve to limit the width of the avalanche zone relative to the drift zone of the diode by shaping the electric field profile favorably. Our experience has shown the LHL Read to be more easily manufactured than the HL Read; hence, further discussion will be limited to it.

The electric field profile, and the doping profile of an idealized LHL Read diode are shown schematically in Figure 1-1. The symbols used in the figure are identified in Table 1-1. The wafer characteristics which most affect the device performance are: (1) the depth of the doping spike, X_p, (2) the integrated charge in the spike (Q) which is reflected as the magnitude of the field step ΔE, and (3) the carrier concentration of the drift zone, n_D. These wafer parameters determine the shape of the electric field profile in the operating diode. This in turn fixes the width of the depletion zone, X_D, which determines the natural frequency of the device. The electric field profile also determines the relative DC voltage across the drift zone and the total breakdown voltage, which together determine the maximum device efficiency.

1.1.2 The Read IMPATT Diode

The gallium arsenide wafer previously described may be considered an input material to the diode assembly operation which begins by the generation of several-hundred individual diode chips or dice from each wafer.

The dice fabrication procedure is based upon methods previously demonstrated at Raytheon, and a major engineering effort on this program was devoted to converting the

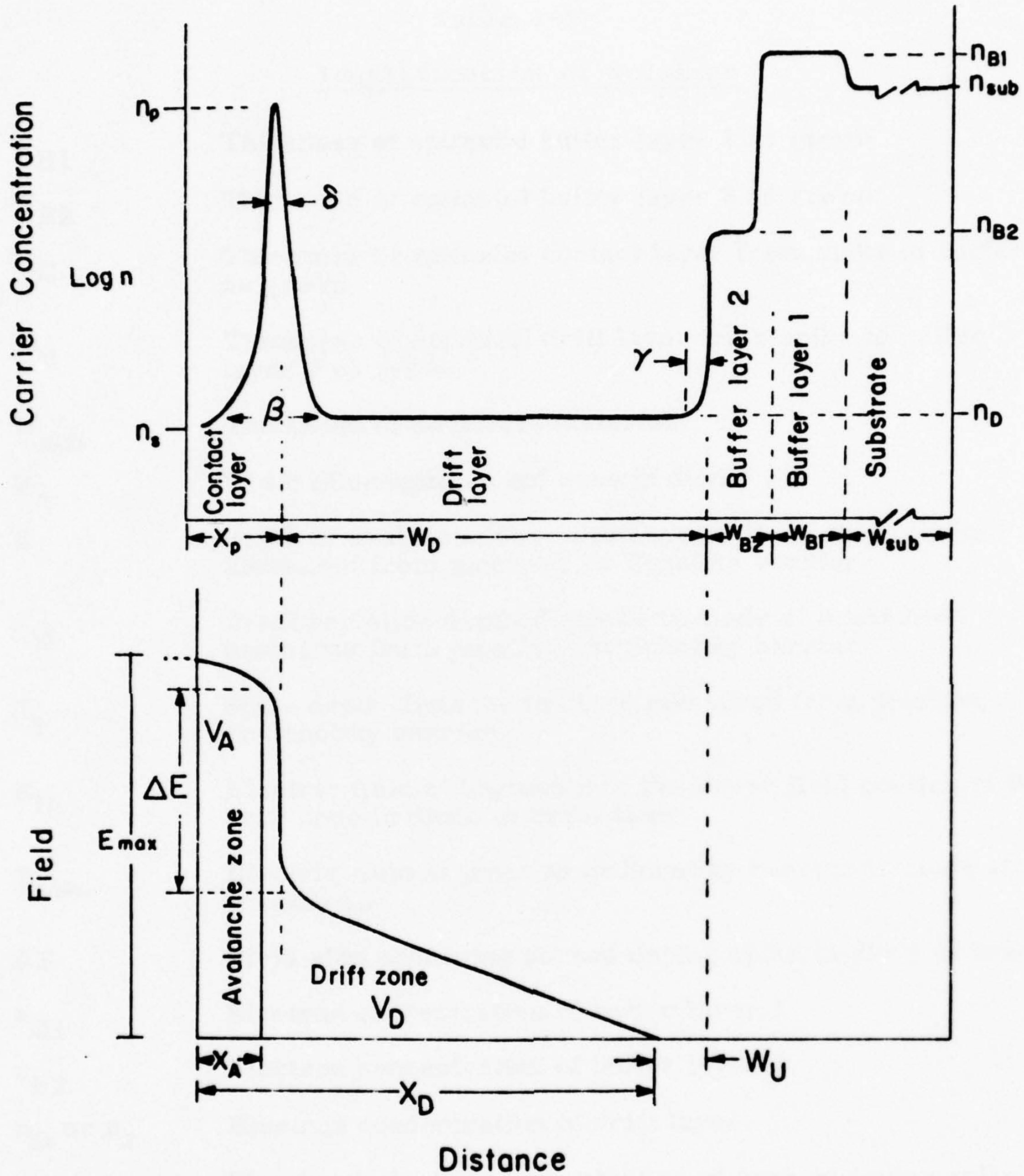

Figure 1-1 Schematic Representation of the Donor Density Profile and the Electric Field Profile of a Stepped Field (LHL) Read Diode. The notation used in this figure is identified in Table 1-1.

Table 1-1

Identification of Notation

Symbol	Definition
W_{B1}	Thickness of epitaxial buffer layer 1 as grown
W_{B2}	Thickness of epitaxial buffer layer 2 as grown
W_C	Thickness of epitaxial contact layer from spike to surface as grown
W_D	Thickness of epitaxial drift layer from spike to buffer layer 2 as grown
W_{sub}	Thickness of substrate material
W_u	Width of undepleted epi zone in diode
X_A	Depth of avalanche zone-distance in diode at breakdown measured from junction, or Schottky barrier
X_D	Total depletion depth-distance in diode at breakdown measured from junction, or Schottky barrier
X_p	Spike depth-distance in diode measured from junction, or Schottky barrier
E_D	Electric field at beginning of the linear field portion of the drift zone in diode at breakdown
E_{max}	Electric field at junction or Schottky barrier in diode at breakdown
ΔE	Field step occurring across doping spike in diode at breakdown
n_{B1}	Electron concentration of buffer layer 1
n_{B2}	Electron concentration of buffer layer 2
n_D or n_2	Electron concentration of drift layer
n_p	Measured electron concentration at peak of doping spike
n_{sub}	Electron concentration of substrate
n_o	Electron concentration measured with zero bias applied to junction or Schottky barrier
β	Base width of doping spike measured at 1.5 n_D
δ	Full width of doping spike measured at half height (0.5 n_p)
γ	Width of doping transition from drift layer to buffer layer 2

design already achieved to that required for production at the rates and yields specified. Several novel processes for improving performance, reducing cost, or enhancing reliability were implemented.

The gallium arsenide die is shown schematically in Figure 1-2.

The diode configuration is shown in cross section in Figure 1-3. The package is the Raytheon type 16A which is a hermetically-sealed microwave diode enclosure commonly used for this class of diode. The gallium arsenide chip has an integral heat sink which serves as the device anode and which is soldered to the pedestal of the package. Contact to the gallium arsenide cathode is by means of crossed gold wires thermocompression-bonded to the chip metallization and then bonded to the flange provided on the package. A lid which is welded to the flange hermetically seals the diode package after completion of diode assembly operations.

After assembly operations have been completed, the diodes are subjected to process conditioning and then to final testing. Process conditioning consists of subjecting the diodes to a series of environmental stresses during which assembly defects are likely to be detected. The devices failing are removed from the lot thereby improving the reliability of the surviving population.

Typically, a hermetic seal test is performed to remove leaky packages. The diodes are then subjected to elevated temperature storage to remove diodes which would potentially fail during early operation at normal temperatures.

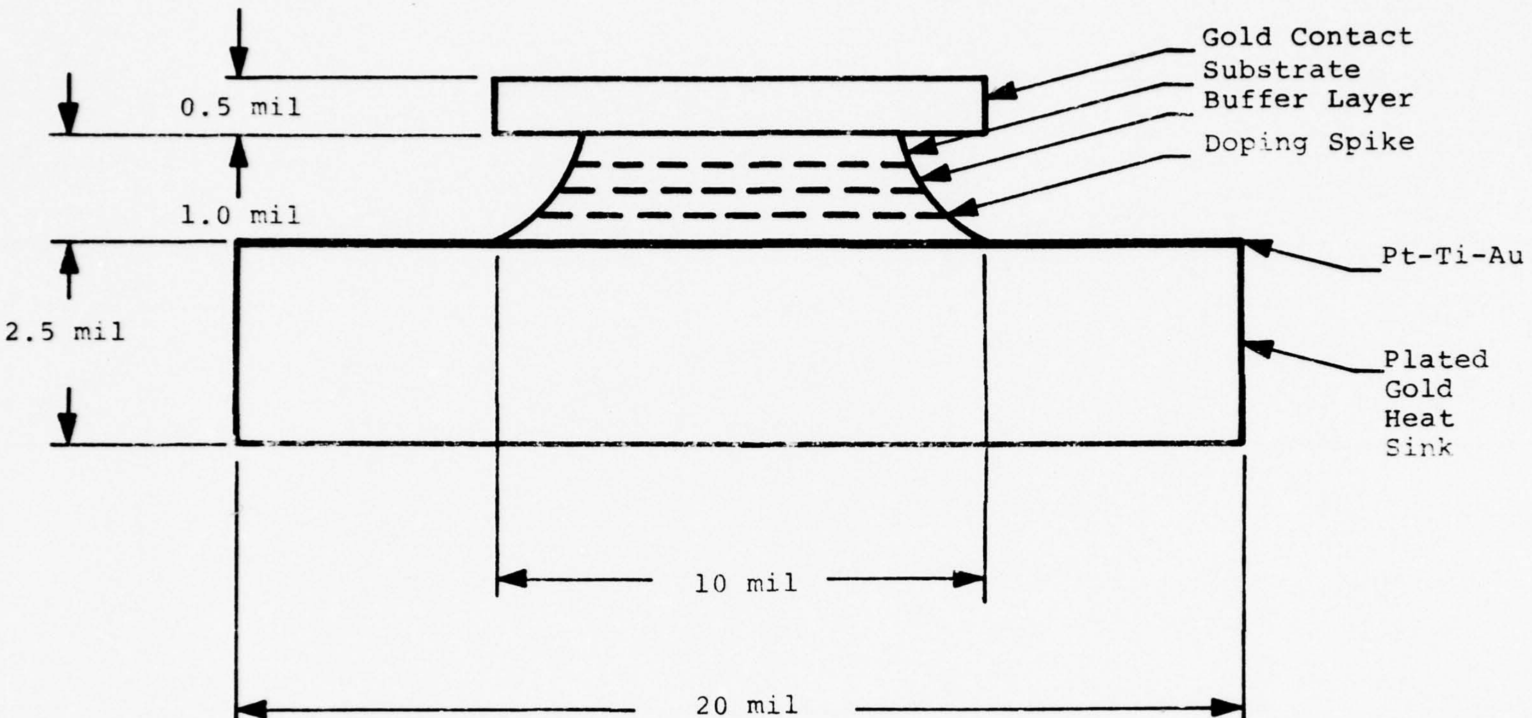

Figure 1-2 Read Profile IMPATT Chip Configuration

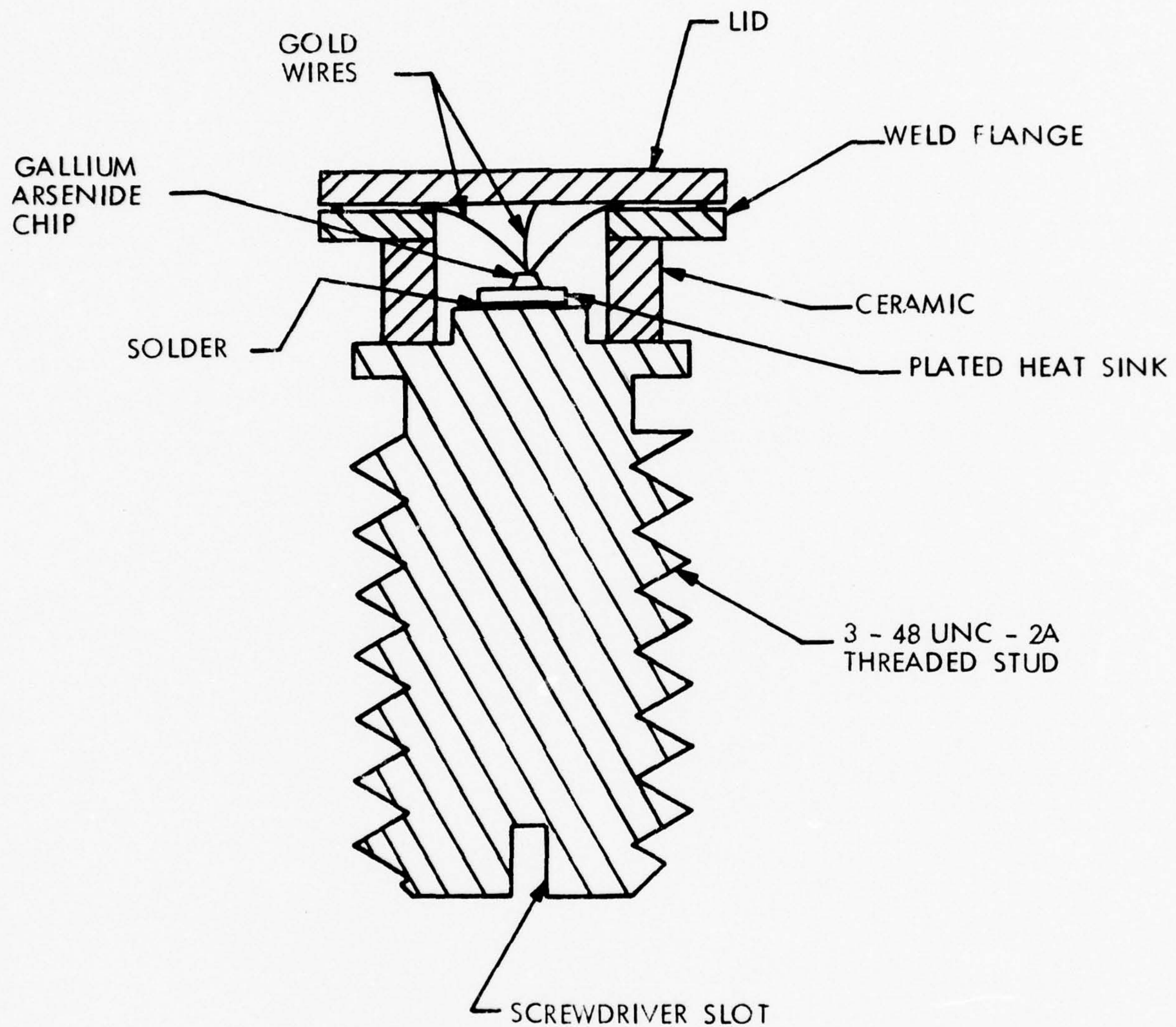

Figure 1-3 Diode Cross Section of Plated Heat Sink Design

1.2 Device Performance and State of the Art

The key performance specifications for an IMPATT diode are its frequency of operation, power output, efficiency, and junction temperature. Other performance characteristics are determined by the design chosen to achieve the primary characteristics. The characteristics are all inter-related to a large extent; a change in one characteristic having an effect on several others.

It is important that the diode specifications be self-consistent within the performance limits of the device. A unifying element is the device area. In general, the area should be large to provide low thermal resistance ($\theta_{th} \approx 1/\sqrt{A}$) but not so large that there is difficulty in matching the device reactance in circuits with reasonable Q. Our experience has taught us that for existing circuit structures, a capacitive reactance of about 10 ohms at the chip level gives optimum results. This requirement implies a chip capacitance near breakdown voltage of 1.7 pF and 1.1 pF for X and Ku-band, respectively. The circuit tolerance is sufficiently broad to allow for ±15% variation in C_j with little degradation in performance.

DC-to-RF conversion efficiencies on the order of 25 percent have been achieved. This is typical of X-band devices as shown in later sections. The conversion efficiencies for Ku-band diodes are in excess of 20 percent, but seldom over 23 percent. If we assume in our analysis a worst case of 20 percent efficiency, we obtain our most conservative prediction of device performance. Assume the diodes are oscillating at P_o = 3.5W(X) and 2.5W(Ku). (See diode specification in Section 1.3.) At the assumed efficiency level, the X and Ku-band devices must dissipate 14 W and 10 W, respectively, as heat. If the

maximum junction temperature is to be 200°C, this allows for a 175°C rise over a 25°C ambient. This requirement, in turn, implies a maximum thermal resistance of 12°C/W and 18°C/W for the X and Ku-band devices. In this regard, our measurements show that the diodes typically achieve above this maximum level. Measurements of thermal resistance on diodes plotted as a function of the diode diameter prior to this program are shown in Figure 1-4. As shown, we had predicted 10°C/W (X) and 14°C/W (Ku). The predicted thermal resistances were not realized. The higher values of thermal resistance typically observed were compensated, however, by efficiency well above the lower limit. Each one percent of increment in the conversion efficiency reduces the temperature by about 7°C.

The cavity circuit used to test Read diodes as oscillators is shown in Figure 1-5. This circuit is referred to as the top hat circuit. At X-band, the loaded Q and external Q are about equal ($Q_{ext} \approx 80$) and are below the maximum limit set in the specifications ($Q_{ext} = 200$).

The mechanically variable elements of the circuit are: (1) the top hat, (2) the diode height above the waveguide floor, (3) the position of the sliding short, and (4) the position of the slide screw tuner at the output end of the cavity. In practice, the device frequency is determined primarily by the top hat, with the other parameters determining the coupling level of the radial RF mode to the cavity mode. Figure 1-6 shows the wide frequency tuning range achieved with a typical diode in X-band. We observe a ±1300 MHz range with only 2.1 dB variation in power output. At all frequencies, the power level stays over 3.5 W CW. It should be noted that these results are

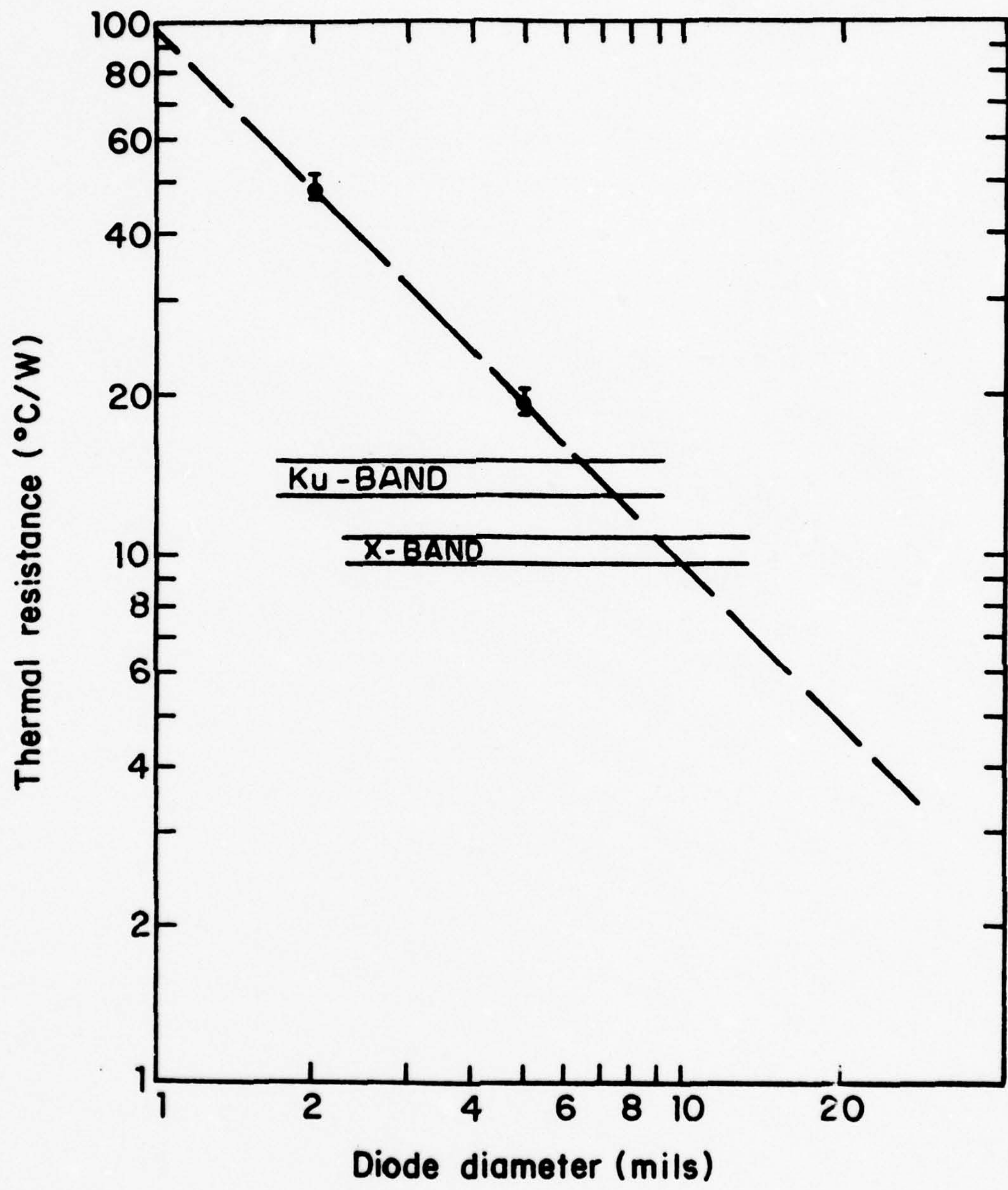

Figure 1-4 Expected Thermal Resistance Ranges for Frequency Bands in Question

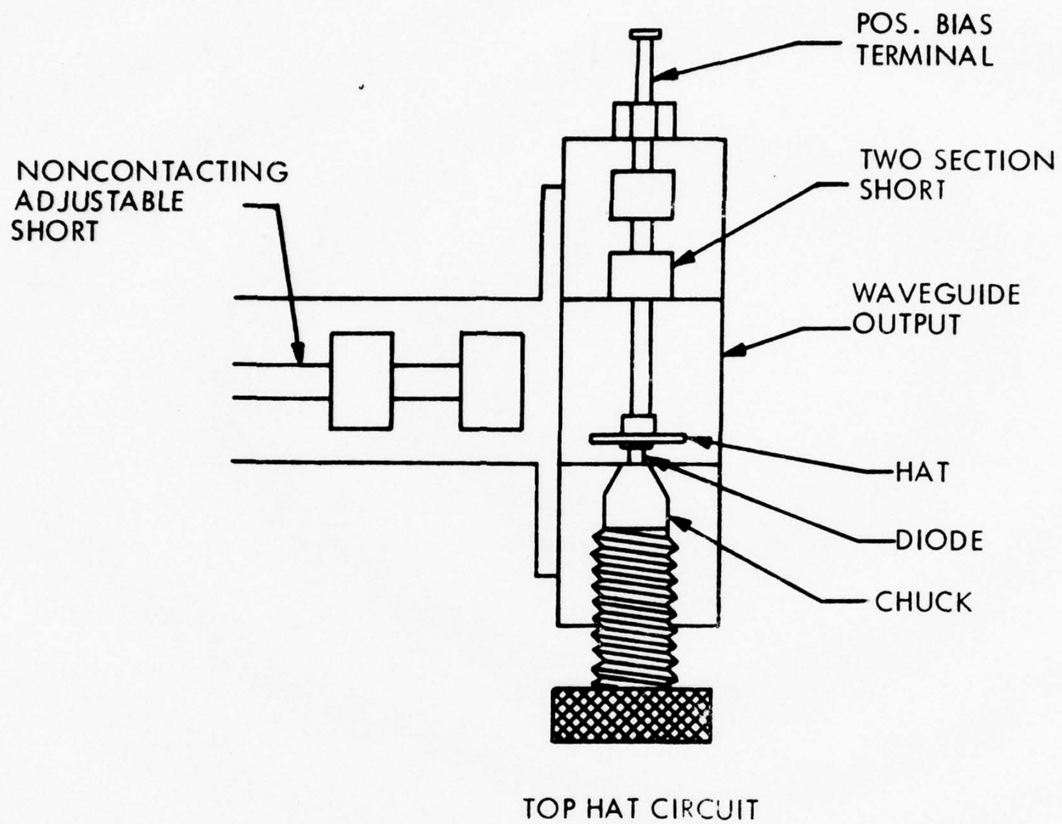

Figure 1-5 Test Circuit for Diode Evaluation

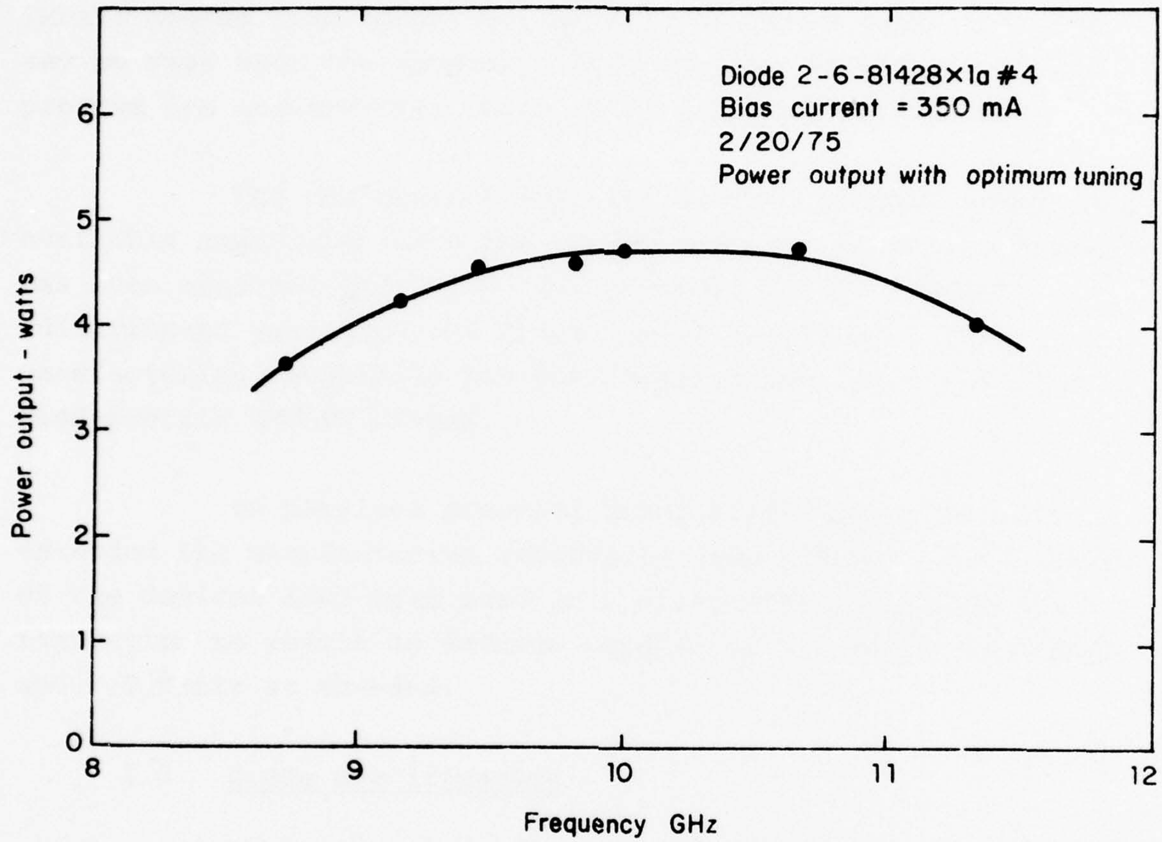

Figure 1-6 Mechanical Tuning Range of a Typical X-Band GaAs Read Diode

for constant current bias conditions. The observed Δf_{mech} well exceeds the device requirements of ±250 MHz.

A listing of the state-of-the-art performance for IMPATT diodes from laboratory work is given in Table 1-2. It may be seen that the specifications for the devices in this program are conservative relative to the best performance.

The performance achieved on this program equals the available capability with the chosen design. Better performance has been obtained only with more advanced design concepts (distributed junctions and double-drift profiles). Thus, a manufacturing capability has been established for X and Ku-band Read-profile IMPATT diodes.

On parallel programs internally-funded, we have extended the manufacturing capability into C-band. Also, some of the devices have been used in a distributed junction configuration to result in devices capable of 9.0 Watts at X-band and 3.5 Watts at Ku-band.

1.3 Diode Specification

The complete diode specifications are included in the following pages. The detailed requirements are essentially the same as the original specification SCS-481, dated 23 December 1974. Additional specifications such as breakdown voltage and thermal resistance have been added in accordance with the contract to better define the diode. The X-band diode has been assigned the Raytheon part number MS-50371. The Ku-band diode has been designated the MS-50372.

Table 1-2

Contract Performance Specifications Compared With Raytheon's Laboratory Results To Date

TEST	SYMBOL	SPECIFICATIONS		ACHIEVED		UNITS
		MIN	MAX	MIN	MAX	
Subgroup 1 Oscillator Performance						
Frequency	f_o	9	16	5	35	GHz
Power Output	P_o	3.5 (X) 2.5 (Ku)			10 (X) 35 (Ku)	W-CW W-CW
Efficiency	η	20 (X) 20 (Ku)			32 (X) 22 (Ku)	% %
Thermal Resistance Junction Temperature =	Θ_{th} 200^oC		10 (X) 14 (Ku)	10 (X) 14 (Ku)		$^oC/W$ $^oC/W$
Assuming 65^oC Heat Sink Temperature						
Subgroup 2						
Mechanical Tuning	Δf_{mech}	±250			±1300	MHz
Subgroup 3						
AM Noise	$(N/S)_{AM}$		-115	-135	-115	dB
FM Noise (1 KHz Bandwidth)	Δf_{rms}		50	53	16	Hz
Subgroup 4						
DC Bias Voltage	V_o		70		55	V
DC Bias Current	I_o		500		400	mA
Subgroup 5						
External Q	Q_{ext}		200	$\approx$80		

RAYTHEON	RAYTHEON COMPANY LEXINGTON, MASS. 02173	CODE IDENT NO. 49956	SPEC NO. 892351 SHEET 1 OF 13 — REV 0

TYPE OF SPEC

SPECIFICATION CONTROL DRAWING

TITLE OF SPEC

MS-50371 - X-BAND READ IMPATT DIODE

FUNCTION	APPROVED	DATE	FUNCTION	APPROVED	DATE
WRITER	[signature]	9.23.77			
CHK	[signature]	9.23.77			
ENGR.	H Chalifoux	9/23/77			

REVISIONS

CHK	DESCRIPTION	REV	CHK	DESCRIPTION	REV
	Originated	0			

REVISION	0	0	0	0	0	0	0	0	0	0	0	0	0
SHEET NO.	1	2	3	4	5	6	7	8	9	10	11	12	13

REV STATUS OF SHEETS	
REVISION	
SHEET NO.	

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1.0 SCOPE

1.1 Scope - This specification covers the detailed requirements for high-efficiency, high power gallium-arsenide Read-type IMPATT diodes.

1.2 Absolute Maximum Ratings - $T_A = 25^{o}C$ unless otherwise specified.

1.2.1 Storage Temperature Range: $-65^{o}C$ to $+200^{o}C$

1.2.2 Operating Ambient Temperature Range: $-40^{o}C$ to $+65^{o}C$

1.2.3 Maximum Junction Temperature: $225^{o}C$

1.2.4 Operating Voltage: 70 Vdc

1.2.5 Operating Current: 400 mA dc

2.0 APPLICABLE DOCUMENTS

2.1 The following documents, of the issue in effect on the date of invitation for bids or request for proposal, form a part of the specification to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-S-19500 Semiconductor Devices, General Specification for

STANDARDS

MILITARY

MIL-STD-750 Test Methods for Semiconductor Devices

MIL-STD-1311 Test Methods for Electron Tubes

3.0 REQUIREMENTS

3.1 Detail Requirements - The individual item requirements shall be in accordance with MIL-S-19500, and as specified herein. In the event of any conflict, the requirements of this specification shall govern.

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3.2 Abbreviations and Symbols - The abbreviations and symbols used herein are defined in MIL-S-19500 and as follows:
Q_{ext} = external quality factor of diode oscillator.

3.3 Design and Construction - The diodes shall be made by epitaxial growth of Read-type profiles. The diode shall consist of a single mesa, single chip mounted in a ceramic-to-metal microwave package.

3.3.1 Physical Dimensions - The package shall be gold plated and hermetically sealed. Physical dimensions of the package shall be as shown in Figure 1. Package characteristics shall be:

C_C = Case Capacitance = 0.30 pf nominal

L_C = Case Inductance = 0.40 nb nominal

3.4 Performance Characteristics - The diode performance characteristics, while operating as oscillators, shall be as specified in Tables I and II and as listed below. The performance characteristics shall apply over the specified ambient operating temperature range unless otherwise specified.

3.4.1 Test Circuit - The test circuit shown in Figure 2 shall be used to verify the performance characteristics as specified in Tables I and II.

3.4.2 Operating Position - The diode shall be capable of proper operation in any position.

3.5 Mechanical Tuning - The RF output power shall not decrease below the specified value. The frequency and power shall vary smoothly with no steps or jumps (see 4.2.6.3).

3.6 External Q - The external quality factor, Q_{ext}, of the diode oscillator shall not be more than 200 (see 4.2.6.4).

3.7 Process Conditioning - All units shall be process conditioned before they are subjected to the tests and examinations defined in Tables I and II.

3.8 Interchangeability - All parts having the same manufacturer's part number shall be directly and completely interchangeable with each other with respect to installation and performance within the requirements of this specification.

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3.9 Marking - Shall be permanent and legible in accordance with MIL-S-19500 and shall include the following: part number, lot identification code and the manufacturer's name or symbol. Marking may appear on the unit container.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection shall be in accordance with MIL-S-19500, and as specified herein.

4.2 Quality Conformance Inspection

4.2.1 Inspection Lot - An inspection lot shall consist of that quantity of devices which the manufacturer processes through the quality conformance inspection at one time.

4.2.2 Group A, Table I - Each inspection lot shall be subjected to the quality conformance examination as specified in Table I. Defective units shall be removed and noted by subgroups. If a given subgroup has failures in excess of the stated LTPD of that subgroup, the entire inspection lot shall be rejected.

4.2.3 Group B, Table II - Sampling acceptance inspection shall be in accordance with Appendix C of MIL-S-19500. Subgroup defects in excess of the stated LTPD in Table II shall cause the entire inspection lot to be rejected. Sample for Group B testing shall be selected from a previously acceptable Group A lot. A composite summary of all Group B test data shall accompany each lot shipped.

4.2.4 Specified LTPD for Subgroup - The LTPD specified in Tables I, II, and III herein shall apply to all the tests combined in the individual subgroup.

4.2.5 Process-Conditioning - Testing and Screening - Process conditioning and testing and screening shall be in accordance with this document and performed in the exact sequence shown. Process-conditioning shall be conducted on 100 percent of the lot prior to submission of the lot to quality conformance inspection.

4.2.5.1 Hermetic Seal (Gross Leak) Test - All devices shall be tested for gross leaks in accordance with MIL-STD-750, Method 1071, Test Conditions D or F.

4.2.5.2 High Temperature Storage - All diodes will be stored, non-operating, under the following conditions:

(a) Junction Temperature: 225°C max.
200°C min.

(b) Storage Time: 168 hours min.

4.2.6 Methods of Examination and Test - Methods of examination and test shall be as specified in Tables I and II and as follows:

4.2.6.1 AM Noise - An AM noise measurement system as shown schematically in Figure 3 shall be used to determine the AM noise to signal ratio. The AM noise spectrum shall be measured continuously from 10 KHz to 100 KHz from the carrier as a minimum and recorded by an X-Y recorder. Noise measurements shall be performed while the diode oscillator is meeting the operating requirements in Table I, Subgroup 3.

4.2.6.2 FM Noise - An FM noise measurement system as shown schematically in Figure 3 shall be used to determine FM noise deviation. The FM noise spectrum shall be measured continuously from 10 KHz to 100 KHz from the carrier as a minimum and recorded by an X-Y recorder. Noise measurement shall be performed while the diode oscillator is meeting the operating requirements in Table I, Subgroup 3.

4.2.6.3 Mechanical Tuning - The oscillator unit will be mechanically tuned over the required frequency range of ±250 MHz from operating frequency.

4.2.6.4 External Q - The external quality factor, Q_{ext}, of the diode oscillator shall be determined by standard injection locking techniques. A small locking signal shall be injected into the diode oscillator for measurement of locking bandwidth as a function of injected power.

4.2.6.5 Efficiency (RF-DC) - The RF-to-DC power efficiency of diodes operating as oscillators shall be determined by measuring the DC input power and using standard mathematical formulations:

$$\text{Power Efficiency (RF-DC)} = \frac{\text{Power Output (RF)} \times 100}{\text{Power In (DC)}}$$

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4.2.6.6 RF Output Power - RF output power of diodes operating as oscillators shall be measured at operating frequency in accordance with Method 4250, MIL-STD-1311 using a calibrated thermistor and power meter.

4.2.6.7 Oscillator Frequency - Frequency of diodes operating as oscillators shall be determined with a spectrum analyzer and verified with a calibrated frequency meter.

4.2.6.8 Thermal Resistance - The junction temperature shall be determined as follows: The breakdown voltage of the diode shall be measured at 40°C intervals between 20°C and 200°C in accordance with Method 4021 of MIL-STD-750. The breakdown voltage shall be that voltage corresponding to a reverse current of 1 mA. The diode shall then be biased under pulsed condition in a lossy circuit to suppress oscillations, thus making input power equivalent to dissipated power. Pulse width shall be sufficient (about 1 msec) for the diode to reach thermal equilibrium. The diode shall then be pulsed down to a current of 1 mA and breakdown voltage shall be measured. The pulse down duration shall be short (several microseconds) to prevent cooling of the diode. From this data, thermal resistance of the diode shall be determined.

4.2.6.9 Junction Temperature - The thermal resistance of the device shall be measured in accordance with 4.2.6.8. The junction temperature shall be calculated as follows:

$$T_j = P_D \times R_{th}$$

where: P_D = power dissipated = $(V_o)(I_o) - P_o$

The symbols are as specified in Table I.

4.2.6.10 Storage Life (Non-Operating) - The diodes shall be stored at an ambient temperature of 200°C ±3°C for 1000 hours minimum. These diodes shall be selected randomly from diodes which have undergone process conditioning and have successfully passed all Group A inspections. Upon completion of storage, the diodes shall be subjected to the following tests described in Table I, Subgroup 3.

4.2.6.11 Operating Life - The diodes shall be tested under operating conditions in accordance with Table I, Subgroup 3 for 1000 hours minimum. Power output shall

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be monitored continuously. The diodes subjected to the operating life test shall be selected randomly from diodes which have undergone process conditioning, and have successfully passed all Group A inspections. The number of failures as a function of time shall be recorded. The test shall be conducted in an ambient temperature of 25 ±3°C and the cavity temperature shall not exceed 75°C during this test.

4.2.6.12 Nuclear Radiation Exposure - Devices will be exposed to the neutron level specified below over a time period not to exceed five (5) minutes. This exposure will be conducted with the devices in a non-operating, non-biased condition and at a temperature not to exceed 40°C. Devices shall not experience temperatures in excess of 40°C prior to evaluation testing. Evaluation will be conducted in such a manner that no device will be operated for more than two (2) minutes prior to completion of the subgroup tests. These precautions are necessary to reduce the effects of high temperature annealing of the radiation induced damage.

10^{13} n/cm^2, 1 MeV equivalent (Si)

10^4 rads (Si) gamma

5.0 PREPARATION FOR DELIVERY

5.1 Preparation for Delivery - Packaging and marking shall be in accordance with MIL-S-19500.

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TABLE I

GROUP A INSPECTION

T_A = 25 ±3°C unless otherwise specified.

Examination or Test	MIL-STD-750 Method	MIL-STD-750 Details	LTPD	Symbol	Min	Max	Units
Subgroup 1							
Visual & Mechanical Examination	2071		7	--	---	---	---
Subgroup 2							
Breakdown Voltage	4021	I_R = 1.0 mA	5	BV	30	50	Vdc
Capacitance	4102	f = 1 mHz V_R= 25 Vdc		C_{TVR}	1.6	2.2	pf
Thermal Resistance		4.2.6.8		R_{th}	---	16.0	°C/W
Subgroup 3							
Operating Frequency		4.2.6.7	5	f_o	9	11	GHz
Power Output		4.2.6.6		P_o	3.5	---	W-CW
Conversion Efficiency		4.2.6.5		η	20.0	---	%
Junction Temperature		4.2.6.9		T_j	---	200	°C
Operating Current	4016			I_o	---	400	mAdc
Operating Voltage	4016			V_o	---	70	Vdc
Subgroup 4							
Mechanical Tuning		4.2.6.3	5	Δf mech	±250		MHz
Subgroup 5							
External Q		4.2.6.4	5	Q_{ext}		200	
Subgroup 6							
AM Noise		4.2.6.1	5	(N/S)AM		-115	dB
FM Noise		4.2.6.2		Δf rms		50	Hz

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TABLE II

GROUP B INSPECTION

Examination or Test	MIL-STD-750 Method	Details	LTPD	Symbol	Min	Max	Units
Subgroup 1							
Physical Dimensions	2066	See Figure 1	7				
Subgroup 2							
Shock	2016	Non-operating; 500G, t = 1.0 msec., X_1, Y_1, and Z_1 orientation.					
Vibration, Variable Freq.	2056	Non-operating; 20G, 50 to 200 Hz	15				
Constant Acceleration	2006	Non-operating; 20,000G min, X_1, Y_1 and Z_1 orientation.					
Hermeticity	1071	Test Condtion H-Traces Gas Fine Leak (Helium)					
End point measurements; Table I, Subgroup 3							
Subgroup 3							
Nuclear Radiation Exposure		4.2.6.12	15				
End point measurements; Table I, Subgroup 3.							
Subgroup 4							
Storage Life (non-operating)		4.2.6.10	15				
End point measurements; Table I, Subgroup 3							

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TABLE II
(continued)

Examination or Test	MIL-STD-750 Method	Details	LTPD	Symbol	Min	Max	Units
Subgroup 5							
Operating Life		4.2.6.11	30				

End point: All diodes which have operated for 1000 hours minimum per the requirements of Table III shall have a power output of no less than 75 percent of the initial power output.

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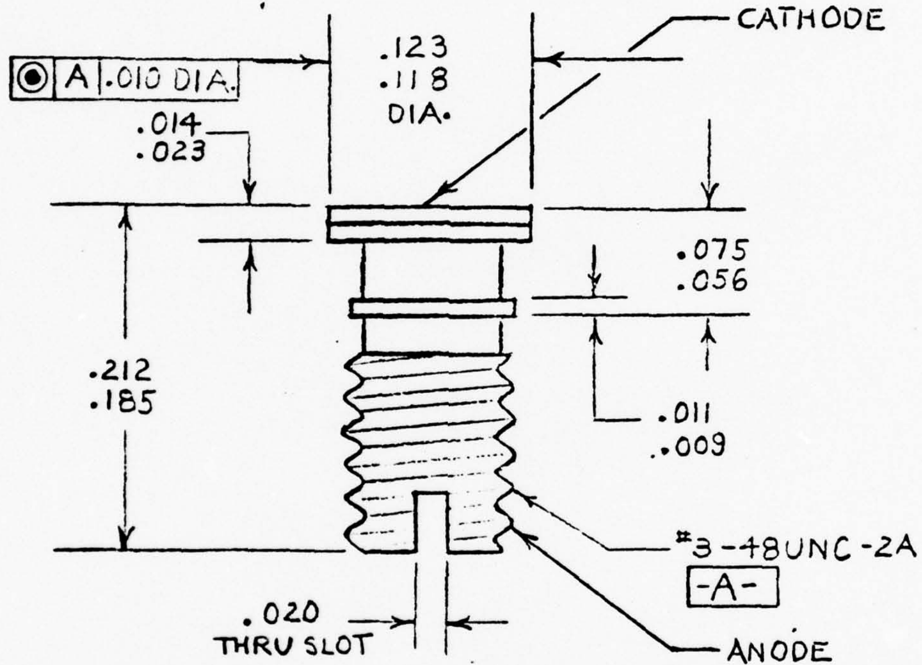

Figure 1

Ceramic-To-Metal Microwave Diode Package

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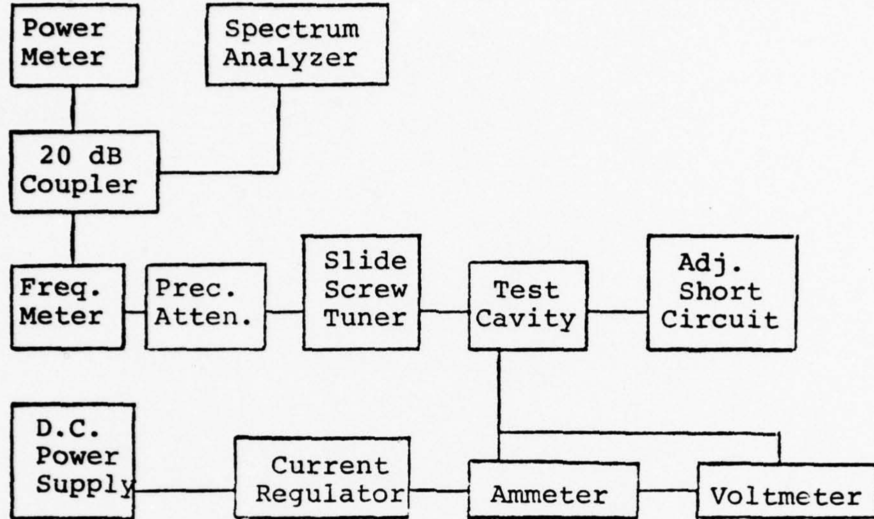

Figure 2(a) Test System Block Diagram

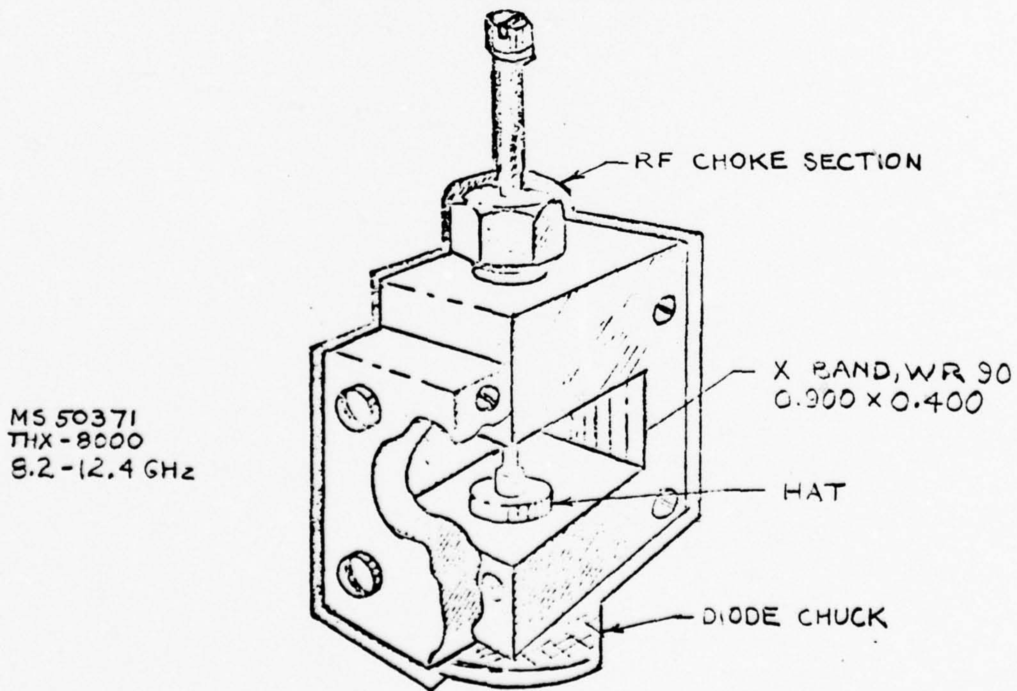

Figure 2(b) Test Cavity

Figure 2 RF Test Measurement System

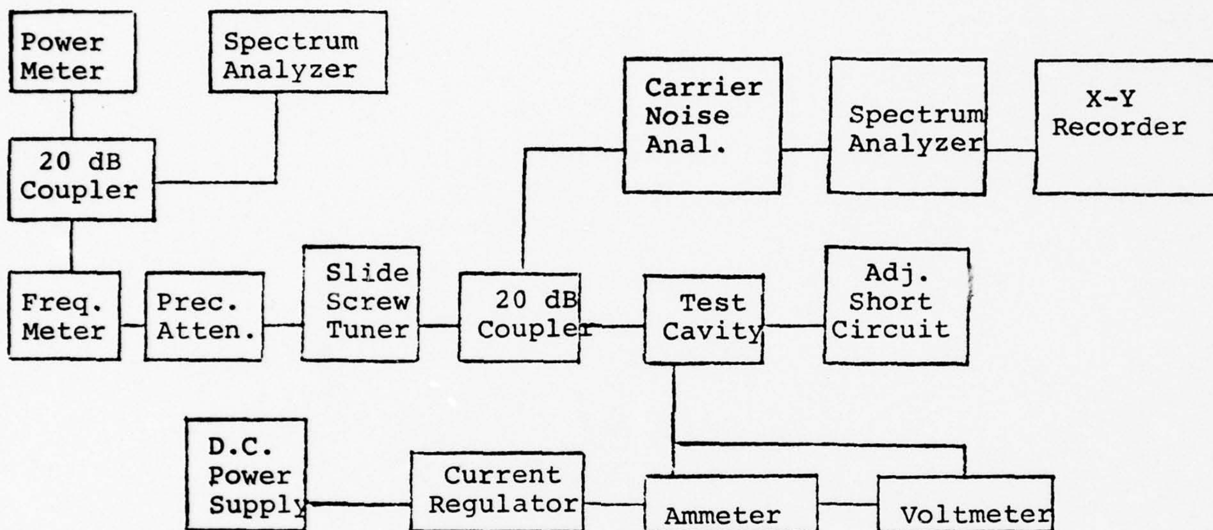

Figure 3 AM-FM Noise Measurement System

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TYPE OF SPEC

SPECIFICATION CONTROL DRAWING

TITLE OF SPEC

MS-50372 - KU-BAND READ IMPATT DIODE

FUNCTION	APPROVED	DATE	FUNCTION	APPROVED	DATE
WRITER	[signature]	9-23-77			
CHK	[signature]	9-23-77			
ENGR.	[signature]	9/23/77			

REVISIONS

CHK	DESCRIPTION	REV	CHK	DESCRIPTION	REV
	Originated	0			

REVISION	0	0	0	0	0	0	0	0	0	0	0	0	0									
SHEET NO.	1	2	3	4	5	6	7	8	9	10	11	12	13									

REV STATUS OF SHEETS	REVISION																			
	SHEET NO.																			

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1.0 SCOPE

1.1 Scope - This specification covers the detailed requirements for high-efficiency, high power gallium-arsenide Read-type IMPATT diodes.

1.2 Absolute Maximum Ratings - $T_A = 25^oC$ unless otherwise specified.

1.2.1 Storage Temperature Range: -65^oC to $+200^oC$

1.2.2 Operating Ambient Temperature Range: -40^oC to $+65^oC$

1.2.3 Maximum Junction Temperature: 225^oC

1.2.4 Operating Voltage: 60 Vdc

1.2.5 Operating Current: 400 mA dc

2.0 APPLICABLE DOCUMENTS

2.1 The following documents, of the issue in effect on the date of invitation for bids or request for proposal, form a part of the specification to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-S-19500 Semiconductor Devices, General Specification for

STANDARDS

MILITARY

MIL-STD-750 Test Methods for Semiconductor Devices

MIL-STD-1311 Test Methods for Electron Tubes

3.0 REQUIREMENTS

3.1 Detail Requirements - The individual item requirements shall be in accordance with MIL-S-19500, and as specified herein. In the event of any conflict, the requirements of this specification shall govern.

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3.2 Abbreviations and Symbols - The abbreviations and symbols used herein are defined in MIL-S-19500 and as follows:
Q_{ext} = external quality factor of diode oscillator.

3.3 Design and Construction - The diodes shall be made by epitaxial growth of Read-type profiles. The diode shall consist of a single mesa, single chip mounted in a ceramic-to-metal microwave package.

3.3.1 Physical Dimensions - The package shall be gold plated and hermetically sealed. Physical dimensions of the package shall be as shown in Figure 1. Package characteristics shall be:

C_C = Case Capacitance = 0.30 pf nominal

L_C = Case Inductance = 0.40 nb nominal

3.4 Performance Characteristics - The diode performance characteristics, while operating as oscillators, shall be as specified in Tables I and II and as listed below. The performance characteristics shall apply over the specified ambient operating temperature range unless otherwise specified.

3.4.1 Test Circuit - The test circuit shown in Figure 2 shall be used to verify the performance characteristics as specified in Tables I and II.

3.4.2 Operating Position - The diode shall be capable of proper operation in any position.

3.5 Mechanical Tuning - The RF output power shall not decrease below the specified value. The frequency and power shall vary smoothly with no steps or jumps (see 4.2.6.3).

3.6 External Q - The external quality factor, Q_{ext}, of the diode oscillator shall not be more than 200 (see 4.2.6.4).

3.7 Process Conditioning - All units shall be process conditioned before they are subjected to the tests and examinations defined in Tables I and II.

3.8 Interchangeability - All parts having the same manufacturer's part number shall be directly and completely interchangeable with each other with respect to installation and performance within the requirements of this specification.

3.9 Marking - Shall be permanent and legible in accordance with MIL-S-19500 and shall include the following: part number, lot identification code and the manufacturer's name or symbol. Marking may appear on the unit container.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection shall be in accordance with MIL-S-19500, and as specified herein.

4.2 Quality Conformance Inspection

4.2.1 Inspection Lot - An inspection lot shall consist of that quantity of devices which the manufacturer processes through the quality conformance inspection at one time.

4.2.2 Group A, Table I - Each inspection lot shall be subjected to the quality conformance examination as specified in Table I. Defective units shall be removed and noted by subgroups. If a given subgroup has failures in excess of the stated LTPD of that subgroup, the entire inspection lot shall be rejected.

4.2.3 Group B, Table II - Sampling acceptance inspection shall be in accordance with Appendix C of MIL-S-19500. Subgroup defects in excess of the stated LTPD in Table II shall cause the entire inspection lot to be rejected. Sample for Group B testing shall be selected from a previously acceptable Group A lot. A composite summary of all Group B test data shall accompany each lot shipped.

4.2.4 Specified LTPD for Subgroup - The LTPD specified in Tables I, II, and III herein shall apply to all the tests combined in the individual subgroup.

4.2.5 Process-Conditioning - Testing and Screening - Process conditioning and testing and screening shall be in accordance with this document and performed in the exact sequence shown. Process-conditioning shall be conducted on 100 percent of the lot prior to submission of the lot to quality conformance inspection.

4.2.5.1 Hermetic Seal (Gross Leak) Test - All devices shall be tested for gross leaks in accordance with MIL-STD-750, Method 1071, Test Conditions D or F.

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4.2.5.2 High Temperature Storage - All diodes will be stored, non-operating, under the following conditions:

(a) Junction Temperature: 225°C max.
200°C min.

(b) Storage Time: 168 hours min.

4.2.6 Methods of Examination and Test - Methods of examination and test shall be as specified in Tables I and II and as follows:

4.2.6.1 AM Noise - An AM noise measurement system as shown schematically in Figure 3 shall be used to determine the AM noise to signal ratio. The AM noise spectrum shall be measured continuously from 10 KHz to 100 KHz from the carrier as a minimum and recorded by an X-Y recorder. Noise measurements shall be performed while the diode oscillator is meeting the operating requirements in Table I, Subgroup 3.

4.2.6.2 FM Noise - An FM noise measurement system as shown schematically in Figure 3 shall be used to determine FM noise deviation. The FM noise spectrum shall be measured continuously from 10 KHz to 100 KHz from the carrier as a minimum and recorded by an X-Y recorder. Noise measurement shall be performed while the diode oscillator is meeting the operating requirements in Table I, Subgroup 3.

4.2.6.3 Mechanical Tuning - The oscillator unit will be mechanically tuned over the required frequency range of ±250 MHz from operating frequency.

4.2.6.4 External Q - The external quality factor, Q_{ext}, of the diode oscillator shall be determined by standard injection locking techniques. A small locking signal shall be injected into the diode oscillator for measurement of locking bandwidth as a function of injected power.

4.2.6.5 Efficiency (RF-DC) - The RF-to-DC power efficiency of diodes operating as oscillators shall be determined by measuring the DC input power and using standard mathematical formulations:

$$\text{Power Efficiency (RF-DC)} = \frac{\text{Power Output (RF)} \times 100}{\text{Power In (DC)}}$$

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4.2.6.6 RF Output Power - RF output power of diodes operating as oscillators shall be measured at operating frequency in accordance with Method 4250, MIL-STD-1311 using a calibrated thermistor and power meter.

4.2.6.7 Oscillator Frequency - Frequency of diodes operating as oscillators shall be determined with a spectrum analyzer and verified with a calibrated frequency meter.

4.2.6.8 Thermal Resistance - The junction temperature shall be determined as follows: The breakdown voltage of the diode shall be measured at 40°C intervals between 20°C and 200°C in accordance with Method 4021 of MIL-STD-750. The breakdown voltage shall be that voltage corresponding to a reverse current of 1 mA. The diode shall then be biased under pulsed condition in a lossy circuit to suppress oscillations, thus making input power equivalent to dissipated power. Pulse width shall be sufficient (about 1 msec) for the diode to reach thermal equilibrium. The diode shall then be pulsed down to a current of 1 mA and breakdown voltage shall be measured. The pulse down duration shall be short (several microseconds) to prevent cooling of the diode. From this data, thermal resistance of the diode shall be determined.

4.2.6.9 Junction Temperature - The thermal resistance of the device shall be measured in accordance with 4.2.6.8. The junction temperature shall be calculated as follows:

$$T_j = P_D \times R_{th}$$

where: P_D = power dissipated = $(V_o)(I_o) - P_o$

The symbols are as specified in Table I.

4.2.6.10 Storage Life (Non-Operating) - The diodes shall be stored at an ambient temperature of 200°C ±3°C for 1000 hours minimum. These diodes shall be selected randomly from diodes which have undergone process conditioning and have successfully passed all Group A inspections. Upon completion of storage, the diodes shall be subjected to the following tests described in Table I, Subgroup 3.

4.2.6.11 Operating Life - The diodes shall be tested under operating conditions in accordance with Table I, Subgroup 3 for 1000 hours minimum. Power output shall

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be monitored continuously. The diodes subjected to the operating life test shall be selected randomly from diodes which have undergone process conditioning; and have successfully passed all Group A inspections. The number of failures as a function of time shall be recorded. The test shall be conducted in an ambient temperature of 25 ±3°C and the cavity temperature shall not exceed 75°C during this test.

4.2.6.12 Nuclear Radiation Exposure - Devices will be exposed to the neutron level specified below over a time period not to exceed five (5) minutes. This exposure will be conducted with the devices in a non-operating, non-biased condition and at a temperature not to exceed 40°C. Devices shall not experience temperatures in excess of 40°C prior to evaluation testing. Evaluation will be conducted in such a manner that no device will be operated for more than two (2) minutes prior to completion of the subgroup tests. These precautions are necessary to reduce the effects of high temperature annealing of the radiation induced damage.

10^{13} n/cm^2, 1 MeV equivalent (Si)

10^4 rads (Si) gamma

5.0 PREPARATION FOR DELIVERY

5.1 Preparation for Delivery - Packaging and marking shall be in accordance with MIL-S-19500.

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TABLE I

GROUP A INSPECTION

T_A = 25 ±3°C unless otherwise specified.

Examination or Test	MIL-STD-750 Method	MIL-STD-750 Details	LTPD	Symbol	Min	Max	Units
Subgroup 1							
Visual & Mechanical Examination	2071		7	--	---	---	---
Subgroup 2							
Breakdown Voltage	4021	I_R = 1.0 mA	5	BV	16	32	Vdc
Capacitance	4102	f = 1 mHz V_R= 25 Vdc		C_{TVR}	1.6	2.4	pf
Thermal Resistance		4.2.6.8		R_{th}	---	22.0	°C/W
Subgroup 3							
Operating Frequency		4.2.6.7	5	f_o	14	16	GHz
Power Output		4.2.6.6		P_o	2.5	---	W-CW
Conversion Efficiency		4.2.6.5		η	20.0	---	%
Junction Temperature		4.2.6.9		T_j	---	200	°C
Operating Current	4016			I_o	---	500	mAdc
Operating Voltage	4016			V_o	---	60	Vdc
Subgroup 4							
Mechanical Tuning		4.2.6.3	5	Δf mech	±250		MHz
Subgroup 5							
External Q		4.2.6.4	5	Q_{ext}		200	
Subgroup 6							
AM Noise		4.2.6.1	5	(N/S)AM		-115	dB
FM Noise		4.2.6.2		Δf rms		50	Hz

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TABLE II

GROUP B INSPECTION

Examination or Test	MIL-STD-750 Method	MIL-STD-750 Details	LTPD	Symbol	Min	Max	Units
Subgroup 1							
Physical Dimensions	2066	See Figure 1	7				
Subgroup 2							
Shock	2016	Non-operating; 500G, t = 1.0 msec., X_1, Y_1, and Z_1 orientation.					
Vibration, Variable Freq.	2056	Non-operating; 20G, 50 to 200 Hz	15				
Constant Acceleration	2006	Non-operating; 20,000G min, X_1, Y_1 and Z_1 orientation.					
Hermeticity	1071	Test Condtion H-Traces Gas Fine Leak (Helium)					
End point measurements; Table I, Subgroup 3							
Subgroup 3							
Nuclear Radiation Exposure		4.2.6.12	15				
End point measurements; Table I, Subgroup 3.							
Subgroup 4							
Storage Life (non-operating)		4.2.6.10	15				
End point measurements; Table I, Subgroup 3							

TABLE II
(continued)

Examination or Test	MIL-STD-750 Method	Details	LTPD	Symbol	Min	Max	Units
Subgroup 5							
Operating Life		4.2.6.11	30				

End point: All diodes which have operated for 1000 hours minimum per the requirements of Table III shall have a power output of no less than 75 percent of the initial power output.

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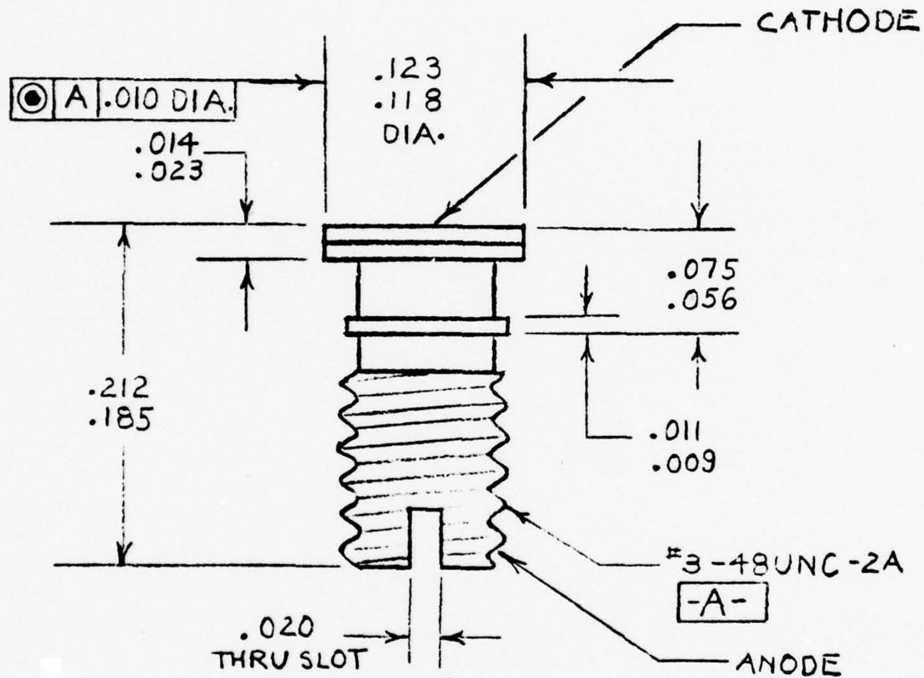

Figure 1

Ceramic-To-Metal Microwave Diode Package

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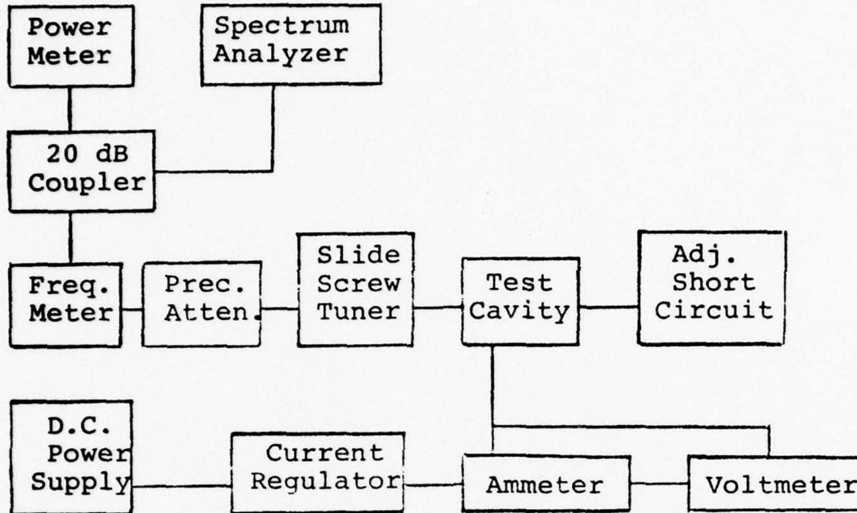

Figure 2(a) Test System Block Diagram

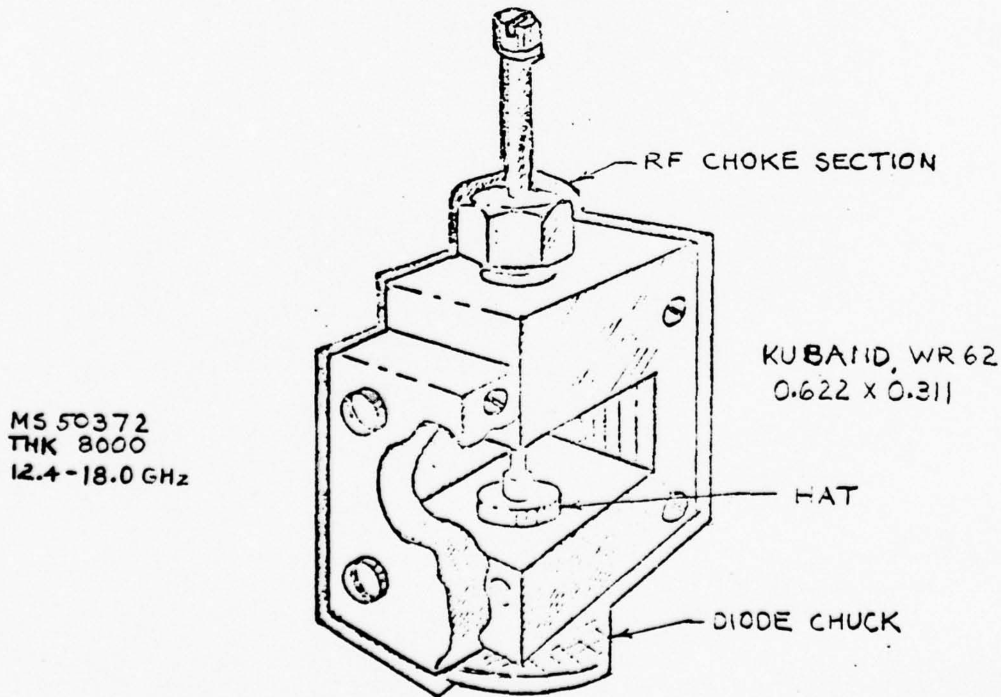

Figure 2(b) Test Cavity

Figure 2 RF Test Measurement System

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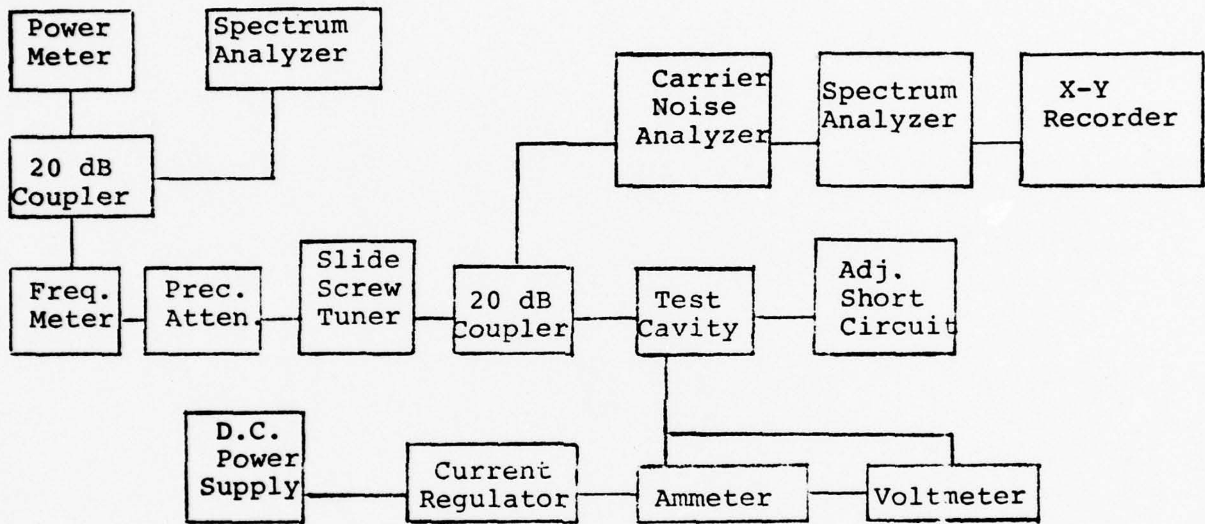

Figure 3 AM-FM Noise Measurement System

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2.0 NARRATIVE PROCESS DESCRIPTION

2.1 Effect of Process Upon Diode Parameters

It was pointed out that the critical parameter of the wafer which controls the operating frequency of the device is the drift zone width. For a Read diode this is approximately equal to the total depletion depth, X_D. The tolerance on X_D is established by the tolerance on operating frequency which then determines the allowed variations in the parameter X_p, ΔE and the drift layer doping n_D. Having established an optimum set of characteristics for a wafer subsequent to growth, they are then subject to modification during further diode processing. The dimension X_p, for example, is decreased during wafer metallization by reaction of the Schottky metal and the surface gallium arsenide. This effect has an influence upon diode performance which is the result of process control. This and similar effects were examined during the course of the program. A large part of the effort on the program was, therefore, process related. The major effort was to define the process which gave the best performance and to control the tolerances for improved reproducibility of parameters and for better yield.

A narrative description of the process is given in this section of the report. Results of process development work are included in the following section. Detailed process specifications and drawings are included in Section II.

2.2 Fabrication of LHL Read Wafers

2.2.1 Introduction

The LHL Read wafers used for this program were produced by the epitaxial deposition of suitably doped gallium

arsenide layers upon a highly conducting gallium arsenide single crystal substrate. The major steps used to fabricate the wafers are: (1) substrate receipt and qualification, (2) substrate preparation, (3) reactor preparation, (4) reactor loading, (5) epitaxial deposition, (6) reactor unloading and clean-up, (7) wafer qualification, and (8) packaging and transfer. Each of these steps will be discussed in the sections which follow.

2.2.2 Substrate Receipt and Qualification

2.2.2.1 Substrate Specifications

The substrate serves as the mechanical support upon which the active layers of the wafers are grown. Its characteristics, however, are very important to the yield of useful wafers. The crystallographic orientation of the substrate, for example, strongly influeces the growth rates and dopant incorporation of the epitaxial layers grown upon it. Thus, the reproducibility of the three most important wafer parameters, X_p, Q, and n_D, are all strongly dependent upon the crystallographic orientation of the substrate. Defects such as dislocations, strains, and precipitates in the substrate, propagate into the epitaxial layers during growth and result in reduced device yield. Even more importantly they interfere with device manufacturing processes, especially with the various thinning and etching steps. Thus, even though the substrates are totally removed in chip manufacture, the substrates must be carefully selected and processed prior to epitaxial growth.

Slices cut from highly doped single crystal boules of gallium arsenide are used as substrates for epitaxial growth. Highly conducting crystals with an n-type dopant are used for Read IMPATT devices. Dopants which might be selected are selenium, tellurium, silicon, and tin. Tellurium was selected

as the dopant for substrates because its large out-diffusion minimizes the occurrence of insulating layers.

The specifications listed in Table 2-1 were established to satisfy these considerations within the limitations of cost and availability.

2.2.2.2 Boule Qualification

Raw substrates are procured as slices from a single crystal boule. At least forty slices, sequentially sliced and numbered, meeting the substrate specifications must be delivered from each boule to be acceptable. The following data must be supplied by the vendor with each shipment: boule number, slice number, electrical characteristics and etch pit density of the first and last slice shipped from each boule, total usable weight of the slices, and approximate dimensions of the average usable slice obtainable from the boule.

Upon receipt at Raytheon, the first and last slices from each boule are subjected to the following tests prior to boule acceptance:

a. Macroscopic Examination. The surface of each slice is examined to determine the quality of the sawing job. Poor slicing results in misorientation, or excessive crystallographic damage which cannot be eliminated in successive processing steps, and invariably manifests itself in poor epitaxial wafer or diode yield. Damage can often be detected by simple visual examination.

b. Microscopic Examination. A section is cleaved

Table 2-1

Specifications for Tellurium Doped GaAs Slices

	MIN	MAX
Measured Donor Concentration	$1 \times 10^{18}\ cm^{-3}$	$2 \times 10^{18}\ cm^{-3}$
Electrical resistivity	Not Spec.	0.002 Ωcm
Etch pit density	Not Spec.	$10{,}000\ cm^{-2}$
Orientation angle of <100> towards <110>	1.5^{o}	2.5^{o}
Thickness	0.381 mm	0.406 mm
Size * - Standard	2.1 x 2.1 cm	Not Spec.
Large	3.5 x 3.5 cm	Not Spec.
Crystallinity - single with no twins		
Precipitates - dimensions	Not Spec.	1 μm
Precipitates - density	Not Spec.	$100\ cm^{2}$
Strains	None	None
Saw damage (into crystal lattice)	Not Spec.	4 μm
Texture - saw damage	Not Spec.	1.5 μm
Mosaic	None	None

* Slice must yield square <110> edges with specified size.

from each slice, and the cleaved edge etched for 30 seconds under a strong light in 7:2:1 sulfuric acid:hydrogen peroxide:water etchant at room temperature. After rinsing and drying, the cleaved edge is examined at high magnification. Precipitates, etch pits, and residual strain can be evaluated quantitatively by this test. Boules not meeting minimum requirements are rejected without further tests. Etch pit density is measured by counting several known areas after etching with either AB etch or molten KOH.

c. Orientation. The vendor's orientation measurements are confirmed by Laue X-ray patterns upon a slice chemically polished by immersion in an ultrasonically agitated 7:2:1 sulfuric:peroxide: water solution at room temperature.

d. Anomolous X-Ray Transmission. A quantitative estimate of the dislocations and amount of strain present in a slice is obtained by measuring the X-ray transmission of a slice positioned so as to give maximum transmission for an orientation near the <220> plane. Maximum transmission of the incident beam is obtained with a crystalline slice nearly free of dislocations, imperfections, precipitates, or strain. Inhomogeneities in the slices are detected by moving the crystal relative to the beam limiting aperture, and noting variations in the anomolous X-ray transmission.

e. Electrical Measurements. D.C. Hall samples are prepared from each slice by forming an ohmic contact

at each corner of a small square sample cleaved from the slice. The doping, resistivity, and mobility of the sample is measured by the van der Pauw method while the sample is immersed in liquid nitrogen. In addition, the doping may be determined by the wavelength at which maximum absorption occurs in the infrared.

f. Dimensional Tolerances. Conformance to dimensional tolerances are determined by measurement of several sample slices from each lot. Thickness, bow, and taper are measured using a precision non-contacting gauge.

g. Polish and Etch. The final step in boule qualification is to subject a sample slice to normal polish, etch, and growth procedures. The surface of the slice is inspected for defects after growth. Defective substrates usually yield epitaxial layers with excessive surface defects. Residual strains and precipitates which interfere with fracture along the normal <110> planes, can be detected by the difficulty observed in cleaving of test strips. Lattice defects are revealed by anomalous etch pits.

h. Boule Acceptance. If the results of all tests are satisfactory, the boule is accepted. Upon acceptance, 10% of the lot is reserved for process verification tests; the remaining 90% are sent to production processing.

2.2.3 Substrate Preparation

2.2.3.1 Wafer Cleaning

Wafers sent to production processing are first sent through an extensive cleaning procedure to remove abrasives, and contaminants introduced during the slicing. Cleaning consists of multiple rinses in trichlorethylene, acetone, alcohol, and filtered, distilled, de-ionised water, followed by an ultrasonic etch in a sulfuric acid:hydrogen peroxide:water solution in a teflon container. The residual acid solutions are removed by multiple rinse in de-ionized water, followed by drying with a jet of filtered nitrogen. Care is taken to preserve the serial number of each slice.

2.2.3.2 Prepolish Inspection

After cleaning, the wafers are individually measured using a precision noncontacting gauge for thickness, bow, and taper.

2.2.3.3 Sizing

In preparation for polishing, the slices are individually cut to fit the reactor substrate holder. Cutting is generally done by cleaving so that the four edges of the wafer follow the <110> crystallographic planes. Three standard wafer sizes are in use at Raytheon. These are: small 2.2 x 2.2 cm, intermediate 3.0 x 3.0 cm, and large 3.8 x 3.8 cm.

2.2.3.4 Mount, Polish, Dismount

Wafers are hot mounted on an optically flat fused silica disc using purified beeswax. Prior to polishing, excess wax is removed from the wafer surface using a cotton swab wet with hot trichlorethylene.

Polishing is carried out on a Unipol machine using a pellon pad and a dilute solution of bromine in methanol. Polishing is continued until the wafers have a mirror finish and contactless measurement indicates that the final thickness is within specifications.

After polishing, the wafers are dismounted by heating and then the mounting wax is removed by several rinses in hot trichlorethylene. The wafers are stored in individual containers, identified by boule and wafer serial numbers.

2.2.3.5 Post Polish Inspection

Polished wafers are individually inspected under a strong light for surface blemishes, such as excessive texture, pits, scratches, or stains. Conformance to thickness, bow, and taper specifications are determined using a contactless gauge. Those that conform are stored under filtered dry nitrogen until needed for growth.

2.2.4 Epitaxial Deposition

2.2.4.1 The Epitaxial Reactor

The LHL Read wafers used for this program were produced by the epitaxial growth of suitably doped gallium arsenide upon a highly conducting gallium arsenide single crystal substrate. Vapor phase reactors constructed at Raytheon prior to the initiation of this program were used to grow these layers. A photograph of the wafer production area showing several of these reactors is shown in Figure 2-1. The reactors use the well-known arsenic trichloride, hydrogen, gallium growth process. Using this process, high purity gallium-arsenide layers can be deposited with reproducible doping levels and thickness upon suitably oriented substrates.

Figure 2-1 Epitaxial Wafer Production Area

Each reactor shown schematically in Figure 2-2 is comprised of an epitaxial growth tube constructed of high purity fused silica, a six-zone furnace, and a gas handling system. It is provided with precise controls stabilized with feedback amplifiers and a deposition programmer to provide the reproducibility to make the growth of Read wafers feasible.

The furnace is mounted on tracks and can be moved longitudinally. This feature is important because it allows daily etching of the reactor tube to remove deposits from the wall. Six independently-controlled temperature zones are provided to allow rapid changes to be made in the temperature profile of the reactor.

The gas handling system is housed in a nitrogen-flushed plastic box to prevent contamination from minor leaks to the ambient atmosphere. Servo-controlled feedback flow controllers are used to maintain and adjust all gas flows. The gas flows are directed by two and three-way solenoid valves. Two arsenic trichloride bubblers are provided; one for the etch and one for growth. Each set of bubblers is provided with its own temperature controller. All hydrogen used in the reactor is purified by diffusion through palladium membranes.

A deposition programmer controls the reactor. Multiple time cycles and controlled functions are preprogrammed for each growth run. The programmer activates the multiple solenoids in correct sequence, controls the various dopant and hydrogen servo-flow controllers, and varies the arsenic trichloride mole fraction. Any function or cycle can be reprogrammed at will between runs without altering the remaining program.

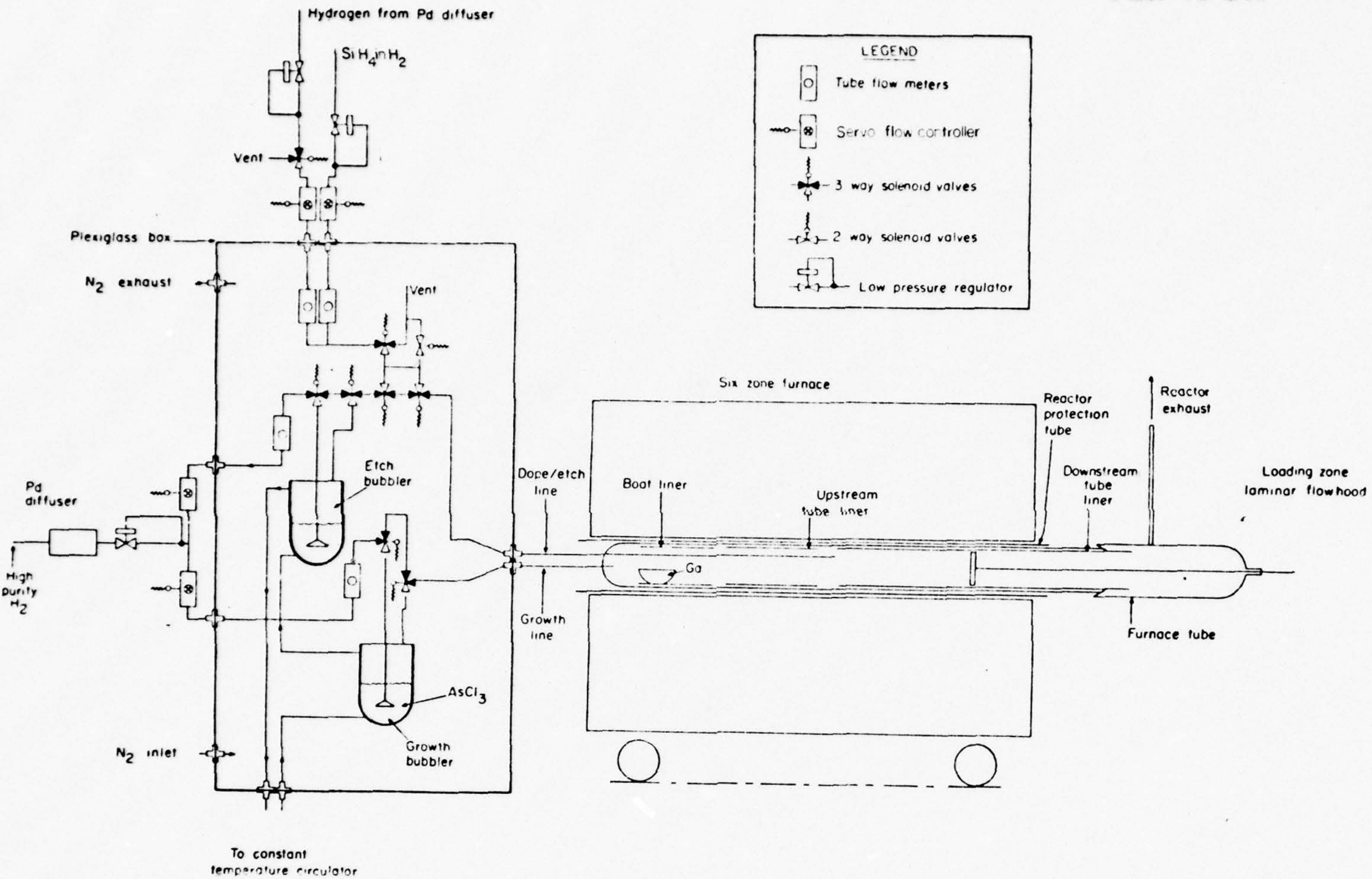

Figure 2-2 Schematic Diagram of the Raytheon Production Reactor and its Controls

2.2.4.2 Pregrowth Reactor Preparation

All removable silica ware of the reactor downstream of the substrate is cleaned between epitaxial growth runs by soaking in freshly prepared high purity aqua regia in clean silica containers. Generally the soak is for about 20 minutes duration, and is followed by thorough rinsing in ultrapure water, and air drying in a laminar flow bench. Every few runs the silica ware is precleaned in dilute hydrofluoric acid to remove deposits which resist solution by aqua regia. All reagents used are of electronic grade or better, and all lot numbers are recorded with data, container number, and epitaxial deposition number for traceability

Deposits on parts of the reactor upstream of the wafer are cleaned, usually between each growth run, by hot vapor etching *in situ*. To accomplish this, the affected parts of the reactor are heated to a temperature between 800°C and 850°C; then H_2 saturated with $AsCl_3$ is admitted through the etch tube. Usually, 30 minutes of vapor etching suffice to clean the silica ware completely.

Prior to loading the wafer, the vent lines and oil bubblers are cleaned and the latter refilled with fresh silicone oil. A clean downstream tube liner is inserted, and a clean wafer holder and end cap are used. At the time of wafer loading, the movable furnace is preheating in the upstream standby position.

2.2.4.3 Substrate Loading

Just prior to loading, selected substrates are removed from storage, heated in polar and non-polar solvents, etched briefly in a moving sulfuric-peroxide etch, and rinsed

repeatedly in very pure water (15 mega-ohms or greater). Finally, they are centrifuged dry in filtered nitrogen, immediately placed in the substrate holder, and loaded into the reactor in the pre-growth position. Loading is carried out in a laminar flow bench to prevent contamination by ambient dust.

2.2.4.4 Deposition

After loading, it is necessary to purge the reactor of all gases admitted while the reactor tube was open to the atmosphere. This is accomplished by flushing with purified hydrogen for 30 to 60 minutes.

After purging, the furnace is moved to the growth position. It is precisely positioned using a knife-edge pointer referenced to a fixed scale. During the thermal stabilization period, the *automatic deposition control* is programmed to yield the desired wafer preheat time, source presaturation and wafer vapor etch, buffer thickness and doping, and active layer thickness and doping, based on measurements of the preceding growth run. Checks are made to see that all automatic controls, such as $AsCl_3$ bubbler circulator temperature, furnace zone temperature controls, and reactant flow controls, are correctly set and functioning.

2.2.5 Wafer Qualification

2.2.5.1 Introduction

Each wafer after deposition must pass rigorous qualification standards prior to being manufactured into chips. Wafers not meeting these standards are unlikely to produce diodes meeting the requirements of this program and are rejected for this application.

2.2.5.2 Characterization Sample

Immediately after the wafer is unloaded from the reactor, a small characterization piece is cleaved off from the right-hand edge of the wafer as it faces the vapor stream during deposition. In addition to providing a characterization sample which can be destructively evaluated, the cleaved edge unmistakably orients the wafer in subsequent processing steps so that systematic trends which affect yield can be identified and corrected. The main portion of the wafer is sent for surface quality inspection and measurement of the mechanical dimensions prior to packaging and storage.

2.2.5.3 Layer Thickness Measurements

A small piece of the characterization sample is removed and used for layer thickness measurement. A freshly cleaved edge is etch stained for a few seconds using an aqueous solution of potassium ferricyanide and potassium hydroxide, followed immediately by D.I. water rinses and nitrogen drying. The cleaved edge is mounted under a high power microscope whereupon the epitaxial layers are plainly visible and can be measured by a calibrated image shearing eye-piece.

This measurement is made as soon as possible after unloading the wafer so that the data obtained can be used to guide the Schottky etch steps as well as to correct the deposition program for the next run in that reactor.

2.2.5.4 Schottky Photolithography and Etching

The doping profile for Read wafers is determined from measurements on Schottky-barrier diodes formed on the remainder of the characterization piece. By changing the reverse

bias voltage on the diode, while simultaneously measuring the capacitance and change in capacitance, we deduce the free carrier concentration through the epitaxial layer.

Surface breakdown limits the depth which can be profiled. Therefore, a deep profile is synthesized by joining several partial profiles together. Each partial profile is obtained from Schottky diodes on adjacent areas, each etched a slightly different depth from the others (Figure 2-3). This is facilitated by a special etch mask used to define the etch steps photolithographically. The sample consists of several arrays of eight 0.125 cm adjacent squares, each of which are etched to different depths. After rinsing and a brief post-bake, the sample is ready for metallization.

2.2.5.5 Schottky Metallization and Lift-Off

Schottky metallization is carried out by the sequential evaporation of aluminum and gold in a vacuum bell jar. Typically, 0.2 μm of aluminum are applied followed by 0.02 μm of gold. The gold is used to minimize surface oxidation of the aluminum upon exposure to air, making electrical contact during measurement more reliable.

After metallization, the sample is removed from the bell jar and immersed in acetone, which is ultrasonically agitated. The acetone swells and dissolves the undeveloped resist under the metallization which eventually floats away leaving a metallized pattern which exactly corresponds to the Schottky mask.

2.2.5.6 Electrical Characterization

The doping profile is determined for the Schottky diodes just described by changing the reverse bias voltage while simultaneously measuring the capacitance and change in capacitance.

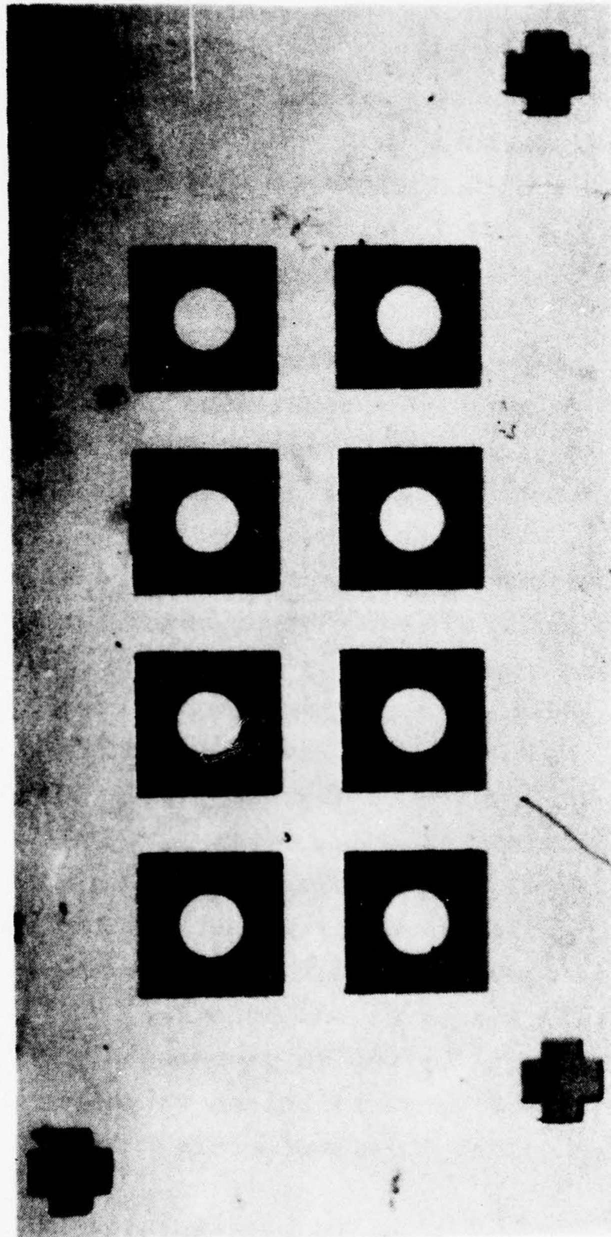

Figure 2-3 Characterization Sample (magnified approximately 8X) showing array of eight Schottky diodes, each centered in a square etched to a different depth. Each diode is 0.400 mm in diameter.

This is accomplished by using an automatic profiler constructed at Raytheon. A deep profile is synthesized by joining several partial profiles together. Special care is taken to ensure that the size of all diodes is identical because the precentage error in the doping measurement approximates four times the percentage error in the diode diameter. Spike depth (X_p) is also determined from these measurements.

The integrated charge in the spike (Q) is determined from these same measurements by summing the product of the capacitance and the incremental bias voltage multiplied by an appropriate constant between limits defined by the spike.

V* is a useful electrical parameter for LHL Read wafers and diodes. The capacitance versus voltage plot of a planar Schottky barrier device on a typical Read profile wafer is given in Figure 3-1. The voltage interval within which $\frac{dC}{dV}$ is small corresponds to the same interval required to deplete the free carriers from the doping spike. Likewise, the transition to a significantly higher $\frac{dC}{dV}$ corresponds to the edge of the carrier depletion region entering the transit layer. We have designated the intersection of the transit region C-V asymptote and the spike C-V asymptote as V*. We have found that V* is a function of both X_p and Q, two of the three critical device parameters and V* is independent of device area. Therefore, this easily measured parameter is an indicator of device performance from the wafer to finished diode levels of device manufacture.

2.2.5.7 Surface Inspection

The surface texture of a GaAs epitaxial wafer is very important in determining the performance of the microwave devices made from it. An uneven surface, for example, is unsuitable for very precise photolithography. Uneven surfaces

usually correlate with nonuniform active epitaxial layer thickness, which is important to field uniformity as well as transit time. Rough surfaces are particularly deleterious to Read avalanche transit-time wafers since they lead to nonuniform field distribution and consequently to "soft" breakdowns and poor power-handling capability.

All wafers are inspected after growth for surface appearance. Macroexamination under a bright lamp, as well as microexamination under an interference microscope, are routine. Surfaces are evaluated on a scale of 1 through 5 using the following criteria:

a. Excellent quality with no visible defects.

b. Very good quality with a few minor defects.

c. Good quality with over 80% of the area usable.

d. Unacceptable poor quality with 30 to 80% of area usable.

e. Very poor quality with less than 30% of area usable.

The types of blemishes which are cause for rejection are: pits (large and small), stains, scratches, mounds, haze, or a very rough texture.

2.2.5.8 Physical Dimensions

The thickness and uniformity in thickness of each wafer is measured as part of the wafer inspection. This thickness and its uniformity are parameters of great importance in facilitating economical wafer processing in subsequent dice fabrication steps. Thickness and uniformity of thickness over the

wafer, as well as bow and taper, are measured using a precision noncontacting gauge to avoid contamination or damage. All handling is carried out in a clean room in a laminar flow bench to avoid contamination with ambient aerosols and particulate matter.

In addition, the width and length of each wafer is measured in centimeters using a simple scale.

2.2.5.9 Packaging and Transfer

The measured characteristics of all wafers are compared to the wafer specifications. All wafers which qualify are packaged in cushioned boxes, and sealed hermetically in mylar bags to prevent damage during transfer and storage.

Quality assurance documents are prepared for each qualified wafer listing its measured characteristics. Copies of these documents are transferred with the wafer to the dice fabrication area.

2.3 Fabrication of Plated Heat Sink Read Dice

2.3.1 Introduction

The dice fabrication procedure is based upon methods previously demonstrated at Raytheon. The present procedure includes several innovations added during this program to result in significant process simplification, yield, or performance improvements.

2.3.2 Receipt of Wafers

As a first step in the effort, the wafer is submitted to incoming inspection. This simply consists of an inspection

of data submitted with the wafer to assure conformance to the specification. A careful visual examination is also performed to assure good wafer surface quality. The wafers utilized on the program were generally outstanding in surface quality. Some few wafers which had a slight haze were accepted and processed, but no detectable performance degradation was observed in the devices assembled from these wafers.

A routing card is initiated to direct the wafer through the dice fabrication sequence of operations. This serves also as a record of processing detail information. Each diode delivered is completely traceable with this system through the entire manufacturing process.

2.3.3 Wafer Cleaning

The wafers are cleaned in order to remove all traces of foreign impurities. Each wafer is then subjected to a thorough microscopic inspection immediately prior to loading into the sputtering system. Should any trace of stain or particulate matter be noticeable under 40X magnification, the wafer is subjected to additional cleaning steps until no visible impurities are present. This painstaking procedure has been found to be necessary in order to insure the high quality Schottky-barriers required for high power IMPATT device operation. Schottky barriers deposited on GaAs cleaned by the above process have been shown to be characterized by excellent adhesion, and exhibit imperfection-free, mirror-like metal surfaces.

2.3.4 Schottky Barrier Metallization

The metallization process is based on the use of a metal layer which prevents diffusion of the gold heat sink metal into the Schottky-barrier metal. The configuration is

schematically illustrated in Figure 2-4. Immediately after cleaning and inspection, the GaAs wafers are loaded into the sputtering system (MRC Model 8802). Three metals are sputtered onto the epitaxial GaAs surface. The first, platinum, forms the Schottky barrier, while the second metal, Ti, forms a metal diffusion barrier. This is necessary in order to prevent the gold plated heat sink metal from rapidly diffusing through the thin Pt and into the GaAs material at even moderate (250°C) temperatures. A technique using titanium as a gold-diffusion barrier metal has been developed at Raytheon and proven to yield high performance devices. Following the deposition of Ti on the Pt, a final film of gold is sputtered over the Ti barrier, and the wafers are removed from the system. A tape test is performed to check adherence of the deposited metal. This is followed by further solvent cleaning.

2.3.5 Gold Plate and Flat Lap

Additional gold is then plated over the sputtered metal to protect the metallization during lapping operations. This plated metal is nominally 0.1 mil thick.

The thickness of each wafer is then measured at several points. A thickness profile map is thus obtained using standard forms. Wafers meeting flatness uniformity specifications of ±0.0001 mil are accepted for gold heat sink plating. Those not meeting this specification are subjected to flatness lapping and remeasured. The operation is repeated if necessary until the wafers are within tolerance. Good control of flatness, parallelism and nominal dimensional control is obviously critical in this process. Each surface of the wafers serves in turn as a reference surface when performing thinning operations on the opposite face. The wafer yield is determined by the measure of control achieved. The diode capacitance tolerance is similarly determined by the final degree of taper on the finished wafer.

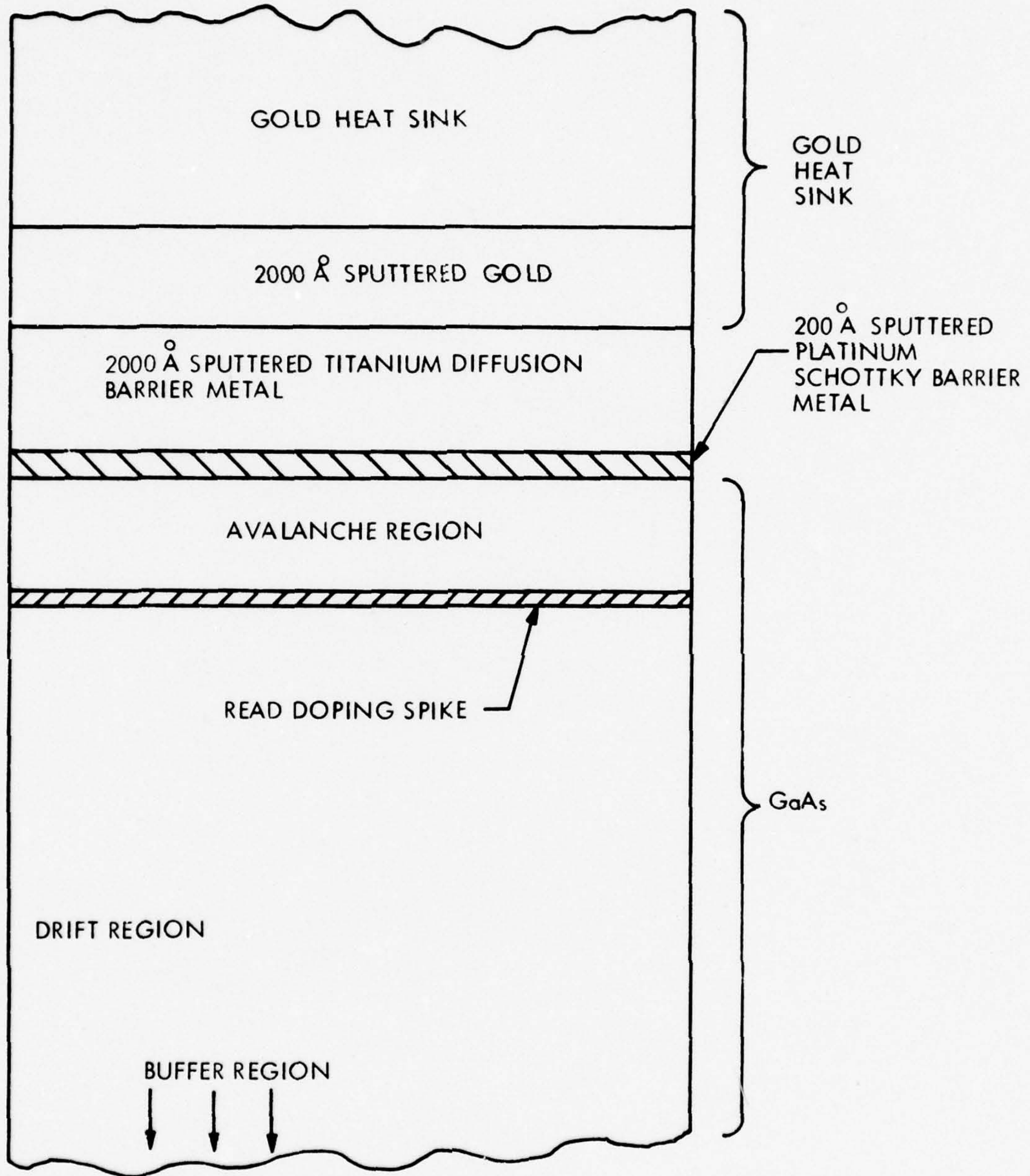

Figure 2-4 Schematic Drawing Illustrating the Diffusion Barrier Schottky Metallization Scheme Used for Fabricating High-Power Read-Profile IMPATT Diodes.

2.3.6 Heat Sink Plating

The wafer is mounted to a glass slide for heat sink plating. In order to minimize edge buildup of the gold plated heat sink, the mounting wax on the sides of the wafers is built up in order to reduce the presence of sharp corners which generally result in high electric field densities in the plating bath. A guard electrode is then applied surrounding the wafer whose effect is to achieve a more uniform electric field pattern in the plating bath. Using this method, it has been shown that a minimum of edge buildup is encountered. Taper of the plated gold has been reduced so that gold lap is not always necessary.

Following wafer mounting, the plated heat sink is applied to the Schottky-barrier metal by means of electroplating gold. An innovation which was found to reduce edge buildup and result in a very dense gold plating is that of pulsed-plating. Such pulsed plating is effective only if very short (less than one millisecond) pulses are used. These pulses must be short enough not to deplete the metal ions from the plating solution during the on-time of the pulse. The solution reaches a new ion-concentration equilibrium between pulses (the off-time is adjusted to approximately 10 times the on-time). The thickness of the plated heat sinks is held to between 2.0 and 3.0 mils. This thickness range has been found ideal for optimum wafer handling and subsequent spray etching to form dice.

2.3.7 Edge Trimming and Gold Lap

Although the above procedure is designed to minimize edge buildup, it has been found necessary to trim the edges prior to further processing. Using a diamond-impregnated wire saw, each edge of the wafer is removed. The distance of the cut from the original edge is determined by the amount of buildup and is typically

0.050". An edge burr of gold is undesirable because it tends to fold over the edge, overlapping the gallium arsenide which hampers subsequent thinning.

2.3.8 Thickness Gauging

All wafers are then gauged for thickness and uniformity. A tolerance of ±0.0001" in thickness uniformity is required for the wafers to be passed for further processing. Wafers not falling within this tolerance window are mounted for flat lapping of the gold. The thickness of each wafer is recorded on the processing sheet.

The above-noted tolerance on thickness uniformity must be met in order to maintain reasonable uniformity in device areas, following the mesa etching step. A flatness tolerance of ±0.0001", implies a GaAs thickness variation of ±10% for a 0.001" thick wafer. Any larger variations can be expected to cause excessive device area nonuniformities over a 3 cm^2 wafer. Typical flat lapping results obtained in the diode production area at Raytheon indicate uniformities of better than ±0.00005". If flat lapping is required at this stage, it is carried out as described below.

2.3.9 Gold Lap

The wafers are mounted on a stainless steel lapping plate using mounting wax. This operation requires skilled operators in order to prevent mishandling and to ensure flatness of mounting to within ±0.00005".

Flat lapping is carried out on the Speed Fam machine using a preset time in order to avoid excessive movement of the abrasive lapping slurry over the wafers. Flatness to within a ±0.0001" tolerance is required at this stage since the

lapped gold heat sink surface forms the reference plane for the later GaAs flat lapping operation. Following removal of the wafers from the mounting fixture by dissolution of the mounting wax by solvents, the wafers are subjected to a thorough cleaning process in order to remove excess lapping grit.

2.3.10 GaAs Thin Lap

The final lapping operation involves thinning the GaAs to a value such that mesas can be readily etched to reasonable uniformity tolerances. Experience has shown that uniform GaAs thickness values of 0.002 inch are manageable and at the same time not so thin as to result in excessive cracking. The wafers are mounted, plated heat sink side down, on stainless steel lapping fixtures and lapping is carried out as described in the above section.

Wafers are removed from the stainless steel mounting fixture by dissolution of the mounting wax in organic solvents. All wafers are then thoroughly cleaned. In order to remove any lapping compound that might remain embedded in the GaAs, each wafer is subjected to a brief chemical etch.

2.3.11 Grid Etch

The GaAs is thinned by lapping as described above to a thickness of 2 mils. Lapping and etching to thinner values often results in stress cracking of the GaAs. A grid is, therefore, etched in the GaAs at this point, resulting in a matrix of GaAs islands on the plated heat sink. The grid etch is performed using standard photoresist techniques. The grid is a two mil wide line on twenty mil center spacing. A 3-1-1 sulphuric, peroxide, water solution is used to etch the GaAs.

Having formed the grid, the photoresist is removed and the GaAs layer is further etched. The GaAs pads are measured

for thickness and the thickness is reduced to 1.0 mil. The etching serves to remove GaAs material damaged by lapping. The final surface is smooth.

2.3.12 Back Metallization

After the GaAs pads have been thinned, the devices on the wafer can be probed for breakdown voltage. The information derived on unmetallized layers is somewhat inaccurate but gives a preview of final results and provides an accept-reject opportunity in some situations. No wafers have been rejected at this stage on this program.

The wafer is then metallized. The procedure is the same as the Schottky metallization described in 2.3.4. Gold is plated to 0.1 mil as described in 2.3.5.

Using standard photolithography, the gold top layer is etched except for a round dot which later serves as the etch mask for mesa etch. The gold is etched with commercial conductor etchant. The titanium is etched in HF. The platinum layer is then removed by sputter etching.

2.3.13 Mesa Etch

Using the gold dot as an etch-resistant mask, the GaAs is now etched. This results in an array of mesas on the wafer, each having a gold top contact for bonding. A photograph of a typical mesa configuration is shown in Figure 2-5. A 10-mil diameter etch mask is used for the X-band devices. A 7-mil etch mask is used for the Ku-band devices.

2.3.14 Wafer Evaluation and Mapping

After mesas are etched on each wafer, evaluation of the wafers is carried out by probing and recording data on mesas at

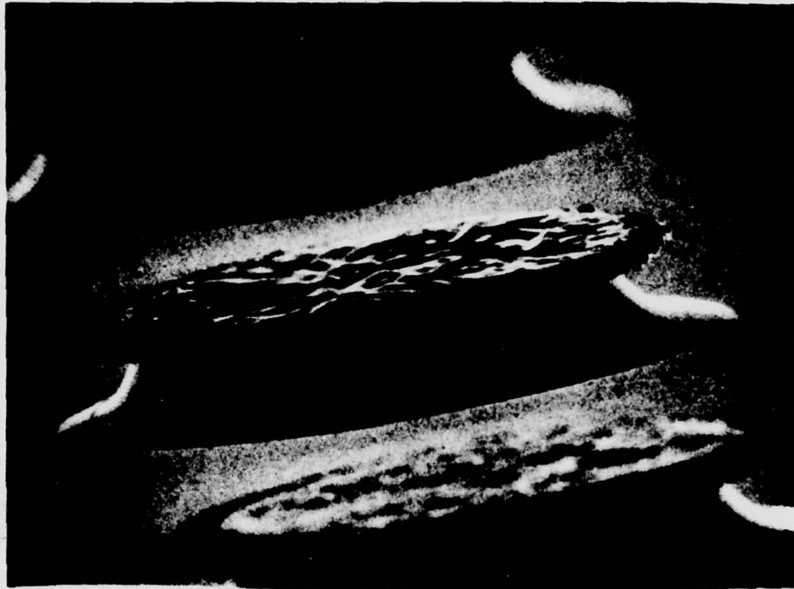

Figure 2-5 Typical GaAs IMPATT Diode Mesa on a Wafer

the intersection of every fifth column and every fifth row. A map of each wafer is, thus, rapidly generated. This map provides information about the nature of the doping profile in the wafer, as well as the quality of the wafer processing. This information is fed back to the materials group and, thus, provides important feedback on epitaxial layer doping profile achievements. A complete description of the total wafer evaluation process is described in a later section of this report.

2.3.15 Spray Dicing

To generate individual diode chips from the wafer, a novel spray dicing technique developed at Raytheon is utilized in the production department. The method involves photolithographic masking techniques. The wafers are placed in a special spray dicing fixture, and a high velocity spray of gold etching solution directed at the plated heat sink side of the wafer. The action of this high velocity spray is such that anisotropic etching occurs and grid lines are cut into the gold in those areas where no photoresist is located. A complete description of the process and a photograph of the finished chips are included in a later section of the report.

Spray dicing completes the dice fabrication portion of the Read diode manufacturing process. The dice are delivered to the diode assembly area for inspection and assembly into packages.

2.4 Diode Assembly and Test

After processing of the wafer and separation into dice, the resultant chips are tested and then assembled into diode packages. The diode configuration is shown in cross section in Figure 1-3.

2.4.1 Lot Documentation

The initial step in the diode assembly process is formation of the production lot and assignment of a lot number. The documentation process utilized for this purpose results in each diode having a unique serial number. Traceability of the diode through all its production steps is thereby possible. Diodes manufactured utilizing this serialization system are delivered with serial number and requested data transcribed to the minimum individual diode container. Complete data and lot history is retained on file.

2.4.2 Die Mounting

Die mounting is a critical operation and several factors influence the quality of the bond between the chip and the package pedestal. Current diode production employs a gold-tin solder disposed between the chip and package. The operation is performed on a commercial die bonder which serves to position and hold the chip with the proper applied pressure during soldering.

We have implemented the use of hot-gas bonding as a method for bonding the chips. In the approach, the parts are located and held in the package with a pick-up tool. The substrate heater is held at a temperature below the soldering temperature. A heated gas is then directed at the part to supply the incremental temperature necessary to flow the solder.

2.4.3 Ribbon Bonding

Following die mounting, the parts are thoroughly batch cleaned to remove the flux and prepare the parts for inspection. One-hundred percent visual inspection is then performed. The parts are inspected to several quality criteria which include inspection of the chip which has been mounted. Typical defects

include broken or cracked chips, stress cracks, poor metallization and geometry or pattern defects. These defects are removed at this time to improve yield at subsequent operations and to improve reliability. The defects are classified and inspection results summarized on process control charts at the station. Yields at this operation vary between 90-98% depending to a large degree upon the quality of the chips being processed.

Contact to the top of the chip is made by thermo-compression bonding of ribbon to the metallization pad on the chip.

The procedure for ribbon installation involves two distinct steps. One end of the ribbon is first welded to the flange of the package. The ribbon is inserted into the package in the desired shape and the other end is similarly welded to the opposing side of the flange. At a separate station the ribbon is "wedge-bonded" to the chip metallization. Two ribbons are bonded in this manner, 90° apart.

2.4.4 Inspection

Following ribbon bonding, the parts are again delivered to Q.C. for inspection. The parts are 100 percent visually inspected for broken or defective bonds. A sample of visually acceptable bonds is non-destructive pull-tested with a bond probe. This testing combined with the destructive testing at setup is considered adequate to assure high quality bonding.

2.4.5 Junction Etching

After die mount and wire connecting, the junction is generally etched to remove surface damage or contamination and to tailor the junction to the specification value of capacitance.

The diodes are first tested and sorted into bins, depending upon the value of starting capacitance. Each bin is then etched for a predetermined time depending upon the bin number. The testing and binning process continues until the lot is completed. Etching is performed using a 3-1-1 solution of sulphuric acid, hydrogen peroxide and water.

Following etching, it is important that the etchant be completely removed from the package. Thorough rinsing is, therefore, performed in specially designed fixtures. A vacuum bake at 175°C follows and the parts are passed directly into the welding enclosure without exposure to room air.

2.4.6 Pre-Cap Inspection

After etching, but prior to final rinsing and baking, a pre-cap inspection is performed according to established MIL-STD-750 Method 2072. The diode is inspected for overall workmanship and for specific quality criteria.

2.4.7 Lid Welding

Subsequent to the stabilization bake, the diode is hermetically sealed. This operation is performed in an enclosed chamber containing pure nitrogen at a dew point of about -90°F.

Setup by a skilled operator is first performed and electrode alignment is accepted by Q.C. after witnessing special imprints made using carbon paper. Samples are then welded and leak tested and again accepted by Q.C. Production welding then proceeds with samples periodically pulled for leak testing to verify that the setup has not changed.

2.4.8 Process Conditioning

After diode assembly, process conditioning is performed in order to stabilize the diode and remove incipient failures. There are recognized failures which occur more frequently than others and these tests are designed to stress the diodes in specific modes to accelerate these "common" failures so that they occur in test rather than in system use.

2.4.8.1 Hermetic Seal Test

All diodes are subjected to a seal check to assure hermeticity. It has been established that leakers causing early system failure are gross in nature. The test performed is the fluorocarbon test specified in MIL-STD-750 which is sensitive to leak rates of 10^{-5} cc/sec. The parts are first pressurized while immersed in a low viscosity fluorocarbon. Leakers are filled with liquid. The parts are then immersed in a second liquid at a temperature exceeding the boiling point of the first liquid forcing it to expand and escape from the filled package. The bubbles generated indicate a leaker.

2.4.8.2 Elevated Temperature Storage

This test is performed according to the specification paragraph 4.5.4 of SCS-481. The devices are placed in stainless steel trays and stored at a temperature within the range of $200^{\circ}C$ to $225^{\circ}C$. Temperature control is within $\pm 3^{\circ}C$.

2.4.9 Final Testing

Final testing is performed in accordance with the specification SCS-481 and the diode specifications MS-50371 and MS-50372 shown in Section 1.3. Details of the test methods are included in Section II in the Acceptance Test Procedure MS-50371/2-1-ATP.

3.0 SUMMARY OF RESULTS - WAFER AND DEVICE PRODUCTION ENGINEERING

3.1 Production Engineering of LHL Read Wafers

3.1.1 Introduction

At the outset of the engineering phase of the program, our objectives were to improve the epitaxial gallium arsenide Read wafer deposition and characterization procedures to a point where the yield of usable wafers met the required fifty percent and the per-wafer cost was reduced to a practical value. The contract required that eighty percent of the area of the wafer be usable (minimum area 3.0 cm^2/wafer). The term usable defines material which meets specifications for dislocation density and doping profile and is capable of producing diodes meeting specification SCS-481, 23 September 1974.

3.1.2 GaAs Epitaxial Wafer Specifications

The first engineering task was to define the epitaxial wafer specifications. A large measure of the performance of a Read IMPATT diode is built in during the growth of the epitaxial wafer from which it is manufactured. The natural frequency and the maximum efficiency of a Read IMPATT oscillator is principally determined by the doping profile of the wafer from which the diode was fabricated. Although it is true that the device characteristics can be modified significantly during the diode manufacturing processes and by the test or operating circuit, the performance is basically limited by the epitaxial wafer characteristics.

The three material characteristics most important to Read device performance are X_p, Q, and n_D. At the outset of the program, the optimum values and the allowable variations of these parameters for material which would yield devices at 10 and

15 GHz meeting specification SCS-481 were not well defined. To determine this, six lots (half at X-band and half at Ku-band) of three wafers each were deposited to the specifications shown in Table 3-1 for standardized diode fabrication and test. The measured characteristics of these wafers are shown in Table 3-2. Three wafers of each lot were processed simultaneously to avoid introducing the effects of process variation into the experiment. Correlation of as-grown wafer characterization and processed wafer data allowed empirical definition of the wafer specifications required to meet diode performance specifications.

The measured device results obtained from these wafers are shown in Table 3-3. From these results, and the results of wafers and devices produced to satisfy other requirements of the engineering phase of the program, wafer specifications were defined. (See Section II.) These were used for the confirmatory and pilot line samples.

3.1.3 Modified Profiles for Higher Efficiency

Throughout the engineering phase of the program, most X-band devices met every specification. Some Ku-band devices, however, were marginal in efficiency. Special wafers were grown with slightly modified profiles in an attempt to improve the yield of Ku-band devices meeting specification.

The profile changes were of two sorts: (a) the amount of undepleted epitaxial material in the transit layer was reduced stepwise to reduce the series resistance, and (b) punch-through devices were made by reducing the transit layer doping and by adding a moderately doped field termination layer located 2.5 to 3.0 micrometers from the avalanche confining spike.

Neither of these profile modifications improved the device efficiency appreciably. For this reason, neither was incorporated into the final wafer specification.

Table 3-1

Specification Definition Wafers Selection Scheme

Lot to Determine Effects of Variation In:	Lot Composed Of:	READ PROFILE PARAMETER VALUES		
		n_D	Q	X_p
Transit Doping (n_D)	Wafer "A" (Control)	Meets Goal	Meets Goal	Meets Goal
	Wafer "B"	>10% Above Goal	Meets Goal	Meets Goal
	Wafer "C"	>10% Below Goal	Meets Goal	Meets Goal
Integrated Charge of Spike (Q)	Wafer "A" (Control)	Meets Goal	Meets Goal	Meets Goal
	Wafer "B"	Meets Goal	>10% Above Goal	Meets Goal
	Wafer "C"	Meets Goal	>10% Below Goal	Meets Goal
Spike Depth (X_p)	Wafer "A" (Control)	Meets Goal	Meets Goal	Meets Goal
	Wafer "B"	Meets Goal	Meets Goal	>10% Above Goal
	Wafer "C"	Meets Goal	Meets Goal	>10% Below Goal

Table 3-2

Measured Properties of Specification Definition Wafers

Wafer No.		Buffer	Transit		Spike				Contact			
Series	Run	W (μm)	W (μm)	$n \times 10^{16}$ (cm^{-3})	W (nm)	$n \times 10^{16}$ (cm^{-3})	$Q^* \times 10^{12}$ ($c\text{-}cm^{-3}$)	V^* (volts)	x_p (μm)	x_o (μm)	$n_o \times 10^{16}$ (cm^{-3})	Band
818	58	6.7	4.0	1.05	52	56	2.5	8.2	0.23	0.18	18	Ku
	63	7.0	4.5	1.30	50	55	2.3	8.1	0.24	0.20	19	Ku
	62	7.0	4.5	0.89	53	50	2.4	8.2	0.24	0.20	14	Ku
	25	5.6	4.0	1.00	53	57	2.5	8.3	0.23	0.19	14	Ku
	48	7.1	4.8	0.98	52	60	2.7	9.8	0.25	0.20	15	Ku
	52	6.9	4.1	1.30	62	39	2.0	6.4	0.22	0.19	18	Ku
	33	5.2	3.9	1.11	40	62	2.4	8.3	0.24	0.20	14	Ku
	41	5.5	4.4	1.02	36	63	2.2	9.9	0.31	0.26	8	Ku
	42	5.8	4.3	1.10	42	65	2.5	8.0	0.22	0.19	21	Ku
816	16	5.0	5.4	0.50	43	56	2.6	9.2	0.24	0.18	9	X
	19	4.1	4.6	0.55	43	56	2.4	8.7	0.23	0.17	9	X
	21	5.1	5.7	0.42	45	53	2.4	9.3	0.25	0.18	6	X
818	93	5.5	4.8	0.50	43	60	2.4	7.6	0.23	0.19	21	X
	94	6.4	5.5	0.54	48	73	2.8	9.6	0.24	0.19	18	X
	97	6.6	5.4	0.52	44	50	2.1	6.9	0.23	0.20	19	X
	80	7.1	4.8	0.57	46	47	2.2	7.9	0.25	0.21	16	X
	88	6.8	5.0	0.60	60	53	2.7	10.4	0.27	0.21	13	X
	82	6.8	4.7	0.59	46	56	2.4	7.5	0.22	0.19	22	X

Table 3-3

Device Results for Specification Definition Wafers

	V* (Volts)	V_{BI} (Volts)	V_{OP} (Volts)	F_o (GHz)	η (%)
Ku Transit Doping					
Wafer 81858 control	5.7	22.1	38.0	14.9	20
81863 high doping	6.7	16.8	31.0	17.0	13
81862 low doping	6.4	18.5	35.0	15.0	17
Ku Spike Charge					
Wafer 81825 control	5.5	21.3	37.0	14.3	19
81848 high Q	6.6	14.7	32.0	15.0	17
81852 low Q	4.1	29.7	44.0	13.5	18
Ku Spike Depth					
Wafer 81833 control	6.3	18.0	36.0	15.0	18.5
81841 deep spike	5.2	21.5	39.0	13.5	20
81842 shallow spike					
X Transit Doping					
Wafer 81616 control	4.8	48.0			
81619 high doping	4.2	58.0			
81621 low doping	6.2	34.0	56.0	8.1	21.5
X Spike Charge					
Wafer 81893 control					
81894 high Q					
81897 low Q					
X Spike Depth					
Wafer 81880 control					
81883 deep spike					
81882 shallow spike					

Note: Early X-band wafers met all requirements and diode evaluation effort was directed to Ku-band wafers. Evaluation of X-band specification definition wafers became unnecessary.

3.1.4 Substrate Doping Specification

In principle, and in practice, the substrate resistivity should be as low as possible in order to achieve maximum device efficiency. This is particularly important at the higher operating frequencies. However, precipitates in the substrates are undesirable because their resistance to chemical etching interferes with etching procedures during device fabrication. This defect has proven to be more critical than is dislocation density. We have, therefore, established upper limits for acceptable precipitate size and density.

We found, during the engineering phase, that more highly doped substrates possessed a greater incidence of large precipitates. Tellurium-doped substrates with a doping density greater than $1.5 \times 10^{18} cm^{-3}$ almost invariably contain excessive numbers of large precipitates. Because of this, substrates with doping densities between 1.0 and $1.5 \times 10^{18} cm^{-3}$ were selected for this program.

3.1.5 Dislocation Density

Dislocation density measurements were made by counting etch pits formed by Abrahams Buiocchi etch. Although this etch is much less satisfactory on the <100> crystallographic orientation than on other orientations, it can be used. For production it was found desirable to define the counting areas photolithographically so that microscope magnification was not critical and counting was not dependent on operator skill.

We found that the etch pit density of substrate and epitaxial layers was not very important to Read IMPATT device performance or yield, provided that the maximum etch pit density of the substrate was less than 10,000 per square centimeter.

3.1.6 Epitaxial Layer Thickness Measurements

One of the requirements was that layer thickness measurements be productionized. The standard method was found to allow adequate processing capacity and was used throughout the program. The method adopted uses stained microsections cleaved from the upper right-hand corner of the wafer. The thicknesses are determined using an image shearing eyepiece on a high quality optical microscope. The measurements are diffraction limited to an absolute precision of about ±0.3 micrometers. For a layer thickness of five micrometers uncertainty of ±6% is introduced in the measurement of thickness and growth rate. The uncertainty in identifying the position of a gradual interface between two differently doped layers, as well as variations introduced by the excessive etching sometimes required to reveal layer boundaries, is added to this. The accuracy achieved in determination of layer thickness is adequate. Deliberate variations in layer thickness by as much as 10% are difficult to detect in device performance.

3.1.7 Doping Profile Measurements

Originally we measured the doping profile on the four corners and the center of the wafer using aluminum Schottky diodes whose dimensions were accurately defined by photolithography and liftoff. After profiling the aluminum Schottky, dots could be removed without damage to the wafer by rinsing in 10% aqueous buffered H.F.

Unfortunately, breakdown and leakage limited the depth to which the sample could be profiled. This could be tolerated for flat-profile IMPATTs, but Read wafers required deep profiling in order to characterize them adequately for production. A method was evolved during the engineering phase which permitted adequate information to be obtained to qualify Read wafers for production processing.

A measurement sample is taken by cleaving a small strip off the right-hand edge of the wafer. This is step-etched in a closely contiguous area. Planar aluminum-gold Schottky discs are prepared by a combination of photolithography and vacuum vapor plating. The profile is measured on our automatic profilometer. Surface breakdown limits the depth which can be profiled. Therefore, the profile is synthesized by joining several partial profiles together.

The design of the characterization sample evolved through several stages during the engineering phase. For the first few months of the program it consisted of several arrays, each comprised of four 0.125 x 0.125 cm close spaced squares each etched to a different depth. Planar aluminum Schottky discs 0.040 cm in diameter were centered in each square. We occasionally experienced difficulty in making good electrical contact to the aluminum Schottky discs because thin oxide surface films formed upon exposure to air. This was corrected by evaporating a thin gold overlay over each dot.

Later, we found that four etch steps often yielded insufficient information for Read IMPATT wafer qualification so we expanded each array to six etch squares, still closely spaced. Even six etch steps sometimes yielded inadequate information about the profile, so a new mask set was designed in which each array was comprised of eight etch squares. It was found desirable to leave at least two squares of each array unetched so that the depth and integrated charge of the spike could be determined unambiguously.

The doping profile for Read wafers is determined from measurements upon the planar Schottky barrier diodes of precisely measured area centered in the etch squares. By changing the reverse bias voltage upon the diode, while simultaneously

measuring the capacitance and change of capacitance, we obtain data from which the free carrier concentration through epitaxial layer can be computed. At Raytheon, this calculation is performed simultaneously with the measurement by an analog computer, and the profile is outputted on an X-Y recorder.

In production, it is desirable to measure the characteristics of the spike of the LHL Read after processing into chips and packaged diodes. Comparisons can then be made with the original wafer data to determine consistency of wafer and processing, and to troubleshoot production problems. Routine doping profile measurements on processed chips and diodes are not feasible because of the uncertainty in their area. The percentage error in a measured doping profile is approximately double the percentage error in the assumed or measured diode area.

To overcome this difficulty, we defined an electrical parameter, V*, derived from the capacitance versus reverse bias voltage plot of a diode. Since this parameter is independent of diode area, it can be measured upon processed chips and packaged diodes, as well as upon the wafer characterization sample. If a capacitance versus reverse bias voltage plot of a typical LHL Read diode (Figure 3-1) is examined, a large voltage interval will be found over which $\frac{dc}{dv}$ is small. In this voltage interval, the free carriers are being depleted from the doping spike. Likewise, the transition to a significantly larger $\frac{dc}{dv}$ corresponds to the edge of the carrier depletion region entering the transit layer. We have designated the intersection of the transit region C-V asymptote and the spike C-V asymptote as V*.

The area under the capacitance versus voltage plot is proportional to the number of charge carriers per unit area in the depletion region. Thus, the charge, Q, in the spike can be found from the area under the C-V plot between the capacitance corresponding to the leading edge of the spike and the capacitance

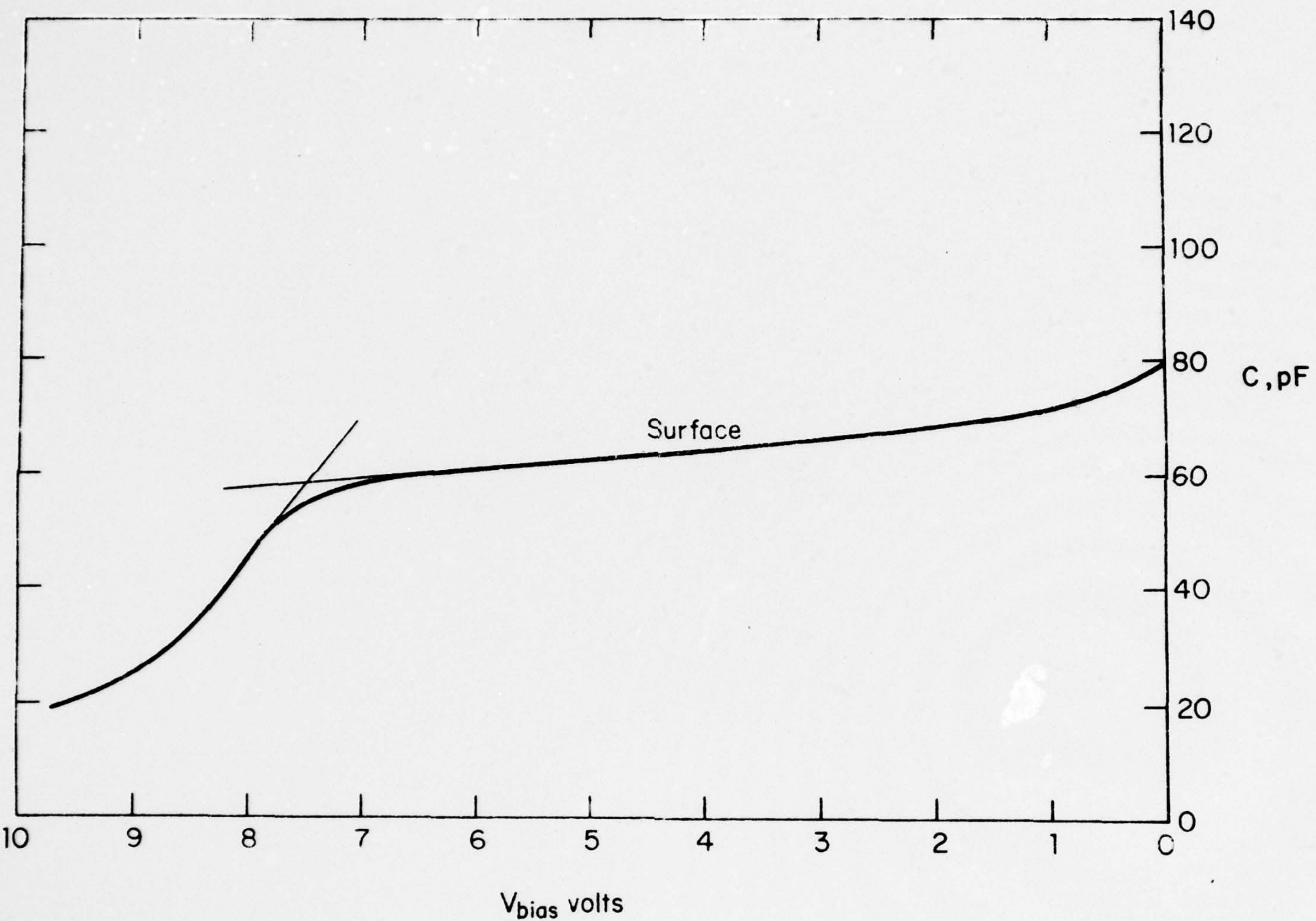

Figure 3-1 Typical Capacitance versus Voltage Plot for Read-Profile IMPATT Diode

corresponding to the trailing edge of the spike. In wafers grown for this program, the leading edge of the spike is approximately located at the surface of the wafer, and the trailing edge is approximately at the capacitance, C*, corresponding to V*. The area under the capacitance-voltage plot can be approximated as a rectangle with altitude $\bar{C}$, the mean capacitance, and length V*. Thus, Q is proportional to $\bar{C}$ x V* and $\bar{C}$ is proportional to X_p.

3.1.8 Wafer Uniformity

Data acquired in the early stages of the program indicated that the breakdown voltage of the finished devices displayed considerable variation over most wafers. An example is shown in Figure 3-2. The variation is particularly evident from top to bottom of the wafer. We concluded from the preliminary data that the spike depth was the most critical parameter and this can be deduced from measurements of V*. The correlation of V* with breakdown voltage for this same wafer is shown in Figure 3-3.

The question remained, however, as to how much of the observed variation was introduced in wafer deposition, and how much was introduced in dice fabrication. An experimental wafer, 81869, was especially processed to determine this. The wafer, after deposition, was metallized with evaporated platinum through a photolithographic mask and liftoff so as to produce an array of planar diodes 0.007 inches in diameter spaced 0.025 inches on center. Platinum was chosen for the metallization to be compatible with subsequent standard diode processing techniques. V* values were measured upon each diode. Figure 3-4 is a map of the results before device processing. The V* values shown in Column 9 on the right-hand side of the wafer are those measured on the standard 0.016 inches in diameter aluminum gold planar diodes on the characterization sample. These values are in good agreement with those measured on the nearby platinum diodes. It should be noted

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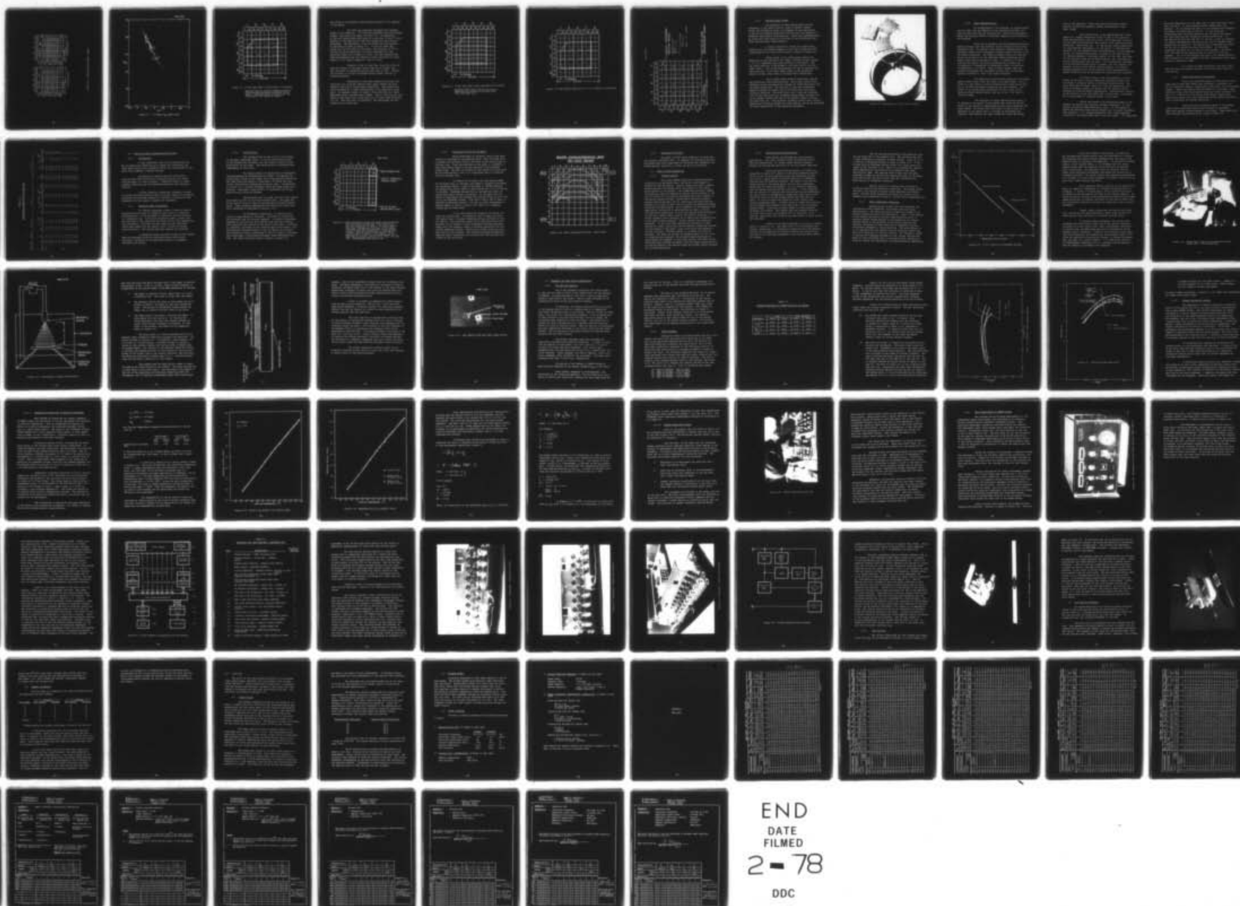

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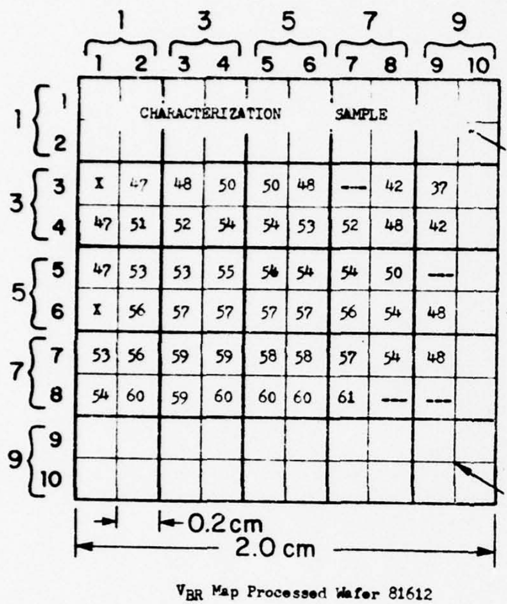
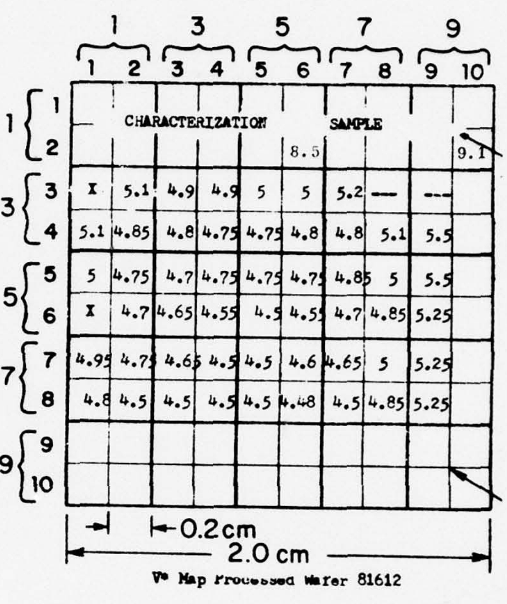


	1	2	3	4	5	6	7	8	9	10
1		CHARACTERIZATION				SAMPLE				
2										
3	X	47	48	50	50	48	—	42	37	
4	47	51	52	54	54	53	52	48	42	
5	47	53	53	55	54	54	54	50	—	
6	X	56	57	57	57	57	56	54	48	
7	53	56	59	59	58	58	57	54	48	
8	54	60	59	60	60	60	61	—	—	
9										
10										

V_{BR} Map Processed Wafer 81612



	1	2	3	4	5	6	7	8	9	10
1		CHARACTERIZATION				SAMPLE				
2						8.5				9.1
3	X	5.1	4.9	4.9	5	5	5.2	—	—	
4	5.1	4.85	4.8	4.75	4.75	4.8	4.8	5.1	5.5	
5	5	4.75	4.7	4.75	4.75	4.75	4.85	5	5.5	
6	X	4.7	4.65	4.55	4.5	4.55	4.7	4.85	5.25	
7	4.95	4.75	4.65	4.5	4.5	4.6	4.65	5	5.25	
8	4.8	4.5	4.5	4.5	4.5	4.48	4.5	4.85	5.25	
9										
10										

V_o Map Processed Wafer 81612

Figure 3-2 Characteristics Map - 81612

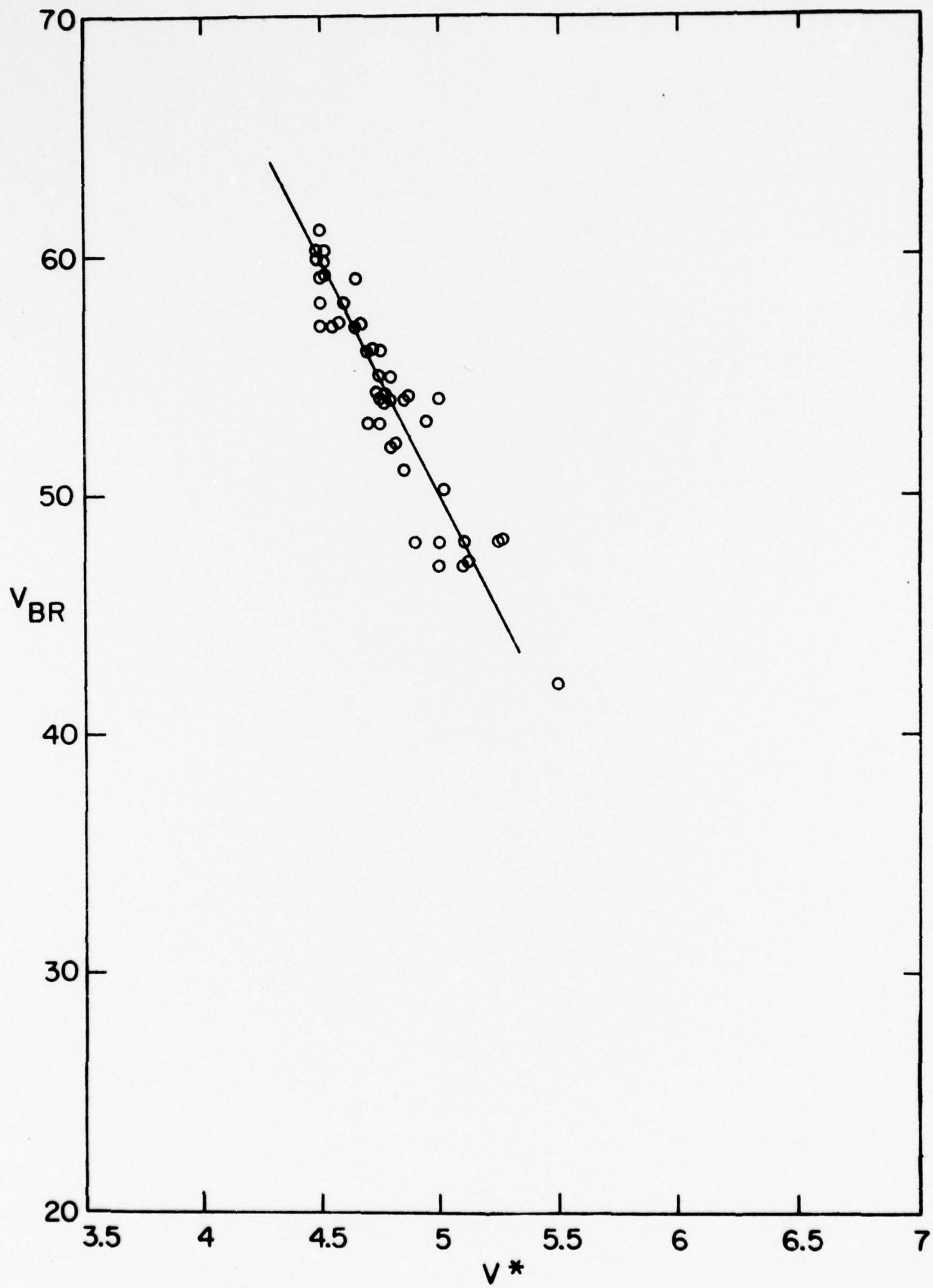


Figure 3-3 V* Versus V_{BR} Wafer 81612

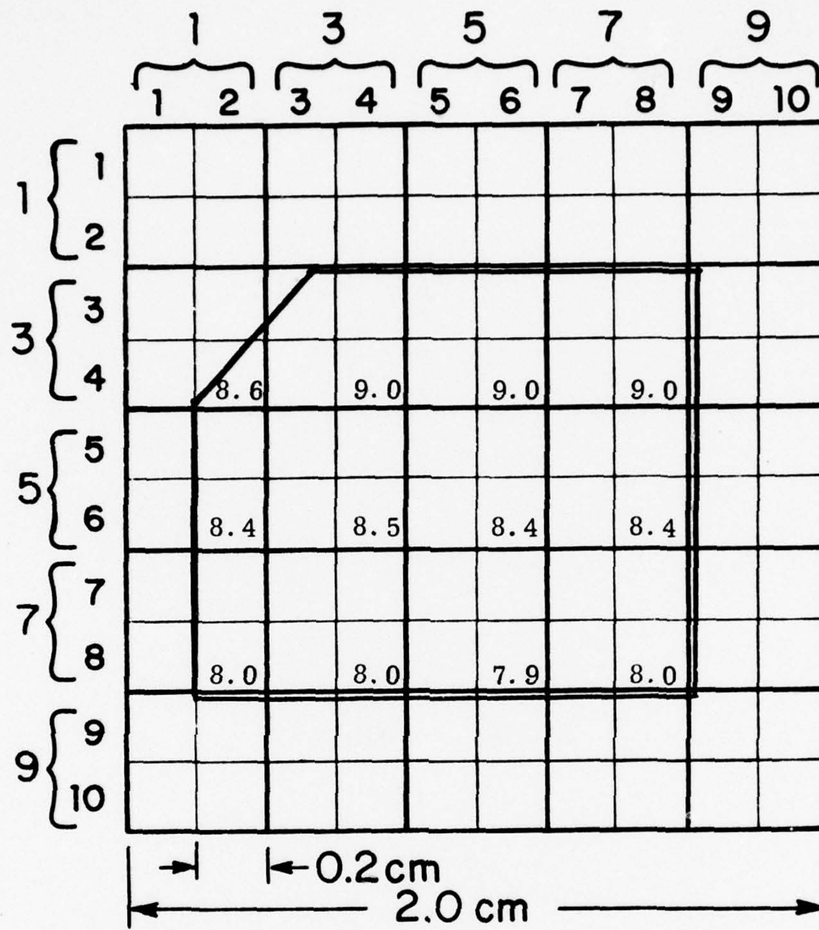


Figure 3-4 V* Map upon Wafer as Delivered to Processing.

Measured upon an array of evaporated planar platinum Schottky diodes formed on wafer 81869. Diode diameters are nominally .007 inch spaced .025 inches on center.

that there is considerable top-to-bottom variation in V* measured on this wafer.

The wafer was thereupon processed into standard diodes in the usual way. V* values were measured upon the finished diodes. The results are shown in Figure 3-5. An examination of the two figures shows that there is a reduction in the V* value measured in the same area of the wafer before and after device processing. The difference in the two values for each location on the wafer is shown in Figure 3-6. It will be noted that, except for the very edges of the wafer, the reduction in V* resulting from dice fabrication is fairly consistent for this particular wafer and is about 2.3 volts. We have observed from other measurements that the reduction varies from wafer to wafer; however, it is usually between 2.5 and 3.5 volts.

Figures 3-4 and 3-5 show that the chief variation over the surface of the wafer occurs from top to bottom, and that the wafer is remarkably uniform from side to side. Further, the variation is chiefly introduced during growth, and not in device processing.

Examination of the wafer deposition process indicated that the variation results from a small thermal and flow gradient from top to bottom during deposition. This problem was easily remedied by a slight modification of the deposition equipment. For example, Figure 3-7 shows a full wafer map of a wafer deposited using a modified wafer holder. The V* variation for this wafer is very small with a mean value of 6.36 and a mean deviation of 2.7%. With this sort of uniformity, the requirement for 80% usable area is easily met.

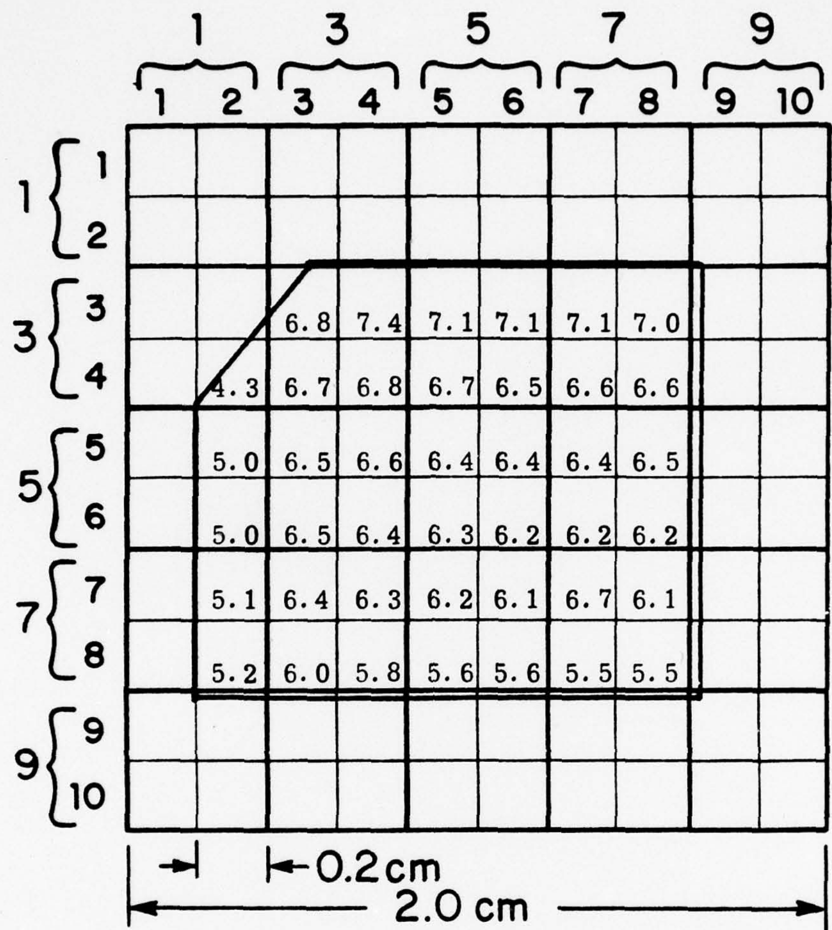


Figure 3-5 V* Map upon Wafer after Processing into Diodes

Measured after mesa etching but prior to separation by etching of the heat sink into individual die.

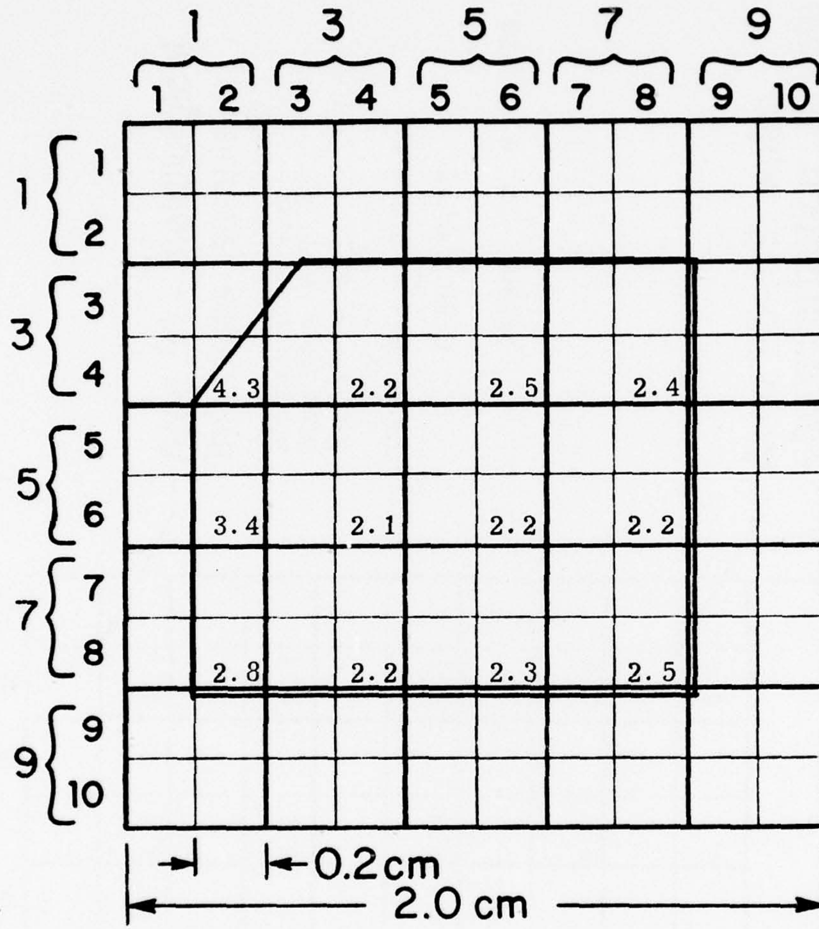


Figure 3-6 Map Showing Reduction in V* as a Result of Processing

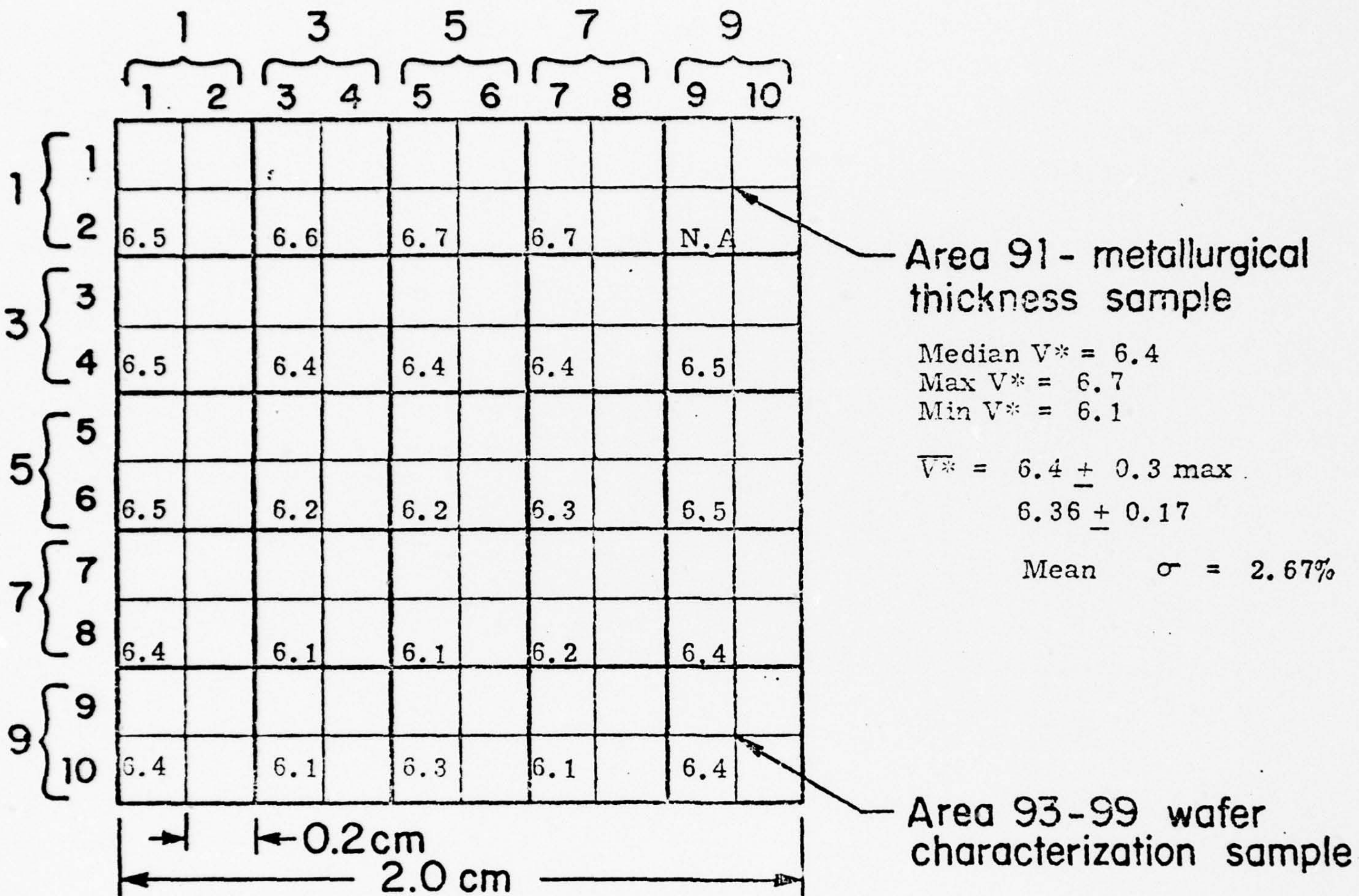


Figure 3-7 As Grown V* Map of Full Wafer
Read Wafer 81632

3.1.9 Multiple Wafer Growth

The production of Read devices would be more economical if the wafers could be grown in greater volume. During the engineering phase, we attempted to grow Read wafers in one of our standard production reactors which are capable of producing three wafers simultaneously. After some experimentation we found that three wafers can be grown to the preliminary Read wafer specifications simultaneously.

A holder constructed to hold the three wafers coplanar and with maximum symmetry in the vapor stream was used. A photograph of the triple wafer holder is shown in Figure 3-8.

Wafers grown in the triple wafer reactor are designated by the deposition run number, followed by the letters A, B, or C, depending upon wafer position in the holder. The top center position is designated A, the lower left B, and the lower right C. The latter designations are used to describe the wafer position in the triple wafer holder in the production reactor in both single wafer or multiple wafer depositions.

Two of three wafers grown in particular runs met the preliminary wafer specifications. Each triple wafer holder possesses unique characteristics because of slight deviations from the design dimensions. The one used to grow the confirmatory samples produced two wafers (the A and B position) which were virtually identical. The other wafer (the C position) although still within specifications, possessed layers which averaged five to ten percent thinner and five to ten percent higher in doping than the other two. This deviation probably results from a slight temperature difference between the three wafers, and can be minimized by slight modification of the deposition equipment.

Figure 3-8 Photograph of Triple Wafer Holder

3.1.10 Wafer Reproducibility

At the beginning of this program, an as-grown wafer yield of about 20% was obtained to the required tolerances, and this was much less than the required 50%. During the engineering phase, the principal effort in epitaxial deposition was directed to this problem.

The yield of epitaxial gallium arsenide Read wafers depends strongly upon the epitaxial reactor design and the growth procedures used. To achieve a high degree of reproducibility, the epitaxial reactor must be designed to permit precise control of all the growth conditions. The growth procedures which are used must be set up so that all of the important growth conditions can be exactly duplicated from wafer to wafer. In addition, to obtain high quality wafers, the growth procedures must prevent the introduction of unsuspected or undesirable layers, transitions, or properties in the wafer. These criteria mandate that the reactor be equipped with precision controls, and, to eliminate operator variability, that it be highly automated.

Our experience indicates that there are three major growth factors which limit the yield of LHL Read wafers. One of these is a slow change in wafer characteristics which occurs from run to run when the process conditions are held constant. The second is an unpredictable fluctuation of one or more of the important wafer characteristics from run to run. The third is start-up losses.

The slow drift in wafer characteristics seems to be related to the length of the elapsed time after the gallium source in the reactor is replenished and the system saturated and vapor etched. We believe that this effect is due in part to a depletion in the source and to a buildup of disordered well deposits; these deplete the vapor stream and reduce the growth

rate at the substrate. These also serve as secondary doping sources, introducing systematic dopant fluctuations in the vapor stream.

The second factor in the reproducibility of Read wafers is a random fluctuation of one or more of the important wafer characteristics from run to run. We believe this to be due to very small fluctuations in one or more of the important growth conditions. Among these are: (1) the gallium source temperature, (2) the substrate temperature, (3) the arsenic trichloride mole fraction, (4) the substrate size and orientation, (5) the substrate doping, (6) unintentional vapors or gasses in the vapor stream, (7) residual dopants in the vapor stream, (8) the total gas flows, (9) the relative flows of the various gasses, (10) the condition of the gallium source and its crust, (11) unintentional contamination of the wafer surface prior to growth, and (12) sporadic malfunction of one or more reactor control modules. To achieve maximum reproducibility of the important wafer characteristics, growth conditions must be monitored and controlled very carefully.

The third factor in the reproducibility of Read wafers is the use of long run sequences comprised of many runs all aimed at producing wafers to identical specifications. For every wafer specification, there is a start-up sequence of runs which is necessary before the reactor and the operator become adjusted to producing wafers reproducibly. Unfortunately, because so many devices can be fabricated from a single wafer, the demand for a large number of identical wafers is not usual.

During the course of the engineering phase of the program, we adopted the following standard procedures: (1) The gallium source was replenished once a week. (2) The deposition system was routinely vapor etched between runs to remove disordered wall deposits. (3) A standard substrate size, crystallographic orientation, and doping were used in each run series. (4) Substrates

were used sequentially in the same order in which they were sliced from the boule. (5) Each substrate boule constituted a run sequence. (6) All deposition runs in a run sequence were scheduled for exactly the same time of the day. (7) All flows and temperatures were carefully monitored and corrective maintenance was instituted upon any indication of minor malfunction. (8) The same silica ware was used for all runs of a given run sequence. (9) Careful documentation was kept of all lots of reagents used in depositions and cleaning. The results were correlated with these, and the use of dubious lots was discontinued. (9) Identical procedures were used for all runs of a run sequence. To ensure this, the same reactor operator made all runs of a given run sequence. (10) A running account was kept of the characterization data of wafers in a run sequence, and when trends were noted, minor corrective steps were taken.

As a result of these procedures, the wafer yield after the startup sequence required for any particular specification was 50%.

3.1.11 Wafers Delivered for Processing

During the engineering phase of the program, forty-eight device grade Read wafers were delivered to processing for use as engineering samples, specification definition, and confirmatory samples. These were equally divided between Ku and X-band. These wafers and their measured characteristics are listed in Tables 3-4 and 3-5. In addition to the device grade wafers, twenty-eight Read profile wafers and fifty unspecified profile wafers were delivered to processing for process evaluation.

During the pilot production phase of the program, twelve device grade Read wafers were delivered to processing. These were equally divided between Ku and X-band. These wafers and their measured characteristics are listed in Table 3-6.

Table 3-4

X-Band Wafers Supplied for Device Fabrication, Engineering Phase

Wafer No.		Buffer	Transit		Spike				Contact			
Series	Run	W (μm)	W (μm)	$n \times 10^{16}$ (cm^{-3})	δ (nm)	$n_p \times 10^{16}$ (cm^{-3})	$Q^* \times 10^{12}$ ($e\text{-}cm^{-2}$)	V^* (volts)	x_p (μm)	x_o (μm)	$n_o \times 10^{16}$ (cm^{-3})	Band
816	03	13.5	4.4	0.54	48	54	2.3	9.2	0.26	0.18	6	X
	06	5.2	5.1	0.49	45	56	2.6	8.6	0.25	0.18	8	X
	08	5.2	4.9	0.51	46	55	2.5	9.4	0.26	0.18	6	X
	12	4.9	4.9	0.51	44	57	2.4	8.8	0.25	0.18	7	X
	16	5.0	5.4	0.50	43	56	2.5	8.5	0.24	0.18	9	X
	19	4.1	4.6	0.55	43	56	2.4	7.7	0.23	0.17	9	X
	21	5.1	5.7	0.42	45	56	2.4	8.7	0.26	0.18	6	X
	46	6.0	5.3	0.56	45	56	2.3	7.5	0.23	0.20	17	X
	53	5.9	4.8	0.54	42	73	2.7	9.4	0.24	0.20	19	X
818	80	7.1	4.8	0.57	46	47	2.2	7.9	0.25	0.21	16	X
	82	6.8	4.7	0.59	46	56	2.4	7.5	0.22	0.19	22	X
	88	6.8	5.0	0.60	60	53	2.7	10.4	0.27	0.21	13	X
	93	5.5	4.8	0.50	43	60	2.4	7.6	0.23	0.19	21	X
	94	6.4	5.5	0.54	48	73	2.8	9.6	0.24	0.19	18	X
	95	6.4	4.9	0.54	45	63	2.5	8.4	0.24	0.20	17	X
	97	6.6	5.4	0.52	44	50	2.1	6.9	0.23	0.20	19	X
	99	6.2	5.0	0.48	43	62	2.3	8.0	0.24	0.20	20	X
819	00	6.2	5.0	0.45	42	64	2.3	8.0	0.24	0.20	15	X
325	28	5.2	5.1	0.56	34	79	2.2	7.8	0.24	0.22	28	X
	29	5.3	5.0	0.56	32	82	2.5	8.7	0.24	0.22	24	X
413	19A	4.9	4.6	0.51	50	46	2.6	8.9	0.24	0.19	11	X
	19B	5.1	4.7	0.50	50	45	2.3	8.1	0.24	0.19	12	X
	20A	5.2	5.1	0.49	52	42	2.5	8.6	0.24	0.19	11	X
	20B	5.7	5.4	0.49	52	43	2.3	8.1	0.24	0.19	13	X

Table 3-5

Ku-Band Wafers Supplied for Device Fabrication, Engineering Phase

Wafer No.		Buffer	Transit		Spike				Contact			
Series	Run	W (μm)	W (μm)	$n \times 10^{16}$ (cm^{-3})	δ (nm)	$n_p \times 10^{16}$ (cm^{-3})	$Q^* \times 10^{12}$ ($e\text{-}cm^{-2}$)	V^* (volts)	x_p (μm)	x_o (μm)	$n_o \times 10^{16}$ (cm^{-3})	Band
815	56	6.2	6.1	0.77	44	66	2.9	11.4	0.27	0.19	7	Ku
	57	5.9	5.2	0.84	44	61	2.7	9.7	0.25	0.19	8	Ku
	60	5.7	5.9	0.78	46	55	2.3	8.6	0.25	0.19	7	Ku
	61	5.9	5.9	0.82	38	57	2.4	9.4	0.27	0.19	5	Ku
	70	5.5	5.8	0.81	44	56	2.5	9.3	0.26	0.19	6	Ku
818	25	5.6	4.0	1.00	53	57	2.5	8.3	0.23	0.19	14	Ku
	30	5.7	4.3	1.05	47	57	2.2	7.8	0.24	0.20	14	Ku
	31	5.9	3.8	1.13	45	59	2.3	7.6	0.22	0.19	19	Ku
	33	5.2	3.9	1.11	40	62	2.4	8.3	0.24	0.20	14	Ku
	37	5.8	4.1	1.10	44	60	2.5	8.9	0.24	0.20	9	Ku
	41	5.5	4.4	1.02	36	63	2.2	9.9	0.31	0.26	8	Ku
	42	5.8	4.3	1.10	42	65	2.5	8.0	0.22	0.19	21	Ku
	44	5.5	4.0	1.20	41	63	2.4	8.1	0.24	0.20	19	Ku
	45	5.4	4.3	1.10	40	63	2.3	8.0	0.24	0.21	19	Ku
	48	7.1	4.8	0.98	52	60	2.7	9.8	0.25	0.20	15	Ku
	52	6.9	4.1	1.30	62	39	2.0	6.4	0.22	0.19	18	Ku
	53	6.7	3.6	1.10	52	56	2.5	8.5	0.24	0.19	18	Ku
	58	6.7	4.0	1.05	52	56	2.5	8.2	0.23	0.18	18	Ku
	62	7.0	4.5	0.89	53	50	2.4	8.2	0.24	0.20	14	Ku
	63	7.0	4.5	1.30	50	55	2.3	8.1	0.24	0.20	19	Ku
820	10	6.5	4.3	1.10	50	43	2.3	8.2	0.25	0.20	18	Ku
413	28A	4.5	3.5	1.03	46	44	2.4	8.0	0.23	0.19	11	Ku
	28B	4.8	3.7	1.06	46	43	2.4	7.9	0.23	0.18	11	Ku
	30C	5.6	4.5	1.15	50	43	2.3	8.3	0.25	0.20	10	Ku

Table 3-6

Read Wafers Supplied for Pilot Run

Wafer No.		Buffer	Transit		Spike				Contact			
Series	Run	W (μm)	W (μm)	$n \times 10^{16}$ (cm^{-3})	δ (nm)	$n_p \times 10^{16}$ (cm^{-3})	$Q^* \times 10^{12}$ ($c\text{-}cm^{-2}$)	V^* (volts)	x_p (μm)	x_o (μm)	$n_o \times 10^{16}$ (cm^{-3})	Band
414	27A	4.8	4.2	1.1	55	40	2.2	7.7	0.24	0.19	7	Ku
	28B	4.3	3.9	1.2	61	36	2.2	7.3	0.23	0.19	8	Ku
	35B	4.2	4.0	1.0	45	55	2.5	8.3	0.23	0.19	10	Ku
	36A	4.5	4.3	1.1	45	55	2.5	8.6	0.24	0.20	10	Ku
	36B	4.5	4.3	1.0	45	52	2.3	8.4	0.25	0.20	10	Ku
	37B	4.2	3.9	1.0	44	49	2.2	7.2	0.23	0.19	11	Ku
414	10A	5.1	5.1	0.50	70	35	2.4	8.2	0.23	0.19	9	X
	10C	5.2	5.3	0.52	74	33	2.4	8.8	0.25	0.20	7	X
	11A	4.9	4.9	0.52	66	36	2.4	8.3	0.24	0.19	8	X
	13A	4.7	4.6	0.53	68	33	2.3	7.5	0.23	0.18	9	X
	15A	4.8	4.8	0.49	69	34	2.4	8.2	0.24	0.19	8	X
	15B	4.8	4.8	0.48	68	34	2.3	8.1	0.24	0.18	8	X

3.2 Wafer and Device Characterization Effort

3.2.1 Introduction

It was recognized early in the program that the key to meeting the objectives was a method for translating the final diode results into parameters which could be measured at the wafer level assuming a constant process.

Variability of results had been sufficiently large so that diode results from a specific portion of a wafer were desirable, at least initially. Suspected effects of diode assembly operations upon the measured parameters also required a solution.

A wafer evaluation system was, therefore, devised to provide thorough evaluation data at several stages of processing. The system has provided information concerning variation in wafer parameters and has helped to improve the uniformity.

3.2.2 Epitaxial Wafer Orientation

To identify systematic trends in wafer or device performance which might be correlated with reactor or substrate characteristics, it was desirable to reference the wafer position in a systematic way. During the engineering phase, a small mask was scratched in the right-hand top corner of the wafer immediately after polishing. This mask routinely made the top right-hand corner when loaded into the reactor and is cleaved off during characterization. The cleaved edge then becomes the reference.

A coordinate system oriented relative to the cleaved edge was developed during the engineering phase and allowed positional information to be maintained during all subsequent processing and testing.

3.2.3 Profile Strip

The cleaved corner of the 2.0 cm x 2.0 cm wafer is the upper right-hand corner. A 0.4 cm wide vertical strip is now removed from the wafer, and this strip is used for characterization of the wafer. The doping profile is obtained from measurements on this strip.

The doping profile for Read wafers is determined from measurements on Schottky barrier diodes. By changing the reverse bias voltage on the diode, while simultaneously measuring the capacitance and change in capacitance, we deduce the free carrier concentration through the epitaxial layer. As explained in Section 3.1.7, surface breakdown limits the depth which can be profiled. Therefore, a deep profile is synthesized by joining several partial profiles together.

The profiling uses the lower portion of the profile strip wafer and 80% of the total available area. The upper 20% of the profile strip is used for metallurgical thickness measurements. These thickness measurements are obtained by cleave and stain techniques as described in Section 3.1.6.

To standardize terminology, an imaginary grid system is superimposed on the wafer. The wafer is divided into ten horizontal and ten vertical segments. A two-digit coordinate composed by listing first the X-section and then the Y-section thus identifies the location of any point on the wafer. Profiling is, therefore, performed in the 93-99 sections of the wafer. The metallurgical thickness sample is the 9-1 section of the wafer. The orientation cleave is performed in the 9-1 corner of the wafer. This terminology is maintained throughout wafer processing into dice. The wafer coordinate system is shown in Figure 3-9.

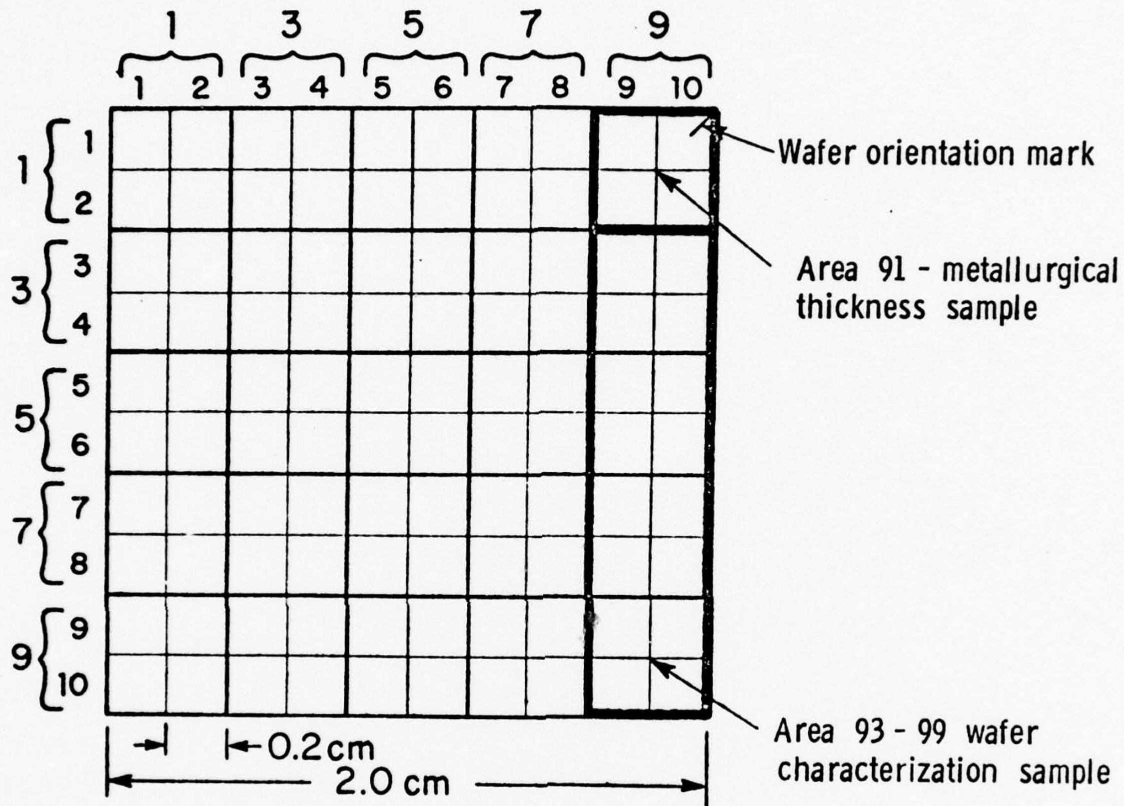


Figure 3-9 Wafer Coordinate System and Sample Area Assignment. The coordinates are deciles of horizontal and vertical length of the wafer. To avoid three or four digit designation for areas of the sample including more than one position, pairs of horizontal or vertical coordinates are indicated by a single digit as shown in the figure. As an example, the 0.4 cm x 0.4 cm metallurgical thickness sample includes positions 9-1, 10-1, 9-2, and 10-2. We designate this area as 91.

3.2.4 Evaluation of Dice on the Wafer

During processing of the wafer, most of the operations are performed on the substrate side. When the diode array is etched, the epitaxial side of the wafer is the side closest to the heat sink. Probe data obtained on the wafer is, therefore, a left-right mirror image of the data derived at the epitaxial growth stage. The data is recorded in this manner on a work sheet by the probe operator, and it is transcribed later to correlate with the original data.

In probing of the wafer, the grid system formed by the diode array is utilized, and diodes at selected coordinates are thoroughly tested. A map of the wafer is thereby obtained. By probing every fourth diode in every fourth row, a 10 x 10 matrix is obtained. Breakdown voltage data is recorded and a plot of capacitance versus voltage is obtained. At the same time, the values of capacitance are recorded for voltage values at zero volts and at the breakdown voltage. From the C-V plot, the V* value is obtained as described earlier. The data is later transcribed to summary sheets as shown in Figure 3-10, which is a breakdown voltage map for wafer 81653.

In the form presented, parameter variations on a wafer are clearly seen. An example of this is shown in Figure 3-10 where lines of constant breakdown voltage are drawn in over the figures. The variations shown can be explained by gas flow patterns in the reactor or other processing peculiarities which might occur; for example, during a sintering operation with non-uniform substrate heating. Minimizing of these variations was a major goal of this program. The evaluation system developed has supplied useful information for analyzing the factors which contribute to the variations.

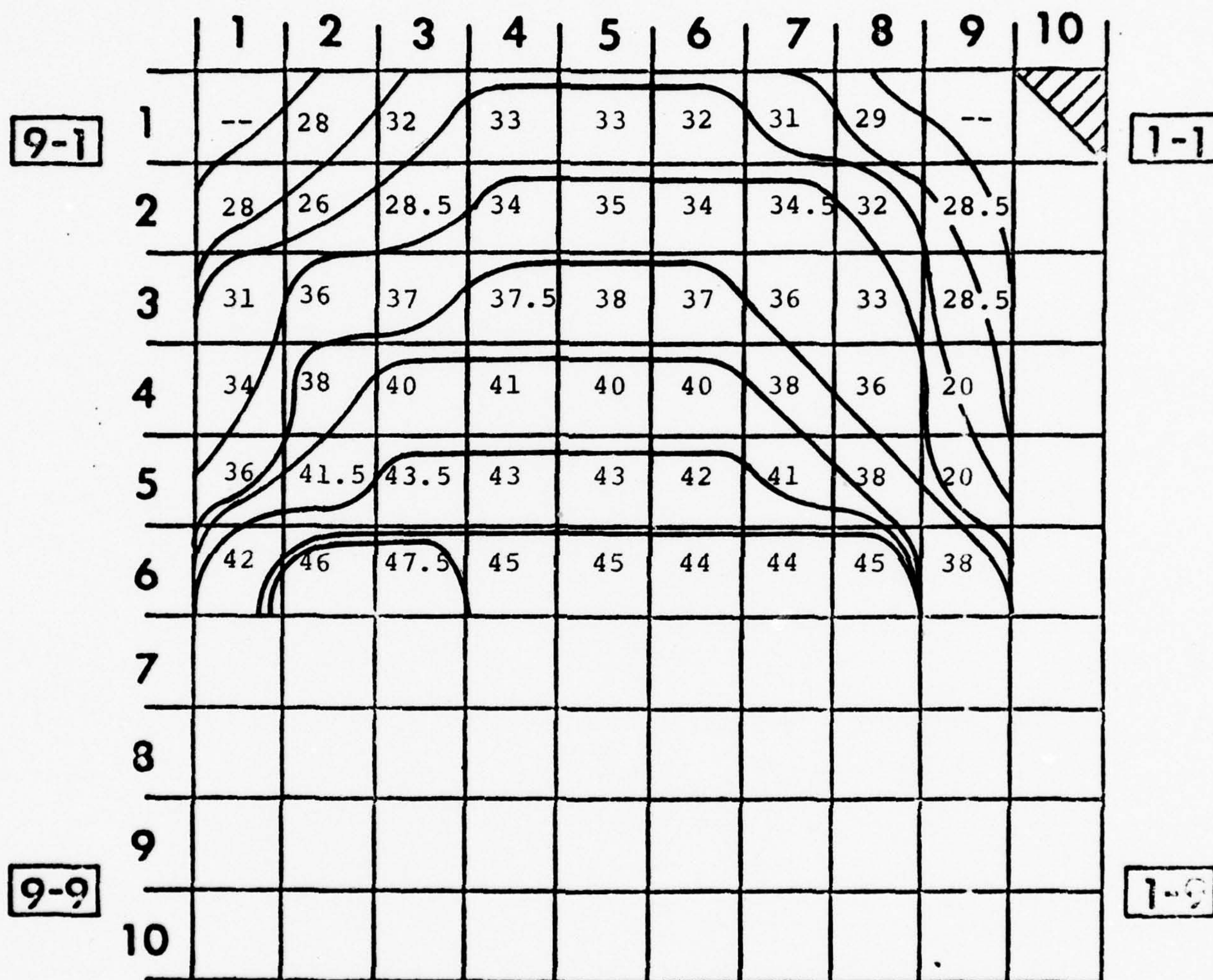


Figure 3-10 Wafer Characteristics Map - Wafer 81653

3.2.5 Evaluation of Diodes

The wafer is diced after evaluation to yield several hundred individual dice. To complete the evaluation process, procedures have been established for selecting and assembling into diodes specific portions of a wafer for RF test evaluation.

3.3 Wafer Process Engineering

3.3.1 Sputter Etching

Early Read IMPATT diode work included mechanical tailoring of the epitaxial layer just prior to processing to achieve the desired profile. Sputter etching was used to remove surface material and thereby alter the position of the doping spike relative to the surface. This sometimes entailed a number of evaluation steps and repetitive sputter etching because of the lack of control to the required tolerances which are inherent in the sputter etching process. Wafers which required extensive sputter etching generally did not yield high efficiency devices, probably as a result of both lack of control and mechanical damage resulting from the process. As an expedient, we had proposed that many wafers, falling out of specification as grown, could be tailored during manufacture to yield the desired diode performance. In this way a usable wafer yield of 50% could be achieved. A better procedure would obviously be to improve the reproducibility of the wafer growth processes. Sputter etching was eventually abandoned. It was found that removing and evaluating a small section of a wafer yields very little reliable information concerning the balance of the wafer. Even if the wafer were perfectly uniform initially, different results in a second run would be possible. The wafer can quickly be consumed merely in evaluation if iterations are required. By straightforward processing of whole wafers and feedback of final data instead, the wafer growth conditions were adjusted and wafers with the proper characteristics are now available at the required rates and yields without reliance on tailoring operations.

3.3.2 Schottky Barrier Metallization

Three metals are sputtered onto the epitaxial GaAs surface. The first, platinum, forms the Schottky barrier, while the second metal, Ti, forms a metal diffusion barrier between the platinum and gold which is the third metal deposited.

During the metallization process, the wafers are subjected to heating as a result of intentional substrate heating as well as by the heat generated during the deposition process. As a result, a small amount of gallium arsenide is consumed by reaction with the deposited platinum. The effect is to move the surface closer to the doping spike, and this has a measurable effect upon the device performance. It is, therefore, important that the sputter operation be well controlled. It was suspected that the reaction of platinum with the surface GaAs was responsible for the variation in parameters of diodes fabricated from a wafer. Controlled tests during the program showed that this does not occur. An array of diodes was formed on a wafer using a non-reactive evaporated metal. A second array of diodes using platinum as the Schottky was disposed on the same wafer in the land areas between diodes. Both sets of diodes showed the same parameter variation on the wafer. This showed that the parameter variation in diodes from a wafer was primarily due to variations in the epitaxy. Recognizing this, significant improvements in wafer epitaxy were realized.

Results of the above experiment are cited in greater detail in Section 3.1.8. The reduction of V* with processing was further investigated. In transferring technology from the Research Division it was observed that variable results were realized from portions of the same wafer processed at two locations using identical systems.

Half of each was metallized on the production unit, and the other half on the research unit. The conclusion was that a minor difference in parameter averages existed. A plot of V* as a function of breakdown voltage is shown in Figure 3-11. It may be seen that the breakdown voltage varies in a linear manner as a result of the variation in V*. There is a discontinuity, however, which separates the units metallized at Research from those metallized at SMDO. The observed results imply that the wafer processed at SMDO has the Schottky positioned closer to the doping spike which means that more surface GaAs was consumed during metallization or subsequent processing.

Results from the two systems were equalized by carefully examining the deposition conditions. The largest effect was found to be caused by unequal target dimensions and sputter power. The Read diode manufacturing process was shown to be as dependent upon processing as upon the original wafer characteristics.

3.3.3 Wafer Dimensional Tolerances

Specifications of wafer size and thickness, and tolerances on these dimensions, were absent from early wafer specifications. The wafer was parallel lapped and etched to the required dimensions during dice fabrication. Early in this program, it was thought desirable to perform these operations prior to epitaxial growth instead because of the possibility of inducing abrasive damage to the epitaxial surface during mounting and handling, and because of the difficulty of adequately cleaning the surface subsequent to these operations. The wafer surface is in its optimum state upon removal from the epitaxial reactor and that is the best time to form the junction. We, therefore, intend to develop the techniques necessary to lap, polish, and etch the wafer to tight tolerances prior to epitaxial growth, perform the epitaxial growth, and then deposit the Schottky barrier immediately.

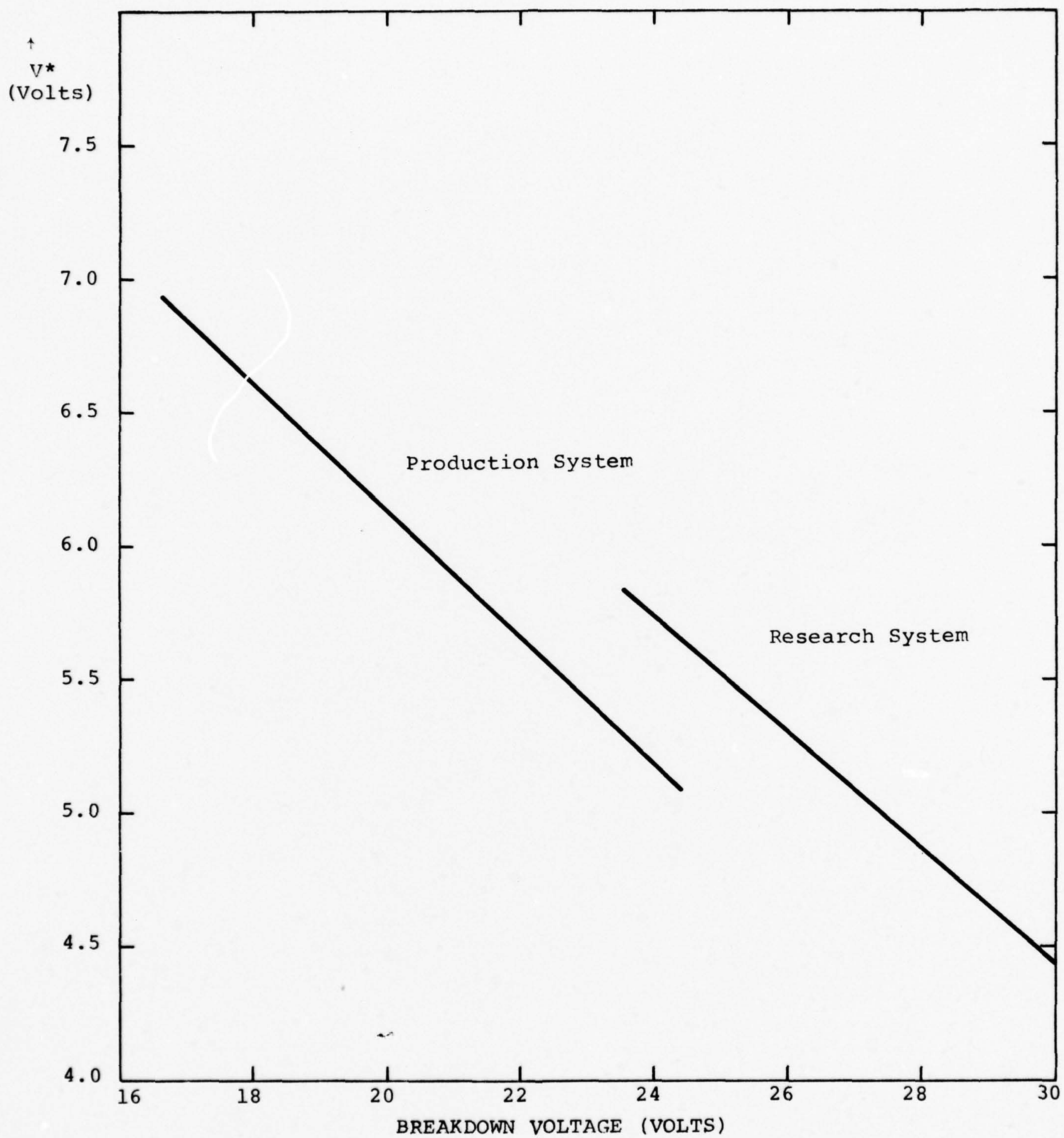


Figure 3-11 V* as a Function of Breakdown Voltage

During the course of this effort, we found that the finished wafer surface quality and the conformance to flatness and thickness goals were strongly dependent upon the state of the substrate prior to polishing and deposition. To achieve the highest quality in the finished wafer, it is necessary that the single crystal slices used for substrates be as identical as possible prior to polishing. The substrate slices as received from the vendor often displayed unacceptable saw damage and slice-to-slice thickness variation. We worked closely with substrate manufacturers in an attempt to correct these problems, but despite great effort on their part, these problems persisted.

As an expedient during a portion of the engineering phase, we lapped all substrates to a standard thickness prior to polishing. A slurry of alumina power, with a particle size which is nominally five micrometers was used as the lapping compound. We found that better surfaces were sporadically obtained using polished lapped slices but on average, the yield of high quality wafers was not sufficiently improved to warrant the additional cost of routine prelapping.

Indeed, unless lapping was carried out with great care, deviations from specifications in wafer taper and bow were often greater than with wafers as received from the vendor.

To minimize wafer processing, the overall wafer thickness should be within 0.0001 inch of the nominal dimension, including all errors such as bow, taper, parallelism, and others. To achieve this, polished substrates prior to deposition should possess similar tolerances. A special all-electronic gauge (Model 3046 Ade Corporation) was obtained for this purpose (Figure 3-12). Using two capacitive non-contacting probes, it displays thickness, bow, and taper on a digital readout. It is especially suitable for measurements immediately prior to epitaxial growth because it does not damage or contaminate the substrate.

Figure 3-12 Photograph of Special All-Electronic Gauge (Model 3046 - Ade Corporation).

The final process which was developed accomplished the objectives without the necessity for duplicating processes in the epitaxial area which were already under development in another area for wafer dimensional control. The wafer is now metallized after epitaxial growth as intended without intermediate dirty operations. A thin layer of gold is then plated over the Schottky metallization to protect this thinner sputtered layer. The parallel lapping step is performed next. The success of this sequence depends upon the fact that the metallized layers are very thin and well controlled relative to the required tolerances and introduce no significant error to the measured dimensions during lapping.

All material processed during the confirmatory and pilot stages of the program were processed in accordance with this sequence.

3.3.4 Spray Dicing

After wafer processing is completed and the diodes are evaluated, the wafer must be separated into individual modes so that they can be mounted into the final packages. For the plated heat sink process, the diodes are held together by the common gold heat sink which serves as a carrier during wafer processing operations. The generation of individual diode chips means, therefore, that the gold carrier must be separated into several hundred pieces, each containing a diode.

Several techniques have been used for doing this in the past. The first was razor cleaving. This was later replaced by wire cutting. In this operation, a diamond impregnated wire is dragged across the surface between diode rows until it wears through the gold. It is then indexed to the next rows until all of the rows in one direction have been cut. This operation is repeated after indexing the wafer 90 degrees. Although this technique is mechanized, there are several problems:

1) Wafers must be handled singularly, and 3-4 hours are required to process each wafer.

2) The exiting wire drags gold leaving a burr on the bottom edge of the chips. This results in poor chip mounting quality and high thermal resistance. A similar burr is raised on the top surface of the chip which interferes with die collet pickup.

3) Operational problems such as wire breakage, nonuniform indexing, slurry impregnation and several others.

Although the above technique was used extensively, current production dice have been generated by razor cleaving instead. This technique is crude but simple, and a skilled operator generates dice of higher quality than those typically produced by the wire saw. The time element is about the same as the wire saw.

A major improvement in dicing capability has been realized by implementing on the production line the spray dicing technique which was developed with independent funds by Raytheon Research Division. The necessary production engineering effort was accomplished on this program. Because of the success achieved, the technique has been extended to include spray dicing of all IMPATT diodes. The method involves photolithographic masking techniques. The wafers are placed in a special spray dicing fixture, and a high velocity spray of gold etching solution is directed at the plated heat sink side of the wafer. (See Figure 3-13.) The action of this spray is such that anisotropic etching occurs and grid lines are cut into the gold in those areas where no photoresist is located. A front-to-backside registration of the mask is required during masking.

The technique involves spray etching completely through the heat sink a grid pattern with .002" wide lines. The etching is

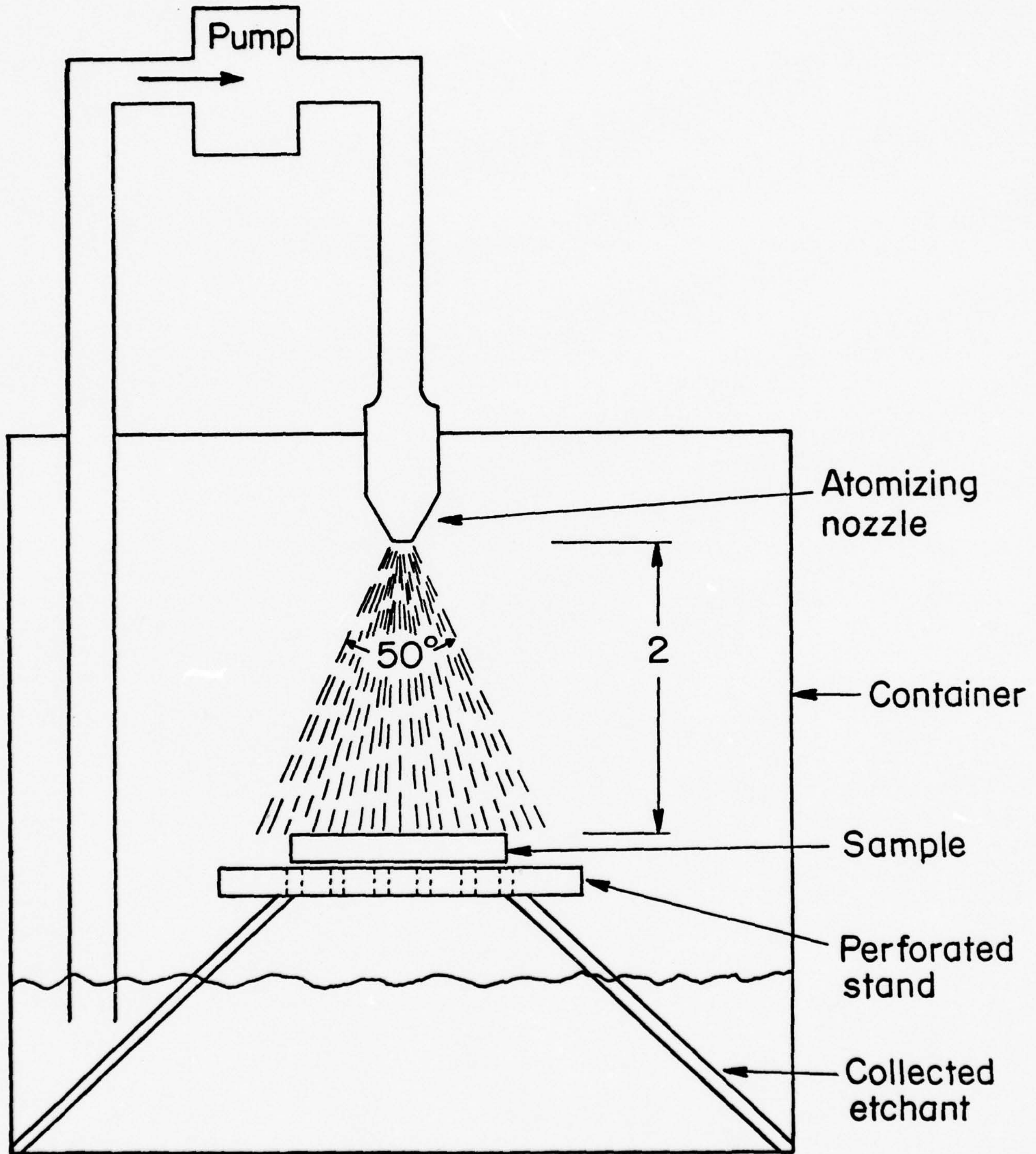


Figure 3-13 Illustration of Spray Dicing Device

done from the back side while the mesa side of the sample is mounted protectively in wax. Prior to etching, front-to-back alignment is accomplished on the mounted sample using KMER photoresist as follows:

1) The sample is mounted on glass, mesas down, in a clear, "picolastic" wax. The glass is larger than the sample.

2) The opposite side of the glass is then masked with grid pattern aligned to the mesas as they show through the glass. The pattern in photoresist extends beyond the sample and is visible from both sides of the glass.

3) The sample side of the glass, including the sample, is then masked with the same grid. By aligning the second masking to the grid lines showing through the glass, front-to-back alignment is achieved. At this point in the process, the sample has the appearance shown in Figure 3-14.

The spray etcher is a device designed and built by Raytheon using inexpensive laboratory equipment and materials. The device is shown in Figure 3-13. In operation, liquid etchant, recirculated in a closed system, is sprayed through an atomizing nozzle so that droplets impinge with nearly normal incidence upon the masked sample. The velocity of the droplets causes the etchant to dissolve the exposed material far more rapidly in the direction normal to the surface than in the lateral direction, thus providing the effective anisotropy of better than 10 to 1. Detailed process steps are included in Section II of this report.

The elapsed time for spray dicing a wafer is about the same as for blade cutting or wire sawing. The labor involved for a single wafer is also about equal. One advantage of the method is that all of the operations are batch-type operations where the incremental cost of handling increasingly larger batch sizes drops

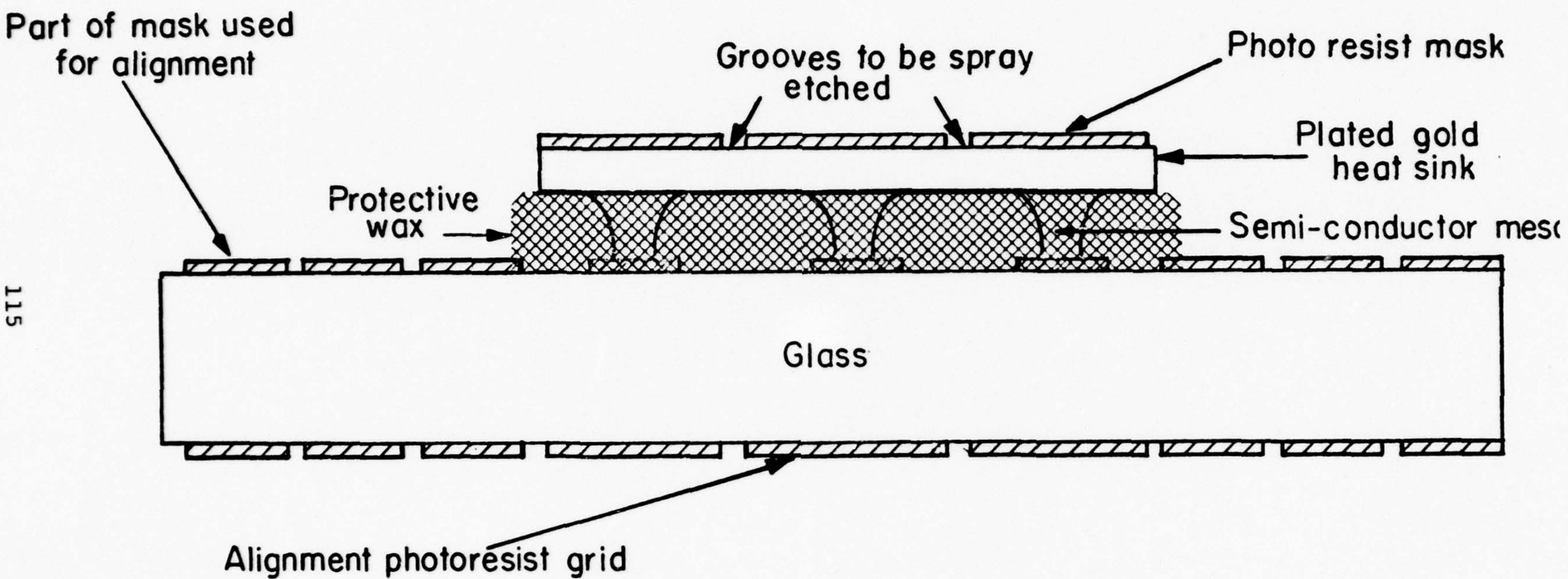


Figure 3-14 Mounted Sample for Spray Dicing

rapidly. Each of the individual process steps can be readily automated. The major advantage of the method at the present volume of production for Read diodes lies in the quality of the chip produced. Dimensional uniformity is better than previous methods which will result in more tightly distributed diode characteristics for production line devices and better yield.

Figure 3-15 shows the completed die which results from the spray dicing operation. The die has a cross sectional shape which resembles a truncated pyramid, its base being somewhat smaller than the top surface as a result of mask undercutting as etching proceeds from the back side.

The final chip size is determined by the mask size, and the amount of undercutting allowed which is in turn a function of several process variables, among them the gold thickness and its tolerance across the wafer. The tolerance on the gold thickness is the dominant factor in determining the tolerance which can be maintained on the chip size. As etching proceeds, thin areas of the wafer will etch thru first. Further etching reduces the dimension of these as the thicker portions of the wafer are etched through. The tolerance is, therefore, dependent upon the flatness and parallelism control which has been achieved throughout wafer processing.

The overall dimensional tolerance which can be presently achieved by spray dicing is less than 0.001 inch compared to several mils for the previous method.

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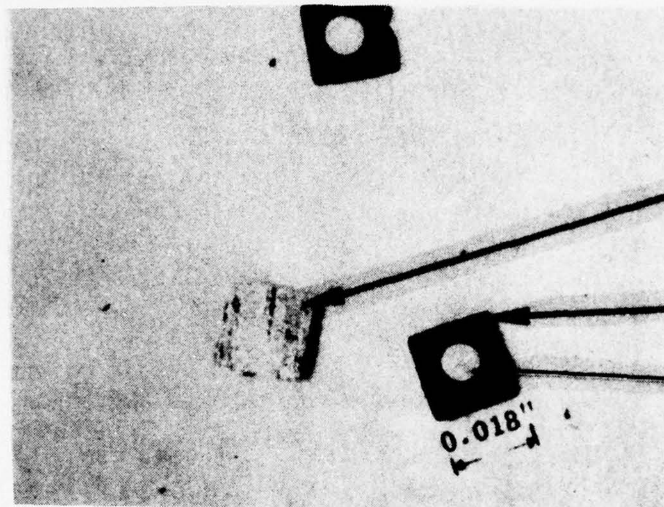

Figure 3-15 GaAs IMPATT Diode Chip After Spray Dicing

3.4 Assembly and Test Process Engineering

3.4.1 Hot Gas Chip Bonding

One of the problems in mounting dice using solder is that the dice tend to float on the solder after the tip pressure is removed. A second problem is that flux is usually required to achieve a good flow of the solder. Both of these problems can be eliminated by using the hot gas method of bonding.

In operation, the solder preform and die are placed in the package which is held on a heated stage at a temperature just below the melting point of the solder. The die is held in place using a die collet as in conventional bonding. A jet of heated gas is then directed to the bond area through a nozzle to supply the incremental heat necessary to melt the solder. The heated gas is forming gas which replaces the air to prevent oxidation and also serves as a flux by reducing oxides. When the gas jet is interrupted, the local temperature decreases to its initial value and the solder freezes. The tip pressure is maintained during the freezing which prevents the chip from floating.

The bonding equipment which was purchased and installed is manufactured by Mech-El Industries. In order to evaluate the Mech-El hot gas bonder, four lots (Lots B, C, D, and E) of about ten diodes each were assembled. Lots B and C were assembled using the K&S bonder with 50 and 70 gr, respectively, die collet pressure. These represent the control samples. Lots D and E were assembled using the Mech-El hot gas bonder. The same collet pressures were used, 50 and 70 gr, respectively.

The quality of die bonding of IMPATT diodes is quantitatively measured by the thermal impedance R_{TH} of the device.

Since thermal impedance is area-dependent, the capacitance of all diodes was measured. This was used as an indication of device area variations, assuming the same capacitance per

unit area for all devices. This is a reasonable assumption considering that all of the devices came from the same Ku-band wafer, 81844M2.

The mean (μ) and standard deviation (σ) of thermal impedance and capacitance were calculated for every lot. The results are compiled in Table 3-7. An analysis of the results indicates that there is no significant difference between the two bonders. However, there is a tendency towards lower R_{TH} values at the lower collet pressure for both bonders. Even though the percentage change is quite small, the direction of change is surprising. Higher collet pressure should force out more solder from under the chip, hence better R_{TH} values. One possible explanation would be that layers which are five to ten percent thinner, and five to ten percent higher in doping. We conclude that Read wafers can be produced economically in our triple wafer reactor.

3.4.2 Ribbon Bonding

Evaluation results on Ku-band wafers had led to the general conclusion that the diodes were operating in the lower part of the specified frequency band of 14-16 GHz and that the diode efficiency was straddling the specification limit of 20%. Tests were conducted to determine if the efficiency could be improved by minor modifications in assembly procedure in order to enhance the yield. The following summarizes the results of experiments performed with various size mesh and ribbon contacts and also compares results with type 16 and type 18 packages. The type 16 package is the standard package used for this program (see Figure 1-3). The type 18 is a reduced size ceramic mounted on the same threaded stud as the type 16. Five (5) variables were tested.

(1) Type 16 Package - 750 LPI mesh
(2) Type 16 Package - 2000 LPI mesh
(3) Type 16 Package - 5 mil ribbon
(4) Type 16 Package - 10 mil ribbon
(5) Type 18 Package - 750 LPI mesh

Table 3-7

Thermal Resistance of Diodes from Hot Gas Bonder

Parameter		K&S		H.G. Mech-El	
		Lot B	Lot C	Lot D	Lot E
C (pF)	μ	2.01	1.98	1.95	2.00
	σ	0.13	0.10	0.18	0.18
R_{TH} (^{o}C/W)	μ	17.4	18.2	17.8	18.6
	σ	0.57	0.85	0.69	0.8

Figure 3-16 is a plot of efficiency versus output frequency. The efficiency was measured at an output power of 2.5 Watts. At the band center, more power was available (up to 3.0 Watts). It may be seen that the efficiency is optimized at about 14 GHz independent of construction style. The diode impedance varied as the construction was varied, necessitating different matching impedances, but the optimum operating point was constant.

Figure 3-17 contains plots of diode efficiency versus output power for various construction styles. The two conclusions resulting from this plot are:

(1) The diodes have their optimum efficiency at the specification test point of P_o = 2.5 Watts. This verifies previous data showing that the efficiency is optimum at a power output of 2.5 Watts for diodes having a capacitance of about 1.6 pf (measured at breakdown voltage). It should be noted that for this particular lot, 1.7 is a better value and the optimum value will vary somewhat as the wafer parameters change to keep the current density constant.

(2) The diode efficiency is improved as the screen material becomes less transparent. The solid ribbon gives the lowest loss. Presumably this reflects the lossy nature of the electroformed screen material. The cross sectional area increases as the number of strands increases. The type 18 package has better efficiency than the type 16 and about the same as the 2000 LPI in the type 16. This is probably because the screen length is shorter in the type 18. The data of Figure 3-17 is for a typical diode from each lot. Considering the total data and possible adjusting factors because the data was not all taken at the optimum point, it can be concluded that an efficiency improvement of 0.5 to 1.0% can be achieved by converting

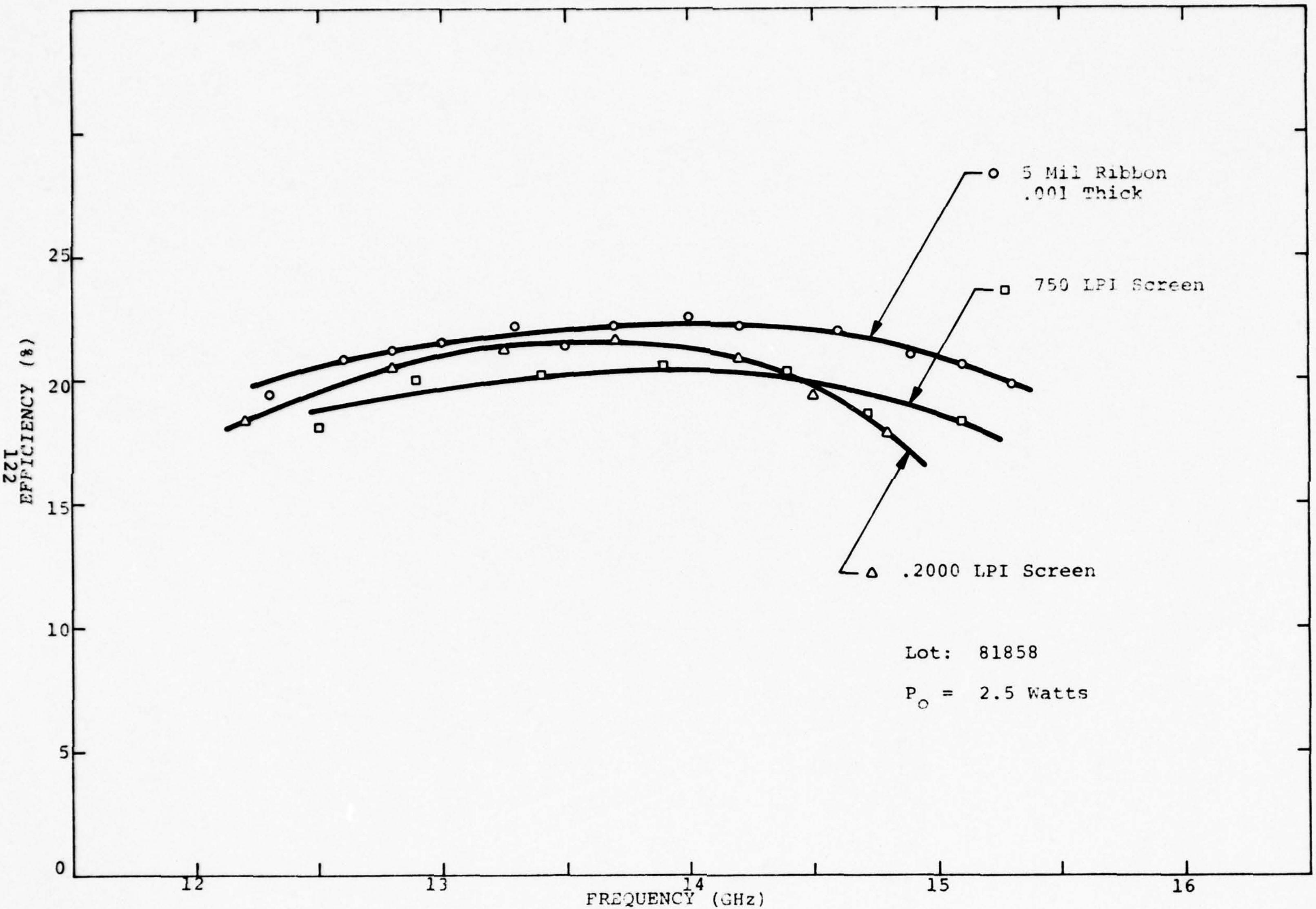

Figure 3-16 Efficiency Versus Operating Frequency

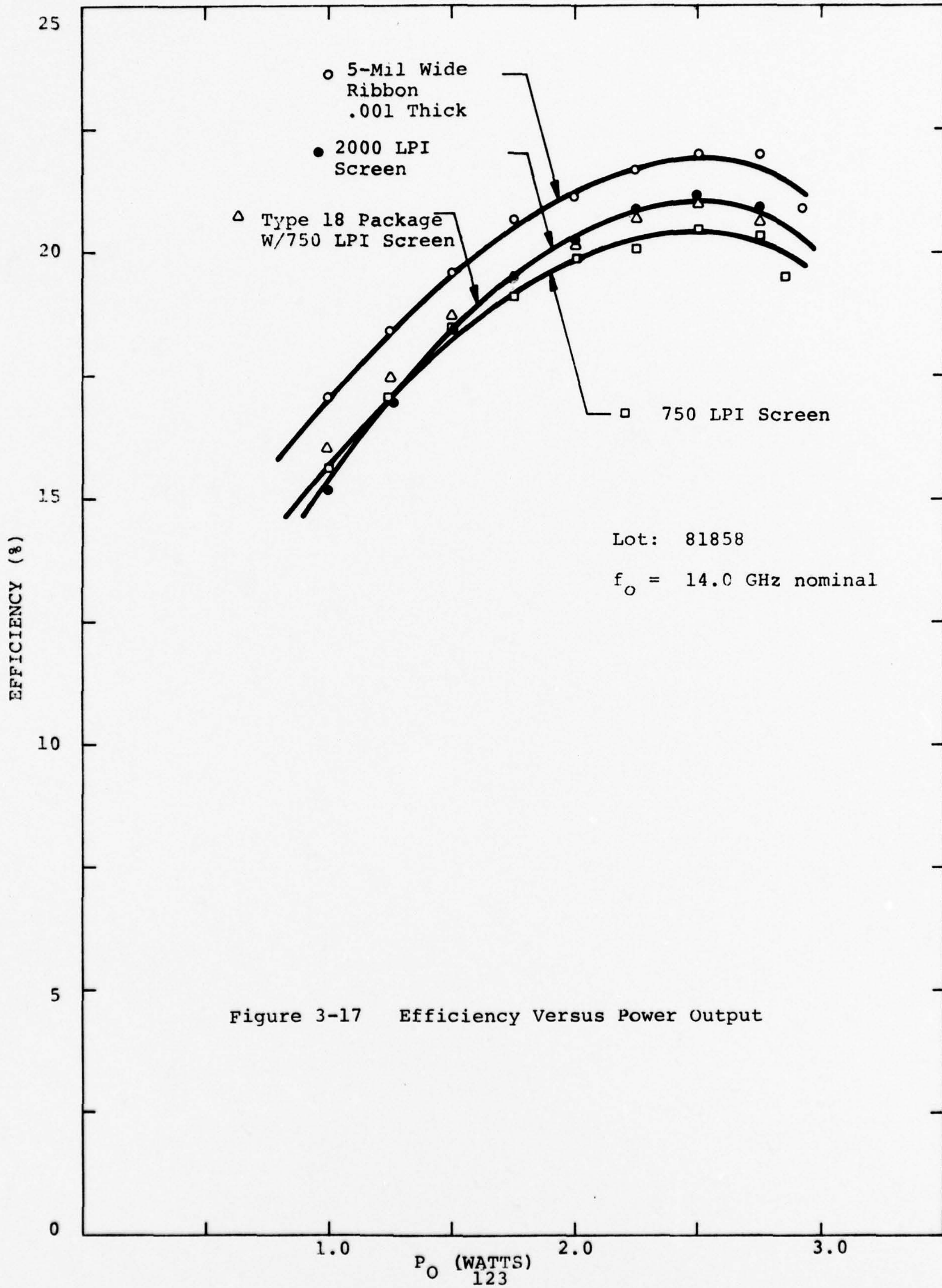

Figure 3-17 Efficiency Versus Power Output

to denser material for the diode contact. Ribbon of 5 mil width appears to be a good choice. Wider ribbon (10 mil) shows no further improvement.

In view of these conclusions, a change to 5 mil ribbon was implemented for X-band and Ku-band diodes.

3.4.3 Thermal Resistance Testing

The measurement of thermal resistance as performed prior to this program was one of the factors gating the production rate of Read IMPATT diodes. The accurate measurement of thermal resistance is a fairly lengthy two-step process involving first the calibration of the diode breakdown voltage with temperature, and secondly, the use of this calibrated diode thermometer during a pulsed power test to measure the device temperature. Knowing the amount of power dissipated in the device and its temperature, the thermal resistance of the device is calculated. We had been performing this measurement sequence in a multi-station test fixture capable of measuring twelve devices simultaneously. The cycle time was approximately four hours per batch. A doubling of this rate was the minimum required to meet the rate objective of 1000 units/month.

To accomplish this, temperature calibration and pulsing portion of the measurement were separated. A large portion of the total time had been consumed in waiting for the fixture and diodes to heat and to reach equilibrium during the temperature calibration portion during which time the pulsing equipment had also been inaccessible.

A twenty-five position fixture was, therefore, designed and fitted to an oven so that temperature calibration curves could be obtained on twenty-five units simultaneously, separate from the pulsing apparatus. This capacity is adequate for the present requirement and can be readily expanded -- commercial equipment with high throughput can be purchased. Using this system, the diodes are

individually tested in turn through a selector switch at room temperature and at a temperature of 125°C.

During the heating and stabilization period, a separate batch of diodes, previously temperature calibrated, can be pulsed. To increase the rate for this portion of the measurement, a test instrument was purchased from Sage Enterprises. This instrument measures devices and provides a digital readout of the result in nine seconds. The throughput is limited by the desired accuracy, which sometimes requires that the measurement cycle be repeated (i.e., when the diodes are not sufficiently uniform in characteristics), and by loading, unloading and data recording.

Considering all aspects of the thermal resistance measurement, devices are now measured at the rate of 75-100 units per eight-hour shift by a single operator. For simpler devices such as flat-profile IMPATTs, the temperature calibration of breakdown voltage is performed on a sample basis and much higher rates are realized.

The accuracy and repeatability of the measurement has been analyzed. A discussion of these aspects of the measurement follows. All of the discussion is referenced to the Sage instrument shown in Figure 3-18. In the use of this instrument, the temperature coefficient of avalanche breakdown voltage is normalized to the room temperature breakdown voltage and is referred to as the Beta Factor (β).

$$\beta = \frac{V_{B2}-V_{B1}}{(T2-T1)\ (V_{B1})}$$

where: V_{B2} = Breakdown Voltage At T2 (ex. 125°C)

V_{B1} = Breakdown Voltage At T1 (ex. 25°C)

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Figure 3-18 Photograph of Sage Instrument

3.4.3.1 Temperature Coefficient of Avalanche Breakdown

Most methods for measuring the thermal impedance of IMPATT diodes use the device as its own thermometer for measuring its junction temperature. This is accomplished by heating the device in an oven and measuring the avalanche breakdown voltage (V_B) at a small sense current. The slope of the "breakdown voltage versus temperature" curve, normalized with respect to room temperature voltage, is the β coefficient. Potential sources of error in measuring and applying β have been analyzed.

A potential source of error in measuring the breakdown voltage is the voltage drop across contact resistances. To establish whether this was significant, the measurement was simulated using an empty diode package internally short circuited. The results indicate a residual resistance of 0.5 ohms in the system which corresponds to a voltage drop of 1 mV or less in a current range of 1-2 mA. This is insignificant when compared to the resolution in measuring the breakdown voltage, which for the present equipment can be measured within an accuracy of ±50 mV including the error due to a 5% uncertainty in the sense current.

Temperature is directly monitored in $^{\circ}C$ by a digital temperature indicator with a $0.1^{\circ}C$ resolution and $\pm 0.5^{\circ}C$ accuracy. Calibration was checked at the ice point and water boiling point. An offset of $0.1^{\circ}C$ was found. This offset does not really affect β measurements since it is eliminated in the subtraction, and β is a function of ΔT instead of just T. Hence, there is a $\pm 0.6^{\circ}C$ uncertainty in the indicated temperature. The diodes are mounted in an aluminum block having a thermocouple attached. The temperature uniformity of the block was checked and found to be better than the accuracy of the measurement.

The contribution to heating by the power dissipated in the diode at low currents was considered. For diodes of interest having the following typical characteristics:

V_B (25°C) = 40 Volts

V_B (125°C) = 47 Volts

R_{th} = 23°C/W

the junction temperature increase at bias currents of 1 mA and 2 mA is:

	I_S = 1 mA		I_S = 2 mA	
	25°C	125°C	25°C	125°C
Contribution to Heating (°C)	0.92	1.08	1.84	2.16

If the only effect of I_S is as shown above, the error in β will be insignificant due, once again, to the ΔT rather than T dependence of β.

A curve of V_B versus T for a typical diode is shown in Figure 3-19. The curve is nonlinear over the entire temperature range. A linear approximation does not introduce a very large error, but this error can be entirely eliminated even in a production environment by proper application of technique. During measurement of β, the same temperature end points should be consistently used. We have selected 25°C and 125°C as these points. This corresponds to a ΔT of 100°C. During the pulse measurement on the Sage, the diode is always heated with sufficient power to achieve the same T = 100°C. With this approach, the shape of the V_B versus T curve between the two points does not affect the accuracy of the measurement.

The repeatability of the V_B versus T curves was evaluated by testing points on the curve on several different days. This data is given in Figure 3-20 as identified in the legend and shows that the repeatability is quite good.

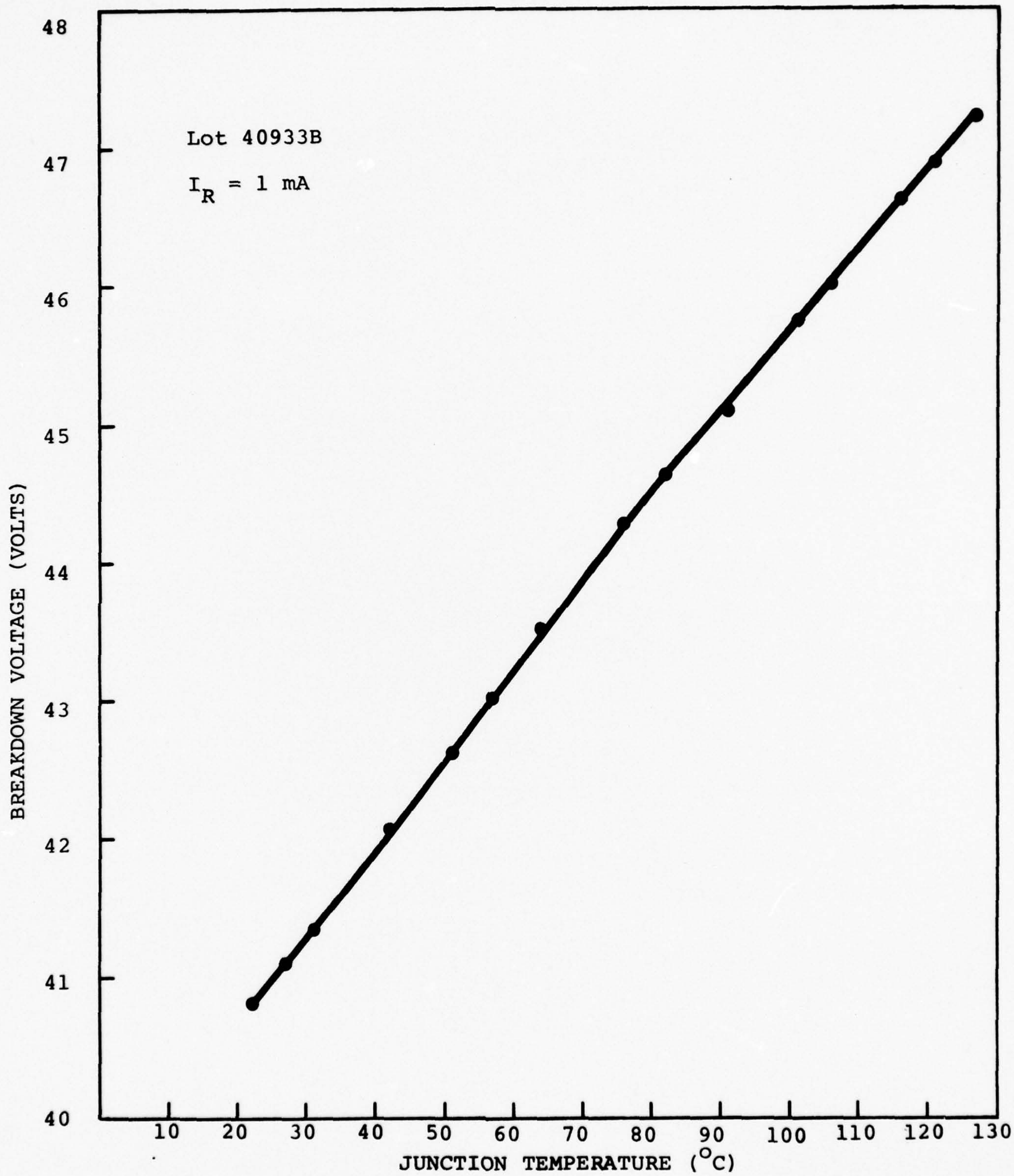

Figure 3-19 Curve of V_B versus T for Typical Diode

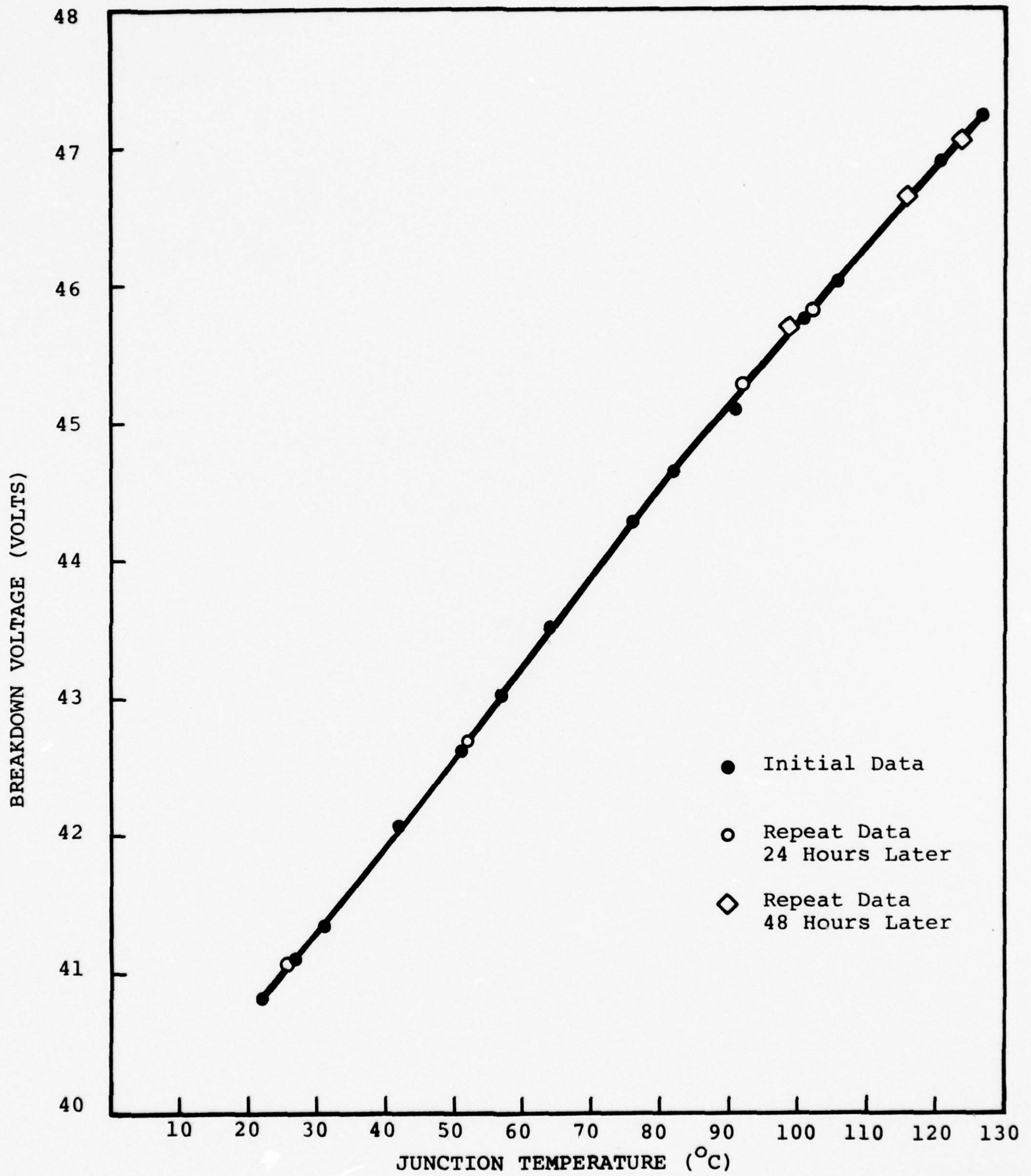

Figure 3-20 Repeatability of V_B versus T Curve

Other observations resulting from the investigation indicate that the nominal value of β is lot dependent, and the standard deviation within a lot varies from 1.4% to 3.4% for the lots tested. The value and distribution of β are also current dependent. The mean β per lot is lower and the distribution tighter at I_S = 2 mA than at 1 mA. These observations do not affect the accuracy of the measurement as described, but rather determine the accuracy obtainable from performing a sample test of β if this technique were adopted.

A detailed error analysis was performed in order to understand and place in perspective the degree to which the error of each measurement cumulatively affects β.

$$\beta = \frac{\Delta V_B}{\Delta T}\frac{1}{V_{B_i}} \equiv S\frac{1}{V_{B_i}}$$

1) $$\frac{\Delta S}{S} = \pm\left(\frac{\Delta T}{(\Delta T \mp 2t)}\ \frac{(\Delta V \pm 2v)}{\Delta V} - 1\right)$$

where: v = the error in V_B.

t = the error in T.

If for example,

ΔV_B = 6V

ΔT = $100^\circ C$

v = ±0.050V

t = $\pm 0.6^\circ C$

$\frac{\Delta S}{S}$ = ±2.9%

Hence, the uncertainty in the calculated slope is $\pm 1.7 \times 10^{-3} V/^\circ C$.

2) $$\frac{\Delta\beta}{\beta} = \pm\left(\frac{S \pm s}{S} \; \frac{V_{B_i}}{V_{B_i} \mp v} \; -1\right)$$

where: s = the error in S.

For example,

$S = 0.058 V/^{o}C$
$s = 0.0017 V/^{o}C$
$V_B = 40.0\ V$
$v = 0.05 V$
$\frac{\Delta\beta}{\beta} = \pm 3.1\%$

The example above indicates a 3.1% uncertainty in β due to various measurement errors only. Since β is a normalized coefficient with respect to V_{B_i}, which is a function of T_i, a new source of error exists, unless T_i at β measurement is the same as the R_{th} measurement. In other words, the diode heat sink temperatures should be the same when determining V_{B_i} and R_{th}. A simple calculation indicates the relative significance of a worst case $\Delta T_i = \pm 5^{o}C$.

$S = 0.058\ V/^{o}C$
$s = \pm 0.0034\ V/^{o}C$
$V_B = 40.0\ V$
$v = \pm 0.05 \pm .29 = 0.34\ V$

Meas. Error   Ti Error

$\frac{\Delta\beta}{\beta} = \pm 3.8\%$

In summary, @ T = 100°C, a 0.6% error in T and 0.13% error in V_{B_i} cause a 3.1% error in β. An uncertainty of 0.29 Volts

in V_{B_i} due to a worst case 5^oC difference in heat sink temperatures (R_{th} versus β heat sinks) adds another .7% to the error in β. The preceding actual laboratory measurements indicate an uncertainty in β of about 3%.

3.4.3.2 Thermal Resistance Tester

Early in the program, the unit shown in Figure 3-18 was purchased from Sage Enterprises to replace the test set in use at the time (Figure 3-21). The motivation improved speed, accuracy, and simplicity of operation.

Upon delivery, it was found that the instrument, indeed, promised greatly improved production rates because of the rapidity of measurement and computation relative to the existing equipment. Correlation with the existing method was poor, however, which led to a rather comprehensive evaluation exercise. The following conclusions resulted from the evaluation:

1) Repeatability of measurement was excellent over a short time period (days).

2) There was an occasional shift in the measurements which were again very repeatable at the new level over a short time period (days).

3) Thermal resistance varied greatly as the input power was changed leading to uncertainty in the true value which made the correlation problem appear worse.

The instrument was returned to the vendor with all of the test data. The shift in measurement level was explained as being due to a defective integrated circuit component and was quickly corrected. Further details on correction action were not sought. The variation in thermal resistance required design

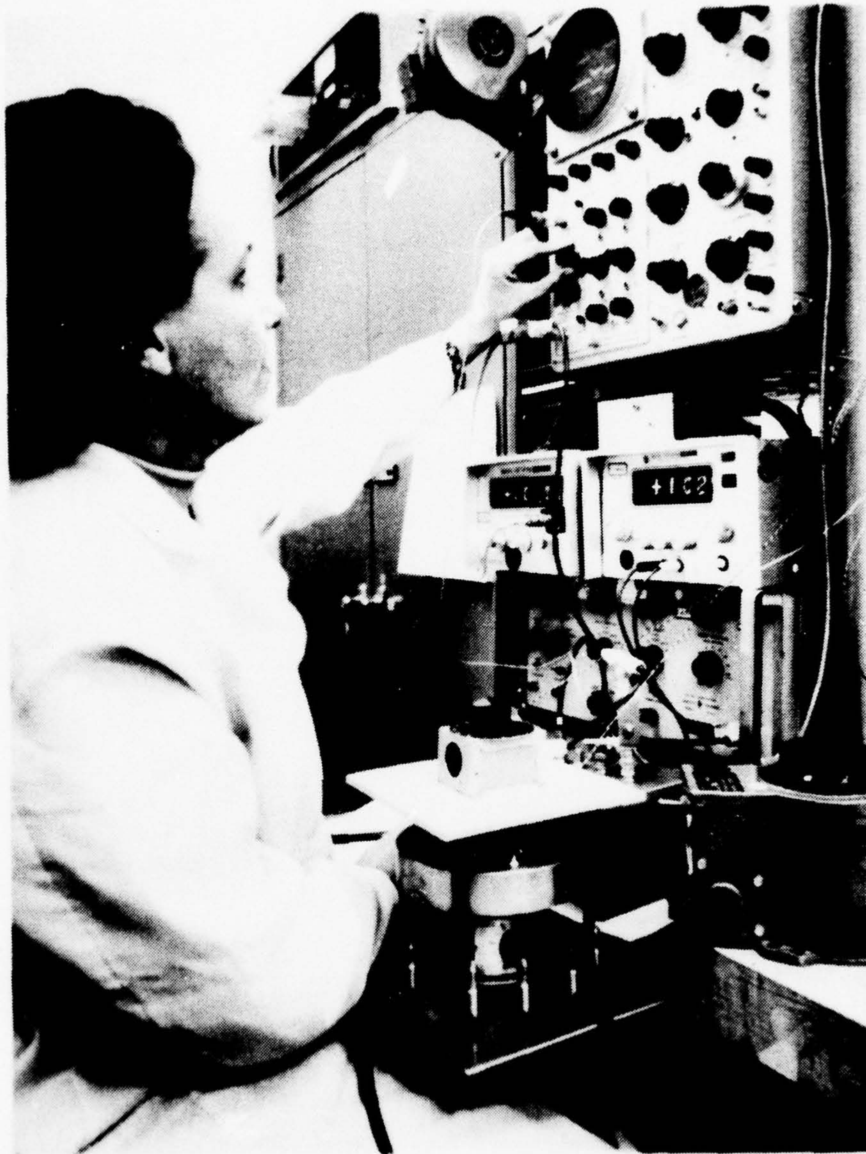

Figure 3-21 Thermal Resistance Test Set

modifications, necessitated in part by the properties of the devices being tested. Sharp pulses used to switch the diode rapidly apparently caused the diode to oscillate which led to inaccuracies in measured currents and voltages used in the computation. This problem was solved by adding lossy material to the diode terminals to damp the oscillations. During the evaluation, it had also been concluded that knowledge of the junction temperature during test would be a desirable feature. This feature was added as the accessory digital meter shown in the figure.

The "Theta 120" was subjected to a second evaluation by the vendor and also by Raytheon. Based upon these tests, the instrument was accepted and is being phased into the production line.

Standard diodes have been designated and are measured each time the instrument is used. Repeatability of measurement is excellent and is about 0.5% over a two-month period. Correlation with the prior method continued to be somewhat erratic for a while. Initially, the approach had been to apply a factor to the Sage via an artificial value for β to force agreement between the two methods. Using this technique, highly reproducible thermal resistance data was obtained for all devices, and this data agreed with the method which had been in use up to this time.

Meanwhile, the potential source of errors in the two techniques was examined, and data was obtained from other sources. It was concluded as a result of the program that the Sage instrument gave more accurate results than the prior method. The differences are explained by how fast the junction temperature is sensed following interruption of the heating pulse. The short thermal time constant of these devices imposes the requirement. Correction of the standard method for cooling which occurred during switching gave results in close agreement with the Sage unit.

3.4.4 Noise Measurement of IMPATT Diodes

The original AM and FM noise measurements, on the engineering sample Read diodes, were performed on an elaborate general purpose setup at Raytheon's Research Division. This particular measurement system was conceived mainly for research and development needs, hence became quite unsuitable for production testing. Disregarding setup time, one could measure at the rate of two to four diodes a day. The main cause for the low throughput is the need for constant recalibration of AM and FM sensitivity. This problem is compounded when measuring FM noise by small drifts in the carrier frequency. After obtaining the point-by-point data, it must be submitted to calculations to obtain the results and then manually plotted.

During the course of this program, a computer program was developed to accept the raw data, perform the calculations, and plot the results. Samples of the resultant curves were included in prior reports. This was mainly for convenience of the operator and gave more presentable data, but resulted in only 10% rate improvements.

Several alternatives for faster measurement systems were considered. A circuit design was completed for a "go-no-go" system which appeared quite attractive. An excellent alternative was found, however, in a powerful carrier noise analyzer, Model CNA-20, manufactured by the Electronics Equipment Group of Raytheon's Microwave and Power Tube Division. The unit was originally designed for measuring low noise tubes. This unit uses a microwave discriminator and direct detection techniques, thus eliminating the complex operations and adjustments associated with heterodyne systems. Self-calibration is accomplished directly at the microwave frequency. Achievable rates exceed ten times that of the former method.

Such a carrier noise analyzer for Ku-band has been acquired and evaluated. The unit is shown in Figure 3-22. The unit,

Figure 3-22 Photograph of Carrier Noise Analyzer (Model CNA-20)

in conjunction with a low frequency spectrum analyzer and an X-Y recorder, yields a hard-copy plot of noise as a function of frequency from carrier. A typical plot is given in Figure 3-23.

The measurement of semiconductor device noise is quite often limited by the power supply used in biasing the device under test. An evaluation of such limitations in the case of Ku-band Read diodes was conducted. The power supply "pushing" figure is defined as the ratio of the deviation frequency to the "pushing" signal voltage (FM). Then the power supply noise level was plotted. At 10 KHz, the plot indicates a noise level of about -107 dBV which corresponds to an equivalent frequency ($\Delta f \approx 200$ Hz/100 Hz-BW). All measured devices indicate an FM noise level of about the same magnitude; hence, it is believed that the actual FM noise level of the diodes is below this level. In the case of AM noise, both the power supply level and diode noise level are below the limiting sensitivity of the noise analyzer.

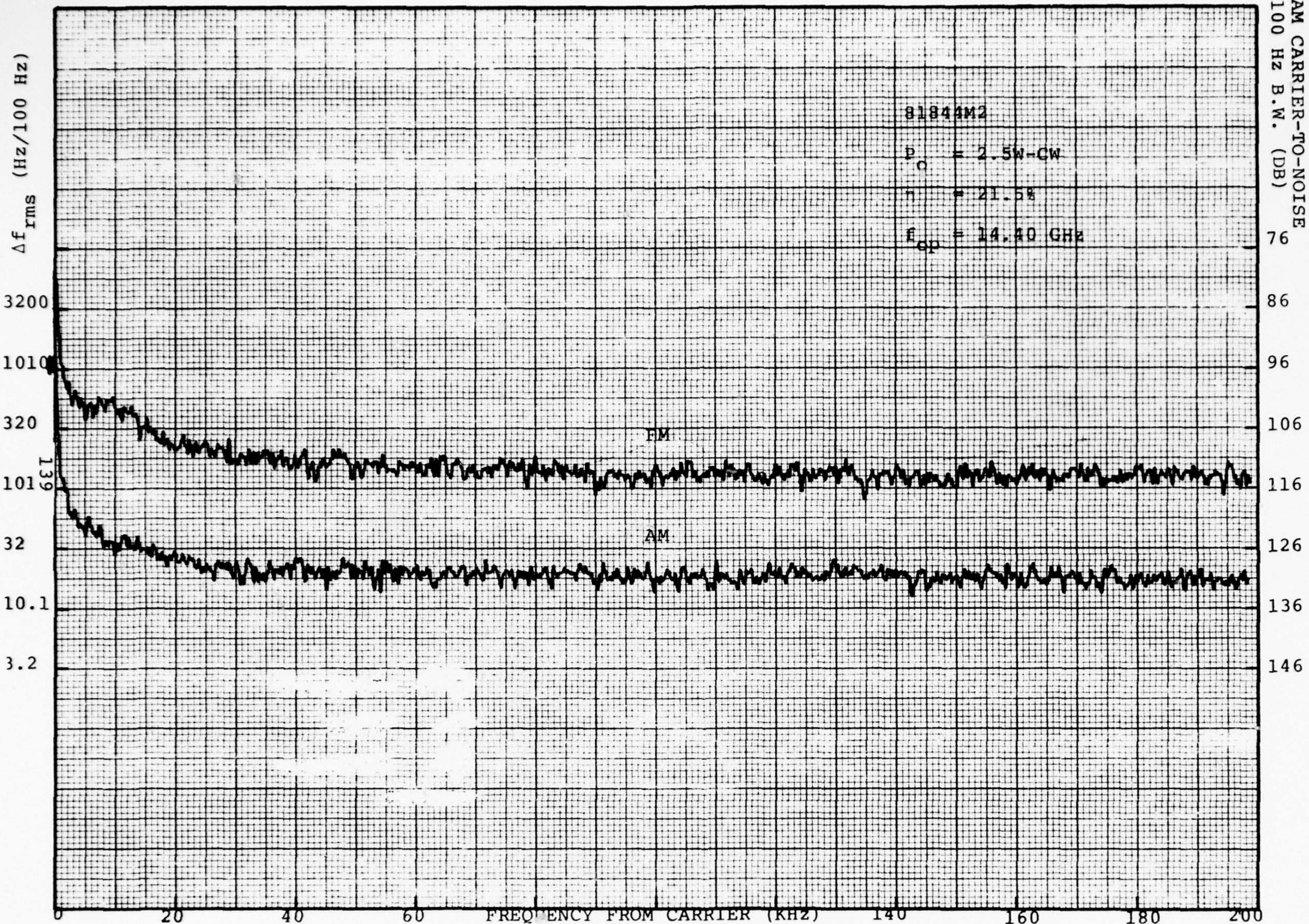

Figure 3-23 Plot of Noise as a Function of Frequency from Carrier

4.0 OPERATING LIFE TEST PROGRAM

4.1 Requirements

Operating life test requirements of this program specified that diodes periodically be subjected to 1000-hour life tests while operating as oscillators. The tests were initiated at the end of the first quarter and repeated quarterly for a total of seven (7) tests. The sample size for each test was five (5) diodes of each type randomly selected from a corresponding wafer. Nine (9) diodes of each type were life tested for 1000 hours as a part of the Group B quality Conformance Inspection at the time of confirmatory sample testing and again at the time of pilot run sample testing.

The testing was conducted at an ambient temperature of 25°C with the test cavity temperature also held at 25°C and the diode junction temperature held below 200°C. To identify failures, the power output was monitored with failures defined by a 25% decrease in the power output of a diode relative to its initial value. The Group B life testing was performed with the diode operating within its rated power output, frequency, efficiency, and junction temperature specifications. The quarterly tests were conducted in such a way as to demonstrate progress toward successfully meeting these test requirements.

Two operating life test stations, one for X-band diodes and one for Ku-band diodes, were designed and constructed to meet the operating life test requirements described. A description of the equipment and diode life testing procedure follows.

4.2 Operating Life Test System

Two (2) test stations each containing nine identical positions were designed and constructed. Raytheon-designed oscillator test cavities (described in Section 4.2.1) and current regulators were integrated with various commercially available components to create two panel-instrumented stations. Some of

the salient design features of the system include: typical current regulation of <0.5%, transient protection out to 10 MHz, regulator "fail-safe" protection against diode failure, constant heat sink temperature via a closed loop water circulating system, thermal overtemperature protection and complete protection against line voltage failure. Each station continuously monitors RF output on a sampling basis by recording the detected RF on strip chart recorders which were available for use on this program. Diode bias voltage and current monitoring is available at the station thru a nine-position selector switch. The life test station by itself is relatively compact and is bench mounted. The two stations are installed on a single bench top which also contains a common driver/programmer. A water circulating system that is also common to both stations is located under the bench. The long term operational behavior of Read diodes as microwave oscillators will be tested under controlled conditions using these stations.

Figure 4-1 is a block diagram of the basic life test station. Table 4-1 lists the equipment utilized. The diodes under test are installed in oscillator test cavities which were designed during the first quarterly period of this program. The cavities are described in detail in Section 4.2.1. Bias is supplied by Raytheon-designed adjustable current regulators. Each test cavity is terminated into an appropriate waveguide variable attenuator followed by a standard SMA coax to waveguide transition. The transition is connected by coaxial cable to one of the nine inputs of a Raytheon-designed SP9T diode switch. The output of the switch is detected and displayed on a strip chart recorder. Eight additional test cavities with their accompanying accessories provide a total of nine individual diode test positions. The basic setup is identical for each of the two stations required except for the dimensions of the test cavities and the waveguide components. A single driver and automatic programmer control the two SP9T switches simultaneously so that each test channel is sequentially sampled and its detected output displayed on the strip chart recorder. The

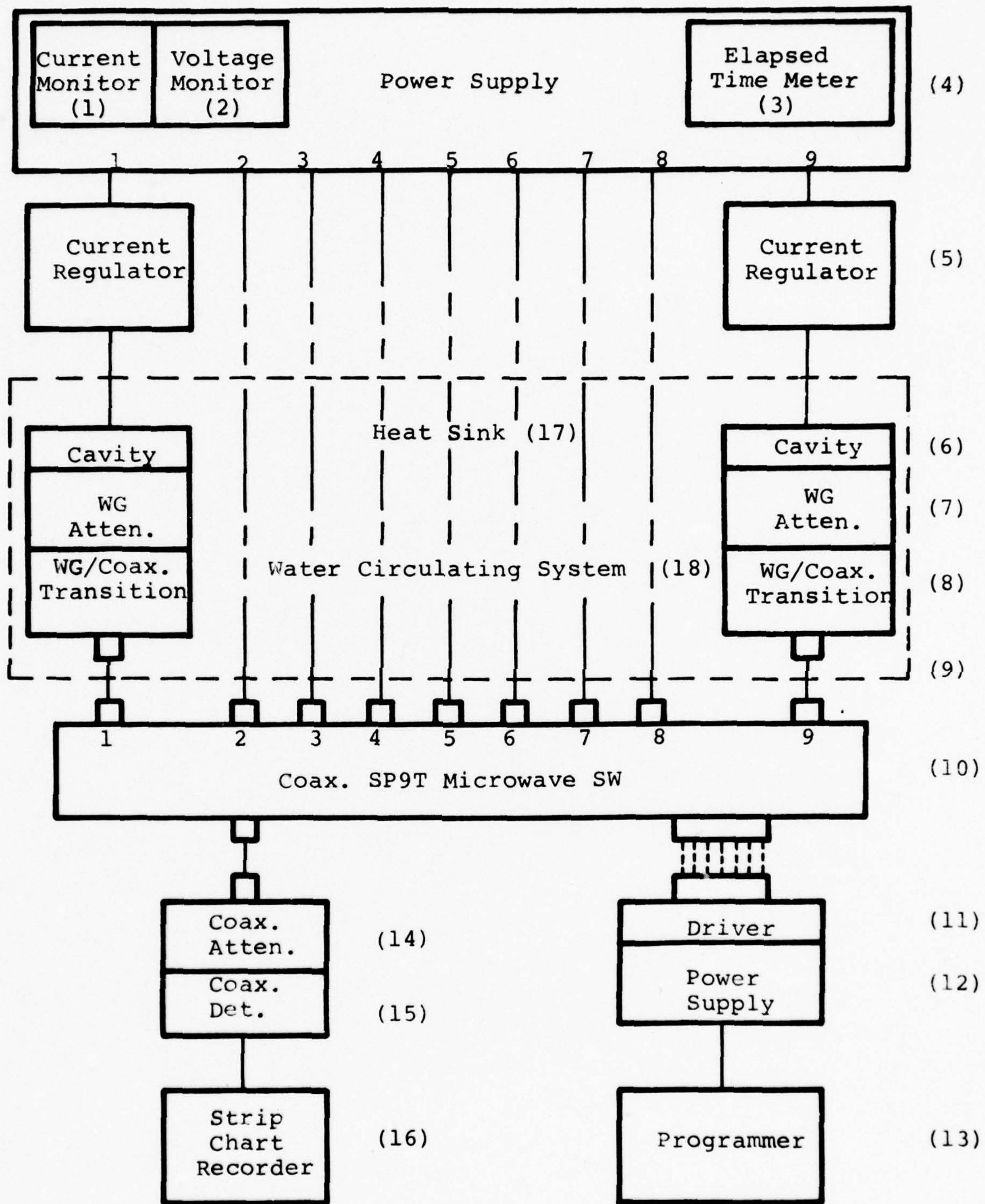

Figure 4-1 Block Diagram of Operating Life Test Station

Table 4-1

OPERATING LIFE TEST STATIONS - EQUIPMENT LIST

ITEM	DESCRIPTION	QUANTITY/ STATION
1	Current Monitor - (DVM) Fairchild 7050	1
2	Voltage Monitor - (0-100 VDC) - Simpson #2123	1
3	Elapsed Time Indicator - General Time #EF1335	1
4	Power Supply - Sorensen #DCR8-30	1
5	Current Regulator - Raytheon Design (details in this report)	9
6	Test Cavity (containing diode under test) - Raytheon THX-8000A, or	9
	Test Cavity (containing diode under test) - Raytheon THK-8000A	9
7.	WG Variable Attenuator - Narda #730 - X-Band, or	9
	WG Variable Attenuator - Narda #729 - Ku-Band	9
8.	SMA Coax to WG Transition - Am. 6254 - X-Band, or	9
	SMA Coax to WG Transition - Am. 6255 - Ku-Band	9
9.	SMA to SMA Semi-Rigid Coax Cable Assembly	9
10.	Coax SP9T Microwave Switch - Raytheon SKEL-5009	1
11.	Switch Driver Board - (12) LRC SD1201 Single Drivers	1
12.	Power Supply (Driver) - Raytheon Design	1
13.	Automatic Electronic Programmer - Raytheon Design	1
14.	Coax Atten Pad (Fixed) - Hewlett Packard 8493B	1
15.	Coax Detector Mount - Hewlett Packard #8472A	1
16.	Strip Chart Recorder - Simpson Model 604	1
17.	Extruded Heat Sink - Wakefield Engineering #180-12-36C	1
18.	Water Circulating System - Forma Scientific #2095	1

programmer is set so that each diode position on the station is sampled for approximately 2.6 hours over each 24-hour period.

The cavities are securely mounted to a heat sink surface that is temperature controlled by a closed loop water circulating system that has both heating and refrigerating capability. The circulating system maintains the heat sink temperature of each station to within $\pm 3^{\circ}C$ of the setting. Each of the heat sinks are equipped with thermal sensing devices that will automatically shut off all electrical power should a preset temperature be exceeded. This provides protection against failure of the circulating system. If electrical power is interrupted for any reason, such as a power failure, the system will remain shut off until power is restored manually.

Figures 4-2 and 4-3 are photographs of the individual test stations described. Figure 4-4 is a photograph of the overall system.

The current regulator circuit selected for use in the operating life stations is a constant-current regulator design that was developed by Raytheon with independent development funding. The output section of this regulator is capable of delivering bias voltage levels up to 200 VDC at 600 milliamps. The regulator is fabricated from standard components. The design took into account the many limitations imposed by the practicalities of power supplies, transistors, I.C.s, and IMPATT diodes. Extensive use of manufacturer's data was used in an effort to more closely define operating parameters, control efficiency and cost, increase reliability of operation, protect all devices, and keep physical size within practical limits. The resulting design has produced the current regulator circuit shown as a block diagram in Figure 4-5. This circuit not only operates over a large current range (0-600 mA), but also provides "fail-safe" protection against diode failure and is essentially immune from power system disturbances as evidenced by a

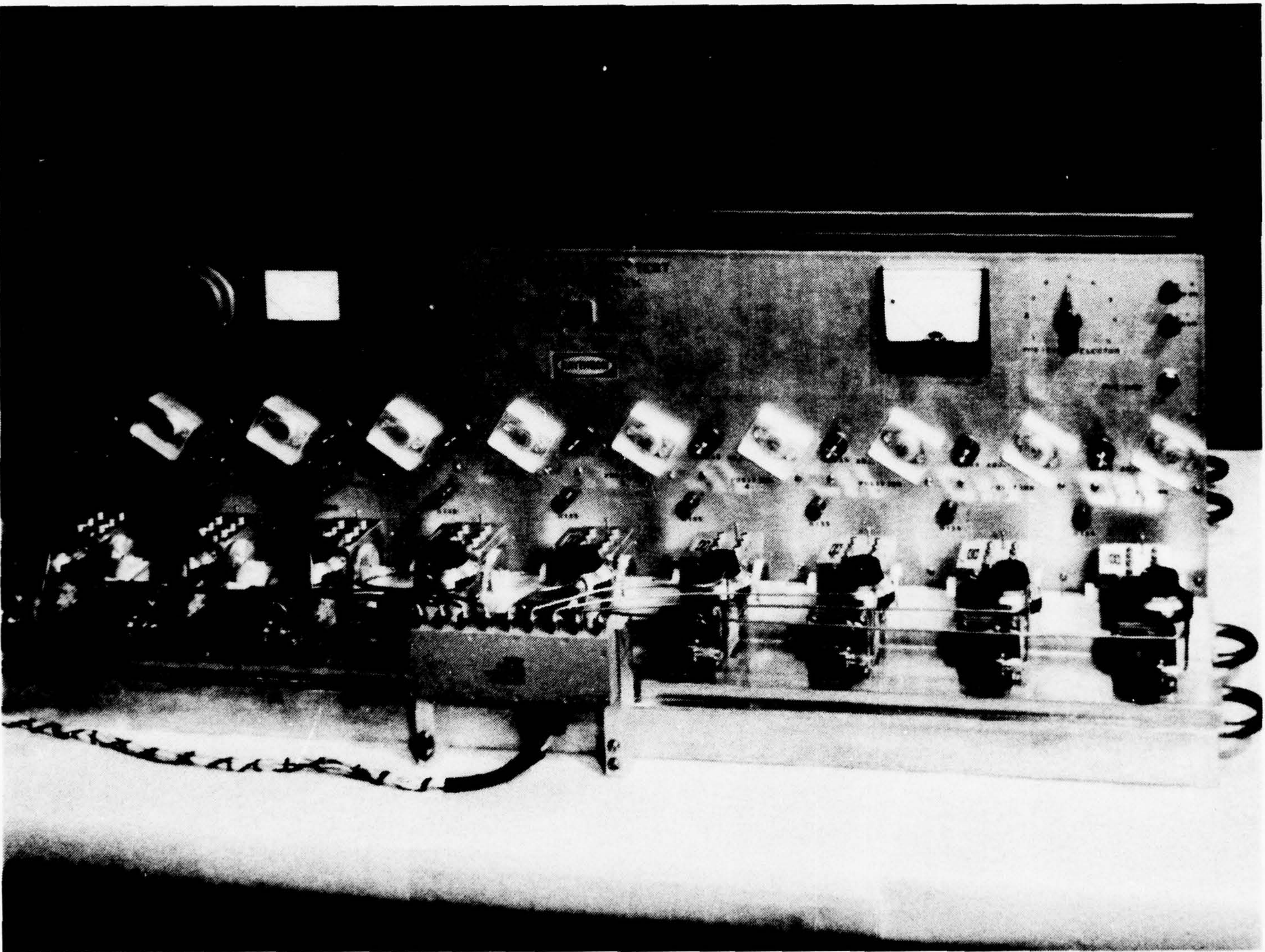

Figure 4-2 Photograph - X-Band Test Station

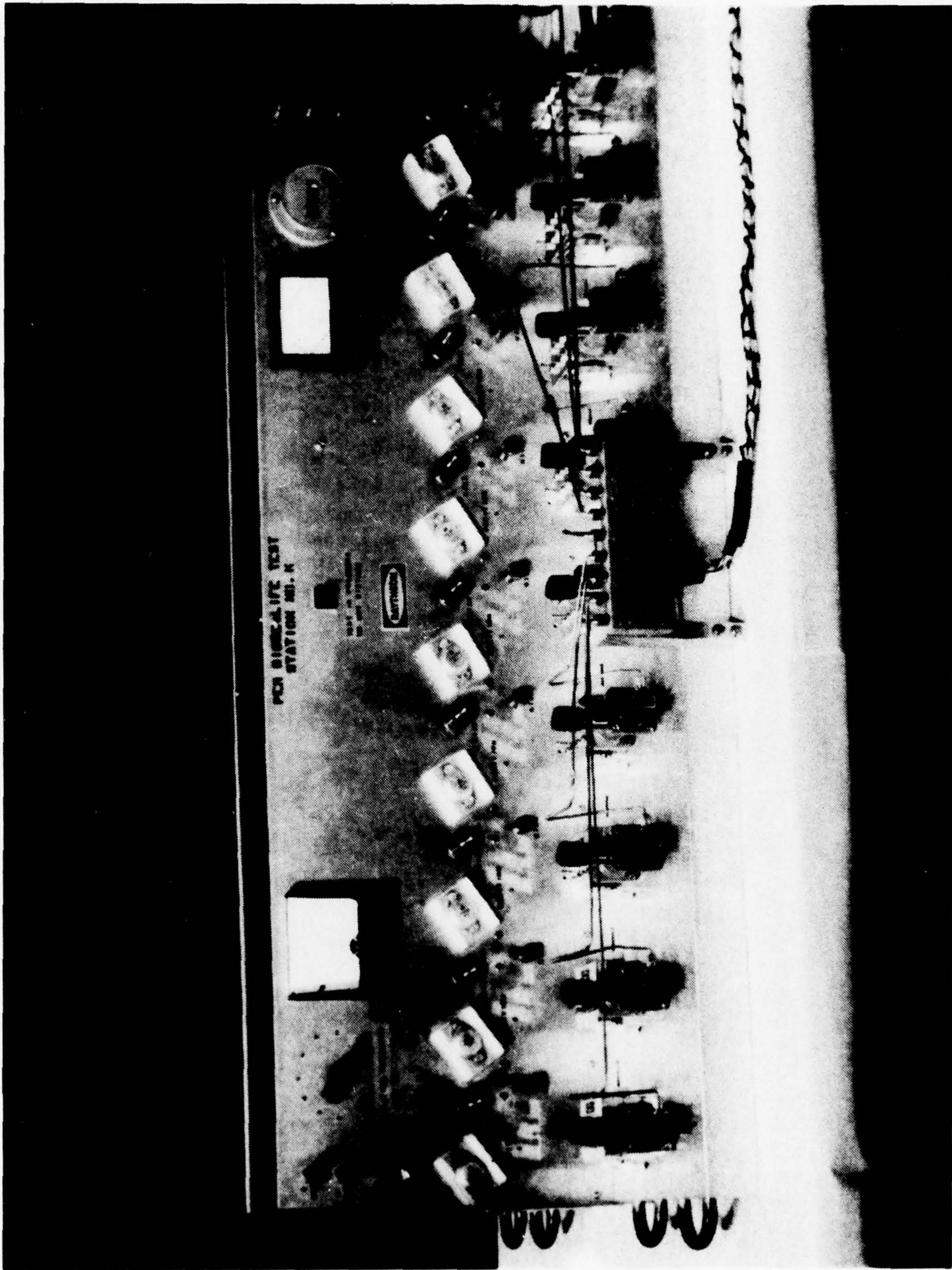

Figure 4-3 Photograph - Ku-Band Test Station

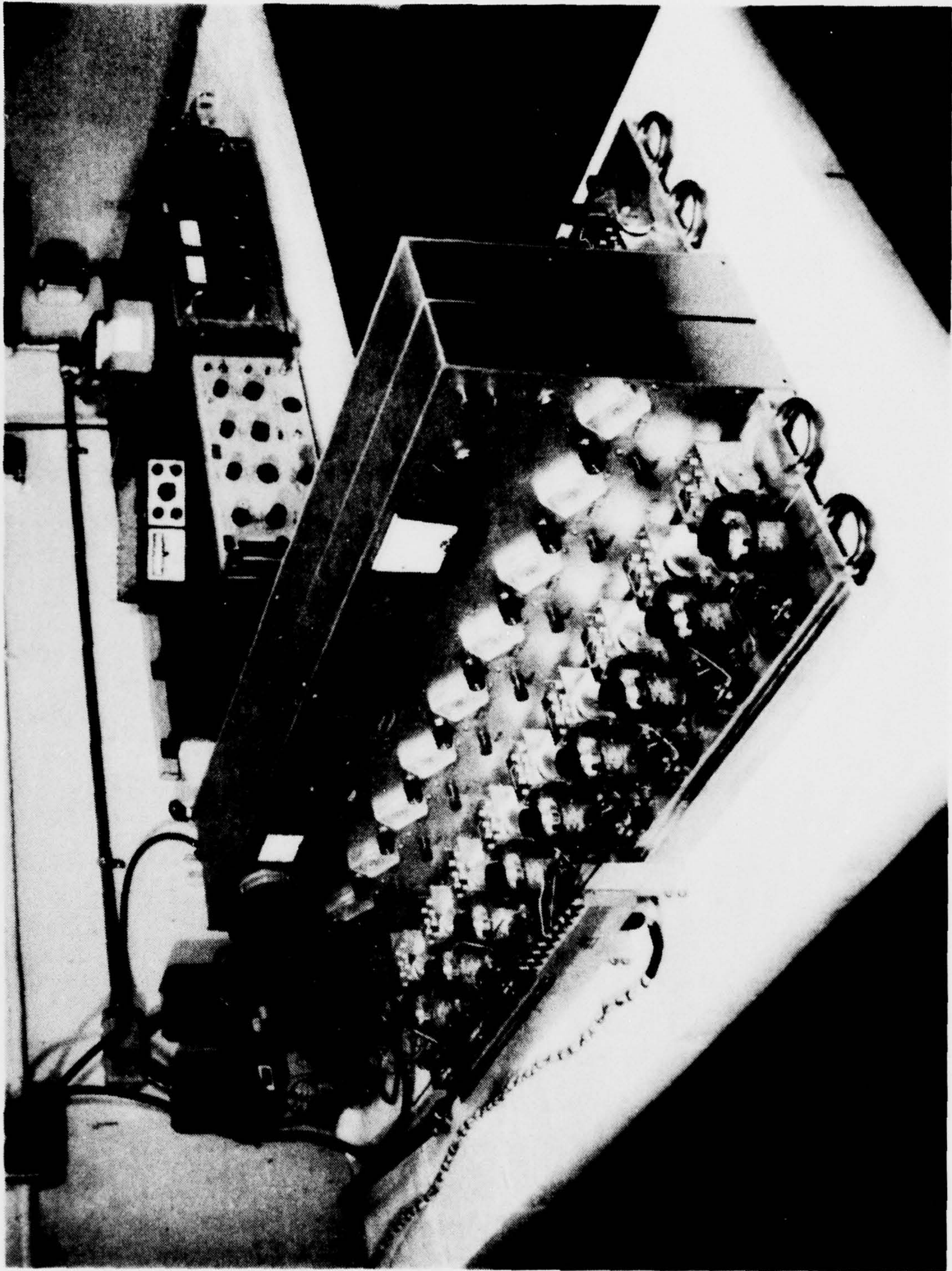

Figure 4-4 Photograph - Overall Test System

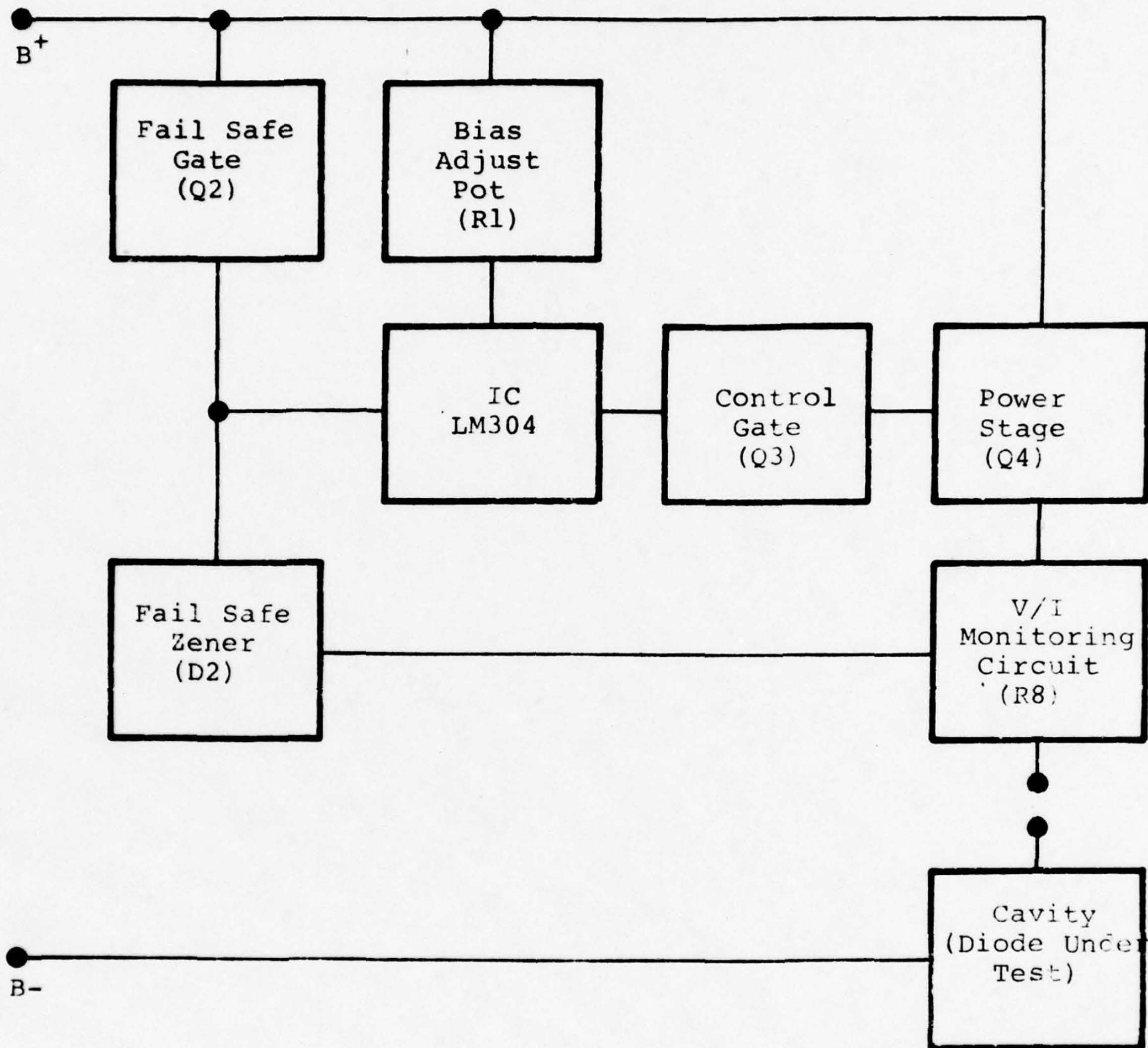

Figure 4-5 Current Regulator Block Diagram

supply isolation exceeding 20 dB out to greater than 10 MHz. Effect on regulator due to all causes (long-term drift, power supplies, temperature, transients, etc.) is typically less than 0.5%.

The basic integrated negative voltage regulator used in this design is the inexpensive LM304 whose output can be clamped to zero by shorting the bias adjust potentiometer R_1. This is an important feature since the current regulator will deliver no output with the IC output at zero. In most situations, when the diode being driven by the current regulator fails, it is necessary to shut down the regulator either to protect the regulator, conserve power, or to signal distress. With the circuit being described, the diode failure is sensed by Zener diode (D_2) which turns on transistor Q_2, thus shorting the adjustment potentiometer (R_1). With R_1 shorted and the IC clamped to zero, the power transistor Q_4 will shut down in less than a millisecond; sufficiently fast to avoid damaging the regulator. Figure 4-6 is a photograph of the current regulator printed circuit board fabricated for use in the operating life test stations. Each position on the test station contains one of these regulators. Ten-turn precision potentiometers (R_1) and the power transistors (Q_4) are outboarded on a control panel. The voltage and current monitoring points are connected to a multi-wafer switch located on the control panel where each position on the test station can be selected individually for readout on an appropriate meter. The voltage monitoring points are connected to a standard 0-100 VDC voltmeter mounted on the panel. Current monitoring is achieved indirectly by connecting a high impedance digital voltmeter to the current monitoring terminals. The voltage readout is directly proportional to the current thru R_8 which, in turn, is essentially the same current that is delivered to the diode under test thru the power transistor (Q_4).

4.2.1 Test Cavities

The cavities fabricated for test purposes are essentially the same cavity described in Section 1.0 of this report and

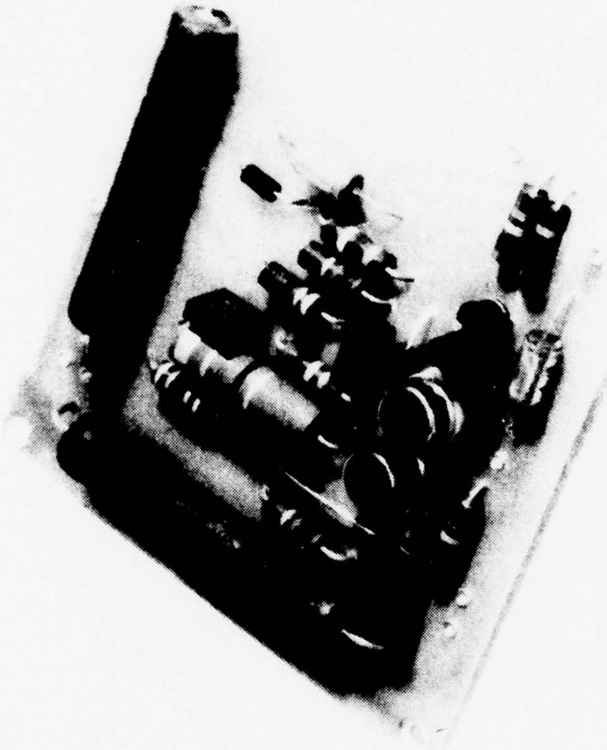

Figure 4-6 Photograph - Current Regulator Circuit

shown in Figure 1-5. To facilitate the use of this cavity for the operating life test station, the design was modified to incorporate into the assembly a sliding short. The cavities are designated THX-8000A (X-Band) and THK-8000A (Ku-Band). Drawings are included in Section II-D of this report.

Two outwardly identical configurations are utilized; one designed for X-band operation and the other for Ku-band. Copper construction was chosen because of its good heat transfer characteristics. Light tin plating is employed as corrosion protection. A simple two section, low pass filter network serves as the bias terminal. A thin layer of teflon around the filter insulates the bias terminal from the cavity body. The noncontacting sliding short circuit is of a standard design and is built in as part of the cavity. A tin-plated copper tapered chuck retains the diode and provides optimum heat transfer from diode to cavity body. Figures 4-7 and 4-8 are photographs of the X and Ku-band cavities just described. When used on the life test station, the cavities are bolted to the heat sink surface in the position shown in the photograph; i.e., with the side of the cavity against the heat sink. This affords easy access to both the bias terminal and the diode chuck holder.

4.3 Life Testing Procedure

All diodes which were to be tested had been previously tested to the electrical specification and subjected to an in-process "burn-in". Randomly selected diodes were then loaded into the test cavities and installed on the life test system. To accomplish this, the following procedure is utilized:

The cavity and its attenuator are first removed from the rack. This assembly with diode mounted in place is placed into the standard production RF test system to replace the standard production test cavity. The assembly is then tuned for the desired power level and the following data recorded: power output, frequency, bias voltage

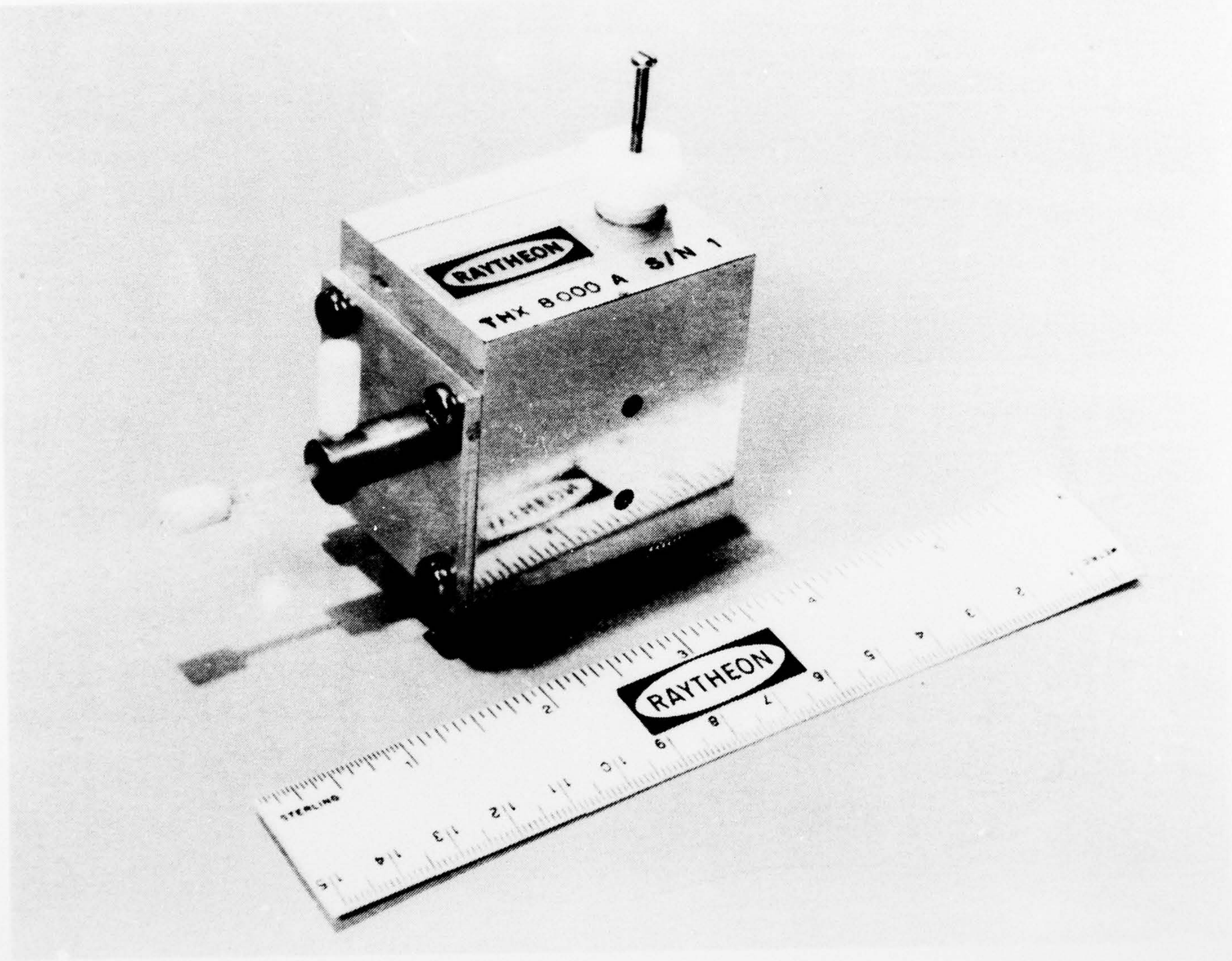

Figure 4-7 X-Band Test Cavity

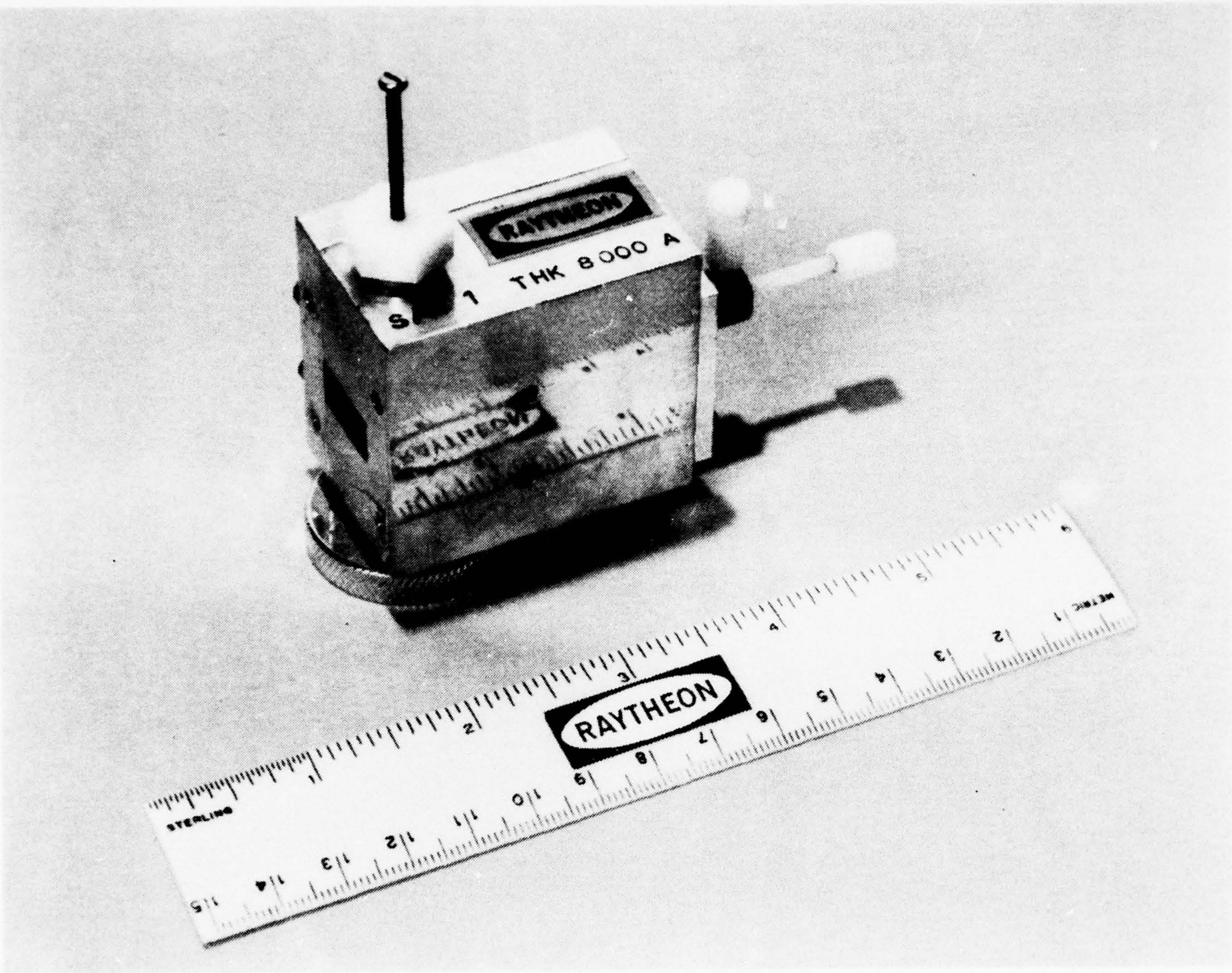

Figure 4-8 Ku-Band Test Cavity

and current. The attenuator setting is set at approximately 15 dB which renders the cavity relatively immune to loading effects. The cavity and its attenuator are then reinstalled on the life test station heat sink.

After the diodes to be life tested have been installed in this manner, the station is ready to be activated by applying supply voltage; i.e., 90 VDC, -12 VDC, and 110 VAC. Application of these voltages will energize the running time meter. The bias voltage and current requirements for each diode are set by first switching the position switch to the desired cavity. After connecting the cavity bias terminal to the appropriate bias terminal on the control panel, a momentary switch is depressed and by use of the bias adjust potentiometer, the desired voltage and current are set as readout on monitoring meters. The momentary switch depression is necessary to override a Zener diode clamping circuit in the current regulator which keeps the bias voltage and current at zero as long as the diode bias voltage is greater than 70 VDC below B+ (90 VDC). This is a built-in safety precaution that allows the regulator to completely shut down should a diode fail (short). The depressed momentary switch can be released anytime after the bias adjust potentiometer has been adjusted sufficiently so that the voltage across the diode exceeds 20 VDC. After setting the bias to the desired meter reading, the next position is selected by the position switch and the procedure repeated until all active positions have the proper bias applied and all diodes are oscillating.

Again, each position is manually selected on the programmer, and the variable attenuator adjusted to produce identical near full scale deflections on the strip chart recorder. A calibration level representing a 25% power reduction is then noted on the recorder. The programmer is set to automatic and the life test commences. Each of the outputs, in turn, contribute to a constant level on the recorder and anytime an output falls below the 25% calibration point, that position is deemed to have a diode failure.

During the 1000-hour test cycle, periodic daily checks were performed on the test stations and all pertinent data recorded on a data sheet; i.e., bias voltage and current, significant changes in output level and running time.

4.4 Summary of Results

The following is a summary of the results obtained during the operating life test program.

	X-Band		Ku-Band	
Test Number	Qty. Tested	Failures	Qty. Tested	Failures
1	5	1	5	1
2	5	1	5	5*
3	5	1	5	0
4	5	0	5	0
5	5	0	5	1
6	5	0	5	0
7	5	0	5	0
Totals	35	3	35	7

* System malfunction caused catastrophic failure of all devices.

It should be noted that all of the failures occurred early in the program. There was only one failure after the third test. In addition to the above results, additional diodes were life tested to fulfill the confirmatory and pilot run Group B test requirements. Nine diodes of each type were used each time and there were no failures in these tests.

In the first test, the two failures were found to be defective diodes; one had a gold filament, the other exhibited a soft breakdown voltage characteristic, the cause of which was not positively assigned. In the second test, one diode failed because of cavity detuning; five failed catastrophically due to failure of the Ku-band system. Failures in the second test were not diode related. Remaining failures in the later testing were also found to be most probably caused by cavity tuning problems. This is,

in turn, attributable to a mechanically erratic microwave short incorporated as part of the construction of the life test cavities. Use of this concept allowed the economic testing of the diodes on this program while avoiding the cost of expensive precision microwave shorts.

5.0 PILOT RUN

The pilot run for this program consisted of five hundred (500) X-band diodes (MS-50371) and five hundred (500) Ku-band diodes (MS-50372). These diodes were manufactured in accordance with the process specifications included in this report and then tested in accordance with the diode specification SCS-481. The test data is included in Appendix I-A.

5.1 X-Band Diodes

The average breakdown voltage for the diodes is 42.9 Volts. A specification of 30-50 Volts was established based upon observations that few diodes above 50 Volts operated successfully while diodes as low as 30 Volts worked quite well. The operating voltage is typically 58 Volts, the 15 Volt increase above the breakdown voltage being due to the combined effect of the diode series resistance and heating as the current is increased to a typical operating value of 260 ma. The operating current and voltage are well below the specification limits of 500 ma and 70 Volts.

The diode capacitance has an average value of 1.85 picofarads with a range of 1.6 - 2.2 pf. The specification was empirically established. Diodes having a lower value of capacitance had saturated output power below the specification value or else operated at junction temperatures above the specification limit. Difficulty in tuning was experienced with diodes whose capacitance was above 2.2 pf, which resulted in poor efficiency.

The diodes were tested at 3.5 Watts power output at a frequency of approximately 9.5 GHz. The diodes will typically deliver as much as 5 Watts of output power and no difficulty was experienced with the 3.5 Watt specification; 3.5 Watts is typically available in a 2 GHz bandwidth, thus the ±250 MHz specification was readily met as well. The choice of 9.5 GHz as the test frequency

was made on the basis of noise measurements. A reference cavity was available for noise measurements at the selected test frequency.

The efficiency for the X-band diodes was in the range of 23-25% for the majority of the diodes, which is a good value for a 20% minimum specification.

The operating junction temperature was calculated from measurements of thermal resistance and power dissipated during RF test. A specification maximum of 16.0^{o}C/W is recommended for thermal resistance. This limit rejects diodes which are very poor thermally as a result of manufacturing anomalies. Within the specification limit, diodes are rejectable if the combination of thermal resistance and efficiency yields an operating temperature above 200°C. The following table shows the maximum thermal resistance allowable for various diode efficiencies.

Minimum Diode Efficiency	Maximum Thermal Resistance
20	12.5
21	13.3
22	14.1
23	14.9
24	15.8
25	16.7

The average value for thermal resistance is 13°C/W with a range of 10-16°C/W. The average operating junction temperature is about 175°C.

The AM and FM noise are within the specification as shown by the data. External Q was typically 80 during the noise measurement. Actual values were not calculated for each diode. The external Q was measured by injection locking techniques. The locking bandwidth corresponding to the specification limit was indicated on the spectrum analyzer. Conformance to specification was verified by the operator prior to test but data was not recorded.

5.2 Ku-Band Diodes

A parallel discussion to that above applies to the Ku-band diodes. The Ku-band diodes have typically lower efficiency than the X-band. Twenty-three percent is a lower limit for the X-band units, while very few Ku-band devices achieve that value. This requires a tighter control on thermal resistance to achieve the operating junction temperatures below the maximum value. Lots 41436 and 41435 have breakdown voltage and operating voltage higher than Lot 41427. Lot 41427 has an optimized efficiency at 15 GHz, while the former lot has best efficiency at 14.3 GHz. The lower breakdown voltage for 41427 results in lower operating voltage and higher current.

5.3 Group B Testing

The Group B testing consisted of the following sequence of tests:

1) Operating Life Test (9 diodes of each type)

	X-Band	Ku-Band	
Oscillator Frequency:	10.0 ±1.0	15.0 ±1.0	GHz
Oscillator Output Power (min):	3.5	2.5	Watts
Oscillator Efficiency (min):	20	20	%
Junction Temperature (max.):	200	200	°C
Ambient Temperature:	25 ±3	25 ±3	°C
Test Duration:	1000	1000	Hours

2) Storage Life - Nonoperating (9 diodes of each type)

Ambient Temperature:	200°C
Test Duration:	1000 Hours

3) <u>Nuclear Radiation Exposure</u> (3 diodes of each type)

Power Level:	10 KW
Exposure Time:	7 Minutes
Gamma Exposure:	1.2×10^5 rads (Silicon)
Neutron Exposure:	1.04×10^{13} n/cm^2, 1 Mev Si damage equivalent

4) <u>Shock, Vibration, Accelerating, Hermeticity</u> (4 diodes of each type)

Shock MIL-STD-750, Method 2016

500 G, 1 ms
1/2 Sine Pulse 3 planes
5 shocks per plane

Vibration MIL-STD-750, Method 2056

20 G
50 - 2000 - 50 Hz
3 planes - 4 cycles/plane
3 minutes/cycle

Acceleration MIL-STD-750, Method 2006

20,000 G
3 planes
1 minute/plane

Hermeticity MIL-STD-750, Method 1071, Condition H

4 hours @ 60 psi Helium
1×10^{-8} atm cc/sec. maximum

Test results for Group B testing are included in Appendix I-A. There were no failures in any of the group tests.

APPENDIX A

TEST DATA

DATA SHEET - SCS 481 - TYPE 1 (MS-50371)

CHARACTERISTIC		B_V	C_{TVR}	R_{TH}	P_O	F_o	V_{OP}	I_{OP}	η	Mech. Tun.	HAT	T_J	$Q_{Ext.}$	ΔF_{RMS}	(N/S)AM
TEST CONDITION		Ima	V_B=25V												
UNITS		Volts	P_F	°C/W	Watts	GHz	Volts	ma	%			°C		Hz	db
LIMITS	MIN.	30	1.6	---	3.5	9	---	---	20	+ 250	.360	---	---	---	---
	MAX.	50	2.2	16.0	---	11	70	500	---	---	.420	200	200	50	-115
Serial No.	Diode I.D. Number														
2.11	41415B-G-3	42.1	1.87	13.6	3.5	9.5	55.7	260	22.8	OK	410x2	174	OK	0.20	133
2.12	7	44.6	1.84	13.5	3.5	9.6	58.8	250	23.8	OK	410x2	176	OK	0.20	132
2.13	8	44.7	1.89	13.2	3.5	9.4	60.2	252	23.0	OK	410x2	179	OK	0.25	131
2.14	9	41.9	1.87	12.2	3.5	9.4	55.8	255	24.5	OK	410x2	156	OK	0.20	131
2.15	10	37.9	1.87	14.1	3.5	9.5	55.6	275	22.8	OK	410x2	191	OK	0.25	130
2.16	11	36.9	1.78	14.7	3.5	9.6	54.5	260	24.7	OK	410x2	181	OK	0.19	131
2.17	12	41.8	1.82	13.0	3.5	9.5	57.4	257	23.7	OK	410x2	171	OK	0.20	135
2.18	13	43.2	1.81	11.0	3.5	9.5	58.5	254	23.6	OK	410x2	150	OK	0.50	130
2.19	14	47.0	1.81	10.5	3.5	9.4	60.0	250	23.3	OK	410x2	146	OK	0.40	135
2.20	17	42.1	1.88	13.4	3.5	9.4	56.3	264	23.3	OK	410x2	177	OK	0.20	132
2.21	18	41.5	1.88	13.4	3.5	9.4	57.7	260	22.8	OK	410x2	179	OK	0.20	133
2.22	19	43.8	1.89	12.2	3.5	9.5	57.9	265	22.8	OK	410x2	169	OK	0.50	134
2.23	20	43.2	1.63	12.3	3.5	9.4	58.5	258	23.1	OK	410x2	167	OK	0.25	132
2.24	27	39.7	1.83	14.7	3.5	9.6	56.5	270	22.9	OK	410x2	191	OK	0.19	134
2.25	30	46.0	1.88	11.8	3.5	9.5	58.5	252	22.7	OK	410x2	158	OK	0.50	130
2.26	31	45.3	1.83	12.5	3.5	9.5	59.3	261	23.7	OK	410x2	175	OK	0.25	133
2.27	36	47.7	1.89	12.2	3.5	9.5	60.2	273	21.2	OK	410x2	183	OK	0.30	135
2.28	37	38.7	1.86	12.8	3.5	9.6	55.9	270	23.1	OK	410x2	173	OK	0.25	135
2.29	38	47.0	1.82	10.5	3.5	9.5	60.7	270	21.2	OK	410x2	160	OK	0.70	134
2.30	41415B-H-2	40.5	1.83	13.6	3.5	9.6	56.8	265	23.3	OK	410x2	182	OK	0.18	133

Sheet 21

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DATA SHEET - SCS 481 - TYPE 1 (MS-50371)

CHARACTERISTIC		B_V	C_{TVR}	R_{TH}	P_O	F_o	V_{OP}	I_{OP}	η	Mech. Tun.	HAT	T_J	$Q_{Ext.}$	ΔF_{RMS}	(N/S)AM
TEST CONDITION		1ma	V_B=25V												
UNITS		Volts	P_F	°C/W	Watts	GHz	Volts	ma	%			°C		Hz	db
LIMITS MIN.		30	1.6	---	3.5	9	---	---	20	+ 250	.360	---	---	---	---
LIMITS MAX.		50	2.2	16.0	---	11	70	500	---	---	.420	200	200	50	-115
Serial No.	Diode I. D. Number														
371	41410C-P-22	44.6	1.88	12.6	3.5	9.4	58.0	2.85	21.0	OK	410x2	189	OK	0.60	138
372	24	40.8	1.83	13.3	3.5	9.4	55.7	2.93	21.4	OK	410x2	175	OK	0.50	136
373	25	44.2	1.85	14.1	3.5	9.3	58.8	2.68	22.2	OK	410x2	197	OK	0.55	138
374	29	45.0	1.84	13.2	3.5	9.4	58.4	2.40	25.0	OK	410x2	164	OK	0.50	136
375	31	35.6	1.87	12.3	3.5	9.6	53.0	2.90	22.8	OK	410x2	171	OK	0.11	143
376	41410C-C-1	41.5	1.88	11.8	3.5	9.4	56.9	2.85	21.6	OK	410x2	175	OK	0.20	138
377	2	45.0	1.82	11.7	3.5	9.4	58.4	2.74	21.9	OK	410x2	174	OK	0.75	139
378	9	44.9	1.88	12.8	3.5	9.5	57.6	2.80	21.7	OK	390x2	186	OK	0.45	137
379	10	43.9	1.86	12.5	3.5	9.3	57.7	2.80	21.7	OK	390x2	183	OK	0.17	137
380	17	47.5	1.87	11.9	3.5	9.3	59.2	2.72	21.7	OK	390x2	175	OK	0.50	137
381	18	42.7	1.87	14.2	3.5	9.7	57.6	2.50	24.2	OK	410x2	179	OK	0.45	137
382	19	44.0	1.86	12.9	3.5	9.6	58.4	2.42	24.5	OK	410x2	162	OK	0.04	142
383	24	43.2	1.90	13.5	3.5	9.6	58.8	2.58	23.0	OK	410x2	182	OK	0.12	137
384	29	45.2	1.87	13.4	3.5	9.5	57.9	2.80	21.6	OK	400x2	195	OK	0.09	140
385	31	47.0	1.88	13.0	3.5	9.5	59.1	2.85	20.7	OK	400x2	198	OK	0.60	137
386	36	43.1	1.85	13.9	3.5	9.5	57.0	2.60	23.6	OK	400x2	182	OK	0.40	143
387	38	44.3	1.74	13.3	3.5	9.6	57.9	2.64	22.9	OK	400x2	181	OK	0.25	145
388	39	44.2	1.85	12.0	3.5	9.5	57.3	2.64	23.1	OK	400x2	164	OK	0.50	140
389	41	40.8	1.87	14.5	3.5	9.5	56.4	2.75	22.6	OK	400x2	199	OK	0.06	141
390	43	44.1	1.87	12.0	3.5	9.5	57.5	2.73	22.2	OK	400x2	171	OK	0.40	141

Sheet 21

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DATA SHEET - SCS 481 - TYPE 1 (MS-50371)

CHARACTERISTIC		B_V	C_{TVR}	R_{TH}	P_O	F_o	V_{OP}	I_{OP}	η	Mech. Tun.	HAT	T_J	$Q_{Ext.}$	ΔF_{RMS}	(N/S)AM
TEST CONDITION		1ma	V_B=25V												
UNITS		Volts	P_F	°C/W	Watts	GHz	Volts	ma	%			°C		Hz	db
LIMITS	MIN.	30	1.6	---	3.5	9	---	---	20	± 250	.360	---	---	---	---
	MAX.	50	2.2	16.0	---	11	70	500	---	---	.420	200	200	50	-115
Serial No.	Diode I. D. Number														
611	41413B-B-33	37.9	1.87	13.2	3.5	9.6	56.9	245	25.1	OK	410x2	163	ok	0.10	144
612	34	41.0	1.90	12.1	3.5	9.5	58.0	250	24.1	OK	410x2	158	ok	0.10	145
613	35	43.5	1.94	12.6	3.5	9.4	59.4	240	24.6	OK	410x2	160	OK	0.14	144
614	36	40.0	1.87	13.1	3.5	9.5	57.7	246	24.7	OK	410x2	165	ok	0.11	146
615	37	47.2	1.93	12.0	3.5	9.5	61.6	230	24.7	OK	410x2	153	ok	0.19	150
616	39	44.2	1.93	12.4	3.5	9.4	60.0	235	24.8	OK	410x2	156	OK	0.15	144
617	41	42.0	1.84	12.0	3.5	9.6	57.9	236	25.6	OK	410x2	157	OK	0.04	141
618	41413B-C-3	37.2	1.91	14.3	3.5	9.7	55.0	259	24.6	ok	410x2	179	ok	0.22	141
619	4	42.7	1.93	14.6	3.5	9.5	58.6	246	24.2	ok	410x2	184	OK	0.16	143
620	5	42.1	1.94	12.5	3.5	9.5	59.5	252	23.3	OK	410x2	180	ok	0.25	[illegible]
621	6	43.6	1.89	13.6	3.5	9.4	60.5	235	24.6	ok	410x2	171	ok	0.17	149
622	7	45.8	1.92	13.3	3.5	9.5	60.4	240	24.1	ok	410x2	171	ok	0.17	150
623	8	20.5	1.88	15.9	3.5	9.7	50.2	285	24.5	OK	410x2	196	ok	[illegible]	150
624	9	40.4	1.90	13.2	3.5	9.5	58.4	240	25.0	ok	410x2	164	ok	0.10	148
625	10	43.2	1.86	12.8	3.5	9.6	[illegible]	235	25.0	OK	410x2	170	ok	0.11	144
626	12	41.1	1.91	13.9	3.5	9.5	58.3	250	24.0	ok	410x2	179	ok	0.15	143
627	13	40.4	1.88	13.7	3.5	9.5	57.1	247	24.8	ok	410x2	170	ok	0.07	148
628	14	46.2	1.89	14.4	3.5	9.5	61.7	235	24.1	OK	410x2	184	OK	0.25	156
629	15	38.2	1.84	13.8	3.5	9.6	55.8	246	25.5	OK	410x2	166	ok	0.20	148
630	16	43.1	1.91	14.3	3.5	9.6	58.8	235	25.3	ok	410x2	172	ok	0.25	155

DATA SHEET - SCS481 - TYPE 2 (MS-50372)

CHARACTERISTIC		B_V	C_{TVR}	R_{TH}	P_o	F_o	V_{OP}	I_{OP}	η	Mech. Tun.	HAT	T_J	$Q_{Ext.}$	ΔF_{RMS}	(N/S)AM
TEST CONDITION		1ma	V_R = 10V												
UNITS		Volts	P_F	°C/W	Watts	GHz	Volts	ma	%			°C		Hz	db
LIMITS	MIN.	16	1.6	---	2.5	14	---	---	20	±250	150	---	---	---	---
	MAX.	32	2.4	22	---	16	70	500	---	---	220	200	200	50	-115
Serial No.	Diode I. D. Number														
651	414[illegible]-[illegible]-38	29.4	2.29	17.1	2.5	14.1	40.0	302	20.7	OK	190	189	OK	20	135
652	41	26.6	2.45	17.3	2.5	14.0	40.2	312	20.0	OK	190	198	OK	10	127
653	42	32.8	2.07	15.0	2.5	14.0	43.4	264	21.8	OK	200	160	OK	15	133
654	41435B-B- 8	29.5	2.20	16.8	2.5	14.[illegible]	40.8	293	20.9	OK	190	184	OK	20	136
655	12	28.3	2.30	17.0	2.5	14.[illegible]	41.6	292	[illegible]	OK	190	189	OK	22	133
656	16	29.3	2.35	16.0	2.5	14.[illegible]	41.4	304	20.5	OK	190	180	OK	20	134
657	29	29.0	2.22	15.3	2.5	14.0	41.0	294	20.7	OK	190	172	OK	22	137
658	30	34.3	2.23	14.0	2.5	14.1	42.5	295	20.6	OK	190	160	OK	24	131
659	31	27.8	2.16	17.2	2.5	14.[illegible]	40.7	293	21.0	OK	190	187	OK	10	138
660	32	28.7	2.31	17.0	2.5	14.1	40.4	259	21.4	OK	190	181	OK	24	136
661	3[illegible]	35.4	2.15	14.0	2.5	14.[illegible]	44.1	265	21.4	OK	190	154	OK	18	140
662	3[illegible]	31.3	2.19	14.8	2.5	14.1	41.8	290	20.6	OK	190	168	OK	20	136
663	3[illegible]	34.5	2.18	12.6	2.5	14.1	42.0	298	20.0	OK	190	151	OK	35	134
664	39	33.9	2.12	13.5	2.5	[illegible]	43.6	267	21.5	OK	190	148	OK	10	130
665	4[illegible]	30.7	2.16	15.5	2.5	14.2	42.1	290	20.5	OK	190	175	OK	10	136
666	41	33.5	2.20	14.4	2.5	14.1	41.7	294	20.4	OK	190	165	OK	20	136
667	4[illegible]	30.8	1.96	17.0	2.5	14.2	41.7	294	[illegible]	OK	190	191	OK	25	135
668	4[illegible]	29.5	1.85	17.6	2.5	14.[illegible]	41.7	297	22.2	OK	190	199	OK	20	134
669	46	33.6	2.24	14.0	2.5	14.1	42.4	297	[illegible]	OK	190	161	OK	25	136
670	47	27.6	2.32	16.8	2.5	14.1	40.5	307	20.1	OK	190	192	OK	30	132

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DATA SHEET - SCS481 - TYPE 2 (MS-50372)

CHARACTERISTIC		B_V	C_{TVR}	R_{TH}	P_o	F_o	V_{OP}	I_{OP}	η	Mech. Tun.	HAT	T_J	$Q_{Ext.}$	ΔF_{RMS}	(N/S)AM
TEST CONDITION		1ma	V_R = 10V												
UNITS		Volts	P_F	°C/W	Watts	GHz	Volts	ma	%			°C		Hz	db
LIMITS	MIN.	16	1.6	---	2.5	14	---	---	20	± 250	150	---	---	---	---
	MAX.	32	2.4	22	---	16	70	500	---	---	220	200	200	50	-115
Serial No.	Diode I. D. Number														
731	41436A - C - 16	26.4	2.31	15.3	2.5	14.3	42.1	285	20.8	OK	190	171	OK	12	142
732	17	27.2	2.24	14.8	2.5	14.2	41.0	301	20.3	OK	190	170	OK	10	135
733	26	25.7	2.35	15.9	2.5	14.[illegible]	40.1	298	20.9	OK	190	175	OK	20	127
734	27	24.8	2.37	15.8	2.5	14.4	40.6	299	20.6	OK	190	177	OK	15	141
735	28	32.0	2.04	14.5	2.5	14.1	39.9	298	21.0	OK	190	161	OK	17	131
736	29	25.4	2.27	15.9	2.5	14.3	37.9	298	21.0	OK	190	175	OK	16	140
737	30	26.7	2.23	14.8	2.5	14.[illegible]	40.6	285	21.6	OK	190	159	OK	9	140
738	31	26.5	2.32	17.2	2.5	14.1	41.1	291	20.0	OK	190	197	OK	17	129
739	32	26.0	2.29	14.6	2.5	14.1	40.5	282	21.9	OK	190	155	OK	25	134
740	33	24.6	2.31	16.8	2.5	14.5	39.8	309	21.9	OK	190	175	OK	30	131
741	34	[illegible]	2.28	14.4	2.5	14.5	41.7	276	21.7	OK	190	155	OK	25	131
742	41436A - D - 7	28.2	2.35	15.2	2.5	14.3	41.1	290	21.0	OK	190	168	OK	9	135
743	8	26.8	[illegible]	15.8	2.5	14.2	41.2	29[illegible]	20.7	OK	190	176	OK	17	135
744	9	27.1	2.27	15.5	2.5	14.3	41.3	298	20.2	OK	190	177	OK	16	133
745	10	28.5	2.37	15.4	2.5	14.1	41.9	284	21.0	OK	190	170	OK	20	137
746	11	27.4	2.25	15.7	2.5	14.2	41.4	289	20.9	OK	190	174	OK	16	138
747	14	26.9	[illegible]	16.4	2.5	14.1	41.1	293	20.8	OK	190	181	OK	20	136
748	15	27.0	2.31	16.4	2.5	14.2	41.0	293	20.8	OK	190	181	OK	15	136
749	18	24.7	2.25	17.4	2.5	14.2	40.0	312	20.0	OK	190	199	OK	12	139
750	19	27.4	2.23	17.0	2.5	14.4	41.0	302	20.2	OK	190	193	OK	8	140

Sheet 22

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DATA SHEET - SCS481 - TYPE 2 (MS-50372)

CHARACTERISTIC		B_V	C_{TVR}	R_{TH}	P_o	F_o	V_{OP}	I_{OP}	η	Mech. Tun.	HAT	T_J	$Q_{Ext.}$	ΔF_{RMS}	(N/S)AM
TEST CONDITION		Ima	V_R = 10V												
UNITS		Volts	P_F	°C/W	Watts	GHz	Volts	ma	%			°C		Hz	db
LIMITS	MIN.	16	1.6	---	2.5	14	---	---	20	±250	150	---	---	---	---
	MAX.	32	2.4	22	---	16	70	500	---	---	220	200	200	50	-115
Serial No.	Diode I. D. Number														
[illegible]	[illegible] - 6	21.6	2.14	15.8	2.5	14.3	37.4	318	21.0	OK	170	174	OK	20	132
[illegible]	7	25.7	2.53	15.0	2.5	14.6	40.1	297	20.0	OK	165	166	OK	20	129
[illegible]	8	25.6	2.55	14.3	2.5	14.5	39.6	289	21.8	OK	165	153	OK	17	133
[illegible]	9	25.5	2.62	14.7	2.5	14.5	41.5	286	21.1	OK	175	162	OK	20	135
[illegible]	10	25.7	2.47	14.6	2.5	14.7	40.5	290	21.3	OK	165	160	OK	20	131
[illegible]	11	20.6	2.57	16.9	2.5	14.3	37.0	328	20.6	OK	165	188	OK	18	131
[illegible]	13	20.3	2.54	15.9	2.5	14.7	36.5	342	20.0	OK	175	184	OK	40	137
[illegible]	14	19.3	2.55	16.9	2.5	14.3	34.7	354	20.4	OK	175	190	OK	40	137
[illegible]	15	20.1	2.50	15.9	2.5	14.8	35.8	344	20.0	OK	160	184	OK	35	135
[illegible]	20	25.1	2.61	15.5	2.5	14.5	40.0	288	21.7	OK	165	165	OK	35	138
[illegible]	21	21.5	2.56	15.8	2.5	14.6	38.2	320	20.1	OK	165	182	OK	32	120
1002	22	21.5	2.53	15.6	2.5	14.6	37.2	320	21.0	OK	165	172	OK	22	130
[illegible]	23	25.1	2.54	14.1	2.5	14.5	40.2	289	21.5	OK	165	154	OK	30	130
1004	25	20.9	2.61	15.8	2.5	14.2	37.2	332	20.2	OK	165	181	OK	18	134
1005	28	21.2	2.64	15.7	2.5	14.3	37.6	334	20.0	OK	165	182	OK	29	131
1006	29	21.4	2.56	15.2	2.5	14.7	37.6	327	20.3	OK	165	174	OK	30	132
1007	31	21.0	2.60	15.5	2.5	14.8	37.6	331	20.0	OK	165	180	OK	17	137
1008	32	22.7	2.57	15.2	2.5	14.6	37.2	325	20.7	OK	165	171	OK	22	136
1009	33	20.7	2.59	15.6	2.5	14.8	36.8	331	20.5	OK	165	176	OK	20	132
1010	34	21.6	2.62	16.0	2.5	14.8	37.9	326	20.2	OK	165	183	OK	20	132

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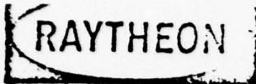

GROUP B INSPECTION
SCS-481 TYPE 1
X-BAND DIODES

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SUBGROUP 1 Shock, Vibration, Acceleration, Hermeticity

CONDITIONS:

Shock	Vibration	Acceleration	Hermeticity
per MIL-STD-750 Method 2016	per MIL-STD-750 Method 2056	per MIL-STD-750 Method 2006	per MIL-STD-750 Method 1071
500G	20 G	20000 G	Test Condition H
1 ms	50-2000-50 Hz	3 Planes	4 Hours @ 60 lb He Pressure
1/2 Sine Pulse	3 Planes	1 Min/Plane	
3 Planes	4 Cycles/Plane		He-Leak Detector <1 x 10-8
5 Shocks/Plane	4 Min/Cycle		

Reference attached Environmental Test Lab. Report dated 7/6/77.

The above reliability tests were performed at Raytheon SMDO by Quality Control Personnel.

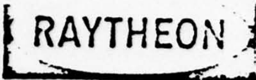
[signature]

CHARACTERISTIC		P_o		F_o		η		T_j	
UNITS		Watts		GHz		%		°C	
LIMITS Min.		3.5		9		20			
LIMITS Max.				11				200	
END POINT *		I	F	I	F	I	F	I	F
Serial No.	Diode I.D. Number								
330	41415B-N-1	3.5	3.5	9.7	9.7	24.2	24.2	185	185
331	41415B-N-2	3.5	3.5	9.4	9.6	23.4	24.4	165	158
332	41415B-N-3	3.5	3.5	9.5	9.5	24.0	24.8	152	147
333	41415B-N-9	3.5	3.5	9.7	9.7	23.0	23.5	190	186
334	41415B-N-10	3.5	3.5	9.7	9.7	23.8	23.8	174	174

Operator: [signature]
Date: 8/2/77

Q.C. Approved: [signature]
Date: 8/19/77

I - Initial; F- Final



GROUP B INSPECTION
SCS-481 TYPE 2
KU-BAND DIODES

SUBGROUP 1 Shock, Vibration, Acceleration, Hermeticity

CONDITIONS:

Shock	Vibration	Acceleration	Hermeticity
per MIL-STD-750 Method 2016	per MIL-STD-750 Method 2056	per MIL-STD-750 Method 2006	per MIL-STD-750 Method 1071
500G	20 G	20000 G	Test Condition H
1 ms	50-2000-50 Hz	3 Planes	4 Hours @ 60 lb He Pressure
1/2 Sine Pulse	3 Planes	1 Min/Plane	
3 Planes	4 Cycles/Plane		He-Leak Detector $<1 \times 10^{-8}$
5 Shocks/Plane	4 Min/Cycle		

Reference attached Environmental Test Lab. Report dated

The above reliability tests were performed at Raytheon SMDO by Quality Control Personnel.

David M. [signature]

CHARACTERISTIC		P_o		F_o		η		T_j	
UNITS		Watts		GHz		%		°C	
LIMITS	Min.	2.5		14		20		---	
	Max.	---		16		---		200	
END POINT *		I	F	I	F	I	F	I	F
Serial No.	Diode I.D. Number								
783	41436A-F-	2.5	2.5	14.1	14.2	20.7	20.9	172	170
784	41436A-F-	2.5	2.5	14.1	14.2	20.4	20.2	191	193
785	41436A-F-	2.5	2.5	14.1	14.2	20.8	20.8	192	192
786	41436A-F-	2.5	2.5	14.1	14.1	21.3	21.6	168	166

Operator: [signature]

Date:

Q.C. Approved: [signature]

Date: 9/30/77

I - Initial; F- Final

GROUP B INSPECTION
SCS-481 TYPE 1
X-BAND DIODES

SUBGROUP 2 Nuclear Radiation Exposure

CONDITIONS: Power Level - 10 KW

7 Min. Exposure

Gamma Exposure - 1.2×10^{5} rads (Si)

Neutron Exposure - $1.04 \times 10^{13} n/cm^{2}$, 1 MeV Si Damage Equivalent (indicated by sulphur pellet dosimetry).

NOTES:

1 - The exposed devices are radioactive (Av^{198}) and they are being stored in a controlled access and storage area with Raytheon's flash X-ray facility.

2 - Device S/N 574 was a control device; hence, it was not exposed to radiation.

CHARACTERISTIC		P_o		F_o		η		T_j	
UNITS		Watts		GHz		%		°C	
LIMITS	Min.	3.5		9		20			
	Max.			11				200	
END POINT *		I	F	I	F	I	F	I	F
Serial No.	Diode I.D. Number								
570	41413A-A-5	3.5	3.5	9.7	9.65	25.1	24.1	157	165
571	41413A-A-8	3.5	3.5	9.5	9.50	24.6	23.4	180	191
572	41413A-A-10	3.5	3.5	9.6	9.50	24.6	22.9	174	189
574	41413A-A-12	3.5	3.5	9.6	9.55	24.7	24.0	188	195

Operator:

Date:

Q.C. Approved:

Date: 9/26/77

I - Initial; F- Final

GROUP B INSPECTION
SCS-481 TYPE 2
KU-BAND DIODES

SUBGROUP 2 Nuclear Radiation Exposure

CONDITIONS: Power Level - 10 KW

7 Min. Exposure

Gamma Exposure - 1.2×10^5 rads (Si)

Neutron Exposure - 1.04×10^{13} n/cm^2, 1 MeV Si Damage Equivalent (indicated by sulphur pellet dosimetry).

NOTES:

1 - The exposed devices are radioactive (Av^{198}) and they are being stored in a controlled access and storage area with Raytheon's flash X-ray facility.

2 - Device S/N 641 was a control device; hence, it was not exposed to radiation.

CHARACTERISTIC		P_o		F_o		η		T_j	
UNITS		Watts		GHz		%		°C	
LIMITS	Min.	2.5		14		20		---	
	Max.	---		16		---		200	
END POINT *		I	F	I	F	I	F	I	F
Serial No.	Diode I.D. Number								
632	41435B-A-4	2.5	2.5	14.3	14.2	20.8	21.1	173	170
637	41435B-A-14	2.5	2.5	14.5	14.2	20.9	21.8	198	189
641	41435B-A-20	2.5	2.5	14.1	14.1	20.1	20.0	198	199
642	41435B-A-24	2.5	2.5	14.3	14.6	21.4	21.9	187	182

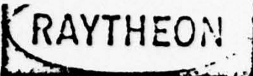
Operator: [illegible signature]

Date:

Q.C. Approved: [signature]

Date: 9/26/77

I - Initial; F- Final



GROUP B INSPECTION
SCS-481 TYPE 1
X-BAND DIODES

SUBGROUP 3 Storage Life

CONDITIONS:
- Nonoperating
- Ambient Temperature 200°C ±3°C
- Duration, 1015 Hours

The above reliability test was performed at Raytheon SMDO beginning on 5/13/77 and ended on 7/13/77.

Test monitored by: C. Mazza
Raytheon SMDO Q.C.

CHARACTERISTIC		P_o		F_o		η		T_j	
UNITS		Watts		GHz		%		°C	
LIMITS	Min.	3.5		9		20			
	Max.			11				200	
END POINT *		I	F	I	F	I	F	I	F
Serial No.	Diode I.D. Number								
131	41415B-A-3	3.5	3.5	9.6	9.7	23.7	23.5	175	176
132	41415B-A-4	3.5	3.5	9.3	9.4	20.2	20.3	182	181
133	41415B-A-6	3.5	3.5	9.8	9.9	24.1	24.9	177	171
136	41415B-A-9	3.5	3.5	9.4	9.5	20.7	21.4	181	174
'38	41415B-A-11	3.5	3.5	9.5	9.6	22.7	23.0	191	188
140	41415B-A-13	3.5	3.5	9.6	9.7	23.4	22.6	193	199
143	41415B-A-16	3.5	3.5	9.4	9.4	22.5	21.1	184	197
147	41415B-A-22	3.5	3.5	9.7	9.8	23.7	24.0	178	176
148	4141513A-23	3.5	3.5	9.6	9.7	23.0	22.7	183	186

I - Initial; F- Final

Operator: [signature]
Date: 7/15/77

Q.C. Approved: [signature]
Date: 8/19/77

GROUP B INSPECTION
SCS-481 TYPE 2
KU-BAND DIODES

SUBGROUP 3 Storage Life

CONDITIONS:
- Nonoperating
- Ambient Temperature 200°C ±3°C
- Duration, 1025 Hours

The above reliability test was performed at Raytheon SMDO beginning on 8/3/77 - 9/16/77.

Test Monitored by: C. Musa
Raytheon SMDO Q.C.

CHARACTERISTIC		P_o		F_o		η		T_j	
UNITS		Watts		GHz		%		°C	
LIMITS	Min.	2.5		14		20		---	
	Max.	---		16		---		200	
END POINT *		I	F	I	F	I	F	I	F
Serial No.	Diode I.D. Number								
644	41435B-A-28	2.5	2.5	14.0	14.2	21.6	22.0	167	164
645	41435B-A-29	2.5	2.5	14.4	14.5	20.8	21.7	196	187
646	41435B-A-31	2.5	2.5	14.1	14.1	20.3	20.7	199	195
647	41435B-A-33	2.5	2.5	14.1	14.2	20.9	21.3	196	192
648	41435B-A-35	2.5	2.5	14.1	14.2	20.3	20.1	187	189
649	41435B-A-36	2.5	2.5	14.1	14.2	20.8	20.7	178	178
650	41435B-A-37	2.5	2.5	14.1	14.1	20.6	20.5	189	190
651	41435B-A-38	2.5	2.5	14.1	14.2	20.7	21.1	189	185
652	41435B-A-41	2.5	2.5	14.0	14.2	20.0	20.0	198	198

Operator: [illegible]

Date: [illegible]

Q.C. Approved: [illegible signature]

Date: 9/26/77

* I - Initial; F- Final

RAYTHEON

GROUP B INSPECTION
SCS-481 TYPE 1
X-BAND DIODES

SUBGROUP 4 Operating Life

CONDITIONS:

Oscillator Frequency:	10.0 GHz ±1.0 GHz
Oscillator Output Power:	3.5 W-CW, Min.
Oscillator Efficiency (RF-DC):	20% Min.
Junction Temperature:	200°C Max.
Ambient Temperature:	25 ±3°C
Duration:	1015 Hours

The above reliability test was performed at Raytheon SMDO beginning on 5/31/77 and ended on 7/13/77.

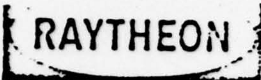
Test monitored by: C. Mazza
Raytheon SMDO Q.C.

CHARACTERISTIC		P_o		F_o		η		T_j	
UNITS		Watts		GHz		%		°C	
LIMITS	Min.	3.5		9		20			
	Max.			11				200	
END POINT *		I	F	I	F	I	F	I	F
Serial No.	Diode I.D. Number								
134	41415B-A-7	3.5	3.5	9.6	9.6	23.3	23.3	180	180
135	41415B-A-8	3.5	3.5	9.6	9.7	25.2	25.2	180	180
137	41415B-A-10	3.5	3.5	9.5	9.5	25.2	24.8	140	143
139	41415B-A-12	3.5	3.5	9.5	9.5	24.3	24.2	148	149
141	41415B-A-14	3.5	3.5	9.7	9.7	24.3	24.4	152	152
142	41415B-A-15	3.5	3.5	9.6	9.7	25.1	24.8	172	175
144	41415B-A-17	3.5	3.5	9.6	9.6	23.2	23.4	145	144
145	41415B-A-18	3.5	3.5	9.7	9.7	25.6	25.1	164	168
146	41415B-A-19	3.5	3.5	9.3	9.3	20.7	20.8	183	182

* I - Initial; F- Final

Operator: [signature]
Date: 7/15/77

Q.C. Approved: Paul [signature]
Date: 8/19/77



GROUP B INSPECTION
SCS-481 TYPE 2
KU-BAND DIODES

SUBGROUP 4 Operating Life

CONDITIONS:

Oscillator Frequency:	14.0 GHz ±1.0 GHz
Oscillator Output Power:	2.5W-CW, Min.
Oscillator Efficiency (RF-DC):	20% Min.
Junction Temperature:	200°C Max.
Ambient Temperature:	25 ±3°C
Duration:	1025 Hours

The above reliability test was performed at Raytheon SMDO beginning on 8/3/77 and ended on 9/16/77.

Test monitored by: C. Mazza
Raytheon SMDO Q.C.

CHARACTERISTIC		P_o		F_o		η		T_j	
UNITS		Watts		GHz		%		°C	
LIMITS	Min.	2.5		14		20		---	
	Max.	---		16		---		200	
END POINT *		I	F	I	F	I	F	I	F
Serial No.	Diode I.D. Number								
631	41435B-A-3	2.5	2.5	14.2	14.2	21.7	21.9	181	179
633	41435B-A-5	2.5	2.5	14.2	14.1	21.0	20.9	191	192
634	41435B-A-9	2.5	2.5	14.2	14.2	22.0	21.9	182	183
635	41435B-A-12	2.5	2.5	14.2	14.2	21.0	21.3	192	189
636	41435B-A-13	2.5	2.5	14.4	14.3	21.5	22.2	189	183
638	41435B-A-15	2.5	2.5	14.2	14.1	21.1	20.9	184	186
639	41435B-A-16	2.5	2.5	14.1	14.1	21.1	21.1	190	190
640	41435B-A-19	2.5	2.5	14.2	14.2	20.5	21.0	194	189
643	41435B-A-25	2.5	2.5	14.1	14.1	21.5	21.4	185	186

* I - Initial; F- Final

Operator: [illegible]

Date: [illegible]

Q.C. Approved: [illegible]

Date: 9/26/77