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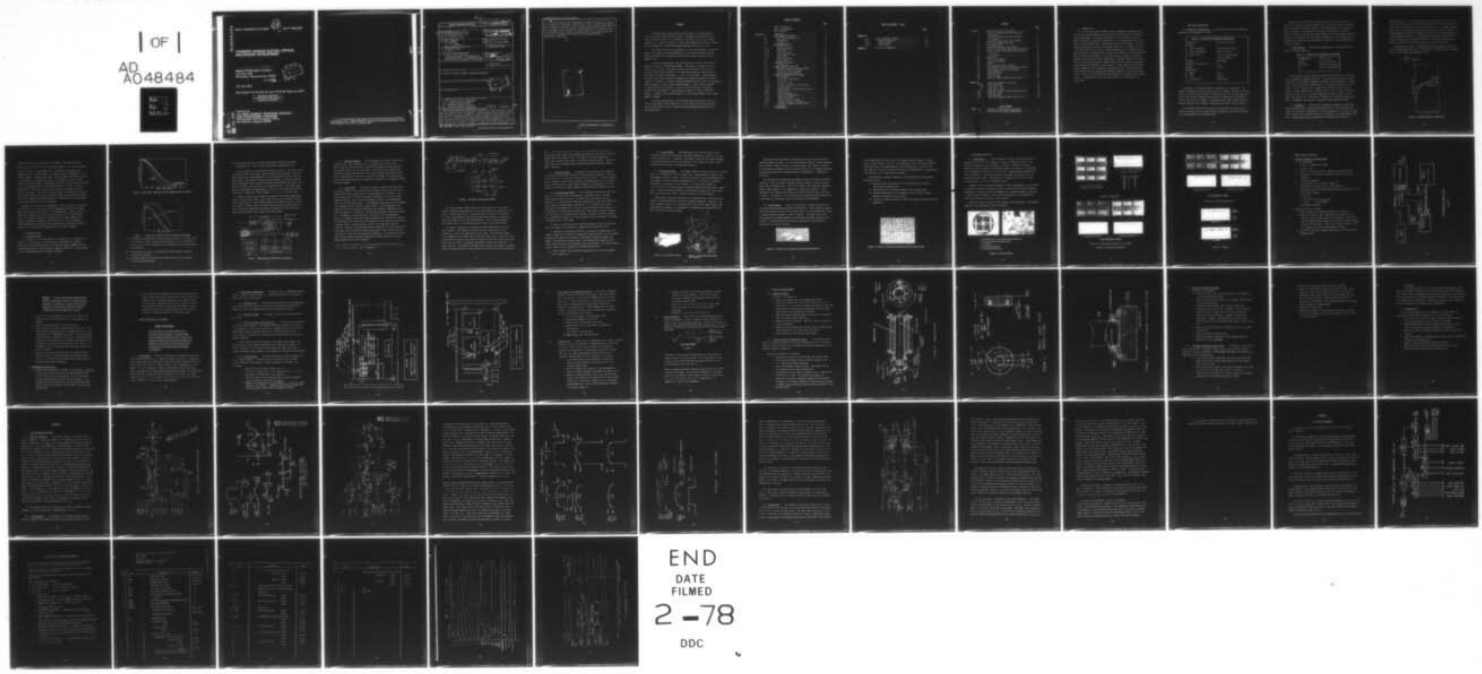

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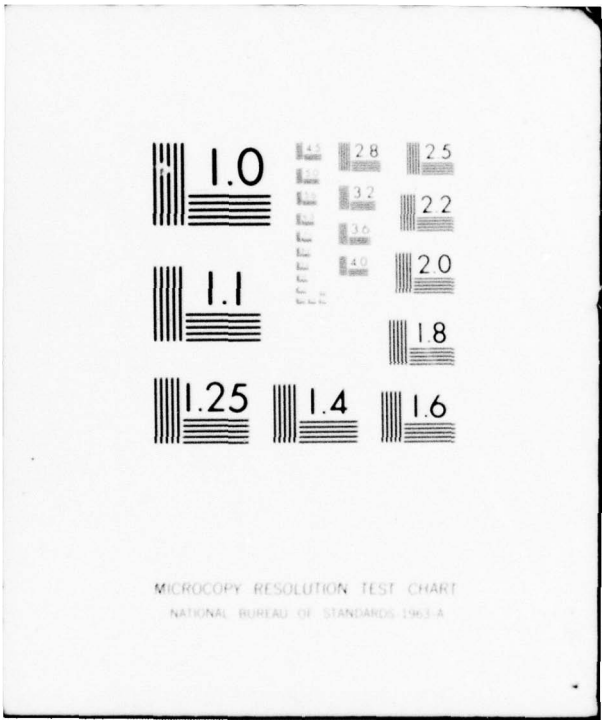
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Report DAAG53-76-C-0184 CR 77-588-009

COMMON MODULE ELECTRO OPTICAL MULTIPLEXER DEVELOPMENT

RAC Govt + Comm Systems, Burl, MA
~~RCA~~/AUTOMATED SYSTEMS Div
P.O. Box 588
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25 July 1977

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E/O MUX (ELECTRO OPTICAL MULTIPLEXER)
FLIR (FORWARD LOOKING INFRARED)
MTF (MODULATION TRANSFER FUNCTION)
MRT (MINIMUM RESOLVABLE TEMPERATURE)

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The output imagery of parallel scan, modular FLIR systems is commonly viewed through an ocular or biocular eyepiece. For system applications requiring serial video for remote imagery or automatic tracking, parallel to serial multiplexing is required. A militarized (1") silicon television camera compatible with projected modular systems has been developed with extensive use of hybrid circuitry. The camera weight and volume are reduced to 2.0 Kg and 1600 cm^3 and the total required input power is less than 8 watts to minimize the internal temperature →

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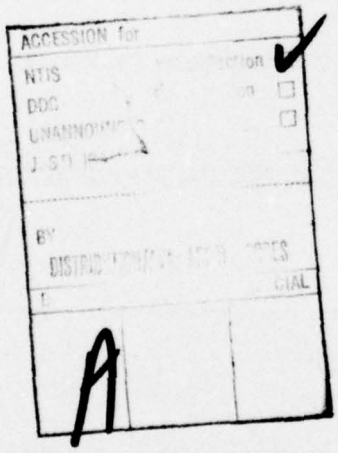
20. .... rise and power source requirements. Automatic black level and gain control circuitry are provided, thereby insuring that the darkest and lightest scene elements are displayed at full contrast. Camera outputs are EIA Standard RS-343-A composite video, unregulated non-composite video and vertical sync. The unregulated video is suitable for external generation of IR level and gain control signals and the vertical sync pulse useful for camera/IR scanner synchronization. Performance and test data are discussed and design features are highlighted.



PREFACE

The Common Module Electro-Optical Multiplexer is an advanced design one inch silicon vidicon television camera. The camera makes extensive use of thick film hybrid circuitry for compactness, reliability, and low cost volume producibility. Careful attention to circuit design emphasizing low power consumption has resulted in a single piece camera dissipating less than 8 watts.

This report covering the developments of the E/O Multiplexer has been prepared in fulfillment of the requirements for a final report covering the work authorized under Contract DAAG53-76-C-0184 during the period from June 1976 to Fegruary 1977.

The work was administered under the direction of the U.S. Army Mobility Equipment Research and Development Command - Procurement and Production Office, Fort Belvoir, Virginia. The program monitor was Dr. Ronald D. Graft of the U.S. Army Night Vision Laboratory. Dr. Graft made substantial contributions to the material presented in sections 1, 2, and 3 of this report. Acknowledgements are made to the following RCA-AS management and technical personnel that participated in the design, J. Aronson, Project Management Office; W. Hannan, Engineering Section Manager; J. Klein, Project Design Manager; L. Arlan, Project Engineer, R. Spiecker, Electrical Design; P. Arntsen, Electrical Design; S. Waldstein, Mechanical Design Manager; R. DeMeo, Mechanical Design; R. Rooney, Mechanical Design; J. Bouchard, Hybrid Design Manager; B. Joyce, Hybrid Design; and J. Nazak, Marketing Manager.

The major subcontractors on this program were Wilmore Electronics, Inc. for the power supply, Solar Systems Inc. for the deflection yoke, RCA Lancaster for the bonded target vidicon, and RCA, Solid State Technology Center for the LSI synchronizer.

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1. INTRODUCTION

This is the Final Technical Report which is submitted in response to Data Item A001 for Contract DAAG53-76-C-0184 covering the development of an Electro Optical Multiplexer. The camera-multiplexer is a one inch silicon vidicon television camera of single unit construction. It is designed to serve a dual function when integrated with a direct-view infrared imaging system: (a) provides remote imagery at one or more selected sites, and (b) serves as a source of standard serial video for use in tracking applications. By extensive use of hybrid circuitry, the camera weight and volume are reduced to 2.0 Kg and 1600 cm^3. The total required input power is less than 8 watts to minimize the internal temperature rise and power source requirements. Automatic black level and gain control circuitry are provided, thereby insuring that the darkest and lightest scene elements are displayed at full contrast. Camera outputs are EIA Standard RS-343-A composite video, unregulated non-composite video, and vertical sync. The unregulated video is suitable for external generation of IR level and gain control signals and the vertical sync pulse useful for camera/IR scanner synchronization. Performance and test data are discussed and design features are highlighted.

2. MULTIPLEXER REQUIREMENTS

2.1 Electrical and Mechanical. The principal electrical and mechanical requirements are summarized in Table I.

TABLE I. ELECTRICAL AND MECHANICAL REQUIREMENTS

Prime Power	20 ± 0.1 VDC, 8 watts
Outputs	
Video (regulated)	RS-343-A; AGC and ABLC
Video (unregulated)	RS-343-A, 2 mv/na
Vertical sync	+4 ± 1V, active interval;
	OV, sync interval
Shading	25% maximum
Geometrical distortion	±2%
Gamma	1 ± 0.1
Mechanical	
Weight	2 Kg
Size	1600 cm^3
Configuration	Single piece

Minimization of dissipated power is considered a key requirement. The internal temperature differential above ambient, assuming a minimal heat sinking through the front mounting flange, is estimated to be 0.5°C per dissipated watt. Vidicon dark current increases exponentially with temperature, approximately doubling for each 10°C increment. As discussed later, dark current limits the maximum available signal current by determining the onset of tube saturation.

EIA Standard RS-343-A video format (875 lines/frame, 60 fields/second, 2:1 interlace) was selected to minimize aliasing between the FLIR raster structure an the multiplexer vertical sampling rate.

Automatic gain control (AGC) and automatic black level control (ABLC) are required to eliminate a variable pedestal due to vidicon dark current variations and to insure 100% displayed contrast for the maximum temperature differential within the scene. The unregulated video output is required as a potential source of automatic level and gain control signals for the FLIR system; external vertical sync is required for IR scanner synchronization. The single piece configuration was selected to minimize EMI and to reduce the cabling required for gimballed systems.

2.2 Environmental. The multiplexer operational environmental requirements are listed in Table II.

TABLE II. OPERATIONAL ENVIRONMENTAL REQUIREMENTS

Temperature	$-54^{\circ}C$ to $+71^{\circ}C$
Shock	20g, 11 milliseconds
Vibration	Curves M and B, Figure 514, 2-3, MIL-STD-810C

Raster stability, image tube dark current, and microphonics are the critical environmentally dependent parameters. Raster positional stability must be maintained over the required temperature extremes if system boresight is dependent upon an electronically generated reticle. The required stability is $\pm 0.2\%$ (± 2 scan lines). Assuming 700 na maximum target current and 480 na signal current, the dark current must not exceed 220 na at $+71^{\circ}C$. Since dark current doubles for each $10^{\circ}C$ rise in target temperature, the dark current at $+30^{\circ}C$ should not exceed 14 na. Elimination or reduction of microphonics requires the use of a hardened vidicon gun and a ruggedized target support structure.

2.3 Performance. The principal performance parameters are broad area signal-to-noise ratio and modulation transfer function. Typical modular FLIR systems have an $NE\Delta T$ of approximately $0.3^{\circ}C$ when measured at full electronic bandwidth. Dynamic range limitations restrict the maximum ΔT to approximately $20^{\circ}C$, the resultant maximum signal-to-noise ratio in the electronic channel is

approximately 60:1. A channel-to-channel non-uniformity of ±5% and the LED visible line structure act as additional sources of fixed pattern noise. Thus a multiplexer signal-to-noise ratio of approximately 40:1 is assumed adequate, particularly for temperature differentials less than 5 to 10°C. The multiplexer preamplifier noise is estimated to be 12 na for 12-14 MHz bandwidth and 8 dB of aperture correction. The required signal current is then 480 na to achieve the desired 40:1 signal-to-noise ratio. The effect of multiplexer signal-to-noise ratio upon system performance is shown in Figure 1.

At maximum power output, a 180 element LED array generates an effective, continuous power density of 4×10^{-4} watts/cm^2 in the emitter plane. The power density at the camera tube faceplate is then

$$P = \frac{4 \times 10^{-4} T_o}{4f^2} \text{ , watts/cm}^2$$

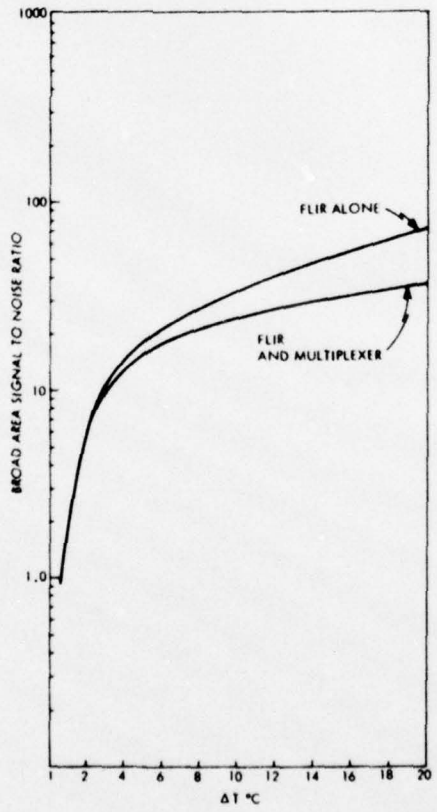


FIGURE 1. BROAD AREA SIGNAL TO NOISE RATIO

where T_o and f are the transmission and f number of the coupling optics. Assuming $T_o = 0.7$ and f/2.2, the total power incident on a 1" vidicon format is 17.4×10^{-6} watts. At this power level, an antimony trisulphide vidicon generates 230 na of signal current at a target voltage corresponding to 20 na of dark current. Increasing the target voltage provides additional sensitivity at the expense of increased dark current. For example, at 100 na of dark current, the signal current is approximately 450 na. At this dark current level, an antimony trisulphide vidicon approaches saturation at $+40^{o}C$. Silicon is approximately 6 times more sensitive than antimony trisulphide at the LED emission wavelength. Thus sufficient signal current is available from silicon to provide the required 40:1 signal-to-noise ratio over the specified temperature range. Antimony trisulphide, despite an attractive MTF, is not suitable due to sensitivity/dark current limitations.

The MTF of a typical modular FLIR system is shown in Figure 2. Also shown is the MTF of a 1" silicon vidicon without aperture correction; the coupled MTF shows a significant degradation in FLIR performance. Figure 3 shows the improvement obtained with 8 dB aperture correction at 500 TV lines/raster height. The coupled performance is enhanced at the lower frequencies and slightly degraded at frequencies above 350 TV lines. The 8 dB aperture correction approximately doubles the preamplifier noise and limits an MRT improvement to a narrow band of frequencies near the boost frequency.

3. MULTIPLEXER DESIGN

3.1 Electrical Design

Power dissipation of the Multiplexer is considered to be an important requirement. Minimal power dissipation enables dense packaging, reduces or eliminates the need for heat sinking, and prevents internal temperatures from far exceeding ambient, thereby improving component reliability. Power dissipation is minimized through the following techniques:

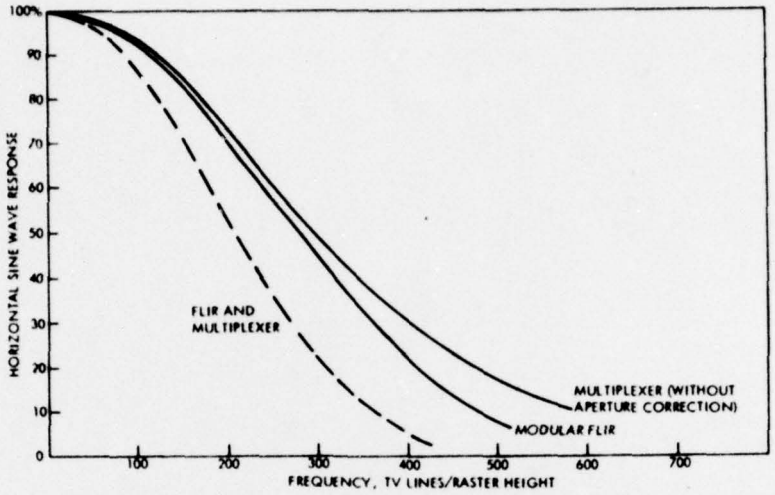


FIGURE 2. COUPLED MTF, MODULAR FLIR AND UNCORRECTED MULTIPLEXER

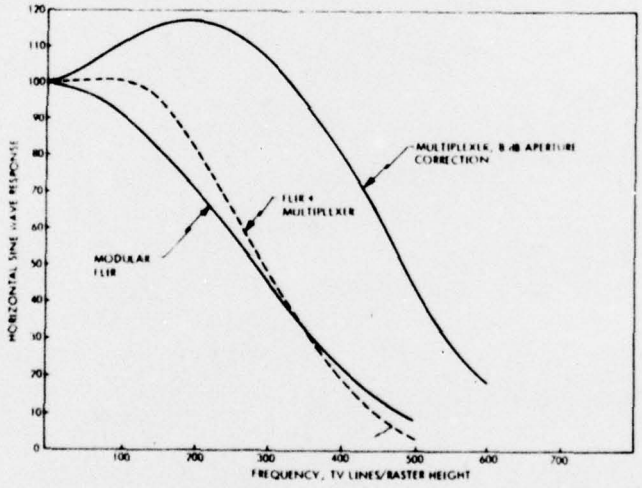


FIGURE 3. COUPLED MTF, MODULAR FLIR AND CORRECTED MULTIPLEXER

(1) The deflection assembly uses a large focus coil producing a 42 gauss field with 59 mA at 18 volts. The horizontal deflection coil is designed with high Q to provide good linearity; only 220 mA pk-pk current is required for full deflection.

(2) Discrete parts are used in video amplifiers when available integrated circuits are inefficient.

(3) Micropower operational amplifiers and CMOS devices are used throughout the design where applicable.

(4) A high efficiency dc-dc converter power supply, designed by Wilmore Electronics, Inc., has an overall efficiency of approximately 75%.

A block diagram of the Multiplexer is shown in Figure 4. The unit consists of 4 printed circuit boards and a sensor tube/deflection assembly. The video board contains the video preamplifier, the video processor, and the video control hybrids. The deflection board contains horizontal, and vertical hybrids. The focus/beam/sync board contains the dynamic focus/cathode blank hybrid, the focus/sync hybrid, and the 875 scan line synchronizer LSI. Each board, apart from the power supply is approximately 2.5" by 4.5". The hybrid microcircuits are packed in hermetically sealed standard 1.3" x 1.3" x 0.25" containers.

Principal circuit design features are automatic black level compensation (ABLC), automatic gain control, black clamp, white clip, and dynamic focusing. The combined effects of AGC and ABLC provide fully automatic contrast control. The automatic contrast control circuitry senses the peak to peak amplitude of the video signal, regardless of contrast, and corrects the gain and signal black level to provide a full dynamic range video signal.

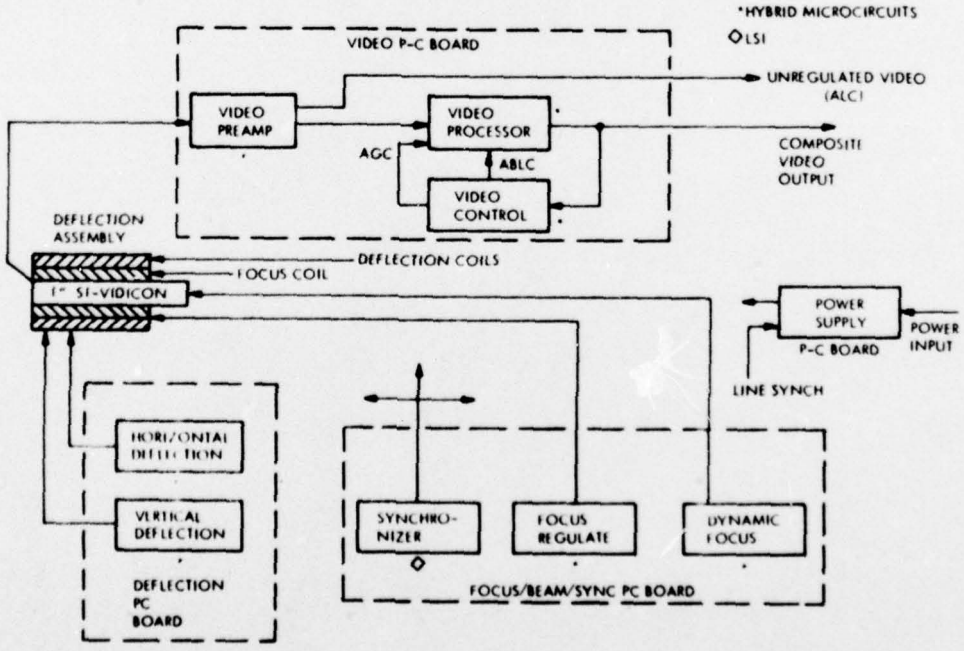


FIGURE 4. COMMON MODULE SIMPLIFIED BLOCK DIAGRAM

3.1.1 Tube/Yoke Assembly. The Multiplexer uses an RCA C23174B silicon target vidicon. The C23174B vidicon is a bonded target version of the RCA C23174A with high sensitivity, board spectral response, high resolution, low residual signal, and low dark current. The bonded target decreases the vibration and shock susceptibility of the sensor, thereby improving the microphonic characteristics. The yoke is similar to the YLFA-959 (Cleveland Electronics) with modifications for low power and incorporation of permanent magnets for beam alignment.

3.1.2 Video Board.* A detailed functional diagram of the video board is shown in Figure 5. The target signal is coupled to the input of the video preamplifier and the output signal is video processed and controlled. The video preamplifier is a hybrid microcircuit consisting of a low noise transimpedance amplifier with a 50,000 ohm feedback resistor, two wideband amplifiers, and a video output buffer. A transimpedance amplifier is used to present a low impedance load to the video signal current. The low impedance input eliminates the need for peaking compensation and minimizes undesirable noise pickup and parasitic oscillations. The measured equivalent input noise current is 7.5 nanoamperes (15 MHz bandwidth). The output of the transimpedance amplifier is coupled through two cascaded wideband video amplifiers to produce an unregulated video output useful for generation of an external control signal. A separate output is coupled through a buffer to the aperture correction circuitry. The delay line aperture corrector compensates for vidicon spot size by increasing the definition of abrupt transitions in video tone through the introduction of controlled overshoots and undershoots. Its function is to provide a rising frequency response characteristic while maintaining a linear phase response over the full bandwidth.

* A more detailed discussion of the aperture correction, video processor, and video control circuits is given in Appendix A.

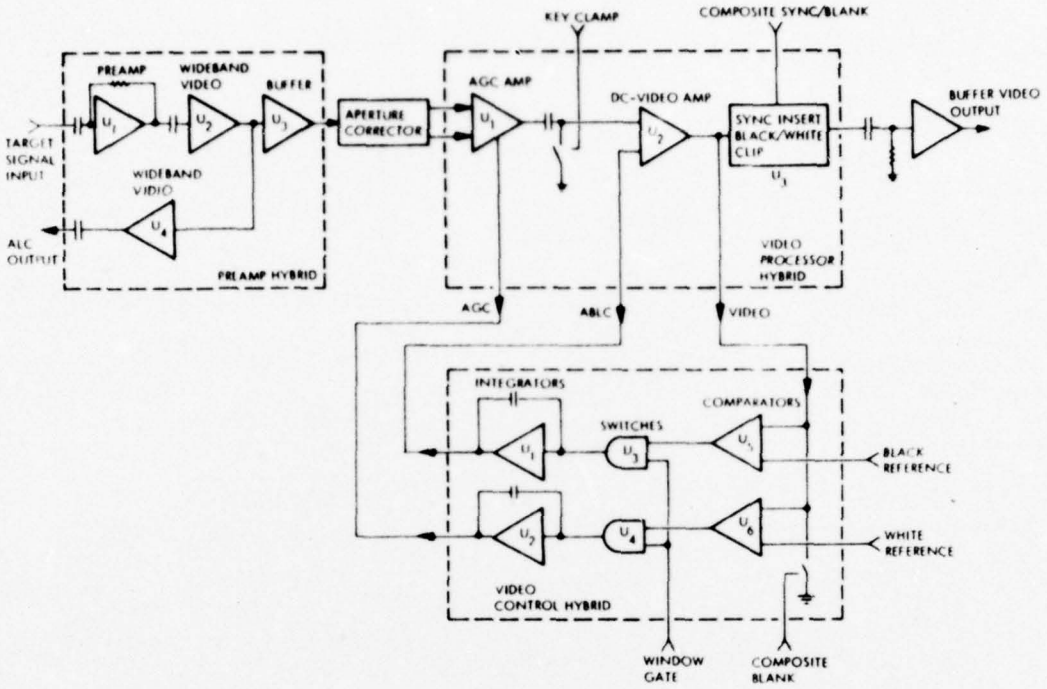


FIGURE 5. FUNCTIONAL DIAGRAM VIDEO BOARD

The video processor hybrid consists of an AGC amplifier, a key clamp, a wideband dc coupled video amplifier, a sync-blank insert and a black/white clip circuit. The AGC amplifier, in conjunction with the clamp and the wideband dc coupled video amplifier, maintains the peak white signal at a constant dc level with respect to the black level reference. The dc level difference is held constant over a 30 dB signal range and a 10% to 100% contrast range.

The video is compared to black and white level references on the video control hybrid. The comparators produce high error outputs for millivolt differences in either the peak white or black level. The individual outputs of the comparators are "Anded" with a window gate (WG) signal, allowing only the center 80% of the raster video signal to control the black and white level loops. This allows the video to be sampled independent of raster edge transients or blanking levels. The outputs of the AND circuits control the inputs to individual integrators which provide dc control signals for the AGC and the ABLC amplifiers.

The sync and blanking levels are added to the video as shown. This circuit also prevents video spikes from extending below the blank level and clips white spikes higher than a preset level. The output of the video processor is capacitively coupled to the input of a unity gain buffer amplifier. The video signal output and the camera output circuit are designed to meet all requirements of RS-343-A.

3.1.3 Deflection Board. The deflection board contains the circuitry for horizontal and vertical deflection and sweep failure protection. The horizontal hybrid is a high efficiency resonant flyback circuit. A stable reference voltage regulator maintains size stability with temperature; full scan output is obtained with a total circuit power dissipation of approximately 0.5 watts. The vertical hybrid is a stable feedback controlled linear deflection circuit.

3.1.4 Focus/Beam/Sync Board.* The focus/beam/sync board has four microcircuits; an 875 scan line sync generator, a focus/sync hybrid, a dynamic focus/cathode blank hybrid, and a 1.155 MHz crystal oscillator. The sync generator is a custom monolithic CMOS LSI manufactured by RCA, Solid State Division, meeting all requirements of EIA RS-343. It is driven by the crystal oscillator and generates all of the timing signals required by the camera. It is packaged in a standard 24 pin ceramic DIP. The crystal oscillator consists of a high stability 4.620 MHz crystal (AT cut), 2 bipolar oscillator circuits, and a divide by 4X counter. The circuit requires only 20 mA current; the output is compatible with +11 VDC CMOS.

The focus is maintained over the required temperature range by regulating the focus current within $\pm$0.250% by a series-current feedback circuit.

To optimize the Multiplexer resolution, including the extreme edges and corners, dynamic focus correction is applied to focus electrode G_3 of the vidicon. Horizontal and vertical rate parabolic waveforms are generated, summed, and added to the quiescent dc focus voltage. The improved beam landing provides better corner resolution and minimizes signal non-uniformity. The cathode blanking main driver is also included in the dynamic focus hybrid.

* A detailed discussion and preliminary specification for the sync generator is given in Appendix B.

3.1.5 Power Supply. The power supply is a high efficiency (75%) dc-dc horizontal line synchronized converter packaged on a single 4 x 5.5 inch printed circuit board. A separate transformer is used for the higher voltages to minimize size and weight of the magnetics. All outputs are short circuit protected and the input is overvoltage protected.

3.2 Mechanical Design. The camera weighs 4.25 pounds, and is 3.54 inches high, 4.33 inches wide, and 6.30 inches long. The photograph of Figure 6 and the assembly drawing of Figure 7 indicate the overall size and configuration of the camera. A mounting flange, approximately 4.4 x 5.2 inches, is provided for mounting the camera to a flat surface. The front plate contains a 2 1/2" x 2 1/2" lens "C" mount mounting plate centered about the optical centerline. Protection and EMI shielding is provided by an upper three sided cover and a rear flat cover; Figure 7 shows the camera with covers removed.

Input/output connectors are mounted on a recessed step at the rear of the camera to prevent protrusion outside the required dimensions. Removal of the covers provides access to the three printed circuit boards, power supply, and tube deflection assembly; all assemblies and components are supported by the main structure and mounting flange.

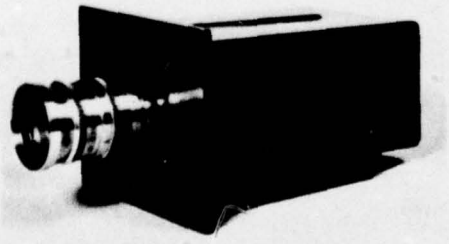


FIGURE 6. MULTIPLEXER CAMERA

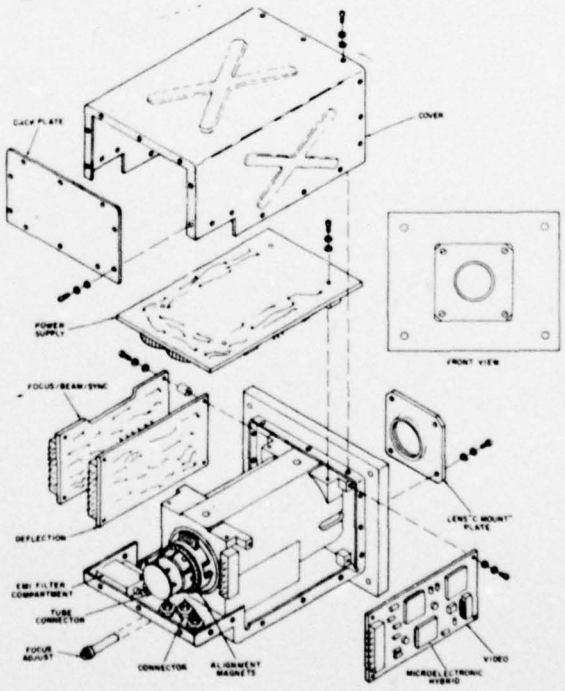


FIGURE 7. MULTIPLEXER EXPLODED VIEW ASSEMBLY

Mechanical focus adjustment is achieved by sliding the front and rear internal support structure. It is driven externally through a focus adjustment drive screw and locked in place by a synchro clamp. The vidicon is mounted to the deflection assembly and can be rotated $\pm 90^{\circ}$ within the support structure. The mounting maintains the faceplate position independent of temperature variations.

All printed wiring boards are conformally coated for fungus and moisture protection. The main camera structure, mounting flange and outer cover are fabricated of aluminum alloy. Use of the internal center structure assures a simple, rugged support to all components for shock and vibration. Board adjustments are located on the edge of the boards facing the sides for ease of access. A connector on the rear edge of each board facilitates removal and a tube socket is provided for ease of maintenance and replacement.

3.3 Hybrid Design. Many of the electronic circuits have been constructed using custom-designed hybrid microcircuits. Seven different types of thick film hybrids are used in the camera system. All are hermetically sealed in rugged platform packages as shown in Figure 8. All seven hybrids are manufactured to the same sequence of well-documented process operations and controls. The hybrids meet the screening requirements of MIL-STD-883 A, Method 5004, for Class B devices.

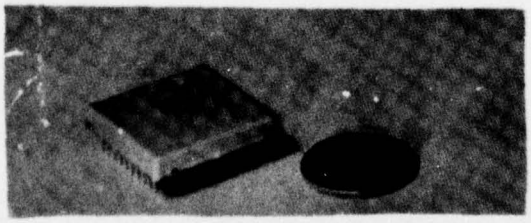


FIGURE 8. DYNAMIC FOCUS/CATHODE BLANK HYBRID MICROCIRCUIT

Three representative hybrids used in the camera system are shown in Figure 9 prior to cover sealing. The 1 x 1 inch substrates, with thick film resistors and metalization, are solder-mounted to the platform base. Visible in the photograph are the active and passive devices, the assembled and interconnected chip capacitors, IC's, transistors and diodes.

Some processing highlights relative to the manufacture of these hybrid microcircuits are:

(1) Eutectic solder chip mounting of all transistors and diodes to gold-plated molybdenum tabs.

(2) Solder mounting of chip-tab assemblies and chip capacitors.

(3) Approved epoxy mounting of integrated circuit chips (no current passage in backside of silicon chip).

(4) Ultrasonic gold-ball bonding of wires with automatic wire bonding for production.

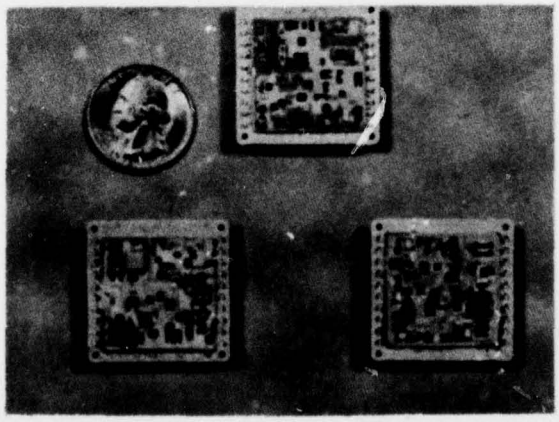


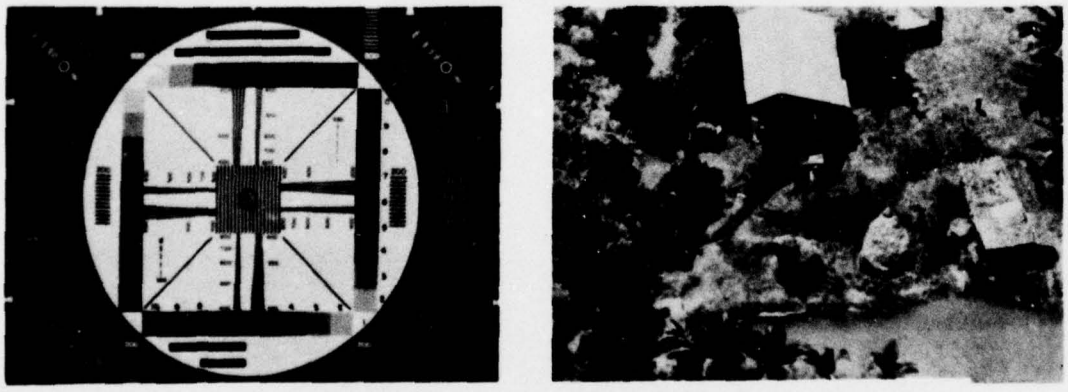
FIGURE 9. THREE (3) TYPICAL MULTIPLEXER HYBRIDS BEFORE SEALING

4. PERFORMANCE TEST DATA

4.1 Image Quality. The photographs of Figure 10 were taken from the faceplate of an 875 TV line display, the slight distortions visible in the picture were caused by the photographic technique. There are no visible blemishes or Moire patterns; the measured preamplifier noise is 14 nanoamperes with 6 dB aperture correction at 590 TV lines. The Multiplexer resolution is shown in Figure 11. The center resolution measurements were taken from the oscilloscope photo shown. The resolution is greater than 600 TV lines per picture height in 7 of the 9 resolution bursts.

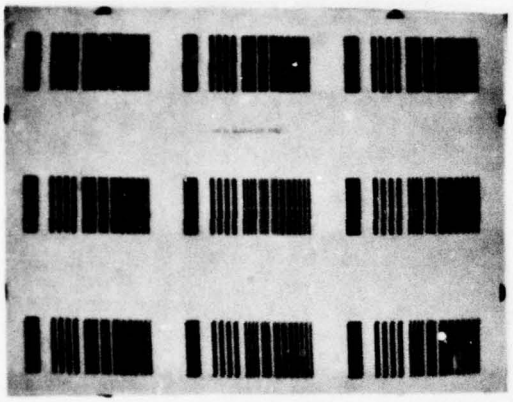
Figures 12 and 13 illustrate Automatic Contrast Enhancement; in each figure the results of viewing low contrast scenes is shown with and without contrast enhancement. The video without enhancement has a sizeable pedestal containing no useful video information. With contrast enhancement, the displayed contrasts are equal for 30% and 60% scene contrasts.

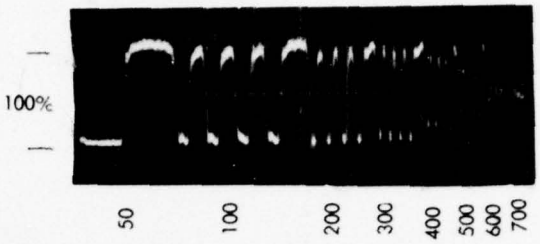
Figure 14 shows the vertical and horizontal video uniformity. The measured shading is less than plus or minus ten percent.



- PREAMPLIFIER NOISE 14 NANOAMPERES (WITH CORRECTION)
- NO VISIBLE BLEMISHES OR MOIRE PATTERNS
- 1% LINEARITY
- CONTRAST ENHANCEMENT
- 20% RESPONSE @ 600 TVL/RH

FIGURE 10. PICTURE QUALITY

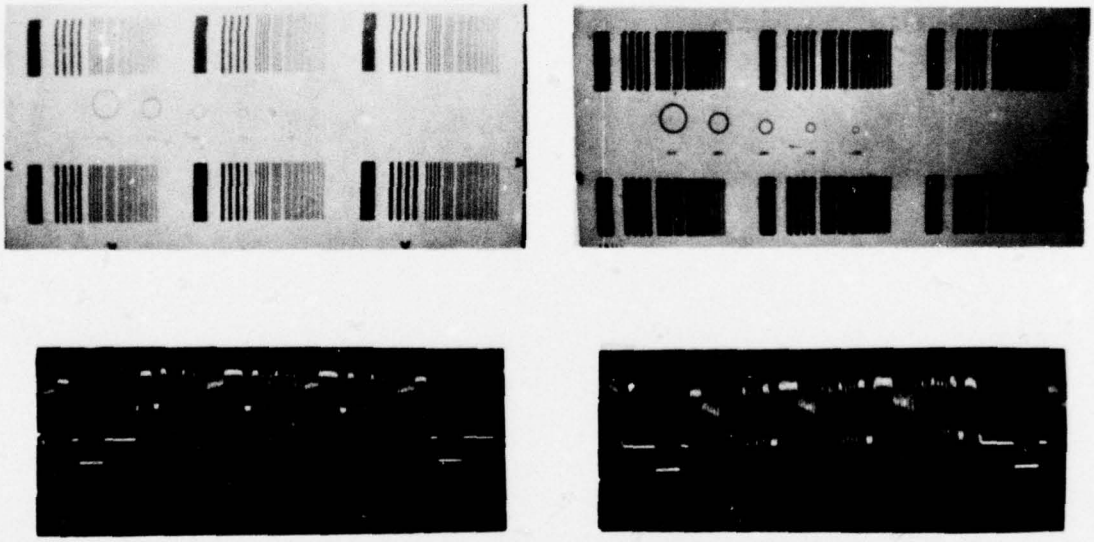




- 500 TVL/PH IN ALL 9 SEGMENTS
- 600 TVL/PH IN 7 OF 9 SEGMENTS

TVL/PH	% RESPONSE
50	100
100	100
200	100
300	100
400	80
500	55
600	22

FIGURE 11. RESOLUTION



WITHOUT ENHANCEMENT

ENHANCED TO FULL 100%

60% CONTRAST SCENE

EQUIVALENT TO DARK CURRENT DEGREDATION AT +71°C AMBIENT

FIGURE 12. CONTRAST ENHANCEMENT

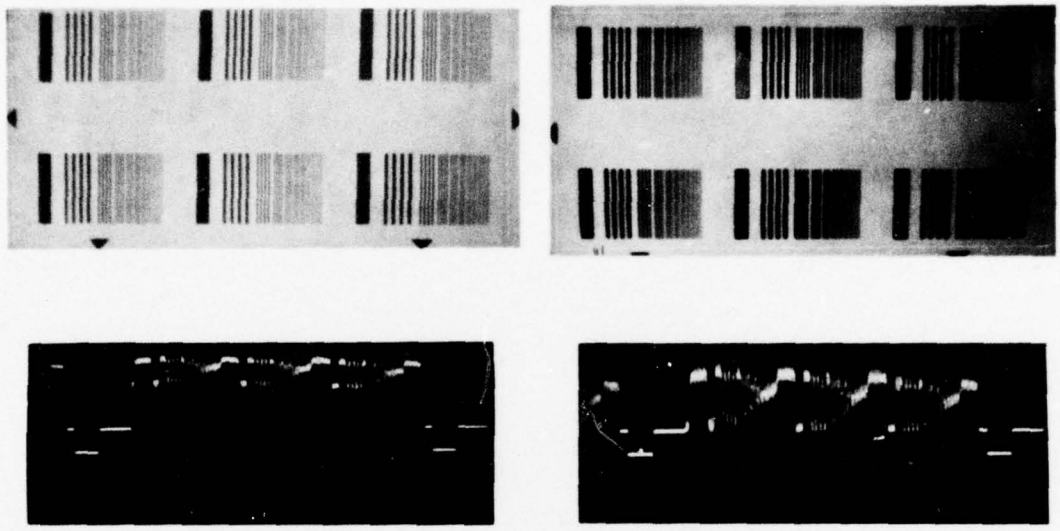


FIGURE 13. CONTRAST ENHANCEMENT

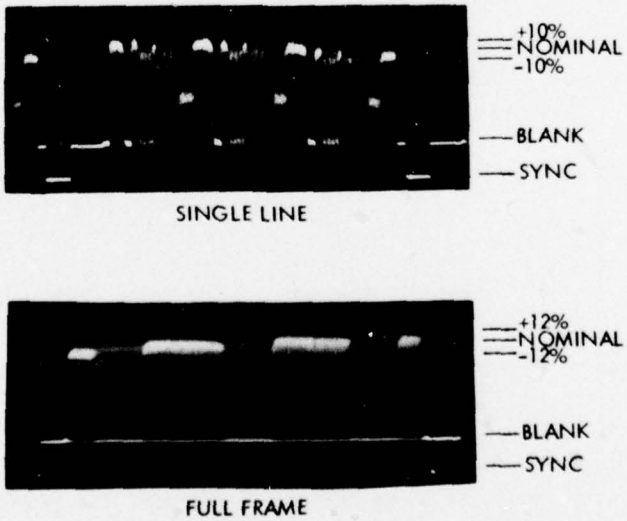


FIGURE 14. SHADING

5. CAMERA OPERATION PROCEDURE

5.1 Equipment Required to Operate Camera.

- o E/O Multiplexer
- o +20 VDC, 0.5 ampere power supply
- o "C-Mount" lens
- o 875/60, 2:1 interlace monitor, composite sync per EIA-RS-343
- o Video cable, 75 ohm coaxial (RG/159U or equivalent) with BNC connectors
- o 75 ohm BNC termination
- o Vertical sync cable, coaxial BNC (optional)
- o Unregulated video cable, coaxial - BNC (optional)
- o Camera power cable, twisted shielded pair with a JT06RE-8-98S1 (014) plug wired as follows:

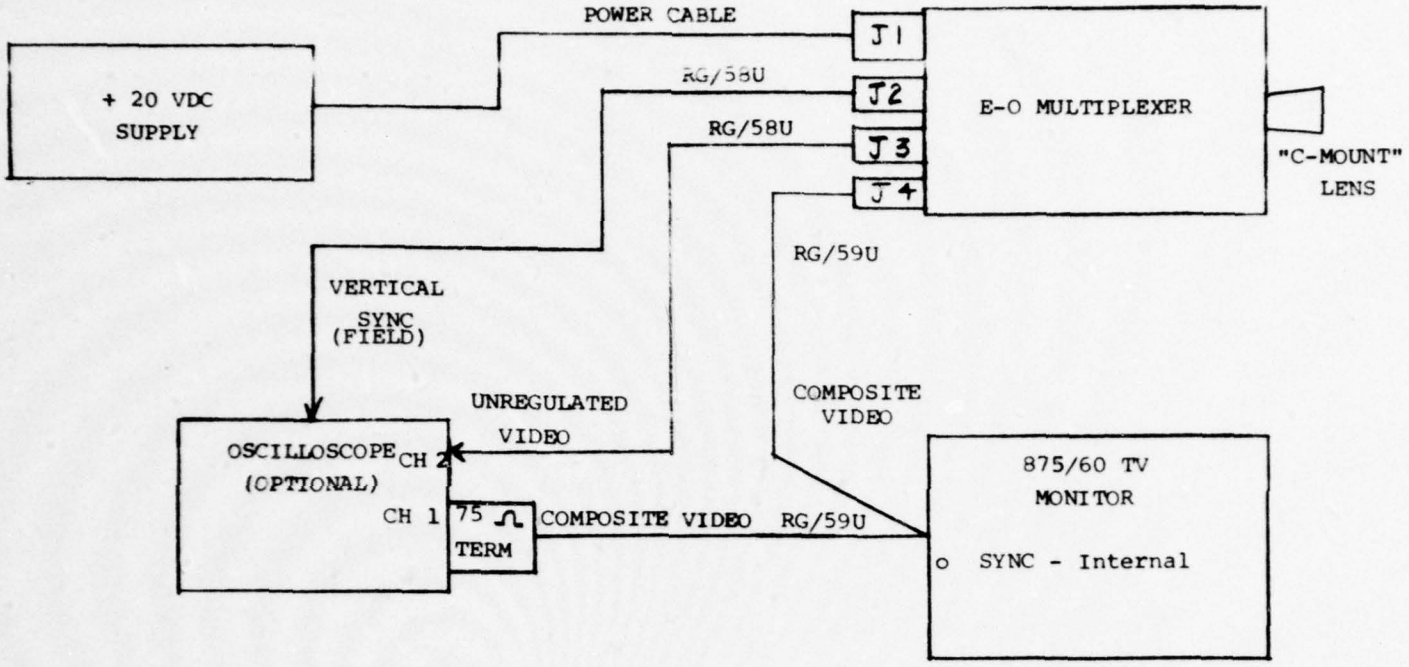
  A - +20 VDC

  B - +20 VDC return } Tied together
  C - Shield } at supply

- o Oscilloscope (Optional)

5.2 Set Up and Turn On Procedure

1. Mount the camera in a suitable fixture or on a tripod.
2. Install the "C-Mount" lens. Make sure that the lens will not touch the vidicon faceplate when fully installed. Turning the camera focussing screw clockwise will retract the vidicon assembly away from the lens mount. (The focusing screw is between J1 and J2. Release the set-lock before adjusting focus).
3. Interconnect the above equipments per Figure 15, E/O Multiplexer Operation Setup.



E/O MULTIPLEXER OPERATION SETUP

FIGURE 15

CAUTION!! Care must be exercised connecting the +20 VDC to the camera; there is no reverse polarity protection. In addition, J1-B and C must be tied together for the internal camera power supply to synchronize with the camera sync generator.

4. Turn on all of the equipments and the +20 VDC camera power. Verify that the +20 VDC supply current is approximately 0.4 amperes.
5. Allow 15 seconds warm-up for the vidicon heater.
6. Adjust the lens iris and/or scene brightness to obtain 1 volt peak-to-peak unclipped video from J3 (unregulated Video). This corresponds to 500 nanoampere signal level. If an oscilloscope is not available, observe the TV monitor and increase the scene brightness or lens opening until just before the corners of the picture begin to white saturate (beam limiting). This too, is equivalent to 500 na signal level and yields the highest signal-to-noise picture.
7. Focus the lens, or with a fixed focus lens, focus the multiplexer to the lens. Use the focussing screw mounted between J1 and J2. The vidicon moves toward lens for CCW rotation and away from the lens for CW rotation.

5.3 Maximizing Picture Quality

1. Proper monitor adjustment of contrast and brightness is important. "Linear" gray scales are helpful and proper adjustment is obtained when all shades are discernible. With 100% contrast, 2 level scenes (resolution charts) adjust the whites to the desired level and the blacks such that the blanked area around the edge of the picture (which is true black) is not quite but almost, black.

2. Since the lens (or TV optoliner) is near the sensitive vidicon target, noise pick-up and oscillations may occur if the lens or optoliner are not adequately grounded to the camera chassis via the C-mount. Make sure that the lens connection is secure and also that the C-mount flange screws are secure. Since an optoliner is an active source of electrical noise, it may be necessary to strap the optoliner to the camera chassis.

6. CAMERA MAINTENANCE AND ADJUSTMENT

DANGER - HIGH VOLTAGE

+400 VDC exists in the power supply and on the vidicon tube connector. The power supply is the largest PC board which lays on top of the deflection assembly with the printed wiring side exposed. Do not handle the power supply board or back end of the vidicon tube and connector with power ON.

6.1 Cover Removal. The four sided cover must be removed to gain access to the camera adjustments, or to remove and replace PC boards. To remove the cover simply remove the cover mounting screws from around the edge of the cover. The cover will then lift off. Refer to Figure 7 for an exploded view of the camera. It is not necessary to remove the back plate from the three sided cover, only remove the 3 screws along the bottom edge adjacent to the connectors. (Note that these 3 screws are longer than the rest (3/16 inch). For cover reassembly be sure to use the proper length screws (1/4 inch) for the remaining screws. Damage may result if longer screws are used.

6.2 Potentiometer Adjustments. Locations of the 15 adjustment potentiometers are shown on Figures 16 and 17. Detailed descriptions of the potentiometer functions are listed below:

6.2.1 Horizontal Size. Varies horizontal deflection current amplitude. The vidicon protection circuits will blank the beam whenever the deflection amplitude is less than approximately one half of the nominal setting.

6.2.2 Horizontal Center. DC current is varied in the yoke to center the raster.

6.2.3 Vertical Top Edge and Vertical Size. Vertical size and centering are interactive adjustments. The VERTICAL TOP EDGE pot controls the position of the beginning of the raster, but also has a reduced effect on vertical size. The VERTICAL SIZE pot adjusts the deflection current amplitude but has a slight effect on the position of the top edge since part of the top edge of the raster is blanked.

To adjust vertical size and centering first adjust the TOP EDGE to the desired location, then adjust the SIZE until the bottom edge is proper. It will be necessary to first readjust the TOP EDGE, then SIZE a few times to achieve the desired result because of the interaction of these two potentiometers.

6.2.4 G1 Beam Current. The beam current level is set by adjusting the G1 to cathode potential. Increasing the G1 voltage from -100 VDC toward 0 VDC increases the beam current. Proper beam current is obtained by the procedure:

1. Adjust for very high beam current (G1 = 0 V)
2. Set scene brightness level to 600 nanoamperes which is 1.2 volts peak-peak on the Unregulated Video Output J3.
3. Reduce the beam (G1 more negative) until the point just before any white saturation occurs in the corners.
4. Reduce scene brightness to 500 nanoamperes (J3 - 1 Vpp) for normal operation. Any time G1 is changed, the beam profile changes and the Electrostatic Focus G3 must be readjusted slightly.

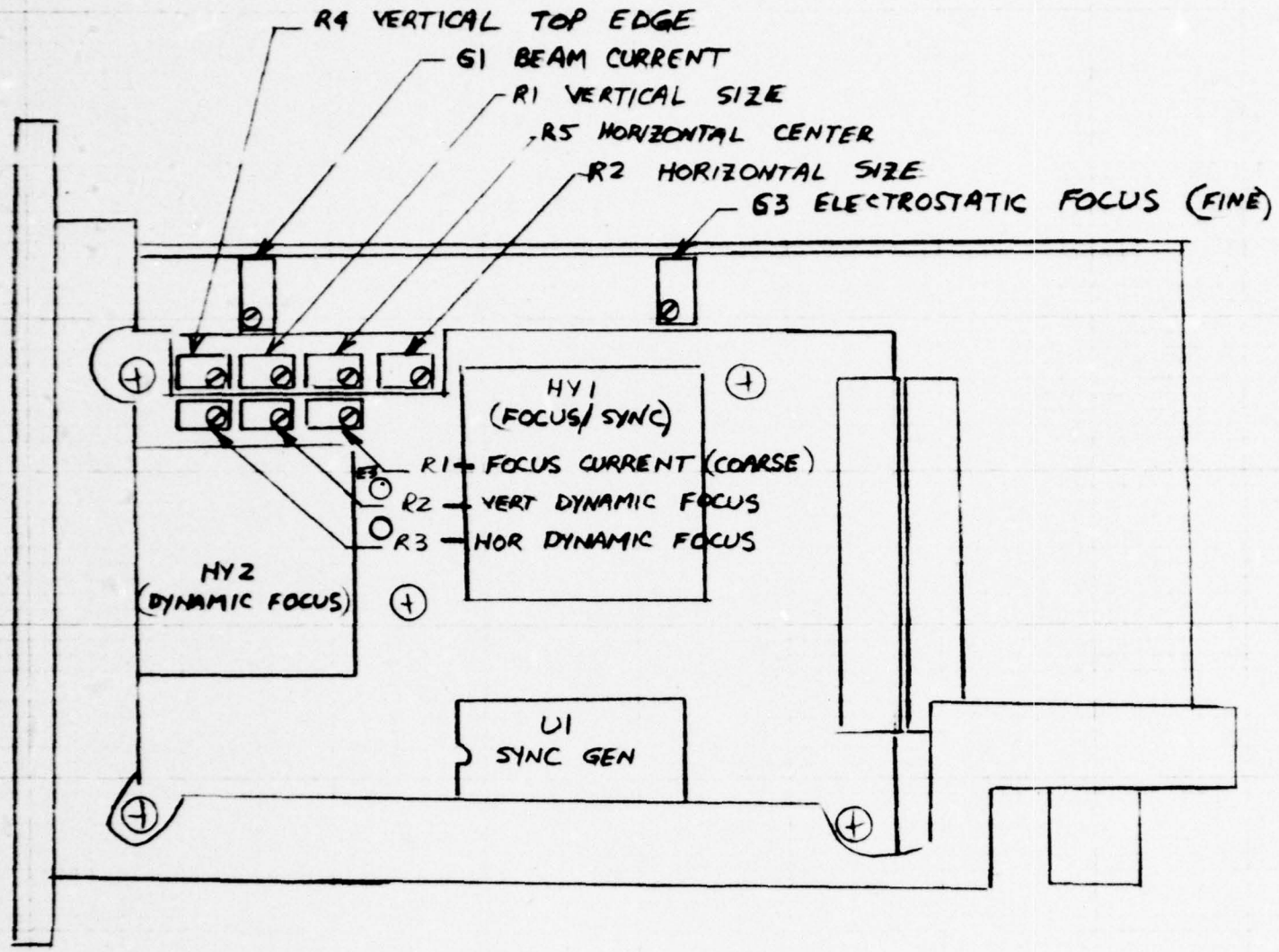


FIGURE 16

POTENTIOMETER LOCATIONS
BEAM / DEFLECTION / FOCUS

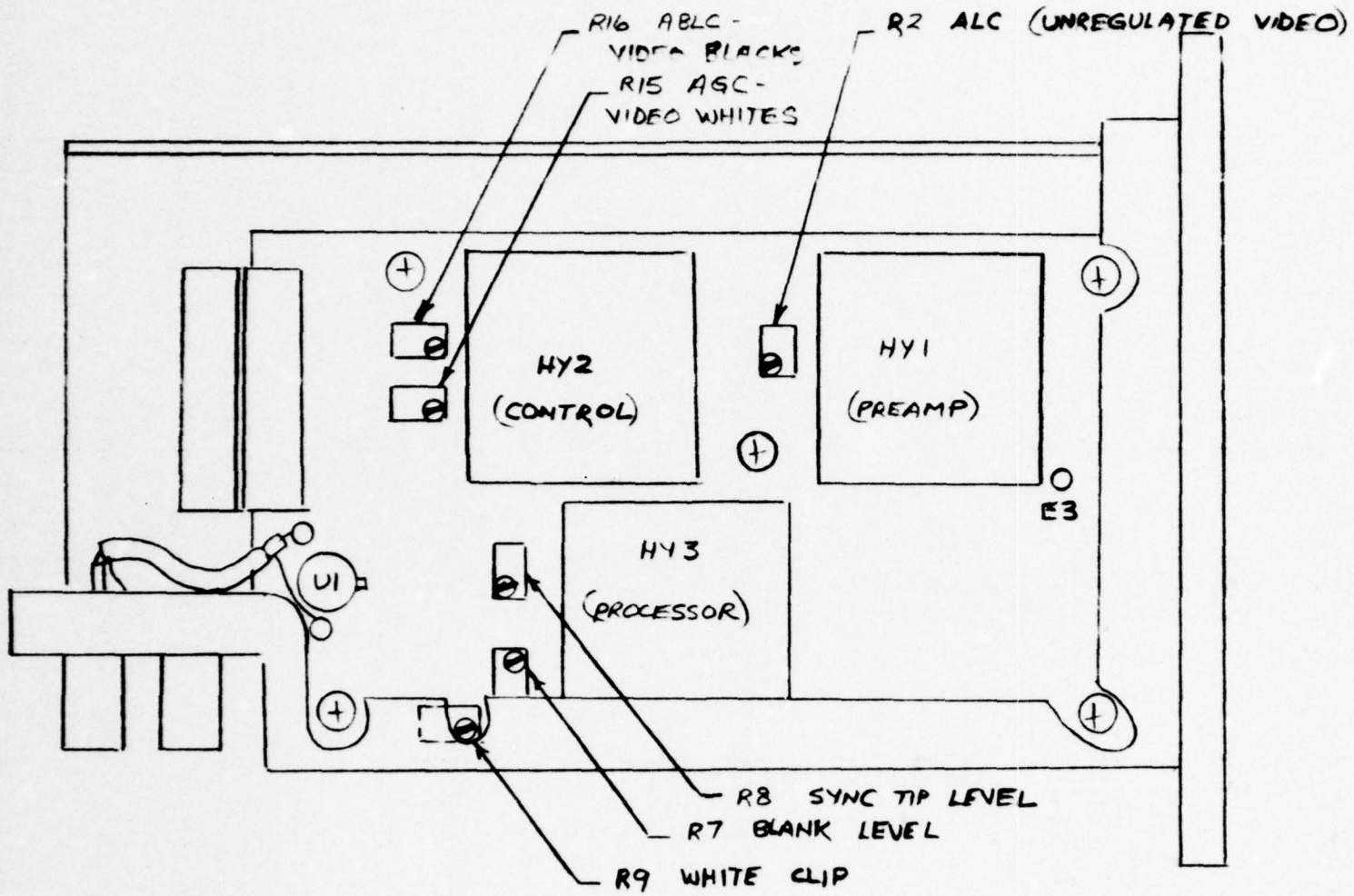


FIGURE 17
POTENTIOMETER LOCATIONS
VIDEO BOARD

6.2.5 Focus Current & G3 Electrostatic Focus - The camera is focussed by making the spot size as small as possible. The coarse adjustment for spot size is the FOCUS coil CURRENT and the fine adjustment is G3. Vidicon cathode aging or G1 readjustment causes the beam profile to change slightly, and optimum refocussing is achieved by G3 adjustment only. FOCUS CURRENT should not need changing. When vidicon tubes or focus PC boards are changed, the full focus procedure must be followed:

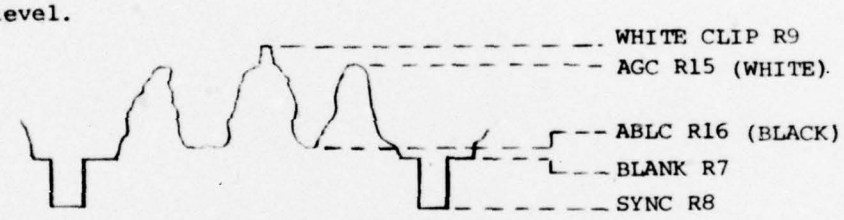
1. Set G3 to the center of its adjustment range.
2. Adjust FOCUS CURRENT for best focus.
3. Optimize lens or optoliner optical focus.
4. Repeat steps 2 and 3 as many times as required for optimum focus.
5. Fine adjust G3 for best focus.
6. Repeat steps 3 and 5 for best focus.

6.2.6 Dynamic Focus - Dynamic Focus is accomplished by AC coupling composite horizontal and vertical parabolic voltage waveforms to the G3 high DC voltage. These increase the G3 voltage in the corners to optimize corner resolution. The horizontal and vertical dynamic focus does not require readjustment unless a new vidicon is installed. The procedure for this adjustment is as follows:

1. First optimize the vidicon performance including G1, raster size and centering, focus current and G3, and alignment magnet setup.
2. Short E3 (Dynamic Focus Output) of the Focus/Beam/Sync board to ground to eliminate any dynamic correction on G3.
3. Adjust G3 voltage and make a plot of V_{G3} for best focus versus raster position in the center and all four corners. Measure V_{G3} on the center conductor of the G3 adjustment potentiometer with a high voltage differential voltmeter (to prevent loading G3.)

4. Determine the peak to peak voltage required for optimum center and corner resolution. Select the horizontal and vertical parabola amplitudes which will combine to achieve the desired result.
5. Remove the short on E3 and adjust HOR and VERT DYNAMIC FOCUS potentiometers to the selected peak-peak amplitudes.
6. Readjust G3 for optimum center resolution.

6.2.7 Video Adjustments - None of the video board potentiometers will require readjustment. Figure 18 shows the levels which are controlled by the video board potentiometers. The pots should be set to produce voltage levels per EIA RS-343 when measured at J4, with 75 ohm termination. White clip (R9) should be set 0.2 volts above the AGC white level.



VIDEO ADJUSTMENTS

FIGURE 18

Adjustment of these controls may unbalance the video within the dynamic range of the video processor. The video signal (not including sync and blank) must have an average value of +3 volts at the Processor output (HY3 pin 15).

The ALC (Unregulated Video) control R2 varies the gain of the raw video from the Preamp. This has been calibrated to 1 volt peak-peak for 500 nanoamperes signal current. The gain of the Preamp to the ALC BOT 1 output (HY1 pin 17) is approximately 1.6 Megohms or 1.8 Vpp at 500 nanoamperes.

6.3 Vidicon Tube Replacement

6.3.1 Removal Procedure.

See Figure 7 and Figure 19.

1. Remove the C-Mount plate and the power supply board.
2. Unsolder the target lead, the G4 filter capacitor, and the ground wire to the cylindrical ground plane around the tube neck.
3. Unscrew the two socket head cap screws which hold the target coaxial lead to the yoke mounting cylinder.
4. Remove the potting material holding the tube in the deflection yoke (only near the tube connector).
5. Remove the vidicon connector. (Caution: Note its orientation to the clipped pin).
6. Remove the target signal clip and the 8 plastic screws holding the tube mounting ring to the front of the yoke.
7. Slide the tube out of the front of the camera.

6.3.2 Vidicon Potting in Tube Mounting Ring. A new vidicon must be properly aligned and potted into a phenolic tube mounting ring. The potting fixture is shown in Figure 20 and the setup for potting the mounting ring to the tube is shown in Figure 21.

The potting procedure is as follows:

1. Wipe mounting surfaces clean with Methy Ethyl Ketone (MEK).
2. Prime mounting surfaces (area of bonding interface) using H. P. Fuller epoxy primer polyamide.
3. Seat silicone rubber gasket as shown. This gasket will act as a retainer dam for the potting material.
4. Align mounting ring so that its largest cutout is opposite the short pin on the tube. (See Figure 19 and Figure 21).
5. Secure ring to potting fixture and prepare potting material solithane 113 100 parts by weight with TC-700 catalyst 12 parts by weight. Load syringe and inject as shown on Figure 21. Cure for four hours.

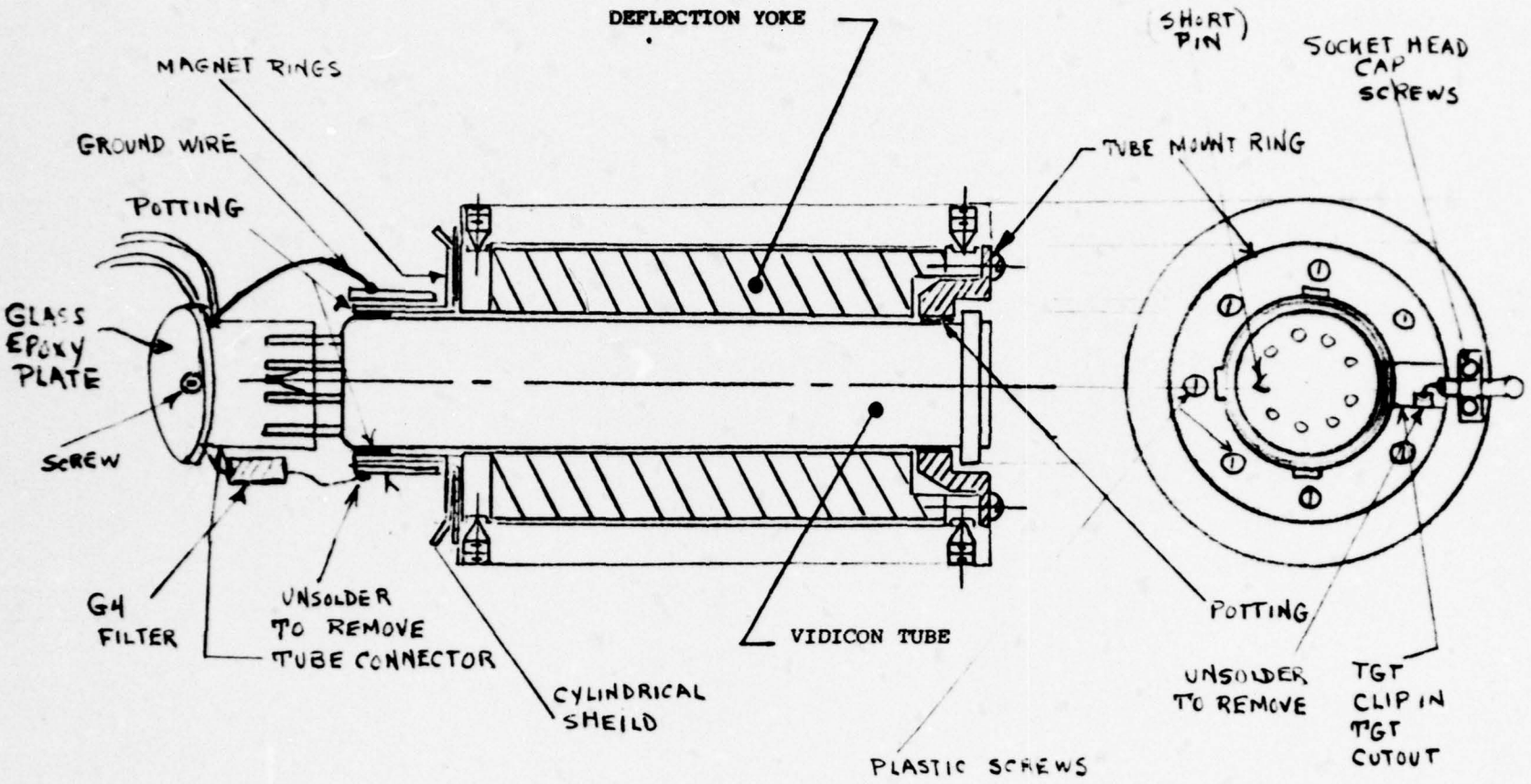
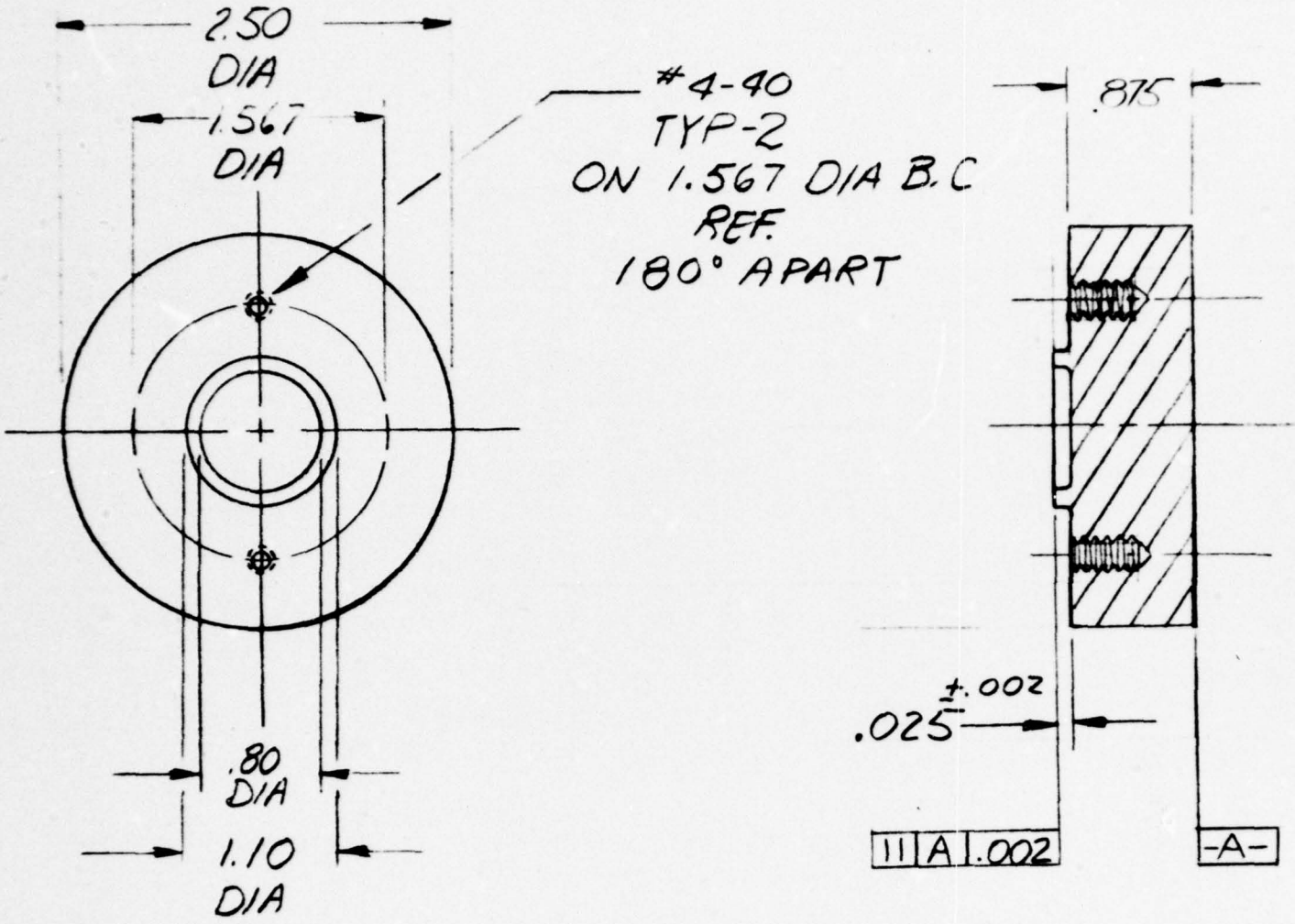


FIGURE 19 TUBE/YOKE MOUNT



MAT'L: 6061 ALUM.

FIGURE 20 POTTING FIXTURE

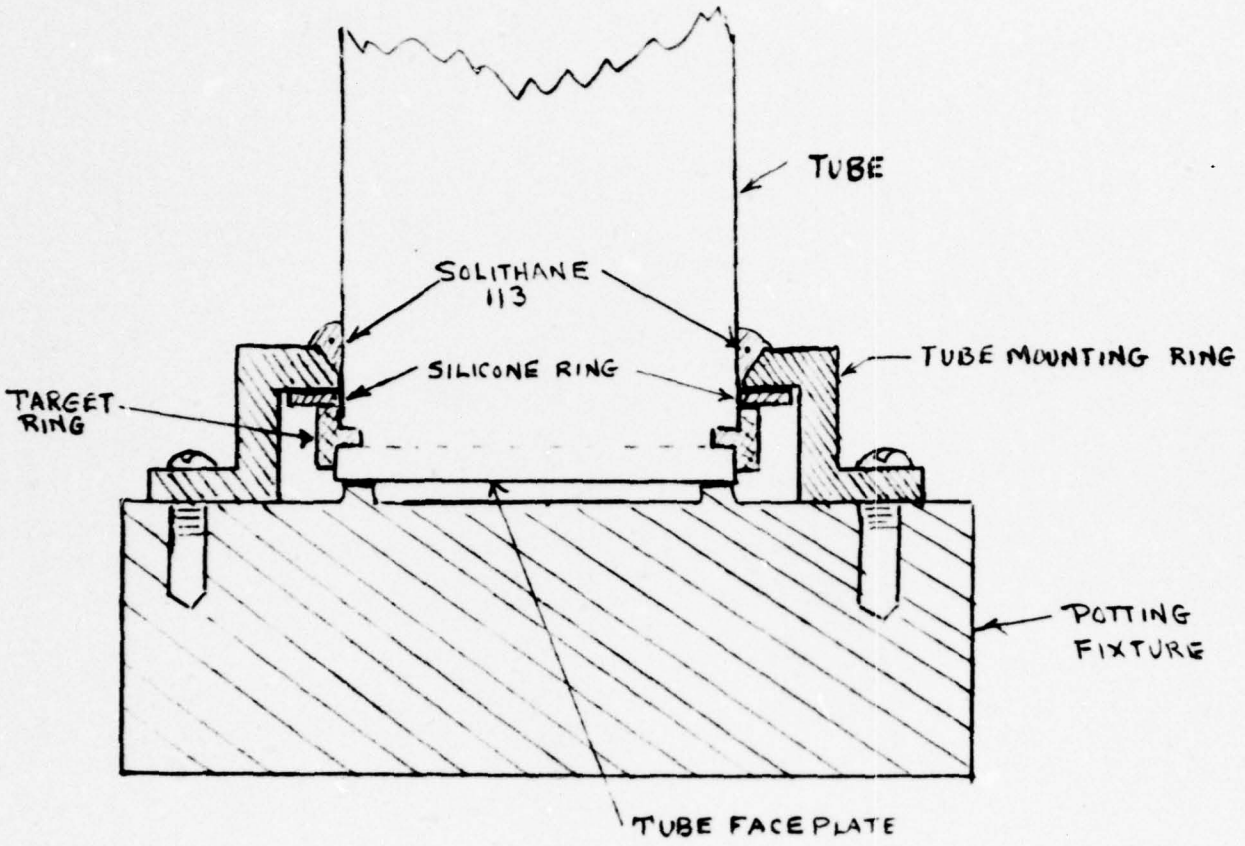


FIGURE 21 SETUP FOR BONDING MOUNTING RING TO TUBE

6.3.3 Vidicon Installation Procedure

See Figure 7 and Figure 19.

1. Install the tube in the front of the camera so the clipped pin is toward the deflection board.
2. Install the target signal clip and the 8 plastic screws holding the tube potting flange.
3. Install the target coaxial lead and socket head screws.
4. Solder the target lead to clip. (CAUTION: Do not break the target lead or get solder flux on the vidicon faceplate).
5. Install the vidicon connector. (CAUTION: Make sure the orientation is proper. The screw holding the glass epoxy protective plates to the connector should align with the clipped pin).
6. Solder the G4 filter capacitor and ground lead to the cylinder ground plane.
7. Install the C-Mount plate and lens.
8. Operate the camera and perform a full alignment procedure, outline in the next paragraph.

6.4 Alignment Procecure for New Vidicon. In order to do final alignment of the new tube, the camera should be fairly close to normal operating conditions. Refer to paragraph 6.2 POTENTIOMETER ADJUSTMENTS for procedures and guidelines for the following steps.

1. Set up the deflection amplitudes (just within the target ring), light level to 500 na and G1 beam current, and focus current and G3 focus voltage.
2. When a fairly good picture is obtained the alignment magnets must be positioned to optimize beam landing on the target.
3. Reduce the target voltage to 3.5 volts by loading the Alignment Test Point E3 on the video board with 75 K ohms.

4. Reduce the light level until some picture is visible.
5. Rotate the two alignment rings in the rear of the yoke. One is toothed as a gear, and the other has two tabs. Use a cutoff orange wood stick to turn the rings to avoid touching the +400 VDC on the tube connector. Rotate the rings to achieve a symmetrical picture where all four corners become white saturated (target saturation) an equal amount.
6. Remove the 75 K ohm load.
7. Repeat the calibration of light level, beam current G1, deflection size and centering, G3 and focus current, and optical focus to the final values.

7. CONCLUSIONS

The overall objectives of the E/O Multiplexer development program were fully achieved. Extensive use of hybrid microelectronic devices resulted in the weight and size requirements being satisfied. Employment of CMOS devices and utilization of design tradeoff techniques resulted in a total power input of 7.6 watts with full compliance to resolution, signal-to-noise, distortion, shading and picture quality specification requirements.

8. RECOMMENDATIONS

The following recommendations are suggested to further improve the environmental and performance capability of the E/O Multiplexer.

a) Reconfigure with the C23262B ceramic vidicon to reduce microphonic signal levels when used in high vibration environment.

b) Expend further design effort on the Preamplifier hybrid to reduce noise and improve the bandwidth stability with temperature.

c) Employ full tube length potting technique to secure the tube within the yoke.

d) Modify Power Supply to accommodate higher ripple input for applications requiring less susceptibility.

e) Improve horizontal deflection temperature stability.

f) EMI gasket seals should be used between the cover and the main chassis structure to reduce the RF susceptibility.

APPENDIX A

A1. VIDEO PROCESSING CIRCUITRY

A1.1 Aperture Correction. The overall schematic of the video board is shown in Figure A1. A simplified schematic of the aperture correction circuit is shown in Figure A2(c). The output of the video preamplifier hybrid is coupled to delay line DL1. The output impedance of the preamp hybrid is matched to the characteristic impedance of DL1. Typical video waveforms are shown in Figure A2(a). The video waveform $\sim_A$ is the input $\sim_i$ delayed by DL1 and attenuated by R_3 and R_4. R_3 and R_4 have been selected such that they represent an open circuit termination to DL1. The waveform $\sim_B$ is the sum of the input waveform $\sim_i$ and the reflected DL1 waveform attenuated by resistors R_5 and R_6. R_5 and R_6 have been selected to prevent loading of the DL1 input. The waveforms $\sim_A$ and $\sim_B$ are subtracted in a differential amplifier at the input of the Video Processor hybrid. The resultant boost in the video frequency response is shown in Figure A2(b). The boost peak occurs at a frequency f_o which is equal to the reciprocal of twice the time delay, td, of DL1. The shape of the boost is cosinusoidal around f_o and is equal to the nominal low frequency gain b at zero frequency and at 2 f_o. For an ideal delay line the boost peak is repeated at 3 f_o, but, typically, the actual delay line bandwidth will extend to only 2.5 f_o. The gain peak is b plus 4a as shown. For this example, b + 4a is equal to 2b which corresponds to a boost of 2 at f_o. If b is nominalized to 1, the b + 4a = 2b becomes 4a = 1 or a = 0.25. The waveform $\sim_A$ = b + 2a = 1.5 and $\sim_B$ = 2a = 0.5 or the ratio of $\sim_A$ to $\sim_B$ is three for a frequency boost of two. The resistors R_3, R_4 and R_5, R_6 are adjusted appropriately to yield this ratio of $\sim_A$ to $\sim_B$.

For the resistor values, the time delay, etc. shown on Figure A1 the boost frequency is 10 MHz and the boost is approximately 1.7 to 1.

A1.2 Video Processor. The schematic of the video processor hybrid is shown in Figure A3. The outputs of the delay line aperture correction circuit

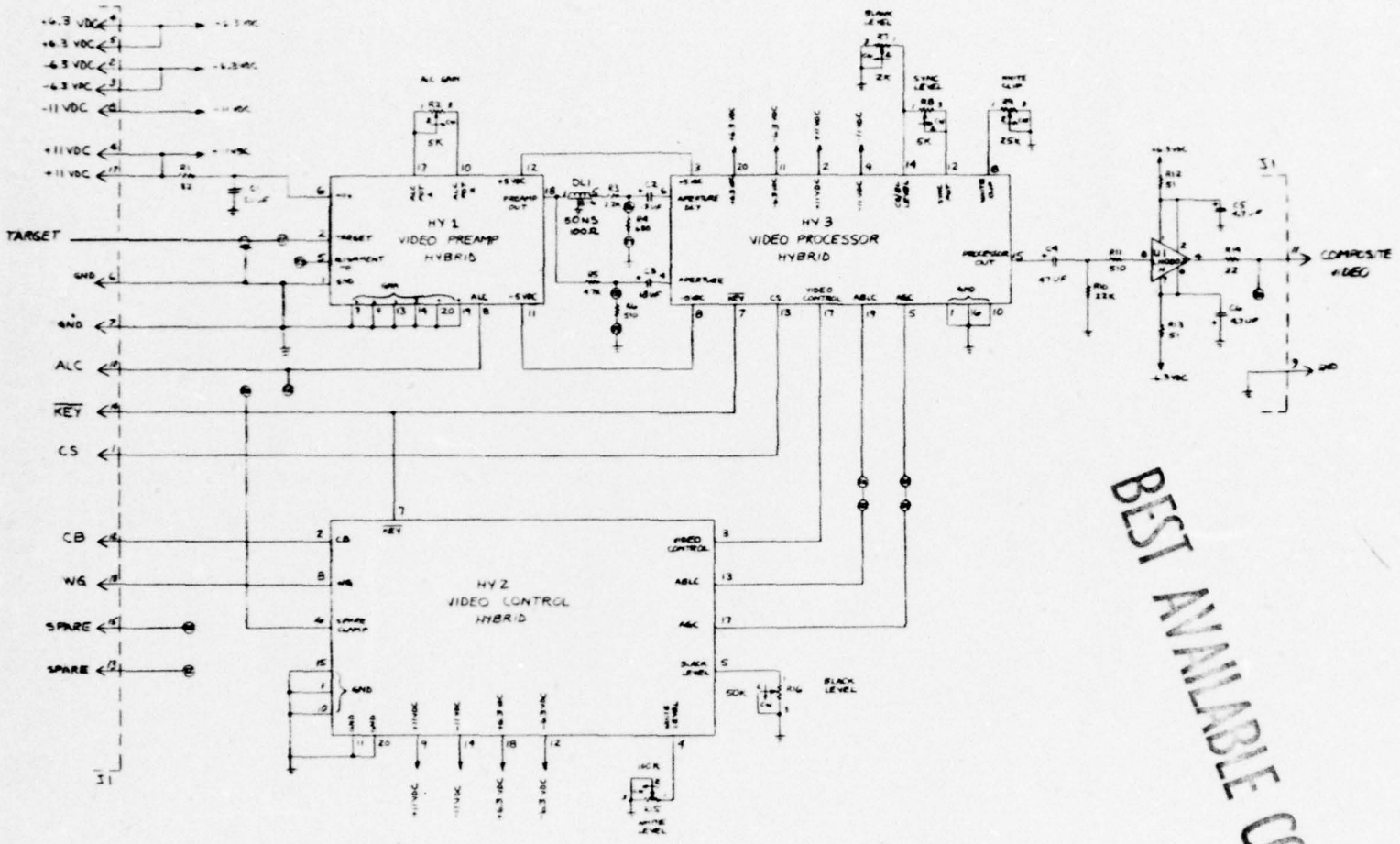


Figure A-1. ELECTRICAL SCHEMATIC VIDEO BOARD

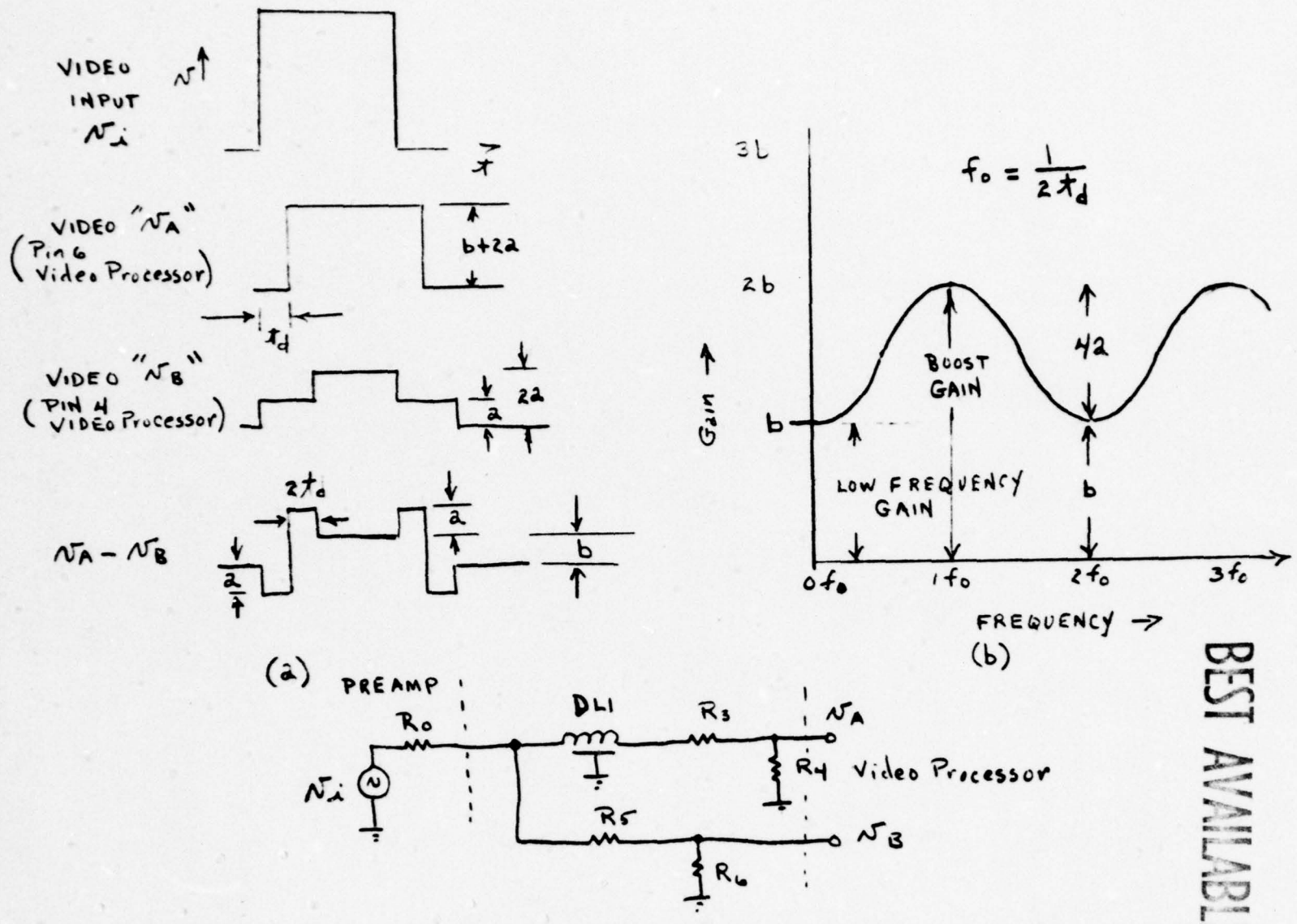


FIGURE A2 (a) VIDEO WAVE FORMS
(b) VIDEO GAIN VS FREQ
(c) Simplified Circuit

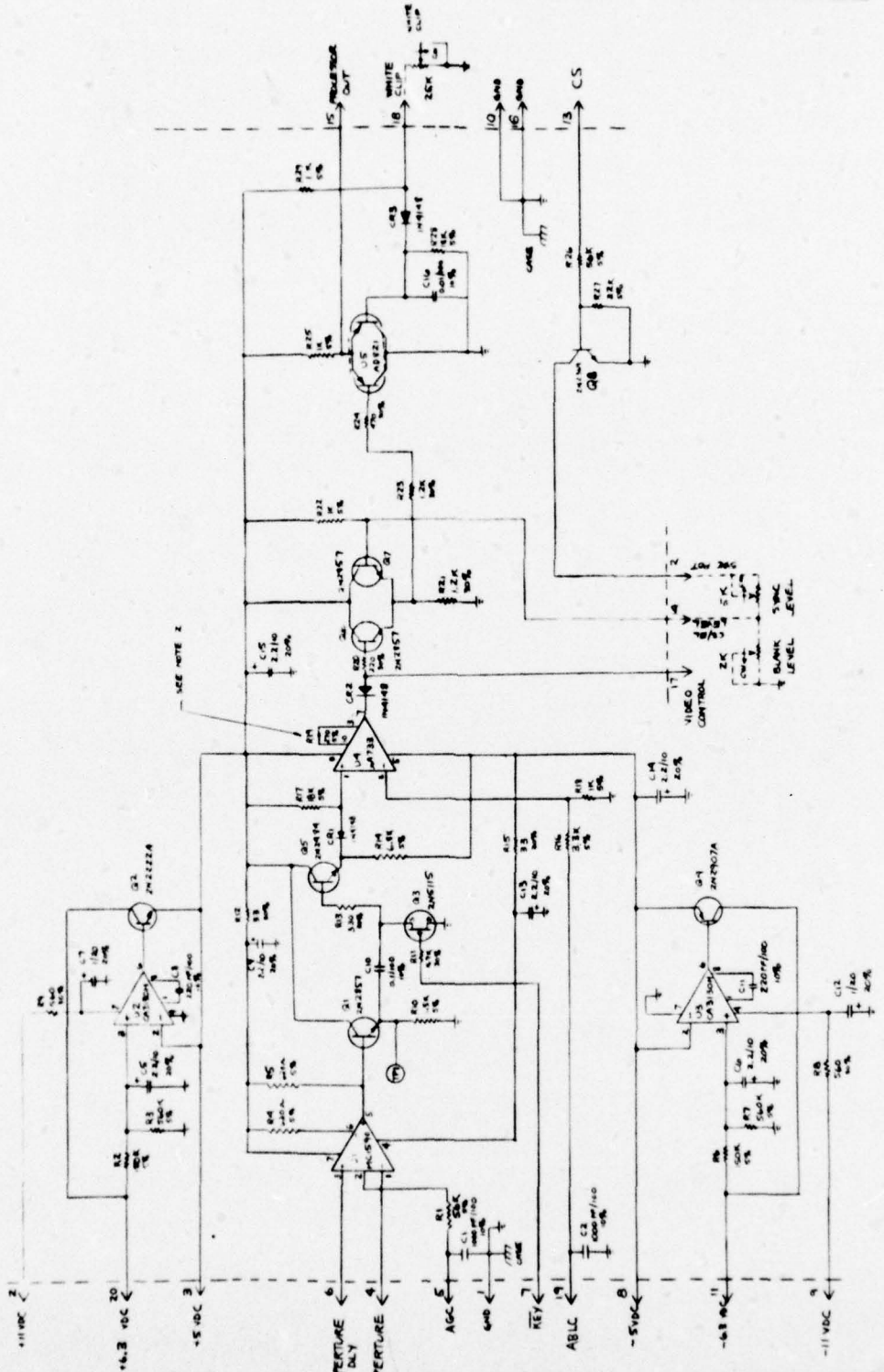
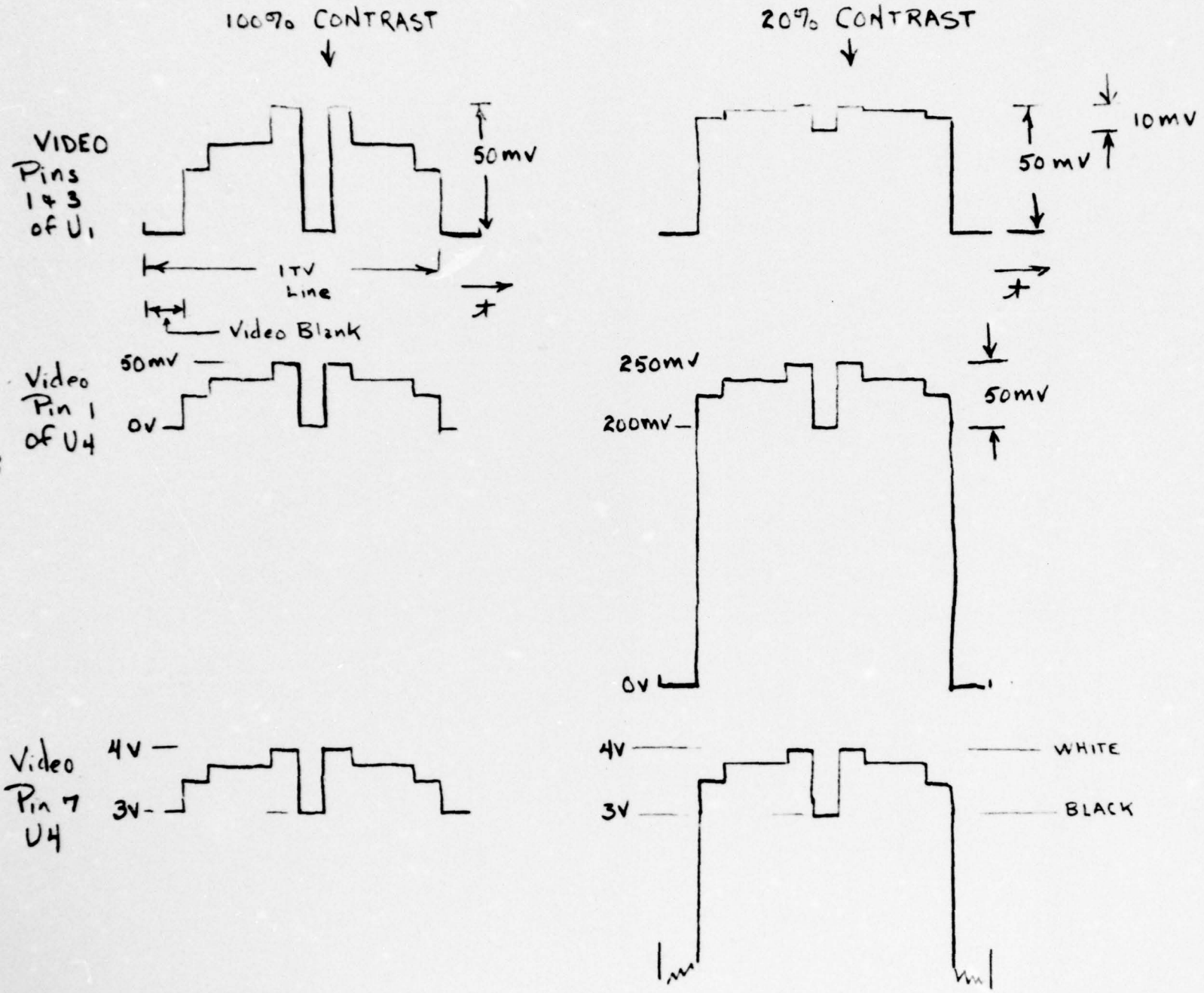


Figure A-3. ELECTRICAL SCHEMATIC VIDEO PROCESSOR HYBRID

are applied to the inputs 1 and 3 of U_1, which is a wide band differential video amplifier with an Automatic Gain Control (AGC). The gain control input is a d-c voltage which is applied to pin 2 through R_1. The range of gain control is approximately 26 db. The usable video input ranges from approximately 50 mV for 100% contrast to 5 mV for 10% contrast scenes. The usable video output signal at pin 5 of U_1 is maintained at a constant peak-to-peak value of approximately 50 mV. Waveforms are shown in Figure A4. Note that for 100% contrast, the peak-to-peak video extends from the video cathode blank level to a maximum of 50 mV and for 20% contrast the total signal is 50 mV but the information content of the video is only 10 mV peak-to-peak. The gain of U_1 is controlled to maintain the information content of its video output at a constant 50 mV peak-to-peak. The video at pin 5 of U_1 is unity buffered by Q_1 and then clamped to ground during the blank level portions of the video waveform. The clamped video is coupled to pin 1 of U_4 through Q_5 and CR1 and appears as shown in Figure A4 for both the 20% and the 100% contrast conditions. Note that the usable video is the same, but that the video pedestal is huge for the video with 20% contrast. The gain of U_1 from pin 1 to pin 7 is approximately 20 from zero to 25 MHz. The Automatic Black Level Control (ABLC) d-c voltage is applied to pin 2 of U_4.

The ABLC voltage automatically adjusts the output video d-c level such that the whitest portion of video is at 4 V and the blackest portion is at 3 V as shown on Figure A4. The extra pedestal length on the video for the 20% contrast case is removed by the black clamp (Q_6 and Q_7). Additional pedestal is added to the video by clamping the input of Q_6 to ground during the video blank level to insure that the video at 100% contrast level has a proper black reference level. The video waveform at the input of Q_6 is shown in Figure A5. Q_6 is a unity gain buffer during the active video period and it becomes a black clipper during the blank period. The clipping level of the blank is set by adjusting the 2K Ω blank level potentiometer which sets a d-c voltage level equal to the blank level on the base of Q_7. This level is modified instantaneously to a lower level by the action of the switch Q_8 which is switched on during the composite sync intervals. The amount by which the blank level is lowered to the sync

FIGURE A4 VIDEO AGC & ABLC



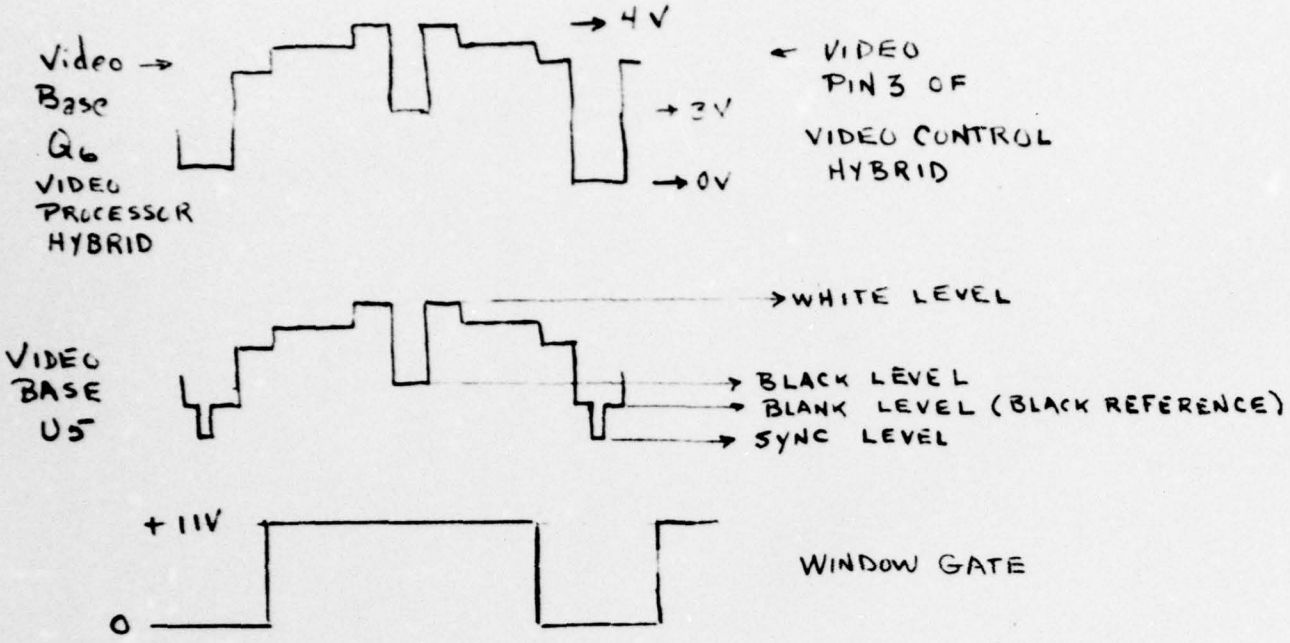


FIGURE A5 VIDEO WAVEFORMS

level is determined by the adjustment of the 5K Ω sync level potentiometer. The video output waveform with the proper blank and sync levels inserted is shown in Figure A5. The operation of Q_6 and Q_7 is as follows. During the active video line time the video voltage levels are higher than the voltage set on the base of Q_7; hence Q_6 acts as a unity gain emitter follower with Q_7 held off. During the blank intervals the video waveform voltage levels are always less than the voltage set on the base of Q_7; hence the output video will clamp to the levels set on the base of Q_7 and Q_6 will be held off. The video from Q_6 and Q_7 is coupled to one base input of the PNP transistor pair designated as U_5. The other base input of U_5 is held at a constant d-c level which has been set by the 25K white clip potentiometer to a level which is just slightly higher than the maximum allowed peak white level. Video spikes or noise extending above this level will be clipped in a manner similar to that provided by the NPN transistor pair Q_6 and Q_7.

The combination of U_2 and Q_2 is an active filter that provides a ripple free very low impedance output of +5 V DC, which is used to provide power to both the preamplifier and video processor. Ripple on both the +11 V DC and +6.3 V DC supplies are reduced by a factor of 150 or more for ripple frequencies extending from 60 Hz to 20 MHz. The same function for the -5V DC power is provided by the combination of U_3 and Q_4.

The output video is coupled from the video processor at pin 15 of the hybrid. This output as shown on Figure A1 is capacitively to an output video buffer U_1. The output of U_1 is designed to drive a video cable with a termination of 75 Ω.

A1.3 Video Control. The schematic of the video control hybrid is shown in Figure A6. The basic operation of the video white level control and the black level control circuitry are very similar. The input video designated as video control is applied to two high speed comparators. The U_{1B} comparator generates an error signal whenever the peak black video signal falls below a set reference

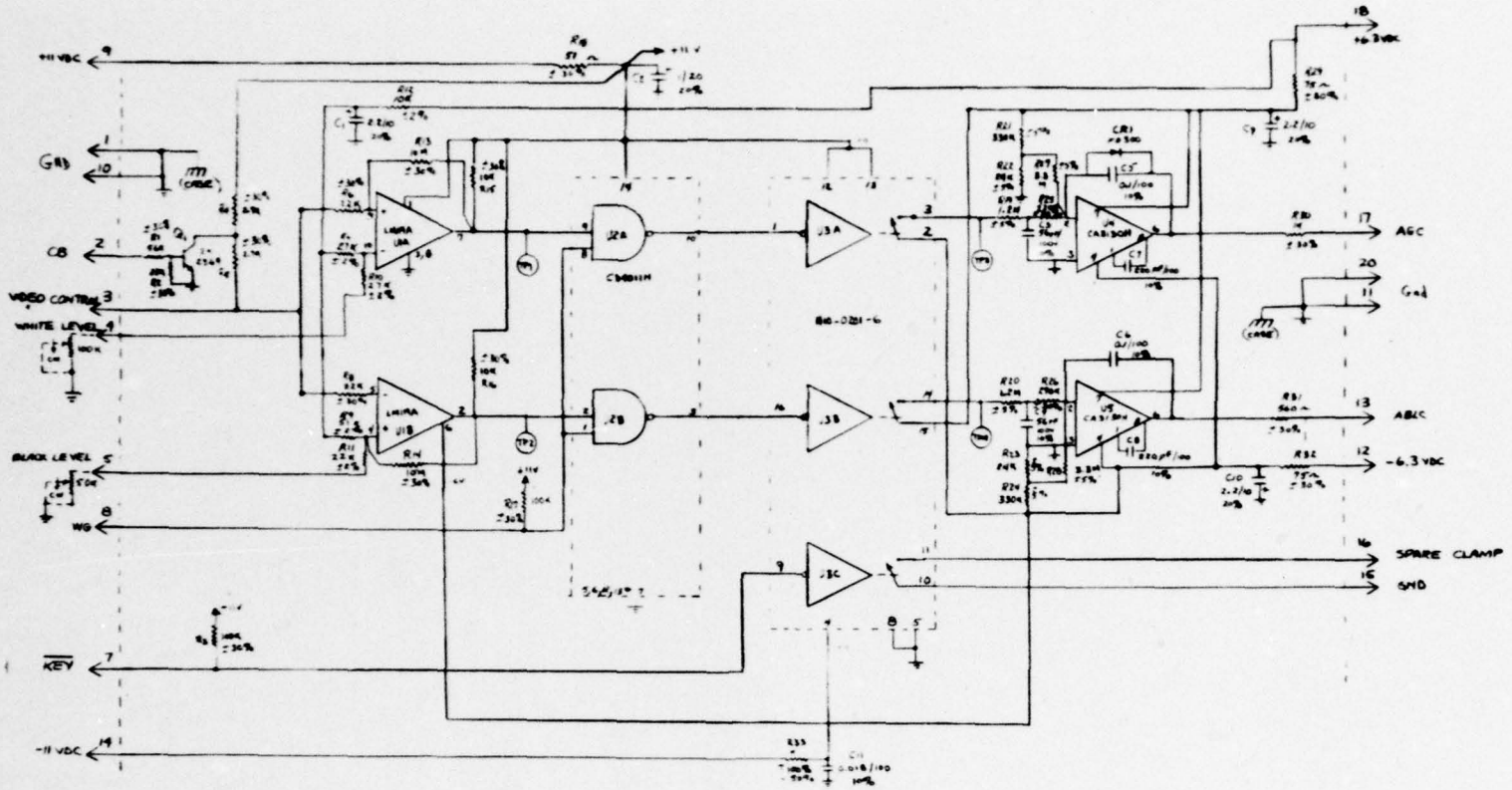


Figure A-6. ELECTRICAL SCHEMATIC VIDEO CONTROL HYBRID

black level of 3 volts. This error signal causes the output integrator U_5 to slew very rapidly in a direction which drives the black signal level above 3 volts. A much weaker slew is also applied to the integrator to return the peak black video to the black reference level whenever there is no peak black video crossing the reference level. The U_{1A} comparator generates an error signal whenever the peak white video signal goes above a white reference level of 4 volts. This error signal causes the output of integrator U_4 to slew very rapidly in a direction which drives the peak white signal below 4 volts. A much weaker slew is also applied to the integrator to return the peak white signal to the white reference level whenever there is no peak white video crossing the reference. Both loops are bi-stable, that is the video levels are continually being driven towards and away from their reference levels. The resultant video ripple is made negligible by making the strength of the video drive weak in one direction and strong in the other, and by proper selection of the integrator's time constants. The loop's time constants and gains were obtained empirically.

The details of the black level and white level control circuits are as follows. The video input to the base of Q_6 of the video processor hybrid, see Figure 3, is coupled directly to pin 3 of the video control hybrid. The video waveform at pin 3 is shown in Figure A5. The additional pedestal insertion shown was discussed in section 1.2 and is needed for proper addition of blank and sync. The circuit, which provides the pedestal insertion is shown on Figure A6. It consists of associated resistors and switch Q_1 which is switched on during the video blank periods. When Q_1 is on diode CR_2 of Figure 3 goes off and the video level is pulled to the ground voltage level, see waveform Figure A5.

U_{1A} and U_{1B}, shown on Figure A6, are high speed comparators. The voltage level on pin 10 of U_{1A} is adjusted to approximately 4 volts by the white level adjustment potentiometer and the voltage on pin 4 of U_{1B} is adjusted to approximately 3 volts by the black level potentiometer. The input video is applied to pin 9 of U_{1A} and to pin 5 of U_{1B}. Since pin 9 is the positive input pin of U_{1A} any white video which exceeds 4 volts will cause the output pin 7 of U_{1A} to go

positive, and since pin 5 is the negative input of U_{1B}, any black video which is less than +3 volts will cause the output pin 2 of U_{1B} to go positive. Positive feedback which is obtained through resistors R_{13} and of U_{1A} and R_{14} of U_{1B}, provides a small amount of hysteresis which prevents the comparators from self oscillating. The positive outputs of the comparators are applied to the inputs of the And gates U_{2A} and U_{2B}. The outputs of U_{2A} and U_{2B} are also controlled by a window gate pulse WG. The WG allows only the center 80% of the raster video signal to control the outputs of U_{2A} and U_{2B}; hence, the video is sampled independent of raster edge transients or blanking levels. U_{2A} will only go low whenever the active video exceeds 4 volts and U_{2B} will only go low whenever the active video is less than 3 volts. The outputs of U_{2A} and U_{2B} control FET switches U_{3A} and U_{2B} respectively. Whenever U_{2A} is low the FET switch between pin 2 and 3 of U_3 will couple a negative -6.3 volts through R_{19} and R_{25} to the input of the d-c integrator U_4, which has a gain of approximately +45 volts per second. Since U_{2A} will be low only when the input video exceeds 4 volts, the output of U_4 will very rapidly lower the gain of the video processor to a value which places the peak video output at a level of 4 volts. A positive voltage of approximately 0.4 volts is applied to U_4 through R_{27}, the integrator resultant output voltage change will be -1.3 volts/sec. This -1.3 V/sec provides a positive gain adjust in the video processor.

A positive gain adjust is required to increase the video to the 4 volt peak value where it is then controlled to this level by the negative gain adjustment provided by the input to the integrator from the white level control loop consisting of U_{1A}, U_{2A}, U_{3A}, U_4, and the video processor.

The black level integrator U_5 which is controlled by FET switch U_{3B} operates in a manner similar to that of the white level integrator U_4 with the following exceptions. The integrator is slewed very rapidly (-45 volts/sec) to drive the peak video black above 3 volts and is constantly slewed slowly in a direction to place the video peak black at 3 volts. The output integrator voltage adjusts the d-c level of the video processor.

This technique for video control is very accurate and provides very fast control for rapid increases or decreases in the video content of imaged scenes.

APPENDIX B.

875 TVL SYNC GENERATOR

A simplified functional block diagram of the 875 TVL Sync Generator is shown in Figure B1.

The 875 TVL Sync Generator is a custom monolithic CMOS LSI manufactured by RCA, Solid State Division, which meets all requirements of EIA RS-343. It is driven by a 1.155 MHz Crystal Oscillator and generates all of the timing signals required by the camera. It is packaged in a standard 24 pin ceramic Dual In Line "D".

The Clock Select U_1 is normally not used but is built in for use in GEN LOCK applications. The Horizontal Counter, U_2 and U_3 is synchronous and divides by a total of 44X. All of the horizontal logic signals to deflection, power supply, key clamp, dynamic focus, sync, blank, and ABLC/AGC window gate are decoded by a Synchronized Decoder U_4.

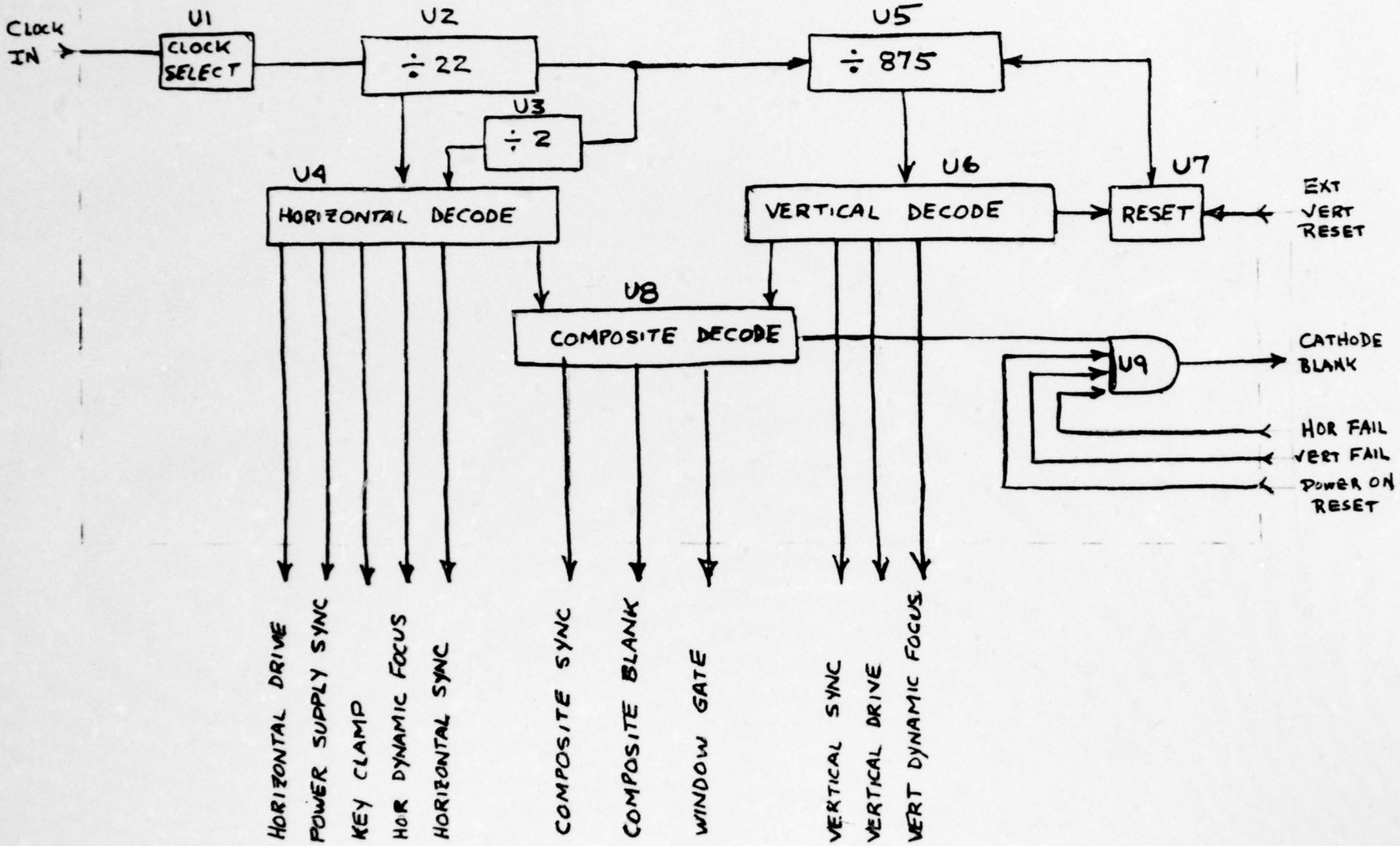
The Vertical Counter U_5, divides each half line by 875X resulting in the 60 Hz field rate. All of the vertical logic signals for deflection, sync output signal, dynamic focus, sync, blank, and window gate are decoded by U_6.

Composite logic signals are combined from U_4 and U_6 by the Decoder U_8 to provide composite sync, composite blank, window gate, and cathode drive. The Cathode Drive is inhibited and the beam cut off in the event of horizontal or vertical deflection failure or during power turn on via U_9.

The Vertical Counter U_5 is reset and recycled internally at the count of 875 half lines via U_6 decoding and U_7 reset circuit. For external GEN LOCK applications, the vertical counter may be reset to the first vertical sync serration pulse by the external input into U_7.

The Sync Generator specification and waveforms are given on the following pages.

FIGURE B1 875 TVL SYNC GENERATOR CMOS LSI



875 TVL SYNC GENERATOR SPECIFICATION

Design and fabricate an LSI version of TCC051102, TV Sync Generator. Package should be a standard 24 lead Dual In Line ceramic "D".

Input clock frequency is 1.155 MHz. The composite blank and sync output wave forms must comply with EIA-RS343.

In addition, the package shall be designed to meet the requirements of MIL-STD-883B.

Test requirements are as follows:

1. Stabilization Bake - at +150°C for 24 hours.
2. Temperature Cycle - -55°C to +125°C for 5 cycles.
3. Seal Test - Fine & Gross leak.
4. Performance Tests
   a. Functional Low Frequency test at V_{DD} = 5 and 12.5 volts.
   b. Noise immunity test - noise immunity shall be at least 20%.
   c. Output Source Voltage Test - Verify $V_o \geq 4.5V$ for I_DP_{MIN}, +25°C, V_{DD} = 5V.
   d. Output Sink Voltage Test - Verify $V_o \leq 0.5V$ for I_DN_{MIN}, + 25°C, V_{DD} = 5V.
   e. Device Leakage Current Test - With V_{DD} = 12.5V, I_{DD} shall be less than 100 ua with all inputs in the state to eliminate current through internal pull-up and pull-down resistors.
   f. Operational Leakage Current Test - with V_{DD} = 12.5V, during the functional test. At no logic state shall I_{DD} exceed the sum of the Device Leakage plus the allowable current through biased internal resistors.
   g. Input Terminal Leakage Test - input current I_I shall be less than 10 ua at V_{DD} = 12.5V.

875 TV SYNC GEN TIMING AND SIGNAL DEFINITION
TCC 05 1102
EIA RS-343

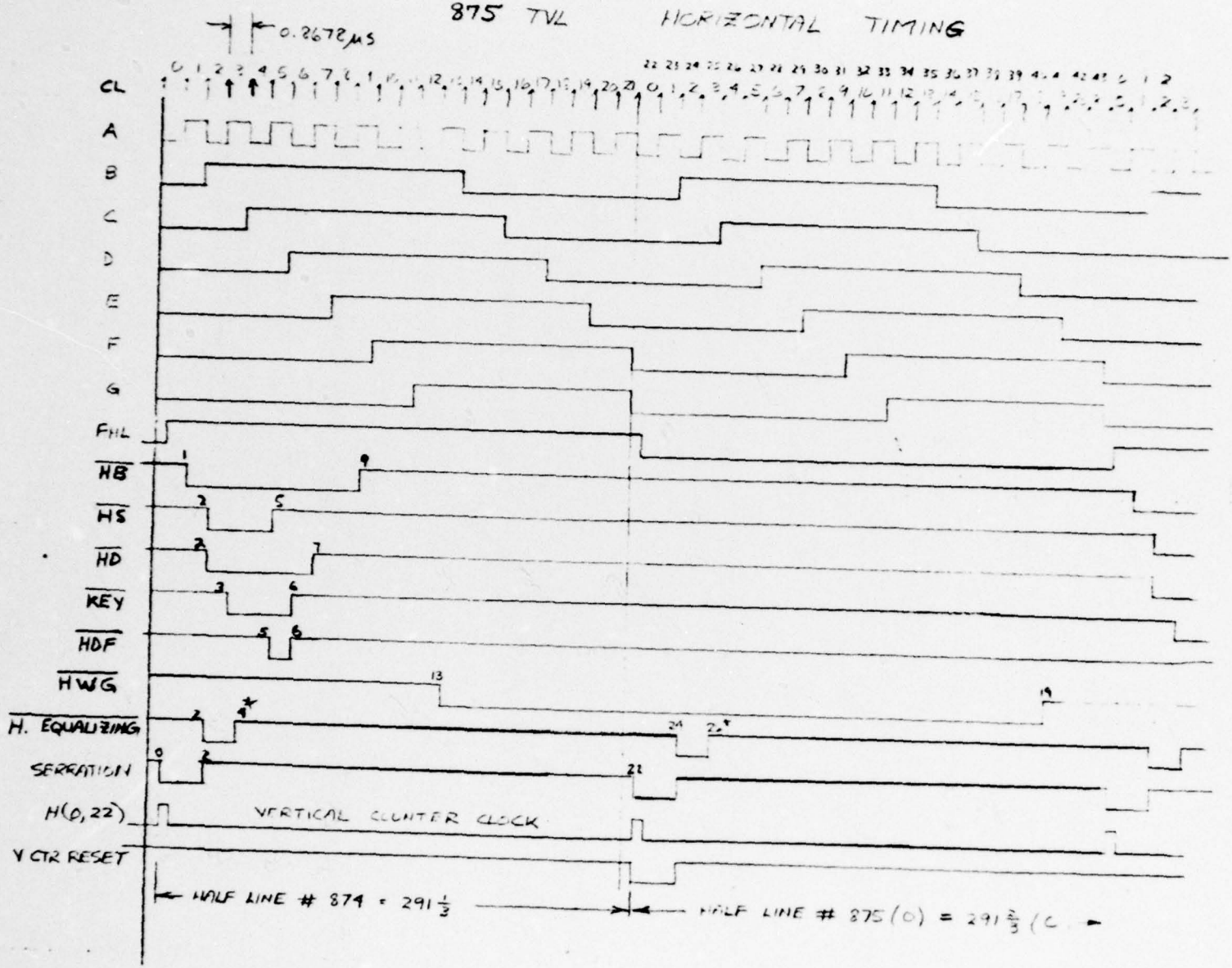
HORIZONTAL FREQUENCY = 26.250 KHZ
VERTICAL FREQUENCY = 60 HZ

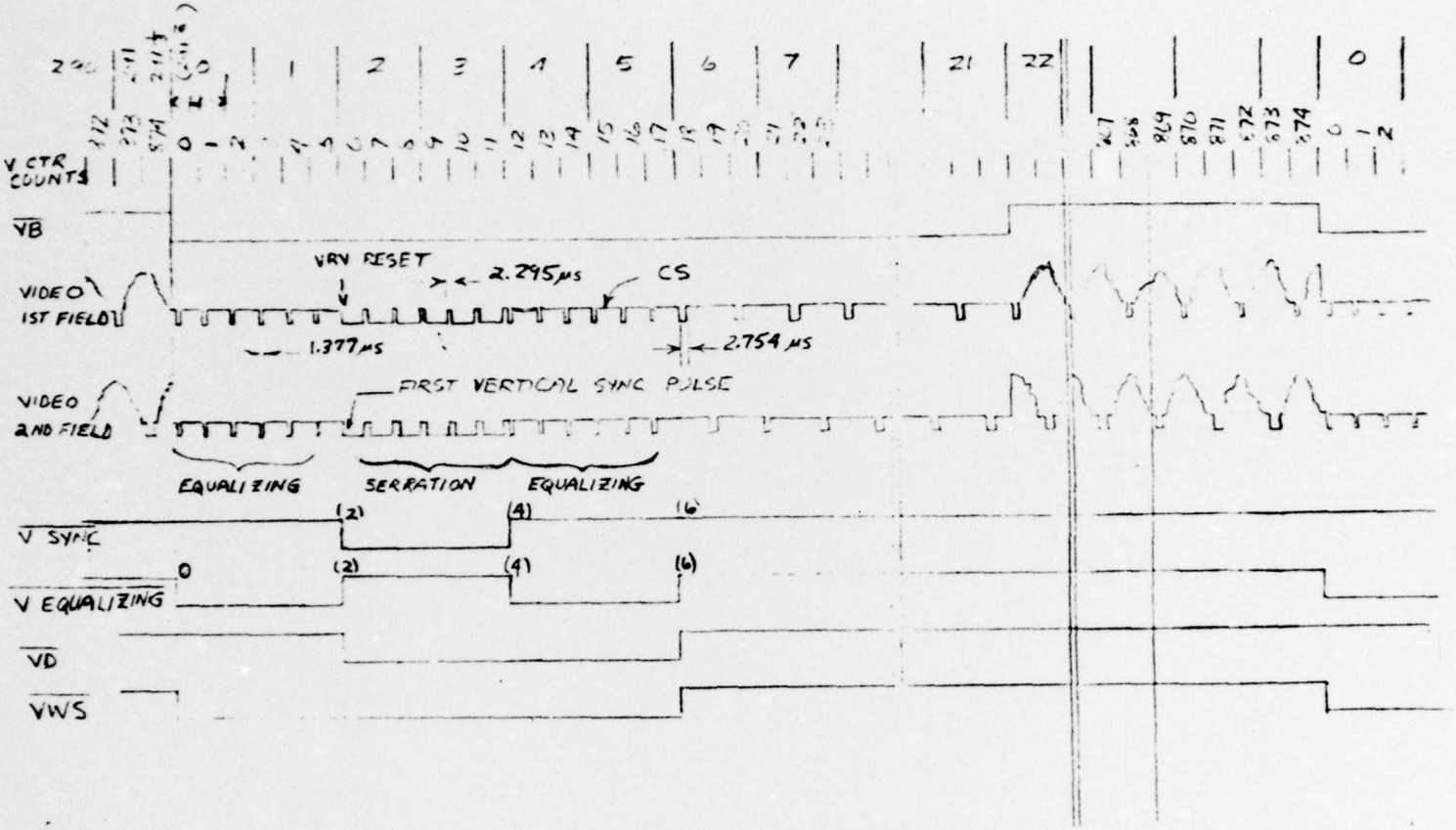
PIN NO.	SIGNAL	DESCRIPTION	TIMING
2	XIN	CMOS CLOCK INPUT	1.15500 MHZ
5	AUXCL	Auxilliary clock input	1.15500 MHZ
3	XOUT	INVERTED XIN OUTPUT	1.15500 MHZ
4	CL	Buffered clock output	1.15500 MHZ
9	XINHIB	High level inhibits XIN	---
8	$\overline{HR}$	Low resets horizontal counter	---
23	$\overline{HFAIL}$	Low indicates horizontal deflection	---
		failure	---
21	$\overline{VFAIL}$	Low indicates vertical deflection failure	---
20	$\overline{RESET}$	Low forces $\overline{CATBLK}$ low	---
7	$\overline{CATBLK}$	Low blanks the cathode	
		Horizontal drive timing	Same as $\overline{HD}$
		Vertical drive timing	Same as $\overline{HD}$
1	CB	Composite blank	
		Horizontal Delay	0
		Width	6.93 µs
		Vertical Delay	0
		Width	1256 µs
6	CS	Composite sync signal	---
		a. Equalizing at 2X Horizontal rate	---
		horizontal delay	0.87 µs
		width	1.3 µs
		vertical delay	0
		width*	343 µs
		*Equalizing pulses occur during first 1/3 and last 1/3 of this interval.	

PIN No.	SIGNAL	DESCRIPTION		TIMING
		b. Serration at 2X horizontal rate		
		horizontal	delay	-0.87 μs
			width	1.7 μs
		vertical	delay	114 μs
			width	114 μs
15	VRV	Vertical counter is reset to the first vertical sync pulse on the VRV falling transition.		---
22	$\overline{HS}$	Low horizontal sync	delay	0.87 μs
			width	2.6 μs
19	$\overline{HD}$	Low horizontal drive	delay	0.87 μs
			width	4.3 μs
18	$\overline{HDP}$	Same as 19		
14	$\overline{KEY}$	Low key clamp pulse	delay	1.7 μs
			width	2.6 μs
16	$\overline{HDF}$	Low horizontal dynamic focus pulse		---
			delay	3.5 μs
			width	0.87 μs
11	$\overline{VS}$	Low vertical sync	delay	114 μs
			width	114 μs
13	$\overline{VDF}$	Low vertical dynamic focus pulse		---
			delay	573 μs
			width	114 μs
10	VD	Low vertical drive	delay	114 μs
			width	229 μs

PIN NO.	SIGNAL	DESCRIPTION		TIMING
17	WG	Window gate, high during center of raster		
		Horizontal	delay	10.4 μs
			width	24.2 μs
		Vertical	delay	2.3 ms
			width	13.4 ms
24	+11 VDC	V_{DD}		---
12	GND	V_{DD} Return		

875 TVL HORIZONTAL TIMING





NOTE: EACH VERTICAL COUNTER COUNT IS ½ HORIZONTAL LINE OR 22 HORIZONTAL COUNTS. A FULL HORIZONTAL LINE IS 44 HORIZONTAL COUNTS

875 TVL SYNCHRONIZER - VERTICAL TIMING