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(6) EPITAXIAL GROWTH OF SEMI-INSULATING GaAs

Epitaxial Growth/GaAs

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SUMMARY INFORMATION

This Quarterly Report describes research done in the Microwave Technology Center of RCA Laboratories under Contract No. N00014-77-C-0542 during the period 1 July 1977 to 30 September 1977. F. Sterzer is the Center's Director; S. Y. Narayan is the Project Supervisor, and S. T. Jolly the Project Scientist. D. Capewell also participated in the research project.

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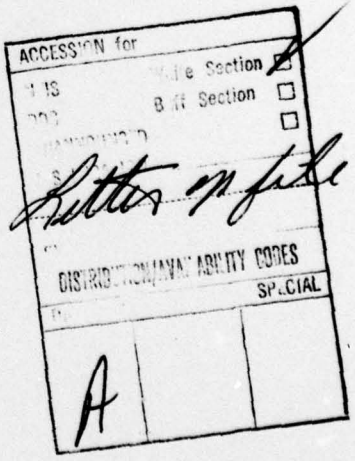


SECTION I
INTRODUCTION

The objective of this program is to develop techniques for the vapor phase growth of high resistivity epitaxial layers of gallium arsenide on semi-insulating gallium arsenide substrates. A capability to grow such layers of high quality material with minimum structural defects and good surface quality for use as "buffer" layers prior to the growth of active layers for such devices as FETs and TELDs will eliminate the device performance problems caused by poor and inconsistent substrate quality.

A vapor phase reactor together with its associated gas control system has been constructed which will enable the experimental growth techniques envisaged for this program to be carried out. Preliminary test runs have been performed in order to check the system performance under "normal" operating conditions. That is to determine reactor performance regarding quality and characteristics of the material it can grow before attempting the growth of high resistivity material.

After completion of initial reactor evaluation, experiments on doping with chromium and iron will be carried out. The first series of experiments will be on Cr doping using a liquid CrO_2Cl_2 source.

SECTION II
MATERIAL GROWTH

A. INTRODUCTION

The success of the planar devices such as field effect transistors depends on the capability of growing thin ($\leq$ 1.5 μm) high quality n-layers on substrates which are "inert", i.e., they do not affect the electrical and mechanical properties of thin layers grown epitaxially on them. A major problem is the present unreliability of available substrate material. A possible solution which this project proposes to investigate is the growth of a high quality semi-insulating buffer layer with good surface morphology and high electrical resistivity with the minimum of interaction with the active n-layer subsequently grown on it.

In a previous company sponsored effort, we have established the feasibility of the epitaxial growth of semi-insulating (SI) GaAs. This study established the following points:

1. The background donor density in the reactor must be $\leq 2 \times 10^{15} cm^{-3}$ for chrome doping to be effective.

2. When the background donor density is in the required range, chrome doped SI GaAs layers can be grown. The point contact breakdown voltage of epi-SI GaAs layers is in excess of 1500 V. Measurements carried out at the USAF Avionics Laboratory indicate a resistivity in the 10^6-10^7 ohm cm range.

3. The surface morphology of the chrome doped epi-layers was poor compared to that of epi-n-layers. The reason for this poor morphology is not well understood. Careful adjustment of the CrO_2Cl_2 gas flow resulted in some improvement.

4. The CrO_2Cl_2/H_2 mixture decomposed in the feed tube and the deposit clogged the tube. It was suspected that the H_2 in the mixture reduced CrO_2Cl_2 in the hot part of the feed tube.

5. The 500 ppm CrO_2Cl_2/H_2 mixture was replaced by a 500 ppm CrO_2Cl_2/He mixture. This greatly minimized the decomposition in the feed tube. Furthermore, lower flow rates of the CrO_2Cl_2/He mixtures could be used to obtain SI GaAs. The surface quality also improved slightly. The point contact breakdown was again in excess of 1500 V.

TABLE 1

Data Taken by USAF Avionics Laboratory, Dayton, Ohio

	Type	Resistivity ohm-cm	$n\text{-}cm^{-3}$	$p\text{-}cm^{-3}$	μ_n $cm^2/V\cdot s$	μ_p $cm^2/V\cdot s$
Substrate	n	7.11×10^{7}			1041	
Epitaxial Buffer Layer	n	7.09×10^{7}	1.65×10^{7}	1.58×10^{8}	4202	403

TABLE 2

RCA GaAs FET Performance (with chrome doped buffer layer)

Freq. (GHz)	Linear Gain (dB)	Output Power (mW)	Gain at P_{out} (dB)	Power Added Efficiency (%)	Operating Condition (Source Periphery)
9	5.5	1000	4.3	16.3	Class A (1800 μm)
15	6.7	451	5.2	12.5	Class A (1200 μm)
18	6.3	225	4.5	5.4	Class A (1200 μm)
21	5	186	4.3	11.9	Class A (600 μm)
22	5.6	141	4.8	9	Class A (600 μm)

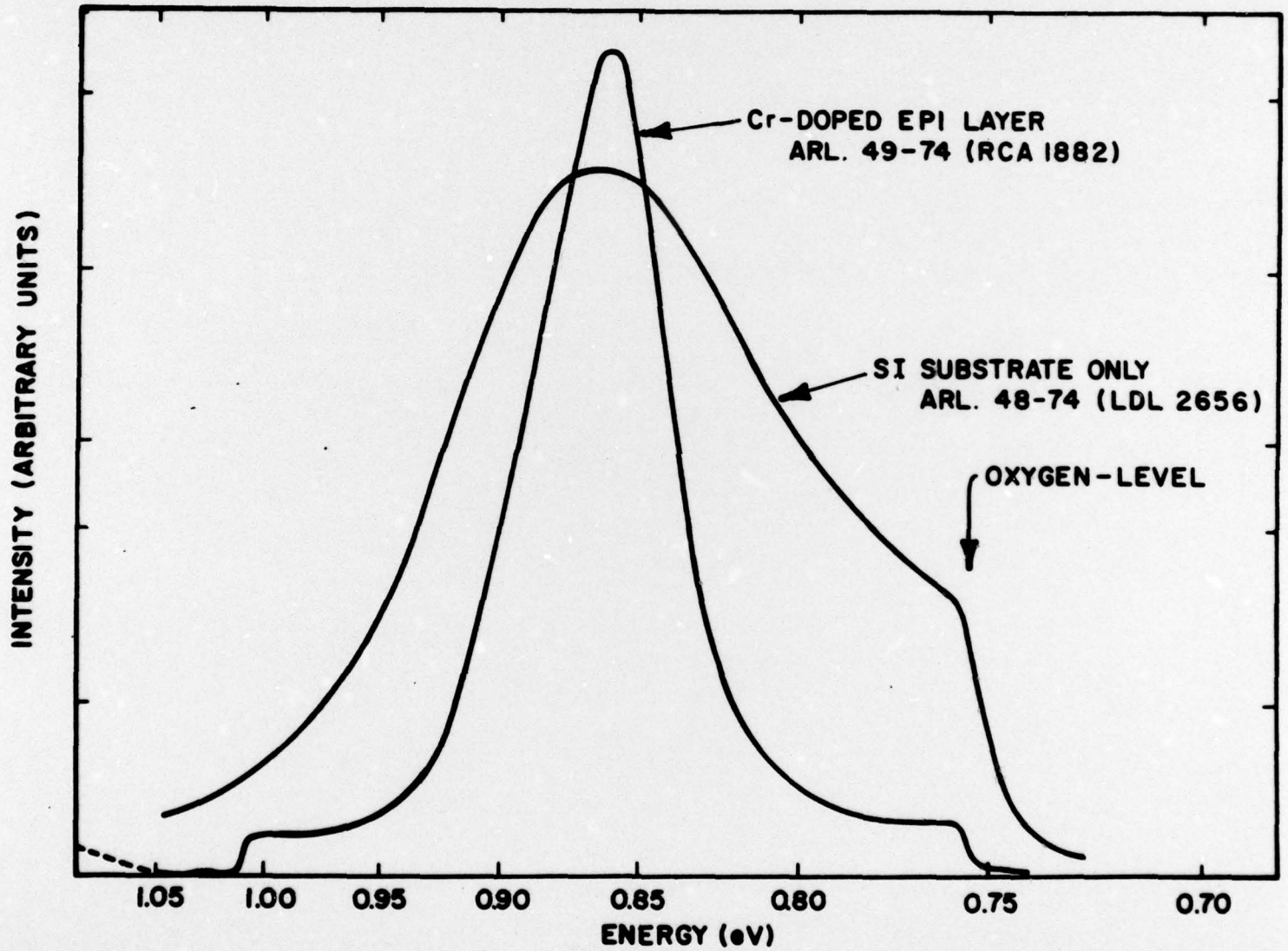


Figure 1. Photoconductivity response of bulk Cr-doped substrate and epitaxial Cr-doped buffer layer. Measurement made at AFAL, Dayton, Ohio.

One chrome doped epitaxial layer was evaluated at the USAF Avionics Laboratory, Dayton, Ohio. In one experiment, an (100) oriented slice from a bulk grown SI GaAs substrate was cut into two pieces. On one, a 5 μm thick epitaxial chrome doped layer was grown and the other was used as a control sample. At the Avionics Laboratory, the electron ahd hole concentration, mobility and IR photoconductivity were measured. Table 1 and Figure 1 illustrate the results. The superior properties of the epi-SI layer are evident. The resistivity of the epi-layer is 10^7 ohm cm. Figure 1 shows that the photoconductive response of the epi-layer is much sharper than that of the substrate. This is believed to be indicative of superior crystal quality.

In the final analysis, the best measure of material quality is the performance of an active device fabricated from it. n^+-n-n_B (buffer) -SI GaAs wafers were grown in-situ for power FET fabrication. n_B denotes an epitaxial Si GaAs buffer layer. The buffer layer thickness was about 5 μm. 1.5 μm gate length FETs were fabricated from this wafer. Table 2 summarizes the results obtained. Note that excellent performance was obtained from a 1.5 μm gate length FET at frequencies as high as 22 GHz [1]. These data indicate that the n-layer grown on an epi-SI buffer layer has excellent electron drift mobility. These results are far superior to those obtained from 0.8 μm gate FETs fabricated from n-layers grown directly on bulk grown SI GaAs substrates.

We have also fabricated planar transferred electron logic devices (TELDs) from a wafer with an epitaxial SI GaAs buffer layer. Post threshold current drops as high as 28% were obtained with three terminal TELDs which is again indicative of higher electron drift mobility in n-layers grown on epitaxial SI GaAs layers.

While the feasibility of growth of SI GaAs layers by VPE and its impact on planar GaAs devices has been established, further research work is necessary.

1. Improvement of surface morphology. The occurrence of microscopic pit like defects must be eliminated. This is necessary to obtain submicron line lengths and features required for microwave and multigigabit rate logic circuits. The reasons for the occurrence of these imperfections is not understood.

2. Optimum conditions for reproducible and repeatable growth of SI GaAs layers have to be established.

3. The use of metallic Cr and its transport by Cl_2 gas may eliminate the need for CrO_2Cl_2 which is highly toxic. This needs to be investigated.

4. Researchers at Fujitsu in Japan have established that using metallic Fe and transporting it to the substrate as $FeCl_2$ can result in high resistivity Fe doped GaAs [2]. They report excellent FET results from wafers with Fe doped buffer layers. Fe doped GaAs with resistivities as high as 10^5 ohm cm have been achieved.

B. REACTOR DESCRIPTION

The vapor phase reactor in which the original experiments were carried out was modified to be more suitable for this particular program. Fig. 2 shows the schematic of the gas handling system. This system has the following capabilities:

1. To operate as a "normal" $Ga/Cl_2/AsH_3$ system employing palladium diffused hydrogen as the diluting gas. It is also planned to add later the ability to substitute ultrapure nitrogen for the hydrogen. This will be of significance when attempting to employ metallic chromium or iron as the doping element.

2. Addition of a third input line for the introduction of a variable composition, chromyl chloride/helium mixture to the reactor input.

3. Addition of hydrogen chloride to the arsine/hydrogen line to both add hydrogen chloride to the reactant gas mixture down stream of the gallium to determine its effect on growth rate, background carrier concentration, etc., and also to etch clean the reactor tube and substrate holder prior to a deposition run.

4. Addition of "n"-type doping gases such as hydrogen sulphide, hydrogen selenide or hydrogen telluride.

5. Inclusion of a line for addition of other doping materials such as diethyl zinc to allow "p" type doping.

6. An ability to introduce chlorine into the "chrome" doping line. When metallic chromium or iron is introduced into the "chrome" feed tube of the reactor this will permit the addition of the respective metallic chlorides into the reacting gas stream. This could be a considerably more convenient and safer method of adding chromium than the use of chromyl chloride.

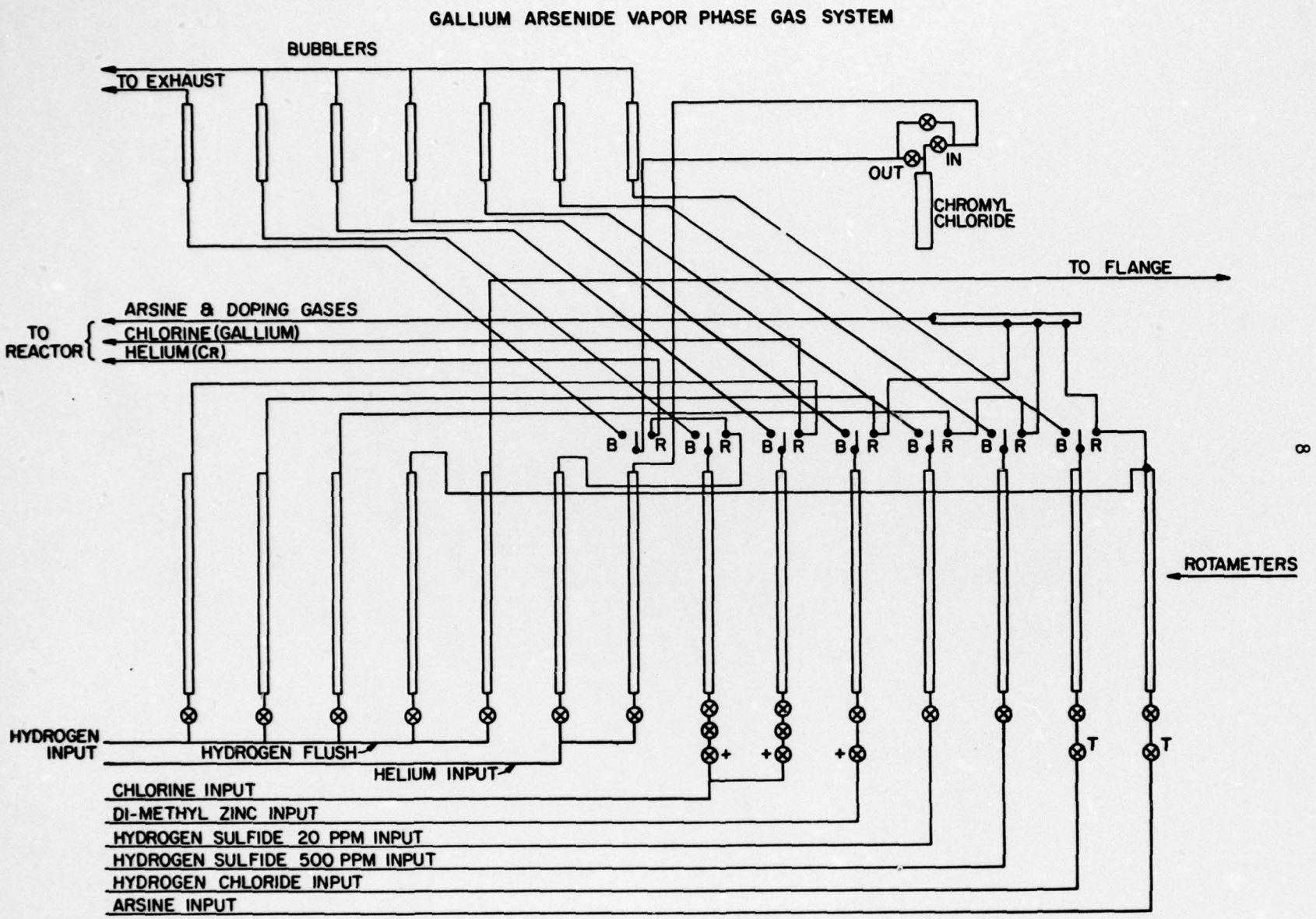


Figure 2. Schematic Diagram of reactor gas handling system.

Fig. 3 is a schematic diagram of the reactor tube and furnace assembly. The reacoor tube configuration has been changed from that previously employed at RCA for vapor deposition of GaAs using the $Ga/HCl/AsH_3$ system. The "side arm" previously used to discharge the waste products of the system has been eliminated.

The reactor now consists of a single straight quartz tube. The exit end of the tube is closed by an end cap with a sleeve extending sufficiently far up the reactor tube so that by sliding the furnace down the tube it can be heated to allow it to be etched clean of reaction products. A slow flow of hydrogen or nitrogen flows upstream between the reactor tube and the sleeve which prevents reaction products from being deposited on the walls of the reactor tube down stream of the end of the sleeve, and restricts them to the interior of the sleeve. The substrate holder is incorporated in the end cap holder-sleeve assembly and extends beyond the end of the sleeve into the deposition region of the reactor. Fig. 4 is a photograph of the reactor.

The elimination of the side arm achieves several objectives:

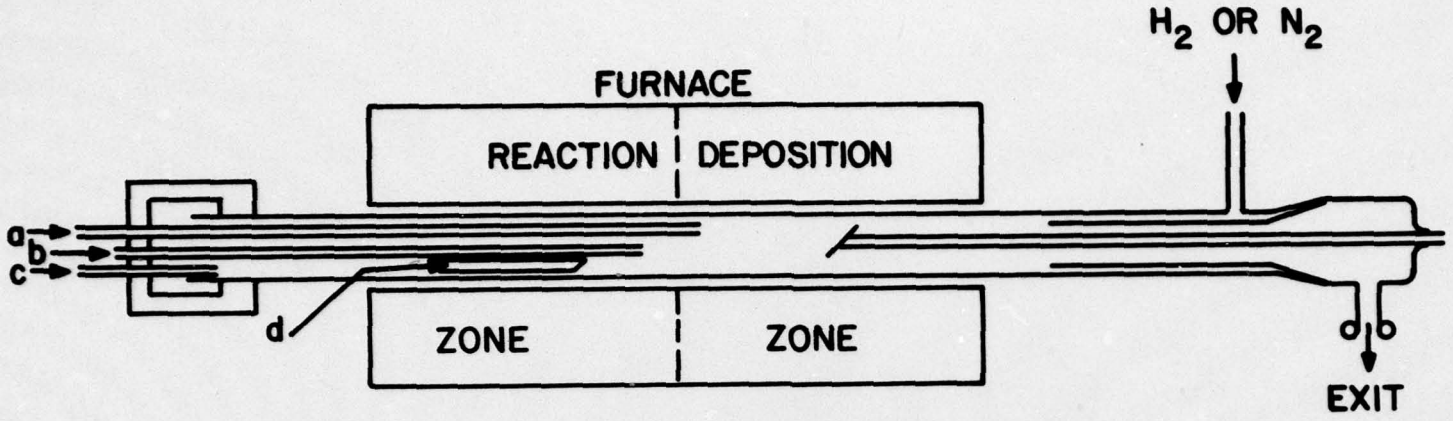
1. It eliminates the necessity to dismantle the assembly to remove the reactor tube for cleaning whenever the performance of the reactor is affected by the deposits of reaction products in the side arm.

2. Reduces the "history" effect, (i.e., change in the background impurity level produced after growth of highly doped layers). This feature is important when attempting to grow a "buffer" layer after a highly doped device wafer has been grown.

3. The reactor tube can be etch cleaned (with hydrogen chloride gas) before every run without dismantling the system.

4. The gas flow pattern is uniform down the tube and is not affected by the reverse gas flow from the loading end of the reactor required to force the reaction products down the side exit arm.

Other features of the reactor assembly are the employment of a sapphire feed tube for the introduction of the chromyl chloride/helium mixture into the reaction zone, the use of a pyrolytic boron nitride sleeve to protect the reactor tube from attack by the chromyl chloride in the reaction zone, and the employment of an annular heat pipe using sodium as the heat transfer medium, as a heating device for the deposition zone.



a CHROME TUBE
b As H_3 TUBE
c Cl_2 OR HCl TUBE
d GALLIUM BOAT

Figure 3. Schematic of reactor tube/furnace assembly.

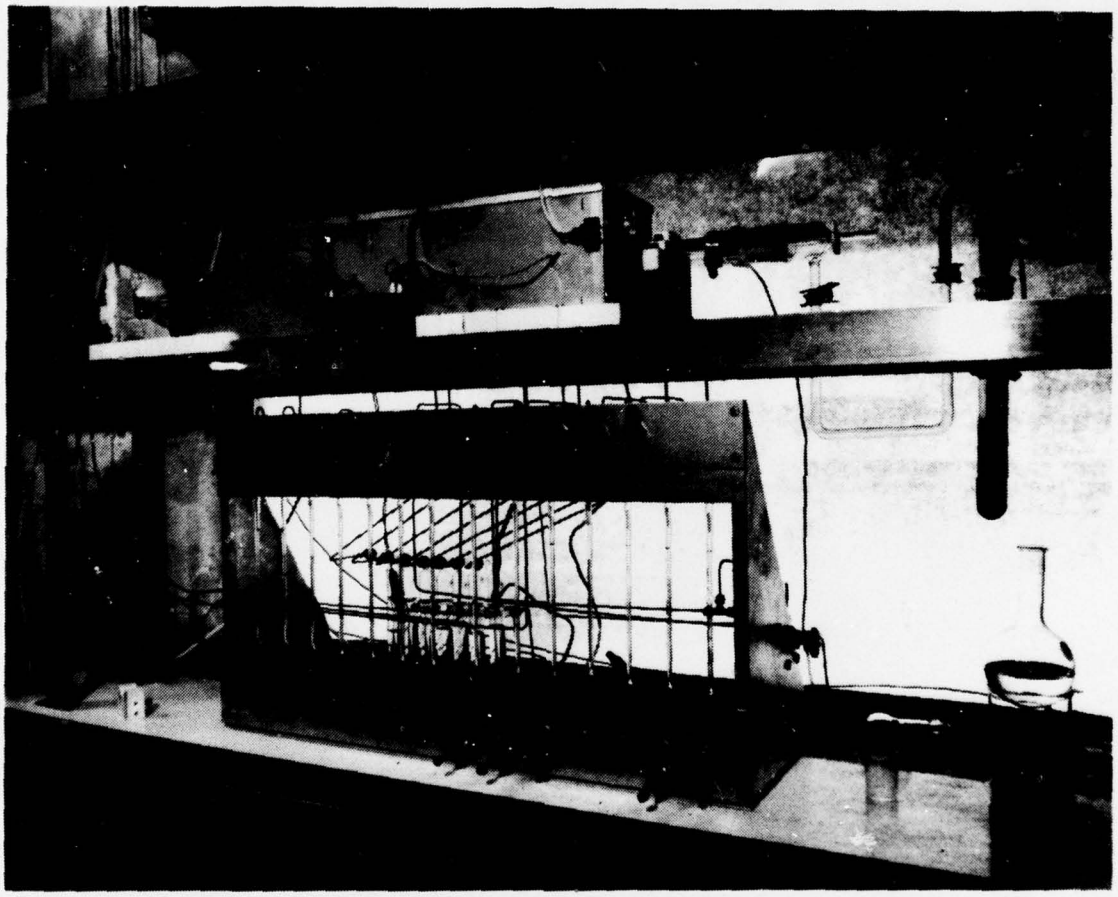


Fig. 4 Photograph of reactor

C. RESULTS

The reactor has been fabricated and is now operational. As discussed earlier, to obtain Cr-doped epitaxial SI layers, it is necessary to ensure that the reactor background is n-type and (N_D-N_A) is less than $2x10^{15}cm^{-3}$. The initial wafers grown in the reactor were found to be of high resistivity even in the absence of added Cr. The reactor was completely leak checked to ensure that there was no oxygen or moisture present. Epitaxial layers were again grown on SI GaAs substrates. The epitaxial layers were found to be of high resistivity with $p>3x10^4$ ohm cm at 300K. The resistivity at 77K was too high to measure. This indicates that the high resistivity is due to some deep level or levels. A sample has been sent to our analysis group for evaluation by SIMS to determine whether it is due to a specific dopant or caused by defects.

The occurrance of high resistivity background layers has been noticed before for growth on high resistivity substrates [3]. The experiments of Cox and DiLorenzo [3] indicate that this is due to the diffusion of acceptors from the substrate or the substrate-epi layer interface. In fact, Cox and DiLorenzo utilize this high resistivity layer as a "buffer" layer for FETs [3]. We have observed such layers previously with the $AsH_3/Ga/Cl_2$ process. The nature of the accpetors is not known and it is suspected that the acceptors are point defects.

In the next quarter, we will continue with our experiments. We will attempt to introduce some H_2S into the gas stream to obtain (N_D-N_A) of $1x10^{15}$ cm^{-3} and then introduce Cr to obtain epitaxial SI GaAs.

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