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Report DECC-61098-007

LOW-COST LIGHT-WEIGHT EFFICIENT 1.5 KW INVERTERS WITH AND WITHOUT OUTPUT TRANSFORMERS

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Final Report

Approved for Public Release;
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Prepared for:

Department of the Army
Mobility Equipment Research
and Development Command
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Optimization efforts were completed on the 1.5 kW inverter described in report DECC-61098-003 (September 1975). A second inverter design was developed; in the second design the output transformer was eliminated. Tests were performed on both the optimized transformer-output inverter and the transformerless-output inverter. Tests included environmental tests on the transformer-output inverter.

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PREFACE

The work reported herin was performed by DECC (Delta Electronic Control Corporation) under contract to the United States Army Mobility Research and Development Command (contract DAAK02-74C-0388). The Contract_ng Officer's Representative was Dietrich J. Roesler at Fort Belvoir, Virginia.

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1.0 INTRODUCTION

1.1 SCOPE

This report discusses the continued effort in the development of low-cost, light-weight, efficient 1.5 kW inverters for use with fuel cell or battery power plants. The inverters are to be capable of supplying 1.5 kW, 0.8 PF (lagging), single-phase, selectable 120 or 240 volt sinewave at selectable frequencies of 60 or 400 Hz.

In the first phase of the 1.5 kW inverter development program (under the contract no. DAAK02-74-C-0388) Delta Electronic Control Corporation (DECC) developed and fabricated two prototype inverters. These were delivered to the U.S. Army Mobility Equipment Research and Development Command (MERADCOM). A pre-prototype inverter fabricated during this program remained at DECC, and was used for further development efforts. The results of the first phase development effort were presented in the final report DECC-61098-003: "Development of a Low-Cost, Light-Weight, Efficient, 1.5 kW Inverter" (September 1975).

The second phase of the program began October 2, 1975, and was divided into two related development programs: (1) Optimization of the original inverter design.

The optimization included the development of a cooling-fan assembly with the associated fan-drive inverter along with other improvements emphasizing the priorities of low production cost, high reliability, maintainability, minimization of size and weight, and efficiency. (2) The development of a second inverter design not utilizing a transformer for the power output.

This interim report describes the development of the optimized inverter and the transformerless-output inverter. Also included are the results of environmental and electrical tests on the inverters.

2.0 INVESTIGATION

2.1 OPTIMIZATION OF THE TRANSFORMER-OUTPUT INVERTER

2.1.1 Design Approach

The optimization investigation consisted of three main efforts: 1) correcting difficulties which had been observed during the testing and operation of the original inverters; 2) performing a detailed stress-analysis reliability investigation (per MIL-HDBK-217B) to determine whether any components suffered unduly high stress levels and to determine what improvement in expected lifetime could be obtained by using higher-cost established reliability components; 3) reviewing future modifications and additions which could result in a more general-purpose device with improved operating performance, although such modifications might involve extensive redesign and mechanical modification.

2.1.2 Known Difficulties

Listed in Table 1 are the major design performance objectives for the inverters. The actual performance of the original transformer-output inverters was discussed in detail in the Final Report DECC-61098-003 and is summarized below:

1) The basic output waveform quality (e.g.

distortion, deviation factor, etc.) and load regulation were well within the design objectives.

2) The efficiency objective of 85% was not achieved, the measured efficiency being 81-82% for the worst case input of 36 Vdc.

3) The original cooling objective was operation with natural convection only. With the achieved 81% efficiency, however, the power dissipation was greater than could be handled without installing massive cooling fins. A relatively small amount of forced-air cooling, however, would permit continuous operation at full power at an ambient temperature of 125°F. Without the aid of forced-air cooling, however, the power was limited to half power (750 watts) under the extreme conditions.

4) Electromagnetic interference (EMI) measurements for conducted emission CE04 (MIL-STD-462) and radiated emission RE02 were performed by MERADCOM. The measured levels, when compared to the limits of MIL-STD-461A showed that a) the conducted EMI was within the specification limit for both the input and output leads except for the frequency range 1-5 MHz where the EMI exceeded the limits by about 15 db, and b) the radiated EMI exceeded the limits by about 25 db over the frequency range 15kHz-5MHz, reaching a maximum excursion of 45 db at about 900 kHz.

TABLE 1

DESIGN OBJECTIVES FOR A 1.5 KW INVERTER

DESCRIPTION	DATA
Power	1.5 kW
Freq In/Freq Out	DC/ 60 or 400 Hz
Voltage In/ Voltage Out	36-60 DC/ 120 or 240 VAC
Power Factor	.8
Phases	1
Frequency Regulation	± .5%
Voltage Regulation	2%
Single Harmonic/ Total Harmonic	3% / 6%
Deviation Factor	6%
Efficiency	85%
Cooling	External cooling air available
Transient Overload	2.25 kVA for 10sec. @ V_{in} =40 V

DESCRIPTION	DATA
Protection	Reverse polarity, short circuit, temperature
Noise	at 10 ft: 68 db max.
EMI	MIL-STD-461
MTBF	5000 hrs.
Temperature Range	Operation: -25°F to +125°F
	Storage: -65°F to +155°F
Altitude	Sea level to 8000 ft.
Humidity	5 to 95%
Housing	Weatherproof
Volume	≤ 1500 cu.in.
Weight	60 lbs max.

2.1.3 Correcting Known Difficulties

2.1.3.1 Providing a Blower Assembly for Cooling. A cooling-fan (blower) assembly was designed and installed in the optimized inverter. The rear panel, which was previously finned for natural convective cooling was redesigned to encompass a housing compartment containing the cooling fan and a transformerless circuit to provide the 60 Hz square waves to drive the blower. The side panels were louvered to provide for exhaust of the cooling air. The resulting package is shown in Figure 1.

2.1.3.2 Increasing Efficiency. The block diagram of the transformer-output inverter is presented in Figure 2. The major power conversion stages are the boost-voltage converter, the power output stage, and the output transformer. The power output stage and output transformer are shown in Figure 3. The power dissipation in transistors Q1-Q4 is divided between switching losses and forward conduction losses. The switching losses are minimized by minimizing the switching times and by using fast turn-off diodes for CR1-CR4. For reactive loads, the transistors must be able to turn on to approximately twice the load current in a very short time to insure a short turn-off time for the diodes (e.g. CR3 turning off when Q2 is turning on). The transistor will thus have full supply voltage

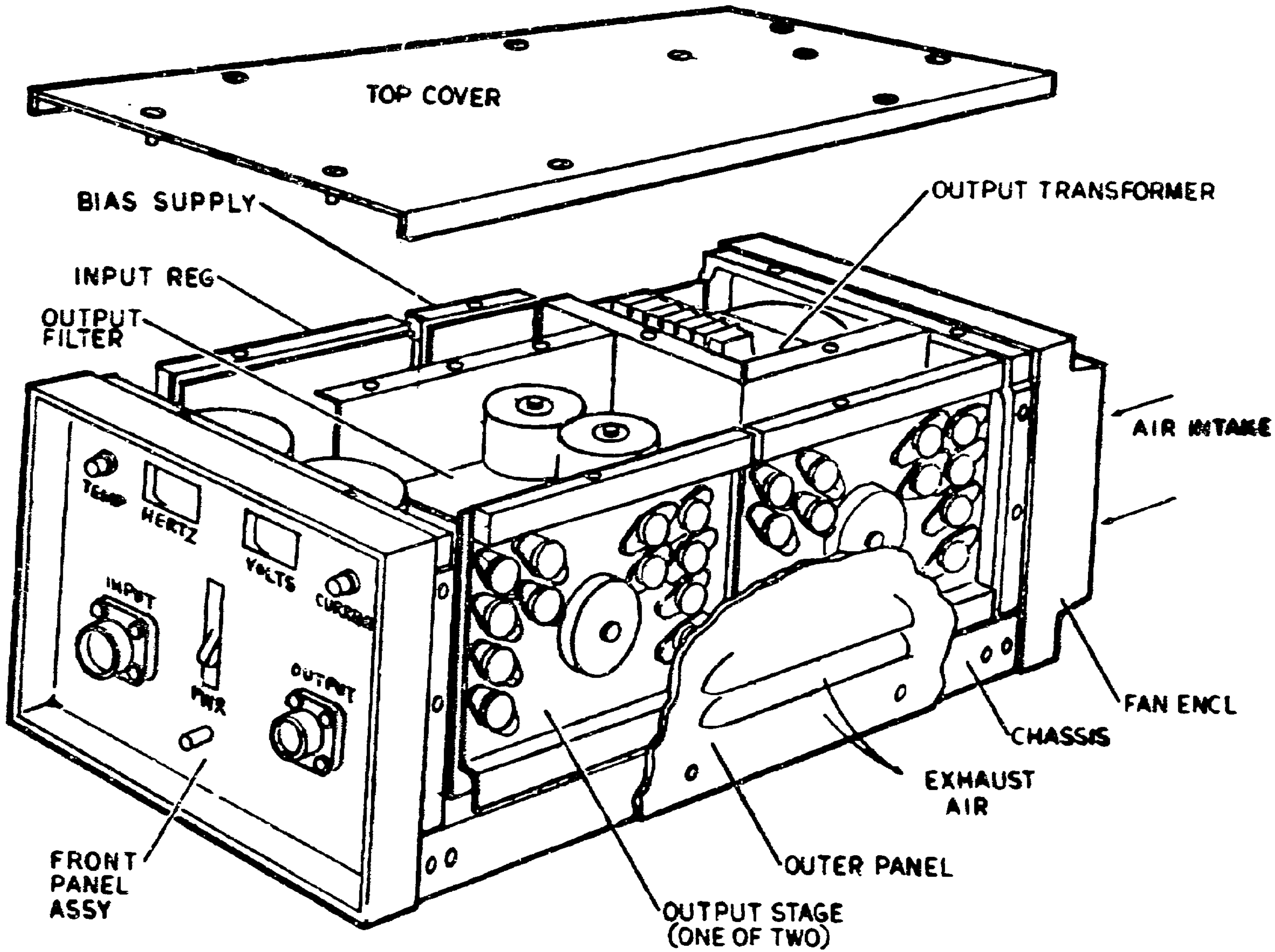


Figure 1. Transformer-Output Inverter

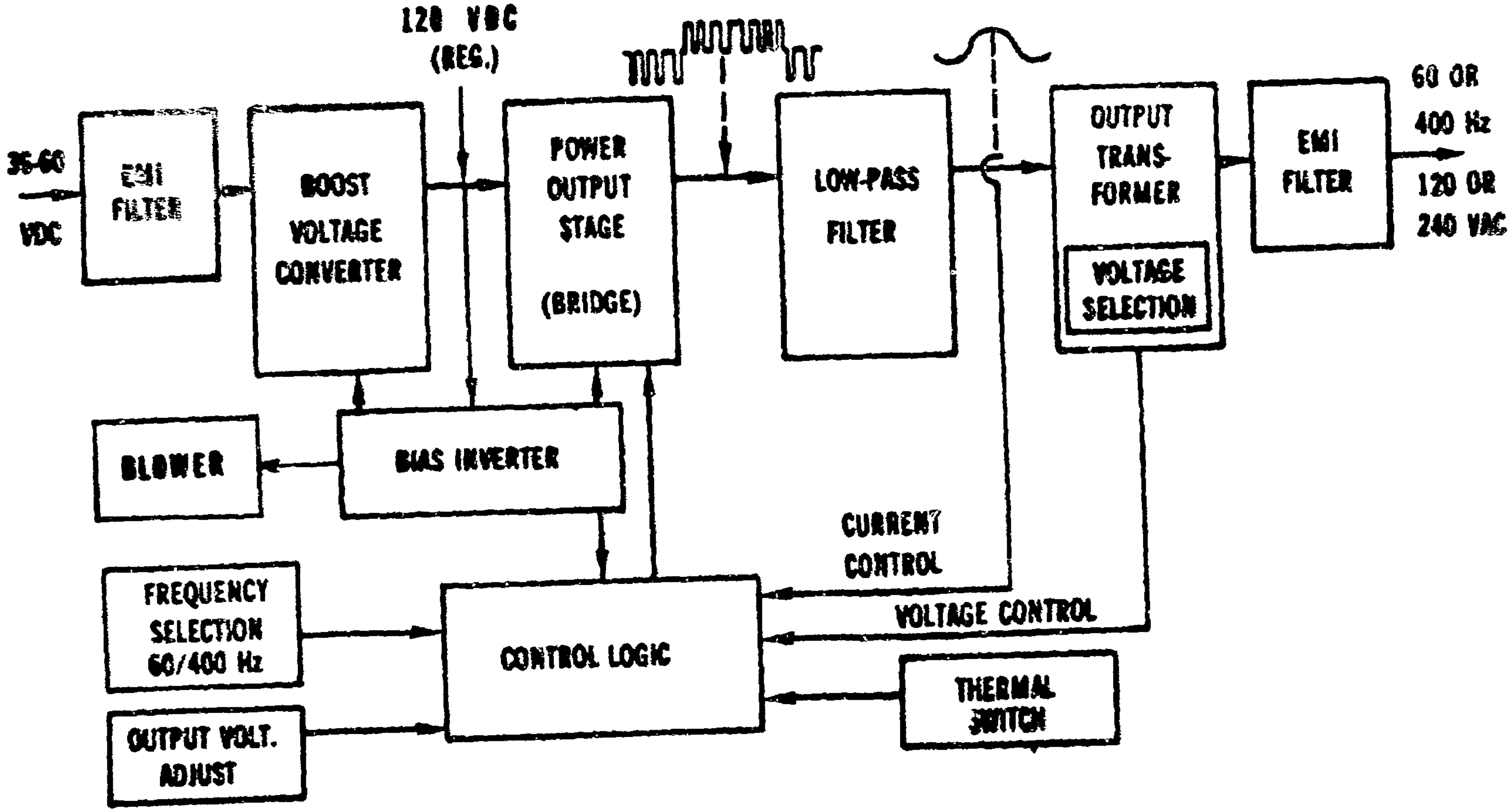


Figure 2. Block Diagram of the Transformer-Output Inverter

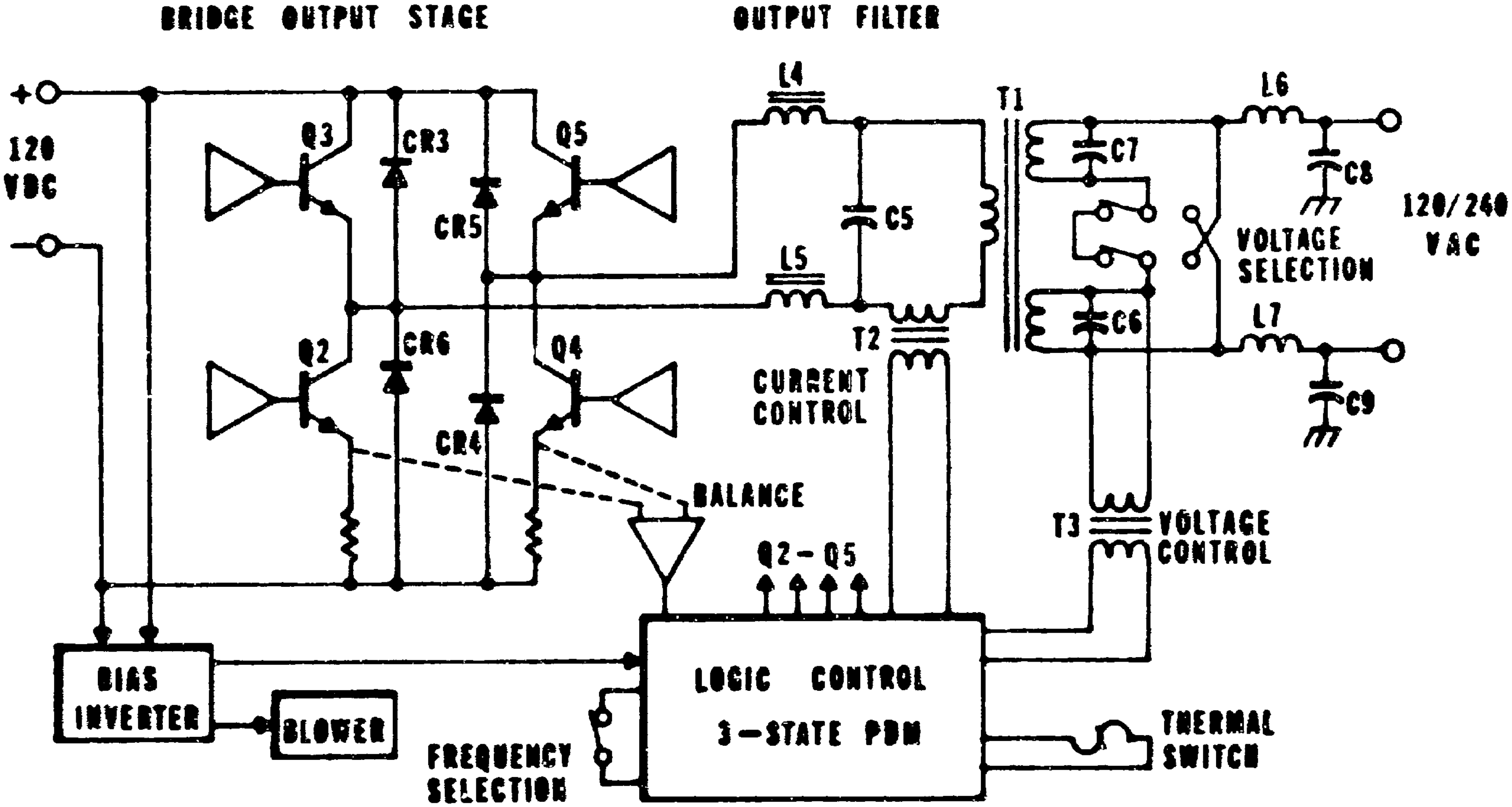


Figure 3. Simplified Schematic of Inverter Section

and a large current and must therefore have a good forward-conduction secondary-breakdown capability.

The forward conduction losses are minimized by using the highest practicable supply voltage. For good switching characteristics, the minimum collector-to-emitter voltages are limited to about one volt. A higher supply voltage results in a lower current demand from the output stage and thus a lower forward conduction loss given the fixed collector-to-emitter voltage.

A survey of switching transistors was made to select a transistor which would provide a reasonable trade-off between performance and cost. The survey revealed that it was possible to use transistors with 300-volt CEO ratings without sacrificing speed or current capability. Consideration of the transistors available indicated further that using several paralleled 10 amp transistors in TO-3 type packages yielded improvements over a single transistor. The improvements included current gain, power capabilities, thermal resistance, and cost. Table 2 presents a comparison of the characteristics of four paralleled Solitron SDT12303 transistors and one Power Tech PT-3512 transistor. The Solitron SDT12303 transistor was chosen because of its excellent characteristics (see Table 2) and its low cost. The

TABLE 2

PERFORMANCE COMPARISON BETWEEN
ONE POWERTECH PT-3512 TRANSISTOR AND
FOUR SOLITRON SDT12303 TRANSISTORS

RATING	PT -3512	SDT12303 (4)
V_{CEO}	325 V	300 V
V_{EBO}	10 V	5 V
I_C peak	70 A	80 A
I_C dc	30 A	40 A
Power dissipation @T_c=100°C	200 W	500 W
Thermal resistance	.5°C/W	.2°C/W
Max. junction temp.	200°C	200°C
h_{FE}@30 A	10 min.	
@40 A		10 min.
@70 A	5 min.	
@80 A		5 min.
$V_{sat.}$ (30A, 3A base)	.6V max.	Approx. .8V max.
f_t	Approx. 10MHz	Approx. 25MHz
t_r	.5 microsec.	.2 microsec.
t_s	1.2 microsec.	1.2 microsec.
t_f	.5 microsec.	.2 microsec.
I_{SB}@300V, 100 microsecs.	30 A	56 A
Price	$130 (1 at 25-piece price)	$35 (4 at 100-piece price)

TRW SVT300-10 was also tested, but although it is slightly faster than the SDT12303 and has a slightly better secondary breakdown capability, it is also more than four times the cost. The original inverters had 2N6250 transistors in the output stage. The 2N6250 transistors are considerably slower than the SDT12303 and about equal in cost and power capability. The SDT12303 is manufactured for high reliability.

Using the 300 volt transistors, it was originally thought that the output stage could be operated reliably at 200 volts supply voltage. At 200 volts, the required currents in the output stage would be only 60% of the currents required at the 120 volts of the prototype inverters. Power loss in the diodes and transistors at 200 volts was estimated to be about 70% of the loss at 120 volts (switching loss included). The increase in the overall efficiency of the output stage would be about 2%.

There are, however, two major difficulties in increasing the supply voltage to 200 volts. Firstly, with the boost type voltage converter used in the inverter, a boost from 36 volts to 200 volts is somewhat difficult from the control standpoint and is at least 1% less efficient than boosting to 120 volts (see Figure 4). Secondly, if operation below -25°F is desired, it is

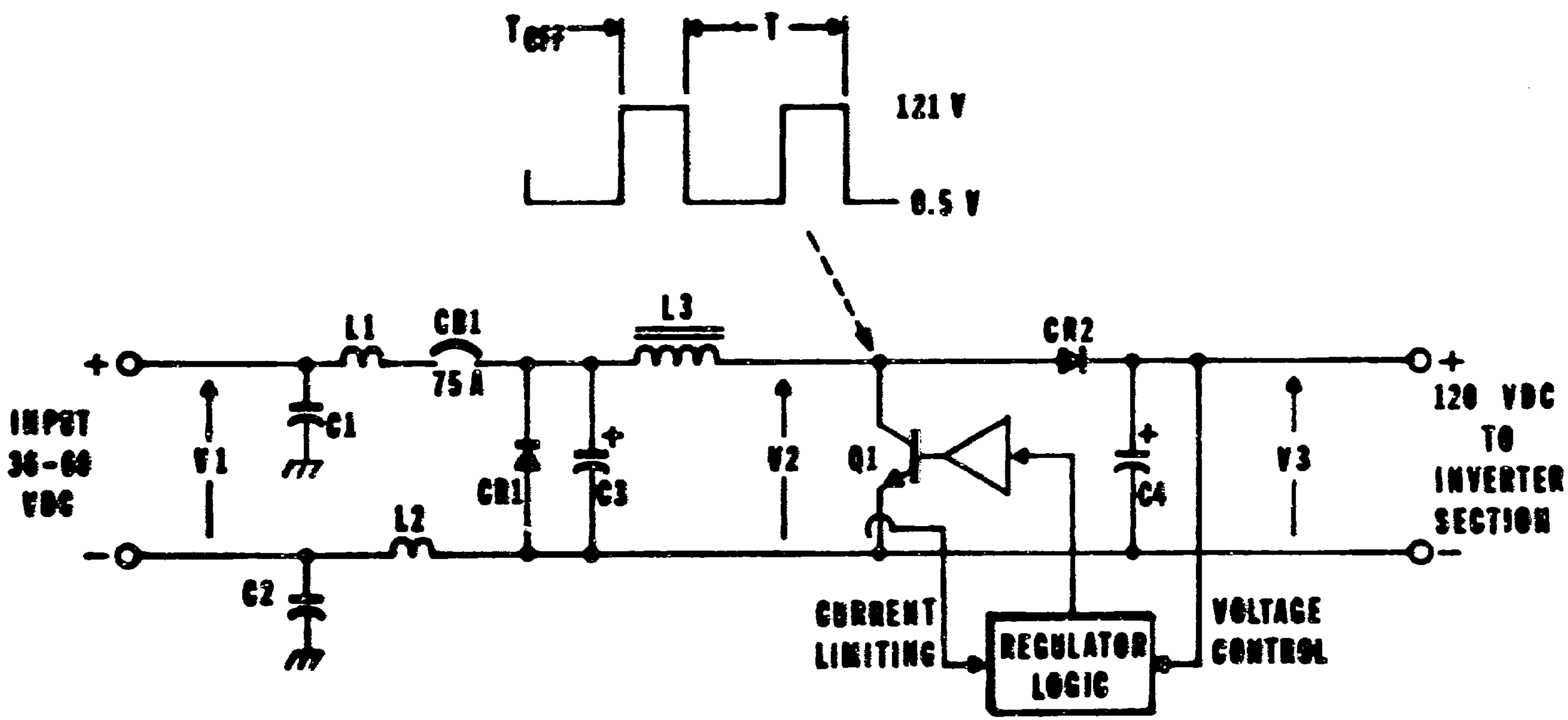


Figure 4. Simplified Schematic of Boost Regulator

necessary to use a type of filter capacitor (e.g. C4 in Figure 4) which is presently not available at voltage ratings above 150 volts. Because of these difficulties, the output stages of the optimized inverter have been designed to operate from a source voltage near the original 120 volts. Some benefit was derived from increasing the voltage to 130 volts.

The efficiency of the inverter was also increased 0.5-1.0% by operating the output stage with a little larger modulation index and allowing a slight increase in distortion (peak clipping) when the unit is operated at 127 Vrms output. A further slight increase in efficiency was obtained by operating the output transformer (T1 in Figure 2) at a slightly higher flux density resulting in an improved trade-off between winding losses and core losses.

2.1.3.3 Improving EMI. The sources of conducted EMI in the original inverters were well understood and measures were taken to reduce the conducted EMI in the optimized inverters. Changes in the design of the high current inductors reduced the radiated emission from the inductors by approximately 14 db. The addition of the louvres for cooling-air exhaust, however, caused some (about 3 db) increase in the local field radiation levels near the louvres.

2.1.4 Stress Analysis

A detailed part-by-part stress analysis of the optimized design was performed to reveal any components which might experience excessive stress, to reveal which components had the greatest effect on reliability and to determine the improvement factor of replacing some of these components with high-reliability components, and to determine the range of expected lifetimes possible using all commercial-grade components or using JAN, MIL, and M-grade established-reliability components where available.

The analysis uncovered a few components which were being unnecessarily highly stressed, and these components were replaced with components having higher ratings to improve the reliability of the unit.

The overall calculation of expected lifetime was performed for the case of all commercial-grade components and the case of JAN, MIL, and M-grade established reliability components being used wherever possible. The expected mean time between failures with all commercial components was calculated to be 3736 hours. The mean time between failures with all possible higher reliability components was calculated to be 15,916 hours.

2.2 DESIGN OF THE TRANSFORMERLESS-OUTPUT INVERTER

The design of the transformerless-output inverter involved several design problems in addition to those of the transformer-output inverter discussed above: (1) Since output isolation is no longer provided by an output transformer, the power output stages must themselves be isolated electrically except for enough capacitance to the chassis (ground) to satisfy EMI filtering requirements; (2) An input power converter becomes necessary to provide the isolated dc voltage to the inverter stage; (3) the 120/240 Vac selection can not be made by series or parallel connection of the windings of an output transformer; (4) Control signal communication to and from the output stages must be accomplished in an isolated fashion (e.g., optical or high-frequency coupling).

A block diagram of the transformerless-output design is presented in Figure 5 and a simplified circuit diagram is given in Figure 6. A dc-to-dc converter circuit provides two isolated sources of 200 Vdc, one for each of two output stages. The converter circuit is similar to the boost regulator circuit utilized in the transformer-output inverter with the exception that the flyback energy is magnetically coupled to the isolated outputs. A transformer-coupled boost converter circuit usually has an input ripple

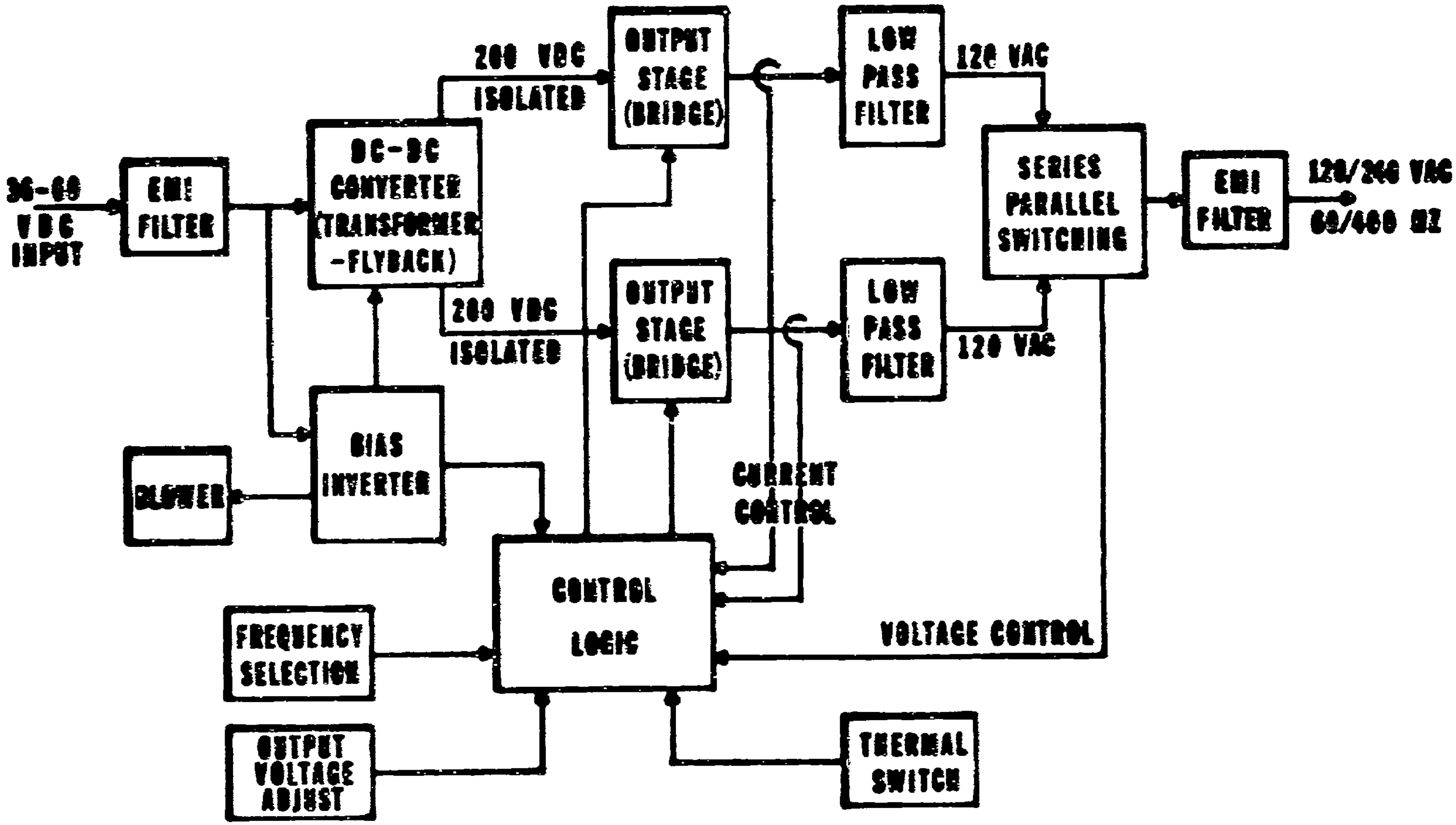


Figure 5. Block Diagram of Transformerless - Output Inverter

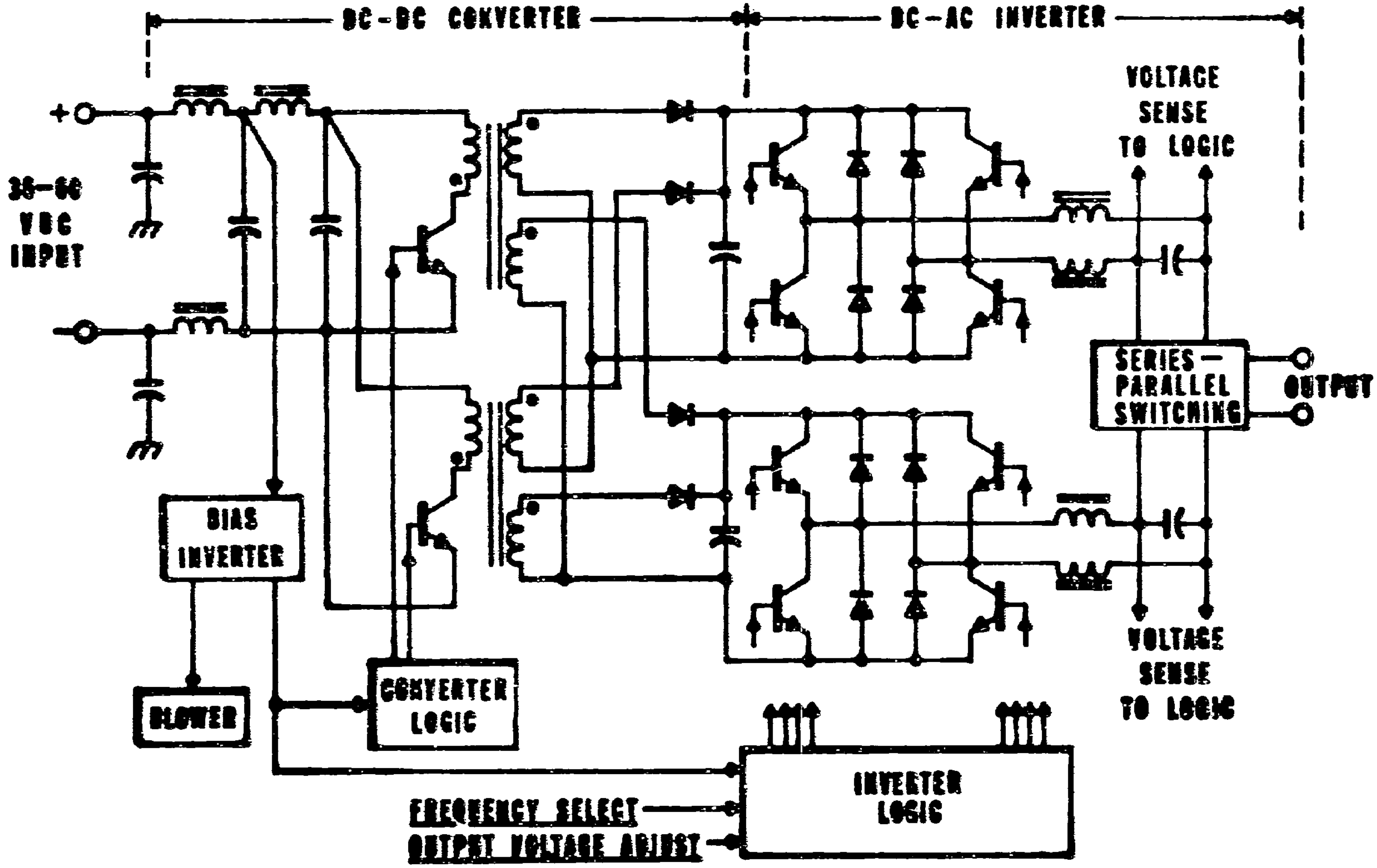


Figure 6. Simplified Schematic of Transformerless-Output Inverter

current which is large compared with the direct boost converter used with the transformer-output inverter. For this reason, the two transformer-coupled converter circuits are operated 180 degrees out-of-phase to reduce the filtering requirements. The transformer-coupled boost circuit has an efficiency of 89% typical, 4% less than the direct boost circuit.

Two separate bridge-connected output power stages are employed. Each produces a 34 kHz three-state, pulse-duration-modulated output waveform which, when filtered by a low-pass filter, becomes a 120 V sinusoidal waveform of low distortion (< 2% THD). The outputs are paralleled for the 120 Vac operation and are connected in series for the 240 Vac operation. A bias inverter circuit operates from the input voltage and provides the necessary power to the logic control circuits; it also provides 400 Hz power to operate the blower (two-phase 400 Hz blower). Drive signals are transformer coupled to the output stages and consist of 200 kHz switched square-waves.

The three-state pulse-duration modulation scheme is the same as that used in the transformer-output inverter. The reference sinewave source for the transformerless inverter, however, utilizes a crystal oscillator and count-down logic for digital generation of the reference sinewave.

A sinewave oscillator is a simpler circuit. It requires, however, more expensive components than digital generation to meet the ±0.5% frequency stability over the operating temperature range. In additiion to the 60 and 400 Hz frequencies, 50 Hz was included as a selectible frequency option. The 50 Hz capability is available without any penalty in power or weight.

As can be seen in Figure 7, except for the front panel and controls, the packaging concept used for the transformerless inverter was different from that used for the transformer output inverter. For the transformerless-output inverter, the power transistor circuit assemblies were mounted laterully between the sides of the unit. The sides are double walled, permitting cooling air to flow external to the circuitry. This double-box construction maintains a reasonable environmental separation between the cooling air and the circuitry and reduces the high-frequency electromagnetic radiated emissions.

In an attempt to minimize production costs, the inverter was designed with a single mother-board printed circuit control assembly. The power transistor circuit assemblies plug directly into receptacles on the mother board.

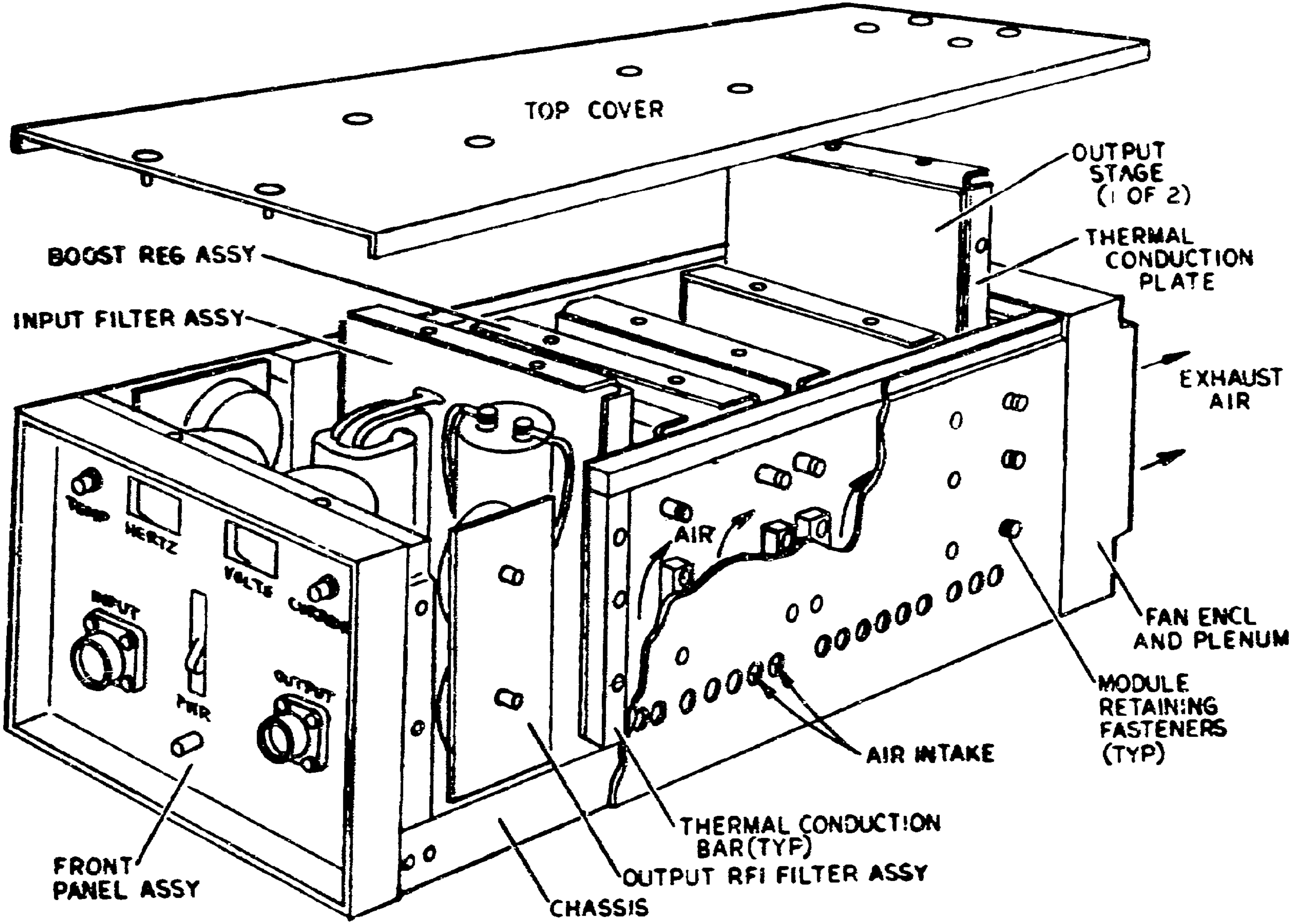


Figure 7. Transformerless-Output Inverter

3.0 RESULTS

3.1 TESTS

A set of test procedures was written for evaluating the transformer and transformerless-output inverters. The procedures include both electrical and environmental tests. The tests are described in Appendix A. Test results for one optimized transformer-output and one transformerless-output inverter are included in Appendix B. The results are summarized and evaluated below.

3.2 GENERAL RESULTS

Although the same external package was used for both inverters, the internal structure of the transformerless-output inverter was entirely different from that of the transformer-output inverter. The design was to result in improved isolation between the cooling air and the electronics and in reduced production costs. Although the final package did isolate the electronics environmentally, it presented other problems. Although the mother-board concept might reduce the cost of the inverter on a production basis, the actual package was impractical for development purposes. The inaccessability of some of the circuitry on the mother-board and power transistor circuit boards made trouble-shooting and circuit evaluation extremely difficult, and further design work would be required to modify the package for reasonable maintainability.

The transformerless-output inverter was, however, made operable and ambient temperature tests were performed on it to evaluate its electrical performance. No environmental tests were performed. From package design considerations, however, the transformerless-output inverter should perform even better than the transformer-output inverter under conditions of extreme temperature and humidity.

Since the original 85% efficiency objective was for inverters without fans, the 30 watt fan power has been subtracted from the measured input power in calculating the efficiencies in Tables 3 and 4.

TABLE 3. Test Summary; 1.5 kW Inverter with Output Transformer

Description of Test			Test-Adjusted for Fan -25° F	Test-Adjusted for Fan 70° F	Test-Adjusted for Fan 125° F	Objective
EFFICIENCY 60Hz, 120V	36-45Vdc	Resist Half Load	----	----	----	85%
		Resist Full Load	84.7 %	84.2%	82.2%	
		PF 0.8 Full Load	----	81.0%	----	
	60Vdc	Resist Half Load	----	----	----	85%
		Resist Full Load	86.1%	85.0%	82.8%	
		PF 0.8 Full Load	----	----	----	
EFFICIENCY 400Hz, 120V	36-40V	Resist Half Load	----	86.3%	----	85%
		Resist Full Load	84.[illegible]%	84.4%	83.1%	
		PF 0.8 Full Load	----	83.0%	----	
	60Vdc	Resist Half Load	----	----	----	85%
		Resist Full Load	86.6%	85.4%	83.9%	
		PF 0.8 Full Load	----	----	----	
THD 400 Hz, 120V,	36-40Vdc	Resist Full Load	1.75%	1.7%	2.6%	6%
		PF 0.8 Full Load	1.25%	----	----	
	60Vdc	Resist Full Load	1.45%	1.35%	1.7%	6%
		PF 0.8 Full Load	1.0 %	----	----	
No Load Losses		36-45 Vdc	----	43 W	----	----
		60 Vdc	----	55 W	55-61 W	

Frequency Regulation	0.2% with input, load 1% with temperature	0.5%
Voltage Regulation	0.3% with input, load 1% with temperature	2%
MTBF*	3736 hrs calculated	5000 hrs
Volume	1517 in ^{3}	1500 in ^{3}
Weight	54 lbs	60 lbs
Cost **	$1000	$1000

*See Appendix D
**See Appendix E

TABLE 4. Test Summary; 1.5 kW Inverter without Output Transformer

Test	Results (Adjusted for Fan)	Objective
Efficiency		
60 Hz, 240V 36-45 Vdc input Full load resistive	84%	85%
60 Hz, 240V 60 Vdc input Full load resistive	85%	85%
400 Hz, 120V 36-45 Vdc input		
Full load resistive	82%	85%
Half load resistive	84%	85%
400 Hz, 120V 60 Vdc input Full load resistive	86%	85%
THD		
400 Hz, 120V Full load resistive	1.9%	6%
No load losses	77 W	
Frequency regulation with input and load	0.2%	0.5%
Frequency regulation with temperature	0.1%	0.5%
Voltage regulation with input and load	0.3%	2%
Voltage ragulation with temperature	1%	2%
Volume	1517 in^3	1500 in^3
Weight	54 lbs	60 lbs
MTBF*	5736 hrs calc.	5000 hrs
Cost**	$1000	$1000

*Comparable to the transformer-output inverter
**See Appendix E

4.0 FUTURE EFFORT

The third phase of the inverter development program will involve efforts in several directions.

The development of the two 1.5 kW inverters is the first step in a MERADCOM program to develop a family of low-cost, light-weight efficient inverters having single-phase and/or three-phase outputs at power levels between 1.5 kW and 10 kW. The voltage connections for the family are shown in Table 5.

During the third phase of the development program a basic electronic design will be developed for the complete family. The use of common logic and power-stage assemblies for the entire family will be a primary goal.

A packaging concept for the complete family will also be developed. The use of separate plug-together packages for the input-power conditioner and the dc to ac inverter will be investigated. This concept allows a standard inverter package to operate from different input power sources such as batteries and fuel cells by changing power conditioner sections.

Further evaluation of the transformerless-output

TABLE 5.

Standard Voltage Connection

kW Rating	Single Phase			Three Phases	
kW	120 V 2 wire	240 V 2 wire	120/240 V 3 wire	120/208 V 4 wire	240/416 V 4 wire
1.5	X	X			
3	X	X	X	X	
5	X	X	X	X	
10	X		X	X	

concept will be performed. Many of the problems with the original transformerless-output inverter arose from the attempt to build it in the same package as the transformer-output inverter. The use of two-state rather than three-state modulation in a transformerless-output inverter will be evaluated. This will result in some simplification of the circuitry while requiring additional output filtering.

The circuitry developed during phase three will be bread-boarded and evaluated for performance. A package for a 1.5 kW inverter will be designed according to the packaging concept developed. The package will be built and evaluated for size, weight, cooling and cost. A complete pre-prototype 1.5 kW inverter will be constructed and thoroughly evaluated by DECC. Any corrections or modifications arising from the evaluation will be incorporated into the design for two 1.5 kW inverters which will be delivered to MERADCOM.

APPENDIX A

TEST PLAN

1.0 INTRODUCTION

1.1 PURPOSE

The purpose of this test plan is to evaluate the ability of 1.5 kW inverters developed for the U. S. Army Mobility Equipment Research and Development Command (MERADCOM) to perform as required by MERADCOM Purchase Description EED 74021301.

1.2 USE

The tests to be performed and the order of performance are presented in section 2.0 of this test plan. The test descriptions and criteria are presented in section 3.0. Sample data sheets are presented in section 4.0.

2.0 TEST SEQUENCE

2.1 GENERAL

The apparatus shall be tested in the sequence given below at the given parameters using the referenced test methods. Figure A1 shows the test set-up. Table A1 lists the performance test equipment specifications. Table A2 lists the environmental test equipment. The test loads are defined as the fraction of full power, followed by the type of load, R standing for resistive and X standing for reactive with 0.8 PF (lagging); e.g. ½R means half power resistive (750W), and 1X means full power reactive (1875 kVA) for the given output voltage and frequency. The external output-voltage adjustment may be adjusted only after a change in the output voltage or frequency selection. To adjust the voltage, operate the apparatus at the selected voltage and frequency, 45 Vdc input, 1R load and an ambient temperature of 78±10°F for at least 15 minutes. Adjust the voltage to the nominal voltage ± 0.2%.

2.2 ASSEMBLY

Perform paragraphs 3.1 and 3.2.1 as appropriate during fabrication and assembly. Perform paragraph 3.2.3 after final assembly.

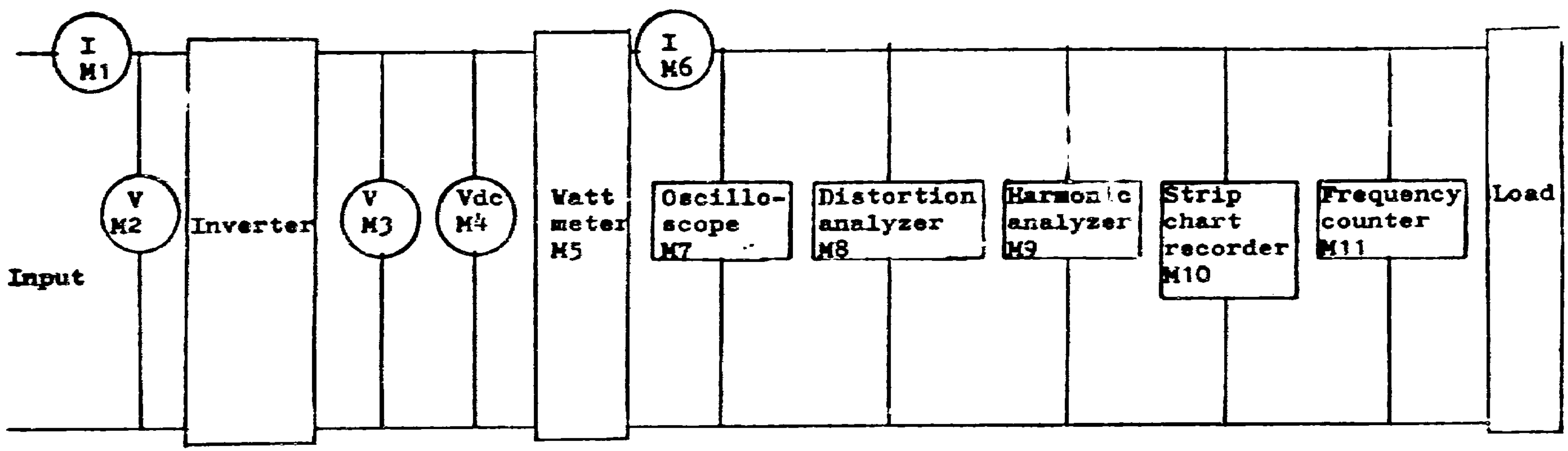


Figure A1. Test Set-Up

Table A1. Performance Test Equipment

Note: The instruments listed here are adequate for the required applications. Equivalent equipment may be substituted.

Current meter	M1, M6	Digital voltmeter with 0.3% accuracy (e.g. Dana 4200) and calibrated shunt with 0.3% accuracy
Voltmeter	M2, M3	Digital voltmeter, 0.3% accuracy
DC voltmeter	M4	Digital voltmeter (e.g. Dana 4200) with ac voltage rejection filter (e.g. White Instrument Company model 3702) or high-ac-rejection digital voltmeter (e.g. Fluke 8300A)
Wattmeter	M5	60 and 400 Hz calibration, e.g. Weston 310
Oscilloscope	M7	0-15 MHz minimum bandwidth, with camera, e.g. Tektronix 543
Distortion analyzer	M8	0-100 kHz, e.g. HP331A
Harmonic analyzer	M9	0-50 kHz, e.g. HP302A Wave Analyzer
Strip chart recorder	M10	Adjustable speed (¼"-2" per second range), 2½" chart width minimum, e.g. Visilight 5M21
Frequency counter	M11	0.05% accuracy, e.g. Ballantine 5500A

Table A2. Environmental Test Equipment

Environmental chamber	Controlled temperature: -25°F to 125°F
Environmental chamber	Controlled temperature: 68°F to 125°F Controlled humidity: 90-98% Controlled pressure: 0-50,000 ft. altitud
Shake table	2.5g, 60 lb mass, 7-200 Hz
EMI equipment	As required by MIL-STD-462, CE03 and RE02
Tunable sound pressure detector	Sensitive to 40 db (referenced to 0.0002 microbars) over the range 75-9600 Hz

ENVIRONMENTAL TESTS

Test Description	Test Paragraphs	Input Volt.	V Out Set	f Out Set	Load
HIGH TEMPERATURE (V & f, efficiency, THD)	3.3.1	36	120	60	1R
		45			
		60			ØR
LOW TEMPERATURE (V & f, efficiency, THD)	3.3.2	36			1R
		45			
		60			ØR
400 Hz. Repeat the above tests at 400 Hz.					
TEMPERATURE, HUMIDITY, ALTITUDE	3.3.3	—	—	—	—
CORROSION	3.2.2	—	—	—	—
INSULATION RESISTANCE	3.2.3	—	—	—	—
VIBRATION	3.3.4	—	—	—	—
SHOCK	3.3.5	—	—	—	—

ELECTRICAL PERFORMANCE TESTS

Test Description	Test Paragraphs	Input Volt.	V Out Set	f Out Set	Load
ELECTRICAL PERFORMANCE					
V & f, THD, DC	3.4.1, 3.4.3.1, 3.4.3.4	45V	120	400	ØR
V & f, THD	3.4.1, 3.4.3.1				½R
V & f Efficiency, THD, Distortion, Waveform, DC	3.4.1, 3.4.2, 3.4.3.1, 3.4.3.2,3.4.3.3,3.4.3.4				1R
					1X
V & f, Efficiency, THD	3.4.1, 3.4.2, 3.4.3.1	36			1R
		60			
Stability, transient	3.4.4	45			
Polarity Rev.	3.4.6	45			
Overload	3.4.7	45			
Improper Input	3.4.8	——			1R
Hi-imped. source	3.4.9	——			
Audible noise	3.5	45			

Test Description	Test Paragraphs	Input Volt.	V Out Set	f Out Set	Load
V & f, THD, Efficiency	3.4.1, 3.4.2, 3.4.3.1	45	120	60	1R
Distortion, Waveform, DC	3.4.3.2, 3.4.3.3, 3.4.3.4				
V & f, THD, DC	3.4.1, 3.4.3.1, 3.4.3.4				1X
V & f, THD, DC	3.4.1, 3.4.3.1, 3.4.3.4				ØR
V & f, THD	3.4.1, 3.4.3.1	60			
V & f, THD		36			1R
		45			
Stability, transient	3.4.4				
EMI	3.4.5				
Audible Noise	3.5				
V & f, THD, DC	3.4.1, 3.4.3.1, 3.4.3.4		240	60	
V & f, THD	3.4.1, 3.4.3.1	36			
		60			
DC	3.4.3.4	45			ØR
					1X
V & f, THD, DC	3.4.1, 3.4.3.1, 3.4.3.4			400	1R

Test Description	Test Paragraphs	Input Volt.	V Out Set	f Out Set	Load
V & f, THD	3.4.1, 3.4.3.1	36	240	400	1R
DC	3.4.3.4	60			
		45			ØR
					1X

3.0 TEST METHODS

3.1 PRE-ASSEMBLY TESTS

Prior to assembly into the inverter, all power coupling transformers shall be tested for insulation resistance:

Winding to core: At 1700 Vdc, the leakage current between any one winding and the core shall be less than 100 microamps.

Winding to winding: At 1700 Vdc, the leakage current between any pair of windings shall be less than 100 microamps.

3.2 INSPECTION

3.2.1 DURING ASSEMBLY. Inspect all assemblies for workmanship and general appearance.

3.2.2 CORROSION. Inspect for evidences of corrosion or other material deterioration or distortion. Record description of any such deterioration.

3.2.3 INSULATION RESISTANCE. Short the output leads together. Short the input leads together. Measure the resistance between the input leads and the chassis at 200±10VDC. The resistance shall exceed 200 k ohm (less than 2 mA). At 1000±50Vdc measure the resistance between the input leads and output leads. The resistance shall exceed 1 M ohm (less than 1 mA). At 1000±50Vdc, measure the resistance between the output leads and the chassis. The resistance shall exceed 1 M ohm (less than 1 mA).

3.3 ENVIRONMENTAL

3.3.1 HIGH TEMPERATURE. With a 1R load, turn the apparatus on and soak it at an ambient temperature of 125±5°F for 2 hours. During the soak, monitor the operation of the unit every 15 minutes for the following failures:

Overtemperature alarm
Decrease of output voltage from initial value by more than 5%
Increase in input power over initial value by more than 3% (at constant output power)

Turn the apparatus off for one minute. Turn the apparatus back on and perform the tests 3.4.1, 3.4.2, and 3.4.3.1 under all conditions specified.

3.3.2 LOW TEMPERATURE. With the apparatus off, decrease the ambient temperature to -25°F. Soak at -25±5°F for 3 hours. Turn the apparatus on and perform the tests of 3.4.1, 3.4.2, and 3.4.3.1 under the specified conditions.

3.3.3 TEMPERATURE-HUMIDITY-ALTITUDE. Place the apparatus in a temperature-humidity-altitude chamber. With the unit non-operative, reduce the chamber pressure at a rate of 1000-1500 ft/min. to 50,000 feet altitude, allowing corresponding temperature decrease. After 30 minutes, increase the chamber pressure to 8000 feet altitude and and the temperature to 95°F. Operate the apparatus for 15 minutes at 60 Hz, 120V and load .9R and perform test paragraphs 3.4.1, and 3.4.3.1. Increase the chamber pressure to 5000 feet altitude and increase the temperature to 107°F. Operate the apparatus for 15 minutes at 60 Hz, 120 V and load 1R and perform test paragraphs 3.4.1 and 3.4.3.1. With the apparatus non-operative, subject the apparatus to 5 of the 24-hour temperature-humidity-cycles shown in Figure A2.

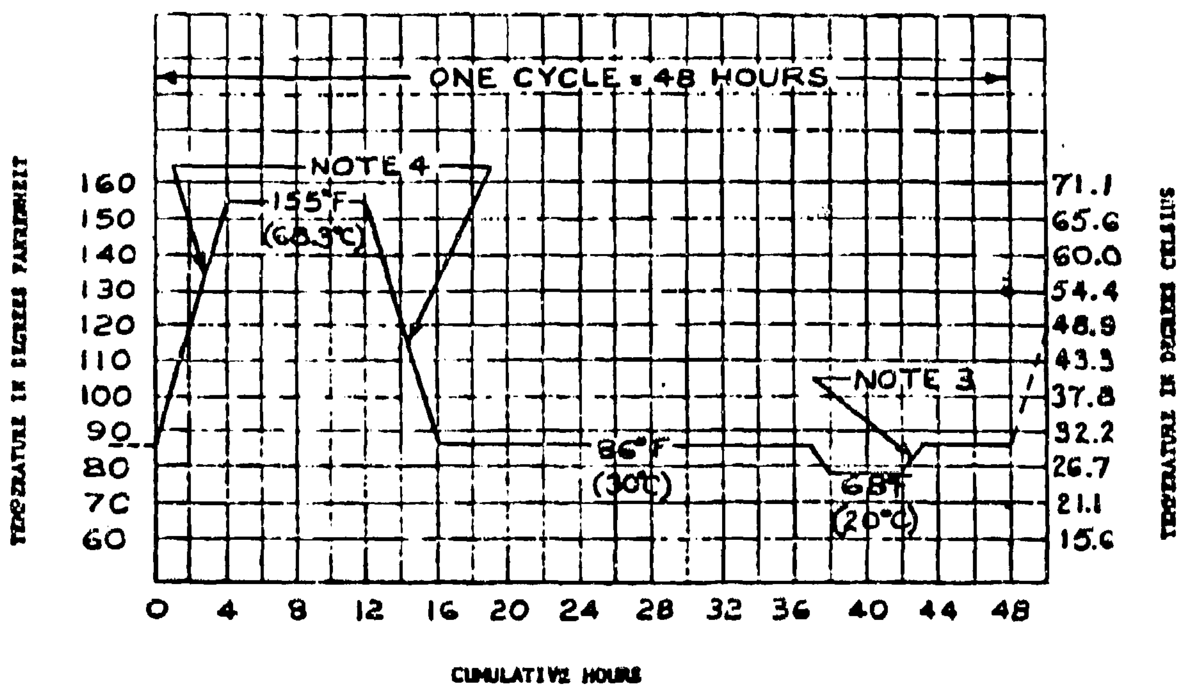
3.3.4 VIBRATION (Non-operative). The apparatus shall be mounted to a shake table and vibrated along each of its primary axes at 2.5 g. The vibration frequency shall be cycled from 7 Hz to 200 Hz to 7 Hz seven times, each cycle lasting 12 minutes. The test shall be terminated and considered failed if there is any evidence of loss of mechanical integrity. The unit may be mounted to the shake table by means of integral mounting provisions. It may also be clamped between two 1-inch pieces of plywood (with clearances cut for feet or other protrusions), one of the pieces of plywood being mounted to the shake table.

3.3.5 DROP (Non-operative). From a height of 12 inches, drop the apparatus on its bottom surface or supports on a surface consisting of 2-inch plywood backed by concrete. To perform the drop, two persons shall support opposite ends of the apparatus and drop the apparatus simultaneously.

Note: Criteria for passage of 3.3.4 and 3.3.5 are passage of succeeding tests.

3.4 ELECTRICAL PERFORMANCE

The following tests are to be performed under the input and output conditions specified in the test sequence.



NOTES:

1. The actual temperature during the cycle shall be within 5°F (2.7°C) of the temperature shown on the chart.

2. Relative humidity shall be maintained between 90 and 98% at all times during the cycle.

3. The measured increase in temperature from 68 ± 5°F (20 ± 2.7°C) to 86 ± 5°F (30 ± 2.7°C) shall not be less than 18°F (10°C).

4. The rate of temperature change between 86°F (30°C) and 155°F (68.3°C) shall be not less than 15°F (8.3°C) per hour.

Figure A2. Temperature-Humidity Cycle

3.4.1 VOLTAGE AND FREQUENCY. Measure the output voltage and frequency. Output voltage shall be the selected voltage ±2%; output frequency shall be the selected value ±½%.

3.4.2 EFFICIENCY. Measure the input voltage, input current, and output power. Calculate $\frac{P_{out}}{V_{in} \times I_{in}}$. This ratio shall be greater than 0.85.

3.4.3 DISTORTION.

3.4.3.1 Total Harmonic Distortion. Measure the total harmonic distortion of the output. The THD shall not exceed 5%.

3.4.3.2 Distortion Analysis. With a spectrum analyzer perform a harmonic analysis of the output voltage through at least the thirteenth harmonic. No single harmonic shall exceed 3% of the output.

3.4.3.3 Waveform. With an oscilloscope (having a dc-15 MHz minimum bandwidth) set to show a full output voltage cycle, photograph the oscilloscope trace. Expand the scale vertically by at least a factor of 5. Photograph the peak of the signal. Photograph the zero crossing point of the signal. There shall be no evident discontinuities, spikes, or notches. A discontinuity will be defined as any step in the waveform which exhibits a rise time of less than ¼ the width of the succeeding step in the waveform. A spike or notch shall be defined as an overshoot or undershoot in any step which falls outside the band defined by the final amplitudes of the previous and succeeding steps.

3.4.3.4 DC CONTENT. Connect an ac voltage rejection filter to the output terminals and observe the output from the filter with a dc voltmeter having sensitivity of at least 20,000 ohms/volt on a full scale range of no more than 0.75 volts. Output shall be less than 0.1 Vdc.

3.4.4 SHORT TERM STABILITY AND TRANSIENT RESPONSE. Using a chart recorder to record the output voltage, start the chart recorder at a speed of 1-2 inches per second and operate the apparatus for at least 30 seconds. Amplitude shall be stable to within 2% with no periodic variations. Increase chart speed to 2-5 inches per second. Remove and reapply the load 5 times at approximately 10 second intervals. Apply and remove half the specified load 5 times at approximately 10 second intervals. At each step the steady state voltage shall not deviate from the steady state voltage by more than 20% and shall recover to the steady state voltage within 3 seconds.

3.4.5 ELECTROMAGNETIC INTERFERENCE. Test for EMI per MIL-STD-461A Notice 4 (EL), using the methods of MIL-STD-462 for class V mobile electric power equipment conducted emission CE03 and radiated emission RE02, except that the frequency band for RE02 shall be 14 kHz to 100 MHz. CE03 (0.02-50 MHz) shall be applied to both input leads and output leads.

3.4.6 REVERSE INPUT. Apply the input voltage in the reverse direction. Apparatus shall not be damaged.

3.4.7 OVERLOAD. Apply a 1.5X load and verify that the output voltage remains greater than 0.9 times the set value for at least 10 seconds. After 10 seconds the the apparatus may trip out from overcurrent. Remove the load and reset the overcurrent trip if necessary. Observing the output current, short the output. The output current shall at no time exceed 2½ times the current into a 1X load, and the apparatus shall trip from overcurrent. Remove the short and reset the overcurrent trip.

3.4.8 INPUT VOLTAGE EXTREMES. Operating the chart recorder at ½-1 inch/second, decrease the input voltage at a rate of 1 volt/second until the apparatus turns off. Continue to decrease the voltage 10 volts more. Increase the voltage at about 1 volt/second to 45Vdc. The apparatus shall come back on and the turn-off and turn-on shall be orderly with no repeated spikes or oscillations in the output voltage. Increase the input voltage at 1 volt per second until the apparatus turns off. Continue to increase the input to 80 Vdc and then decrease it to 45 Vdc. Overvoltage turn-off and turn-on shall occur in an orderly manner with no repeated spikes or oscillations in the output voltage.

3.4.9 HIGH IMPEDANCE SOURCE. This test verifies the stability of the apparatus when operating from a high impedance source such as a fuel cell. Connect a variable resistance in series with the input power source. The power source voltage and the resistor value shall be such that when the apparatus is unloaded (ØR load) the input voltage to the apparatus is 60 Vdc, and when the apparatus is loaded with a 1.3R load, the input voltage to the apparatus is 36 Vdc. Perform paragraph 3.4.4

3.5 AUDIBLE NOISE

Operate the apparatus under the given conditions and measure the sound pressure levels with a microphone at ten feet from the unit. In any direction from the unit the sound pressure shall not exceed the values below for the given frequency bands:

Frequency Band (Hz)	Maximum level in decibels (0.0002 microbar reference)
75-150	68
150-300	54
300-600	54
600-1200	48
1200-2400	48
2400-4800	54
4800-9600	55

If pure tones or a narrow band of noise are present in any octave band, the sound pressure permissible for that octave shall be 5 db less than the values given for frequencies above 1200 Hz and 10 db less than the value given for frequencies below 1200 Hz.

APPENDIX B

TEST DATA FOR THE TRANSFORMERLESS-OUTPUT INVERTER

Electrical Performance

Part No. ________ Serial No. ________ Date ________

Test Description / Remarks	Load	f. set	Vout set	Vin set	Iout (M6)	Vin x Iin	THD	
		f (M11)	Vout (M3)	Vin (M2)	Iin (M1)	Pout (M5) / Vin x Iin	Max. Harmonic / %	
Electri[illegible]	0 R	[illegible]	120	[illegible]	0	76.4	—	PC_{out} =
			120	37.1	2.06	—	—	
	½ R	400	120	45	6.6	1929	—	
			120	47.9	41.27	1584/1929 = 82%	—	

Part No. ______ Serial No. ______ Date ______

Test Description / Paragraph	Load	f set	Vout set	Vin set	Iout (M6)	Vin x Iin	THD	
		f (M11)	Vout (M3)	Vin (M2)	Iin (M1)	Pout (M5) / Vin x Iin	Max Harmonic %	
Perf.	1R	400	120	45	13.14	1941		DC out = 0
			119.6	47.7	40.61	1571/1941 = 81%		
	1X	400	120	45	—	—	—	DC out = —
	—	—	—	—	—	—	—	
	1R	400	120	36	12.20	1830	1.7%	
			120.05	33.4	54 8	1465/1830 = 80%	—	
	1R	400	120	60	12.3	1756	1.75%	
			12005	64.99	27.02	1472/1756 = 84%	—	
Perf. 60Hz	1R	60	120	45	12.26	1770	1.94%	DC out = 0.04
			120.05	47.2	37.5	1472/1770 = 83%		
	1X	60	120	45	—	—	—	DC out = —
	—	—	—	—	—	—	—	

Part No. ________ Serial No. ________ Date ________

Test Description / Paragraph	Load	f set	Vout set	Vin set	Iout (M6)	Vin x Iin	THD	
		f (M11)	Vout (M3)	Vin (M2)	Iin (M1)	Pout (M5) / Vin x Iin	Max. Harmonic %	
Perf. [illegible] Hz	0R	60	120	~~45~~		71.[illegible]		Pout =
			119.9	37.1	2.04		—	
	0R	6[illegible]	[illegible]	60	—	—	—	
	—	—	—	—	—	—	5th -4[illegible]db	
	1R	60	120	36	—	—	—	
	—	—	—	—	—	—	3rd -40db	
Perf. 240V	1R	60	240	45	6.6	1898	—	Pout = [illegible]
			239.1	47.8	39.7	[illegible]/1898 = 83%	—	
	1R	60	[illegible]	36	6.6	1944	—	
			239.5	36.2	53.7	1573/1944 = 81%	—	
	1R	60	240	60	6.6	1877	—	[illegible]
			239.5	60.1	27.4	1573/1877 = 84%	—	

Part No. ________ Serial No. ________ Date ________

Test Description / Paragraph	Load	f set / f (M 11)	Vout set / Vout (M3)	Vin set / Vin (M2)	Iout (M6) / Iin (M1)	Vin x Iin / Pout (M5) / Vin x Iin	THD / Max Harmonic %	
[illegible]	0R	60	240	45		—	—	D[illegible]
					—	—	—	
	1X	60	240	45	—		—	DC[illegible] =
					—	—	—	
Perf [illegible] 400 Hz	1R	400	240	45	6.6		—	[illegible] - 0.05
			239.1	47.9	4027	—	—	
	1R	400	240	36	6.6	1969	—	
			240.1	35.8	55.0	1585/1969 = 81%	—	
	1R	400	240	60	6.6	—	2%	
			239.6	66.1	28.4	—	—	
	ØR	400	240	45	—	—	—	DC out =
	—	—	—	—	—	—	—	

APPENDIX C

TEST DATA FOR THE TRANSFORMER-OUTPUT INVERTER

Transformer-Output Inverter

Part No. 61098-2 Serial No. 105 Date 7/6/77

Test Description / Paragraph	Load	f set	Vout set	Vin set	Iout (M6)	Vin x Iin	THD	
		f (M11)	Vout (M3)	Vin (M2)	Iin (M1)	Pout (M5) / Vin x Iin	Max. Harmonic %	
[illegible]	R	[illegible]	120	45	12.5	1784	—	
		—	120	45.5	39.2	1505/1784 = 84.3%	—	12:15 PM
[illegible]	R	[illegible]	[illegible]	[illegible]	12.46	1808	—	
		—	119.78	45.1	40.10	1500/1808 = 83.0%	—	12:30
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	12.42	1824	-	
		—	119.52	45.15	40.4	1496/1824 = 82.0%	—	12:45
[illegible]	[illegible]	[illegible]	[illegible]	45	12.41	1827	—	
		—	119.50	45.23	40.40	1492/1827 = 81.7%	—	1:00
[illegible]	[illegible]		[illegible]	45	12.41	1830	—	
		-	119.44	45.3	40.40	1492/1830 = 81.5%	—	1:15
[illegible]	[illegible]		[illegible]	[illegible]	12.40	1833	—	
		—	119.42	45.6	40.2	1492/1833 = 81.3%	—	1:30

Part No. 61078-2 Serial No. 105 Date 7/6/77

Test Description / Paragraph	Load	f set	Vout set	Vin set	Iout (M6)	Vin x Iin	THD	
		f (M 11)	Vout (M3)	Vin (M2)	Iin (M1)	Pout (M5) / Vin x Iin	Max. Harmonic %	
[illegible]	1R	60	120	45	12.40	1841	—	
		—	119.42	45.7	40.25	1490/1841 = 80.9%	—	1.45
[illegible]	1R	60	120	45	12.40	1842	—	
		—	119.40	45.6	40.40	1490/1842 = 80.9%	—	2:00
[illegible]	[illegible]	[illegible]	120	45	12.40	1854	—	
		—	119.39	45.9	40.40	1490/1854 = 80.4%	—	2:15

Part No. 61098-2 Serial No. 125 Date 7/6/77

Test Description / Paragraph	Load	f set / f (M11)	Vout set / Vout (M3)	Vin set / Vin (M2)	Iout (M6) / Iin (M1)	Vin x Iin / Pout (M5) / Vin x Iin	THD / Max Harmonic %
High Temperature 60 Hz	1R	60	120	36	2.46	1900	2.6%
		60.6	119.32	36.40	56.2	1497/1900 = 78.8%	—
"	1R	60	120	45	12.46	1858	2.6%
		60.4	119.32	45.10	41.2	1497/1858 = 80.6%	—
	1R	60	120	60	12.46	1847	2.6%
		60.6	119.32	60.35	30.6	1498/1847 = 21.1%	—
	ØR	60	120	60	0	96	1.65%
		60.5	119.76	60.07	1.6	0	—
Low Temperature 60 Hz	1R	60	120	36	12.72	1919	1.7%
		59.3	120.79	36.00	53.3	1573/1918 = [illegible]%	—
	1R	60	120	45	12.70	1882	1.6%
		59.3	120.75	45.25	41.6	1515/1882 = [illegible]%	—

Part No. [illegible]   Serial No. [illegible]   Date [illegible]

Test Description / Paragraph	Load	f set / f (M11)	Vout set / Vout (M3)	Vin set / Vin (M2)	Iout (M6) / Iin (M1)	Vin x Iin / Pout (M5) / Vin x Iin	THD / Max. Harmonic %	
Low Temperature 60 Hz	1R	60	120	60	12.7[illegible]	[illegible]	.6%	
		59.2	120.74	59.27	31.4	[illegible]	—	
	0R	60	120	60	0	73[illegible]	1.5%	
		59.3	120.[illegible]	59.40	1.4	0	—	
High Temp. 400 Hz	1R	400	120	36	12.[illegible]	1871	1.7%	
		401	19	36.54	51.2	[illegible]/1871 = [illegible]%	—	
	1R	400	120	45	12.47	184[illegible]	1.6%	
		401	119.79	45.10	[illegible]	1535/1842 = [illegible]%	—	
"	1R	400	120	60	12.4%	1822	2%	
		401	119.82	60.22	30.25	1502/1822 = 82.5%	—	
"	0R	400	120	60	0	76.1	1%	
		401	120.[illegible]	5[illegible]	.75	0	—	

Part No. [illegible] Serial No. [illegible] Date 7/ /

Test Description / Paragraph	Load	f. set / f (M11)	Vout set / Vout (M3)	V_{in} set / V_{in} (M2)	I_{out} (M6) / I_{in} (M1)	$V_{in} \times I_{in}$ / $\frac{P_{out} (M5)}{V_{in} \times I_{in}}$	THD / Max. Harmonic %	
Low Temp 400 Hz	1R	400	[illegible]	[illegible]	[illegible] .584	[illegible]	[illegible]	
		396	[illegible]	[illegible]	[illegible]	[illegible] 81.[illegible]	—	
	1K	400	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	
		396	[illegible]	[illegible]	[illegible]	[illegible] 12.8%	—	
	.1R	400	[illegible]	60	[illegible]	12[illegible]	1.3[illegible]	
		397	[illegible]	[illegible].81	30.1	15[illegible] / 1802 = [illegible]%	—	
	0R	[illegible]	[illegible]	[illegible]	0	99.4	1.1%	
		[illegible]	[illegible].44	59.58	1.5	—	—	
Temp. Humidity Alt. [illegible] F	1R	[illegible]	[illegible]	[illegible]	[illegible]	—	1.75[illegible]	[illegible]
	1390	[illegible]	[illegible].74	40.20	[illegible]	—	—	
500 ft 107° F	1R	[illegible]	120	[illegible]	[illegible]	—	1.88%	
	1501	[illegible]	[illegible]70	45.57	[illegible]	—	—	

[illegible]

Electrical Performance

Part No. [illegible]-2 Serial No. 10[illegible] Date [illegible]

Test Description / Request	Load	f. set	Vout set	Vin set	Iout (M6)	Vin x Iin	THD	
		f (M11)	Vout (M3)	Vin (M2)	Iin (M1)	Pout (M5) / Vin x Iin	Max Harmonic %	
Electrical Performance	OR	[illegible]	20	[illegible]	0	[illegible]	%	[illegible] = 0
		[illegible]	[illegible]	45.[illegible]	[illegible]	)	—	
	½ R	400	[illegible]	45	[illegible]	[illegible]	1.3[illegible] %	
		400	120.21	45.00	[illegible]	7[illegible] / 90 = [illegible]	—	

Part No. [illegible] Serial No. [illegible] Date [illegible]

Test Description / Paragraph	Load	f set / f (M11)	Vout set / Vout (M3)	V_{in} set / V_{in} (M2)	I_{out} (M6) / I_{in} (M1)	$V_{in} \times I_{in}$ / $\frac{P_{out} (M5)}{V_{in} \times I_{in}}$	THD / Max. Harmonic %	
Perf.	1R	400	120	45	[illegible]	[illegible]	[illegible]	DC_{out} [illegible]
		[illegible]	120.1[illegible]	45.0	[illegible]	[illegible]	Third [illegible]	
	1X	400	120	45	[illegible]	[illegible]	[illegible]	DC [illegible]
		400	[illegible]	45.1[illegible]	[illegible]	[illegible]	—	[illegible]
	1R	400	120	36	[illegible]	1837	[illegible]	
		400	120.14	35.[illegible]	[illegible]	1435 / 1837 = [illegible]	—	
	1R	400	120	60	[illegible]	[illegible]	1.4[illegible]	See later pages for remaining 400 Hz, 120V tests
		400	[illegible]	[illegible]	[illegible]	[illegible]	—	
Perf. [illegible] 2	1R	60	120	45	[illegible]	1797	1.7%	[illegible]
		60.0	120[illegible]	45.3[illegible]	[illegible]	[illegible]	[illegible] %	
	1X	60	120	45	15[illegible]	[illegible]	[illegible]	[illegible] = [illegible]
		60.[illegible]	[illegible]	45[illegible]	[illegible]	[illegible]	—	

Part No. [illegible]   Serial No. 10[illegible]   Date [illegible]

Test Description / Paragraph	Load	f set / f (M11)	Vout set / Vout (M3)	Vin set / Vin (M2)	Iout (M6) / Iin (M1)	Vin x Iin / Pout (M5) / Vin x Iin	THD / Max. Harmonic %	
Perf. [illegible] Hz	0R	60	120	45	0	7[illegible]	[illegible]%	D[illegible] = [illegible]
		60.[illegible]	120.[illegible]	45.[illegible]	[illegible]	0	—	
	0R	6[illegible]	[illegible]	60	0	20.[illegible]	[illegible]%	
		60.8	120.[illegible]3	59.5	1.35	^	—	
	1R	60	120	36	12.4	1851	1.75%	
		60.1	120.[illegible]	36.45	50.5	1500/1841 = 81.5%	—	
Perf. 240V 60Hz	1R	60	240	45	6.290	1829	1.8%	D[illegible] = [illegible]
		60.1	240.00	45.00	40.65	1510/18[illegible] = 82.5%	—	
	1R	60	240	36	6.290	1766	1.8%	
		60.1	239.96	35.95	51.9	1510/1766 = 80.9%	—	
	1R	60	240	60	6.216	1798	1.76%	VC[illegible] = 0
		60.0	240.03	59.45	30.25	15[illegible]/1798 = 84.1%	—	

Part No. [illegible] Serial No. 105 Date [illegible]

Test Description / Paragraph	Load	f set / f (M11)	Vout set / Vout (M3)	Vin set / Vin (M2)	Iout (M6) / Iin (M1)	Vin x Iin / Pout (M5) / (Vin x Iin)	THD / Max. Harmonic %	
[illegible] 2401.	[illegible]R	[illegible]	240	45	—	—	—	DC out [illegible]
		[illegible]	240.32	44.82	—	—	—	
	1X	[illegible]	240	45	—		—	DC out = [illegible]
	—	—	—	—	—	—	—	
[illegible]	1R	400	240	45	[illegible]	—	1.4%	DC out [illegible]
		400	240.65	45.1	10.5	—	—	
	1R	[illegible]	240	36	6.38	1887	1.4%	
		[illegible]	240.0[illegible]	35.5	53.15	1524/1887 = [illegible]%	—	
	[illegible]	4[illegible]	240	[illegible]	6.[illegible]	—	1.4%	
		400	240.08	[illegible]9.75	[illegible]	—	—	
	[illegible]R	400	240	[illegible]5	—	—	—	DC out
		400	240.[illegible]	[illegible]	—	—	—	

Part No. ____________ Serial No. ____________ Date ____________

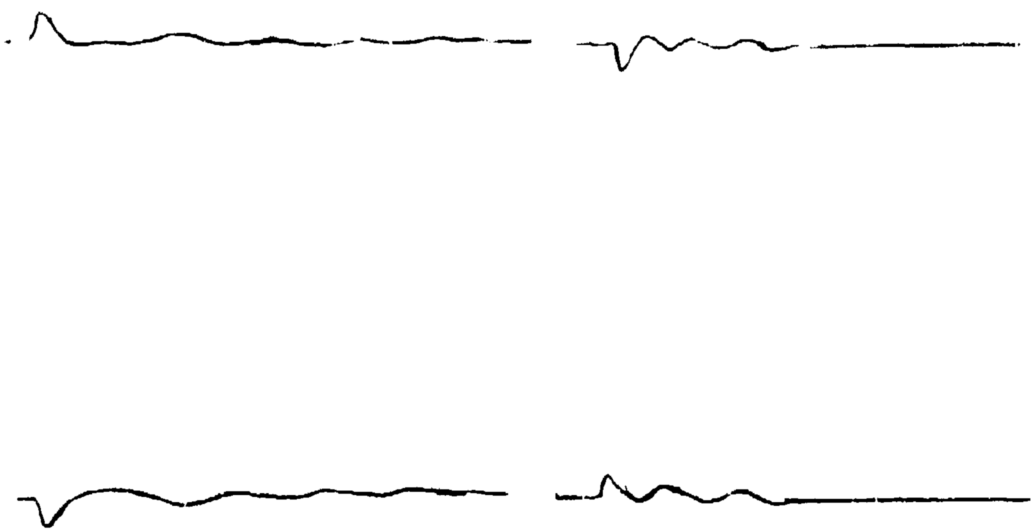
Test Description / Paragraph	Load	f set	V_{out} set	V_{in} set	I_{out} (M6)	$V_{in} \times I_{in}$	THD	
		f (M11)	V_{out} (M3)	V_{in} (M2)	I_{in} (M1)	$\frac{P_{out}(M5)}{V_{in} \times I_{in}}$	Max Harm. %	

1. Stability and Transient Response. The chart recordings do not lend themselves readily to reproduction. For this reason descriptions and envelope tracings are appended as data rather than the charts themselves. A single tracing is included for each transient condition. The charts for identical load-change conditions were indistinguishable from one another. Under conditions of constant load there were no observable variations or oscillations in the output voltage.

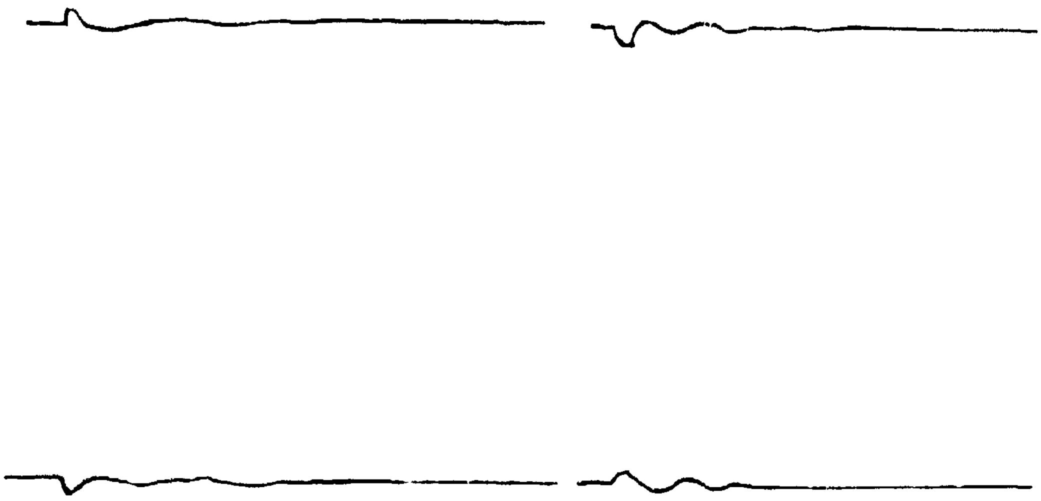
2. Polarity Reversal. Polarity reversal causes the circuit breaker to open with no damage to the inverter.

3. Input Voltage Extremes. The envelope tracing shows turn-off as the input voltage decreases below an acceptable level, and turn-on when the input voltage increases again. No input over-voltage protection was incorporated in this model; the inverter was capable of operating at a voltage several times the nominal.

4. High Impedance Source. Tracings of the voltage envelopes during load transients are appended.

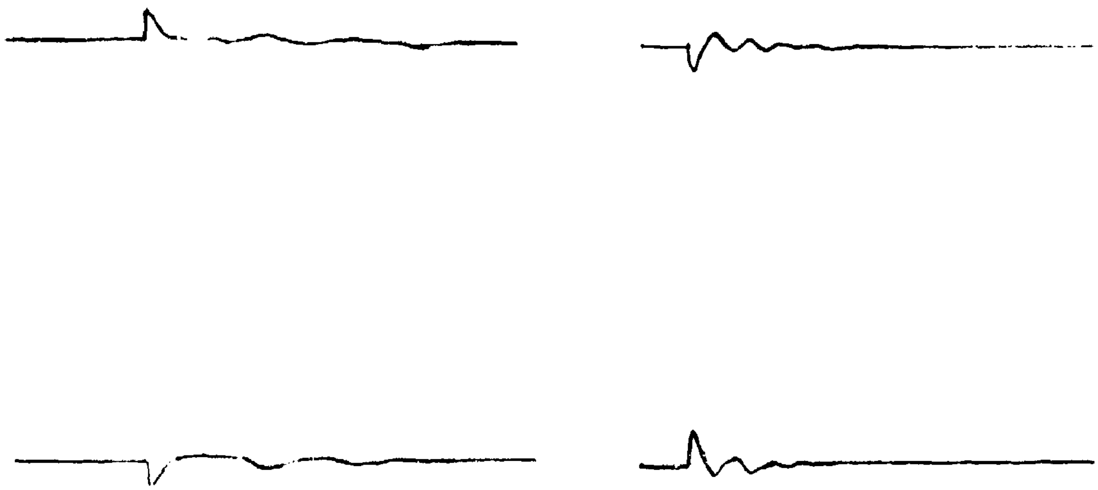


Removal and Reapplication of Full Load

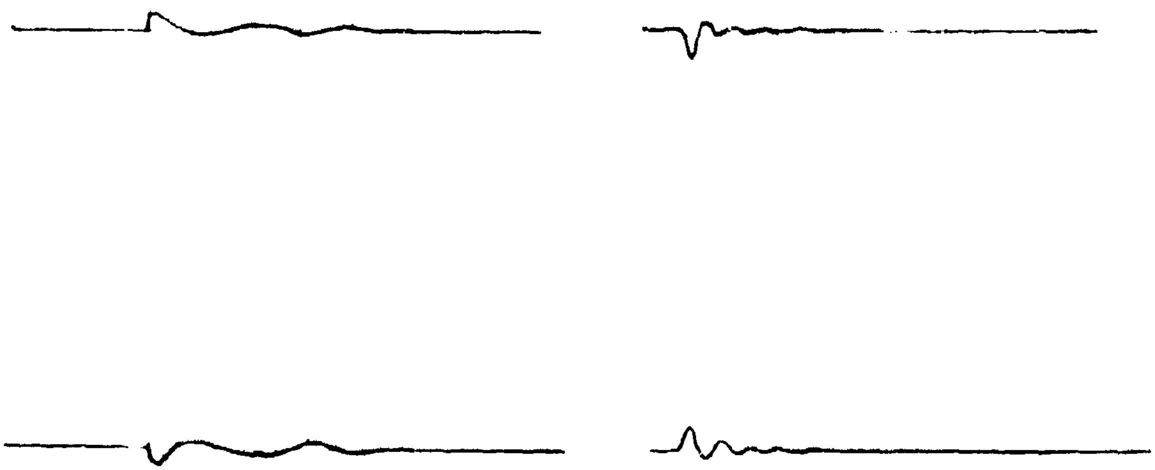


Removal and Reapplication of Half Load

High Impedance Source--Output Envelope: 45 Vdc Input, 120V 400Hz Output, Chart Speed 5 cm/sec



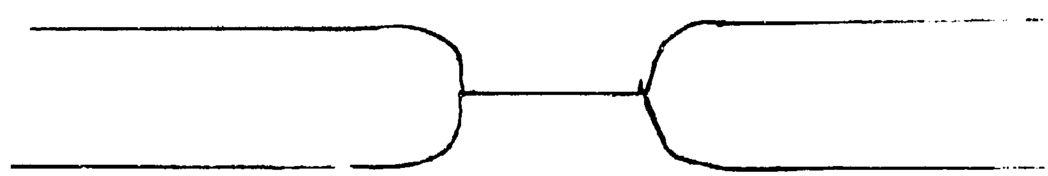
Removal and Reapplication of Full Load



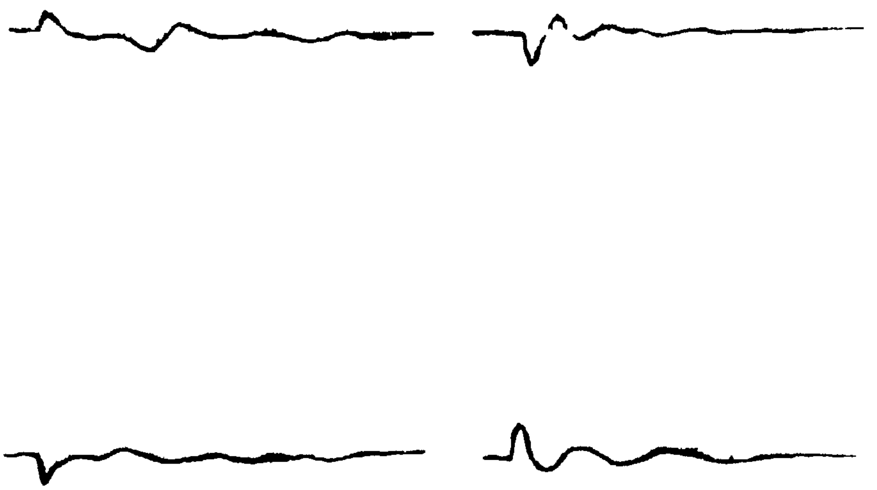
Removal and Reapplication of Half Load

Output Envelope: 45 Vdc Input, 120V 400 Hz Output,

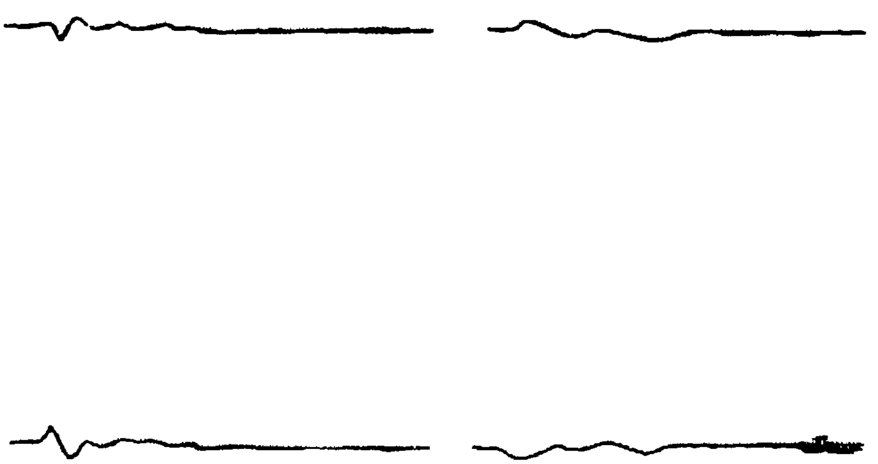
Chart Speed 5 cm/sec



Input Voltage Extremes



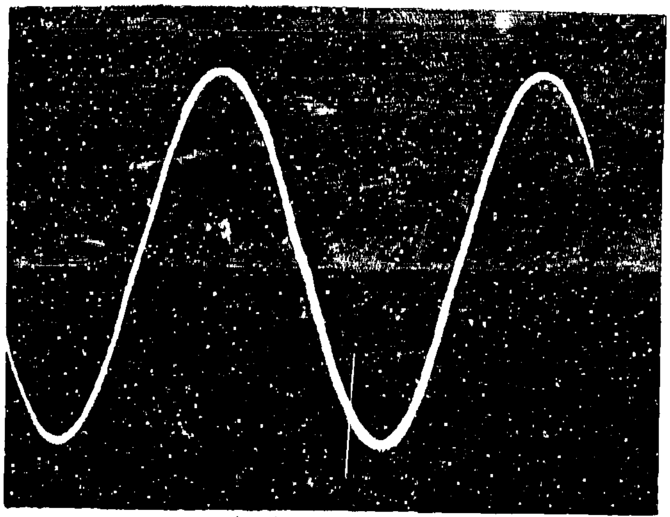
Removal and Reapplication of Full Load



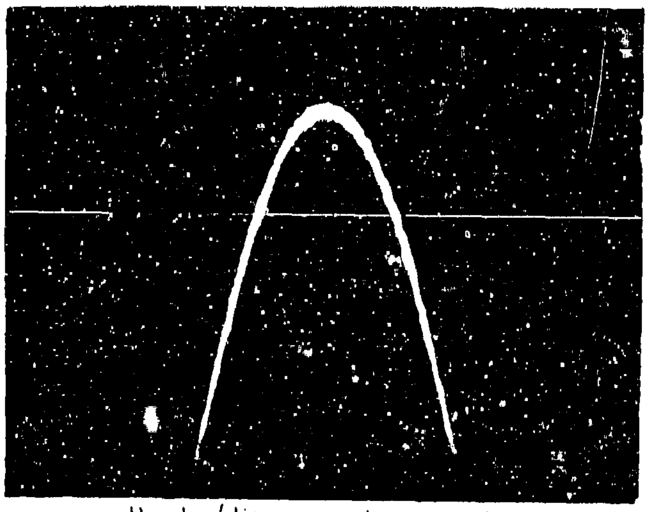
Removal and Reapplication of Half Load

Output Envolope: 45 Vdc Input, 120V 60 Hz Output,

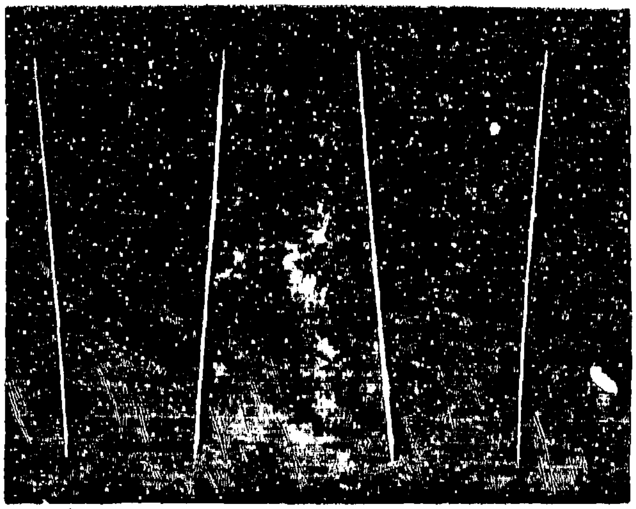
Chart Speed 5 cm/sec



Full Cycle

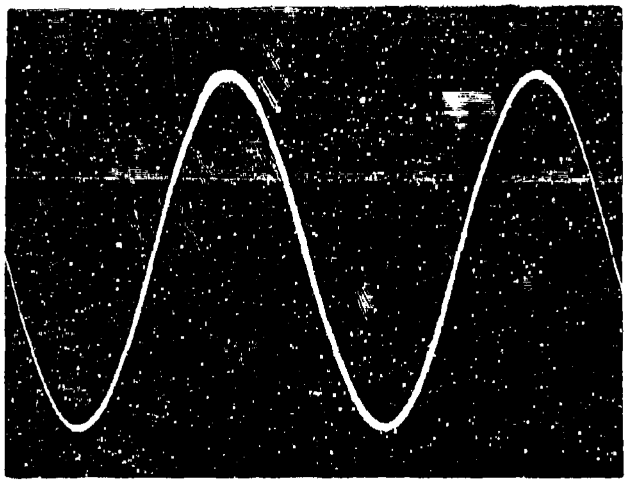


Peak (Expanded Scale)

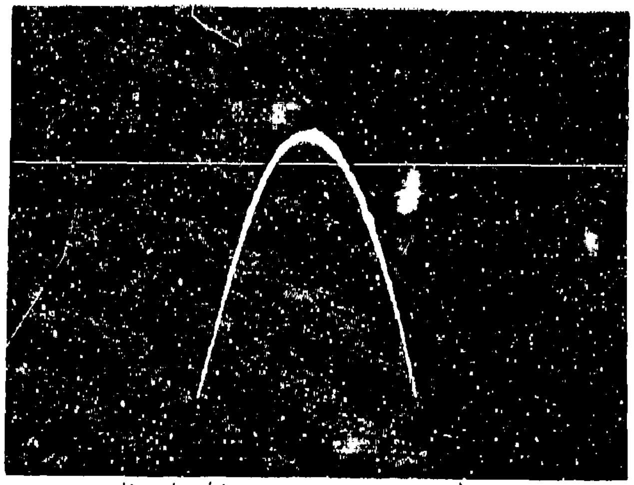


Zero-Crossing (Expanded Scale)

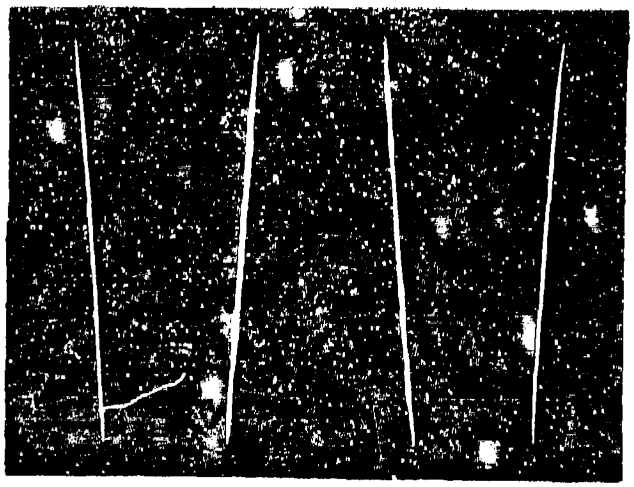
Waveform with 45V Input and 120V, 400 Hz Output,
Resistive Load



Full Cycle

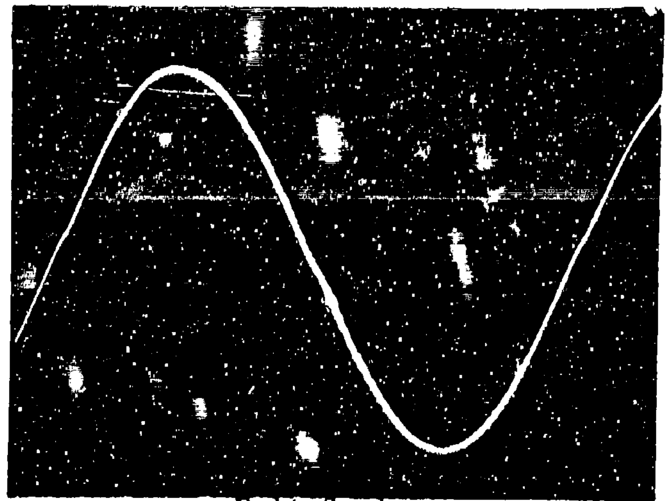


Peak (Expanded Scale)

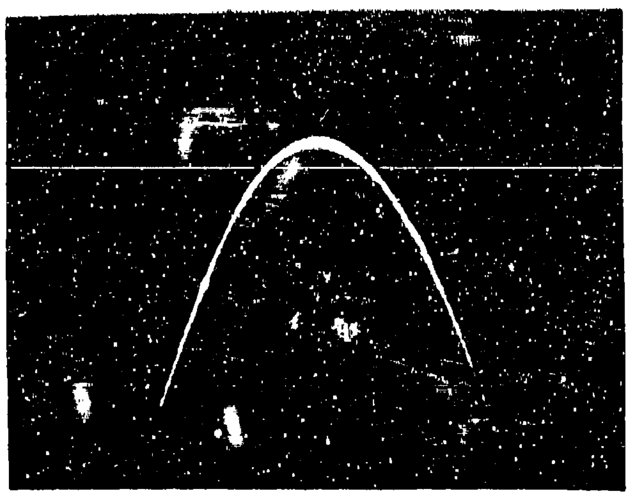


Zero-Crossing (Expanded Scale)

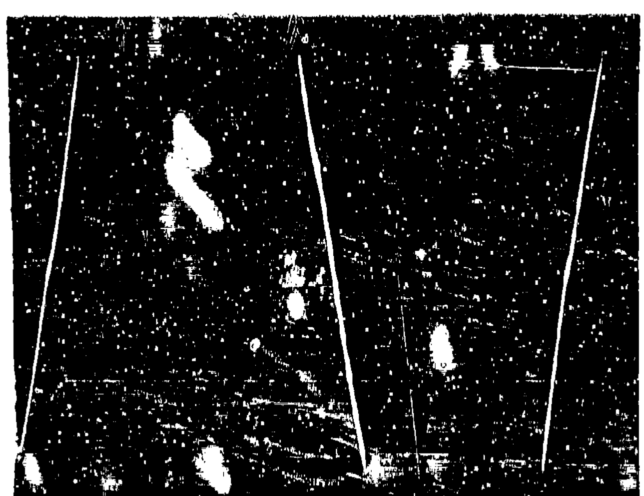
Waveform with 45V Input and 120V, 400 Hz Output, 0.8 PF Load



Full Cycle

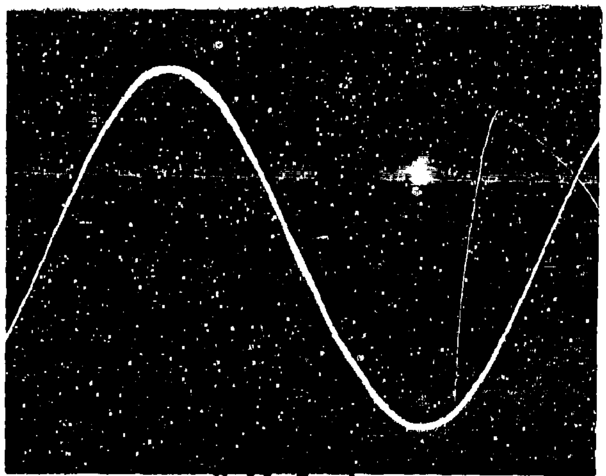


Peak (Expanded Scale)

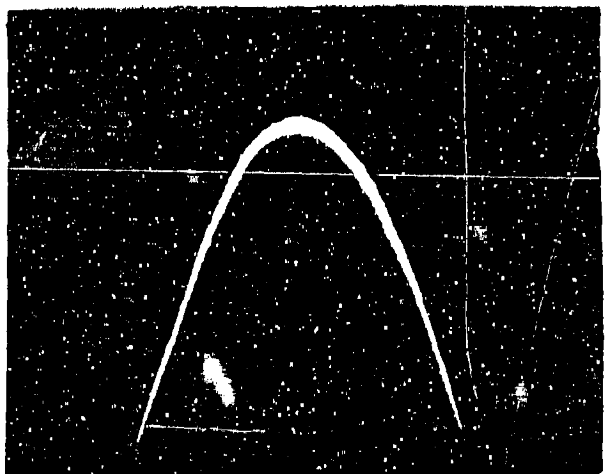


Zero-Crossing (Expanded Scale)

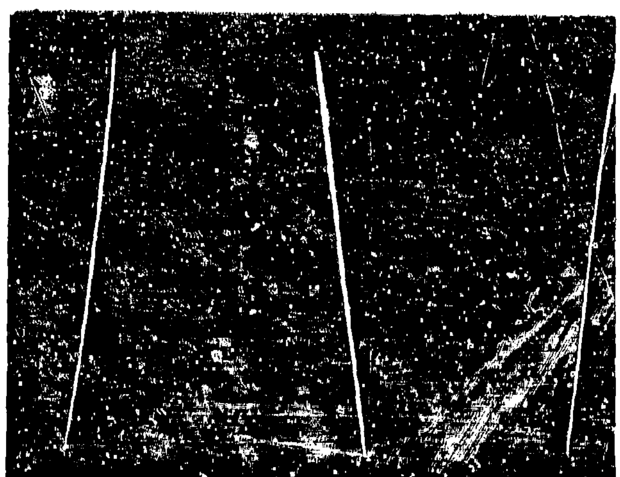
Waveform with 45V Input and 120V, 60 Hz Output, Resistive Load



Full Cycle



Peak (Expanded Scale)



Zero-Crossing (Expanded Scale)

Waveform with 45V Input and 120V, 60 Hz Output, 0.8 PF Load

DECC President Charles Jobbins and MERADCOM Technical Representative
Dietrich Roesler Performing the Drop Test

GARWOOD LABORATORIES, INC.

708 SOUTH VAIL AVE.
MONTEBELLO, CALIF.

TEST REPORT

REPORT NO. 7036

July 18, 1977

REPORT NO. 7036
TEMPERATURE-HUMIDITY-ALTITUDE AND
VIBRATION TESTS ON
DELTA ELECTRONIC CONTROL CORP.
P/N 61098-2, 1.5 KW. INVERTER, TO
SPECIFICATION DECC-61098-006

Mfg. By: Delta Electronic Control Corp.
2801 S.E. Main Street
Irvine, California 92714

Test By: D. M. Martin	Concurred:
Report By: C. F. Myers	

County of Los Angeles
State of California } ss. C. F. Myers, being first duly sworn, deposes and says: that the information contained in this report has been obtained as the result of complete and carefully conducted tests, and is to the best of his knowledge and belief, true and correct in all respects.

Subscribed and sworn to before me on this 19th day of July 1977

OFFICIAL SEAL
SHIRLEY J. FRETWELL
NOTARY PUBLIC - CALIFORNIA
LOS ANGELES COUNTY
My comm. expires NOV 29, 1980
708 So. Vail Avenue, Montebello, CA 90640

Notary in and for said County and State
Shirley J. Fretwell

C. F. Myers, Manager, Test Laboratory

G-6A 1M 6-76

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GARWOOD LABORATORIES, INC.
708 SOUTH VAIL AVE.
MONTEBELLO, CALIF.

TEST REPORT

1. REFERENCES

Abbreviated Form	Full Reference Description
P.O. 7317	Purchase Order No. 7317 dated 6-26-77 from Delta Electronic Control Corporation.
DECC-61098-006	Delta Electronic Control Specification DECC-61098-006: Test Plan for 1.5 KW Inverters Developed for Mobile Applications.

2. DESCRIPTION OF UNIT TESTED

The unit submitted for test was one specimen of Delta Electronic Control Corporation P/N 61098-2, S/N 105; Inverter. The unit was a cased electronic device which was designed for an input voltage between 36 and 60 volts DC and had a selectable output of 120 or 240 volts at 60 or 400 Hz single phase electrical power at 1.5 KW.

3. PURPOSE

The purpose of this test program was to subject the unit to the Temperature-Humidity-Altitude Test as outlined in Para. 3.3.3 and the Vibration Test as outlined in Para. 3.3.4 of Specification DECC-61098-006. All operation of the unit when required during the test program was to be conducted by the manufacturer.

4. CONCLUSIONS

Examination of the unit at the completion of each test disclosed no evidence of damage, deterioration or other deleterious effects which could in any way prevent the unit from meeting service requirements. Delta Electronic Control engineering personnel indicated that during operation and during all functional testing that the unit functioned in conformance with the specification requirements. The unit was considered to have passed the tests as conducted in this Laboratory and were returned to Delta Electronic Control Corporation.

5. TEST METHODS AND RESULTS

5.1 TEMPERATURE-HUMIDITY-ALTITUDE TEST

5.1.1 Requirements -- DECC-61098-006, Para. 3.3.3.

5.1.2 Methods -- The unit was installed in a temperature/altitude test chamber with electrical connections made through penetration ports in the chamber wall. The chamber contained a fan to provide adequate circulation of the chamber atmosphere around the unit. The door of the chamber was equipped with an observation window which allowed the unit to be viewed during the test. The chamber was sealed and with the unit de-energized, the chamber pressure was reducer to a simulated altitude of 50,000 feet at a rate of between 1000 and 1500 feet per minute. These conditions were maintained for a period of 30 minutes after which time the unit was examined for evidence of damage through the observation window in the chamber door. Following this, the chamber altitude was reduced to 8000 feet, and the chamber temperature was increased to +95°F. After stabilization of these conditions, the unit was operated at rated electrical power for a period of 15 minutes by the manufacturer. The unit was then de-energized, and the chamber altitude was reduced to 5000 feet, and the temperature was increased to +107°F. After stabilization of these conditions, the unit was again operated for 15 minutes by the manufacturer at rated electrical power. The chamber was then returned to room ambient conditions, and the unit was removed and examined. Following examination, the unit was installed in a humidity test chamber with no electrical connections made. The chamber was sealed, and the relative humidity within the chamber was adjusted to a value between 90 and 98%. The unit was then subjected to one 48 hour temperature cycle as follows. During the first 4 hours, the temperature was increased from approximately 85° to 155°F. The temperature was maintained at 155°F between the 4th and 12th hour. The temperature was then decreased between the 12th and 16th hour to 86°F and maintained at this temperature between the 16th and 36½th hour. The temperature was decreased from 86°F to 68°F between the 36½th and 37th hour. The unit was maintained at 68°F between the 37th hour and the 42nd hour. The temperature was increased from 68°F to 86°F for the 42nd to 42½th hour. The chamber temperature was then maintained at 86°F for the remainder of the 48 hour cycle. Following this, the unit was removed from the test chamber and examined, then subjected to functional tests by Delta Electronic Control Corporation engineering personnel.

5.1.3 Results -- Examination of the unit during and after the test disclosed no evidence of damage, deterioration or corrosion which could in any way prevent the unit from meeting service requirements. Delta Electronic Control Corporation engineering personnel indicated that all measurements on the unit were within the specification limits. The unit was considered to have passed the Temperature-Humidity-Altitude Test as conducted in this Laboratory.

5.2 VIBRATION TEST

5.2.1 Requirements -- DECC-61098-006, Para. 3.3.4

5.2.2 Methods -- The unit was clamped to a base plate which was fabricated from thick magnesium tooling plate. See Photo. This assembly was installed on the vibration exciter for application of vibration along the vertical axis. An accelerometer was installed on the base plate near the unit mounting to control and monitor the input vibration. Vibration was applied to the unit with the frequency cycling from 7 to 200 and back to 7 Hz in 12 minute cycles for a total of 84 minutes. The vibration amplitude was maintained at ±2.5 g's throughout the frequency range of the test.

5.2.3 Results -- Careful examination of the unit following the test disclosed no evidence of damage, distortion or looseness ~~of~~ of sub-components resulting from the test conditions. The unit was considered to have passed the Vibration Test as conducted in this Laboratory and was returned to the manufacturer for disposition.

TEST EQUIPMENT LIST

Items maintained within current applicable calibration period.

-Accelerometer: Endevco Model 2242C, S/N NA55, 7.47 rms mv/peak g. Used to monitor and control vibration test levels.

-Humidity Chamber: Tenney Engineering Model 40-H, S/N 1750. Temperature range +50 to +200°F, 50 to 98% relative humidity. Equipped with the control instruments listed below:

--Humidity Controller-Recorder: Bristol's Dynamaster Model 1P12G565FCIX-21-T111, S/N 552737, 0 - 100% relative humidity. Used to control and record chamber relative humidity during the test.

--Temperature Controller-Recorder: Bristol's Dynamaster Model 64A-1PG575FAT, S/N 66W1249, -100 to +200°F. Used to program temperature during the test.

-Vibration Exciter: MB Model C-125, S/N 130, rated at 10,000 force pounds with sinusoidal exertation. Ling Electronics Model PP50-70, S/N 10, Power Amplifier. Equipped with sinusoidal oscillator and controller MB Model N575/N576, S/N 234 (B&K Model 1028, S/N 113603).

GARWOOD LABORATORIES, INC.
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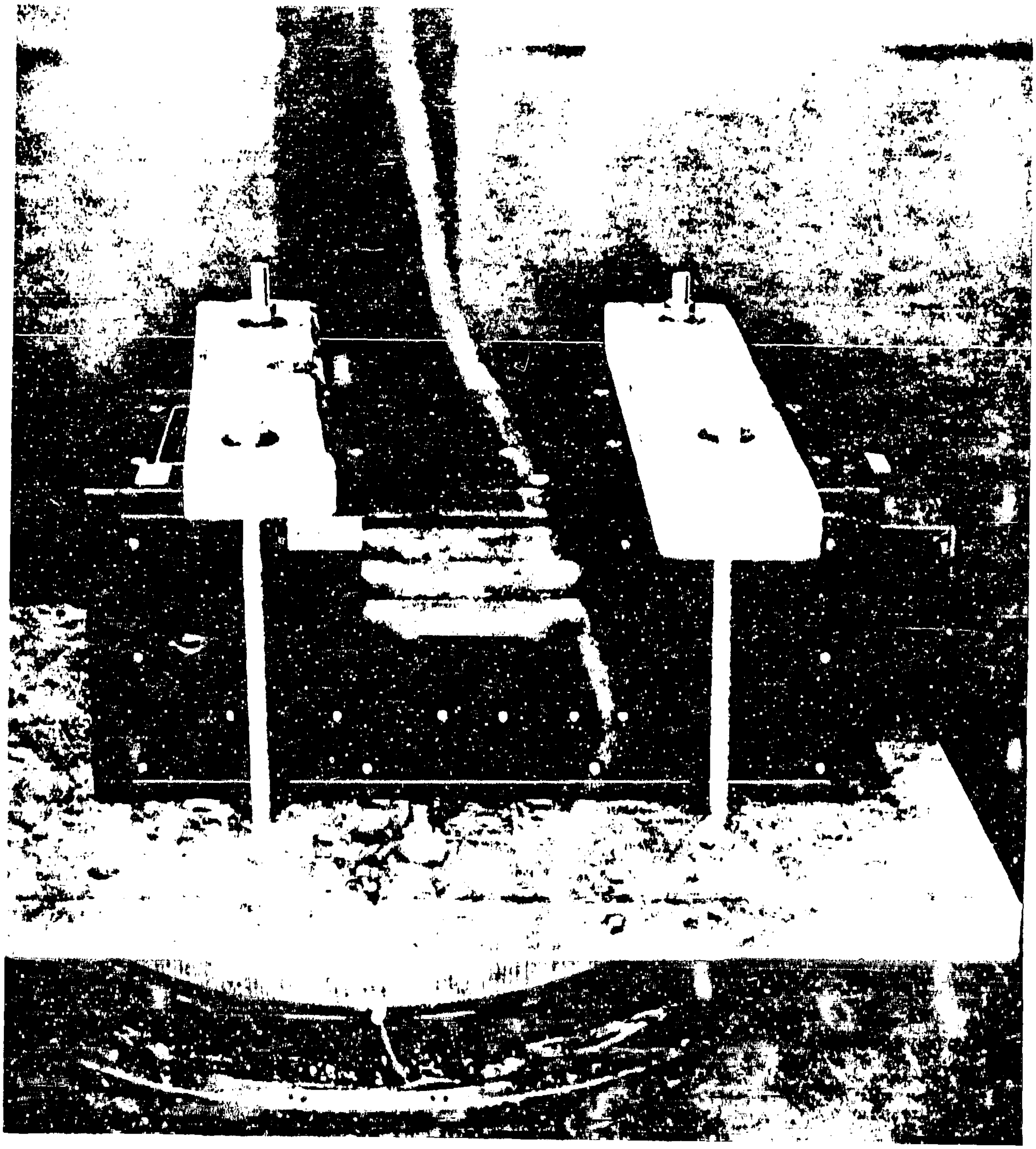
TEST REPORT

REPORT NO. [illegible]
PAGE
PHOTO

VIBRATION TEST SETUP



APPENDIX D

RELIABILITY CALCULATIONS

FOR THE TRANSFORMER OUTPUT INVERTER

FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Top ASSEMBLY NO. ____ ASSEMBLY TEMP. 60°C ENVIRONMENT G_F

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETER(S)	OPERATING PARAMETER(S)	STRESS RATIO	λ_b	π_E	π_Q	π	π	π	λ_p fpmh	REMARKS
A1	Regulator												15.565 /	54.4601
A2	Bias												2.0762 /	6.2204
A3	Output stage												4.949 /	26.9358
A4	Output stage												4.949 /	26.9358
A5	Logic												26.7515 /	122.9846
A6	Output filter												.092 / .11	
A7	Boost and filter												.6783	
A8	Inverter												1.6801 / 8.808	
C6	CE	980pf		[illegible]	60V	.6	.1775	2	3				1.065	
C7		[illegible]		150V	125V	.5	.1352	↓	↓				.8112	
C8	↓	[illegible]		150V	125V	.5	↓	↓	↓				↓	
C9	↓	3		400V	120V	.3	.0818	↓	↓				.5388	
C10	↓	3		400V	120V	.3	↓	↓	↓				↓	
C11	CQR/CG	5	M/-	[illegible]	60V	.3	.00008	2	1/10				.0002/.0016	
C12	↓	[illegible]	↓	[illegible]	60V	.3	.00008	↓	↓				↓	
C13	↓	.1	↓	[illegible]	240V	.4	.0001	↓	↓				.0002/.0020	

PREPARED BY: J Suchle
DATE: 12-75

PAGE TOTAL 60.5067 / 250.9032

PAGE 1 OF 3

FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY ICP ASSEMBLY NO. ______ ASSEMBLY TEMP 60°C ENVIRONMENT GF

REFERENCE DESIGNATOR	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π_F or π_{SR}	π_C	π_{cyc}	λ_p fpmh	REMARKS
C14	KQR/CQ	.1	M/-	600V	240V	.4	.0001	2	1/10				.0002/.002	
C15	CSR/CE	1200	↓	25V	12V	.5	.016/.1352	2	1/10	.07/1			.0022/2.704	
C16	↓	1200	↓	25V	12V	.5	↓	↓	↓	↓			↓	
R1	[illegible]	0-10K											non-catastrophic	
R2	RLR/RL	4.7Ω	M/-	½W	<.05W	<.1	.0019	5	1/5				.0095/.0475	
R3	↓	4.7Ω	↓	½W	↓	↓	↓	↓	↓				↓	
T1	T_{HS} = 110°C	mil spec insul					.003	5	3				.045	
T2							↓						↓	
B1	MU2A1	λ_b=.0020	π_T=3	π=1.5	π_N=2.5		L+M-T F=19000 [illegible]		π_{EM}=.5		λ_W=2		2.02	Ir replaced every 9500 hrs
CB1	IXAM						.0085	2/4		12/24	1.5	.1	.0306/.1224	
DS1													non-catastrophic	
DS2														
DS3														
DS4													↓	

PREPARED BY: J Suelzle
DATE: 12-75

PAGE TOTAL 2.1642/2.7374

PAGE 2 OF 3

D2

FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY TOP ASSEMBLY NO.: ____ ASSEMBLY TEMP. 60°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π_C	π_{cyc}	π	λ_p fpmh	REMARKS
S1	Toggle	DPDT	Mil/lower				.01/.75	1		3	1		.03/2.25	
S2	↓	SPST	↓				↓	↓		1	↓		↓	
S3		SPST								1				
S4	↓	SPST	↓				↓	↓		↓	↓		↓	
J7	MIL-C-26482, D material, 16 gauge						.0051	4					.0204	
J8	"							↓					↓	

PREPARED BY: J Suelzle

DATE: 12-75

PAGE TOTAL .1608/9.0408

FAILURE RATE DETERMINATION

EQUIPMENT 61477-2 ASSEMBLY Regulator ASSEMBLY NO. A1 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π_{Taps}	π_V	π_R	λ_p fpmh	REMARKS
R1	RLR/RL	75K	M/–	1/4W	<.025	<.1	.0019	5	1/5				.0095/.0475	
R2		3K			<.025W									
R3		10K												
R4		5.6K												
R5		8.2K												
R6		270K												
R7		10K												
R8		3K												
R9	↓	8.2K	↓				↓	↓	↓				↓	
R10	R1	0-5K	M.I/–		↓	↓	.584	3	2/4	1	1	1	3.5/7.0	
R11	RLR/RL	200K	M/–		.072	.29	.0024	5	1/5			1.1	[illegible]/.066	
R12		10K			<.025	<.1	.0019						.0095/.0475	
R13		2K		↓	↓	↓	↓						↓	
R15		3K		1/2W	.3W	.6	.0035						.0175/.0875	
16		10K		1/4W	<.025W	<.1	.0019						.0095/.0475	
?		1.5K												
?		18K												
19	↓	1.0	↓	↓	↓	↓	↓	↓	↓				↓	

PREPARED BY: J Swelzle
DATE: 12-75

PAGE TOTAL 3.6732/7.866

FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Regulator ASSEMBLY NO. A1 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π_{Tapc}	π_V	π_R	λ_p fpmh	REMARKS
R20	RLR/RL	3K	M/-	¼W	<.025W	<.1	.0019	5	1/5				.0095/.0475	
21	RJ	0-20K	M.I/-				.584	3	2/4	1	1	1	3.5/7.0	
25	RLR/RL	3.3K	M/-	¼W			.0019	5	1/5				.0095/.0475	
26		2K												
27		2K												
28		5.6K												
29		2K												
30		62K												
31		6.2K												
32		5.6K												
33		2K												
34		2K												
35		510												
36		300												
37		27												
38		1K												
39		43		1W	.2W	.2	.0021						.0105/.0525	
40		3K		¼W	<.025	<.1	.0019						.0095/.0475	

PREPARED BY: J Sch[illegible]
DATE: 12-7[illegible]

PAGE TOTAL 3.6625/7.8125

FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Regulator ASSEMBLY NO. A1 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π_{Taps}	π_V	π_R	λ_p fpmh	REMARKS
R41	RLR/RL	68	M/-	1/4W	<.025W	<.1	.0019	5	1/5				.0095/.0475	
42	↓	16	↓	1/2W	<.05W	↓	↓	↓	↓				↓	
43	RCR/RC	1	M/-	1/2W	<.1W	<.2	.009	2	1/5				.018/.09	
46	RLR/RL	300		1/4W	<.025W	<.1	.0019	5	1/5				.0095/.0475	
47		100		1/2W	.1W	.2	.0021						.0105/.0525	
54		470		1/4W	<.025	<.1	.0019						.0095/.0475	
55	↓	56K	↓				↓	↓	↓				↓	
56	RJ	0-20K	M.1/-				.584	3	2/4	1	1	1	3.50/7.0	
57	RLR/RL	1K	M/-				.0019	5	1/5				.0095/.0475	
58		1K		↓	↓									
[illegible]		.001		2 W	2.5								↓	
62		120K		1/4W	<.025W							1.1	.0104/.052	
63		24K		↓	↓	↓	↓						.0095/.0475	
64		3K		1/2W	.3W	.6	.0035						.0175/.0875	
65		510		1/4W	<.025W	<.1	.0019						.0095/.0475	
66		2K												
67		1K											↓	
72 73	↓	200 1K	↓	↓	↓	↓	↓	↓	↓				[illegible]/.0475 [illegible]/.0475	

PREPARED BY: J Suelzle
DATE: 12-75

PAGE TOTAL 3.6894/7.947

FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Regulator ASSEMBLY NO. A1 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π_{SR}	π	π	λ_p f pmh	REMARKS
AR1	741	C.P.	Jan B / Com	TTL = 1	C_1 = .0064 C_2 = .014	π_T = 2.5 π_E = 1	.029		2/150				.058/4.35	
AR2	748		↓				↓		↓				↓	
AR3	↓													
C1	CKR06/CK06	.01µf	M/–	200V	< 1V	<.1	.0021	2	1/10				.0042/.042	
C2	CKR06/CK06	.47µf		50V	< 18V	.36	.0070	↓	↓				.014/.14	
C3	CKR05/CK05	.1µf		50V	15V	.3	.0070						↓	
C4		.0022µf		100V	<10V	<.1	.0021						.0042/.042	
C5		.0033µf		100V	10V	↓	↓						↓	
C6	CKR05/CK05	.01µf		200V	10V									
C8		.01µf	↓		12V									
C9	↓	↓			↓									
C10	CKR05/CK05	560pf			<12V									
C11		330pf		↓	6V									
C12	↓	.01µf		200V	<6V									
C13	CKR06/CK06	[illegible]		[illegible]V	6V	↓	↓	↓	↓				↓	
C14	CSR13/CE	220µf		10V	6V	.6	[illegible]/.139	2	1/10	.07			.003/.196	
C15	[illegible]/CK05	.01µf	↓	[illegible]V	12V	<.1	.0021	2	1/10				.0042/.042	

PREPARED BY: J Suelzle
DATE: 12-76

PAGE TOTAL .2512/13.9866

FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Regulator ASSEMBLY NO. A1 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π	π	π	λ_p f pr h	REMARKS
C18	CSR13/CS13	220µf	M/	10V	6V	.6	[illegible]/.13	2	1/10	.07			.003/.046	
C19	↓	↓	↓	↓	↓		↓		↓	↓			↓	
20	H2-[illegible]	.22		200	120		.0005						.001/.01	
21	↓	.22		200	120	↓	.0005	↓	↓				↓	
22	CKR06/CK06	.01	M/-	200	12V	<.1	.0021	2	1/10				.0042/.042	
23					↓									
24					-5V									
25	↓	↓		↓	<5V	↓	↓	↓	↓				↓	
26	KSR[illegible]/CE	10µf		35V	12V	.4	.01[illegible]/.0[illegible]	2	1/10	.07/1			.0014/.168	
27	↓	↓		↓	12V	↓	↓	↓	↓	↓			↓	
28	CKR05/CK05	.001µf		200V	<12V	<.1	.0021	2	1/10				.0041/.041	
30	↓	↓		↓	<10V	↓								
32	CKR06/CK06	.015µf		200V	100V	↓	↓						↓	
33	CKR05/CK05	.1µf		50V	6V	<.2	.0026						.0052/.052	
34	↓	100pf	↓	200V	<10V	<.1	.0021		↓				.0042/.042	
35	BA2[illegible]	.22		200V	-1V	↓	.0006	↓	↓				.0001/.001	

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DATE: 12-75

PAGE TOTAL .0494/4.1552

FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Regulator ASSEMBLY NO.: A1 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π_A	π_{S2}	π	λ_p fpmh	REMARKS
CR 1	1N4148		Jan/Com	100V 200mA	12V <20mA	<.1	.0021	5	5/25	.7	.7		.0257/.1286	
2	zener 1N753A		↓	400mW	<400mW	<.1	.0042	↓	↓	1			.0735/.3675	
3	↓													
4	zener 985 B			↓	↓	↓				↓			↓	
7	4 layer 5786					<.1	↓						.105/.525	
8	4148			100V 200mA	<10V <20mA	<.1	.0021			.7	.7		.0257/.1286	
9										↓			↓	
10										1			.0368/.1837	
11										1			↓	
12										.7			.0257/.1286	
13										1			.0368/.1837	
14										1				
15	↓			↓	↓					1			↓	
16	S2F			200V 1A	120V <.1A					.7			.0257/.1286	
17	4148			100V 200mA	<6V <20mA					1			.0368/.1837	
18	↓				↓	↓	↓			1			↓	
19	3SF2			200V 3A	120V .8A	.26	.0036			1.5			.0945/.4725	
20	↓		↓	↓	120V .4A	.13	.0027	↓	↓	1.5	↓		.0709/.3544	

PREPARED BY: J Suelzle
DATE: 12-75

PAGE TOTAL .877/4.3833

FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Regulator ASSEMBLY NO. A1 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATOR	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π_A	π_{S2}	π	λ_p fpmh	REMARKS
CR21	3SF2		Jan/buet	200V 3A	120V .4A	.13	.0027	5	5/25	15	.7		.0708/.3544	
22	↓		↓	↓	120V .8A	.26	.0036	↓	↓	↓	↓		.0945/.4725	
23					120V .4A	.13	.0027						.0708/.3544	
24	↓			↓	120V .4A	.13	↓			↓			↓	
29	4148			100V 200mA	<12V <20mA	<.1	.0021			.7			.0257/.1286	
31	↓			↓	<6V <20mA	↓	↓			1			.0368/.1838	
32	3SF2			200V 3A	120V <.5A	.16	.0027			.7			.3675/.3375	
34	1N749A	Zener		400mW	<2mW	<.1	.0042			1			.0735/.3675	
35	4148			100V 200mW	<3V <20mA		.0021			1			.0368/.1838	
36	3SF1		↓	100V 3A	<6V <20mA	↓	.0021	↓	↓	.7	↓		.0257/.1286	
E1		1A		1A									.1	
2		↓		↓									↓	
3														
4														
5														
6		↓		↓										
7				12A									↓	

PREPARED BY: J. Suelzle
DATE: 12-75

PAGE TOTAL 1.2747/3.5655

FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Regulator ASSEMBLY NO.: A1 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π_F	π_A	π_{S2}	λ_p fpmh	REMARKS
F8				12A									.1	
9														
10														
11														
12				↓									↓	
L1		68μh	Mil/[illegible]	1.6A	T_{HS}		.002	2		3/1.5			.012/.03	
2		100μh												
3		5.6mh												
4		100μh					↓	↓		↓			↓	
Q1	2N2907		Jan/Com	60V 400mW	15V <40mW	<.1	.010	5	2/10		1.5	.36	.054/.27	
2	2N2222			15V 1/2 W	12V <50mW		.0071				1.5	.3	.0320/.1598	
3	↓		↓	↓	12V <15mW		↓		↓		1.5		↓	
4	2N[illegible]	UJT		30V 360mW	<12V <20mW		.020		40		.7		.84	
6	2N[illegible]		[illegible]	15V 1/2 W	8V <20mW		.0071		2/10		.7		.0149/.0745	
7					↓						.7		↓	
8	↓		↓	↓	6V <20mW	↓	↓	↓	↓		1.5	↓	.0320/.1598	

PREPARED BY: [illegible]
DATE: 12-75

PAGE TOTAL 1.5678/2.3584

FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Regulator ASSEMBLY NO.: A1 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π_P	π_A	π_{S2}	λ_p fpmh	REMARKS
Q 9	2N2907		Jan/TX	60V 400mW	2V 240mW	<.1	.010	5	2/10		.7	.3	.021/.105	
10	2N2219			40V 380mW	6V 100mW	.36	.0071						.0149/.0746	
11	2N2222			75V 480mW	4V <40mW	<.1								
12	↓			↓	↓		↓						↓	
13	2N2907			60V 400mW	<40mW		.010						.021/.105	
14	2N5879		↓	60V 160W	6V 6W		↓				↓	↓	↓	Tc=90°C
15	[illegible]			300V 125W	<100V 10W		.0071				.7	.36	.0179/.0895	
16					120V 8W							.48	.0239/.1193	
17														
18														
19														
20														
21	↓			↓	↓		↓				↓	↓	↓	↓
22	2N2907		Jan/TX	60V 400mW	<6V <40mW		.010				.7	.3	.021/.105	
24	↓			↓	4V <40mW	↓	↓	↓			.7	↓	↓	
PCB							.0012	2					.0024	
Connector			Mil/[illegible]				.19		4/16	.72			.206/.826	
Solder													.0044	

PREPARED BY: J Suelzle
DATE: 12-75

PAGE TOTAL .5198/2.3856

FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Bias Supply ASSEMBLY NO.: A2 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

Reference Designation	Style	Value	Reliability Grade	Rated Parameters	Operating Parameters	Stress Ratio	λ_b	π_E	π_Q	π_R	π_A	π_{S2}	λ_p fpmh	Remarks
R1	RLR/RL	150K	M/-	1/2 W	.08W	.16	.0021	5	1/5	1.1			.0116/.0578	
2	↓	30	↓	↓	.03W	<.1	.0019	↓	↓				.0095/.0475	
3	↓	15	↓	↓	.015W	↓	↓	↓	↓				↓	
4	↓	30	↓	↓	.03W	↓	↓	↓	↓				↓	
5	↓	15	↓	↓	.015W	↓	↓	↓	↓				↓	
6	↓	15	↓	↓	.015W	↓	↓	↓	↓				↓	
7	↓	30	↓	↓	.03W	↓	↓	↓	↓				↓	
8	↓	15	↓	↓	.015W	↓	↓	↓	↓				↓	
9	↓	30	↓	↓	.03W	↓	↓	↓	↓				↓	
10	↓	50	↓	3W	1W	.33	.0027	↓	↓				.0135/.0675	
F1							.1						.1	
Q1	2N6235		com	325V 46W	120V 2W	<.1	.0071	5	10		.48	1.0	.1704	T_c = 70°C
2	↓		↓	↓	↓	↓	↓	↓	↓		↓		↓	
3	↓		↓	↓	↓	↓	↓	↓	↓		↓		↓	
4	↓		↓	↓	↓	↓	↓	↓	↓		↓		↓	

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PAGE TOTAL .8827/1.867

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FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Bias Supply ASSEMBLY NO.: A2 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETER(S)	OPERATING PARAMETER(S)	STRESS RATIO	λ_b	π_E	π_Q	π_A	π_{S2}	π	λ_p f/mh	REMARKS
CR1	1N5160	4-layer	Jan/Lower	.5W	<.05W	<.1	.0021	5	5/25	.6	—		.0315/.1575	
2	S2F		JAN/ICM	200V 1A	<7V <.1A	<.1				1	.70		.0368/.1838	
3					110V <.1A									
4					<2V <.1A									
5					120V <.1A					.6	.75		.0236/.1181	
6														
7														
8														
9					<2V <.1A					1	.70		.0368/.1838	
10					<2V <.1A									
11					<24V <.1A									
12														
13														
14														
15					<12V <.1A									
16														
17														
18														

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PAGE TOTAL .6043/3.019

FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Bias Supply ASSEMBLY NO. A2 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETER(S)	OPERATING PARAMETER(S)	STRESS RATIO	λ_b	π_E	π_Q	π	π	π	λ_p f/pmh	REMARKS
C1	[illegible]	1µf	M/-	200V	120V	.6	.0005	2	1/10				.001/.01	
2	CKR/CK	.1µf	M/-	100V	13V	.13	.0026	↓	↓				.0056/.056	
3	↓	.022µf	↓	↓	2V	<.1	.0021	↓	↓				.0042/.042	
4	↓	↓	↓	↓	↓	↓	↓	↓	↓				↓	
5	↓	↓	↓	↓	↓	↓	↓	↓	↓				↓	
6	↓	↓	↓	↓	↓	↓	↓	↓	↓				↓	
7	↓	.0022µf	↓	↓	7V	↓	↓	↓	↓				↓	
8	CSR/CE	5.6µf	M/-	35V	12V	.34	.0069	↓	↓				.0138/.138	
9	↓	↓	↓	↓	↓	↓	↓	↓	↓				↓	
10	↓	10µf	↓	20V	6V	.3	↓	↓	↓				↓	
11	↓	↓	↓	↓	↓	↓	↓	↓	↓				↓	
T1	T HS	≅100	°C	Mil-Spec			.003	5	3				.045	
2	T HS	≅ ↓		↓			↓	↓	↓				.045	
PCB													.0004	
Connector													.196	
Solder													.22	

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PAGE TOTAL .5892/1.3341

FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Output stage-2 ASSEMBLY NO. A3A4 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π	π	π	λ_p f pmh	REMARKS
R1	RLR/RL	2K	M/-	1/4 W	<.025	<.1	.0019	5	1/5				.0095/.0475	
R2		300			<.025									
R3		680			<.025									
R4		1.6K												
5		↓			↓									
6		91			<.025									
7		300			<.025	↓	↓						↓	
8		27			.03	.12	.0021						.0105/.0525	
9		820			.04	.16								
10		3K			.036	.14	↓						↓	
11		68			<.025W	<.1	.0019						.0095/.0475	
12		10		↓	↓	↓	↓						↓	
13		.1		1W	.2W	.2	.0021						.0105/.0525	
14		10		1/4 W	<.025W	<.1	.0019						.0095/.0475	
15		1		1/2W	<.05W									
17		100		1/2W	.05W									
22		300		1/4 W	<.025W	↓	↓						↓	
23	↓	27	↓	↓	.03	.12	.0021	↓	↓				.0105/.0525	

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PREPARED BY: J Suelzle

DATE: 12-75

PAGE TOTAL .176/.88

FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Output Stage ASSEMBLY NO. A3A4 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π	π	π	λ_p f/10⁶h	REMARKS
R24	RLR/RL	820	M/-	1/4 W	.04 W	.16	.0021	5	1/5				.0105/.0525	
25		3K			.036	.14	↓						↓	
26		68			<.025W	<.1	.0019						.0095/.0475	
27		10		↓	↓	↓	↓						↓	
28		.1		1W	.2W	.2	.0021						.0105/.0525	
29		1		1/4W	<.025W	<.1	.0019						.0095/.0475	
30		1		1/2W	<.05W									
31		33		1/4W	<.025W									
32		100		1/2W	.05W									
34		2K		1/4W	<.025W									
35	↓	1K		↓	↓	↓	↓	↓	↓				↓	
37	Manganin wire	.01		10 W	.44W	.14							.0001	est
38	RLR/-	100		1/4 W	<.025W	<.1	.0019	5	1/5				.0095/.0475	
39		300												
40		390												
41		10K												
42		470			↓									
44	↓	2K	↓	↓	<.025W	↓	↓	↓	↓				↓	

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DATE: 12-75

PAGE TOTAL .1646/.8226

FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Output Stage ASSEMBLY NO. A3A4 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π	π	π	λ_p fpmh	REMARKS
R45	RLR/–	33	M/–	1/4W	<.025W	<.1	.0019	5	1/5				.0095/.0475	
46		1K												
49		1K												
50		1K												
51		2K												
52		2K												
53		47												
54	↓	↓	↓	↓	↓	↓	↓	↓	↓				↓	
C1	CKR/CK	560pf	M/–	200V	<2V	<.1	.002	2	1/10				.004/.04	
2		↓		↓	2V									
3		220pf		[illegible]V	<3V									
4		.01µf			6V									
5		↓			6V									
6		.001µf			2V									
7		.0015µf		100V	9V	↓	↓						↓	
8		330pf		200V	120V	.6	.017						.034/.34	
9	↓	.047µf	↓	50V	2V	<.1	.002	↓	↓				.004/.04	

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PREPARED BY: J Suelzle
DATE: 12-75

PAGE TOTAL .142/1.04

FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Output Stage ASSEMBLY NO. A3, A4 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π_{SR}	π	π	λ_P fpmh	REMARKS
10	CSR CE	220µf	M/Lower	10V	6V	.6	.023/.177	2	1/10	.07/1			.0032/1.7	
11	↓	↓		↓	6V	↓	↓	↓	1/10	.07/1			↓	
12	CKR/CK	220pf		200	-2V	<.1	.002	2	1/10				.004/.04	
13		.01µf		200	6V									
14		↓			6V									
15		.001µf		↓	2V									
16		.0015µf		100V	9V	↓	↓						↓	
17		300pf		200	120V	.6	.017						.034/.34	
18	↓	.047µf		50V	2V	<.1	.002	↓	↓				.004/.04	
19	CSR/CE	220µf		10V	6V	.6	.023/.177	2	1/10	.07/1			.0032/1.7	
20	↓	↓		↓	6V		↓		↓	↓			↓	
21	CQR/CQ	5µf		200V	120V	↓	.0005	↓	1/10				.0005/.005	
22	CKR/CK	.01µf		200V	<1V	<.1	.002	2	1/10				.004/.04	
23		.47µf		50	1.5V									
24		.1µf		100	6V									
25				↓	6V									
26	↓	.022µf	↓	[illegible]	<.5V	↓	↓	↓	↓				↓	

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FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Output Stage ASSEMBLY NO. A3,A4 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π_A	π_{S2}	π	λ_p fpmh	REMARKS
CR1	35F1		JAN/Lot	100V 3A	6V <1A	.3	.0036	5	5/25	1.5	.7		.0945/.4725	
2	↓		↓	↓	6V <.1A	<.1	.0021	↓	↓	1	↓		.0367/.1837	
3					6V <1A	.3	.0036			1.5			.0945/.4725	
4					6V <.1A	<.1	.0021			1			.0367/.1837	
5					6V <1A	.3	.0036			1.5			.0945/.4725	
6					6V <.1A	<.1	.0021			1			.0367/.1837	
7					6V <1A	.3	.0036			1.5			.0945/.4725	
8	↓			↓	6V <.1A	<.1	.0021			1			.0367/.1837	
9	1N4148			100V 200mA	5V <10mA	<.1	↓			1			↓	
10	↓			↓	↓	↓				↓				
11					<12V <20mA					.6			.022/.11	
13	↓			↓	↓	↓	↓			1	↓		.0367/.1837	
15	1N4148			100V 200mA	<12V <20mA	<.1	.0021			1	.7		.0367/.1837	
16	↓			↓	↓	↓	↓			↓	↓		↓	
17														
18	↓			↓	↓	↓	↓			↓	↓		↓	
19	1N5230		↓	400mW	.04W	.1	.0042	↓	↓	1			.105/.525	

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FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Output Stage ASSEMBLY NO. A3, A4 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π_A	π_{S2}	π	λ_p fpmh	REMARKS
CR21	S2F		Jan/low	200V 1A	120V <100mA	<.1	.0021	5	5/25	1	.7		.0367/.1837	
22	1N4148		↓	100V 200mA	0V <20mA	↓	↓	↓	↓	1	↓		↓	
23	3SF1			100V 3A	≤1V ≤.3A					.6			.022/.11	
24	1N4148			100V 200mA	≤12V <20mA					1			.0367/.1837	
25	↓			↓	↓					↓			↓	
26														
27	↓			↓	↓	↓	↓			↓	↓		↓	
28	1N5230			400mW	.04W	.1	.0042			1			.105/.525	
29	S2F		↓	200V 1A	120V <100mA	<.1	.0021	↓	↓	1	.7		.0367/.1837	
31	3SF1			100V 3A	<1V <.3A	<.1	.0021	5	5/25	.6	.7		.022/.11	
32	1N4148			100V 200mA	<1V <20mA	↓	↓	↓	↓	1	↓		.0367/.1837	
33	↓				↓	↓	↓	↓	↓	↓	↓		↓	
T1													.0029	
			↓											
AR1	741		Jan/Com	$\pi_L=1$	$C_1=.006$ $C_2=.014$	$\pi_{L2}=2.5$ $\pi_T=1$	.029		2/150				.058/4.35	

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FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Output Stage ASSEMBLY NO. A3, A4 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π_A	π_{S2}	π	λ_p f/mh	REMARKS
Q 1	2N2907		JAN/com	6?V .4	≤12V <50mW	<.1	.010	5	2/10	.7	.3		.021/.105	
2	2222			75V .5W	<12V <50mW		.0071				↓		.0149/.0745	
3	3440			250 1W	125V <10mW					↓	.75		.0372/.1864	
4	2222			75V .5W	<12V <50mW		↓			1.5	.3		.0320/.16	
5	2907			60V .4W	11V 25mW		.010			.7			.021/.105	
6	2222			75V .5W	11V 11mW		.0071			1.5			.0320/.16	
7	↓		↓	↓	11V 70mW				↓	.7			.0149/.0745	
8	5881		com	60V 135W	12V 3W				10	↓			.0745	$T_c = 90°C$
9	2222		JAN/com	75V .5W	3V <20mW				2/10	1.5			.0320/.16	
10	2222			↓	11V 11mW		↓			.7			.0149/.0745	
11	2907		↓	60V .4W	11V .1W		.010		↓				.021/.105	
12	5879		com	60V 135W	11V <1W	↓	↓		10		↓		.105	
13	SDT12303		Hi Rel	300V 200W	125V <5W	<.1	.0071		2		.75		.0372	$T_c = 90°C$
14														
15														
16	↓		↓	↓	↓		↓		↓		↓		↓	↓
17	2907		JAN	60V .4W	11V 25mW		.010		2/10	↓	.3		.021/.105	
18	2222		↓	75V .5W	11V 11mW	↓	.0071	↓	↓	1.5	↓		.0320/.16	

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PAGE TOTAL .6222/1.7982

FAILURE RATE DETERMINATION

EQUIPMENT 61088-2 ASSEMBLY Output Stage ASSEMBLY NO. A3, A4 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π_A	π_{S2}	π_ρ	λ_p f/mh	REMARKS
Q19	2N2222		JAN/Com	30V .5W	11V 70mW	<.1	.0071	5	2/10	.7	.3		.0149/.0745	
20	5881		com	60V 135W	12V 3W	↓	↓	↓	10	↓	↓		.0745	
21	2222		JAN/com	75V .5W	3V <20mW				2/10	1.5			.0320/.16	
22	↓		↓	↓	11V 6mW		↓			.7			.0149/.0745	
23	2907		↓	60V .4W	6V 3mW		.010		↓				.021/.105	
24	5879		com	60V 135W	11V <1W		↓		10		↓		.105	
25	SDT2303		Hi-Rel	300V 200W	125V <5W		.0071		2		.75		.0372	T_c=90°C
26														
27														
28	↓		↓	↓	↓		↓		↓		↓		↓	↓
29	2907		Jan/Com	60V .4W	11V 25mW		.010		2/10		.3		.021/.105	
31	↓			↓	↓									
33	2907			60V .4W	6V 3mW									
34	↓		↓	↓	↓	↓	↓	↓	↓	↓	↓		↓	
Connector			Mil/Lower				.019		4/16			2.72	.206/.826	
FI-16	.1 X 16												1.6	
PCB							.0012	2					.0024	
Solder													.00044	

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PAGE TOTAL 2.304/3.696

FAILURE RATE DETERMINATION

EQUIPMENT 610'2-2 ASSEMBLY Logic ASSEMBLY NO. A5 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETER(S)	OPERATING PARAMETER(S)	STRESS RATIO	λ_b	π_E	π_Q	π_R	π	π_V	λ_p fpmh	REMARKS
R1	RLR/RL	20K	M/-	1/4W	.029W	.11	.0021	5	1/5				.0105/.0525	
2		36K			<.025W	<.1	.0019						.0095/.0475	π_{eff} of
3	↓	10K	↓				↓	↓	↓				↓	RJ's = 1
4	RJ	10K	Com				.105	3	4				1.26	when wiper
5	RNR/RN	12.4K	M/-				.0019	2.5	1/5				.0048/.0238	failure is
6	RLR/RL	3K						5	1/5				.0095/.0475	non catastrophic
7	RNR/RN	12.4K						2.5	1/5				.0048/.0238	
8	RLR/RL	20K						5	1/5				.0095/.0475	
9	RNR/RN	118K	↓				↓	2.5	1/5	1.1			.0053/.0264	
10	RJ	50K	Com				.105	3	4				1.26	
11	RNR/RN	116K	M/-				.0019	2.5	1/5	1.1			.0053/.0264	
12	RLR/RL	43K	↓	↓			.0019	5	1/5				.0095/.0475	
13	RJ	100K	Mil/Com	1/4W			.105	3	2/4	1.1		1	.62/1.26	
14	RLR/RL	30K	M/-				.0019	5	1/5				.0095/.0475	
15														
16		↓												
17		100K												
18	↓	12K	↓	↓	↓	↓	↓	↓	↓				↓	

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PAGE TOTAL 3.2657/4.4079

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FAILURE RATE DETERMINATION

EQUIPMENT 61198-2 ASSEMBLY LOGIC ASSEMBLY NO. 45 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETER(S)	OPERATING PARAMETER(S)	STRESS RATIO	λ_b	π_E	π_G	π_R	π_V	π	λ_p f/mh	REMARKS
R19	RJ	20K	MIL/Com.	1/4 W	<.025W	<.1	.105	3	2/4		1		.63/1.24	π_{ecc} = 1
20	RLR/RL	100K	M/-				.0019	5	1/5	1.1			.0104/.0522	
21	↓	20K	↓		↓	↓	↓	↓	↓				.0095/.0475	
22	↓	39K	↓		↓	↓	↓	↓	↓				↓	
23	↓	18K	↓		↓	↓	↓	↓	↓				↓	
24	RJ	20K	MIL/Com		.029W	.12	.120	3	2/4		1		.72/1.44	π_{ecc} = .9
25	RLR/RL	25K	M/-		<.025W	<.1	.0019	5	1/5				.0095/.0475	
26	↓	150K	↓		↓	↓	↓	↓	↓	1.1			.0104/.0522	
27	↓	↓	↓		↓	↓	↓	↓	↓	1.1			↓	
28	↓	15K	↓		↓	↓	↓	↓	↓				.0095/.0475	
29	↓	6.8K	↓		↓	↓	↓	↓	↓				↓	
30	↓	15K	↓		↓	↓	↓	↓	↓				↓	
31	↓	↓	↓		↓	↓	↓	↓	↓				↓	
32	↓	2K	↓		↓	↓	↓	↓	↓				↓	
33	↓	↓	↓		↓	↓	↓	↓	↓				↓	
34	↓	8.2K	↓		↓	↓	↓	↓	↓				↓	
35	↓	↓	↓		↓	↓	↓	↓	↓				↓	
36	↓	4.7K	↓	↓	↓	↓	↓	↓	↓				↓	

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PAGE TOTAL 1.4944/3.4541

FAILURE RATE DETERMINATION

EQUIPMENT______ ASSEMBLY______ ASSEMBLY NO.______ ASSEMBLY TEMP.______ ENVIRONMENT______

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π	π	π	λ_p f pr h	REMARKS
R37	RLR/RL	4.7K	M/-	1/4W	<.025W	<.1	.0019	5	1/5				.0095/.0475	
38		2.4K												
39		3.6K												
40		2.4K												
41		3.6K												
42		390												
43		390												
44		2K												
45		5.1K												
46		5.6K												
47		5.6K												
48		11K												
49		20K			↓	↓	↓						↓	
50		820			.046	.18	.0021						.0105/.0525	
51		16K			<.025	<.1	.0019						.0095/.0475	
52		12K												
53		3K												
54	↓		↓	↓	↓	↓	↓	↓	↓				↓	

PAGE TOTAL .172/.86

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FAILURE RATE DETERMINATION

EQUIPMENT______ ASSEMBLY______ ASSEMBLY NO.______ ASSEMBLY TEMP.______ ENVIRONMENT______

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π_R	π_V	π	λ_p f/m.h	REMARKS
R55	RCR/RC	1Meg	M/–	1/4W	<.025W	<.1	.0007	2	1/5				.0014/.007	
56	↓	820K	↓	↓			↓	↓	↓				↓	
57	RLR/RL	5.1K	M/–				.0019	5	1/5				.0095/.0475	
58	↓	↓	↓	↓			↓	↓	↓				↓	
59	RJ	50K	M.1/com	1/4W		<.1	.105	3	2/4		1		.62/1.24	π_{eff} = .88
60	RLR/RL	300K	M/–			<.1	.0019	5	1/5	1.1			.0104/.0522	
61		7.5K											.0095/.0475	
62		↓											↓	
63	↓	100K	↓	↓			↓	↓	↓	1.1			.0104/.05[illegible]	
64	RCR/RC	1Meg	M/–	1/4W			.0007	2	1/5				.0014/.007	
65	↓	↓					↓	↓	↓				↓	
66	RLR/RL	3.9K					.0019	5	1/5				.0095/.0475	
67		↓												
68	↓	2.2K	↓	↓			↓	↓	↓				↓	
69	RJ	10K	M.1/com	1/4W			.105	3	2/4		1		.62/1.24	π_{eff} = 1
70	RLR/RL	6.2K	M/–				.0019	5	1/5				.0095/.0475	
71		3.9K												
72	↓	↓	↓	↓	↓	↓	↓	↓	↓				↓	

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PAGE TOTAL 1.3614/3.0874

FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Logic ASSEMBLY NO. A5 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATOR	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETER(S)	OPERATING PARAMETER(S)	STRESS RATIO	λ_b	π_E	π_Q	π	π_V	π	λ_p f pmh	REMARKS
R73	RLR/RL	10	M/-	1/4W	<.025	<.1	.0019	5	1/5				.0095/.0475	
74	↓	↓	↓	↓	↓	↓	↓	↓	↓				↓	
75		51			.08W	.16	.0021						.0105/.0525	
76		2K			<.025W	<.1	.0019						.0095/.0475	
77		1.3K												
78		20K												
79		2.7K												
80		10K												
81		200												
82		10K												
83		12K												
84		30K												
85		2K												
86		20K												
87	↓	1K	↓	↓		↓	↓	↓	↓				↓	
88	RJ	50K	Mil/Com	1/4W		.1	.105	3	2/4		1		.62/1.24	π_{eff} = .72
89	RLR/RL	51K	M/-				.0019	5	1/5				.0095/.0475	
90	↓	30K	↓	↓	↓	↓	↓	↓	↓				↓	

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PAGE TOTAL .877/2.0525

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FAILURE RATE DETERMINATION

EQUIPMENT 61095-2 ASSEMBLY LOGIC ASSEMBLY NO. A5 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π_R	π_V	π	λ_p f/10⁶ h	REMARKS
R91	RLR/RL		M/-	1/4W	<.025W	<.1	.0019	5	1/5				.0095/.0475	
92	↓	18K	↓	↓	↓	↓	↓	↓	↓				↓	
93	RCR/RC	2Meg	M/-	1/4W	↓		.0007	2	1/5	1.6			.0022/.0122	
													—	
95	RLR/RL	2K	M/-	1/4W			.0019	5	1/5				.0095/.0475	
96		6.2K												
97		2K												
98		2K												
99		5.6K												
100	↓	33	↓	1/2W	.16W	.32	.0627	↓	↓				.0135/.0675	
101	RJ	20K	Hi-Rel/com	1/4W	<.025W	<.1	.105	3	2/4		1		.62/1.24	π_{eff} = .25
102	RLR/RL	5.6K	M/-				.0019	5	1/5				.0095/.0475	
103		↓												
104		13K												
105	↓	1K	↓	↓			↓	↓	↓				↓	
106	RJ	50K	Hi-Rel/com	1/4W	↓	↓	.105	3	2/4		1		.62/1.24	π_{eff} = [illegible]
[illegible]	RLR/RL	200K	M/-		.05	.2	.0021	5	1/5				.0105/.0525	
[illegible]	↓	12K	↓	↓	<.025W	<.1	.0019	↓	↓				.0095/.0475	

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PAGE TOTAL 1.3802/3.1822

FAILURE RATE DETERMINATION

EQUIPMENT 1098-2 ASSEMBLY Logic ASSEMBLY NO. A5 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π_R	π	π	λ_p fpmh	REMARKS
R109	RLR/RL	300K	M/-	1/4 W	<.025W	<.1	.0019	5	1/5				.0095/.0475	
110		39K												
111		1K												
112		200K								1.1			.0104/.0522	
113		20K											.0095/.0475	
114		2.2K												
115		120K												
116		10 K												
117		62K												
118		470												
119		11K												
120		2K												
121		5.6K												
122		2K												
123		33		1/2 W	.053W	.11	.0021						.0105/.0525	
124		10K		1/4W	<.025W	<.01	.0019						.0095/.0475	
125		2K												
126		12K												

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FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Logic ASSEMBLY NO. A5 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π	π	π	λ_p f pmh	REMARKS
R27	RLR/RL	12K	M/-	1/4W	<.025W	<.1	.0019	5	1/5				.0095/.0475	
AR1	LM741	JANB/com		C_1=.0048, C_2=.0074	π_L=1, N_F=22			4	2/150				.0678/5.085	
2	↓							↓	↓				↓	
3	↓							↓	↓				↓	
4	↓							↓	↓				↓	
5	LM748							↓	↓				↓	
6	↓							↓	↓				↓	
7	LM74							↓	↓				↓	
8	↓							↓	↓				↓	
9	↓							↓	↓				↓	
10	↓							↓	↓				↓	
12	↓							↓	↓				↓	
14	LM74							↓	↓				↓	
U1	8038AM	—		C_1=.0069, C_2=.0095	π_L=1, N_T=50	π_T=.8		4	150				6.735	
U2	8038BM	—						0	↓				↓	

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DATE: 12-75

PAGE TOTAL 4.2931/74.5375

FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Logic ASSEMBLY NO. A5 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π_{SR}	π	π	λ_p fpmh	REMARKS
C1	CKR/CK	.01µf	M/–	100V	24V	.3	.0041	2	1/10				.0082/.082	
2	↓	.022µf		50V	3.6V	<.1	.0021	↓	↓				.0042/.042	
3	CQR/CQ	.033µf		50V	15V	.3	.00008	2	1/10				.00016/.0016	
4	CKR/CK	.01µf		100V	<1V	<.1	.0021	2	1/10				.0042/.042	
5		↓		↓	<12V	.12	.0026	2	1/10				.0052/.052	
6		.06µf		50V	8V	.16	↓	↓	↓				.0052/.052	
7		.01µf		100V	8V	<.1	.0021	2	1/10				.0042/.042	
8	CSR/CE	.47µf		35V	1V		.0055/.0777	2	1/10	.07/1			.00077/1.554	
9	CKR/CK	.015µf		50V	9V		.0021	2	1/10				.0042/.042	
10		.01µf		100V	↓								.0042/.042	
11		100pf		200V	10V								.0042/.042	
12		↓		↓	↓	↓	↓						.0042/.042	
13		.01µf		100V	12V	.12	.0026						.0052/.052	
14					↓								.0052/.052	
15					12V								.0052/.052	
16					↓	↓	↓						.0052/.052	
17		.047µf		50V	12V	.24	.0041						.0082/.082	
18	↓	↓	↓	↓	↓	↓	↓	↓	↓				.0082/.082	

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DATE: 12-5

PAGE TOTAL .08613/2.4076

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FAILURE RATE DETERMINATION

EQUIPMENT 61198-2 ASSEMBLY Logic ASSEMBLY NO. A5 ASSEMBLY TEMP. 15°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π_{SR}	π	π	λ_p f/10⁶ h	REMARKS
C19	CKR/CK	.01µf	M/-	100V	6V	<.1	.0021	2	1/10				.0042/.042	
20	CSR/CE	5.6µf	↓	35V	4V	.11	.0061/.0854	↓	↓	.07/1			.00854/1.618	
21	↓	2.2µf	↓	20V	2V	.1	↓	↓	↓	↓			.00854/1.618	
22	CKR/CK	.01µf	↓	100V	<1V	<.1	.0021	2	1/10				.0042/.042	
			↓											
			↓											
25	CSR/CE	1.2µf	↓	20V	2V	.1	.0055/.0777	2	1/10	.07/1			.00777/1.554	
26	CKR/CK	.01µf	↓	100V	12V	.12	.0026	2	1/10				.0052/.52	
27	↓	↓	↓	↓	↓	↓	↓	↓	↓				.0052/.052	
28	CMR/CM	.0022µf	↓	100V	15V	.15	.0006	4	1/10				.0024/.024	
29	CKR/CK	.47µf	↓	50V	2V	<.1	.0021	2	1/10				.0042/.042	
30	↓	↓	↓	↓	↓	↓	↓	↓	↓				.0042/.042	
31	↓	.047µf	↓	↓	↓	↓	↓	↓	↓				.0042/.042	
32	↓	↓	↓	100V	↓	↓	↓	↓	↓				.0042/.042	
33	↓	.01µf	↓	↓	↓	↓	↓	↓	↓				.0042/[illegible]	
34	CSR/CE	10µf	↓	20V	12V	.6	.023/.1775	↓	↓	.07/1			.00322/3.55	
35	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓			.00322/3.55	
36	CKR/CK	47µf	↓	100V	.2mV	<.1	.0021	2	1/10				.0042/.042	
												PAGE TOTAL	.0553[illegible]/12.354	

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DATE: 1-5

D33

FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Logic ASSEMBLY NO. A5 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π_{SR}	π	π	λ_p fpmh	REMARKS
C37	CKR/CK	.01μf	M/-	100V	12V	.12	.0026	2	1/10				.0052/.052	
38	↓	↓	↓	↓	↓	↓	↓	↓	↓				.0052/.052	
41	CSR/CE	5.6μf	↓	35V	1V	<.1	.0055/.777	2	1/10	.07/1			.0077/1.554	
43	CKR/CK	.47μf	↓	50V	12V	.24	.0041	2	1/10				.0082/.082	
44	↓	.01μf	↓	100V	<1V	<.1	.0021	↓	↓				.0042/.042	
45	↓	↓	↓	↓	<2V	↓	↓	↓	↓				.0042/.042	
46	↓	.1μf	↓	100V	<1 V	↓	↓	↓	↓				.0042/.042	
47	↓	.0015μf	↓	↓	3V	↓	↓	↓	↓				.0042/.042	
48	↓	↓	↓	↓	↓	↓	↓	↓	↓				.0042/.042	
49	CR/CM	.0047μf	↓	100V	15V	.15	.0006	4	1/10				.0024/.024	

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PAGE TOTAL .04277/1.97

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FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Logic ASSEMBLY NO. A5 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π_A	π_{S2}	π	λ_p f pmh	REMARKS
CR1	IN4148		Jan/com	100V 200mA	<12V <20mA	<.1	.0049	5	5/25		.7		.08575 / .42875	
2	↓		↓	↓	↓	↓	↓	↓	↓		↓		.08575 / .42875	
3	↓		↓	↓	↓	↓	↓	↓	↓	↓	↓		.08575 / .42875	
4	↓		↓	↓	↓	↓	↓	↓	↓	↓	↓		.08575 / .42875	
5	↓		↓	↓	↓	↓	↓	↓	↓	↓	↓		.08575 / .42875	
6	↓		↓	↓	↓	↓	↓	↓	↓	↓	↓		.08575 / .42875	
8	IN823	Ref	↓	250mW	45mW	.18	.0048	↓	↓	1.5			.18 / .90	
9	IN4148		↓	100V 200mA	<12V <20mA	<.1	.0049	↓	↓	.6	.7		.05145 / .25725	
10	↓		↓	↓	↓	↓	↓	↓	↓	↓	↓		.05145 / .25725	
11	↓		↓	↓	↓	↓	↓	↓	↓	↓	↓		.05145 / .25725	
12	↓		↓	↓	↓	↓	↓	↓	↓	↓	↓		.05145 / .25725	
13	↓		↓	↓	↓	↓	↓	↓	↓	↓	↓		.05145 / .25725	
14	↓		↓	↓	↓	↓	↓	↓	↓	↓	↓		.05145 / .25725	
15	IN753A	Zener	↓	400mW	<40mW	↓	.0042	↓	↓	1			.105 / .525	
16	IN4148		↓	100V 200mA	<12V <20mA	↓	.0049	↓	↓	.6	.7		.05145 / .25725	
17	↓		↓	↓	↓	↓	↓	↓	↓	↓	↓		.05145 / .25725	
18	IN753A	Zener	↓	400mW	35mW	↓	.0042	↓	↓	1			.105 / .525	
19	IN4148		↓	100V 200mA	<12V <20mA	↓	.0049	↓	↓	.6	.7		.05145 / .25725	

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PAGE TOTAL 1.56755 / 7.83775

FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Logic ASSEMBLY NO. A5 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REF. DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_G	π_A	π_{S2}	π	λ_p f/pmh	REMARKS
CR21	1N4148		JAN[illegible]	155V 200mA	<12V <20mA	<.1	.0049	5	5/25	1	.7		[illegible]	
22	↓		↓	↓	↓	↓	↓	↓	↓	1	↓		[illegible]	
23	1N754A	Zener		400mW	<40mW		.0042			1			[illegible]	
24	1N4148			100V 200mA	<12V <200mA		.0049			1	.7		[illegible]	
25	↓			↓	↓	↓	↓			1	↓		[illegible]	
27	1N4148		↓	100V 200mA	<12V <20mA	<.1	.0049	↓	↓	.6	.7		[illegible]	
L1	Type U	33 NH	M.1	T_{HS}<100°C			.003	5	3				.045	
2	[illegible]	↓	↓	↓	↓		.003	↓	↓				↓	

PREPARED BY: J [illegible]

DATE: 12-75

PAGE TOTAL [illegible]

FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Logic ASSEMBLY NO. A5 ASSEMBLY TEMP. 55°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π_A	π_{S2}	π	λ_p f/mh	REMARKS
Q1	2N3822	FET	JAN/Com	50V 260mW	<5V <4mW	<.1	.020	5	2/10	1.5			[illegible]	
2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓			[illegible]	
3	3N171	MOSFET	Com	35V 330mW	3V 2.3mW		↓		10	.7			[illegible]	
4	2N2222		JAN/Com	75V .5W	<7V <40mW		.0071		12/10	.7	.3		[illegible]	
5	↓			75V .5W	↓	↓	↓			.7			[illegible]	
6	2N2907			60V 1.8W	<12V <.1W	<.1	.010			1.5			[illegible]	
7	↓			↓	↓	<.1	↓			↓			[illegible]	
8	2N2222			75V .5W	24V <.05W	<.1	.0071			.7			[illegible]	
9	2N2907			60V 1.8W	<1V [illegible]		.010			.7			[illegible]	
10	2N2222			75V .5W	24V <40mW		.0071						[illegible]	
11	2N2907			60V 1.8W	<12V <40mW		.010			↓			[illegible]	
12					<12V <40mW					1.5			[illegible]	
13	↓			↓	<12V [illegible]		↓			.7			[illegible]	
14	2N2222			75V .5W	<7V <40mW		.0071			.7			[illegible]	
15	2N2907		↓	60V 1.8W	<8V <40mW	↓	.010	↓	↓	.7	↓		[illegible]	

PAGE TOTAL [illegible]

PREPARED BY: [illegible signature]
DATE: 12-75

FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Output filter ASSEMBLY NO. A6 ASSEMBLY TEMP. 65°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π	π	π	λ_p f.p.m.h	REMARKS
L1	$T_{HS} \leq 100°C$		M.I. Spec type V		insul		.003	5	3				.045	
L2							↓	↓	↓				.045	
C1	CQR/CQ	5 µf	+/-	200V	120V	.6	.0005	2	1/10				.001/.01	
C2	↓	↓	↓	↓	↓	↓	↓	↓	↓				.001/.01	

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PAGE TOTAL .092/.11

PAGE 1 OF 1

FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Boost & Filter ASSEMBLY NO. A7 ASSEMBLY TEMP. 65°C ENVIRONMENT G_F

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π_A	π_{S2}	π	λ_p f/mh	REMARKS
CR1	MR[illegible]SL		com	150V 100A	66V <1A	<.1	.0021	5	25	.6	.7		.1102	
CR2	5C5F4		↓	400V 160A	<120V 20A	.2	.0033	5	25	1.5	.7		.4331	T_c = 96°C
L1	see chassis magnetics calculations												.045	
T1													.045	
T2													↓	

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PAGE TOTAL .6783

PAGE 1 OF 1

FAILURE RATE DETERMINATION

EQUIPMENT 2198-2 ASSEMBLY Inverter ASSEMBLY NO. A8 ASSEMBLY TEMP. 60°C ENVIRONMENT GF

REFERENCE DESIGNATION	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETER(S)	OPERATING PARAMETER(S)	STRESS RATIO	λ_b	π_E	π_Q	π_R	π	π	λ_P f pmh	REMARKS
R1	RLR/RL	47K	M/-	1W	.5W	.5	.0029	5	1/5				.0145/.0725	
R2	↓	1.5K	↓	1/4W	.03W	.15	.0020	↓	↓				.01/.05	
3		100		10W	1W	.1	.0018						.009/.045	
4	↓	1K	↓	4W	<.025	<.1	↓	↓	↓				↓	
5	RWR/RW	1.5		1/2W	<.025	<.1	.0042	3	1/5	1			.0126/.063	
6	RLR/RL	22K		1/2W	.3	.6	.0033	5	↓				.0165/.0825	
7	↓	240K		1/4W	.032W	.13	.0020	↓		1.1			.011/.055	
8		470	↓		<.025	<.1	.0018						.009/.045	
9		2.2K			<.025	<.1	↓						↓	
10		1K			↓	↓								
11	↓	470		↓	↓	↓	↓	↓					↓	
12	RWR/	1.5		1/2W	<.025	<.1	.0042	3					.0126/.063	
13	RLR/RL	1K		4W	↓	↓	.0018	5					.009/.045	
14	↓	1.5K		1/4W	.03	.15	.0020	↓					.01/.05	
15		470		↓	<.025	<.1	.0018						.009/.045	
16		240K		↓	.032	.13	.0020			1.1			.011/.055	
17		22K		1/2W	.3	.6	.0033						.0165/.0825	
18	↓	47K		1W	.5W	.5	.0029	↓	↓				.0145/.0725	

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PAGE TOTAL .2012/1.006

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FAILURE RATE DETERMINATION

EQUIPMENT 1695-2 ASSEMBLY Inverter ASSEMBLY NO. 38 ASSEMBLY TEMP. 60°C ENVIRONMENT GF

REFERENCE DESIGNATOR	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π_{SR}, π_{S2}	π_A ($\pi_C = 1$)	λ_p for n	REMARKS
R20	RLR/RL	2.2K		1/4W	<.25W	<.1	.0018	5	1/5			.009/.045	
21	↓	470		↓	↓	↓	↓	↓	↓			↓	
22	↓	1K		↓	↓	↓	↓	↓	↓			↓	
C1	CSR/CE	10µf	M/lower	200V	125V	.625	.032/.185	2	1/10	.07/1		.0045/3.7	
2	CKR05/CK05	100pf	M/–	200V		.55	.018	2	1/10			.036/.36	
3	CQR/CQ	.68µf		300V	125V	.417	.0002	2	1/10			.0004/.004	
4	CKR05/CK05	100pf	M/–	200V		.55	.018	2	1/10			.036/.36	
5	CQR/CQ	.68µf		300V	125V	.417	.0002	2	1/10			.0004/.004	
CR1	S2F		JAN/lower	200V 1A	125V <.1A	<.1	.0019	5	5/25	.75	.6	.013/.106	
2			↓	↓	100V <.1A	↓	↓	↓	↓	.70	1	.033/.166	
3			↓	↓	125V <.1A	↓	↓	↓	↓	.75	.6	.013/.106	
4			↓	↓	125V <.1A	↓	↓	↓	↓	↓	↓	↓	
5			↓	↓	100V <.1A	↓	↓	↓	↓	↓	↓	↓	
6			↓	↓	100V <.1A	↓	↓	↓	↓	.70	1	.033/.166	
F1												.1	

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PAGE TOTAL .3621/5.419

FAILURE RATE DETERMINATION

EQUIPMENT 61098-2 ASSEMBLY Inverter ASSEMBLY NO. A8 ASSEMBLY TEMP. [illegible] C ENVIRONMENT GF

REFERENCE DESIGNATOR	STYLE	VALUE	RELIABILITY GRADE	RATED PARAMETERS	OPERATING PARAMETERS	STRESS RATIO	λ_b	π_E	π_Q	π_A	π_{S2}	π_P	λ_p f pmh	REMARKS
Q1	2N2907		Jan/Com	60V .4W	8V <20mW	<.1	.010	5	2/10	1.5	.3		.045/.225	
2	5416		↓	350V 1W	<10mW	<.1	.010		↓	.7	.2		.02/[illegible]	
3	6234		Com	275V 36W	125V [illegible]mW	<.1	.0071		10		.75		.1864	Tc [illegible] C
4	3439		Jan/Com	350V .7W	<35V <10mW	↓	.0071		2/10		.2		.0149/.0745	
5	6234		Com	275V 36W	125V 100mW		↓		10		.75		.1864	Tc 75 C
6	6234		↓	275V 36W	25V 188mW	↓	↓		↓	↓	↓		.1864	Tc = 75°C
7	5416		Jan/Com	350V 1W	<3[illegible] [illegible]W		.010		2/10	↓	.2		[illegible]	
8	2907		Jan/Com	60V .4W	8V <20mW	<.1	.010		↓	1.5	.3		.045/.225	
9	6234		Com	275V 36W	12.5V 100mW		.0071		10	.7	.75		.1864	T[illegible]
10	3439		Jan/Com	350V .7W	[illegible]	↓	↓	↓	2/10	↓	.3		.014[illegible]/[illegible]	
[illegible]			Mil/Lower				.[illegible]		[illegible]			2.72	[illegible]	
[illegible]							.00212						.0[illegible]1	
[illegible]													.00044	

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DATE: 12-75

PAGE TOTAL 1.1162/2.383

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APPENDIX E

COST DATA FOR THE

TRANSFORMER OUTPUT AND TRANSFORMERLESS OUTPUT

INVERTERS

In spite of the design differences, the costs of the transformer-output and transformerless-output inverters are essentially equal. The following costs are based on 1975 prices.

Source	Per unit in lots of 1	Per unit in lots of 1000
Material	$ 1865	$ 500
Production	441	200
Overhead and profit	1641	300
	$ 3947	$ 1000