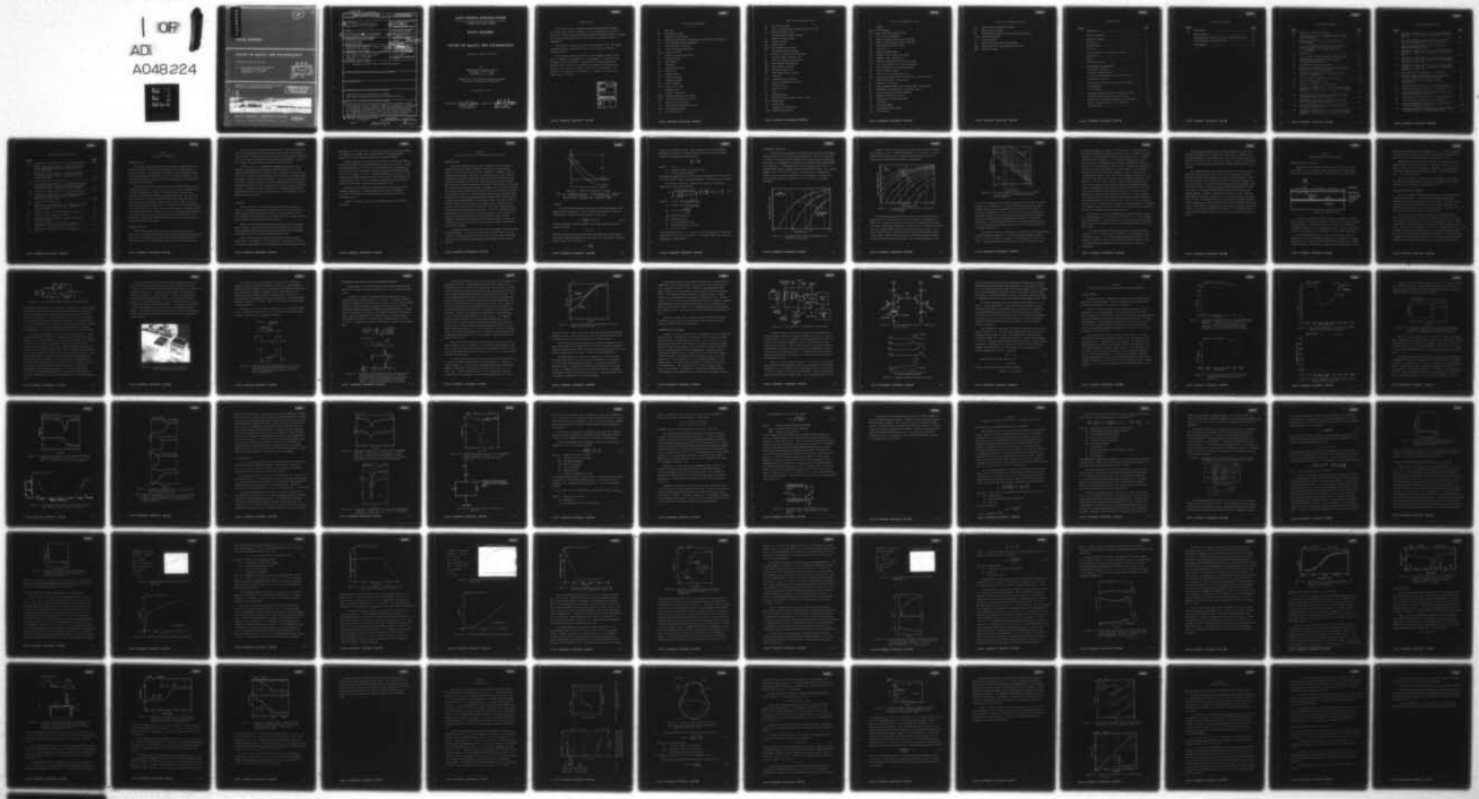
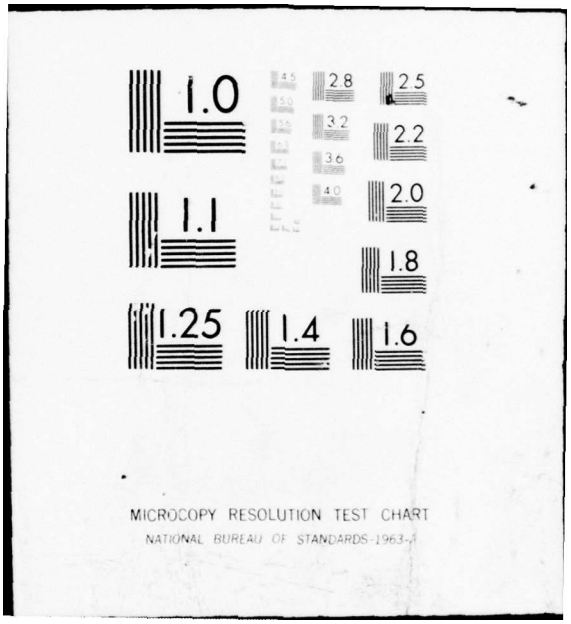
AD-A048 224 SANTA BARBARA RESEARCH CENTER GOLETA CALIF F/G 17/5
STUDY OF HGCDTE MIS TECHNOLOGY.(U)
NOV 77 D R RHIGER, J D LANGAN N00173-76-C-0316
UNCLASSIFIED NL



END
DATE FILMED
1-78
DDC


1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
4.5
5.0
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

(12) F.G

FINAL REPORT

STUDY OF HgCdTe MIS TECHNOLOGY

Contract No. N00173-76-C-0316

For - Naval Research Laboratory N00173
Code 5262, Dr. W. D. Baker
Washington, D. C. 20375

Sponsored by: Naval Electronic Systems Command
Directed by: Naval Research Laboratory

SANTA BARBARA RESEARCH CENTER
A Subsidiary of Hughes Aircraft Company
SBRC

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER
2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER

4. TITLE (and Subtitle)
(6) Study of HgCdTe MIS Technology,

5. TYPE OF REPORT & PERIOD COVERED
(9) Final Report,

6. PERFORMING ORG. REPORT NUMBER

7. AUTHOR(s)
(10) David R. Rhiger [redacted] John D. Langan

8. CONTRACT OR GRANT NUMBER(s)
(15) N00173-76-C-0316 NEW

9. PERFORMING ORGANIZATION NAME AND ADDRESS
Santa Barbara Research Center
75 Coromar Drive
Goleta, CA 93017

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
62762N
(16) F54583
(17) XF54583004

11. CONTROLLING OFFICE NAME AND ADDRESS
Naval Electronic Systems Command N00039
Code 304, L. W. Sumney
Washington, D. C. 20360

12. REPORT DATE
(11) 15 Nov [redacted] 77

13. NUMBER OF PAGES
84 (12) 82p.

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)
Naval Research Laboratory N00173
Code 5262, Dr. W. D. Baker
Washington, D. C. 20375

15. SECURITY CLASS. (of this report)
Unclassified

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

A. — Approved for public release, distribution unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Focal Plane Arrays, Infrared Arrays, HgCdTe,
Metal-Insulator-Semiconductor Devices, Photogate Detectors

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Metal-insulator-semiconductor (MIS) devices were fabricated on single-crystal HgCdTe with both 5-μm and 12-μm cutoff wavelengths. The purpose was to evaluate existing technology and identify fundamental limitations, for the application of HgCdTe to monolithic intrinsic focal plane arrays. For 12-μm material it was shown that interband tunneling provides such a large dark current that a MIS device cannot store charge effectively.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE
S/N 0102-014-6601

Unclassified
SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

* micrometer

315650

SANTA BARBARA RESEARCH CENTER
A Subsidiary of Hughes Aircraft Company
75 COROMAR DRIVE, GOLETA, CALIFORNIA

FINAL REPORT

STUDY OF HgCdTe MIS TECHNOLOGY

Contract No. N00173-76-C-0316

For

Naval Research Laboratory N00173
Code 5262, Dr. W. D. Baker
Washington, D. C. 20375

Sponsored by: Naval Electronic Systems Command
Directed by: Naval Research Laboratory

November 15, 1977

Prepared by David R. Rhiger
David R. Rhiger
Project Engineer

Approved by John D. Langan
John D. Langan
Program Manager

FOREWORD

This Final Report was prepared by Santa Barbara Research Center, 75 Coromar Drive, Goleta, California 93017 under Contract No. N00173-76-C-0316. The work was sponsored by the Naval Electronic Systems Command. The contract was monitored by Dr. W. D. Baker of the Naval Research Laboratory.

The effective date of the contract was 10 September 1976. The original completion date was 10 May 1977, which was subsequently extended to 30 October 1977.

The following employees of SBRC are acknowledged for their contributions. Samples were prepared by J. K. Campbell, F. I. Gesswein, B. F. Levenstein, and G. E. Newman. Valuable advice and discussions were provided by H. D. Adams, P. R. Bratt, R. H. Brody, C. B. Burgett, R. A. Chandos, P. S. Chia, C. A. Cockrum, R. A. Cole, S. P. Emmons, J. F. Kreider, W. E. McCary, S. F. Pellicori, F. J. Renda, K. J. Riley, R. D. Thom, and K. R. Winrich.

LIST OF SYMBOLS

A	gate area
A_D	photosensitive area
C	capacitance of MIS device
C_D	equivalent capacitance of deep depletion region (in series with C_o)
C_i	initial capacitance (deep depletion)
C_f	final capacitance (well full)
C_o	"oxide" (insulator) capacitance
C_{var}	variable capacitor
C_l	capacitor in series with detector
d	sample thickness
D	gate diameter
D^*	detectivity
E_c	conduction band edge
E_F	Fermi level
E_g	bandgap energy
E_v	valence band edge
f_c	chopper frequency
Δf	noise bandwidth
FOV	field of view, angle
g	amplifier gain
$\hbar$	Planck's constant/2π
H_{BB}	blackbody irradiance at detector
HF	labels high-frequency C-V curve
I_S	signal current at detector
J_G	thermally-generated dark current
J_{pd}	hole diffusion current
J_T	tunneling current

LIST OF SYMBOLS (Cont)

L_p	hole diffusion length
LF	labels quasi-static (low-frequency-like) C-V curve
m^*	electron effective mass
n	bulk equilibrium electron density
n_i	intrinsic electron density
N_A	acceptor density
N_D	donor density
N_{SS}	fast interface state density
p	bulk equilibrium hole density
p_s	holes per unit area in inversion layer
q	electron charge, absolute value
Q_n	electron capacity of storage well
Q_p	hole capacity of storage well
ΔQ	signal charge on detector
Q_B	background photon flux
Q_s	source photon flux at detector
R	resistance
$R(\lambda)$	responsivity at wavelength λ
s	surface recombination velocity
s_o	initial value of s
s_1	plateau value of s
t	time
Δt	integration time
$\Delta t'$	time allowed to eliminate inversion layer
T_{inj}	injection time
T_s	storage time
T	temperature of MIS device
T_{BB}	blackbody temperature

LIST OF SYMBOLS (Cont)

V	voltage
V_{FB}	V_G at flatband
V_G	gate voltage with respect to bulk
V_N	rms noise in bandwidth Δf
V_p	height of positive peak in pulsed operation
V_q	height of negative peak in pulsed operation
V_S	rms signal at amplifier output
V_T	V_G at turn-on
V_x	voltage at detector gate
V_{xo}	voltage at detector gate during reset
V_y	voltage at upper plate of C_{var}
V_{yo}	voltage at upper plate of C_{var} during reset
V_1	V_G on accumulation side in pulsed operation
V_2	V_G on depletion side in pulsed operation
W	width of depletion region
W_f	value of W when storage well is full
W_m	maximum equilibrium value of W during C-V measurement
x	mole fraction CdTe in $Hg_{1-x}Cd_xTe$
α	absorption coefficient
α	slope of applied voltage ramp in quasi-static measurement
β	blackbody-to-peak detectivity conversion factor
ϵ_s	semiconductor dielectric permittivity
η	MIS device quantum efficiency
η_s	semiconductor quantum efficiency
λ	wavelength
λ_{co}	cutoff wavelength
λ_p	wavelength at peak response
τ_p	hole lifetime

LIST OF SYMBOLS (Cont)

τ_{no}	electron bulk recombination lifetime
τ_g	bulk generation lifetime
τ_g'	bulk generation lifetime derived from Zerbst analysis
ϕ_{max}	tunneling-limited ϕ_s
ϕ_s	surface potential
ϕ_{si}	initial surface potential (deep depletion)
ϕ_{sb}	surface potential at semiconductor breakdown
$\Delta\psi_s$	storage well depth

CONTENTS

CONTENTS (Cont)

ILLUSTRATIONS

ILLUSTRATIONS (Cont)

ILLUSTRATIONS (Cont)

Section 1
REPORT SUMMARY

INTRODUCTION

This report presents the results of a program to investigate the suitability of mercury-cadmium telluride (HgCdTe) for monolithic intrinsic focal plane arrays. The approach is to fabricate, test, and analyze metal-insulator-semiconductor (MIS) structures on single-crystal HgCdTe. The work includes both the evaluation of existing technology and the identification of fundamental limitations.

MIS structures are an essential part of any monolithic intrinsic array of infrared detectors. In general, such arrays use as basic elements either the charge-coupled device (CCD) or the charge injection device (CID) structure, fabricated on a narrow bandgap semiconductor. MIS structures in the CCD serve to store and transfer signal charges within the array. In the CID they store and transfer charges and provide the means of readout from the array to the external circuit. In both types of devices MIS structures with thin metal gates may serve as the detector elements. For these reasons the adequate performance of MIS structures on narrow bandgap semiconductors is necessary for the successful operation of any monolithic intrinsic focal plane array. Furthermore MIS measurements provide unique information on material and interface properties.

PROGRAM GOALS

Goals of the program can be described in terms of the two major tasks. The first task was to fabricate single-element charge injection devices. They were to be made on single-crystal HgCdTe selected for long bulk lifetime, with both n- and p-type doping and a variety of low doping densities.

The second task was the heart of the program. The fabricated devices were to be thoroughly tested and evaluated by measurement of capacitance versus voltage, transient capacitance response, and radiometric performance. These were aided by computerized data acquisition and reduction. In addition, comparisons with theoretical estimates were to be made.

Material with a 0.1 eV bandgap was originally emphasized in the program. It is appropriate for detectors operating in the 8- to 12.5-μm spectral band because of its cutoff near 12 μm. However, during the course of the work, MIS devices on this material were found to have severely limited performance because of interband tunneling. This was shown by theoretical calculations conducted at SBRC, and by the experimental results of Section 5. Subsequent publication of a paper by Anderson[1] provided a firmer quantitative estimate of tunneling currents. (See Section 2.) Emphasis was therefore shifted with the consent of the Program Monitor, to 5 μm material, in which the bandgap is about 0.24 eV.

OVERVIEW

Section 2 outlines a tunneling calculation and presents numerical results. It is shown that for any reasonable values of surface potential and doping density interband tunneling provides such a large dark current in 12 μm material that a MIS device is not a practical means of charge storage. In 5 μm material tunneling is generally negligible.

Section 3 describes the experimental techniques used and the preparation of samples. Of particular interest are the common-mode correlated double sampling method for detector signal processing, and the application of substrate injection to the measurement of storage times.

Section 4 presents the results of high-frequency and quasi-static measurements of capacitance versus gate voltage. The minimum observed fast interface state density on 5 μm material as measured by the quasi-static

technique, is 2×10^{11} cm^{-2} eV^{-1}. For 12 μm material it is seen that charges are supplied very rapidly to the inversion layer even at liquid helium temperature. This is taken as evidence for interband tunneling.

Section 5 provides a discussion of thermal dark currents and presents results of capacitance-versus-time measurements in 5 μm material. Storage times between 100 ms and 1 sec are routinely obtained, and a storage time of 25 sec was seen in one sample. Surface recombination velocities ranged from 10^3 to less than 10 cm/sec. Storage well depths were seen up to 1 volt with storage capacities greater than 10^{11} carriers/cm^2. Injection time was measured to be 9 μsec. In 12 μm material no storage time was seen down to 200 nsec for the gate voltages and doping densities used.

Section 6 covers radiometric measurements in 5 μm material with a photogate (MIS) detector. Maximum detectivity at peak wavelength is 7.0×10^{11} cm $Hz^{\frac{1}{2}}$/watt and quantum efficiency in the semiconductor is estimated to be 0.67.

Finally, in Section 7, conclusions and implications of this work are presented.

Section 2

CALCULATION OF TUNNELING CURRENT

INTRODUCTION

Interband tunneling may have a major influence on the performance of MIS devices under certain conditions. The process is illustrated in Figure 2-1 for an n-type semiconductor in depletion. A negative voltage is applied to the metal gate, producing a surface potential ϕ_s at the insulator-semiconductor interface. When $q\phi_s > E_g$, where q is the electronic charge and E_g is the bandgap, the top of the valence band at the surface is higher than the bottom of the conduction band in the bulk. This condition is frequently encountered in the testing and operation of MIS devices, but it allows electrons to tunnel horizontally from the valence band to the conduction band, as shown by the arrow in Figure 2-1. Assuming no inversion layer is present initially, the states in the valence band are full, and the states in the conduction band, from the surface to the depth W of the depletion region, are empty. When an electron tunnels across the gap it leaves behind a hole, which becomes a member of the inversion layer. The electron, now in the conduction band, is propelled by the field into the neutral bulk. The flux of tunneling electrons is equivalent to a flux of holes into the inversion layer. For a p-type semiconductor in depletion the bands are bent downward, and the minority electrons tunnel toward the surface into the conduction band. In both cases tunneling is a source of dark current, contributing to filling of the storage well (inversion layer).

Tunneling current is a very strong function of bandgap, surface potential, and doping density. In some cases it can be much greater than any signal current or thermal dark current; in other cases it can be entirely negligible. Values are calculated in the following text for parameters in the range of interest.

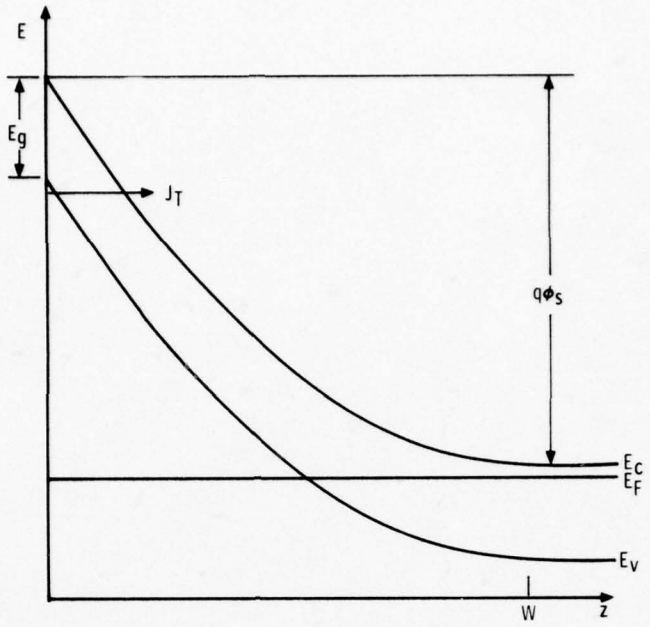


Figure 2-1. Condition for Interband Tunneling

Note: J_T = tunneling current, ϕ_s = surface potential, E_g = bandgap, E_c = conduction band edge, E_v = valence band edge, E_F = Fermi level, W = depletion width. Doping is n-type.

THEORY

The best available theoretical treatment of interband tunneling in MIS devices is that of Anderson.[1] From the WKB approximation[2,3] Anderson calculates the z-component of the tunneling current J_z as

$$J_z = \int \frac{2q}{(2\pi)^3} v_z \, T(\vec{k}) \, d^3\vec{k} \qquad (2\text{-}1)$$

where the integral is over all possible values of the electron wavevector change $\vec{k}$, given by

$$\vec{k} = \vec{k}_f - \vec{k}_i$$

Here $\vec{k}_i$ and $\vec{k}_f$ are the wavevectors of the filled initial state in the valence band and the empty final state in the conduction band, respectively. Electron group velocity in the z-direction is

$$v_z = \frac{1}{\hbar} \frac{\partial E}{\partial k_z}$$

where E is the electron energy. Also in Equation (2-1) is the tunneling probability $T(\vec{k})$ which is evaluated in terms of the electron energy within the gap. An approximation that is made is

$$\frac{m^*_i}{E_g} = \frac{3}{4}\frac{\hbar^2}{P^2}$$

where i = x, y, z

m^*_i = electron effective mass along i-axis

P = interband matrix element.

An average of published values of P according to Anderson[1] is $P = 8.4 \times 10^{-8}$ eV cm for HgCdTe. After some approximations, a formula for J_z is obtained.

The formula in Anderson's paper can be recast in a form[4] that is convenient for numerical evaluation:

$$J_T = \frac{D_1 D_3 \sqrt{N_D}\,(q\phi_s - E_g/2)^{\frac{3}{2}}}{\left[4 + \frac{D_2 E_g^2}{D_3\sqrt{N_D}}\,(q\phi_s - E_g/2)^{-\frac{1}{2}}\right]} \exp\left[-\frac{D_2 E_g^2}{D_3\sqrt{N_D}}\,(q\phi_s - E_g/2)^{-\frac{1}{2}}\right] \qquad (2\text{-}2)$$

where $D_1 = 2.2299 \times 10^{41}\ \frac{coul}{joule^2\ sec\ meter}$

$D_2 = 4.4620 \times 10^{46}\ \frac{1}{coul\ joule\ meter}$

$D_3 = 1.15265 \times 10^{5}\ \frac{meter^{\frac{1}{2}}}{farad^{\frac{1}{2}}}$

N_D = doping density in m^{-3}

E_g = bandgap in joules

ϕ_s = surface potential in volts

q = electronic charge in coulombs

$J_T = J_z/q$ in $m^{-2}\,sec^{-1}$

In the graphs (Figures 2-2, 2-3, and 2-4) in the following text, J_T has been converted from $m^{-2}\,sec^{-1}$ to $cm^{-2}\,sec^{-1}$. The values of D_1, D_2, and D_3 are appropriate for HgCdTe only.

NUMERICAL RESULTS

For three different bandgaps, tunneling current is shown versus doping density in Figure 2-2 for a fixed surface potential of 1 volt. It is clear that J_T changes by several orders of magnitude for small changes in N_D and E_g. Also shown is an estimate of thermally-generated dark current from Equation (5-3) of Section 5. Tunneling becomes a serious problem only when J_T is approximately equal to or larger than the thermal dark current. For a typical doping of $N_D = 5 \times 10^{14}$ cm^{-3} Figure 2-2 shows that J_T is prohibitively large in 12 μm material and negligible in 5 μm material. In fact the 5 μm material can be doped to more than 2×10^{15} cm^{-3} before J_T becomes significant.

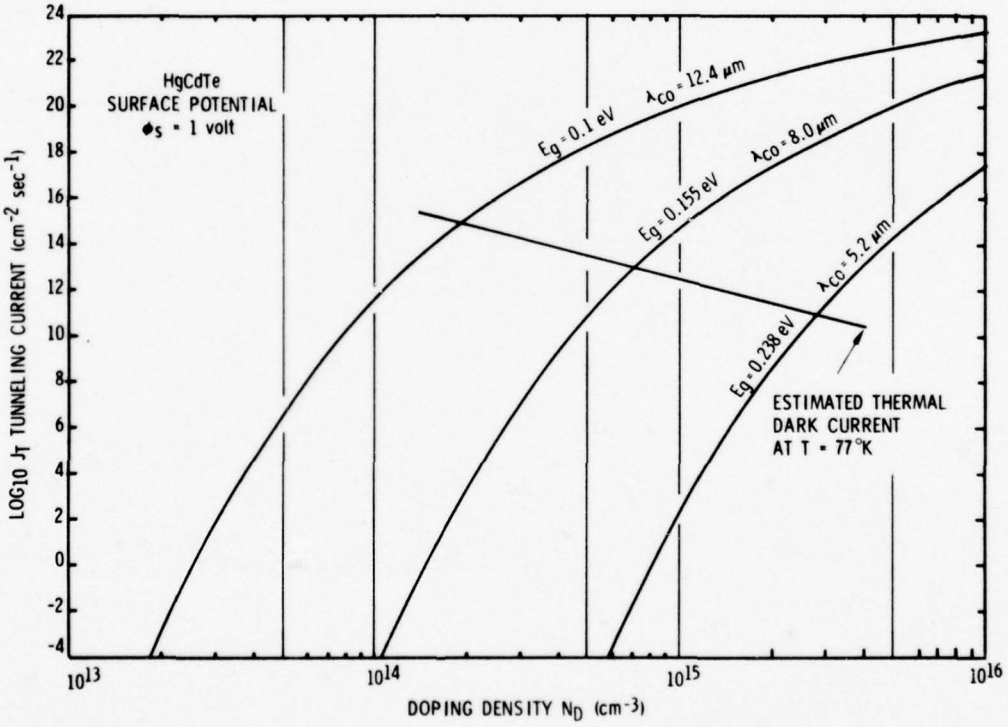


Figure 2-2. Tunneling Current Versus Doping Density for Three Different Bandgaps

Figure 2-3 shows J_T versus ϕ_s for several values of N_D with bandgap held constant at 0.1 eV. (Cutoff wavelength is λ_{co} = 12.4 μm.) J_T rises rapidly as ϕ_s or N_D increases. Large tunneling currents are seen for comparatively small surface potentials and low dopings.

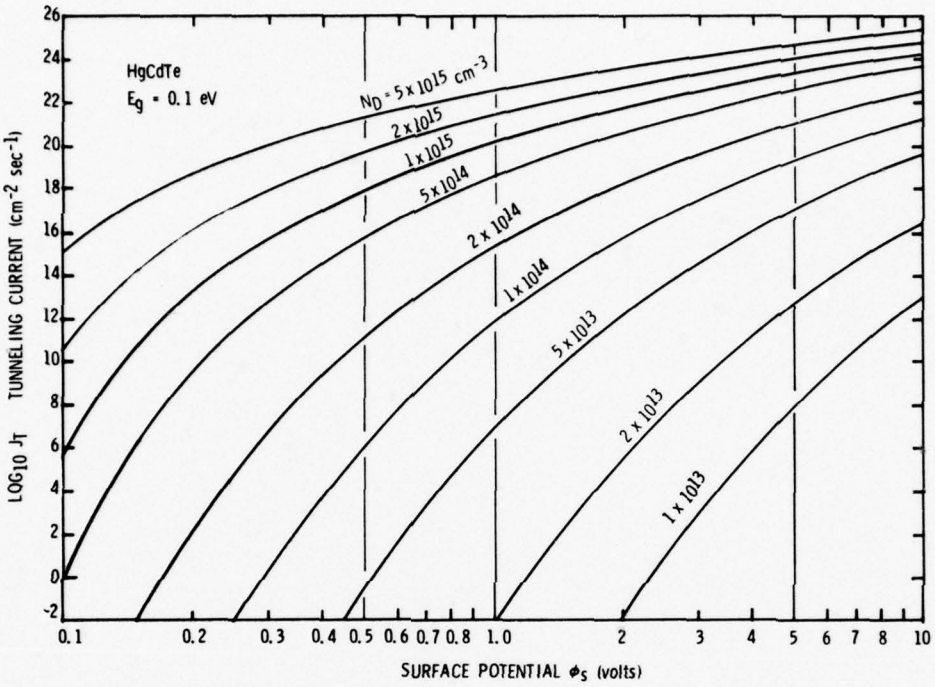


Figure 2-3. Tunneling Current Versus Surface Potential for 0.1 eV Bandgap

To study the limitations imposed by tunneling on the performance of MIS devices in 12 μm material it is helpful to display the parameters as in *Figure 2-4. Curves of constant* J_T *are* located on a graph of ϕ_s versus N_D. It should be noted that the tunneling currents have been calculated for the ideal case of an infinite gate area and a perfect semiconductor crystal. In any real device there will be edge fields around the finite gate and dislocations in the crystal. Both of these will produce locally high potential gradients, and thus narrower barriers to tunneling. Such potential gradients may be

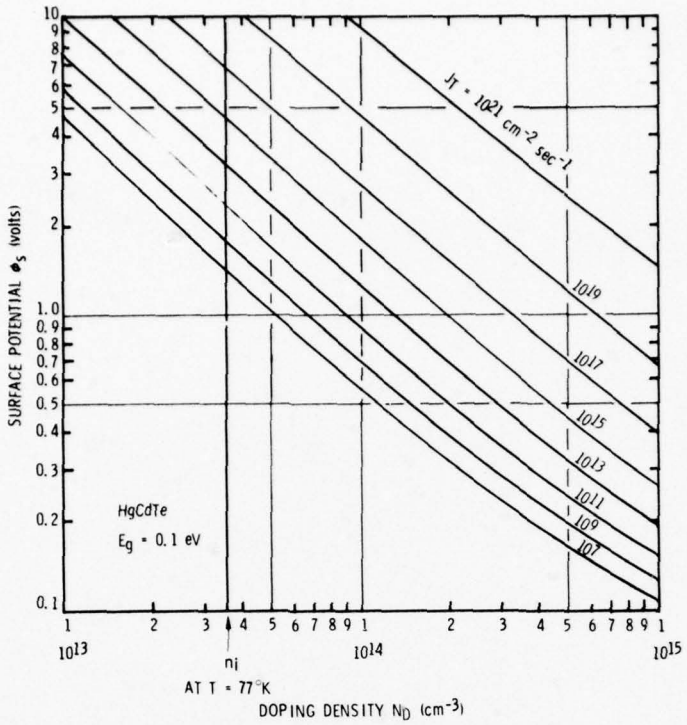


Figure 2-4. Curves of Constant Tunneling Current on a Plot of Surface Potential Versus Doping Density for 0.1 eV Bandgap

1.5 or 2 times higher than the gradient represented by the slope of the band edges at z = 0 in Figure 2-1. The increase in tunneling current in high-gradient regions may be estimated by the increase found from Figure 2-4 when ϕ_s is multiplied by 1.5 or 2. The result for a given combination of N_D and ϕ_s, is that J_T over most of the device area remains as indicated in Figure 2-4, but within the small high-gradient regions J_T is about 10^4 times larger. If high potential gradients occur over only 10% of the device area, the average tunneling current will be about 10^3 times larger than the J_T shown in Figure 2-4.

The effect of a large J_T on MIS device performance can be characterized by the resulting storage time T_s. Consider a typical example, in which $N_D = 1 \times 10^{14}$ cm^{-3} and ϕ_s = 1.25 volts. J_T from Figure 2-4 is 10^{13} cm^{-2} sec^{-1}. Taking the factor of 10^3 increase for non-ideal samples from the

preceding paragraph, we obtain $J_T = 10^{16}$ cm^{-2} sec^{-1}. With the given ϕ_s the storage capacity of the well is about 10^{11} cm^{-2}. We define storage time crudely as the time required for the well to fill at the rate J_T. (A better definition is given in Section 3.) The resulting storage time is 10 μsec. The cycle time or integration time of the device would therefore have to be less than 1 μsec or possibly less than 100 nsec. Storage time becomes even shorter if N_D or ϕ_s is increased. On the other hand, it is not practical to operate at lower N_D or ϕ_s for the following, reasons. First, HgCdTe crystals with N_D below 1×10^{14} cm^{-3} are not readily available, and in any case the effective N_D at 77°K cannot be reduced below the intrinsic concentration $n_i = 3.5 \times 10^{13}$ cm^{-3}. Second, surface potential should reach at least 1 volt to assure sufficient storage capacity and operating flexibility. Another consideration is that a margin of safety is necessary in the choice of N_D and ϕ_s because of the extreme sensitivity of J_T to these and other parameters. It must be assumed that J_T is larger by a factor of perhaps 10^3 than previously calculated to ensure that tunneling remains insignificant. In the above example J_T then becomes 10^{19} cm^{-2} sec^{-1}, and T_s may be as short as 10 nsec. The conclusion in general is that storage times, as limited by tunneling currents alone, are so short in 12 μm HgCdTe that no MIS device can serve as a practical charge storage element.

Storage time is also affected by thermally-generated dark current J_G. It is estimated that at 77°K, J_G is about 10^{15} cm^{-2} sec^{-1}. This is smaller than the probable J_T, so that tunneling is the primary limitation to storage time, and the above discussion need not be modified to account for thermal dark current.

To consider operation at lower temperatures, we require that E_g remain at 0.1 eV. In other words, the HgCdTe alloy composition must be chosen to give $E_g = 0.1$ eV at the specified operating temperature. The tunneling currents in Figure 2-4 will therefore remain unchanged. Hence, the tunneling-imposed limitations are not removed by a reduction in temperature.

It should be noted that because of the approximations required in the derivation of Equation (2-2), and because of the extreme sensitivity of J_T to input parameters, the calculated values of J_T may easily be in error by a factor of 10 or possibly 100. Such errors, however, would not significantly alter our conclusions on the impracticality of MIS storage elements in 12 μm material.

One refinement of the above discussion would be to consider the time dependence of ϕ_s as the well fills. This is quite complicated, however, because the larger values of ϕ_s and J_T are never actually realized. This is because the storage well is initially created by a step in gate voltage with a nonzero rise time. The surface potential begins to rise in proportion at the same rate. However, before ϕ_s reaches its theoretical empty-well (maximum) value, J_T can become large enough to fill the well as fast as new storage capacity is created. Therefore ϕ_s increases no more. After the gate voltage step levels off, ϕ_s falls due to continued tunneling and thermal dark currents. Eventually ϕ_s becomes so small that tunneling is negligible, and the remaining well capacity is filled more slowly by thermal dark current alone. (At this point it is interesting to note that the remaining well capacity could be used to collect photogenerated charges, as in a photogate detector, but the quantum efficiency would be low and the cycle time would have to be short.)

Section 3

EXPERIMENTAL METHODS

PREPARATION OF SAMPLES

MIS devices were prepared on HgCdTe with 5- and 12-μm cutoff wavelengths, and n- and p-type doping, using both thick and thin wafers. The structure is shown in Figure 3-1 and the process is outlined below.

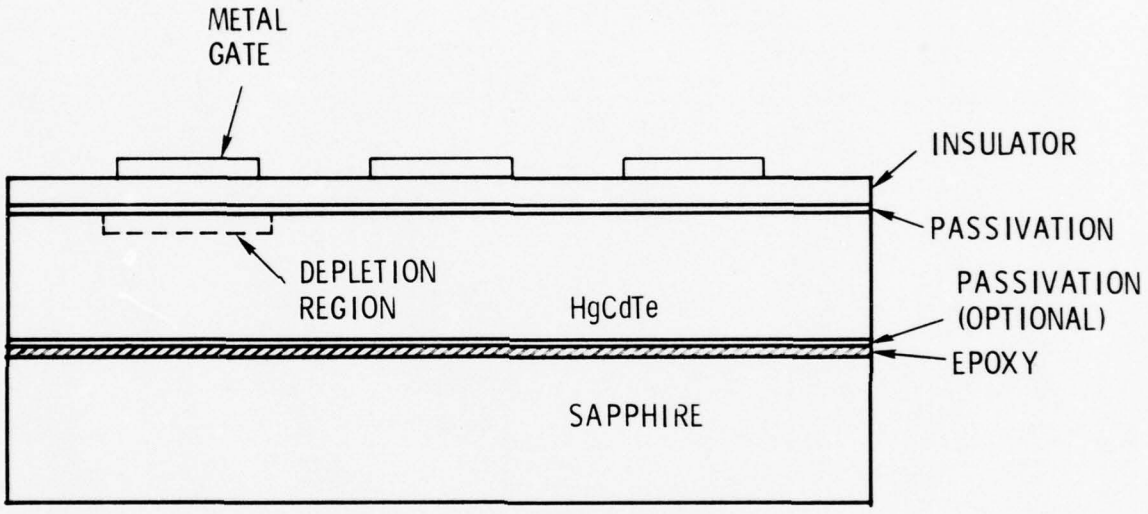


Figure 3-1. MIS Structure

An annealed and polished wafer is epoxied to a sapphire substrate. If the sample is to retain the original 15-mil thickness, the exposed surface is then passivated. For thinner samples, the wafer is first lapped and polished to less than 1 mil, then passivated. (Also, the surface against the sapphire is passivated prior to epoxying in the case of thinned samples.)

Upon the passivated surface, a layer of ZnS, usually 3700Å, is deposited to serve as an additional insulator and an antireflection coating. This layer is thin enough so that the total device capacitance, the quantity measured directly, is sensitive to conditions in the semiconductor. Yet it

is thick enough to provide 88% transmittance at λ = 5 μm, the approximate wavelength of peak response for our detector samples. The maximum of antireflection, namely 95% transmittance, occurs at λ = 3.5 μm.

Metal gates are next deposited on the ZnS. The wafer is sliced into 100-mil-square chips, and each chip is cemented to a twelve-pin TO-5 header. Each chip bears several gates, called dots. Contact to each dot is through a gold wire attached with silver epoxy. Contact to the semiconductor is via indium solder.

Most of the gates are circular, 25 mils in diameter. On samples for radiometric measurements the gates are Ni 100Å thick with a smaller dot of the usual gate metal in the center for contact.

CAPACITANCE MEASUREMENTS

Most of the testing of MIS devices consists of measuring capacitance in three different modes. First of all, high-frequency small-signal capacitance is measured using a PAR 410 C-V plotter. The voltage of the metal gate relative to the HgCdTe bulk is varied while capacitance, as determined by response to a 10 mv, 1 MHz sine wave, is recorded. The curves thus obtained are labeled in Section 4 by "HF."

The second mode of capacitance measurement is known as quasi-static.[6] Direct current is recorded in response to a slow, linear ramp of gate voltage. Quasi-static curves in Section 4 are labeled by "LF" (because in shape they resemble capacitance as measured with a low-frequency sine wave). The circuit used is shown in Figure 3-2. A ramp voltage $V(t) = V_1 + \alpha t$ is applied to the gate of the MIS capacitor, causing a charging current $I(t)$ to flow. $I(t) = \alpha C(t)$ because the operational amplifier, via feedback, holds its negative input terminal at virtual ground. Because of the very high input impedance of the operational amplifier, the full charging current flows

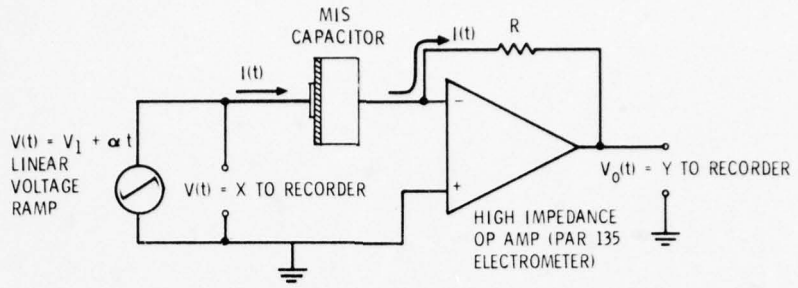
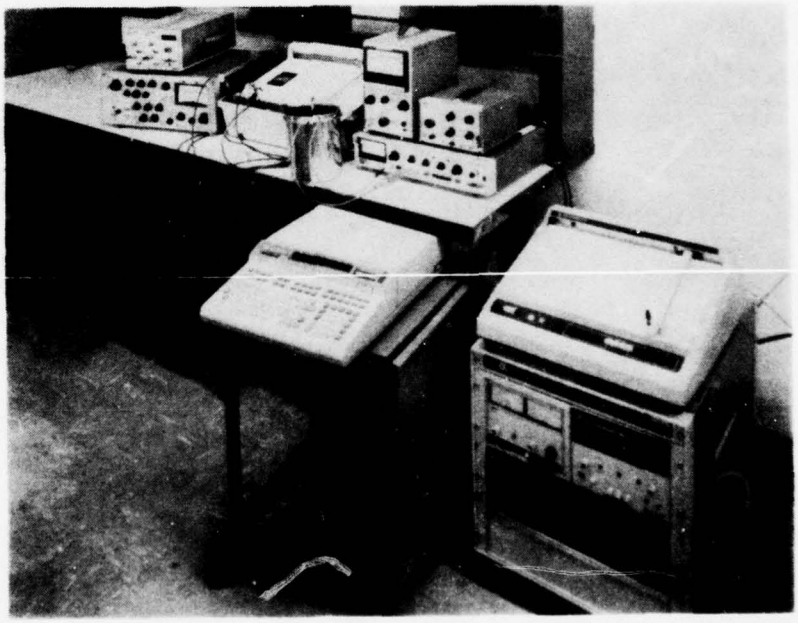


Figure 3-2. Circuit for Quasi-Static Capacitance Measurements

through the feedback resistor R. Therefore, a voltage $V_o(t) = -\alpha RC(t)$ appears at the output. The applied ramp and the amplifier output go to the X and Y inputs, respectively, of a chart recorder. Since the ramp is linear, α is constant and changes in V_o represent changes only in the device capacitance. Also, for data reduction only the fractional change in V_o is important, not the sign or total magnitude. Because the smallest changes represent currents on the order of 10^{-13} amp, the dewar is specially designed to minimize current leakage, and the dewar and instrument leads are carefully shielded.

The quasi-static method is very useful for the determination of a very important parameter of MIS devices, namely the fast interface state density N_{SS}. Under our implementation of the method, the sensitivity of N_{SS} is about 2×10^{10} cm^{-2} eV^{-1} over a large portion of the bandgap, assuming the insulator-semiconductor interface under the gate is laterally homogeneous. The method is convenient to computerize so that a complete N_{SS} characterization of many samples may be made without laborious manual analysis. Also in the range from accumulation to the onset of inversion, the dispersion between the measured quasi-static and high-frequency capacitance curves provides a direct determination of N_{SS} without recourse to ideal characteristics. Thus, an independent check on N_{SS} is provided. Furthermore, integration of the quasi-static capacitance curve from accumulation to inversion via the Berglund[7] method provides an accurate determination of the surface potential as a function of the gate voltage — also readily computerized.

Both the high-frequency and the quasi-static measurements are done with the aid of on-line data processing and printout utilizing an HP 9825 computer and an HP 3052A automatic data acquisition system (see Figure 3-3). Calculation of N_{SS} uses a comparison of quasi-static low-frequency and 1 MHz high-frequency C-V measurements. The data are acquired by an autoranging DVM and multichannel scanner and then processed by the computer. The system then prints out on an x-y plotter various surface property diagnostic information on command. One of these is a direct plot of surface state density as a function of the surface potential within the bandgap. The ability to make these rapid characterizations of the electrical surface conditions has been a key feature in the evaluation of MIS devices on this program.



77-6-71

Figure 3-3. Automated Data Acquisition System for MIS C-V Measurement and Analysis

The third mode in which capacitance is measured is by transient response to a gate voltage step, as shown in Figure 3-4. Gate voltage is repeatedly stepped between V_1 and V_2, the latter corresponding to inversion under equilibrium conditions. Initially, however, the condition is not equilibrium, but deep depletion with no inversion layer. The lack of an inversion layer is represented as an empty storage well. We measure high-frequency capacitance versus time, the C-t curve, as the well fills by dark current mechanisms.

From the C-t curve one obtains storage time T_s, as defined in Figure 3-4(c). A computer analysis of the C-t curve by the Zerbst method yields a variety of information, as explained in Section 5.

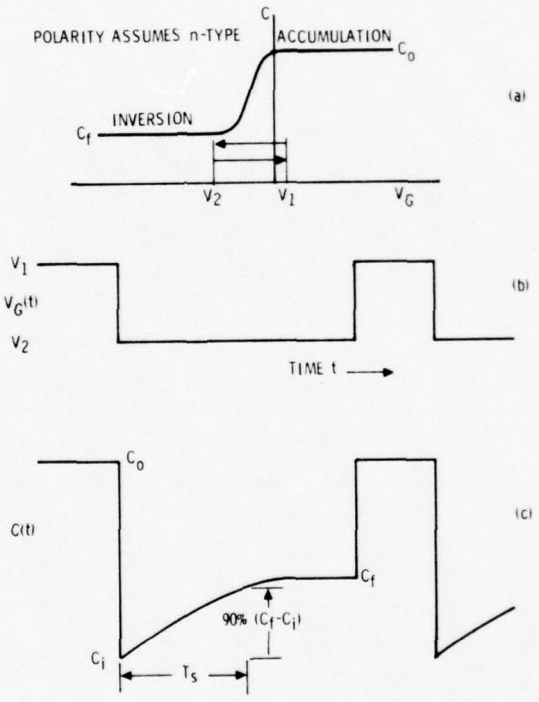


Figure 3-4. Transient Capacitance Measurement. (a) C-V curve showing gate voltage steps; (b) gate voltage versus time; (c) high-frequency capacitance versus time, showing storage time T_s.

TECHNIQUE FOR SHORT STORAGE TIME MEASUREMENT

Storage times are usually obtained from C-t curves acquired by the PAR 410 C-V plotter, but this instrument cannot resolve events faster than 1 msec.

To measure or search for storage times less than about 1 msec, a substrate injection technique (Figure 3-5) is used. The voltage applied to the gate is periodically switched between V_1 and V_2, where V_1 is sufficiently positive (for n-type samples) to eliminate the inversion layer and V_2 is sufficiently negative to establish initially a deep depletion region. For each step a spike appears on the output. The positive and negative spike amplitudes V_p and V_q, respectively, are measured on an oscilloscope with a high sensitivity Tektronix 7A13 differential comparitor plug-in unit as Δt is varied. V_p rises with increasing Δt and levels off at $\Delta t \simeq T_s$, the storage time.

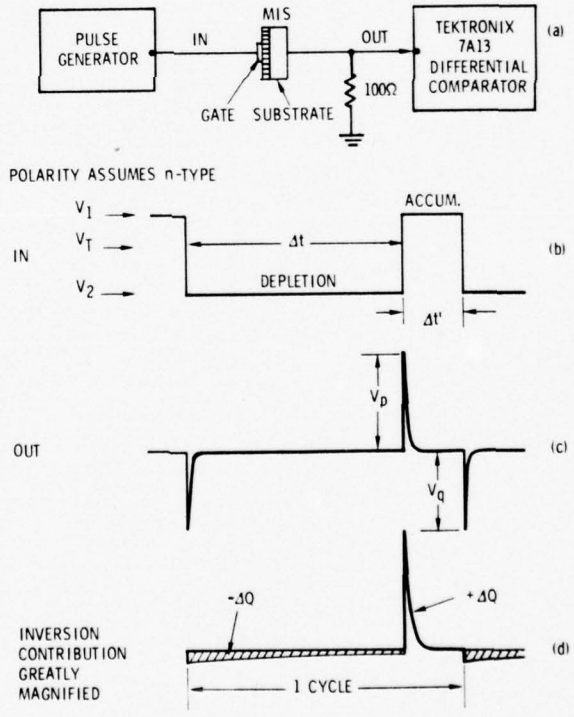


Figure 3-5. Schematic of the Substrate Injection Technique for the Measurement of Short Storage Times: (a) Circuit, (b) Input to Gate, (c) Output Signal Across the Load Resistor, (d) Inversion Contribution to the Output Signal. V_p Changes Going from $\Delta t < T_s$ to $\Delta t > T_s$.

To explain the observed V_p one must consider the flow of charges as the inversion layer builds. Immediately following the gate voltage step to V_2, the depletion region is wide and an inversion layer does not exist. As dark current mechanisms generate electron-hole pairs, most of the holes collect at the insulator-semiconductor interface to form the inversion layer. The corresponding electrons go either of two ways: some to neutralize ionized donors at the edge of the depletion region, thereby reducing its width, and others out of the substrate and through the load resistor. Since plates of a capacitor must bear equal and opposite charges, the pulse generator (the gate voltage supply) sends one electron to the gate for each one leaving the substrate. Thus, both the charge and the capacitance of the MIS device increase while its potential difference is held constant. The integrated current out of the substrate is represented by the shaded area $-\Delta Q$ in Figure 3-5(d). Since the net charge gained by the device over each cycle must be zero, a charge $+\Delta Q$ must flow through the load resistor when the gate voltage steps back up to V_1. This constitutes the spike area of Figure 3-5(d). The inversion contribution is superimposed on the currents due to charging and discharging of the "oxide" (insulator) capacitance to give the signal of Figure 3-5(c).

When Δt is much less than the storage time T_s, the inversion layer is almost empty and ΔQ is very small. As Δt increases, ΔQ increases, until $\Delta t \simeq T_s$, after which the inversion layer is full and ΔQ can increase no more. Thus V_p rises with increasing Δt and levels off at $\Delta t \simeq T_s$. V_p can be called the injection peak height.

As a test T_s was measured by both the present method and by the usual C-t curve for a SiO_2-Si sample with a sufficiently long T_s. Results are shown in Figure 3-6. The C-t curve was photographed on an oscilloscope, digitized, and linearly transformed to match the other curve at $\Delta t = 0.5$ and 1.8 sec. Both are flat above about 1.5 sec. Applying an arbitrary criterion of 90% of capacitance rise to define storage time, $T_s \simeq 1.1$ sec

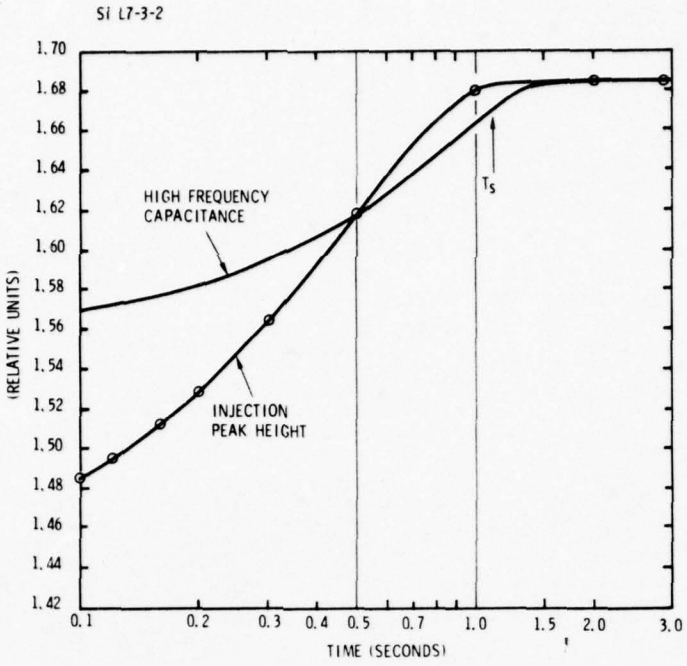


Figure 3-6. Injection Peak Height V_p and Capacitance Versus Time for a Si MOS Device

from the C-t curve. Near this time the injection peak plot shows maximum negative curvature, which we may take as the criterion for locating T_s from an injection measurement in the absence of a C-t measurement.

The minimum observable storage time is 200 nsec, determined by impedance mismatches in the dewar leads. The RC time constant of the device-with-load resistor is only 5 nsec for a typical device capacitance of 50 pf, and the gate voltage risetime is 5 nsec, so these are not limiting factors.

The shape difference of the curves in Figure 3-6 is not surprising, because the dependence of V_p on Δt is quite complicated.[8] The change in V_p is not simply proportional to capacitance. There are at least three reasons for this: 1) ΔQ depends nonlinearly on the actual inversion layer charge, 2) in addition to the change of capacitance during Δt, capacitance also changes rapidly during the step from V_2 to V_1, and 3) the shape of the output spike is modified by circuit time constants.

Injection time T_{inj} is a device parameter which can be measured by a modification of the above technique. T_{inj} is defined as the minimum value of $\Delta t'$, identified in Figure 3-5(b), necessary to eliminate the inversion layer. Details of the measurement of T_{inj} are given in Section 5 (Injection Time). For storage time measurements, we simply require a constant value of $\Delta t'$ of the same order of magnitude or greater than T_{inj}. Often $\Delta t'$ is set at 1 μsec. If $\Delta t'$ is not long enough, then V_q will vary with Δt, because the degree to which the inversion layer empties during $\Delta t'$ depends on the degree to which it fills during Δt. A corresponding change in the magnitude of V_p will also occur. This effect can be cancelled by taking the difference $V_p - V_q$.

Therefore, storage time is determined with the injection technique by plotting $(V_p - V_q)$ versus Δt and locating T_s where the plot shows the greatest curvature just prior to leveling off.

RADIOMETRIC TECHNIQUE

Figure 3-7 shows a block diagram of the apparatus used for radiometric measurements. The MIS device is mounted on a TO-5 header (not shown), which is securely clamped with good thermal contact to the bottom of the liquid nitrogen reservoir of the dewar. The device is electrically isolated from the header base and dewar. It is surrounded by a small cold-shield with an uncoated Ge window of 45% transmittance. Outside the shield a cold aperture establishes a 9.5° field of view (f/6.0). Given this aperture and the Ge window, the background flux at the device is $Q_B = 5.3 \times 10^{13}$ photons sec^{-1} cm^{-2} between the 1.8-μm Ge cutoff and a typical 5.2-μm sample cutoff. On the outer cap of the dewar is an IRtran-4 window with 69% transmittance. The infrared source is a 500°K blackbody with a square-wave chopper. The MIS device is alternately switched between accumulation and deep depletion at a rate faster than the chopper frequency.

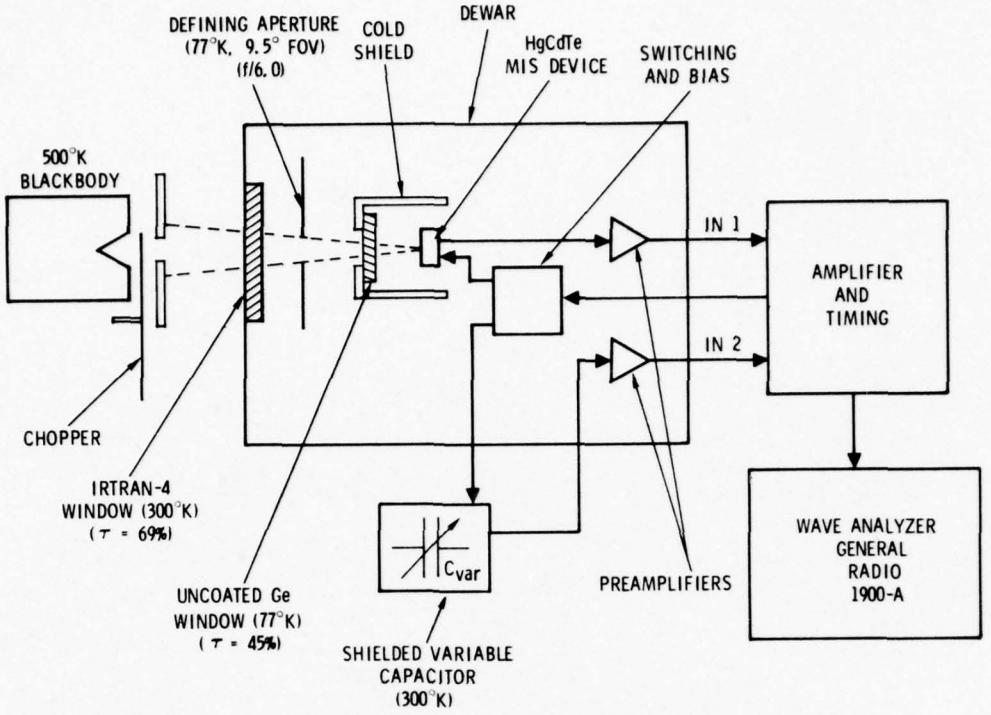


Figure 3-7. Block Diagram for Radiometric Measurements

Correlated double sampling is the signal processing method used.[9] Identical electrical signals are applied to the MIS device and to a variable capacitor (Figure 3-8). The output of each is preamplified by a FET in the dewar, before going to the amplifier, which is designed for very high common-mode rejection. If the variable capacitor is adjusted to balance the MIS device, the signal after the common-mode stage should contain a minimal level of switching transients. It should represent the amount of photo-generated charge on the MIS device collected since the beginning of the integration interval.

Figure 3-9 shows the timing diagrams. First of all, the reset pulse turns on the two switching FETs (Figure 3-8), grounding V_x, the MIS gate potential, and V_y, the potential on the upper plate of C_{var}. The dc V_{bias} is chosen such that $V_x \rightarrow 0$ produces deep depletion. Then during the integration time the gate is allowed to float. The increasing population of the

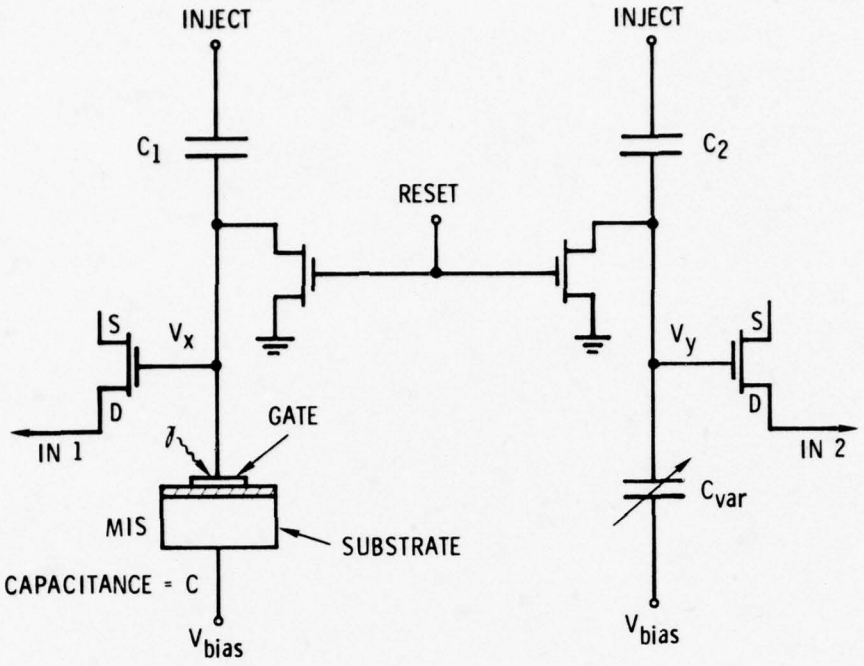


Figure 3-8. Detector-Preamplifier Circuit. Only C_{var} is not in Dewar.

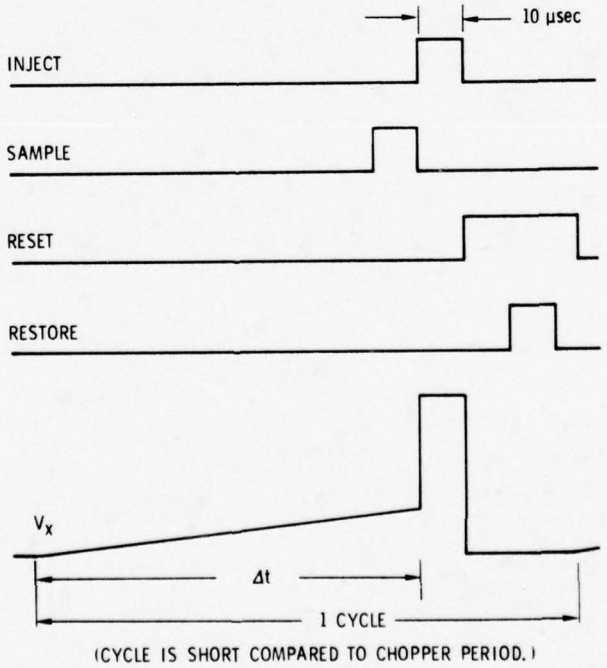


Figure 3-9. Amplifier and Detector Timing Diagram

inversion layer produces a rise in capacitance of the MIS device, causing a redistribution of charge between the device and C_1. The result is a rise in V_x. At the sample interval near the end of Δt the quantity $(V_x - V_y)$ is sampled and held in the amplifier beyond the common-mode stage. Next the inject pulse drives V_x sufficiently high (for n-type) to eliminate the inversion layer. To complete the cycle, the reset again establishes deep depletion in the MIS.

The double sampling involves an additional measurement of $V_x = V_{xo}$ and $V_y = V_{yo}$ during the reset. In the restore interval, which is nested within the reset interval, the quantity $(V_{xo} - V_{yo})$ is stored on a capacitor. It is substracted from the signal of the next sample interval in order to cancel offsets present at the amplifier input. The final result, proportional to $(V_x - V_y) - (V_{xo} - V_{yo})$, is held and presented for a full cycle to the wave analyzer, which is tuned to the chopper frequency. The wave analyzer reads rms signal V_s.

The amplifier was calibrated by inserting a small 500-Hz sine wave in place of V_{bias} on C_{var}. The voltage gain g with respect to V_y or V_x is 66.7. Calibration with respect to charge on the MIS device is done as follows, referring to Figure 3-8. Let ΔQ be the increase in charge on the substrate of the device since the beginning of the integration interval. Then the charge on the gate is changed by $-\Delta Q$. By charge conservation, since the gate is floating, $+\Delta Q$ must appear on the lower plate of C_1, accompanied by a voltage change from zero to V_x. Therefore

$$\Delta Q = C_1 V_x. \tag{3-1}$$

Effective current on the device is just

$$I_s = \Delta Q / \Delta t.$$

Finally, in terms of the wave analyzer reading V_s

$$I_s(\text{rms}) = C_1 V_s(\text{rms})/g. \tag{3-2}$$

Section 4

CAPACITANCE AND SURFACE STATE DENSITY

5-μm MATERIAL

As stated in Section 3, MIS devices were prepared on HgCdTe with 5- and 12-μm cutoff wavelengths. Results of capacitance measurements are presented here for both n- and p-type 5-μm material.

Figure 4-1 shows an example of the computer-acquired C-V curves obtained for 5-μm n-type material. The lower curve (HF) is the small-signal capacitance at 1 MHz and the upper (LF) is the quasi-static capacitance. The sweep direction is right to left. (Sample temperatures are 77°K unless stated otherwise.) Our computer analysis of these curves gives $N_D = 2.0 \times 10^{14}$ cm^{-3} with a depletion width W_m maximum of 1.2 μm, and it yields the plot of fast interface state density N_{SS} shown in Figure 4-2. The minimum N_{SS} is 2×10^{11} cm^{-2} eV^{-1}.

The computer analysis also provides the plot in Figure 4-3. The experimental quasi-static capacitance (dotted curve) is compared with the ideal (solid curve). The ideal curve is asymmetric. The symmetry of the experimental curve indicates some degree of lateral inhomogeneity of the insulator-semiconductor interface under the gate. Also, matching of the two curves in inversion and accumulation, where capacitance equals the "oxide" (insulator) capacitance C_o, is the means by which the computer determines the additive constant in the Berglund integration[7] to get surface potential. Another result is the plot of surface potential versus gate voltage in Figure 4-4. Zero surface potential locates the flatband voltage: -8.4 volts.

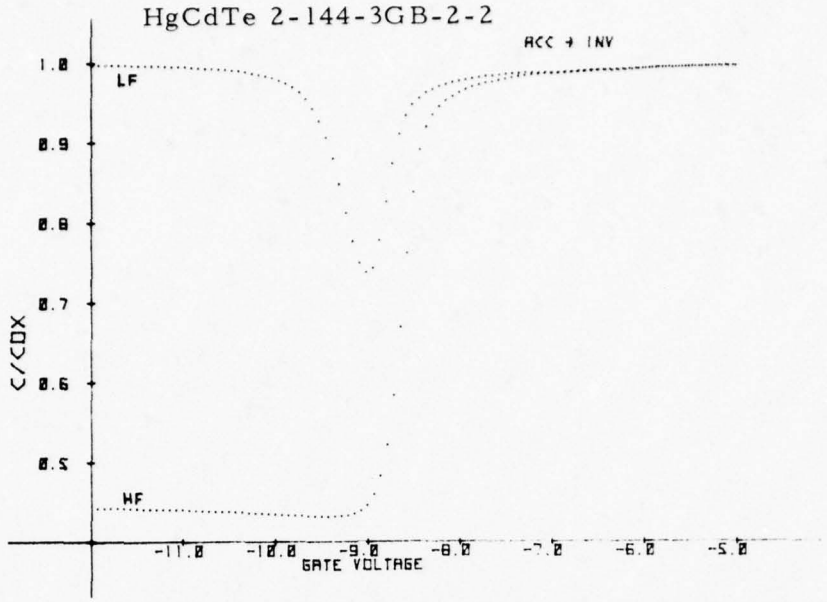


Figure 4-1. Capacitance-Voltage Plot for 5-μm n-Type MIS Sample Thickness = 15 mils, $N_D = 2.0 \times 10^{14}$ cm^{-3}, T = 77°K, FOV = 0°. Curve HF is high-frequency (1 MHz) capacitance. LF is low-frequency (quasi-static) capacitance with ramp only (no sine wave) applied.

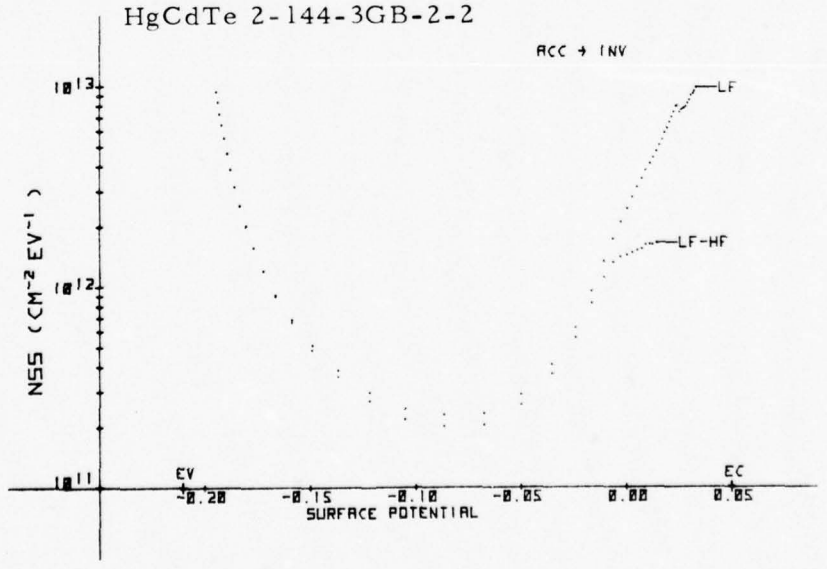


Figure 4-2. Fast Interface State Density Versus Surface Potential Derived from the Curves of Figure 4-1

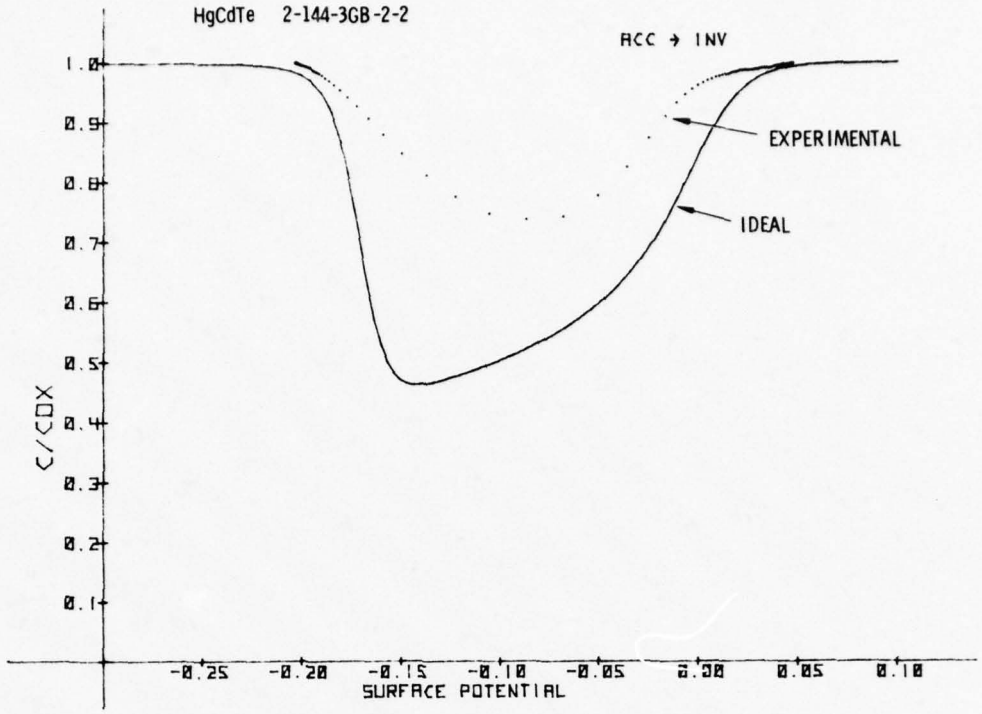


Figure 4-3. Quasi-Static Capacitance Versus Surface Potential Derived from the Curves of Figure 4-1

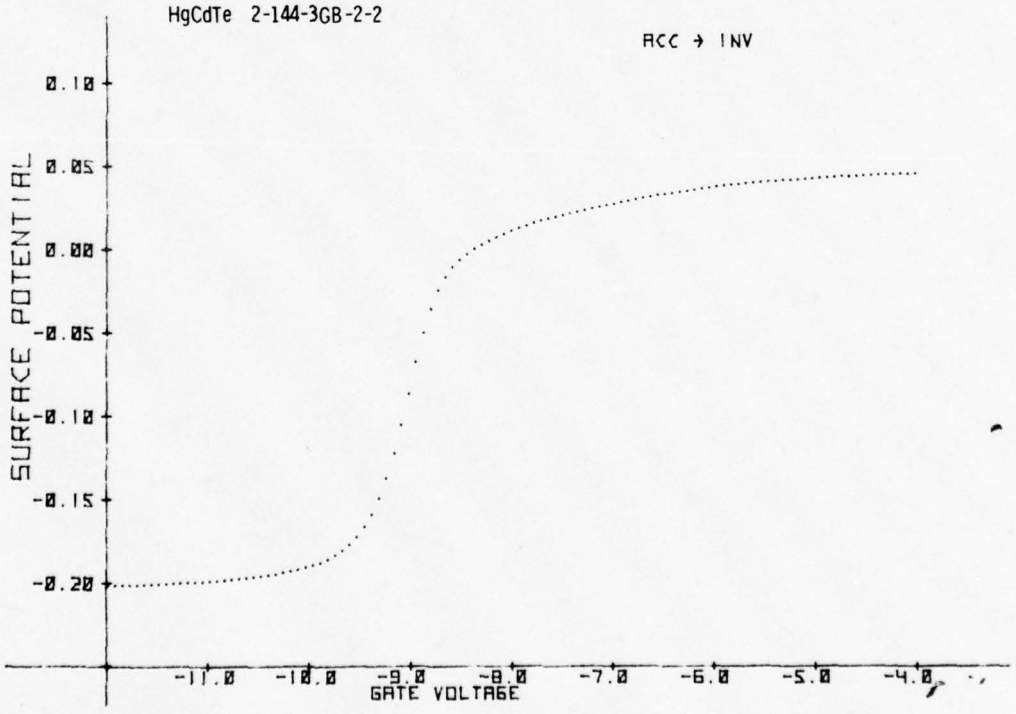


Figure 4-4. Surface Potential Versus Gate Voltage Derived from the Curves of Figure 4-1

Another 5-μm n-type sample is shown in Figure 4-5. N_D is 6.9×10^{14} cm^{-3}. Maximum W_m is 0.7 μm and minimum N_{SS} is 4×10^{11} cm^{-2} eV^{-1}. In both this and the sample of Figure 4-1 maximum hysteresis between the forward and reverse sweep directions is 0.4 volt.

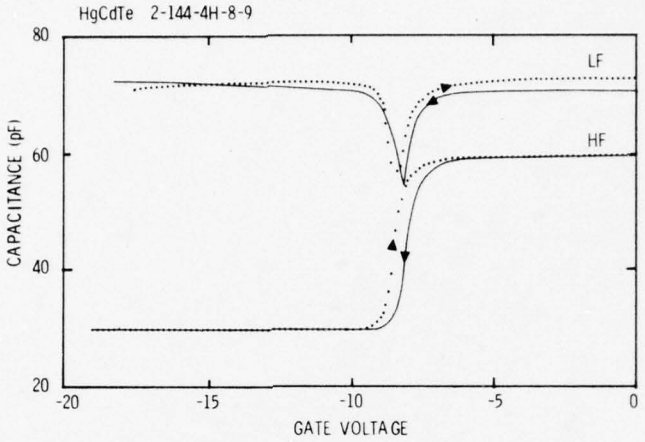


Figure 4-5. Capacitance-Voltage Plot for 5-μm n-Type MIS Sample Thickness = 15 mils, $N_D = 6.9 \times 10^{14}$ cm^{-3}, T = 77°K, FOV = 0°. Scale Factor of LF Curves is Arbitrary.

Figure 4-6 shows experimental C-V curves for a 5-μm p-type sample. The LF magnitude is arbitrary, and the dip will scale down by nearly a factor of two when LF and HF coincide in accumulation. N_A is 8.5×10^{14} cm^{-3}. Maximum W_m is 0.7 μm and minimum N_{SS} is 1.5×10^{11} cm^{-2} eV^{-1}. Figure 4-7 gives N_{SS} computed from the LF curve swept from inversion to accumulation.

Some of the samples with smaller than usual gate areas developed an instability with respect to contaminants from the atmosphere, as illustrated in Figure 4-8. Initially the HF and LF curves were very similar to those of part (c). After several weeks of exposure to ambient air, the curves (a) were obtained. The spreading of the HF accumulation → inversion transition indicates a spread of flatband voltages or an increased N_{SS}. The peaks in the LF curve are attributed to traps, either at the interface or a short

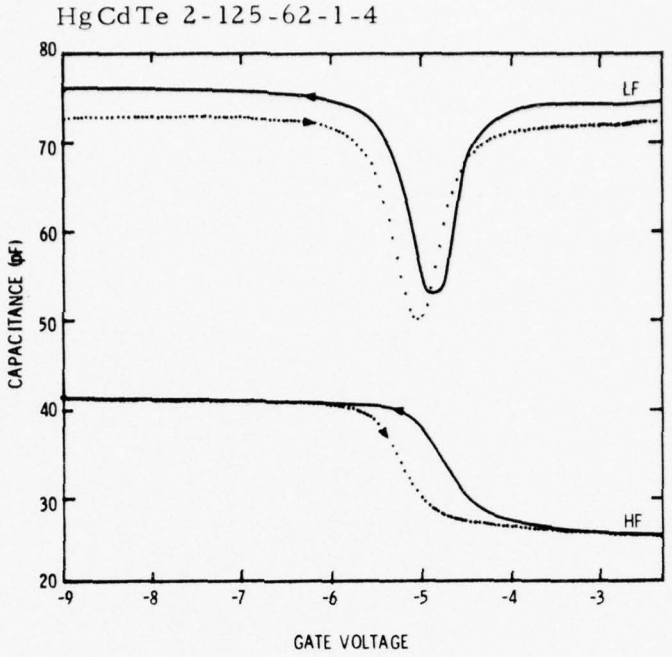


Figure 4-6. Capacitance-Voltage Plot for 5-μm p-Type MIS Sample Thickness = 0.8 mil, $N_A = 8.5 \times 10^{14}$ cm^{-3}, T = 77°K, FOV = 0°. Scale Factor of LF Curves is Arbitrary.

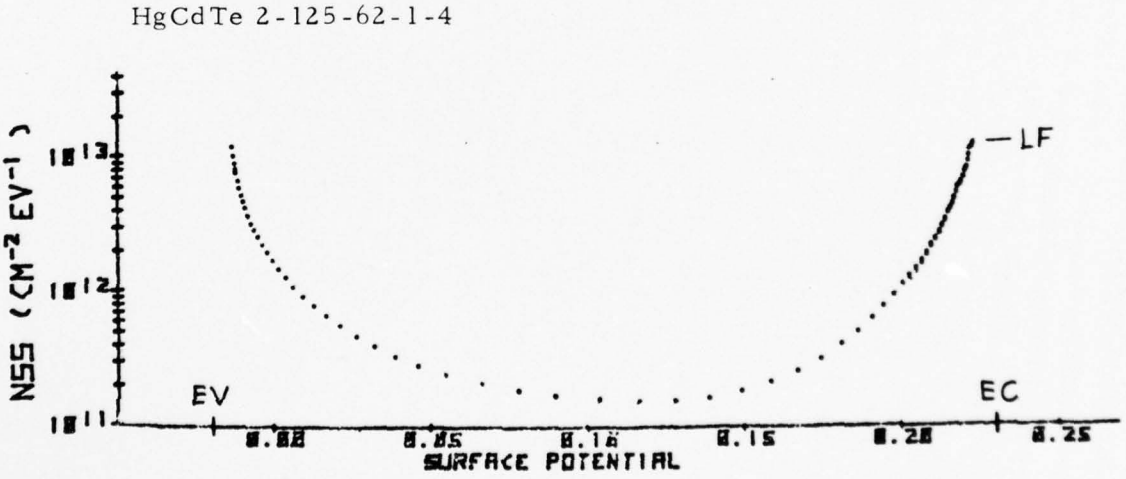


Figure 4-7. Fast Interface State Density versus Surface Potential Derived from the Solid LF Curve of Figure 4-6

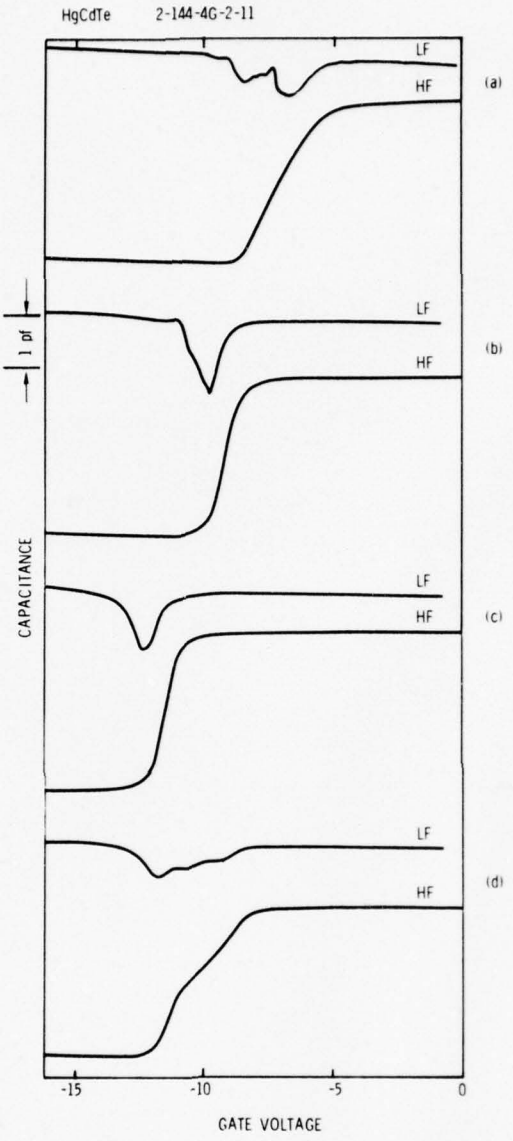


Figure 4-8. Capacitance-Voltage Plots for 5-μm n-Type MIS Sample with Small Gate Area

Note: a) After several weeks in air; b) after 1 hour vacuum bake at 100°C; c) after 14 more hours vacuum bake at 100°C; d) after 48 hours reexposure to air. Scale factor of LF curves is arbitrary.

distance into the insulator, occurring in large numbers at particular energies. As the Fermi level crosses the trap energy, the trap abruptly fills or empties, contributing to the observed quasi-static current. The curves (b) show great improvement after baking in the dewar for 1 hour at 100°C, but a hint of the traps remains. An additional 14-hour bake at 100°C yields the curves of part (c) with excellent interface properties. Finally, 48 hours of exposure to ambient air degrades the interface as shown in part (d). Both the HF and LF curves in (d) appear to be proportional to the sum of the corresponding curves of parts (a) and (c). Thus in part (d), a fraction of the interface area under the gate has returned to pre-bake conditions. It is reasonable to speculate that the contaminant is water, and that the region most readily contaminated is an annulus extending inward from the gate perimeter. Other samples, with large gate areas, did not show such an instability.

12-μm MATERIAL

For 12-μm material, Figure 4-9 shows that the HF and LF curves are nearly identical (LF magnitude arbitrary). The crystal is p-type with $N_A = 3 \times 10^{14}$ cm^{-3}. The rise of the HF curve in inversion is attributed to interband tunneling of carriers as explained in Section 2.

A similar HF curve for a 12-μm n-type sample with $N_D = 1 \times 10^{14}$ cm^{-3} is shown in Figure 4-10. Two additional curves are shown for lower temperatures, displaced downward for clarity. (The intermediate temperature was obtained with a probe in the neck of a liquid helium dewar.) Figure 4-11 shows curves at two temperatures for a p-type sample with $N_A = 3 \times 10^{14}$ cm^{-3}.

The most significant feature of Figures 4-10 and 4-11 is the rise of the capacitance in inversion at 4.2°K. This is strong evidence for interband tunneling, as the following argument shows. The capacitance as plotted indicates the response of the sample to a small, 1-MHz sine wave. An equivalent circuit for the device in inversion is shown in Figure 4-12. Since capacitance in inversion rises to roughly the same level as in accumulation,

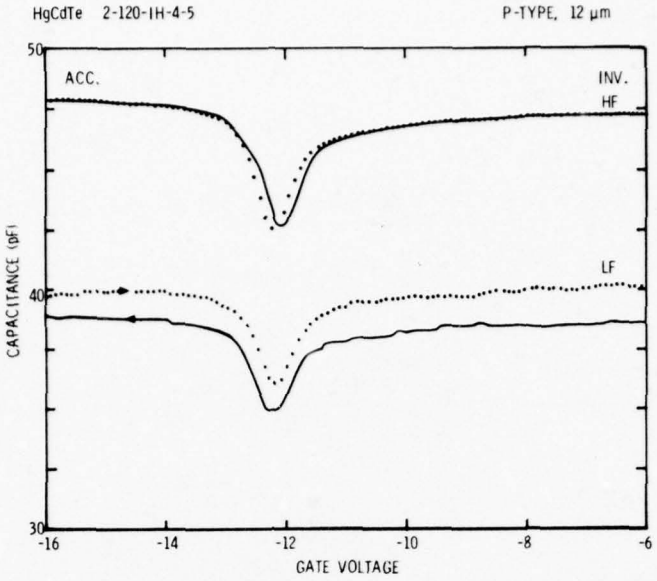


Figure 4-9. Capacitance-Voltage Plot for 12-μm p-Type MIS Sample, Thickness = 15 mils, $N_A = 3 \times 10^{14}$ cm^{-3}, T = 77°K, FOV = 0°. Curves HF are high-frequency (1 MHz) capacitance. Curves LF are low-frequency (quasi-static) capacitance with ramp only (no sine wave) applied.

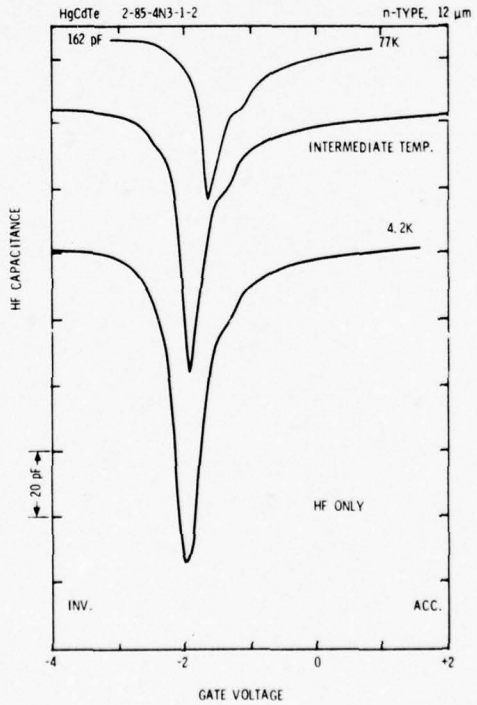


Figure 4-10. Capacitance-Voltage Plot for 12-μm n-Type MIS Sample, Thickness = 15 mils, $N_D = 1 \times 10^{14}$ cm^{-3}, Temperature Indicated on Curves, FOV = 0°.

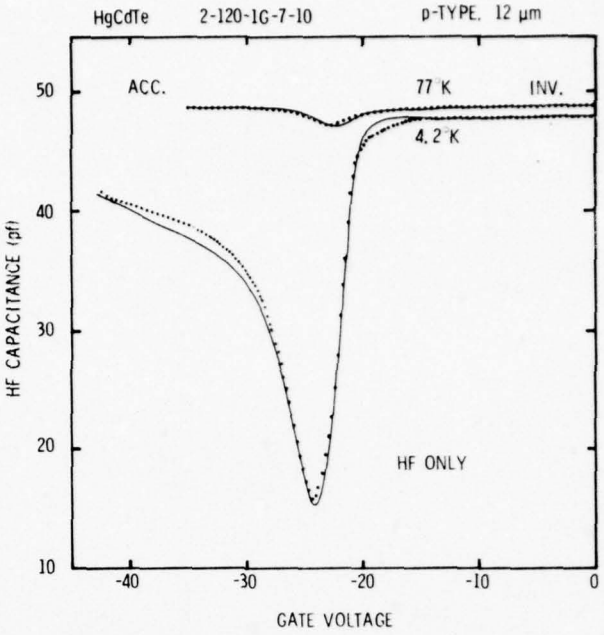


Figure 4-11. Capacitance-Voltage Plot for 12-μm p-Type MIS Sample, Thickness = 15 mils, $N_A = 3 \times 10^{14}$ cm^{-3}, Temperature Indicated on Curves, FOV = 0°.

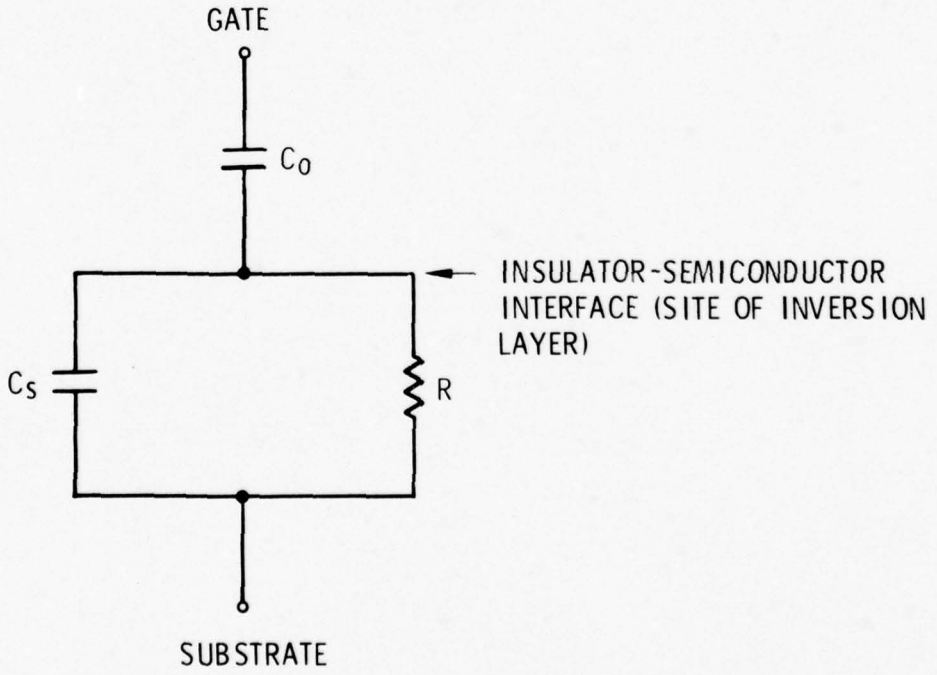


Figure 4-12. Equivalent Circuit for MIS Device in Inversion

the equivalent semiconductor time constant RC_s must be short compared to 1 μsec. Thus at T = 4.2°K charges are able to enter and leave the inversion layer within times short compared to 1 μsec. To account for these charges, three currents must be considered: photoexcitation, thermal generation, and tunneling.

First, photo-currents are not expected, because the TO-5 header on which the sample is mounted is covered with a tight metal cap providing a 0° FOV. The cap, header, and probe are immersed in liquid helium.

Second, the thermally-generated dark current J_G is expected to be negligible at 4.2°K. For n-type samples[10]

$$J_G = qn_i \left(\frac{n_i L_p}{N_D \tau_p} + \frac{W}{2\tau_p} + \frac{s}{2} \right) \tag{4-1}$$

where q = magnitude of electron charge

n_i = intrinsic carrier concentration

L_p = hole diffusion length

N_D = donor concentration

τ_p = hole bulk lifetime

W = depletion width

s = surface recombination velocity

An analogous relation holds for p-type samples. Although most parameters in Equation (4-1) will change with temperature, the value of J_G at low temperatures is overwhelmingly dominated by n_i. We use the empirical formula[5]

$$n_i = (1.093 - 0.296x + 0.000442T)(5.16)(10^{14})\, E_g^{\frac{3}{4}}\, T^{\frac{3}{2}} \exp(-E_g/2kT) \tag{4-2}$$

where T = temperature in Kelvins

E_g = bandgap in eV

x = the mole fraction CdTe in $Hg_{1-x}Cd_xTe$.

We take a nominal x = 0.20, so that $\lambda_{co} \simeq 13$ μm. Also the bandgap[11] is 0.094 eV at 77°K and 0.072 eV at 4.2°K. The result is

$$n_i = 5.3 \times 10^{13} \text{ cm}^{-3} \text{ at } 77^\circ\text{K}$$
$$n_i = 4.7 \times 10^{-29} \text{ cm}^{-3} \text{ at } 4.2^\circ\text{K}.$$

The latter value of n_i is practically zero so that $J_G \simeq 0$ at 4.2°K.

The third current is interband tunneling in the region of high-band curvature, as developed theoretically in Section 2. Tunneling current J_T is given by Equation (2-2). The only significant temperature influence on J_T is through the bandgap E_g, primarily in the exponential factor. Taking values of E_g from the preceding paragraph and making reasonable estimates of other parameters, it can be shown that J_T increases by roughly a factor of 100 on cooling from 77°K to 4.2°K. Considering this result and the theory of Section 2, we conclude that tunneling is the mechanism that supplies charges to the inversion layer in 12-μm material, and that the well-filling time-constant is less than 1 μsec.

Therefore, no useful well can be established under a gate in 12-μm material, because if any such well could be formed initially empty, it would be immediately filled by the tunneling current. This constitutes a fundamental limitation to the use of long-wavelength material in practical MIS devices. Further experimental evidence for this limitation is given in Section 5.

Another interesting feature in Figures 4-10 and 4-11 is the increase in the dip of the curve as temperature is reduced. The dip at 77°K is determined by both the doping density and the fast interface state density N_{SS}. The increase, however, in the dip on cooling to 4.2°K indicates an increase in the depletion region width W. This in turn is a result of either the freeze-out of carriers or an increase in the inversion surface potential.

The maximum W is given by (for n-type)[12]

$$W_m = \sqrt{\frac{2\epsilon_s \phi_{max}}{qN_D^+}} \qquad (4\text{-}3)$$

where ϵ_s = semiconductor dielectric permittivity

ϕ_{max} = tunneling-limited surface potential

N_D^+ = density of ionized donors

For the p-type case N_D^+ is replaced by the ionized acceptor density N_A^-. There is a striking difference of the dip increase for p-type (Figure 4-11) compared to n-type (Figure 4-10). This is a result of the different excitation energies of donors and acceptors, which Figure 4-13 shows.[13] The shallow levels have been located by low-temperature Hall measurements, and the deep acceptor level by lifetime versus temperature data. The donor level is so close to the conduction band edge that no freeze-out of electrons occurs down to T = 0.04°K[14] and N_D^+ decreases only slightly. For the n-type sample, the modest increase in the capacitance dip on cooling to 4.2°K is attributed mainly to a small increase in ϕ_{max} because of the suppression of the thermal contribution to the dark current. Acceptor levels, on the other hand, are deep enough so that holes freeze out at 4.2°K and N_A^- becomes small. Replacing N_D^+ with N_A^- in Equation (4-3), we find a large depletion width for p-type samples. This explains the large increase in the capacitance dip in Figure 4-11.

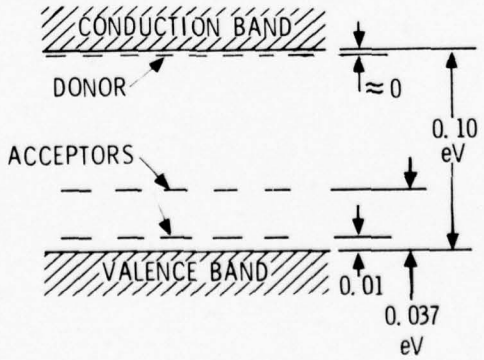


Figure 4-13. Impurity Energy Levels Identified in 0.1 eV HgCdTe by Means of Hall Effect and Lifetime Studies

The actual means of bulk conduction, however, in p-type samples at 4.2°K is probably impurity hopping. Electrons from the donors fall down to fill some of the acceptors. Since $N_D < N_A$ some of the acceptors remain neutral. This partly-filled "acceptor band" provides conduction as electrons hop (tunnel) from one acceptor site to another. Therefore conductivity does not go to zero when the holes freeze out. Hence W_m does not become arbitrarily large as T decreases, and the capacitance minimum of Figure 4-11 approaches a nonzero limit.

Section 5

STORAGE TIME AND OTHER DYNAMIC EFFECTS

STORAGE WELL PARAMETERS AND DARK CURRENTS

When the MIS structure is pulsed into deep depletion, a storage well is formed. Minority carriers immediately begin to fill the well, forming an inversion layer at a rate dependent on the source currents. Sources of minority carriers are 1) thermal generation in the bulk, depletion region, and surface, known as thermal dark current; 2) photoexcitation, as in a detector; 3) transfer from an adjacent well, as in CCD operation; and 4) possibly tunneling, as seen in 12-μm material. For successful operation as a photogate detector or a charge storage element, the storage time T_s (defined below) must be long compared to the device cycle time. Measurements of capacitance versus time as diagrammed in Figure 3-4 provide information on storage time, well parameters, and the origins of the carriers. All our C-t curves are for 0° FOV, 77°K background.

C_i is the initial capacitance following the gate voltage step to deep depletion. After a sufficient time, while gate voltage is held constant, the capacitance rises to its final value C_f. We define storage time T_s as the time required for capacitance to rise by 90% of the difference between C_f and C_i. The well capacity Q_p (assuming n-type) in holes per unit area is[4]

$$Q_p \simeq \frac{N_D \epsilon_s A}{1.2\, C_o}\left\{\left(\frac{C_o}{C_i} - 1\right)^2 - \left(\frac{C_o}{C_f} - 1\right)^2\right\} \qquad (5\text{-}1)$$

where C_o = "oxide" (insulator) capacitance, measured in accumulation

N_D = doping density

ϵ_s = semiconductor dielectric permittivity

A = gate area.

The well depth $\Delta\psi_s$ is

$$\Delta\psi_s \simeq \frac{0.6\, q\, Q_p\, A}{C_o} \qquad (5\text{-}2)$$

where q = electronic charge.

Considering dark currents only, for an n-type sample with a circular gate, the rate at which the well fills can be written as[15,16]

$$\frac{dp_s}{dt} = n_i \left| \frac{1}{\tau_g} (W - W_f) + \frac{2n_i L_p}{N_D \tau_g} \tanh (d/L_p) + s + \frac{4 s_o}{D} (W - W_f) \right| \qquad (5\text{-}3)$$

where p_s = inversion layer density, in holes per unit area

τ_g = bulk minority carrier generation lifetime

W = time-dependent depletion width

W_f = value of W when the well is full

n_i = intrinsic carrier concentration

L_p = hole diffusion length

d = sample thickness

s = time-dependent surface recombination velocity

s_o = initial value of s

D = gate diameter.

Note that the well capacity Q_p of equation (5-1) is the limit that p_s approaches for large time t. With n_i in front of the whole expression in Equation (5-3), each term in the square brackets has units of velocity.

The first term represents thermal generation of carriers within the depletion region. Every hole in this region is immediately swept into the inversion layer by the electric field. The second term is the diffusion current due to thermally generated holes in the neutral bulk. The factor $\tanh (d/L_p)$ represents the reduction of this current when the sample is thinned. In the following discussions both of these terms are called "bulk" sources even though W can be much smaller than d.

The third and fourth terms are currents due to surface generation. The surface recombination (actually, generation) velocity s is large for an empty well and decreases with time, as explained below. The third term represents carriers produced at the semiconductor surface, that is, the semiconductor-insulator interface, immediately below the gate area. The fourth term is current generated at the semiconductor surface around the periphery of the gate. Here the effective s is the initial s_o because this

region is not screened, as explained below. To be strictly correct, the second and third terms should be multiplied by some dimensionless factor which goes to zero as $W \rightarrow W_f$, but this correction is negligible during most of the filling time.

The terms of Equation (5-3) are estimated in Table 5-1. Parameters used are typical for our samples. Initially surface generation under the gate is the principal source of carriers, and the sample is said to be "surface dominated." Later generation in the depletion region takes over and the sample is "bulk dominated." The diffusion current is very small for any thickness d. (This term becomes important for $T > 77^\circ K$ because of the great increase of n_i, as discussed in the following subsection.) Peripheral surface current, the fourth term, is small for our samples because of the large diameter of the gates.

Table 5-1. Estimate of Well-Filling Rates by Dark Current Sources (Multiply each term by n_i to get carriers sec^{-1} cm^{-2}).

			(cm/sec)
BULK	DEPLETION REGION	$\frac{1}{\tau_g}(W-W_f)$	100
	NEUTRAL BULK	$\frac{2n_i L_p}{N_D \tau_g} \tanh (d/L_p)$	0.08
SURFACE	AREA UNDER GATE	initial $s = s_0$	1000
		plateau $s = s_1$	10
	PERIPHERY OF GATE	$\frac{4s_0}{D}(W-W_f)$	6

THE FOLLOWING VALUES ARE USED:

$\tau_g = 10^{-6}$ sec
$W-W_f = 1\ \mu m$
$n_i = 10^9\ cm^{-3}$ at $T = 77K$
$L_p = 80\ \mu m$
$N_D = 2 \times 10^{14}\ cm^{-3}$
$s_0 = 1000$ cm/sec
$s_1 = 10$ cm/sec
$D = 0.064$ cm
$d >> L_p$

From the experimental C-t curve, one can construct the Zerbst plot, namely $-d/dt\ (C_o/C)^2$ versus $(C_f/C-1)$. Assuming thermal dark currents to be the only source of minority carriers, the dominant kind of dark current can be determined from the shape of the Zerbst plot. Examples are given

in the following subsection. Also, by further analysis one can estimate the bulk minority carrier lifetime τ_g' and the time-dependent surface recombination velocity s. Defining M as the reciprocal slope of the Zerbst plot at the appropriate abscissa, one finds[17]

$$\tau_g' = 2M \frac{n_i}{N_D} \frac{C_o}{C_f} \tag{5-4}$$

where C_o and C_f are defined in the second paragraph of this Section. The true bulk minority carrier generation lifetime τ_g used in Equation (5-3), is related to the measured lifetime τ_g' by [16]

$$\tau_g' \simeq [1/\tau_g + 4\, s_o/D]^{-1} \tag{5-5}$$

The second term here is a correction for peripheral surface generation. For most of our samples this correction is very small so that the measured τ_g' is a good approximation to the true τ_g. From the experimental C-t curve the time-dependent surface recombination velocity is calculated using[16]

$$s(t) = \epsilon_s A \left[\frac{1/C_f - 1/C(t)}{\tau_g'} - \frac{C_o N_D}{2n_i} \frac{d}{dt} \left(\frac{1}{C^2(t)} \right) \right] \tag{5-6}$$

and $s_o = s(o)$. Parameters are defined above.

The typical variation of s with time is shown schematically in Figure 5-1. It represents the rate at which minority carriers are generated by surface mechanisms. At first, when the well is empty, $s = s_o$ and carriers are generated at a high rate. s_o is proportional to the fast interface state density N_{SS} because such states are the generation-recombination centers which thermally produce carriers at the surface. During the initial influx of minority carriers to the well, between $t = 0$ and $t = t_A$ in Figure 5-1, the fast interface states become partly filled (or "screened"), greatly reducing their ability to generate carriers, and s therefore falls rapidly. Next, in the interval $t_A < t < t_B$, s reaches a plateau s_1. Here the well continues to fill and the depletion region continues to shrink, but at slower rates. In general, surface-generated dark currents become smaller than

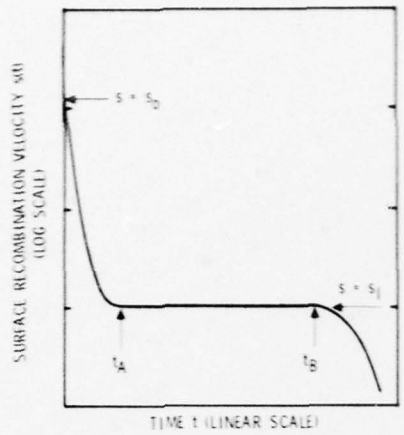


Figure 5-1. Schematic of Surface Recombination Velocity Versus Time. (t_A and t_B Mark Changes of Character of the Curve.)

those from bulk sources. Finally, for $t > t_B$, when the well is nearly full, analyses of experimental data generally show s falling again, but the true behavior of s is difficult to determine in this interval.

STORAGE TIME AND ZERBST ANALYSIS FOR 5-μm MATERIAL

Figure 5-2 is a C-t curve for an n-type sample with $N_D = 6.9 \times 10^{14}$ cm^{-3}. $T_s \simeq 3.5$ sec. A computer Zerbst analysis of Figure 5-2 is shown in Figure 5-3. It is important to remember that time as a parameter on the Zerbst plot runs from right to left, and that the transformation from the abscissa $(C_f/C-1)$ to time t is nonlinear. The time interval of the nearly-horizontal segment at the extreme right of the C-t curve (Figure 5-2) is compressed into a very small interval of $(C_f/C-1)$ near the origin of the Zerbst plot (Figure 5-3). The point at the end of the long, straight segment of Figure 5-3 near $(C_f/C-1) \simeq 0.17$ corresponds to $t = 0$ on the C-t curve. The straightness of the plot for $0.04 < (C_f/C-1) < 0.17$ implies that the total dark current filling the well is bulk-dominated. Considering the insignificance of the expected diffusion from the neutral bulk (Table 5-1) it is concluded that most carriers originate in the depletion region. Inserting the reciprocal slope of this straight segment into Equation (5-4), we find the experimental

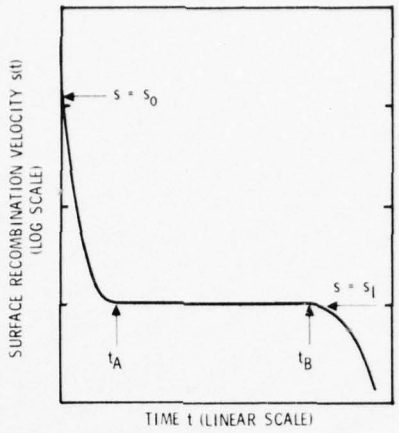


Figure 5-1. Schematic of Surface Recombination Velocity Versus Time. (t_A and t_B Mark Changes of Character of the Curve.)

those from bulk sources. Finally, for $t > t_B$, when the well is nearly full, analyses of experimental data generally show s falling again, but the true behavior of s is difficult to determine in this interval.

STORAGE TIME AND ZERBST ANALYSIS FOR 5-μm MATERIAL

Figure 5-2 is a C-t curve for an n-type sample with $N_D = 6.9 \times 10^{14}$ cm^{-3}. $T_s \simeq 3.5$ sec. A computer Zerbst analysis of Figure 5-2 is shown in Figure 5-3. It is important to remember that time as a parameter on the Zerbst plot runs from right to left, and that the transformation from the abscissa $(C_f/C-1)$ to time t is nonlinear. The time interval of the nearly-horizontal segment at the extreme right of the C-t curve (Figure 5-2) is compressed into a very small interval of $(C_f/C-1)$ near the origin of the Zerbst plot (Figure 5-3). The point at the end of the long, straight segment of Figure 5-3 near $(C_f/C-1) \simeq 0.17$ corresponds to $t = 0$ on the C-t curve. The straightness of the plot for $0.04 < (C_f/C-1) < 0.17$ implies that the total dark current filling the well is bulk-dominated. Considering the insignificance of the expected diffusion from the neutral bulk (Table 5-1) it is concluded that most carriers originate in the depletion region. Inserting the reciprocal slope of this straight segment into Equation (5-4), we find the experimental

Horizontal: 0.6 sec/div

Vertical: 2 pf/div

$T_s \simeq 3.5$ sec

$\Delta\psi_s = 207$ mv

$Q_P = 4.1 \times 10^{10}$ cm^{-2}

$N_D = 6.9 \times 10^{14}$ cm^{-3}

15 mils thick

0° FOV

T = 77°K

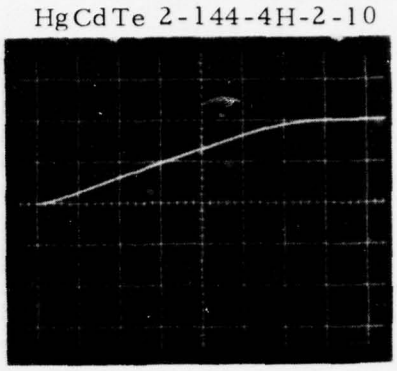


Figure 5-2. Capacitance versus Time for 5-μm n-Type MIS Sample

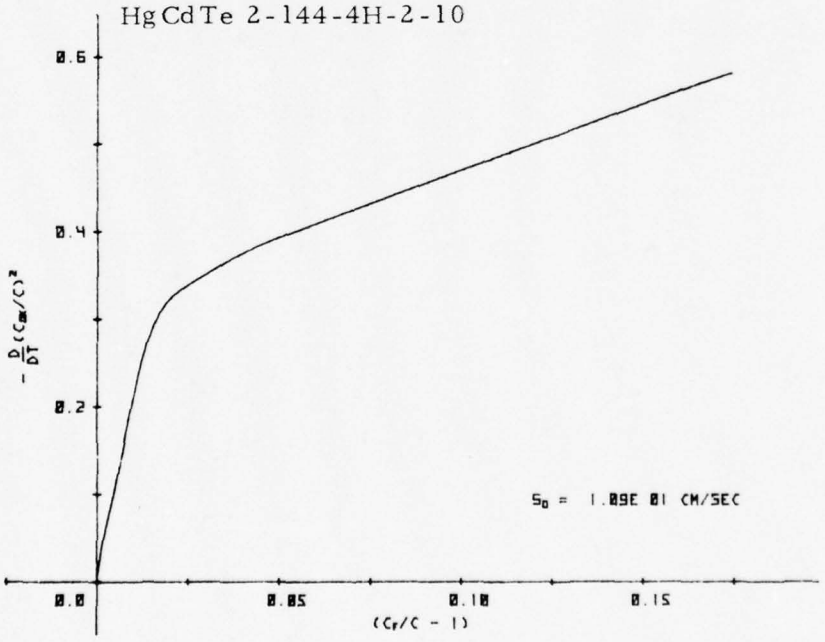


Figure 5-3. Zerbst Plot Derived from the Curve of Figure 5-2

bulk minority carrier generation lifetime to be $\tau_g' = 6.1 \times 10^{-6}$ sec. As shown with Equation (5-5), τ_g' is a good approximation to τ_g. To compare this to the recombination lifetimes, we use[17]

$$\tau_g = \tau_{po} \exp\left[(E_r - E_i)/kT\right] + \tau_{no} \exp\left[(E_i - E_r)/kT\right] \qquad (5\text{-}7)$$

where τ_{po} = bulk hole recombination lifetime

τ_{no} = bulk electron recombination lifetime

E_r = energy of recombination center

E_i = intrinsic Fermi energy

k = Boltzmann's constant.

The usual assumptions (carried over from Si work) are that $E_r = E_i$ and $\tau_{po} = \tau_{no}$. If these are true, then $\tau_{no} = \tau_g/2 \simeq 3 \times 10^{-6}$ sec. The experimental recombination lifetime (from the decay of conductance following a laser pulse) in an adjacent wafer is 1.2×10^{-6} sec, which compares well, within experimental error.

The assumption that $E_r = E_i$, however, is not correct. It is known that $E_r < E_i$ in HgCdTe.[15] The second term of Equation (5-7) therefore dominates. Consequently, $\tau_{no} < \tau_g/2$. Since E_r is unknown, a better estimate of τ_{no} is not possible.

One feature of the usual Zerbst plots[16, 17] that is missing from Figure 5-3 is an upturn at larger values of $(C_f/C - 1)$, to the right of the long, straight segment. Such an upturn would represent surface-dominated dark current as the well begins to fill. Initial surface-domination probably does occur in the present sample, but because of the large time scale of Figure 5-2, it is not resolved. The changeover to bulk-domination is probably accomplished in less than 100 msec. The time-dependent surface recombination velocity derived from Figure 5-3 is shown in Figure 5-4. The value is small and constant during most of the storage time. The shape resembles Figure 5-1 for $t > t_A$. The steep region at small t, where s is large, is missing because of the absence of the above-mentioned

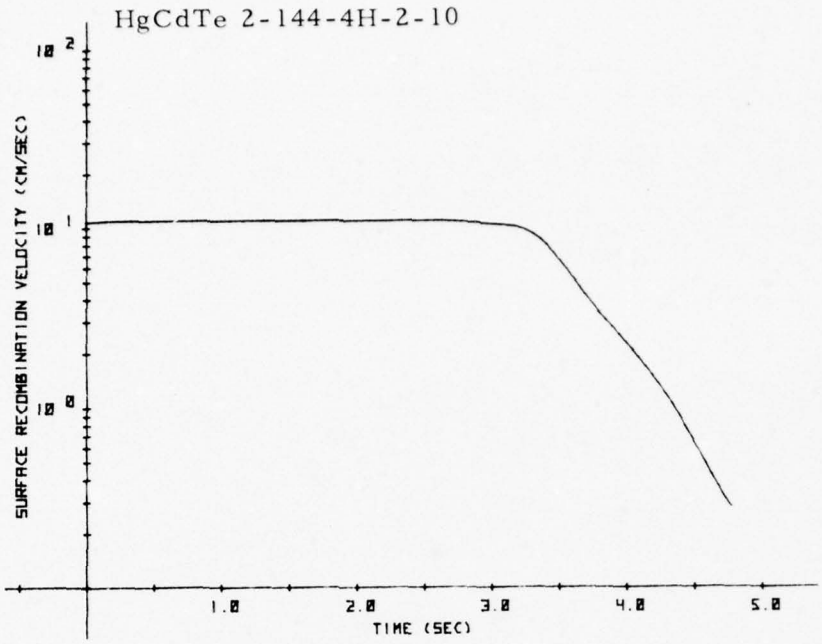
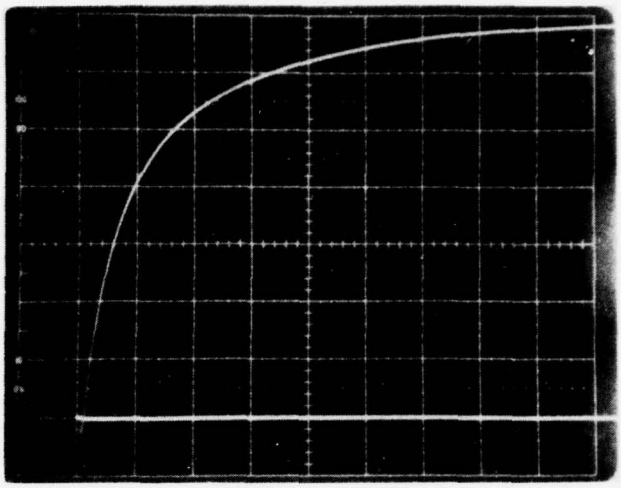


Figure 5-4. Surface Recombination Velocity versus Time Derived from the Zerbst Plot of Figure 5-3

upturn at the end of the Zerbst plot. Hence, for this sample $(T_S - t_A) >> t_A$, and the sample is said, in general, to be "bulk dominated." Also, from Figure 5-2, using Equations 5-1 and 5-2, we find that the well depth $\Delta\psi_S$ is 207 mV and the well capacity Q_p is 4.1×10^{10} cm^{-2}. $\Delta\psi_S$ is determined by the small, convenient gate bias step applied and is not the maximum attainable.

By contrast the sample of Figure 5-5 can be said, in general, to be "surface dominated." The resulting Zerbst plot is shown in Figure 5-6. The straight segement, expected for the interval when the bulk contributes most of the current, is very short. It occurs only for $(C_f/C-1) < 0.03$. All the rest of the Zerbst plot consists of the "upturn" expected for larger values of $(C_f/C-1)$, which represents surface-generated currents. The surface recombination velocity is shown in Figure 5-7. The initially large s and its subsequent decline are clearly seen, in contrast to Figure 5-4 for the previous sample. Since $T_S = 0.50$ sec, we see that $t_A > T_S/2$. Because of the importance of surface currents during most of T_S, the sample is called, in general, "surface dominated."

HgCdTe 2-144-4G-4-12



Horizontal: 100 ms/div

Vertical: 1 pf/div

T_s = 500 ms

$\Delta\psi_s$ = 235 mv

$Q_P = 4.5 \times 10^{10}$ cm^{-2}

$N_D = 6.5 \times 10^{14}$ cm^{-3}

0.5 mils thick

0° FOV

T = 77°K

Figure 5-5. Capacitance versus Time for 5-μm n-Type MIS Sample

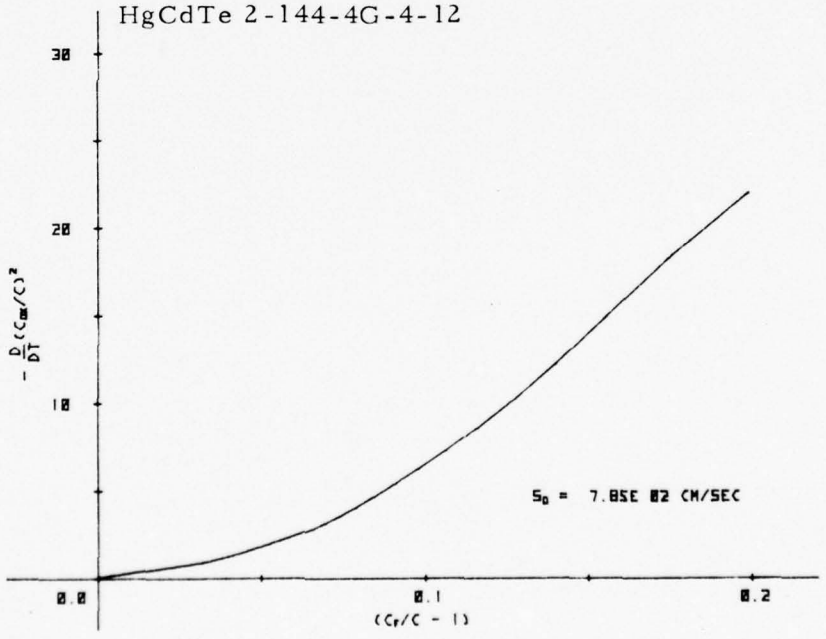


Figure 5-6. Zerbst Plot Derived from the Curve of Figure 5-5

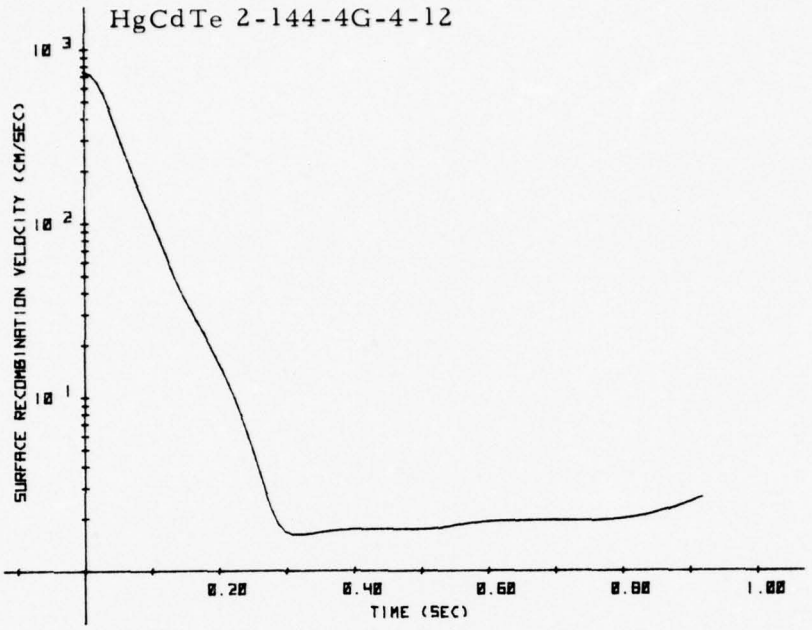


Figure 5-7. Surface Recombination Velocity versus Time Derived from the Zerbst Plot of Figure 5-6

From the straight segment for $(C_f/C-1) < 0.03$ in Figure 5-6 we get $\tau_g' = 1.6 \times 10^{-7}$ sec. This value is about an order of magnitude smaller than expected on the basis of bulk lifetime measurements on the original wafer. The experimental τ_g' is probably in error because it is very sensitive to small capacitance changes near the upper end of the C-t curve. The effect of τ_g' on s can be seen by inserting typical values of the other parameters in Equation (5-6). A factor of 10 increase in τ_g' causes approximately a 20% increase in s. Other properties of the sample, from Figure 5-5, are $\Delta\psi_s = 235$ mv and $Q_p = 4.5 \times 10^{10}$ cm^{-2}. Again $\Delta\psi_s$ was not optimized but just determined by a convenient gate bias step.

The longest storage time observed in HgCdTe was 25 sec, for an n-type sample with $N_D = 2.0 \times 10^{14}$ cm^{-3}. The C-V curve of a similar sample, having T_s about 20 sec, is shown in Figure 5-8. Two types of hysteresis can be seen. Horizontal hysteresis is due to slow interface states and depends, among other things, on the voltage extremes to which the MIS device is stressed. In a C-t measurement if one pulses to a voltage

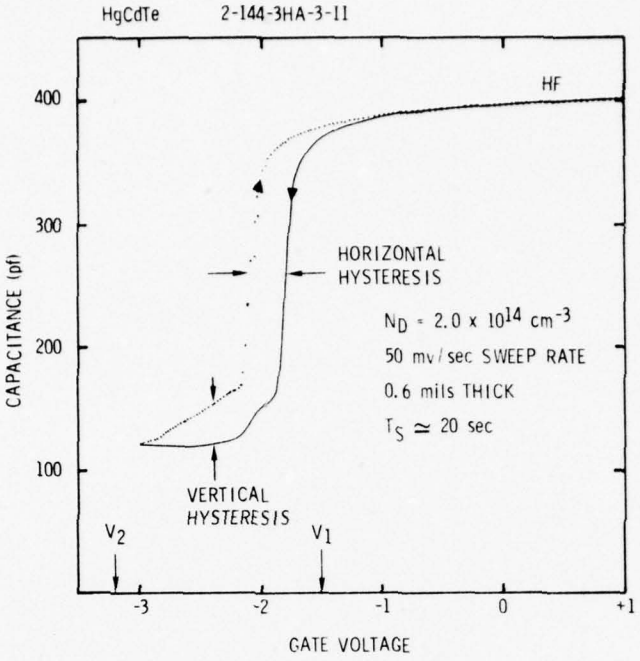


Figure 5-8. Capacitance-Voltage Plot Showing Sweep-Rate-Dependent Vertical Hysteresis Due to Long Storage Time

within the horizontal hysteresis range, the approach of the slow states to equilibrium can obscure the other capacitance change due to filling of the inversion layer, thereby giving an incorrect T_s. On the other hand, vertical hysteresis is a true storage phenomenon. It is independent of the extremes of voltage stress, and depends on only the voltage sweep rate. On the sweep *into inversion, minority carriers do not fill the well as fast as its storage capacity increases*, so that total capacitance is reduced. At any given gate voltage during the sweep, the fields and carrier populations are the same as *would be established by pulsing a partly-filled well to that voltage. If during* the sweep the gate voltage is stopped and held fixed, the capacitance is seen to rise toward the full-well condition, analogous to the latter part of a C-t plot. During the return sweep the well is much fuller, so capacitance is higher. The vertical hysteresis is therefore simply due to the difference between inversion populations in the forward and reverse directions. To

measure T_s = 20 sec for the sample of Figure 5-8, gate voltage was pulsed between V_1 and V_2 as shown, where V_2 is well out of the horizontal hysteresis range. (The vertical hysteresis in Figure 5-8 would extend beyond V_2 if the sweep were carried farther.) We therefore conclude that our large values of T_s are true storage times.

Gate voltage is another factor influencing the storage parameters. For a p-type sample T_s ranged up to 1.5 sec, depending on V_2 the gate voltage in inversion. Figure 5-9 is the C-t curve for V_2-V_{FB} = 3.1 volts. The results in Figure 5-10 were derived from a sequence of C-t curves for the same sample, for several values of V_2, while $V_{FB}-V_1$ was held at 0.1 volt. T_s falls rapidly at first, as V_2-V_{FB} increases. It then levels off at about 100 msec for $V_2-V_{FB} > 1.5$ volts. The large T_s for small (V_2-V_{FB}) may be due, for this sample at least, to a non-storage contribution from slow interface states because horizontal hysteresis is seen for $V_2-V_{FB} < 1$ volt, or to a decrease of the initial surface recombination velocity s_o when the initial surface potential ϕ_s is reduced. In any case the region of $V_2-V_{FB} > 1.5$ volts is of more importance because of the greater well capacity and depth. Q_n rises to more than 10^{11} carriers/cm^2 and $\Delta\psi_s$ reaches 1.02 volts for V_2-V_{FB} = 3.9 volts.

A limit to the improvement of storage parameters with increasing gate voltage is reached at the breakdown voltage. Here the surface potential ϕ_s cannot increase any further, because the electric field is the maximum sustainable by the semiconductor. As ϕ_s tries to follow an increasing gate voltage, the field (equivalent to band bending) reaches a point where avalanching or tunneling suddenly occurs. Any attempt to increase ϕ_s beyond this limit is immediately counteracted by the rapid generation of carriers. Thus, additional increases in gate voltage produce no change in storage parameters.

Breakdown surface potential ϕ_{sb} is expressed in terms of C_D, the equivalent capacitance of the maximum deep depletion region. If C_i is the total measured capacitance following a gate voltage step beyond the breakdown condition then

Horizontal: 50 msec/div

Vertical: 2.5 pf/div

T_s = 115 msec

$\Delta\psi_s$ = 827 mv

Q_n = 9.61×10^{10} cm^{-2}

N_A = 8.5×10^{14} cm^{-3}

0.8 mils thick

0° FOV

T = 77°K

HgCdTe 2-125-62-1-3

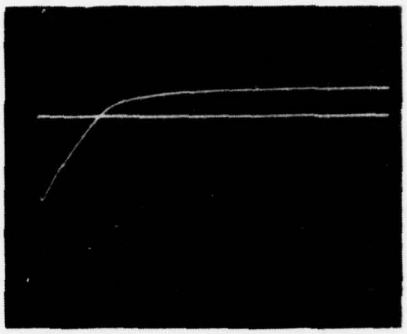


Figure 5-9. Capacitance versus Time for 5-μm p-Type MIS Sample

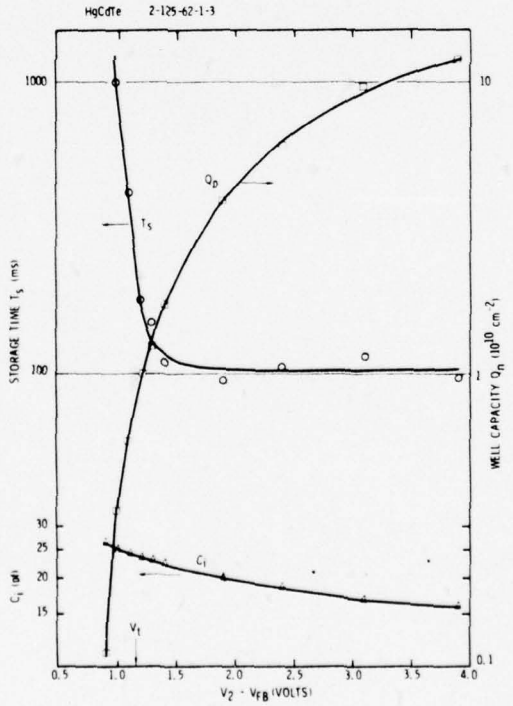


Figure 5-10. Storage Time, Well Capacity, and Initial Capacitance versus Gate Voltage (Relative to Flatband) for 5-μm p-Type MIS Sample. Thickness = 0.8 mils, N_A = 8.5×10^{14} cm^{-3}, T = 77°K, FOV = 0°

$$\frac{1}{C_D} = \frac{1}{C_i} - \frac{1}{C_o}$$

where C_o = "oxide" (insulator) capacitance. C_o and C_D combine in series to make C_i. Breakdown surface potential is

$$\phi_{sb} = \frac{q\, N_A\, \epsilon_s A^2}{2\, C_D^2} \qquad (5\text{-}8)$$

where N_A = doping density

ϵ_s = semiconductor dielectric permittivity

A = gate area

q = electronic charge.

Experimentally the best criterion for locating breakdown voltage is the leveling-off of C_i. In Figure 5-10 C_i reaches a minimum of 16 pf. Since it is not yet strictly level, we can calculate a lower bound to ϕ_{sb} of 1.2 volts.

The mechanism of semiconductor breakdown, which is either avalanching or tunneling, can now be considered. Both mechanisms can produce a current of minority carriers into the inversion layer. The current grows rapidly with increasing surface potential ϕ_s, thereby limiting ϕ_s, but neither mechanism is important until its current reaches about 10^{11} cm^{-2} sec^{-1}, the approximate thermal dark current. Tunneling current J_T can be estimated from Equation (2-2). Although most of Section 2 deals with tunneling limitations to MIS device performance in 12-μm ($E_g \simeq 0.1$ eV) material, J_T can be significant in the present 5-μm material at higher values of ϕ_s and N_A or N_D. For the sample in Figure 5-10 at $\phi_s = 2.0$ volts we calculate $J_T \simeq 2 \times 10^8$ cm^{-2} sec^{-1}. Correcting this for non-ideal device conditions (see Section 2, page 2-6), we estimate $J_T \simeq 2 \times 10^{11}$ cm^{-2} sec^{-1}, which implies $\phi_{sb} \simeq 2$ volts. This is somewhat higher than the observed value $\phi_{sb} \simeq 1.2$ volts, but the agreement is good considering the extreme sensitivity of J_T to several parameters (as discussed in Section 2). Avalanche current, on the other hand, is not so easily estimated. Considering the observation of avalanching[18] in Si and GaAs, the relatively narrow bandgap (0.24 eV) in 5-μm HgCdTe makes avalanching a plausible explanation for the observed

$\phi_{sb} \simeq 1.2$ volts. Therefore, within our present data and calculations, avalanching and tunneling are equally reasonable explanations of semiconductor breakdown.

Another sequence of C-t curves was obtained for an n-type sample, with results in Figure 5-11. Curves begin near $V_2 - V_{FB} = -2$ volts to avoid the interference of slow surface states closer to V_{FB}. It is seen that storage parameters remain nearly constant out to -25 volts. $Q \simeq 10^{11}$ carriers/cm^2 and $\Delta\psi_s \simeq 0.68$ volt. $T_s \simeq 120$ msec. C_i levels off at about 20 pf so that $\phi_{sb} = 0.80$ volt. Again tunneling and avalanching are equally reasonable explanations.

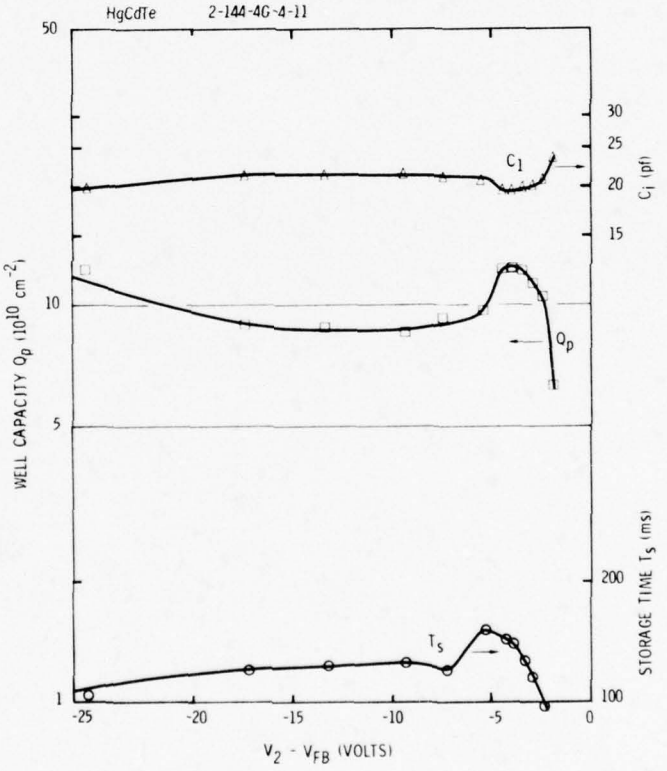


Figure 5-11. Storage Time, Well Capacity, and Initial Capacitance versus Gate Voltage (Relative to Flatband) for 5-μm n-Type MIS Sample. Thickness = 0.5 mil, $N_D = 6.5 \times 10^{14}$ cm^{-3}, T = 77°K, FOV = 0°

Thickness of the sample is another parameter that may influence storage performance. Choices of thickness were described in Section 3 (Preparation of Samples), and specific thickness values are given in many of the figures. Samples thinner than 1 mil appear in general to be surface-dominated, and those retaining the original wafer thickness appear to be bulk-dominated. We attribute the difference to an enhancement of the surface generation mechanisms by the lapping and polishing used to make thin samples. Note that the thinnest samples, 0.5 mil, are still much thicker than the depletion region, so its dark current contribution should be unchanged. As seen in Table 5-1 and Equation (5-3), the thickness d enters the dark current only through diffusion from the neutral bulk, which is very small at 77°K for any thickness. This is confirmed experimentally by the fact that we see no correlation between T_s and d. Thin samples are still of great interest, however, because of their advantage at higher temperatures. Diffusion current increases rapidly with temperature T because of its factor n_i. This can be offset by a reduction of d. For example, at T = 160°K, the diffusion term in Equation (5-3) is 1700 cm/sec for a thick sample. This can be reduced to equal the depletion region contribution (100 cm/sec) by thinning to d = 0.2 mil.

Finally, short storage times were investigated. A sample of 5-μm material showing no storage time down to 1 msec on a C-t plot was tested by the injection method of Section 3 (Technique for Short Storage Time Measurement). Figure 5-12 shows the peak height difference as a function of integration time. We conclude that T_s = 100 μsec. The small T_s is probably a result of accidental damage to the semiconductor material during device fabrication. The purpose of this measurement of short storage time is for comparison to the results for 12-μm material in the following subsection.

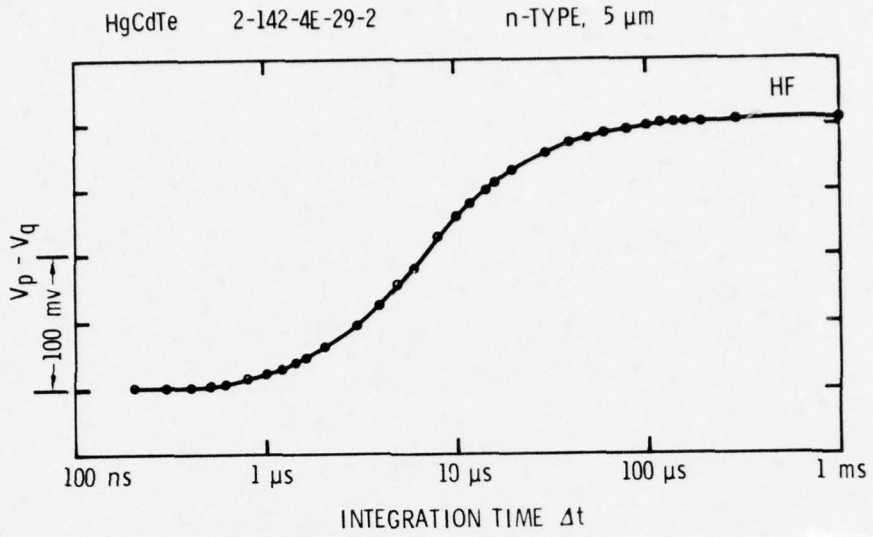


Figure 5-12. Short Storage Time Measurement: Peak Height Difference versus Integration Time. Curve Indicates $T_s \approx 100$ μsec

SEARCH FOR STORAGE TIME IN 12-μm MATERIAL

Of the many 12-μm samples tested none showed a storage time on a C-t plot, which has a minimum time resolution of 1 msec. Indeed, the low-frequency-like appearance of the 1-MHz HF C-V curves indicates that $T_s <$ 1 μsec, because large numbers of carriers are being supplied somehow at a rate fast enough to respond to the 1-MHz signal. To look for possible storage times less than 1 msec, the injection technique of Section 3 (Technique for Short Storage Time Measurements) was used. The technique was shown in the preceding subsection (Figure 5-12) to give reasonable data down to 200 nsec.

In Figure 5-13 the HF capacitance curve for an example is shown. Beginning in accumulation at -12 volt the gate was pulsed repeatedly to -16 volt while V_p and V_q were measured versus the integration time Δt. The experiment was done twice more, pulsing to -17 volt and -18 volt. These voltages cover the range in which storage effects are most likely. V_p-V_q showed no significant variation down to Δt = 200 nsec. Other 12-μm samples gave the same result. Thus, we saw no storage at all in 12-μm material. This result is entirely consistent with the discussion of Section 2.

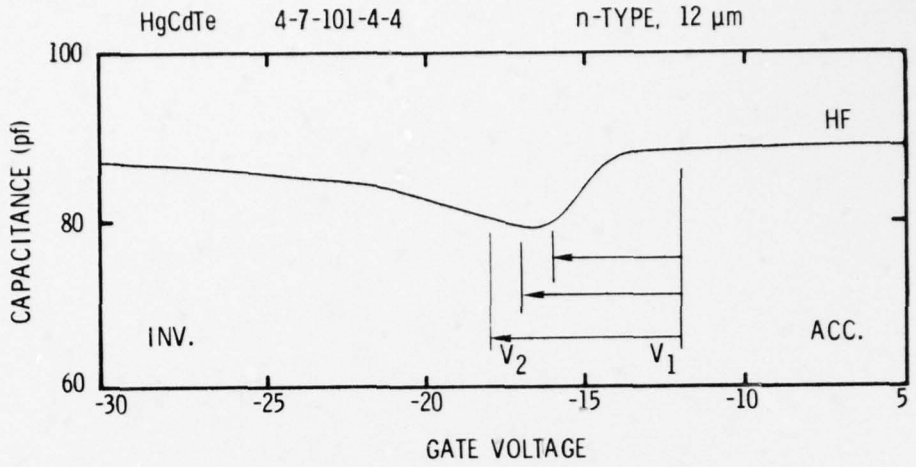


Figure 5-13. Capacitance-Voltage Plot for 12-μm MIS Sample Showing Accumulation Value V_1 and Three Choices V_2 Between Which Gate Voltage is Stepped to Search for Storage

INJECTION TIME

The injection technique described in Section 3 for the measurement of short storage times can be adapted to the measurement of injection time T_{inj}. As shown in Figure 5-14(a), the gate is pulsed between V_1 and V_2. The only difference from the storage time measurement is that Δt is held constant while $\Delta t'$ is varied. We choose $\Delta t > T_s$ so that the storage well is always full at the end of Δt. T_{inj} is defined as the minimum value of $\Delta t'$ necessary at voltage V_1 to empty the well (to eliminate the inversion layer).

Figure 5-14(b) shows the flow of charges involved. If the well is not full at the beginning of Δt, a small electron current flows out of the substrate (for n-type) during Δt. The integrated area is $-\Delta Q$. The only other output currents occur at the steps between V_1 and V_2. Since the net charge gained by the device during each cycle must be zero,

$$\Delta Q_1 = \Delta Q + \Delta Q_2. \qquad (5\text{-}9)$$

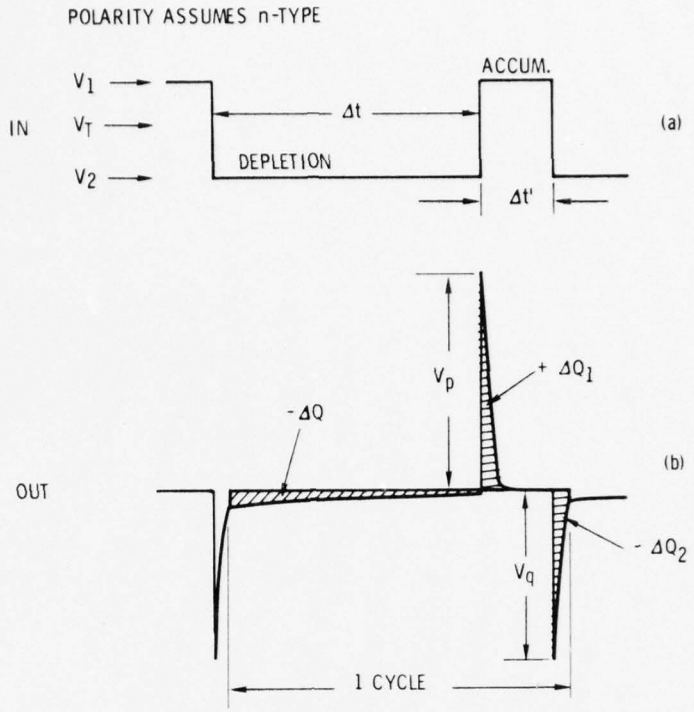


Figure 5-14. Schematic of Signals for Injection Time Measurement: (a) Input to Gate, (b) Output Signal Across Load Resistor. Areas (charges) obey $\Delta Q_1 = \Delta Q + \Delta Q_2$. Circuit is same as Figure 3-5(a)

V_p does not change as a function of $\Delta t'$ because the well is always full at the end of Δt. However, ΔQ and ΔQ_2 can change. If $\Delta t' << T_{inj}$ the well remains full and the well-filling charge ΔQ must be zero. Thus $\Delta Q_2 = \Delta Q_1$ and $V_q = V_p$.

At the other extreme when $\Delta t' >> T_{inj}$ the well is entirely empty at the end of $\Delta t'$ and ΔQ takes its maximum value. ΔQ_2 is therefore a minimum and so is V_q. Further increases in $\Delta t'$ cause no change in V_q. In summary V_q should begin near V_p for small $\Delta t'$, then fall for increasing $\Delta t'$, and level off near $\Delta t' = T_{inj}$.

The capacitance curve of a sample for which T_{inj} was measured is shown in Figure 5-15. The arrows indicate the gate voltage ranges for two separate T_{inj} measurements. When $V_1 = -6.0$ volt, the device is expected

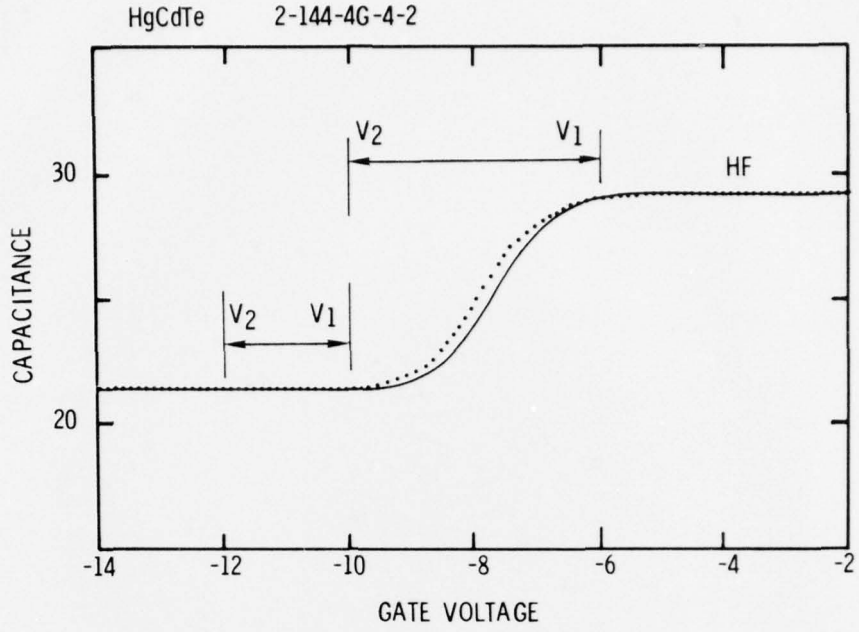


Figure 5-15. Capacitance-Voltage Plot for 5-μm MIS Sample Showing Values Between Which Gate Voltage is Stepped for Injection Time Measurement

to be in accumulation but when $V_1 = -10.0$ volt, weak inversion is expected because the estimated turn-on voltage is $V_T \simeq 9.5$ volt. The purpose of the different ranges is to investigate a variety of processes of minority carrier recombination.

First, storage time was measured by setting $\Delta t' = 1$ μsec and varying Δt. For both gate voltage ranges $T_s = 10$ msec. (The sample was deliberately chosen to have a short storage time because this permits a higher repetition rate for the T_{inj} measurement cycle and hence easier observation of the peaks.)

The results of the T_{inj} measurements are shown in Figure 5-16. Both V_p and V_q behave as expected. Recalling the criterion for locating storage time as maximum curvature before leveling off, we find from both V_q curves that $T_{inj} = 9$ μsec. Assuming an exponential decay, this converts to a characteristic lifetime of 4 μsec. For comparison we note that the bulk minority

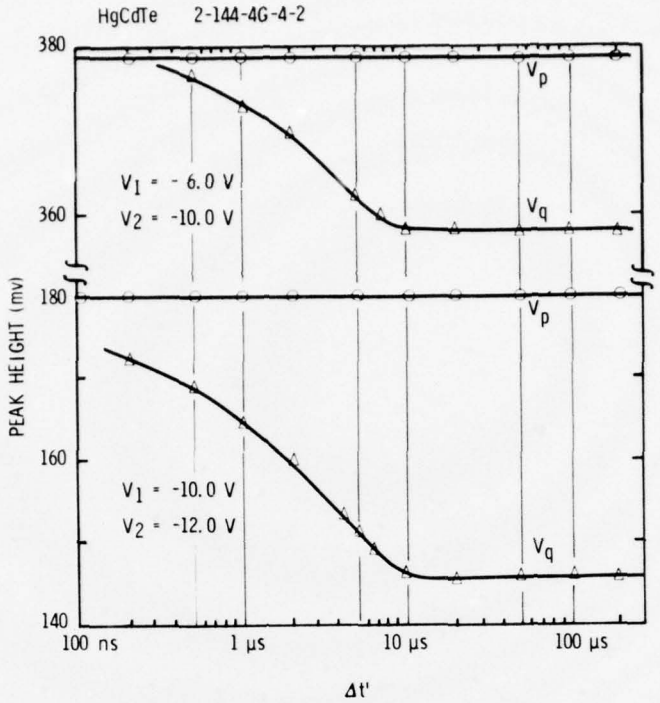


Figure 5-16. Injection Time Measurement: Positive (V_p) and Negative (V_q) Peak Heights versus Time $\Delta t'$ for Two Gate Voltage Ranges. Both V_q Curves Indicate T_{inj} = 9 µsec

lifetime measured at 77°K in the original HgCdTe crystal is 1.2 µsec. Also the Zerbst-plot effective lifetime for a thick sample from the same crystal (Figure 5-3) is 3.0 µsec. The agreement among these three lifetimes is within experimental error. Also, the equality of T_{inj} for the two gate voltage ranges suggests that the same mechanism is operating to recombine minority carriers at V_1 = -6.0 volt and V_1 = -10.0 volt.

Another result is the successful measurement of an approximate storage time in spite of using $\Delta t' < T_{inj}$. Since the well is only partially emptied at the beginning of Δt, the measured value is shorter than the true T_s, but it is of the same order of magnitude.

Injection time is of critical importance to the efficient operation of a multi-element substrate injection detector array. If 9 or 10 μsec must be allowed for the readout and reset of each element, then a large array could not be cycled fast enough to meet forseeable system requirements. Although further study of injection times is needed, our data suggest that large substrate injection arrays on 5-μm HgCdTe would be severely limited in speed.

Section 6

RADIOMETRY

Radiometric measurements were made with the system described under Radiometric Technique (page 3-9) in Section 3. Signal, noise, and detectivity as functions of chopper frequency are shown in Figure 6-1 for a 5-μm n-type sample with a transparent gate. From the spectral response curve, Figure 6-2, the cutoff wavelength λ_{co} = 5.2 μm and the peak wavelength λ_p = 5.1 μm were determined, and the blackbody-to-peak detectivity conversion factor β = 6.083 was calculated. Background flux at the detector was corrected for the 45% transmittance of the 77°K Ge filter. Blackbody irradiance was corrected for the Ge filter and the 69% transmittance of the IRtran-4 dewar window. The small 9.5° FOV (f/6.0) provided a relatively low background flux. The BLIP limit at peak wavelength $D^*(BLIP)(\lambda_p)$ was calculated to be 1.77×10^{12} cm $Hz^{\frac{1}{2}}$/watt assuming a quantum efficiency of 0.50.

The active photosensitive area A_D was determined by a spot scan as illustrated in Figure 6-3. The photogate was scanned with a 2-mil diameter infrared beam, and points where the signal fell to 50% of maximum were charted. The heavier curve in Figure 6-3 is an outline of the gate as scaled from a photomicrograph of the device. The shape of the gate, as determined in the metal deposition procedure, is a circle plus a rectangular tab with rounded corners. (About one quarter of the samples have this shape and the rest are circular.) The 50% contour follows the gate edge very well. The insensitive area in the interior represents the contact. It is wider than the actual contact area, probably because of scattering from the elevated silver-epoxy. To the left of the contact is the shadow of the 2-mil diameter wire lead. The area within the 50% contour is $A_D = 3.8 \times 10^{-3}$ cm^2.

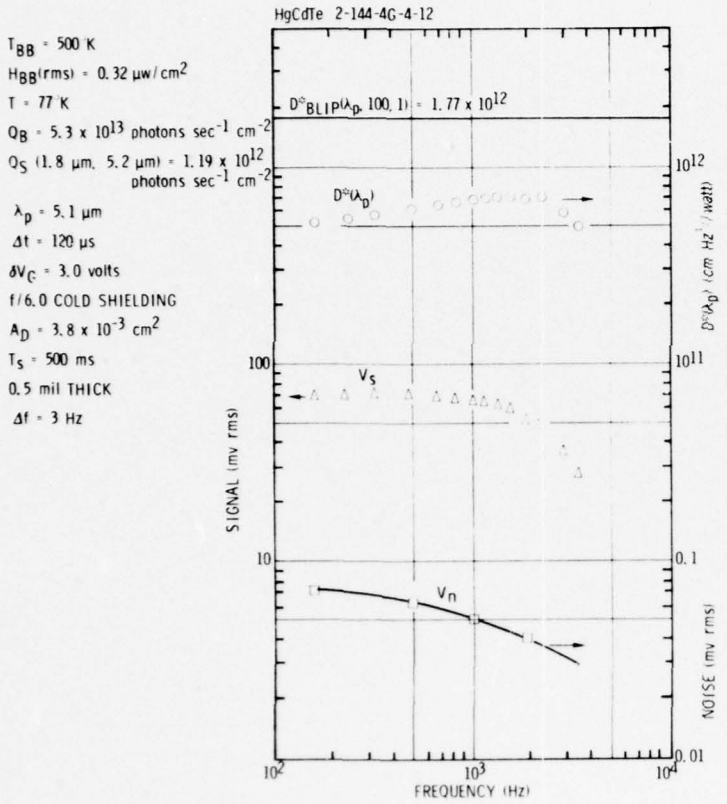


Figure 6-1. Signal, Noise, and Detectivity versus Chopper Frequency for 5-μm n-Type MIS Detector with a 100Å Thick Transparent Gate

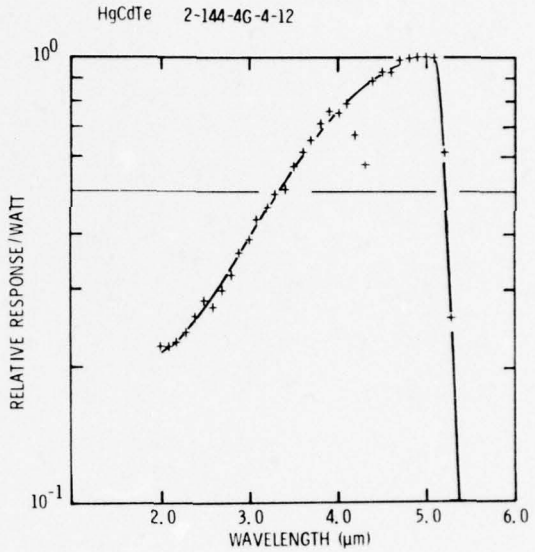


Figure 6-2. Spectral Response of the Same Sample as Figure 6-1

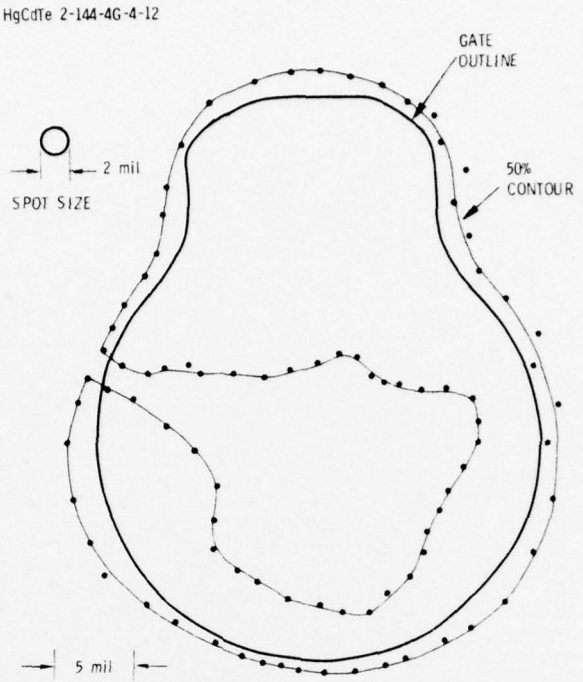


Figure 6-3. Spot Scan of Same Sample as Figure 6-1

Note: Insensitive central area is covered by contact. Shadow of wire lead is to left.

To calculate detectivity $D^*(\lambda_p)$ at the peak wavelength we use

$$D^*(\lambda_p) = \beta \left(\frac{\Delta f}{A_D}\right)^{\frac{1}{2}} \frac{V_S/V_N}{H_{BB}} \qquad (6\text{-}1)$$

where V_S = rms signal voltage

V_N = rms noise voltage in bandwidth Δf

H_{BB} = blackbody irradiance at the detector

β = blackbody-to-peak conversion factor.

Our maximum $D^*(\lambda_p)$ is 7.0×10^{11} cm $Hz^{\frac{1}{2}}$/watt at 1300 Hz.

Responsivity $R(\lambda_p)$ at the peak wavelength is calculated from

$$R(\lambda_p) = \beta \frac{I_S}{H_{BB} A_D} \qquad (6\text{-}2)$$

where I_S is the rms signal current at the detector, from Equation (3-2). $R(\lambda_p)$ versus chopper frequency f_c is simply proportional to V_S of Figure 6-1. The maximum value of $R(\lambda_p)$ occurs over the entire interval of 150 Hz < f_c < 500 Hz, namely $R_{max}(\lambda_p)$ = 2.0 amp/watt.

Quantum efficiency η is found by comparing $R_{max}(\lambda_p)$ to the ideal $R_{id}(\lambda_p) = q\lambda_p/hc$ = 4.11 amp/watt for λ_p = 5.1 μm.

$$\eta = R_{max}(\lambda_p)/R_{id}(\lambda_p) = 0.48$$

Another way to obtain quantum efficiency is to calculate carriers produced per incident photon. At the maximum V_S of Figure 6-1, I_S = 4.03×10^{-10} amp [from Equation (3-2)]. This represents 2.52×10^9 carriers/sec rms. In the relevant wavelength interval (1.8- to 5.2-μm) the incident photon rate over the active detector area is 4.56×10^9 photons/sec rms. Thus η = 0.55.

The agreement between the two values of η is very good. Taking the average for use in subsequent calculations, the MIS device quantum efficiency is η = 0.53.

The quantum efficiency of the device contains contributions from the semiconductor and from the insulator and photogate:

$$\eta = \tau_{ins}\, \tau_{gate}\, \eta_s \qquad (6\text{-}3)$$

where η_s is the actual semiconductor quantum efficiency, and τ_{ins} and τ_{gate} are the transmittances of the 3700Å ZnS insulator and the 100Å Ni photogate, respectively. From the theory of antireflection coatings, 3700Å of ZnS gives τ_{ins} = 0.88 at λ = 5 μm. Estimating an absorption length of 1000Å for Ni at 5 μm, τ_{gate} = 0.90. Thus

$$\eta_s = 0.67.$$

Corrections to η_s for sample and depletion-region thicknesses are unnecessary for the following reasons. See Figure 6-4 Transmitted intensity versus depth x goes as exp ($-\alpha x$) where the absorption coefficient α

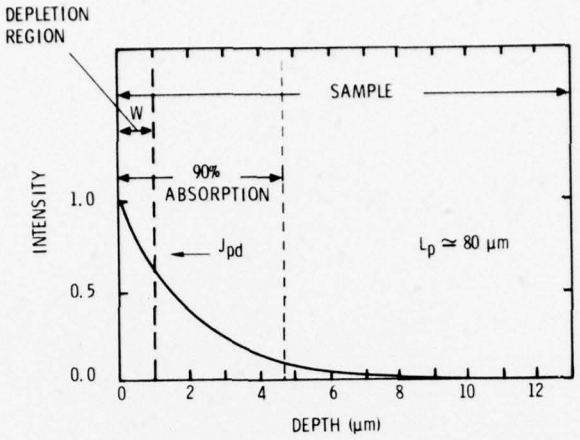


Figure 6-4. Relation of Sample Thickness, Depletion Width, and Absorption Length. Minority diffusion length is much larger than the other lengths

is estimated to be 5×10^3 cm^{-1} for HgCdTe at 5 μm.[19] Within the full 13-μm (0.5-mil) sample thickness 99.8% of the radiation is abosrbed. Within a typical 1-μm depletion width 39% is absorbed. The remaining 61% is absorbed in the neutral bulk. Since the depletion region acts as a sink for minority carriers (holes), a hole diffusion current J_{pd} flows from the neutral bulk into the depletion region, thence on to the inversion layer. Collection should be very efficient because the estimated diffusion length L_p is 80 μm. Also the hole bulk lifetime, about 3 μsec, is much smaller than the circuit integration time, Δt = 120 μsec. The back side repels holes because of fixed positive charges in the passivation layer. Theoretical quantum efficiency is[20]

$$1 - \frac{\exp(-\alpha W)}{1 + \alpha L_p} = 0.99 \qquad (6\text{-}4)$$

where W is the depletion width, and the above-specified parameters have been inserted. The difference between this and the observed η_s = 0.67 may be due to errors in estimating transmittances and to non-electronic modes of absorption.

Returning to detectivity, we consider the reasons why the maximum falls short of BLIP shown in Figure 6-1. Since the quantum efficiency has been found to be close to that assumed for the plotted BLIP, the discrepancy must be due to noise in excess of the background photon contribution. Some noise may originate in the MIS device, but the majority probably comes from the external circuitry. The shielding of the amplifier, cables, and dewar leads was not optimized. Furthermore, not all amplifier components were chosen for low noise operation. When these are corrected, performance should be much closer to BLIP.

Figure 6-5 shows signal versus integration time Δt at f_c = 395 Hz, for three irradiance levels. Figure 6-6 shows signal versus irradiance at 395 Hz for a fixed Δt = 120 μsec. In both Figures correction of H_{BB} for window transmittance was not necessary. The linearity of signal with respect to irradiance is clearly seen in Figure 6-6.

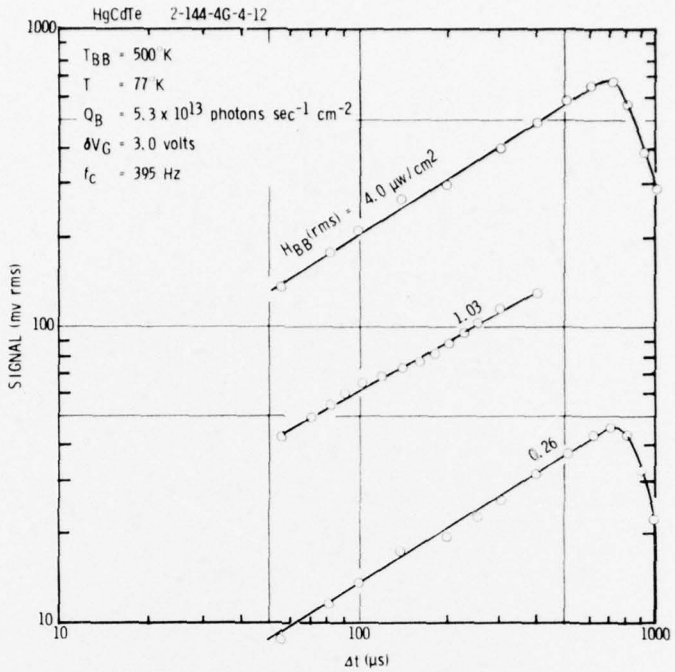


Figure 6-5. Signal versus Integration Time with Irradiance as a Parameter, for the Same Sample as Figure 6-1

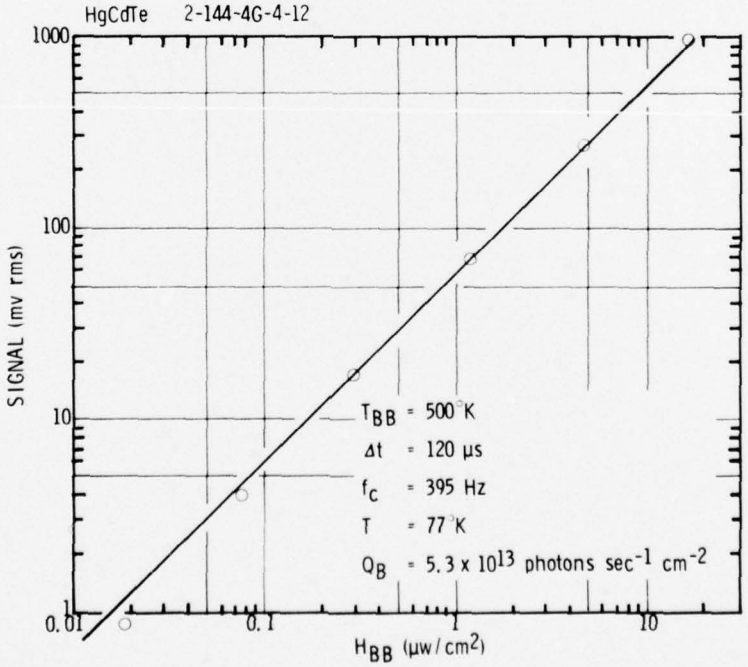


Figure 6-6. Signal versus Irradiance for the Same Sample as Figure 6-1

Section 7
CONCLUSIONS

IMPLICATIONS FOR MONOLITHIC INTRINSIC FOCAL PLANE ARRAYS

As stated in Section 1, the adequate performance of MIS structures on a narrow bandgap semiconductor is necessary for the successful operation of any monolithic intrinsic array of infrared detectors. The purpose of this program was to investigate the feasibility of HgCdTe for such arrays, through the use of MIS devices. The major conclusions of the program are as follows:

1. No CCD, CID, or high-efficiency photogate detector can operate effectively on 12-μm (E_g = 0.1 eV) material. The reason is that for any desirable surface potential and any attainable doping density, interband tunneling current is so large that it immediately fills any storage well. This current cannot be frozen out by a reduction in temperature. Interband tunneling is not merely a state-of-the-art problem, but a basic quantum mechanical limitation.

2. In 5-μm material, over a moderate range of doping density and surface potential, interband tunneling is negligible. It therefore does not prohibit the operation of a CCD or CID.

3. For a CCD in 5-μm material, the measured parameters look very favorable. Storage time between 100 msec and 20 sec was seen for many samples, and a sufficient well capacity, about 10^{11} cm^{-2}, was observed. Well depth was limited to about 1 or 2 volts, but the origin of this limitation is not clear; with additional work the well depth might be increased. Fast interface state density was measured as low as 2×10^{11} cm^{-2} eV^{-1}, which is sufficient to provide good charge transfer efficiency in a moderate-length CCD. Available doping densities, in the 10^{14} cm^{-3} range, are appropriate for CCD operation.

4. For a CID in 5-μm material, performance would be severely restricted by the measured injection time of 9 μsec. To allow this much time for the readout and reset of each element, or row of elements, would cause a large array to cycle too slowly. Further work, however, is necessary to confirm the injection time measurements.

5. No clear preference for n- or p-type doping is seen in 5-μm material. Although n-type samples generally showed the longer storage times, this may be due to processing variables, or to differences other than doping type between the original wafers.

6. Photogate detectors have been shown to perform very well in 5-μm material. Maximum detectivity at peak wavelength was measured to be 7.0×10^{11} cm $Hz^{\frac{1}{2}}$/watt, which falls short of BLIP by a factor of only 2.5. Most of the difference is attributable to amplifier and dewar-lead noise. Quantum efficiency in the semiconductor was estimated to be 0.67.

RECOMMENDATIONS FOR FUTURE WORK

The following items are recommended for continuing tests and analyses of MIS devices on HgCdTe. These apply primarily to 5-μm material unless stated otherwise. A valuable extension of the present program would include:

1. Continuation of the basic measurements of capacitance versus voltage and capaictance versus time because of their proven diagnostic utility.

2. Improvement of surface passivation to reduce fast interface state density, flatband shift, and hysteresis. This work would also take into account antireflection properties and compatibility with photolithographic techniques.

3. A theoretical study of noise sources inherent to a photogate detector.

4. Continuation of radiometric measurements, including reduction of noise, and extension to a variety of cutoff wavelengths.

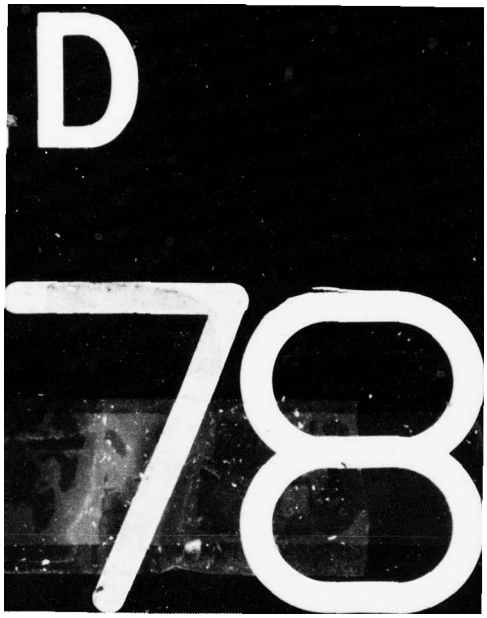
5. Further injection time measurements on a wide variety of samples.

6. Measurement of semiconductor breakdown parameters as functions of temperature to distinguish between tunneling and avalanching; and a study of breakdown at higher temperatures to determine the suitability of HgCdTe for operation up to $T = 150^{\circ}K$.

7. Tests of MIS devices on very thin wafers (< 0.4 mil) of 12-μm material to reduce thermal dark current diffusing from the neutral bulk.

REFERENCES

1. W. W. Anderson, Infrared Physics 17, 147 (1977).
2. E. L. Wolf, Solid State Phys. 20, 7 (1975).
3. C. B. Duke, Tunneling in Solids, Academic Press, New York (1969), page 53.
4. R. D. Thom, private communication.
5. J. L. Schmit, J. Appl. Phys. 41, 2876 (1970).
6. M. Kuhn, Solid State Electronics 13, 873 (1970).
7. C. N. Berglund, IEEE Trans. Electron Devices ED-13, 701 (1966).
8. Final Technical Report, Contract No. DAAK02-74-C-0241, "Indium Antimonide MIS Technology for On-Chip Processing," R. D. Thom, Santa Barbara Research Center, December 1975, Section 8.
9. Circuit design supplied by Dr. Dean Baker, Naval Research Laboratory, Washington, D. C. 20375. Modified by R. A. Chandos.
10. A. S. Grove, Physics and Technology of Semiconductor Devices, Wiley, New York (1967).
11. J. L. Schmit and E. L. Stelzer, J. Appl. Phys. 40, 4865 (1969).
12. S. M. Sze, Physics of Semiconductor Devices, Wiley, New York (1969). Adaptation of equation 28 on page 436.
13. Data for Figure 4-13 assembled by P. R. Bratt.
14. R. Dornhaus, H. Happ, K. H. Muller, G. Nimtz, W. Schlabitz, P. Zaplinski, and G. Bauer: in Proc. XIIth Int. Conf. Phys. Semicond., Stuttgart 1974, ed. by M. H. Pilkuhn (Teubner, Stuttgart, 1974), page 1157.
15. P. R. Bratt, private communication.
16. D. K. Schroder and H. C. Nathanson, Solid-State Electronics 13, 577 (1970).
17. D. K. Schroder and J. Guldberg, Solid-State Electronics 14, 1285 (1971).
18. A. Goetzberger and E. H. Nicollian, Appl. Phys. Lett. 9, 444 (1966).
19. M. D. Blue, Phys. Rev. 134, A226 (1964).
20. D. H. Seib, IEEE Trans. Elec. Dev. ED-21, 210 (1974).


D
78