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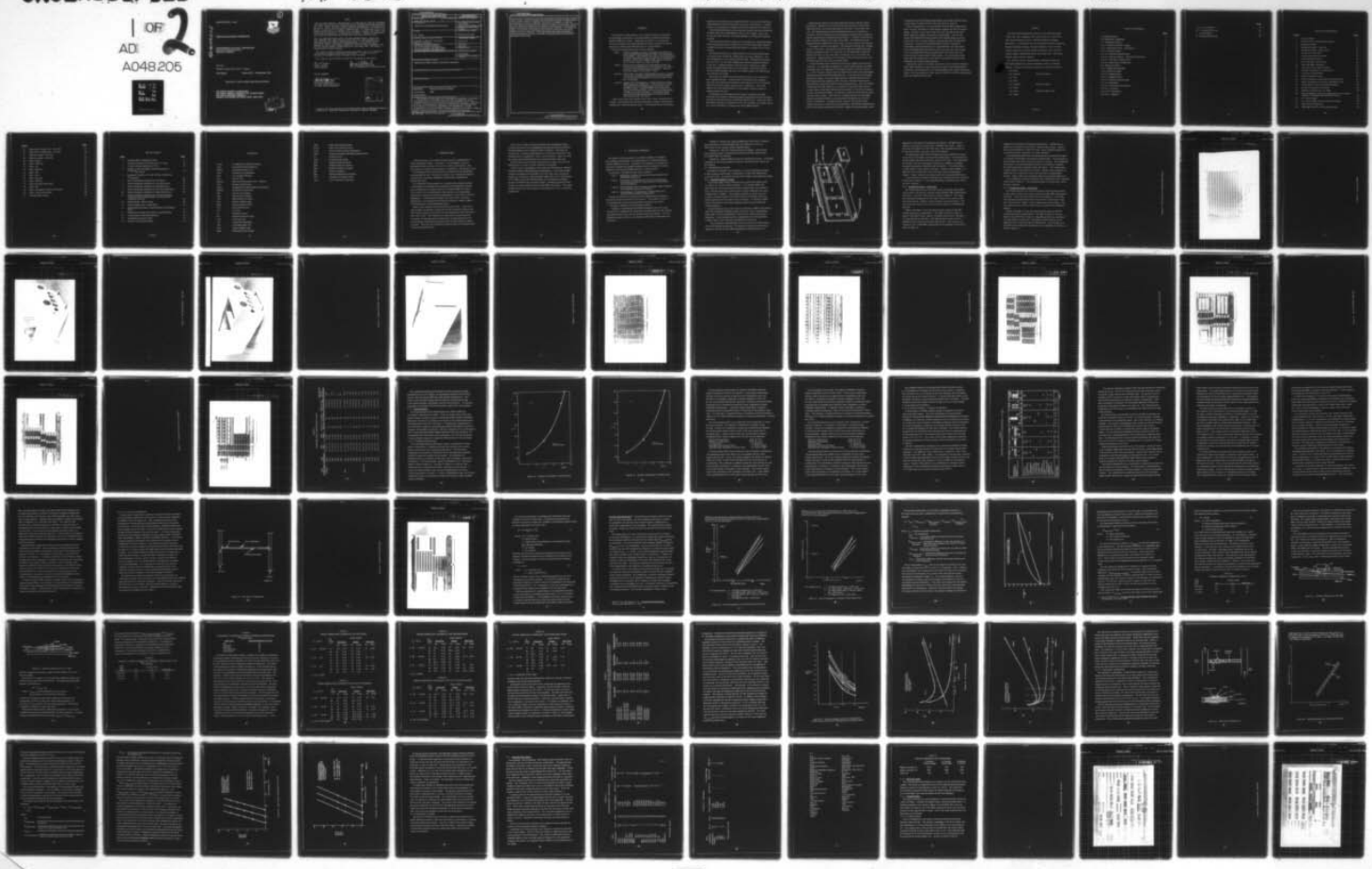

AFAL-TR-76-61, Vol II

MODULAR PACKAGING APPROACHES

WESTINGHOUSE ELECTRIC CORPORATION
Systems Development Divison
Baltimore, Maryland

July 1977

Technical Report AFAL-TR-76-31, Volume II

Final Report 1 March 1976 - 30 September 1976

AIR FORCE AVIONICS LABORATORY
AIR FORCE WRIGHT AERONAUTICAL LABORATORIES
AIR FORCE SYSTEMS COMMAND
WRIGHT-PATTERSON AIR FORCE BASE, OHIO 45433

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This Final Engineering Report covers the work performed between 1 March 1976 and 1 September 1976, under Contract #F33615-75-C-1269, Project/Task/Work Unit #6096-05-48 entitled "Modular Packaging Approaches". It was prepared by the Westinghouse Electric Corporation, Systems Development Division, Baltimore, Maryland for the Air Force Avionics Laboratory, Air Force Wright Aeronautical Labs, Air Force Systems Command, Wright-Patterson Air Force Base, Ohio. The Project Engineer was Mr. David G. McLaine.

This report has been reviewed by the Information Office (OI) and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nationals.

This technical report has been reviewed and is approved for publication.

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The objective of this study is to investigate the feasibility, practicality, and implementation of standard electronic modules (SEM) for avionics. Tradeoff studies are used to provide quantitative SEM format(s). The broad spectrum of considerations necessary to characterize standard packaging for a wide class of avionics applications are investigated. In depth quantification is placed primarily on digital signal processing and to a lesser degree on analog circuitry. The work is performed in four tasks

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whereby Task I evaluates current and past industry and DOD module programs, Task II studies present technology and technological trends for determination of the standard avionics module(s), Task III is a compilation of industry and DOD data concerning standard module information and concepts, and Task IV is the detailed development and evaluation of the proposed "Westinghouse SEM" including the construction of demonstration hardware. The efforts of Tasks I, II, and III are described in the previous issued Interim Report AFAL-TR-76-61, Volume I. This Final Report describes the details of the study performed on Task IV with the conclusions made and recommendations for future work.

SUMMARY

The objectives of this program are to perform studies to investigate the feasibility, practicality, and implementation of standard electronic modules (SEM) for avionics. Explicitly, this effort is to perform the necessary tradeoffs and provide quantitative data to assist the Air Force engineers in selecting the SEM format(s) is a timely fashion.

The work was performed in four tasks as follows:

Task I - Conduct quantitative analysis of the past and present industry and DOD module programs where such information was available. The analysis was made on a broad spectrum of systems applications, both for high and low performance aircraft, in the areas of digital radar signal processing and to a lesser degree in analog circuitry.

Task II - Study present technology and technological trends with parametric considerations for data pertinent to the determination of the standard avionics module(s). Areas of study were again as described in Task I.

Task III - Collect data concerning standardization sources to include all contractor facilities, independent industrial facilities, and all pertinent DOD facilities to insure as wide a data base as possible.

Task IV - Evaluate the "Westinghouse" standard Electronic Module (SEM) packaging configuration. The evaluation covered repartitioning several digital signal processors using the SEM concept. Tradeoff studies were conducted in the areas of weight/volume, and cost to show the benefits of SEM versus custom designs. A mechanical model was detail designed and fabricated to demonstrate the SEM concept to the LRU level.

Tasks I and II were both studied in four major areas: functional partitioning, environmental and mechanical interfaces, logistic support costs/maintenance, and technological impact. Concentrated efforts of individual

engineers on the program were supplemented by a series of internal workshops attended by many Westinghouse engineers and scientists. Tradeoff studies were performed to evaluate various data collected in matrix form.

Functional partitioning of past and present systems have been influenced by things other than standardization such as cost, weight, volume, etc. It was concluded, however, that standardization is possible and should be pursued.

Environmental interfaces appear to be no problem for standard modules. Reviewing both high and low performance aircraft requirements indicates a standard avionics environmental specification is possible and is recommended.

Mechanical interfaces are highly dependent on functional partitioning. I/O requirements and device configurations are major influences. The LRU configuration is the starting point for SEM. Westinghouse proposed the ATR (1/2, 3/4, and full) configuration as being a practical approach to the LRU. Standard printed circuit card sizes as well as an initial family of standard SEM sizes are recommended. Data indicates that size and weight penalties will exist, but careful design of the SEM family can minimize the penalty.

Life cycle cost studies show that acquisition cost is more significant than originally thought. It appears that the predicted high reliability from both the improved semiconductor technology and the use of standardization has reduced logistic support cost to a minimum. This would indicate that with standardization a strong efforts should be placed on reducing hardware costs.

Technology and technological trends appear compatible with SEM. Emerging semiconductor technology appears promising with more functions per chip at low power levels as promised with I^2L logic. Also major DOD and industry thrusts in development of low cost materials and designs should be a major contributor to reducing cost of the SEM hardware.

Repartitioning studies of two digital signal processors indicate a good potential for "standard" electrical functions which can have a high level of usage both within and between equipments of this type. It was found, however, that approximately 25 percent additional devices are required in a "standard" function implementation having high commonality when compared with the existing custom design signal processors. It should be noted that no major circuitry changes were made in this study. The additional devices required would be significantly less if major circuitry changes were allowed.

Two types of circuits were defined. The functional type circuits, ranging from 5 to 21 devices, are testable as functions while the nonfunctional type circuits, generally of only 3 or 4 devices, are not identifiable by specific function but rather occur in the same arrangement many times within both processors. Approximately 60 to 70 percent of both processors can be constructed using these two types of potential SEMs.

Trade-off studies were conducted in the areas of weight/volume and life cycle cost. It is generally accepted that a custom design system is smaller and lighter than one employing a SEM design; however, the type of devices (i.e., DIP, flat pack, hybrid) used can influence the extent of the size/weight penality associated with SEM implementation. In the case of the two signal processors studied, the custom implementation employed DIP devices and SEM implementations employing DIP, flat pack, and hybrid devices were postulated for comparison with the custom implementation. The use of SEMs constructed with DIPs resulted in a processor 150 percent larger than the custom design, while SEMs with flat packs resulted in a 50 percent increase in size, and with hybrid SEMs, the processor would be only 20 percent larger than the custom design. Thus it can be concluded that the size and weight penalty associated with SEM can be minimized through the use of hybrid circuits in the SEMs. It should be noted, however, that the 20 percent penalty cited above is valid only when comparing a hybrid SEM implementation with a DIP custom implementation and that a higher percentage penalty would

be expected if the hybrid SEM implementation were being compared with a custom design of higher density such as flat packs or hybrids.

When considering cost, it was found that all three SEM configurations (DIP, flat pack, hybrid) had a lower logistic support cost than the custom design. However, in the case of life cycle cost, the DIP and flat pack SEM's reflected a higher cost than the custom design. This was the result of the additional devices needed in the standard design as well as the fact that even in custom designs, automatic insertion of components is possible. In the case of the hybrid SEM's (which is currently a costly hand-assembled operation) it is projected that a low cost hybrid can be developed which will result in lower cost than the custom design. A low cost hybrid SEM design is projected that shows life cycle cost about 8 percent lower than the custom design. The assumptions made were felt to be conservative, and if the low cost hybrid concept is fully developed, the savings could be greater.

The work of tasks I, II and III is reported in AFAL-TR-76-61 Volume I. This report describes the work performed on task IV and detailed data is presented, conclusions drawn, and recommendations for further studies are made. Work was performed under contract F33615-75-C-1269, project/task/work unit numbers 6096-05-48.

PREFACE

This Final Engineering Report covers the work performed between 1 March 1976, and 1 September 1976, under contract No. F33615-75-C-1269, Project/Task/Work Unit No. 6096-05-48 "Modular Packaging Approaches". It was prepared by the Westinghouse Electric Corporation, Systems Development Division, Baltimore Maryland for the Air Force Avionics Laboratory, Air Force Wright Aeronautical Labs, Air Force Systems Command, Wright-Patterson Air Force Base, Ohio. The Project Engineer was Mr. David G. McLaine.

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G.L. Kaiser	
E.R. Levitt	Logistics Support Cost
J.H. Pessin	

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ACRONYMS

AADC	-	All Applications Digital Computer
AGE	-	Associated Ground Equipment
ARINC	-	Aeronautical Radio, Inc.
ATE	-	Automatic Test Equipment
ATR	-	Air Transport Racking
BIT	-	Built In Test
BORAM	-	Block Oriented Random Access Memory
CCC	-	Charge Coupled Device
CMOS	-	Complimentary Metal Oxide Semiconductor
CONUS	-	Continental United States
DIP	-	Dual In Line Package
DOD	-	Department of Defense
DSP	-	Digital Signal Processor
ECL	-	Emitter Coupled Logic
EMP	-	Electro Magnetic Pulse
FIT	-	Fault Isolation Test
FP	-	Flat Pack
IC	-	Integrated Circuit
I^2C	-	Integrated Injection Logic
LCC	-	Life Cycle Cost
LSI	-	Large Scale Integration
LRU	-	Line Replaceable Unit
LSC	-	Logistic Support Cost
MHP	-	Multichip Hybrid Package

MOS	-	Metal Oxide Semiconductor
MTBF	-	Mean Time Between Failure
NAFI	-	Naval Avionics Facility Indianapolis
NASA	-	National Aeronautic and Space Administration
PC	-	Printed Circuit
PWB	-	Printed Wiring Board
SAM	-	Standard Avionics Module
SEM	-	Standard Electronic Module
SHP	-	Standard Hardware Program
SOS	-	Silicon on Saphire
SRA	-	Smallest Replaceable Assembly
T^2L	-	Transistor Transistor Logic
VLSI	-	Very Large Scale Integration

1. INTRODUCTION

Avionics systems are currently characterized by a proliferation of unique packaging concepts. In general, a new packaging concept is developed by each contractor for each new system procurement. This has resulted in rapidly rising acquisition, maintenance, and logistics costs.

The development and enforcement of commonality and standardization are potentially the key to lowering acquisition cost, reducing maintenance requirements, improving reliability, and improving availability of replacement parts.

The objectives of this program are to perform the necessary studies to investigate the feasibility and practicality of standardization and how best to implement the *standard electronic modules* (SEM) for avionics. These studies have investigated the broad spectrum of considerations necessary to characterize standard packaging for a wide class of avionics applications. Considerations included four major areas: functional partitioning, environmental and mechanical interfaces, logistic support cost/maintenance, and technological impact.

Study on this program has been directed to four tasks. Task I was a study making a quantitative analysis of the past and present industry and DOD module programs where such data was available in each of the above four major areas. This analysis was made across a broad spectrum of systems on both high and low performance aircraft primarily in the area of digital radar signal processing and to a lesser degree on analog circuitry. This task was to determine what has been or is being done and what are the driving forces.

Task II was a study of present technology and technological trends. Pertinent parameters were highlighted to provide the data necessary for the determination of the standard avionics module(s). This task was to determine, assuming standardization was the primary objective, what driving forces or parameters, if any, were necessary. Again, all of the four major areas mentioned above were areas of study in this task.

Task III was set up to include information from other contractor and DOD sources to insure as broad a data base as possible.

Task IV was an investigation of the proposed "Westinghouse" Standard Electronic Module (SEM) packaging configurations. The proposed SEM concept was designed mechanically to the LRU level and a mechanical model was constructed. Representative digital LRU's were repartitioned for the SEM concept and tradeoff studies were conducted to establish the value of SEM versus the custom design. Prototype electrical model boards were fabricated that demonstrated SEM commonality. The proposed SEM concept was also evaluated for feasibility of its use in analog/RF applications.

2. TECHNICAL PROGRAM

The objective of this program is to perform studies to investigate the feasibility, practicality, and implementation of standard electronic modules (SEM) for avionics. Explicitly, this program is to perform the necessary tradeoffs and provide quantitative data to assist the Air Force engineers in selecting the SEM format(s) in a timely fashion.

The program is divided into four tasks as follows:

Task I - Quantitative Analysis of Past and Present Industry and DOD Module Programs.

Task II - Parametric Consideration of Present Technology and Technological Trends for Determination of the Standard Avionics Module(s).

Task III - Data Collection from Contractor Facilities, DOD Facilities, and Independent Industrial Facilities.

Task IV - Investigation of "Westinghouse" Standard Electronic Module (SEM) packaging configurations

Results of the first three tasks have been reported and discussed in the Interim Report AFAL-TR-76-61 Volume I. The results of Task IV are discussed in this document and further conclusions are drawn.

The effort is divided into the following subtasks:

Subtask I: Detail Design the SEM Mechanically to the LRU Level - Using the ATR configurations, fully design (mechanically) the LRU chassis, the printed wiring cards, and the standard electronic modules. A set of detailed drawings as well as a mechanical model shall be delivered to the Air Force.

Subtask II: Measure the impact of SEM at the LRU Level - Functionally repartition two selected digital LRU's to determine the value of SEM versus custom designs through tradeoff studies.

Subtask III: Fabricate Prototype Electrical Models - Demonstrate inter and intra system commonality with selected printed wiring boards that exhibit SEM commonality.

Subtask IV: Evaluate SEM Concept for Analog/RF Functions - Investigate feasibility of using this packaging concept for standard function analog and RF modules.

2.1 MECHANICAL STUDIES

The efforts of Subtask I were directed to a series of mechanical studies to fully develop, detail design, and fabricate a model of the SEM family to the LRU level. The studies are discussed in detail in the following writeup.

2.1.1 Mechanical Model - Design

The Avionics SEM concept proposed as the result of the efforts spent on Tasks I, II, and III is shown in figure 1. The concept utilizes the basic ATR (Air Transport Racking) chassis configuration with standard-size printed circuit cards containing the circuitry subdivided into small modules known as SEM's. This smaller breakdown is found necessary in order to find the function with a high level of commonality within and between systems from the higher level of circuitry. A "family" of SEM sizes is projected as necessary to package various sizes of functional circuits required.

In determining the sizes to be used in the "family" of SEM's many factors have been considered including number of devices, device configuration, device size, I/O Pin requirements, ATR card size and circuitry power dissipation. Three principal device configurations were felt applicable to SEM - dual-in-line, flat pack, and hybrid microcircuits.

The concept for standardization has been carried to the hole pattern on the ATR printed wiring card. The pattern is based on the DIP device spacing of 100 mils for the fundamental pattern with provisions for a

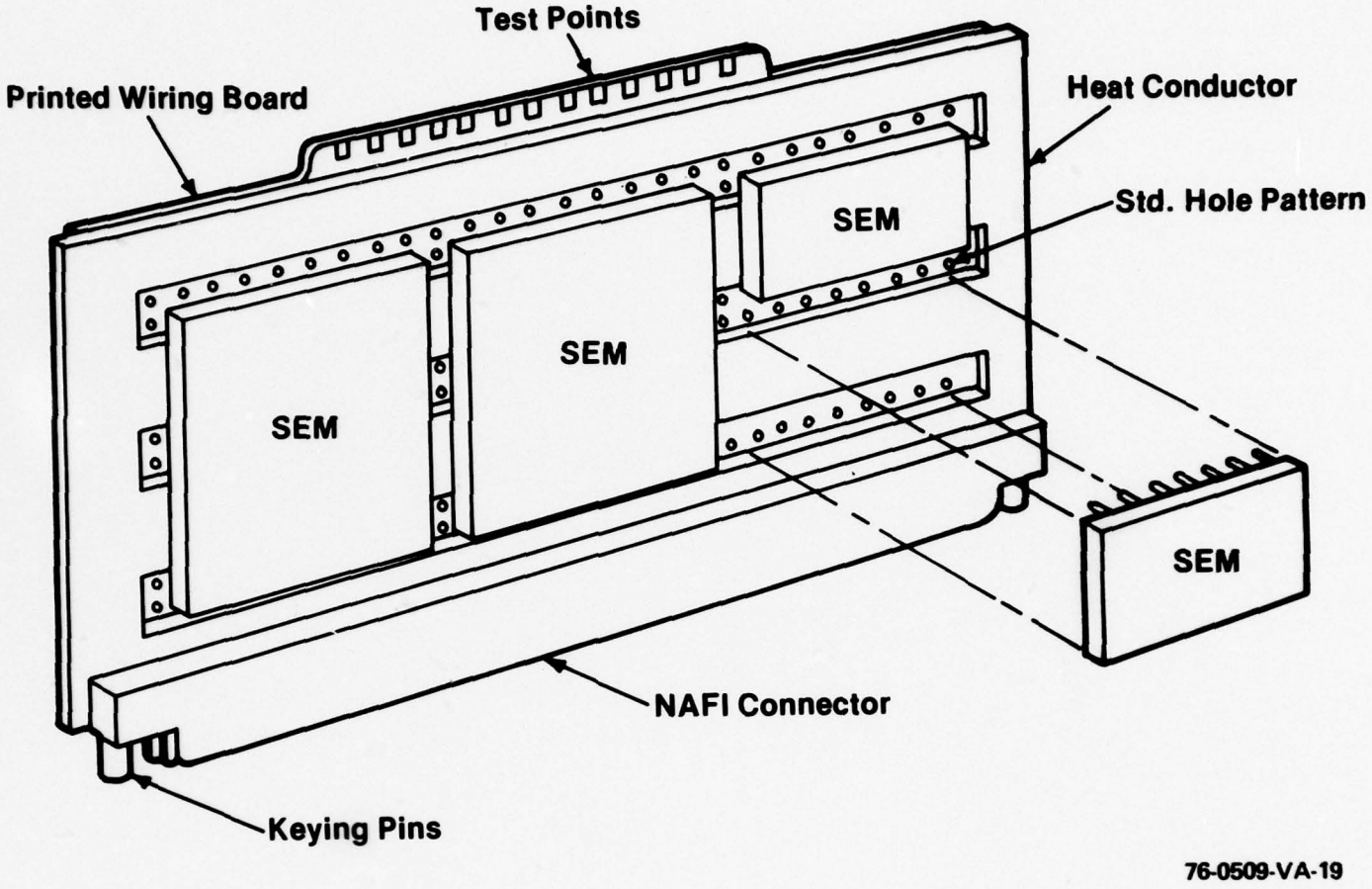

Figure 1. Avionics "SEM"

staggered 50 mil pattern for flat packs and hybrids. All SEM I/O pin patterns are designed to match these "standard" hole arrays. Figure 2 shows the hole pattern on a full ATR card. Other standard features are the thermal overlay, connector, and card extractors.

The partitioning study of the two signal processors indicates two types of circuitry commonality, functional and nonfunctional. The functional circuitry usually required more devices and fewer I/O pins. The nonfunctional circuitry were small groupings of devices not related as a function but appearing together frequently within the system. The nonfunctional circuits require a high number of I/O pins. Based on data available, the SEM sizes were selected for each of the three device configurations studied. Table 1 shows the mechanical data for the proposed SEM sizes.

A set of detailed mechanical drawings were completed for the mechanical model shown in figure 3. The original drawings were delivered to AFAL for their retention.

2.1.2 Mechanical Model - Fabrication

The model delivered was a full ATR chassis containing eight printed wiring cards on which were mounted various possible SEM configurations and sizes. A top view of the chassis is shown in figure 4. The wedge lock clamping arrangement for the cards is shown in the interior right side of the chassis. Figure 5 shows a bottom view of the chassis. The wire wrap pins may be seen as well as the air intakes to the forced air plennum.

Figure 6 and figure 7 show the general custom approach with DIP and flat pack device configurations. The SEM versions are shown in figure 8 using DIP devices, figure 9 using flat pack devices, and figure 10 using hybrid microcircuits. Note that the devices that are not in SEM format are mounted as discrete DIP devices. The concept is not limited to just a single SEM configuration but is adaptable to all three as shown in figure 11.

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Figure 2. Full ATR Card - Standard Hole Pattern

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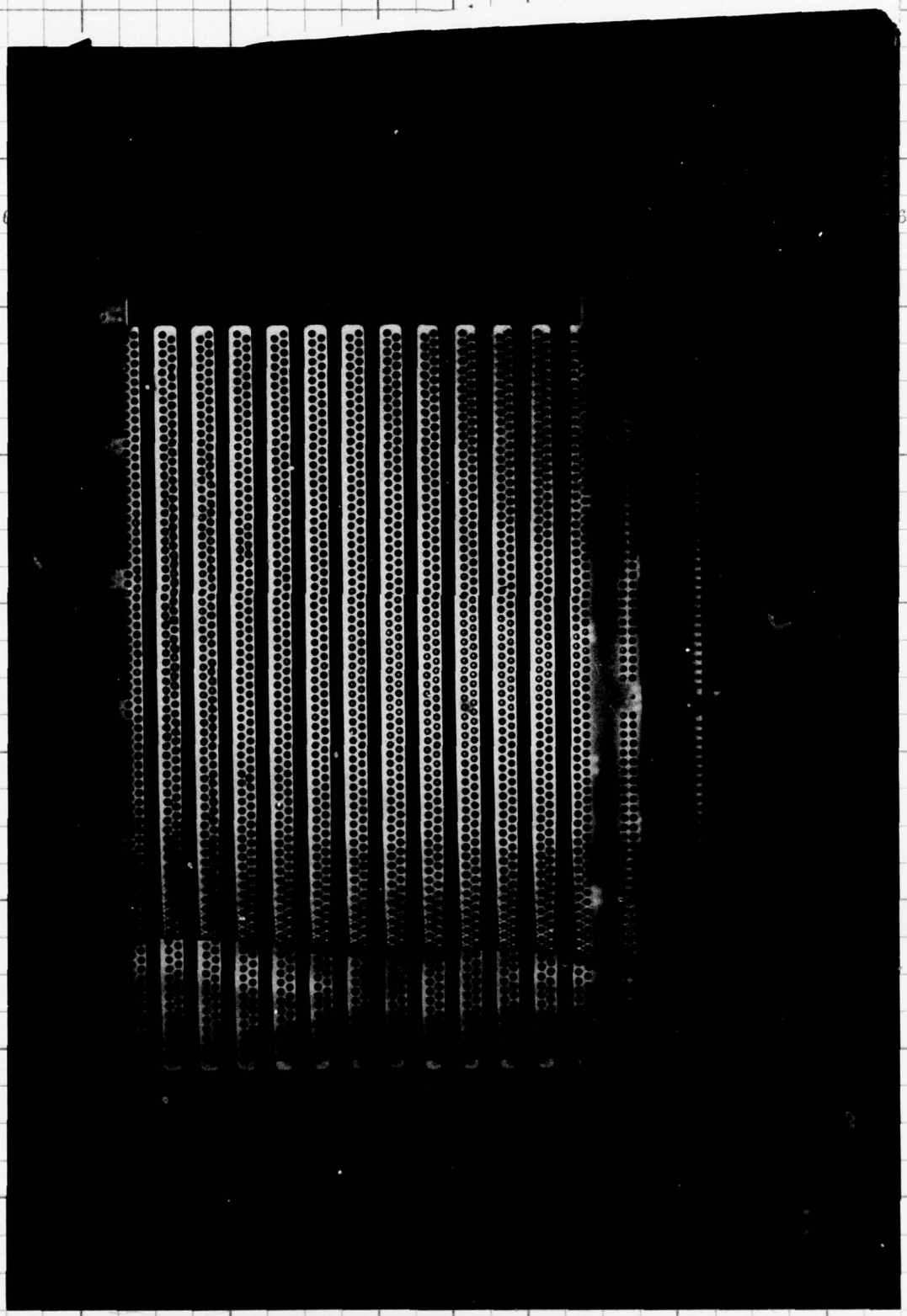

Figure 3. Mechanical Model

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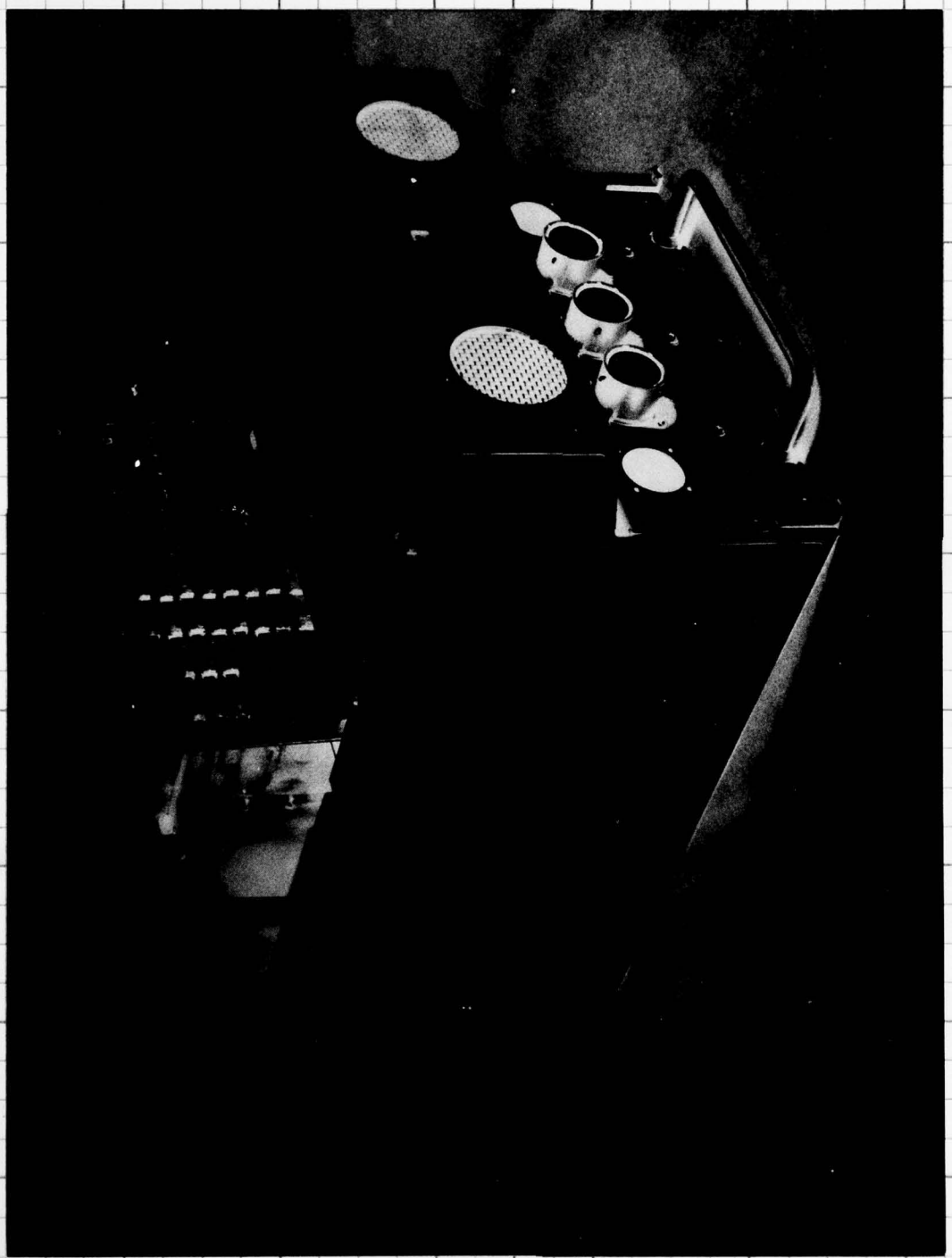

Figure 4. Mechanical Model - Top View

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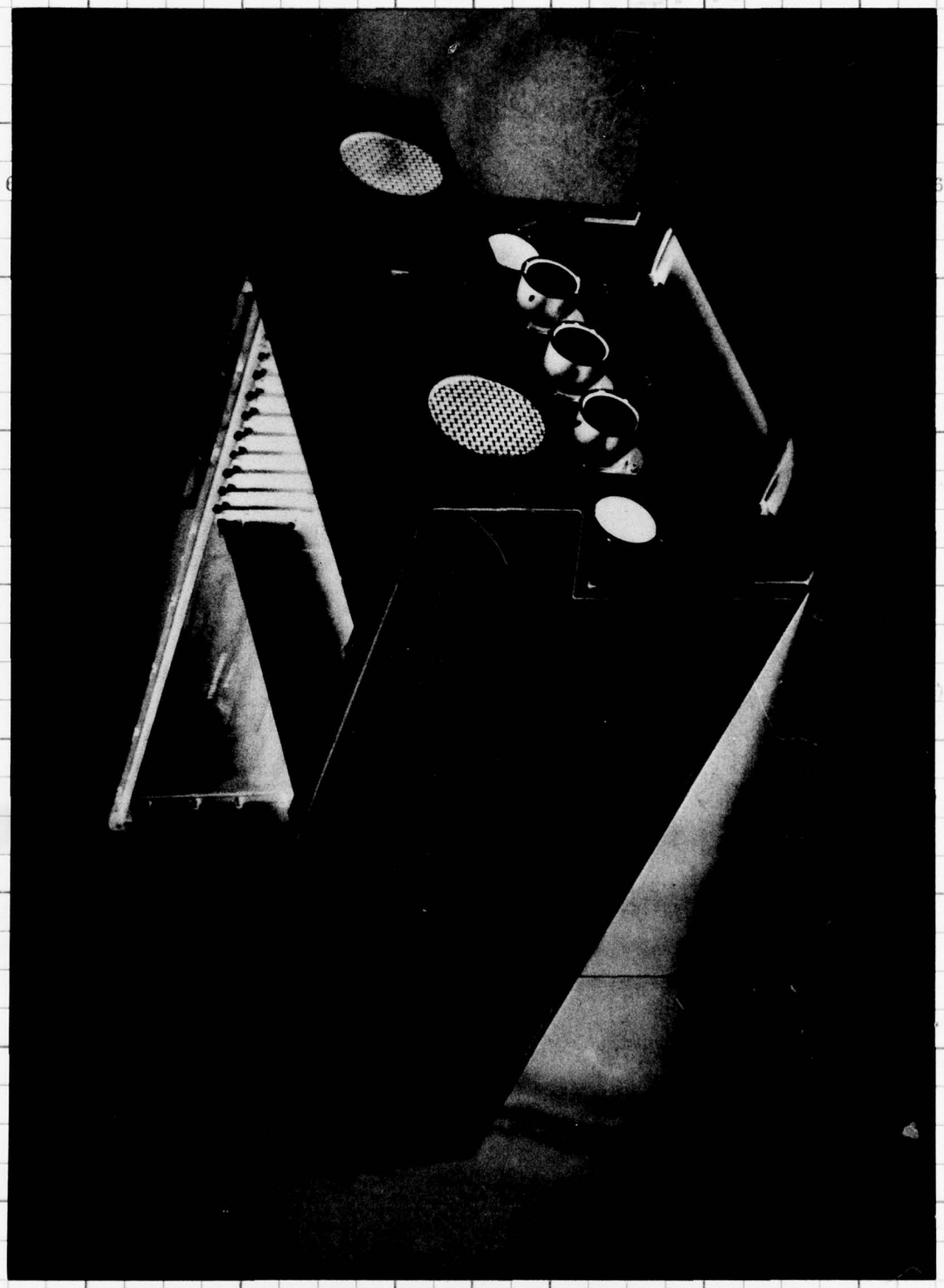

Figure 5. Mechanical Model - Bottom View

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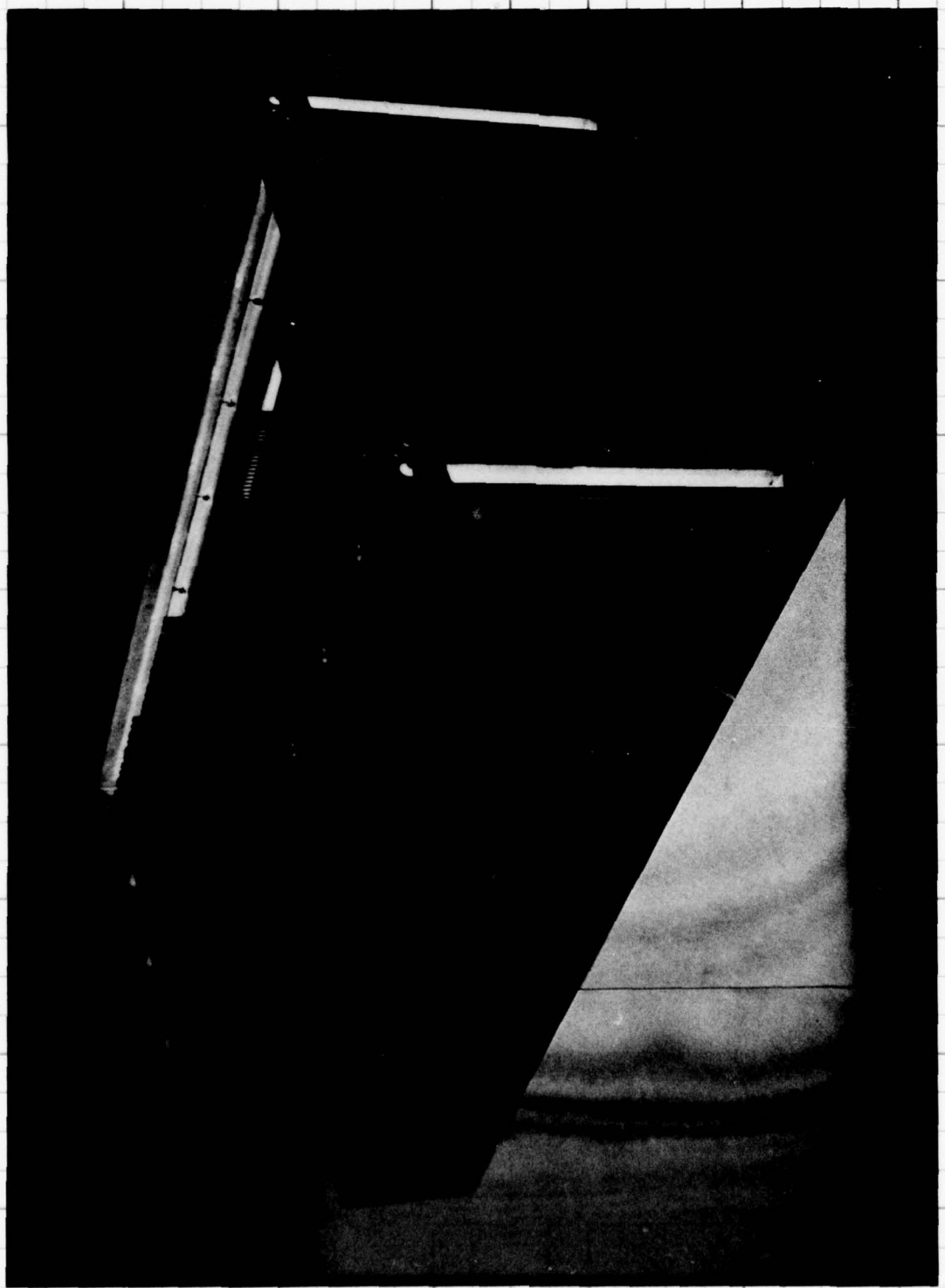

Figure 6. Custom Card with DIP's

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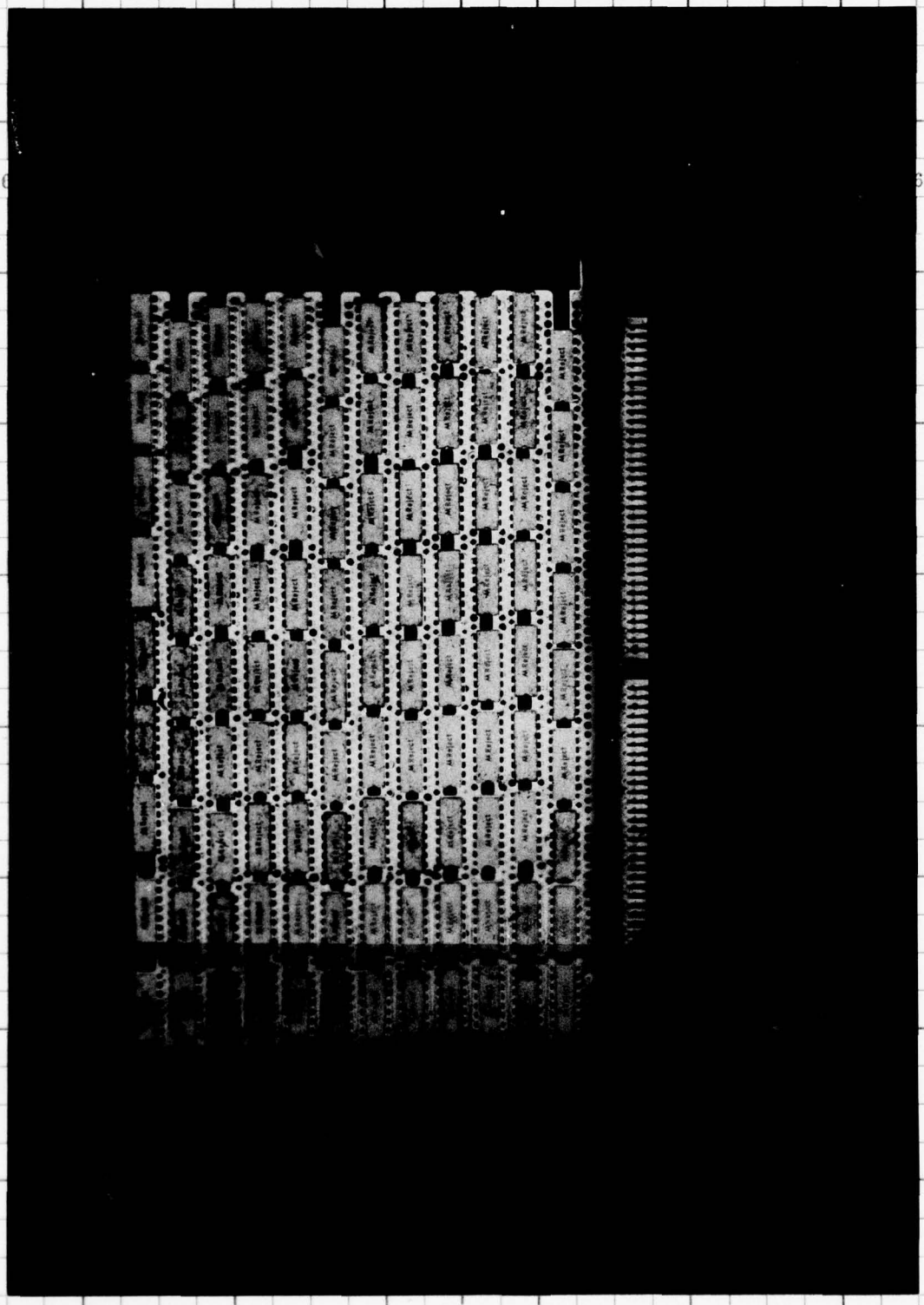

Figure 7. Custom Card with Flat Packs

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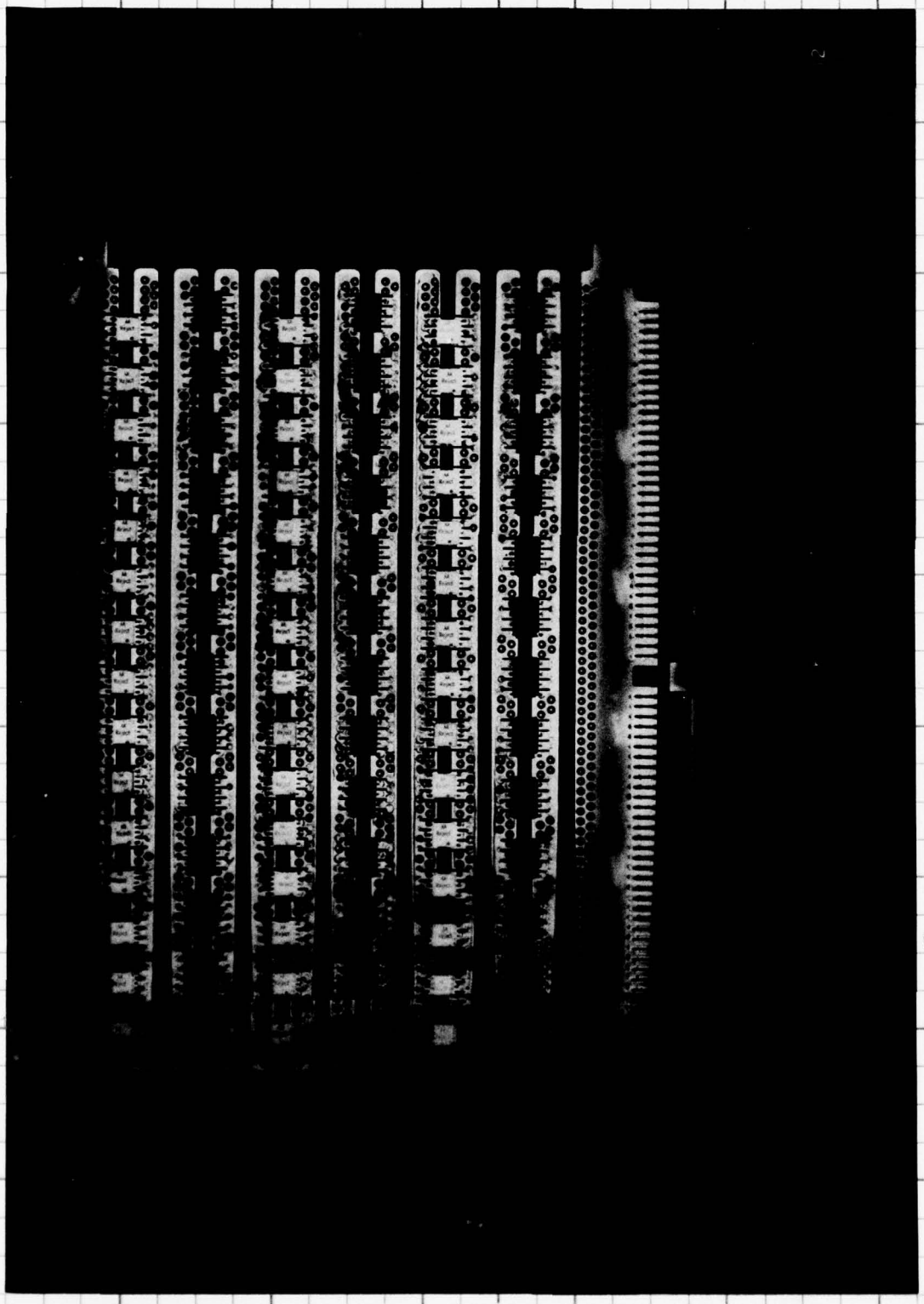

Figure 8. Card with SEM's (DIP's)

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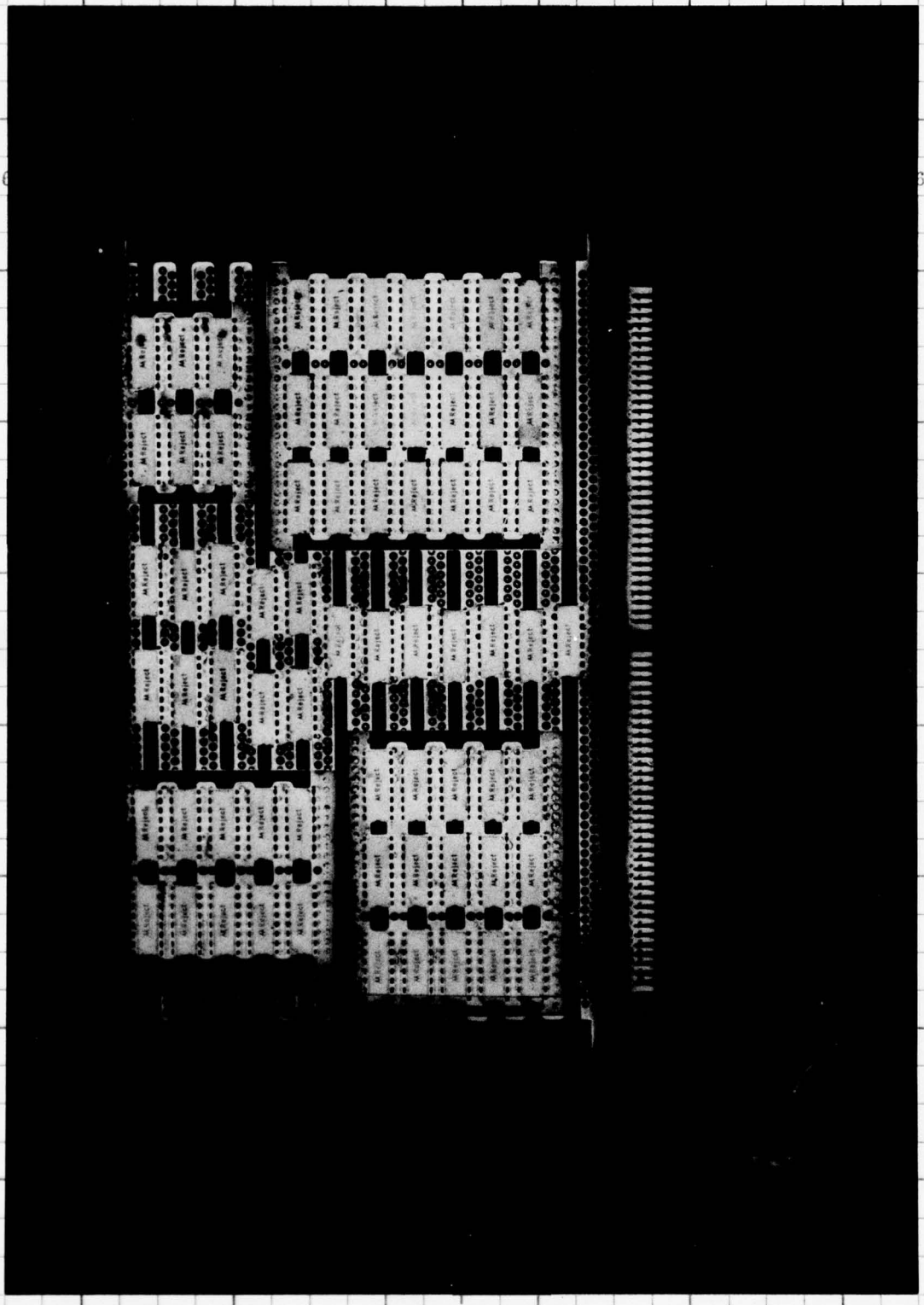

Figure 9. Card with SEM's (Flat Packs)

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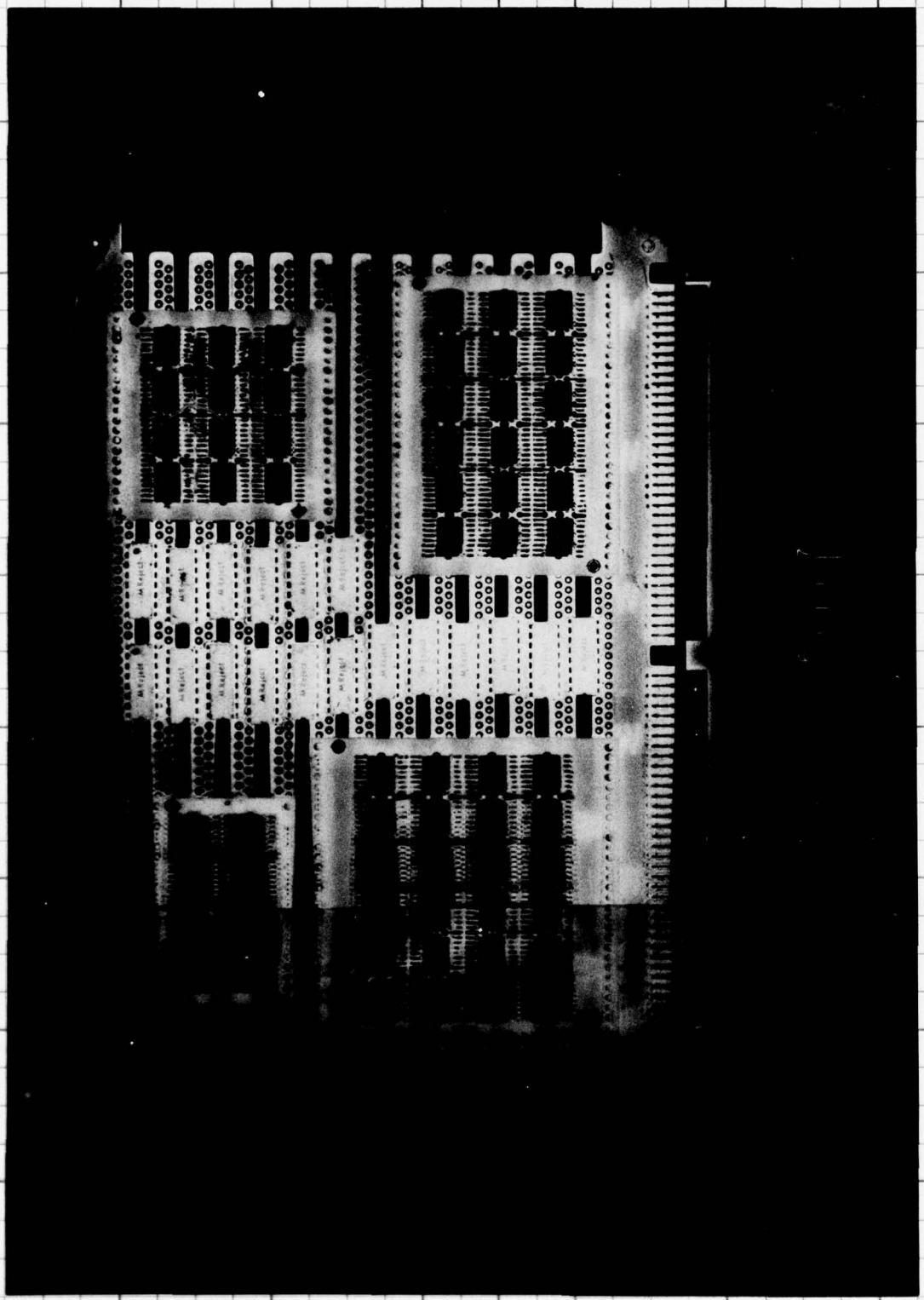

Figure 10. Card with SEM's (Hybrids)

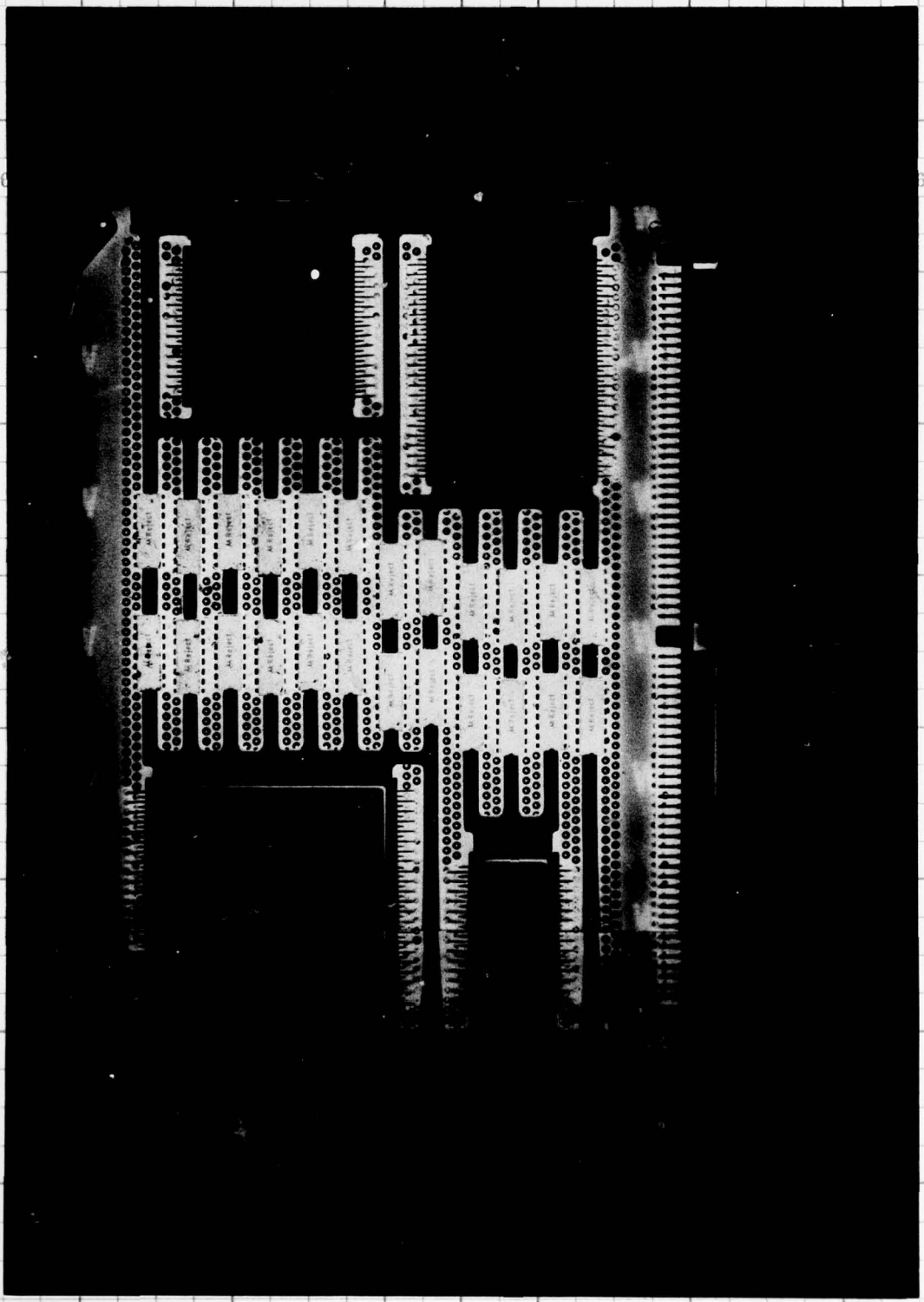

Figure 11. Card with Various Types of SEM's

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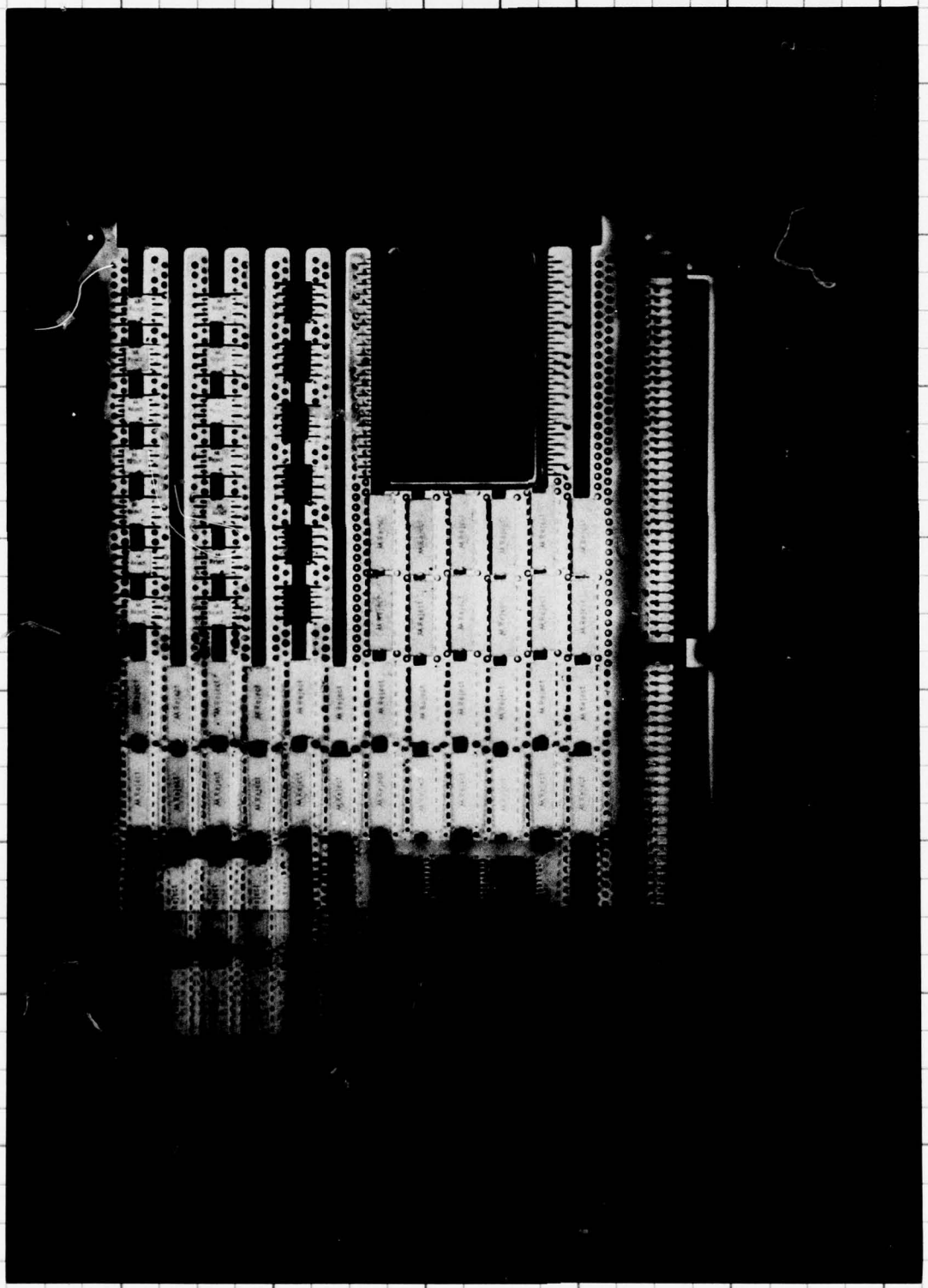

TABLE 1

PROPOSED SEM's (MECHANICAL DATA)

SEM Configuration	SEM Designation	SEM Size	SEM Height	Number of Devices	Number of I/O pins	Effective Bd Area per SEM	Approximate Power Dissipation
Hybrid	H1A	0.6 x 1.6	0.165	5	56	1.0 x 1.6	2.2
	H2A	0.9 x 1.6	0.165	10	56	1.3 x 1.6	3
	H1B	0.9 x 2.4	0.165	16	88	1.3 x 2.4	3.8
	H3A	1.7 x 1.6	0.165	25	56	2.1 x 1.6	5
	H2B	1.7 x 2.4	0.165	40	88	2.1 x 2.4	7
	H3B	2.5 x 2.4	0.165	64	88	2.9 x 2.4	10
DIP	D1A	0.7 x 2.5	0.34	3	46	0.7 x 2.5	0.8
	D2A	1.1 x 2.5	0.34	6	46	1.1 x 2.5	1.5
	D1B	1.1 x 3.8	0.34	8	72	1.1 x 3.8	1.8
	D2B	1.5 x 3.8	0.34	12	72	1.5 x 3.8	2.7
	D3A	2.7 x 2.5	0.34	18	46	2.7 x 2.5	4.2
	D3B	2.7 x 3.8	0.34	24	72	2.7 x 3.8	5.7
Flat Pack	F1A	0.9 x 1.6	0.175	3	30	0.9 x 1.6	0.4
	F2A	1.5 x 1.6	0.175	6	30	1.5 x 1.6	1.0
	F1B	1.5 x 2.1	0.175	8	42	1.5 x 2.1	1.4
	F1C	1.5 x 3.1	0.175	12	60	1.5 x 3.1	2.5
	F2C	2.1 x 3.1	0.175	18	60	2.1 x 3.1	3.5
	F3C	2.7 x 3.1	0.175	24	60	2.7 x 3.1	5.0

The mechanical model fully illustrates the total mechanical concept. Illustrated are the ATR chassis, the appropriate standard ATR card size and the various proposed SEM sizes and possible configurations. Also shown is the total thermal path from the device to the thermal overlay to the chassis interface and finally to the forced air plennum. An extensive discussion is presented on the thermal studies performed on this program.

2.1.3 Thermal Studies

The thermal design of the Standard Electronic Module (SEM) has two primary requirements to fulfill. First, the design must provide adequate cooling to maintain component reliability without violation of Military Standards, and second, the design must conform to the physical dimensions and restrictions of the ATR case sizes. To satisfy these requirements it was necessary to study the environmental conditions provided for numerous systems, the available components and their respective sizes, and the power that is commonly dissipated by digital equipment of the type specified. By accumulating this information and incorporating it into the thermal design, a recommended technique for cooling the SEM chassis has been developed.

2.1.3.1 Analytical Requirements

To successfully design an electronics system, consideration must be given to many factors. Included in this list are elements such as reliability, environment, and mechanical configuration. The first factor, reliability, has increased in importance as the complexity and packaging density of electronics systems has increased. The reliability of a particular device is a function of logic type, chip complexity, and junction temperature. The last property, junction temperature, has a significant effect as shown in figure 12. This data is based on an airborne radar signal processor containing 4100 active, integrated, circuit devices. It can be seen that the failure rate increases significantly as the device junction temperature increases. To have a satisfactory design, the junction temperatures must be maintained at a value low enough to insure adequate system reliability.

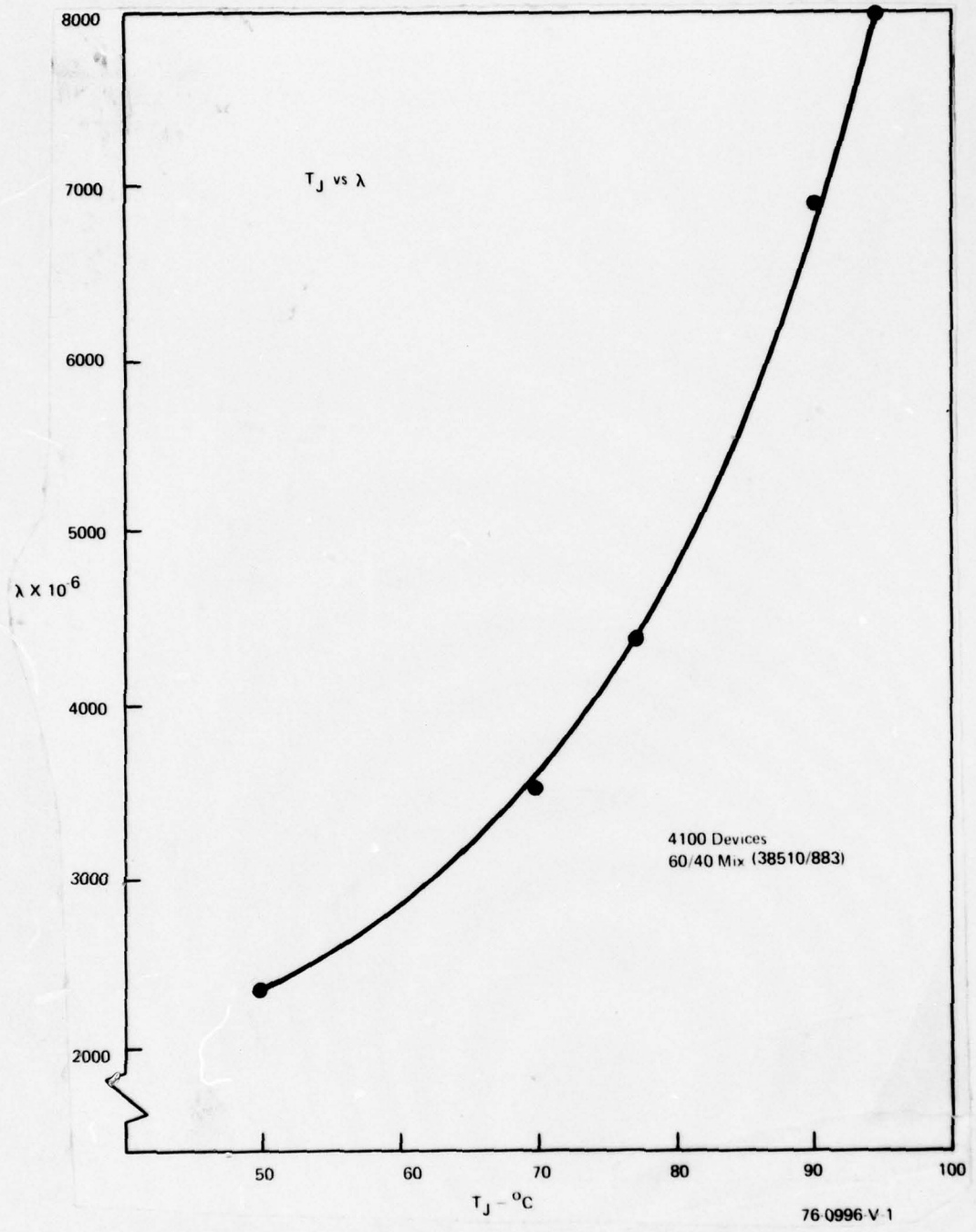

Figure 12. Junction Temperature vs Failure Rate

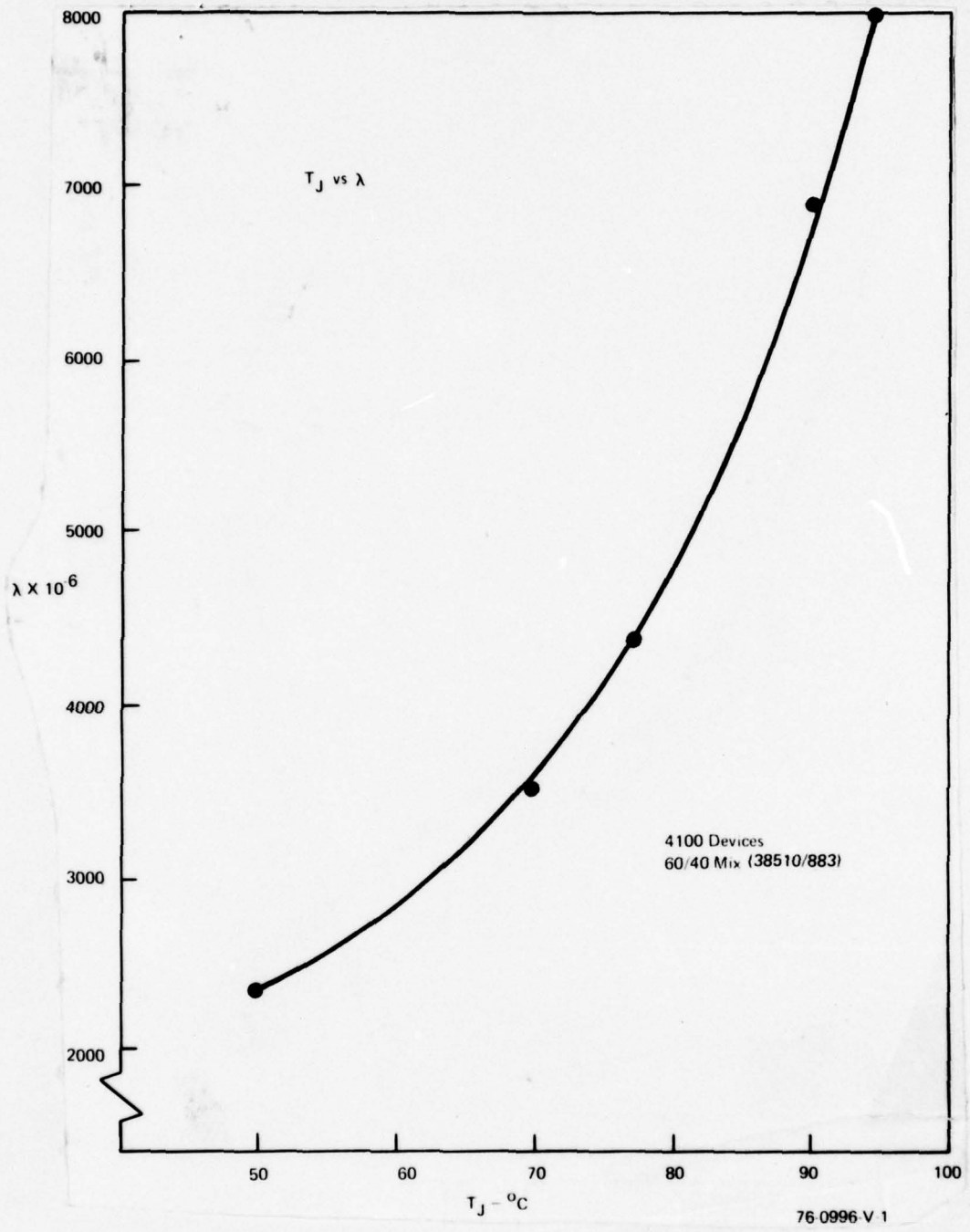

Figure 12. Junction Temperature vs Failure Rate

For the purposes of this study, the maximum allowable component junction temperature has been set at 125°C. This junction temperature has been used in the past as an upper limit for integrated circuits and will allow a reasonable comparison of cooling techniques in this case. For the actual design of electronic equipment, maximum component junction temperatures are normally lower than this value, depending on system reliability requirements. A "typical" design would allow a maximum component junction temperature which is 60 percent of the maximum rated value. For example, a component that has a maximum junction temperature rating of 175°C would be allowed to operate at a junction temperature no greater than 105°C.

The second design factor to be considered is the environment to which the unit is exposed. In an attempt to determine a versatile cooling concept, a survey was conducted to compare the environmental conditions of several present systems and to use the worst case environment as the design guide. Based on this survey, the environmental conditions established as the design conditions for this study are the following:

Inlet Air Temperature:	62°F (16.7°C)
Outlet Air Temperature:	160°F (71.1°C)
Air Flow Rate:	2.4 lb/min-kw
Allowable Unit Pressure Drop:	1.5 inches of H_2O
Allowable Heat Exchanger Pressure Drop:	1.0 inches of H_2O

The third design factor to be considered is the mechanical configuration. The packaging design of the SEM must be compatible with two major design requirements. First, the cooling technique must follow the specifications described in MIL-E-5400 and MIL-STD-454, Requirement 52. In particular, this specification prohibits cooling air from passing over any internal parts, circuitry, or connectors; and consequently, the air must be directed through a cold plate or heat exchanger. The second requirement is that cold plates, heat exchangers, air ducts, etc., must conform to the specified dimensions of the basic chassis design, the ATR case.

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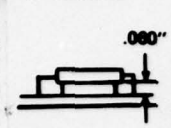
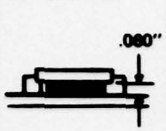
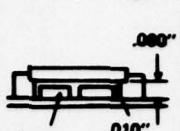
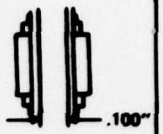
The conditions placed on the design dictate that the cooling concept is a combination of conduction and convection heat transfer. Conduction from the heat source or component to the heat exchanger which dissipates the heat to the air by forced convection. To handle both high and low power dissipation situations, separate thermal designs may be required. The ideal situation would be to provide a thermal design that can be easily adapted to accommodate both situations.

2.1.3.2 General Analysis - Technique Comparison

In determining a versatile cooling concept, an analysis was made of several possible designs. The power dissipation per printed circuit board is 19.4 watts and the maximum component power dissipation is 0.25 watts. In addition, the maximum junction temperature was not enforced, but rather, an average was used to present a meaningful comparison between techniques. For each configuration considered, the average junction temperature for an IC package dissipating 0.25 watts was calculated. The average junction temperature was determined at the location where the air passing through the heat exchanger was at the average temperature between the inlet and outlet (111°F, 43.9°C). The results of this study including the respective temperature differences and the average junction temperatures are shown in table 2.

The first configuration considered was a solid metal conductive overlay between the component and the PC board which is in contact with the heat exchanger. Two different metal overlays were considered: 0.060" thick aluminum and 0.060" thick copper. The advantage of the aluminum conductor is that it weighs approximately one-third of the copper overlay; however, the thermal conductivity of the aluminum is only one-half the conductivity of copper. Because of this difference in conductivity the average junction temperature of the configuration utilizing an aluminum overlay (92°C) is 16°C higher than the one with the copper overlay (76°C).

TABLE 2
COOLING TECHNIQUES (2.4 LB/MIN-KW, 1.5" H_2O)

Air Temperature and Temperature Difference Description (°C) 19.4 w/pwb, .25 w/comp. max	1. Solid Bar 	2. Heat Pipe 	3. Air Passage 	4. Solid Plate 				5. Heat Pipe 		6. Finned Heat Exchanger 	
				A1 w/o PTH	A1 w PTH	Cu w/o PTH	Cu w PTH	w/o PTH	w PTH	w/o PTH	w PTH
– Inlet Air Temp	16.7	16.7	16.7	16.7				16.7		16.7	
–Avg. Air Temp Rise	27.2	27.2	27.2	27.2				27.2		27.2	
– ΔT Wall Heat Exchanger Fins to Air	5.0	5.0		5.0				5.0			
– ΔT Heat Exchanger Wall To Metal Conductor	4.0	4.0		8.0				8.0			
– ΔT Al Conductor-Strips	31										
– ΔT A1 Conductor–Plate				30.4							
– ΔT Cu Conductor-Strips	15.4										
– ΔT Cu Conductor-Plate						14.9					
– ΔT Heat Pipe		1.8						3.2			
– ΔT Tube Surface to Air			13								
– ΔT Coplanar Heat Exchanger Fins to Air										4.3	
– ΔT Printed Wiring Bd (PWB)				17	1	17	1	17	1	17	1
– ΔT Component Case to Mounting Surface	0.5	0.5	0.5	0.5				0.5		0.5	
– ΔT Component Junction to Case	7.5	7.5	7.5	7.5				7.5		7.5	
Average Component Junction Temperature	92 / 76	63	65	112	96	97	81	85	69	73	57

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The second configuration utilized a flat heat pipe between the components and the PC board. This 0.060" thick heat pipe has the condenser section in intimate contact with the heat exchanger wall. The primary thermal resistance of the heat pipe is at the points where heat is conducted into and out of the evaporator and condenser sections, respectively. At the power dissipation considered, the temperature difference between the evaporator and condenser regions was quite low. The average junction temperature was 63°C which is substantially lower than that for the solid metal overlays.

The third technique incorporated a group of parallel air passages between the components and the PC board. Air enters through a manifold, is distributed to the parallel flow paths, and is then collected in an exhaust manifold. The primary disadvantages of this system are that the delivery and distribution tends to be a difficult task, and the tubes must be constructed very carefully to maintain the pressure drop at acceptable values. For the dimensions illustrated and the assumed air flow, the pressure drop is approximately one inch of water for an eight inch long tube. The advantage of this concept is that the conduction path from the heat source to the air stream is minimized, and as a result, the average junction temperature is only 65°C.

Of the three designs described so far, all consider a single PC board as the smallest replaceable assembly (SRA); however, only configurations 1 and 2 could be used in the same chassis. Both of these systems rely on conduction to wall heat exchangers to dissipate the heat. As a result, these two concepts could handle both high and low power situations without requiring any changes to the basic chassis design.

The fourth configuration uses a metal plate to conduct the heat from the two PC boards to a heat exchanger. The metal plate is bonded between the PC boards and provides a mounting surface as well as a heat transfer medium. The configurations considered utilized an 0.063 inch thick plate of either aluminum or copper both with and without plated through

holes (PTH) in the PC board to transfer heat from the source to the conductor plate. The results indicate that it is necessary to provide plated through holes in the PC board because it reduces the temperature difference through the PC board itself by approximately 16°C. Assuming the PC board contained plated through holes beneath the components/SEM's, average junction temperatures of 96°C and 81°C were determined for the aluminum and copper, respectively.

The fifth cooling concept reverts back to a heat pipe, however, in this instance it is represented as a one-tenth inch thick plate. It could be either a wickless heat pipe in the form of a hollow plate or a series of individual heat pipes embedded in a solid plate. Again, the PC boards are bonded to both sides of the plate and the edges are in contact with the heat exchanger walls to transfer heat tothe finned surfaces. With this configuration, the average junction temperature, assuming there are plated through holes in the PC board to conduct heat to the heat pipe plate, is 69°C. The average junction temperature without the PTH is 16°C higher at 85°C. These results again show that the PTH are necessary to maintain junction temperatures at a low value. In addition, it should be noted that the average junction temperature is slightly higher than for configuration 2 because in this situation the heat pipe and the interface at the heat exchanger must transfer the heat dissipated by two PC boards instead of one.

The sixth and final concept places the heat exchanger closer to the heat sources rather than relying on conduction to the finned surface. In this configuration, 0.100" aluminum fin stock is bonded between two PC boards and heat is conducted from the components/SEM's through the PC board to the fins. This concept requires that the walls of the unit act as a distribution plenum from which the PC board pairs are provided the required air supply. The air is passed from the plenum through a sliding gasket which in some instances is a disadvantage because of leakage. This configuration does, however, provide the lowest average junction

temperature provided the PC board contains plated through holes under the components/SEM's to conduct to the heat exchanger. In this situation, the average junction temperature is only 57°C.

The last three designs (4, 5 and 6) have two inherent disadvantages. First, the components/SEM's mounted on the PC boards must have planar leads rather than leads passing through the PC board. Second, the smallest replaceable assembly (SRA) is a pair of PC boards rather than a single one. Both of these disadvantages, however, relate to the cost of the system rather than thermal design.

As was noted in the first three systems, two of these concepts could be accommodated in the same chassis. In fact, with slight modification, configurations 1, 2, 4, and 5 could all be accommodated in a single chassis. These concepts depend on conduction from the heat sources to a mounting tab on the heat exchanger. The two remaining designs could also be accommodated by a second chassis design in which air is collected in intake and exhaust plenums located at the sides of the ATR case. It is conceivable that these concepts could be used as the high and low power configurations. The air passing through tubes under the components/SEM's could be the low power design since pressure drop limitations will only allow low air flows. The high power configuration would then be configuration 6 in which air passes through fins bonded between two PC boards.

The component considered in the analysis was a dual-in-line package dissipating approximately 0.250 watts. It was assumed that in configurations 1, 2 and 3 it was mounted with leads passing through the PC board and in configurations 4, 5 and 6 it was mounted with the leads parallel to the PC board surface. The reason for using a common device was to present a fair comparison of the cooling concepts.

In general, the thermal resistance of various components are not the same value. In actual practice, however, the temperature difference from the chip junction to the case for dual-in-line or flat pack components mounted on a heat sink are approximately the same. This is primarily

due to the effective heat transfer area of the bottom of the package case. If a good heat conductor is present, both types of packages exhibit about the same effective heat transfer area; and consequently, the same resistance to heat transfer. This generality also applies to hybrid microcircuits when considered on an individual chip basis. The effective heat transfer area, provided the package is mounted on a good heat sink, is approximately the same as that for a single chip in a dual-in-line package or a flat pack. The reason for the low thermal resistance value for a hybrid microcircuit is primarily analytical. In this instance, the maximum temperature difference from the chip junction to the case is divided by the total package power instead of the individual chip power to derive a package thermal resistance.

Special thermal consideration must be given to the SEM's which are constructed on PC boards. These modules are smaller printed circuit boards containing dual-in-line packages or flat packs which plug into the primary PC board. As a consequence of the design, an extra thermal interface is introduced. To minimize the effects of this interface, plated through holes must be provided in the SEM PC board under the components. In addition, a thermally conductive interface must be provided either between the SEM PC board and the thermal overlay or the SEM PC board and the primary PC board as in the case of the fins between PC boards. Since this SEM has an inherent higher thermal resistance than other microelectronic components, it may be necessary to establish an upper limit on the allowable power dissipation for these modules.

To further study the SEM concept, a detailed analysis of two prospective designs utilizing SEM's was conducted. The selection of the configurations were based on the advantages and disadvantages presented for the cooling techniques in table 3. These designs, the low and high power concepts, are described in detail in the following sections.

2.1.3.3 Low Power Configuration

The low power configuration consists of a chassis with heat exchangers in the side walls and printed circuit boards or memory stacks conductively coupled to them (see figure 13). Heat is transfered from the active components to a metal thermal overlay bonded to the face of the printed circuit board. The metal of the overlay provides a conduction path to the heat exchangers in the side wall. The heat is transferred to the air passing through the heat exchanger by forced convection. The active components considered in the analysis include dual-in-line packages (DIP), flat packs (FP), hybrid SEM's, SEM's with DIP's and SEM's with FP's. The thermal overlays analyzed in this portion of the study are the standard overlay configuration as shown in figure 2. The thickness of these overlays is 0.050 inches to insure component lead extension through the PC board, and the width is 9.0 inches to match the width of the memory modules presently available. This standard thermal overlay will at times be replaced by a custom thermal overlay, a sample of which is illustrated in figure 14. The justification for using a custom overlay is based on the fact that power dissipation may vary significantly from component to component in an actual application. As a consequence, when excessive thermal gradients cannot be reduced satisfactorily by placement close to the ends of the standard overlay, a custom design with additional metal to reduce the thermal resistance to the heat exchanger is utilized.

The first step in the thermal analysis of the low power design was to determine the type of fin material which would physically fit in the available space allowed for the wall heat exchangers. Since the overall width of the full ATR case is 10.12 inches, and the PC board width is 9.0 inches, the difference is only 1.12 inches. Allowing for the heat exchanger walls, the maximum fin height was 0.375 inches.

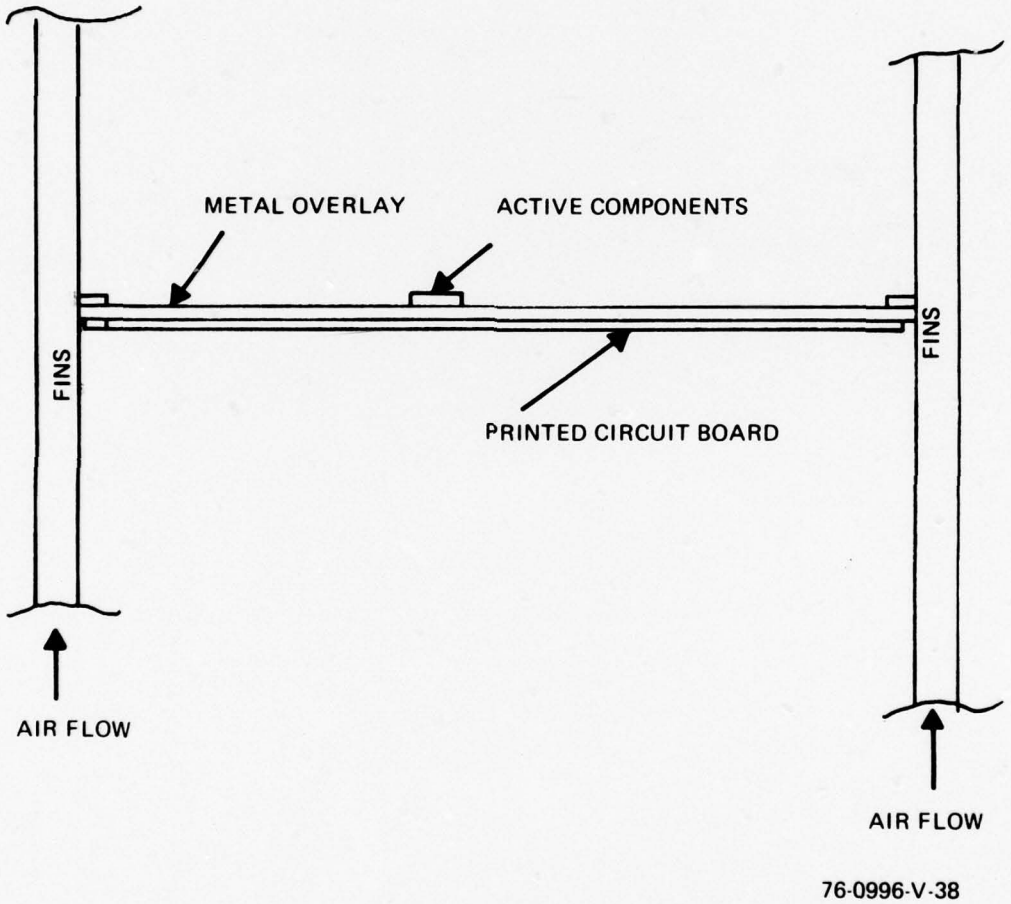
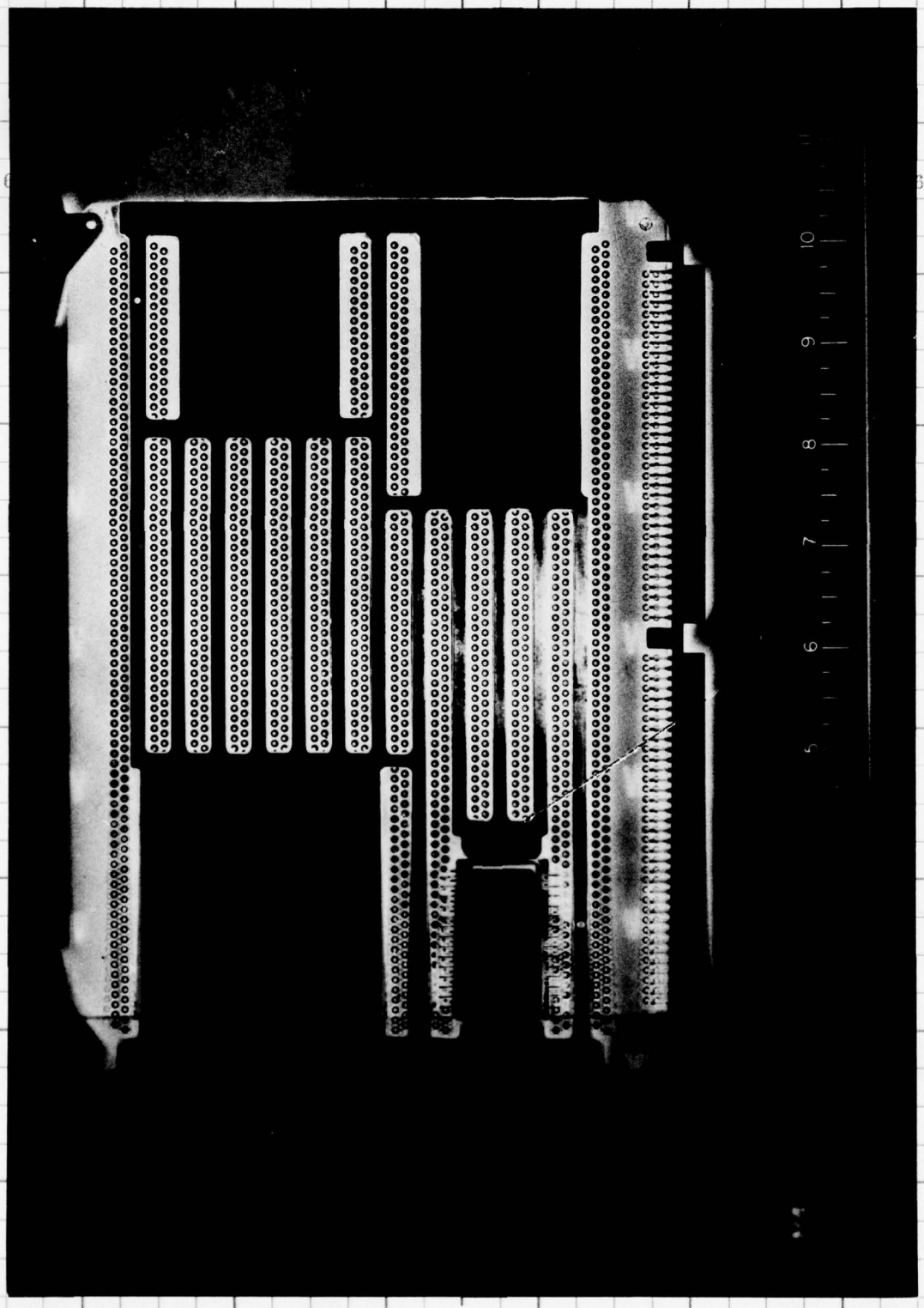


Figure 13. Low Power Configuration

Figure 14. Custom Thermal Overlay



The second consideration in selecting a fin material for the heat exchangers was the pressure drop. To optimize this parameter it becomes necessary to analyze the variables in the following equation which is used to calculate the pressure drop:

$$\Delta P = f\, L/D_H \left[1/2\, \rho V^2\right] \qquad (1)$$

Where ΔP = pressure drop

f = friction factor

L = length of the heat exchangers in the direction of flow

D_H = hydraulic diameter

ρ = air density

V = air velocity

Since the pressure drop is directly proportional to the square of the velocity, the largest reduction can be realized by decreasing the air velocity. The air velocity, as it passes through the heat exchanger, is defined by:

$$V = m/\rho A \qquad (2)$$

where m = mass flow rate

A = cross-sectional area

The air velocity is shown to be inversely proportional to the cross-sectional area of the flow passage. It now becomes apparent that the largest reduction in pressure drop can be obtained by increasing the cross-sectional area. As a consequence, it becomes advantageous to maximize the fin height to the available 0.375 inch dimension.

With the appropriate fin height defined, it was possible to develop curves which show the corrected pressure drop, $\sigma \Delta P$, as a function of unit power dissipation. The calculations were done with the aid of a computer program which has on file the friction factor and heat transfer data for the fin configurations described in Kays and London

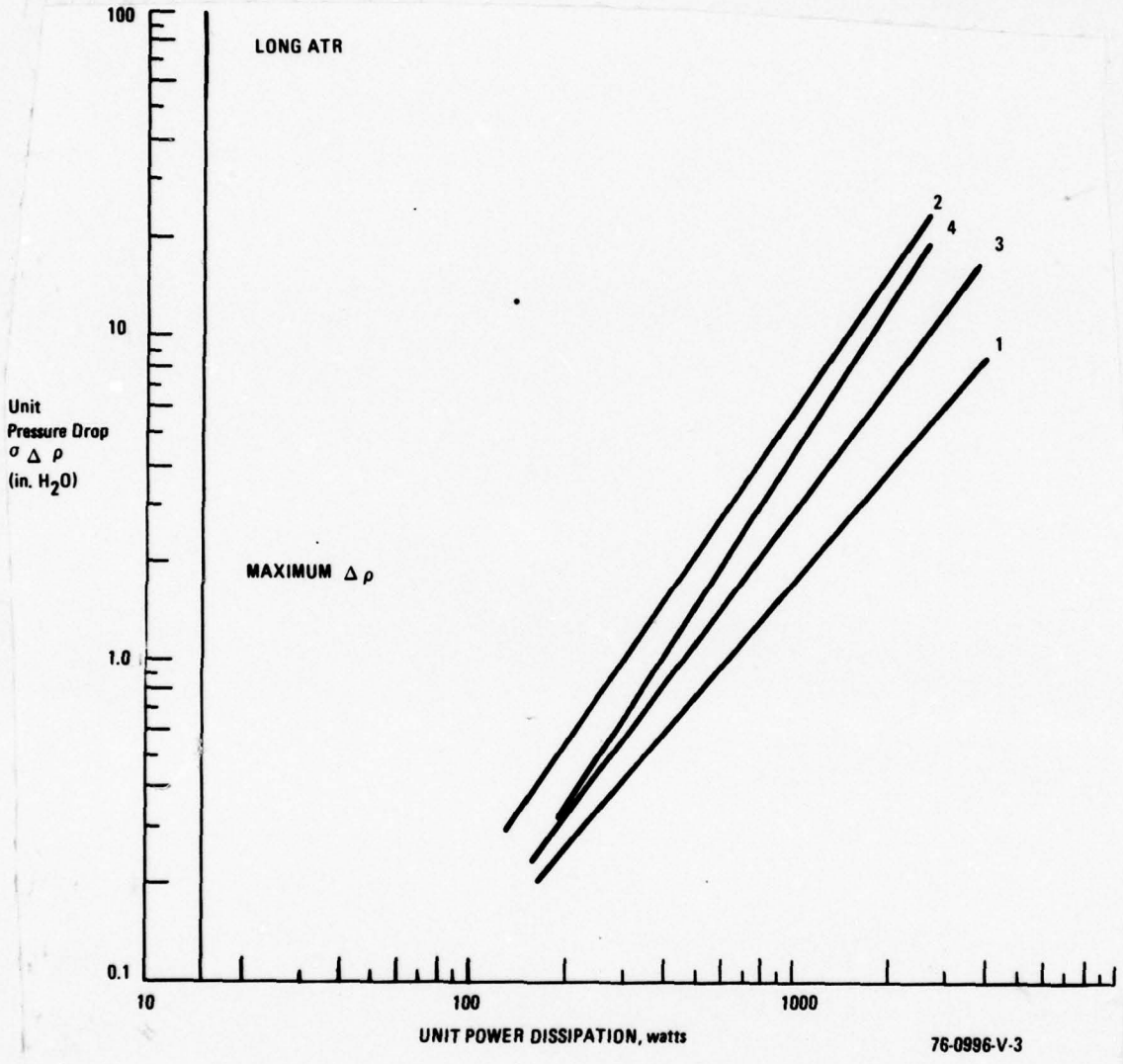
Compact Heat Exchangers[1]. By providing the computer with the air flow rate, the power dissipation, the heat exchanger's dimensions, and the air properties; the pressure drop and heat transfer coefficients for various fin configurations were claculated. The results of this analysis are shown in figures 15 and 16 for the long and short ATR cases respectively.

In studying figures 15 and 16 which show a plot of $\sigma\Delta P$ as a function of unit power dissipation, it is important to realize that another parameter, the temperature difference between the fins and the air $(\Delta T_{\text{fin-air}})$ must be considered. To insure an efficient heat exchanger design, a maximum $\Delta T_{\text{fin-air}}$ of 10°C was established. At the pressure drop of 1.5 inches of H_2O in the long ATR configuration of figure 15, all four fin types satisfy this requirement. As a result, a unit power dissipation of approximately 880 watts is feasible at the air flow rate of 2.4 lb/min-kw. In figure 16, fin type #1 does not satisfy this requirement, and as a consequence, the maximum unit power dissipation in the short ATR configuration is still only about 900 watts. The primary difference between the long and short ATR configurations is the reduction in available surface area.

The second step in the analysis of the low power design was to calculate the maximum unit power dissipation based on the heat transfer capability of the mechanical design. By establishing a maximum component junction temperature of 125°C, it was possible to calculate the maximum power dissipation per PC board for these conductive overlays and eventually a maximum power dissipation per unit. This figure could then be compared to the maximum power dissipation based on pressure drop to determine the controlling parameter - heat transfer capability or pressure drop.

1. Kays, W.M. and London, A.L., Compact Heat Exchangers, McGraw and Hill Book Co., 1964

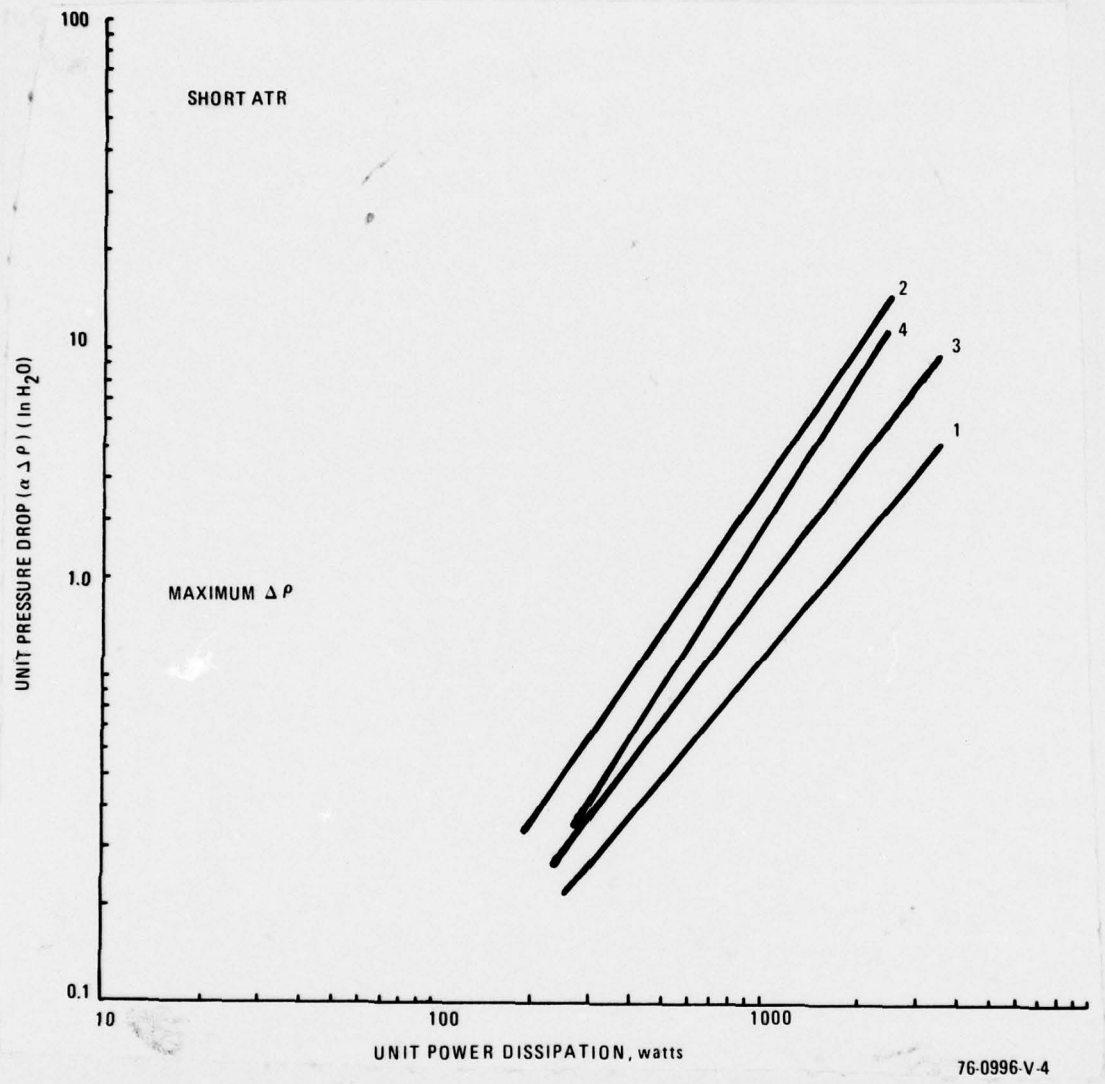
SEM low power design flow characteristics at a flow rate of 2.4 lb/min/kw and an inlet temperature of 62°F for various fin configurations (19.5" x 6.5" heat exchanger)



Fin Configurations:
1 - .330 High straight fins, 15 fins/inch
2 - .375 High lanced, offset fins, 14 fins/inch
3 - .353 High double layer of lanced, offset fins 12 fins/inch
4 - .375 High wavy fins, 12 fins/inch

Figure 15. Power Dissipation vs Pressure Drop (Long ATR)

SEM low power design flow characteristics at a flow rate of 2.4 lb/min/kw and an inlet temperature of 62°F for various fin configurations (12.5" x 6.5" heat exchanger)



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3 - .353 High double layer of lanced, offset fins, 12 fins/inch
4 - .375 High wavy fins, 12 fins/inch

Figure 16. Power Dissipation vs Pressure Drop (Short ATR)

The junction temperature T_J of an active component mounted on a PC board in the low power configuration is determined by the following equation:

$$T_J = T_{air} + \Delta T_{fins-air} + \Delta T_{\substack{HE-overlay \\ interface}} + \Delta T_{overlay} + \Delta T_{\substack{overlay-comp \\ interface}} + \Delta T_{JC} \quad (3)$$

where: T_J - component junction temperature

T_{air} - air temperature

$\Delta T_{fins-air}$ - temperature difference between the heat exchanger fins and the air

$\Delta T_{\substack{HE-overlay \\ interface}}$ - temperature difference across the interface between the heat exchanger wall and the PC board thermal overlay

$\Delta T_{overlay}$ - temperature difference between the end and the center of the thermal overlay

$\Delta T_{\substack{overlay-comp \\ interface}}$ - temperature difference between the overlay and the case of the component

ΔT_{JC} - temperature difference between the junction and the case of the component

The air temperature, T_{air}, used in the analysis was based on the inlet and outlet air temperature of 17°C and 71°C respectively. Since a uniform power distribution was assumed from PC board to PC board in the chassis, the average air temperature was reached at the mid-point of the heat exchanger as illustrated in figure 17. In an actual situation, however, the temperature profile in the heat exchanger would follow the curve for a nonuniform power distribution. This would occur because the PC boards dissipating the most power would be closest to the inlet to take advantage of the lower air temperature. Similarly, the lowest power dissipating PC boards would be near the outlet in an attempt to equalize the maximum

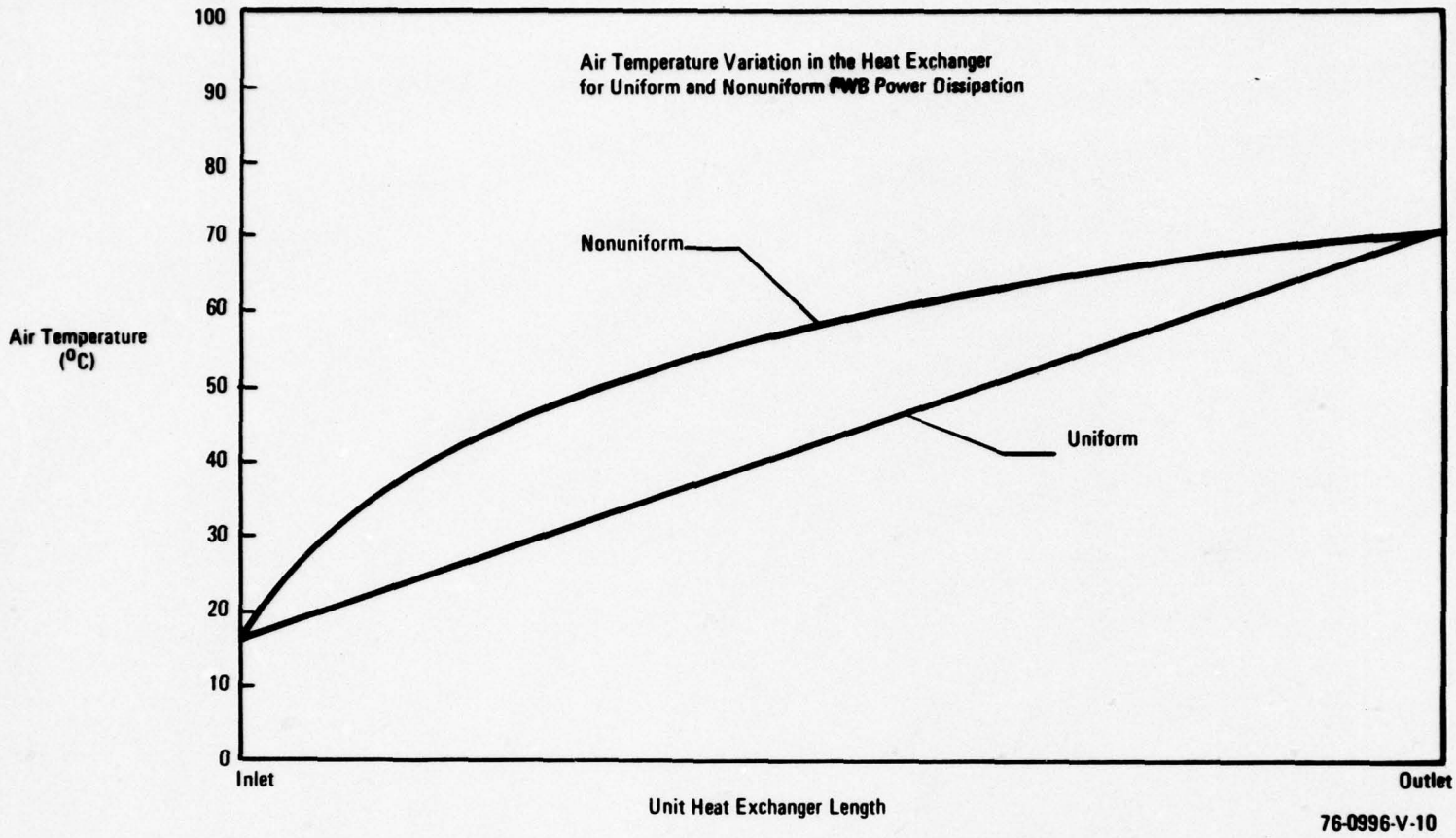

Figure 17. Temperature Variations in Heat Exchangers

component junction temperatures on all PC boards in a particular unit. The only difference between the two cases, uniform and nonuniform PC board power dissipation, is the location along the heat exchanger where the average air temperature occurs.

The temperature difference between the heat exchanger fins and the air temperature is governed by the equation:

$$\Delta T_{fins\text{-}amb} = Q/hA \qquad (4)$$

where: Q = power dissipation

h = heat transfer coefficient

A = fin surface area

As can be seen from the equation, $\Delta T_{fin\text{-}air}$ is inversely proportional to the product of hA. The heat transfer coefficient, h, is dependent upon the air properties and the fin geometry whereas the fin surface area is dependent upon the number and size of the fins. This temperature difference, as mentioned previously, was limited to a maximum of 10°C. This was done to insure an effective heat exchanger design to limit this portion of the available temperature difference to a reasonable value.

The next temperature difference in equation 3 is between the heat exchanger wall and the PC board thermal overlay. This temperature difference, $\Delta T_{HE\text{-}overlay\ interface}$, is a function of the thermal contact resistance at this interface. Based on published data[2] as well as internal experimental work, the contact resistance at this interface was determined to be 0.5 °C-in^2/watt. Since the area in contact at each end of the thermal overlay was 0.225" x 4.80", the thermal resistance at each interface was 0.46 °C/w.

The temperature difference between the edges of the thermal overlay and the center, $\Delta T_{overlay}$, is the one value that can be varied significantly.

2. General Electric Co., General Electric Heat Transfer Data Book, Schenectady, New York, 1970.

Since this temperature difference is governed by the incremental equation for conduction heat transfer,

$$\Delta T = Qt/KA \qquad (5)$$

where: Q = power dissipation

t = distance through which heat is being transferred

K = thermal conductivity of the material

A = cross sectional area

it is evident that the only parameters which are variable are t and K, since the value of A is already maximized. As a consequence, reduction in the overlay gradient can be accomplished by using a material with a high conductivity such as aluminum or copper or by changing the distance the heat must be transferred. The latter can be done in two manners. First, the size of the chassis can be reduced to the 3/4 or 1/2 ATR sizes. Secondly, a heat pipe which is dependent only on the thermal resistance at the condenser and evaporation ends can be utilized to effectively reduce this distance. The heat pipe is most advantageous for large PC board sizes because its thermal resistance is much lower than a metal overlay of the same distance. However, as the size of the PC board decreases, the temperature gradient in a metal overlay approaches that of a heat pipe. A comparison of the thermal resistance in the overlays and the heat pipe for three ATR case sizes are shown in table 3.

TABLE 3

OVERLAY THERMAL RESISTANCE (°C/w)

ATR Case Size	Overlay Type		
	Al	Cu	Heat Pipe
Full ATR	3.7	2.2	.10
3/4 ATR	2.8	1.6	.10
1/2 ATR	1.6	1.0	.10

The next temperature difference of equation 3 is between the overlay and the case of the active component. The thermal resistance at this interface is dependent on the type of component that is being mounted on the PC board. For a dual-in-line package (DIP), a flat pack, and a hybrid SEM, only one layer of filler material is present between the overlay surface and the component case. In this analysis, a 0.010" thick layer of Ablethern 12-1 with a thermal conductivity of 0.83 Btu/hr. ft. °F was assumed.

For a DIP SEM a series of materials must be present to provide a path for the heat to be transferred from the component case to the overlay. The materials are shown in figure 18. Heat is transferred through, in succession, a layer of thermal filler (12-1), an aluminum spacer, a film adhesive, plated through holes, another layer of thermal filler, and finally into the overlay. The flat pack SEM also presents a series of materials to resist the transfer of heat from the component to the thermal overlay. The materials for this configuration are shown in figure 19. In this case, heat is transferred through a layer of film

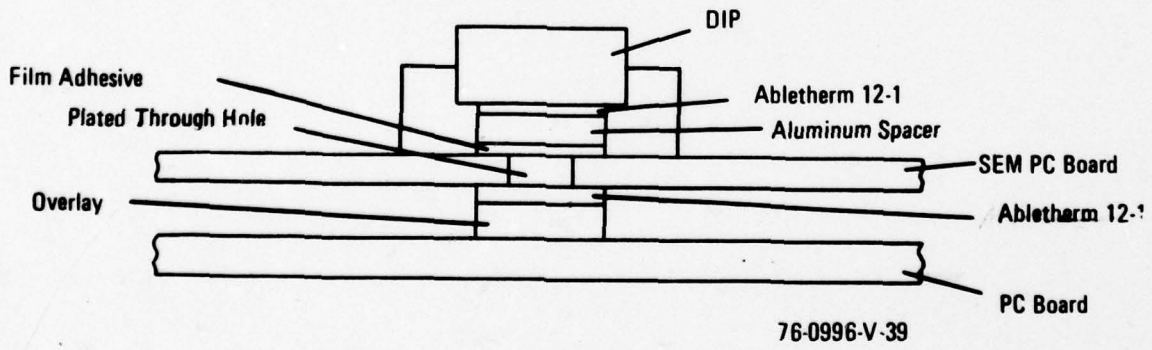

Figure 18. Interface Materials for DIP SEM

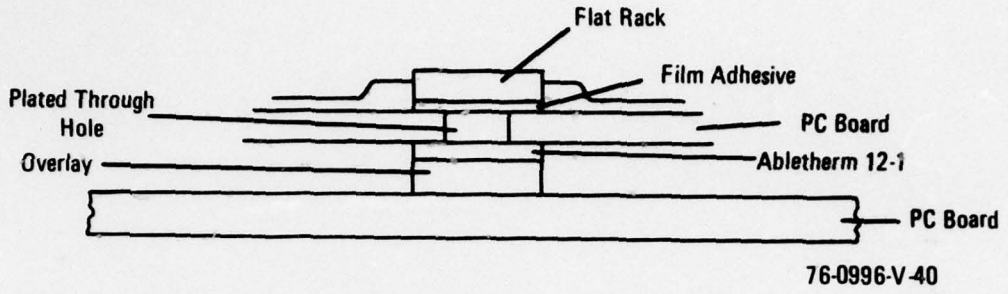

Figure 19. Interface Materials for F. P. SEM

adhesive, plated through holes, a layer of thermal filler (12-1), and into the overlay.

The final ΔT of equation 3 is the temperature difference between the junction and the case of the active device. The equation governing this quantity is the following:

$$\Delta T = P_{comp} \; R_{JC} \tag{6}$$

where: P_{comp} = power dissipation of the component

R_{JC} = junction to case thermal resistance.

The thermal resistances used in this analysis for the three basic components, the DIP, the flat pack, and the hybrid package, are 30 °C/w, 45 °C/w, and 17 °C/w per chip respectively. The thermal resistance is defined on a "per chip" basis.

Based on the nature of the constituents of equation 3, it is possible to divide the terms on the right hand side into three categories. The first category contains fixed values and include T_{amb} and $\Delta T_{fins\text{-}amb}$.

The second category includes $\Delta T_{\text{HE-overlay interface}}$ and $\Delta T_{\text{overlay}}$, the terms which are determined by the power dissipation of the PC board. The third category includes the terms which are determined by the power dissipation of the individual components. To simplify the discussion, the last two categories will be defined as the temperature difference at the PC board and the temperature difference at the component. The thermal resistances required to calculate these values as incorporated in the analysis are shown in tables 4 and 5.

TABLE 4

OVERLAY TO HEAT EXCHANGER THERMAL RESISTANCES (°C/W)
($R_{\text{PC BOARD}}$)

ATR Case Size	Overlay Type		
	Al	Cu	Heat Pipe
Full ATR	4.2	2.6	0.32
3/4 ATR	3.3	2.1	0.32
1/2 ATR	2.1	1.4	0.32

TABLE 5

COMPONENT JUNCTION TO OVERLAY THERMAL RESISTANCES ($R_{COMPONENT}$)

SEM Type	Thermal Resistance (°C/W)
DIP	34
Flat Pack	53
DIP SEM	38
Flat Pack SEM	57
Hybrid SEM	21

For SEM types described in table 5, Equation 3 was applied to determine the maximum power dissipation per PC board and per component at a maximum component junction temperature of 125°C for each ATR size, each overlay type, and each of three significant ambient temperatures. The results of this analysis are shown in tables 6 through 10. At the left hand side of the tables are the number of individual components of each particular type that can be accommodated on the PC boards of the three ATR sizes. For example, in table 6 the number of DIP's that can be accommodated by the full, 3/4, and 1/2 ATR PC boards are 96, 60, and 36. The number of components are not in the same ratio as the case size primarily due to the space required for conduction to the wall of the heat exchanger. The three ambient temperatures are also shown on the table with the corresponding power dissipation figures for a maximum component junction temperature of 125°C at each location along the heat exchanger. The data shows that the PC board nearest the inlet can dissipate the most power and the one nearest the outlet the least. Another comparison that can be made is the amount of power the three types of thermal overlays can accommodate. It is apparent that the order of increasing power dissipating capability in all cases is first-aluminum, second - copper, and third - heat pipe. For example, with a full ATR PC Board with DIP's (table 6), the power dissipation to maintain a maximum of 125°C at the hottest component junction with aluminum, copper, and heat pipes are 17.5, 26, and 65 watts respectively. At the

TABLE 6

POWER DISSIPATION CAPABILITY FOR DIP BOARD

T_j = 125°C		Air Temp (°C)	Power (Watts) Aluminum		Copper		Heat Pipe	
			Bd	Comp	Bd	Comp	Bd	Comp
n = 96	Full Bd	71	17.5	0.18	26	0.27	65	0.68
		44	29	0.30	43	0.45	-	-
		17	40	0.42	59	0.61	-	-
n = 60	3/4	71	20	0.33	27	0.45	48	0.80
		44	32	0.53	45	0.75	-	-
		17	45	0.75	61	1.02	-	-
n = 36	1/2	71	22	0.61	26	0.72	34	0.94
		44	35	0.97	43	1.19	53	1.47
		17	49	1.36	59	1.64	-	-

n = No. of DIP's

TABLE 7

POWER DISSIPATION CAPABILITY FOR FLAT PACK BOARD

T_j = 125°C		Air Temp (°C)	Power (Watts) Aluminum		Copper		Heat Pipe	
			Bd	Comp	Bd	Comp	Bd	Comp
n = 102	Full Bd	71	16.5	0.16	24	0.24	52	0.51
		44	27	0.26	39.5	0.39	-	-
		17	36	0.35	54	0.53	-	-
n = 68	3/4 Bd	71	18	0.26	24	0.35	39	0.57
		44	29	0.43	39	0.57	62	0.91
		17	40	0.59	53.5	0.79	-	-
n = 38	1/2 Bd	71	18	0.47	20.5	0.54	26	0.68
		44	29	0.76	33.5	0.88	41	1.08
		17	40	1.05	45.5	1.20	-	-

n = No. of Flat Packs

TABLE 8

POWER DISSIPATION CAPABILITY FOR DIP SEM BOARD

T_j = 125°C		Air Temp (°C)	Power (Watts) Aluminum		Copper		Heat Pipe	
			Bd	Comp	Bd	Comp	Bd	Comp
n = 72	Full Bd	71	16.5	0.23	24	0.33	52	0.72
		44	27	0.37	38.5	0.53	-	-
		17	37	0.51	53	0.74	-	-
n = 48	3/4 Bd	71	18	0.37	24	0.50	37.5	0.78
		44	29	0.60	39	0.81	-	-
		17	40.5	0.84	54	1.12	-	-
n = 27	1/2 Bd	71	17.5	0.65	21	0.78	25	0.93
		44	28.5	1.06	34	1.26	40	1.48
		17	39.5	1.46	47	1.74	54.5	2.02

n = No. of DIPs

TABLE 9

POWER DISSIPATION CAPABILITY FOR FLAT PACK SEM BOARD

T_j = 125°C		Air Temp (°C)	Power (Watts) Aluminum		Copper		Heat Pipe	
			Bd	Comp	Bd	Comp	Bd	Comp
n = 84	Full Bd	71	15.5	0.18	22	0.26	42.5	0.51
		44	25	0.29	36	0.43	-	-
		17	35	0.41	49.5	0.59	-	-
n = 56	3/4 Bd	71	17	0.30	21.5	0.38	31.5	0.56
		44	27	0.48	34.5	0.62	51	0.91
		17	37	0.66	48	0.86	-	-
n = 31	1/2 Bd	71	15	0.48	17	0.55	19.5	0.63
		44	24.5	0.79	28	0.90	32	1.03
		17	34	1.10	38.5	1.24	43.5	1.40

n = No. of Flat Packs

TABLE 10

POWER DISSIPATION CAPABILITY FOR HYBRID SEM BOARD

T_j = 125°C		Air Temp (°C)	Power (Watts) Aluminum		Copper		Heat Pipe	
			Bd	Comp	Bd	Comp	Bd	Comp
n = 200	Full Bd	71	20	0.10	31	0.16	> 60	-
		44	32	0.16	51	0.26	-	-
		17	44.5	0.22	-	-	-	-
n = 132	3/4 Bd	71	25	0.19	38	0.29	> 60	-
		44	40.5	0.31	61	0.46	-	-
		17	55.5	0.42	-	-	-	-
n = 70	1/2 Bd	71	33.5	0.48	46.5	0.66	> 60	-
		44	54	0.77	-	-	-	-
		17	-	-	-	-	-	-

n = No. of integrated circuit chips

locations under the heat pipe heading where values are missing, the power dissipation was beyond the plotted data.

An additional trend can be observed by comparing the magnitude of the power figures of the five tables. In general, the hybrid SEM's allow the highest power dissipation per PC board. The primary reason for this is the low thermal resistance of the hybrid package. The SEM type which can dissipate the least amount of power is the flat pack SEM. Again this is a direct reflection of the data in table 5. When the component power dissipation is compared, a reverse trend is noted. It can easily be explained, however, when the number of active components on a PC board are observed. The hybrid SEM, which has an extremely high component density, dissipates the least amount of power per device. A tabular presentation of these trends at the average ambient air temperature is shown in table 11, and a graphic representation of the component power dissipation of that table is illustrated

TABLE 11

POWER DISSIPATION CAPABILITY FOR VARIOUS PACKAGING CONCEPTS
AT THE AVERAGE AMBIENT AIR TEMPERATURE (Aluminum Overlay)

	No. Devices	Board Size	Board Power	Component Power
Discrete DIP's	96	Full ATR	29 watts	0.30 watts
Discrete DIP's	60	3/4 ATR	32	0.53
Discrete DIP's	36	1/2 ATR	35	0.97
Discrete Flat Packs	102	Full ATR	27	0.26
Discrete Flat Packs	68	3/4 ATR	29	0.43
Discrete Flat Packs	38	1/2 ATR	29	0.76
DIP/SEM's	72	Full ATR	27	0.37
DIP/SEM's	48	3/4 ATR	29	0.60
DIP/SEM's	27	1/2 ATR	28.5	0.59
Flat Pack/SEM's	84	Full ATR	25	0.29
Flat Pack/SEM's	56	3/4 ATR	27	0.48
Flat Pack/SEM's	31	1/2 ATR	24.5	0.79
Hybrid/SEM's	200	Full ATR	32	0.16
Hybrid/SEM's	132	3/4 ATR	40.5	0.31
Hybrid/SEM's	70	1/2 ATR	54	0.77

in figure 20. It should be noted that the extremely high power dissipations for individual components on the small PC board sizes may not be feasible.

An unusual trend can be observed by comparing the power dissipation capability between PC board sizes for a particular type of overlay. The first place this trend occurs is for the copper overlay in table 6. For example, at an air temperature of 71°C at the heat exchanger outlet, the full ATR PC board can dissipate 26 watts while maintaining the maximum junction temperature at 125°C. For the same conditions, the 3/4 ATR PC board can dissipate 27 watts, an increase of one watt. The reverse trend occurs when the dissipation capability of the 1/2 ATR PC board is observed. For the same conditions, the power limit decreases back to 26 watts. This same trend occurs in several places in the tables and can be explained by studying the terms of Equation 3. The trend results from the dependency of T_J on the sum of the temperature differences at the PC board and at the component level. As the PC board size decreases, the temperature difference from the center to the end of the overlay decreases. On the other hand, since the number of components is decreasing, and the power per component is increasing, the temperature difference from the component junction to the overlay is increasing significantly. Consequently, as the number of components decreases the temperature difference at the component level increases at a faster rate than the temperature difference at the PC board level decreases. This behavier is illustrated for the DIP components in figure 21 along with the summation of these two curves. In addition, this resultant curve was calculated for the DIP components using a copper overlay and a heat pipe overlay as illustrated in figure 22. It can be readily seen that for the aluminum and copper overlays at PC board sizes of the 1/2, 3/4, and full ATR cases, a minimum in the curve of the temperature difference from the junction to the air in the heat exchange is obtained. The same general trend occurs for the heat pipe overlay, however, in this case the $\Delta T_{J\text{-air}}$ decreases asymptotically to a minimum at PC board lengths far beyond reasonable sizes.

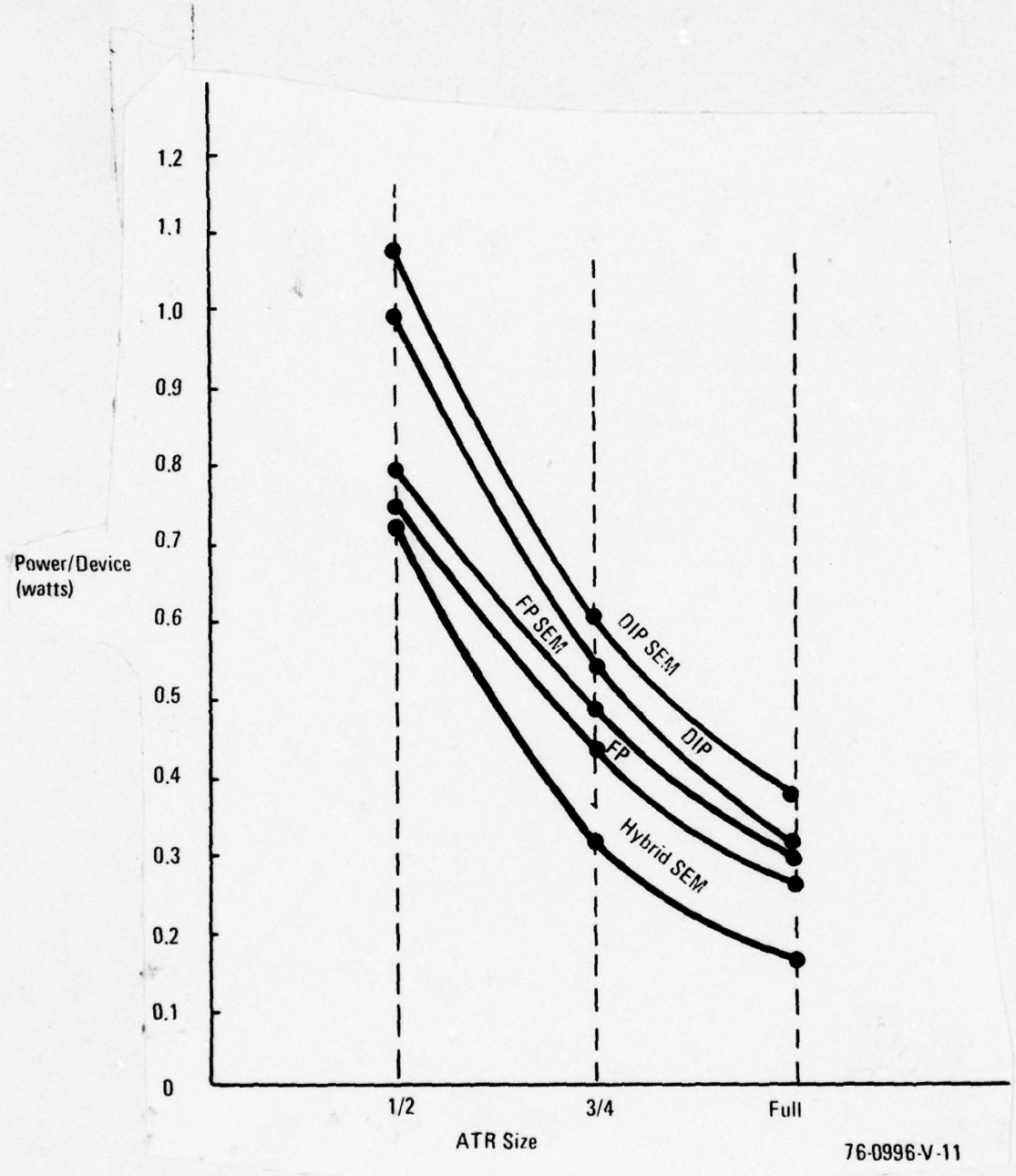

Figure 20. Power Dissipation vs Device Configuration at the Average Ambient Air Temperature Aluminum Overlay

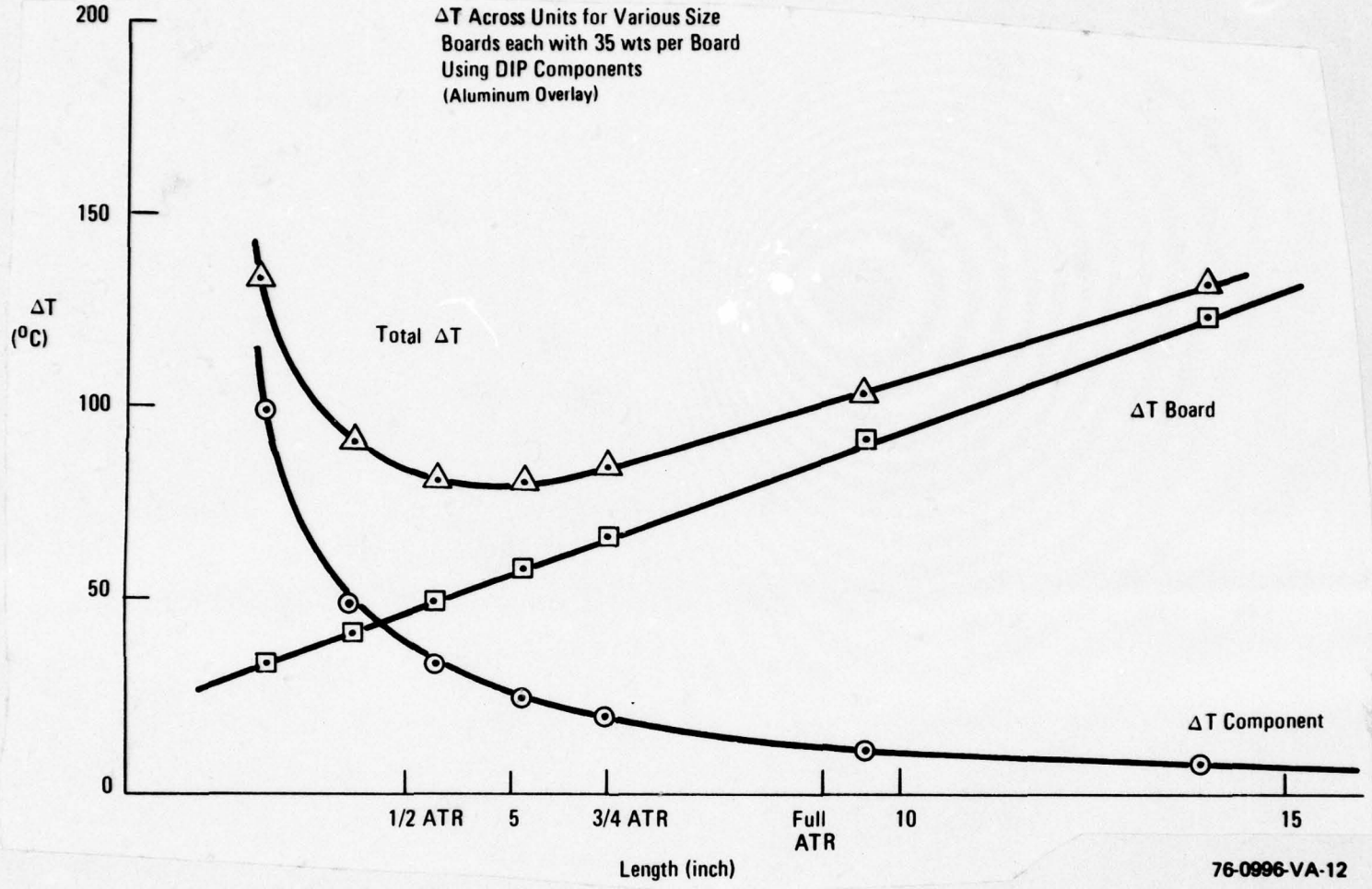

Figure 21. Δt vs Card Length

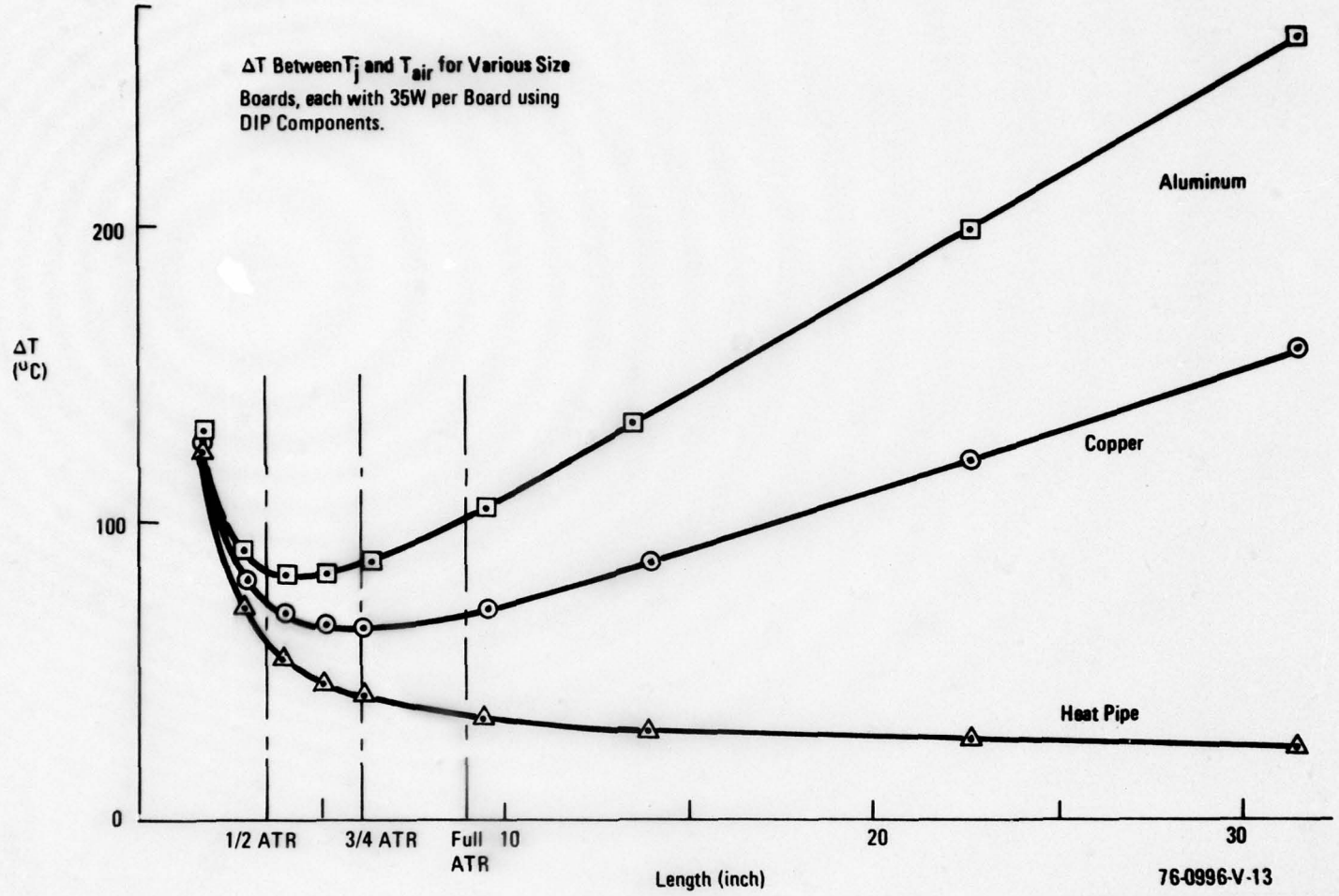

Figure 22. Δt vs Card Length (various Thermal Overlays)

The final and most important feature to be observed in the tables of results is the order of magnitude of the power dissipation capabilities of the various PC Board sizes and overlay types. These values can be compared to the power dissipation capability based on the pressure drop. With 1.5 inches of H_2O pressure drop as the limiting factor, the maximum power dissipation for both the long and short ATR cases was approximately 900 watts. By assuming 0.5 inch PC board spacing, the average power dissipation per PC board for the long and short ATR cases was approximately 23 watts and 36 watts respectively. Comparison of these values with the average power dissipation capabilities of tables 7 through 10 points out that in all cases, pressure drop is the limiting factor when the long ATR case is used. It can also be noted that power dissipation capability generally is a limiting factor only when aluminum overlays are utilized in the short ATR case.

2.1.3.4 High Power Configuration

The high power configuration, as illustrated in figure 23, consists of a chassis with inlet and outlet plenums in the side walls and PC board pairs with each pair having its own integral heat exchanger. This configuration eliminates the need for a conductive overlay to transfer heat to a heat exchanger; and as a consequence, has a lower thermal resistance between the component junction and the air. Since a relatively large plenum is required in the side walls to limit pressure drop at that location and to provide a uniform air distribution system, the size of the PC board that can be used is smaller than for the low power configuration. The PC board sizes for the full and 3/4 ATR case are 8.0 x 4.5 and 5.5 x 4.5. The smaller dimension being perpendicular to the direction of air flow through the finned exchanges.

The fin material used in this configuration is 0.10 inch high, lanced fins with a 0.125 inch offset and a fin density of 16 fins per inch. The PC board pair pressure drop as a function of board pair power dissipation for these fins is shown in figure 24. The only two case sizes illustrated are the full ATR and 3/4 ATR because the PC board size for the1/2 ATR would be impractical. The environmental conditions are again the same as for the

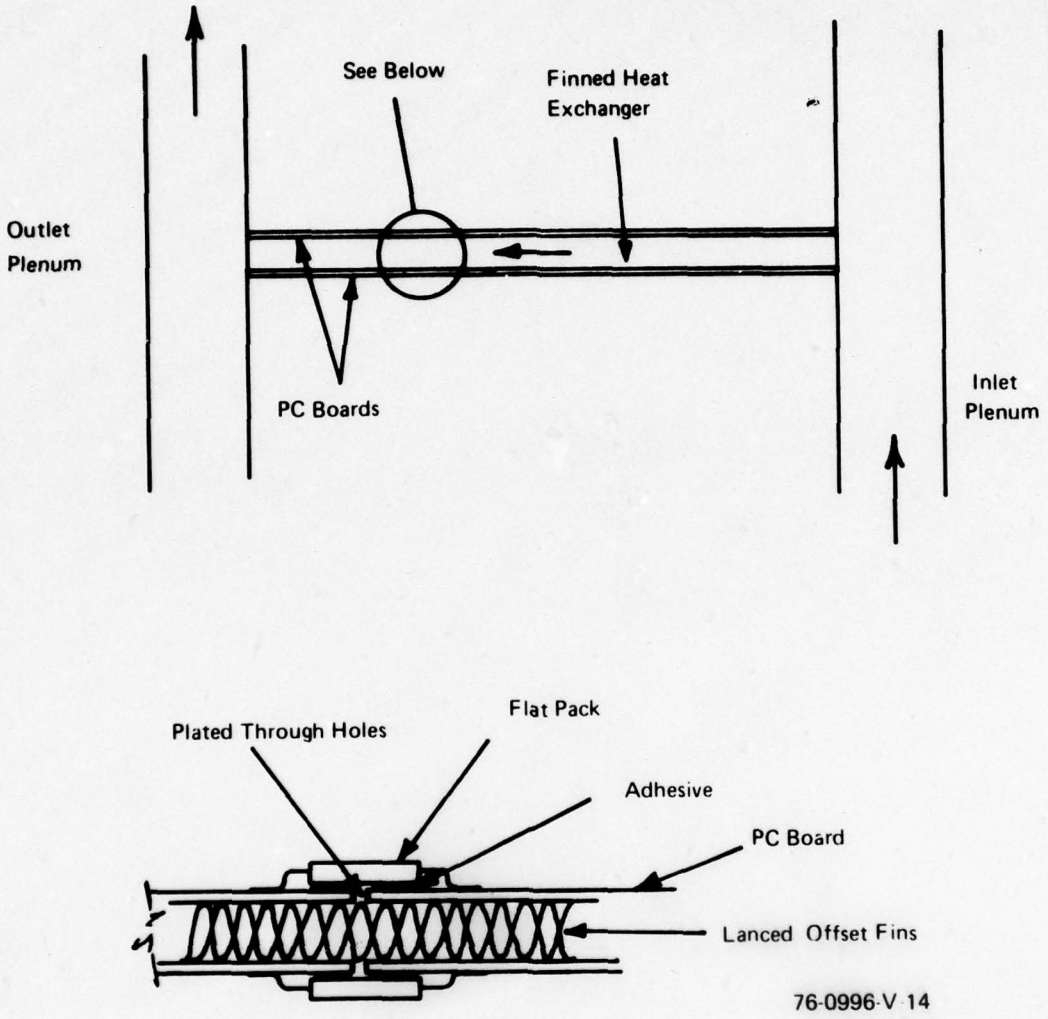

Figure 23. High Power Configuration

SEM High Power Air Flow Characteristics at a flow rate of 2.4 lb/min/kw and an inlet temperature of 62° F for a PWB pair with an integral heat exchanger (4.5" wide x .10" thick) (16 fins/inch, .125" offset on strip fins).

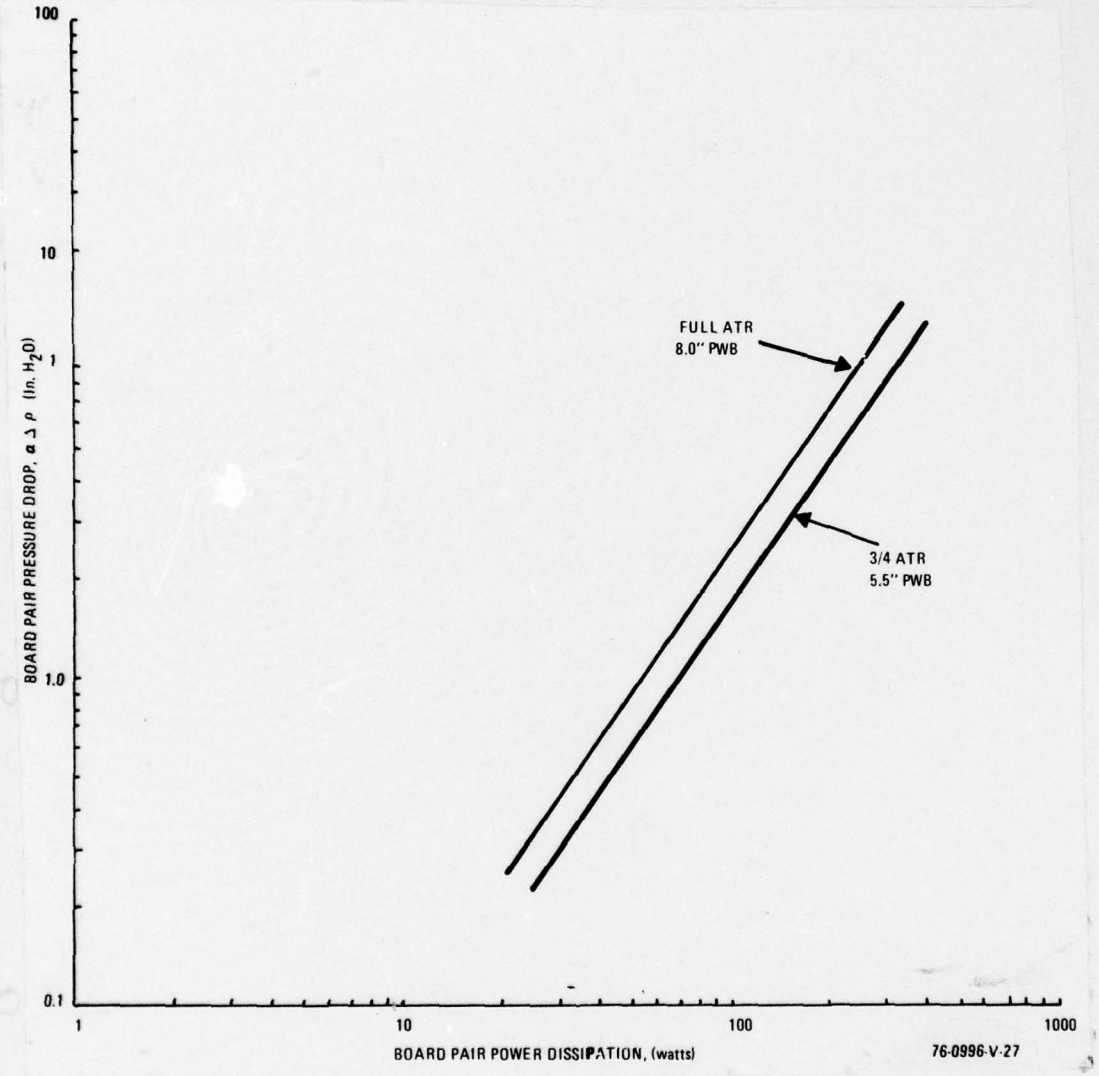

Figure 24. SEM High Power Air Flow Characteristics

low power configuration analysis with the air flow rate being 2.4 lbs/min-kw at an inlet temperature of 62°F (16.7°C).

Since the allowable pressure drop for the unit is 1.5 inches of H_2O, the pressure drop allotment for the finned heat exchangers is only 1.0 inch of H_2O. The remaining 0.5 inches of H_2O must be allotted to the inlet and outlet plenums. By observing the results presented in figure 24, it becomes apparent that at a pressure drop of 1.0 inch of H_2O, the PC board pairs of the full ATR and 3/4 ATR cases can dissipate 52 and 70 watts respectively. As a consequence, each PC board can dissipate only 26 watts and 35 watts respectively. Since this power dissipation is approximately the same as for the low power design, it appears that this design is practical only if the available pressure drop is somewhat higher than 1.0 inch of H_2O.

The second consideration in the analysis of the high power design is the power dissipation capability. For this design, it is necessary to analyze only one type of component, the flat pack. The reason for this limitation is that the components mounted on the PC boards in this configuration cannot have leads protruding into the heat exchanger.

The equation governing the junction temperature for the flat pack is the following:

$$T_J = T_{air} + \Delta T_{FINS-AIR} + \Delta T_{PCB-FINS} + \Delta T_{PTH} + \Delta T_{INTERFACE} + \Delta T_{JC} \quad (7)$$

where:

T_{air} = air temperature

$\Delta T_{FINS-AIR}$ = temperature difference between the heat exchanger fins and the air

$\Delta T_{PCB-FINS}$ = temperature difference at the interface between the PC board and the heat exchanger fins.

ΔT_{PTH} = temperature difference across the plated through holes

$\Delta T_{INTERFACE}$ = temperature difference across the adhesive used to bond the flat pack case to the PC board.

ΔT_{JC} = the temperature difference between the component junction and the package case.

Since this heat transfer process relies only on conduction from the component through a layer of adhesive, through a plated through hole and into the heat exchanger (see figure 11) the components act as independent sources mounted on a heat exchanger that varies in temperature from 17°C at the inlet to 71°C at the outlet. Lateral heat transfer from component to component is minimized by the epoxy glass PC board to cause this independence. In addition, it should be noted that even as the power dissipation of the PC boards increases, the heat exchanger air temperature remains constant since air is supplied according to a constant flow rate per kilowatt of power.

The $\Delta T_{FINS-AIR}$ was again held at a constant value of 10°C; thus assuming that if necessary the heat exchanger heat transfer coefficients and surface area could be altered to maintain this temperature difference. The $\Delta T_{PCB-FINS}$, ΔT_{PTH}, and $\Delta T_{INTERFACE}$ are strictly confined to conduction which is governed by equation 5. The final ΔT is governed by equation 6 when the junction-to-case thermal resistance for the flat pack is 45°C/W.

The results of the application of equation 7 to the full ATR and 3/4 ATR PC boards are shown graphically in figure 25 and 26. To maintain the junction temperature of the hottest component below 125°C, assuming a uniform distribution of power on the PC board, the components located at the outlet are considered as the critical devices. By studying the graphs, it becomes apparent that the maximum power dissipation for a single PC board for the full ATR and 3/4 ATR case sizes is 74 watts and 50 watts respectively. Since it was assumed the PC board of the full ATR configuration and the 3/4 ATR configurations were 102 and 68 respectively, the power dissipation per component is approximately 0.73 watts in each case. The power dissipation distribution on the PC boards can be varied by following the same type of procedure depicted in Figure 17 except that component rather than PC board placement would be involved. Higher dissipating components could be moved close to the inlet and lower dissipators near the outlet to preserve a maximum junction temperature of 125°C.

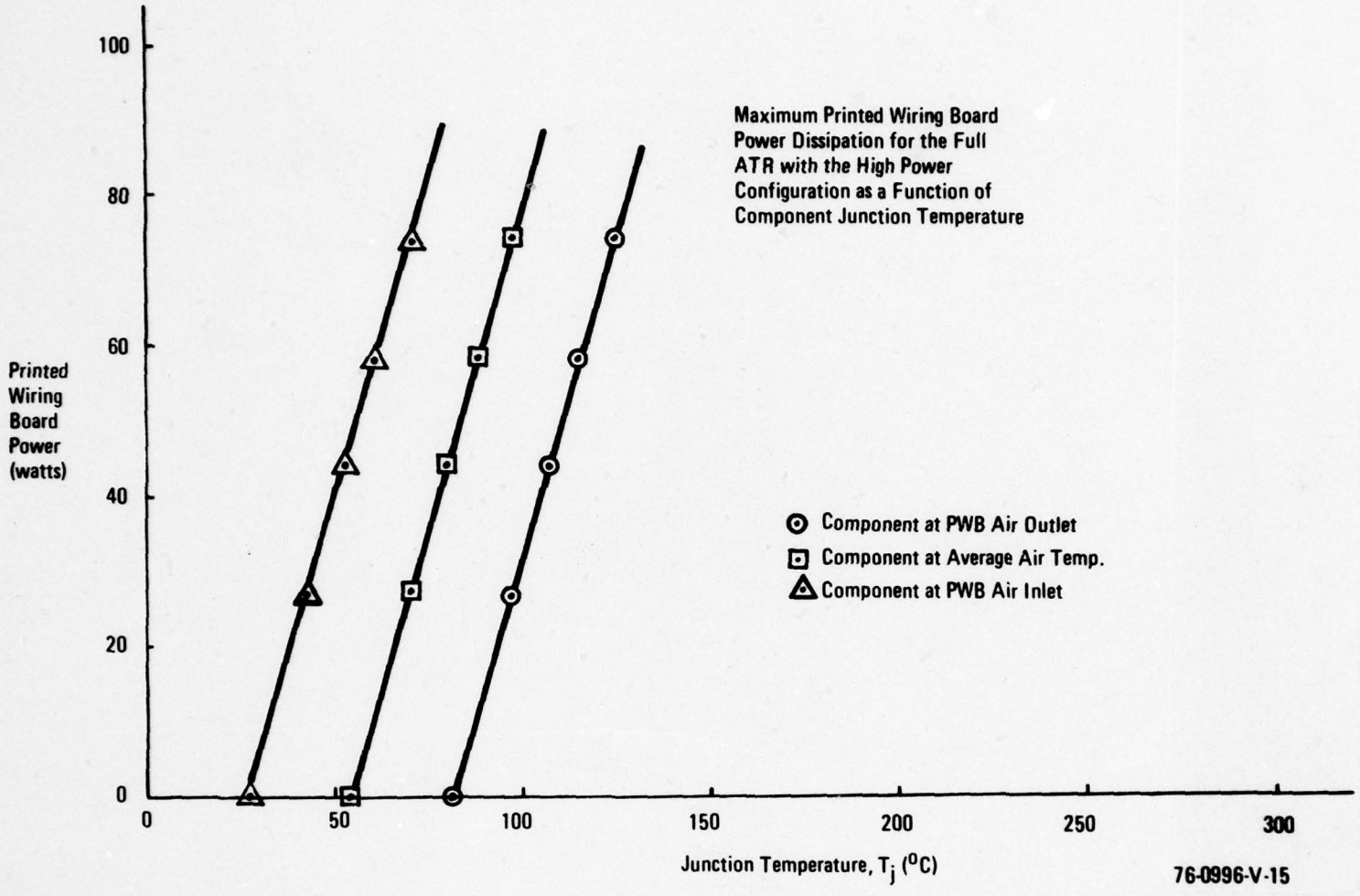

Figure 25. High Power Configuration-Full ATR

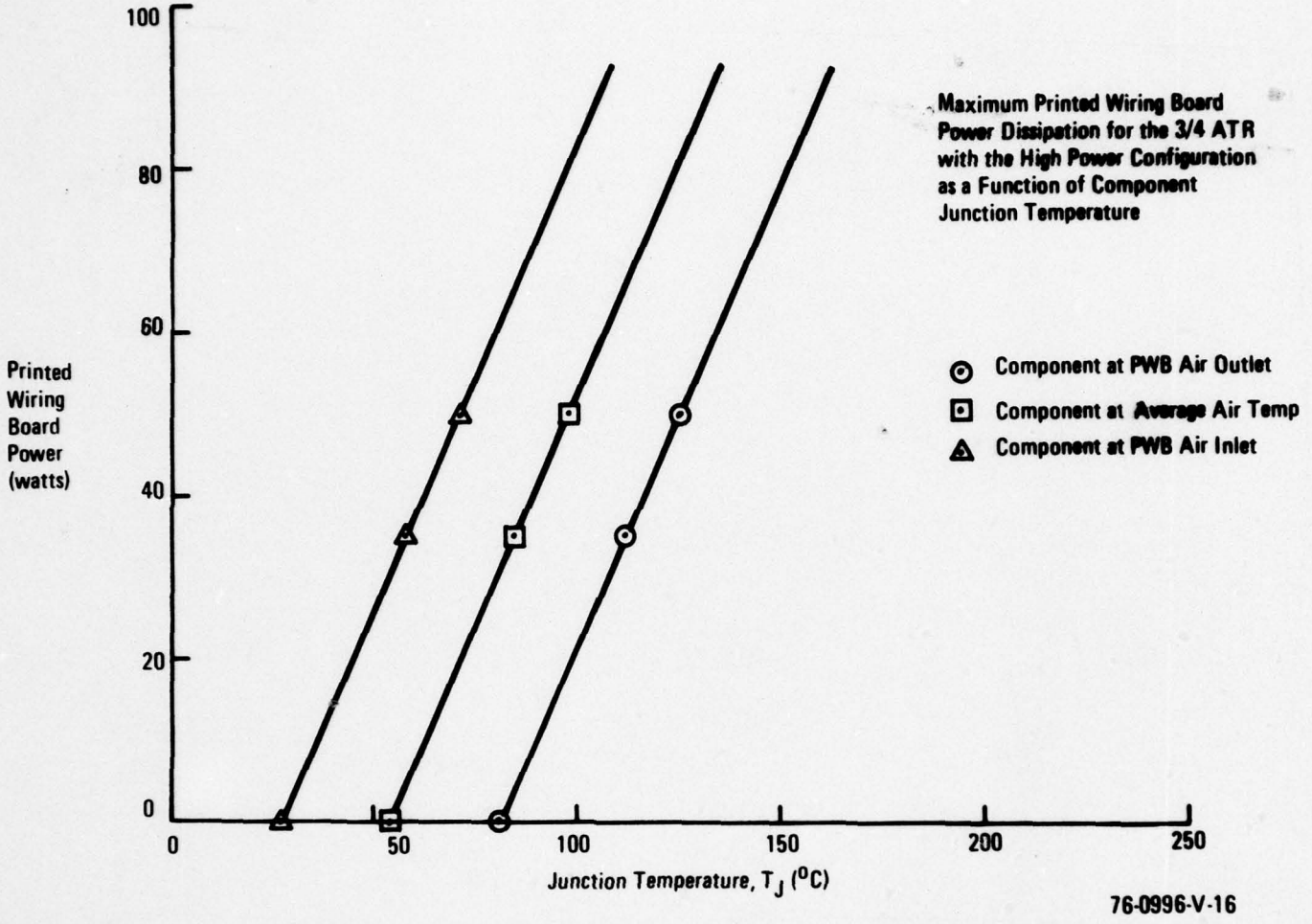

Figure 26. High Power Configuration - 3/4 ATR

As was previously mentioned, this high power design becomes practical only if the available pressure drop for the heat exchanger exceeds 1.0 inch of H_2O. To determine the magnitude of the pressure drop necessary to utilize the 74 watt full ATR PC board and the 50 watt 3/4 ATR board, it is necessary to return to figure 24. The pressure drop required for a PC board pair power dissipation of 148 watts with the full ATR case is 4.3 inches of H_2O. Similarly for a 3/4 ATR PC board pair power dissipation of 100 watts, the required heat exchanger pressure drop is 1.7 inches of H_2O. The greatest limitation of this design is the requirement for a high pressure head; however, if this is available, the advantages in terms of power dissipation capability are significant.

The high power design can dissipate more power than the low power design because the number of PC boards which can be accommodated in a given length of chassis is much higher. The spacing required between PC board pairs is approximately 0.5 inches, the same spacing as the single PC boards of the low power design. As a consequence, in a given chassis size, the high power technique can accommodate about twice as many PC boards as the low power technique. The result of this being that even though the power dissipation per PC board for the high power design is not much larger than the power dissipating capability of the low power heat pipe design, the former can dissipate at least twice as much power.

2.2 ELECTRICAL STUDIES

The efforts of subtask II were directed to repartitioning studies of two digital signal processors to determine the extent of commonality of circuitry within and between the systems. The value of SEM versus custom design was measured through a series of trade-off studies. Subtask III consisted of fabricating prototype electrical models that exhibit inter and intra-system commonality.

2.2.1 Repartitioning Studies

Two existing, custom-designed, radar digital signal processors were repartitioned to fit into the SEM mechanical configuration. The approach that was taken in this effort was to review the entire set of existing schematics from one LRU and try to identify functions that were used repeatedly. These functions were then used in repartitioning the second LRU. Two new SEM's were required in the second LRU and two more were modified to make them more universal. Redesign on both signal processors was held to a minimum.

Several complex functions were identified that would make good SEM candidates. The remainder of the circuitry was partitioned into SEM's of less complex functions and SEM's that are just chip holders with all pins available. Several of these less complex functions are used many times. These are similar to many of the circuits used in the Navy's SEM inventory.

A separate task was the repartitioning of the DAIS computer's I/O into functional SEM's. Again the original approach taken was to review the existing schematics to try and find functions that were used repeatedly. This approach proved less fruitful for the DAIS I/O than it did for the signal processors. There were several large functions but they were only used once. These functions were then examined to see what the limitations on other computers would be if they became SEM's. The restrictions appeared to be acceptable and might be overcome in each design with a nominal amount of custom circuitry. Therefore, these large functions were partitioned as SEM's.

Table 12 shows the data collected on the signal processors and the I/O portion of the DAIS general purpose computer.

In all three LRU's more devices were required in the SEM version than in the custom design. Table 13 shows the number of additional devices that were necessary in the SEM designs. The number of additional devices is probably higher in each case than might be required if a more significant redesign were done or if a complete family of SEM's were available prior to the design.

TABLE 12

REPARTITIONING - SEM'S USAGE

SEM ** Designation	#IC's	#Pins	Power Dissipation	# of SEM's Used Sig Proc #1	Sig Proc #2	DAIS I/O
RAR*	14	64	3.2W	14	18	
R-R*	20	54	3.9W	7	6	
M-R*	7	62	1.3W	9	8	
RMR*	21	69	9.3W	4	8	
MEM 64 9*	2	54	1.5W	13	-	
MEM 11*	8	30	800mW	15	32	
MEM 5124*	4	28	3.4W	18	1	
MEM 2561*	8	30		-	20	
HSM*	22	74	9.5W	-	2	
TSI	3	44	285mW	10	29	
INV	3	38	420mW	51	44	
TSB	3	44	975mW	13	1	
Reg 161	3	44	975mW	25	45	
Mux 157	3	44	459mW	23	32	
Reg 174	3	44	680mW	45	119	
Add 283	3	44	730mW	11	25	
Com 324	3	44	600mW	7	16	
Mux 9309	3	44	450mW	14	20	
RCV 9615	4	58	2.9W	9	8	
DRV 9614	4	58	2.9W	9	5	
FF 74	4	50	420mW	21	22	
EO 86	4	50	600mW	4	2	
PI0*	25	49	3.4W	-	-	2
DMA*	38	68	5.9W	-	-	1
PROTECT*	14	26	2.3W	-	-	1

*Functional Circuits

TABLE 12. (Continued)

SEM Designation	#IC's	#Pins	Power Dissipation	# of SEM's Used Sig Proc #1	Sig Proc #2	DAIS I/O
INTERRUPT*	29	48	3.4W	-	-	1
TIMER*	21	45	4.9W	-	-	1
138	5	46	630mW	-	-	6
7551	3	44	750mW	-	-	3
7820	3	38	1.4W	-	-	15
7832	2	30	1.2W	-	-	14
161	3	44	975mW	-	-	1

*Functional Circuits

**

RAR	Com 324
Register-Adder-Register	Comparator
R-R	Mux 9309
Register-Register	Multiplexer
M-R	RCV 9615
Multiplexer-Register	Differential Line Receiver
RMR	DRV 9615
Register-Multiplier-Register	Differential Line Driver
MEM 649	FF 74
Memory RAM	Flip Flop
MEM 11	E086
Memory RAM	Exclusive "OR"
MEM 5124	PIO
Memory PROM	Parallel I/O
MEM 2561	DMA
Memory	Direct Memory Access
HSM	PROTECT
High Speed Memory	INTERRUPT
TSI	TIMER
Tri-State Inverter	D138
INV	3 to 8 Decoders
Inverter	Reg 7551
TSB	Register
Tri-State Buffer	7820
Reg 161	Line Receiver
Register	7832
MUX	Line Driver
Multiplexer	Reg 161
Reg 174	Register
Register	
Add 283	
Adder	

TABLE 13

DEVICES REQUIRED FOR CUSTOM/SEM

	# Devices Custom Design	# Devices SEM Design	# Devices in SEM's
Signal Processor #1	1612	1977	1463
Signal Processor #2	2232	2887	2235
DAIS I/O	189	276	264

2.2.2 Electrical Model

Two of the SEMed board designs were chosen to be built as demonstration models. One board was selected from each of the digital signal processors. Figures 27 and 28 are photographs of these two boards. The schematics for the SEM's mounted on these boards are shown in figures 29 through 36. Four of the SEM's are common between the two board designs.

2.2.3 Tradeoff Studies

The value of SEM versus custom designs is measured through a series of trade-off studies. Included are weight/volume, electrical performance, reliability, acquisition cost, logistic support cost and finally life cycle cost. The studies are based on one of the digital signal processors that was repartitioned for the proposed SEM concept. Each of the three proposed SEM configurations are evaluated.

2.2.3.1 Weight/Volume

Volume is dependent on the number of printed wiring boards and the spacing of these boards. The spacing is dependent on the device height and board thickness or, in some instances, the connector is the controlling factor. The original data on this processor indicated that the custom design contained 29 boards but later information put it at 35. The subsequent data was adjusted for the later information, so that a correct comparison could be made with the custom design cost. All data is shown in table 14.

Figure 27. Electrical Model - Board #1

CUSTOMER 53979 JOB NO. 5462

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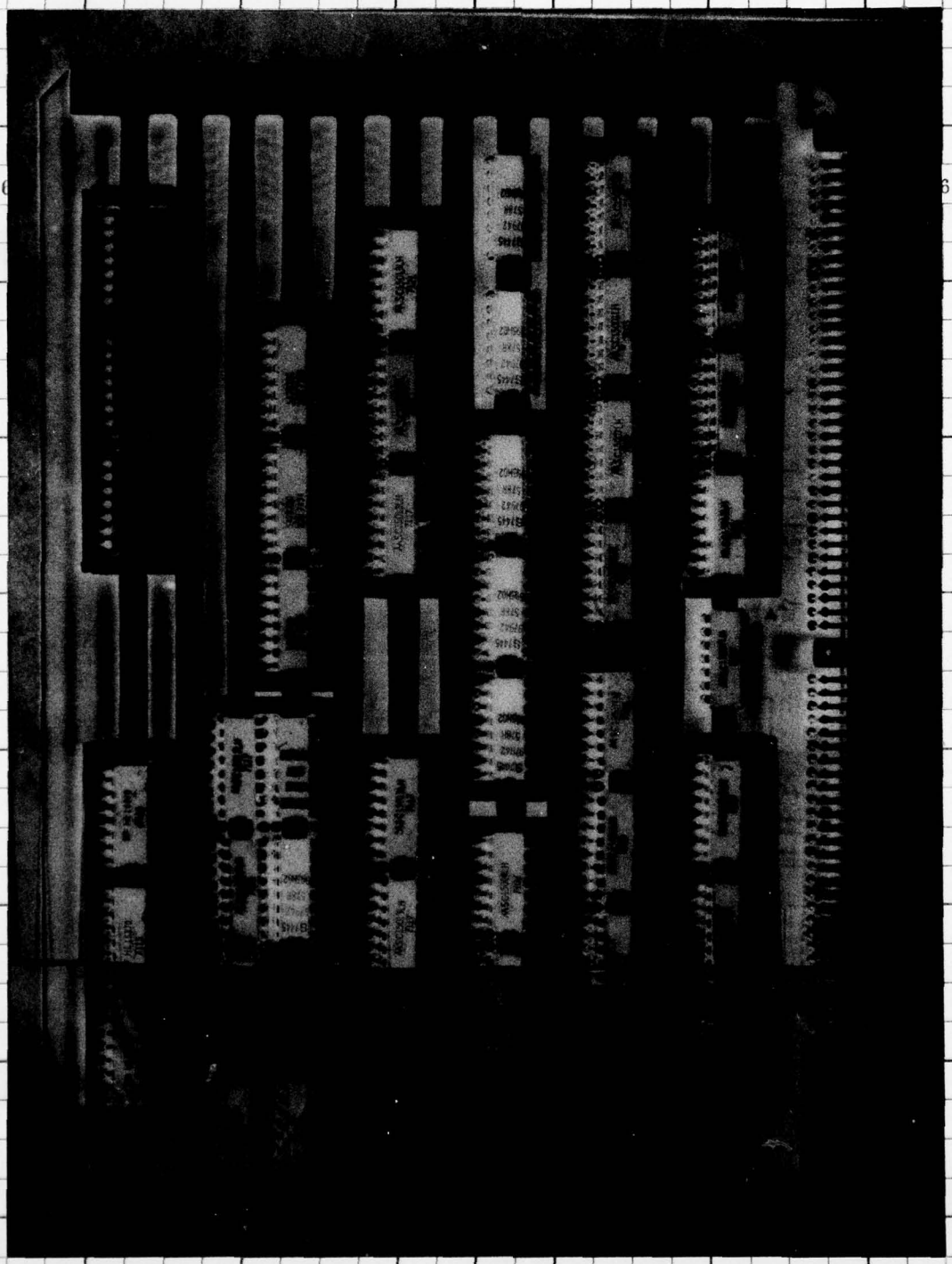

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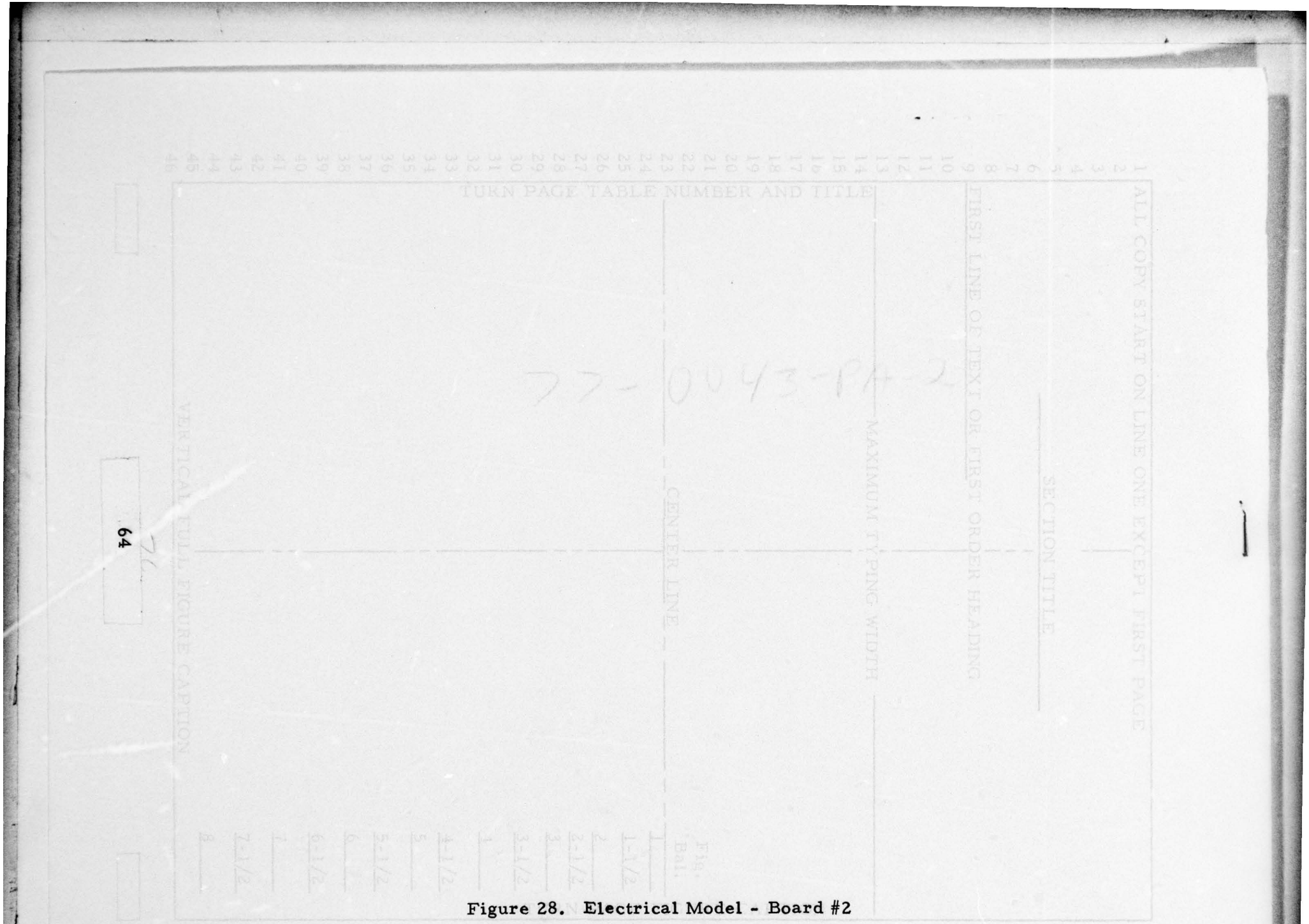

Figure 28. Electrical Model - Board #2

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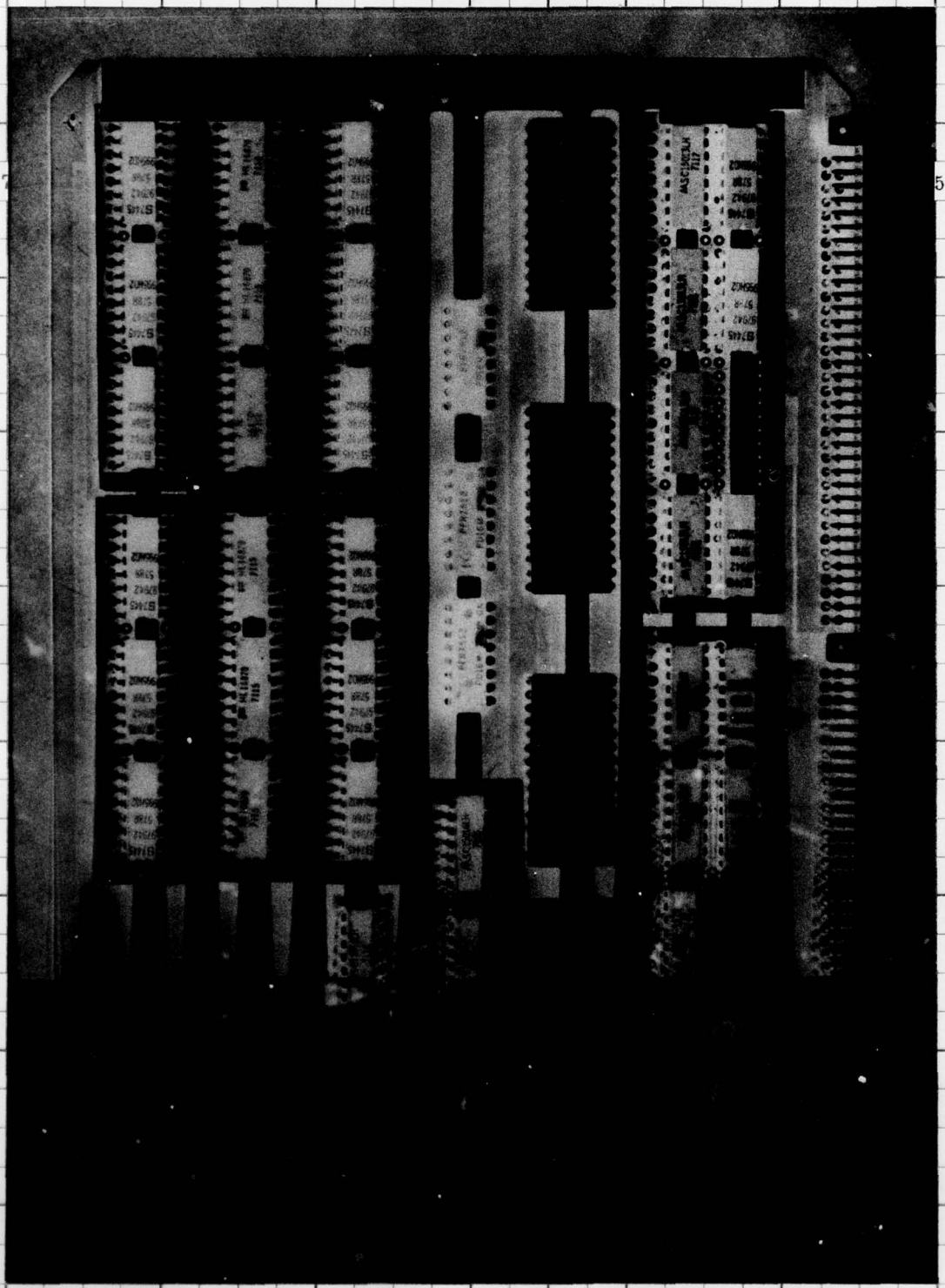

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AD-A048 205 WESTINGHOUSE ELECTRIC CORP BALTIMORE MD F/G 9/3
MODULAR PACKAGING APPROACHES.(U)
JUL 77 W W STALEY F33615-75-C-1269
UNCLASSIFIED 77-0043 AFAL-TR-76-61-VOL-2 NL

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Figure 29. SEM - EO 86

CUSTOMER 55-979 JOB NO. 5462

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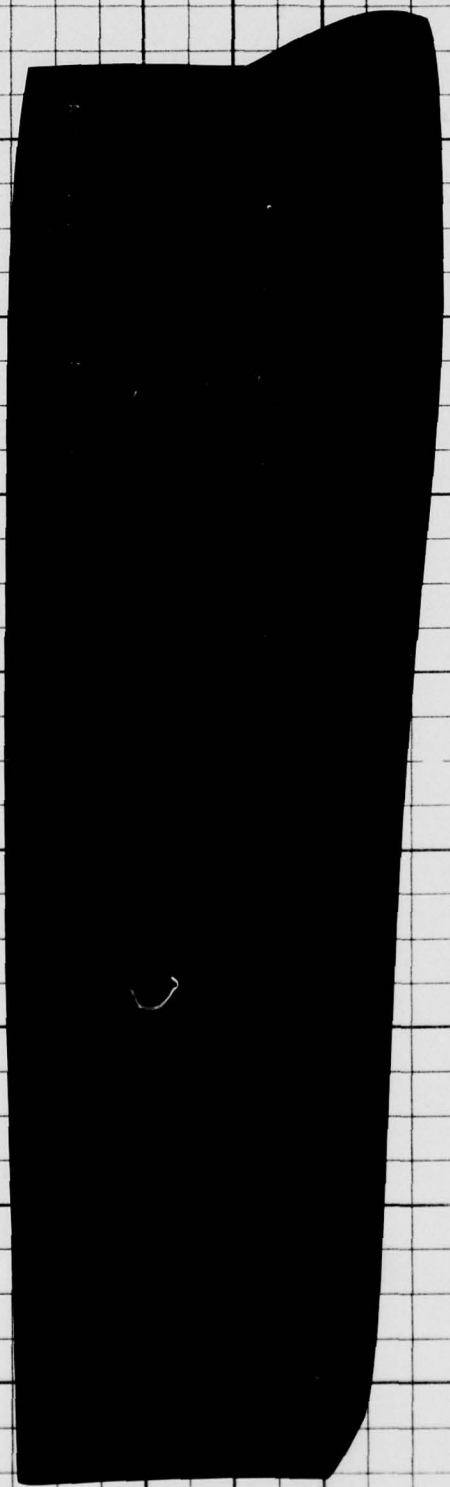

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Figure 30. SEM - COM 324

CUSTOMER 55973 JOB NO. 57582

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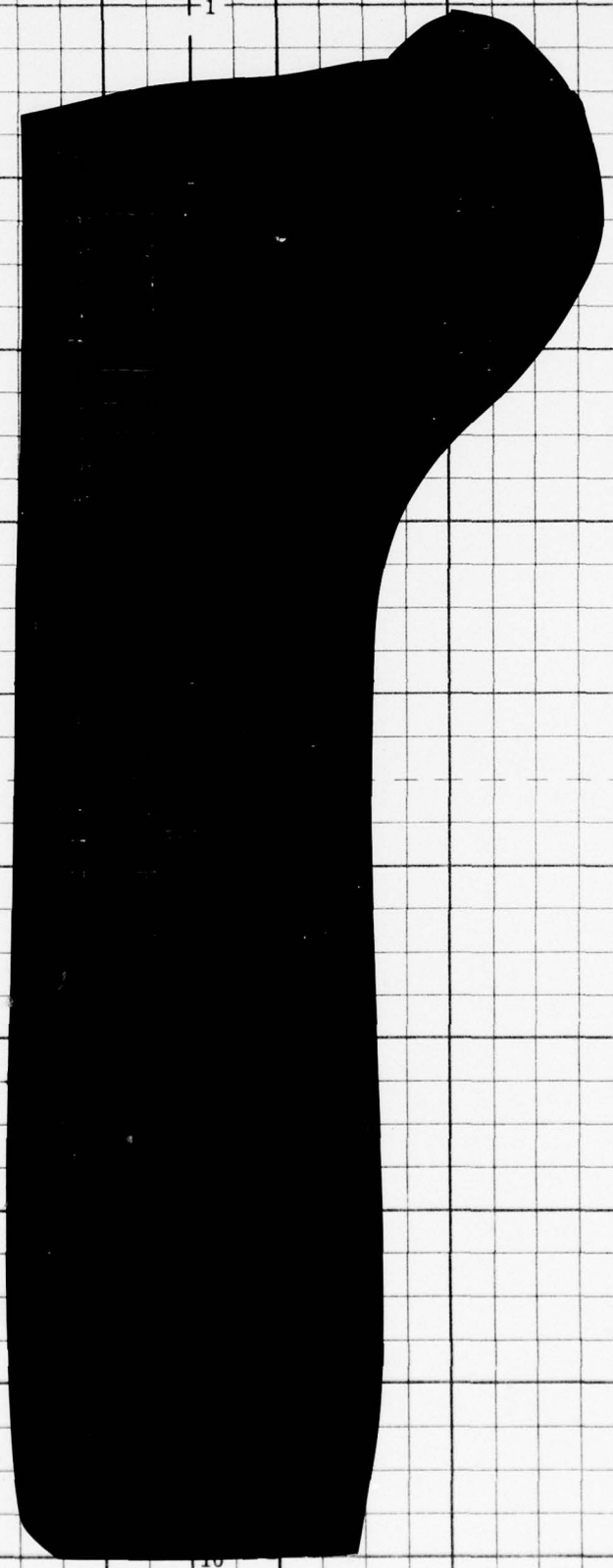

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Figure 31. SEM - Inv.

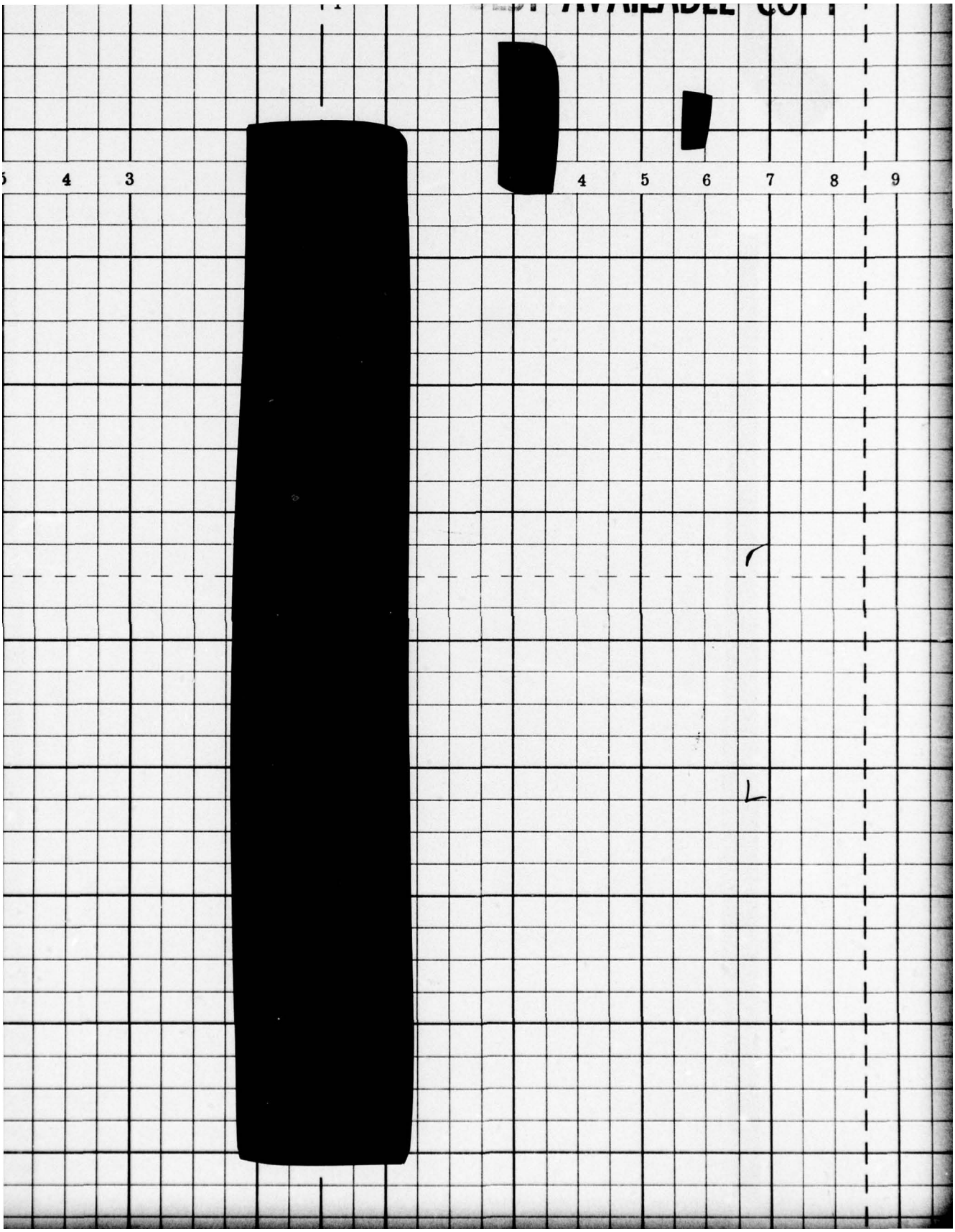

Figure 32. SEM - Reg 174

CUSTOMER 555973 JOB NO. 5456-2

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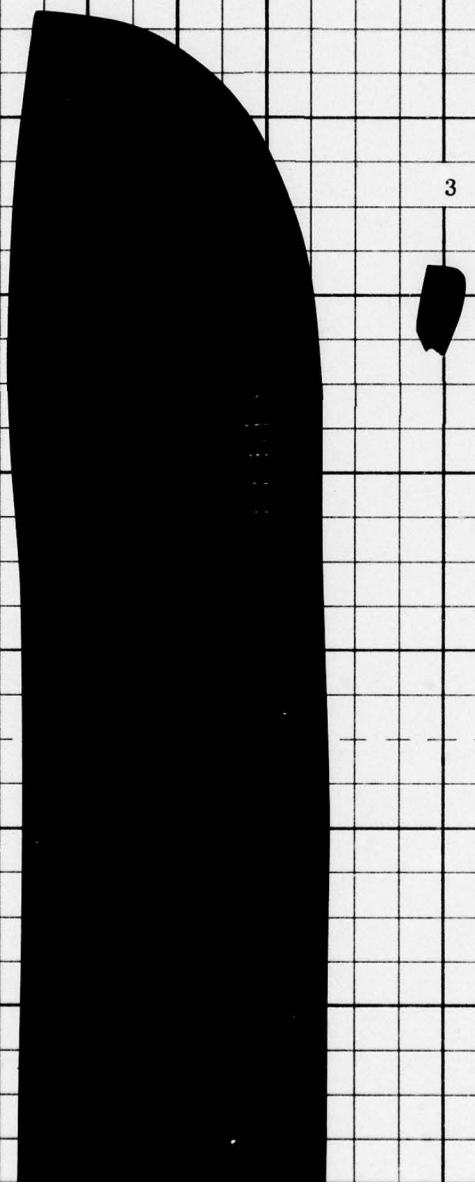

Figure 33. SEM - TSI

CUSTOMER 55979 JOB NO. ~~54565~~

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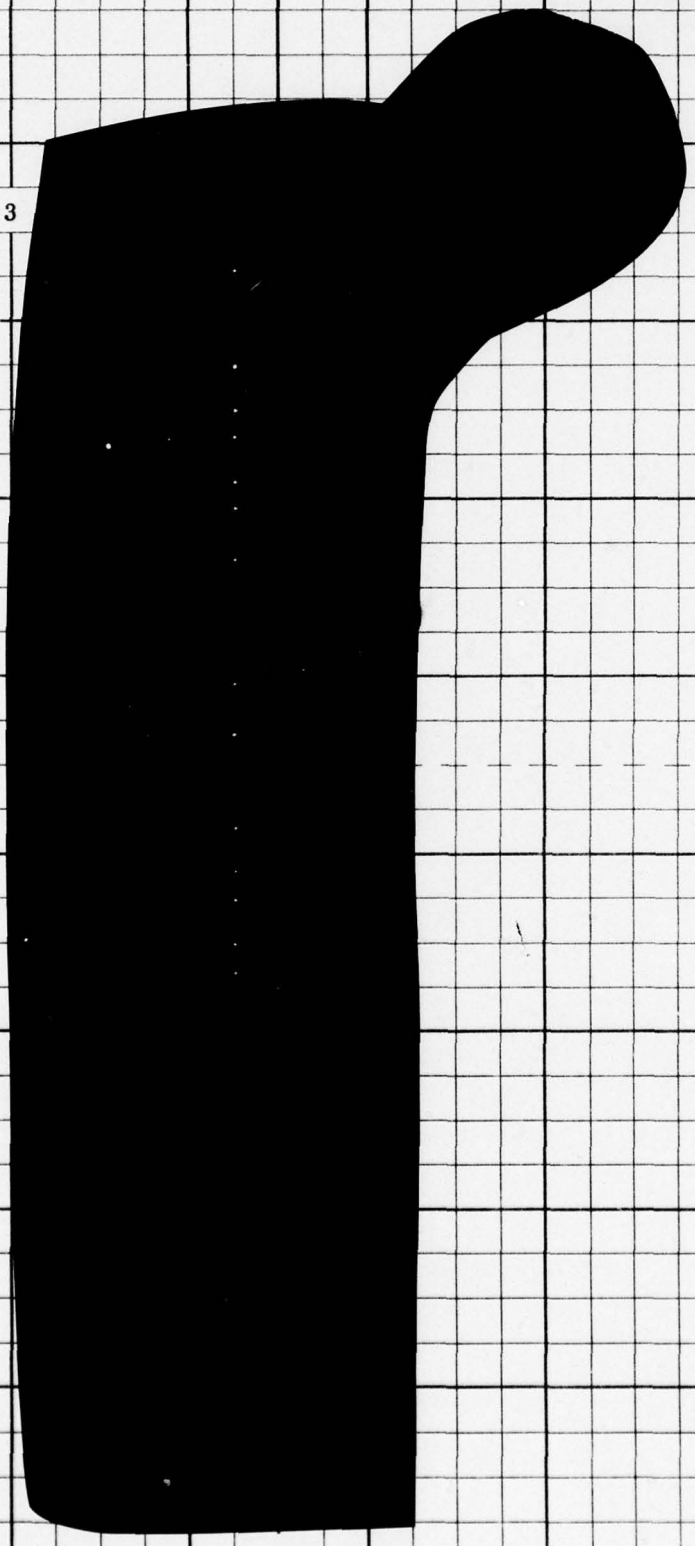

Figure 34. SEM - M-R

CUSTOMER 55973 JOB NO. 54565

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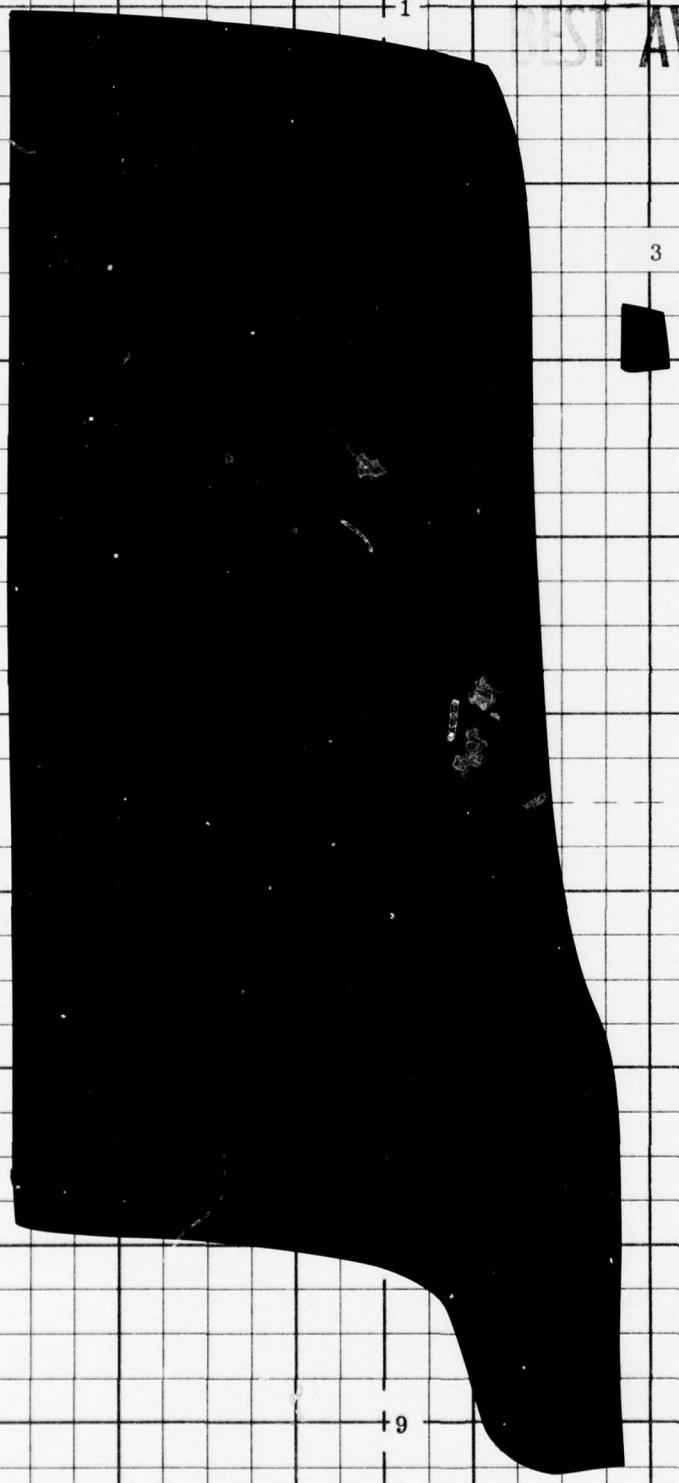

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Figure 35. SEM - Mux 157

CUSTOMER 55973 JOB NO. 5456

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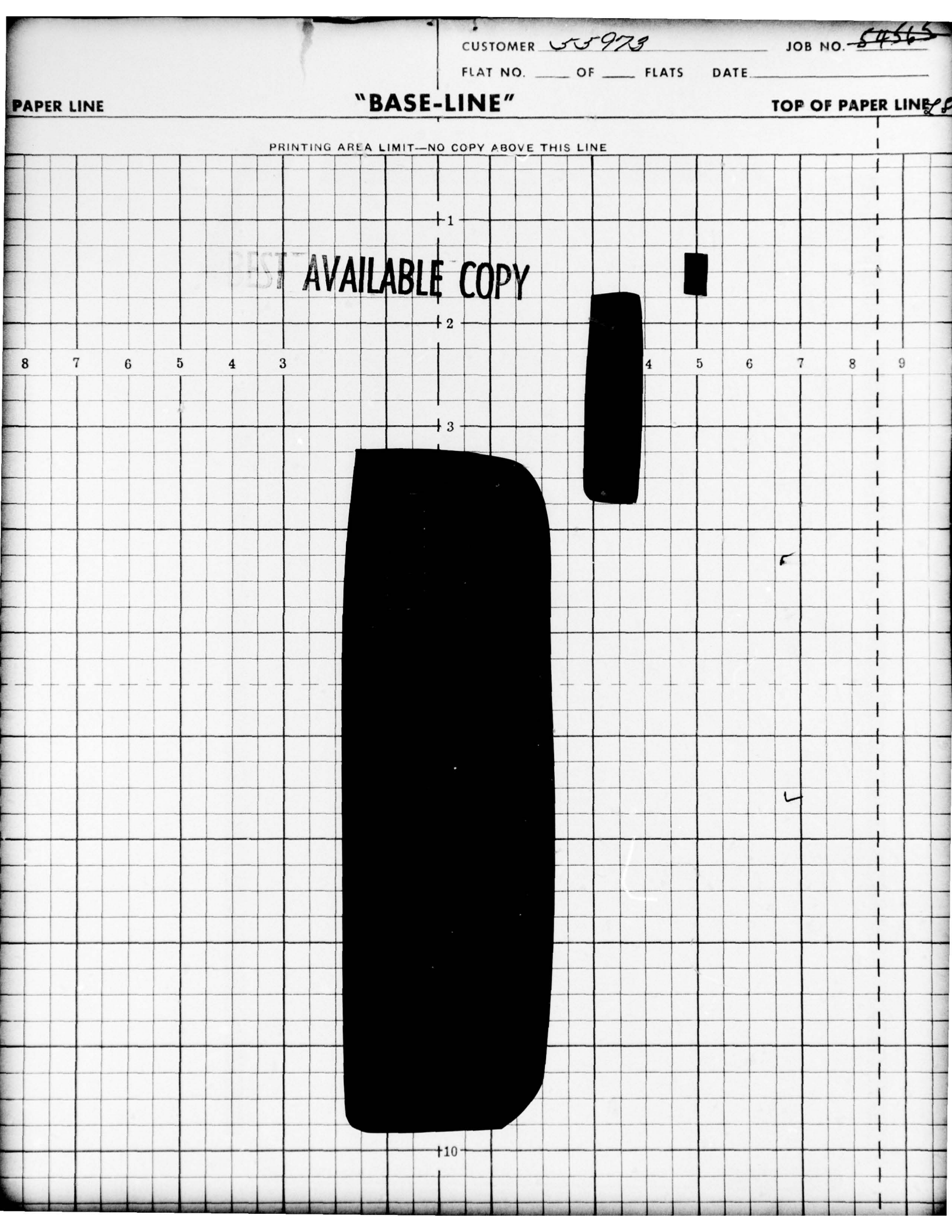

Figure 36. SEM - Add 283

CUSTOMER 55973 JOB NO. 5456

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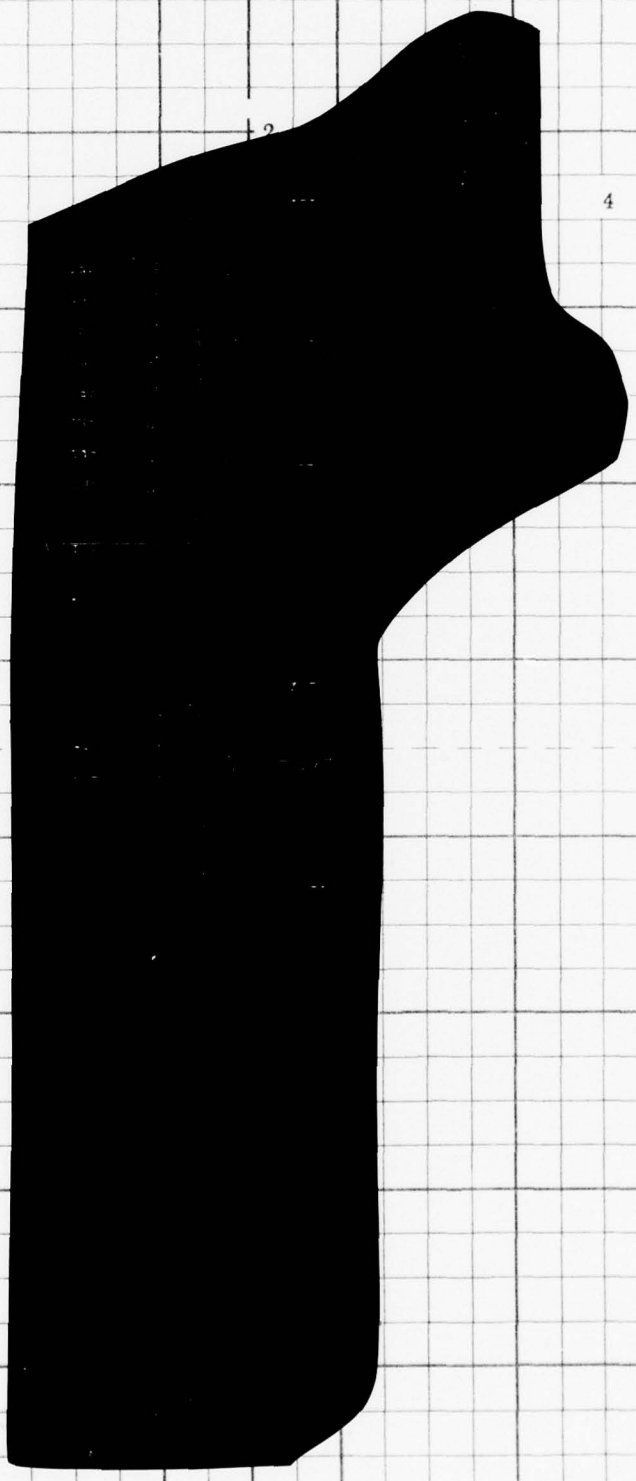

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TABLE 14

DIGITAL SIGNAL PROCESSOR PRINTED WIRING BOARD REQUIREMENTS

Custom Board Designation		Custom # Devices	Standard # Devices	In SEM's	Discretes	Boards Required DIP SEM's 60/Bd	F. P. SEM's 80/Bd	Hybrid SEM's 100/Bd
FO	1	89	126	126		2	1-1/2	1-1/4
	2	90	126	126		2	1-1/2	1-1/4
	3	88	168	160	8	2-3/4	2	1-1/2
(4 times)	4	91	93	85	8	1-1/2	1-1/4	1
	5	92	94	73	21	1-1/2	1-1/4	1
	6	85	119	102	17	2	1-1/2	1-1/4
(3 times)	7	89	92	71	21	1-1/2	1-1/4	1
	8	76	113	97	16	2	1-1/2	1-1/4
	9	87	91	69	22	1-1/2	1-1/4	1
	10	43	48	43	5	1	3/4	1/2
	11	91	94	61	33	1-1/2	1-1/4	1
	12	62	71	61	10	1-1/4	1	3/4
	14	89	120	97	23	2	1-1/2	1-1/4
	15	64	64	0	64	1-1/4	1	3/4
	16	87	147	122	25	2-1/2	2	1-1/2
	17	96	101	29	72	2	1-1/4	1
	18	74	88	70	18	1-1/2	1-1/4	1
	19	92	100	70	30	2	1-1/4	1
	20	86	90	39	61	1-1/2	1-1/4	3/4
	21	30	37	32	5	3/4	1/2	1/2
	22	86	107	76	31	2	1-1/2	1-1/4
	23	86	92	56	36	2	1-1/4	1
	24	102	123	88	35	2	1-1/2	1-1/4
	25	106	121	96	25	2	1-1/2	1-1/4
Total*	29	2432	2888	2236	652	49-1/2	38	29
Adjusted Total	35	2935	3486	2697	763	60	45	35

*This total was based on an initial design containing 29 PWB's - later changes to the processor required 35 PWB's on which the Base System data is predicated. Adjustments were made accordingly.

The board to board spacing computations are shown in table 15.

The computations of the comparative volume of the custom design versus the various SEM designs is shown in table 16.

It should be noted that standardization imposes volume penalties for two reasons. First, it physically takes more volume to package devices in a standard format, and second, additional devices are necessary to improve the standard circuits for a high level of commonality of use. It should also be noted, as shown in table 16, that the hybrid approach is the most effective packaging concept in keeping the volume penalty to an acceptable minimum.

Although weight was not studied in detail in this program, it can be expected that the penalty will be at the same relative levels.

2.2.3.2 Electrical Performance

It is expected that the same performance specifications can be met with SEM designs as with most custom designs. There is no basic limitation to achieving electrical performance with the SEM packaging concept. Performance will be limited only to the degree that the latest technology advancements have not been incorporated into the SEM family. This limitation can be minimized with an agressive updating program and through the use of custom modules in the SEM designs. The real penalty for equal performance is additional circuitry with its increased power, volume, weight, etc. This penalty will become less as designers become more accustomed to designing with standard modules and as functions in the standard's family become more complex and diversified.

2.2.3.3 Reliability

It has already been well proved from field data on the Navy's SEM concept that reliability is significantly improved (1 to 2 orders of magnitude). This is attributed to the qualification procedures and controls imposed on the design and manufacture of these SEM's. Since it is expected to follow the same general philosophy on the proposed SEM, the reliability has been assumed

TABLE 15

DIMENSIONAL BREAKDOWN FOR BOARD TO BOARD SPACING

Custom (DIP)		SEM (DIP)		SEM (Flat Pack)		SEM (Hybrid)	
Device	0.200	Device	0.200	Device	0.075	Device	0.125
Overlay	0.050	Able Therm	0.010	Able Therm	0.010	Able Therm	0.010
Able Therm	0.010	Overlay	0.050	P.C. Bd.	0.032	Overlay	0.050
P.C. Bd.	0.064	P.C. Bd.	0.032	Able Therm	0.010	P.C. Bd.	0.064
Lead Proj.	0.060	Able Therm	0.010	Overlay	0.050	Lead Proj.	0.060
	0.384	Overlay	0.050	P.C. Bd.	0.064		0.309
		P.C. Bd.	0.064	Lead Proj.	0.060		
		Lead Proj.	0.060		0.301		
			0.476				
Board Spacing	0.45"		0.55"		0.45"		0.45"

TABLE 16

VOLUME PENALTY WITH STANDARDIZATION

	# Bd's	Chassis Dimensions Spacing in.	Length in.	Width in.	Height in.	Volume in.^{3}	Volume Increase %
Custom (DIP)	35	0.45	15.75	9.12	7.06	1014	
SEM (DIP)	60	0.55	33*	10.12	7.62	2545	151%
SEM (Flat Pack)	45	0.45	20.25*	10.12	7.62	1562	54%
SEM (Hybrid)	35	0.45	15.75	10.12	7.62	1215	20%

*Requires 2nd chassis

to be an order of magnitude better than the custom circuit. Table 17 shows the data and computations of the SEM approach. For simplicity, it is assumed that the reliability is the same for all three SEM approaches.

2.2.3.4 Life Cycle Cost Analysis

Cost, reliability, and maintainability characteristics of various standard electronic module (SEM) designs were developed during earlier phases of this contract. The three classes of SEM modules included in this effort are dual in-line package (DIP), flat pack (FP), and hybrid.

The selected digital signal processor (DSP) current design was selected as a baseline for comparison with each of the above three classes of SEM modules. A preliminary design effort resulted in estimates of packaging the DSP with SEM DIPS, SEM FP, and SEM hybrid.

2.2.3.4.1 Scenerio. - To perform this analysis a scenerio was generated that assumes there are:

7 Bases
72 AC/BASE
30 FH/AC/Month
650 Total A/C procurred
15 year Maintenance Life

TABLE 17

COMPUTATION OF FAILURE RATES

λ/device = 0.17 failures/10^6 hours

# Devices	λ/SEM	# SEM's	Total SEM Failure Rate
3	0.51	310	158.10
4	0.68	63	42.84
7	1.19	6	7.14
8	1.36	29	39.44
14	2.38	22	52.36
20	3.40	7	23.80
21	3.57	10	35.70
22	3.74	2	7.48
			366.86

λ Total for SEM's = 366.86

λ Total Dips not in SEM's

$= 763 \times 1.7 \times 10^{-6}$ = 1297.10

Total λ = 1663.96

2.2.3.4.2 Maintenance. - The maintenance philosophy assumed is for built-in-test (BIT) fault isolation to the line replaceable unit (LRU), in this case the DSP. This unit is then installed on the field AGE to fault isolate to the smallest replaceable assembly (SRA) which in this case is a printed wiring board (PWB). The PWB is then returned to the depot for replacement of the bad element, either a DIP or a SEM as applicable.

2.2.3.4.3 Approach. -

a. Logistic Support Costs

The USAF Logistic Support Cost model developed by the Avionics Laboratory, for the EAR Program, was used by Westinghouse to quantify LSC for each design. The model is described in the User Documentation, dated May 1974, and revised July 1975 by Westinghouse. A copy of the basis document is available in the EAR Program Office of the Avionics Laboratory.

The summary results of the LSC tradeoff studies are shown in table 18.

b. Life Cycle Costs

The life cycle cost model developed by NAVELEXSYSCOM Program Office (PME-107X), Naval Material Command, Washington, D.C., with minor modifications by Westinghouse, was used by Westinghouse to quantify the LCC in these tradeoff studies.

The output products of the LCC model include a series of output reports, each with a comprehensive breakdown displayed for each cost category.

The LCC results include the impact of inflation at an annual rate of 10 percent. Discounting at an annual rate of 10 percent is also included. The summary results of the LCC tradeoff studies are shown in Table 18.

2.2.3.4.4 Reliability. - The reliability of the various versions of the Digital Signal Processor was calculated as follows:

The failure rate in a custom design is about 1.7×10^{-6} failures/hour/DIP. Now, from Navy Data on their SEM's, we can expect that the reliability of circuits in SEM's will be about an order of magnitude better or = 0.17×10^{-6}. The 763 conventional DIP's on the boards retain the 1.7×10^{-6} Failure Rate. Using these figures we obtain a failure rate for a SEM version of the DSP of 1663.96 failures per million hours or an MTBF of 600.98 hours. For the purposes of this analysis all SEM versions are assumed to have the same MTBF.

Cost

Unit sell prices for the DIP, FP, and hybrid configurations are summarized in the following tables. Each configuration includes separate costs for the chassis including assembly, and testing bare boards, and material comprising all SEM packages plus the DIP's not in SEM packages.

Note: There are 35 PWB's in the Base Design.

- Cost of DIP SEM LRU (60 PWB's per LRU)
- Chassis: 60/35 x 3015.34 + 1774 = 6943.22
- BARE PWB's: 60 x 123.63 = 7418.15
- DIP SEM Circuits

IC's per SEM	SEMS per LRU		Sell Price/ SEM		Total Cost of SEM Type	
3	310	x	30.36	=	9411.09	
4	63	x	37.16	=	2341.15	
7	6	x	56.69	=	340.11	
8	29	x	61.44	=	1781.85	
14	22	x	94.96	=	2089.12	
20	7	x	128.81	=	901.67	
21	10	x	136.86	=	1368.66	
22	2	x	171.05	=	342.11	
						18575.75

- DIP's not in SEM 763 x 5.33 = 4068.32
- DIP SEM LRU Sell Price $37,005.44

Average Cost of PWB Assy $568.84

- Cost of FP SEM LRU (45 PWB's per LRU)
- Chassis: 45/35 x 3015.24 + 1774 = 5650.97
- BARE PWB: 45 x 123.63 = 5561.81
- FP SEM Circuits

IC's/ SEM	SEMS/ LRU		Sell Price/ SEM	Total Cost of SEM Types	
3	310	x	37.31	11566.33	
4	63	x	44.97	2832.83	
7	6	x	71.98	431.87	
8	29	x	79.20	2296.92	
14	22	x	131.22	2886.92	
20	7	x	182.62	1278.36	
21	10	x	189.58	1895.80	
22	2	x	240.06	480.11	
					23671.67

- DIP's Not in SEMs 763 x 5.33 = 4068.32
- FP SEM LRU Sell Price = $38,953.13

Average Cost of PWB Assembly = $748.90

- Cost of Hybrid SEM (MHP) (35 PWB's per LRU)
- Chassis 3015.24 + 1774 = 4789.47
- Bare PWB's: 35 x 123.63 = 4327.25
- MHP SEM Circuits

IC's/ SEM	SEMS/ LRU	Sell Price/ SEM	Total Cost of SEM Types
3	310	25.47	7897.04
4	63	39.90	2514.21
7	6	45.54	273.24
8	29	47.80	1386.21
14	22	70.30	1546.61
20	7	86.30	604.13
21	10	90.04	900.40
22	2	111.91	223.82
			15,345.70

- DIP's Not in SEM 763 x 5.33 = 4,068.32
- MHP SEM LRU Sell Price = $28,562.71

Note Average Cost of PWB Assembly = $794.26

All cost data was accumulated on the basis of large quantity production (5000-10000) and a maximum of automated manufacturing, inspection, and test. DIPs and flat packs have been used in custom systems for many years and production techniques are already matured. Little reduction in fabrication cost will be realized with these devices in the SEM format. This, however, is not true with hybrids which is a relatively immature technology. A concept is projected for low cost which uses a minimum of fabrication labor with devices on tape carriers and a simplified ceramic package with soldered (or brazed) on lead frames. Devices may be tested before being assembled and maximum yield can be expected. Significant reduction in production costs can be expected.

The LSC and LCC results are summarized in table 18. LSC results include a cost breakdown for each of the eight basic equations. In addition, the operational availability is shown for each result. The LCC includes development, acquisition, initial, and recurring costs.

The LSC for DIP, FP and HYBRID are all less than the BASE design. The LCC summary shows the impact of higher acquisition costs for DIP and FP. As a result, only the HYBRID offers a reduction in both LSC and LCC. With a HYBRID SEM the LCC is about $3,000,000 (8%) less than LCC for the BASE package.

TABLE 18

LSC/LCC TRADE STUDY RESULTS

X $1,000

LSC	BASE	DIP	FP	HYBRID
1. Pipeline Spares	1020.	684.	745.	565.
2. Replenishment	0.	0.	0.	0.
3. On-Eq. Maint.	22.	10.	10.	10.
4. Off-Eq. Maint.	1188.	669.	721.	650.
5. Inv. Entry	414.	692.	524.	414.
6. Supp. Equip.	3831.	3972.	3862.	3773.
7. Training	62.	43.	43.	43.
8. Data & Mgmt	1328.	1239.	1239.	1239.
TOTAL LSC	7866.	7309.	7143.	6694.
OPER AVAIL.	0.9926	0.9968	0.9968	0.9968
LCC				
1. Development	1074.	974.	974.	974.
2. Acquisition	20349.	24053.	25319.	18566.
3. Initial	2204.	1751.	1792.	1672.
4. Recurring	11588.	11160.	11149.	11018.
	35215.	37939.	39234.	32230.

2.2.4 Analog/RF Review

The SEM packaging concept was evaluated for use with standard function analog and RF modules. Two parameters will be the dominate factors in limiting the use of the SEM package for analog circuits. These are the upper frequency limits of the circuit and signal levels.

If boards are plugged into a wire wrapped matrix plate the upper frequency limit of analog signals is less than 30 MHz for any level signal and less than 1 MHz for low level signals. These limits can be raised if provisions are made for coax interconnections between boards. With coax it should be possible to use PC assemblies up to 100 MHz. Above this frequency, PC assemblies will cease to be lumped circuits (circuits so concentrated in space that the assumption of simultaneous actions through the system is a good approximation) and layout and shielding considerations become critical.

At these frequencies crosstalk can limit gain and dynamic range. For high gain and dynamic range circuits, shielding should be used between boards, and filters should be used on boards to keep power supply and other interconnecting lines free from interference. High frequency circuits should also be mounted on boards which have a ground plane. The ground plane should make electrical contact with the chassis and shields to prevent ground currents.

It should not be difficult to design a standard, high frequency, completely shielded, plug-in board assembly that uses coax interconnections. It may also be necessary to provide shielded troughs or cable runs in the matrix plate for critical signals.

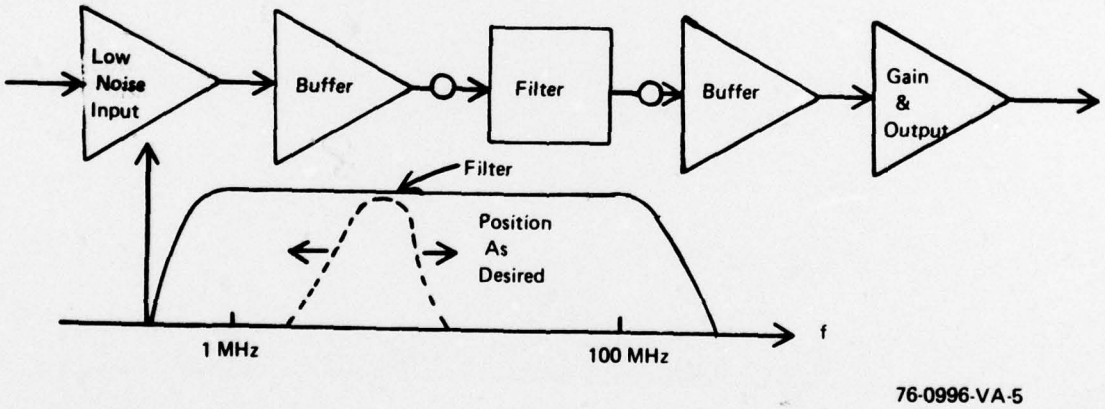
The SEM modules which are mounted on the boards can be used for analog circuits as well as digital. At frequencies above approximately 30 MHz, controlled impedance lines such as strip line or microstrip needs to be used for both analog and digital signals. For low level analog signals it may be necessary to develop a shielded SEM module. The shields of these modules should be designed so that when they are mounted on the PC board they make good electrical contact to the ground plane.

Special cautions must be taken if analog and digital circuits are to be included in the same enclosure. A single point grounding scheme becomes a necessity, with the digital ground and the analog ground kept completely

isolated from each other and only tied together at the one common ground point. Similarly power supplies should not be shared between analog and digital circuits. Analog and digital wiring should be kept as separate as possible in the matrix plate. Any highly sensitive circuits should be shielded. Other precautions such as special filtering and decoupling may be necessary also. The proposed SEM packaging concept with slight modifications is compatible with all the cautions that must be observed when analog and digital circuits are mixed.

The SEM packaging concept can be used with all of the analog modules in the current SHP inventory. The following are ideas for new analog/RF SEM's:

a. One module could be a low noise broadband module with enough power gain to be the primary noise contributor of a low noise system. It could contain provisions to mount a filter to select a band of interest, thereby rejecting unwanted signals which could be effective jammers. A block diagram could be as shown in figure 37.



This would be used in typical low noise modules where:

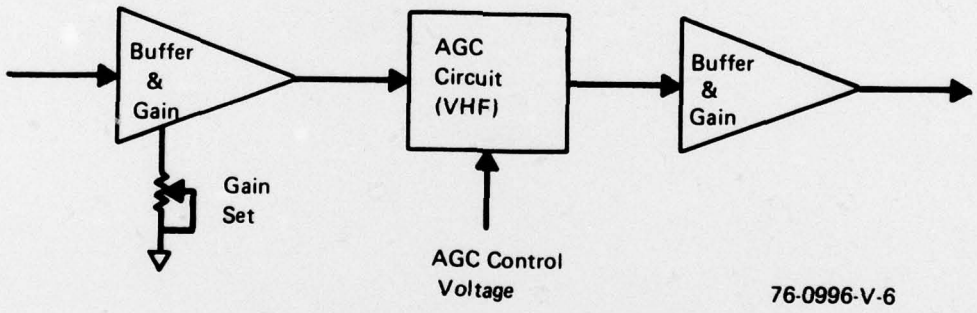
NF = 2 dB
Gp = 10 to 20 dB
BW = 200 MHz
Reverse transfer loss = 30 dB

Figure 37. SEM Low Noise Broad Band

b. A module could be made with AGC function and gain to be used typically after module A. This Module (figure 38) could also contain other functions such as a gain set. This module could have a nominal gain of 20-40 dB depending on where it is set. AGC could give 40 dB attenuation from nominal.

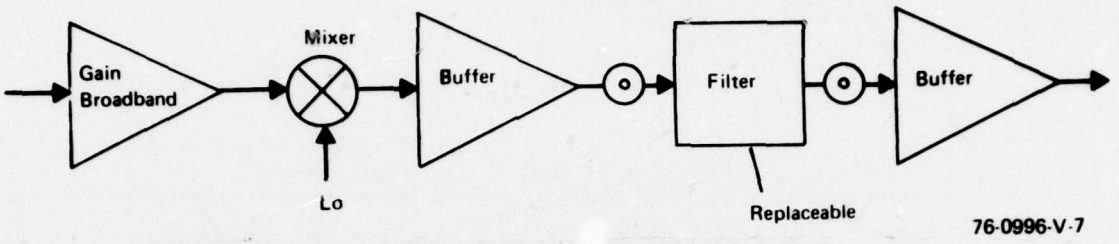
c. A module could be made with a broadband frequency converter on it for heterodyne systems. This module could also contain a replaceable filter which would allow selection or rejection of the mixer products. See figure 39. This module could allow IF's from base band to RF frequency.

d. A power gain module (figure 40) could also be made which would be used as an output stage for large signals on coax lines or for the mixer driver where exceptional mixer linearity is required. This module could be made to provide as much as 20 dBm output from 1 to 100 MHz.



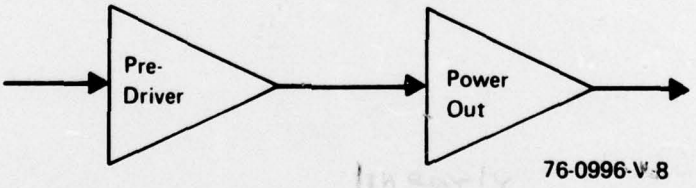
This could be used in any receiver application with an IF from 10 to 200 MHz - either pulse or cw typically 1 AGC per receiver channel would be used.

Figure 38. SEM - ASC



This could be used where the IF is 10 to 200 MHz typical. One per receiver channel would be used unless it were multiple conversion. The filter would be a matched filter or a frequency select filter to accept mixed products of interest.

Figure 39. SEM - Broadband Frequency Converter



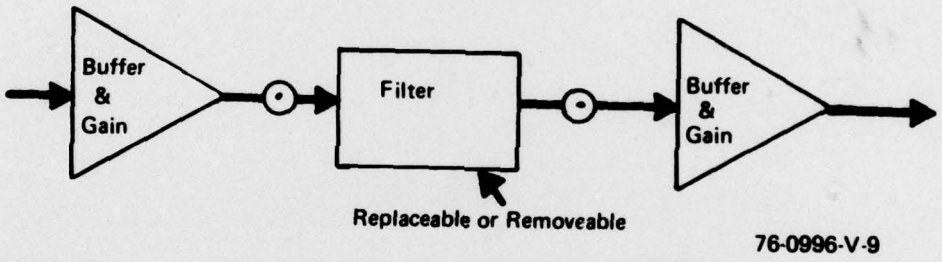
This would be used to handle large signals linearly at end of receive chain (i.e. pre detection gain). Typical use would be in doppler system where linearity is essential to avoid intermodulation products.

This module could be made to provide as much as 20 dBm output from 1 to 100 MHz.

Figure 40. SEM - Power Gain Module

d. A family of modules might be made to provide varying amounts of gain and power output level, to be used between a pre selector module (A) and power driver module (D). These modules could be made with provisions for band selecting if desired. See figure 41. Many other low frequency modules can be built to provide such functions as:

- AGC driver circuits
- Video amplifiers
- Sample and hold circuits
- Transfer functions for AGC, phase lock loops, etc.



This would be used for intermediate gain and band selecting (if required) in high gain systems. This would go between low noise gain stages and high power output stages - might include filtering.

Figure 41. Analog Module Family

SECTION III

3. CONCLUSIONS

The following conclusions may be drawn as the result of the work on this program:

- The proposed DIP and Flat Pack SEM concepts will have higher LCC due to higher acquisition cost than the custom design DIP implementation, however a significant reduction in LCC cost can be achieved through the use of Hybrid SEMs and automated fabrication and test.
- The proposed SEM concept reflects lower logistic support cost in all three configurations, i.e., DIP's, flat packs, and hybrids, when compared to the custom DIP design.
- The acquisition costs of the SEM DIP's and SEM flat packs are greater than the custom design because of the additional devices required to raise the level of commonality as well as the additional cost of more PWBs required to package the SEMs.
- Two similar types of digital signal processors show a high level intra and inter circuit commonality.
- Repartitioning of existing digital signal processors for SEM's is possible but approximately 25 percent more devices are required to obtain a high level of commonality. New designs or greater flexibility in redesigning existing processors would significantly reduce the additional devices required.
- The additional devices required in repartitioning an existing system coupled with the need for more volume to package in the SEM format makes the SEM DIP's and SEM flat pack volume penalty unacceptable for avionics applications.
- The low volume possible with hybrid microcircuits make the proposed SEM concept acceptable from a volume standpoint in repartitioning for standard circuits when replacing a custom DIP design.
- A significant benefit in power handling capability is realized with hybrid SEM's.
- The hybrid SEM has the highest power handling capability per board but the lowest per device because of the high device density.

- The proposed SEM configurations do not significantly decrease the power handling capability of discrete DIP's and flat packs.
- The flat pack SEM has the lowest power handling capability.
- In the proposed SEM concept, analog circuitry is practical in many cases but there are frequency limitations. Coaxial connections must be used in the higher frequencies.

4. RECOMMENDATIONS

- Major efforts should be placed in developing low cost hybrid microcircuit packaging.
- Additional partitioning studies are recommended with emphasis on new designs rather than repartitioning existing systems.
- Further life cycle cost studies should be conducted to optimize maintenance senerios.
- Consideration should be given to building demonstration hardware-preferably a system with large production potential.
- Work should be started on the many nontechnical areas related to standardization such as module specifications, approval procedures, qualification procedures, etc.
- Work should start on an effective management plan necessary for acceptance of SEM.