

AD-A048 052

STANFORD UNIV CALIF DIGITAL SYSTEMS LAB  
AN ALGORITHM FOR TESTING THE PLANARITY OF PARTIALLY ORIENTED GR--ETC(U)  
JUN 77 W M VANCLEEMPUT  
DSL-TN-116

F/G 9/3

N00014-75-C-0601

NL

UNCLASSIFIED

1 of 1  
AD  
A048052



END  
DATE  
FILMED

1- 78

DDC

FG.

11

AD A 0 48052

AN ALGORITHM FOR TESTING THE PLANARITY  
OF PARTIALLY ORIENTED GRAPHS

by  
W.M. vanCleemput

(See back page  
for 1473)

June 1977

Technical Note No. 116

Digital Systems Laboratory  
Departments of Electrical Engineering and Computer Science  
Stanford University  
Stanford, California 94305

AD No. \_\_\_\_\_  
JDC FILE COPY

DDC  
RECEIVED  
DEC 28 1977  
REGISTERED  
B

This work was supported by the Joint Services Electronics Program  
under contract N-00014-75-C-0601.

**DISTRIBUTION STATEMENT A**  
Approved for public release;  
Distribution Unlimited

Digital Systems Laboratory  
Departments of Electrical Engineering and Computer Science  
Stanford University  
Stanford, California 94305

Technical Note No. 116

June 1977

AN ALGORITHM FOR TESTING THE PLANARITY  
OF PARTIALLY ORIENTED GRAPHS

by

W.M. vanCleemput

ACCESSION for	
NTIS	White Section <input checked="" type="checkbox"/>
DDC	Buff Section <input type="checkbox"/>
UNANNOUNCED	<input type="checkbox"/>
JUSTIFICATION	<i>OK H.P.</i>
BY	
DISTRIBUTION/AVAILABILITY CODES	
Dist.	AVAIL. and/or SPECIAL
<i>A</i>	

ABSTRACT

An efficient algorithm will be presented for testing the planarity of oriented and partially oriented graphs. This algorithm is very useful for solving problems related to the circuit layout problem.

INDEX TERMS: graph theory, planarity, circuit layout problem, partially oriented graphs

This work was supported by the Joint Services Electronics Program under contract N-00014-75-C-0601.

## 1. INTRODUCTION

The problem of laying out printed circuits and integrated circuits shows a striking similarity with the problem of testing a graph for planarity [4].

In [2,3] a graph model for the circuit layout problem was presented. This model introduced the concept of a partially oriented graph.

A partially oriented graph is a triple  $(V,E,O)$  where  $V$  is the set of vertices,  $E$  is the set of edges and  $O$  is a collection of cyclic permutations of vertices that are adjacent to the same vertex.

An important step in obtaining an optimal layout of a circuit using graph-theoretical methods consists of testing the graph representation of the circuit for planarity.

In [5] an  $O(|V|^2)$  algorithm for this problem was presented, where  $|V|$  is the number of vertices of the graph model. This algorithm is based on the one by Lempel, Even and Cederbaum [9].

In this paper an algorithm, based on Tarjan's [1] algorithm for testing the planarity of simple (i.e. non-oriented) graphs will be presented. This new algorithm requires  $O(|V|)$  steps, which is a significant improvement.

## 2. DEFINITIONS

All undefined theoretical concepts used in this paper follow Behzad and Chartrand [6] and Harary [7].

The following definitions concerning oriented graphs are adapted from [8]:

### DEFINITION 1:

An oriented graph is a triple  $(V,E,O)$ , where  $V$  is the set of vertices,  $E$  is a family of subsets of  $V$  of cardinality 2 and  $O$  is a collection of cyclic permutations of members of  $V$ , that are adjacent to the same vertex.  $\square$

In other words, if  $v$  is a member of  $V$ , then there exists in  $O$ , a



member  $F$ , such that  $F$  is a cyclic permutation of the vertices of  $V$ , that are adjacent to  $v$ .

DEFINITION 2:

An oriented graph  $G$  is planar if it can be embedded in the plane such that for the arcs  $a(i)$  with a common endpoint  $P$  that correspond to the edges incident to a given vertex  $v$ , a clockwise sweep around  $P$  encounters these arcs  $a(i)$  in the order prescribed by the orientation.  $\square$

Let  $a, b$  and  $c$  be three adjacent edges incident to a vertex  $v$ ; by  $b \ll [a, c]$ , we will indicate that a clockwise sweep around  $v$  encounters these three edges in the order  $a, b, c$  (i.e.  $b$  lies between  $a$  and  $c$ ).

DEFINITION 3:

A planar oriented graph is outerplanar if it can be embedded such that every vertex of  $G$  lies on the boundary of some region (usually the exterior region).  $\square$

DEFINITION 4:

$G$  is an oriented graph of type 1 if there exist in  $G$  two distinct vertices  $m$  and  $n$  and three paths  $p_1, p_2$  and  $p_3$ , from  $n$  to  $m$ , such that each edge of  $G$  belongs to exactly one of these paths and if  $N_1, N_2$  and  $N_3$  are edges incident to  $n$  and belonging to  $p_1, p_2$  and  $p_3$  respectively and if  $M_1, M_2$  and  $M_3$  are edges incident to  $m$  and belonging to  $p_1, p_2$  and  $p_3$  respectively then  $N_1 \ll [N_2, N_3]$  if and only if  $M_1 \ll [M_2, M_3]$ .  $\square$

An example of such a graph is given in Fig. 1(a).

DEFINITION 5:

$G$  is an oriented graph of type 2 if there exists a vertex  $n$  and two cycles  $C_1$  and  $C_2$  such that each edge of  $G$  belongs to exactly one of the cycles and if vertex  $n$  is incident to edges  $M_1$  and  $N_1$  of cycle  $C_1$  and to edges  $M_2$  and  $N_2$  of cycle  $C_2$  then  $M_2 \ll [M_1, N_1]$  if and only if  $M_1 \ll [M_2, N_2]$ .  $\square$

Fig. 1(b) shows an example of a graph of type 2.

Theorem 1: if  $G$  is a minimal non-planar subgraph of an oriented graph, then  $G$  is an oriented graph of type 1 or  $G$  is an oriented graph of type 2. [8].  $\square$

Testing an oriented graph for planarity, using this characterization

is not practical.

DEFINITION 6:

A graph  $G(V,E,0)$  is partially oriented if for some  $v$  in  $V$ , there exists a cyclic permutation  $F$  that belongs to  $0$ .  $\square$

The following definitions, related to efficient algorithms are from [1].

DEFINITION 7:

The adjacency list of a vertex  $v$  is an unordered list of the vertices, adjacent to  $v$ .  $\square$

DEFINITION 8:

The adjacency structure  $A$  of a graph  $G$  is the collection of adjacency lists for all vertices of  $G$ .  $\square$

DEFINITION 9:

In a directed graph,  $v$  is an ancestor of  $w$  and  $w$  is a descendant of  $v$  if there exists a path from  $v$  to  $w$ . If the path is of length 1, then  $v$  is the father of  $w$  and  $w$  is the son of  $v$ .  $\square$

### 3. TARJAN'S ALGORITHM

Tarjan's algorithm [1] forms the basis for the algorithm, described in section 4. It is required that the graph being tested is 2-connected. The graph is specified in the form of an adjacency structure  $A$ .

Tarjan's algorithm is linear in  $|V(G)|$ . If the graph is not 2-connected, then it can be decomposed into 2-connected components in  $O(|V|)$  time and the planarity of each of these 2-connected components has to be tested separately.

### 4. PLANARITY TESTING FOR PARTIALLY ORIENTED GRAPHS

This section is concerned with an extension to Tarjan's algorithm for testing the planarity of a partially oriented graph  $G$  in linear time. We can reduce the problem to testing the planarity of partially oriented graphs with oriented vertices of valency 3 only. This can be accomplished by replacing every oriented vertex of valency  $n$ , greater than 3, by a cycle with  $n$  new oriented vertices of valency 3, as illustrated in Fig. 2.

Let  $G'$  be the partially oriented graph, obtained by this transformation. Then the following holds.

Theorem 2:  $G'$  is planar if and only if  $G$  is planar.

Proof: a) suppose  $G'$  is planar. Then  $G$  can be obtained from  $G'$  by contracting the cycles that replaced the oriented vertices of valency greater than 3. Then  $G$  is planar.

b) if  $G$  is planar, then  $G'$  is planar. If  $G$  is planar, then there exists a cycle basis  $Z(1), \dots, Z(m)$  and a cycle  $Z(0)$  in  $G$ , such that every edge of  $G$  belongs to exactly two of these cycles (MacLane). Then, because of the transformation defined, there exists a cycle basis  $Z'(1), \dots, Z'(n)$  and a cycle  $Z'(0)$  in  $G'$ , such that every edge of  $G'$  belongs to exactly two of these cycles.

For most circuit layout graphs, oriented vertices will be of valency 3. If not, it will be assumed that the component models have been transformed such that this property holds.

It can easily be verified that  $|E(G')| \leq |E(G)|$  and that  $|V(G')| \leq 2 \cdot E(G)$ . Therefore, if  $|E(G)| = k \cdot |V(G)|$  then  $|E(G')| = k' \cdot |V(G')|$ .

The following algorithm is a modification of Tarjan's algorithm. It allows one to test the planarity of a partially oriented graph  $G(V, E)$  with oriented vertices of valency 3 only, in time proportional to  $|V|$  if  $|E| = k \cdot |V|$ .

Steps 1-3 are essentially the same as in Tarjan's algorithm.

(1) Apply a depth-first search to  $G$ , starting from some (arbitrarily chosen) vertex  $s$ . This search imposes a direction upon the edges of  $G$ , depending on the order in which its end-vertices were reached by the search. By doing so,  $G$  is transformed into a directed graph  $G'$ , whose edges are partitioned into a set of edges, forming a spanning tree, and a set of fronds. The directed graph  $G'$  is called a palm tree

(2) Reorder the adjacency structure, using the information



collected in the first step. This is done using a radix sort.

(3) Perform a depth-first search on the new adjacency structure, thereby partitioning  $G$  into a set of edge-disjoint paths. Let  $p = (s, \dots, f)$  be a path and let  $p_0 = (s_0, \dots, f_0)$  be the first path containing  $s$ . Then  $p$  is a special path if  $f = f_0$  and a normal path otherwise.

(4) Examine all paths  $p = (s, \dots, f)$ . If  $s$  is an oriented vertex, then determine on which side (Left or Right)  $p$  has to be embedded in order to satisfy the orientation imposed around  $s$ . If  $f$  is oriented, then determine on which side the frond has to descend. We can represent this as a function  $SIDE(p, v)$  with possible values L(ef), R(ight) and U(ndefined).  $SIDE(p, v) = U$  if vertex is not oriented.

First assume that  $p$  is a normal path. Then the frond of  $p$  has to descend on the same side as the embedding of the path. The following decision table indicates the action to be taken for each possible case.

---

$SIDE(p, s) \backslash SIDE(p, f)$	L	R	U
L	l	n	l
R	n	r	r
U	l	r	u

where l: embed  $p$  on the left.  
 r: embed  $p$  on the right.  
 u:  $p$  can be embedded on both sides.  
 n: the graph is non planar.

---

If  $p = (s, \dots, f)$  is a special path, then its frond has to descend on the same side as the frond of  $p_0$ , i.e. the path on which  $s$



debut, unless  $f=f_0=1$ . However, if  $f \neq 1$  then the valency of  $f$  must be at least 4 and therefore  $f$  cannot be an oriented vertex. If  $f=1$  and oriented, then we can require without loss of generality that the frond of  $p$  descend on the same side as the path's embedding (similar to normal paths). The only case left for special paths is when  $s$  is an oriented vertex. Then the embedding of  $p$  is determined by  $SIDE(p,s)$ .

5) Build a dependency graph. This step is essentially the same as in Tarjan's algorithm. Embed the first path (a circuit) in the plane as a polygon. Try to embed the other paths, in the order in which they were generated in step 3), one at a time. Each new path has exactly two points in common with the already embedded subgraph. Certain paths have to be embedded in different faces or in the same face, with respect to other paths. This relationship between paths can be represented by a dependency graph. Tarjan proves that it is sufficient to construct only a subgraph of this dependency graph, for which the number of edges is a linear function of  $V(G)$ .

6) Try to bicolor the dependency graph  $DG$ , using the colors L(ef) and R(igh).  $DG$  consists of one or more disconnected components. The difference with Tarjan's algorithm is that there are a number of vertices in  $V(DG)$  that have preassigned colors. Every vertex in  $V(DG)$  represents a path in the original graph. The bicoloring procedure consists of the following major steps.

- mark all vertices as unexplored.
- find a colored, but not explored vertex and mark it as explored. If no such vertex exists, then find an unexplored vertex and assign it any color (e.g. L). If all vertices have been explored, then  $DG$  can be colored with 2 colors and hence  $G$  is planar.
- use a depth-first search to explore the component of  $DG$ , containing the selected start-vertex: each time a vertex is reached, check whether it is colored or not. If not,

assign it the appropriate color. If it was already colored, check the colors: if they are compatible, continue; if not, the graph  $G$  is non-planar.

The procedure for enforcing the embedding of paths (step 4) requires  $O(|E|)$  time for general graphs and  $O(|V|)$  time if  $|E| = k \cdot |V|$ . Bicoloring the dependency graph requires time proportional to the number of edges in  $E(DG)$ . If a dependency subgraph was constructed and if  $|E| = k \cdot |V|$  then  $|E(DG)| = O(|V|)$  and the time required for testing the planarity of  $G$  is  $O(|V|)$ .

REFERENCES

- [1] Hopcroft, J., and Tarjan, R.E. "Efficient Planarity Testing", Journal ACM, Vol. 21, No. 4, pp. 549-568, October 1974.
- [2] vanCleemput, W. Mathematical Models and Algorithms for the Circuit Layout Problem, University of Waterloo, Ontario, Canada, Ph.D. Thesis, 1975.
- [3] vanCleemput, W. "Mathematical Models for the Circuit Layout Problem", IEEE Trans. on Circuits and Systems, Vol. CAS-23, No. 12, pp. 759-767, December 1976.
- [4] vanCleemput, W., "On the Topological Aspects of the Circuit Layout Problem", Proc. 13th Design Automation Workshop, San Francisco, California, June 1976.
- [5] Uyehara, T. et al, "Embedding a graph in a plane with local constraints", Proc. IEEE Int. Symposium on Circuits and Systems, San Francisco, California, pp. 181-185, April, 1974.
- [6] Behzad, M. and Chartrand, G., Introduction to the Theory of Graphs, Allyn and Bacon, Boston, Massachusetts, 1971.
- [7] Harary, F., Graph Theory, Addison Wesley Publishing Company, Reading, Massachusetts, 1969.
- [8] Ulrich, J.W., "A Characterization of Planar Oriented Graphs", SIAM Journal Applied Mathematics, Vol. 18, No. 2, pp. 364-371, March 1970.
- [9] Lempel, A., Even, S. and Cederbaum, I. "An Algorithm for Planarity Testing of Graphs", Proc. Int. Symp. on the Theory of Graphs (Ed. P. Rosenstiehl), Paris, France: Dunod, 1966, pp. 215-232.

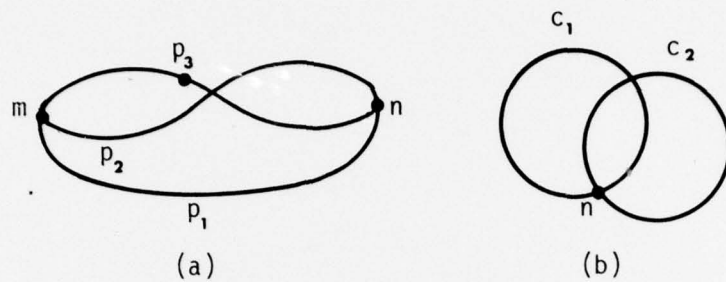


FIGURE 1 (a) Oriented graph of type 1.  
 (b) Oriented graph of type 2.



FIGURE 2 Replacing an oriented vertex of valency  $n$   
 by oriented vertices of valency 3.



14 DSL-TN-116

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER ✓ Technical Note #116	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) 6 AN ALGORITHM FOR TESTING THE PLANARITY OF PARTIALLY ORIENTED GRAPHS.		5. TYPE OF REPORT & PERIOD COVERED 9 Technical Note,
7. AUTHOR(s) 10 W.M./ van Cleemput		6. PERFORMING ORG. REPORT NUMBER
9. PERFORMING ORGANIZATION NAME AND ADDRESS ✓ Stanford Electronics Laboratories Stanford University Stanford, CA 94305		8. CONTRACT OR GRANT NUMBER(s) 15 N00014-75-0601
11. CONTROLLING OFFICE NAME AND ADDRESS Office of Naval Research Department of the Navy Washington, DC 22217		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
14. MONITORING AGENCY NAME & ADDRESS (if diff. from Controlling Office)		12. REPORT DATE June 1977
		13. NO. OF PAGES 11 12 p.
		15. SECURITY CLASS. (of this report)
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE
16. DISTRIBUTION STATEMENT (of this report) Reproduction in whole or part is permitted for any purpose of the United States government.		
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from report)		
18. SUPPLEMENTARY NOTES		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number) graph theory, planarity, circuit layout problem, partially oriented graphs		
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) An efficient algorithm will be presented for testing the planarity of oriented and partially oriented graphs. This algorithm is very useful for solving problems related to the circuit layout problem.		

**DISTRIBUTION STATEMENT A**  
 Approved for public release;  
 Distribution Unlimited

DD FORM 1473

EDITION OF 1 NOV 65 IS OBSOLETE

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

JSEP REPORTS DISTRIBUTION LIST

	<u>No. of Copies</u>		<u>No. of Copies</u>
<u>Department of Defense</u>			
Defense Documentation Center Attn: DDC-TCA (Mrs. V.Caponio) Cameron Station Alexandria, Virginia 22314	12	Dr. R. Reynolds Defense Advanced Research Projects Agency Attn: Technical Library 1400 Wilson Boulevard Arlington, Virginia 22209	1
Asst. Dir., Electronics and Computer Sciences Office of Director of Defense Research and Engineering The Pentagon Washington, D.C. 20315	1	<u>Department of the Air Force</u>	
Office of Director of Defense Research and Engineering Information Office Lib. Branch The Pentagon Washington, D.C. 20301	1	AF/RDPS The Pentagon Washington, D.C. 20330	1
ODDR&E Advisory Group on Electron Devices 201 Varick Street New York, New York 10014	1	AFSC (LJ/ Mr. Irving R. Mirman) Andrews Air Force Base Washington, D.C. 20334	1
Chief, R&D Division (340) Defense Communications Agency Washington, D.C. 20301	1	Directorate of Electronics and Weapons HQ AFSC/DLC Andrews AFB, Maryland 20334	1
Director, Nat. Security Agency Fort George G. Meade Maryland 20755 Attn: Dr. T.J.Beahn	1	Directorate of Science HQ AFSC/DLS Andrews Air Force Base Washington, D.C. 20334	1
Institute for Defense Analysis Science and Technology Division 400 Army-Navy Drive Arlington, Virginia 22202	1	LTC J.W. Gregory AF Member, TAC Air Force Office of Scientific Research Bolling Air Force Base Washington, D.C. 20332	5
Dr. Stickley Defense Advanced Research Projects Agency Attn: Technical Library 1400 Wilson Boulevard Arlington, Virginia 22209	1	Mr. Carl Sletten RADC/ETE Hanscom AFB, Maryland 01731	1
		Dr. Richard Picard RADC/ETSL Hanscom AFB, Maryland 01731	1
		Mr. Robert Barrett RADC/ETS Hanscom AFB, Maryland 01731	1

	<u>No. of Copies</u>		<u>No. of Copies</u>
Dr. John N. Howard AFGL/CA Hanscom AFB, Maryland 01731	1	Mr. John Mottsmith (MCIT) HQ ESD (AFSC) Hanscom AFB, Maryland 01731	1
Dr. Richard B. Mack RADC/ETER Hanscom AFB, Maryland 01731	1	LTC Richard J. Gowen Professor Dept. of Electrical Engineering USAF Academy, Colorado 80840	1
Documents Library (TILD) Rome Air Development Center Griffiss AFB, New York 13441	1	AUL/LSE-9663 Maxwell AFB, Alabama 36112	1
Mr. H. E. Webb, Jr. (ISCP) Rome Air Development center Griffiss AFB, New York 13441	1	AFETR Technical Library P.O. Box 4608, MU 5650 Patrick AFB, Florida 32542	1
Mr. Murray Kesselman (ISCA) Rome Air Development Center Griffiss AFB, New York 13441	1	ADTC (DLOSL) Eglin AFB, Florida 32542	1
Mr. W. Edwards AFAL/TE Wright-Patterson AFB Ohio 45433	1	HQ AMD (RDR/Col. Godden) Brooks AFB, Texas 78235	1
Mr. R. D. Larson AFAL/DHR Wright-Patterson AFB Ohio 45433	1	USAF European Office of Aerospace Research Technical Information Office Box 14, FPO, New York 09510	1
Howard H. Steenbergen AFAL/DHE Wright-Patterson AFB Ohio 45433	1	Dr. Carl E. Baum AFWL (ES) Kirtland AFB, New Mexico 87117	1
Chief Scientist AFAL/CA Wright-Patterson AFB Ohio 45433	1	ASAFSAM/RAL Brooks AFB, Texas	1
HQ ESD (DRI/Stop22) Hanscom AFB, Maryland 01731	1	<u>Department of the Army</u> HQDA (DAMA0ARZ-A) Washington, D.C. 20310	1
Professor R. E. Fontana Head, Dept. of Electrical Engr. AFIT/ENE Wright-Patterson AFB Ohio 45433	1	Commander U.S. Army Security Agency Attn: IARD-T Arlington Hall Station Arlington, Virginia 22212	1



	<u>No. of Copies</u>		<u>No. of Copies</u>
Commander U.S. Army Materiel Dev. & Readiness Command Attn: Tech. Library Rm 7S 35 5001 Eisenhower Ave. Alexandria, Virginia 22333	1	Commander Harry Diamond Laboratories ATTN: Mr. John E. Rosenberg 2800 Posder Mill Road Adelphi, Maryland 20783	1
Commander Research Laboratory ATTN. DRXRD-BAD U.S. Army Ballistics Aberdeen Proving Ground Aberdeen, Maryland 21005	1	Commandant U.S. Army Air Defense School Attn: ATSAD-T-CSM Fort Bliss, Texas 79916	1
Commander Picatinny Arsenal Dover, New Jersey 07081  ATTN: SMUPA-TS-T-S	1	Commandant U.S. Army Command and General Staff College Attn: Acquisition, Library Div Fort Leavenworth, Kansas 66027	1
ATTN: Dr. Herman Robl U.S. Army Research Office P.O. Box 12211 Research Triangle Park North Carolina 27709	1	Dr. Hans K. Ziegler (AMSEL-TL-D) Army Member, TAC/JSEP U.S. Army Electronics Command (DRSEL-TL-D) Fort Monmouth, New Jersey 07703	1
ATTN: MR. Richard O. Ulsh U.S. Army Research Office P.O. Box 12211 Research Triangle Park North Carolina 27709	1	Mr. J.E. Teti (AMSEL-TL-DT) Executive Secretary, TAC/JSEP U.S. Army Electronics Command (DRSEL-TL-DT) Fort Monmouth, New Jersey 07703	3
Mr. George C. White, Jr. Deputy Director Pitman-Dunn Laboratory Frankford Arsenal Philadelphia, Penna. 19137	1	Director Night Vision Laboratory, ECOM ATTN: DRSEL-NV-D Fort Belvoir, Virginia 22060	1
Commander Attn: Chief, Document Section U.S. Army Missile Command Redstone Arsenal, Alabama 35809	1	Commander/Director Atmospheric Sciences Laboratory (ECOM) Attn: DRSEL-BL/DD White Sands Missile Range New Mexico 88002	1
Commander U.S. Army Missile Command Attn: DRSMI-RR Redstone Arsenal, Alabama 35809	1	Director Electronic Warfare Lab., ECOM Attn: DRSEL-WL-MY White Sands Missile Range New Mexico 88002	1
Commander Chief, Materials Sciences Division, Bldg. 292 Army Materials and Mechanics Research Center Watertown, Massachusetts 02172		Commander US Army Armament Command Attn: DRSAR-RD Rock Island, Illinois 61201	1



	<u>No. of Copies</u>		<u>No. of Copies</u>
Project Manager	1	NL-H Dr. F. Schwering	1
Ballistic Missile Defense Program Office		TL-E Dr. S. Kronenberg	1
Attn: DACS-BMP ( Mr. A. Gold)		TL-E Dr. J. Kohn	1
1300 Wilson Blvd.		TL-I Dr. C. Thornton	1
Washington, D.C. 22209		NL-B Dr. S. Amorsos	1
Director, Division of Neuropsychiatry		Col. Robt. W. Noce	
Walter Reed Army Institute	1	Senior Standardization Rep.	1
of Research		U.S. Army Standardization Group, Canada	
Washington, D.C. 20012		Canadian Force Headquarters	
Commander, USASATCOM	1	Ottawa, Ontario, Canada KIA OK2	
Fort Monmouth, New Jersey 07703		Commander	
Commander, U.S. Army	1	CCOPS-PD	
Communications Command		Fort Huachuca, Arizona 85613	
Attn: Director, Advanced Concepts Office		Attn: H.A. Lasitter	
Fort Huachuca, Arizona 85613		<u>Department of the Navy</u>	
Project Manager, ARTADS	1	Dr. Sam Koslov	1
EAI Building		ASN (R&D)	
West Long Branch, N.J. 07764		Room 4E741	
U.S. Army White Sands Missile Range		The Pentagon	
STEWS-ID-R	1	Washington, D.C. 20350	
Attn: Commander		Office of Naval Research	1
White Sands Missile Range		800 N. Quincy Street	
New Mexico 88002		Arlington, Virginia 22217	
Mr. William T. Kawai		Attn: Codes 100	
U.S. Army R&D Group (Far East)	1	102	
APO, San Francisco, Ca. 96343		201	
Director, TRI-TAC	1	220	
Attn: TT-AD (Mrs. Briller)		221	
Fort Monmouth, N.J. 07703		401	
Commander	1	420	
U.S. Army Electronics Command		421	
Fort Monmouth, N.J. 07703		427 (All Hands)	
Attn: AMSEL-RD-O (Dr. W.S. McAfee)	1	432	
CT-L (Dr. G. Buser)	1	437	
NL-O (Dr. H.S. Bennett)	1	Naval Research Laboratory	
NL-T (Mr. R. Kulinyi)	1	4555 Overlook Aven. SW	
TL-B	1	Washington, D.C. 20375	
VL-D	1	Attn: Codes 4000 - Dr. A Berman	
WL-D	1	4105 - Dr. S. Teitler	
TL-MM (Mr. Lipetz)	1	4207 - Dr. J. McCaffrey	
(cont'd)		5000 - Dr. H. North	
		5200 - Mr. A. Brodzinsky	
		5203 - Dr. L. Young	
		5210 - Dr. J. Davey	

	<u>No. of Copies</u>		<u>No. of Copies</u>
Naval Research Laboratory 4555 Overlook Ave. SW Washington, D.C. 20375 Attn: Codes	1	R.N. Keeler NAVMAT - Code 03T CP # 5 2211 Jefferson Davis Hwy. Arlington, Virginia 20360	1
5220 - Mr. H. Lessoff			
5230 - Dr. R. Green			
5250 - Cf. L. Whicker			
5260 - Dr. D. Barbe		Mel Nunn	1
5270 - Dr. B. McCombe		NVMAT 0343	
5300 - Dr. M. Skolnik		CP# 5, Room 1044	
5403 - Dr. J. Shore		2211 Jefferson Davis Hwy.	
5464/5410 - Dr. J. Davis		Arlington, Virginia 20360	
5500 - Dr. T. Jacobs			
5509 - Dr. T. Giallorenzi		Dr. F.I. Tanczos	1
5510 - Dr. W. Faust		NAVAIR-03B	
6400 - Dr. C. Klick		JP# 1, Room 412	
7701 - Mr. J. Brown		1411 Jefferson Davis Hwy Arlington, Virginia 20360	
Director Office of Naval Research 495 Summer Street Boston, Mass. 02210	1	Dr. H.J. Mueller Naval Air Systems Command Code 310 JP # 1 1411 Jefferson Davis Hwy. Arlington, Virginia 20360	1
Director Office of Naval Research New York Area Office 715 Broadway 5th Floor New York, New York 10003	1	Mr. N. Butler Naval Electronics Systems Command Code 304 NC # 1 2511 Jefferson Davis Hwy. Arlington, Virginia 20360	1
Director of Naval Research Branch Office 536 South Clark Street Chicago, Illinois 60605	1	Mr. L.W. Sumney Naval Electronics Systems Command NC # 1 2511 Jefferson Davis Hwy. Arlington, Virginia 20360	1
Director of Naval Research Branch Office 1030 East Green Street Pasadena, Calif. 91101	1	J.H. Huth NAVSEA - Code 03C NC # 3, Room 11E08 2531 Jefferson Davis Hwy. Arlington, Virginia 20362	1
Office of Naval Research San Francisco Area Office 760 Market St. Room 447 San Francisco, Calif. 94102	1		
Harris B. Stone Office of Research, Development, Test & Evaluation NOP-987 The Pentagon, Room 5D760 Washington, D.C. 20350	1	Capt. R.B. Meeks Naval Sea Systems Command NC #3 2531 Jefferson Davis Hwy. Arlington, Virginia 20362	1
Dr. A.L. Slafkosky Code RD-1 Headquarters Marine Corps Washington, D.C. 20380	1		





	<u>No of Copies</u>		<u>No. of Copies</u>
Naval Weapons Center China Lake, Calif. 93555 Attn: Codes 605 - W.S. McEwan	1	Robert E. Frischell Johns Hopkins University Applied Physics Laboratory Laurel, Maryland 20810	1
5515 - M.H. Ritchie		Mr. G.H. Gleissmer	1
3945 - D.G. McCauley		Code 18	
5525 - Webster		David Taylor Naval Ship R&D Center	
35 - D.J. Russell		Bethesda, Maryland 20084	
55 - B.W. Hayes		Commander	1
3544 - H.W. Swinford		Pacific Missile Test Center	
3815 - R.S. Hughes		Code 4253-3	
D.E. Kirk	1	Point Mugu, Calif. 93042	
Professor & Chairman, Electronic Engineering Sp-304 Naval Postgraduate School Monterey, Calif. 93940		Richard Holden	1
Professor Sydney P. Parker	1	DF - 34	
Electrical Engineering Sp-62 Naval Postgraduate School Monterey, Calif. 93940		Naval Surface Weapons Center Dahlgren Laboratory Dahlgren, Virginia 22448	
Dr. Roy F. Potter	1	<u>Other Government Agencies</u>	
3868 Talbot Street San Diego, Calif. 92106		Mr. F.C. Schwenk, RD-T	1
Mr. J.C. French	1	National Aeronautics and Space Administration Washington, D.C. 20546	
Electronics Technology Division National Bureau of Standards Washington, D.C. 20234		Los Alamos Scientific Lab	1
John L. Allen	1	Attn: Reports Library P.O. Box 1663 Los Alamos, New Mexico 87544	
Deputy Director (Research & Advanced Technology) ODDR&E The Pentagon, Room 3E114 Washington, D.C. 20301		M. Zane Thornton	1
Leonard R. Weisberg	1	Deputy Director, Institute for Computer Sciences & Technology National Bureau of Standards Washington, D.C. 20550	
Assistant Director (Electronics & Physical Sciences) ODDR&E The Pentagon Washington, D.C. 20301		Director, Office of Postal Technology (R&D) U.S. Postal Service 11711 Parklawn Drive Rockville, Maryland 20852	1
George Gamota	1	NASA Lewis Research Center	1
Staff Specialist for Research ODDR&E The Pentagon, Room 3D1079 Washington, D.C. 20301		Attn: Library 21000 Brookpark Road Cleveland, Ohio 44135	



	<u>No. of Copies</u>		<u>No. of Copies</u>
Library - R51 Bureau of Standards Acquisition Boulder, Colorado 80302	1	Director Columbia Radiation Laboratory Department of Physics Columbia University 538 West 120th Street New York, New York 10027	1
MIT Lincoln Laboratory Attn: Library A-082 P.O. Box 73 Lexington, Mass. 02173	1	Director Electronics Research Laboratory University of California Berkeley, Calif. 94720	1
Dr. Jay Harris Program Director, Devices and Waves Program National Science Foundation 1800 G. Street Washington, D.C. 20550	1	Director Electronics Sciences Laboratory University of Southern California Los Angeles, California 90007	1
Dr. Howard W. Etzel, Deputy Director Division of Materials Research National Science Foundation 1800 G. Street Washington, D.C. 20550	1	Director Electronics Research Center The University of Texas at Austin Engineering-Science Bldg. 112 Austin, Texas 78712	1
Dr. Dean Mitchell, Program Director Solid-State Physics Div. of Materials Research National Science	1	Director of Laboratories Division of Engineering and Applied Physics - Tech. Reports Collection Harvard University Pierce Hall Cambridge, Massachusetts 02138	1
<u>Non-Government Agencies</u>			
Director Research Lab. of Electronics Massachusetts Inst. of Tech. Cambridge, Mass. 02139	1		
Director Microwave Research Institute Polytechnic Inst. of New York Long Island Graduate Center Route 110 Farmingdale, New York 11735	1		
Assistant Director Microwave Research Institute Polytechnic Inst. of New York 333 Jay Street Brooklyn, New York 11201			