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W. M. vanCleemput

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Technical Note No. 115

June 1977

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ABSTRACT

Two definitions for the planarity of a hypergraph will be given. These definitions are related to the problem of modelling circuits for circuit layout. It is shown that if a hypergraph is planar according to the first definition, then it is planar according to the second definition, but the reverse does not hold. Testing the planarity can be done in linear time by using the first definition but requires an enumeration using the second definition. The more accurate model for the circuit layout problem uses the second definition.

INDEX TERMS: Graph theory, hypergraphs, planarity of hypergraphs.



## INTRODUCTION

In [4] it is shown that hypergraphs can be used as an abstract model for electronic circuits. When considering the problem of laying out circuits in a single plane the problem of defining the planarity of a hypergraph arises. In [4] the components are modelled by edges of cardinality 2, while the connections are modelled by hyperedges (of cardinality 2 or greater).

In this paper we will derive two definitions for the planarity of a hypergraph and relate these definitions to the circuit layout problem. The first definition allows the testing of planarity in time linearly proportional to the number of vertices and hyperedges. The second definition, however, requires the generation of all possible combinations and does not appear to be polynomially bounded.

It will be shown that, if a hypergraph is planar according to the first definition, then it is planar according to the second definition.

### Definition 1:

A hypergraph  $H(A, X)$  is an algebraic structure, where  $A$  is a set of elements called the vertices and  $X$  is a family of non-empty subsets  $x(i)$  of  $A$ , called hyperedges satisfying  $\bigcup_{i=1, |X|} x(i) = A$  (see e.g. [1]).

### First Definition of Hypergraph Planarity

#### Definition 2:

A hypergraph  $H(A, X)$  is mapped into a simple graph  $G_1(V_1, E_1)$  as follows:

- a) every vertex  $a$  of  $H$  is mapped into a distinct vertex  $v'$  of  $G_1$   
 $[v' = f_1(a)]$ ; let  $V_1'$  be the set of all such vertices of  $G_1$ .
- b) every hyperedge  $x$  of  $H$  is mapped into a star subgraph with a distinct vertex  $v''$  in  $G_1$ , being the center vertex [i.e.  $v'' = g_1(x)$ ] and a collection of edges  $\{v'', v\}$  in  $G_1$ , corresponding to each of the vertices  $v$  in  $x$ . In other words, for every vertex  $a$  in a hyperedge  $x$ , there is an edge  $\{v'', v\}$  in  $G_1$  such that  $f_1(a) = v$  and  $g_1(x) = v''$ ; let  $V_1''$  be the set of all center vertices in  $G_1$  corresponding to the hyperedges in  $H$ . It is clear that  $G_1$  is a bipartite graph.



**Definition 3:**

A hypergraph  $H$  is planar (first definition) if and only if its associated simple  $G_1$  is planar<sup>†</sup>.

This definition of hypergraph planarity can lead to difficulties with respect to the circuit layout problem. Assume that components are modelled by simple subgraphs and nets by proper hyperedges (of which the cardinality can be greater than 2). Then the mapping defined here is not adequate since a net can be realized as any spanning tree on its vertex set.

It can be verified easily that testing the planarity of a hypergraph  $H(A, X)$  can be done in time  $O(|A| + |X|)$  using Tarjan's algorithm [5] on the associated simple graph.

**Second Definition of Hypergraph Planarity****Definition 4:**

A hypergraph  $H(A, X)$  is mapped into a collection  $\mathcal{C}$  of simple graphs  $G_2(V_2, E_2)$  as follows:

- a) Every vertex  $a$  of  $H$  is mapped into a distinct vertex  $v'$  of  $G_2$  [ $v' = f_2(a)$ ]. Let  $V'_2$  be the set of all such vertices of  $G_2$ .
- b) Every hyperedge  $x$  of  $H$  is mapped into a spanning tree on the set of vertices  $\{v(i) \mid v(i) = f_2(a(i)) \text{ and } a(i) \in x\}$ .

**Definition 5:**

A hypergraph is planar (second definition) if and only if there exists an associated simple graph  $G_2$  in the collection  $\mathcal{C}$  (as defined above), that is planar.

---

<sup>†</sup> For a definition of planarity of simple graphs see [3].

**Theorem** If a hypergraph is planar, according to the first definition, then it is planar according to the second definition.

**Proof:** Let  $H$  be a hypergraph, planar according to the first definition of planarity and let  $G_1$  be its associated simple graph. Then  $G_1$  is planar.

A hyperedge  $x=\{a(i), i=1, n\}$  is mapped into a star subgraph of  $G_1$ . Let  $v$  be the center vertex and  $v(i), i=1, n$  [where  $v(i) = f_1(a(i))$ ], the end vertices of this star subgraph. Apply the following transformation to  $G_1$ : select an edge of the star subgraph and contract it. The resulting graph is still planar. We can repeat this procedure for all hyperedges of  $H$ .

The resulting simple graph  $G_2$  satisfies the mapping used to define the planarity according to definition 2. Since  $G_2$  is planar,  $H$  is planar according to definition 2.

The converse of this theorem is not true. This can be illustrated by the following example:

The hypergraph in Figure 1 (a) is planar according to the second definition if the hyperedge  $\{2,3,5\}$  is mapped into simple edges  $\{2,4\}$  and  $\{4,5\}$  [Fig. 1 (b)]. But the mapping according to the first definition results in a non-planar graph as shown in Figure 1 (c). Replacing the hyperedge  $\{2,4,5\}$  by a star subgraph with a new vertex 6 as the center and with edges  $\{6,2\}$ ,  $\{6,4\}$  and  $\{6,5\}$  results in one of the well-known Kuratowski graphs i.e.  $K_{3,3}$ , the complete bipartite graph on six vertices, which is known to be non-planar [3].

The second definition of hypergraph planarity is a better model for the circuit layout problem, since in reality a conductor net can be represented by any connected graph without loops i.e. a tree.

Testing the planarity can no longer be done in linear time since one is required to enumerate all combinations of spanning tree decompositions for each of the hyperedges.



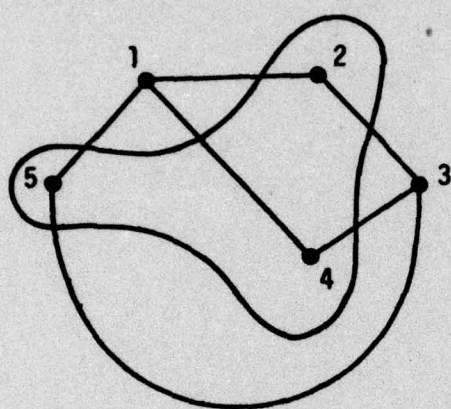
**CONCLUSIONS**

For solving the circuit layout problem optimally, it is necessary to use the second definition of hypergraph planarity. This would require enumerating all spanning trees over all of the hyperedges. Since this is impractical, the less desirable definition of hypergraph planarity is often used in conjunction with the circuit layout problem.

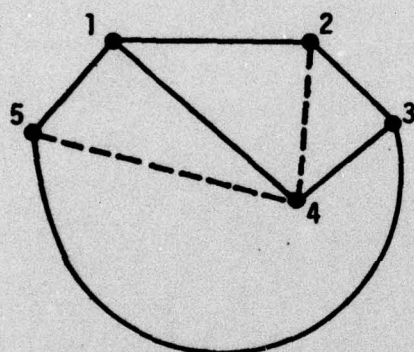


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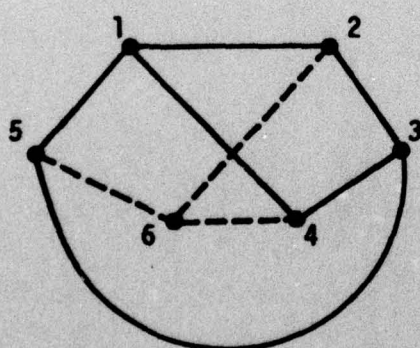
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(a)



(b)



(c)

Figure 1 Example of a hypergraph (a) that is planar according to the second definition (b) and non-planar according to the first definition (c).



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