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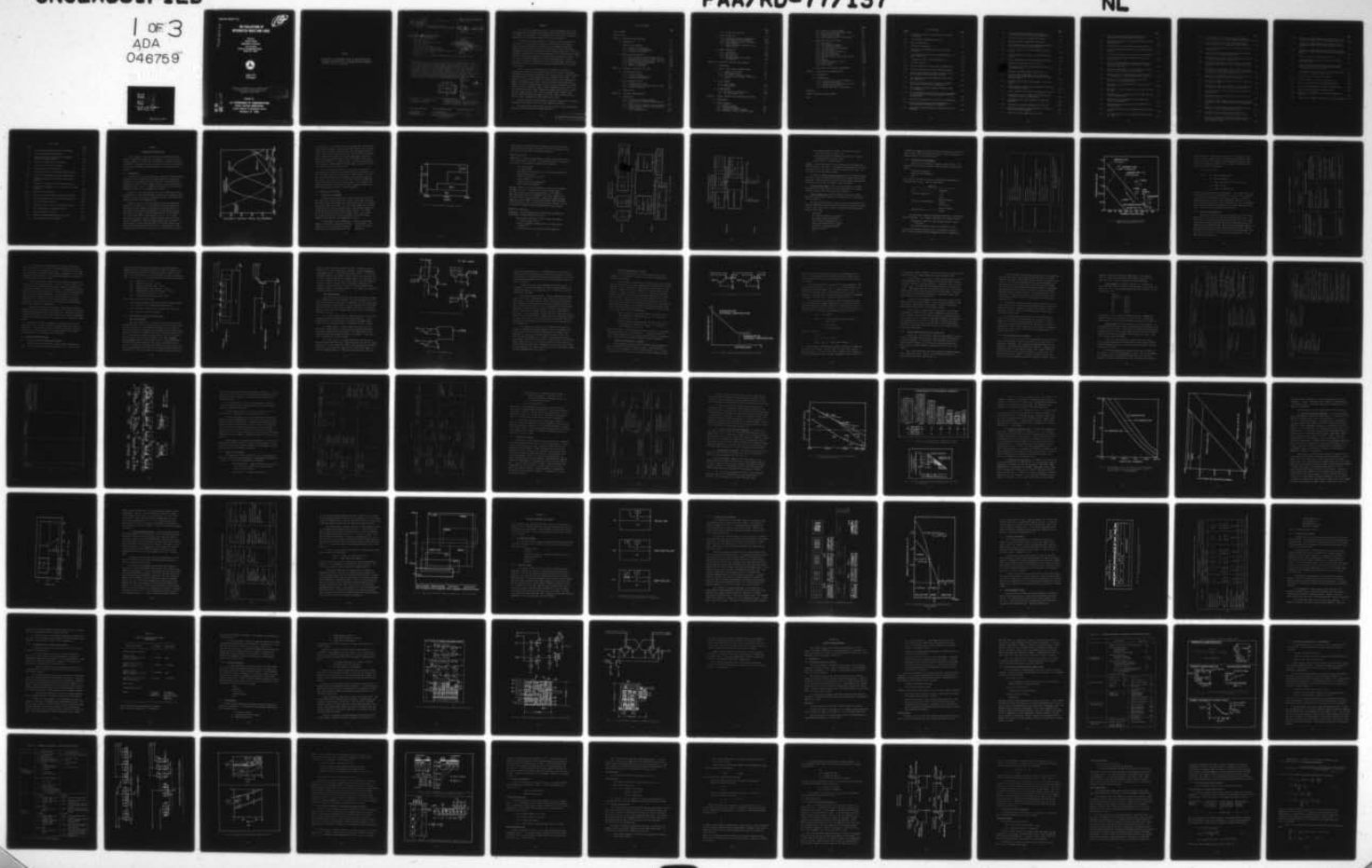

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AN EVALUATION OF INTEGRATED INJECTION LOGIC

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Final Report

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16. Abstract

Integrated injection logic is a relatively new integrated circuit technology which shows great promise for LSI applications. Although it is slow compared to other bipolar logic families, it has the lowest power-delay product of any technology, high packing density, and simple processing in certain versions. It has the capability of providing both analog and digital circuits on one chip. It is extremely flexible in that it can be tailored to meet diverse requirements such as LED drivers and low-current watch circuits. This report includes details of processing, theoretical and experimental characteristics, applications, and commercial activities.

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FOREWORD

This effort was conducted by the U.S. Naval Postgraduate School under the sponsorship of the Rome Air Development Center Post-Doctoral Program for the Federal Aviation Agency. Mr. Fred Sakate of the FAA was the task project engineer and provided overall technical direction and guidance.

The RADC Post-Doctoral Program is a cooperative venture between RADC and some sixty-five universities eligible to participate in the program. Syracuse University (Department of Electrical and Computer Engineering), Purdue University (School of Electrical Engineering), Georgia Institute of Technology (School of Electrical Engineering), and State University of New York at Buffalo (Department of Electrical Engineering) act as prime contractor schools with other schools participating via sub-contracts with the prime schools. The U.S. Air Force Academy (Department of Electrical Engineering), Air Force Institute of Technology (Department of Electrical Engineering), and the Naval Post Graduate School (Department of Electrical Engineering) also participate in the program.

The Post-Doctoral Program provides an opportunity for faculty at participating universities to spend up to one year full time on exploratory development and problem-solving efforts with the post-doctorals splitting their time between the customer location and their educational institutions. The program is totally customer-funded with current projects being undertaken for Rome Air Development Center (RADC), Space and Missile Systems Organization SAMSO), Aeronautical Systems Division (ASD), Electronic Systems Division (ESD), Air Force Avionics Laboratory (AFAL), Foreign Technology Division (FTD), Air Force Weapons Laboratory (AFWL), Armament Development and Test Center (ADTC), Air Force Communications Service (AFCS), Aerospace Defense Command (ADC), Hq USAF, Defense Communications Agency (DCA), Navy, Army, Aerospace Medical Division (AMD), and Federal Aviation Administration (FAA).

Further information about the RADC Post-Doctoral Program can be obtained from Jacob Scherer, RADC, Tel. AV 587-2543, COMM (315)-330-2543.

The authors of this report are Dr. Tien Tao of the U.S. Naval Postgraduate School and Dr. Robert Pierret of Purdue University

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CHAPTER I

BIPOLAR LSI INJECTION LOGIC

In this chapter an overview of the new bipolar injection logic family of integrated circuits will be presented. It includes the basic circuit concepts, a brief history, their present achievements and future developments. Detailed discussions of physical and electrical characteristics, device performance and applications will be presented in later chapters.

1.1. INTRODUCTION

In the past few years, the electronics industry has undergone rapid evolution because of the impressive progress made in LSI (large scale integration). The changes can be seen in Fig. 1-1 which presents the percentage of digital circuits shared by different types of electronics technologies since 1955. It is apparent that within the next few years, digital electronics will be dominated by LSI devices.

When LSI was first developed in the late 60's, MOS (metal - oxide - semiconductor) was the only technology considered because bipolar circuits at that time were more complex, dissipated more power, and did not lend themselves readily to LSI implementation.

However, since the late 60's, bipolar LSI has been making giant strides in two directions. In one direction, innovative fabrication techniques have been applied to conventional SSI and MSI bipolar circuits (small scale integration and medium scale integration), pushing them into the LSI domain. Some outstanding examples are LSI Schottky TTL, LSI ECL, LSI DCTTL[1] (direct coupled TTL), etc. In the other direction, new bipolar circuits have been invented which are tailored for LSI implementation. Some outstanding examples are EFL (emitter follower logic)[2], emitter function logic,[3] CHL (current hogging logic)[4] and several new bipolar circuits which share a common feature in that current injection schemes are used in one way or another for switching

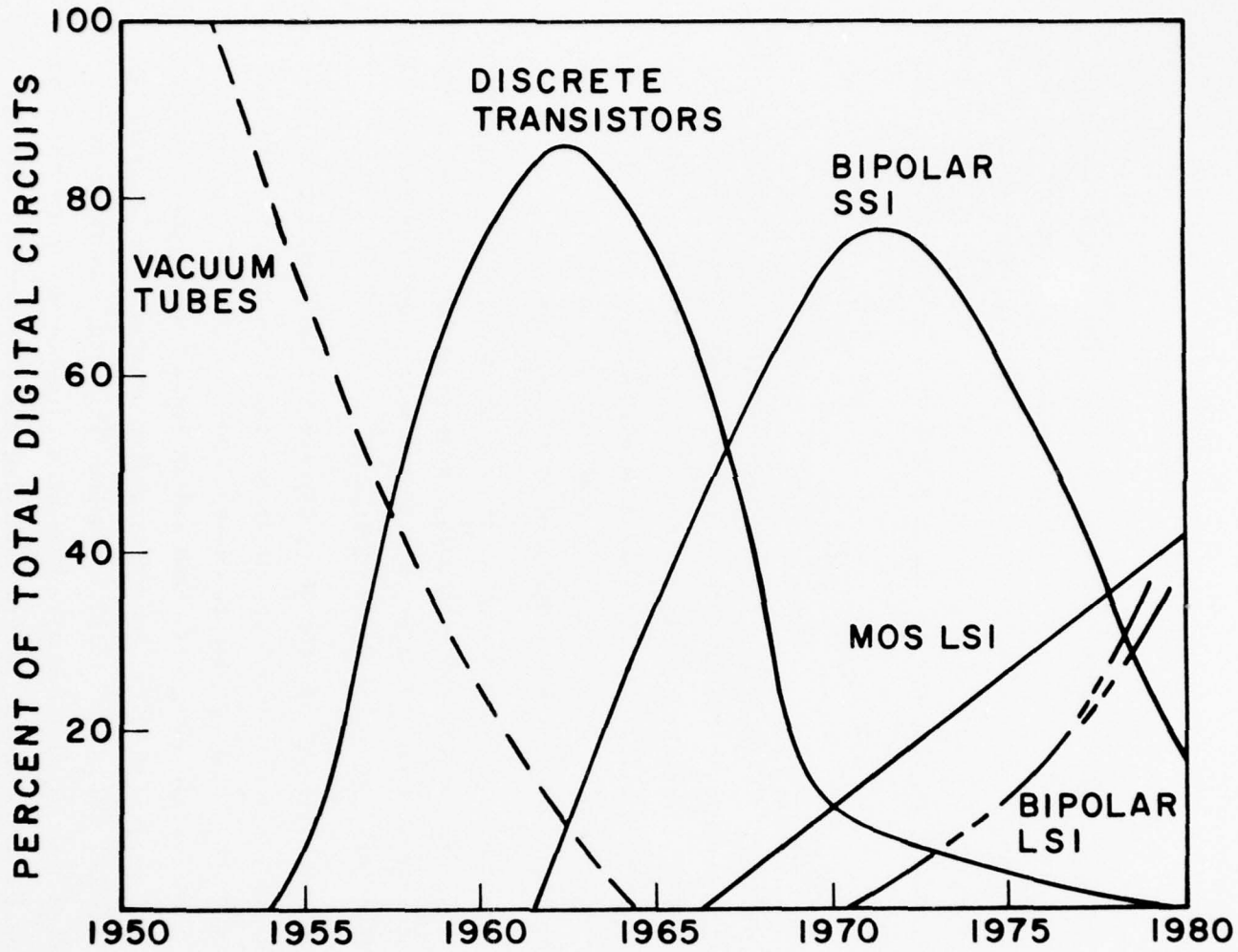


FIG. 1-1 PERCENTAGE OF DIGITAL CIRCUITS SHARED BY DIFFERENT ELECTRONIC TECHNOLOGIES

of transistors.[5] In this report, they are grouped into a family called "bipolar injection logic." The most well known and the first announced of this group is I^2L/MTL (integrated injection logic/merged transistor logic). These two names refer to the same circuit but have been adopted by the companies who invented the circuit independently around 1971: Philips of Netherlands who used the name I^2L[6] and IBM of West Germany who used the name MTL[7]. It seems that I^2L is now being more popularly used although the combined name of I^2L/MTL suggests two of the outstanding characteristics of this new circuit.

Since its invention, a short five years ago, the interest in injection logic is increasing at an amazing rate with superlative claims like, "I^2L looks like logic of the future," "Bipolar logic steps up to LSI, with the smart money on I^2L"[9] appearing in Electronics magazine. This report is the result of a survey of the activities, progress and state-of-the-art of bipolar LSI injection logic. It will digest the available information from journals, progress reports and private communications and present them in an organized manner.

1.2 LARGE SCALE INTEGRATION

1.2.1 Digital LSI Technologies

Integrated circuits have been classified into SSI, MSI, LSI and VLSI (very large scale integration) according to the number of devices on a single chip. The dividing lines are presented in Fig. 1-2 although they are not meant to be exact. SSI first became commercially available in the early 60's and were bipolar circuits. MSI appeared commercially in the mid 60's and were also mainly bipolar circuits. LSI became available during the late 60's and were MOS circuits. Only recently have commercial bipolar LSI devices appeared in the form of large memories, microprocessors, and random logic circuits.

A large number of LSI technologies are being developed today. Although this report is concerned with bipol[illegible] injection logic, it is useful to give an overview of LSI technolog[illegible]t this point so that injection logic can be presented in its pr[illegible]erspective.

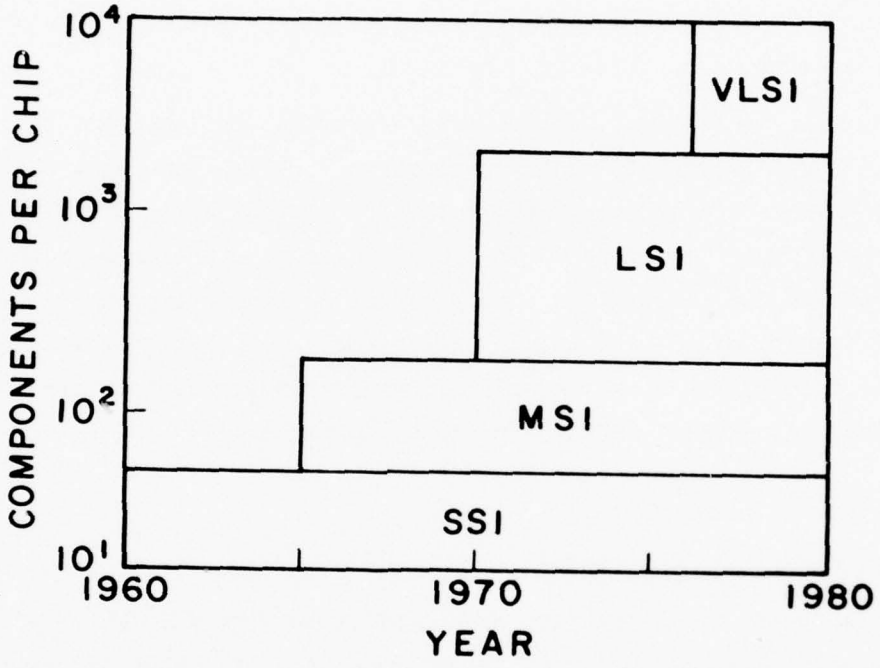


FIG. 1-2 CLASSIFICATION OF INTEGRATED CIRCUITS.

Since advances in both fabrication techniques and in circuit concepts worked together in helping the emergence of LSI, the overview will list fabrication techniques and circuit types separately.

MOS LSI (Fig. 1-3)

Fabrication: The basic building block is the MOS or MIS (metal - insulator - semiconductor) structure. The following advances in fabrication techniques are instrumental in making MOS LSI possible:

- Poly-silicon gate[10]
- Ion implantation[11]
- Heteroepitaxial growth of silicon on insulating substrates[12]
- Depletion MOS devices[13]
- Charge transfer device concepts[14]
- V-groove etching[15]
- Silicon nitride insulating layer[16]
- Double diffusion techniques[17]

Circuits: PMOS was the first commercially successful LSI technology. Its operating speed is relatively slow, in the low MHZ range. Other MOS technologies with better performance, such as NMOS,[18] CMOS (complementary MOS),[19] and CMOS/SOS (silicon on sapphire),[20] are receiving more and more attention. Several other promising MOS technologies such as DMOS[17] (double diffusion MOS), VMOS[15] and CTD[14] (charge transport devices) are also being actively developed. CTD will be covered in a companion report being prepared for this project.

Bipolar LSI (Fig. 1-4)

Fabrication: The following advances in fabrication techniques are instrumental in making bipolar LSI possible:

- Schottky barrier contacts to limit voltage swing and/or to increase speed (B75-3)
- Dielectric isolation to reduce device size and parasitic effects[12,19]
- Ion implantation to more precisely control impurities

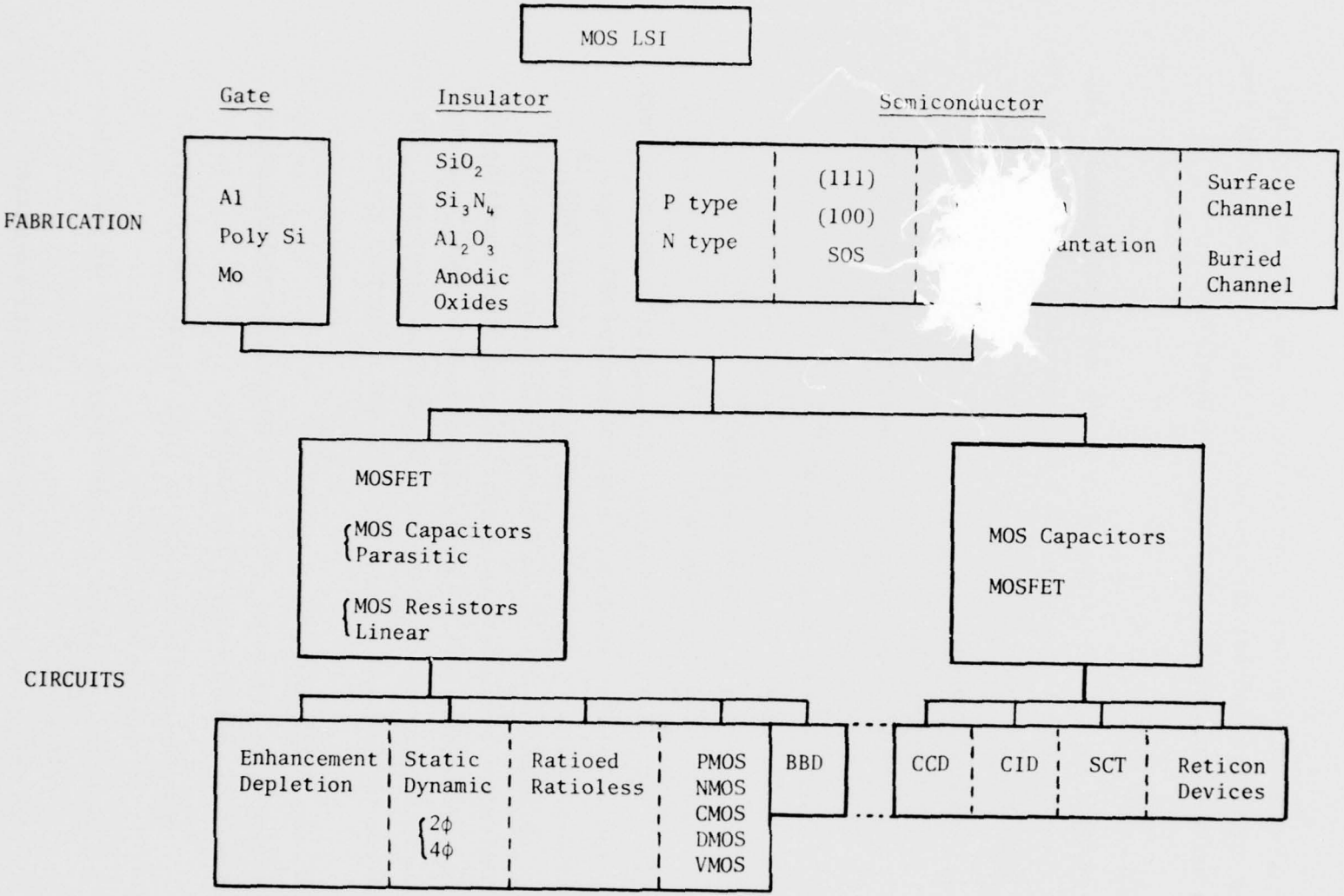


FIG. 1-3 MOS LSI TECHNOLOGIES

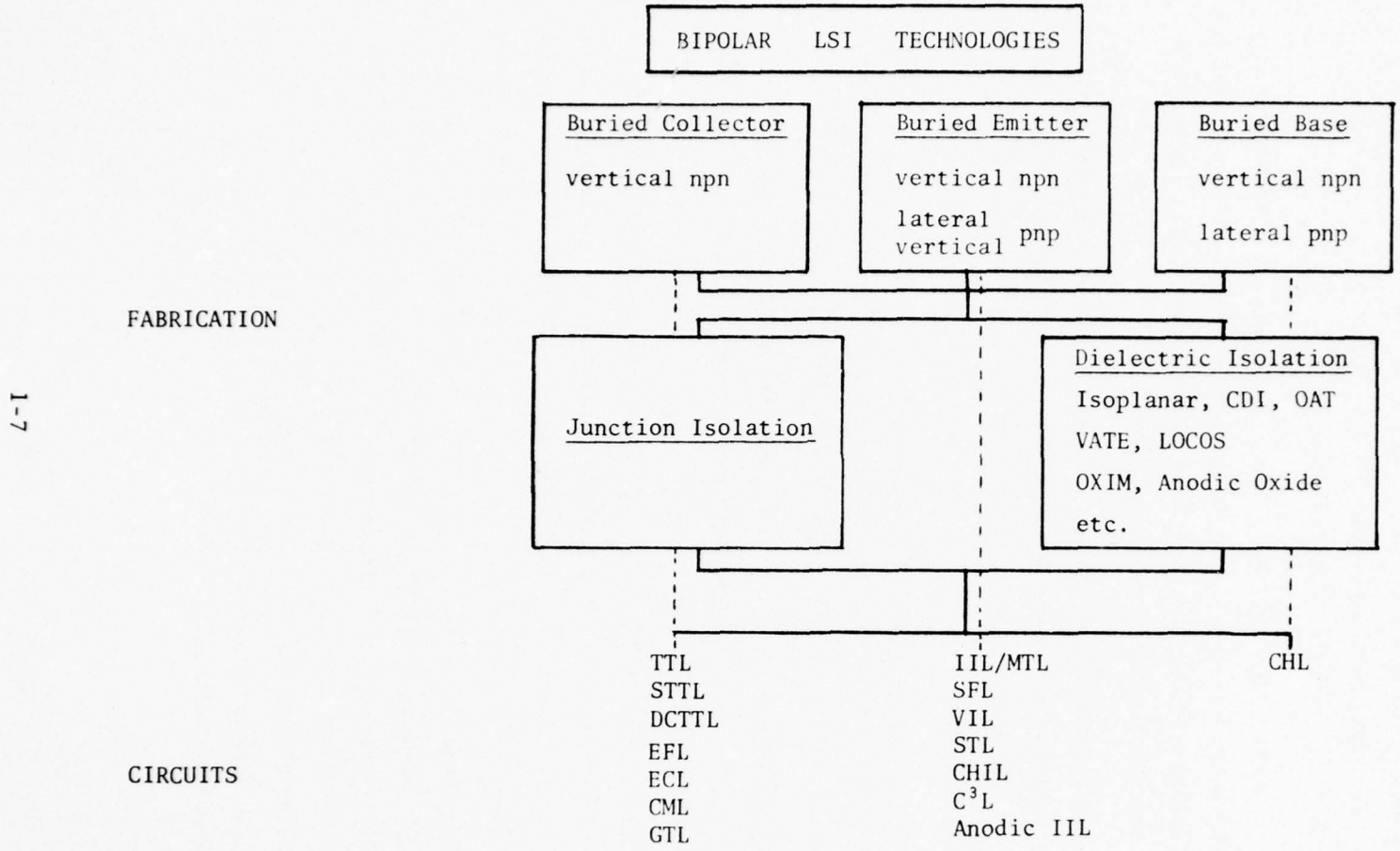


FIG. 1-4 BIPOLAR LSI TECHNOLOGIES

Thin epitaxial growth of silicon (few microns or less) to help the reduction of device size

Triple diffusion process without a buried layer to simplify fabrication and to increase yield

pnp transistors as current sources

Circuits: Conventional bipolar IC's use vertical npn transistors with buried collectors. New ways of simultaneously making both pnp transistors and npn transistors have led to several new bipolar LSI circuits. The following are some outstanding examples.

The family of bipolar injection logic circuits uses pnp transistors as current sources and vertical npn transistors as drivers (and also for switching). Furthermore, the npn transistors are inverted because their collectors are on top and the emitters are at the bottom.

Emitter follower logic circuits are fabricated by a 3D (triple diffusion) process and consists of vertical npn transistors (without a buried collector layer) and adjacent pnp transistors.

Current hogging logic circuits consist of lateral npn and pnp transistors with a heavily doped n+ layer under the device functioning as the buried base.

For these bipolar LSI logic circuits, the device structure will be different depending on whether junction isolation or dielectric isolation is used. Several dielectric isolation techniques have been developed under different names:

Isoplanar[21]

CDI (collector diffusion isolation)[22]

OAT (oxide aligned transistor)[23]

V-ATE (vertical anisotropic etch)[24]

LOCOS (local oxidation of silicon)[25]

OXIM (oxide isolated monolithic)[26]

Anodized silicon[27]

etc.

It should be recognized that the use of silicon nitride as an oxidation mask to enable selective oxidation of silicon is most instrumental in making dielectric isolation practical.[16]

1.2.2 Trade-Offs in LSI Performance

How good an LSI technology is depends on many factors. Some important ones are listed in Table I-1 and separated into three categories:

Fabrication complexity
Operation and performance
Cost

It is obvious that they can not all be accomplished simultaneously. Trade-offs must be made. Some are listed below.

Trade-Offs	
Cost ----------	Performance
Fabrication Complexity ------	Yield
Chip Size, Chip Complexity --	Yield Power Dissipation Cooling Ease of Test
Speed (or Delay) ----------	Power Dissipation Cooling

One of the most frequently considered trade-offs is "Speed versus Power Dissipation". It is commonly expressed by two figures of merit:

"Speed-Power" product (or clock frequency-power) in units of Hz-watt

"Delay-Power" product in units of second-watt or joule.

It can also be displayed graphically by a log-log plot as shown in Fig. 1-5, which presents the gate propagation delay as a function of

TABLE I-1. FACTORS DETERMINING QUALITY OF LSI TECHNOLOGY

Fabrication Complexity	Epitaxial layer Number of masks Number of diffusions and ion implantations Number of metal layers or gate layers Packaging methods
Performance and Operation	Speed and delay Power dissipation Fan in and fan out capability Noise immunity Power supply requirements: voltage, current levels, regulation Ease of interface with other circuits Driving capability Temperature range and cooling requirements Radiation hardness
Cost	Initial cost: Device size, chip density or complexity Fabrication complexity and yield Ease of packaging and test Life cycle cost: Reliability

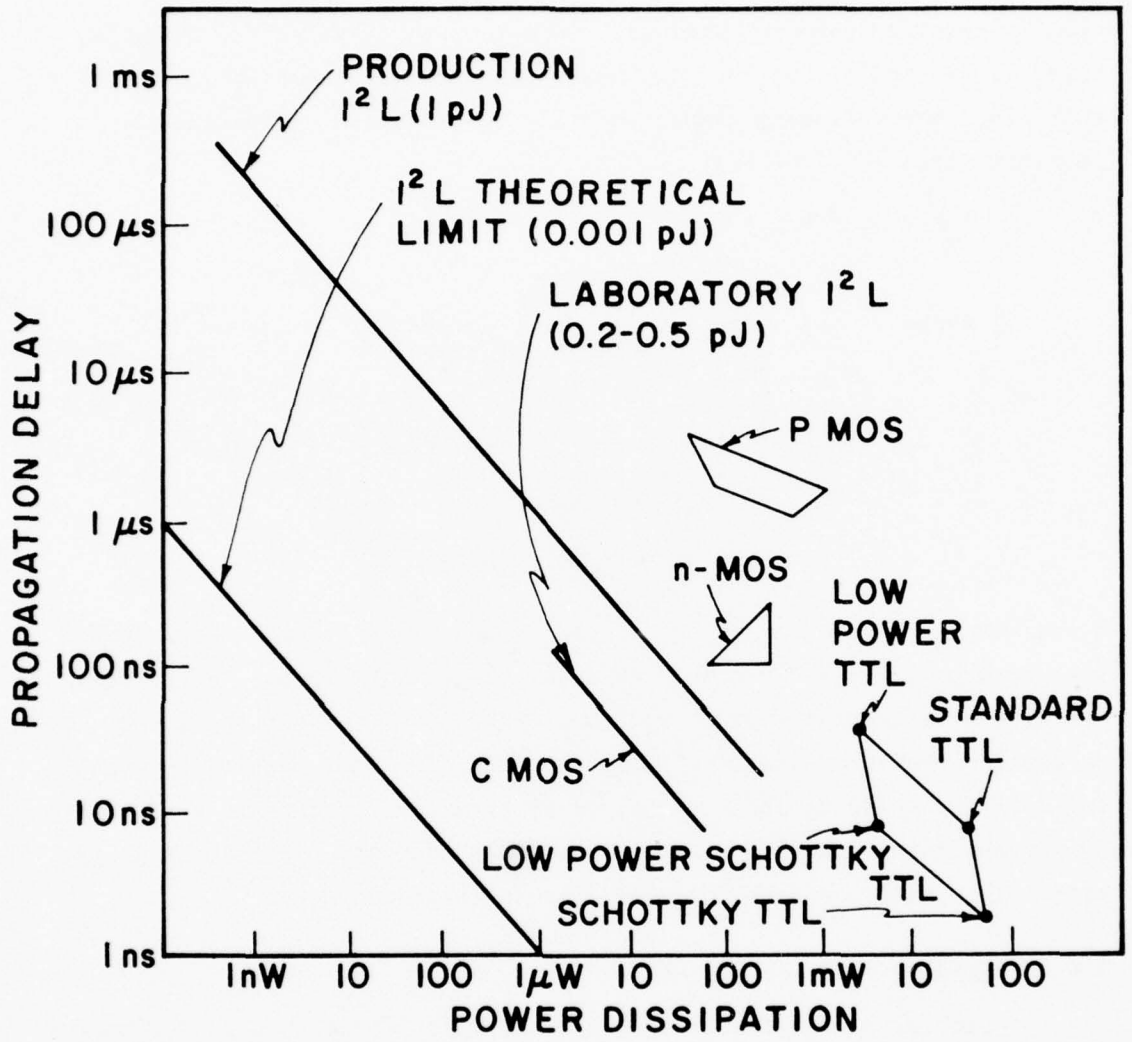


FIG. 1-5 COMPARATIVE GATE PROPAGATION DELAY VERSUS POWER DISSIPATION. (H75-1)

power dissipation. Theoretical calculation of these figures of merit usually requires computer analysis. However, in cases where the device speed is limited by the charging and discharging of capacitance during switching, the following simple relation is useful in expressing the important trade-off considerations:

$$t_d P \simeq \Delta V \cdot V_{DC} \cdot C_T$$

where t_d = gate propagation delay

P = power consumption

ΔV = logic swing between "0" and "1" states

V_{DC} = supply voltage

C_T = total gate capacitance.

A smaller $t_d P$ product means better performance. It is clear that it will take more power to achieve shorter delay (i.e., more speed). A reduction of $t_d P$ can be accomplished by reducing ΔV, V_{DC} and C_T. It should be recognized that this relation is not accurate for some bipolar IC circuits if the build-up and the removal of minority carriers in a transistor during switching contribute significantly to the gate propagation delay time. They have not been included in this relation.

1.2.3 Emergence of Bipolar LSI

Bipolar IC's were originally not a major force in LSI development because the circuits were more complex and dissipated more power. Also, the junction isolations and large diffused resistors used in the conventional bipolar circuits required large chip area and hence did not lend themselves to LSI implementation. MOS LSI was first developed because it did not need large area for isolation and diffused resistors. However, solutions to overcome the bipolar limitations have been developed. Some are indicated in Table I-2. It can be seen that bipolar LSI is being developed in two directions.

TABLE I-2 FACTORS AFFECTING LSI DEVELOPMENTS

MOS IC	BIPOLAR IC	
	Limitations of SBC Structure	LSI Solutions
Two-dimensional structure	Three-dimensional structure	
Isolation is not needed for enhancement mode devices. Device is smaller.	Isolations are needed in all three directions around every device. Device is larger.	Use dielectric isolation. Use MTL concept to eliminate the need of isolation between devices in a logic cell.
MOSFET resistors are used. Their values are high.	Diffused resistors are used. Their values are low. Large area is needed if high resistance is used to limit power.	Use ion implantation to yield higher surface resistance. Reduce the need of resistors using new circuit concept. Use I^2L concept to inject switching current and eliminate the need of large resistors.
Current level and power dissipations are low	Current level and power dissipations are higher.	Use Schottky barrier diodes to limit logic swing.

In one direction, the improvements are mainly in fabrication techniques and in device structures; the circuit concepts are basically the same as used in SSI and MSI bipolar IC's. In some cases, logic swing has been reduced to save power. Some examples are Schottky TTL, low level differential ECL, and others. The following improvements are important for their growth into the LSI domain.

First, line resolution in masks has been steadily decreased from 0.5 mil (≃ 13μ) in typical SSI to 0.3 - 0.4 mil (≃7 - 10μ) in MSI to 0.2 mil (≃ 5μ) commonly used today in LSI processing. Second, ion implantation is used more frequently to fabricate resistors. Its advantages are higher and more accurately controlled surface resistance values, less temperature drift and higher frequency performance. Third, dielectric isolation is used which not only reduces the device size and increases the circuit complexity but also increases the speed because parasitic capacitances are reduced. Fourth, a thin epi-layer is sometimes used which generally reduces size and parasitic capacitances.

Using these innovations, much progress has been made in pushing bipolar IC's into the LSI domain, as witnessed by the marketing of Schottky TTL RAM's and microprocessors, ECL 10K modules, etc. However, the need for resistors and isolation in these bipolar circuits still poses a fundamental limitation in reaching ultimate LSI achievements in size, complexity, speed and cost.

Consequently, several developments in a different direction are significant. They all employ new device structures and/or new circuits which reduce, if not totally eliminate, the need for device isolation and resistors. One such development is the bipolar injection logic family. Its highlights will be presented in the next section.

1.3 BIPOLAR LSI INJECTION LOGIC

1.3.1 Family of Bipolar Injection Logic Circuits

Bipolar injection logic now has a family of eight different circuits. The original version was first reported in 1971. It was called

integrated injection logic (IIL) by Philips of the Netherlands and merged transistor logic (MTL) by IBM of West Germany. Although called different names, their device structures and circuit concepts are the same. The original circuit has now been modified to improve performance. Seven new modifications are now being developed with the following names:

SI^2L -- Schottky I^2L (H75-3)
SFL -- Substrate Fed Logic (B74-4)
STL -- Schottky Transistor Logic (B75-1)
CHIL -- Current Hogging Injection Logic (M75-1)
C^3L -- Complementary Constant Current Logic (P75-2)
VIL -- Vertical Injection Logic (N75-1)
S^2L -- Self-Aligned Superinjection Logic (T76-1)

They include the following innovations:

a. Use of Schottky diodes either for decoupling of several outputs on the same gate or for clamping of voltage levels.

b. Use of different current injection schemes (SFL, CHIL, VIL).

c. Use of different isolation techniques.

1.3.2 Basic Concepts of Digital I^2L/MTL Circuits

Basic Cell--Inverter

The basic I^2L/MTL cell is an inverter consisting of one pnp and one npn transistor. Its circuit representation and cross-sectional view are shown in Fig. 1-6. It eliminates the fundamental limitations of conventional bipolar IC circuits--space consuming resistors and isolation because resistors are not needed to control the switching current from a d.c. voltage source. Instead, the pnp transistor is used as an active current source to switch the npn transistor. The name "Integrated Injection Logic" refers to this unusual feature. Although pnp and npn transistors are shown separately in the circuit representation (Fig. 1-6(b)), in reality they are fabricated together as shown in Fig. 1-6(a). The diffused p region serves both as the base of npn and the collector of pnp transistors. The n+ epi-layer (or n+ substrate) serves both as the

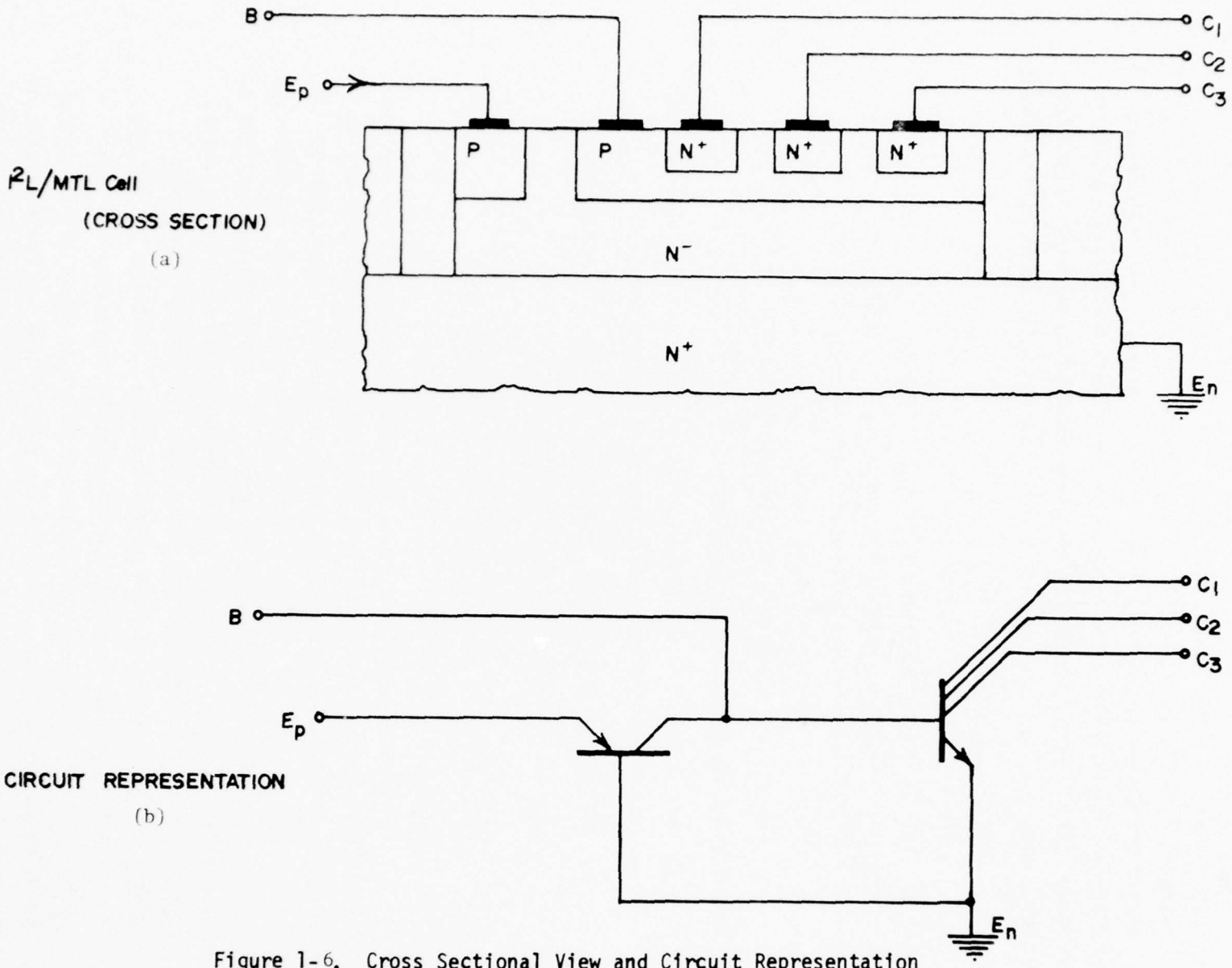


Figure 1-6. Cross Sectional View and Circuit Representation of a Basic I^2L/MTL Cell

emitter of npn and the base of pnp transistors. Therefore, these two transistors can not and need not be isolated. The name "Merged Transistor Logic" refers to this second outstanding feature. It should be understood, however, that complex I^2L/MTL circuits are usually not built by simply combining this type of unisolated basic cell. Although isolation is not needed for every cell, another form of isolation, known as "isolation collar" or "guard ring" is often used around parts of a circuit to prevent the vertical current flow in npn transistors from spreading laterally to neighboring devices. This improves the speed and speed-power product of the circuit.

Logic Implementation

Logic operation of an I^2L/MTL circuit can be explained by comparing its NAND gate with a TTL NAND gate. They are both shown in Fig. 1-7. The TTL gate requires 4 transistors, 1 diode and 4 resistors with all the isolations and metal interconnects. On the other hand, the I^2L/MTL NAND gate is obtained by simply tying two inputs to the base of an inverter. From the circuit operation viewpoint, both types of gate can be separated into three sections:

(1) Current Control Section -- Switching current in the TTL gate is set by the resistor connected to the voltage supply V_{cc}. In the I^2L/MTL gate, the switching current is fed from an external current source by way of the pnp transistor. No internal resistor is needed.

(2) Output Section -- Output section of a typical TTL gate consists of a totem pole circuit and a driving transistor which makes the transfer characteristics more abrupt. The I^2L/MTL gate uses the simple multiple-collector npn transistor as the output. A "NOT" operation is performed by the output section.

(3) Logic Section -- TTL gates perform the AND logic at the multiple emitter input transistor. When both inputs are high, the switching current is steered toward the output circuit and turns on the output transistor. On the other hand, when any one or more of the inputs is low, the switching current is steered away from the output circuit and

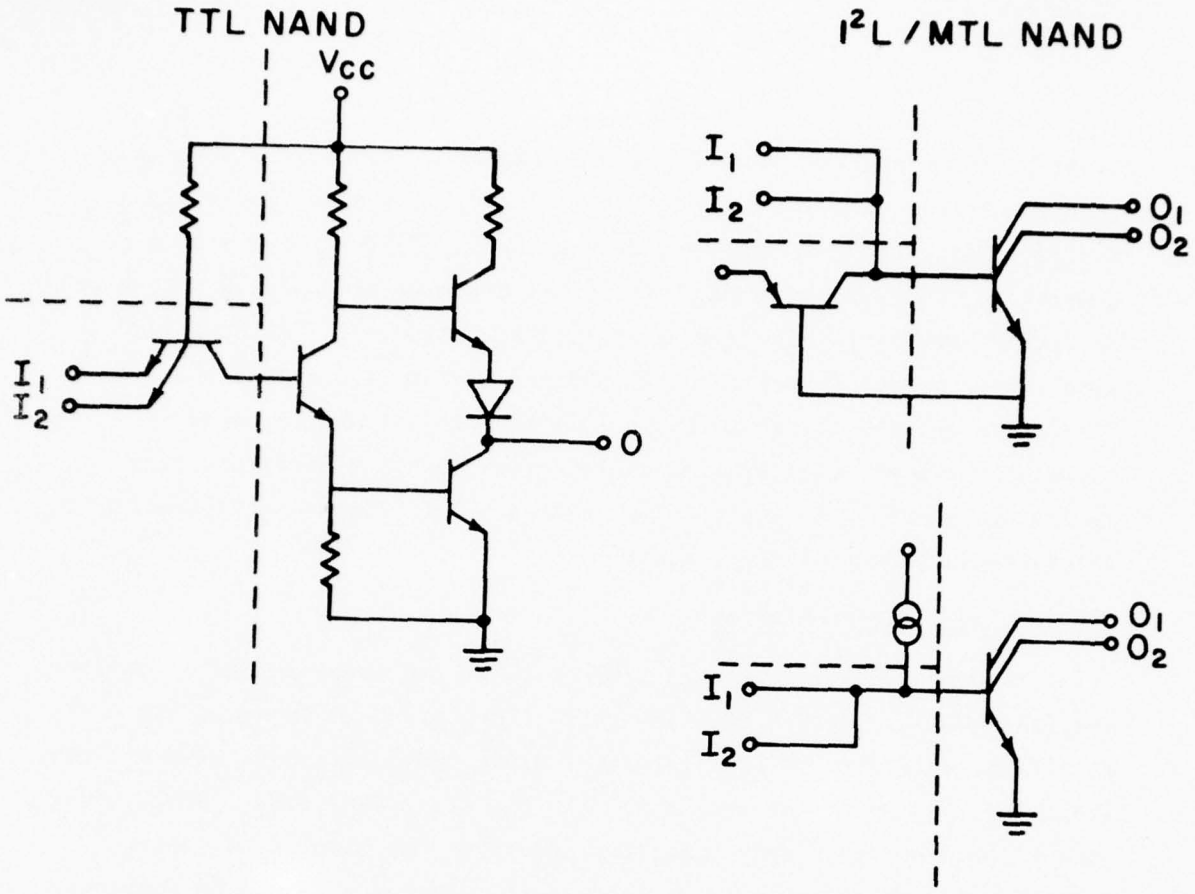


Fig. 1-7 A Comparison of TTL and I^2L/MTL NAND Gates.

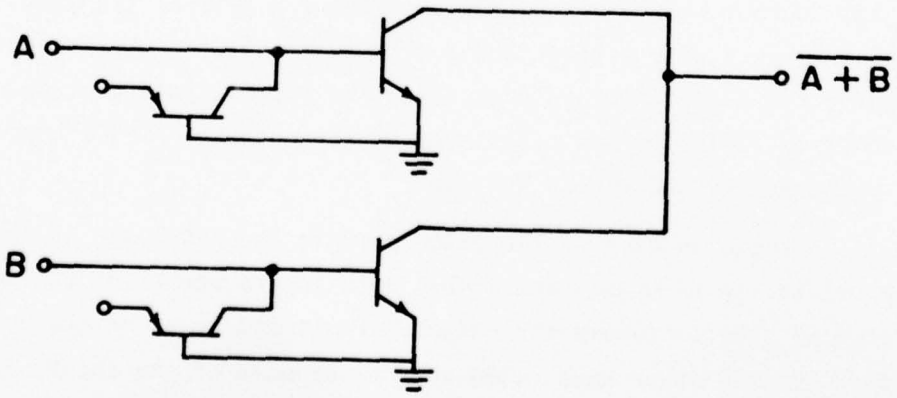


Fig. 1-8 An I^2L/MTL NOR Gate.

cuts off the output transistor. In I^2L/MTL gates, the same action of current steering takes place except that the output circuit uses only one transistor. The whole gate consists of two transistors. In reality, they are merged together and occupy an area of approximately only one normal transistor.

A "NOR" gate can be easily implemented by connecting the collectors of two inverters together in what is sometimes known as the "wired NOR" connection, as shown in Fig. 1-8. In this case, logic is performed at the output.

Using these three basic gates: Inverter, NAND and NOR, complex logic circuits can be implemented. Some examples will be given in the next chapter. Great space saving in circuit layout has been achieved not only because isolations and resistors are no longer used but also due to another unique feature. It is a consequence of the inverted npn structure. In bipolar circuits, emitters are often tied together to ground. When the usual buried collector structure is used, emitters are on top. A metal ground line on the surface of IC chip must be provided for emitter interconnects. However, when the inverted npn structure is used, as in I^2L/MTL circuits, emitters are at the bottom. They are conveniently tied together by the n+ layer, thus eliminating the need for a ground line.

It is important to point out that I^2L/MTL does not have the attractive serial-parallel gating capability which is frequently used in MOS circuits for very efficient implementation of complex logic. Therefore, in some cases, even when I^2L/MTL has smaller device size than some other technologies, e.g., NMOS, its logic gate density may not be higher. One of the new versions of injection logic, CHIL (current hogging injection logic), uses a circuit which has two pnp transistors in the current injection path. Consequently, several inputs can be added for serial gating. This enables the application of serial-parallel gating in logic implementation in this version.

Electrical Performance I -- Static

Although I^2L/MTL circuits can be analyzed from the voltage viewpoint, it is convenient to discuss its electrical operation from current considerations.

Electrical power is supplied to an I^2L/MTL circuit from a current injector rail which serves as the common emitters of many pnp transistors. npn transistors are not directly connected to the power supply. An npn collector (output) of one cell is connected to the npn base (input) of another cell, shown as the node X in Fig. 1-9. Current injected from the pnp transistor can flow in two directions, depending on the voltage level at node X. It will be steered toward the npn base in the same cell if the node voltage is high enough to turn on the npn transistor. It will flow away from this cell toward the npn collector in the previous cell if the node voltage is low corresponding to the state: npn of this cell "off," npn of the previous cell "on." Therefore, the voltage swing at X sets the logic levels of I^2L/MTL gates:

Logic "1" level V(1) is the base-emitter bias voltage of the npn transistor in saturation, $V_{BE\ Sat}$. It is typically in the range 0.6 - 0.8V.

Logic "0" level V(0) is the collector-emitter voltage of the npn transistor in saturation, $V_{CE\ Sat}$. It is typically in the range 0.02 - 0.1 volt.

This logic swing (< 0.8V) is comparable to that of ECL but is considerably smaller than the 3.5 to 5 volt swing of TTL. In Schottky Transistor Logic, Schottky diodes are used to reduce the logic swing to even smaller values, around 300-350 MV to further decrease the power consumption.

Electrical Performance II -- Dynamic

Speed and power consumption are two important dynamic properties. They are characterized by three figures of merit: gate propagation delay, t_d, power consumption P, and delay-power product, t_dP. It should be pointed out that the device used to measure the gate propagation delay

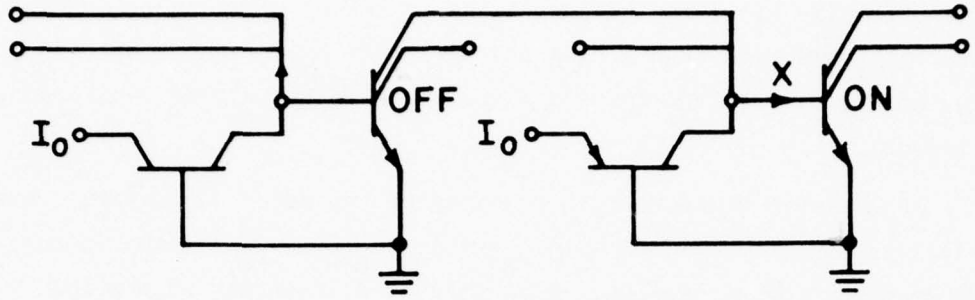


Fig. 1-9 Electrical Operation of Two Levels of I^2L/MTL Gates.

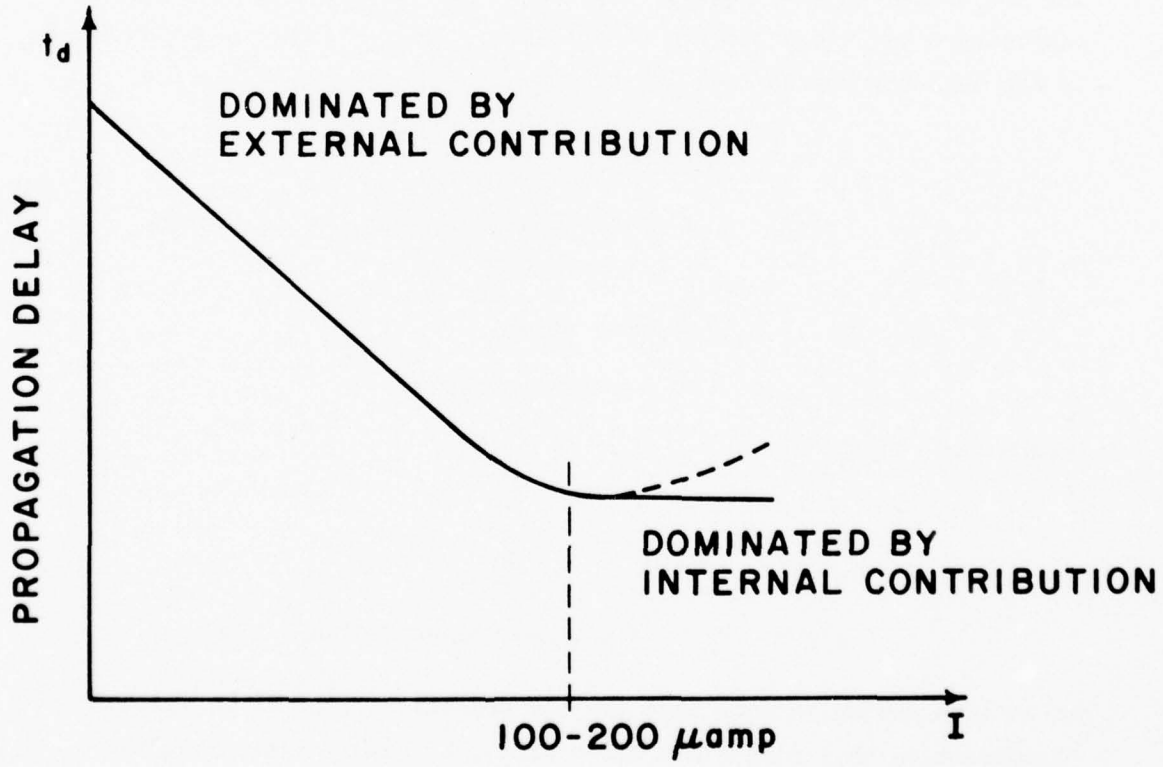


Fig. 1-10 Typical Propagation Delay Versus Injection Current.

must be carefully specified because t_d has a strong dependence on the fanout. A t_d measured from a ring counter which has a fanout of one will be different from the t_d of a flip-flop or other circuit which has more fanouts.

It has been found that t_d consists of two major components: one external and one internal, $t_d = t_{d\ ext} + t_{d\ int}$. They dominate in different injector current ranges. $t_{d\ ext}$ is more important in the low injector current range and is inversely proportional to current. $t_{d\ int}$ dominates in the high injector current range and is generally independent of current. A typical t_d vs I relation is shown in Fig. 1-10.

In low ranges of I, t_d can be as long as several milliseconds. It is dominated by the external component which is caused by the charging and discharging of circuit capacitances including both the device capacitance and the parasitic capacitance. It is inversely proportional to the injector current and can be approximated by the expression

$$t_d = 5 \sim 10 \frac{(\Sigma C)\Delta V}{I}$$

where ΣC = total capacitance, typically around 1 pF or less.

ΔV = logic swing

I = injection current

Under this condition:

$$P = V I$$

$$t_d P = 5 \sim 10(\Sigma C) \cdot V_{DC} \cdot \Delta V$$

where V_{DC} = d.c. power supply voltage $\simeq \Delta V$.

It is interesting to note that the $t_d P$ product of I^2L/MTL is independent of current in this range. In other words, by simply increasing the injector current I, the device can be made to operate faster (smaller t_d) but with accompanying increase of power consumption in such a way that

the $t_d P$ product remains constant. This will continue up to a certain current range when $t_{d\ ext}$ no longer dominates the gate propagation delay.

In this range, $t_{d\ int}$ starts to become an appreciable part of the total propagation delay. Its mechanism is the build-up and the removal of minority carriers in the npn transistor. Eventually, when I is large enough, $t_{d\ ext}$ is so small that the propagation delay t_d is essentially $t_{d\ int}$. Under these conditions, the propagation delay will stay constant. Speed cannot be improved by increasing the injector current. The delay-power product will deteriorate (increase) in the medium current range which typically lies above 100-200 μamp.

In some cases, the propagation delay could even increase in the high current range for two reasons. First, the series resistance of the base prevents fast charging and discharging. Second, these charges increase more than linearly with increasing currents.

The fact that the speed and power consumption can be adjusted to perform at different levels by simply changing the injector current offers a unique advantage of I^2L/MTL to optimize the speed-power trade-off. In many complex IC circuits, high speed performance is needed only in certain parts of the circuit. Using I^2L/MTL, optimal speed-power performance can be achieved by supplying large injector current where high speed is needed and reducing the current level elsewhere according to the speed requirement.

1.3.3 Combined Analog/Digital Circuits on One Chip

Probably due to the relatively limited driving capability and low frequency performance of MOS circuits, analog IC's have been dominately a bipolar technology. In recent years, JFET and MOSFET circuits are being used more frequently at the front end of analog circuits where their low noise and high impedance characteristics can be used to advantage.

On the other hand, until the recent emergence of digital bipolar LSI's, large scale digital circuits such as big memories and microprocessors have been mainly MOS LSI devices.

There have always been many applications which can be benefitted by having analog and digital circuits on the same chip. The answer heretofore has been in combining MOS digital circuits and bipolar analog circuits on the same chip although their processing requirements are quite different. Now, I^2L/MTL digital circuits are as good as NMOS circuits in speed, packing density and power dissipation. Furthermore, good performance I^2L/MTL circuits can be made by using the standard processing steps for analog circuits. It is obvious that the new bipolar injection logics offer a natural solution to the desire of combining analog and digital circuits on the same chip, using the same processing steps.

Looking ahead, bipolar injection digital circuits will have to compete with several other bipolar LSI and MOS LSI digital circuits in performance and cost. However, the combined analog/digital circuits using injection logic offers solutions which have no other strong alternative at this time.

It should be noted, however, that the new Gold Transistor Logic[29] (GTL) reported by Nippon Electric Co. of Japan may become a competitor for the combined analog/digital applications. It was reported that GTL possesses packing densities and delay power products comparable to today's I^2L but operates five times faster. Furthermore, the GTL process can be applied to fabricate the standard bipolar IC families--TTL, ECL, etc.

1.3.4 Brief Chronology of Developments

Only five years after their first announcement, bipolar injection logic has already been accepted by the industry as a major force in bipolar LSI development. Many companies are pouring efforts into its development, a few openly, most with little publicity. Because of the competitive nature of the commercial market, only a small fraction of the development activities has been publicized. In many cases, only brief hints are given. However, an attempt was made to collect the bits and pieces of information available in technical journals, reports,

marketing projections and private communications. The result is Table I-3 which presents the publicized bipolar injection developments since 1971. They are separated into three categories.

First category is the device structure. It is noted that eight different versions of bipolar injection logic are currently being developed. Their circuit representations and cross-sectional views are shown in Fig. 1-11.

I^2L/MTL	
Schottky I^2L	(H75-3)
SFL	(B74-4)
STL	(B75-1)
CHIL	(M75-1)
C^3L	(P75-2)
VIL	(N75-1)
S^2L	(T76-1)

Each structure can be further divided into two types, depending on whether junction collar or dielectric collar is used. The physical layout and cross-section will be described in more detail in Chapter II.

Second category is the device physics and circuit studies. It was found that most of these studies considered only the original version of I^2L/MTL device structure. Effects due to Schottky diode decoupling or clamping, dielectric collar and/or doping profile control by ion implantation have not been investigated in these theoretical studies. They can be separated into four groups.

In the first group, transistor characteristics are studied. They are needed because both the pnp current injector and the inverted npn switch transistor were not used in conventional bipolar IC and have not been well analyzed.

In the second group, device physics of the basic I^2L/MTL cell are studied. They are "phenomenological" studies. The cell performance is investigated as to its dependence on physical layout, material parameters, operating conditions and so on. The results are presented

TABLE I-3 CHRONOLOGY OF PUBLICIZED ACTIVITIES IN BIPOLAR INJECTION LOGIC DEVELOPMENTS

YEAR	DEVICE STRUCTURES	DEVICE PHYSICS, AND CIRCUITS STUDIES	APPLICATIONS DEVELOPMENT
1971	I^2L/MTL (integrated-injection logic) (merged-transistor logic) 4-5 mask technology		IBM/Germany Basic memory cell
1972	Oxide isolation		IBM/Germany 7 stage inverter, 3 bit decoder, half adder, voltage clamp Philips 256 bit shift register frequency divider for electronic organ tone generator 7 segment decoder for LCD driver 4 decade counter for digital voltmeter small calculator 108 bit shift register 1536 bit ROM control logic
1973			IBM/Germany 4 x 8 bit RAM Speculation on 16 kilobit RAM (oxide isolation, self aligned n+)
1974	Combined digital and analog circuits (7-9 mask technology) SFL (Plessey) (substrate-fed logic)	Current injection from 3 sides (0.13 pJ) Proposal of ion implementation of base layer of npn transistor (1.5 ns) delay predicted). Study the effects of isolation on the current gains of inverted npn transistor Shallow diffusion (7 ns) Equivalent circuits and modeling terminal oriented model structure oriented model lumped model	Northrop Frequency synthesizer (3 bit input, 10 bit output) 36 bit ROM, PS master-slave flip-flop 3 bit adder Philips 2^{19} bit counter, memory, shift registers, random logic, 5 bit D/A converter RTC - La Radio Technique Compelec 8 bit word parallel processing microprocessor TI Logic modules for digital watch with LED display First generation microprocessor

TABLE I-3 (Continued)

YEAR	DEVICE STRUCTURES	DEVICE PHYSICS, AND CIRCUITS STUDIES	APPLICATIONS DEVELOPMENT
1975	STL (IBM/Germany) (Schottky-transistor logic) CHIL (Siemans) (current hogging injection logic) C^3L (Motorola) (complementary constant current logic) VIL (Mitsubishi) (vertical injection logic) SI^2L (Bell Telephone Lab) (Schottky I^2L) Anodic I^2L (ITT Semiconductors)	Radiation effect studies: Gamma radiation Neutrons Phenomenological theory for pnp and npn transistor and one standard structure I^2K cell	Bell Telephone Laboratory Schottky I^2L technology development Telephone application Exar Integrated Systems Digital watch module Digital-linear circuits Fairchild 4 kilobit RAM, microprocessor Intermetall Character generator & checker Electronic organ, alarm clocks IT&T Semiconductors Digital watch modules Mitsubishi 8-16 bit microprocessor, digital watch, 4 kilobit 16 kilobit RAM, D/A, A/D interface circuits Motorola 8 bit Microprocessor, peripheral, interface circuits, auto radio tuner, clock 8 x 8 Multiplier, direct memory access controller, programmable delay module National Semiconductors Digital watch module Philips Electronic organ IC (ECL, I^2L combination) 19 dividers by two Plessey 225 gate programmable pseudo-random sequence generator, quad decade counter, 256 bit RAM RCA digital-linear circuits, A/D and D/A converters, television, time keeping, instrumentation and automotive applications Sharp electrochronic display driver, microprocessor, digital watch chip

YEAR	DEVICE STRUCTURE	DEVICE PHYSICS, AND CIRCUITS STUDIES	APPLICATIONS DEVELOPMENT
1975 (cont)			Signetics FIFO shift register, LIFO memory, 16 x 16 multiplier, microprocessor TI 4 kilobit RAM, second and third generation microprocessor (16 bits)

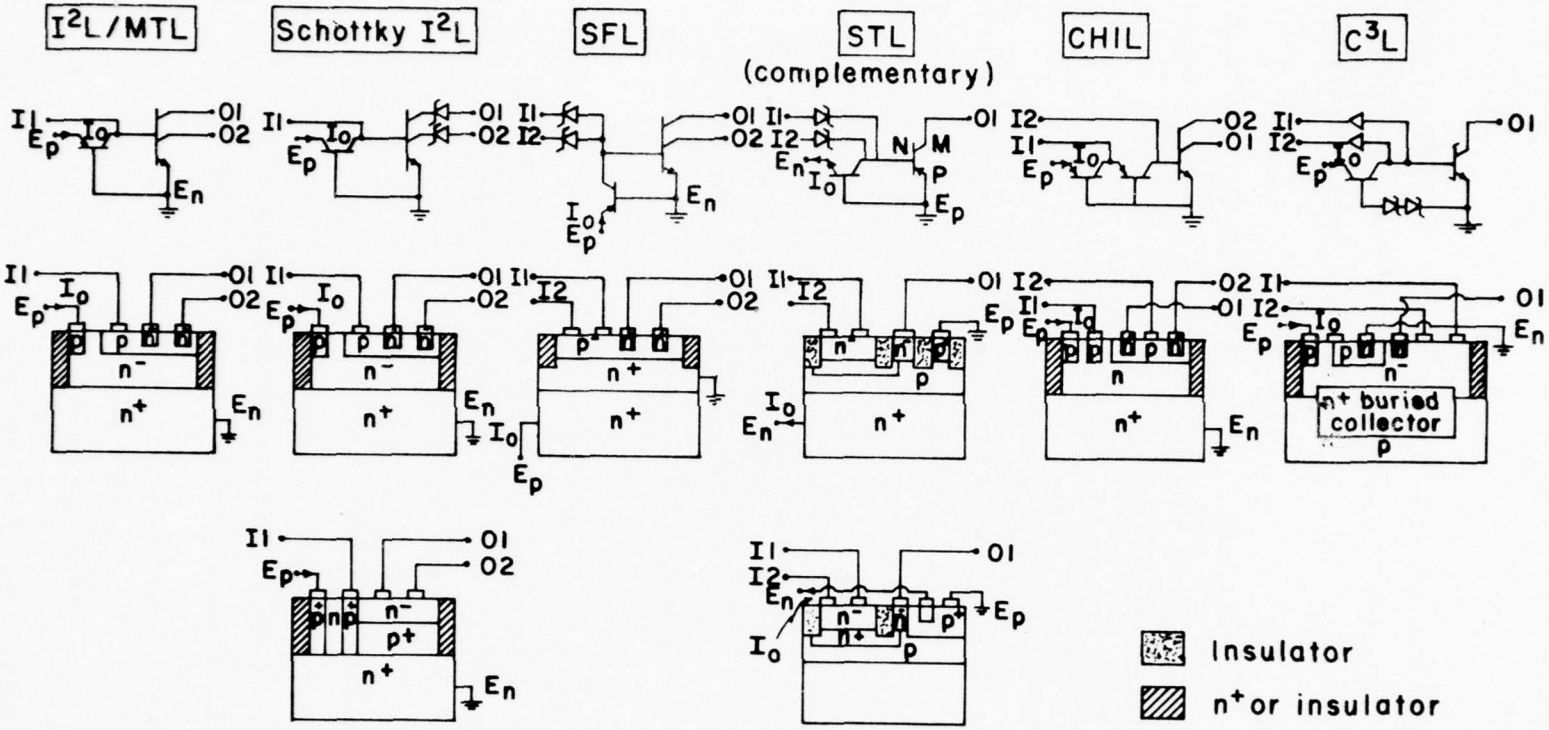


Fig. 1-11 Circuit Representations and Cross-Sectional View of Different Bipolar Injection Logic Circuits.

in relatively simple and approximate expressions. However, it is well known that in LSI circuits, the interactions among neighboring devices are appreciable and significant. Useful analysis has to depend on computer modeling.

The third group of studies is for this purpose. Equivalent circuits and modeling studies were made which can be used in computer analysis or computer-aided design.

The last group includes the rest of the studies, such as the investigation of temperature drift, radiation effects, etc.

It can be concluded that a basic understanding of the device physics, material requirements and circuit analysis has been achieved for the standard I^2L/MTL structure. However, optimal design considerations in regard to circuit layout (such as the skill in reducing the voltage drop along the current injector rail), processing control (such as the use of arsenic diffusion to avoid collector dipping, ion implantation, etc.) will have to wait for the accumulation of experience. Furthermore, the developments of improved versions of I^2L/MTL have just begun.

Third category is the application developments. It can be seen that the range of applications is very wide covering computer, instrumentation, timing device, control, automotive, entertainment, and some others which will be explored in the future.

1.3.5 Progress of Performance

Achievements of bipolar injection logic will be presented in two ways. First, the device performance is highlighted chronologically in Table I-4. Four areas of performance are presented.

Circuit Complexity -- expressed by device size in mil^2 or μ^2; chip size in mm^2 or mil^2 and/or circuit density in devices/chip.

Speed or Delay -- expressed by delay in ns.

TABLE I-4 PROGRESS OF I^2L/MTL DEVICE PERFORMANCE

YEAR	COMPANY (REFERENCE)	DEVICE	SIZE*	DELAY (nsec)	POWER CONSUMPTION (μw)	DELAY POWER PRODUCT (pJ)	REMARKS
1972	IBM/Germany (K72-1)	Single RAM cell	4 mil^2/bit	30 (write) 10 (read)	100 μa		
	(B72-1)	Inverter	100 gates/mm^2	100	35	0.35	
			1000 gates on 130x130 mil^2	20	35	0.7	
				12	100	1.2	
	Philips (K72-1)	Shift register	21 mil^2/SR 72 SR/mm	7.5 MHz (13.3 ns)	200/bit	2.66	
	(H72-2)	Inverter	200 gates/mm^2			0.4	
		Inverter	1000 gates on 160x160 mil^2			1.75	
1973	IBM/Germany (W73-1)	RAM	3.1 mil^2/bit 4x8 bits	50 (access)			
	(W73-2)	RAM	4 Kbits on 150x160 mil^2				Speculation based on standard process
		RAM	1.1 mil^2/bit 16 Kbits on 175x175 mil^2				Speculation based on improved process
1974	Northrop (A74-1)	Inverter				0.22 0.17	n+ isolation oxide isolation
	Philips (T74-1)	Inverter				1 0.25 0.13	10μ 5μ 5μ with 3 side current injection
				7	140	1	Shallow diffusion
				1.5			Speculation based on ion implanted base layer

TABLE I-4 (Continued)

YEAR	COMPANY (REFERENCE)	DEVICE	SIZE*	DELAY (nsec)	POWER CONSUMPTION (μw)	DELAY POWER PRODUCT (pJ)	REMARKS
1974 (cont)		Memory, shift register	400 bits/mm^2				
		Logic	100-200 gates/mm^2				
	Plessey (B74-2)	SFL ring oscillator	stage	100 20	0.5 100	0.05 2	
	RTC-La Radio Technique Compelec	Parallel microprocessor	8 bits 520 gates & I/O on 15 mm^2 (160x160 mil^2)	Logic: 900 Arithmetic: 1200	400 mw		
1975	TI	4 bit +Microprocessor	1,600 gates on 30,000 mil^2 with I/O	1 μsec machine cycle time	120 mw	∿1	First generation, standard I^2L structure
	Fairchild	RAM	4 K bits	100 (access time)			
	IBM/Germany (B75-1)	STL ring oscillator	7 stage	4.5	100 μa	0.07	150-350 mv logic swing
	Motorola (P75-1)	C^3L		7.5	300	2.25	
	BTL	SI^2L	Random logic 250 gates/mm^2 85 gates/mm^2	10-30		1 5μ 10μ	
	Mitsubishi	VIL		85	7.95	0.07	

* 5μ line resolution unless specified otherwise.

\+ Performance of commercial products

To convert current to power consumption, multiply current by power supply voltage (∿1 volt).

Power Dissipation -- expressed either by power in μwatt or by current in μamp (which can be converted into power if multiplied by V_{DC}, the d.c. power supply voltage).

Delay Power Product in pJ.

However, most of the performance data presented in Table I-4 are achievements in research samples and devices. Some are even from pure speculation. Therefore, they are reorganized and presented in a different way in Table I-5. In this table, achievements in production devices, in research devices and from speculation are separated.

It can be concluded that at the present time, I^2L/MTL is a moderately high packing density, low power consumption, relatively slow but very glamorous LSI technology. Its performance probably is comparable to that of NMOS. Promising speculations are ahead of real delivery of performance at this moment. Its potential seems high and will be discussed in the next section.

1.3.6 Potential and Promise

The future of injection logic can be speculated on by comparing its potential performance with that of other LSI technologies. In this section, several figures and tables comparing I^2L/MTL with other LSI technologies are reproduced. It must be emphasized that in the fast moving field of LSI, comparisons are difficult to make and are often controversial, especially when one technology is new and still on its early learning curve, such as in this case of injection logic. In articles touting injection logic, laboratory achievements are sometimes compared with performance of production line devices of other technologies. They are biased in favor of I^2L/MTL. On the other hand, when disadvantages of injection logic are being singled out, as in the question of radiation hardness, a young technology is compared with other much better developed technologies. The comparison is biased in the other direction.

TABLE I-5 STATE OF ART OF I^2L/MTL PERFORMANCE

ITEMS	PRODUCTION RESULTS*	LABORATORY RESULTS	SPECULATION
Logics			
Inverter	20 -50 ns	I^2L/MTL: 6 ns at 1 pJ (shallow diffusion 0.17 pJ (oxide isolation) 0.13 pJ (3 sides injection) SFL: 20 ns at ∿ 1 pJ 0.05 pJ at 100 ns STL: 0.07 pJ at 10-20 ns VIL: 8.8 ns at 0.07 pJ	I^2L/MTL: 1 ∿ 1.5 ns SI^2L: 1 ns 0.1 pJ VIL: 1 ns
Random Logic	1660 gates including I/O on 30,000 mil^2 chip (∿ 15-20 mil^2/gate)	250 gates/mm^2 (∿ 6.4 mil^2/gate)	
Memory (RAM)		4 kbits 400 bits/mm^2 (∿ 4 mil^2/bit)	16 kbits (∿ 1.1 mil^2/bits)
LSI Chips			
Microprocessor	1st generation--4 bits 1 μsec machine cycle time 110-530 ns operation	2nd generation--4 bits 4-5 times faster 3-4 times more complex t_dP about the same	16 bit microprocessor
Digital Watch		∿20,000 mil^2	
Electronic Organ		3.5 mm^2 (5600 mil^2)	
Multiplier		8 x 8, 16 x 16 bits	

* Based on TI 4 bit microprocessors

However, recognizing these possible pitfalls and considering only the I^2L/MTL data presented in these figures and tables, an examination in several performance areas and applications will go a long way in recognizing the potential and promise of bipolar injection logic.

(1) Cost: The price per gate of bipolar and MOS IC's is compared in Fig. 1-12, which also includes the projected decrease of price from 1975 to the early '80s. The important message in this figure is the breakaway of I^2L/MTL price from the more expensive bipolar curve to the lower priced MOS curve. It should be recognized, however, that although I^2L/MTL is a bipolar technology, its present performance is somewhere in betweeen that of bipolar TTL and commercial NMOS. In other words, even when the I^2L price catches up to the moving MOS price line, it is not achieving TTL performance at MOS prices.

(2) Device Size and Processing Complexity: The layouts of a four input (or output) gate using seven different technologies are compared in Fig. 1-13. I^2L/MTL gate is shown to be the smallest and needs the fewest fabrication steps--4 masks and 2 diffusions. However, caution must be exercised because using modern fabrication techniques such as ion implantation, double metal levels of interconnects and small scaling techniques, NMOS gate size has been much reduced. In other words, the up-to-date NMOS achievements have not been represented in this figure.

(3) Chip Complexity and Speed: The number of gates which could be packed on an LSI chip of less than 30,000 mil^2 is presented as a function of gate propagation delay in Fig. 1-14.

From the performance viewpoint, delay below 100 ns is considered bipolar LSI domain, while the slower region belongs to MOS LSI. This partition will certainly receive rebuttal from CMOS/SOS and NMOS developers. However, it is probably correct in partitioning the performance ranges for the three bipolar LSI technologies as follows:

a. 100-25 ns gate propagation delay -- This range characterizes today's I^2L/MTL performance using the conventional I^2L structure. The chip complexity is around 1,000 gates today.

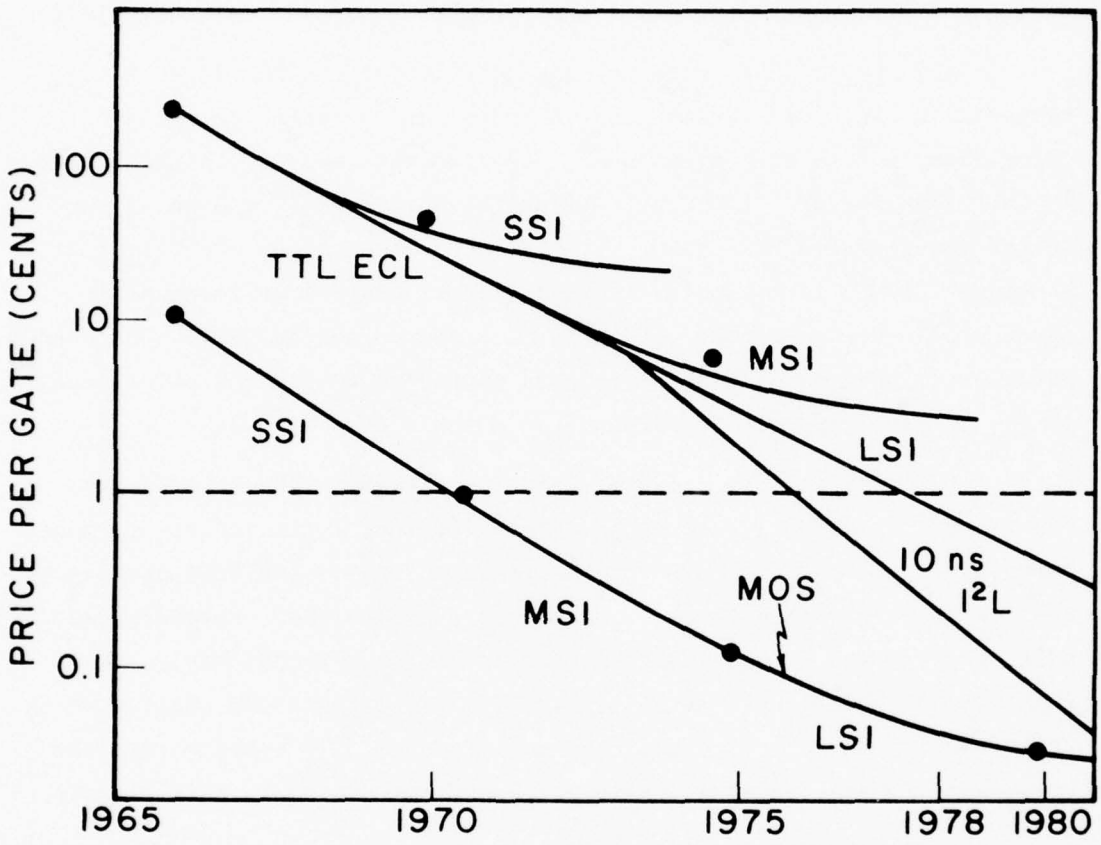


Fig. 1-12 Projected Decrease of Price Per Gate of Bipolar and MOS Integrated Circuits.

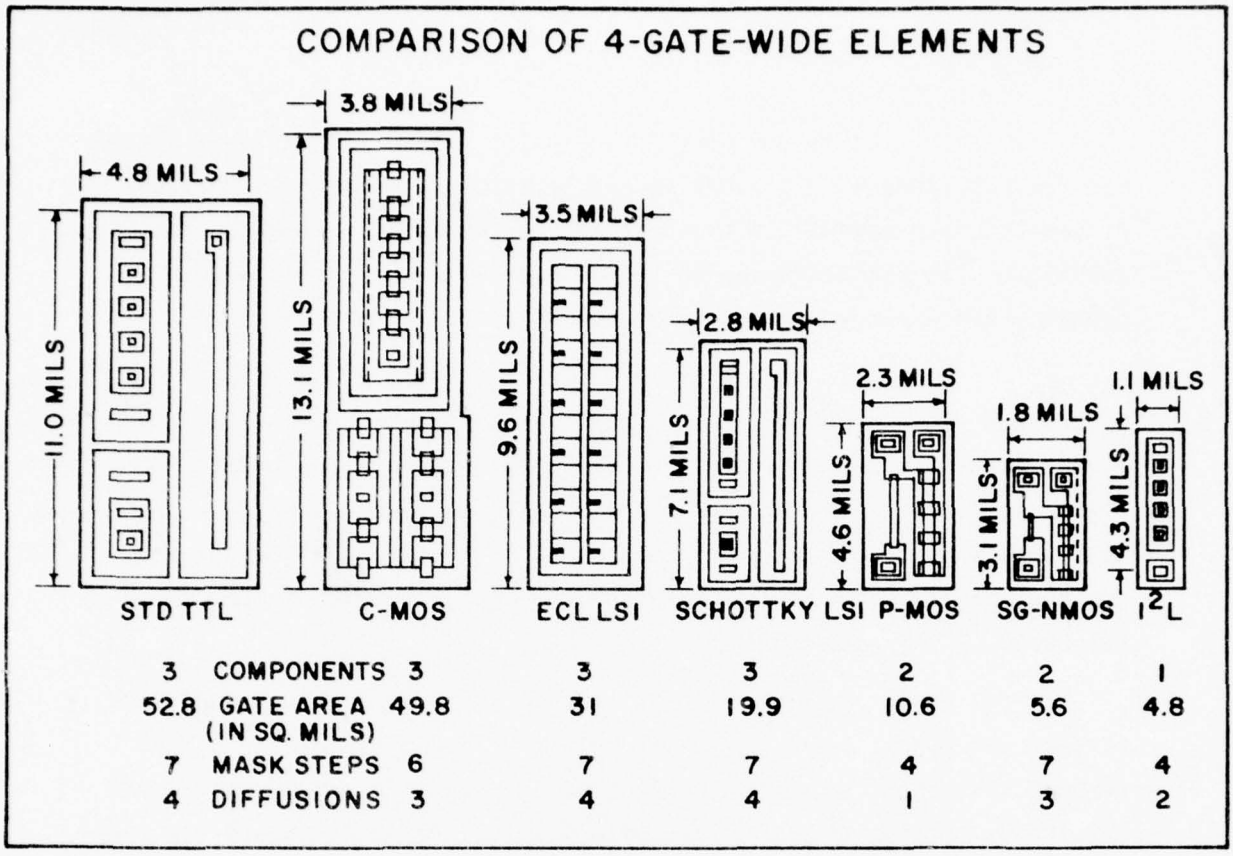


Fig. 1-13 Comparison of Layouts of a Four Inputs (or Outputs) Gate Using Seven Different IC Technologies. (H75-1)

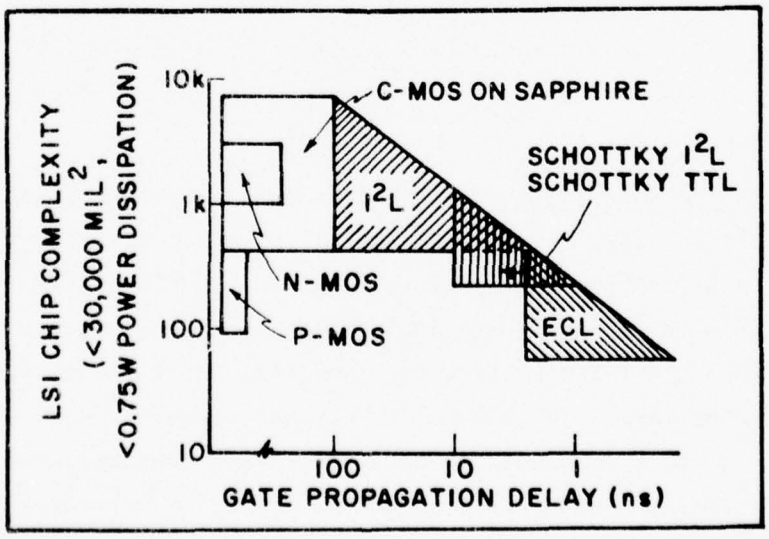


Fig. 1-14 Chip Complexity and Gate Propagation Delay of Seven LSI Technologies

b. 25-10 ns gate propagation delay -- This range is the standard TTL domain. It seems that TI's second generation I^2L microprocessor using standard I^2L structure but ion-implantation fabricating technique will achieve speed in this range. The packing density probably has already been increased to 4000-4000 gates/chip.

c. 10-1 ns gate propagation delay -- This range belongs to the ECL and some of the best Schottky TTL. Whether I^2L/MTL will ever deliver the 1-2 ns performance is pure speculation today. However, using the improved versions of I^2L/MTL circuits, several claims have been made that 2-10 ns performance is possible. They all use Schottky diodes, dielectric isolation and ion implantation to achieve the below 10 ns performance.

(4) Delay-Power Characteristics: The delay-power products of several LSI technologies have been compared in Fig. 1-5. The unique feature that speed performance and power dissipation can be traded off by simply changing the injector current is clearly demonstrated by the straight line in that figure because the t_dP product is a constant. It is interesting to note that CMOS circuits also possesses this type of characteristic. Its propagation delay can be reduced if higher drain voltage is used. In Fig. 1-15, gate propagation delay of TI's 4-bit microprocessor is presented as a function of injector current. Three generations of that product are shown in this figure. It seems that the second generation represents essentially the same process except in using smaller line resolution of 5 μ.

(5) Speed-Power Characteristics: Performance can be characterized in a different way, as shown in Fig. 1-16, which presents the power dissipation as a function of the clock frequency. NMOS, LSTTL, CMOS, CMOS/SOS and I^2L technologies are included. Speed-power can be traded-off in both CMOS and I^2L/MTL circuits. However, their trade-offs are made in different ways. In CMOS circuits, power consumption is directly proportional to clock frequency. Faster operation consumes more power. However, in I^2L/MTL circuits, as long as the injection current remains

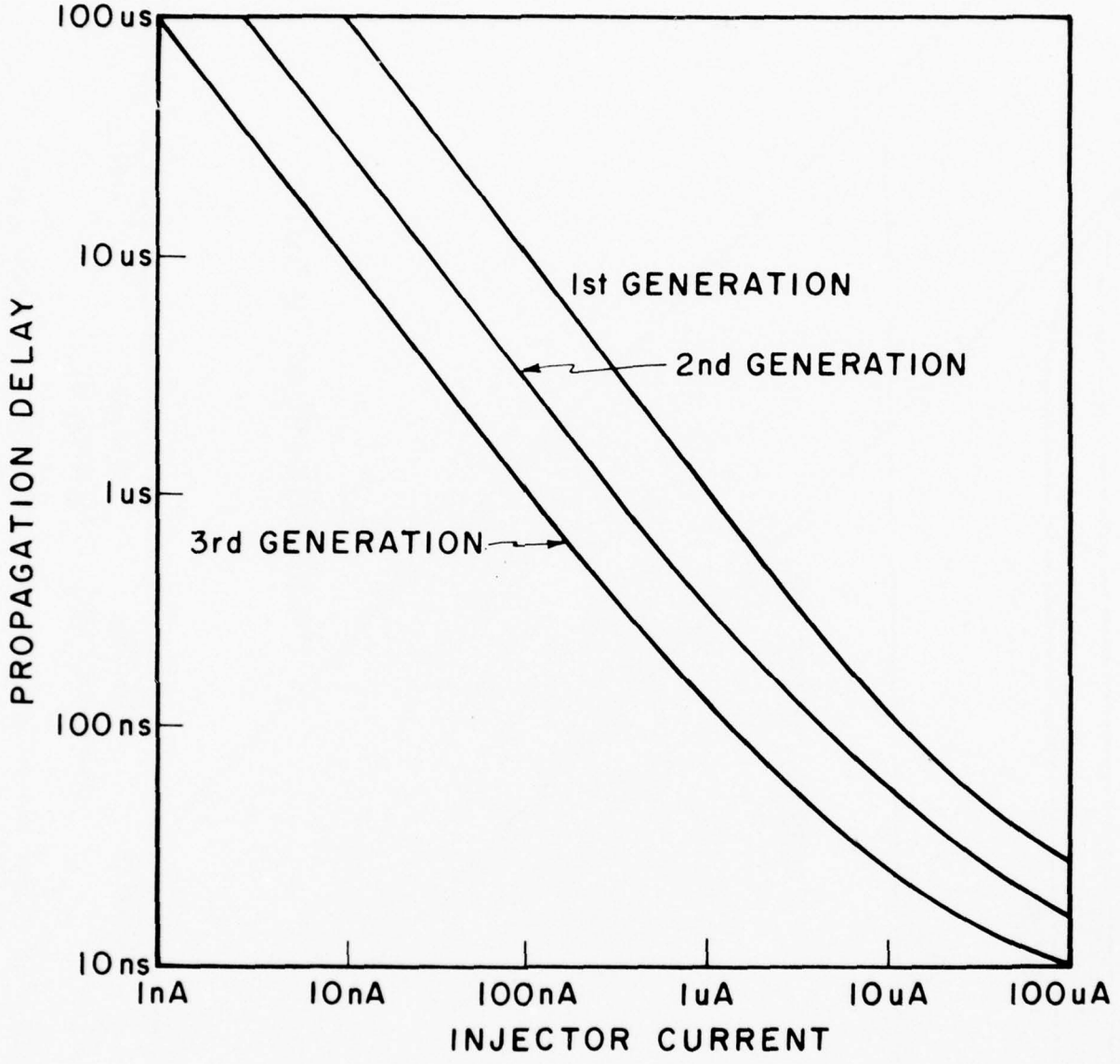


Fig. 1-15 Gate Propagation Delay and Injector Current Performance of Three Generations of Texas Instruments' 4 Bit I²L Microprocessors. (TEXAS INSTRUMENTS)

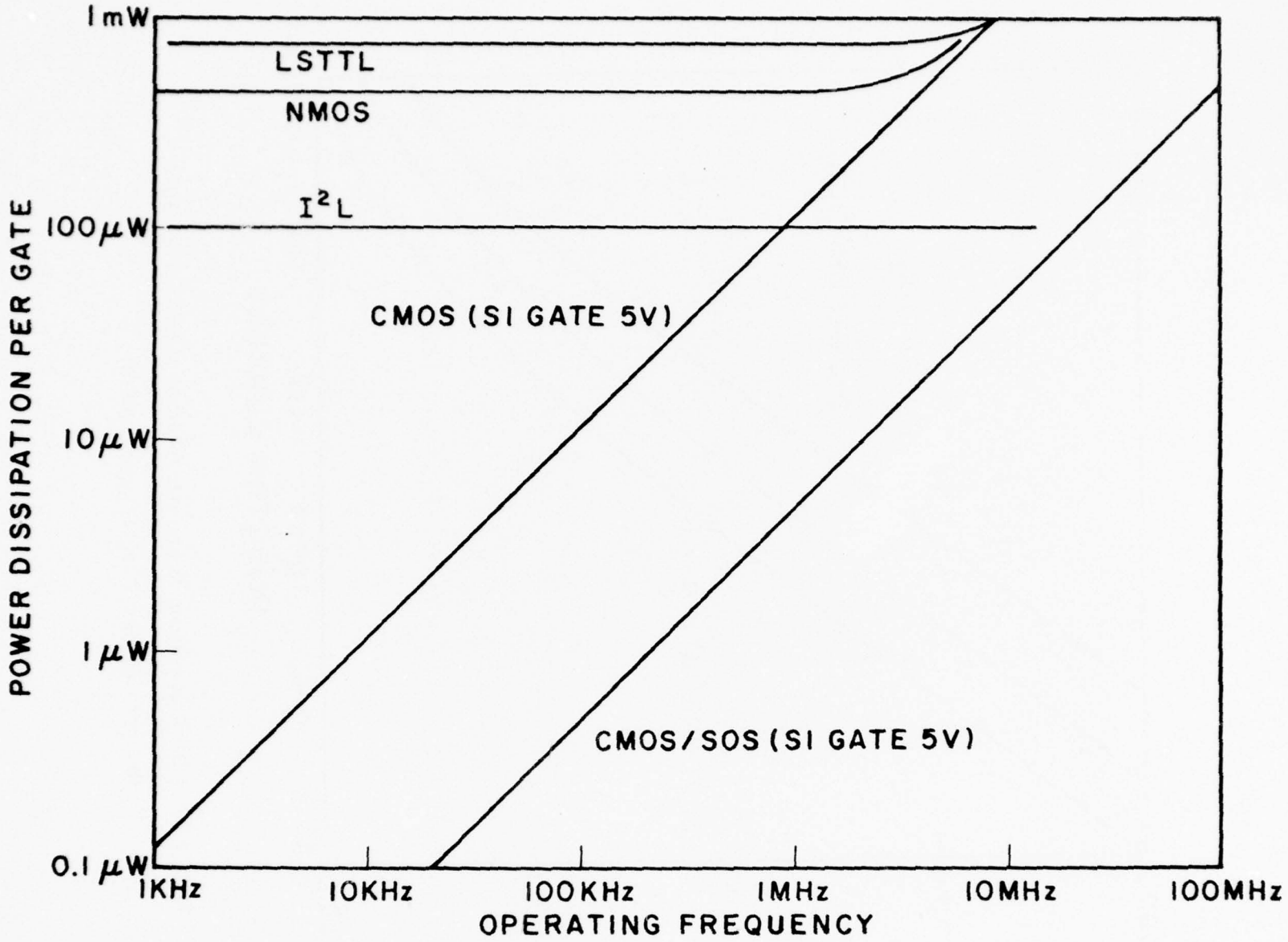


Fig. 1-16 Speed-Power Characteristics of Several LSI Technologies.

constant the power consumption is the same, regardless of the clock frequencies. However, the maximum clock frequency is proportional to the injection current. Therefore, larger power consumption can offer higher clock frequency.

In the following, two major applications will be considered.

(6) Random Access Memory Performance: In the next few months, memory technology will achieve two major advances. First, a 4096 bit I^2L RAM will be introduced with access time around 100 ns. This will be the first 4 kbit bipolar memory. It probably will be considered for main memory applications which up till now has been dominated by MOS memories. However, MOS memory technology is also making significant progress. A 16 kbit NMOS RAM will be introduced this year, which is the second advance. It will help to keep the lead of MOS memory ahead of bipolar memory. From the performance viewpoint, NMOS memory probably will eventually perform at today's TTL level. Intel's soon to be announced 1024 bit static RAM has an access time around 70 ns using the advanced NMOS process. Nippon Electronic's developmental DMOS arithmetic and logic devices operate at a gate propagation delay of 3 ns at 2 volts, comparable to the speed of Schottky TTL. Furthermore, its delay-power product is 2 pJ and it has a density of 141 gates/mm^2 approaching today's I^2L achievements.

Looking ahead, it has been speculated that I^2L memory of area on the order of 1.1 mil^2/bit is possible, which corresponds to a 16 kbit memory on a 175 x 175 mil^2 chip. The relative role of I^2L memory is shown in Fig. 1-17, which partitions the memory field in the "bit density versus access time" plot into several regions for MOS and bipolar memories. I^2L memory will occupy the performance range from 20 to 100 ns in access time and from 4 kbits to 16 kbits in bit density. However, if the performance-cost tradeoff is also considered, the picture for I^2L is not clear at this moment because its cost has not been stabilized. If the cost is high compared to dynamic MOS memories, they will not be considered very much as main-frame memories. However, they could compete with fast static bipolar and NMOS in buffer systems since 4 kbit I^2L

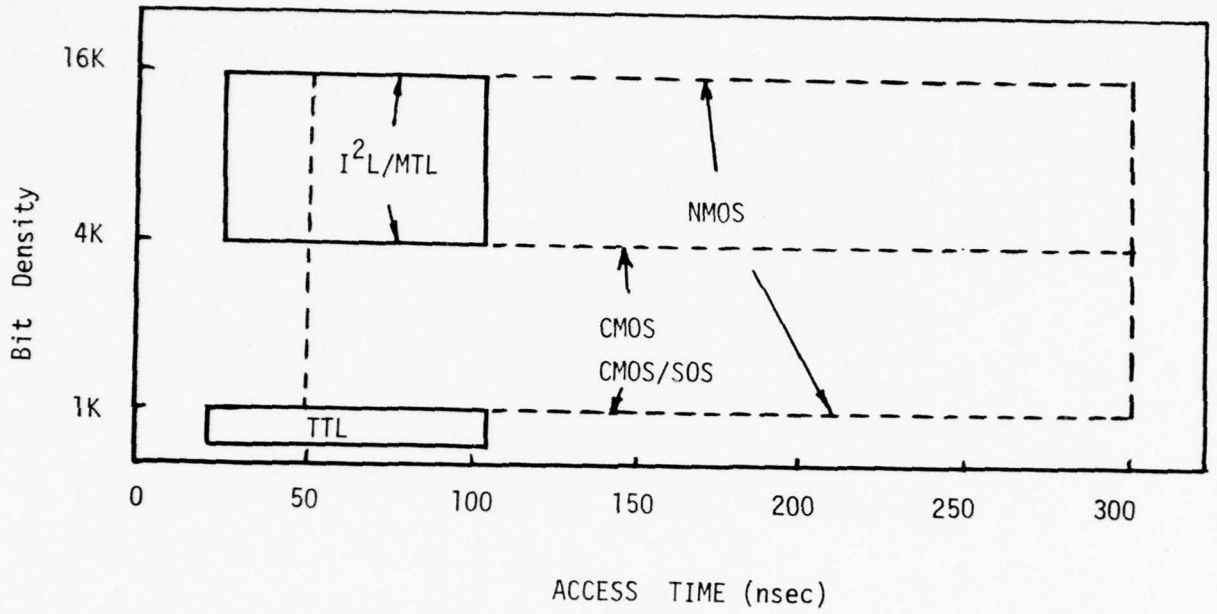


Fig. 1-17 Speculated Bit Density-Access Time Performance of Bipolar and MOS LSI Random Access Memories

memory should be cheaper than 1 kbit bipolar memories based on other technologies. However, since I^2L processing is relatively simple, it is reasonable to expect that its cost will be low. If this is true, and the price is low enough versus that of dynamic MOS, then even a 4 kbit I^2L RAM operating at a 50 ns access time and dissipating about 100 mw will have a major impact on the MOS main-frame memories. The advantage of a 16 kbit I^2L RAM, if it can be successfully developed, is obvious.

(7) Data and Signal Processors: Significant changes in data and signal processing are taking place at this time toward distributed processing. Because of the LSI advances, mini- and micro-computers are delivering better and better performance at lower and lower price. While mini-computers have just begun to use LSI devices, micro-computers (micro-processors) are entirely an LSI creation. The trend is to distribute processing power throughout the system rather than centralize it in a big computer room behind glass panels as we know it today. Fundamental questions like "Are big computers necessary?" are being asked.

To appreciate the LSI impact to this development and to assess the role of injection logic in this "processing power revolution," a two-step presentation will be made.

First, processing equipments are separated into different categories in Table I-6 according to their speed. Some typical applications are also listed. It is well known that there are several rather confusing specifications of speed: cycle time, execution time, state time, micro-instruction time, macro-instruction time, time to add two numbers (real or complex?), time to multiply two numbers, interrupt response time, etc. They not only depend on the basic speed of the hardware but also on the imagination of the program and architecture designer. In this report, a micro-instruction time will be used which refers to the time to perform basic operations like register to register read, modify, write, etc. It can be somewhere from 5 to 10 times the gate propagation delay. It is obvious that specifications like this

TABLE I-6 CLASSIFICATION OF DATA PROCESSORS

	Special Purpose Data Processing	General Purpose Data Processing	Controller	Simple Controller
No. of Bits	20, 24, 32	16, 12, 10	8, 4	4, 2
Microinstruction Time	Below 50 ns	0.05 - 0.1 μs 50 - 100 ns	0.1 - 10 μs 100 - 1000 ns	Above 1 μs
	SP computer Signal processing Fourier transform Correlation Convolution Match filtering Digital filter Multiplier Frequency synthesizer etc. Interface to large computer etc.	GP computer Data acquisition A/D, D/A Process monitoring Navigation Automatic test etc.	Intelligent terminals Data acquisition Communication preprocessor Automobile computer Process monitoring and control Automatic text editing Traffic control Medical electron etc.	Calculator Electronic cash register Accounting system Credit card verification Intelligent instruments Appliances Electronic games etc.
Gate Propagation Delay	Below 10 ns	10-25 ns	25-100 ns	Above 100 ns

can only give qualitative comparison at best. However, it does relate to the hardware performance and will serve the purpose of this discussion. It must be remembered that a critical comparison can only be made by using a benchmark program selected from the application being considered.

Big general purpose computers and some fast mini-computers operate in the instruction time range from 50 to 100 ns. New LSI processors have extended the speed range in both directions. Most mini-computers and micro-processors operate in the 100 ns to few μs range. Calculators and simple controllers are slower and operate above 1 μs. On the fast side, special purpose computers and dedicated signal processors performing special signal processing functions require instruction times below 50 ns, which corresponds to gate propagation delay times of less than 10 ns.

In Fig. 1-18, the processing equipments are approximately matched against several LSI technologies:

Bipolar: I^2L/MTL, EFL, Schottky TTL, ECL

MOS : PMOS, NMOS, CMOS, CMOS/SOS.

I^2L/MTL potentially can cover a broad range of speed and applications. However, for fast equipments with instruction times below 50 ns, the field seems to belong to ECL, Schottky TTL, CMOS/SOS and EFL.

It should be noted that this figure does not include cost-performance tradeoff. How well can I^2L/MTL processors compare with others will have to wait for the stabilization of their costs. However, low performance I^2L/MTL processors should not be too expensive because their fabrication is relatively simple. However, at the high performance end, the jury is out for speculations that modified versions of injection circuits like SFL, SI^2L, VIL, STL, etc. can achieve gate propagation delay in the 1-2 ns range which rivals the best of CMOS/SOS and Schottky TTL. If this can be achieved, the chance is good that injection logic circuits will be cheaper because other high performance logic circuits are all fairly complex and expensive.

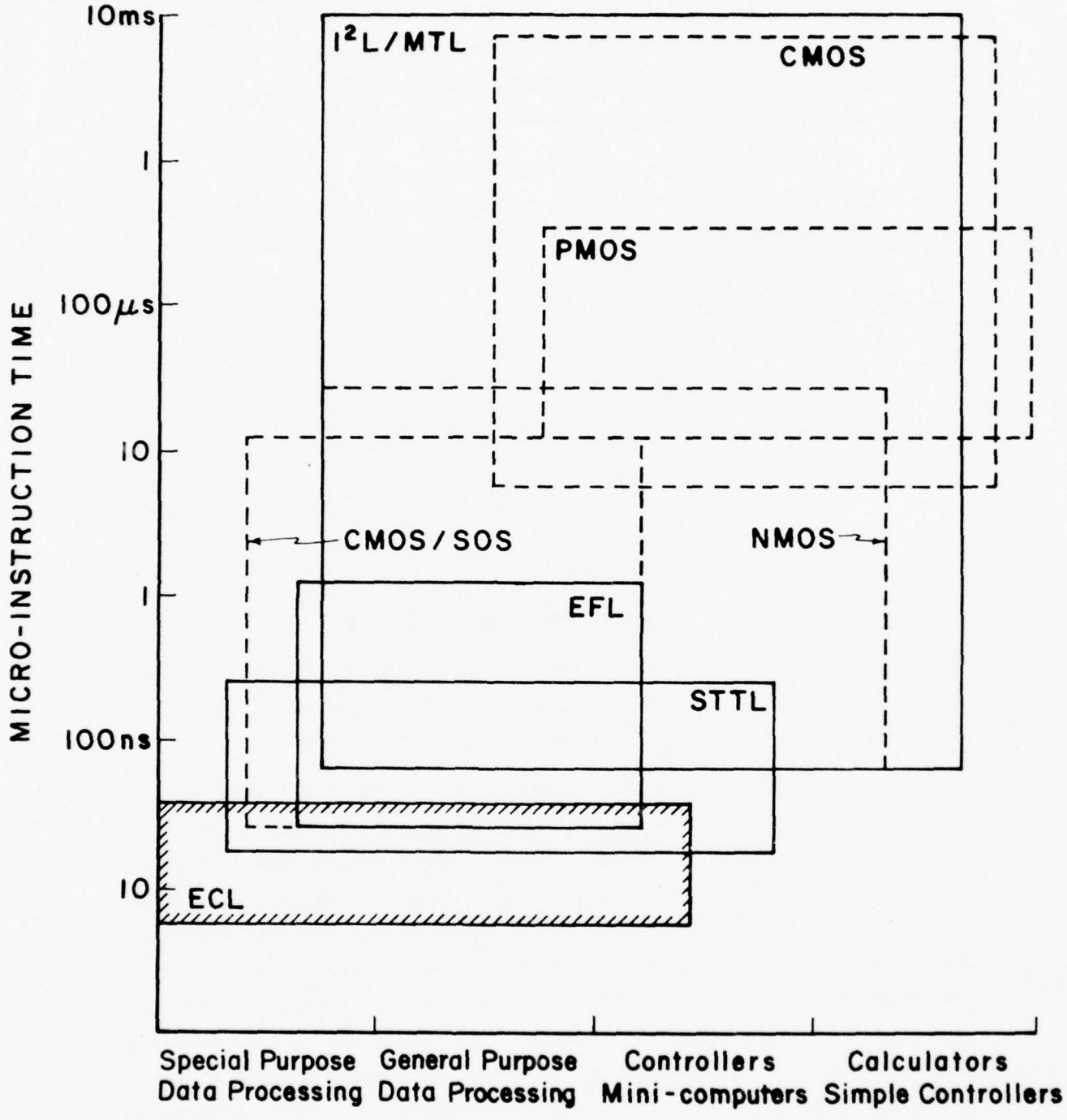


Fig. 1-18 Approximate Performance Ranges and Applications of LSI Processors.

CHAPTER II

STRUCTURES, PROCESSING AND LAYOUT

In this chapter, the structure of I^2L/MTL circuits will be described. Modifications of standard fabrication steps for the purpose of improving performance will be discussed. Finally, layouts of three simple digital circuits will be given. Electrical characteristics will be described in the next chapter.

2.1 THE FABRICATION PROCESS

Injection logic circuits can be fabricated with the same processing steps used in other bipolar IC families. They consist of a repetition of the following steps:

Epitaxial growth
Oxidation
Photoresist process -- application, exposure, etch, etc.
Impurity distribution
Metallization
Packaging

2.1.2 Isolation Schemes

The original I^2L/MTL circuit was simpler to manufacture than conventional bipolar IC's because it required only four masks and two diffusions. The buried subcollector step and the deep isolation diffusion were not required, hence the fabrication was nearly as simple as PMOS processing. It soon became apparent, however, that isolation between adjoining cells was required, and today virtually all circuits use some form of isolation collar. Three isolation schemes are depicted in Fig. 2-1. Both the "no collar" and "shallow collar" versions can be fabricated with a total of four masks and two diffusions, since the shallow collar can be diffused at the same time as the n+ collector. The deep collar requires an additional mask, but is required for improved electrical performance, as will be explained in the next chapter.

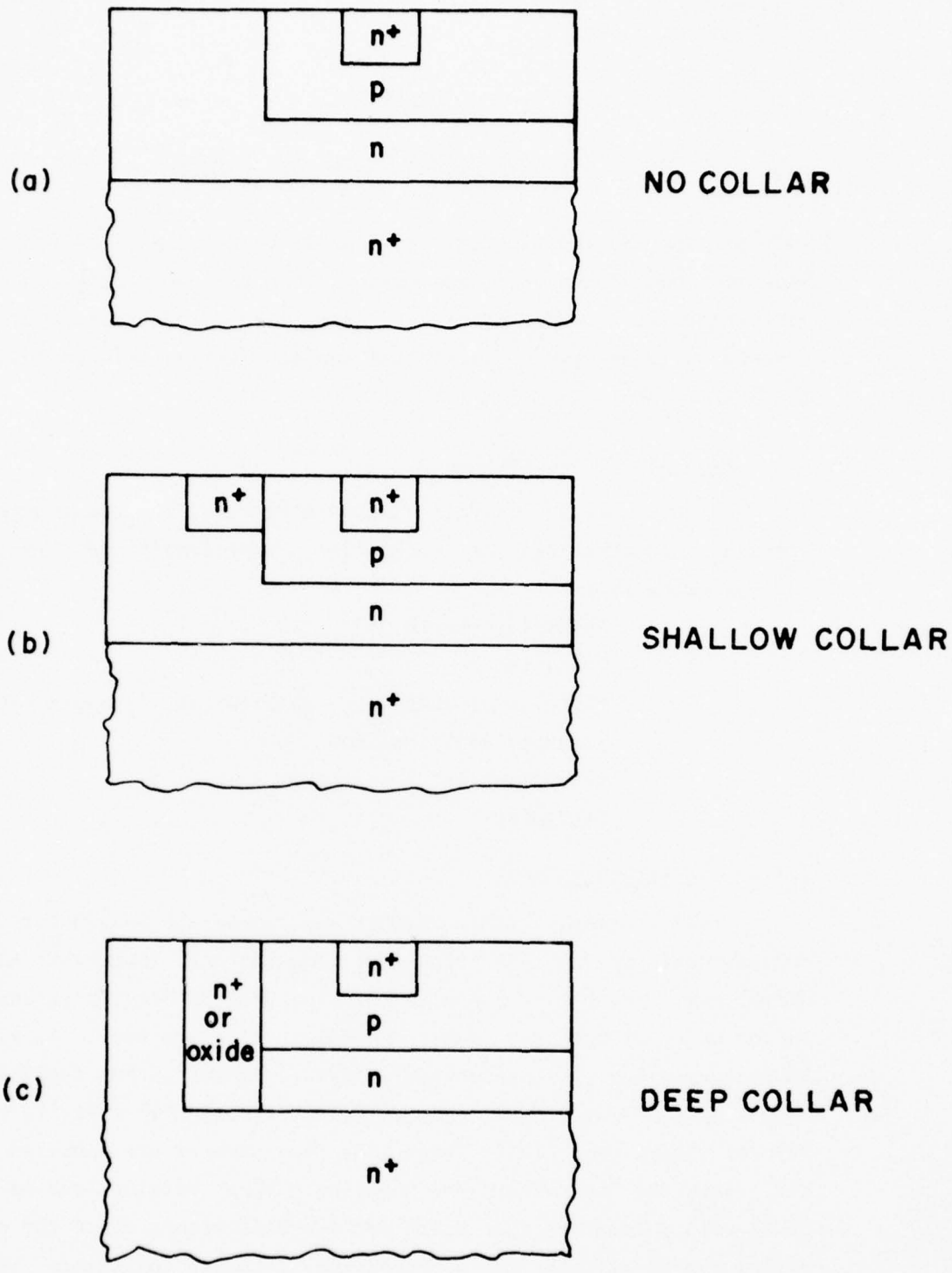


Fig. 2-1 Isolation of Bipolar Injection Logic Circuits
(a) No Collar (b) Shallow Collar (c) Deep Collar

2.1.2 Five-mask, Isolated Process

The "standard" process for I^2L/MTL refers to a five-mask, three diffusion process with a deep collar for isolation. The fabrication steps are summarized in Fig. 2-2. Starting with an n+ substrate, an n-type epitaxial layer is grown several microns thick. Together they serve as the emitters of the npn switching transistors and as the base of the lateral pnp injector.

The first mask is for the deep n+ isolation collar. The second mask then defines the injector rail and the p-type tubs for the switching transistors. The third mask level is for the n+ collectors. Finally, fourth and fifth masks are used for contact and metallization etch steps, respectively. Typical vertical dimensions and a doping profile are shown in Fig. 2-3.

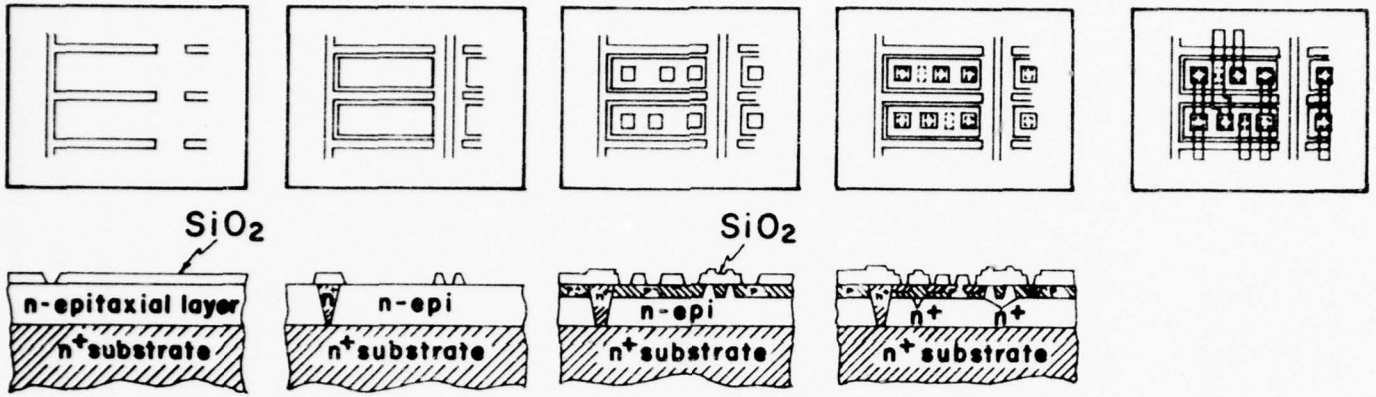
Note that the impurity distribution is not much different from that of a conventional bipolar circuit. The important difference is that in injection logic chips, the epi-layer serves as the buried emitter instead of the buried collector in other bipolar chips, and the collectors are diffused from the top. Therefore, the doping concentration in the base region decreases from the top collector side toward the bottom emitter side in a direction which discourages the desirable upward electron flow in the base from the emitter side toward the collector side. Such a doping concentration in the "wrong" direction will increase the intrinsic propagation delay of an injection logic circuit. In several modified injection logic circuits, the doping profile is reversed in such a way that the acceptor concentration in the base region increases from the collector side toward the emitter side in order to favor the desirable upward electron flow and improve the speed performance.

Since I^2L/MTL is a bipolar technology, it was hoped that it would reach the high performance of other bipolar circuits while at the same time would require simpler processing, enabling it to compete successfully with MOS circuits. This has not been the case. The standard process just described is capable of 10-40 ns propagation delays -- not as good as older T^2L circuits. The speed is inherently limited by minority

Starting S_i = N^+ substrate or N^+ buried layer on P substrate (> 1 x 10^{17} donor atoms/cc, = 0.0|Ω-cm)

(1) Epitaxial layer growth: N^-, 0.5 Ω-cm, 4 - 7μ

(2) Isolation Mask (5) Base Mask (8) Collector Mask (11) Contact Mask (13) Metal Etch Mask



(3) Isolation Diffusion
Phosphorus, B^+
4 - 7μ

(6) Base Diffusion
Boron, P
200-400 Ω/
1.5 - 2μ

(9) Collector Diffusion
Phosphorus or Arsenic, N^+
= 20 Ω/
1 - 1.5μ

(12) Metal Evaporation
Aluminum
= 0.8μ

(14) Metal Etch and Alloy Cycle for Ohmic Contact

(4) Oxide Regrowth (7) Oxide Regrowth (10) Oxide Regrowth

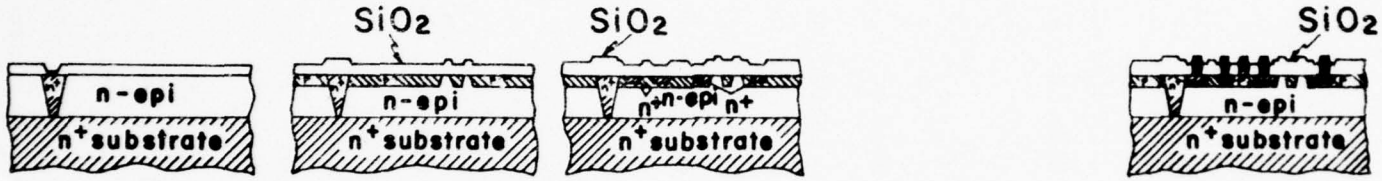


Fig. 2-2 Fabrication Steps for a Standard I^2L Process.

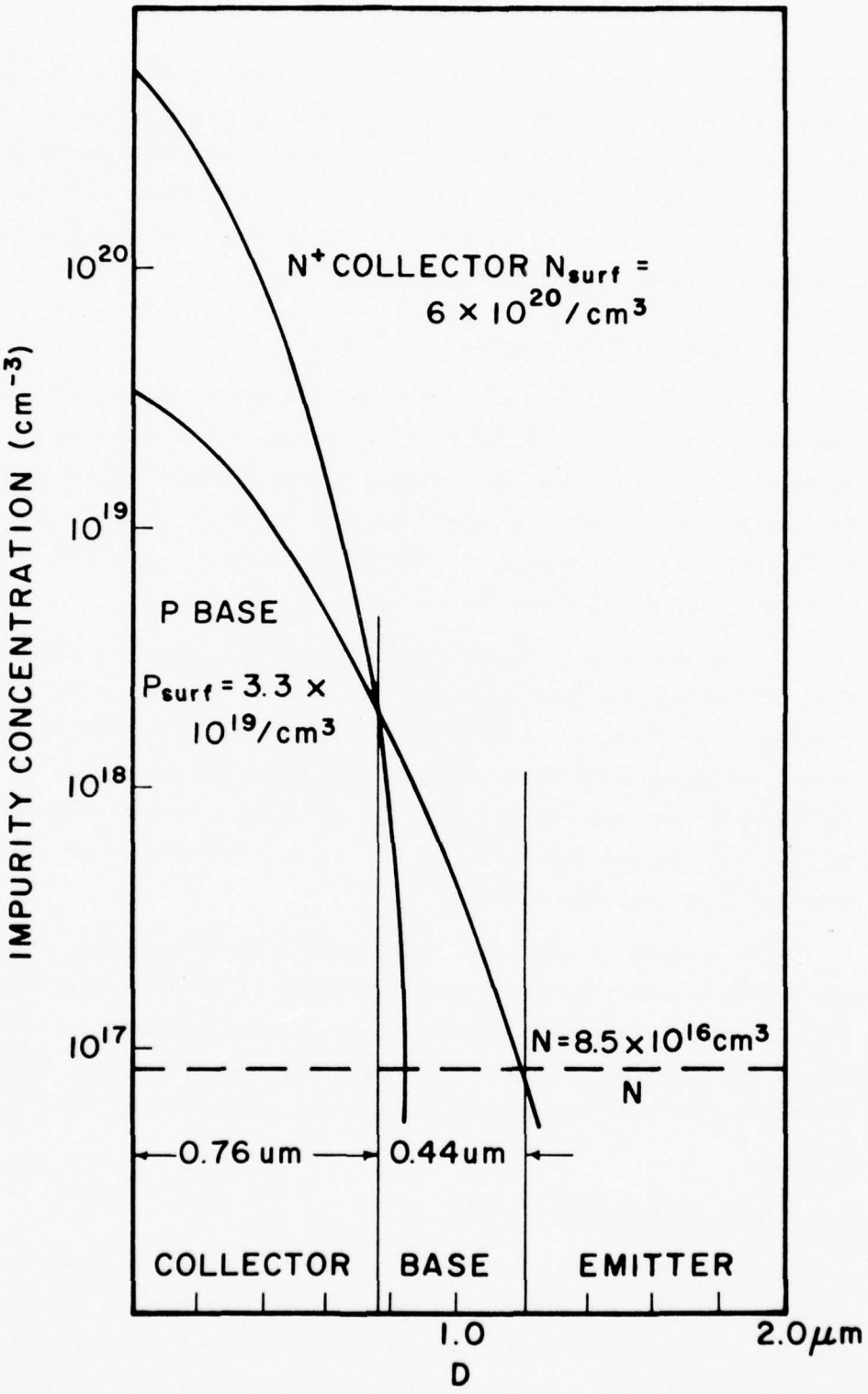


Fig. 2-3 Doping Profile of a Standard IIL/MTL Process (Northrup Data)

carrier storage and by the poor frequency response of the vertical npn transistor due to its retrograde base impurity profile. In addition, any requirement for interface circuits on the same chip cannot be met by the standard five-mask process. Correction of these deficiencies makes it necessary to modify the processing steps, adding mask steps and hence increasing the manufacturing cost.

2.1.3 Interface Requirements

One of the touted advantages of I^2L/MTL is the ability to combine it with other bipolar circuits on one chip. Whether these other circuits are linear or digital, junction isolation schemes normally employed require a p-type substrate and deep p-type isolation diffusions, with corresponding additional masks. A cross-section view of such a circuit is shown in Fig. 2-4.

For the circuit shown in the figure, at least six masks and four diffusions are needed, making the processing as complex as standard bipolar. Furthermore, it should be apparent that the fabrication process cannot simultaneously optimize the performance of both types of circuits. For example, the gold doping which is often utilized to enhance the speed of T^2L will degrade the operation of I^2L (for reasons to be discussed more fully in the next chapter).

A summary of the major processing steps for several combinations of interface requirements is given in Table II-1. Note that the processes vary from the simple case of four masks and two diffusions for the digital circuits using shallow collars to the complex case of eight masks and five diffusions for combined linear and digital circuits with deep n+ or oxide collars.

2.2 HIGH PERFORMANCE I^2L/MTL

Several versions of I^2L/MTL have been introduced in an attempt to improve such characteristics as speed, power dissipation and packing density. The various modifications were discussed in Chapter I (see Fig. 1-10). Innovative processing techniques have made it possible to implement these improved versions. Among these methods are

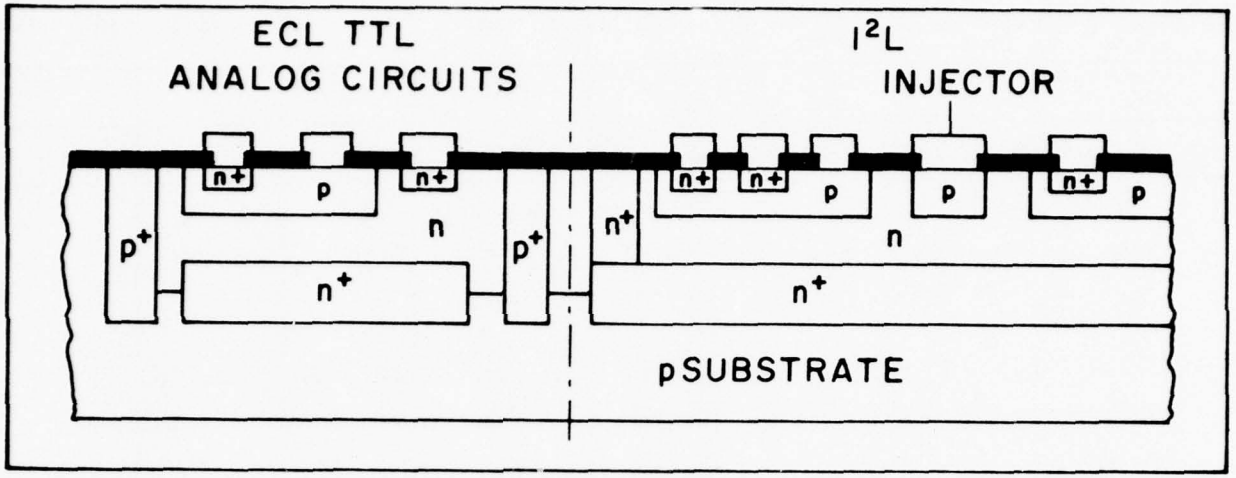


Fig. 2-4 Cross Sectional View of a Chip Combining IIL/MTL and ECL (or TTL or Linear) Circuits (H74-1).

TABLE II-1 PROCESSING STEPS FOR I^2L/MTL WITH ON-CHIP INTERFACE

Process Flow	DIGITAL CIRCUITS				DIGITAL/LINEAR CIRUCITS	
	I^2L/MTL only		Combined with TTL/ECL		Shallow Collar	Deep Collar
	Shallow Collar	Deep Collar	Shallow Collar	Deep Collar		
Starting Silicon	n+	n+	p	p	p	p
Buried Layer (n+)	--	--	M1, D1	M1, D1	M1, D1	M1, D1
Epi-layer (n^-)	Yes	Yes	Yes	Yes	Yes	Yes
Collar or Isolation						
p+ or oxide	--	--	M2, D2	M2, D2	M2, D2	M2, D2
n+ or oxide	--	M1, D1	--	M3, D3	--	M3, D3
Base (p)	M1, D1	M2, D2	M3, D3	M4, D4	M3, D3	M4, D4
Collector and/or Emitter (n+)	M2, D2	M3, D3	M4, D4	M5, D5	M4, D4	M5, D5
Capacitor (oxidation)	--	--	--	--	M5	M6
Metal contact	M3	M4	M5	M6	M6	M7
Metal Interconnect	M4	M5	M6	M7	M7	M8
Number of Masks	4	5	6	7	7	8
Number of Diffusions	2	3	4	5	4	5

Note: M - standard photolithographic mask (metal or emulsion), D - oxide layer to mask against diffusion

Schottky barrier diodes
Ion implantation
Doping profile control
Dielectric isolation.

They are discussed in this section.

2.2.1 Schottky Barrier Diodes

Schottky diodes are used in T^2L logic to prevent the transistors from saturating. This eliminates the storage time delay and improves the switching speed. The mechanism is appropriately referred to as Schottky clamping to point out the clamping of the collector base voltage by the action of the Schottky diode.

In injection logic, Schottky diodes can be used for the same purpose (substrate-fed logic and Schottky I^2L). However, there is an additional mechanism which also serves to enhance the speed. When Schottky diodes are used to decouple different collector outputs (or base inputs), the logic swing is reduced by the voltage drop of the diode. If the forward voltage drop is 500 mV and the normal logic swing is 800 mV, the net result is a logic level difference of 300 mV. This is sufficient to switch the following transistor, and the reduced logic swing means faster charging and discharging of the internal and parasitic capacitors.

The presence of Schottky diodes is not without its drawbacks, however. Parasitic transistor action can occur in which the Schottky barrier metal serves as the collector of the parasitic pnp. In addition, the fabrication steps must be more carefully controlled in the following respects:

a) The standard n+ collector region cannot be used as the cathode of Schottky diodes. Such diodes would have poor rectification characteristics because of tunneling currents. Normally, the n epilayer should be utilized, and its doping concentration carefully controlled.

b) When Schottky diodes are used at the input terminals as in substrate-fed logic, the anode is the p-type base material. Again, for

proper diode action the doping level must be light, but not so light as to create a possible problem with surface inversion.

Evidently the use of Schottky diode technology in bipolar injection logic circuits requires careful control of surface impurity concentrations. One means of doing this is by ion implantation.

2.2.2 Ion Implantation and Doping Profile Control

Ion implantation can be used in bipolar injection logic fabrication for several purposes.

a) It can be used to control the surface concentration of impurities by proper choice of the ion beam current, beam energy, implantation period and oxide thickness. If the implantation is through an oxide, the impurity concentration is maximum at the surface and decreases for increasing depth from the surface.

Precise control of the surface concentration can be used to optimize device performance, prevent surface inversion, and even to form channel stoppers.

b) By proper choice of beam voltage the range of the implanted ions can be controlled such that the impurity distribution is Gaussian, with a maximum value below the surface of the semiconductor. Depending on the type of background doping and the species of the implant, the impurity gradient can be adjusted to either retard the flow of minority carriers toward the surface (desirable when Schottky diodes are used) or to enhance the flow (to improve upward gain and frequency response).

Because of the high voltages used in sub-surface implantation, a post heating cycle is required to anneal crystalline damage.

In Table II-2, two examples of ion implantation processes are listed. In both cases the implantation is made through an oxide. For the low energy example, a standard I^2L/MTL circuit is being fabricated, with the implantation being used to control surface concentrations. For the high energy case, the doping profile is adjusted to improve the speed. The striking feature of these two examples is that ordinary

TABLE II-2

EXAMPLE OF ION IMPLANTATION PROCESS
THROUGH OXIDE

Implantation Process	Low Energy	High Energy
Initial oxidation (1000 Å)		
Define collars Implant phosphorus (150 keV) Drive in phosphorus	$1 \times 10^{15}/cm^2$	Same
Define base and injector Implant boron (60 keV) Drive in boron (x_j = 1.8μ)	$2 \times 10^{14}/cm^2$	$5 \times 10^{14} cm^2$
Define collectors Implant phosphorus (150 keV) Drive in phosphorus (x_j = 1μ)	$1.5 \times 10^{15}/cm^2$	Same
Implant deep boron (500 keV) Anneal boron implant	not used	$5 \times 10^{12}/cm^2$
Open contacts		
Aluminum metallization		
Remark	To fabricate a standard I^2L/MTL cell	To fabricate an I^2L/MTL cell whose base doping profile is controlled

Sheet resistivity of npn collectors = 70 Ω/Square

Sheet resistivity of npn base = 450 Ω/Square

diffusions are completely eliminated. All impurities are introduced by ion implantation.

It is also possible to control the impurity profiles in the base without employing high energy ion implantation. One procedure is to predope the surface of the substrate with acceptors, then grow a p epi-layer for the npn base. It should be remembered that the reason for controlling the base doping profile is to create a rising acceptor profile from the npn collector to the npn emitter. Therefore, outdiffusing the predoped acceptors on the emitter face should help to obtain such a profile. (C75-2)

2.2.3 Dielectric Isolation

In conventional bipolar circuits, dielectric isolation schemes are used to increase packing density, improve isolation, reduce parasitic capacitances, and increase radiation hardness. These advantages also accrue to I^2L/MTL. In addition, it can also be used as an isolation collar to eliminate the unwanted lateral spread of the desired vertical current flow. Several different isolation schemes are available which use thermal oxide, anodic oxide, or air as the dielectric. Interested readers are referred to the literature.

LOCOS
Isoplanar
Anodic oxide
V-groove etching
etc.

2.3 CIRCUIT LAYOUT

The space-saving features of the merged transistor concept have already been pointed out. To refresh these outstanding accomplishments, they are again listed.

1. No resistor required
2. pnp and npn transistors merged
3. Common injector rail

4. Minimum geometry devices
5. Common emitter ground at substrate
6. Simple metal interconnects.

The compactness of I^2L/MTL circuit will be further demonstrated by several examples.

Figure 2-5 illustrates first of all the amazing simplicity of converting a logic diagram to a circuit layout. If the logic diagram consists only of NAND gates (and inverters) the circuit schematic diagram can be derived directly from the logic diagram by observing three rules:

1. Each output from a gate is a separate collector.
2. Each output drives only one gate.
3. All gate inputs are tied together.

From the circuit schematic diagram the chip layout can be immediately drawn. Each transistor occupies a p-type tub. One injector rail supplies all the bias currents. Each electrical connection appears as a metal stripe between the various collector outputs and one base input terminal.

Actually, the chip layout could be done directly from the logic diagram without the intermediate circuit schematic. It should be pointed out, however, that the layout illustrated here is a rudimentary one and does not necessarily illustrate conventional layout practice, as the following examples show.

Figure 2-6 shows an early form of a layout for an AND circuit. The circuit consists of two inverters and a NOR gate. Inverted inputs and two extra, unused outputs are available. Note that the n+ collector diffusion is used as a cross-under in the upper left-hand corner of the layout. Note also that the injector is a p-tub of irregular shape with a single connection. Of particular importance is the compact size and efficient space utilization.

Figure 2-7 illustrates a computer-generated R-S flip-flop layout. In this example, efficient injection is achieved by providing each

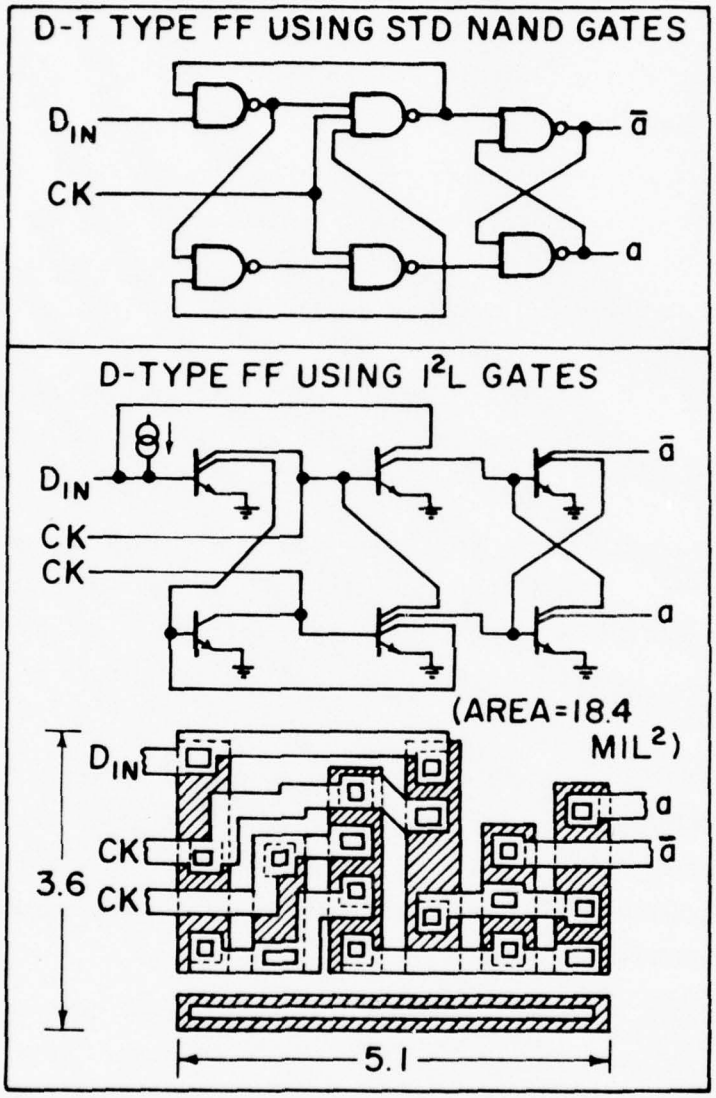


Fig. 2-5 Circuit and Physical Layout of IIL/MTL D Flip-Flop (H75-1).

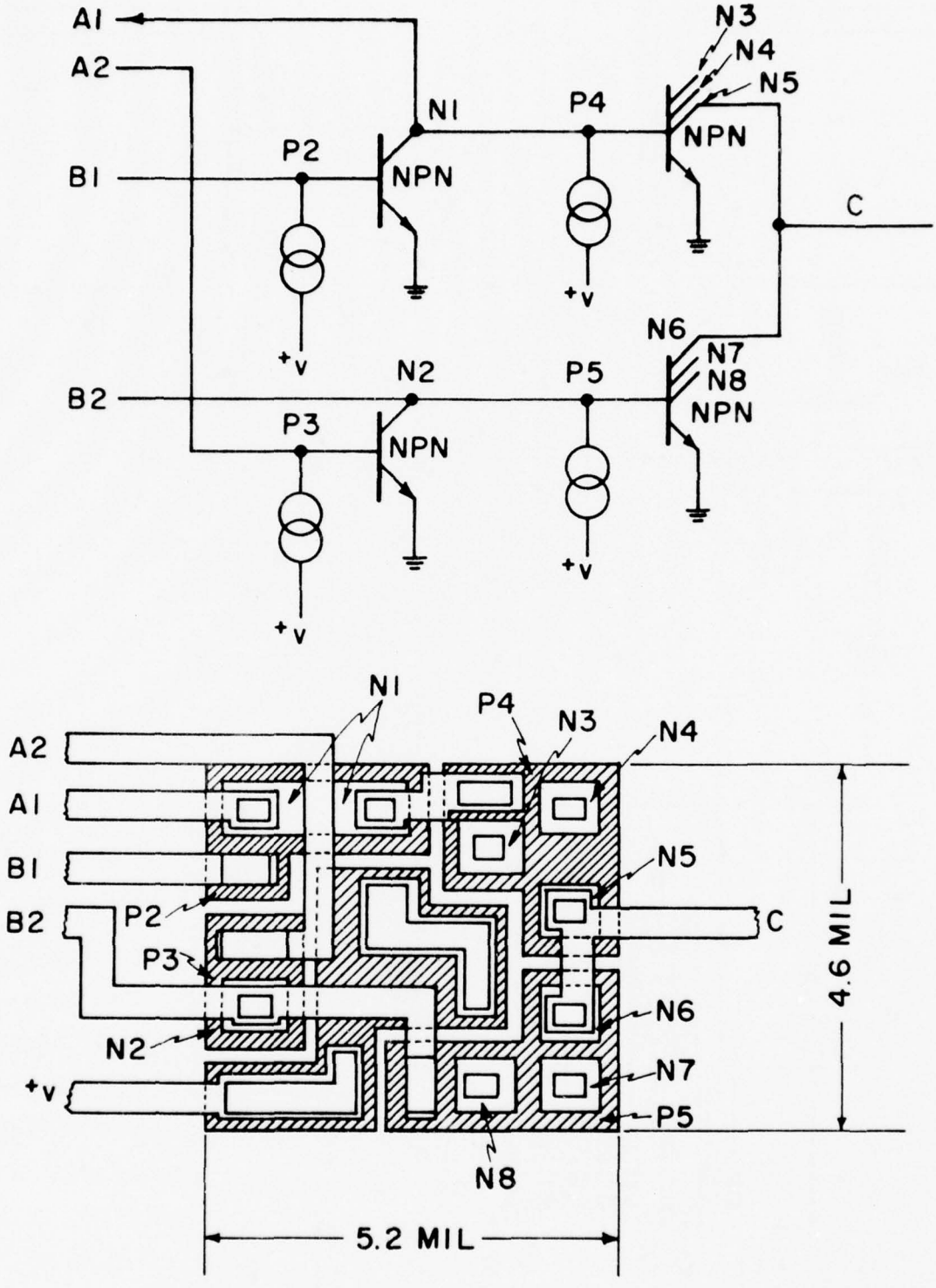


Fig. 2-6 Circuit and Physical Layouts of an IIL/MTL Exclusive OR Gate.

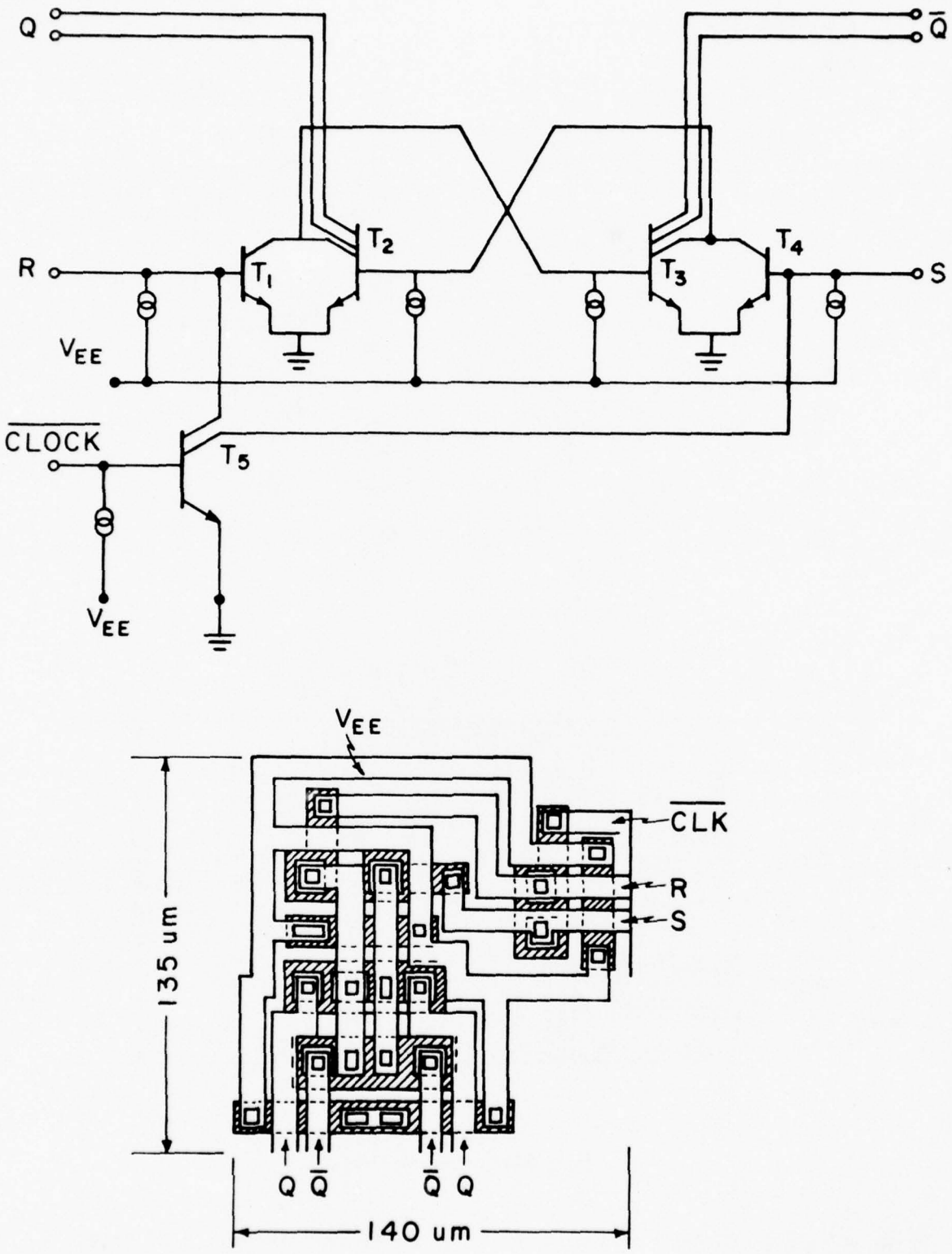


Fig. 2-7 Circuit and Physical Layout of IIL/MTL R-S Flip-Flop.

transistor with its own (usually) broadside injector, even though this requires more complicated metal routing and less efficient packing. But the benefit of efficient current injection more than offsets the slightly more complex metal routing. It is well to recognize that the efficient current injection holds the key to fast response.

Perhaps the most distinctive feature of these three examples is the small size of the circuits and the efficient way of implementing the logic circuit. This can be emphasized by pointing out that each of them is only slightly larger than a bonding pad.

This completes the discussion of fabrication and structural features. In the next chapter the electrical characteristics of these devices will be discussed.

CHAPTER III

ELECTRICAL CHARACTERISTICS

This chapter presents the electrical characteristics of three devices: the basic I^2L/MTL cell-- a modified inverter, the pnp transistor and the npn transistor. Details of circuit modeling are also given. Circuit performance will be presented in Chapter IV.

3.1 INTRODUCTION

3.1.1 New Device and Circuit Problems

Electrical properties of bipolar injection logic will be presented separately in three categories: device characteristics, circuit modeling and circuit performance. This chapter is concerned with device characteristics and circuit modeling.

The original injection logic cell consisted of only two devices: a lateral pnp transistor and an inverted vertical npn transistor. In most of the modified versions of injection logic circuits, Schottky diodes are used. In the new Schottky transistor logic circuit, a pnM transistor was proposed which replaces one of the p layers of a conventional transistor by a metal layer. Therefore, there are three types of transistors and one type of diode used in injection logic circuits.

It is important to recognize that these transistors and diodes are substantially different from the transistors and diodes used in conventional bipolar IC circuits.

Transistors

The pnp transistor was not used in earlier bipolar IC circuits.

The pmM transistor is a new device. Its concept has been demonstrated only by simulation. There is no report yet of its successful fabrication.

The npn transistor in injection logic circuit is different from the conventional npn transistor in several ways:

- It has several collectors. Their number equals the fan out. The collector area is smaller than the emitter and the base area. Each collector receives only a fraction of the emitter current. Current gain is low.

- Collectors are usually heavily doped when a diffusion process is used for their fabrication.

- Collectors are on top. Emitters are at the bottom. The doping profile in the p-base decreases toward the emitter. It retards the upward flow of electrons from the n-type emitter through the p-type base to the n-type collector. It increases the transit time and decreases the cut-off frequency of the npn transistor, slowing down its switching.

Besides these differences, the merged transistor layout created new problems. On the one hand, compromises had to be made in optimizing the performance of both pnp and npn transistors because a semiconductor of a given doping concentration must serve two roles:

- Collector of pnp and base of npn.

- Base of pnp and emitter of npn.

Secondly, current flow in one transistor now can leak to another transistor:

- For lateral flow in the pnp, a vertical leakage path to the base of the npn and the substrate is present.

- For vertical flow in the npn, lateral leakage paths exist. Even when isolation collars are used, there is always one lateral leakage path to the pnp side. Furthermore, since the collector areas are smaller than the emitter area, a part of emitter current never reaches the collectors.

Schottky Diodes

A Schottky diode is used in TTL circuits to limit the base-collector bias of the switch transistor and also to reduce the minority carrier

switching time. It is fabricated in parallel with the base-collector junction by a simple widening of a metal deposition aperture. Its action should be considered as "clamping." However, in injection logic circuits, Schottky diodes are used in a different way as explained in Chapter II. They are inserted in series either in the output paths or in the input paths to decouple these outputs (or inputs). Although they do reduce the logic swing, the circuit operation is not quite the same as clamping.

It is clear then that new device and circuit analyses are needed to study injection logic circuits. Three approaches have been taken. Two of them have been reported in the open literature.

3.1.2 First Analytical Approach--Device Physics Study

The first approach is phenomenological and was developed by Klaassen of Philips. Based on the basic understanding of device physics, the following characteristics were analyzed:

- For the basic I^2L cell:

  static properties--transfer characteristics and noise margin
  dynamic properties--propagation delay

- For npn switch transistor:

  current gain and cut-off frequency

- For pnp injector transistor:

  current gain.

The device and electrical parameters are listed in Table III-1. Their results have been presented in one paper [K75-1] and are highlighted here in Fig. 3-1. Several results are presented which also include their experimental data. The agreement between theory and measurement is very close, suggesting that a theoretical model has been developed which can be used to analyze the effects of device parameters on circuit performance. However, whether its success for an inverter of the original I^2L/MTL structure can be extended to more complex LSI circuits or to other modified versions of injection logic circuits remains to be seen.

TABLE III-1 - PARAMETERS CONSIDERED IN KLAASSEN'S DEVICE PHYSICS ANALYSIS

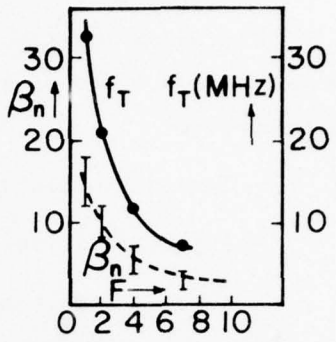
	pnp Injector		npn Switch	
Semiconductor Parameters	Doping Profile, Epi-layer doping density	N_{epi}		
	Carrier concentration:			
	electron density	n		
	hole density	p		
	intrinsic concentration	n_i		
	Transport properties:			
	electrical mobility	u_n, u_p		
	diffusion coefficient	D_n, D_p		
	Excess carrier properties:			
	Minority carrier lifetime (effective hole lifetime in n type epi-layer	τ_{eff}		
	Interface recombination velocity (hole recombination velocity at n-n^+ interface)	S_p		
	Dielectric constant	ϵ_r		
Device Structure	Emitter area	S_{Einj}	Base area	S_B
	Collector area	S_{cinj}	Collector area	S_c
	Base width	W_B	Base diffusion depth	X_j
	Length of emitter	W_{inj}	Epi-layer thickness below base	W_{epi}
			No. of collectors (fan-out)	F
Electrical Device Characteristics	Common base Current gain	β_p	Common emitter Current gain	β_n
			Transition frequency	f_T
			Emitter capacitance	C_{eb}
			Collector capacitance	C_{cb}
			Base resistance	R_b
			Base impurities under collector	$\int N'_g dx$
			Base impurities beside collector	$\int N_g dx$
			Hole density in epi-layer	Q_{epi}
Electrical Operation Conditions	Injector voltage	V_{bias}	Base current	i_B
	Injector current	I_p	Collector current	i_c
	Inverse injector current from npn	i_p		

Fig. 3-1 Highlights of Klaassen's Analysis [K75-1].

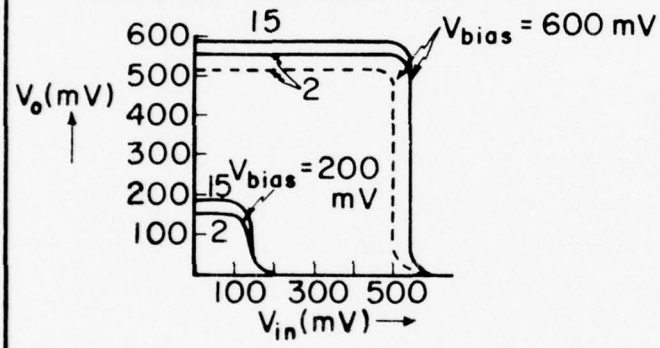
TRANSISTOR CHARACTERISTICS

$$\beta_n \approx \left(\frac{S_C}{S_B}\right)\frac{[\int N_B\,dx]^{-1}}{[1+F(1-S_C/S_B)][\int N_B dx]^{-1}+(F+1)S_p/D_n V_{epi}}$$

$$f_T \approx \left(\frac{S_C}{S_B}\right)\frac{D_n N_{epi}}{2\pi(F+1)W_{epi}\int N_B\,dx}$$

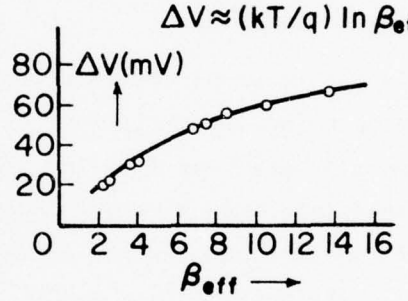


TRANSFER CHARACTERISTICS



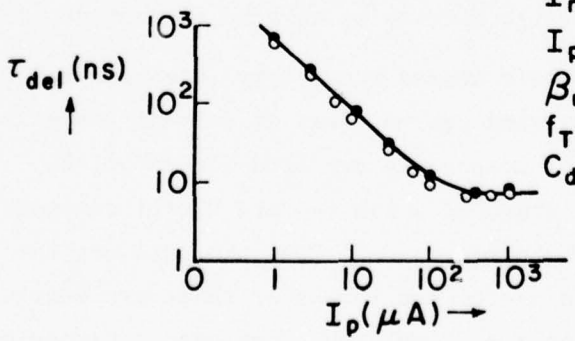
VOLTAGE NOISE MARGIN

$$\Delta V \approx (kT/q)\ln \beta_{eff}$$



$$\exp qV_{in}/kT = \frac{(I_{po}/I_{no})[\exp qV_{bias}/kT - \exp qV_o/kT] - \beta_n^{-1}\exp qV_o/kT}{1 - \exp - qV_o/kT}$$

DYNAMIC PROPERTIES – Propagation Delay



$I_{no} = 210 \times 10^{-18}$ A
$I_{po} = 41 \times 10^{-18}$ A
$\beta_n = 17$
$f_T = 50$ MHz
$C_{dep} = 1.2$ pF

3.1.3 Second Analytical Approach--Circuit Modeling

The second approach is circuit modeling. Three different studies are being made. Two of them have already been reported in the open literature.

- Terminal oriented model [B74-2]
- Injection oriented (or physical structure oriented model)[B74-3]
- Lumped circuit model--Northrup study.

Reported results from the first two studies are in the area of speed analysis--gate propagation delay. Parameters considered are summarized in Table III-2. Both studies are being carried out at the IBM Research Laboratory in Boeblingen.

In the terminal oriented model, the analysis is based on the Ebers-Moll approach and is carried out in terms of parameters which can be experimentally measured from the terminals of an MTL/I^2L device: Specifically, four common base current gains. The propagation constant is expressed in terms of two time constants: an emitter time constant and a collector time constant. The main results are

- an equivalent circuit shown in Fig. 3.2(a)
- An analysis of the intrinsic component of the propagation delay shown by two representative diagrams in Fig. 3-3.

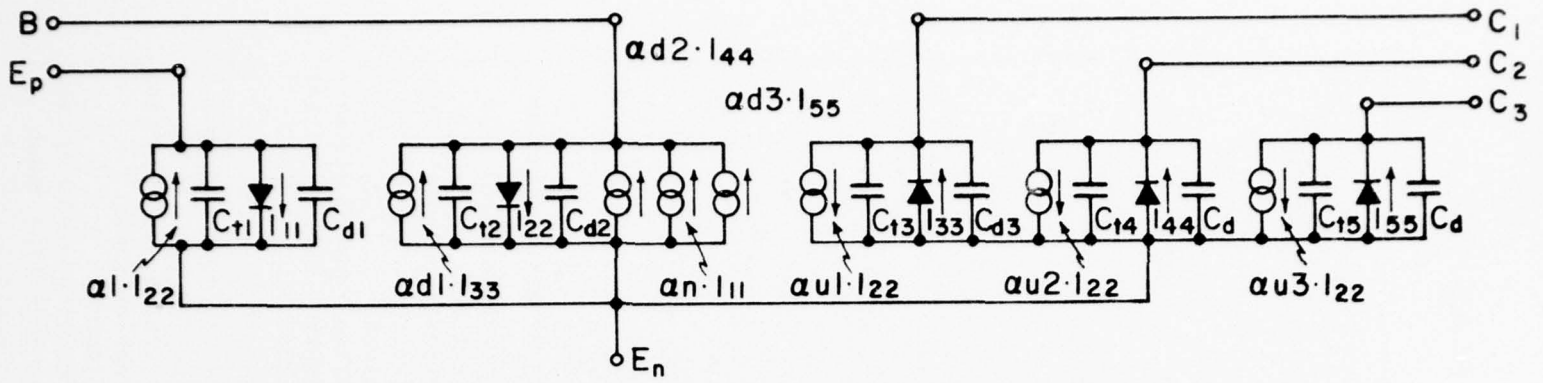
Since this analysis is based on experimental data taken from an MTL device already fabricated, it cannot be used for device optimization if different parameters in the device design have to be changed for better performance.

On the other hand, their second study--the injection model, is based on a new approach and is carried out in terms of current (injection) components. For the basic MTL cell, nine components are used (Table III-2). Five are used for the vertical npn transistor, of which two are useful components; the other three are detrimental to the performance. Four are used for the lateral pnp transistor, of which one is useful and the other three are detrimental. Only terminal current can be measured. Individual components cannot be separately measured.

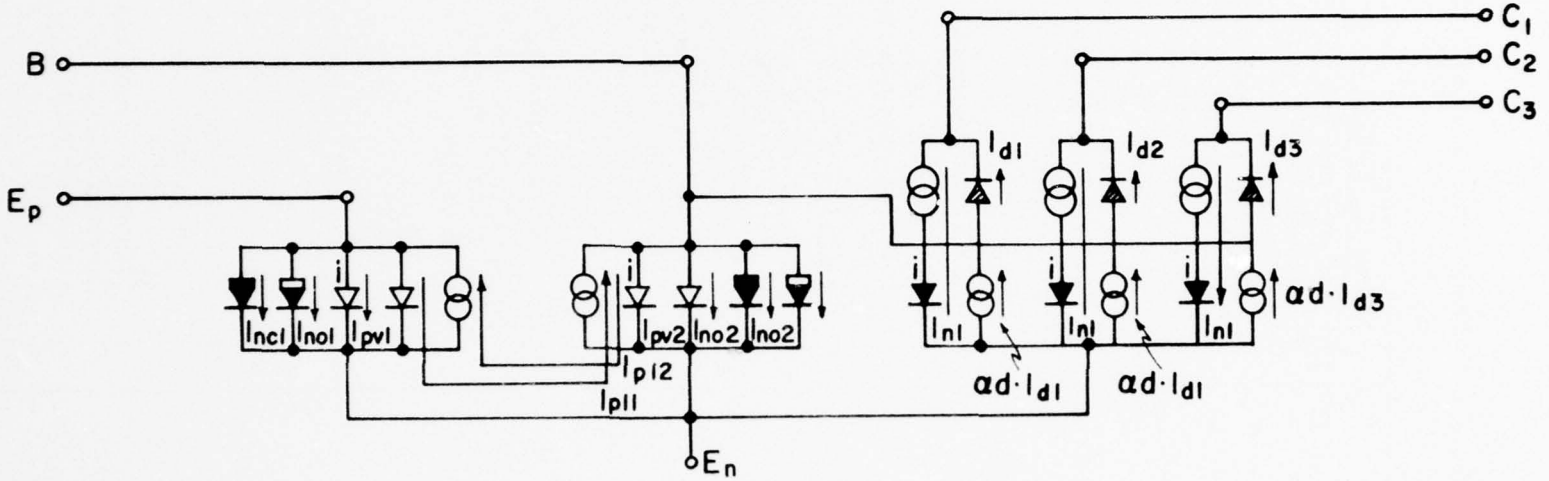
TABLE III-2 PARAMETERS CONSIDERED IN CIRCUIT MODELING ANALYSIS

	Terminal Model	Injection Model
Electrical Characteristics at Terminals	V_i = bias voltage at terminal i I_{ik} = injected current i=k collected current i≠k Q_i = minority carriers due to I_{ii} i = 1 emitter current 2 reverse emitter current 3 4 Collectors 5 (F) = fan-outs) ⋮ C_{ti} = depletion capacitance $= C_o(1 - \frac{V_i}{V_D})^{1/n}$ C_o = zero bias junction capacitance V_D = contact potential n = 2 for abrupt junction 3 for linearly graded junction	V_j = bias voltage at terminal j I_v = vertical current $= A_v j_v(V_j)$ I_ℓ = lateral current $= \ell j_\ell(V_j)$ m = no. of fan-outs
Device Parameters	For pnp α_n = forward common base current gain α_i = inverse common base current gain $\alpha'_{pnp} = \frac{\alpha_i}{1-\alpha_u\alpha_d}$ = pnp recollection factor For npn α_u - upward common base current gain (forward gain) α_d - downward common base current gain) (inverse gain) $\alpha'_{npn} = \frac{\alpha_i}{1-\alpha_u}$ = npn recollection factor	For pnp *$j'_{p\ell 1}$ = lateral hole injection j_{pv1} = vertical downward hole injection j_{nc1} = vertical upward electron injection under emitter contact j_{no1} = vertical upward electron injection beside emitter contact For npn *j'_{pv2} = vertical downward hole injection *j_{ni2} = vertical upward electron injection under collectors j_{nc2} = vertical upward electron base injection under base contact j_{no2} = vertical upward electron injection beside base contact and collectors $j'_{p\ell 2}$ = lateral reverse hole injection

*These injection currents are useful components.



(a) TERMINAL MODEL



(b) INJECTION MODEL (STRUCTURE ORIENTED)

Fig. 3-2 Equivalent Circuits For Terminal Model and Injection Model (B74-2) (B74-3).

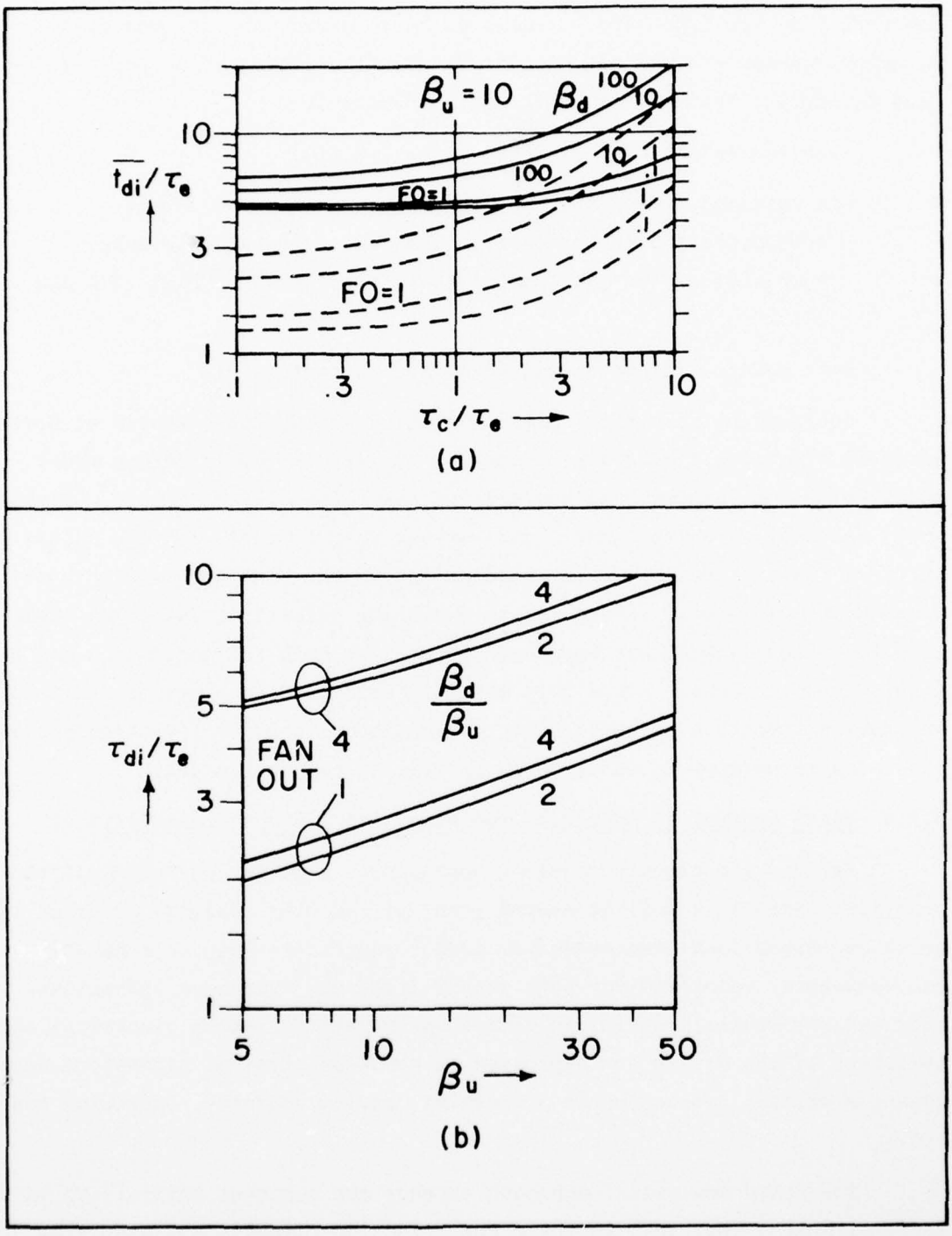


Fig. 3-3 Highlights of Terminal Model Analysis (B74-2).

However, they are expressed in terms of basic device physics and device structure parameters and can be calculated. Therefore, this model can be used for device optimization. The main results are

- an equivalent circuit shown in Fig. 3.2(b)
- a detailed analysis of the individual injection current components and their contributions to the total intrinsic component of the gate propagation delay shown by Figs. 3-4 and 3-5.

Both models will be discussed in more detail later.

Independently, a third circuit model is being investigated at Northrup Research and Technology Center, somewhat similar to the injection model. It modifies the one dimensional analysis of conventional transistors--Linville's model and charge control model, and extends them to deal with the unique problems in LSI I^2L/MTL structures. It could be called the "lumped circuit" model. Since Northrup is also interested in radiation effects on injection logic circuits, such a model has been used to analyze both the ionization and the displacement effects. Since this model is expressed in terms of device physics and device structure parameters, it could also be used to investigate radiation hardening techniques in addition to optimizing the device design.

3.1.4 Third Analytical Approach--Two Dimensional Computer Analysis

Besides the circuit modeling approach to analyze conventional transistor behavior, there is a well developed group of computer analysis programs to solve one-dimensional semiconductor device equations--Poisson's equation and two continuity equations for both steady state and transient operations. They are particularly useful in device optimization because electrical characteristics of the device are expressed in terms of physical parameters such as doping profiles, semiconductor properties, device geometry, operating condition, etc.

The third analytical approach extends the computer analysis to injection logic circuits. However, in these new injection circuits and many other LSI circuits, the interactions among neighboring devices are strong. The unique

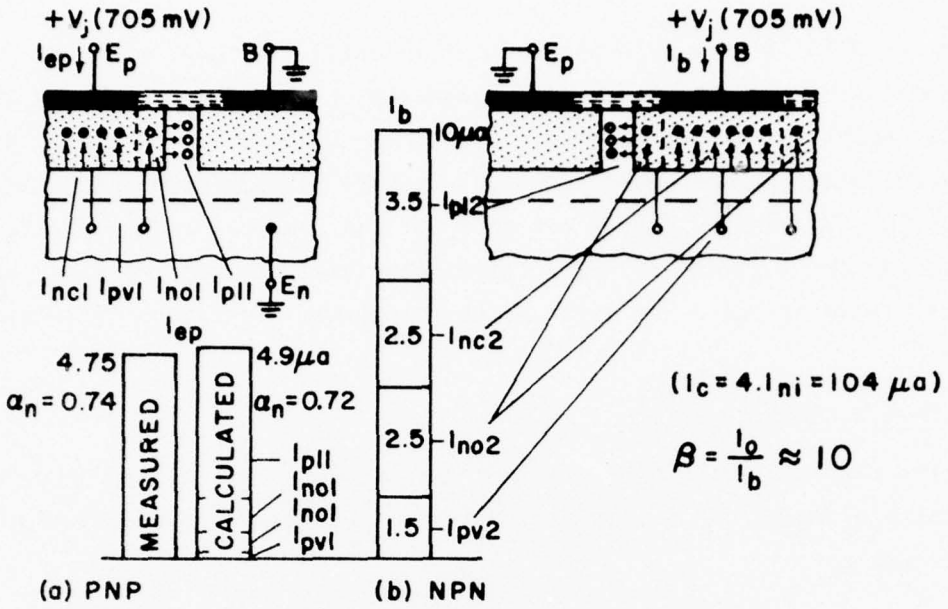


Fig. 3-4 Injection Current Components for (a) Lateral pnp Transistor and (b) Base Current of the Vertical npn Transistor (B74-3).

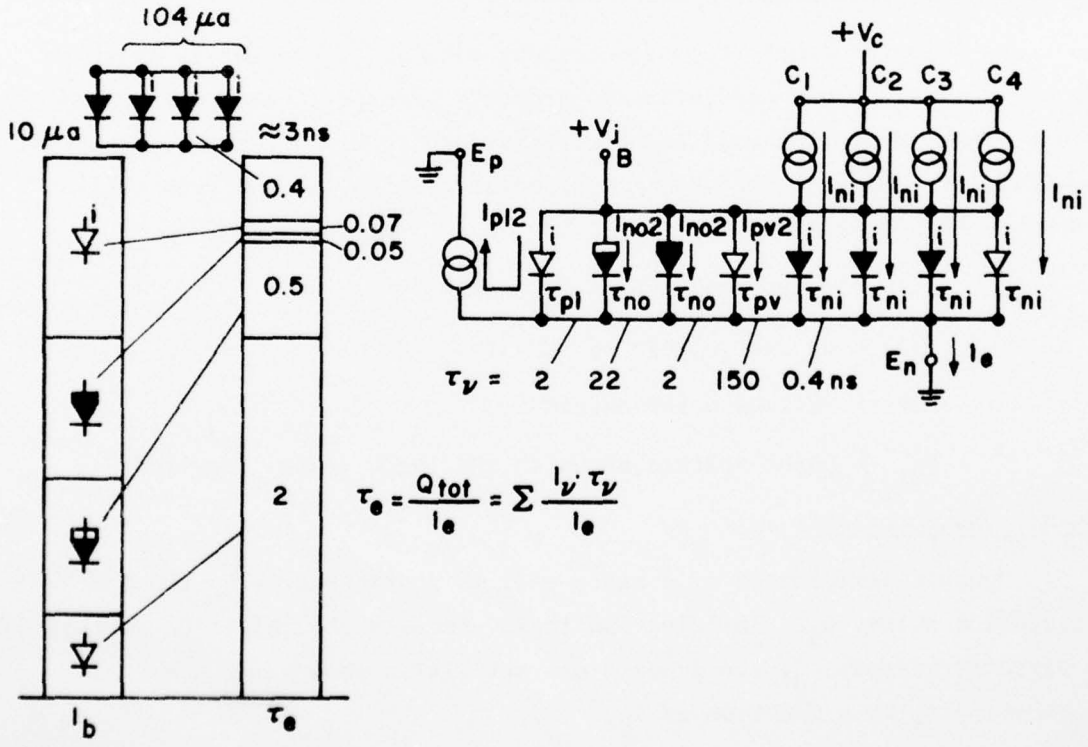


Fig. 3-5 Components of the Emitter Time Constant of a MTL Cell (B74-3).

problems of MTL/I^2L have been pointed out in 3.1.1. Extension of the one dimensional computer analysis to two dimensions probably is necessary in order to apply it to injection logic circuits. It is noted that Philips and several other groups are developing, or have already developed, the 2D analysis. It will be useful not only for the simple I^2L/MTL circuits but also for the modified and more complicated versions of injection logic circuits. However, no publication of this computer simulation is available to date.

3.1.5 Device Characteristics

The basic building block of injection logic is a modified inverter with multiple inputs and multiple outputs. It can be described by two characteristics:

transfer characteristics

dynamic characteristics

Transfer Characteristics

An output voltage (V_o) versus input voltage (V_{in}) plot is shown in Fig. 3-1. It is considered a static property because it can be measured in d.c. experiments although logic circuits are rarely used at d.c. in real applications. Several performance parameters can be derived from this transfer characteristics:

V(1) = output voltage of "1" state

V(0) = output voltage of "0" state

ΔV = voltage noise margin

V_{tr} = input voltage at which the logic state is switched.

Dynamic Characteristics

Dynamic performance of a basic cell is characterized by the gate propagation delay, t_d. In injection logic, because the injection current I_p directly affects t_d, the dynamic characteristic is usually presented by plotting t_d as a function of I_p.

Both characteristics have been studied theoretically. In section 3.2, their results will be summarized first, followed by several experimental results investigating the effects of device parameters on t_d. From these summaries, the requirements of the pnp injector and the npn switch transistor for good basic cell performance will become clear.

pnp Requirement

- large forward common base current gain (α, α_n, α_f)

npn Requirements

- large upward common emitter current gain (β_u, h_{FE}, β_i)
- high cut-off frequency (f_T)
- small circuit capacitance including:

  depletion capacitance

  parasitic capacitance.

In sections 3.3 and 3.4, properties of these transistors will be discussed and followed by some comments on their optimization and tradeoff.

3.1.6 Current Gain Notations

It is obvious that current gains of both the pnp and the npn transistors play critical roles in determining injection logic performance because the basic logic operation is carried out by steering the current in different directions to turn on or turn off the proper npn transistors. The notations for current gains have been somewhat confusing because the npn transistors are fabricated upside down and are operated in the "inverted" mode. A clarification will be attempted here.

To begin, it should be recognized that the pnp is operated in the common base mode and the npn is operated in the common emitter mode. For a transistor, there are four different current gains:

α = large signal common base current gain relating emitter current and collector current.

β = large signal common emitter current gain relating base current and collector current

$\simeq$ large signal h_{FE} if the base current is large compared with I_{CBO}.

α and β are related by the relation

$$\beta = \frac{\alpha}{1-\alpha} \quad , \quad \alpha = \frac{\beta}{1+\beta}$$

They can be further separated into two types:

- Forward or normal characteristics--current is flowing from emitter (or base) to collector.

  α_f, α_n

  β_f, β_n

- Inverse or reverse characteristics--current is flowing from collector to emitter (or base).

  α_i , α_r $\quad \alpha_i \simeq 0.5 - 1\ \alpha_f$

  β_i $\quad \beta_r$

When these parameters are applied to injection circuits, there is no real confusion for the pnp injector. The forward common emitter current gain for current flowing from emitter to collector is variously represented by the notations:

α

α_n

α_f

It should be noted that the common emitter current gain β_p is used in Klaassen's excellent analysis instead of the more conventional α notation. The inverse common base current gain for current flowing from collector to emitter is represented by α_i.

Because of the merged transistor structure, this reverse (inverse) current flow could be considerably larger than typically found in conventional bipolar IC transistors.

For the npn transistor, the notations are more confusing. The forward common emitter current gain from base to collector is variously represented by:

h_{FE}

β_n (n stands for npn)

β_u (u stands for upward)

β_i (i stands for inverted structure).

β_i could cause some confusion because it is also one of the two notations used for inverse common emitter current gain:

β_i (i stands for inverse)

β_d (d stands for downward).

In this report, the notations β_u and β_d will be used following Berger & Wiedman's papers [B74-2], [B74-3].

3.2 BASIC I^2L/MTL CELL

3.2.1 Circuit Configuration and Operation

The basic building block of the injection logic circuit is a modified inverter. An inverter consists of only one pnp injector and one npn switch transitor. The pnp supplies the power by injecting a current I_p. The npn performs the logic. It has one input at the base and one output at the collector. The basic cell is essentially an inverter but the numbers of inputs and outputs are increased. Several inputs are tied together at the base of the npn transistor. Their number is equal to the fan in FI. They are connected to the collectors of FI different cells. The npn transistor has FO collectors, where FO = number of collectors = fan out. In practice, FI and FO of up to four are not uncommon. But FI or FO above five is rare.

The circuit operation cannot be adequately studied by considering only one cell because the injector current coming out of the pnp, αI_p, is either kept in the same cell or steered to another cell depending on the input voltage. When the inputs are all high, αI_p flows toward the npn transistor T2 and stays in the same cell as shown in Fig. 3-6(a).

$V(1) \simeq 0.7$
$V(0) \simeq 0.05$

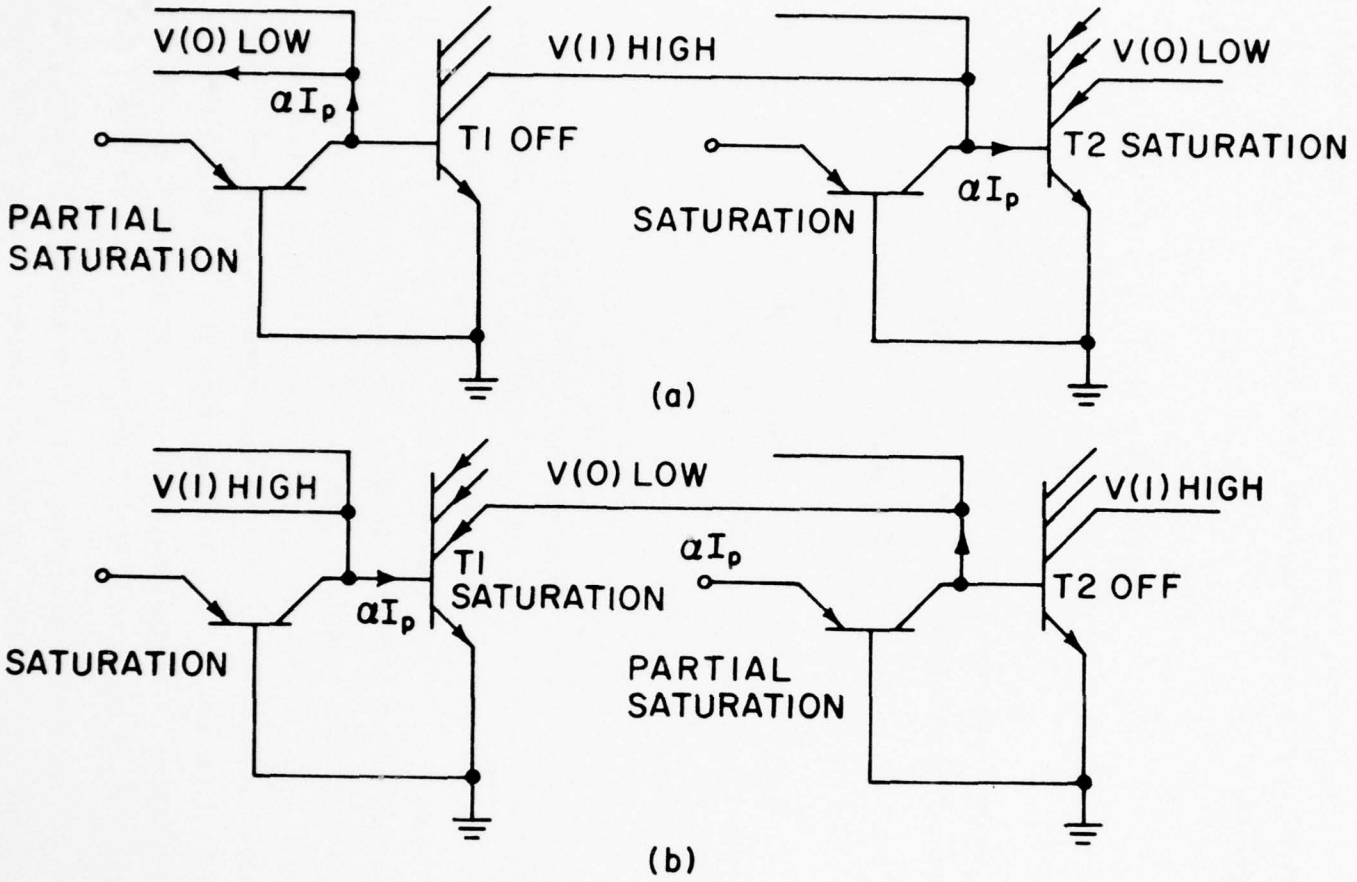


Fig. 3-6 Voltage Levels, Current Flows and Transistor Conditions of the Two Binary States.

T2 is in saturation and is sinking all the currents from FO cells connected to its collectors. In order to keep T2 in saturation, its common emitter current gain β_u must satisfy the requirement

$$\beta_u \cdot \alpha I_p \geq FO \cdot \alpha I_p$$

$$\text{i.e.,} \qquad \beta_u \geq FO$$

When one or more of the inputs is low, the current αI_p will be directed toward the npn transistor of the preceding stage T1. (Fig. 3-6(b)).

It is clear then, that a proper study of the circuit operation should consider at least two stages. The diagrams in Fig. 3-6 show the approximate voltage levels at various points of the circuit for both of the binary states. It should be noted that the voltage levels are only approximate. They will be different depending on the d.c. power supply voltage, device design, fan out, etc. It is noted that the pnp transistor is never switched although it probably is moved slightly out of saturation when the input is low. However, the npn transistor is switched back and forth between the "off" and the "saturation" states. Therefore, the speed of the circuit will be mainly determined by the time it will take to build up and to remove the charges around the npn transistor.

3.2.2 Requirements of Good Performance

From these qualitative explanations, the following list of requirements for good performance can be readily obtained.

Voltage Requirements

Two voltage levels are involved:

$V(1) \simeq V_{BE}$ to turn on npn transitor $\simeq V_{bias}$

$V(0) \simeq V_{CE}$ when the npn is in saturation.

There is no need to use a d.c. voltage supply much higher than V_{BE} (saturation). In fact, V_{DC} is usually around 1 volt. Power consumption can be reduced by decreasing V(1). It cannot be too low lest it will not turn on the npn transistor. V(0) should be as low as possible.

Furthermore, the transition between V(1) and V(0) must be sharp and occur over a narrow voltage range.

Current Requirements

Current is used in two roles:

- to turn on and turn off the npn transistor,
- to charge and discharge the capacitance around the npn transistor.

More current can be used to gain speed until the propagation delay reaches the intrinsic limit. This typically occurs in the current range around 100-300 microamps. If low power consumption is desirable, small current should be used. It has been reported that current as low as 10 namp is able to switch an npn transistor of five collectors but at a terribly long propagation delay of a few milliseconds.

Device Requirements

To translate these requirements into device design, current gain and cut-off frequency have been two of the most frequently used parameters.

For the pnp injector, the common base current gain should be as high as feasible so that a large fraction of the externally injected current can be used to switch npn transistors. However, in merged transistor structures, there are always vertical paths for injected current to leak downwards. Attempts to minimize these leakages are being pursued such as the use of vertical injection schemes, higher doping concentration in the substrate, narrow pnp base width, etc.

For the npn switch, the design optimization is more complicated. In principle, its common emitter current gain should be high not only for faster charging and discharging but also for higher "current sinking" capability, i.e., more fan-out. Generally speaking, the device should be made as small as possible, short of getting into yield and reliability problems. Since area and depth usually go hand in hand, a small device also means thin epi-layer and shallow diffusions. Resistivity or doping concentration are usually chosen from the depletion width consideration based on circuit performance requirements. Side wall isolation using either heavy diffusion or dielectric regions usually helps in reducing capacitance, reducing size, increasing speed, and reducing delay-power product but at the expense of higher cost.

It should be remembered that there are always compromises and tradeoffs. Performance in one area is usually gained at the expense of some others. Two-dimensional computer simulation analysis is needed for design optimization. However, some phenomenological theories and circuit models have been developed to shed light on design optimization without going into number crunching on the computer. The following discussion is based on one of the most useful phenomenological theories developed by Klaassen of Philips [K-75-1].

3.2.3 Device Physics Analysis by Klaassen

Static and dynamic properties will be presented separately.

Static Property I--Transfer Characteristics

All static properties can be derived from the transfer characteristics. Although it is presented in terms of voltage, its derivation is based on current considerations. The starting point is the current conservation relation.

Injected current from pnp transistor	=	Current flowing to the base of npn transistor in the same cell	+	Current flowing to the collector of npn transistor in the preceding cell	+	Reverse current flowing back into pnp transistor

$$I_p = i_B + I_{n1}(V_0, V_{in}) + i_p \qquad (3 - 1)$$

The i_p term represents the problem unique to the merged transistor structure and is detrimental to the circuit performance. All four current components can be expressed in terms of device parameters and operation parameters.

$$I_p = I_{po} \exp (q V_{bias}/kT)$$

$$i_B(V_o) = \frac{I_{no} \exp (q V_o/kT)}{\beta_n(F)} \qquad (3 - 2)$$

$$I_{n1} = I_{no}[\exp (q V_{in}/kT) - \exp (q \overline{V_{in} - V_o}/kT)]$$

Definition of these parameters can be found in Table III-1.

Substituting (3 - 2) into (3 - 1), an equation relating V_{in} and V_o is obtained which is the transfer characteristic.

$$\exp(q V_{in}/kT) = \frac{(I_{po}/I_{no})[\exp(q V_{bias}/kT) - \exp(q V_o/kT] - \beta_n^{-1}\exp(q V_o/kT)}{1 - \exp(-q V_o/kT)} \qquad (3 - 3)$$

From (3 - 3), the following performance parameters can be derived.

$$V(1) \simeq V_{bias} - \left(\frac{kT}{q}\right)\ell n\left[1 + \left(\frac{1}{\beta_n}\right) \cdot \left(\frac{I_{no}}{I_{po}}\right)\right]$$

$$V(0) \simeq \frac{kT}{q}\left[\frac{1}{\left(\frac{I_{no}}{I_{po}}\right)} + \frac{1}{\beta_n}\right] \qquad (3 - 4)$$

$$V_{tr} \simeq V_{bias} - \left(\frac{kT}{q}\right) \ell n \left[\frac{I_{no}}{I_{po}}\right]$$

$$\Delta V - \left(\frac{kT}{q}\right) \ell n \left[\frac{1}{\frac{1}{\left(\frac{I_{no}}{I_{po}}\right)} + \frac{1}{\beta_n}}\right] = \frac{kT}{q} \ell n(\beta_{eff})$$

It can be seen that the ratio I_{no}/I_{po} is one of the most important device parameters used in this analysis. It represents the device geometry and doping profile. It seems that this important ratio cannot be expressed by a simple relation and was not included in Klaassen's excellent paper. Its importance in device design will be discussed after the dynamic characteristics are presented.

In Fig. 3-1, the transfer characteristics were plotted for the following cases:

$$\frac{I_{no}}{I_{po}} = 10, \quad V_{bias} = 0.6V \text{ or } 0.2V, \quad FO = 2 \text{ or } 15$$

$$\frac{I_{no}}{I_{po}} = 50, \quad V_{bias} = 0.6V \quad , FO = 2$$

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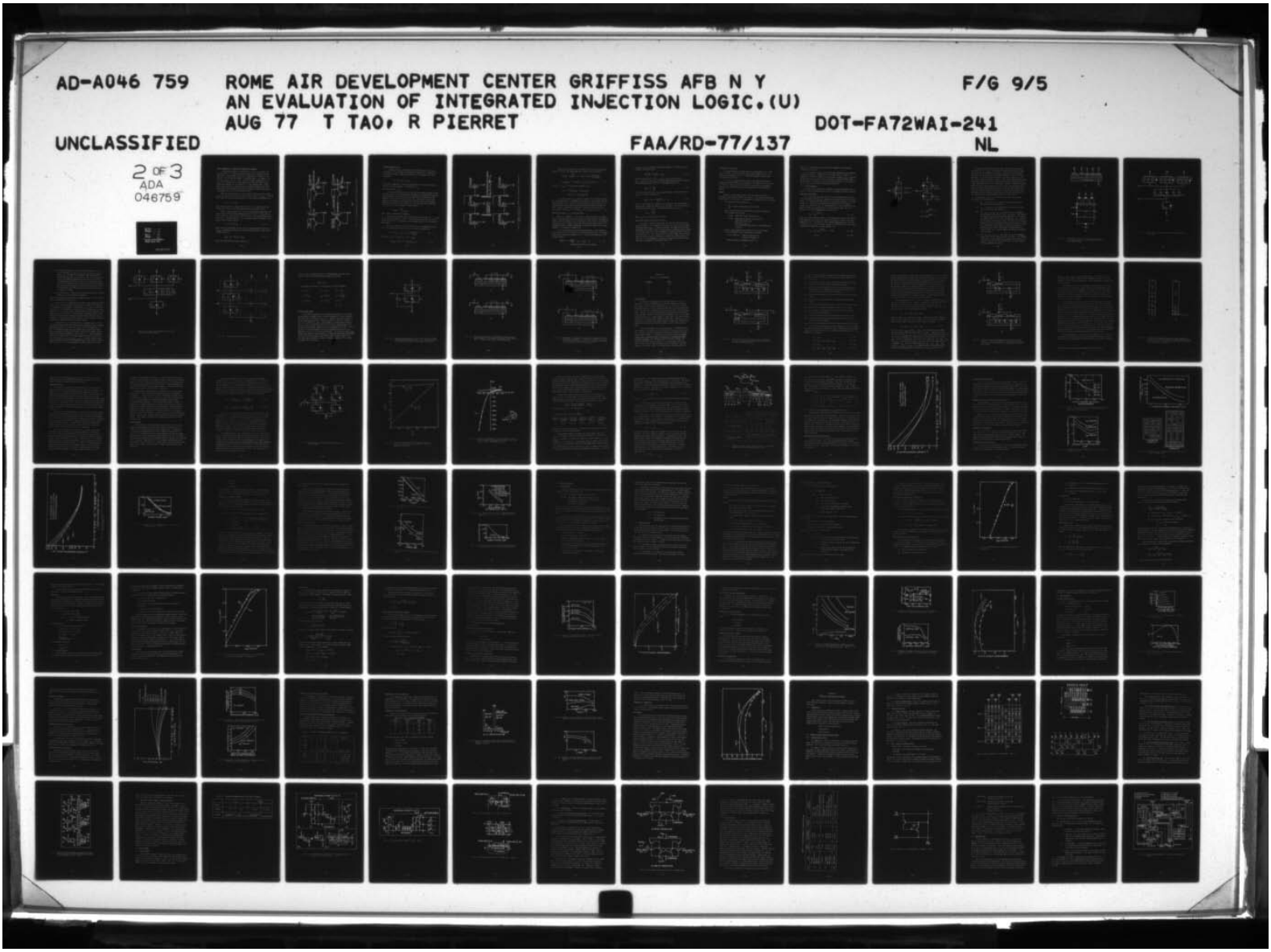


Static Properties II-- Voltage and Current Noise Margins

Voltage noise margin ΔV is defined as $\Delta V = V(1) - V_{tr}$ and was also plotted in Fig. 3-1. Some experimental results are also presented in the same figure. The agreement is excellent, supporting the validity of this analysis. The voltage noise margin is in general small. For example, for $F = 1$ and $I_{no}/I_{po} = 20$, $\Delta V \simeq 60$ mv. From the transfer characteristics, it can be seen that the critical noise margin occurs when the input is high and the npn transistor is in saturation. A slight downward noise voltage spike could turn it off. However, the noise immunity probably should also be examined from the current consideration because the current noise margin corresponding to this ΔV is not necessarily small.

When the npn transistor T2 is in saturation, the pnp injector current αI_p flows toward the base of T2, as shown in Fig. 3-7(a). If $I_{B\ off}$ = threshold base current to turn off the npn transistor, then current noise spikes up to

$$I_N = \alpha I_p - I_{B\ off}$$

can be tolerated without a faulty turn-off of T2. It is readily clear that current noise margin can be increased by raising the injector current.

When the npn transistor T2 is "off," the noise current spike which will cause a faulty turn-on can be estimated using Fig. 3-7(b). In this case, T1 is in saturation. Since its base current is αI_p, it can sink collector current up to $\beta_u\ \alpha I_p$. However, only $FO \cdot \alpha I_p$ is flowing through T1, therefore it can take on a noise current spike of

$$I_N = (\beta_u - FO)\ \alpha I_p \qquad (3 - 5)$$

before diverting any further increase of noise current toward the base of T2. If I_{Bon} = threshold base current to turn on the npn transistor, then a noise current spike up to

$$I_{Nth} = (\beta_u - FO)\ \alpha I_p + I_{Bon} \qquad (3 - 6)$$

can be tolerated without a faulty turn-on of T2.

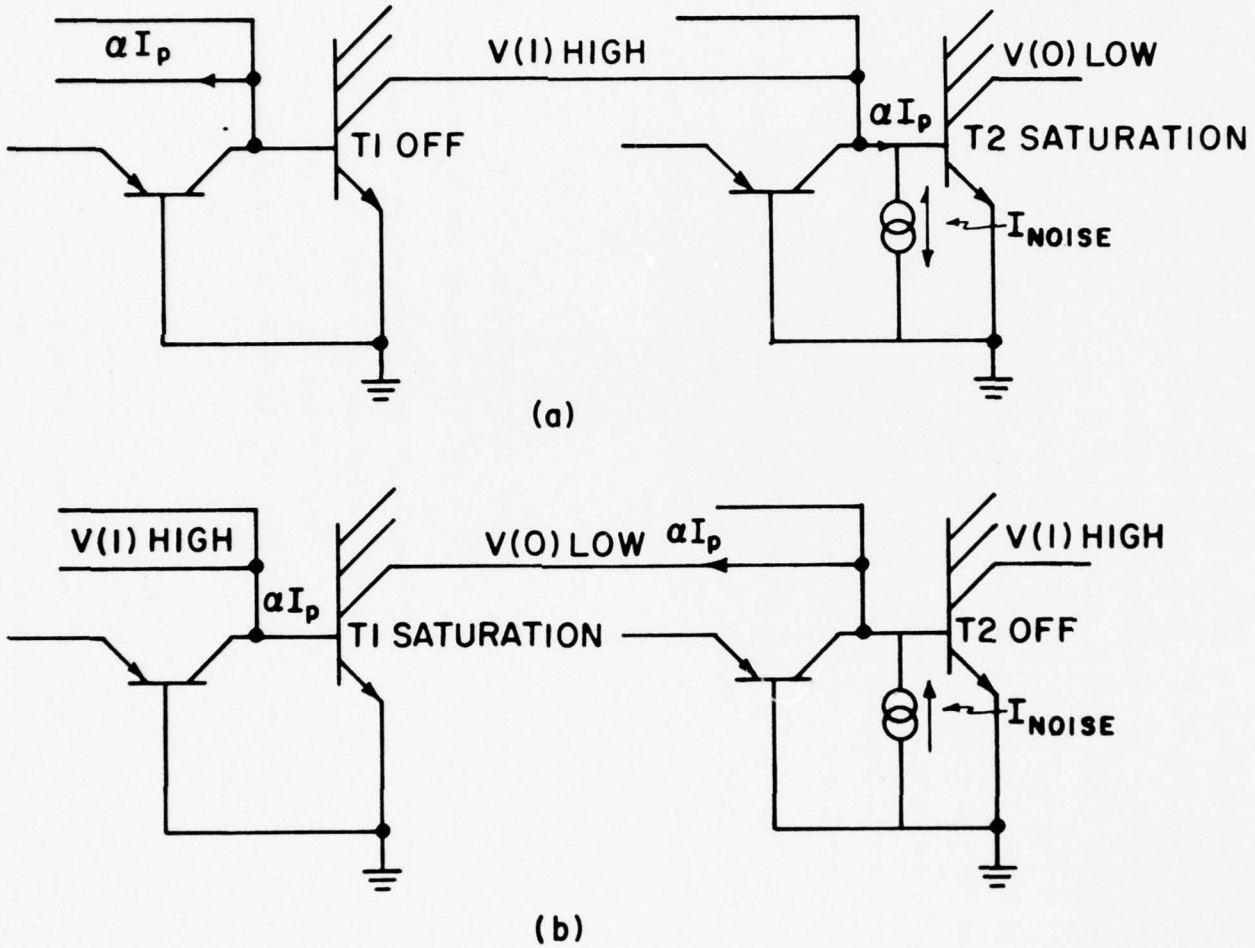


Fig. 3-7 Circuit Conditions for Current Noise Margin Calculation.

Dynamic Characteristics

Propagation delay is determined by the building up and the removal of charges, or the charging and discharging of capacitances. Depending on the location of these charges and capacitances, two components have been identified

$$t_d = t_{d\ ext}\ (\bar{I}_p) + t_{d\ int}$$

The external component is inversely proportional to the injector current I_p while the internal component is independent of I_p.

Low Current Range, $t_{d\ ext}$:

In low current ranges typically below 50-80 microamp, propagation delay is caused mainly by the charging and discharging of the depletion capacitances and the parasitic capacitances associated with metal interconnections and tunnels. Since the voltage variation is small, these capacitances remain practically unchanged; the charging and discharging times are consequently inversely proportional to the current I_p. They are the external components of t_d and can be derived using the simple relation

$$I_{charging} = C\frac{\Delta V}{t}_{charging}$$

and a similar relation for discharging.

The charging and discharging situations are shown in Fig. 3-8. Initially, T1 and T3 are "on" and T2 is "off." After switching, T1 and T3 will be "off" and T2 will be "on." The charging and discharging currents are also given in this figure.

First, the collector of T1 and the base of T2 are charged from V(0) to V(1). The charging time constant can be calculated approximately by

$$I_p \simeq (C_{cb1} + C_{eb2} + \bar{F}C_{cb2})\ \frac{V(1) - V(0)}{t_{charge}} \qquad (3 - 7)$$

Since $C_{cb1} = C_{cb2} = C_{cb}$ and $V(1) - V(0) \simeq V_{bias}$,

$$t_{charge} \simeq [C_{eb} + (F + 1)C_{cb}]V_{bias}/I_p \qquad (3 - 8)$$

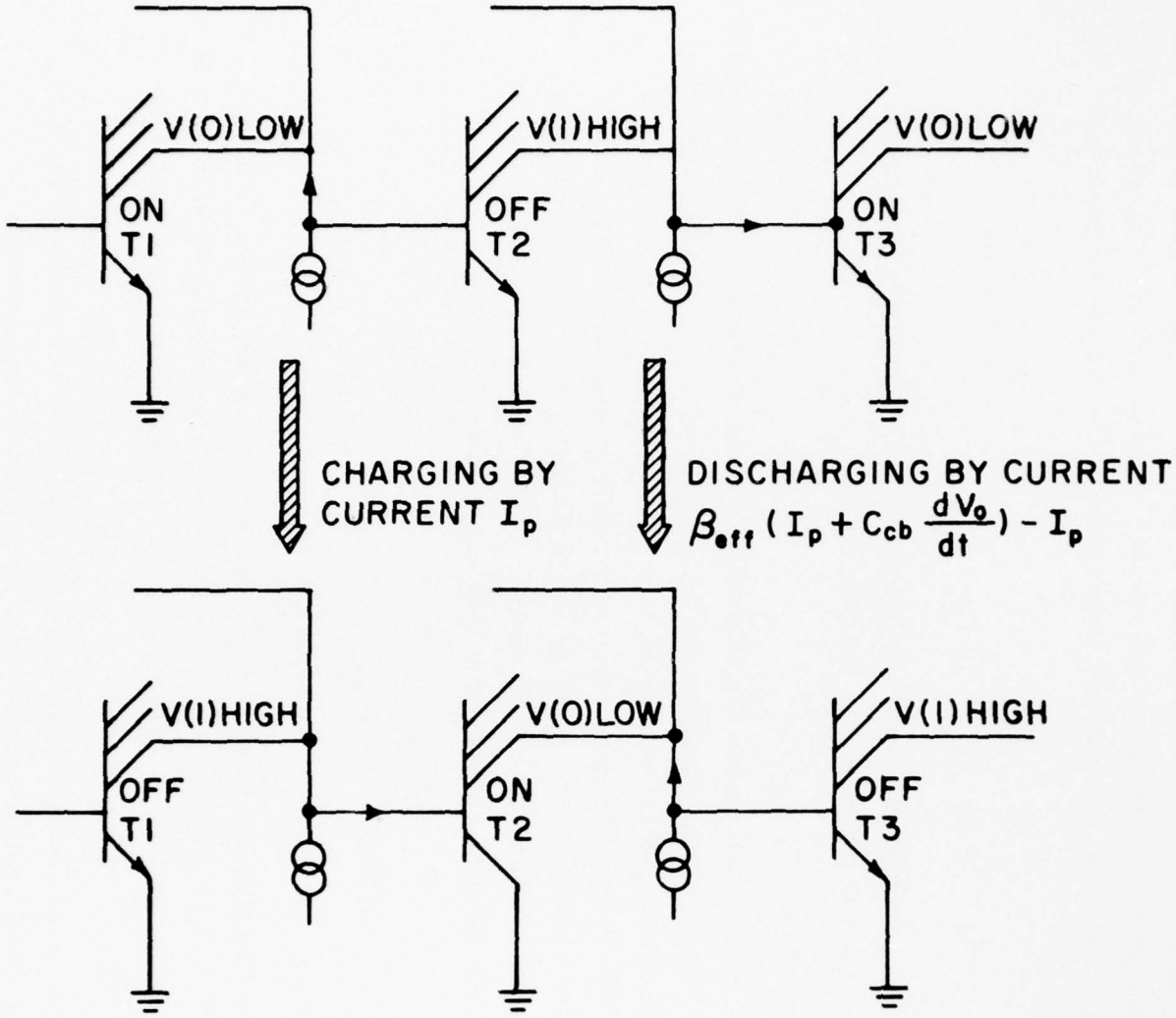


Fig. 3-8 Change of States in an I^2L/MTL Cell by Charging and Discharging of Depletion Capacitances.

Afterward, the collector of T2 and the base of T3 will be discharged from V(1) to V(0). The discharging time constant can be estimated by

$$\beta_{eff}(I_p + C_{cb}\frac{dV_o}{dt}) - I_p \simeq (C_{eb3} + FC_{eb3})\frac{V(1) - V(0)}{t_{discharge}}$$

$$t_{discharge} \simeq \{F + \beta_{eff})C_{cb} + C_{eb}\} V_{bias}/(\beta_{eff}-1)I_p \qquad (3 - 9)$$

If $\beta_{eff} \geq F$, $\beta_{eff} \geq 1$, the external component of t_d is

$$t_{d\ ext} = \frac{1}{2}(t_{charging} + t_{discharging})$$

$$\simeq [C_{eb} + (F + 2)C_{cb}]V_{bias}/2I_p \qquad (3 - 10)$$

It can be seen that $t_{d\ ext}$ decreases linearly with increasing current. It is also proportional to the number of collectors F, the voltage swing and the capacitance values. The main contribution of C_{eb} comes from the p - n^+ sidewall which can be reduced if recessed dielectric isolation collars are used. The total capacitance is typically in the range from 0.5 to 2 pF. As an example, for V_{bias} = 1 volt and I_p = 50 μa, $t_{d\ ext}$ = 10 ns if C = 1 pF.

High Current Range--$t_{d\ int}$ and minimum delay:

When I_p is increased, it will reach a value beyond which the charges stored in the epi-layer are more dominant than charges stored in the depletion layers. The total charges will be proportional to the current. Consequently, increasing I_p will no longer shorten the time to remove these charges. The propagation delay is current independent and consists of mainly the intrinsic component. It becomes the minimum delay.

It can be calculated using the following approach. The p diffusion area is split into F + 1 sections for F collectors and one base. The charges stored in each region are assumed to be Q. The time varying equation for Q is approximately

$$\frac{d}{dt}(F+1)Q = -\frac{(F+1)Q}{\tau_{eff}} + [I_p - i_p(V_o) + I_n] \qquad (3 - 11)$$

recombination building up & removing

To express $i_p(V_o)$ in terms of other known parameters, a new term τ'_{eff} is introduced by the definition

$$\frac{(F + 1)Q}{\tau'_{eff}} = \frac{(F + 1)Q}{\tau_{eff}} + i_p(V_o) \qquad (3 - 12)$$

Using the relation $(F + 1)Q/\tau_{eff} = I_n/\beta_n$, τ'_{eff} can be expressed as $\tau'_{eff} = \tau_{eff}\, \beta_{eff}/\beta_n$ where β_{eff} is another useful parameter which is defined by the following relation and can be experimentally measured.

$$\frac{1}{\beta_{eff}} = \frac{1}{\beta_n} + \frac{I_{no}}{I_{po}} \qquad (3 - 13)$$

It can be seen that the ratio I_{no}/I_{po} appears again. Using the new term τ'_{eff}, (3-12) can be rewritten as:

$$\frac{d}{dt}(F + 1)Q = - \frac{(F + 1)Q}{\tau'_{eff}} + I_p - I_n \qquad (3 - 14)$$

(3-14) is the differential equation used to determine the time required to build up and to remove the charges in the epi-layer. The detailed steps can be found in Klaassen's paper. The important result for $t_{d\ int}$ is:

$$t_{d\ int} \simeq \frac{/\overline{\beta_{eff}}}{2\pi f_T} \qquad (3 - 15)$$

Both β_{eff} and f_T are functions of fan-out F.

High Current Range--High Injection Effects:

The analysis presented before does not take into account the high injection effects. It was found that in some cases, t_d will increase from the minimum delay when I_p is further increased. In other words, the speed performance will suffer instead of being helped by injecting too much current. It is believed that this is the consequence of voltage drop across the base resistance R_b of T2. This voltage drop will cause a higher reverse flow i_p back into the pnp injector resulting in a smaller net injector current to the base of T2. Consequently, the collector current of T2 increases more slowly which lengthens the discharging time of T3.

Experimental Verification:

The dynamic analysis has been verified by measurements on a 5-stage ring oscillator. No fan-out data was given and is assumed to be 1. The results are reproduced in Fig. 3-1. Excellent agreement between theory and experiments are noted.

In Fig. 3-1, calculated results using a two-dimensional computer simulation program PHILPAC were also included. The effect of base resistance was analyzed. Using a value of 300 ohms, the calculated t_d was found to increase with I_p beyond 200-300 μ amp in agreement with the experimental finding.

Summary

Klaassen's device physics study is the most extensive analysis published for the standard I^2L/MTL cell to date. It has been well supported by experimental verifications. Its highlights are summarized in the following:

- The important device parameters are

  $\frac{I_{no}}{I_{po}}$, F, Doping concentrations, Device layout

- Device characteristics can be determined from these parameters in a straight forward manner

  For pnp: common base forward current gain β_p

  For npn: common emitter forward current gain β_n*
  transition frequency f_T^*
  capacitances C_{eb}, C_{cb}
  a new current gain β_{eff} which can be experimentally measured

- Based on these parameters and characteristics, the following circuit performance can be theoretically calculated

  static properties: transfer characteristics
  voltage noise margin, ΔV^*

  dynamic properties: propagation delay, t_d^*

Items with * sign indicate that they have been supported by experimental verifications (Fig. 3-1).

It is noted that I_{no}/I_{po} is one of the most important device parameters in Klaassen's analysis. Values from 2 to 50 were used in his study. A compromise is required to choose its value because a large I_{no}/I_{po} is desirable for good voltage noise margin while a low value is required to yield small minimum delay. In practice, the delay requirement probably is more important and will override the voltage noise margin requirement.

3.2.4 Circuit Modeling

Two early circuit models were developed by Berger and Wiedman [B74-2], [B74-3]. They are presented here in detail to complement Klaassen's analysis.

Terminal-Oriented Model

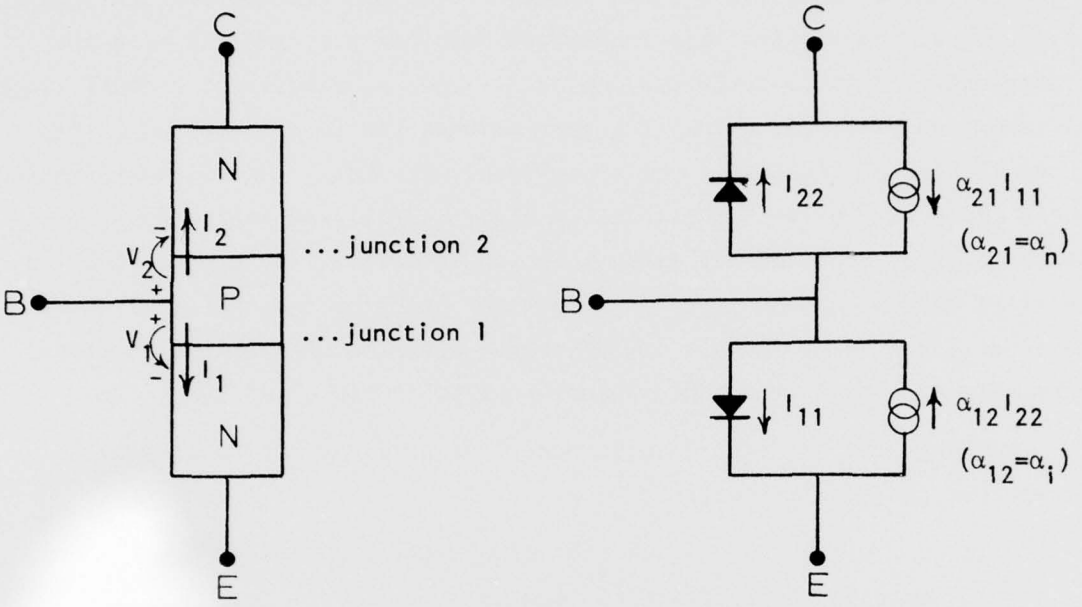
The terminal-oriented model results from a straightforward extension of the well-known Ebers-Moll (or coupled diode) modeling of bipolar transistor action. The standard Ebers-Moll model for a single npn transistor is as shown in Fig. 3-9. Note that in the Ebers-Moll formulation the total junction current I_i crossing junction i is simply modeled as a linear superposition of partial currents I_{ik} being injected (i=k) and collected (i≠k) across the junction. The current injected across a junction is

$$I_{ii} = I_{is}(e^{qV_i/kT} - 1) \qquad (3 - 16)$$

where I_{is} is the saturation current, V_i the potential drop across the junction, q the magnitude of the electronic charge, k Boltzmann's constant, and T the temperature in °K. The minority carrier current collected across a junction is some fraction α_{ik} of the current injected at the other junction which shares a common region with the collecting junction; i.e.,

$$I_{ik} = -\alpha_{ik} I_{ks}(e^{qV_k/kT} - 1) \quad ...(i\neq k) \qquad (3 - 17a)$$

$$= -\alpha_{ik} I_{kk} \qquad (3 - 17b)$$



$$I_{11} = I_{1s}(e^{qV_1/kT} - 1)$$

$$I_{22} = I_{2s}(e^{qV_2/kT} - 1)$$

Fig. 3-9. Standard Ebers-Moll circuit model for a single npn transistor.

Turning to the I^2L gate, let us assume a three collector structure as pictured in Fig. 3-10(a). The figure also defines the terminal designations to be used in subsequent discussions. E_p is the emitter terminal of the lateral pnp transistor; E_n, the emittter terminal for the vertical npn transistor; B, the vertical npn transistor base contact; and the C_j's are the vertical transistor collector contacts. Now, paralleling the usual single transistor analysis, the actual I^2L gate assumes the form exhibited in Fig. 3-10(b) when idealized into a one dimensional structure. Noting the junction numbers and total currents appearing in Fig. 3-10(b), and taking the total junction current crossing any given junction to be the linear superposition of partial currents being injected across the junction and being collected from other junctions sharing a common region with the collecting junction, one rapidly arrives at the representation given in Fig. 3-10(c).

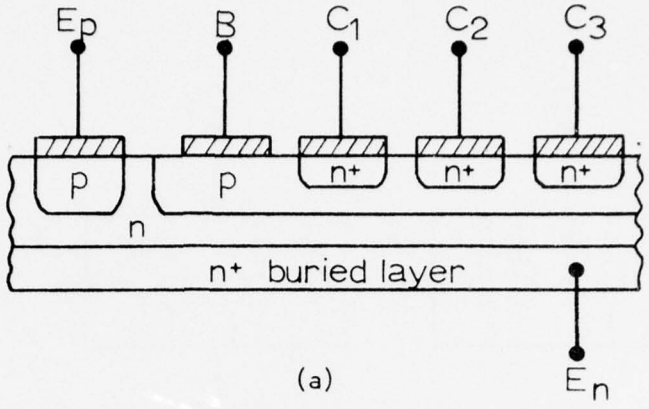
Working with the Fig. 3-10(c) model, we next make the following observations and simplifications:

(i) $\alpha_{21} = \alpha_n$, where α_n is the normal-active common-base current gain of the lateral pnp transistor.

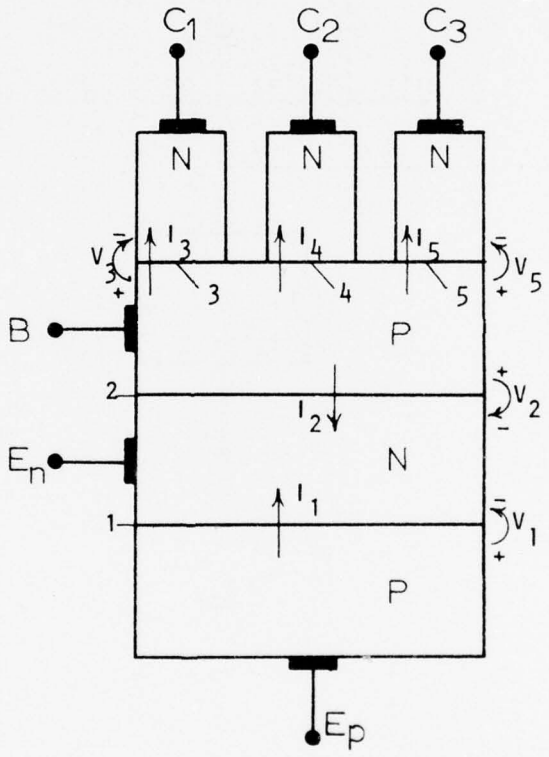
(ii) $\alpha_{12} = \alpha_i$, where α_i is the inverted-active common-base current gain of the lateral pnp transistor.

(iii) $\alpha_{32} = \alpha_{u1}$, $\alpha_{42} = \alpha_{u2}$, $\alpha_{52} = \alpha_{u3}$, where the α_{uj}'s are <u>upward</u> current gains of the vertical E_n-B-C_j transistors. The "upward" and "downward" designations have been introduced in I^2L analyses to minimize confusion. The upward current gain is the current gain associated with minority carrier injection into the vertical transistor base directed upwards toward the semiconductor surface. This corresponds to the forward (or normal) current gain in I^2L circuits and the inverse current gain in regular monolithic circuits (where the n^+ surface islands are routinely considered to be emitters.)

(iv) $\alpha_{23} = \alpha_{d1}$, $\alpha_{24} = \alpha_{d2}$, $\alpha_{25} = \alpha_{d3}$, where the α_{di}'s are <u>downward</u> current gains of the vertical E_n-B-C_j transistors. The downward current gain is the current gain associated with minority carrier injection into the vertical transistor base directed downwards from the semiconductor surface.

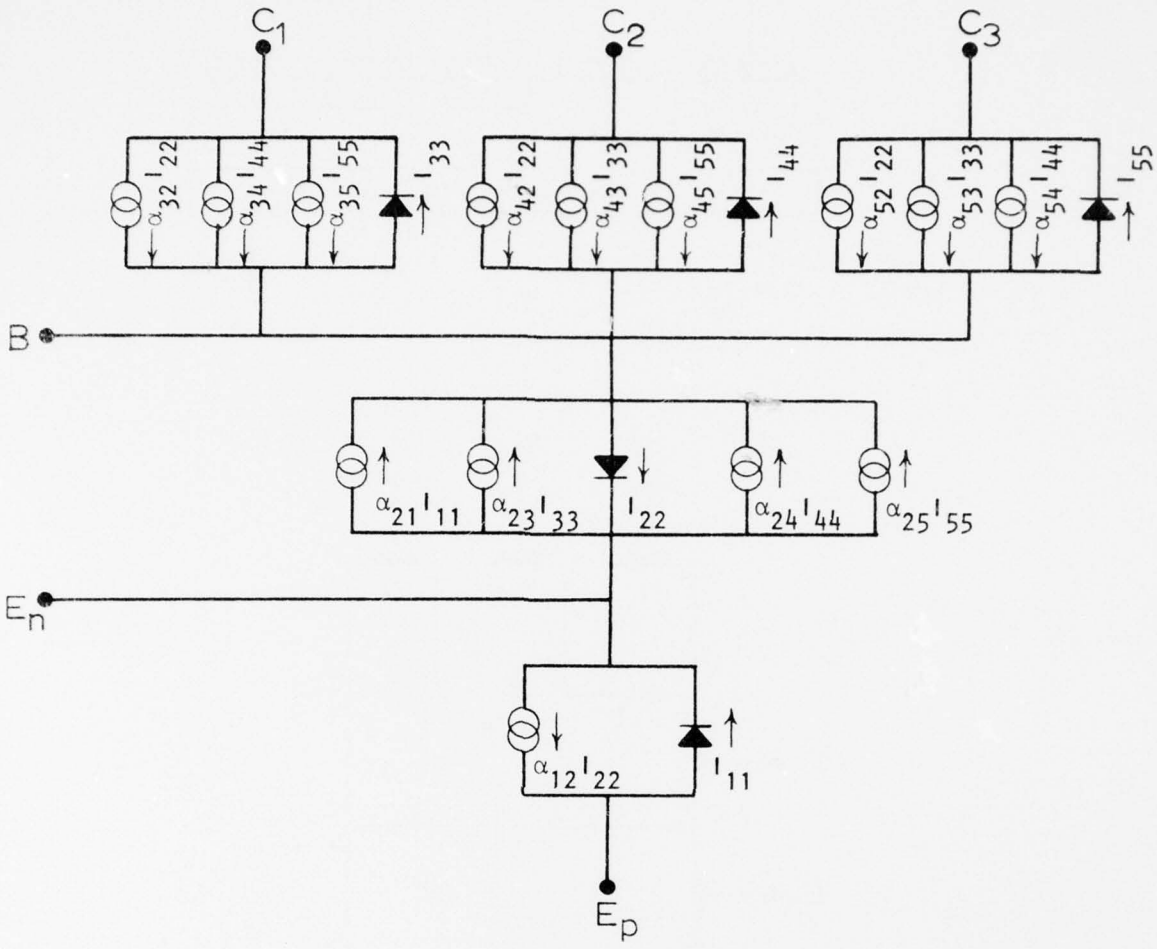


(a)



(b)

Fig. 3-10. Extending the Ebers-Moll formulation to I^2L gates. (a) Assumed structure. (b) One-dimensional form of the assumed structure.



(c)

Fig. 3-10. (continued). (c) Complete Ebers-Moll representation of an I^2L gate.

(v) The coupling between the collectors represented by Fig. 3-10(c) current generators $\alpha_{34} I_{44}$, $\alpha_{35} I_{55}$, $\alpha_{43} I_{33}$, $\alpha_{45} I_{55}$, $\alpha_{53} I_{33}$ and $\alpha_{54} I_{44}$ is assumed to be negligible, and the aforelisted current generators are to be neglected. This is justified by noting that the downward current gain of the vertical transistors (corresponding to the forward current gain in regular monolithic circuits) is expected to be very close to unity, in turn implying that nearly all of the minority carriers injected from any given n^+ island proceed into the epi-layer and very few are collected at adjacent n^+ islands.

(vi) For other than d.c. operation, junction capacitances must be added between each of the structure's terminals.

Thus, upon implementing modifications and simplifications (i)-(vi), one obtains the representation of Fig. 3-11.

At this point it is convenient to note that, under normal operational conditions, E_n is grounded and the injector rail is biased so as to hold E_p at a constant positive potential. Consequently, I_{11} in Fig. 3-11 will be a constant under these conditions, allowing $\alpha_n I_{11}$ to be replaced by a constant current cource I_o between E_n and B. Since no other circuit component in the upper two thirds of the Fig. 3-11 model depends on components in the lower one third of the model, the vertical transistor portion of the I^2L gate can be modeled as simply a multicollector transistor with an additional constant current source connected between the base and emitter.

Although the Fig. 3-11 representation is sometimes useful in itself, an alternate "partial tranistor" form finds more widespread usage. Assuming equal collector sizes (as is the usual case), each of the components in Fig. 3-11 between the E_p-E_n and E_n-B terminals can be divided into equal parts according to the number of collectors (three in our example) and the subdivided components rearranged as shown in Fig. 3-12. The correspondence between Fig. 3-11 and Fig. 3-12 circuit elements is listed in Table III-3. ($\alpha_u = 3\alpha_{ul}$ because $\alpha_{ul} I_{22} \rightarrow 3\alpha_{ul} I_{ee} = \alpha_u I_{ee}$.) Finally, using the same argument presented in the previous paragraph, each of the "partial" vertical transistors in Fig. 3-12 can be decoupled from their respective "partial"

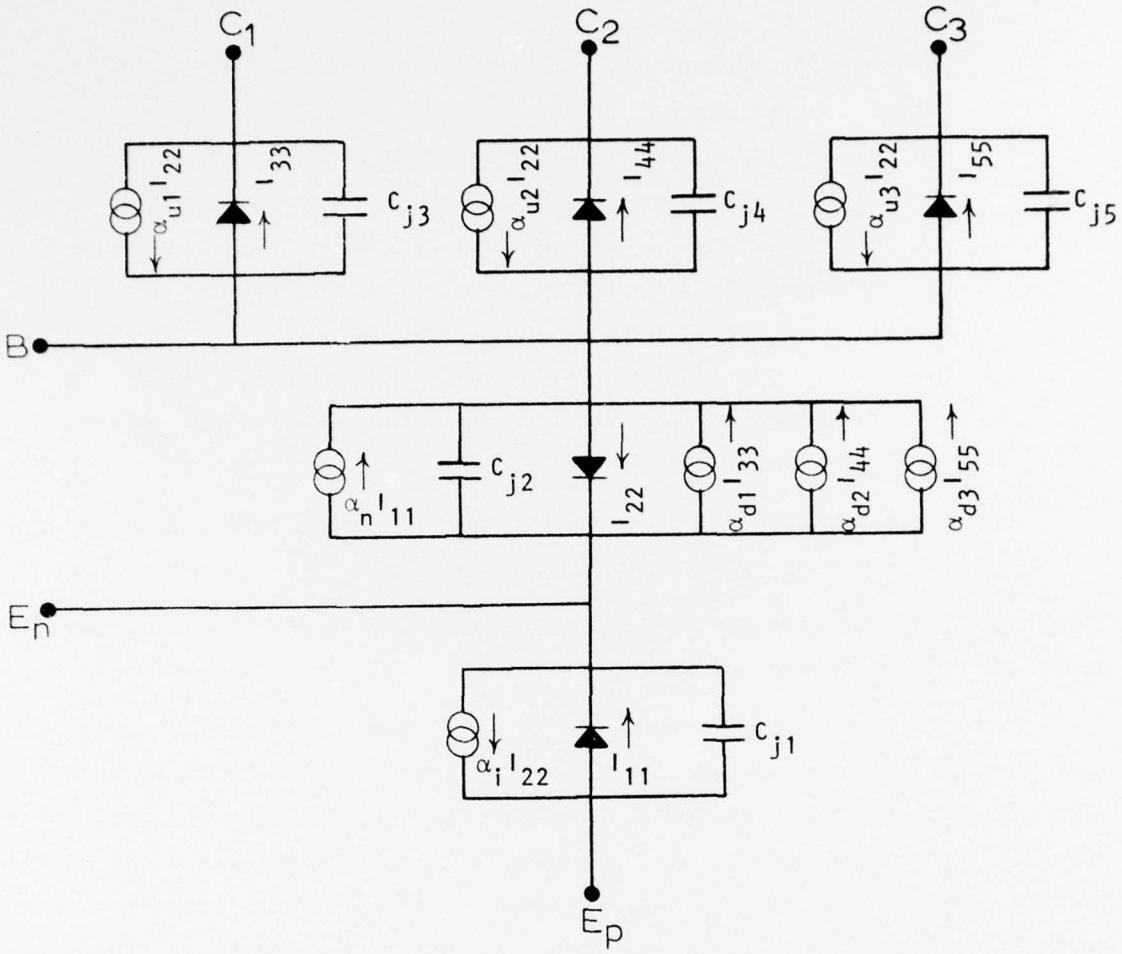


Fig. 3-[illegible] Simplified Ebers-Moll circuit model for an I^2L gate---multicollector representation.

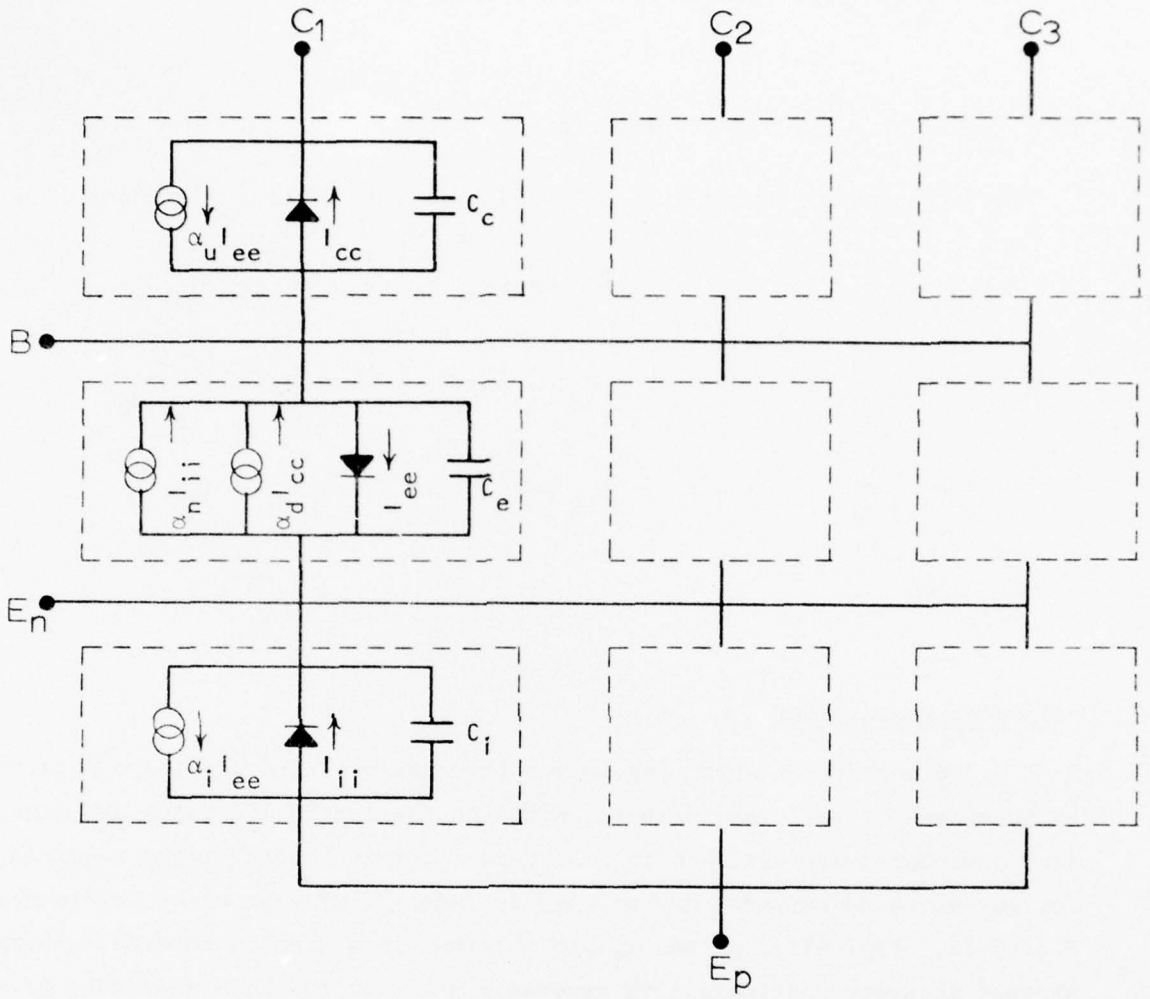


Fig. 3-12. "Partial transistor" model for an I^2L gate.

lateral transistor yielding the Fig. 3-13 representation for each of the "partial" logic associated transistors making up an I^2L gate.

Table III-3

Correspondence between Fig. 3-11 and Fig. 3-12 circuit elements.

$C_c \leftrightarrow C_{j3}$ $\quad I_{cc} \leftrightarrow I_{33}$ $\quad \alpha_u \leftrightarrow 3\alpha_{u1}$

$C_e \leftrightarrow \frac{1}{3} C_{j2}$ $\quad I_{ee} \leftrightarrow \frac{1}{3} I_{22}$ $\quad \alpha_d \leftrightarrow \frac{1}{3} \sum_{j=1}^{3} \alpha_{dj}$

$C_i \leftrightarrow \frac{1}{3} C_{j1}$ $\quad I_{ii} \leftrightarrow \frac{1}{3} I_{11}$ $\quad \alpha_n \leftrightarrow \alpha_n$

$\alpha_i \leftrightarrow \alpha_i$

Parameter Measurements

The parameters appearing in the terminal-oriented model are obtained by measurements performed directly with the fabricated I^2L gates and measurement procedures are outlined in Fig. 3-14. Terminal connections required for any given measurement may be readily deduced, of course, by reference to Fig. 3-12. Typically, α_n and α_i are obtained in a straightforward fashion, whereas accuracy considerations generally necessitate the measurement of β_u and β_d and the subsequent computation of the corresponding α's from $\beta = \alpha/(1-\alpha)$. If desired, similar measurements may also be performed to obtain the α_{uj}'s appearing in the Fig. 3-11 multi-collector model. (As a word of caution, some confusion has arisen in the literature as to precisely what upward and downward current gains are being quoted, and careful attention must be paid to the exact measurement procedures utilized.) Parameters typical of I^2L circuits are summarized in Table 3-10.

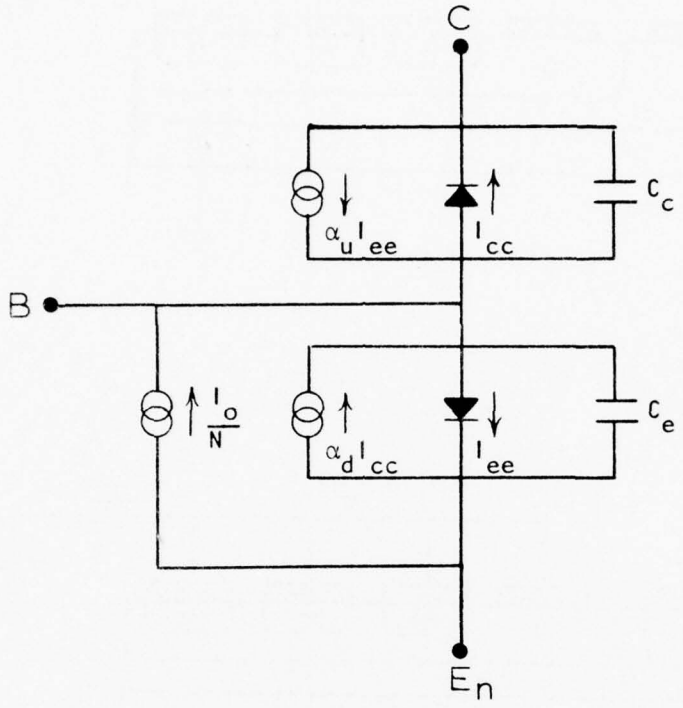
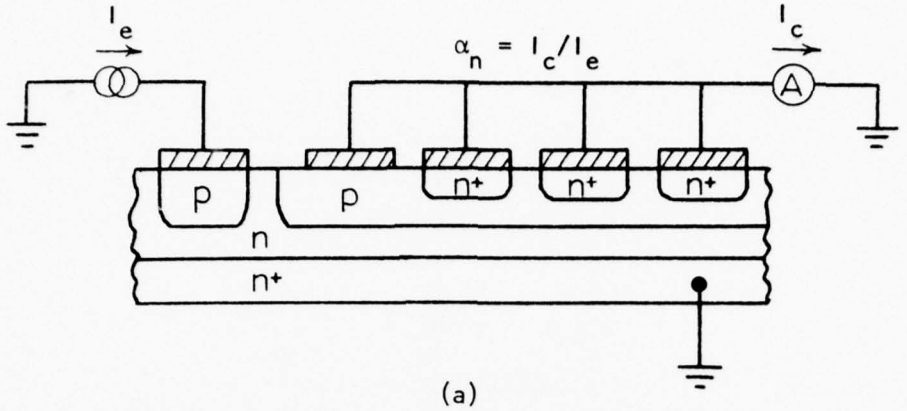
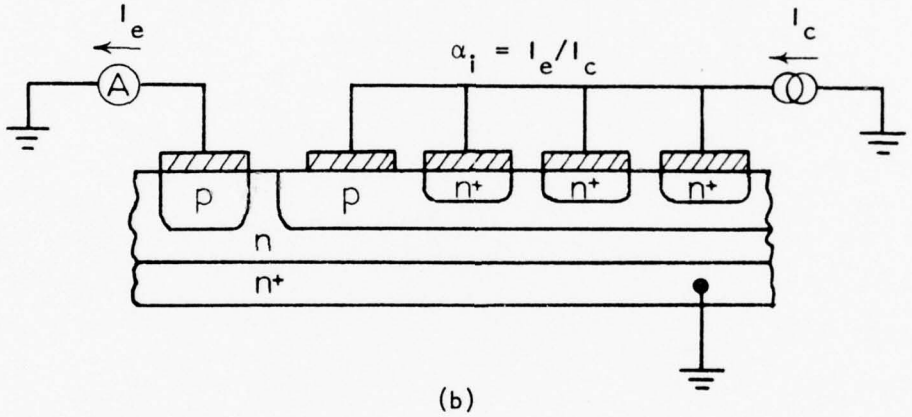


Fig. 3-13. Injector decoupled model for each of the partial switching transistors making up an I^2L gate. The symbol N appearing in this model is set equal to the number of collectors.

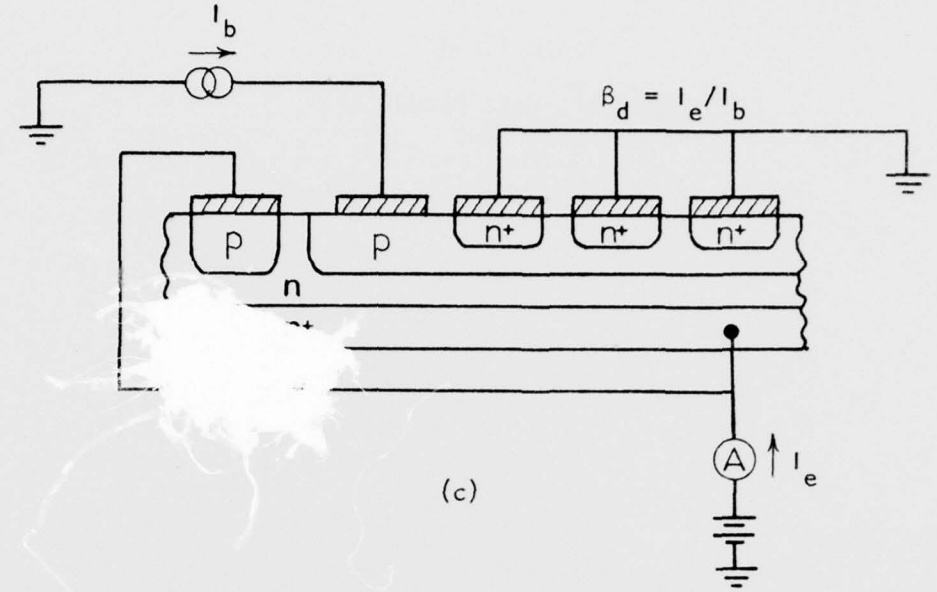


(a)

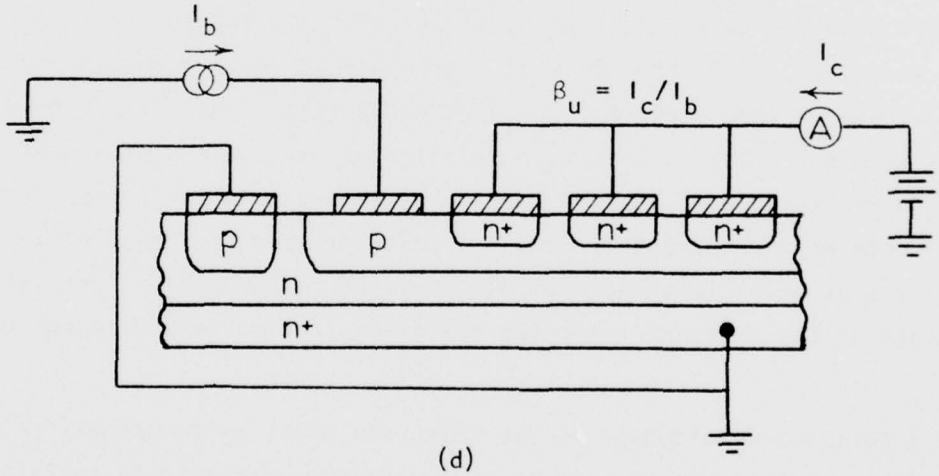


(b)

Fig. 3-14. Measurement procedures for determining terminal-oriented model parameters. (a) Forward current gain of the lateral pnp. (b) Inverse current gain of the lateral pnp.



(c)



(d)

Fig. 3-14. (continued). Measurement procedures for determining terminal-oriented model parameters. (c) Downward current gain (β_d) of the partial vertical npn transistors. (d) Upward current gain (β_u) of the partial vertical npn transistors.

Table III-4

Typical I^2L Gate Parameters

Parameter	Value
α_n	.4-.7
α_i	.5
α_d	100
α_u	10-30

Injection Model

The terminal-oriented model is an excellent analytical tool for predicting I^2L circuit performance once a specific fabrication procedure and I^2L gate layours have been established. By its very nature, however, the model provides very little physical insight into the internal operation of the sturcture and is therefore of little use in initial design considerations. Ideally, the structural designer would like a physical model which relates terminal currents to internal device parameters, such as base widths, diffusion profiles, etc. Unfortunately, at this time a truly physical model (which would be understandably complex) does not exist. What does exist is a quasi-physical model relating terminal currents to physically identifiable components of the internal injection currents---the so called injection model.

A detailed development of the injection model is inappropriate for the purposes of this report, and we thus endeavor here only to explain the basic concepts involved and concentrate primarily on the physical insight derived from the model. In establishing the injection model one tacitly assumes carrier injection occurs only vertically or horizontally across structural junctions, and, looking inside the I^2L gate structure, one partitions internal injection currents as to carrier type, vertical or lateral carrier motion, and positioning within the structure. This procedure is illustrated in Fig. 3-15 for two specific biasing conditions.

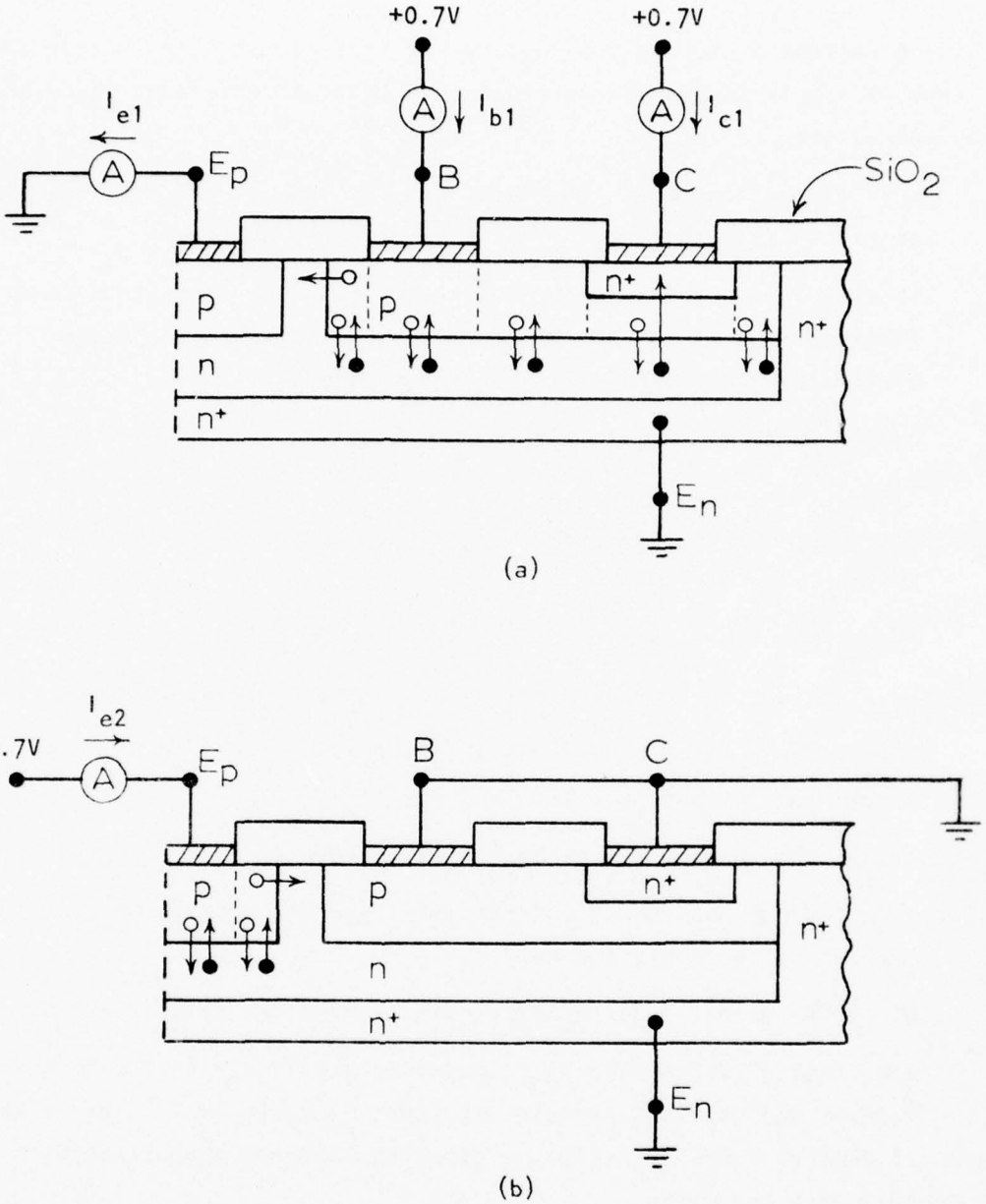


Fig. 3-15. Identification of injection model current components (a) across the npn emitter-base junction and (b) across the pnp emitter-base junction.

(A single collector structure is assumed in this illustration merely for the sake of simplicity.) The internal injection currents identified in Fig. 3-15(a) are:

I_{p11}...hole current injected laterally from the base of the vertical npn transitor into the base of the lateral pnp transistor.

I_{pv1}...total hole current injected vertically into the n-type epi-layer. (This current is the summation of all hole currents injected vertically across the emitter-base junction.)

I_{n01}...total electron current injected vertically toward an oxide covered surface.

I_{nM1}...electron current injected vertically toward the metalized base contact.

I_{nC1}...electron current injected vertically toward the n^+ collector island.

The internal injection currents identified in Fig. 3-15(b) include:

I_{p12}...hole current injected laterally from the emitter into the base of the lateral pnp transistor.

I_{pv2}...total hole current injected vertically into the n-type epi-layer.

I_{n02}...electron current injected vertically toward the oxide covered portion of the pnp's emitter.

I_{nM2}...electron current injected vertically toward the metalized E_p contact.

Now, taking volume recombination to be negligible in the base regions of the lateral and vertical transistors (this is equivalent to assuming base transport factors equal to unity---a situation closely approximated in I^2L structures), one can write

$$I_{e1} = I_{p11} \tag{3 - 18}$$

$$I_{b1} = I_{p11} + I_{pv1} + I_{n01} + I_{nM1} \tag{3 - 19}$$

$$I_{c1} = I_{nC1} \tag{3 - 20}$$

$$I_{e2} = I_{p12} + I_{pv2} + I_{n02} + I_{nM2} \tag{3 - 21}$$

In words, the preceding equations state that, for biasing case 1 [Fig. 3-15(a)]: the E_p terminal current is equal to the hole current injected laterally from the npn transistor base; the current flowing into B supplies the holes required for injection from the npn transistor base into the lateral transistor base and epi-layer in addition to the holes required for recombination at the matalized base contact and at oxidized surfaces; the collector current is the result of electron injection across the transistor base into the n^+ island. For biasing case 2 [Fig. 3-15(b)], the injector current supplies the holes required for injection from the pnp emitter into the lteral transistor base and epi-layer in addition to the holes required for recombination at the metalized emitter contact and at the oxidized emitter furface.

Upon examining eqs. (3-18) - (3-21), it should be obvious that I_{p11} and I_{nC1} can be measured directly. Suppose, in addition, second and third structures were constructed and biased as visualized in Fig. 3-16. For the "collector replaced by oxidized surface" structure of Fig. 3-16(a), one can write (assuming no other structural modifications)

$$I'_{b1} = I_{p11} + O_{pv1} + I'_{n01} + I_{nM1} \qquad (3 - 22)$$

where the prime in I'_{n01} indicates a change in the oxidized surface component relative to the Fig. 3-15(a) case. Likewise, for the "collector replaced by matalized base contact" structure of Fig. 3-16(b), one obtains

$$I''_{b1} = I_{p11} + I_{pv1} + I_{n01} + I'_{nM1} \qquad (3 - 23)$$

where the prime in I'_{nM1} indicates a change in the electron current component injected vertically toward the metalized base contact. Subtracting (3-19) from (3-22) yields $I'_{b1} - I_{b1} = I'_{n01} - I_{n01}$. Thus a measurement of base terminal currents and a knowledge of the oxidized surface areas allows one to deduce I_{n01}. Similarly, subtracting (3-19) from (3-23) yields $I''_{b1} - I_{b1} = I'_{nM1} - I_{nM1}$. Since I_{p11} can be measured directly as previously noted, the remaining case 1 component, I_{pv1}, can be calculated from $I_{pv1} = I_{b1} - I_{p11} - I_{n01} - I_{nM1}$. Finally, I_{pv2}, I_{n02}, and I_{nM2} can be computed from the corresponding case 1 components employing geometrical considerations and I_{p12} calculated from

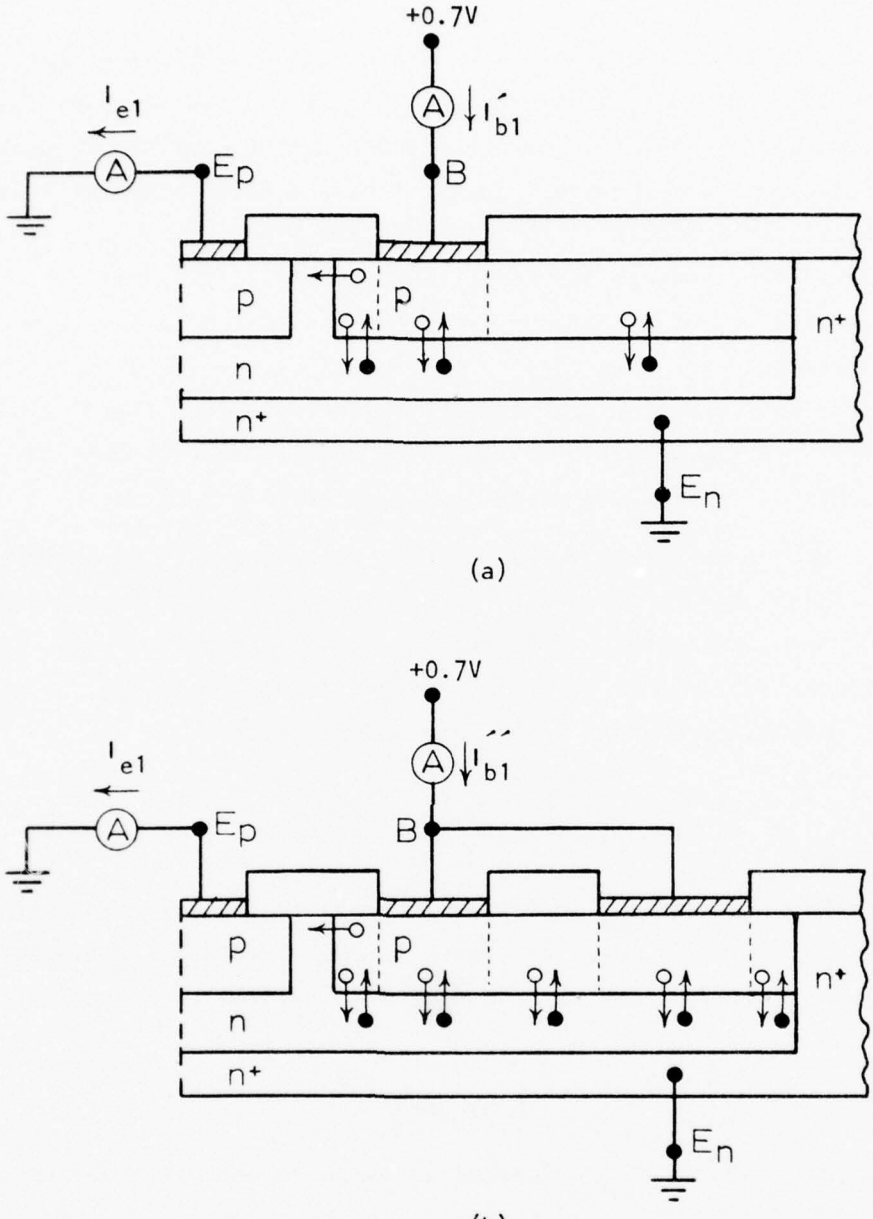


Fig. 3-16. Structural modifications employed in the injection model analysis. In (a) the collector is replaced by an oxidized surface and in (b) the collector is replaced by a metalized base contact.

$I_{p12} = I_{e2} - I_{pv2} - I_{n02} - I_{nM2}$ after measuring I_{e2}. In other words, all of the physically related internal current components of interest in an I^2L structure, the injection model components, could be deduced by experimentation as just described.

Experiments have in fact been performed using structures of the type pictured in Figs. 3-15 and 3-16, and the internal current components deduced as described in the preceding paragraph. The results of these experiments are summarized in Fig. 3-17. Although the quoted results are understandably dependent on the precise parameters (surface areas, diffusion depths, base widths, etc.) of the test structures, they are nevertheless fairly representative of I^2L structures in general.

In examining Fig. 3-17(a), note that a large percentage (85%) of the vertical base current is spent on back injection into the lateral transistor (I_{p11}) and surface recombination currents (I_{n01} and I_{nM1}). On the other hand, I_{pv1}, corresponding to hole injection across the entire extent of the vertical base-epitaxial layer junction, is relatively low, taking up only 15% of the base current. The foregoing result may come as somewhat of a surprise since the vertical base-epitaxial layer junction is a p-n^- type junction and, without further considerations (to be undertaken in the next subsection), one might expect hole injection to totally dominate electron injection. The small amount of vertical hole injection in these structures, we might add, also leads to a large intrinsic upward current gain for the vertical transistors. $\beta_u^{(i)}$, defined as $I_{nC1}(=I_{c1})$ divided by that portion of I_{pv1} injected toward the n^+ collector*, was 180 for one test structure and 226 for a second test structure! The measured extrinsic upward current gain, $\beta_u = I_{c1}/I_{b1} \simeq 10$, was consistent with typically observed values and reflected of course gain degrading base current losses.

Lastly, examining Fig. 3-17(b), note that a majority (72% in the test structure) of the forward injector current is directed toward the vertical transistor base, as desired for efficient operation and low power consumption.

*This definition assumes a base transport factor equal to unity.

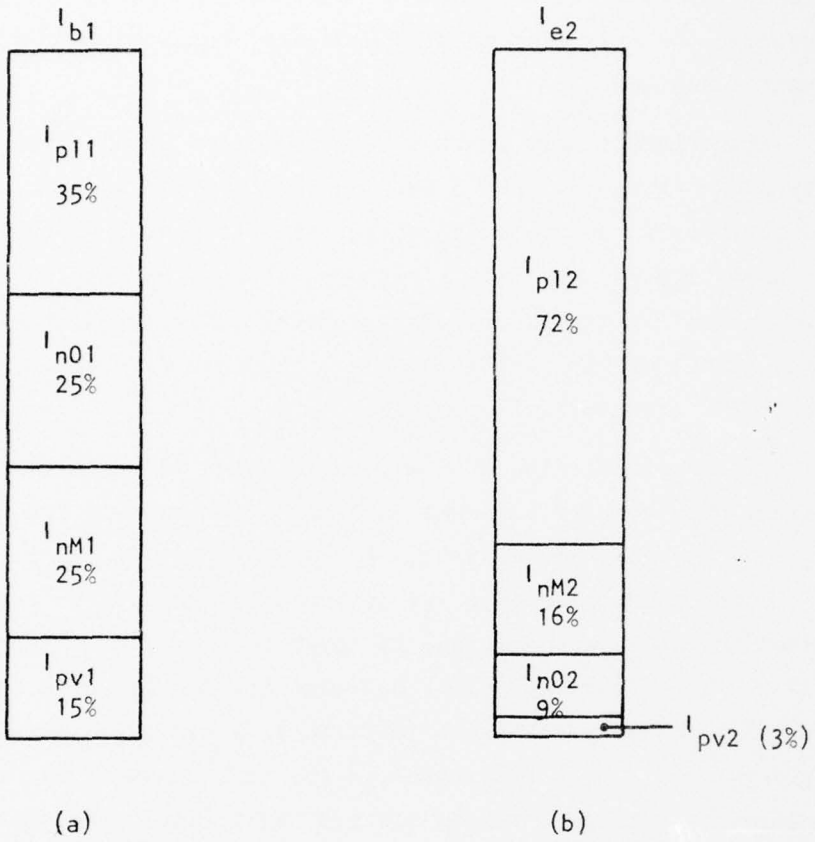


Fig. 3-17. Percentage contribution of injection current components to (a) the vertical npn transistor base current when the injector is grounded and to (b) the current flowing into the injector when the npn base is grounded.

Again vertical hole injection (I_{pv2}) is seen to be relatively low, with electron injection and subsequent recombination at metalized and oxidized surfaces dominating forward injection current losses.

Upward Current Gain

We address ourselves here to the question, "Why is the extrinisic upward current gain (β_u) of the vertical n^--p-n^+ transistors so high in I^2L structures?" It is a well-known fact that hole injection will totally dominate electron injection in a wide-base n^--p diode. If this be the case, then hole injection should dominate over electron injection across the epitaxial layer-base junction in the I^2L vertical transistor, the upward emitter efficiency should in turn be poor, and hence the intrinsic current gain should be quite low. Furthermore, the I^2L emitter to collector ratio is adverse and a "parasitic" lateral transitor current adds to the vertical transistor base current. Consequently, one might apriori expect a very low extrinsic upward current gain.

Our injection model considerations revealed that the extrinsic upward current gain is indeed reduced by a large portion of the base current being wasted on other than intrinsic transistor action. However, those considerations also revealed a very high intrinsic current gain, and hence a respectable $\beta_u \geq 10$, arising from a dominance of electron injection over hole injection across the epi-base junction. Granting a high β_u results from favorable carrier injection across the epi-base junction, there still remains the question of why the carrier injection itself is favorable.

First of all, it should be recognized the n^- region is quite thin, much shorter than a minority carrier diffusion length in I^2L structures; i.e., the n^- region is not a "wide-base" region and the n^+ buried layer must be included in any injection analysis. With this realization, one can conceive of two possibilities. (1) The n^+ buried layer acts as a sink for minority carriers, with the excess minority carrier concentration in the n^- region vanishing at the n^+-n^- junction. (2) The n^+-n^- junction presents an additional potential barrier to the diffusion of holes into the emitter, thereby causing a pile-up of holes in the n^- region and very little hole injection into the n^+ region. The second possibility appears to be in

agreement with experimental observations. If the n^+ buried layer acted as a sink for minority carriers, the predicted hole to electron injection ratio would be even less favorable than that expected from a n^--p wide-base diode. On the other hand, if the n^+-n^- junction presents an additional potential barrier to the diffusion of holes into the emitter, electron injection will dominate hole injection across the n^+-n^--p junction.

Arguing from a lightly different viewpoint, hole injection/electron injection is >> 1 in a n^--p wide-base diode and electron injection/hole injection is >> 1 in a n^+-p wide-base diode. Performing a gedunken experiment where the n^- region in a n^+-n^--p diode is systematically reduced from ∞ to 0, one should expect a corresponding systematic change from hole injection/electron injection >> 1 to electron injection/hole injection >> 1. Likewise, it is logical to expect the reversal of the injection ratio will begin when the width of the n^- region is comparable to the hole diffusion length in this region. Our conclusion then is that the n^+ buried layer-n^- epitaxial layer-p base junction in I^2L structures functions in a manner similar to a wide-base n^+-p diode. There will be an excess hole concentration in the n^- region (a hole storage) and an associated recombination-generation current. This, however, will have little effect on the electron to hole injection ratio.

Current Hogging

In the operation of Direct-Coupled Transistor Logic (DCTL) current suppled from the output of one stage to the input of subsequent gates is found to be distributed unevenly between the input gates. This phenomena is called "current hogging" and can lead to improper functioning of the logic circuit. Introductory literature descriptions of I^2L have frequently capitalized upon circuit similarities between DCTL and I^2L, and it is therefore natural to ask whether current hogging effects are present in the operation of I^2L structures. When applied to I^2L, the current hogging question more specifically assumes the form, "Does current flowing into one collector of the multicollector vertical transistor affect current flowing into any other collector?"

To answer the question we have posed, consider the measurement visualized in Fig. 3-18. With E_n and E_p grounded (hence $I_o = 0$) and with the base current held constant at $2I_b$ (an I_b input for each of the two partial transistors), I_{c1} is monitored as a function of I_{c2} ($0 \leq I_{c2} \leq I_{c1}$). The device model utilized is of course a two collector adaptation of Fig. 3-12. Noting $I_{ee1} = I_{ee2}$ because the B-E_n bias is the same for both partial transistors, and taking $I_{cc1} = 0$ (the B-C_1 junction is assumed to be back biased more than a few kT/q), one can readily solve the Fig. 3-18 circuit to obtain

$$I_{c1} = \frac{2\alpha_u}{2 - (1+\alpha_d)\alpha_u} I_b + \frac{\alpha_u(1-\alpha_d)}{2 - (1+\alpha_d)\alpha_u} I_{c2} \qquad (3 - 24)$$

or

$$\frac{I_{c1}}{\beta_u I_b} = \frac{2 - 2\alpha_u}{2 - (1+\alpha_d)\alpha_u} + \frac{u(1-\alpha_d)}{2 - (1+\alpha_d)\alpha_u} \frac{I_{c2}}{\beta_u I_b} \qquad (3 - 25)$$

$I_{c1}/\beta_u I_b$ vs. $I_{c2}/\beta_u I_b$ specified by eq. 3-25 is plotted in Fig. 3-19 for two sets of gains, ($\beta_d = 100$, $\beta_u = 10$) and ($\beta_d = 0.5$, $\beta_u = 33$). With $\beta_d = 100$ and $\beta_u = 10$, typical I^2L structural gains, there is very little predicted current hogging; i.e., I_{c1} is essentially independent of I_{c2}. However, with $\beta_d = 0.5$ and $\beta_u = 33$, I_{c1} is a strong function of the C_2 collector current. This latter set of gains is typical of standard gold doped logic circuits if one identifies β_u as the forward current gain (actually the downward current gain in standard circuits where the n^+ - islands are identified as emitters) and β_d as the inverse current gain.

The foregoing analysis can be extended to 3, 4 and 5 collector structures by concentrating on the worst case situation where one collector is drawing current and all other collectors are open circuited. The net conclusion, however, remains the same---current hogging is not expected to be a problem in I^2L circuits because of the intrinsically high inverse (downward) current gains routinely achieved in I^2L structures. Direct experimental confirmation of this theoretically based conclusion has been achieved using matched transistor pairs and with actual I^2L gates. The I^2L gate experimental results are presented in Fig. 3-20.

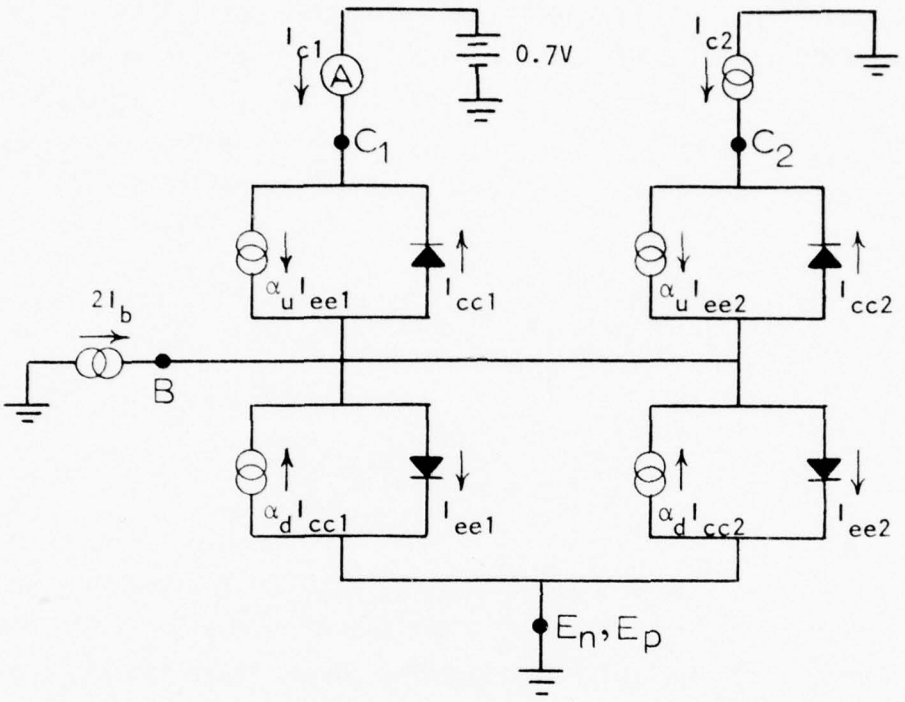


Fig. 3-18. Envisioned current hogging measurement using a two collector gate.

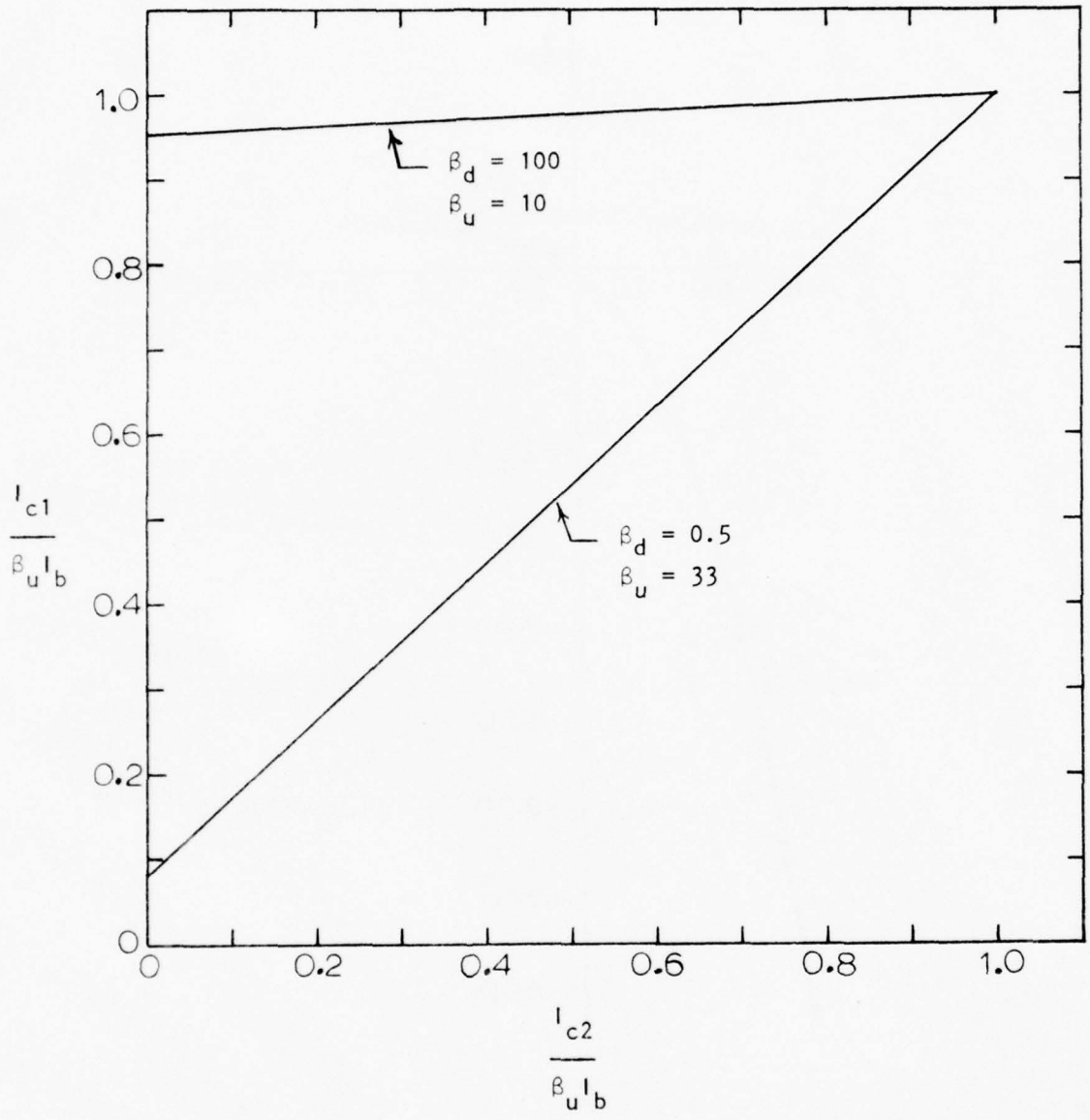


Fig. 3-19. Predicted interdependence of collector currents in a bicollector structure for two assumed sets of upward-downward current gains.

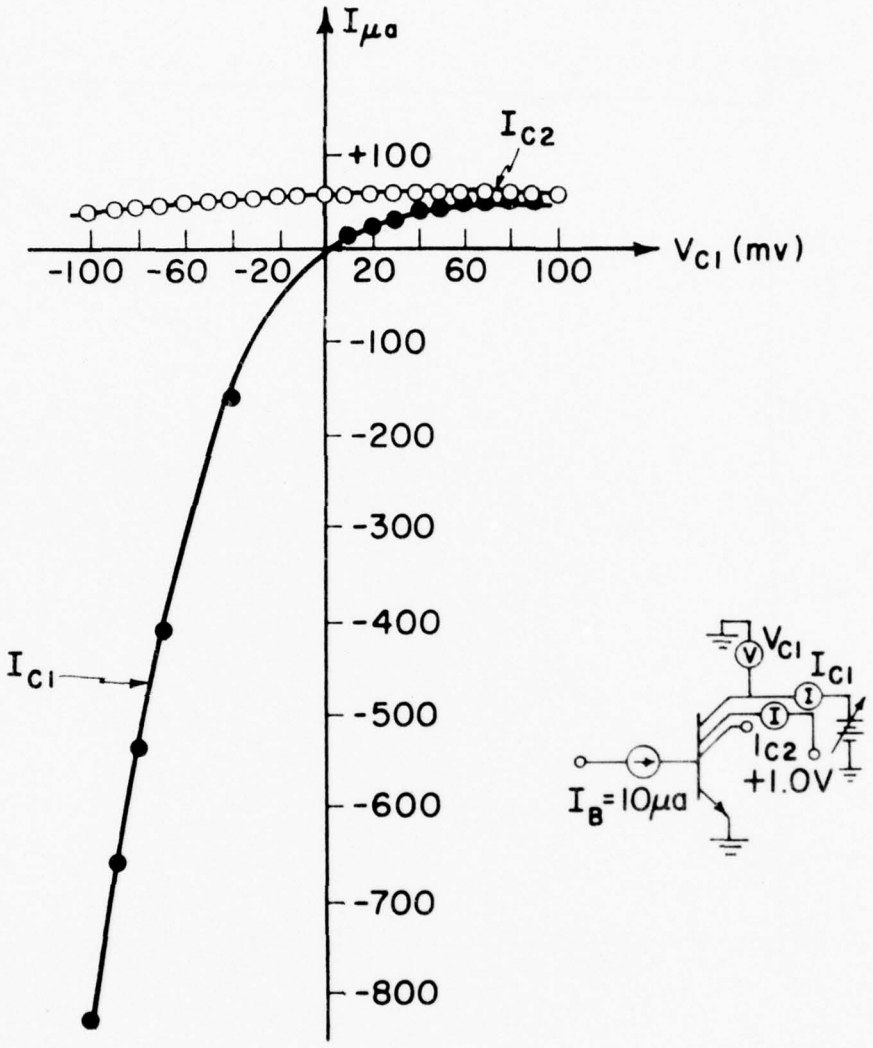


Fig. 3-20 Measured Interdependence of I^2L Gate Collector Currents Derived From Bell Laboratory Unit 6402B012. The Insert Provides Specific Measurement Details.[4]

Klaassen stated that the charges responsible for the minimum delay are mainly located in the epi-layer. Without giving detailed calculations, Berger and Wiedman's modeling studies are able to calculate not only the amount of charges but also their contributions to propagation delay in greater detail. They divided the charge, current and propagation delay into several components associated with either holes or electrons located at different parts of the cell. Such detailed breakdown provides a great deal of insight into the methods which could be used to reduce the minimum delay.

Although using different device characteristics in formulating the analysis, these two circuit models have the same objective and share some common approaches. One of the most important is the concept of time constant associated with charge storage. They are defined by the basic relation

$$\begin{matrix}\text{stored} \\ \text{charge}\end{matrix} = \begin{matrix}\text{current responsible} \\ \text{for these charges}\end{matrix} \cdot \begin{matrix}\text{time} \\ \text{constant}\end{matrix}$$

The most important case is the npn emitter:

$$Q_e = I_e \cdot \tau_e$$

It can be broken down into five components

$$\begin{matrix}\text{emitter} \\ \text{charges}\end{matrix} = \begin{matrix}\text{holes due} \\ \text{to downward} \\ \text{injection}\end{matrix} + \begin{matrix}\text{holes due} \\ \text{to lateral} \\ \text{injection}\end{matrix} + \begin{matrix}\text{electrons} \\ \text{under base} \\ \text{contact}\end{matrix} + \begin{matrix}\text{electrons} \\ \text{under} \\ \text{collectors}\end{matrix} + \begin{matrix}\text{electrons} \\ \text{beyond these} \\ \text{regions}\end{matrix}$$

$$I_e \tau_e = I_{pv} \tau_{pv} + I_{p\ell} \tau_{p\ell} + I_{nc} \tau_{nc} + I_{ni} \tau_{ni} + I_{no} \tau_{no} \qquad (3 - 26)$$

Electrons are all injected upwards. The emitter time constant is also used to normalize all other time constants.

In the terminal model, the effects of current gains β_u and β_d on $t_{d_{int}}$ were analyzed. The results are presented in two ways. In Fig. 3-3a, $t_{d_{int}}/\tau_e$ is plotted as a function of normalized collector constant τ_c/τ_e for different β_u, β_d and fan-out. A more useful figure is shown in Fig. 3-3b in which $t_{d_{int}}/\tau_e$ is plotted as a function of the common emitter upward current gain β_u for different fan-out and ratio of β_u/β_d as a parameter is the result of their observation that it remains approximately constant when β_u is varied

for optimization. Caution must be exercised in interpreting this figure to the effect that $t_{d_{int}}$ will be increased when β_u is increased. This implies that a higher current gain could be detrimental to speed performance which contradicts the common sense position that larger collector current, in general, speeds up the response. That this is a fallacy is apparent if it is recognized that τ_e is inversely proportional to β_u.

$$\tau_e \sim \frac{1}{I_e} \sim \frac{1}{mI_{ni}} \sim \frac{1}{\beta_u} \qquad (3 - 27)$$

Therefore, $t_{d_{int}}$ will decrease but not in linear proportion with increasing β_u.

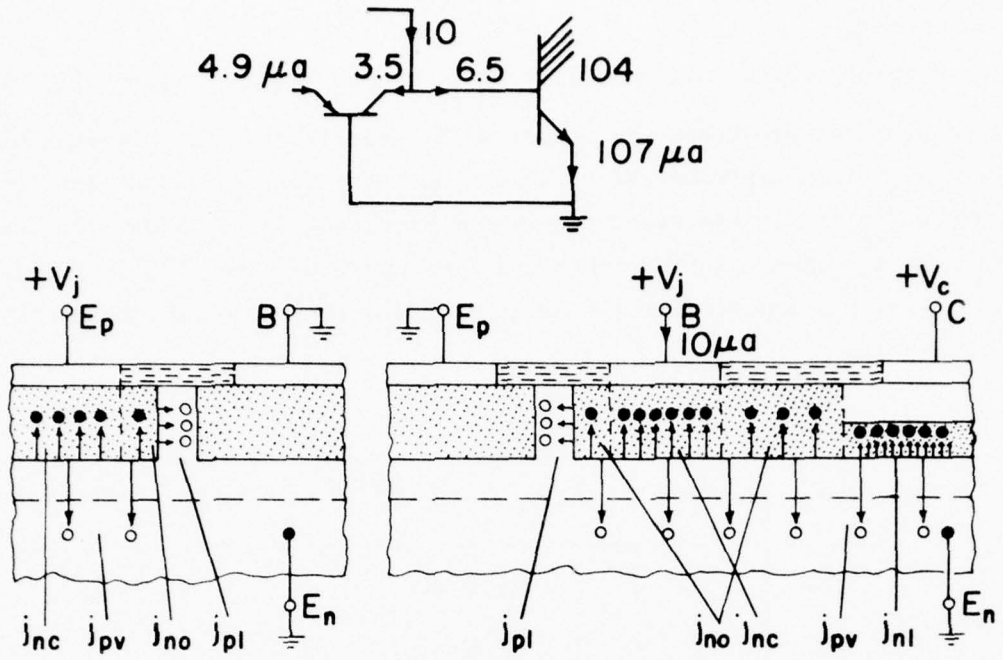
It is obvious that τ_e must first be determined in order to use the terminal model. Unfortunately, the terminal model is not able to calculate τ_e directly. Such a drawback was overcome in the injection model, in which current components as well as charge and time constant components are used in formulating the model. They can be calculated directly from device parameters.

Their results for the minimum delay study can be summarized in Fig. 3-21 for a standard MTL cell of 4 collectors. It was found that the largest component of charge storage is due to the holes in the epi-layer. It amounted to a whopping 67.4%. Their contribution to τ_e is also large in proportion, not linearly, but weighted by their corresponding current.

$$\tau_e = (\Sigma I_v \tau_v)/I_e \qquad (3 - 28)$$

An effective method to reduce this component is to decrease the epi-layer thickness. The second important component is due to electrons in regions beside the base contact and the collectors. It amounted to 16.48%. The effective way to reduce this component is obviously by reducing the area not covered by the base and the collectors without getting into short circuit problems between contacts. Another effective way is by using isolation collars (dielectric is better than n^+ diffusion). The third large component is due to electrons under the collectors and is 12.47%. They reported that for the MTL devices investigated, τ_e can be well approximated by

$$\tau_e = 30 \text{ ns}/\beta_u$$



		$j_{p\ell}$	j_{no}	j_{nc}	j_{pv}	j_{ni}	Total
npn base current (μa)		3.5	2.5	2.5	1.5		10
npn collectors current (μa)						4x26	104
time constant component (ns)		2	22	2	150	0.4	
charge storage	1_τ	7	55	5	225	41.6	333
	%	2.1	16.48	1.5	67.4	12.47	100
contribution to emitter constant (ns)		0.07	0.5	0.05	2	0.4	3

Fig. 3-21 Summary of Current, Stored Charge and Emitter Time Constant Components in Injection Model Analysis (B74-3).

τ_e is determined, the minimum delay $t_{d_{int}}$ can be found by using Fig. 3-3. This analytical procedure was supported by experimental measurements also. In achieving the experimental verification, they have to adjust the time constant τ_{pv} to fit the measured emitter time constant τ_e. One this is done, the agreement for currents and time constants are close. Furthermore, using the empirical relation $\tau_e = 30/\beta_u$, they also reported satisfactory agreement for $t_{d_{int}}$.

β_u	β_d	$t_{d_{int}}$ (calculated)	$t_{d_{int}}$ (measured)
12	55	15.5 ns	13.5 ns
18	80	11.5	10

3.2.5 Effects of Device Parameters on t_d-I_p Characteristics

The propagation delay-injector current plot is probably the most useful characteristic to describe circuit performance. Both the device physics and the circuit modeling analysis presented in the last two sections can be used to calculate this characteristic. Two dimensional computer simulations have also been developed (but not yet published) which can perform even more extensive device calculations. Therefore, families of such characteristics for different device parameters can be generated on computers for design optimization. However, the validity of these calculations must be checked by experimental results investigating the dependence of t_d - I_p characteristics on several parameters.

Dependence on Epi-layer Resistivity

In Fig. 3-22, t_d - I_p characteristics for three different epi-layer resistivities are shown. It is noted that optimization for low power consideration and for fast speed consideration are different. For low power performance, 0.6Ω-cm is preferred. For high speed performance, 0.3Ω-cm seems to be superior.

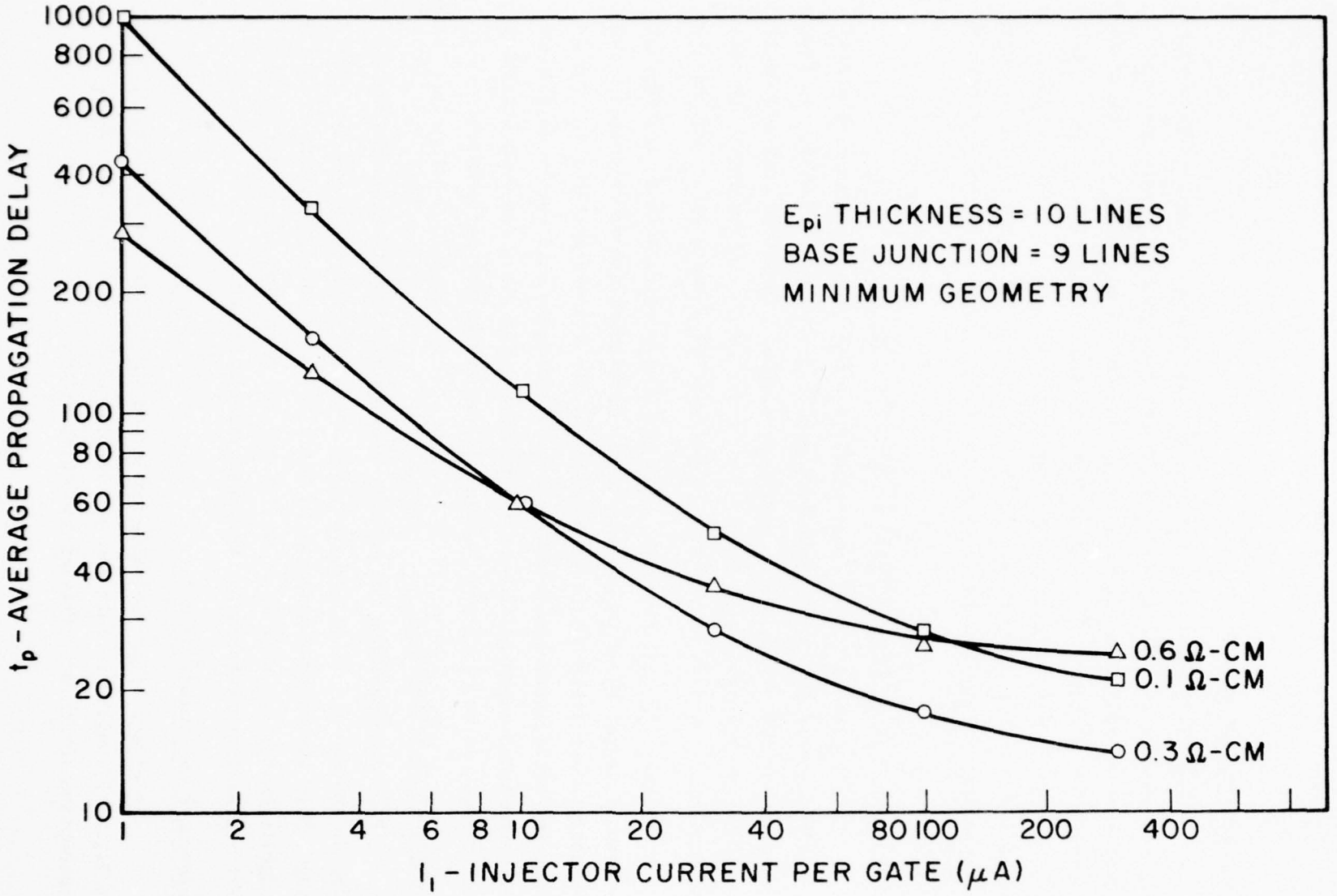


Fig. 3-22 Dependence of t_d-I_p Characteristics on Epi-layer Resistivity (Texas Instrument Data).

Dependence on npn Base Width

In Fig. 3-23, the effect of the npn base width is shown. These data were measured on two MTL cells which were fabricated by the same process except that an additional drive-in step was applied to one of the cells after the collector diffusion. As its base width became thinner, its current gains were increased, and the emitter time constant was reduced. The minimum delay was 13.5 ns for one cell and was 10 ns for the cell of thinner base but with no appreciable change in the delay-power product performance at low current range.

Dependence on Cell Area and Metal Interconnection

Most published t_d - I_p characteristics are obtained from simple test circuits--usually a 5 to 10 stage ring oscillator or ring counter. In these test devices, the circuits are relatively simple. Their fan-outs are usually less than two and metal interconnections are simple. Consequently, the base and collector contacts can usually be designed as close together as possible.

However, in real circuits, even for memory applications, the fan-out is usually higher than two and the metal cross-overs are often needed. Consequently, cell area must be increased, not for its own sake but to provide space for metal interconnections. Their performance will not be as good as the performance measured from a ring counter. Fig. 3-24 and 3-25 present two such cases. It is clear that smaller cells have better performance.

Dependence on Temperature

Fig. 3-26 presents the t_d - I_p characteristics at three temperatures: 125, 25 and -55°C. It is seen that the speed is improved in the low power range while the minimum propagation delay is not strongly affected. This suggests that there will be no difficulty for injection logic circuits to meet the military temperature variation specification.

Dependence on Isolation Collar

The effect of an isolation collar on the circuit performance is shown in Fig. 3-27 which presents the propagation delay as a function of power consumption for three different isolation schemes:

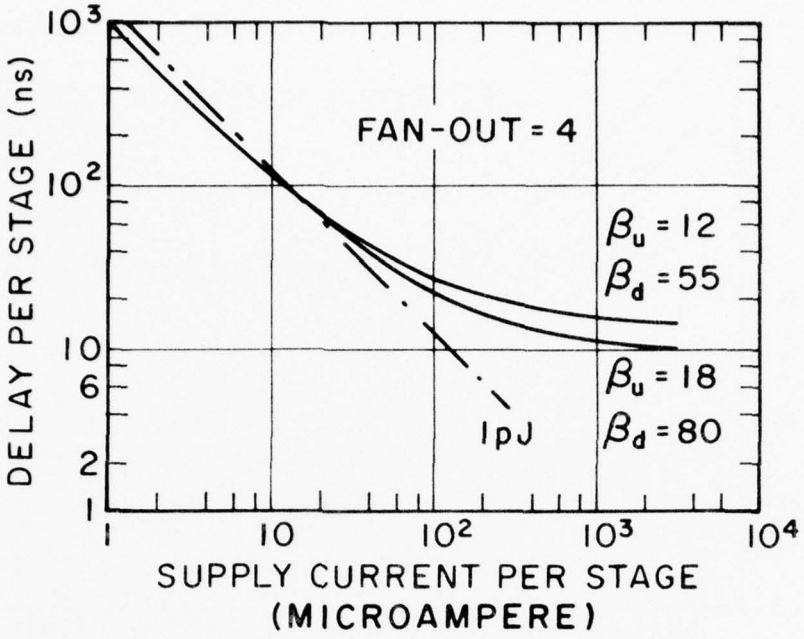


Fig. 3-23 Dependence of t_d-I_p Characteristics on npn Transistor Base Width. One Transistor (β_u=18) was fabricated with an Additional Drive In. (B74-3).

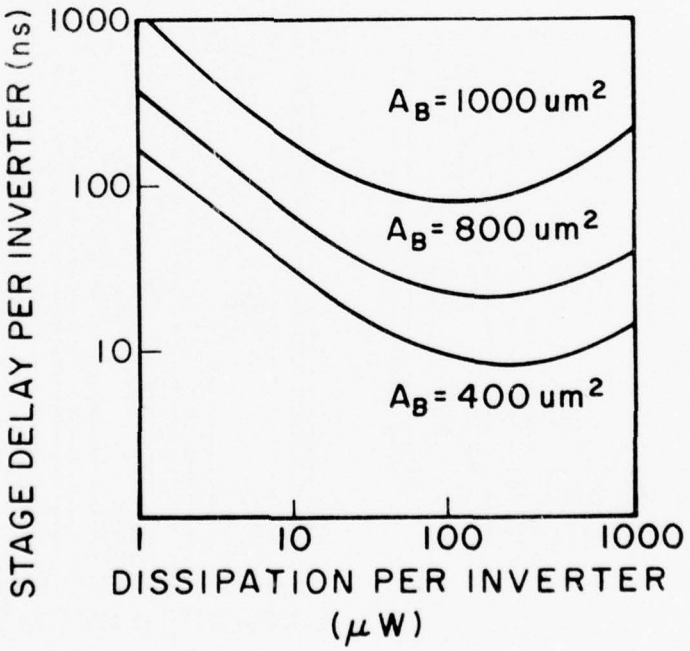


Fig. 3-24 Dependence of t_d-Power Characteristics on npn Transistor Base Area. (A75-4).

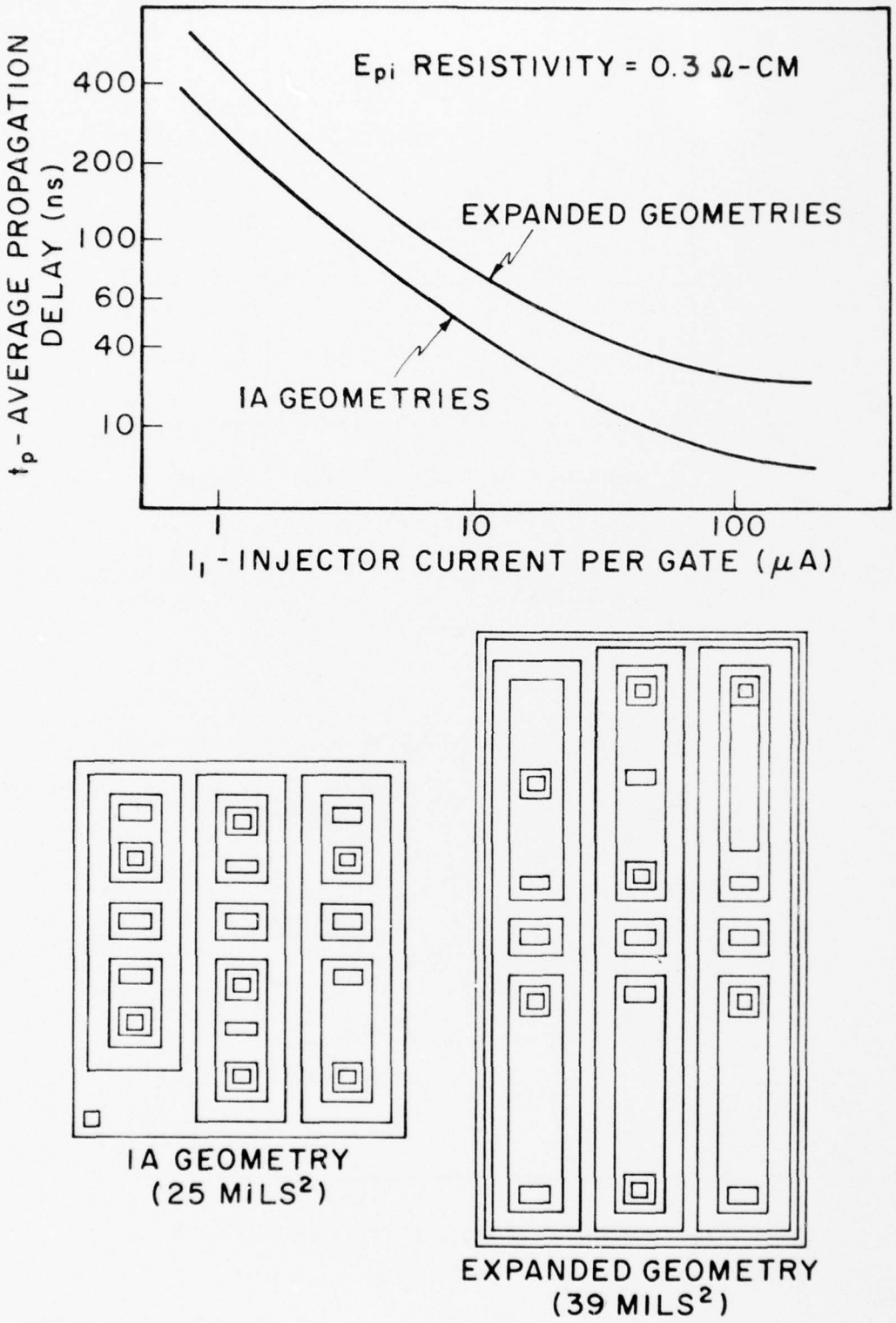


Fig. 3-25 Dependence of t_d-I_p Characteristics on I^2L/MTL Cell Area (Texas Instruments Data).

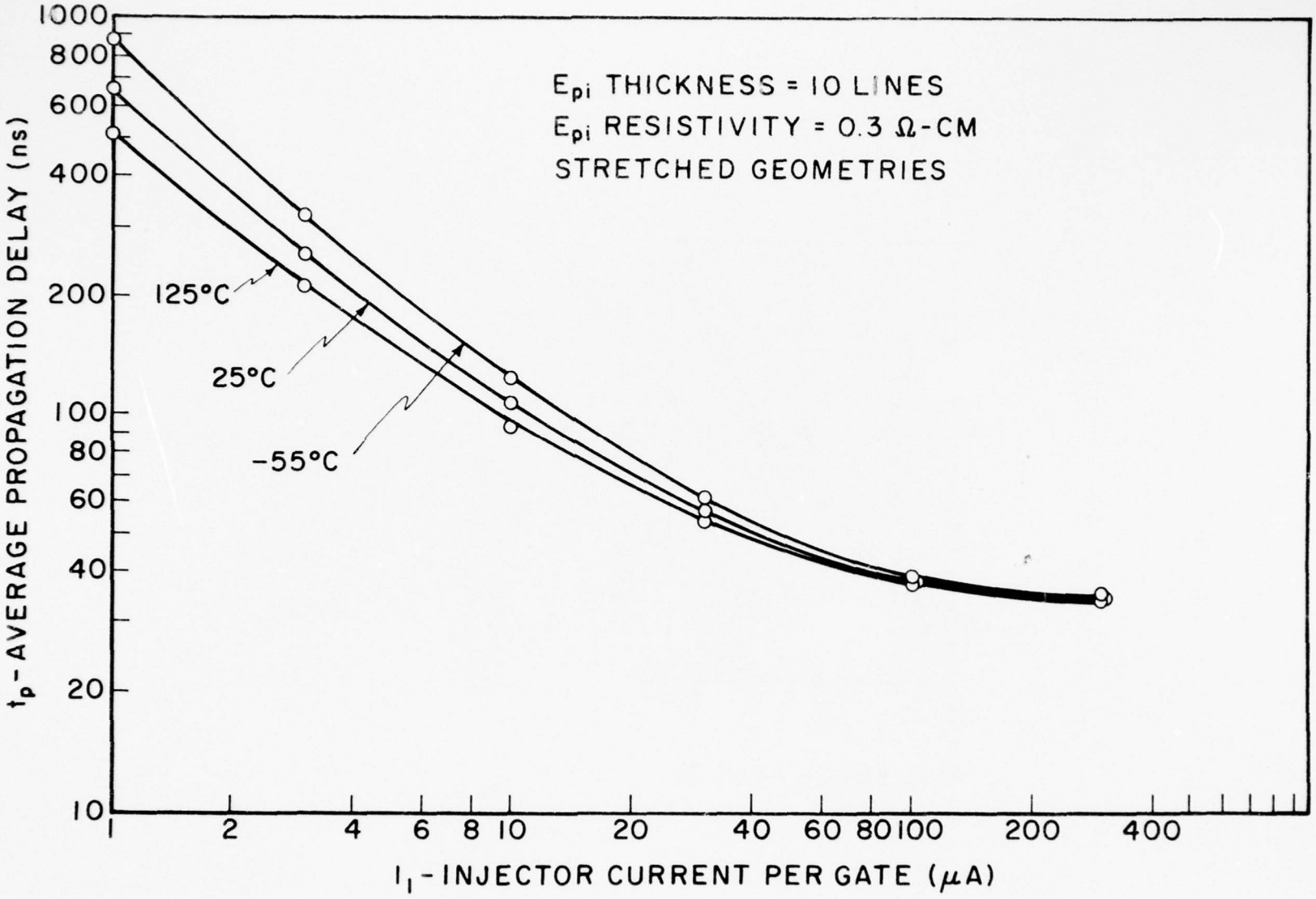


Fig. 3-26 Dependence of t_d-I_p Characteristics On Temperature (Texas Instrument Data).

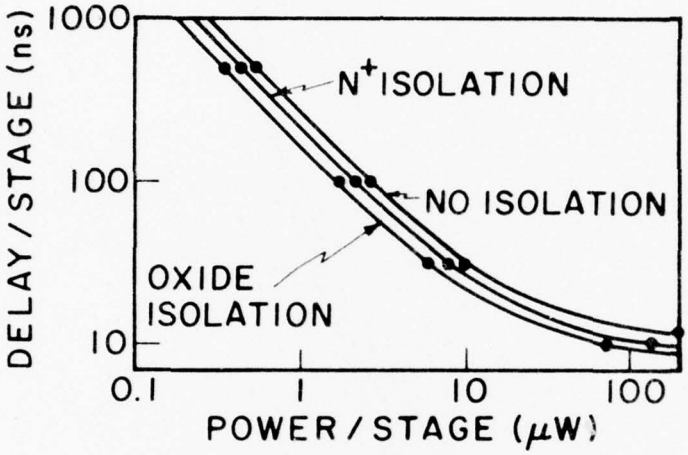


Fig. 3-27 Dependence of t_d-P Characteristics of I^2L/MTL Cell on Isolation Collar. (A74-1).

no collar

n^+ collar

oxide collar

The improvements in delay-power product are obvious. The minimum delay is 11 ns in the case of an n^+ collar and 9.5 ns in the case of an oxide collar. It is not known whether these collars are shallow or deep.

Dependence on Injection Schemes

It has been repeatedly pointed out that injection current is most crucial in determining the circuit performance. Several different injection schemes have been investigated in attempts to achieve the most efficient use of the externally injected current.

Table III-5 shows the effect of lateral injection schemes.

TABLE III-5 EFFECTS OF INJECTION SCHEMES ON DELAY-POWER PRODUCT

Circuit	Delay-Power Product (pJ)
10μ geometry	1
5μ geometry	0.25
3 sides injection	0.13

The first case is the standard circuit with 10 micron geometry. The second case is also a standard circuit but with smaller 5 micron geometry. Improvement of a factor of four in reducing the delay-power product is reported. The main cause of this improvement is probably the decrease of capacitance. The third case uses a different lateral current injection scheme. Instead of injection from one side, the current rail surrounds the p-diffusion on three sides. Therefore, current is more efficiently injected and results in further decrease of the delay-power product. 0.13 pJ is the lowest value ever reported for the standard I^2L circuit without using other innovative variations such as the oxide collar, Schottky diodes, injection from under, etc. However,

it is not practical to use this three-sided injection too frequently in complex logic.

Because lateral injection has two inherent limitations--wide base width and vertical injection component, vertical injection schemes were proposed, first in SFL, recently in VIL. The base width can be made much thinner. More efficient carrier injection from emitter to collector is also expected. Fig. 3-28 shows the t_d-P performance of SFL. Its 0.05 pJ performance at low current range is the lowest delay-power product reported of all injection circuits. However, the minimum delay is still above 10 ns. It must be pointed out that Schottky diodes are used at the inputs of the SFL cell. Therefore, the logic swing was reduced to around 0.35 volts, which also contributed to the performance improvement.

The improvement of performance using the VIL scheme is shown by the t_d-P plot in Fig. 3-29 which also includes the performance of an I^2L cell fabricated during the same process. The delay-power product was improved from 0.3 pJ to 0.07 pJ. However, the speed performance should be considered mediocre, 8.8 ns versus 37 ns, since the test device is a simple inverter.

Dependence on Logic Swing

Schottky diodes are used to reduce the logic swing. In Fig. 28, which shows the t_d-P performance for SFL, some improvement was already demonstrated. There are several other versions of injection logic circuit using the Schottky diodes to reduce logic swing. Fig. 3-30 shows the t_d-P performance for the Schottky I^2L logic circuit, reported by Bell Telephone Laboratories. It can be seen that SI^2L improves the performance by approximately a factor of 2. However, its delay-power product is only 1 pJ. The data also did not extend beyond the current level of 100 μa. Therefore, the minimum delay data is not included in this figure. On the other hand, a research group at the University of Utah reported the t_d-P performance of their SI^2L circuit shown in Fig. 3-3. The delay-power product is excellent at 0.15 pJ. But the minimum delay is in the neighborhood of 20 ns only.

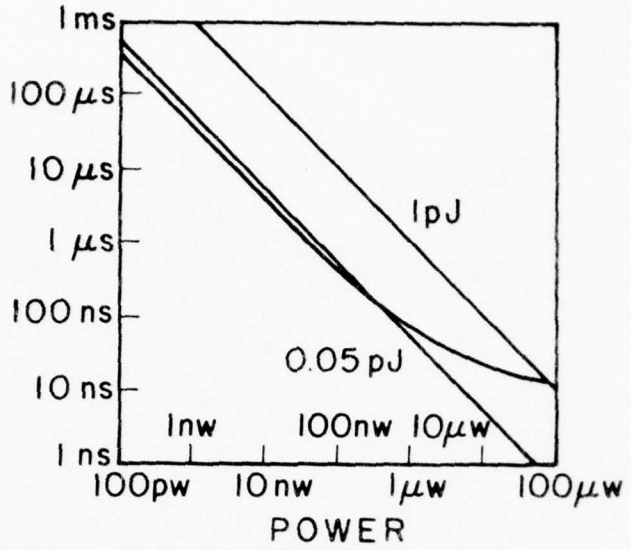


Fig. 3-28 t_d-P Characteristics of a SFL (Substrate-Fed Logic) Cell (B75-5).

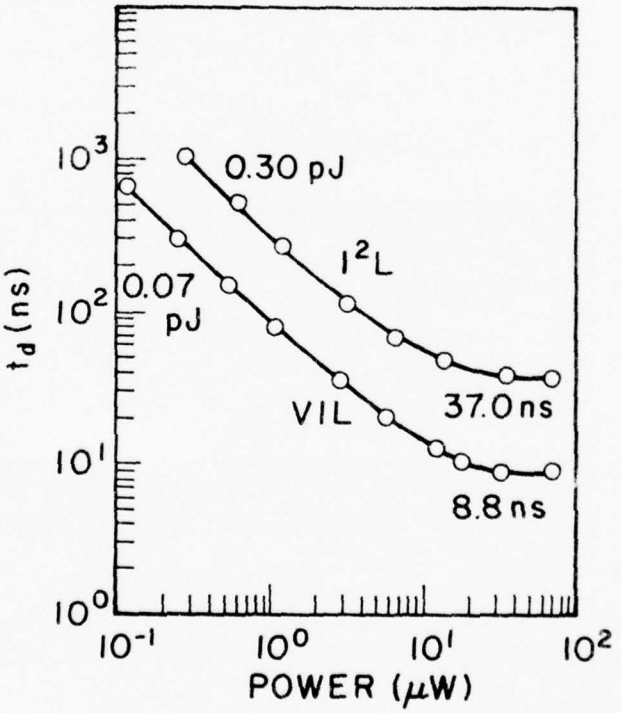


Fig. 3-29 t_d-P Characteristics of a VIL (Vertical Injection Logic) Cell (N75-1).

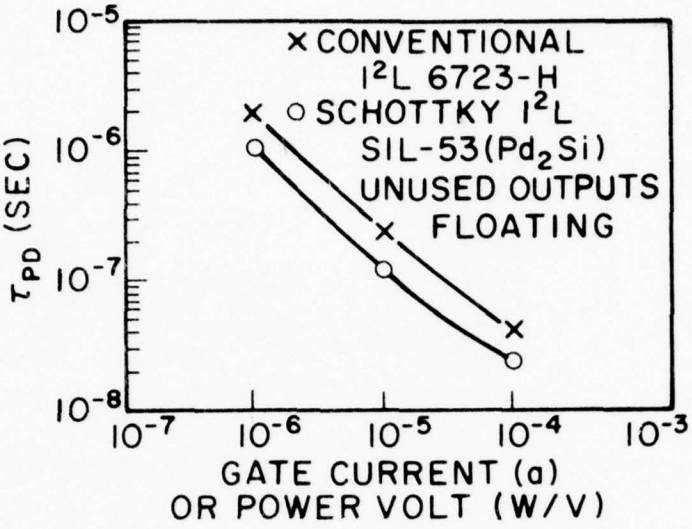


Fig. 3-30 t_d-I Characteristics of a SI^2L (Schottky Integrated Injection Logic) Cell by Bell Telephone Laboratory (H75-3).

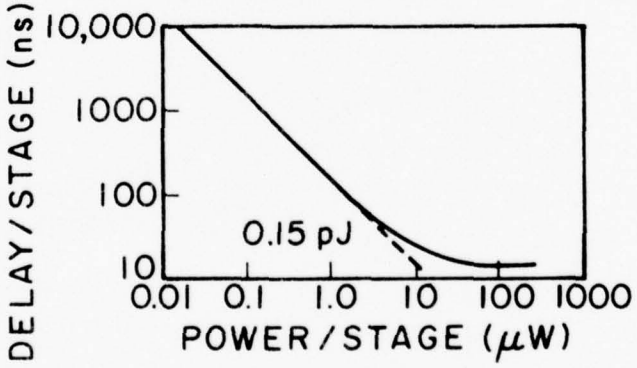


Fig. 3-31 t_d-P Characteristics of a SI^2L (Schottky Integrated Injection Logic) Cell by University of Utah. (H75-2).

3.3 MERGED TRANSISTORS

3.3.1 Introduction

From the I^2L/MTL basic cell discussion, the requirements for the pnp and npn transistors have become clear.

For pnp: high forward common base current gain α_f

For npn: high upward common emitter current gain β_u
high downward common emitter current gain β_d
high transition frequency f_T
small total capacitance.

However, it must be recognized that in the new LSI technology, devices are not always separated. Consequently, when the conventional transistor characteristics are applied to these new transistors, more specifications must be added.

For a pnp transistor, lateral current flow from the npn base and downward injection to the substrate must be considered. For a proper description of α_f, it must be specified whether a neighboring npn transistor exists or not. If it exists, its operating mode must be specified.

For npn transistors, lateral current flow to pnp and vertical current flow outside the collectors and base contact must be considered. For a proper description of β_u and β_d, the following parameters must be given:

- Fan out = number of collectors
- Collar--shallow, deep or dielectric
- Whether a neighboring pnp exists or not. If it does, whether it is open or short circuited.
- Current gains of different collectors in the same npn transistor are different depending on its location with respect to the lateral pnp transistor.
- Current gain of one collector also depends on how the other collectors are operated.

Unfortunately, some transistor characteristics reported to date have not adequately provided this information.

Although the names "transistor" and "diode" are used in injection logic, they are more complicated than the conventional devices. New understanding and descriptions are necessary. For theoretical analysis, computer simulation or CAD (computer aided design) may prove to be indispensible. For bipolar transistors in conventional integrated circuits, the large signal Ebers-Moll model and the charge control model of Gummel and Poon have been developed with considerable sophistication. Extension of these analyses to the new bipolar LSI circuits was started not too long ago. It will be some time before a unified analysis will come forth and be widely accepted. However, some preliminary progress has already been reported and will be highlighted in the following:

3.3.2 -- pnp transistors

3.3.3 -- npn transistors

3.3.4 -- experimental results, optimization and trade-off considerations.

3.3.2 pnp Transistors

Just a few years ago, the current gain of a lateral pnp transistor was so low that it was not practically useful. Now, it is one of the two basic devices which make the injection circuit possible. But its current gain is still low, due to the following reasons.

(a) Because of the limitation of line resolution in the diffusion mask and the effect of lateral diffusion, it has been difficult to fabricate a base width less than 2 microns. In comparison, the base width of an ordinary npn transistor can be less than 0.5 micron.

(b) The emitter current is laterally injected toward the collector. There is always a vertical component directed to the substrate which does not contribute to transistor action.

(c) Furthermore, it was found that the current gain generally decreases with increasing current. For some pnp transistors, α started

to fail off at current levels as low as 40-50 μa.

It is fortunate that the new injection circuit is able to operate with low α and at low current levels. However, improvements are needed to further reduce the power consumption, increase the speed and/or reduce the delay-power product.

Theory

The lateral pnp transistor has been studied theoretically by several authors:

- H.C. Lin, T.B. Tan, C.Y. Chang, B. Van der leest and N. Formigoni, Proc. IEEE, 52, p. 1491 (1964).
- W.K. Tsang and K.M. Busen, Proc. International Electron Devices Meeting, Washington, D.C., Oct. 1965.
- J. Lindmayer and W. Schneider, Solid State Elect., 10, pp. 225, (1967).
- G. Rey, Solid State Elect., 10, p. 1112 (1967).
- D. Fulkerson, Solid State Elect., 11, p. 821 (1968).
- H.C. Lin, IEEE J. Solid State Circuits, SC-4, p. 20 (1969).
- S. Chou, Solid State Elect., 14, p. 811 (1971).

These authors analyzed a single pnp transistor. Klaassen [K75-1] has calculated the common emitter current gain of a lateral pnp transistor in I^2L cell. Berger and Wiedman considered the effect of the npn transistor on the injector current in the pnp transistor [B75-2].

Lin et al., and Lindmayer and Schneider separated the emitter current into a lateral component which is mostly collected and a vertical component which is injected into the substrate and does not contribute to transistor action. Tsang and Busen showed that the presence of an n^+ layer below the emitter could improve transistor gain and frequency response. Fulkerson, and later Chou, made two dimensional numerical analyses of this device structure. Lindmayer and Schneider, Rey and Chou studied the current dependence of the common emitter current gain and suggested different explanations. Some highlights are presented in the following.

Collector Current I_c - V_{EB} Characteristics

From an ideal model, it was calculated that

$$I_{co} = (\ell_E X_j) q \frac{D_p}{W_{bo}} P_{nE'}$$

where ℓ_E = length of emitter

X_j = diffusion depth of emitter

W_{bo} = lateral base width

D_p = hole diffusion coefficient in the base

$P_{nE'}$ = excess hole concentration at the base edge of the emitter space charge layer

$$= \frac{n_i^2}{N_D}[\exp (qV_{EB}/kT) - 1]$$

However, actual collector current I_{cp} differs from this ideal expression in three ways:

- The lateral base width is not uniform.
- There is an epi-layer under the pnp transistor.
- At large V_{EB}, high current injection effects occur.

The collector current can be expressed as:

$$I_{cp} = I_{co} F_{Gc} F_c$$

where I_{co} is the ideal collector current based on one dimensional flow across a uniform base width.

F_{Gc} is a geometric factor accounting for the two dimensional effects.

F_c is another factor which corrects for the high level injection effect, which is only appreciable in the base.

Both factors have been calculated and plotted in Chou's paper.

A typical I_c - V_{EB} characteristic for a test pnp transistor on a I^2L chip is shown in Fig. 3-32. It has an exponential dependence up to around 800 mv and 100 μa but starts to deviate from it after that point. The base donor concentration was approximately 5×10^{16} cm^{-3}. This is considered as evidence of high injection effects which will limit the high speed performance of I^2L.

pnp Injection Current in an I^2L/MTL Cell

The collector current of the pnp is the net injector current, I_o, driving the npn switch transistor. Its emitter current is the injector current, I_i. In an I^2L/MTL cell, their relation depends on the condition of the npn transistor [B75-2].

- When the npn transistor is "off" or when the pnp collector is grounded

$$I_o = \alpha_f I_i \quad \text{or} \quad I_{cp} = \alpha_f I_{EP}.$$

- When the npn transistor is "on" or when the pnp collector is floated;

$$I_o = \alpha_f I_i/(1 - \frac{\alpha_f \alpha_r}{1 - \alpha_u \alpha_d}) \quad \text{when npn is saturated}$$

$$= \alpha_f I_i/(1 - \frac{\alpha_f \alpha_r}{1 - \alpha_u}) \quad \text{when npn is nonsaturated}$$

The term in the parenthesis is called the "recollection factor" which is the consequence of additional lateral current flow due to the presence of the npn transistor.

Base Current I_B - V_{EB} Characteristics

The base current is very important in determining the performance of a lateral pnp transistor. It is the rate at which electrons are supplied through the base contact to make up for the recombination in the base emitter regions. Five components have been identified in Chou's study:

I_{B1} = Bulk recombination in neutral base

I_{B2} = Recombination in neutral emitter

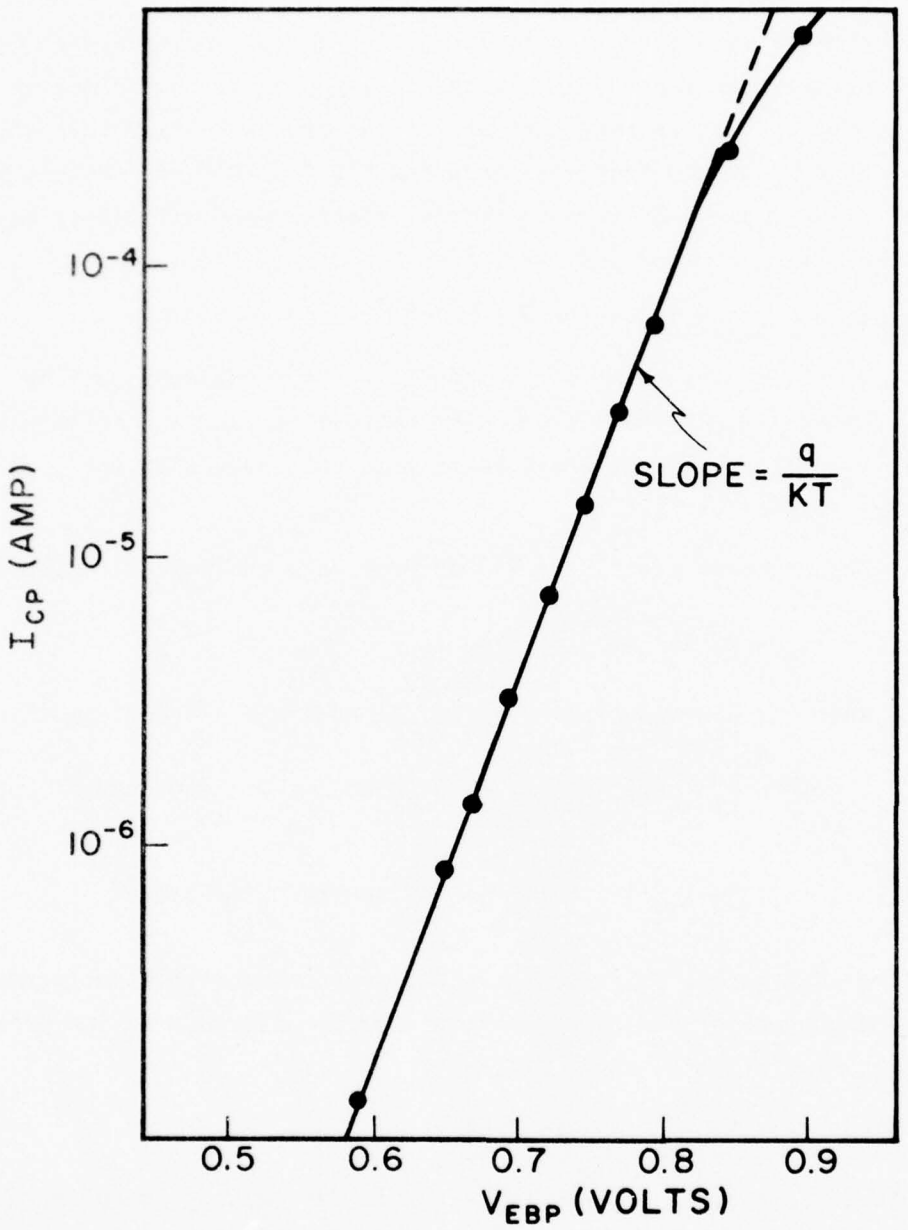


Fig. 3-32 I_{cp} vs V_{EBP} Characteristics of a Lateral pnp Transistor (Northrup Data).

I_{B3} = Recombination at n - n^+ interface between epi-layer and substrate

I_{B4} = Recombination in emitter-base junction depletion layer

I_{B5} = Recombination through surface states at oxide silicon interface.

He found that

I_{B5} is not significant.

At low forward biases, $V_{EB} < 0.3$ v, I_{B4} dominates.

At high biases, when high injection effects become strong, I_{B2} and I_{B3} dominate. It seems to occur in the current ranges around 100 microamps or higher depending on the base doping concentration. At current levels approaching and exceeding 1 ma, the debiasing of the emitter base junction due to series resistance must be taken into account. The high injection effect in the base current characteristics appears also as a deviation from the exponential dependence. It seems to occur at slightly higher V_{EB} bias than that for the I_c - V_{EB} characteristics.

Current Gains α and β

Common emitter current gain β_f or h_{fe} was analyzed in most studies although the characteristics of common base current gain α_f are more useful for a pnp transistor in injection logic circuits. They are, of course, related:

$$\beta_f = h_{fe} = \frac{I_c}{I_B} = \frac{I_c}{I_{BL} + I_{BV}}$$

$$\alpha_f = \frac{I_c}{I_E} = \frac{I_{EL} + I_{BL}}{I_{EL} + I_{EV}}$$

Where the subscript L is for lateral, V is for vertical. If $I_c = I_{EL} + I_{BL}$, $I_{BV} = I_{EV}$, then the conventional relations hold.

$$\alpha_f = \frac{\beta_f}{\beta_f + 1} \quad , \quad \beta_f = \frac{\alpha_f}{1 - \alpha_f}$$

Chou found that h_{fe} peaked around 600 mv or 200-400 μa. The donor concentration of the base was approximately 1.5×10^{15} cm^{-3}. Above this bias, high level injection effects in the base became appreciable. I_c does not increase as fast with respect to V_{EB} as I_B, which results in decreasing h_{fe}. At lower V_{EB} range, h_{fe} also decreases because of depletion layer recombination.

Using basically the charge control approach, the common emitter current gain of the pnp transistor was derived by Klaassen.

$$\beta_p \simeq \left(\frac{S_{c_{inj}}}{S_{e_{inj}}}\right) \frac{D_p/N_{epi}\ W_B}{D_n/(\int N_B dx) + S_p/N_{epi}}$$

For a typical case*: $W_B = 4\mu$, $N_{epi} = 5 \times 10^{15} cm^{-3}$,

S_p = 10-20 m/sec, $D_n = 10\ cm^2/sec$, $S_{c_{inj}}/s_{e_{inj}} \sim X_j/W_{inj} = 0.1$,

the current gain was calculated to be in the range

$$1.5 < \beta_p < 3 \text{ which corresponds to}$$

$$0.6 < \alpha < 0.75.$$

The β_p values were reported to agree with experimental data for current less than 100 amp/cm^2. Since the dimensions of the pnp transistor were not completely specified in his paper, this current density can not be converted into an injector current level. If a typical value of 1.5μ is assumed for X_j, then $W_{inj} = 15\mu$, $A = 22.5\ \mu^2$. A current density of 100 amp/cm^2 corresponds to about 22.5 μamp. Above this level, β_p was reported to start falling off.

Another theoretical calculation of α was achieved by Berger and Wiedman. They expressed α in terms of current components:

$$\alpha_n = \frac{I_{p\ell 1}}{I_{p\ell 1} + I_{pv1} + I_{nc1} + I_{n01}}$$

$$\alpha_i = \frac{I_{p\ell 2}}{I_{p\ell 2} + I_{pv2} + I_{nc2} + I_{n02} + m\ I_{ni}}$$

* N_B and D_p values were not given in the paper.

Explanations of these notations can be found in Table III-2. In this report, we used α_f for α_n and α_r for α_i.

Some experimental results of common base current gain of the pnp transistor in I^2L cell will be given in 3.3.4.

Logic Levels

The voltage levels for the binary logic states are determined by both the pnp and the npn transistors. Klaassen has theoretically calculated the voltage transfer characteristics of an I^2L cell based mainly on the current consideration in the npn transistor. However, an estimate of the voltage level for the logic state "1" can be made using the base-collector bias of the pnp transistor.

$$V(1) = V_{BC} \text{ of pnp} = V_{EB} \text{ of npn}$$
$$= V_{EB} \text{ of pnp} - \frac{kT}{q} \ell n \frac{I_{co}}{\alpha_f I_{eo}}$$

where I_{co} = collector saturation current

I_{eo} = emitter saturation current

Breakdown Voltages

For the following typical pnp transistor

Emitter area: $0.5 \times 0.7 \text{ mil}^2$

Collector area: $0.5 \times 0.5 \text{ mil}^2$

Base width: 0.2 mil

Emitter and
Collector depth: 1.2 μ

the breakdown voltages are

$BV_{CEO} = 17.5$ v

$BF_{CBO} = 18.5$ v.

3.3.3 npn Transistors

When the logic state of a basic I^2L/MTL cell is switched, the pnp transistor changes its operation slightly from saturation to partial

saturation, the npn transistor undergoes drastic switching from "saturation" to "cut-off" or vice versa. Therefore, both d.c. and a.c. characteristics are important.

It was pointed out before that the npn transistor in injection circuits is different from other conventional npn transistors because:

- A lateral pnp transistor is merged with it.
- It has several collectors.
- Its collectors are more heavily doped than in conventional transistors.
- It is operated in the inverted mode.
- Its emitter is less heavily doped than in conventional transistors.

With these complications, two dimensional computer analysis is necessary. although several programs have been referred to in the literature, such as PHILPAC, SINAP, etc., specially developed for bipolar injection circuits, none has been published. Some aspects of the npn transistor characteristics have been reported, based on Ebers-Moll or charge control approaches.

Current Characteristics

No theoretical study to the level of thoroughness as has been done for the lateral pnp transistor was found. A typical set of I_{CN} - V_{EBP} characteristics for a test npn transistor in an I^2L cell is shown in Fig. 3-33 which also included the I_{EP} - V_{EBP} characteristics. Since the common emitter current gain of the npn transistor is related to the ratio I_{CN}/I_{EP}, their variations with V_{EBP} will affect the current gain. It can be seen that the deviation from an exponential dependence occurs at different V_{EBP} values for these two currents. Obviously, high injection effects are playing some role in it. But there is no detailed analysis yet.

Charge Storage

Combining their terminal model and injection model studies, Berger and Wiedman have achieved detailed analysis of stored charges and also current components in an MTL cell. The highlights of their results have been presented in 3.2.4.

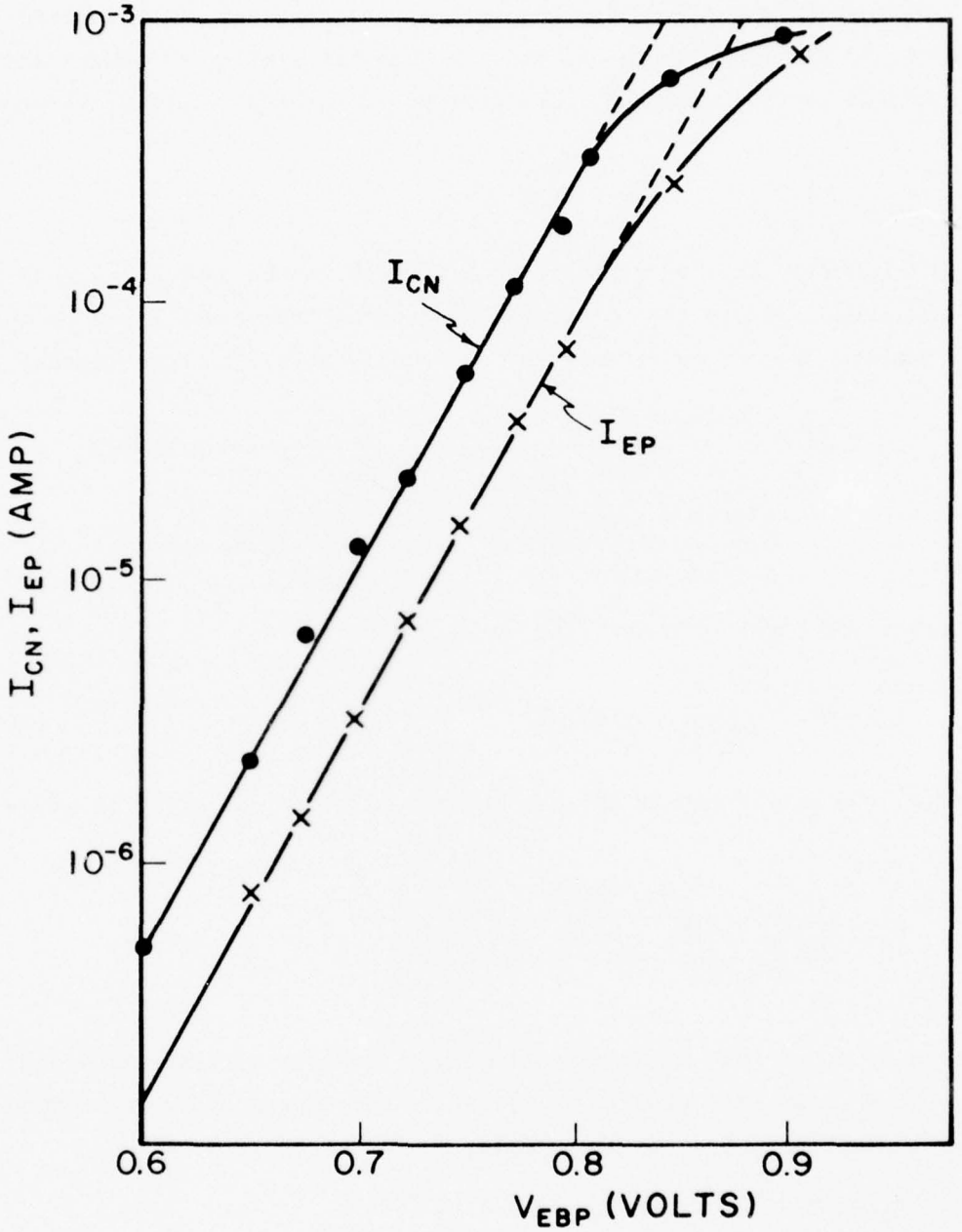


Fig. 3-33 I_{CN} and I_{EP} versus V_{EBP} Characteristics of Inverted npn Transistor with Base Open. (Northrup Data).

Current Gain

One of the most extensive theoretical calculations of β reported to date is by Klaassen, whose analysis is somewhat similar to Gummel and Poon's charge control approach. The concept of intercept current is used.

$$qn_1^2 \frac{DS}{\int N dx}$$

where D = minority carrier diffusion coefficient in the base, S = cross sectional area, $\int N dx$ is the integrated base dopant sometimes known as the Gummel number. For an npn transistor of F collectors, the base current is

$$i_B \simeq qn_i^2 \{\frac{D_n[S_B + F(S_B - S_c)]}{N_B dx} + \frac{(F+1)S_B S_p}{N_{epi}}\} \exp(qV/kT)$$

electron recombination in the p base outside collectors

hole recombination in the n epi-layer under collectors

The current for each collector is

$$i_c - qn_1^2 \frac{D_n S_c}{\int N_B' dx} \exp(qV/kT).$$

Therefore, the upward common emitter current gain per collector is given by

$$\beta_n = \frac{S_c(D_n/\int N_B' dx)}{\frac{D_n[S_B + F(S_B - S_c)]}{(\int N_B dx)} + \frac{(F+1)S_p}{N_{epi}}}$$

It should be noted that Klaassen called this "inverse current gain" and labeled it β_n. In this report, it is called the upward (forward) common emitter current gain β_u. As an example,

$S_c/S_B = 0.7$, $F = 1$, $N_{epi} = 5 \times 10^{15} cm^{-3}$,

$\int N_B dx = 3 \times 10^{14} cm^{-2}$, $\int N_B' dx = 3 \times 10^{12} cm^{-2}$

$D_n \simeq 10\ cm^2\ S^{-1}$, $S_p = 10\text{-}20\ m_S^{-1}$

$10 < \beta_u < 20$

It was reported to agree with experimental values. More extensive agreements for different fan-outs have also been reported and were shown in Fig. 3-1.

Another comprehensive calculation of current gain is reported by Berger and Wiedman. Using the current components found in the terminal and injection models,

$$\alpha_u = \frac{m\, I_{ni}}{I_{p\,2} + I_{pv2} + I_{nc2} + I_{no2} + mI_{ni}}$$

$$\beta_u = \frac{\alpha_u}{1 - \alpha_u}$$

Dynamic Property--Transition Frequency

The transition frequency f_T, or cut-off frequency, can be calculated from the charge control principle from a perturbation of the stored hole concentration and the resulting change in collector current

$$f_T = \frac{1}{2\pi} \frac{\Delta I_c}{\Delta Q_p} = \frac{1}{2\pi} \frac{i_c}{Q_{epi}}$$

Klaassen showed that

$$\Delta Q_p = Q_{epi} \simeq \frac{q n_i^2}{N_{epi}} (F + 1) S_B W_{epi} \exp(qV/kT)$$

Using the i_c expression derived earlier:

$$f_T \simeq \frac{1}{2\pi} \left(\frac{S_c}{S_B}\right) \left[\frac{D_n / \int N_B' dx}{(F + 1) W_{epi}/N_{eip}}\right]$$

Ex. Using $S_c/S_B = 0.7$, $D_n = 10\ cm^2 sec^{-1}$, $N_B' dx = 3 \times 10^{12} cm^{-2}$

$N_{epi} = 5 \times 10^{15}\ cm^{-3}$, $F = 1$, $W_{epi} = 1\mu$

$f_T \simeq 25$ MHZ.

It was reported that values between 20 and 50 MHZ have been measured experimentally at a medium current density of 100-1000 amp/cm^2 which was estimated to correspond to 20-200 μamp injector current. More comparisons of calculated and measured values of f_T were given in Fig. 3-1. The agreement is good. Although Klaassen did not report the base widths of these transitors, it is safe to assume that they are in the range from 0.5 to 1 μ. For these base widths, the transition frequency in a conventional transistor should be around several hundreds of MHZ, yet in these npn transistors, f_T is only 20-50 MHZ. This is because they are operated in the inverted mode; the base doping profile is such that the injected holes from the emitter are retarded in the base. Consequently, the switching speed is affected. In fact, if the base doping profile can be reversed either by ion implantation or by out-diffusion of some pre-imbedded acceptors from the epi-layer, the switching speed performance of the npn transistor can be improved. For such cases, the transition frequency expression probably will not apply.

3.3.4 Experimental Results and Design Considerations

(A) pnp Injector:

Dependence on Base Width and Current

Two of the most critical parameters affecting the common base current gain are:

base width

emitter current

Fig. 3-34 shows its dependence on these factors. It can be seen that for a given base width, α falls off at high current range. It falls off at low current range also but the decrease is not nearly as noticeable as its common emitter current gain. On the other hand, the narrower the base width, the higher is the current gain.

Dependence on p Diffusion Resistivity

Dependence of α on emitter and collector resistivity is shown in Fig. 3-35. It can be seen that lower resistivity (higher doping) yields higher current gain. However, the same p-diffusion region is also used

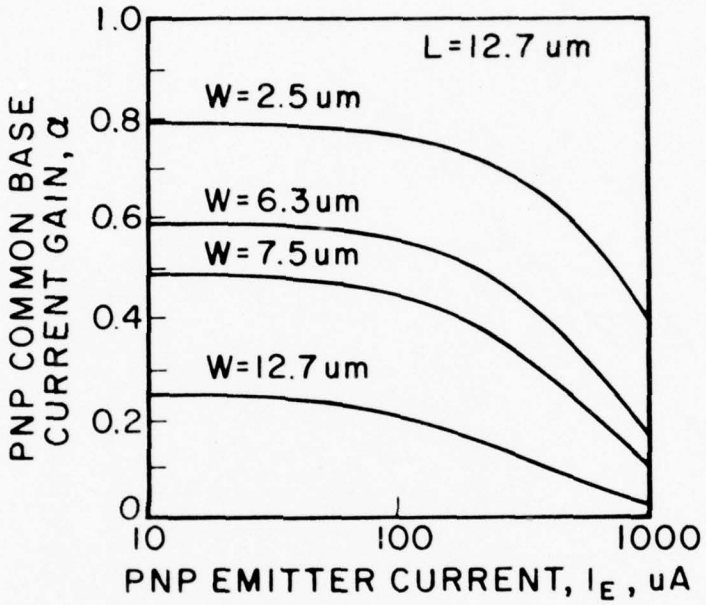


Fig. 3-34 Dependence of Common Base Current Gain of pnp Transistor on Base Width and Emitter Current. (A75-4).

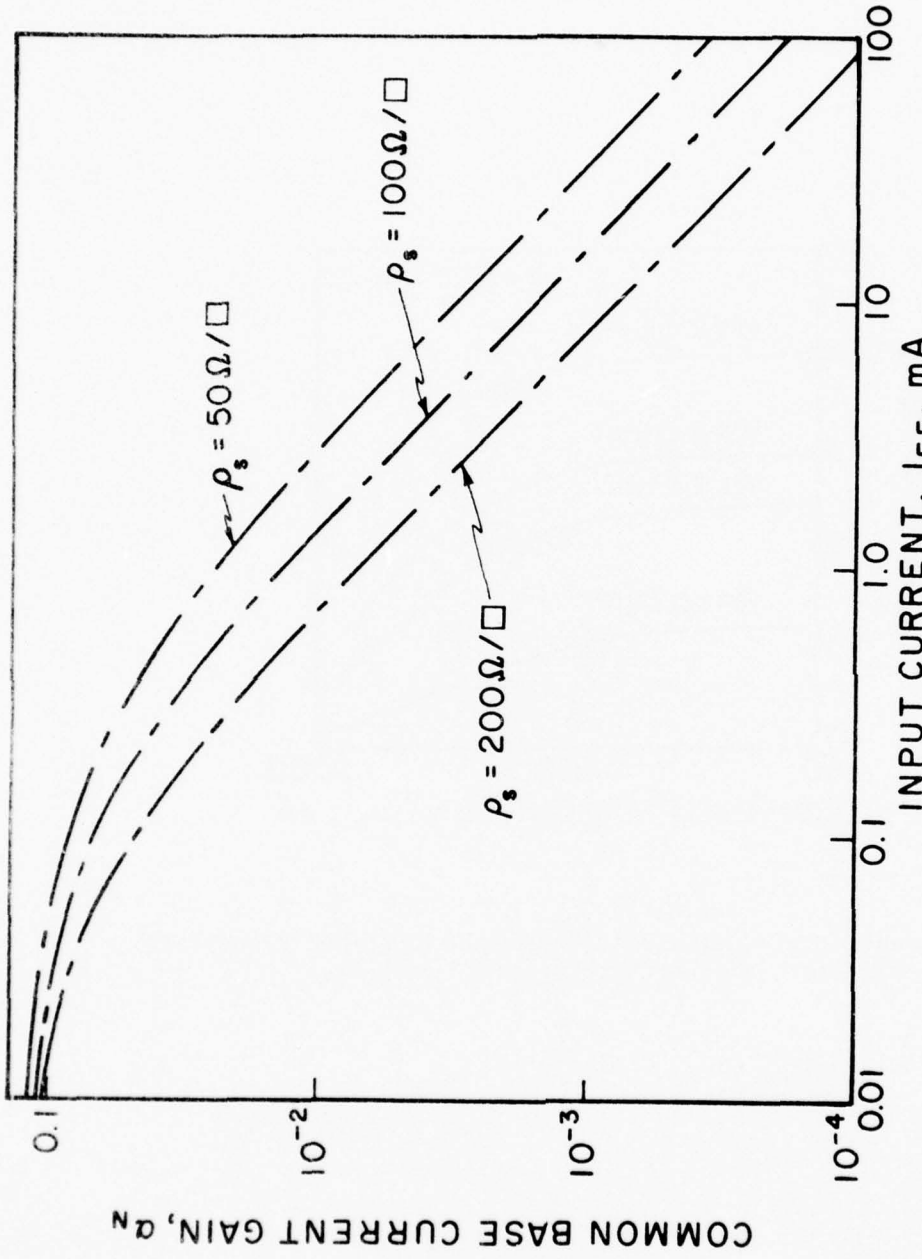


Fig. 3-35 Dependence of Common Base Current Gain of pnp Transistor on Substrate Resistivity and Emitter Current. (Northrup Data).

as the base of the npn transistor which can not tolerate too low a resistivity. A compromise must be made.

Dependence on Epi-Layer Resistivity

Dependence of α on the epi-layer resistivity is shown in Fig. 3-36. Also included in this figure are common emitter current gains of five vertical npn transistors fabricated on the same chip. It can be seen that a compromise in ρ_{epi} is necessary in optimizing the current gains of both the pnp and the npn transistors. It should be remembered that ρ_{epi} affects the minimum propagation delay time also. Its effect must be included in optimization considerations.

Dependence on Isolation Collar

Fig. 3-37 shows the dependence of α on three different isolation layouts:

oxide isolation

n^+ isolation

no isolation

It is not known how deep these two isolations were. Obviously, oxide isolation is the best, followed by n^+ isolation and no isolation.

Dependence on Injection Scheme

In lateral pnp injection scheme, there are always two inherent limiting factors: vertical injection current which does not contribute to the transistor action and the difficulty of making base width narrower than two microns. Vertical injection schemes have been proposed, first in SFL, recently in VIL, which should eliminate both factors. Consequently, α is significantly higher as shown in Fig. 3-38, which also includes the current gain of a lateral pnp transistor fabricated during the same process. The improvement is clearly demonstrated. α for the vertical pnp transistor is around 0.9.

Dependence on Temperature

α - I_c relation is shown in Fig. 3-39 at three temperatures. It is noted that the high injection effect is more or less the same at different

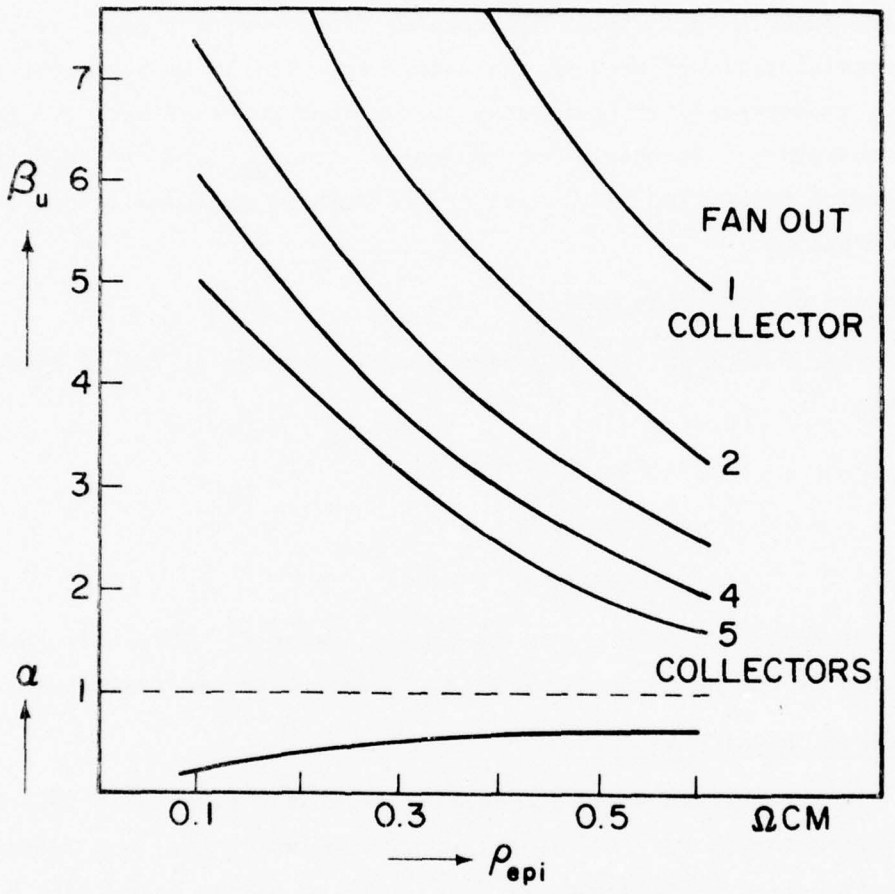


Fig. 3-36 Dependence of Upward Common Emitter Current Gain of npn Transistor and Common Base Current Gain of pnp Transistor on Resistivity of Epi-Layer and Fan Out. (H72-2).

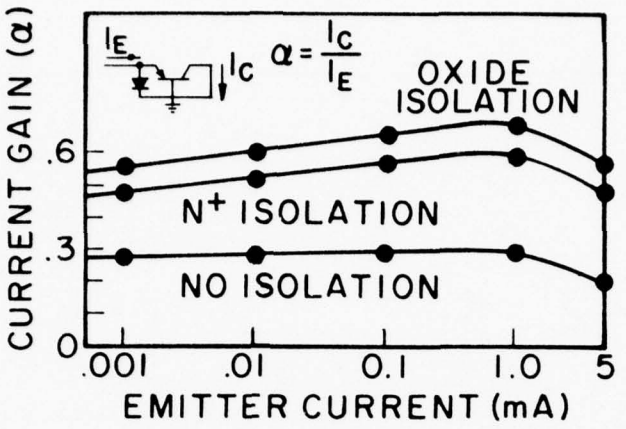


Fig. 3-37 Dependence of Common Base Current Gain of pnp Transistor on Isolation Collar and Emitter Current. (A74-1).

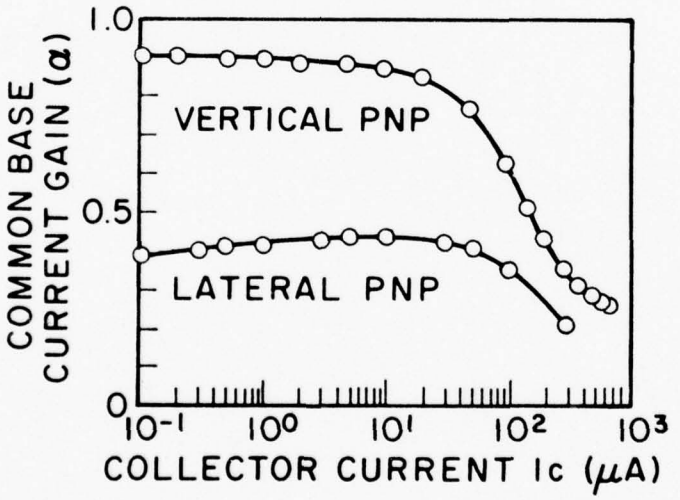


Fig. 3-38 Dependence of Common Base Current Gain of pnp Transistor on Injection Scheme. Vertical pnp versus Lateral pnp. (N75-1).

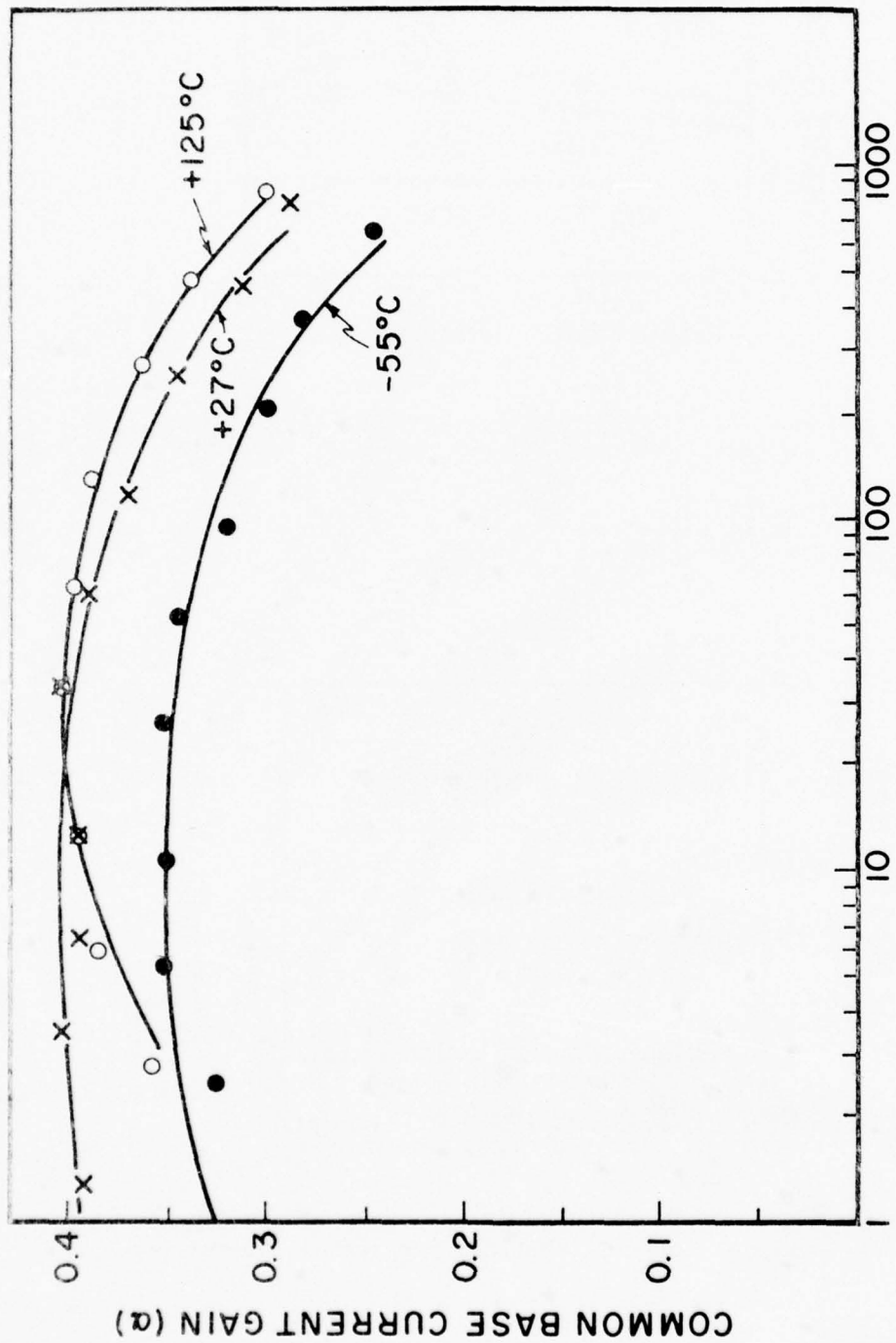


Fig. 3-39 Dependence of Common Base Current Gain of pnp Transistor on Temperature and Collector Current. (Northrup Data).

temperatures. The effect of recombination is increased at higher temperature. Lowering the temperature generally reduces the current gain.

(B) npn Transistors

Transistor Characteristics

The I_C - V_{CE} characteristics of a typical npn transistor are shown in Fig. 3-40. Its dimensions are:

Emitter and base area: $1.41\ mil^2$

Collector area: $0.25\ mil^2$

Base width: $0.44\ \mu$

It should be noted that its saturation voltages are considerably lower than those in typical TTL transistors due to its lower collector resistivity. This is very desirable because V_{CE} (saturation) is the voltage level for the logic "0" state. The voltage level of logic "1" state in injection logic is quite low. It is equal to V_{CE} (on) and varies from 0.5 to 0.8 volts depending on the d.c. power supply voltage. When Schottky diodes are used to limit the logic swing, V(1) is further reduced to 0.3 - 0.35 volts. Therefore, a lower V(0) or lower saturation voltage is desirable for better voltage noise margin.

The breakdown voltages for this npn transistor at 5 μa reverse current are:

$BV_{CEO} = 5\ V$

$BV_{CBO} = 6.1\ V$

$BV_{EBO} = 19.2\ V$

In the following, common emitter current gain data will be given. It should be recognized that because the injection logic is still young, there is no standardization yet. It caused some misleading impressions due to incomplete description of data. This confusion is most serious in performance data and to a slightly lesser degree in the npn characteristics. To begin with, the notation of β must be properly interpreted.

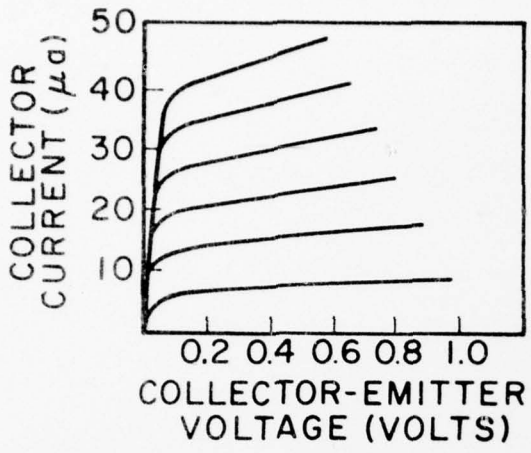


Fig. 3-40 I_C-V_{CE} Characteristics of npn Transistor in I^2L/MTL Cell. (Northrup Data).

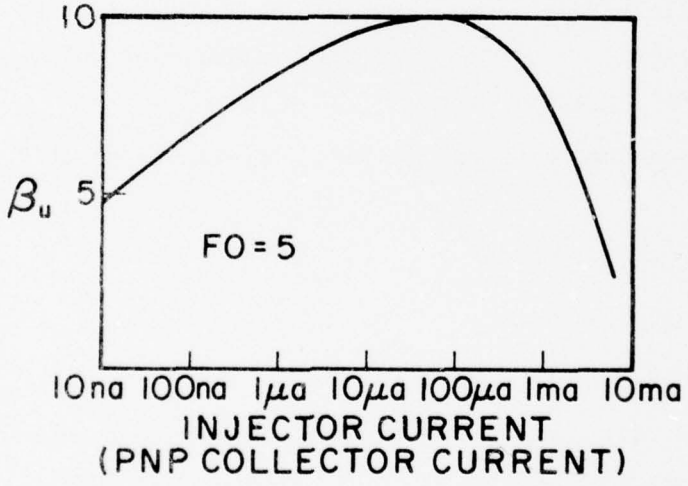


Fig. 3-41 Upward Common Emitter Current Gain of npn Transistor in I^2L/MTL Cell. (B75-4).

Secondly, the physical description of the device and its electrical operation must be completely specified. They are not provided in most cases.

Dependence on Current

It should be distinguished first which current is being referred to. It could be the emitter current, the collector current of the pnp transistor or the base current of the npn transistor. Sometimes the collector current of the npn transistor is used.

A typical β_u - I_p curve for an npn transistor with a fan-out of 5 is shown in Fig. 3-41. It is seen that this npn switch transistor can function ($\beta_U \geq$ FO) over a wide current range from 10 na to 2 ma, over a factor of 200,000! The fall-off of β_U at high current ranges is most likely the result of high injection effects. The fall-off at the low current range is probably due to depletion layer recombination. However, there is no report of detailed theoretical analysis yet.

Dependence on Epi-layer Resistivity

Results of β_u as a function of ρ_{epi} have been included in Fig. 3-36 for several npn tranistors with different fan-outs. β_u decreases with increasing FO because the ratio of collector area to emitter area is also decreased. It was not reported at what current level these data were taken. Presumably, they are the maximum β_u values.

As was mentioned before when the pnp case was presented, compromise is required to choose ρ_{epi}. High pnp α_f prefers higher ρ_{epi}. Furthermore, the device performance favors different ρ_{epi} depending on whether a low delay-power product or a high speed performance is preferred (Fig. 3-22).

Dependence on Collector Location

Current gain is found to depend on the location of the collector relative to the lateral pnp injector as shown in Fig. 3-42 and 3-43 for two cases. One has five collectors. The other has three. It is found that the further a collector is away from the injector, the lower is its β_u. Such a gain variation in the same I^2L cell is undesirable in implementation of complex logic.

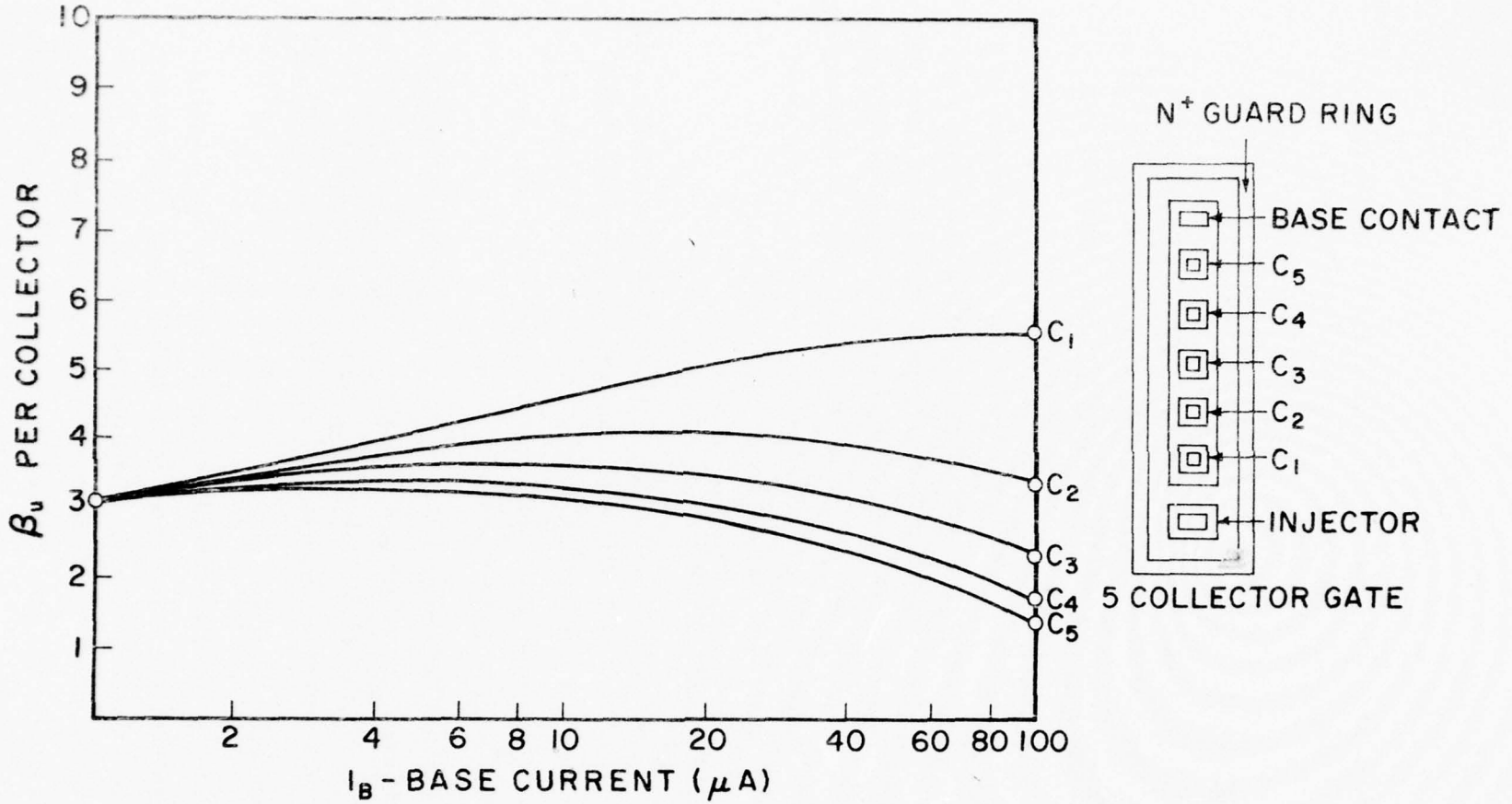


Fig. 3-42 Dependence of Upward Common Emitter Gain of npn Transistor on Collector Location and Base Current. (Texas Instruments Data).

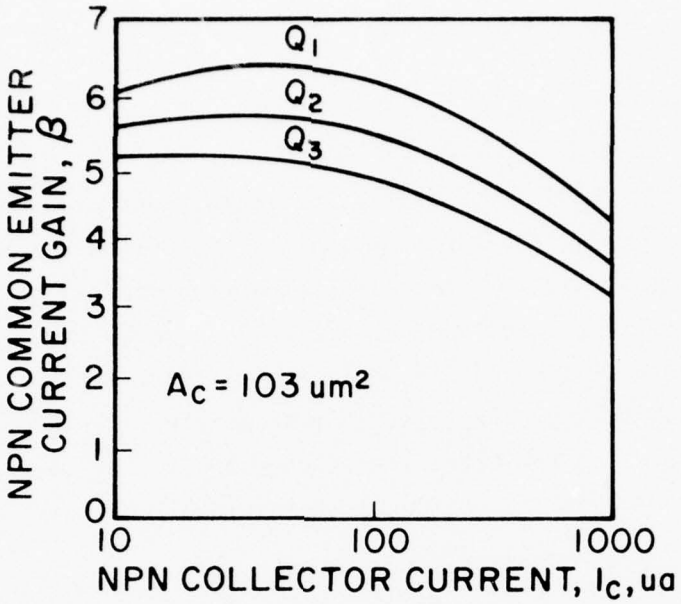


Fig. 3-43 Dependence of Upward Common Emitter Current Gain of npn Transistor on the Collector Location. (A75-4).

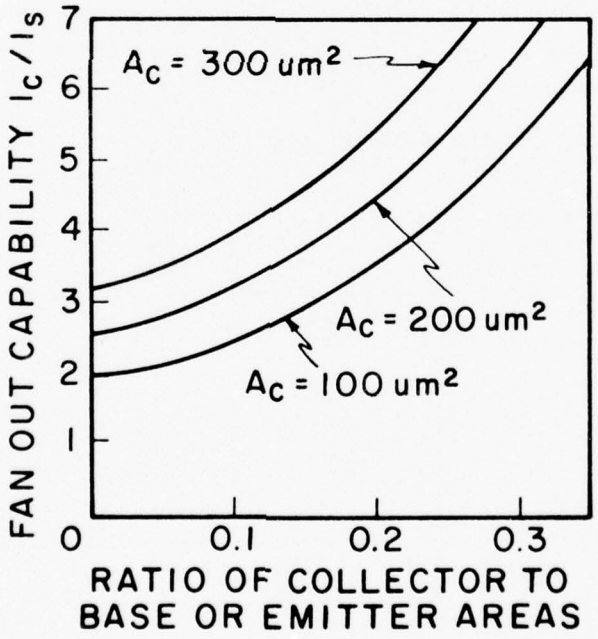


Fig. 3-44 Dependence of Fan Out Capability on the Ratio of Collector to Base Area of the npn Transistor. (A75-4).

Dependence on Collector Area of FAN OUT

In conventional IC transistors, collector area was never a parameter to be varied. However, in injection logic it is one of the most important parameters. More accurately, the ratio of collector area to the emitter area is one of the important factors. Fig. 3-44 shows the dependence of FAN OUT on the area ratio. It is desirable to leave as little space unoccupied by collectors as possible. Unfortunately, in random logic circuits, space must be provided for metal interconnections. For fast circuits when speed is the overriding factor, double metal levels may have to be considered.

Relation Between Upward and Downward Current Gain

Downward current gain β_d should be high in order to minimize the current hogging effect among the collectors. While β_d is generally proportional to β_u, their values do not follow a definite relation. A complete characterization of the npn transistor must provide both current gains. However, many papers report β_u only. The following table is a list of several cases when both β_u and β_d are reported:

TABLE III-6 UPWARD AND DOWNWARD CURRENT GAIN OF npn TRANSISTOR

Transistor	β_u	β_d	FO	Remarks
npn	12	55	4	
in	18	80	4	
I^2L/MTL	10	100		
cell	10	250	5	
	30 - 40	200 - 250	1	Deep n^+ collar
NPN	32.5	135	1	3.5 μ epi layer
transistor	19.6	110	1	3.5 μ epi layer
only	28.6	135	1	5 μ epi layer
	17.6	110	1	5 μ epi layer

Dependence on Epi-layer Thickness

It was found that current gain is higher in thinner epi-layers as demonstrated in the table above. The reason has been pointed out in the injection model study. Its result is shown in Fig. 3-45 for two different epi-layer thicknesses. It is shown that the useful current component j_{ni} is a larger proportion of the emitter current in the thinner layer than in the thicker layer.

Dependence on Isolation Collar

The effect of isolation collar on current gain has been studied in detail using npn transistors of four different dimensions:

TABLE III-7 LIST OF TRANSISTOR GEOMETRIES

epi Thickness (μ)	Collector Area (μ^2)	Base Area (μ^2)	Emitter Area (μ^2)
3.5	360	1080	1990
3.5	90	270	620
5	360	1080	2280
5	90	270	785

For each transistor, three types of isolation collars are provided:

deep n^+ collar

shallow n^+ collar

no collar.

The results can be represented by two figures. In Fig. 3-46, the upward current gains for different collars are shown as a function of the base current I_b. It can be seen that the deep collar yields the best current gain, and also has a smaller dependence on current. In the cases of shallow n^+ collar and no collar, lateral currents exist which deteriorate the current gain. For the case of a deep collar, the transistor size affects the current gain also, as shown in Fig. 3-47. The smaller transistor has lower gain. However, it should not be interpreted that smallness always leads to lower

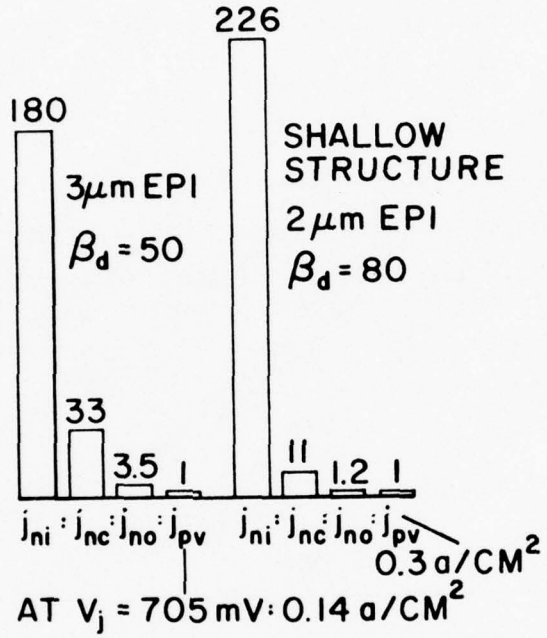


Fig. 3-45 Dependence of Downward Common Emitter Current Gain and Injection Current Densities of npn Transistor on Epi-Layer Thickness. (B74-3).

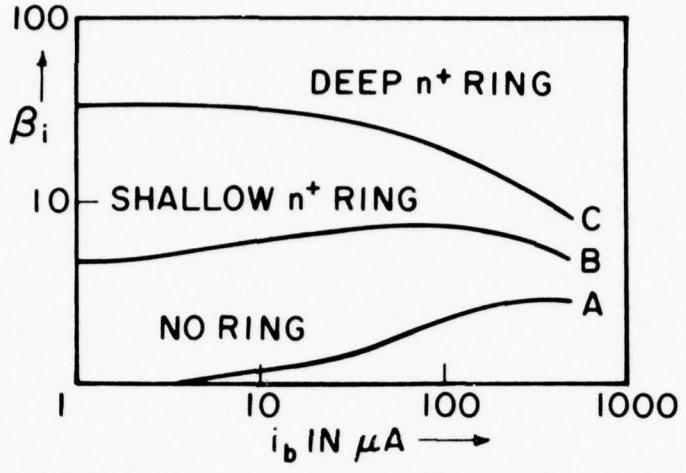


Fig. 3-46 Dependence of Upward Common Emitter Current Gain of npn Transistor on Isolation Collar and Base Current. (S74-1).

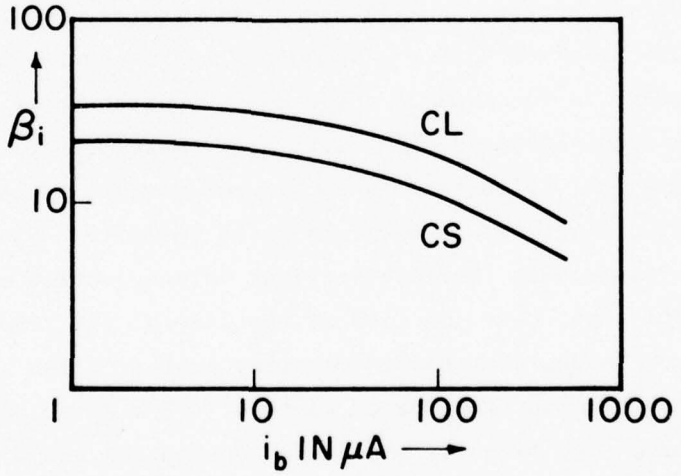


Fig. 3-47 Dependence of Upward Common Emitter Current Gain of npn Transistor on Transistor Size (Deep Isolation Collar). (S74-1).

gain. It must be considered together with the epi-thickness also. It should be noted that these test transistors have only one collector and do not have merged pnp transistors. Therefore, their current gains are higher than those of npn transistors in real I^2L cells.

Dependence on Temperature

β_u - I_c characteristics are shown in Fig. 3-48 for three temperatures--125, 27 and -55°C. The dependence and the comments for npn transistors are similar to pnp transistors.

Gold Doping

I^2L circuit fabrication involves only conventional processing steps and any standard bipolar process can be used to build I^2L circuit elements--with one exception: gold doping, routinely employed in the fabrication of conventional transistors to boost their speed and reduce loading effects, CANNOT be used in the fabrication of I^2L circuits. Although gold doping increases transistor switching speeds, it also simultaneously lowers transistor current gains. Detrimental effects associated with gold doping an I^2L circuit include (1) a decrease in the downward current gain possibly leading to current hogging and (2) a decrease in the upward current gain to the point where observed β_u's < 1 would not be unreasonable. A β_u of at least 1, however, is required in logic operations to short circuit the base current of subsequent stages. In fact, a β_u greater than two times the fan out or number of collectors is considered minimal by some authors. A large β_u is also desirable to maintain noise immunity. Finally, (3) gold doping would drastically increase vertical hole injection across the p emitter-n epi-layer base junction of the lateral pnp transistor (Effectively, the n-epi-layer "appears" wider to minority carrier holes if it is heavily doped with recombination-generation centers.) The α_n of the lateral transistor would be lowered significantly and power consumption would go up. Everything considered, it should be clear that gold doping would be highly detrimental to the operation of I^2L circuits.

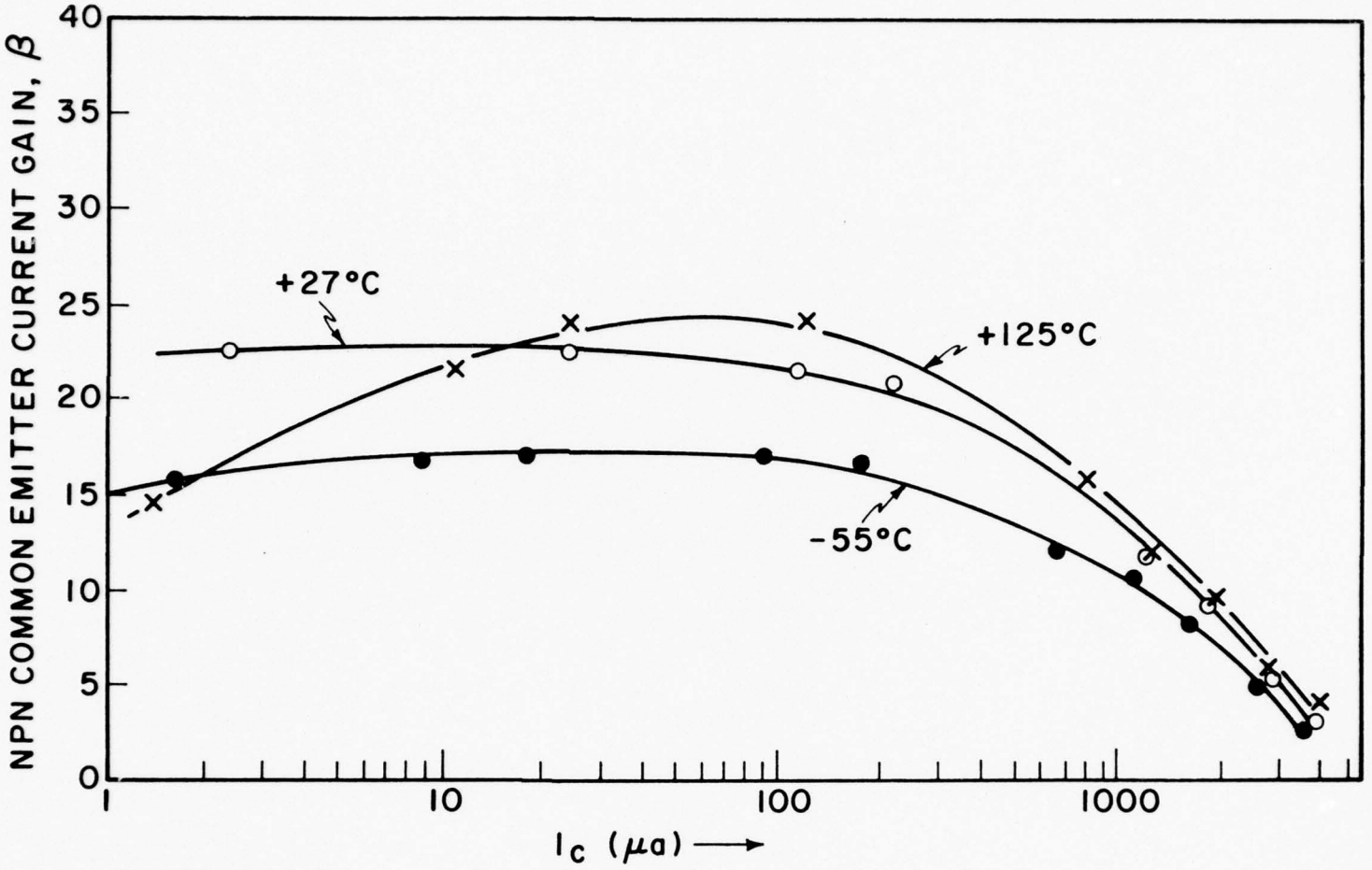


Fig. 3-48 Dependence of Upward Common Emitter Current Gain of npn Transistor on Temperature and Collector Current. (Northrup Data).

CHAPTER IV

BIPOLAR LSI INJECTION LOGIC CIRCUITS

This chapter presents some representative I^2L/MTL circuits in three different categories: digital circuits; memories; and microprocessors.

4.1 INTRODUCTION

Circuit schematics and physical layouts of several simple I^2L/MTL circuits have been presented in previous chapters when the basic concept, processing steps, physical layouts and electrical properties were discussed. In this chapter, more circuit examples will be presented to further demonstrate the LSI capabilities of the I^2L/MTL circuit and to show the wide range of applications served by the new bipolar injection circuits. Examples will be presented in three categories:

Digital circuit building blocks

Large memories

Microprocessors.

4.2 DIGITAL I^2L/MTL CIRCUIT BUILDING BLOCKS

4.2.1 Combinational Circuits

(a) Basic Cell. The basic I^2L/MTL cell is an inverter which has several collectors as its outputs and one input at the base of the npn transistor. Its circuit and layout were shown in Fig. 1-6.

(b) Gates. The basic inverter cell can be easily extended into logic gates by simple connections either at the input or at the output. A NAND gate is obtained by simply tying two input metal lines to the same base terminal. A NOR gate is obtained by simply tying the collector outputs of two inverter cells together. It can be called the "wired NOR" gate.

(c) Decoder. The physical layout of a 3 bit decoder is shown in Fig. 4-1. The simplicity of tying several collector outputs together to implement a logic function is well demonstrated.

(d) Read Only Memory (ROM). The circuit schematic and the physical layout of a four bit read only memory (ROM) is shown in Fig. 4-2. The total area is only 152 x 152 μm^2.

4.2.2 Sequential Circuits

(a) D Type Flip-Flop. The logic diagram of a D type flip-flop was shown in Fig. 2-5(a). It was translated into a circuit schematic in Fig. 2-5(b) when I^2L/MTL gates are used. The corresponding physical layout was shown in Fig. 2-5(c). The total area is only 16.4 mil^2, which is less than the area of one bonding pad.

(b) RS Type Flip-Flop. The circuit schematic and the physical layout of an I^2L/MTL RS flip-flop were also shown in Fig. 2-7. The total area is only 135 x 140 μ^2.

(c) Memories. Two types of memories have been developed. The first type is the conventional latch circuit using two inverters connected together with regenerative feedback which has been used in all other bipolar memories. The second type is a new memory circuit which uses a two-transistor cell operated in a dynamic manner. Both memories are LSI chips and will be described in a later section.

4.2.3 Basic Digital Interface Circuits

I^2L/MTL logic is operated at low power level with

- low current in the range from nanoamps to several hundred microamps
- low voltage in the range from 0.6 to 0.8 volts.

Although the low power operation is an outstanding feature for LSI performance, it lacks the driving capability needed to interact with other electronic circuits. Therefore, I^2L/MTL logic is not used alone and is generally inter-

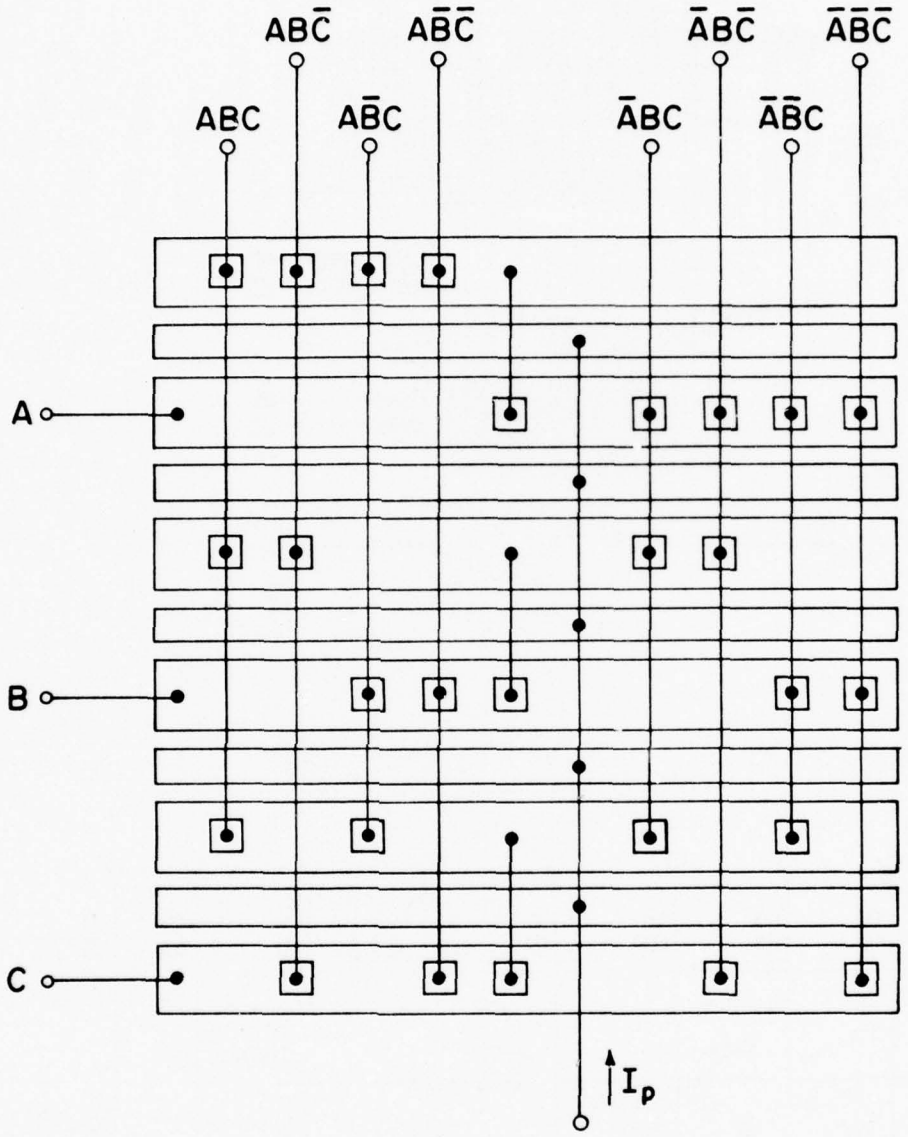


Fig. 4-1 Physical layout of a 3-bit decoder. (B72-1)

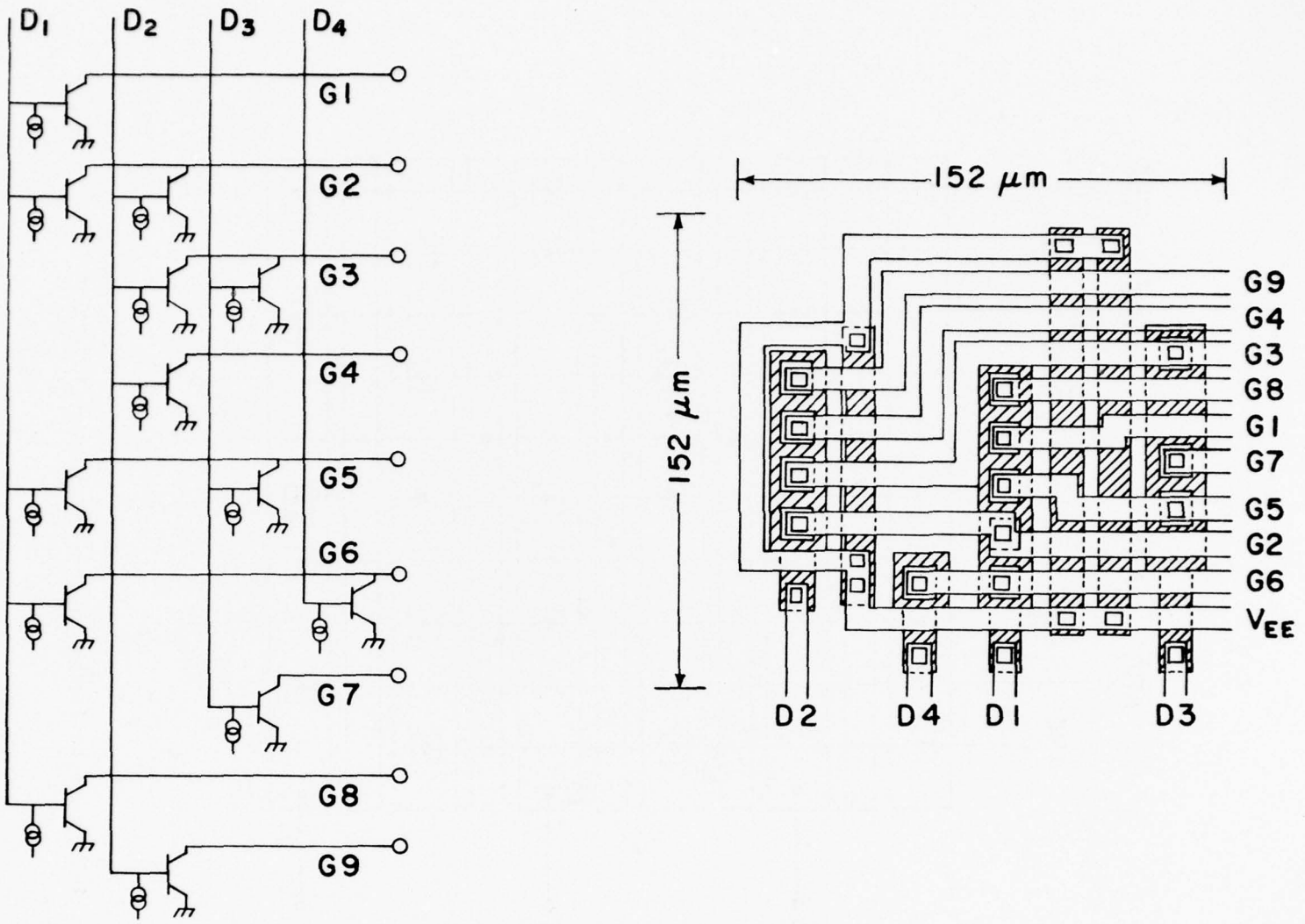


Fig. 4-2 Circuit Schematics and Physical Layout of a 4 Bit Read Only Memory (ROM). (Northrup Research and Technology Center).

faced with TTL, ECL or other linear IC circuits on the same chip.

Five different types of basic interface circuits are shown in Fig. 4-3. It should be noted, however, that practical interface circuits are generally more complicated than these basic circuits. An example will be given in 4.2.4.

(a) Current Amplifier Type (Medium Current). The first type is shown in Fig. 4-3(a). The n+ collector is connected to a positive voltage, V_p, whose value is limited by the collector to emitter breakdown voltage. The logic swing is between 0 and V_p. The maximum output current in the "ON" state is at a medium level from 1 microamp to 1 milliamp. It depends on the current gain of the inverted npn transistor and the injection current.

(b) Emitter Follower Type (High Current). This circuit is shown in Fig. 4-3(b). If the resistor is connected to a negative voltage, then the n+ area acts as an emitter and the transistor is used as an emitter follower. The logic swing is small and is between 0 to -0.7 volts. But the current level is higher, in the range from 10 microamp to 10 milliamp.

(c) This circuit is shown in Fig. 4-3(c). It is similar to the first type except that a pnp transistor is added. The voltage swing is still between 0 and V_p volts. But the current level is lower than that of the first type. Therefore, this circuit is not particularly useful.

(d) Emitter Follower Type with pnp output. This circuit is shown in Fig. 4-3(d). It is similar to the second type except that a pnp transistor is added and is connected to a negative supply voltage. Although its current level is slightly lower than the second type due to the common base current gain of the pnp transistor, the voltage swing is increased because the base of the npn transistor is now driven by a current instead of a voltage.

(e) High Voltage Swing Type. This circuit is shown in Fig. 4-3(e). It has the largest voltage swing because it is limited by the collector-emitter breakdown voltage of the lateral pnp transistor which can be as

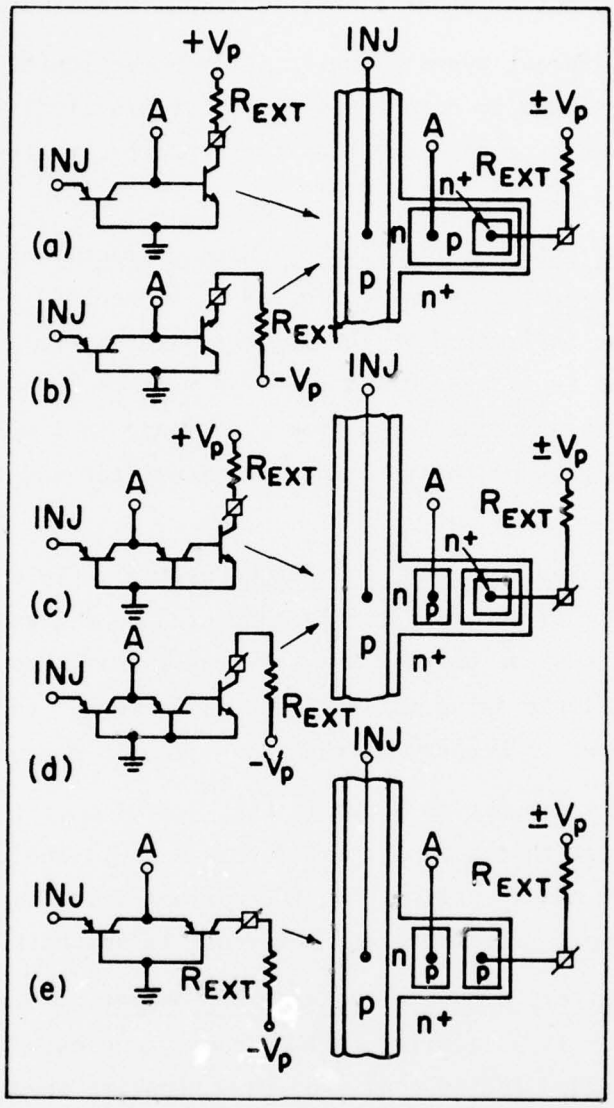


Fig. 4-3 Circuit Schematics and Physical Layout of Five Basic Interface Circuits Between IIL/MTL And Other Digital or Linear Bipolar Circuits. (H74-1).

high as 40 volts. But the maximum current in the "ON" state is rather low, in the range from 0.1 microamp to 0.1 milliamp.

4.2.4 Interface Circuit Example - Between TTL and I^2L

The basic concepts of interface circuits were presented in 4.2.3. Real interface circuits are usually more complex. An example is given in Figs. 4-4 and 4-5 for interface between TTL and I^2L. The circuits will be explained based on the differences between the operational characteristics of a TTL circuit and an I^2L circuit as shown in Table IV-1. In Fig. 4-4(a) the circuit for an interface from TTL to I^2L is shown. The voltage step-down required is accomplished by four transistors. The base and collector of the first transistor are shorted to help the isolation of output and input. In conventional TTL circuits, the effect of output transistors on input transistors is usually minimized by reducing the inverse current gain using gold diffusion. However, in I^2L circuits, the inverse current gain is also the upward current gain which must be kept high for good performance. Gold diffusion is not recommended. Instead the base and collector of T1 in Fig. 4-4 is shorted. The loss of voltage drop because of this short circuit is made up by adding T2 in the voltage step-down circuit. T4 can be made either as a conventional isolated high gain transistor or as an inverted I^2L npn transistor without a pnp current injector. The high gain conventional version is preferred if driving capability is needed, for example, for driving a clock or a reset time. However, if the load is small, for example, with only a few fanouts, the inverted I^2L version can be used.

4.3 DIGITAL MEMORY

4.3.1 Static Memory

All SSI and MSI bipolar IC memories use the cross-coupled type of flip-flop circuit. Stored data can be changed only when the data line is activated. The memory is considered "static". The first bipolar injection memory cell is also a static memory, shown in Fig. 4-6. Two "two input NAND" gates are cross coupled. It has four access lines.

TABLE IV-1 VOLTAGE AND CURRENT LEVELS IN TTL AND I^2L CIRCUITS

	TTL		I^2L/MTL	
State	0	1	0	1
Voltage	~ 0.2 V	4-5 V	< 0.05 V	0.7-0.8 V
Current	~ 2 ma/fan out current sink	< 20 μa current source	< 100 μa/fan out current sink	current source

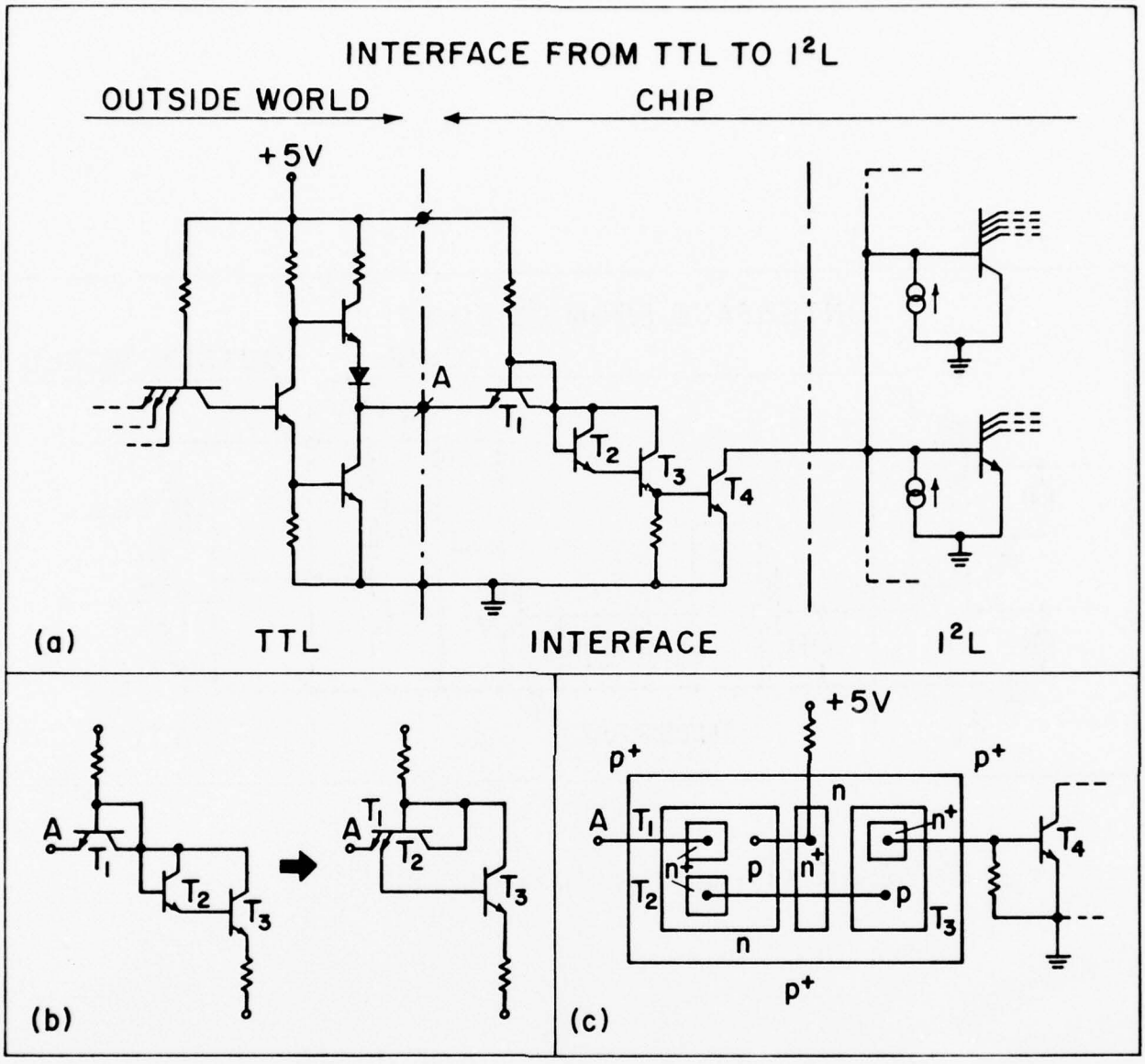


Fig. 4-4 (a) Interface Circuit from TTL to I^2L (b) Simplification of T_1 and T_2 (c) Physical Layout. (H74-1).

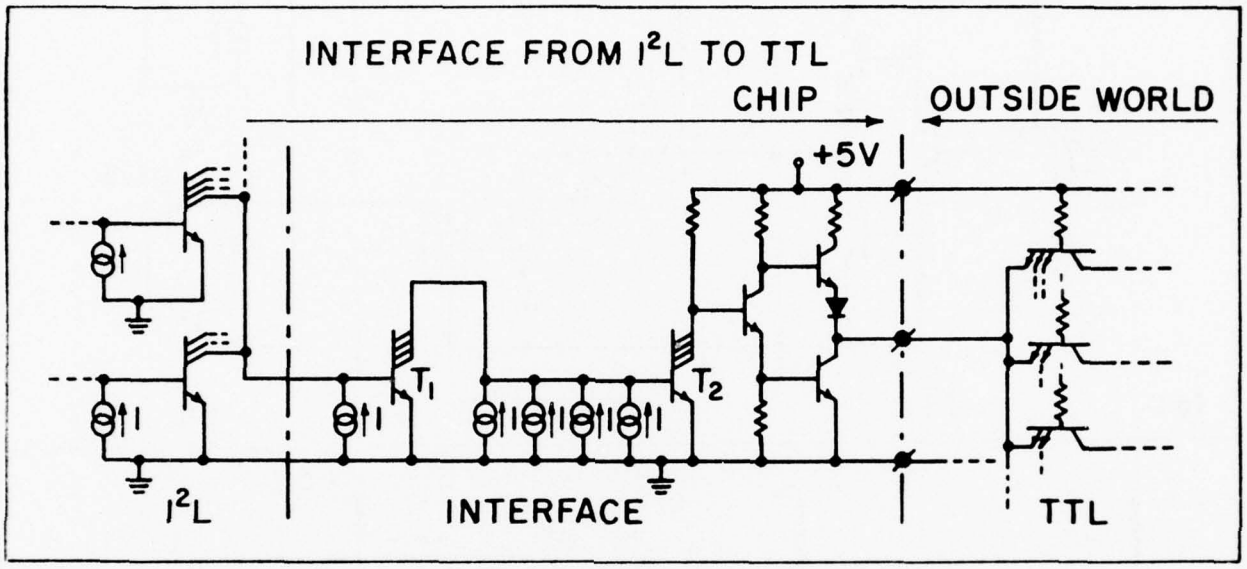


Fig. 4-5 Interface Circuit from I^2L to TTL. (H74-1).

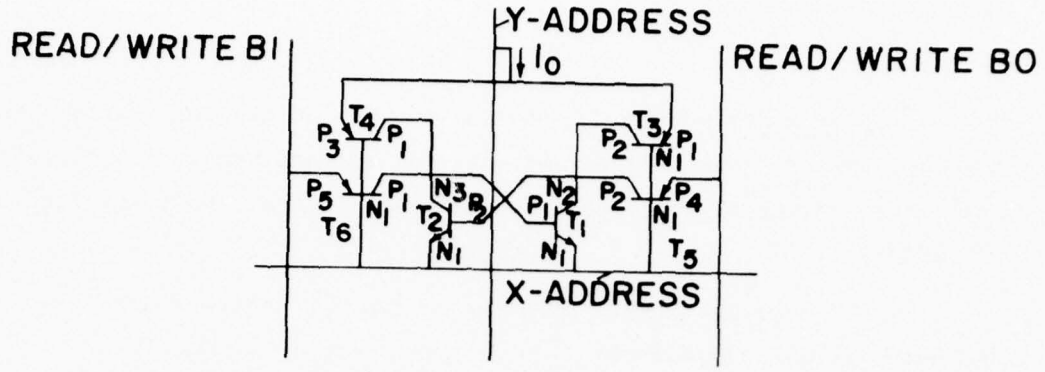


Fig. 4-6 Circuit Schematics of Static I^2L Memory Cell.

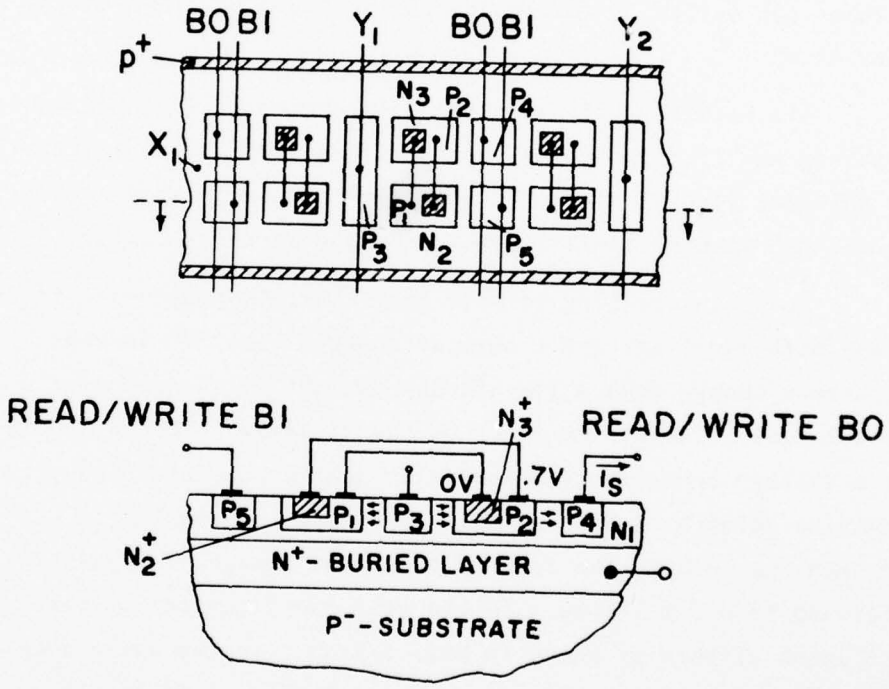


Fig. 4-7 Physical Layout of Static I^2L Memory Cell. (W73-1).

(a) Y address line. Collector outputs of two npn switches are tied together and are connected to the external current supply via two pnp current injectors serving as the load. The external current supply is used as the "Y" address.

(b) X address line. Emitters of two npn switches are tied together and serve as the "X" address.

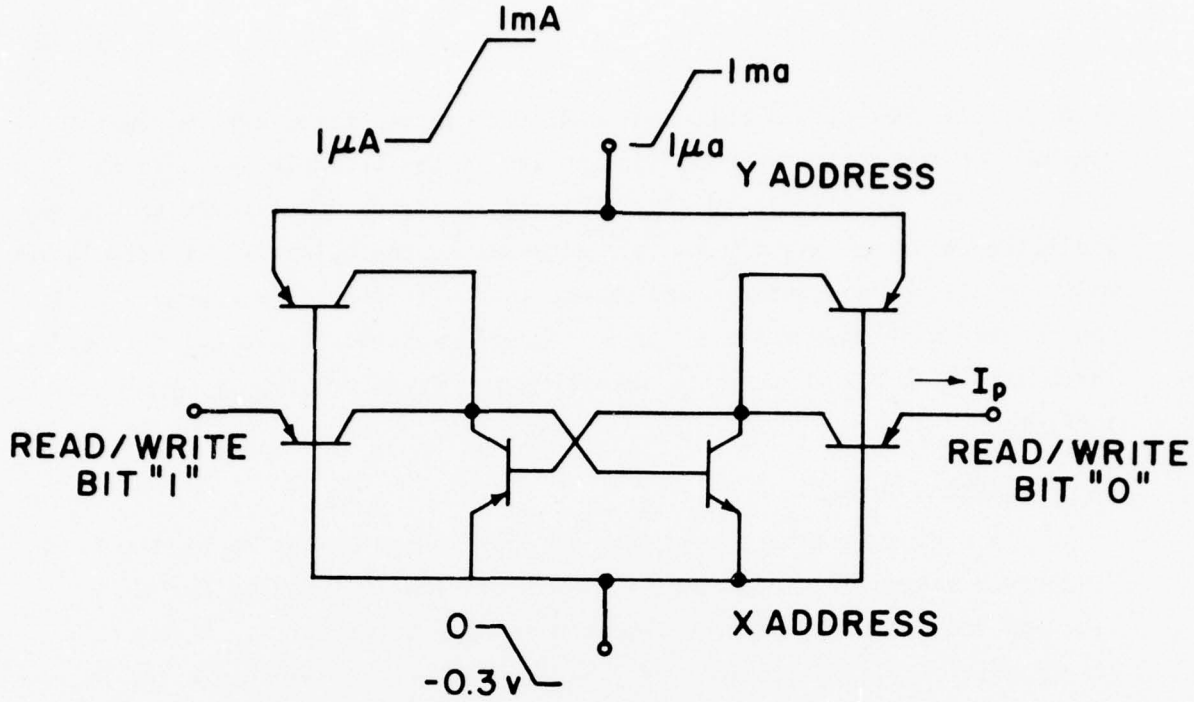
(c) Data "1" line for both read and write. The second base input of one npn switch is connected outside via a pnp injector. It is the bit "1" data line.

(d) Data "0" line for both read and write. The base input of another npn switch is connected outside via a pnp injector as the bit "0" data line.

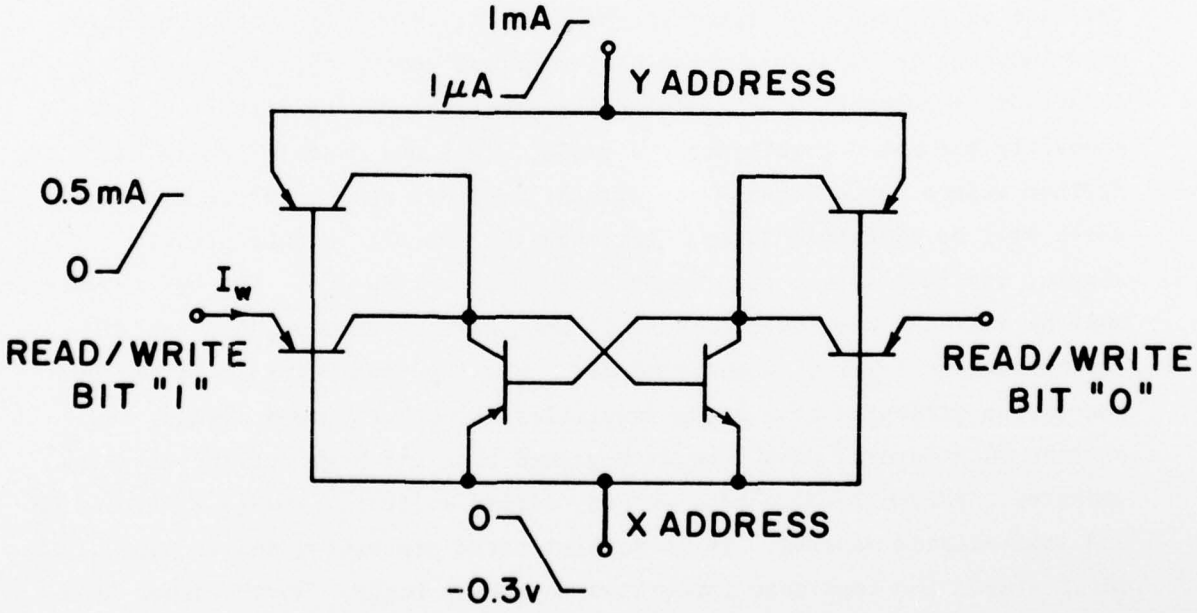
All together, six transistors are used: two npn transistors as switches and four pnp transistors as load and current injectors. However, in physical layout, all six transistors are merged together within the same n tub with no isolation between them as shown in Fig. 4-7.

It is interesting to note that the call addressing is accomplished by using both a voltage and a current change. The "Y" address is selected by a current change from a low standby current of the order of a few microamps to a larger value of the order of one milliamp. The "X" address is selected by a voltage change from a low value near ground at standby to a larger negative value around -0.3 volt. The data information is read out (or written in) both in the form of a current change, for example, from 1 microamp to 0.5 milliamp. In the read mode, current is taken out of the npn latch circuit as shown in Fig. 4-8(a). In the write mode, current is pumped into the latch circuit as shown in Fig. 4-8(b).

The first static I^2L memory is the Texas Instrument 4 kilo-bit S400 RAM. The fact that it came out in a 4 kbit size testifies to the LSI capability of injection logic technology. Its chip area is 20,000 mil^2, comparable to the size of 4 K dynamic MOS chip. Therefore, the cost should eventually be comparable. However, its access time is reported to



(a) READ OPERATION



(b) WRITE OPERATION

Fig. 4-8 Read and Write Operation of a Static I^2L Memory Cell

be only half that of a 4 kbit NMOS RAM. The access time, active power consumption and estimated cost per bit are listed in Table IV-2, which also includes other semiconductor RAMs. S. K. Wiedmann of IBM/West Germany projected an array layout using the advanced technologies of oxide isolation and self-aligned n^+ contacts and showed that a static I^2L/MTL memory cell can be made with only 1.1 mil^2 area, compared with more than 3-4 mil^2 today. Therefore, a 16 kilo-bit static injection logic RAM is claimed to be feasible.

4.3.2 Dynamic Memory

In a dynamic memory, the data is represented by the charged and discharged states of a capacitor. It was originally invented for MOS circuits and has never been implemented in bipolar circuits. However, a new dynamic bipolar injection logic memory circuit has been invented by Fairchild. Instead of six transistors typically used in the conventional static bipolar memory circuits, it uses only a pair of npn/pnp transistors and the parasitic capacitance of about 0.1 pF between the collector and the base of the npn transistor as shown in Fig. 4-9. Since the collector-base junction is usually reverse biased during memory operation, the capacitor is automatically isolated from the rest of the circuit. Consequently the space requirement is small. This new dynamic memory can further reduce space because its circuit requires only three access lines, which will be explained later. Although the circuit is conceptually simple, its fabrication requirements are quite stringent. The npn transistor must be fast and must have very small emitter-base capacitance. An ion implanted base layer is usually needed. The pnp transistor is formed by successive diffusion of n and p impurities through a common window, resulting in a lateral structure with graded base and high current carrying capacity. Fairchild also uses washed, walled emitters, Isoplanar isolation and self-aligned masking. It is sophisticated processing and is named I^3L, which stands for Isoplanar Integrated Injection Logic. On the other hand, they use only conventional photomasks and one layer of metallization.

For electrical operations, only three access lines are needed:

TABLE IV-2 TYPICAL PERFORMANCE OF SEMICONDUCTOR RAM

SIZE	TYPES	ACCESS TIME (ns)	ACTIVE POWER DISSIPATION (mw)	COST/BIT (Cents)	TYPICAL APPLICATIONS
1K	TTL Static	40-100	600-800	1.5	Buffer, cache
	NMOS Fast Static	70	600-800	1.0	Buffer, cache
	CMOS/SOS	150	4	1.5	Small main frame
	NMOS Static	150-500	300	0.3	Small main frame and peripheral
4K	I^2L Static	70-100	500	0.25	Small main frame, buffer, cache, peripheral
	I^2L Dynamic	90-100	400-500	0.25	Small main frame, etc.
	NMOS Static	150-550	350-500	0.2	Small main frame peripheral
	NMOS Dynamic	150-350	450-700	0.15	Large main frame and peripheral
16K	NMOS Dynamic	200-350	500-750	0.08	Large main frame

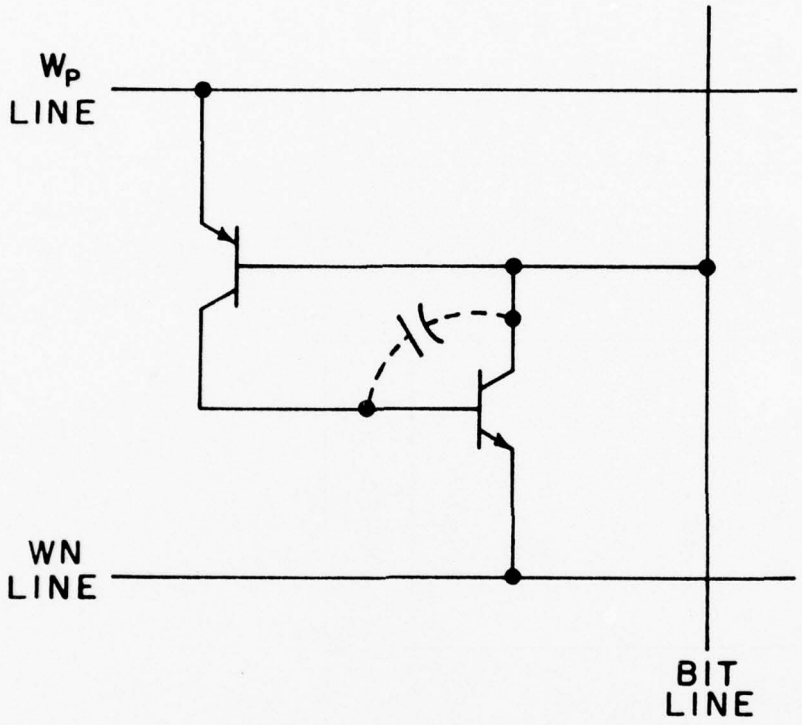


Fig. 4-9 Memory cell in the 4K dynamic I^2L memory. (S76-3).

Word line W_n - Connected to the emitter of the npn.
Normally biased at 3V.

Word line W_p - Connected to the emitter of the pnp.
Normally biased at ground.

Bit line - Connected to the merged collector of the npn and the base of the pnp.
Normally biased at 3V.

A "1" state is represented by 3 volts. The state "0" is represented by 2 volts or less. To write a "1", the W_n line is switched from 3 volts to ground. The bit line is charged to 3 volts throudh the npn transistor. To write a "0", the W_p line is switched from ground to 3 volts. The bit line is discharged through the pnp transistor to 2 volts or less. To read the data, the W_n line is switched from 3 volts to ground. If the capacitor was already charged, i.e., in a "1" state there is no change on the bit line. However, if the capacitor was discharged, i.e., in a "0" state, the bit line will be pulled down. To refresh a "1", the bit line is first sensed. If W_n is low the bit line is latched to 3 volts.

4.4 MICROPROCESSORS

Several companies are developing microprocessors using different bipolar injection logic circuits. However, only Texas Instruments has marketed a 4 bit slice type microprocessor (SBP0400) which was the first I^2L device to appear in the market. TI has also announced the development of a 16 bit I^2L microprocessor which is a part of a larger 990 minicomputer/microcomputer design program using both NMOS and I^2L technologies. The 16 bit NMOS microprocessor is labeled TMS 9900 and is already on the market. The 16 bit I^2L microprocessor is labeled SBP 9900 and will be commercially available in 1977.

When LSI microprocessors were first developed, the objective was limited to relatively simple computations. Most of the 8 bit microprocessors are used for peripheral controllers and small to medium data-handling systems. However, with more experience in LSI development, the objectives of microprocessors have been considerably raised to 16 bit processors offering data

processing performance comparable to a 16 bit minicomputer.

The 990 program has this objective. The architecture was designed for low performance applications using a small number of additional parts but is also flexible so that it can be expanded into more complex systems. 990/4 is the low performance end of the family. It uses one single LSI microprocessor chip and memory mounted on a single printed circuit card. 990/10 is capable of addressing up to one million words of memory and is supported by full range of peripherals (discs, tapes, etc.).

4.4.1 SBP 0400 4 bit Microprocessor

The features of SBP 0400 are summarized as follows.

(a) Architecture. It is a 4 bit slice microprogrammable microprocessor chip. Its organization is shown in Fig. 4-10. It contains the following parts:

(i) Arithmetic. A 16 function symmetrical arithmetic logic unit with full carry look ahead logic.

(ii) Registers. Two 4 bit working registers which can handle both single and double length operations. Eight general register files that include a program counter and incrementor.

(iii) On-chip memory. A factory programmable logic array (PLA) is used instead of the usual fixed size control ROM. It can contain 512 micro operations.

(iv) Access. It has parallel access to all control, data and addressing I/O functions. This helps to reduce the device cycle time.

(b) Devices. The chip is fabricated by a standard I^2L process. It has over 1600 gates on a chip of approximately 30000 mil^2 mounted in a 40 pin package. Devices on the early SBP 0400 chip were reported to operate with typical propagation times of 110 to 530 ns at a power consumption of 28 mW.

(A) PROGRAM CTR REG. 7
(B) RELATIVE POSITION CONTROL
(C) ENCODED POSITION
(D) WR MUX
(E) REGISTER-FILE INPUT
(F) REGISTER-FILE MUX
(G) REGISTER-FILE BUS
(H) OPERATION REGISTER (20 BITS)
(I) EXTENDED WORKING REGISTER

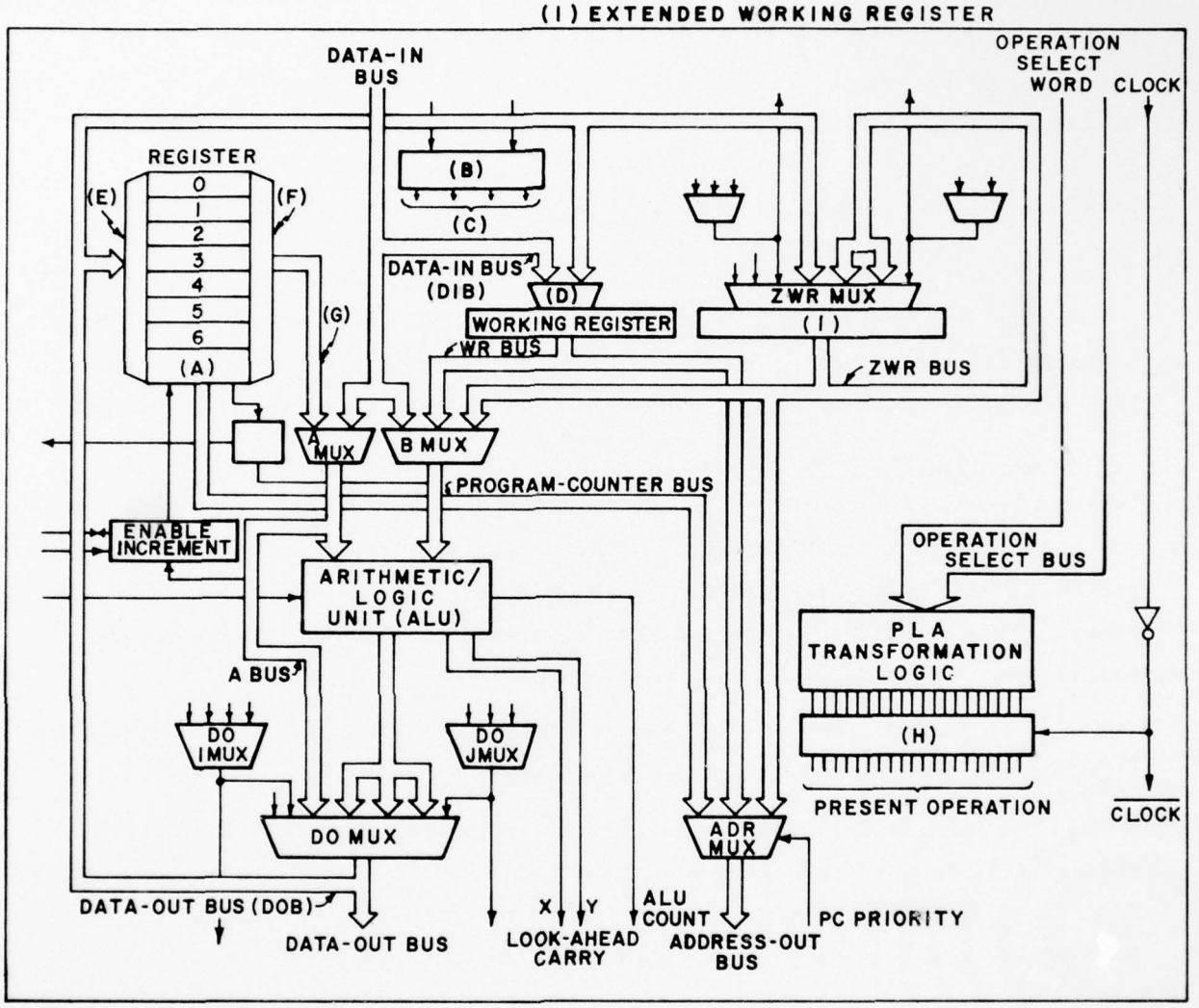


Fig. 4-10 Organization of SBP0400 I^2L 4 Bit Slice Microprocessor (H75-1).

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(c) Operation. The SBP 0400 is operated by static edge triggering, with TTL compatibility. 512 microinstructions can be programmed on the PLA. Each microinstruction can be executed within a single clock cycle. A 9-bit word is used to select the operation. However, the word size is a multiple of four. Using four SBP 0400's, a 16-bit microprocessor can be obtained. For word size over 8 bits, an external look ahead generator should be connected by using both ALU carry generate and ALC carry propagate terminals.

4.4.2 SBP 9900 Microprocessor

Less information is available for the SBP 9900 because it has not been marketed commercially at this time. However, since it will be similar to the NMOS TMS 9900, quite a bit of information can be obtained from TMS 9900.

(a) Architecture. It has a 16-bit CPU which is a single LSI chip implementation of a commercial 16-bit minicomputer containing the instruction set, I/O structures, and parallel bus structures for separate address, control and data lines. Its organization is shown in Fig. 4-11. It is memory to memory oriented instead of register file oriented, as found in many microprocessors.

(b) Instruction Set. It has a 69 instruction set including multiplication and division and seven addressing modes.

(c) Registers. It has 3 hardware working registers and 16 general purpose registers in main memory which may be used as accumulators, pointers, index registers, etc. They also offer efficient handling of context switching by changing the program through subroutines and interrupts.

(d) Fabrication. It probably is fabricated by an improved I^2L process using standard device structures. Shallow epi-layers and ion implantation are probably used. No information can be found on its device density and chip size, except that it is contained in a 64 pin dual in line ceramic package approximately 3.2 x 1 inches.

(e) Operation. Its operation was reported to be similar to that of the TMS 9900 except that it uses only one single-phase clock and one power supply instead of one 4-phase clock and three power supplies. The microcomputer can be operated at 3 MHz.

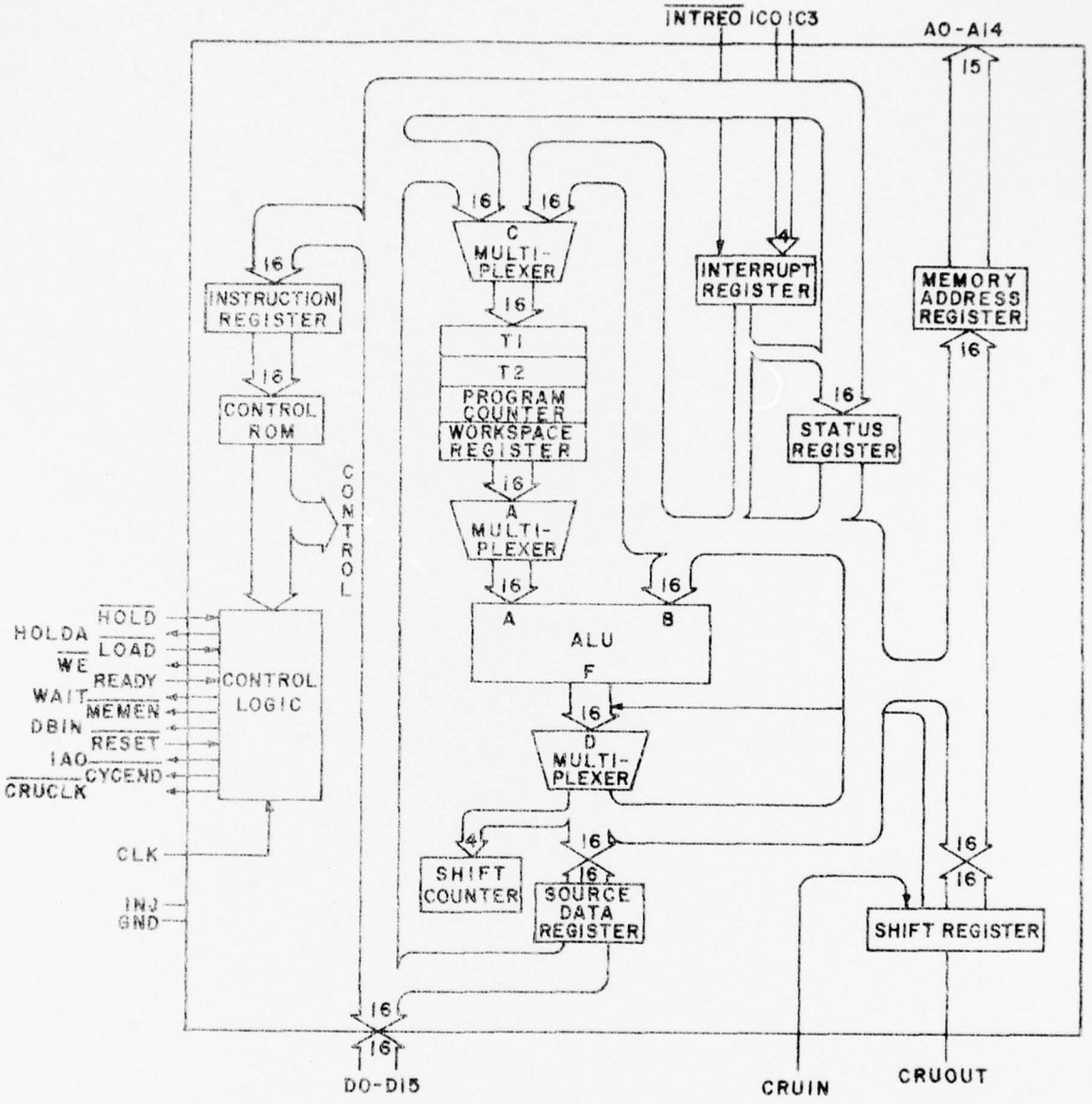

Fig. 4-11 Organization of SBP9900 microprocessor. (Texas Instruments).

CHAPTER V

BIPOLAR INJECTION LOGIC DEVELOPMENT ACTIVITIES

5.1 INTRODUCTION

There is little doubt that the United States is the world's leader in electronics although in some specific areas, such as audio entertainment equipment and a few others, Japan and some European countries are quite advanced. However, in this important development of bipolar LSI injection logic, the invention and early development were made by two European companies: IBM Research Laboratories at Boeblingen, West Germany and Philips Research Laboratories at Eindhoven, Netherlands. The bulk of technical advances and theoretical developments were also reported mainly in papers originated from these two groups. Today, many companies in the United States and other countries are intensively pursuing this technology, some openly but many secretly. While there are hints of commercial equipment development from many companies, new advancements of technologies have been reported in detail by companies abroad. Therefore, this survey will start with foreign companies.

It should be noted that bipolar injection logic has caught the electronics industry's imagination: the development efforts are intensive, competi[illegible]nd the progress is fast. Consequently, some of the most important devel[illegible] probably have never been publicized. Also, results of the following sum[illegible]y will be quickly outdated.

5.2 FOREIGN COMPANIES

5.2.1 IBM/West Germany

IBM/West Germany probably started the development of bipolar injection logic earlier than other groups. Back in 1968, engineers at the IBM Research Laboratories in West Germany developed a "nano-ampere cell." It used a pnp transistor as a current source and combined it with an inverted npn transistor. It did not need large resistors to limit the current and could be operated even at one nano-ampere. Three years later, the invention of MTL, merged transistor logic, was announced.

Probably following the general IBM practice, which does not discuss openly product development until an equipment is ready for sale, not much is publicly known about their application development using MTL. However, the inventors of MTL at IBM, H. Berger and K. Wiedman, have steadily been publishing a series of thorough and authoritative technical papers on MTL. From these papers, it needs no stretch of imagination to guess that IBM/West Germany and IBM in the United States are pursuing the developments of MTL memories, logic circuits, microprocessors, interface circuits and others related to computers. It is also obvious that they have the know-how in developing MTL devices for instrumentation, control, entertainment and other applications. Being a giant company not active in sales of this type of equipment, it is not clear whether they are actively pursuing their developments. However, a short paper on voltage clamp development was published.

5.2.2 Philips/Netherlands

The development of I^2L at Philips was started in 1970 when K. Hart and A. Slob were developing a one nano-second current mode logic chip. After recognizing that a logic gate needs only a switch and a current source, they soon arrived at the ingenious idea of operating the transistor upside down as a switch and a single forward biased diode in the neighborhood of the switch to generate current. I^2L, as it is known today, was announced in 1971-1972.

Since that time, Philips has reported a wide variety of I^2L device developments as listed in Table V-1. In September 1975, an I^2L IC chip for an electronic organ was described. Its chip area is 3.5 mm^2, of which 1.3 mm^2 is taken up by 19 binary dividers, the rest by interface and output stages. It is important to recognize that this chip combined I^2L and ECL technologies. The fast ECL circuit is used for the first two stages of frequency dividers. The following two are special I^2L with parallel gates for larger injector current and higher speeds. The remaining 15 dividers are conventional I^2L. The gate density is 110 gates/mm^2. It could be operated at a voltage of 12 volts and relatively high current up to 40 mamp.

TABLE V-1 I^2L DEVICE DEVELOPMENT AT PHILIPS

	NO. OF GATES	CHIP AREA (mm x mm)
Memory		
108 bit shift register	820	2.96 x 2.85
1536 bit ROM (for small calculator)	∿1000	3 x 4
256 bit shift register (for electronic organ tone generator)		
Logic		
Control logics	980	4 x 4
Modules		
LCD driver	200	2.2 x 2.4
Digital voltmeter counter	325	2.2 x 2.4
Electronic organ tone generator	180	1.2 x 1.5
Electronic organ 2^{19} counter, input/output		3.5

5.2.3 Intermetall GmbH/West Germany

Intermetall is a member of the ITT Semiconductor Group. Two applications are being developed. First is the electronic organ. Two chips, SAA1004 and SAA1005 are being developed. The chip area is approximately 2.4 mm^2 and contains frequency divider circuits. The second application is for digital clocks. A chip, UAA1007 is being developed. Its chip area is 2.9 mm^2 and contains the clock drive circuit, alarm program circuit, and the output stage for the alarm tone. The oscillator frequency is 2 kilohertz.

5.2.4 Mitsubishi Electric Corporation/Japan

Mitsubishi is developing the vertical injection logic technology (VIL). In this device, a vertical pnp current injector is used below the npn switch transistor. It differs from the SFL of Plessey in that the p emitter is reached from the top.

Compared with conventional I^2L, VIL was reported to operate at faster speeds (8.8 nsec), lower power dissipation (8 μW) and smaller delay power product (0.07 pJ). It was claimed that 1 ns gate propagation delay is possible.

Using VIL, the following devices are being developed:

4096 and 16384 bit RAM's

8 and 16 bit microprocessors

digital watch chip

linear to digital and digital to linear interface circuits.

5.2.5 Plessey Co. Limited/England

Plessey is developing Substrate Fed Logic (SFL). In this structure, the npn switching transistor is on top of the pnp injector. Schottky diodes are used at the base input to limit the logic swing. It was reported that its packing density is higher by a factor of two to three over conventional I^2L. The delay-power product is lower. A value of 0.05 pJ was reported for delay down to approximately 100 ns. Further decrease of delay requires an increasingly higher current which resulted in higher t_dP product above 1 pJ.

At a power dissipation of 100 μW, the delay is in the range of 10 to 20 ns. Plessey is fabricating SFL using their process 3 technology which has been used to make fast analog and ECL circuits. V groove etching technique is also used to provide dielectric isolation.

Plessey indicated that they are concentrating on the applications of injection logic in both civilian and military communication markets at the present time and keeping a watchful eye on the television, watch, microprocessor and other markets. They are developing seven new injection logic products. One of them is a large 1000 gate standard array which could be quickly customized. Other developments mentioned are:

225 gate programmable pseudo-random sequenced generator, called WM-1 for secure communication applications

Quad decade fully programmable counter

256 bit RAM for battery powered portable equipment

Frequency synthesizer in the 200-300 MHZ range using combined ECL and injection logic techologies for mobile communication applications.

5.2.6 RTC-La Radiotechnique Compelec/France

An 8 bit parallel operation microprocessor is being developed by RTC-La Radiotechnique Compelec using I^2L, for Electronique Marcel Dassault (EMD). It is called P-8 because it processes 8 bit words in parallel to attain high speeds. Logic operations take 900 ns at most. A logic block performs 11 operations such as intersection, exclusion and jumps. Arithmetic operations on 8 bit words takes less than 1.2 μs.

The chip has an area of 15 mm^2 and is mounted in a 40 pin ceramic package. It contains the following blocks: Logic block, arithmetic unit, and a block for forward carry operations. These three blocks are linked to input and output registers through two multiplexers and an 8 bit, 8 channel shift register. In addition, there are three additional main blocks for control, tests and three state outputs which interface the I^2L circuit to TTL. The whole P-8 contains

the equivalent of 520 gates plus input/output interfaces on 15 mm^2 and consumes only 400 milliwatts.

5.2.7 Sharp Corporation/Japan

The calculator pioneer, Sharp of Japan, revealed their interests in both I^2L and MOS LSI. Development efforts are reported in microprocessor central processing units, digital watch chips for the watchmaker Orient and displays. They hinted that an I^2L/electrochromic display could phase out LED and liquid crystal displays in their guesstimation.

5.2.8 Siemans AG/West Germany

Siemans AG is developing Current-Hogging-Injection Logic (CHIL). It combines the advantage of high packing density, low delay power product of injection logic and the advantage of input flexibility (serial-parallel-gating) of current hogging logic. This is achieved by using two pnp transistors between the external current source and the npn switching transistor. It results in two serial inputs, offering flexibility in logic implementations.

Except for the announcement of this new circuit, no report of device development has been found.

5.2.9 Tokyo Shibaura Electric Company/Japan

Tokyo Shibaura Electric Company is developing S^2L-- Self-Aligned Superinjection Logic which not only uses a self aligned double diffusion technique to make injectors of submicron base width but also surrounds the S^2L cell by a four sided injector. It also permits independent choices of impurity concentrations for emitter and collector of the pnp transistor. For the npn transistor, the doping profile in the base is inverted giving very high β_u in the 10 to 100 range for a S^2L cell with a fan out of 6. Delay-power product in the range of 0.06 - 0.1 pJ/gate with a minimum delay of 10 ns and a power consumption of 80 μW were reported. The packing density is quite high also at 420 gates/mm^2. They also reported the development of oxide isolation circuits. However, no circuit development has been identified.

5.3 COMPANIES IN THE UNITED STATES

5.3.1 Introduction

Although bipolar injection logic was invented and first developed in Europe, companies in the States have been giving more intensive efforts in developing applications. Probably due to the competitive nature of the commercial market, little technical details have been published. In general, companies who plan to sell injection IC chips in the future have been making marketing types of announcements on their activities. Others who are their own customers such as Bell Telephone Laboratories, Hewlett Packard, Hughes Aircraft, IBM, RCA, Rockwell Microelectronics, Tektronix and others probably all have some activities in bipolar injection logic but do not see the need of discussing their developments at this stage. However, much more information will come out in 1977 because in addition to TI, Fairchild, Signetics, several other [illegible]nies are going to introduce more commercial I^2L devices soon.

5.3 [illegible] Telephone Laboratory

Bell's Allentown Laboratory is developing Schottky I^2L technology (SI^2L). Schottky diodes are used at the output collectors for decoupling. It is believed that their OXIM (oxide-isolated-monolithic) technology is used in some SI^2L developments. The delay-power product is around 1 pJ with minimum delay in the 10-30 ns range. It is not definite whether 10 ns has been achieved at 1 pJ. Circuit density was reported to be around 250 gates/mm^2 with 5 micron line resolution and 85 gates/mm^2 with 10 micron line resolution. It was claimed that 1 ns propagation delay and 0.1 pJ delay-power product are feasible.

No report was given in regard to their applications development. It is obvious that they will be used in telephone and data communication systems.

5.3.3 Exar Integrated Systems

Exar is known for their bipolar linear integrated circuit products such as phase lock loops. However, they have reported an I^2L digital watch development. Their unique approach is the use of an RC oscillator as well as the more expensive quartz crystal. The price is 80 cents to one dollar for the RC oscillator versus three dollars or so for the 32.72 kHz quartz crystal. Its

stability is not nearly so good as that of quartz oscillators. But a stability of 90 to 100 parts per million, or about 3 to 4 minutes per month is possible. Such a watch probably is acceptable to some section of the market if the price is low enough. The goal is under 30 dollars. More specifically, a universal watch chip of about 15,000 to 20,000 square mils is being developed. It contains six functions--seconds, minutes, hours, date, month, am/pm, as well as seven segment and digital drivers for LED display. It requires no more than 3 to 5 μamp during standby and should cost about $2-3. Either a crystal oscillator or an RC oscillator can be used. One idea to improve the stability of the RC oscillator is to use an MOS capacitor on the chip connected to a series resistor and to an off chip trimmer capacitor. Using laser trimming of the resistor and external trimming of the capacitor, accuracy within 25 parts per million can be achieved. It was claimed that RC oscillator design could also meet the requirements of stability within 50 parts per million for power supply variations and 25 ppm for component aging. Such an RC oscillator requires about 7 to 10 μamp in addition to the 3 to 5 μamp for I^2L logic circuit. These would be within the one year lifetime of standard silver-oxide batteries. No estimate was given for the current requirement when the LED display is energized. Several parts which are being developed are listed as follows.

Part No.	Type
XR 401	Quad Inverter Array
XR 402	Quad Two Input NOR Gate
XR 403	Dual Latch Exclusive OR Gate
XR 404	Dual D Flip-Flop
XR 405	Decade Counter/Divider
XR 406	Input Buffer/Current Source
XR 407	Output Buffers

5.3.4 Fairchild Camera and Instruments

Fairchild used their patented Isoplanar process and is developing the Isoplanar Integrated Injection Logic (I^3L). Good device performance has been reported:

Delay-power product	< 0.15 pJ
Minimum gate delay (fan out of 4)	4 ns (at 1 mA injection current)
Packing density	> 250 gates/mm^2.

Their I^2L effort seems to be aiming at high performance applications and not in competing with their own MOS efforts. The following developments have been announced.

Memory. 1 kilobit static RAM, 4 kilobit static RAM. A new circuit concept has been developed which uses only one I^3L cell to dynamically store one bit of information. This is the first dynamic memory using bipolar technology. Their first 4 kbit I^3L dynamic memory has access time in the 100 - 150 ns range with a chip size of 112 x 129 mil (14,000 mil^2), no larger than a 4 kbit MOS RAM. The cell size is approximately 648 square microns. This type of memory will obviously be used as a small buffer or cache memory. It might also be used as volume memory for add-on and other high performance main-memory applications.

Processor. It seems that a 16 bit I^3L microprocessor is being developed. 16 bits is chosen probably not to compete with their successful 8 bit NMOS processor. For control section of a processor, they have reported the development of a I^3L program sequencer which has 10 bit address and can address control memories with 1024 word micro-programs. It is a 40 pin DIP package of a 2.5 x 3 mm. Chip frequency is 10 MHz with 700 mW power consumption. It seems that an intensive effort is being pursued to develop a host of I^3L devices for their Macrologic family.

Digital Watch. It seemed that an I^2L digital watch chip was being developed at one time. But it was shelved early in 1976 in favor of a CMOS approach.

5.3.5 ITT Semiconductors

ITT is developing a new oxide-isolation fabrication process using electrolytic anodization. Oxide isolated I^2L circuits are being fabricated using this process, called anodic I^2L, or AI^2L. Preliminary reports claimed that chip density and speed are doubled compared with conventional I^2L circuits. One or more masks could be eliminated which would result in 25% reduction of cost.

Application developments in two areas are reported in progress. First is a digital watch module. Their unique approach is a kit of I^2L watch parts. It is organized in the following way. All watch circuit components--timers, frequency dividers, buffers, crystal inputs, display driver outputs, are fabricated on a master slice. They are scribed and packaged as a kit. A customer can choose different amounts of packages depending on the complexity and number of functions his watch needs. Once a customer competes his design from the kit, it can be reduced and optimized on a single chip using the high density capability of I^2L. Using this approach, I^2L watches from simple four functions to seven functions are being considered, including added features such as elapsed time and time zone. An I^2L design kit is already available which consists of 15 building blocks.

It seems that they are also developing a 4096 bit RAM.

5.3.6 Micro Components Corporation

Micro Components Corporation is a subsidiary of North American Philips. They are developing an I^2L light to frequency converter chip 12 x 36 mil in size, for camera shutter applications. This chip probably will be extensively used in Eastman Kodak's Instamatic camera. It can be operated with only tens of nano amps generated by a photodiode. This tiny current is enough to drive a current controlled 7 stage ring oscillator which produces an output of 0.4 - 0.5 volt peak to peak at frequencies varying from 100 Hz to 1 MHz, proportional to the light level. The delay power product is 0.3 pJ. The oscillator has a buffer amplifier output which can drive an FET load or other high impedance device. This light to frequency converter can be operated by the photodiode without any power supply. But the whole shutter circuit needs battery power. The total functions are four--it selects one of two possible apertures depending on ambient light levels, times the automatic shutter and indicates low light levels and low battery power. They estimated that the circuit can be produced and sold from 50 cents to $2, compared to between $2 and $5 for a more conventional approach.

5.3.7 Motorola Incorporated

At one time Motorola had an extensive program in I^2L. However, they reduced the bipolar LSI effort in the Spring of 1976 and, at the present time,

are concentrating on MOS for LSI applications. I^2L is still being developed but mainly for combined digital and linear applications. Before this policy, they mentioned the development of a wide variety of I^2L/MTL devices. They were also developing complementary constant current logic (C^3L), another version of bipolar injection logic.

In computer applications, it was once rumored that they might second source the 4 bit I^2L processor. Independently, two I^2L microprocessor chips were being developed as part of their Megalogic family which is a mixed collection of TTL compatible circuits. This I^2L processor was to be an 8 bit device bridging the performance gap between their M6800 NMOS processor (fixed instruction, low speed, 50 ns gate delay for point of sale, test equipment type of applications) and high performance M10800 ECL processor (microprogrammable, 2-5 ns gate delay). Since the processor chip development costs as much as support material, the I^2L processor will first use the support material for M6800. However, a host of I^2L peripheral and interface circuits were being developed to serve a wide variety of microprocessor systems besides the Megalogic family. They could be either NMOS or I^2L. The peripherals are all bus oriented. The following were three important members being developed at that time:

(1) Multipliers -- 8 x 8 bit, 6 x 16 bit, 8 x 8 multiplier and divider. The execution time for the 8 x 8 multiplier was reported to be around 2 to 4 μs, compared with 200 to 300 μs, usually required if a software algorithm is used.

(2) Programmable delay module which can generate time windows from microseconds to an hour for computer and industrial applications. It was not for high performance and probably was fabricated by a process not even using epi-layer.

(3) Direct memory access (DMA) controller to be used with a microprocessor. It was fabricated by a high performance I^2L process which yields performance of 5 to 15 ns propagation delay. It allows the microprocessor to be disconnected from the system while the peripheral device and RAM are exchanging data at high rates. Without this DMA, data transfer would be limited by the speed of the microprocessor.

Motorola has a large I^2L/MTL program in automotive applications. They are developing an I^2L clock chip for Chrysler, also a display driver, controller and 3 chip synthesizer for auto-radio. The synthesizer uses an approach similar to one proposed for digital television tuning. It is a classical frequency synthesizer combining harmonic mixing with a birdie counter. The on-chip hardware includes a VCO (voltage controlled oscillator), phase lock loop feedback, a dc ramp generator and a low pass filter. The birdie generator gives a series of frequency blips covering the FM band. When the VCO is addressed digitally, the birdie generator starts the voltage ramp. When the ramp reaches the voltage level stored in the VCO, the synthesizer locks onto the station as the voltage is fed to tuning varactors. The controller chip will be tailored to the customer's specifications. It could contain pre-selected stations, or a signal seeker search for automatically scanning the stations. Together with an I^2L clock chip, the system could be programmed to display time or even engine performance data.

There were some performance data reported around November 1975. For performance at 25-50 ns gate propagation delay, a random logic chip of 150 x 150 mil^2 size typically contains 1,000 gates, consumes about 40 μw/gate (i.e., 40 mw/chip). It will cost around $10-15 or 1 cent/gate.

5.3.8 National Semiconductor

National Semiconductor has a strong bipolar capability. However, it has not yet made big waves in bipolar LSI development. It is safe to assume that they have keen interests in I^2L/MTL development. At present, they are developing digital watch circuits. Recently, they indicated that an I^2L/MTL chip, DM93415, is being developed using oxide isolation on a 100 x 100 mil chip. It is similar to the Fairchild Isoplanar 93415-A 1 k bit static bipolar RAM with 45 ns access time. Another 4 k bit static RAM probably will be developed also with an access time around 100 ns. However, no indication was made if they are pursuing other I^2L developments for microprocessor, instrumentation, industrial or other applications.

5.3.9 Northrup Research and Technology Center

Northrup is not a commercial electronics company. Its R/D programs are mostly oriented toward military electronics applications. Its I^2L

program was to develop a digital frequency synthesizer. The initial goal was moderate for a synthesizer of 3 bit input and 10 bit output. No specification was set for hopping rate, bandwidth, etc. The plan was to develop a device which can be expanded and up-graded to a level useful in command, control and communication systems which will employ a fast frequency hopping technique to achieve anti-jamming and/or low probability intercept capability by way of spread spectrum. They have also investigated the advantages of oxide isolated I^2L. Being a military electronics oriented laboratory, Northrup is also studying radiation effects on I^2L circuits.

5.3.10 RCA

RCA hinted that they are developing I^2L devices for a wide range of applications: television, time keeping, instrumentation and automotive. However, specific developments were openly discussed only in the area of combined linear/I^2L digital circuits with the following application developments:

Analog to digital and digital to analog interface circuits

Monolithic OP AMP which combines I^2L for digital processing and bipolar circuit for linear processing

I^2L circuit to stabilize vertical sweep in TV receivers for cases of marginal TV reception.

5.3.11 Signetics

Signetics has active programs in developing both I^2L digital and combined analog/I^2L digital applications, using their standard Schottky production process.

For computer applications, they will soon introduce two peripheral devices. One is a cyclic-redundancy character generator and checker, 8X-01, which is pin-to-pin compatible with Motorola and Fairchild's TTL devices. The other is 8X-03, a first in-first out shift register for magnetic tape systems to deal with the data synchronization problem. Other peripherals being developed are:

Direct memory access chip

64 word x 9 bit first in-first out memory

16 word x 8 bit last in-first out memory

16 x 16 bit multiplier

Frequency synthesizer.

All these new I^2L circuits will operate at 10 MHz which is very high compared with the speed of other I^2L circuits in development. They are also developing an I^2L microprocessor which is very similar to their 2650 NMOS 8 bit microprocessor.

Signetics also has programs developing analog/I^2L digital circuits. One example is a disk drive. I^2L is being considered to convert the analog data off the disk to digital data.

At present, their I^2L circuits could operate in the 5 to 10 ns range. They claim that 2 ns is possible.

5.3.12 Stewart-Warner Microcircuits

Stewart-Warner Microcircuits is offering a semi-customized I^2L chip, named SWAP (Stewart-Warner Array Programming). Its concept is based on a master chip with a standard pattern of circuits that have not been interconnected. Interconnections can be specially designed and implemented according to the customer's requirements. It is fully compatible with DTL, TTL, CMOS and discrete circuits. Interface circuits are available at each I/O pad. Two SWAP circuits are available:

16 pin device with 208 gates and 14 interface circuits

24 pin device with 408 gates and 22 interface circuits.

Typical circuit functions that can be configured are

logic circuits
monostable and astable multivib
flip-flops
oscillators
Schmitt triggers
etc.

5.3.13 Texas Instruments

TI is considered by many as the industry's leader in I^2L technology because they are the first company introducing a commercial I^2L product--the 4 bit SBP0400 microprocessor. They have a wide range of application developments. We have not found a document describing their overall activities. The following is a partial account of what is available in open literature.

For computer applications, a second generation 4 bit microprocessor is being evaluated in-house. It is believed that a conventional I^2L structure is used without Schottky devices. Ion implementation is probably used in the fabrication process. With smaller line resolution, the second generation microprocessor is 3-4 times denser, operates 4-5 times faster but with the same power-delay product. Propagation delay is now around 10 to 20 ns at a current level in the neighborhood of 100 μamp. A 16 bit microprocessor chip SBP9900 is also being developed which contains the CPU, control memory, input and output interfaces. The main memory is on a separate chip. It is being considered for navigation applications in the Navstar/Global Positioning System. The SBP9900 will be used as the navigation processor in the data processing system. It can be operated with one power supply and one clock at 3 MHz. The power consumption is only 0.5 watt. It is claimed to have met the military temperature specification. For comparison, TI's own NMOS TMS 9900 microprocessor will consume 1 watt at 3 MHz and requires four phase clocks and three power supplies.

For digital watch applications, TI is making I^2L chips for Benrus. It also has plans to market watches directly, including four models starting from $100. The I^2L watch chip has five functions--second, minute, hour, date and month, and LED display. A 32 kHz crystal oscillator is used. The power dissipation is 8 μamp standby and 30 ma when energized for display.

For memory applications, TI is developing two 4 kilobit static RAM's in an 18 pin package.

S 400 For 75 ns access time, the power consumption is 500 mW. It is claimed to be 2 to 3 times faster than NMOS 4k RAM's. It is operated by a 5 volt battery and has Schottky TTL peripheral circuits. The chip

size is 20,000 mil^2, claimed to be only half of NMOS memory.

LS 400 is a low power version of S 400. For 150 ns access time, the power consumption is 165mW.

For camera applications, TI is developing a 3 mm^2 chip which combines half digital and half linear circuits, about 1200 elements. The digital circuit is a 20 stage frequency divider with LED driver. This chip probably will be used in Cannon AE1 35 mm single lens reflex camera. Other semiconductor chips will be used. One is a Toshiba photosensor and preamplifier chip. The other is for a transistor current switch.

For television applications, TI is developing chips for both applications of deflection functions and remote control. Horizontal processor and vertical countdown circuits are being made on the same chip, competing with other multi-chip and discrete approaches.

For analog applications, an analog to digital converter and a universal cathode ray tube controller are being developed.

At present, the custom chip is reported to cost around $10-20.

Because TI is also interested in developing military electronics applications, it has been active in evaluating radiation effects on I^2L devices.

5.3.14 Other Groups

Injection logic is still a young field; there are other active groups wihch either have not reached the stage or see no benefit in announcing their efforts. Chances are good that the following companies have in-house activities from two or three man efforts to much larger programs:

Advanced Micro Devices*, Hughes, Hewlett Packard, Intel*, Monolithic Memories*, Raytheon*, Rockwell, Transitron*, etc.

The * indicates those companies who have bipolar microprocessors on the market, listed in Table V-2.

5.4 OTHER SIDE OF THE COIN--MOS ADVANCEMENTS

Injection logic is one of the most glamorous LSI developments in the past few years. While there is no doubt that it is the logic family which

TABLE V-2 COMMERCIAL BIPOLAR MICROPROCESSOR* (DEC. 1975)

	LSI TECHNOLOGY	CPU BITS	CYCLE TIME (ns)	POWER (watt)	ADDRESS CAPACITY	REMARKS
Advanced Micro Device 2901	LSTTL	4	100	0.92	64 K	
Fairchild 9400		4			64 K	e chip CPU
Intel 3002	STTL	2	150	1.45	512	
Monolithic Memories 6701	STTL	4	200	1.12	64 K	
Motorola 10800	ECL	4			64 K	Clock on chip
Raytheon RP16	ECL	4			64 K	Multiple chip CPU
Texas Instruments SBP0400	IIL	4	1000	0.13	64 K	Clock on chip
Transitron 1601		4			32 K	

* Only a few specs are given. Comparison can only be made using benchmark programs selected for a given application.

vaulted the bipolar IC into LSI and has great potential, it is interesting to take note of some leading companies' activities, or lack of activities, in this area.

A notable example is Intel, one of the industry's leaders in semiconductor memory and microprocessors, who seems to have no commercial I^2L development at this time. Another example is National Semiconductors who has strong bipolar capability but probably is not pushing I^2L for microprocessor, instrumentation and control applications at this time although they do have I^2L digital watch and memory developments. It should not be interpreted that they will not enter the bipolar injection market in the future. But at the present stage, the "cost-performance" tradeoff probably has not convinced them in favor of I^2L yet. The same consideration probably is behind Motorola's decision in slowing down their bipolar LSI effort.

It is clear that considerable mileage is still left in MOS technology, especially for memory application when cost-performance tradeoff is considered. Using innovative fabrication techniques such as ion implanted gates, double level interconnections, small low capacitance scaling technique and new circuit approaches like DMOS, VMOS, substrate back bias, etc., MOS LSI performances are approaching today's bipolar level. A partial list of active companies are: American Microsystems Inc., Bell Telephone Laboratories, Dmost Inc., Hitachi Ltd., Intel, IBM, Monolithic Memories Inc., Mostek Corp., Nippon Electric Co., Signetics, Toshiba Ltd., Westinghouse, to just name a few. Some sample achievements are given in Table V-3.*

It can be seen that some developmental MOS devices have achieved performance comparable or slightly better than injection devices. Their fabrication processes may be more complex but is is still an open question whether simple I^2L/MTL circuit can achieve performance like 2-3 ns or 0.1 - 0.2 pJ without using the more complex versions of the injection logic circuits.

*VMOS gates are formed on the face of an etched V groove. They have very small controllable dimensions around 1 micron. For 5 V random logic, VMOS circuits are 20% faster, use 1/4 chip area, and consume one-sixth the power compared with TTL MSI circuits. Gate delay is 2-3 ns on chip. Off chip drive exceeds 50 MHZ with six TTL loads. For a full adder, VMOS needs 23,200 mil^2 compared with 32,400 mil^2 for I^2L.

TABLE V-3 SOME DEVELOPMENTAL MOS PERFORMANCES

DEVICE	ACCESS TIME (ns)	GATE PROPAGATION DELAY (ns)	POWER CONSUMPTION	DELAY-POWER PRODUCT (pJ)
NMOS				
Intel 1 kbit static RAM (2115, 2125 series)	70-120			
Signetics 1 kbit static RAM	60-80			
Toshiba 4 kbit static RAM	250			
Bell Telephone Laboratories 4 kbit dynamic RAM	50			
16 kbit RAM (Mostek, Intel, TI, etc.)				
IBM 48 kbit ROM				
NMOS/SOS				
Hitachi 21 stage ring oscillator		0.66	0.18	0.12
Toshiba 16 bit microprocessor				
DMOS				
Nippon Electric 4 bit ALU (141 gates/mm^2, 2 volts)		2	1	2
Signetics 4 bit magnitude comparator		4.1	2.5	10
Westinghouse, Univ. Maryland, NASA				
VMOS Stanford University		2-3		

CHAPTER VI

CONCLUSION AND RECOMMENDATION

6.1 INTRODUCTION

Bipolar injection logic came on the scene around 1971 with a big bang. It created a great deal of excitement because it is the first bipolar LSI technology with new innovative circuit concepts tailored to LSI requirements. It promised to combine the advantages of bipolar speed and driving capability with the MOS thrift in power consumption, high packing density and simpler processing steps. Extensive developments were made in the ensuing years and resulted in the marketing of a 4 bit microprocessor in 1975, a 4 kilobit RAM, digital watch circuits and a host of other circuits in 1976.

However, the initial excitement of injection logic has subsided a little recently because the performance of today's injection logic circuits fabricated by the original simple processing is only moderate and has not accomplished the expectation that it combines the advantages of both MOS LSI and bipolar integrated circuits. Furthermore, stimulated by the challenges of the new bipolar injection logic and assisted by some innovative circuit concepts of charge coupled devices, the relatively more mature NMOS technology has been making steady progress. Today, NMOS LSI reports equally impressive if not better performance than today's injection logic circuits but with the benefit of more production experience.

However, bipolar injection logic is still a young technology. Its promise for LSI accomplishments has not been fully realized yet. More R/D efforts, application developments, production and operation experiences are needed before its full potential can be realized and properly compared.

It is interesting to notice that the progress of bipolar injection logic up to this date has been mainly inspired and supported by commercial and consumer interests. Government agencies played relatively minor roles in its growth. Consequently, injection logic devices available today have not met the military specifications in both temperature and radiation hardening requirements. Also, injection logic has not been developed for high performance

special purpose LSI module applications needed in many military systems.

6.2 RECOMMENDATIONS

Looking ahead, the following developments should be considered by government agencies. Because injection logic is capable of achieving a wide range of performances, developments in several directions should be separately considered for different objectives.

6.2.1 Device and Application Developments

Several objectives can be identified.

(1) Low Cost, Moderate Performance LSI: In this category, the major objective is low cost. It is reasonable to anticipate that the fabrication process will be kept simple. As a result, performance will be moderate but yield and packing density will be higher. Furthermore, better reliability can be expected. These characteristics match many nonmilitary applications well. Consequently, developments in this direction probably will be pushed right along independent of government agencies' support except for their abilities to meet military specifications.

(2) High Speed LSI: In this category, the major objective is high speed. Power consumption and cost probably are no objection if they are within reasonable bounds. To achieve this, more complicated processing steps must be used. The following list of processing considerations can all contribute to speed improvements:

- use of Schottky diodes for decoupling or/and clamping
- small geometry
- shallow diffusion
- oxide isolation
- self-aligned n+ contact
- metal covered injector rail
- double metal level
- tailored impurity profile either by ion implantation or by innovative diffusion processes such as out-diffusion from the substrate.

- more efficient current injection such as substrate injection, three or four sided injection, etc.

- lower resistance current injection rail.

At present, the propagation delay of a production type I^2L/MTL gate is in the 10-40 ns range although propagation delays in the few ns range have been reported in computer simulations. With the steady advancement of ECL and CML circuits in accomplishing shorter and shorter delay times, it seems that I^2L/MTL gate will not out-perform these speeds. However, it will offer low power, high packaging density and lower delay-power product performances.

(3) Lower Delay - Power Product LSI: Although I^2L/MTL circuits may not be the best candidates in high speed applications, it is reasonable to expect that even the more complicated I^2L/MTL circuits, which may be capable of accomplishing 1 to 2 ns in propagation delay, will be simpler and consume less power than the Schottky TTL and ECL types of circuits. Therefore, in applications where high speed performance must be traded off with reasonable power consumptions, I^2L/MTL circuits could turn out to be an attractive alternative for both the ECL and the low power Schottky TTL circuits.

It should be recognized that there are now more than seven modified versions of the original I^2L/MTL circuits. Except the low cost LSI applications which probably will keep the original circuits, other LSI applications most likely will use the modified I^2L/MTL circuits. It should also be recognized that these modified circuits are still in their infancies.

6.2.2 LSI Module Development

At present, a wide variety of I^2L/MTL circuits are being developed for commercial applications. They include microprocessor, digital watch, memory, interface circuit, combined linear and digital applications, and many others as listed in Table I-4 and Chapters IV and V. They probably will be adequately developed with or without government support. However, for military applications, there are several special purpose processing operations which are not widely used elsewhere. Some important examples of this type of processor are those listed in the following:

- Filters
  - Nonrecursive filters:
    convolvers, correlators, matched filters, Wiener filters, etc.
  - Recursive filters:
    which include the Kalman filters in a general sense.
- Spectral Analysis
  - Fourier type of transforms:
    discrete Fourier transform, discrete cosine transform, etc.
  - Other types of transforms:
    such as Hilbert transform, Hadamard transform, Kahunen-Loeve transform, et.
- Frequency Synthesizers
- etc.

It is reasonable to speculate that they will not be adequately developed without government agency support and leadership.

6.2.3 Production Yield and Reliability Data

Bipolar injection logic is still in its infancy. It will not be surprising that the eventual production circuit still has not been developed today. It is important to first recognize the potentially successful circuits and then build up their production yield and reliability information.

6.2.4 Theory, Modeling and CAD

So far, all reported theoretical analysis and circuit modeling were developed for the original I^2L/MTL circuit. There is no computer-aided-design (CAD) work reported publicly. Since it is anticipated that future bipolar LSI injection logic circuits probably will take one of the modified forms, the existing theories, circuit modeling and the yet-undeveloped CAD work should be extended for the modified circuits.

6.2.5 Militarized Devices and Equipments

It seems that most of the I^2L/MTL devices available in the market today have not met the military specification yet. There is no basic reason why I^2L/MTL cannot be made to meet these requirements, especially with the versatile characteristics of increasing the injection current to increase the circuit performance. However, optimized circuit design and processing steps have not

yet been reported which consider military specifications in temperature variation and in radiation hardening.

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