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REPORT MDC E1667

INTEGRATED CIRCUIT ELECTROMAGNETIC SUSCEPTIBILITY INVESTIGATION — PHASE III

TECHNICAL REPORT NO. 2

APPROVED FOR PUBLIC RELEASE: DISTRIBUTION UNLIMITED

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INTEGRATED CIRCUIT ELECTROMAGNETIC SUSCEPTIBILITY INVESTIGATION PHASE III

3 JUNE 1977 **REPORT MDC E1667**

AF 030 D19 TR2

TECHNICAL REPORT NO. 2

APPROVED FOR PUBLIC RELEASE: DISTRIBUTION UNLIMITED

SUBMITTED TO THE CONTRACTING OFFICER, U.S. NAVAL SURFACE WEAPONS CENTER – DAHLGREN LABORATORY, DAHLGREN, VIRGINIA, 22448 UNDER CONTRACT NO. N60921-76-C-A030

~~AF 030~~

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(See 1473)

PREFACE

The work reported in this document was performed under Contract No. N60921-76-C-A030 for the U. S. Naval Surface Weapons Center, Dahlgren Laboratory Dahlgren, Virginia 22448. The McDonnell Douglas Astronautics Company personnel involved were:

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1. INTRODUCTION AND SUMMARY

The work described herein was performed by McDonnell Douglas Astronautics Company - East (MDAC-EAST) under contract to the U. S. Naval Surface Weapons Center/Dahlgren Laboratory (NSWC/DL). It is part of an ongoing program seeking to understand high power microwave effects in a cost effective manner. This Integrated Circuit Electromagnetic Susceptibility (ICES) contract is concerned with microwave effects in semiconductor integrated circuits (ICs). This report covers the work performed in the second of three increments which together form the third and last phase of this program. This effort is directed toward characterizing IC susceptibilities to microwave energy and identifying possible means of reducing these susceptibilities.

The primary output of the ICES effort is an ICES Susceptibility Handbook which provides IC susceptibility information to system designers. This information consists of susceptibility models and data. The handbook also contains a complete approach to the Electromagnetic Vulnerability (EMV) problem and a detailed example of using the IC information to determine the system shielding requirements. During the second increment, Draft 1 of the ICES Handbook[1], which was issued after increment 1, was reviewed by potential users. Part of this review occurred at a seminar held in October 1976. In response to the comments received, the ICES Handbook has been revised and Draft 2 is being issued in parallel with this report. This revision includes new models and updated test data from the work performed during the second increment. The review cycle for Draft 2 of the ICES Handbook[2] will include an expanded mailing list, and all those who have shown interest in the IC susceptibility problem will receive a copy. Approximately 500 names are included in the mailing list. Another seminar is planned for the fall of 1977 for further review and comment of Draft 2.

During the second increment the bipolar junction transistor RF effects model was refined. This model is an Ebers-Moll model modified to include the RF effects observed during a large amount of RF testing of diodes and transistors. This model has been used with SPICE (Simulation Program with Integrated Circuit Emphasis) as an example of how RF effects in ICs can be modeled using a standard circuit analysis program.

The study of damage susceptibility was completed in the second increment. A large testing program was performed to study each damage mechanism - junction failure, metallization failure, and bond wire failure. Also a general worst case model was generated for each mechanism based on heat flow from the failure site.

The feasibility of various susceptibility reduction techniques was reviewed during this increment. The value of device screening and circuit design techniques require further study as the modeling effort continues. However the use of lossy material, such as ferrite, as a susceptibility reduction technique, appears to be impractical at this time.

2. IC SUSCEPTIBILITY HANDBOOK REVISION

During increment one, Draft 1 of the ICES Handbook was designed. It was issued to potential users for their comments, criticisms, and suggestions as to content and format. During increment two, the users responded in a generally favorable manner to Draft 1 with specific comments and suggestions. Their responses have been incorporated into Draft 2 wherever possible. Also the modeling and test data have been updated to include the work performed during the second increment.

2.1 System Considerations - From initial comments it was obvious that a detailed example for using the IC Susceptibility Handbook was needed. Therefore, the following example showing how to determine the system shielding requirements with a given EM environment was created and presented at Seminar I.

Electromagnetic environment levels (in terms of power density, P_d) are determined according to the stockpile to end of service life cycle of the system of interest, and a table or graph of required test levels is usually included in contractual documents. A possible environment level for this example is shown in figure 1.

An unshielded wire or cable will pick up various amounts of power from such environments according to such variables as frequency, aspect angle, terminating impedance, etc. One method for determining the maximum amount an unshielded wire will pick up is given by the formula:

$$P = 0.13 \lambda^2 P_d$$

where λ is the wavelength of interest. From this formula, the maximum amount of power expected on system wiring in the given environment can be calculated. This result is also illustrated in figure 1.

Figures 2 and 3 repeat the maximum power levels expected but also add component information which is available in the handbook. In particular, figure 2 shows the

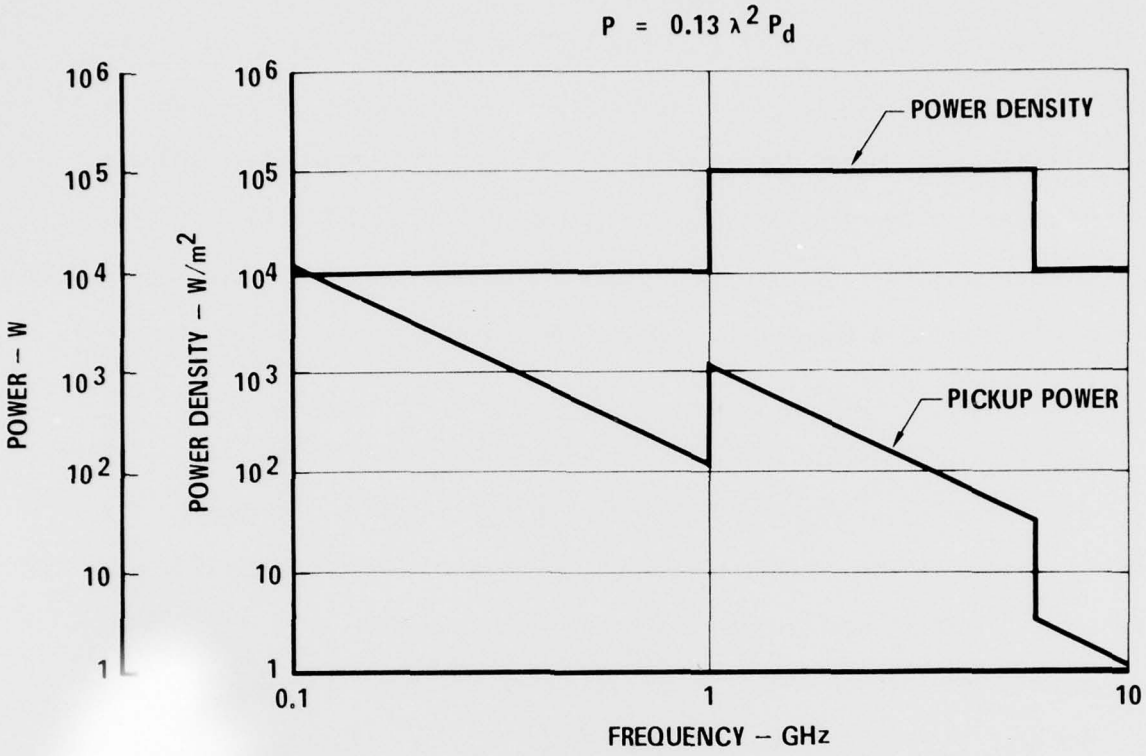


Figure 1 Sample Calculation of Pickup Power From Given Power Density

worst case burnout levels ever observed for IC burnout. It is clear that, in the absence of any shielding, burnout is quite possible across a large frequency range, and some sort of protection in the form of shielding (either enclosure or cable, or both) or filtering is required to guarantee that component burnout will not occur. The amount of protection required is indicated by the separation of the two curves on this logarithmic plot. Figure 3 shows similar results for interference effects.

The degree of overall system protection required for this example is summarized in figure 4. Many options are available to meet such requirements including: splitting the shielding requirements between enclosures and cables, filtering, isolation of particularly sensitive circuits, etc.

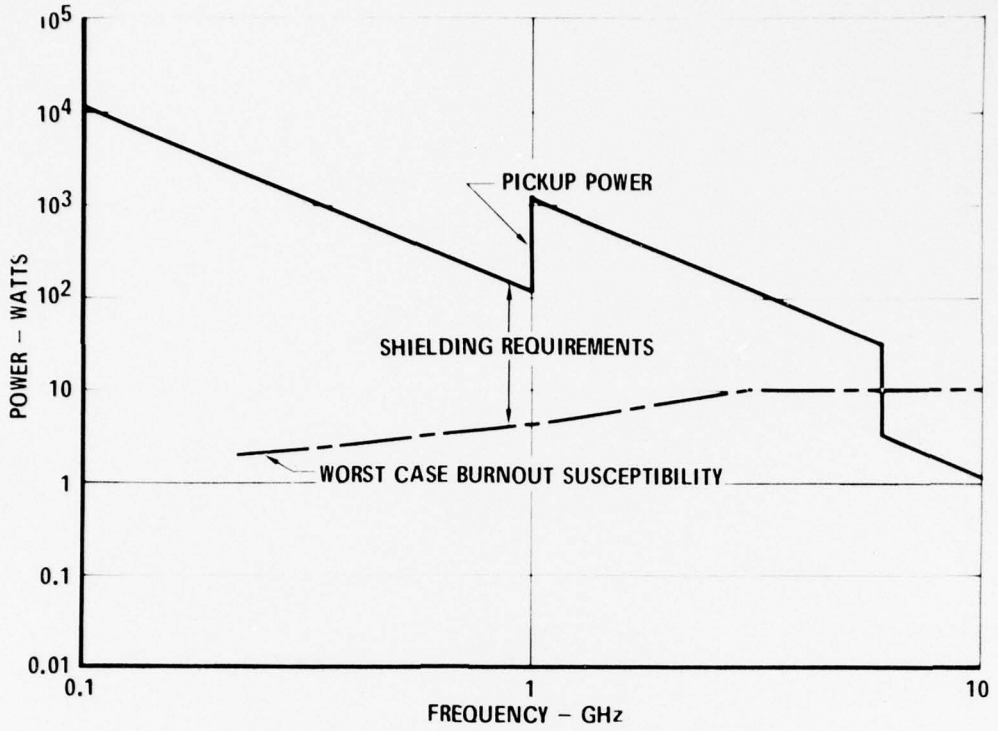


Figure 2 Sample Determination of Shielding Required for Burnout Protection

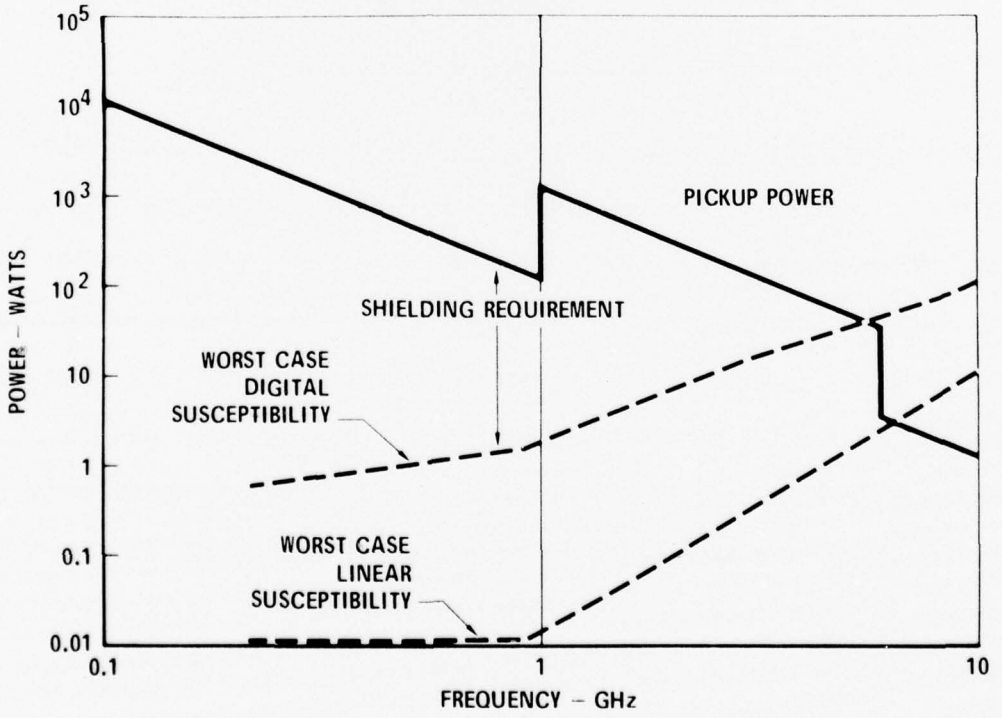


Figure 3 Sample Determination of Shielding Required for Interference Protection

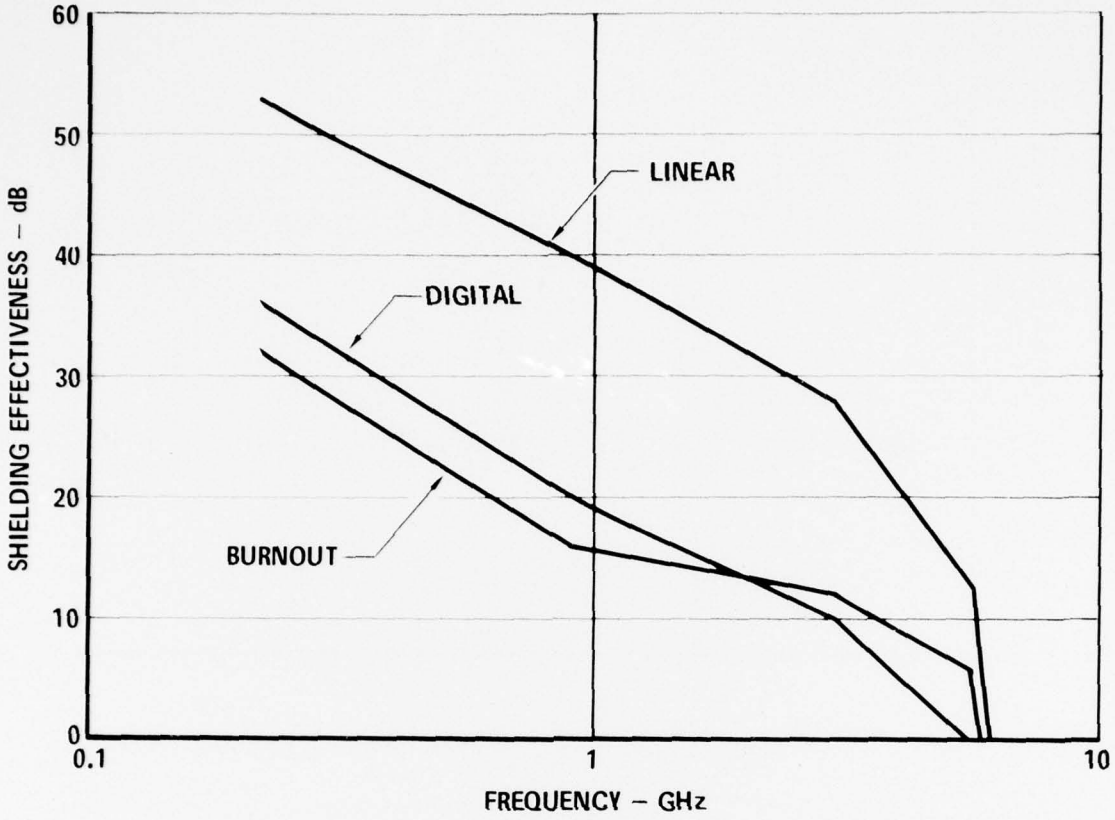


Figure 4 Sample Requirements for System Shielding

2.2 Component Susceptibility Information Requirements - In the susceptibility information section of the revised handbook there have been several major changes while some things remained the same. In Draft I, use of a worst case approach to susceptibility was proposed. Potential users who were questioned concerning this approach approved it and so it will remain the cornerstone of the susceptibility information, both for the modeling and test data. Some of the items that have undergone changes in Draft 2 are: (1) the individual graphs showing the data spread by frequency have been removed; (2) all graphs and models have been changed from absorbed RF power to estimates of minimum RF power; (3) the susceptibility criteria for digital devices have been changed and (4) the composite graphs for digital devices with high and low output states have been combined into one graph.

The individual graphs which showed the data spread for each frequency have been removed in answer to several comments that they were confusing and unnecessary. Originally these graphs were provided to give the designers some idea of the best case susceptibility for the ICs but they were interested in the worst case susceptibility. Since the worst case susceptibility levels were shown on the composite graphs, the composite graphs were retained and the individual graphs deleted.

For the worst case approach adopted in the handbook, the quantity of interest is the minimum amount of power (defined as power available from the source) which will produce the unacceptable component response. The estimates of minimum power contained in the handbook are derived from measurements on statistical samples of ICs and on theoretical considerations based on physical models. The data measured with the measurement scheme described in Chapter 4 of the handbook must have the dependence on the measurement technique removed because it is recognized that the IC susceptibility level may depend upon the driving impedance of the microwave source (whether a laboratory source or a cable or wire exposed to a microwave field). One useful approach is to determine the amount of power dissipated within the package since it can be postulated that reflection losses and external dissipation losses could be minimized under suitable tuning conditions. Likewise, the failure models are derived in terms of power dissipated in the failure site. The use of absorbed power as an estimate of minimum power is conservative since it is probably not possible to match the driving source to a nonlinear load such as a semiconductor junction; and it is likely that losses in diverse parts of the IC chip are inevitable. To minimize the very real danger of producing over-cautious estimates, the degree of conservatism in the handbook predictions has been estimated and these estimates are made clear to the reader and user of the handbook.

The format of the composite graphs also brought comment from designers. It was suggested that whichever output state is susceptible for digital devices is irre-

levant, and only the worst case susceptibility is important. Therefore the composite graph for TTL devices and the composite graph for CMOS digital devices include both the high and low output states. Draft 1 had separate composite graphs for each output state, but Draft 2 has one graph which includes both states. The susceptibility criteria for these two-state composites have also been changed to reflect both states and to make the criteria more useful. The Draft 2 criteria are tied to specification limits wherever possible. For example, in the case of TTL devices the criteria were 0.4, 0.6 and 0.8 volt for the low output state and 2.4, 2.2 and 2.0 volt for the high output state in Draft 1. In Draft 2 the combined criteria values are 0.4 or 2.4 volts (the guaranteed specification limit for low or high state), 0.8 or 2.0 volts (the edge of the 0.4 volt noise margin), and 2.0 volts or 0.8 volt (which is a guaranteed switch from the low or high state), respectively. Figures 5 through 7 show the revised composite graphs as they appear in Draft 2.

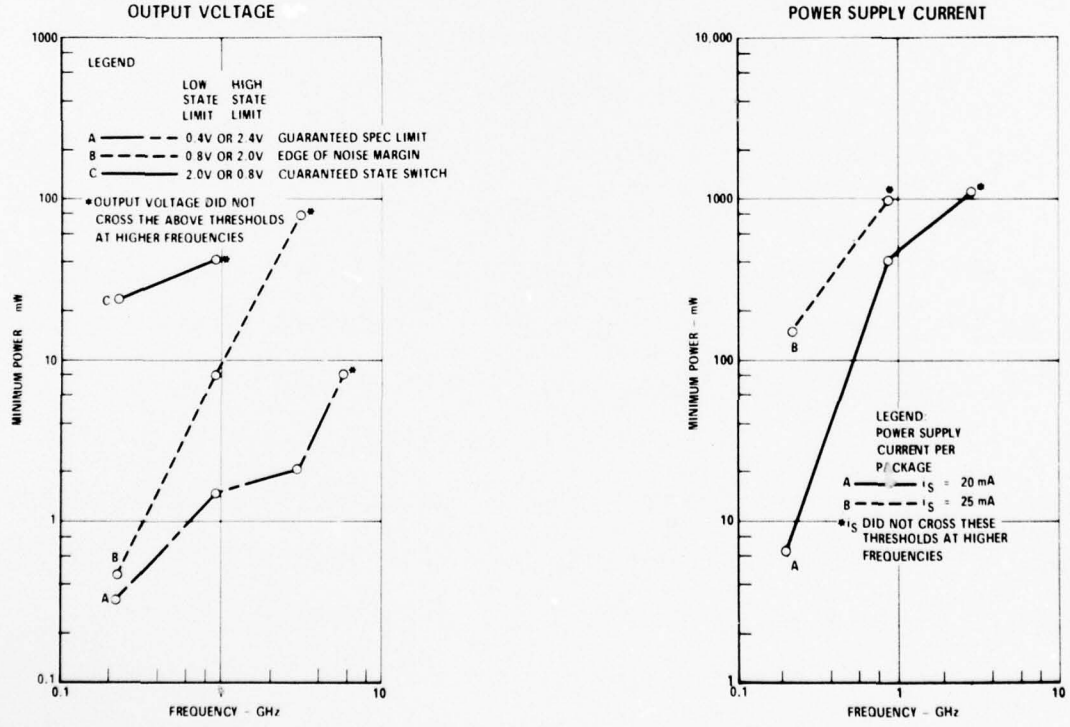


Figure 5 Worst Case Susceptibility Levels For TTL Devices

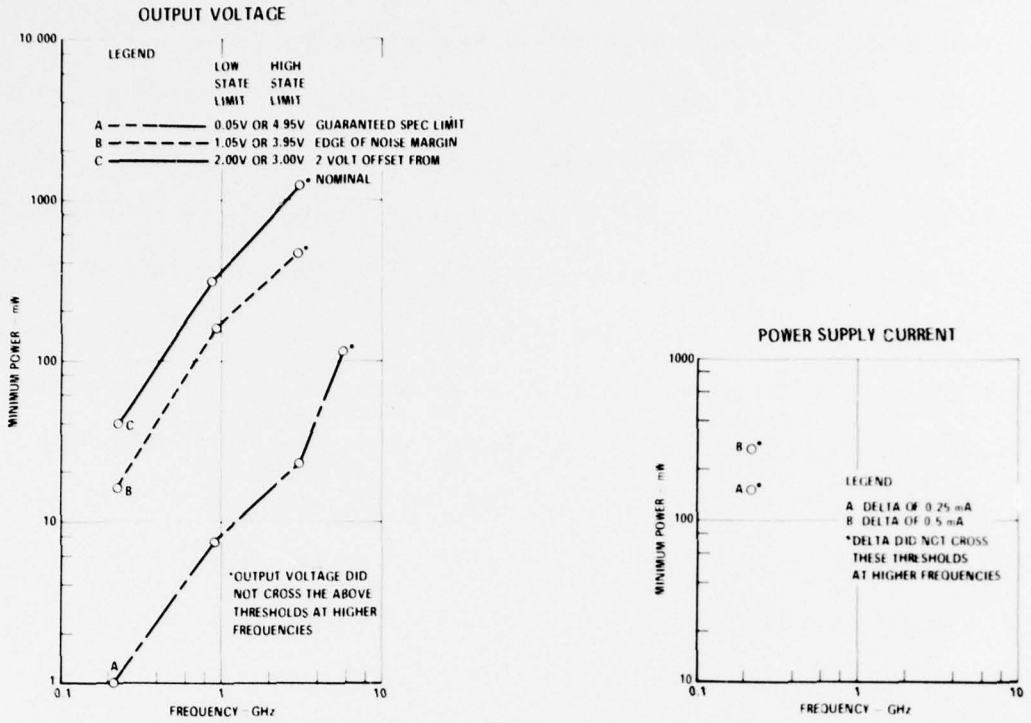


Figure 6 Worst Case Susceptibility Levels For CMOS Digital Devices

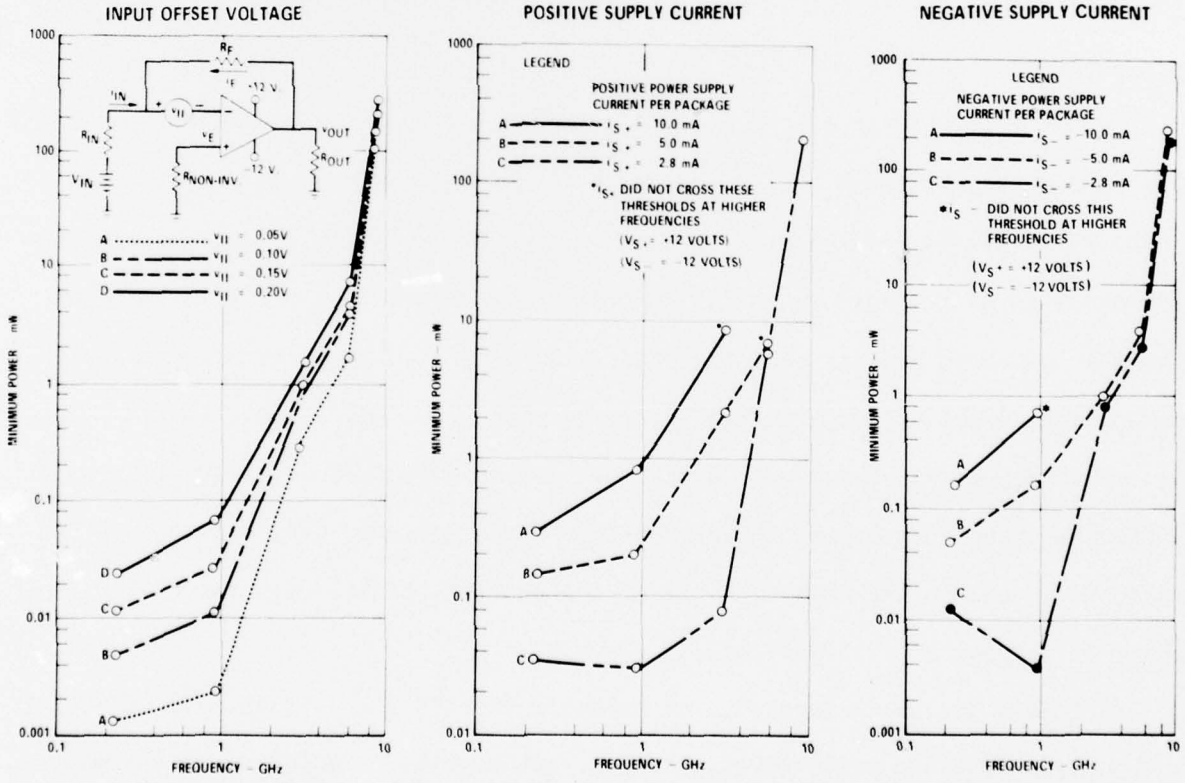


Figure 7 Worst Case Susceptibility Levels For Operational Amplifiers

In Draft 2 several interference models have been presented, including a bipolar junction transistor model with RF effects, which can be used with a circuit analysis program to model ICs, and an op amp input model. These models are intended to serve as analysis tools for the designers who want to go more deeply into the susceptibility problem than is possible using the worst case data presented.

The bipolar transistor model with RF effects is an Ebers-Moll model modified to include the effects of the RF. This model is described in detail in Chapter 3. The op amp input model uses an offset generator in the inverting input lead to simulate the RF effects on the input circuitry. The translation from RF power to input voltage is empirical in Draft 2 and is presented in detail in Chapter 3.

Damage models are also presented in Draft 2 which were not in Draft 1. There is a model for each damage mechanism - junction failure, metallization failure, and bond wire failure. Since these mechanisms are thermal, each model is derived from the heat flow equation with differing boundary conditions. These models are presented in Chapter 4.

Draft 2 of the handbook contains a statement recommending caution when making the complex measurements required to determine integrated circuit susceptibilities. Three particularly error-prone areas are noted: uncertainty in calibrations due to the presence of harmonic signals, the problem of determining small differences between two large numbers when the uncertainties in the large numbers are on the same order as the difference, and instrumentation problems associated with changing RF impedances within the device under test (especially during failure testing). Different means of treating these problems in the measured data must be applied in order to obtain the best estimate of the quantity of interest (usually minimum power to produce a given effect).

Problems due to the presence of harmonic signals are particularly difficult to handle. Coupling coefficients, losses, and crystal detector calibrations are

all frequency dependent. The magnitude and relative distribution among the various harmonics depends upon the device under test and the power level of the fundamental signal injected. It would seem possible to calibrate all couplers and losses at many frequencies and to measure the harmonic content of the reflected and transmitted signals, but such an approach appears to be prohibitively expensive. The most direct solution appears to be use of incident power actually measured as the best indicator of minimum power when harmonic problems are severe.

The task of determining the amount of power absorbed in the device under test is basically a matter of subtracting power reflected, transmitted, and absorbed in known losses in the test fixture from the incident power. Occasionally, a device is encountered which produces such mismatches in the system as to make the sum of the reflected, transmitted, and absorbed powers exceed the measured incident power. In such cases, the uncertainties in the measurements and calibrations (probably aided by the harmonic problem discussed above) overwhelm the expected result and a negative absorbed power is calculated. Two approaches are used to extract useful results from such data. The first is to estimate the amount of power absorbed in the device under test plus the test fixture. This method accounts for the power reflected and transmitted which is obviously not absorbed in the device. If the harmonic problem is still significant, the second option is to use measured incident power as the best estimate of minimum power.

During single pulse testing (as in the failure testing), it is necessary to sample and hold the values of the reflected and transmitted signals to permit acquiring the data. During failure testing especially, the impedance of the device under test can change (at failure) enough to cause the reflected and/or transmitted values to change during the pulse. Ideally, the test setup could be instrumented to provide either a time-history of each signal (as would be obtained from an oscillogram for example), or an adjustable-gate sample and hold could be

employed. Both of these schemes have been implemented in other programs, but the number of channels required (17) in the IC program makes such arrangements prohibitive.

For the pulse testing performed during the failure testing segment of the program, simple peak detectors were employed on the transient signals so that when impedance changes occurred at failure that caused larger signals than before failure, errors were introduced. This problem can be satisfactorily circumvented by performing additional data processing on the total data sample. The Bruceton test technique used in the failure testing typically produces failure in only 50% of the test sample. It is in this part of that data that the absorbed power is uncertain. By using the mean absorbed power in the no-fail data, the mean absorbed power in the failure data can be estimated.

The preliminary MOSFET model presented in Chapter 3 is not ready for the handbook at this time. More effort is required to study the RF effects on the MOSFETs, both testing and analysis, before a final model is ready to be incorporated into the handbook.

2.3 Outline Revisions - There is one major outline revision in Draft 2 of the ICES Handbook which occurs in Chapter 2. The breakdown of Chapter 2 was by device class in Draft 1, (digital devices and linear devices). Each class of devices had its own interference and damage section. During the extensive testing performed in the second increment, all types of damage data were grouped together, and the next logical step was to revise the outline according to the type of susceptibility (interference and damage). This revision was accomplished with the class of device as the subheading for the interference section and the damage section covering all ICs.

2.4 Further Review Planning - In order to obtain the maximum number of reviewers for Draft 2, the external mailing list has been expanded. All those who have

expressed an interest in the IC susceptibility problem will receive a copy of Draft 2 of the handbook for review and comment. In addition another seminar is planned for the fall of 1977 to get comments of users firsthand along with any suggestions for the third and final draft of the handbook which will be issued in 1978.

3. INTERFERENCE EFFECTS

The goals of the interference effects investigation are twofold: 1) to catalog the interference effects in integrated circuits to provide useful information to system designers, and 2) to gain a more complete understanding of the origin of these interference effects. Regarding the first goal, the susceptibility of the TTL family of digital devices and of bipolar operational amplifiers has been studied in detail in previous reports[3,4,5]. This report adds information on line driver/receiver pairs and CMOS digital integrated circuits. In regard to the second goal, the understanding of observed interference effects has increased to the point where it is now possible to form models for the interference effects in integrated circuits. The interference mechanism, which has been documented previously[3], is the rectification of RF signals in the pn junctions of the integrated circuits. Starting with the simplest semiconductor devices, models are shown for the rectification effects in diodes and transistors, then the models are extended to 4-layer integrated circuit construction devices and MOSFET devices. Using a computer program intended for circuit analysis, the transistor model is applied to model the case of RF entering the output of a TTL device, with the output in a low state. Op amps are modeled for the case of RF entering the input by using a small-signal type of approach.

3.1 Large Signal Rectification in PN Junctions - Previous investigation of the RF interference phenomenon in integrated circuits has identified rectification of the microwave signal in pn junctions to be the primary mechanism[3]. However, small signal detection theory does not adequately account for many of the effects observed since the microwave signal may be of large amplitude. A large-signal rectification theory has been developed, based on a time-domain analysis of junction waveforms.

3.1.1 Measured Rectification in Diodes - Figure 8 shows a plot of the measured I-V characteristics of a 1N914 diode and the base-collector diode of a 2N2369A transistor (emitter open) for varying levels of RF power at 220 MHz. The effect of the RF power is to cause the portion of the diode curve below the knee to rise because of increased current flow due to rectification of the RF signal.

The diode characteristic curves were measured using the test setup shown schematically in figure 9. The diode was placed in a microwave test fixture during the test. Microwave energy was conducted into the diode through bias units, which allow the diode to be biased as desired.

3.1.2 Time-Domain Calculation of RF Effects in Diodes - A time-domain calculation was performed to study large signal rectification in diodes. A suitable model was chosen for the diode, and the external circuit of the measuring system was modeled in a simplified manner to enable a computer calculation of the expected rectification in the diode.

The diode model and modified external circuit are shown in figure 10. The diode model consists of the series resistor R_S, junction leakage resistance R_P, a nonlinear diode junction D, and capacitance C. The relation between the current through D, i_j, and the junction voltage v_j, is

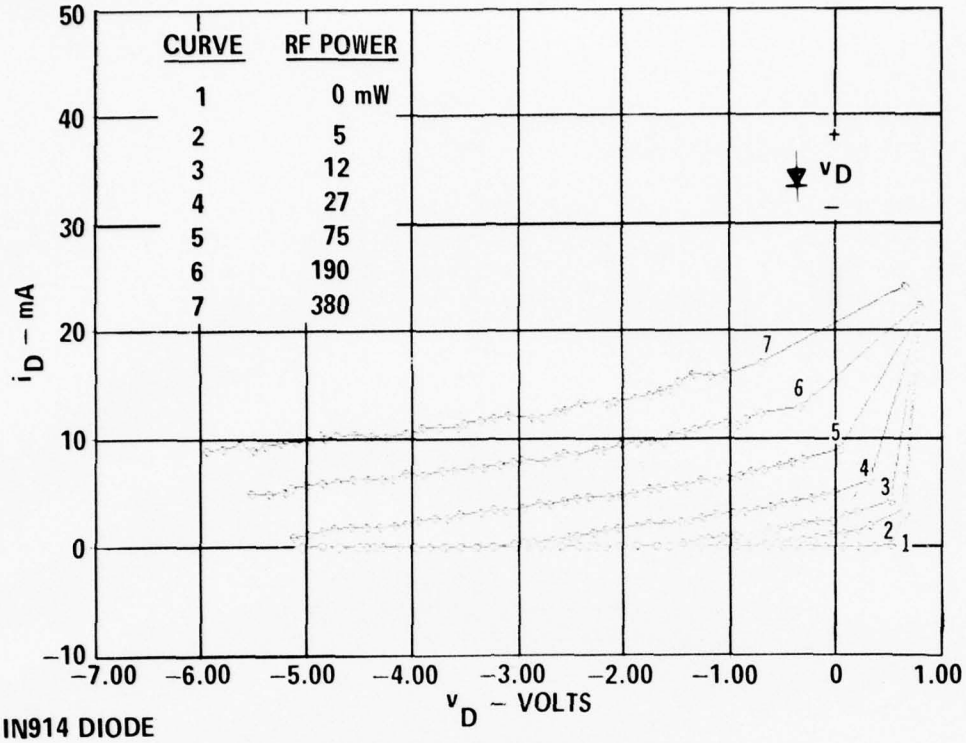
$$i_j = I_o(\exp(Qv_j) - 1)$$

where I_o is the junction reverse saturation current, and Q is a constant with units of volts^{-1}.

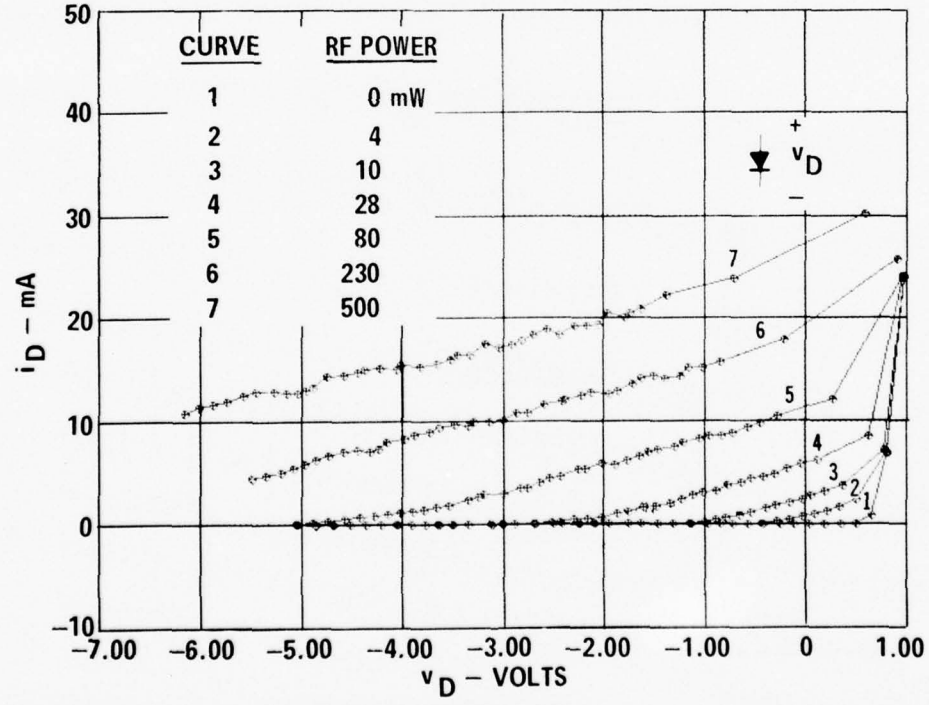
The capacitance of a diode junction varies with the junction bias. When reverse biased, this capacitance, primarily transition capacitance, is given by[6]

$$C = \frac{C_j}{(\phi - v_J)^n}$$

where C_j is a constant capacitance,



a) IN914 DIODE



b) 2N2369A BASE-COLLECTOR DIODE (EMITTER OPEN)

Figure 8 Measured Diode Characteristic Curves for Varying Levels of RF Signal at 220 MHz

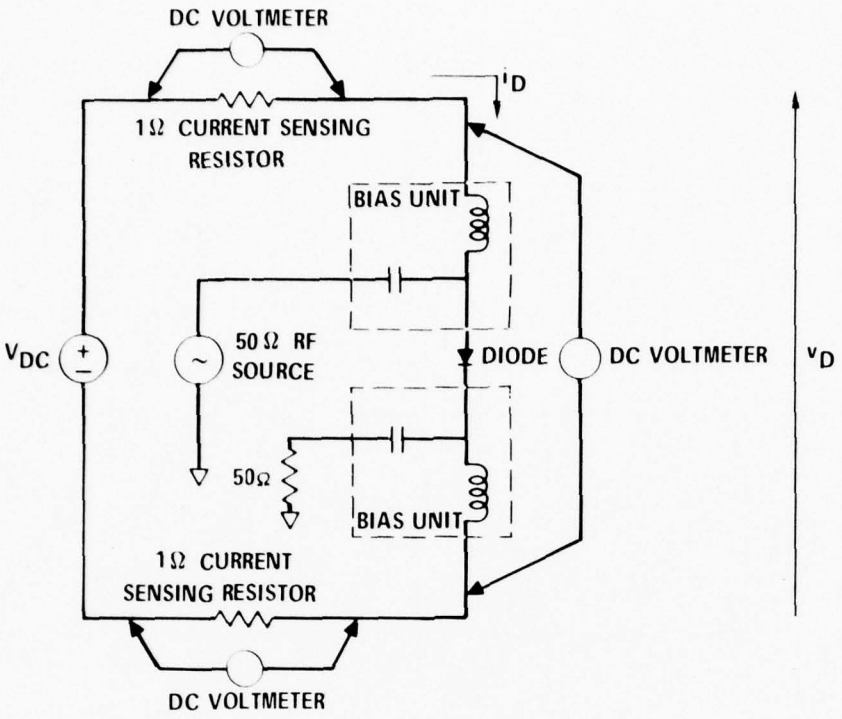


Figure 9 Test Setup for Measurement of Diode Characteristics Curves Under RF Influence

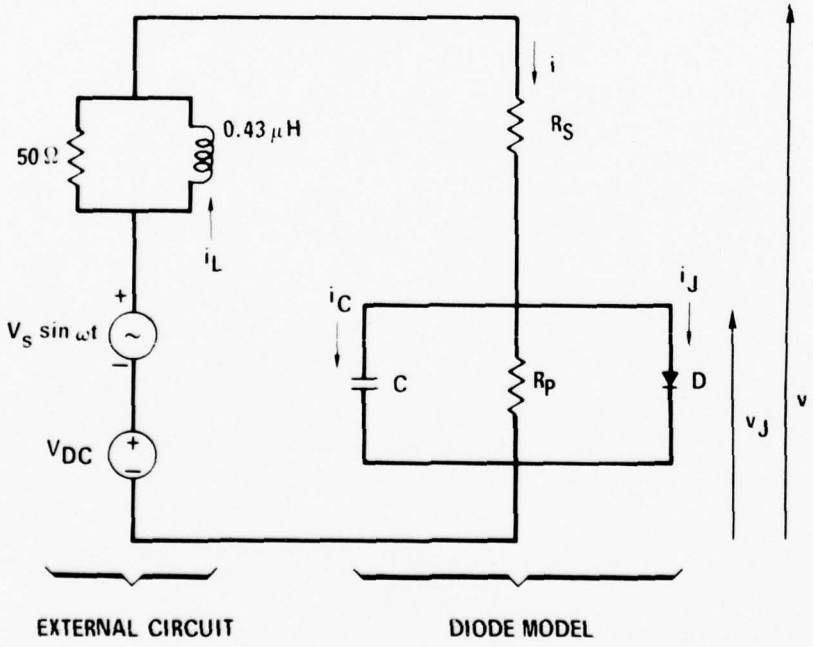


Figure 10 Diode Model and Modified External Circuit for Time-Domain Rectification Calculations at 220 MHz

ϕ is the junction contact potential (which is between 0.6 and 1 volt for most silicon devices, and

n is the junction grading constant (generally between 1/2 and 1/3).

When the diode is conducting, the capacitance (now mainly diffusion capacitance) is approximately proportional to the diode current and is given by[6]

$$C = QT_d I_o \exp(Qv_J)$$

where T_d is a constant with units of seconds.

When the diode is forward biased, the diffusion capacitance can become quite large. On the other hand, for the reverse biased diode, the transition capacitance is rather small for most devices, and does not vary greatly over the range of reverse bias voltages. Therefore, for the time domain model, the capacitance was simplified to

$$C = C_o + QT_d I_o \exp(Q v_J)$$

where C_o is a constant capacitance that approximates the diode transition capacitance.

The relationship between the charge, q, stored in a capacitor and voltage across it, v_J, is

$$q = Cv_J.$$

After differentiation, the capacitor current, i_C, becomes

$$i_C = \frac{dC}{dv_J} \frac{dv_J}{dt} v_J + C \frac{dv_J}{dt}$$

so,

$$i_C = \left(v_J \frac{dC}{dv_J} + C\right) \frac{dv_J}{dt}.$$

The circuit external to the diode model consists of an ideal dc voltage source, an ideal sinusoidal RF voltage source, and a resistor and inductor in parallel. The RF source has a voltage waveform given by

$$v_{source} = V_s \sin\omega t$$

where V_s is the voltage amplitude, ω is the angular frequency of the waveform, and $V_s = \sqrt{8(50\Omega)P}$, where P is the RF power.

Due to the widely different time constants of the two legs of the bias units used in measuring rectification, it is difficult to perform a time domain calculation without requiring large amounts of computer time. For this reason, the bias units were not modeled, but a circuit that performs a similar function as the bias units was implemented instead. Basically, the bias units separate the diode terminals into microwave and low frequency lines. The microwave lines have a microwave impedance of 50Ω, while the dc lines have an impedance of practically zero at low frequency. It was desired to retain this characteristic in the time-domain modeling. The parallel resistor and inductor combination shown in figure 10 does this. At the frequency of the RF source, the inductor has a high impedance, while at dc, the inductor acts as a short. The effect of this circuit is to have a resistance of 50Ω for the RF source, and a resistance of 0 at dc. The value of the inductor, 0.43 μH, was chosen to yield high impedance at 220 MHz, yet give the circuit a settling time short enough to permit reasonably fast computer calculations.

The time-domain solution involves solving two simultaneous differential equations, since there are two charge-storage elements in the circuit. The Runge-Kutta method was used to find the time domain solution from two initial conditions. The values of interest are i_D, defined as the average current through the diode, and v_D, the average voltage across the diode. A trapezoidal integration was performed on these values over one period, after which the average i_D and v_D were computed. The value of v_D was compared with v_{DC}, and if the two were not within a given tolerance, generally 0.001 volt, the process was repeated until it could be assumed that the initial transient had died out.

A time domain calculation was performed on a 1N914 diode and the B-C diode of a 2N2369A transistor using the parameters shown in table 1 for the diodes. The

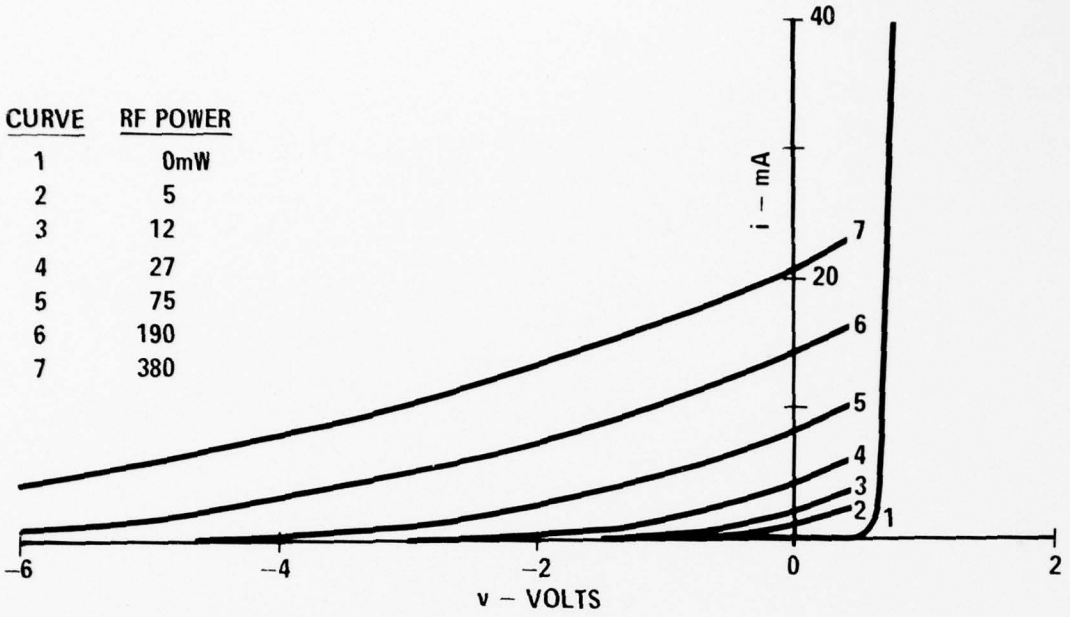
values of R_S, R_P, I_o and Q were obtained from reference 3. The value of C_o corresponds to values listed in semiconductor data books. The value of T_d was chosen for the 1N914 diode to yield a value for i_D of 20.8 mA when v_D = 0 and P = 380 mW, to agree with the observed case. The value of T_d for the 2N2369A base-collector diode was obtained similiarly.

Table 1 Model Parameters for Time-Domain Rectification Calculations

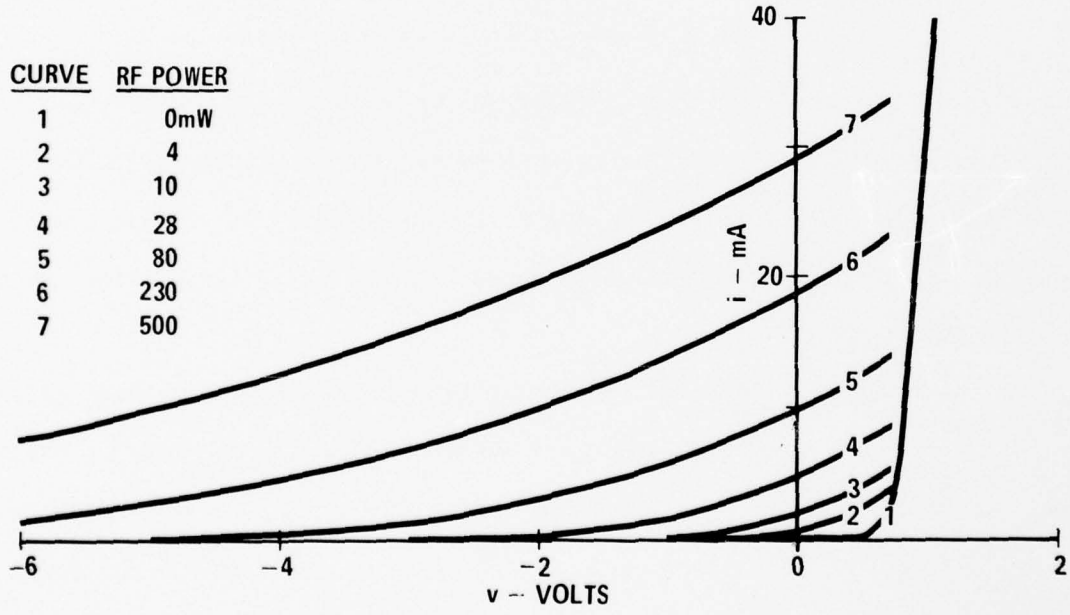
PARAMETER	1N914 DIODE	2N2369A BASE-COLLECTOR DIODE
R_S	2.6 Ω	4.6 Ω
R_P	347K Ω	360K Ω
I_o	7.4 nA	60 nA
Q	19.9 VOLTS^{-1}	15 VOLTS^{-1}
C_o	2 pF	4 pF
T_d	0.43 nSEC	0.37 nSEC

Figure 11 shows the diode I-V characteristics predicted by the time domain model for the 1N914 diode and the 2N2369A base-collector diode at 220 MHz. The curves have very nearly the same shape as the measured curve of figure 8, indicating that a time-domain calculation works well in analyzing large signal rectification of diode junctions.

As the frequency increases into the gigahertz region, it has been observed that interference effects in integrated circuits generally decrease[3]. The time-domain model can be used to analyze the effect of frequency on rectification. Figure 12 shows the calculated diode characteristic curves at 910 MHz and 3 GHz for the 2N2369A base-collector diode (emitter open). The plots indicate that the amount of rectified current decreases as the frequency increases. They agree well with measured rectification of the 2N2369A base-collector diode at 910 MHz and 3 GHz (not shown).

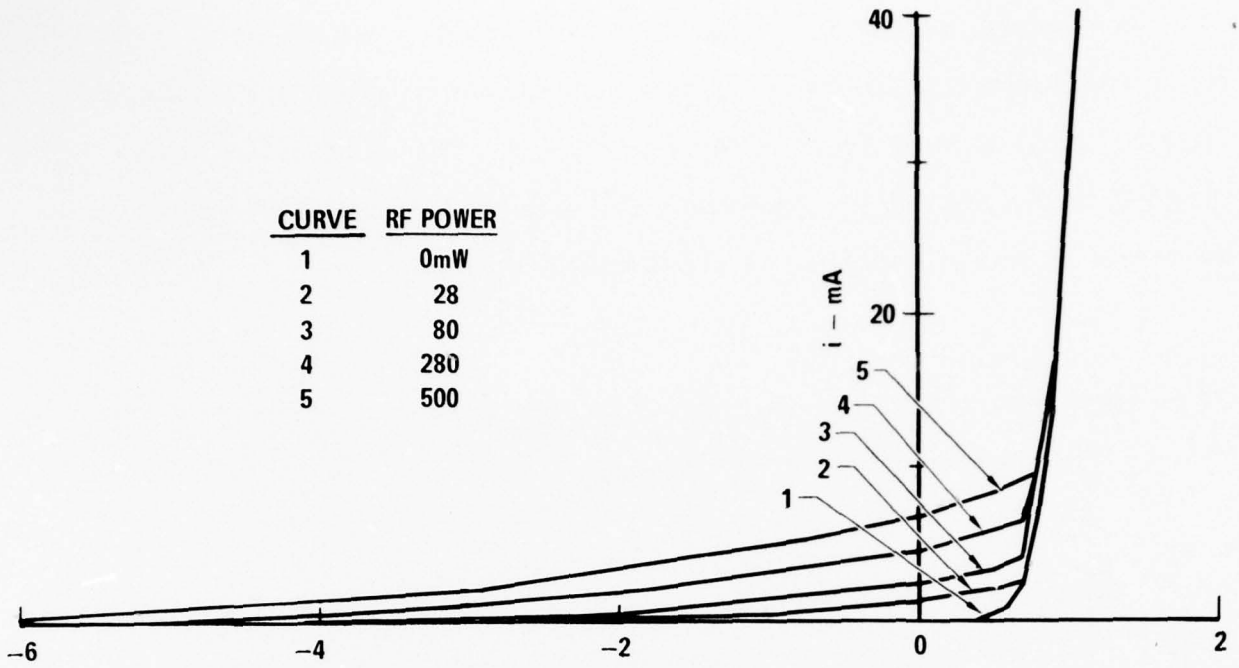


a) IN914 DIODE

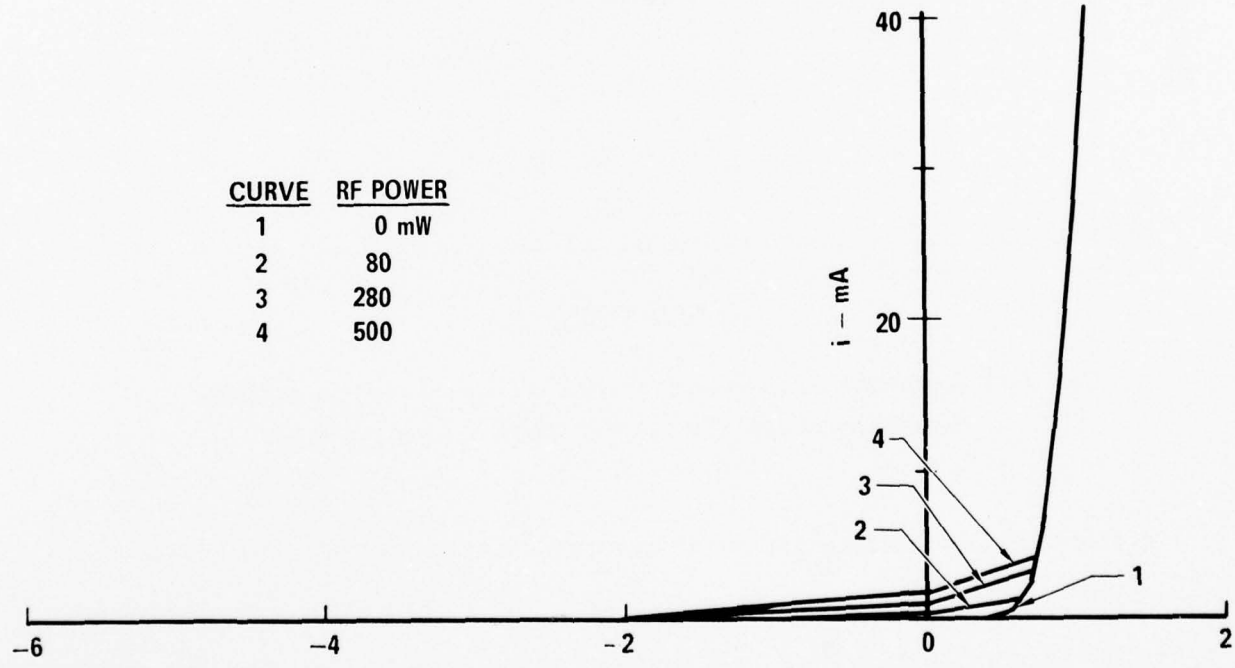


b) 2N2369A BASE-COLLECTOR DIODE (EMITTER OPEN)

Figure 11 Diode Characteristic Curves From Time-Domain Calculations at 220 MHz



a) 910 MHz



b) 3.0 GHz

Figure 12 2N2369A Base-Collector Diode Characteristic Curves From Time-Domain Calculations

The decrease in rectified current with frequency is shown graphically in figure 13. Plotted is the amount of rectified current produced by a 2N2369A base-collector diode at an RF power of 80 mW and v_D = 0. The rectification can be computed for the new driving impedance. This has not been done, but some study of the effect of driving impedance is planned for the future.

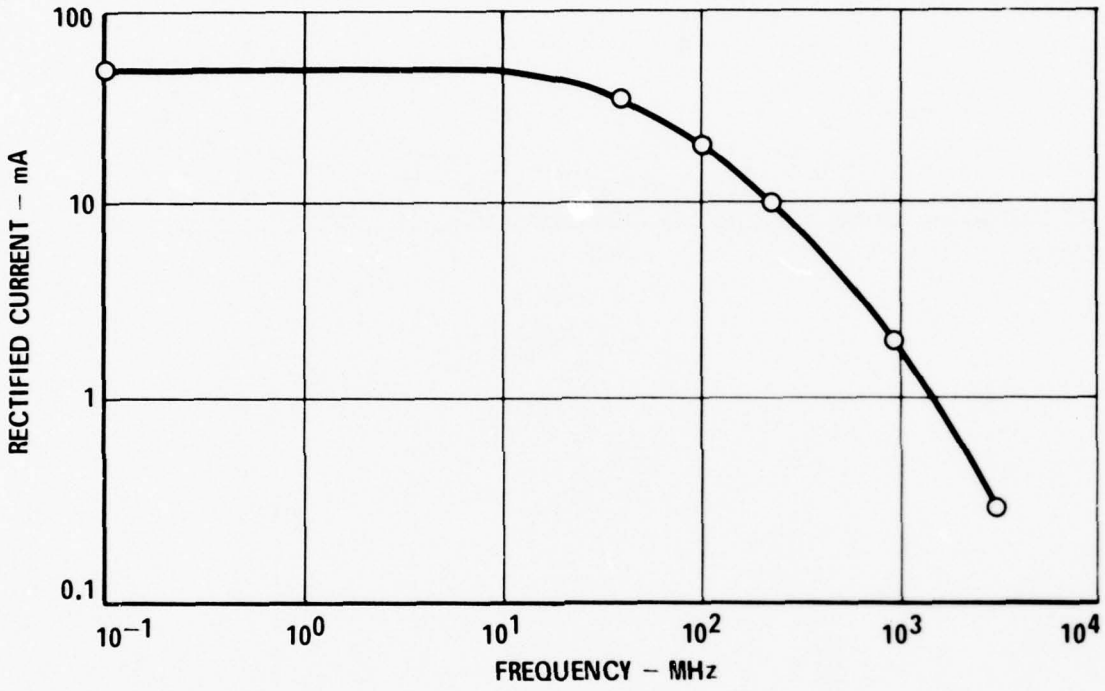


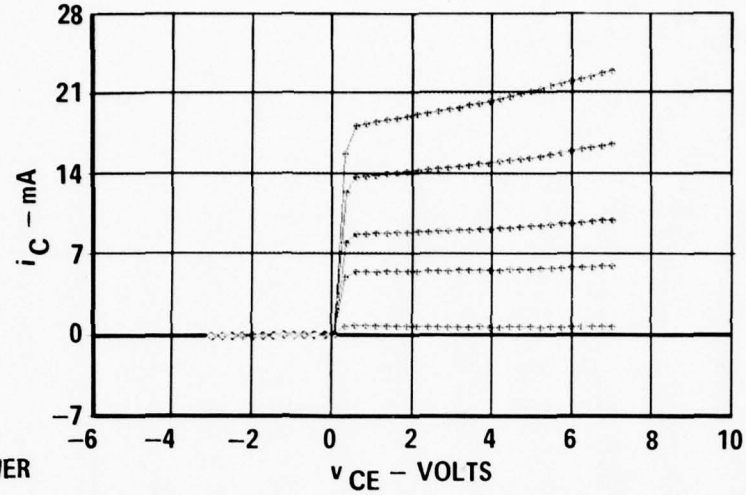
Figure 13 Rectification Current as a Function of Frequency for the 2N2369A Base-Collector Diode (RF Power = 80 mW and V_{DC} = O.V.)

The time-domain rectification model can also be used to study the effects of different RF driving impedances. By replacing the 50 ohm resistor with the observed or predicted RF driving impedance, and performing the calculations, the amount of rectification can be computed for the new driving impedance. This has not been done but some study of the effect of driving impedance is planned for the future.

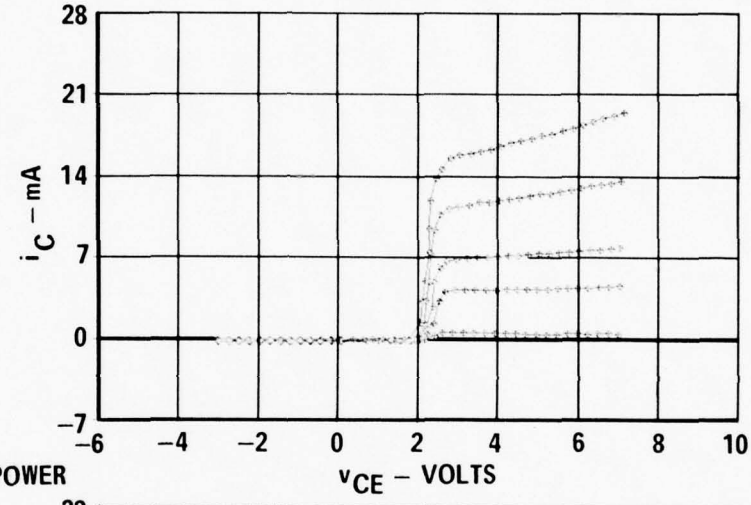
3.2 RF Effects in Transistors - Transistors respond to RF signals through rectification which occurs in the base-emitter and base-collector junctions. The effect of the rectification is to make the transistor characteristic curves appear to change. It is probable that a time-domain type of calculation would account for the effects, but this approach would be unwieldy and of little practical use. In the following sections a transistor model is developed which is both powerful and practical. It can be used with existing computer-aided circuit analysis programs to analyze interference in circuits. An extension of the method allows an analysis of RF effects in 4-layer pnpn structures.

3.2.1 Interference Effects with RF Conducted into Collector - In order to understand the interference effects produced as RF enters the output of a TTL device, it is important to study the effects of RF conducted into a transistor collector lead. Figure 14 shows the i_C vs v_{CE} curves for a 2N2369A transistor with a 220 MHz CW signal conducted into its collector. Figure 15 shows a similar set of curves for a 2N2222A transistor. For both transistors, the effect is a decrease in collector current at low v_{CE}. At high v_{CE}, the collector current is relatively unchanged. For the 2N2369A, the collector current decreases nearly to zero at low v_{CE}, so that it appears that the i_C vs v_{CE} curves have moved to the right. For the 2N2222A, the collector current decrease is less rapid, so that the effect is to cause the curves to become more rounded in the saturation region. These two effects are typical of the response of all transistors observed to date for RF energy conducted into their collectors.

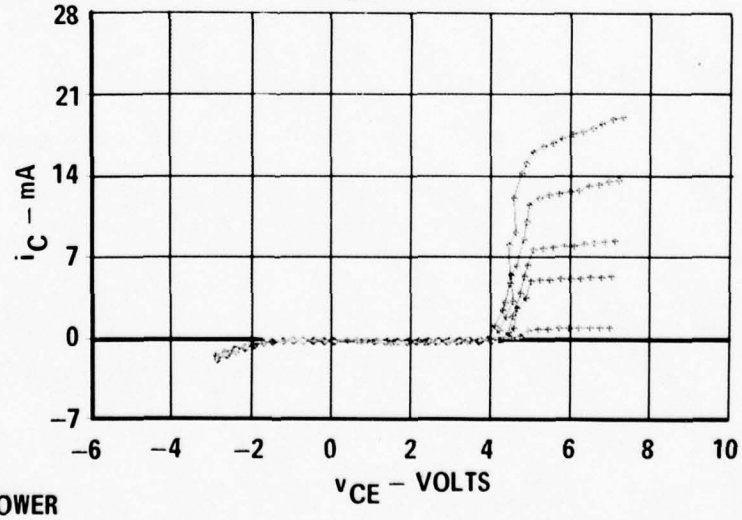
An observation can be made at this point. Since the greatest interference effect occurs at low v_{CE}, it appears that transistors biased at high v_{CE} are less susceptible to RF energy conducted into their collectors than transistors biased at low v_{CE}. This rule of thumb suggests that biasing transistors to operate at high collector-to-emitter voltages will result in circuits less likely to exhibit interference.



a) NO RF POWER

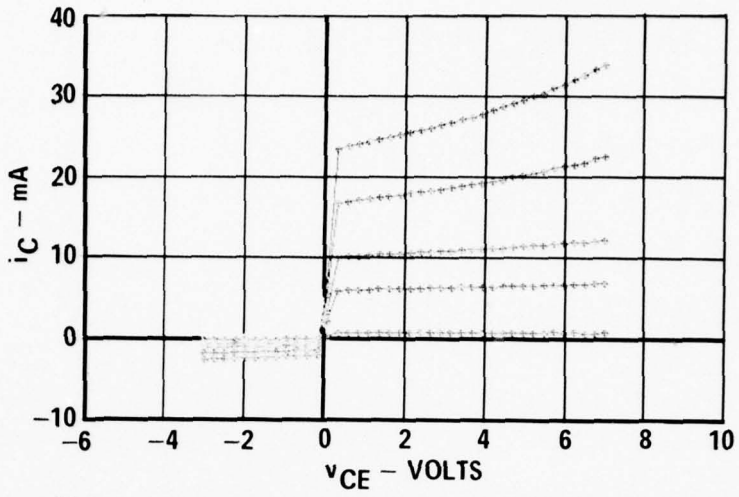


b) 24mW RF POWER

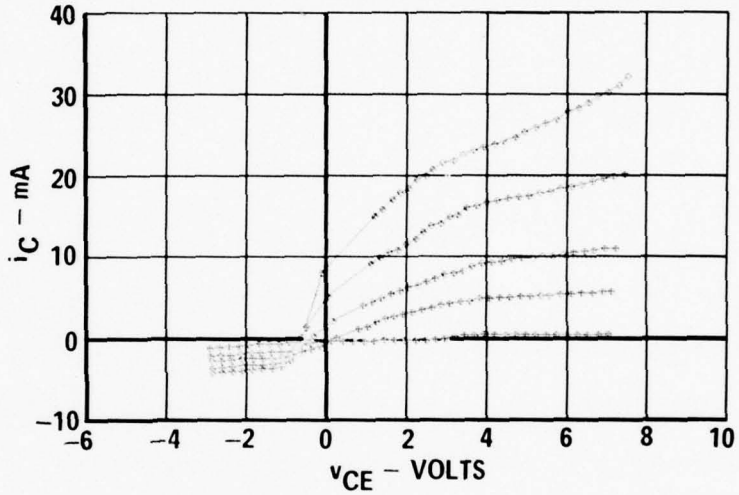


c) 90mW RF POWER

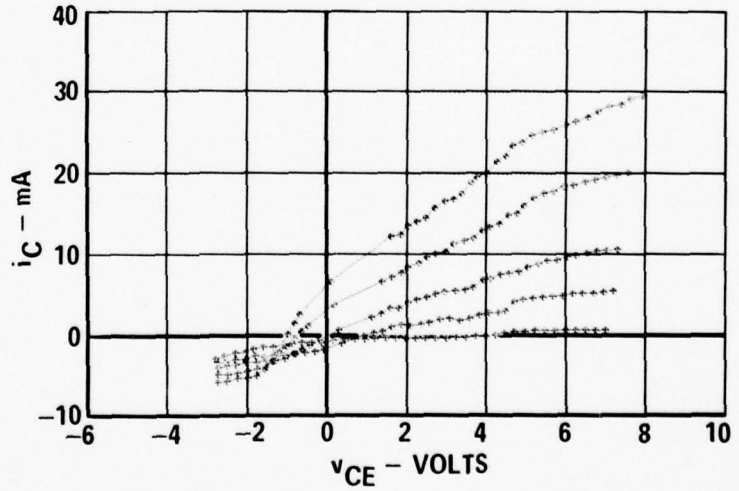
Figure 14 Measured 2N2369A Transistor Characteristic Curves with 220 MHz Conducted into the Collector (0.05 mA Base Current Steps)



a) NO RF POWER



b) 90mW RF POWER



c) 170mW RF POWER

Figure 15 Measured 2N2222A Transistor Characteristic Curves with 220 MHz Conducted into the Collector (0.05 mA Base Current Steps)

3.2.2 Modeling Interference Effects with RF Conducted into Collector - In modeling RF effects in transistors, the approach taken was to start with an existing transistor model, the Ebers-Moll representation, and modify it to account for the RF effects.

Figure 16 shows the standard Ebers-Moll model for an npn transistor, where the characteristics of the two diodes are given by

$$i_F = i_{OF}(\exp(qv_{BE}/KT) - 1),$$

$$i_R = I_{OR}(\exp(qv_{BC}/KT) - 1),$$

and I_{OF} and I_{OR} are the diode reverse saturation currents.

Little interference effect occurs at high v_{CE}, so it is approximately true in this region that

$$i_C = \beta i_B,$$

where β is forward current gain measured when no microwave energy is present. This suggests that, in modifying the Ebers-Moll model, the values α_F and α_R be kept constant at their dc values.

Holding the alphas constant for varying values of RF power requires the I-V characteristics of the two diodes in the Ebers-Moll model to change to account for the observed effects.

The diode I-V characteristics can be calculated at a given RF power from measurements of i_C, i_B, v_{CE}, and v_{BE}. Referring to figure 16, node equations written at the base and collector of the transistor are

$$i_B = (1 - \alpha_F)\, i_F + (1 - \alpha_R)\, i_R$$

$$i_C = \alpha_F\, i_F - i_R.$$

Solving for the two diode currents, i_F and i_R, yields

$$i_F = \frac{i_B + (1 - \alpha_R)\, i_C}{1 - \alpha_F \alpha_R},$$

$$i_R = \frac{\alpha_F \alpha_B - (1 - \alpha_F)\, i_C}{1 - \alpha_F \alpha_R}.$$

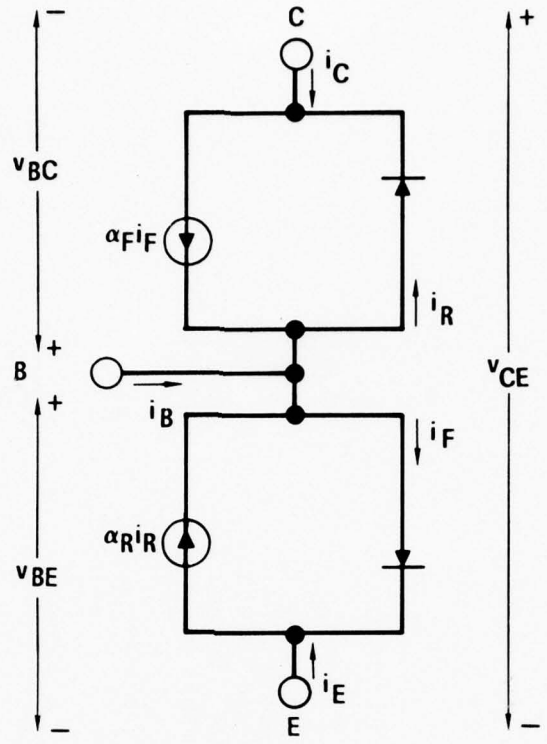


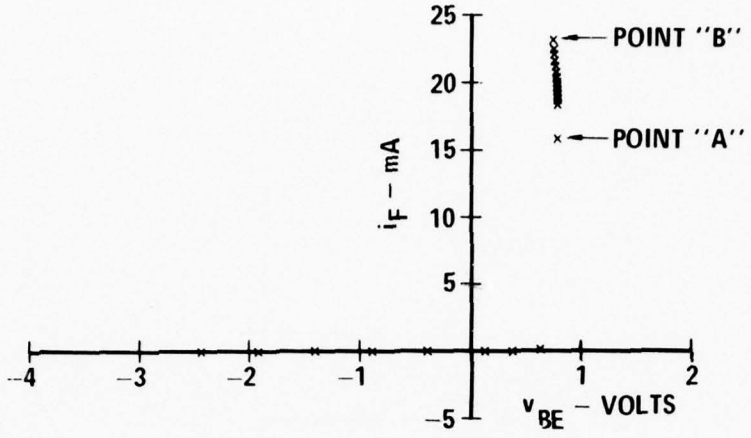
Figure 16 Standard Ebers-Moll Model for NPN Transistor

Also, the base-collector voltage is given by:

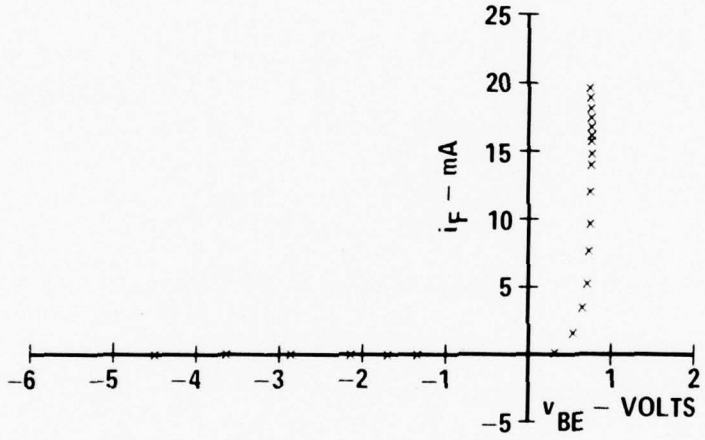
$$v_{BC} \approx v_{BE} - v_{CE}.$$

Measurement of the dc components of i_C, i_B, v_{CE} and v_{BE} allows one point on each of two "inferred" diode curves to be calculated: (v_{BE}, i_F) and (v_{BC}, i_R). Keeping the RF power constant and varying the transistor operating point allow both diode I-V curves at that power level to be determined.

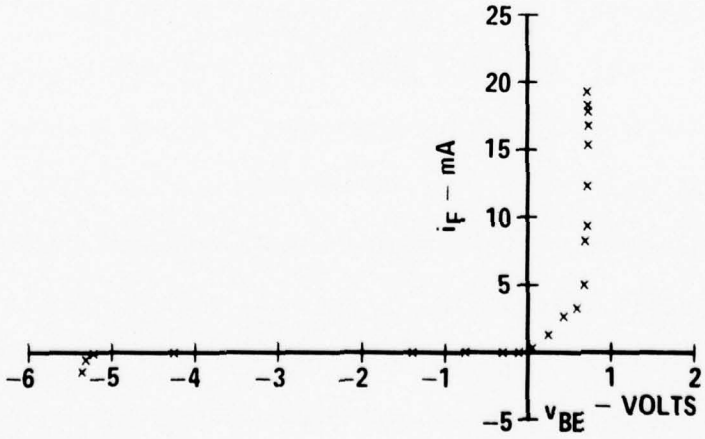
The 2N2369A and 2N2222A data of figures 14 and 15 were measured on an automated test system which simultaneously measures i_C, i_B, v_{CE}, and v_{BE}, as well as other parameters. Using the values of α_F = 0.9895 and α_R = 0 calculated from measurements of the 2N2369A forward and reverse betas, the inferred diode curves were determined from the 2N2369A data, and are shown plotted in figures 17 and 18. The curves are plotted as discrete points because each point is calculated from the transistor



a) NO RF POWER

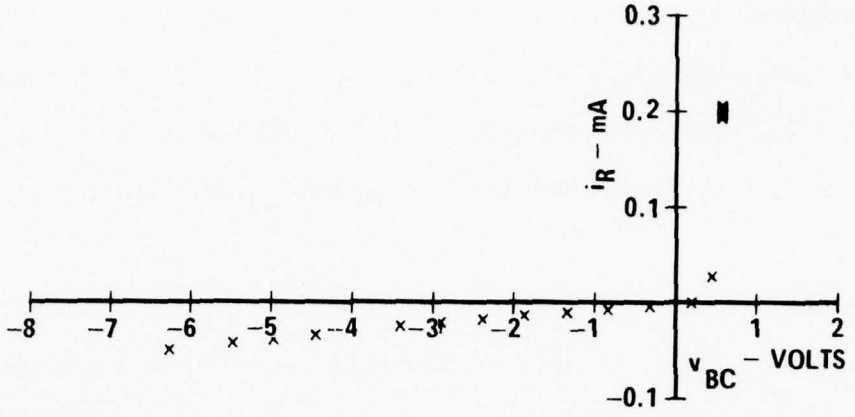


b) 24mW RF POWER

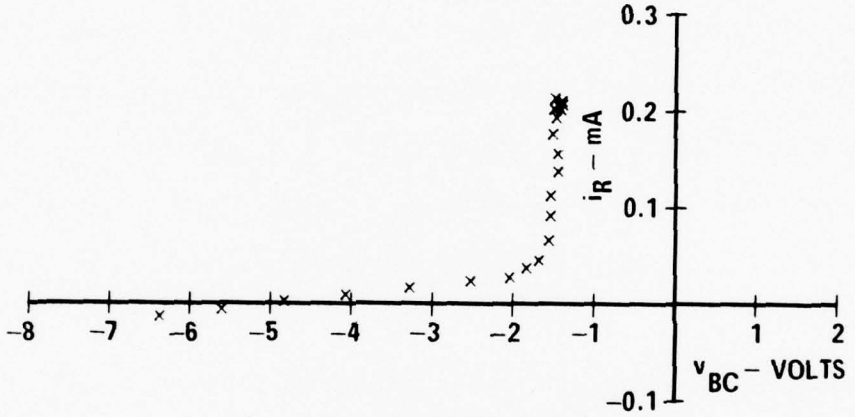


c) 90mW RF POWER

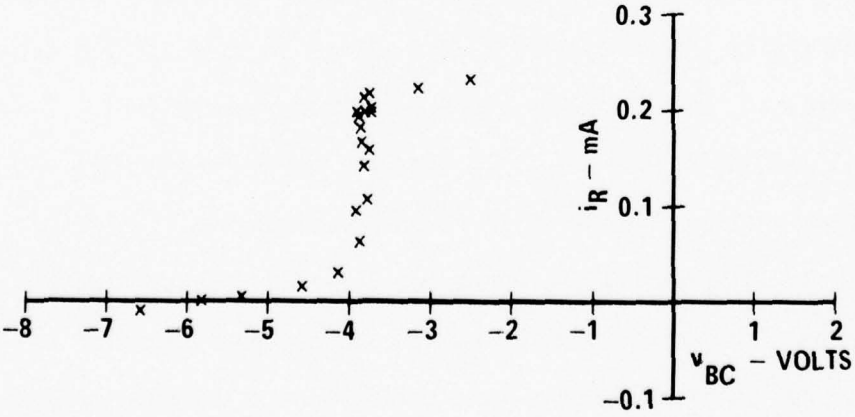
Figure 17 2N2369A Base-Emitter Inferred Diode Curves with 220 MHz Conducted Into the Collector



a) NO RF POWER



b) 24mW RF POWER



c) 90mW RF POWER

Figure 18 2N2369A Base-Collector Inferred Diode Curves With 220 MHz Conducted into the Collector

currents and voltages at a single bias condition. The points were calculated from the transistor curves where i_B = 0.2 mA. The inferred diode curves show considerable heating effect because the automated test system is unable to "sweep" a curve as a curve tracer; it is much slower and causes considerably more heating in the transistor.

The 2N2369A base-emitter inferred diode curves of figure 17 show the diode at 24 mW and 90 mW of RF power incident on the collector. Figure 17a shows a typical diode characteristic, with a sharp turn-on at about 0.8 volt, and little conduction below that. The reverse slope between points "A" and "B" is a thermal effect and will be discussed later. As the RF power increases, the knee becomes less sharp, folding up in an almost linear region between the non-conducting and conducting regions of the diode. Notice also that at 90 mW of RF power (figure 17c) the base-emitter breakdown comes into view at about -5.4 volts. This breakdown occurs because the transistor avalanche breakdown point appears to move to the right with increasing RF power.

The 2N2369A base-collector inferred diode curves shown in figure 18 correspond to the same RF powers as the curves of figure 17. Figure 18a shows a sharp diode turn-on at about 0.5 volt. The rather large reverse currents (up to 0.05 mA) are partially a heating effect, and will also be discussed later. As the RF power is increased, the diode knee appears to move to the left. The heating effect is still present in the points to the left of the diode knee, evidenced by the slope in these points. At 90 mW of RF power (figure 18c) there is a second break point at -4 volts and 0.2 mA, where the curve appears to flatten out, giving the whole curve an "S" shape. The two points at the upper right of the curve occur when the transistor is breaking down, and correspond to the points when the base-emitter diode breaks down. Ordinarily the base-collector diode current becomes clamped at the base current because the base-emitter diode is reverse biased (and

$\alpha_R = 0$), and any v_{CE} change is reflected in a change in reverse voltage of the base-emitter diode. However, when the base-emitter diode breaks down, it conducts and its voltage becomes clamped at the breakdown voltage. A change in v_{CE} must therefore be reflected in a change in v_{BC}. Since the Ebers-Moll model does not account for breakdown, these points are artificial. For a transistor operating on a typical load line, the breakdown region will rarely be a region of operation, even considering RF stimulus. In view of this, the breakdown region of the diodes will not be modeled.

In analyzing the heating effects, consider first the reverse slope of the conduction region of the base-emitter diode (figure 17a). For a silicon diode conducting heavily in the forward region the current is

$$i \approx I_o \exp (v/V_T)$$

where the reverse saturation current I_o is given by[7]

$$I_o = K_1 T^{1.5} \exp (-V_{GO}/V_T)$$

where K_1 is a constant,

T is temperature in degrees Kelvin,

V_T is $\frac{kT}{q} = \frac{T}{11,600}$, and

V_{GO} is a voltage which is numerically equal to the forbidden gap energy in electron volts. For constant i,

$$\frac{dv}{dT} = \frac{v - (V_{GO} + 1.5\ V_T)}{T} . \qquad (1)$$

Temperature measurements were made on the 2N2369A transistor when no RF energy was applied. When biased at v_{CE} = 7.00 volts and i_C = 23.0 mA, which corresponds to the largest power dissipated in figure 14a, 160 mW, the transistor reached a stable case temperature of 118°F (321°K). When the transistor was biased at a v_{CE} of 0.328 volt and i_C of 15.6 mA, only 5 mW was dissipated, and the transistor can be assumed to be at the ambient temperature, 72°F (295°K). The points labeled "B" (v_{BE} of 0.7519 volt, i_F of 23.2 mA) and "A" (v_{BE} of 0.79 volt, i_F of 15.6 mA)

in figure 17a correspond to these two temperatures, respectively. The voltage decrease from point A to B is 0.0381 volt, as the temperature increased 46°F (26°C). At "A" v is 0.79 volt and T = 295°K, so from (1)

$$\frac{dv}{dT} = -1.55 \frac{mV}{°K},$$

The predicted Δv would be

$$\Delta v = \frac{dv}{dT} \Delta T = 0.0403 \text{ volts},$$

which is very nearly the observed voltage change.

For a reversed biased silicon diode, the reverse current is composed mainly of transition-layer charge-generation current, which varies with both bias voltage and temperature. The current is proportional to the square of the reverse bias voltage[8]. The temperature dependence is given by

$$I_o = K_2 T^{1.5} \exp (-V_{GO}/2V_T)$$

where K_2 is a constant.[7]

As the temperature increases from 72°F to 118°F, this relation predicts that I_o will increase by a factor of 7.80. The large reverse current observed in figure 18a as the reverse bias voltage increases is probably due to both the voltage-squared variation and heating effects.

Since heating effects are not the subject of this report, little more will be said about them. However, an awareness of these effects helps interpret the inferred diode curves shown earlier.

The approach used to model the inferred diode curves of figures 17 and 18 is shown in figure 19. Each of the diode I-V curves has a somewhat piecewise linear behavior which can be approximated by summing the two curves shown in figure 19. The solid line represents the dc diode characteristics, while the dashed line represents the effect of RF energy on the diode. The latter is piecewise linear in behavior and is defined as zero current for voltages below some voltage, v_{OC},

and increasing current with a slope of $\frac{1}{R}$ for voltages greater than v_{OC}. The sum is a curve with approximately zero current below v_{OC}, increasing current with a slope of $\frac{1}{R}$ between v_{OC} and $v_{TURN-ON}$, and sharply increasing current above $v_{TURN-ON}$. The curve intercepts the current axis at a value of short-circuit current, i_{SC}.

The similarity of the sum to the curves of figure 17 is evident, but the similarity to the curves of figure 18 is more difficult to see. The curves of figure 18 can be thought to have a large slope $\frac{1}{R}$, and a large i_{SC}, say 20 mA. In this way, both the base-emitter and base-collector inferred diodes of the 2N2369A can be modeled in the same fashion.

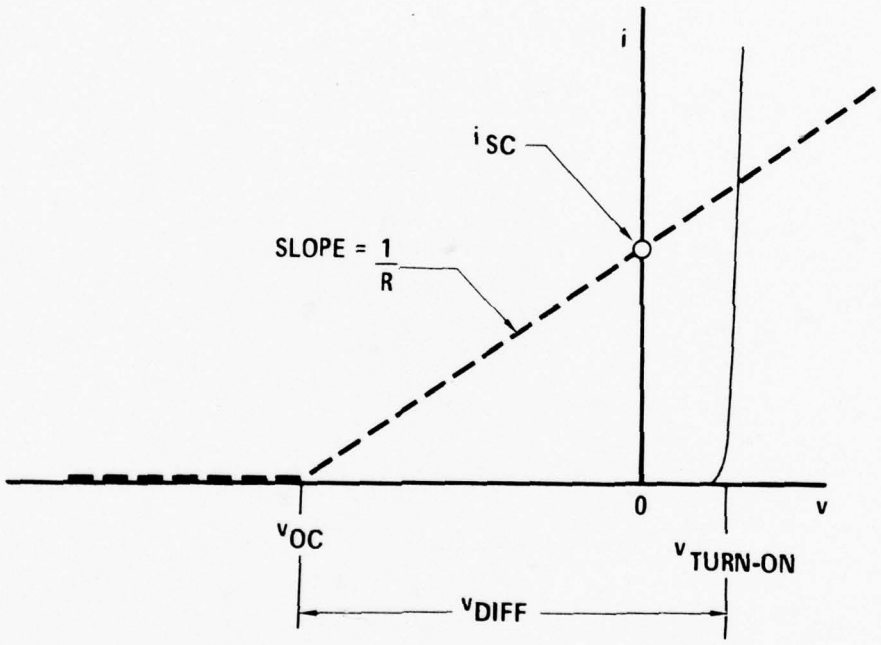


Figure 19 Approach Used to Model Diode Curves

A circuit which realizes the curves of figure 19 is shown in figure 20. Diode D1 is assumed to be the dc diode, having a current-voltage characteristic given by

$$i_{D1} = I_o \left(\exp \left(qv_{D1}/kT\right) - 1\right)$$

where I_o is the diode reverse saturation current. D1 produces the solid line of figure 19, while the left branch of the circuit produces the dashed line. Diode

D2 acts as a switch, allowing current to flow through the Norton equivalent only when it is "on". The voltage at which the diode turns on is determined by the open circuit voltage of the Norton equivalent, $i_X R$. Diode D2 conducts when the voltage across it is greater than its own turn-on voltage, $v_{TURN\text{-}ON_2}$, which occurs when

$$v > v_{OC} = v_{TURN\text{-}ON_2} - i_X R.$$

When v is less than v_{OC}, the current through the left branch is essentially zero. For v greater than v_{OC}, the current through the left branch is

$$i_{D2} = i_X + (v - v_{TURN\text{-}ON_2})/R.$$

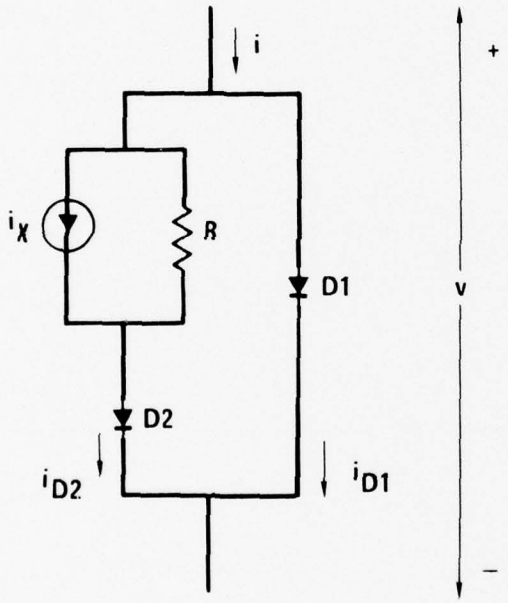


Figure 20 Circuit Model of Diode under RF Influence

Usually it can be assumed that diodes D1 and D2 have the same characteristics, so that

$$v_{TURN\text{-}ON_1} = v_{TURN\text{-}ON_2}$$

and the voltage, v_{DIFF}, of figure 19 is

$$v_{DIFF} = i_X R.$$

The Norton generator elements, i_X and R, are functions of RF power and frequency. Experimental results show that, in general, R is constant for different RF power levels at a given frequency, but that i_X varies with the microwave power level. A relation for i_X that gives good results is

$$i_X = v_{DIFF}/R,$$

where

$$v_{DIFF} = X\sqrt{8R_g P_{RF}}$$

and R_g is the real part of the RF generator impedance in ohms, and P_{RF} is the available RF power in watts, and X is a constant of proportionality. Note that with no RF power, $i_X = 0$. In the forward conduction region with no RF power the model essentially acts as the dc diode, D1, because resistor R limits the current that can flow through diode D2. In the reverse region, the reverse current will be approximately double that of the dc diode. This difference is not thought to be significant. The diode model is accurate both when RF energy is present and when it is removed.

Table 2 lists the diode model parameters obtained from a best fit to the 2N2369A base-emitter and base-collector inferred diode curves at 220 MHz. The generator impedance, R_g, is 50 ohms. The diode curves that result when using these parameters are shown in figure 21 for a range of RF powers at 220 MHz. Comparison with figures 17 and 18 shows the accuracy obtained by using this simple diode model.

The diode model of figure 20 is adequate for modeling discrete diodes under RF influence, such as those discussed in Section 3.1 as well as the inferred diodes discussed here. This might be done, for example, when analyzing the interference effect that might be produced in a circuit containing diodes, where a time-domain calculation would be overly difficult and time-consuming.

Table 2 2N2369A Inferred Diode Model Parameters

220 MHz CW RF POWER CONDUCTED INTO COLLECTOR

BASE-EMITTER DIODE:	
I_{OF}	9.36×10^{-16} AMPS
R_E	180 Ω
X_E	0.12
BASE-COLLECTOR DIODE:	
I_{OR}	7.55×10^{-15} AMPS
R_C	190 Ω
X_C	0.72

By inserting the diode model into the Ebers-Moll representation, a model for the transistor with RF stimulus is obtained. Figure 22 shows the modified Ebers-Moll transistor model. Using the parameters derived for the 2N2369A diodes, the transistor i_C vs v_{CE} curves can be retraced. The result is shown in figure 23. The agreement with the curves of figure 14 is good.

A similar analysis can be performed on the 2N2222A transistor. The inferred diode curves are shown in figures 24 and 25 for the 2N2222A base-emitter and base-collector diodes, respectively. Notice the heating effect evident in the reverse slope of the base-emitter diode forward conduction region, and the large reverse currents in the base-collector diode. Superimposed on these are the results of using the diode model of figure 20 using the parameters listed in table 3. The resulting transistor curves from the modified Ebers-Moll model are shown in figure 26. These curves are a fair approximation to those of figure 15. Notice that the saturation region does not show the continuous curve seen in figure 15, but is approximated by a straight-line region. This difference results from

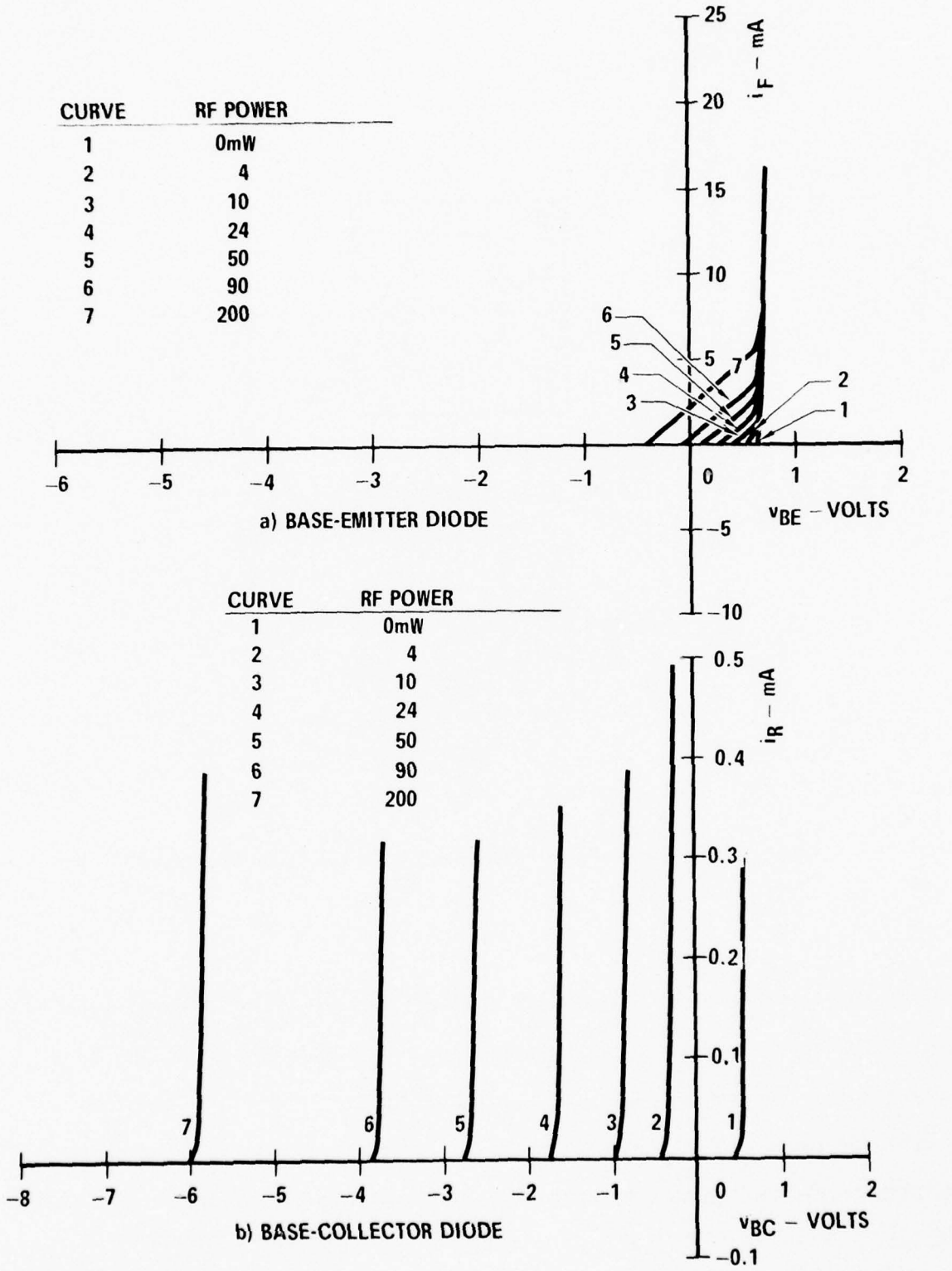


Figure 21 Simulation of 2N2369A Inferred Diode Curves with 220 MHz Conducted Into Collector

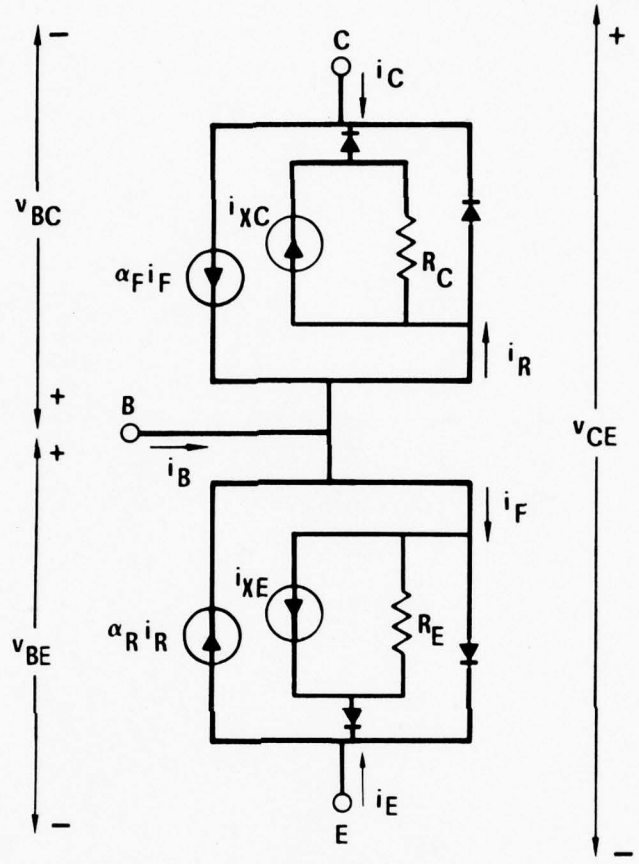
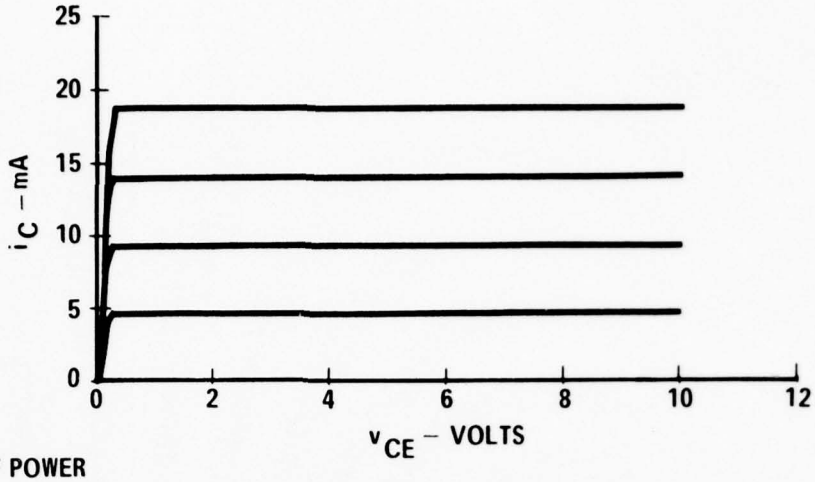
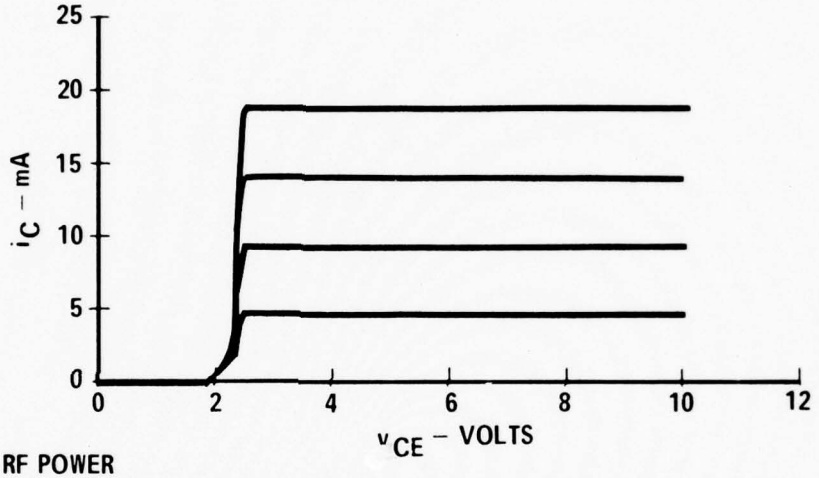


Figure 22 Modified Ebers-Moll Model for a Transistor Under RF Influence

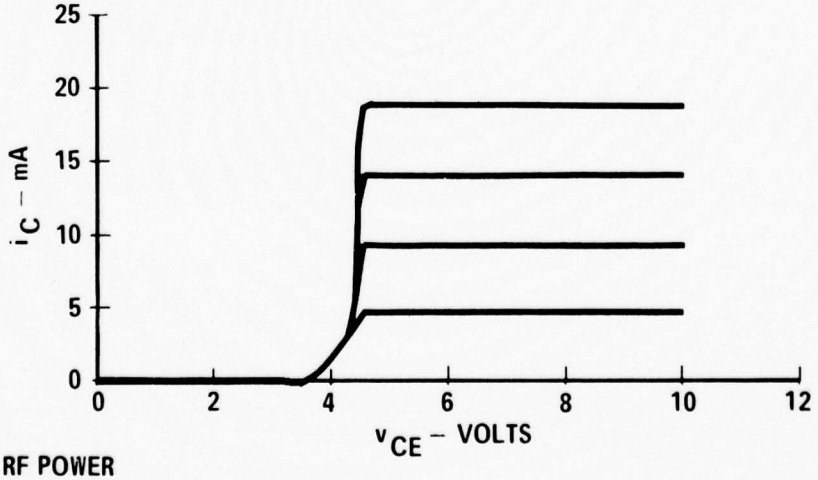
modeling the inferred diode curves with a linear region at the knee due to the RF energy. The base-collector diode, especially, is insufficiently modeled by a linear region. The given transistor simulation is fairly accurate compared with the measured case, and is straightforward to implement. If desired, a better simulation could be obtained by approximating the diode curves with a more complex function.



a) NO RF POWER



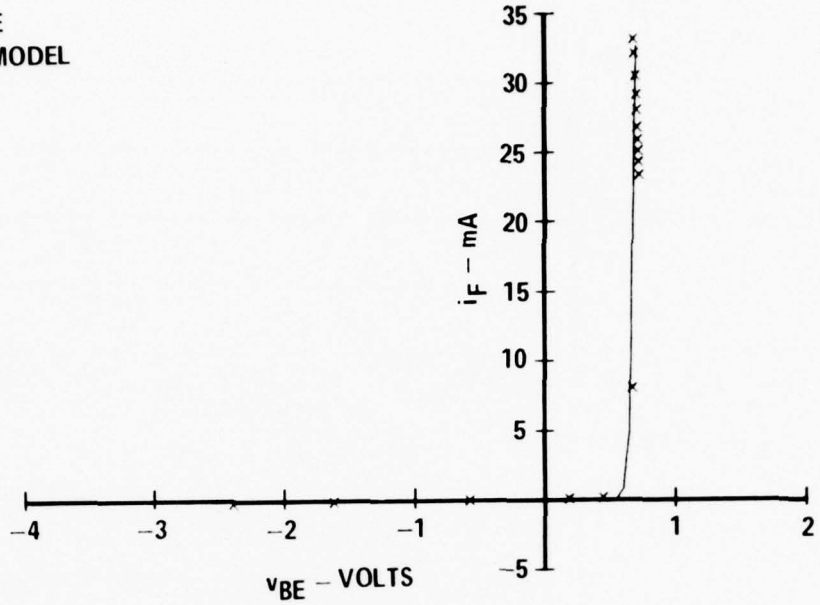
b) 24mW RF POWER



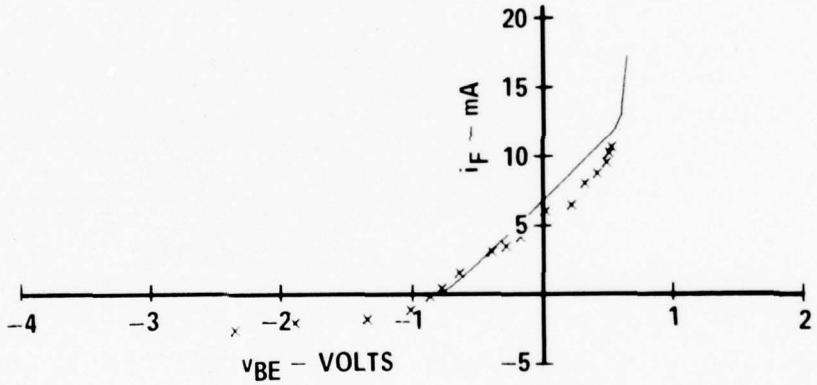
c) 90mW RF POWER

Figure 23 Simulation of 2N2369A Transistor Characteristic Curves with 220 MHz Conducted Into Collector (0.05 mA Base Current Steps)

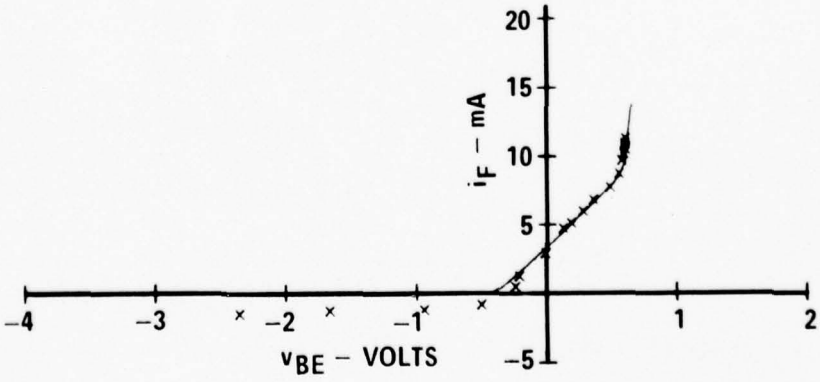
X's – INFERRED DIODE
SOLID LINE – DIODE MODEL



a) NO RF POWER



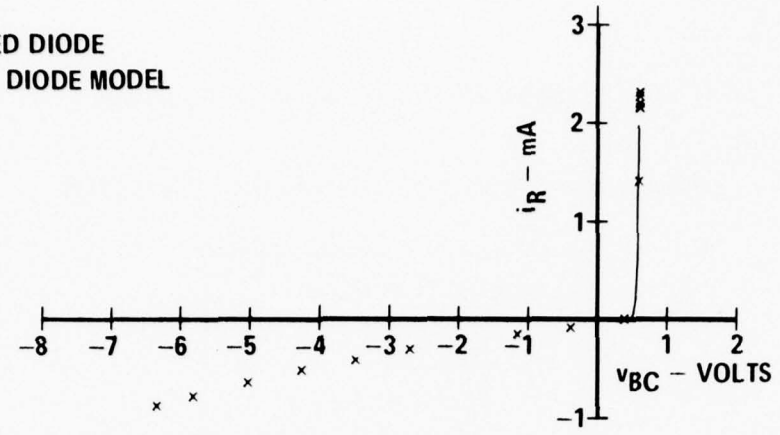
b) 90mW RF POWER



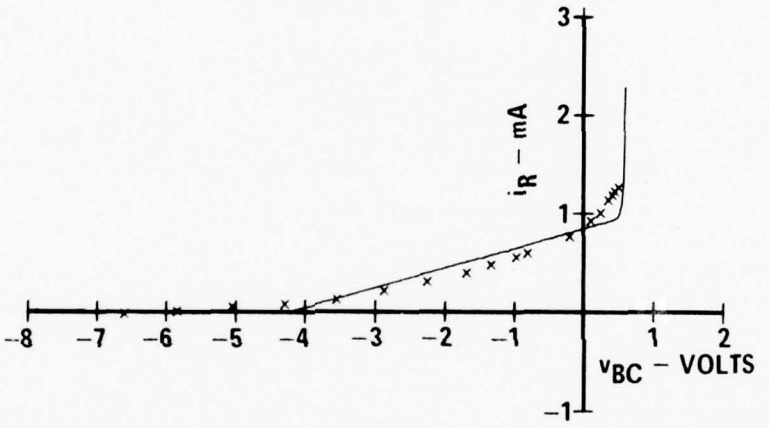
c) 170 mW RF POWER

Figure 24 2N2222A Base-Emitter Inferred Diode Curves with 220 MHz Conducted Into Collector

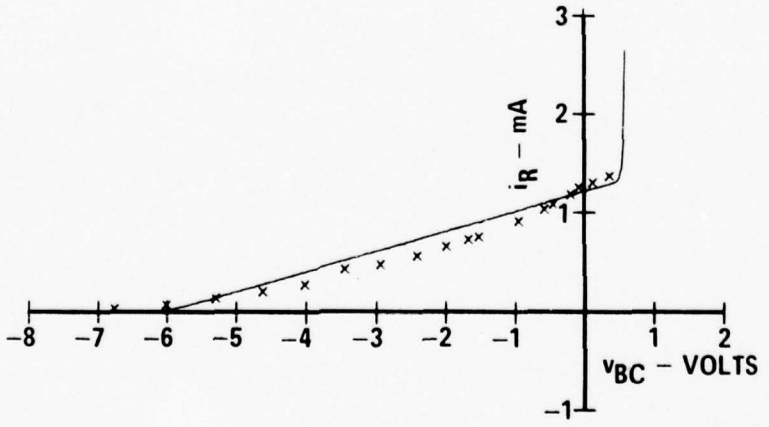
X's – INFERRED DIODE
SOLID LINE – DIODE MODEL



a) NO RF POWER



b) 90mW RF POWER



c) 170 mW RF POWER

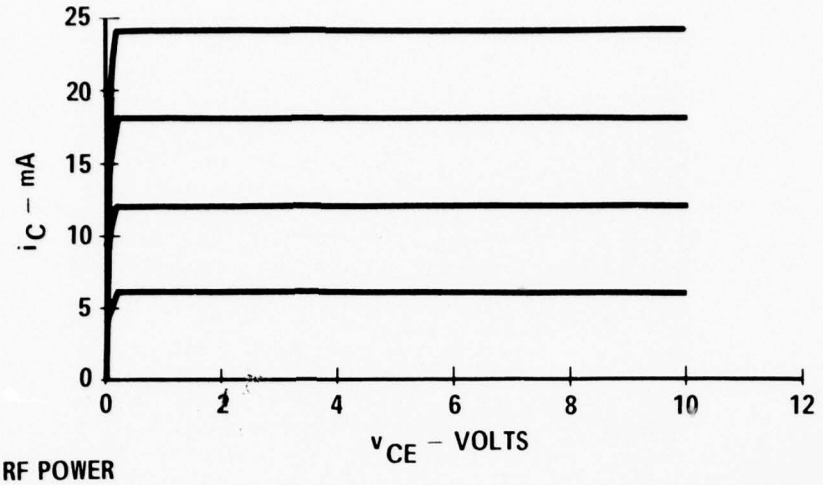
Figure 25 2N2222A Base-Collector Inferred Diode Curves with 220 MHz Conducted Into Collector

Table 3 2N2222A Inferred Diode Model Parameters

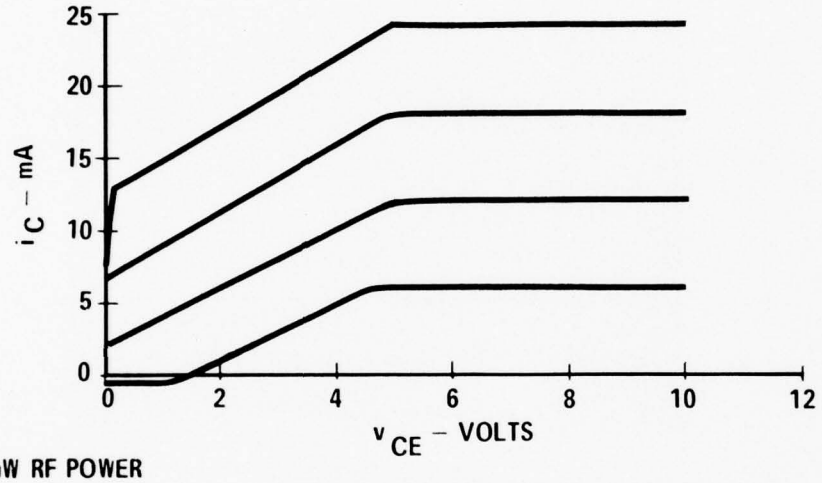
220 MHz CW RF POWER CONDUCTED INTO COLLECTOR

BASE-EMITTER DIODE:	
I_{OF}	2.2×10^{-14} A
R_E	104 Ω
X_E	0.166
BASE-COLLECTOR DIODE:	
I_{OR}	3.3×10^{-14} A
R_C	4.9K Ω
X_C	0.80

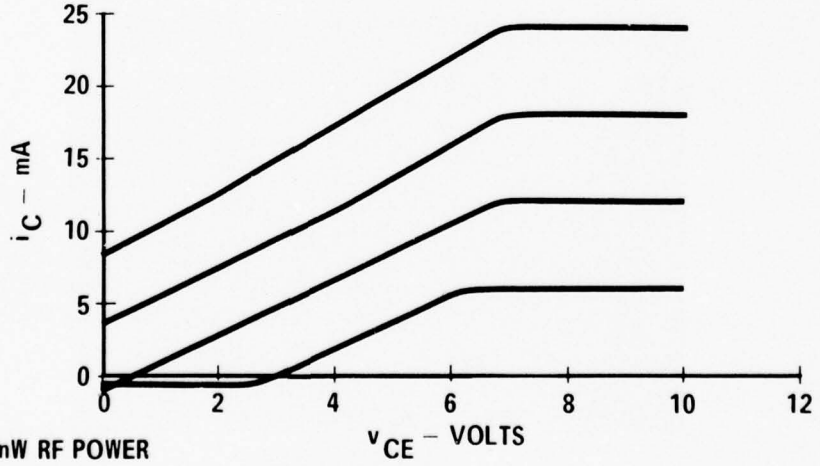
3.2.3 Interference Effects with RF Conducted into Base - Figures 27 and 28 show the 2N2369A and 2N2222A transistor i_C vs v_{CE} characteristics when a 220 MHz CW signal is injected into the base. The interference effect is different for this case than when RF energy is injected into the collector. The forward current gain (beta) decreases significantly with low levels of RF power; for the 2N2222A, only 5.4 mW of RF power reduces the beta to less than half of its original value. The curves appear to shrink uniformly; the ac and dc betas decrease at the same rate. At 55 mW, the 2N2369A curves show an additional effect by rising off the voltage axis with a current offset. The 2N2222A curves move to the left with increasing RF level.



a) NO RF POWER

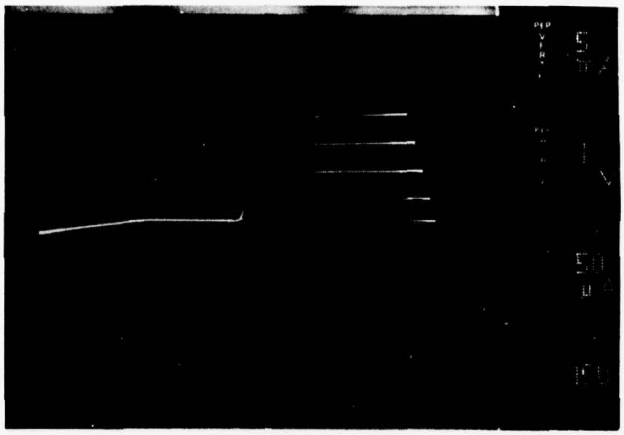


b) 90mW RF POWER

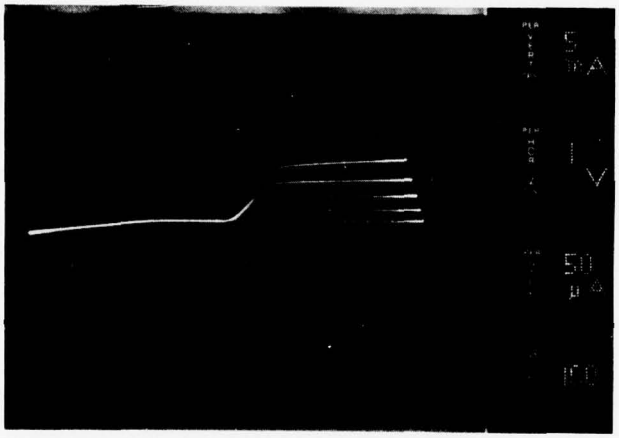


c) 170mW RF POWER

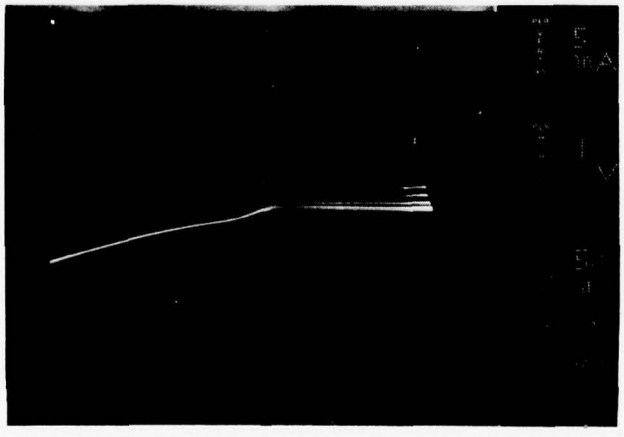
Figure 26 Simulation of 2N2222A Transistor Characteristic Curves with 220 MHz Conducted Into the Collector (0.05 mA Base Current Steps)



a) NO RF POWER

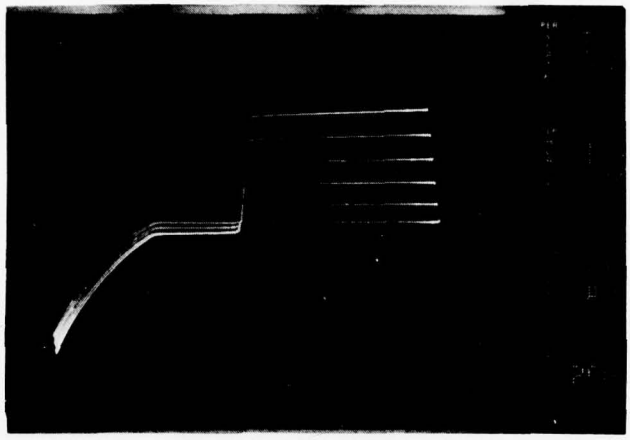


b) 2.8mW RF POWER

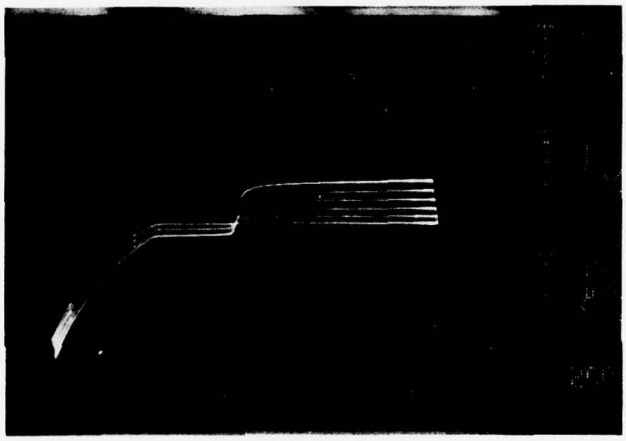


c) 55mW RF POWER

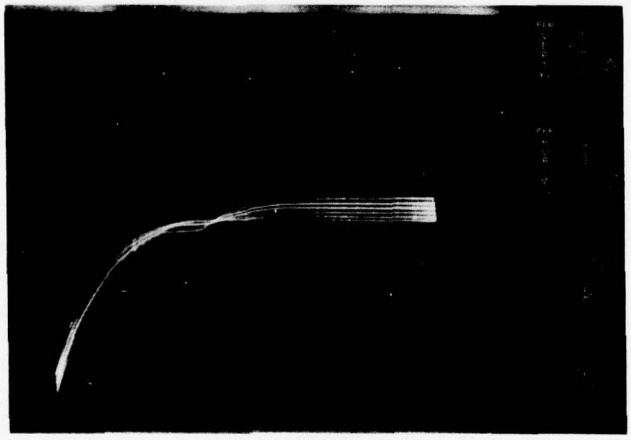
Figure 27 Measured 2N2369A Transistor Characteristic Curves with 220 MHz Conducted into the Base



a) NO RF POWER



b) 5.4mW RF POWER



c) 69mW RF POWER

Figure 28 Measured 2N2222A Transistor Characteristic Curves with 220 MHz Conducted into the Base

Figure 29 shows a plot of beta vs 220 MHz RF power incident on the base for several transistors. For the 2N930 and 2N930A, beta begins to decrease at less than 0.1 mW of RF power, and decreases quite rapidly, reaching one-tenth of its original value at approximately 3 mW. Other transistors do not show a significant beta decrease until about 1 mW of RF power is reached, and decrease less rapidly than the 2N930 and 2N930A. To date, no general quantitative relationship exists between beta and RF power level.

3.2.4 Modeling Interference Effects with RF Conducted into Base - The modified Ebers-Moll model can be applied to transistors with RF energy entering the base if α_F and α_R are allowed to vary as the RF power is increased. This means that the forward and reverse alphas (or equivalently, the betas) must be treated as functions of RF power. Once the betas or alphas ($\alpha = \frac{\beta}{\beta + 1}$) are determined, the inferred diode curves can be obtained as outlined previously. At present, a logarithmic polynomial curve fit may be the best way to characterize beta vs RF power, since no general relation exists.

An interference effect not seen in the curves of figures 27 and 28 is a rapid decrease in v_{BE} as the RF power is increased. At high enough powers, v_{BE} becomes negative. This decrease is due to a rectified voltage in the base-emitter junction of the transistor. Depending on the transistor application, the decrease in v_{BE} may be the dominant interference effect. No special effort is required to model it, as the inferred diode curves contain the required information.

It is evident that modeling the transistor with RF energy entering the base is more difficult than when it enters the collector because the dependence of β on RF power must be obtained for a complete model.

3.2.5 Interference Effects in Integrated Circuit Transistors - The method used to infer diode rectification curves from transistors can be extended to include

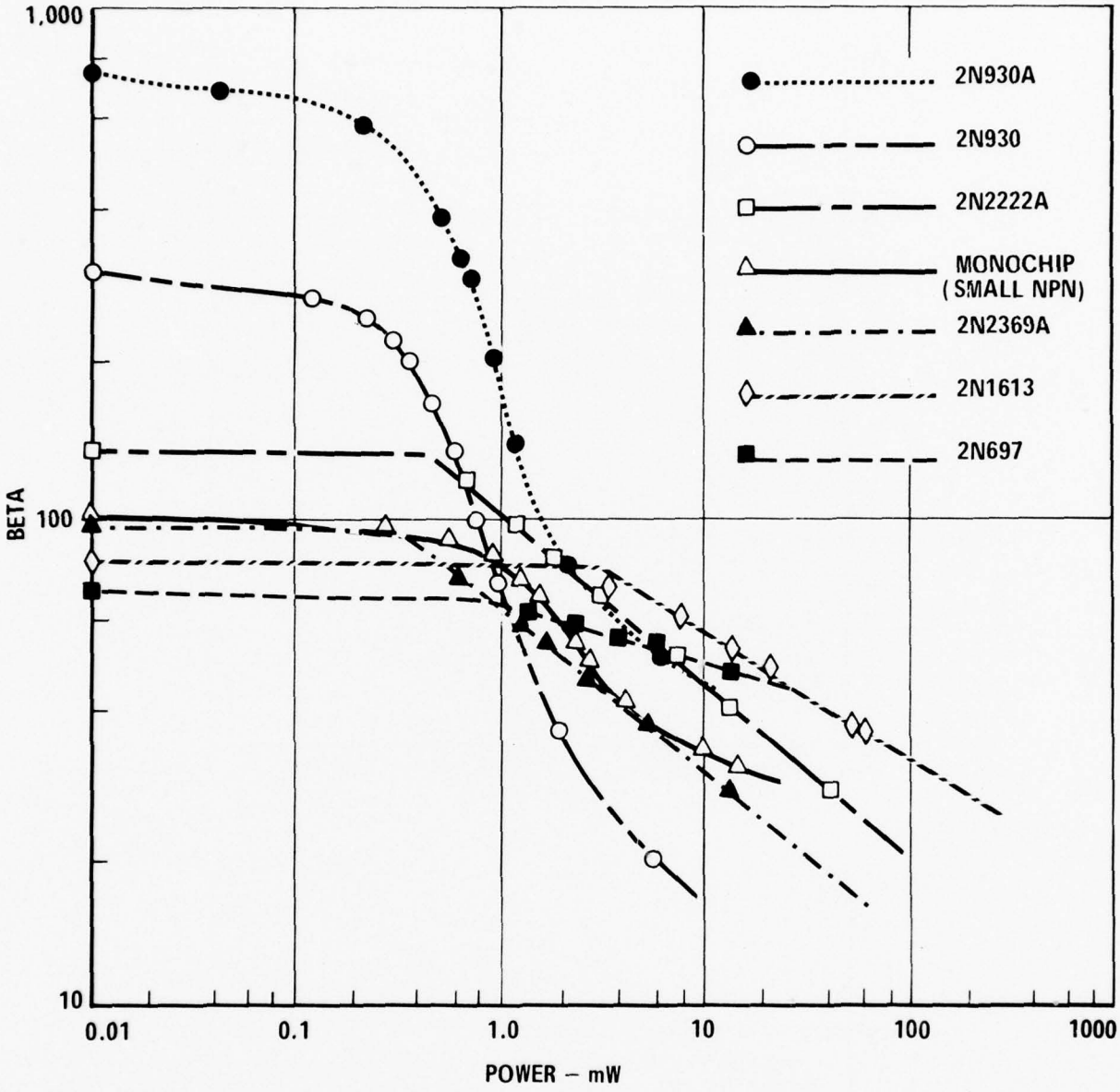
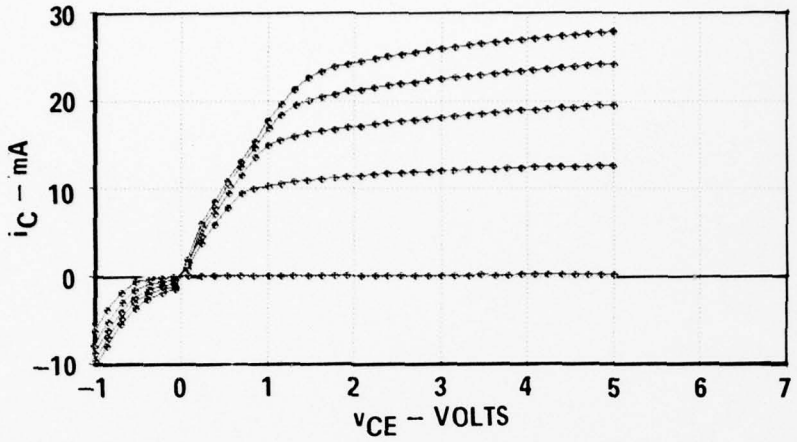
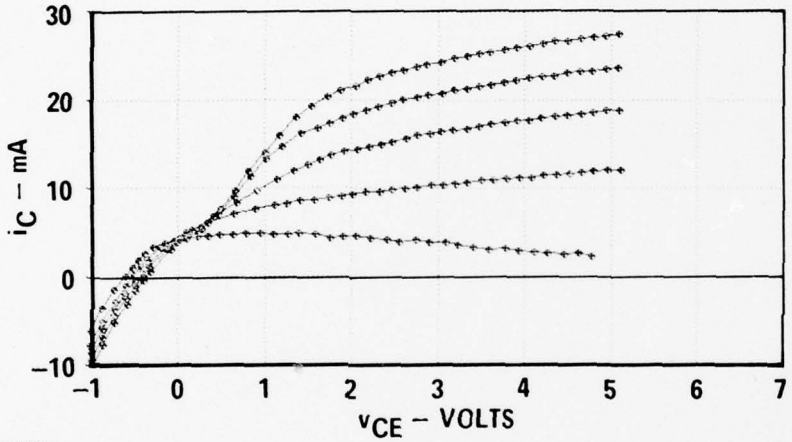


Figure 29 Measured Beta as a Function of RF Power with 220 MHz Conducted into the Base

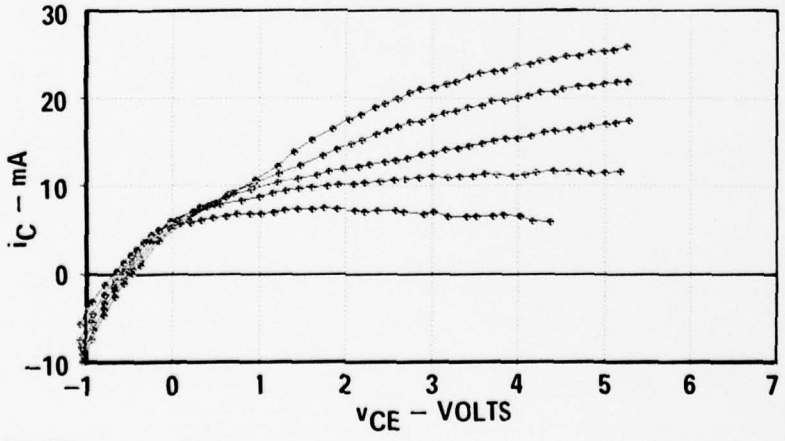
4-layer pnpn structures. The device chosen to illustrate this technique was a Monochip MO-001, which contains 4 "small npn" (Interdesign's designation) transistors on a p-type substrate. Transistor curves are shown in figure 30 for no RF and for 55 mW and 140 mW of RF power on the collector of one of the transistors.



a) NO RF



b) 55 mW RF POWER



c) 140 mW RF POWER

Figure 30 Measured Monochip MO–001 Transistor Characteristic Curves with 220 MHz Conducted into Collector (0.25 mA Base Current Steps)

A proposed 4-layer structure model[9] is shown in figure 31. It is an expanded version of the Ebers-Moll transistor model, with an extra diode to account for the substrate-to-collector junction, and two extra current-controlled current sources to account for coupling between the substrate-to-collector and base-to-collector junctions. The values of α_F and α_R were measured by connecting the device as an npn transistor on a curve tracer using the collector, base, and emitter terminals, with the substrate shorted to the collector. The values of α_1 and α_2 were measured by connecting it as a pnp transistor using the base, collector, and substrate terminals, with the emitter shorted to the base. The measured values are:

$$\alpha_F = 0.9783$$

$$\alpha_R = 0.231$$

$$\alpha_1 = 0.737$$

$$\alpha_2 = 0.074.$$

Rectification is possible in each of the three diode junctions. Using a procedure similar to that used to calculate transistor inferred diode curves, the three inferred diode curves were calculated for RF entering the collector terminal. Figure 32 shows the inferred diode curves for the no RF case. The substrate-collector and base-collector diodes look like typical diodes, while the base-emitter diode shows an unusual reverse conduction at voltages below its turn-on voltage. This is due to limitations in the model; α_R may not be constant, or additional coupling terms may be necessary.

Figure 33 shows the inferred diode curves with 55 mW of RF power at 220 MHz entering the collector terminal. The curves are similar to those seen before for transistors, with the exception of the base-emitter diode which has an unusual "hump", again probably due to model limitations. Figure 34 shows the inferred diodes for 140 mW of 220 MHz RF power entering the collector, and they look similar to those for 55 mW.

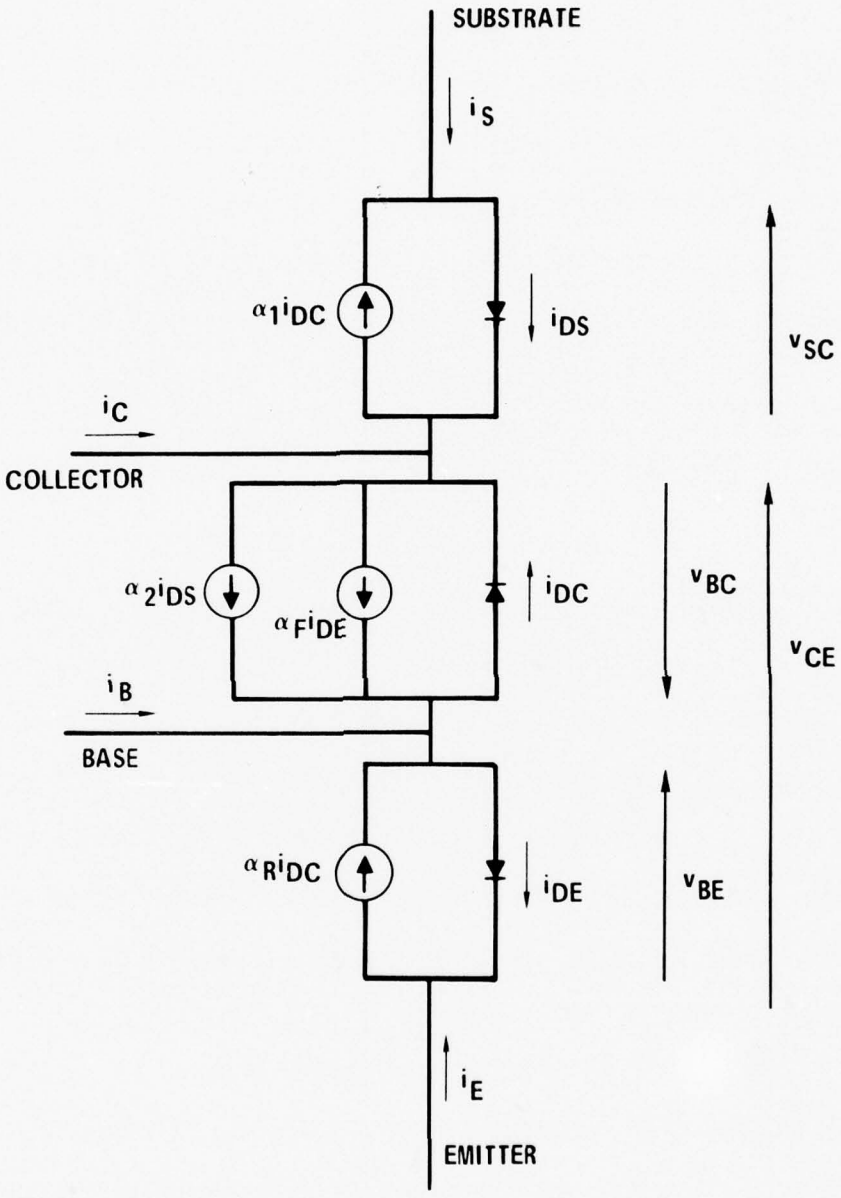
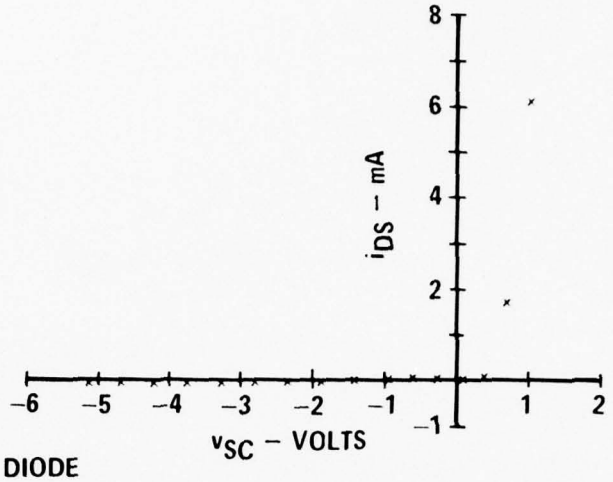
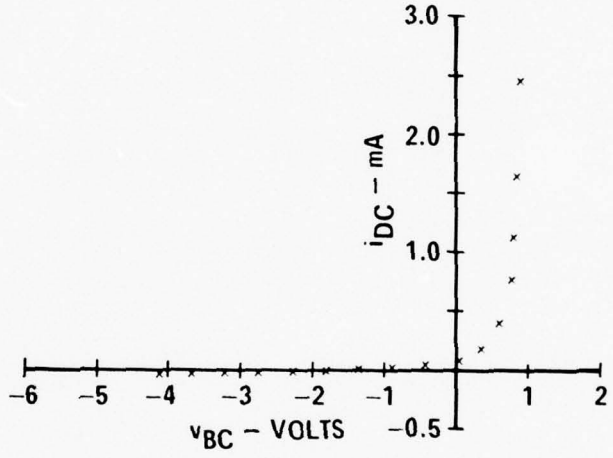


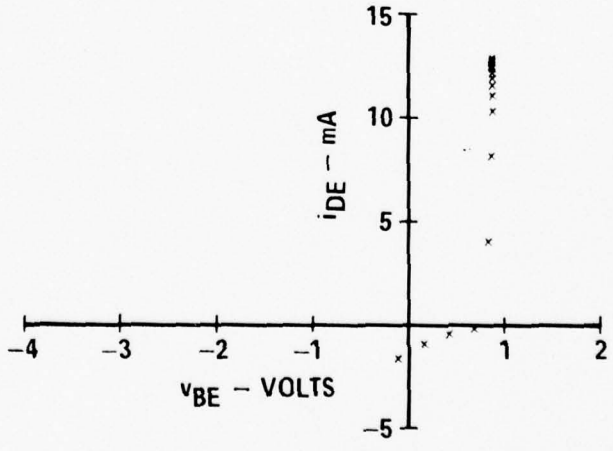
Figure 31 Four Layer Structure Model



a) SUBSTRATE TO COLLECTOR DIODE

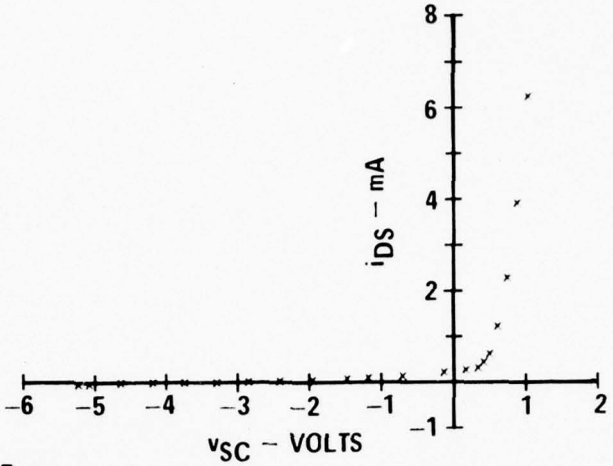


b) BASE TO COLLECTOR DIODE

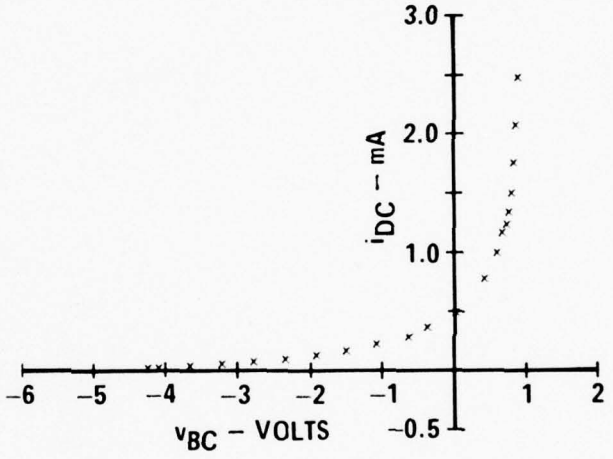


c) BASE TO EMITTER DIODE

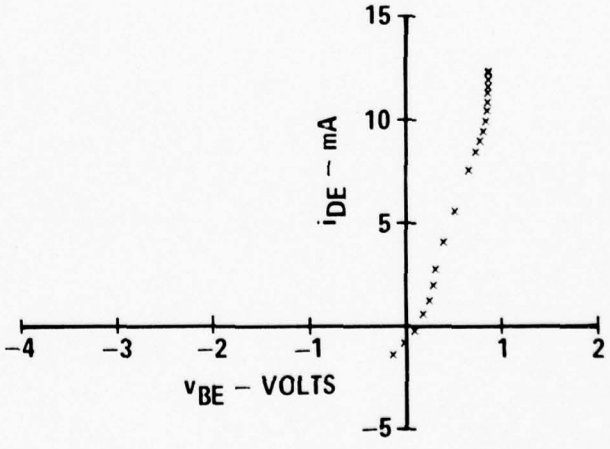
Figure 32 Inferred Diode Curves for Monochip MO−001 Transistor With No RF



a) SUBSTRATE TO COLLECTOR DIODE

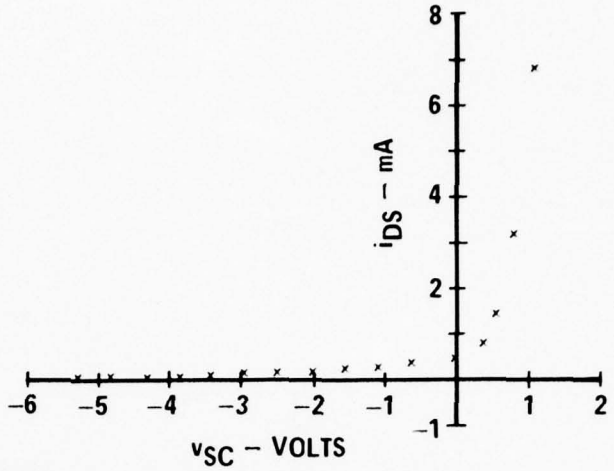


b) BASE TO COLLECTOR DIODE

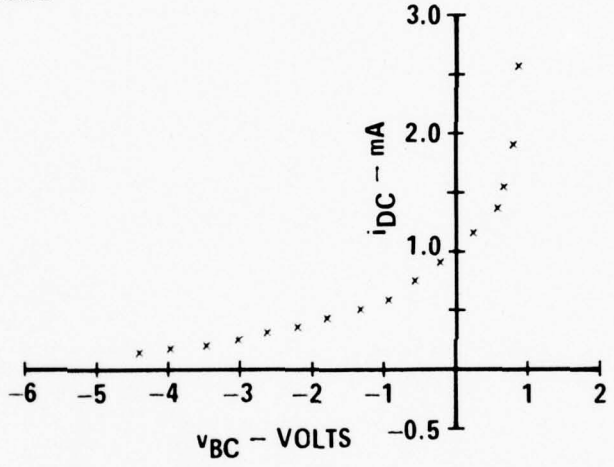


c) BASE TO EMITTER DIODE

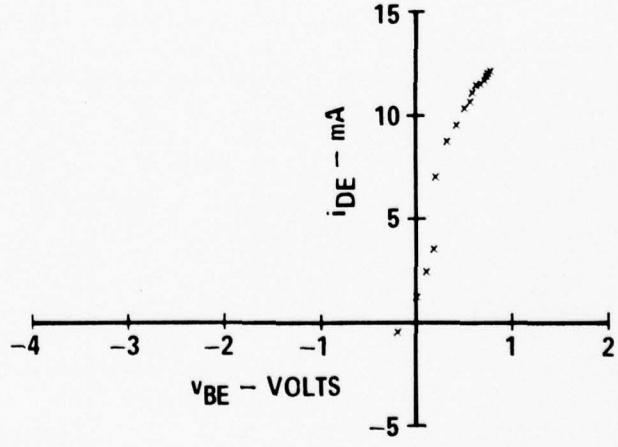
Figure 33 Inferred Diode Curves for Monochip MO–001 Transistor With 55 mW of RF Power at 220 MHz Conducted into the Collector



a) SUBSTRATE TO COLLECTOR DIODE



b) BASE TO COLLECTOR DIODE



c) BASE TO EMITTER DIODE

Figure 34 Inferred Diode Curves for Monochip MO–001 Transistor with 140 mW of RF Power at 220 MHz Conducted into the Collector

These inferred curves suggest that the modified Ebers-Moll model for transistors can be extended to include a substrate junction by modeling the additional junction in the same manner as done before for the base-emitter and base-collector junctions. The proposed 4-layer modified model is shown in figure 35.

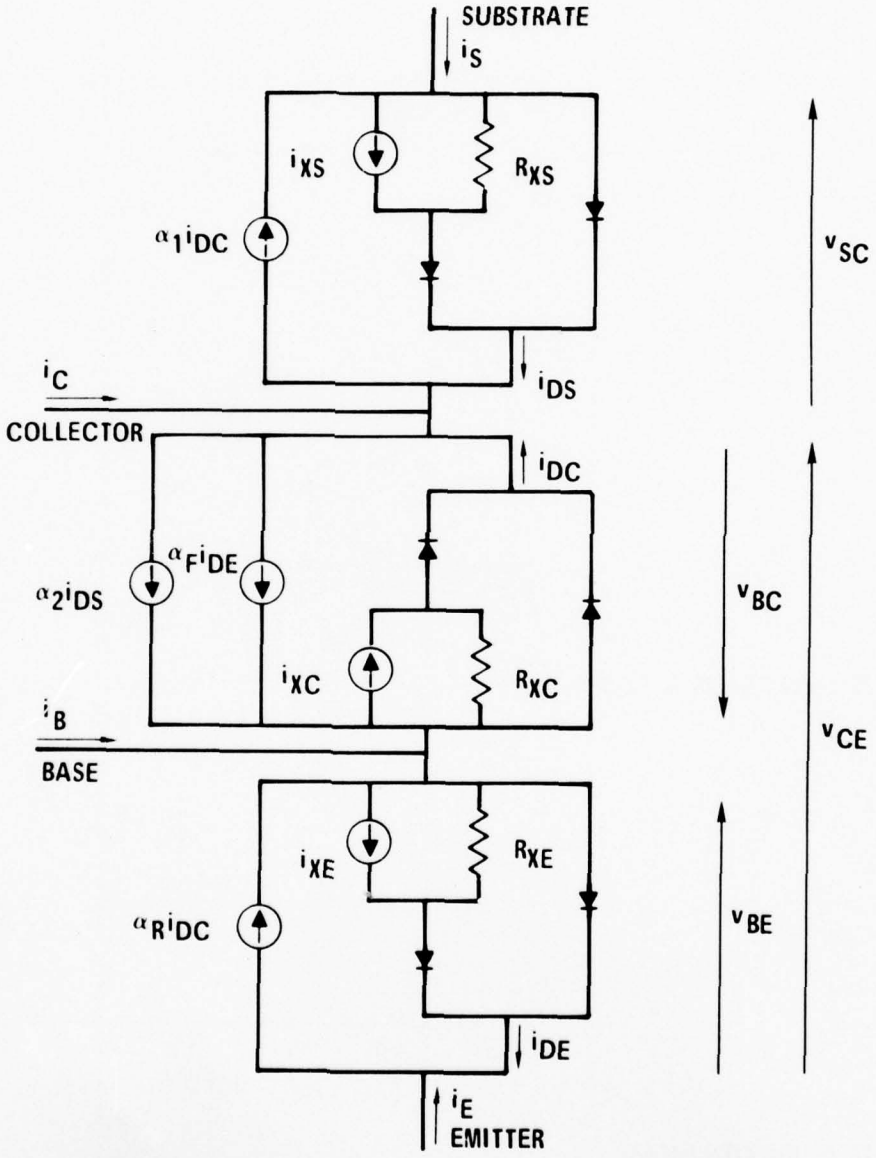


Figure 35 Proposed Model for RF Interference in Four Layer Structures

3.2.6 Comments on Transistor Modeling - The inferred diode curves obtained from a given transistor vary with transistor bias. For example, if the base current is changed, the inferred diode curves may also change. However, for small to moderate changes in transistor bias, the change in inferred diode curves is slight. Therefore, when modeling circuits using the modified Ebers-Moll transistor model (figure 22), the transistor parameters should be obtained at or near the transistor's operating point, for best accuracy.

The parameters R_C, R_E, X_C, and X_E (figure 22) can best be determined through the process described here: using transistor data to infer diode curves, from which the R and X parameters are obtained. However, we can estimate the expected range of these parameters. For the resistors R_C and R_E, lower values are seen at the lower frequencies, where the rectification is greatest; and larger values will occur at high frequencies where the rectification decreases due to diode capacitance.

The parameters X_C and X_E are essentially coupling factors which determine how much RF power is incident on each junction. Based on matching considerations, the expected range of X_C and X_E is from 0 to 1. The value of 0 indicates no RF power incident on the junction, while the value of 1 indicates a matched condition so that the maximum amount of RF power is incident on the junction. Table 4 summarizes the ranges of parameters.

3.3 Modeling RF Effects in Integrated Circuits - The semiconductor models developed earlier can be used to model RF effects in more complex circuits. Of special interest in this report is integrated circuit modeling. Integrated circuits typically contain many devices, including transistors, diodes, resistors, and capacitors, and their analysis can become quite complicated. For this reason, use can be made of any of several available computer programs intended for circuit analysis. These include CIRCUS, CORNAP, ECAP 2, NET 2, SCEPTRE, SLIC and SPICE.

Table 4 Ranges of Parameters in Modified Ebers-Moll Model

	MINIMUM VALUE	MAXIMUM VALUE
R_C	5 Ω*	≈1/ωC − Ω
R_E	5 Ω*	≈1/ωC − Ω
X_C	0	1
X_E	0	1

C = JUNCTION CAPACITANCE

ω = RADIAN FREQUENCY

* = LOWER LIMIT IS SET BY LOSSES IN SYSTEM. VALUE SHOWN IS PROBABLE LOWER LIMIT.

Modeling interference effects in integrated circuits is illustrated using SPICE in this report. The circuit investigated is the 7400 NAND gate, for the case when RF enters the output with the output low. This is its most susceptible configuration. The adaptation of the modified Ebers-Moll transistor model for SPICE is shown, while an RF effects model for the TTL output-low case is developed.

3.3.1 Computer-Aided Analysis of ICs with SPICE - SPICE[10], an acronym for Simulation Program with Integrated Circuit Emphasis, is a versatile, general purpose circuit analysis program. It performs dc analysis, ac analysis, and transient analysis of linear or non-linear electronic circuits. Two versions are in use: SPICE1 has been available since 1972; SPICE2 is an improved version that has been available since 1975. The program is written in FORTRAN IV, and contains approximately 13,000 statements. Versions are available for several large computers, notably the CDC 6400 and the IBM 360. SPICE can be obtained from Prof. D. O. Pederson, c/o University of California at Berkeley, for handling charges only. A time-sharing version, ISPICE, is available commercially from National CSS, Norwalk, Connecticut.

A schematic diagram of the 7400 NAND gate is shown in figure 36. The NAND gate is contained within the dashed box, and consists of 4 transistors (T1, T2, T3, and T4), 3 diodes (D1, D2, and D3), and 4 resistors (R1, R2, R3, and R4). Voltage sources V_{IN} and V_{CC}, and resistors R_L and R_{LL} simulate the external circuitry used in the 7400 NAND gate susceptibility testing. Information on element parameters was obtained from reference 11. The element values were measured from an actual 7400 by probing on the chip. The values obtained for resistors R1 through R4 are listed in table 5. The parameters measured for transistors T1 through T4 were not in a form immediately usable for SPICE, but were converted to a form suitable for SPICE.

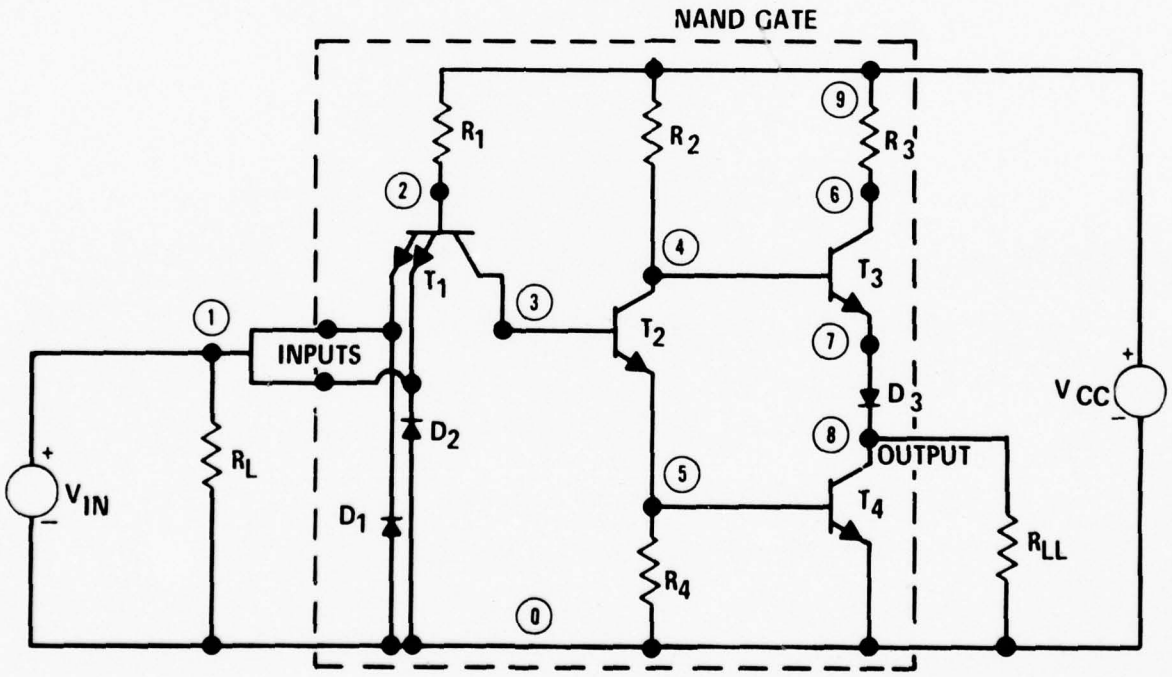


Figure 36 Schematic Diagram of One 7400 NAND Gate With External Connections for Producing Transfer Curves

Table 5 Values of Resistors in 7400 NAND Gate

RESISTOR	VALUE
R1	4.38K Ω
R2	1.43K Ω
R3	0.116K Ω
R4	1.06K Ω

The measured parameters for T1 through T4 are for an Ebers-Moll transistor model as shown in figure 16. The collector and emitter currents are

$$i_C = \alpha_F i_F - i_R \tag{2}$$

$$i_E = \alpha_R i_R - i_F \tag{3}$$

where

$$i_F = [I_{ES}/(1 - \alpha_F\alpha_R)][\exp (qv_{BE}/M_E kT) - 1) \tag{4}$$

$$i_R = [I_{CS}/(1 - \alpha_F\alpha_R)][\exp (qv_{BC}/M_C kT) - 1] \tag{5}$$

where I_{ES} - emitter-base diode saturation current

I_{CS} - collector-base diode saturation current

v_{BE} - base-emitter voltage

v_{BC} - base-collector voltage

α_F - common base normal mode dc current gain

α_R - common base inverted mode dc current gain

q - electron charge

k - Boltzmann's constant

T - junction absolute temperature in °K

M_E - emission constant for emitter-base diode

M_C - emission constant for collector-base diode.

Values for the parameter elements I_{ES}, I_{CS}, α_R, α_F, M_E, and M_C for the four transistors in the NAND gate are summarized in table 6. Also given in table 6 are the diode saturation currents I_{SD} and emission coefficients M_D for the input diodes (D1 and D2 are assumed identical, and are called DIN in table 6), and for diode D3. The dc diode current i_D is given by

$$i_D = I_{SD}[\exp (qv_D/M_D kT) - 1] \tag{6}$$

where v_D - dc voltage across the diode

I_{SD} - diode saturation current

M_D - emission constant for diode.

Table 6 Summary of Ebers-Moll Parameter Values for the 7400 NAND Gate Transistors and Diodes from Reference 9

PARAMETER	T1	T2	T3	T4	DIN	D3
I_{ES} (pA)	2	3	8	20	–	–
I_{CS} (pA)	200	50	100	200	–	–
I_{SD} (pA)	–	–	-	–	100	5
M_E	1.70	1.70	1.67	1.80	–	–
M_C	1.84	1.74	1.80	1.71	–	–
M_D	–	–	–	–	1.64	1.31
α_F	0.24	0.952	0.945	0.956	–	–
α_R	0.0024	0.057	0.076	0.0956	–	–

The simulation program SPICE also has an Ebers-Moll model available for bipolar junction transistors. The SPICE Ebers-Moll model equations for the dc collector current i_C and dc base current i_B of an npn transistor are

$$i_C = I_S[\exp(\frac{qv_{BE}}{kT}) - \exp (\frac{qv_{BC}}{kT})] [1 - \frac{v_{BC}}{V_A}] - \frac{I_S}{\beta_r} [\exp (\frac{qv_{BC}}{kT}) - 1] \tag{7}$$

$$i_B = \frac{I_S}{\beta_f}\left[\exp\left(\frac{qv_{BE}}{kT}\right) - 1\right] + \frac{I_S}{\beta_r}\left[\exp\left(\frac{qv_{BC}}{kT}\right) - 1\right] \quad (8)$$

where q, k, and T have the definitions given previously and

v_{BE} is the base to emitter voltage,

v_{BC} is the base to collector voltage,

β_f is the forward current gain,

β_r is the reverse current gain,

I_S is the saturation current,

V_A is the Early voltage.

The values of I_S, β_f and β_r are supplied by the user. The SPICE Ebers-Moll model also includes parasitic resistances R_E, R_B, and R_C in series with the emitter, base, and collector terminals, respectively. If it is assumed that the Early voltage, V_A, takes on the default value of ∞, and that M_C and M_E equal 1 in equations (4) and (5), and the SPICE equations for i_C and i_B are substituted in equations (2) and (3), where

$$-i_E = i_B + i_C,$$

the following relationships are obtained

$$I_S = [\alpha_F/(1 - \alpha_F\alpha_R)]\, I_{ES} \quad (9)$$

$$\beta_f = \frac{\alpha_{FR}}{1 - \alpha_F} \quad (10)$$

$$\beta_r = \frac{\alpha_F}{1 - \alpha_R}\ . \quad (11)$$

From equations (9) through (11) and the values for I_{ES}, α_F, and α_R given in table 6, the values for I_S, β_f, and β_r were calculated for the four transistors in the 7400 NAND gate. These values are given in table 7. Also given in table 7 are non-zero values for the parasitic series base resistance R_B, and the default values used in SPICE for other transistor parameters which have not been discussed.

Table 7 Parameter Values for the Transistors and Diodes in the 7400 NAND Gate for the SPICE Simulation

PARAMETER	T1	T2	T3	T4	DIN	D3
BF	0.316	19.8	17.2	21.7		
BR	0.0024	0.060	0.082	0.106		
RB	68.	75.	70.	80.		
RC	0	0	0	0		
RE	0	0	0	0		
CCS	0	0	0	0		
TF	0	0	0	0		
TR	0	0	0	0		
CJE	0	0	0	0		
CJC	0	0	0	0		
IS	0.5pA	3.pA	8.pA	20.pA	100.pA	5.pA
PE	1	1	1	1		
PC	1	1	1	1		
VA	∞	∞	∞	∞		
EG	1.11	1.11	1.11	1.11	1.11	1.11
RS					60.	30.
TT					0.	0.
CJO					0.	0.
N					1.	1.
PHI					1.	1.

The procedure for calculating the values of R_B given in table 7 requires some additional explanation. Shown in figure 37 is the emitter-base junction of the Ebers-Moll model (figure 16) and the emitter-base junction of the SPICE Ebers-Moll model shown with the base resistance R_B.

From the SPICE model equations (7) and (8) with $V_A = \infty$ and $qv_{BC}/kT \ll 0$ and assuming $\beta_F \gg 1$, the equation for the dc base-emitter voltage v_{BE} is

$$v_{BE} \simeq (-i_E)\, R_B + (kT/q)\, \ln[-i_E/I_S]. \qquad (12)$$

From equations (2) through (5), assuming $qv_{BC}/kT \ll 0$ and assuming $\beta_f \gg 1$, the dc base-emitter voltage v_{BE} is

$$v_{BE} \simeq (M_E kT/q)\, \ln\,[-i_E/I_{ES}]. \qquad (13)$$

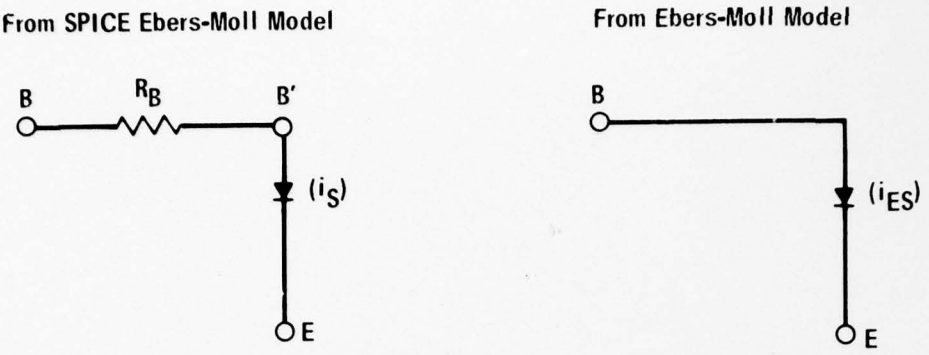


Figure 37 Base-Emitter Junctions of Ebers-Moll and SPICE Ebers-Moll Transistor Models

By equating equations (12) and (13), the following equation is obtained for R_B:

$$R_B = \frac{kT}{q(-i_E)} \left[M_E \ln \frac{(-i_E)}{I_{ES}} - \ln \frac{(-i_E)}{I_S}\right]. \qquad (14)$$

Using the values for M_E, I_{ES} and I_S given in tables 6 and 7, R_B was evaluated at i_E = -5 mA and T = 27°C to obtain the values listed in table 7.

Also listed in table 7 are the diode parameters for diodes DIN and D3. The diode model equation in SPICE is

$$i_D = I_S\left[\exp\left(\frac{qv_D}{nkT}\right) - 1\right] \qquad (15)$$

where i_D and v_D are the diode current and voltage. Setting $I_S = I_{SD}$ and the emission constant, n = 1 (rather than M_D), the values of the diode parasitic series resistance R_S was obtained by using an equation similar to equation (14), which was evaluated at i_D = 5 mA and T = 300°K. The values obtained for R_S are listed in table 7.

The NAND gate operation was tested for normal operation (no RF) by obtaining a dc transfer curve using SPICE. In modeling the NAND gate circuit, figure 36, it was assumed that transistor T1 has only a single emitter, and that diodes D1 and D2 were replaced by a single diode, DIN, in order to simplify the modeling.

Circuit elements are specified in SPICE by numbering the nodes in the circuit and specifying to which node each element is connected along with the element parameters. The node numbers used in the 7400 simulation are shown in figure 36.

As an example of specifying circuit elements, consider resistor R1. The input statement to place R1 in the circuit is

```
R1    9    2    4.38K
```

which tells that resistor R1 is connected between nodes 9 and 2, and that its value is 4.38K ohms. Transistors are inserted with a statement similar to the following statement for T1,

```
QT1    3    2    1    MOD1
```

which indicates that transistor T1 (now only a single emitter transistor) has its collector, base, and emitter connected to nodes 3, 2, and 1 respectively, and that it is of transistor model type "MOD1". A separate statement defines the parameters of each model type. Transistors of type MOD1 are defined by

```
.MODEL    MOD1    NPN    0.316    0.0024    68    IS = 5E - 13
```

which indicates that model MOD1 is an npn transistor with $\beta_f = 0.316$, $\beta_r = 0.0024$, $R_B = 68$ ohms, and $I_S = 5 \times 10^{-13}$ amps. Similar statements are used to insert the other elements used in the model, which includes voltage sources and diodes. See reference 10 for complete information on SPICE input statements.

Figure 38 shows the input statements required to obtain a transfer curve of the NAND gate. Resistors R_L and R_{LL} were set to 200Ω and 9100Ω to agree with their values during testing of the 7400. The dc control card

```
.DC    TC    VIN    0    5    0.05
```

causes the dc input voltage VIN to be stepped from 0 to 5 volts in 0.05 volt steps. The output card

```
.OUT    VOUT    8    0    PRINT    DC    PLOT    DC
```

causes the dc output voltage between nodes 8 and 0 to be printed and plotted versus the dc input voltage VIN between nodes 1 and 0. The SPICE simulation values for V_{OUT} vs V_{IN} are plotted in figure 39. The transfer curve compares favorably with typical curves given by 7400 NAND gate manufacturers.

```
VIN   1  0
VCC   9  0  DC 5
R1    9  2  4.38K
R2    9  4  1.43K
R3    9  6  0.116K
R4    5  0  1.06K
RL    1  0  0.2K
RLL   8  0  9.11K
QT1   3  2  1  MOD1
QT2   4  3  5  MOD2
QT3   6  4  7  MOD3
QT4   8  5  0  MOD4
DIN   0  1     MOD5
D3    7  8     MOD6
• MODEL MOD1 NPN 0.316 0.0024  68  IS = 5E-13
• MODEL MOD2 NPN 19.8  0.060   75  IS = 3E-12
• MODEL MOD3 NPN 17.2  0.082   70  IS = 8E-12
• MODEL MOD4 NPN 21.7  0.106   80  IS = 2E-11
• MODEL MOD5 D  RS = 60  IS = 1E-10
• MODEL MOD6 D  RS = 30  IS = 5E-12
• DC TC VIN  0  5  0.05
• OUTPUT VOUT 8  0  PRINT DC PLOT DC
• TEMP 20
• END
```

Figure 38 Data Cards for Generating DC Transfer Curve for 7400 NAND Gate Using SPICE

3.3.2 Adaptation of Modified Ebers-Moll Transistor for Use with SPICE - When RF energy is conducted into the NAND gate output, with output low, it is postulated that most of the interference effects occur in the output transistor, T4. In this case, the RF energy enters the collector of T4. The RF effects produced can be accounted for in the 7400 model by replacing the output transistor with the modified Ebers-Moll model shown earlier in figure 22.

Examination of transistor T4 on a 7400 chip revealed that it is similar in geometry to a 2N2369A transistor. The modified Ebers-Moll model for RF effects in a 2N2369A was thus chosen to replace transistor T4 in the NAND gate simulation in order to account for RF effects. The modified Ebers-Moll model parameters for

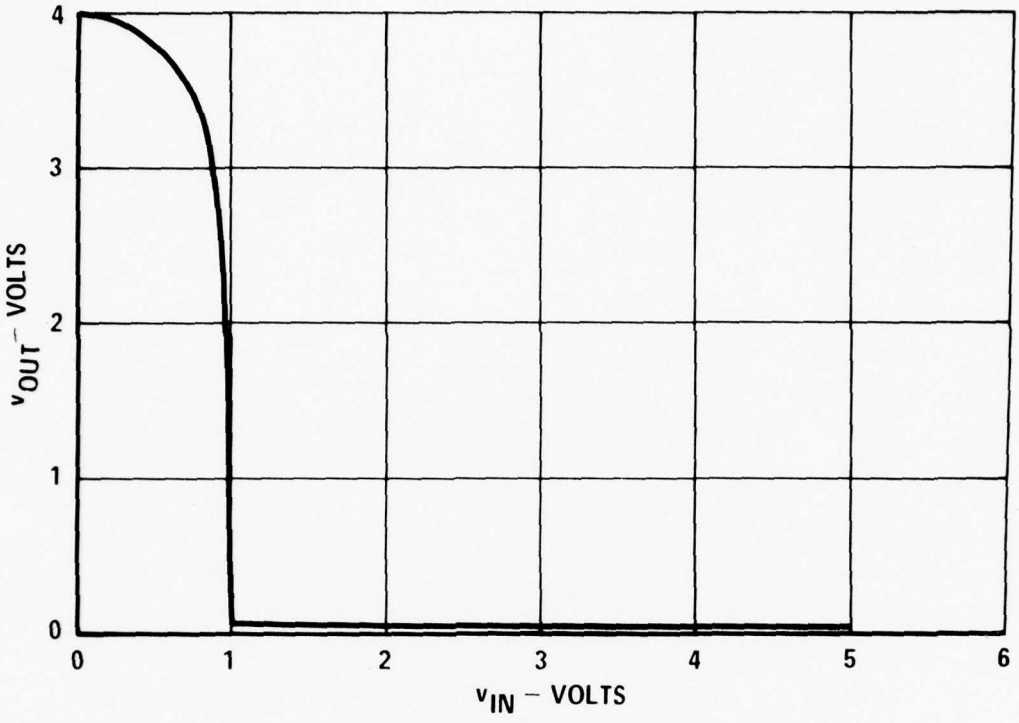


Figure 39 SPICE Simulation of 7400 NAND Gate Transfer Curve

2N2369A were derived earlier, and are listed in table 2. Since the beta of a 2N2369A is much greater than that measured for T4 (94 vs 21.7) the alphas in the 2N2369A used in the model were chosen to be the same as measured for T4, i.e., $\alpha_F = 0.956$ and $\alpha_R = 0.0956$.

The modified Ebers-Moll transistor model shown in figure 22 is a general model which cannot be implemented directly in SPICE. SPICE does not accept current-controlled current sources, so modifications must be made to accommodate the current sources labeled $\alpha_F i_F$ and $\alpha_R i_R$. SPICE does, however, accept voltage-controlled current sources, so the addition of resistors to sense currents i_F and i_R allows the model to be accepted. Figure 40 shows the modified Ebers-Moll model adapted for SPICE by the addition of two 1Ω current-sensing resistors, RCSENSE, and RESENSE.

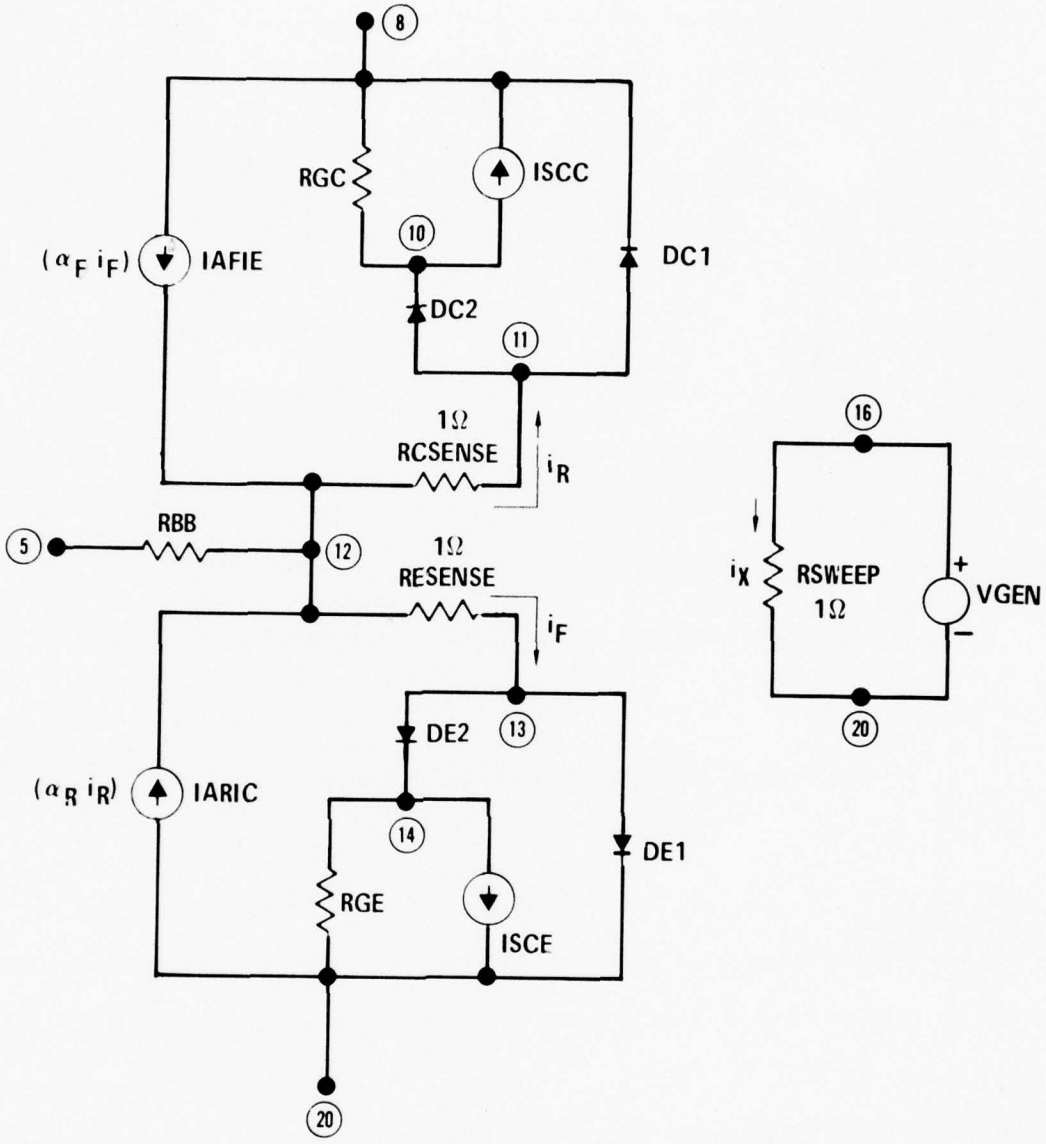


Figure 40 Modified Ebers-Moll Model in an External Model Configuration for SPICE Simulation

The value of 1Ω was chosen because it is small enough that circuit operation is not likely to be upset, and has the additional property that the voltage drop across the resistor is numerically equal to the current flow through it. The voltage-controlled current source IAFIE is entered in the place of $\alpha_F i_F$ with the statement

```
IAFIE    V    8    12    12    13    0.956
```

which indicates that voltage-controlled current source IAFIE is connected between nodes 8 and 12 (referring to the node numbers on figure 40), with positive current defined as flowing through the source in the direction from node 8 to node 12, and with the value given by

$$I = 0.956\ (V_{12} - V_{13})\ \text{amps.}$$

The current source IARIC is entered similarly.

An additional modification can be made if it is desired to find circuit responses as the RF power is swept over a range of values. In Section 3.2.2, it was stated that resistors RGC and RGE (referring to figure 40) remained constant with RF power level, but that ISCC and ISCE varied with RF power level according to the relations

$$ISCC = \frac{X_C}{R_{GC}} \sqrt{8R_g P_{RF}}$$

$$ISCE = \frac{X_E}{R_{GE}} \sqrt{8R_g P_{RF}}\ ,$$

where X_C and X_E are constants,

R_g is the generator resistance,

P_{RF} is the incident RF power.

ISCC and ISCE can be made voltage-controlled current sources if v_{GEN} is defined as

$$v_{GEN} = \sqrt{8R_g P_{RF}}$$

so that

$$ISCC = \frac{X_C}{R_{GC}}\ v_{GEN}$$

and

$$ISCE = \frac{X_E}{R_{GE}}\ v_{GEN}.$$

The voltage v_{GEN} can be swept by SPICE to simulate RF effects over a range of incident RF power levels. In figure 40, VGEN is an independent voltage source

shown to the right of the transistor model. The RF power level as a function of V_{GEN} is given by:

$$P_{RF} = \frac{V_{GEN}^2}{8R_g}. \tag{16}$$

Notice that VGEN and RSWEEP are isolated from the rest of the model, so that their only effect on the model is in controlling current sources ISCC and ISCE.

The current source ISCC, which is now a voltage-controlled current source, is entered with the statement

```
ISCC    V    10    8    16    20    3.79M
```

which indicates that voltage-controlled current source ISCC is connected between nodes 10 and 8 (current flow from node 10 to node 8 through the source), and has the value

$$I = 3.79 \times 10^{-3} (V_{16} - V_{20}) \text{ amps}$$

where

$$V_{GEN} = V_{16} - V_{20}$$

and

$$\frac{X_C}{R_{gc}} = \frac{.72}{190\Omega} = 3.79 \times 10^{-3}\ \Omega^{-1}.$$

Current source ISCE is entered similarly.

Table 8 lists the parameters used in the SPICE adaptation of the modified Ebers-Moll transistor model of the 2N2369A for the 7400 NAND gate simulation.

Table 8 Parameter Values Used in SPICE Adaptation of Modified Ebers-Moll Model of 2N2369A Transistor

Parameter	Value	Parameter	Value
R_{BB} (Ω)	80	X_C	0.72
α_F	0.956	X_E	0.12
α_R	0.0956	R_{gc} (Ω)	190
I_{SE} (pA)	20	R_{ge} (Ω)	180
I_{SC} (pA)	200	X_C/R_{gc}	3.79 millimhos
		X_E/R_{ge}	0.667 millimhos

3.3.3 RF Effects Model for TTL Output-Low Case Using SPICE - A list of the data statements used to simulate the 7400 NAND gate with RF entering the output while it is in a low state are shown in figure 41. Several points are worth mentioning. First, resistors RL and RLL have been changed from those used in generating the transfer curve (see figure 36) to correspond to the external conditions used when RF testing was performed on the 7400 devices. Resistor RL is now between input and power supply, and has a value of 100Ω. This sets the input to a "high" state, which will cause the output to be in a "low" state, under normal conditions. Resistor RL is connected between the output and power supply, and now has the value 300 ohms to simulate the loading of 16 TTL inputs on the output of the gate.

The modified Ebers-Moll transistor parameters are entered as an external model, named RF-EBML. The model is specified at the end of the deck, and is preceded with the card

```
.MODEL    RF-EBML    X    8    5    20    16,
```

which specifies that an external model named RF-EBML which has external nodes numbered 8, 5, 20, and 16 is being made available for use in the circuit. Nodes 8, 5, and 20 correspond to the collector, base, and emitter of the transistor model, while node 16 is part of the circuit which causes the RF power to be swept. The external model is ended with the .FINIS card.

The external model is inserted into the circuit with the statement

```
XT4    8    5    0    15    RF-EBML
```

which indicates that the externally specified device XT4 is connected to circuit nodes 8, 5, 0, and 15, and that its parameters are specified by the external model RF-EBML.

The RF power level is swept with the statement

```
.DC      TC      VGEN      0.2      20      0.2
```

which causes voltage source VGEN to be stepped from 0.2 volts to 20 volts in 0.2 volt steps, so that a transfer curve can be obtained. This corresponds to a range of P_{RF} of 0.1 mW to 1000 mW.

```
VCC 9 0 DC 5
VIN  1 0 DC 4.25
VGEN 15 0
R1 9 2 4.38K
R2 9 4 1.43K
R3 9 6 0.116K
R4 5 0 1.06K
RL 9 1 100
RLL 9 8 300
QT1 3 2 1 MOD1
QT2 4 3 5 MOD2
QT3 6 4 7 MOD3
XT4  8  5  0  15  RF-EBML
DIN  0  1      MOD5
D3  7 8    MOD6
• MODEL MOD1 NPN  0.316 0.0024  68      IS = 5E-13
• MODEL MOD2 NPN   19.8 0.060   75      IS = 3E-12
• MODEL MOD3 NPN   17.2 0.082   70      IS = 8E-12
• MODEL MOD4 NPN   21.7 0.106   80      IS = 2E--11
• MODEL MOD5 D RS = 60  IS = 1E-10
• MODEL MOD6 D RS = 30  IS = 5E-12
• DC TC VGEN 0.2  20  0.2
• OUTPUT VOUT 8 0  PLOT DC  0  5
• TEMP 20
* MDAC RF MODIFIED EBERS-MOLL MODEL
• MODEL RF-EBML X 8  5  20  16
IAFIE V 8 12 12 13 0.956
IARIC V 20 12 12 11 0.0956
RBB 5 12 80
RCSENSE 12  11  1
RESENS E 12  1 3  1
DC1 11  8  MOD7
DE1 13 20 MOD8
• MODEL MOD7 D IS  =  200P
• MODEL MOD8 D IS  =  20P
*RF INDUCED TERMS (ELEMENTS)
RSWEEP 16 20 1
RGC 8 10 190
RGE 14 20 180
ISCC V 10 8 16 20 3.79M
ISCE V 14 20 16 20 0.667M
DC2 11 10 MOD 7
DE2 13 14 MOD8
• FINIS
• END
```

Figure 41 Data Cards for Generating a Plot of v_{OUT} vs v_{GEN}

The results of the 7400 NAND gate simulation are shown in figure 42 compared to measured data for a 7400. The output voltage, V_{OUT}, is plotted as a function of RF power incident on the output. The shape of the curve is the same as that for the measured case, although the SPICE simulation predicts a higher output voltage at high levels of RF power than is actually measured. This may occur because all of the RF power was assumed to be incident on the output transistor. This assumption is conservative, however, since it is unlikely that all of the RF power incident on the output will reach the output transistor. RF impedance mismatches will result in some power being reflected, and of that being absorbed, some will be absorbed by other elemerts within the integrated circuit besides the output transistor.

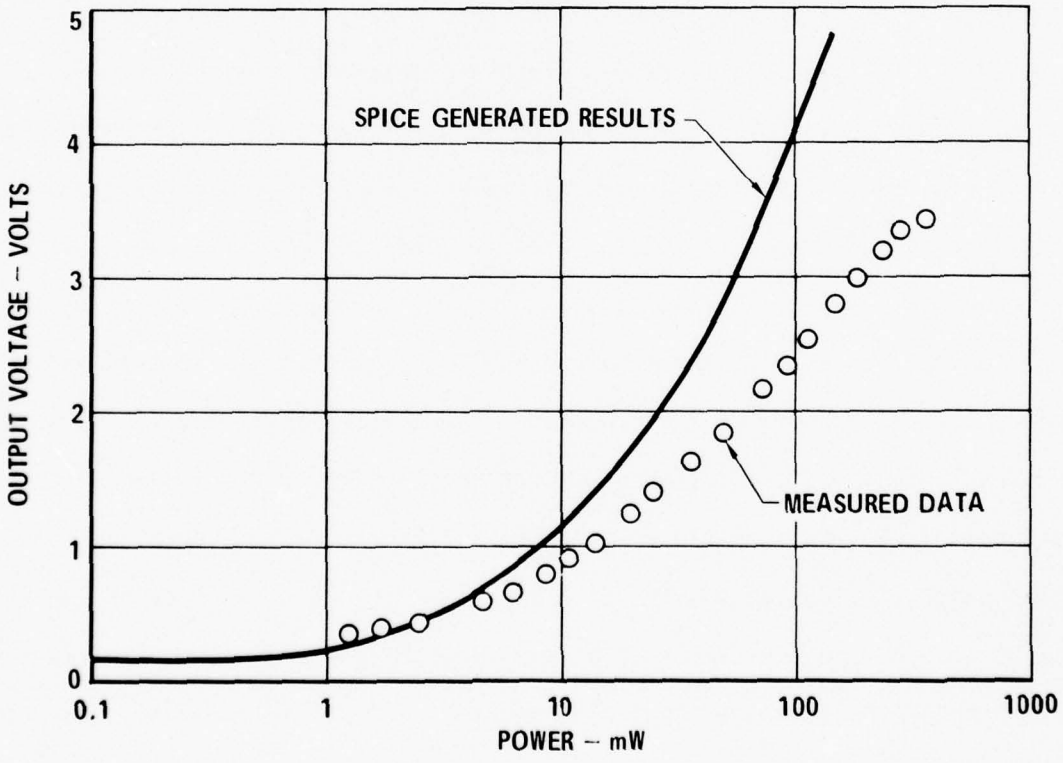


Figure 42 Comparison of SPICE Simulation of 7400 NAND Gate to Measured Results

A more elaborate worst-case analysis can be performed if one considers the ranges of R_C, R_E, X_C, and X_E given in table 4. These parameters can be allowed to vary anywhere over their range, with the purpose of finding the combination which will give the worst-case V_{OUT} vs RF power curve. This worst-case curve can be assumed to be worse than anything that will be observed in practice, and can be used to determine design specifications.

3.4 Measurements of RF Susceptibility in a Line Driver/Line Receiver Pair - Line driver/receiver pairs are of special interest to the IC susceptibility investigation since, for many systems, they represent the major interface between subsystem boxes and, hence, can be expected to be exposed to RF power conducted in on the system interconnect wires. There are many similarities between the circuit design of line drivers and TTL gates; likewise, line receivers bear some resemblance to comparators on the input and TTL gates on the output. Hence there are reasons to believe that line driver/receiver susceptibilities may be estimated from observed susceptibilities of devices with similar circuitry and the modeling techniques described previously may be applied to this class of devices. Because of their importance, a separate look at their susceptibility properties was deemed necessary.

Table 9 lists the measured RF levels at 220 MHz required to produce interference in the 9614/9615 pair. The interference effect is a complete state change in the output as shown in the typical plots of figures 43 and 44. These data are not inconsistent with previous data taken on TTL gates. The relative lack of sensitivity in the input of the line receivers can be explained by the presence of rather large resistors which are between the input pins and the differential pair of transistors.

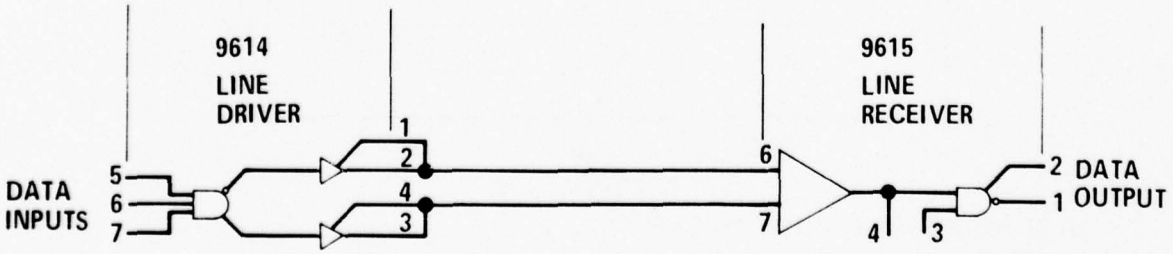
Table 9 RF Susceptibility Characteristics of Line Driver/Line Receiver at 220 MHz

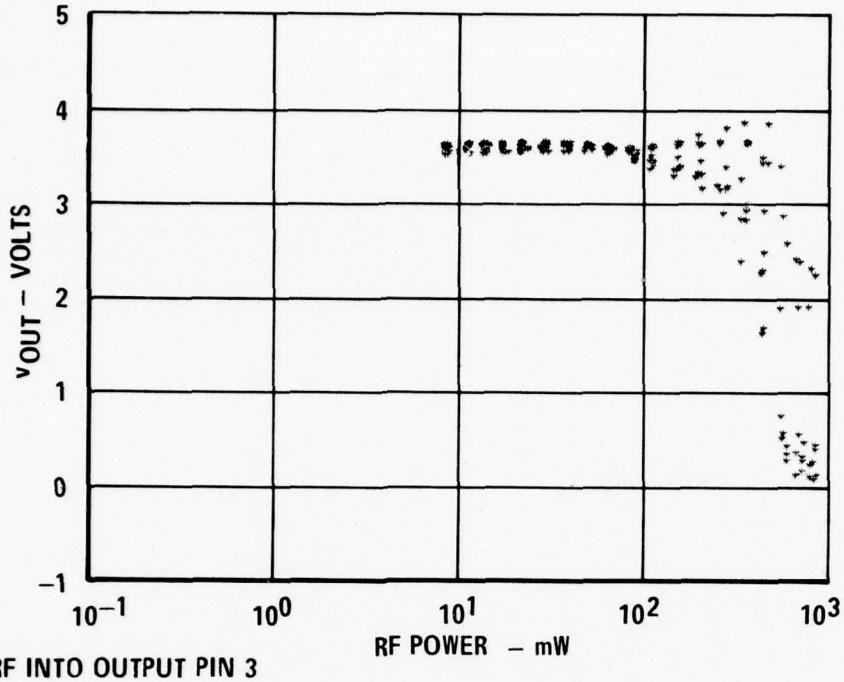
9614 (LINE DRIVER)

RF INJECTION PORT	RF POWER REQUIRED TO PRODUCE STATE CHANGE IN RECEIVER OUTPUT
ACTIVE PULLUP (PIN 1)	> 566 mW
OUTPUT (PIN 2)	> 566 mW
OUTPUT (PIN 3)	464 mW
ACTIVE PULLUP (PIN 4)	175 mW
INPUT (PIN 5)	54 mW
INPUT (PIN 6)	41 mW
INPUT (PIN 7)	41 mW

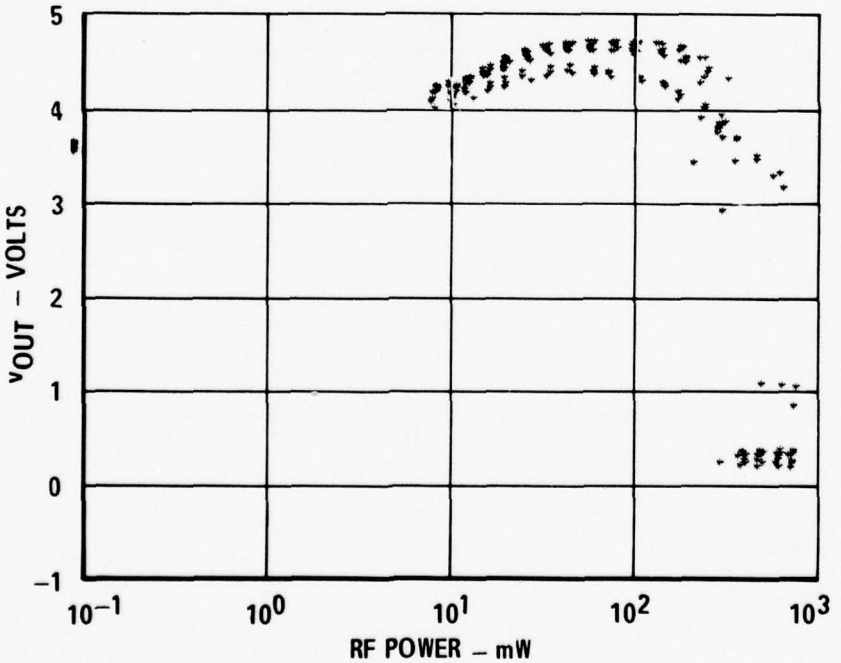
9615 (LINE RECEIVER)

RF INJECTION PORT	RF POWER REQUIRED TO PRODUCE STATE CHANGE IN RECEIVER OUTPUT
OUTPUT (PIN 1)	68 mW
ACTIVE PULLUP (PIN 2)	216 mW
STROBE (PIN 3)	120 mW
RESPONSE CONTROL (PIN 4)	13 mW
INPUT (PIN 5)	> 566 mW
INPUT (PIN 6)	> 566 mW
INPUT (PIN 7)	> 566 mW





a) RF INTO OUTPUT PIN 3



b) RF INTO OUTPUT ACTIVE PULL-UP
PIN 4

Figure 43 Plots of V_{OUT} VS RF Power for the 9614 Line Driver with 220 MHz Conducted into Two Different Pins

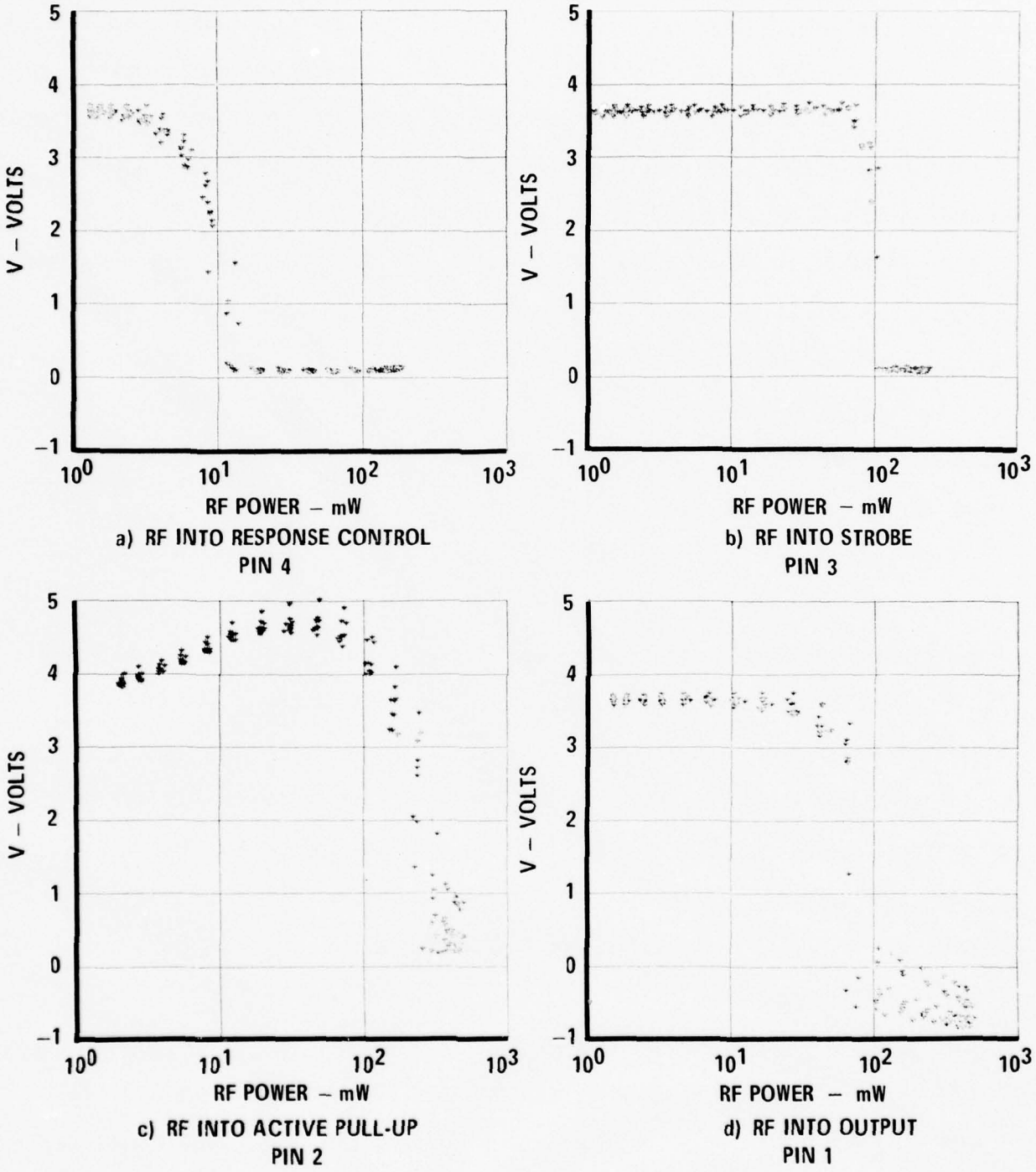


Figure 44 Plots of v_{OUT} VS RF Power for the 9615 Line Receiver with 220 MHz Injected into Four Different Pins

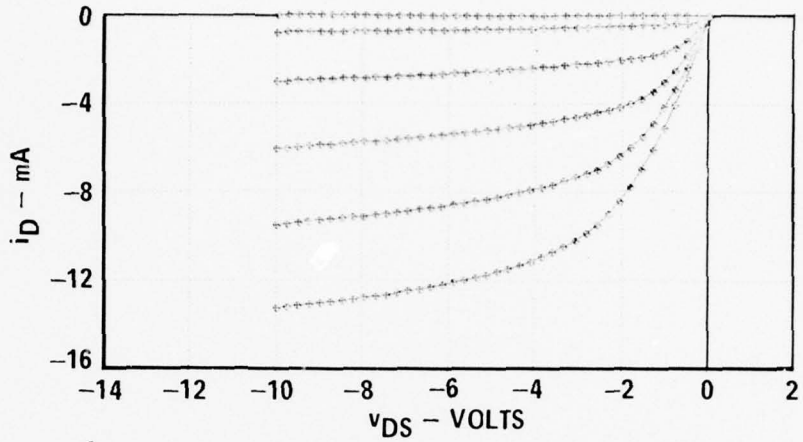
3.5 RF Effects in MOSFETs - Like their bipolar counterparts, MOSFETs are also affected by RF. The pn junctions which are formed at the drain-to-substrate and source-to-substrate interfaces are rectification sites for RF just as the bipolar transistor junctions are. The observed RF effects in MOSFETs will be shown here as well as a preliminary model to explain this behavior.

3.5.1 RF Effects in MOSFETs Without Parasitic and Protective Junctions - When RF energy is conducted into the drain of an n-channel or p-channel MOSFET, the i_D vs v_{DS} characteristic curves change. This effect is similar to the RF effects seen in junction diodes and bipolar transistors. Rectification, which was the mechanism in the case of transistors and diodes, is also the mechanism of the interference in MOSFET devices.

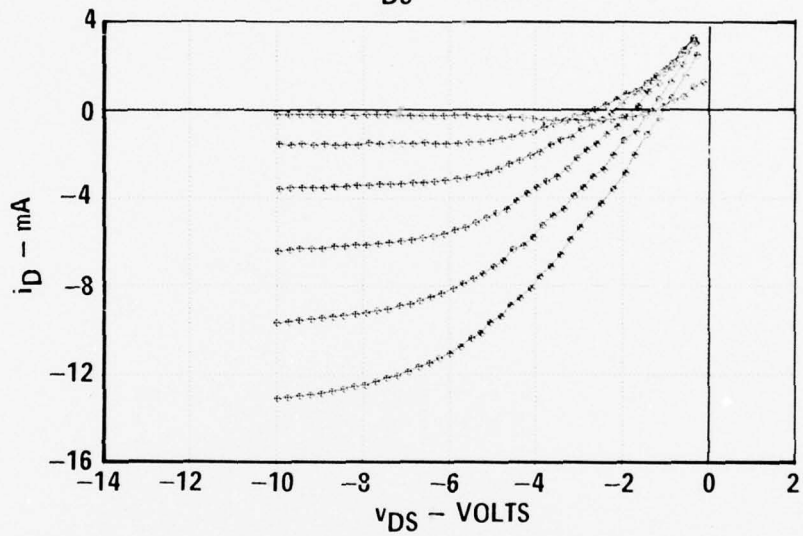
The i_D vs v_{DS} curves for an MFE 3003 p-channel MOSFET are shown in figure 45 for the cases where no RF, 110 mW and 220 mW of RF power are entering the drain. The currents and voltages are labeled as shown in the diagram of figure 46. As the RF power increases, the drain current becomes less negative, especially at the higher drain-to-source voltages.

Figure 47 shows corresponding curves for an MFE 3002 n-channel MOSFET for the cases where no RF, 95 mW and 175 mW of RF are entering the drain. The device currents and voltages are again labeled as in figure 46. As the RF power increases, the drain current decreases drastically at low v_{DS}, but increases slightly at high v_{DS}.

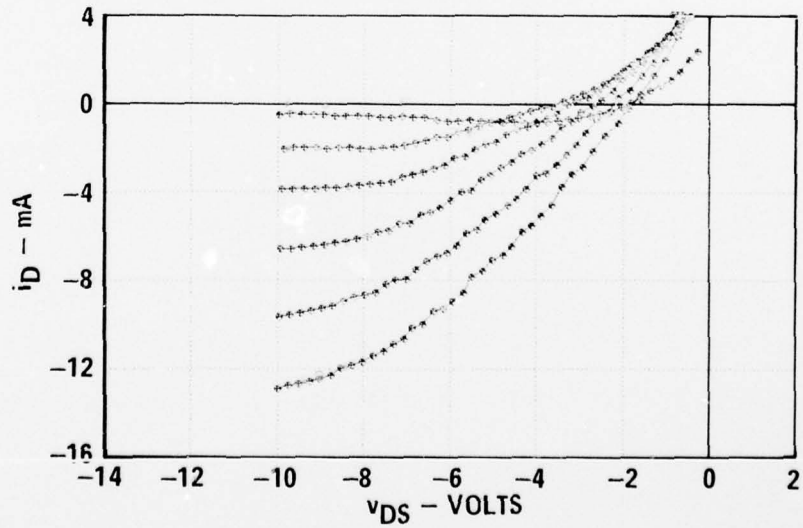
3.5.2 Model of RF Effects in P-Channel MOSFETs Without Parasitic and Protective Junctions - A simplified picture of p-channel MOSFET construction is shown in figure 48. The p-type drain and source are diffused into the n-type substrate, and the p-type channel is field-induced by the voltage on the insulated gate which allows current flow between drain and source. The diode junctions between



a) NO RF



b) 110 mW RF POWER



c) 220 mW RF POWER

Figure 45 Measured MFE 3003 MOSFET Characteristic Curves with 220 MHz Conducted into Drain (v_{GS} = 0, −4, −5, −6, −7, −8 Volts)

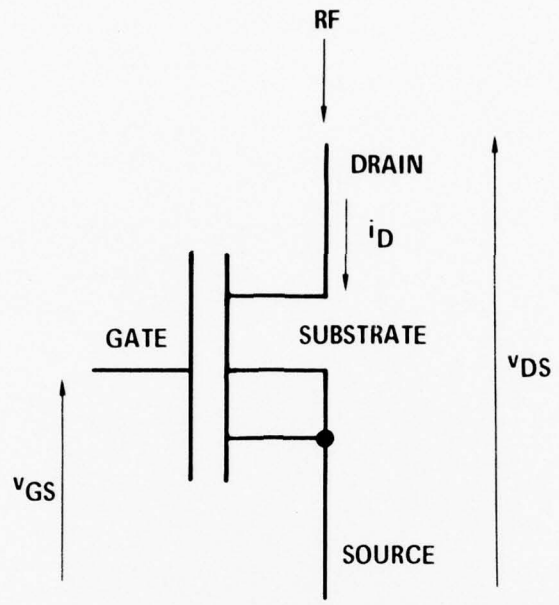
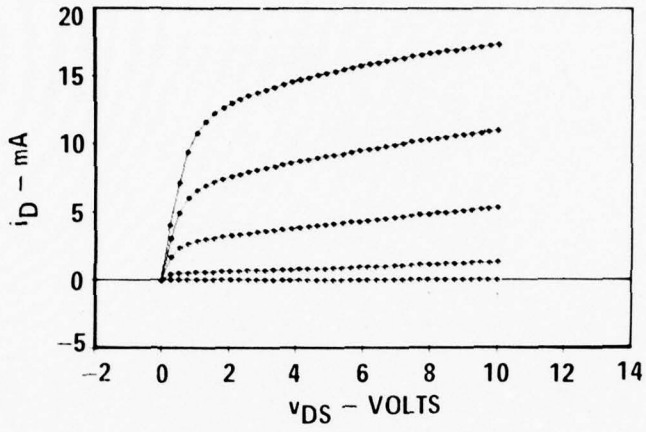


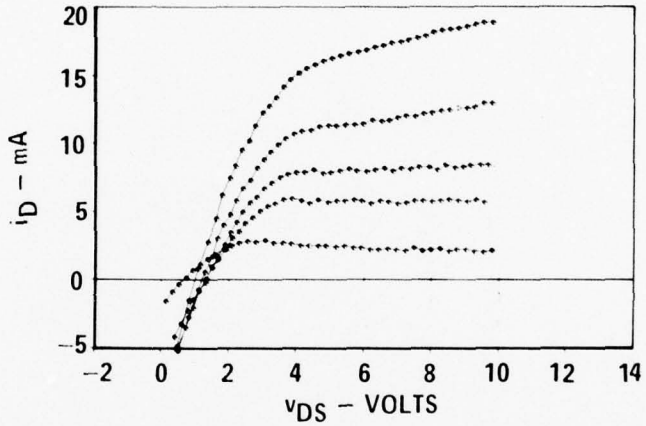
Figure 46 **MOSFET Test Setup for RF Conducted into Drain (P and N-Channel)**

the drain and substrate, and source and substrate, are normally not forward biased so current does not flow into the substrate.

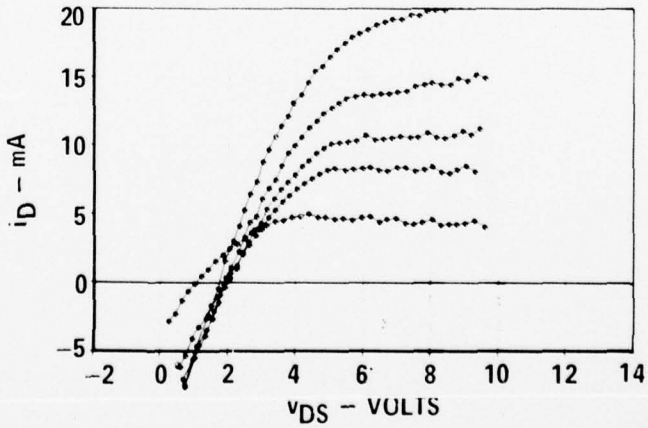
A simplified model of the p-channel MOSFET shown in figure 49 shows its major features. The channel current is represented by a current source which is a function of the gate-source and drain-source voltage. In the computer circuit analysis program SCEPTRE[6], which assumes that the source and substrate are at the same potential, the channel current is given by:



a) NO RF



b) 95mW RF POWER



c) 175mW RF POWER

Figure 47 Measured MFE 3002 MOSFET Characteristic Curves with 220 MHz Conducted into Drain (v_{GS} = 0, 3, 4, 5, 6 Volts)

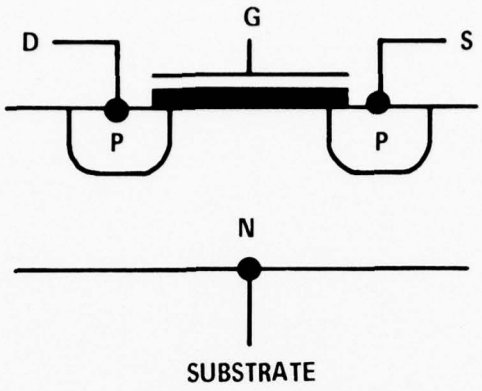


Figure 48 Simplified Construction Details of P-Channel MOSFET

$$J = J_D - \frac{V_{DS}}{I_T R_0} (J_D + K)$$

where

$$J_D = \begin{cases} \frac{B}{2}\{v_{GS}^2 - v_{GD}^2 - 2\,V_T(v_{GS} - v_{GD})\} & \text{triode region} \\ \quad \text{for } V_T \geq v_{GS} \text{ and } V_T \geq v_{GD} & \\ \frac{B}{2}(v_{GS} - V_T)^2 & \text{pinch-off region} \\ \quad \text{for } V_T \geq v_{GS} \text{ and } V_T \leq v_{GD} & \\ -\frac{B}{2}(v_{GD} - V_T)^2 & \text{inverted region} \\ \quad \text{for } V_T \leq v_{GS} \text{ and } V_T \geq v_{GD} & \\ 0 & \text{cut-off region} \\ \quad \text{for } V_T \leq v_{GS} \text{ and } V_T \leq v_{GD} & \end{cases}$$

V_T is the threshold voltage (negative),

and B, I_T, R_0 and K are constants.

Other representations for the channel current are found in references 10, 12 and 13.

The diagram of figure 49 also shows the parasitic diodes between the drain and substrate, and source and substrate.

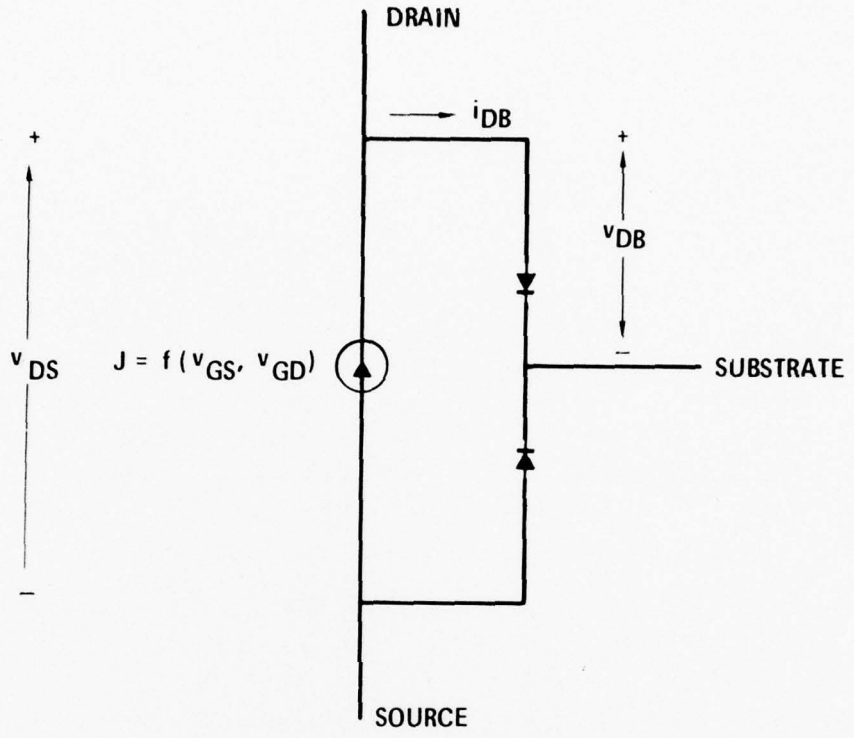


Figure 49 Model of MOSFET for Normal Operation

In the MOSFET, rectification can occur in the drain-substrate and source-substrate junctions. It is necessary to model the rectification in the junctions in order to model the RF effects in the device. For the MFE 3003 p-channel MOSFET, the rectification curves for the drain-substrate and source-substrate junctions were inferred using a method similar to that used to infer rectification curves for transistor junctions in Section 3.2.2. A simplification occurs for this case (shown in figure 46), where the source and substrate are at the same potential and RF energy enters the drain, because the primary rectification effect occurs in the drain-substrate diode, so that it becomes possible to model only the

rectification in that junction. Figure 50 shows the rectification curves for the drain-substrate junction for RF powers of 110 and 220 mW. The rectification also depends on the gate-to-source voltage, so the curves are shown for v_{GS} = -4 and -8 volts.

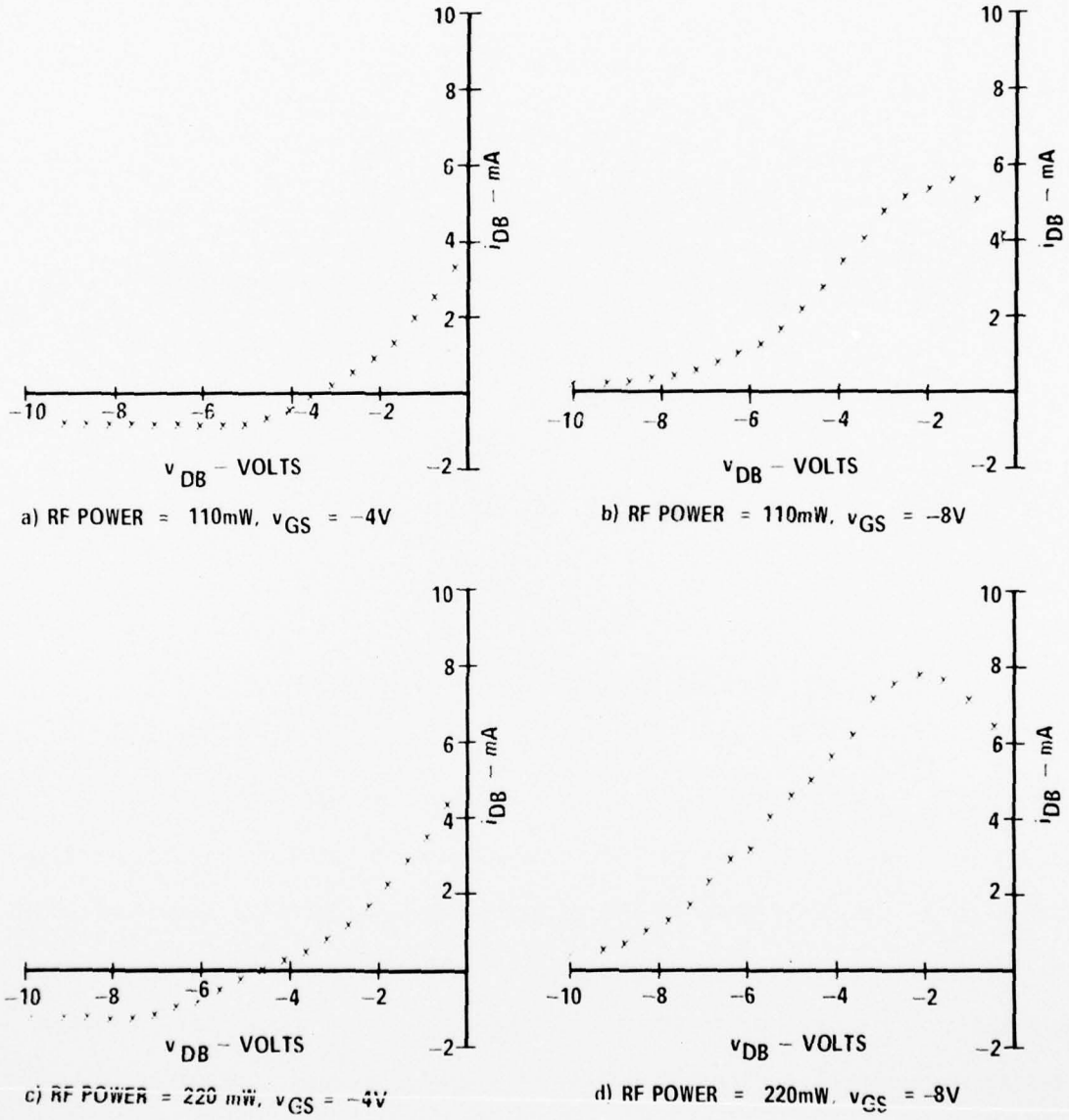


Figure 50 Simulated Drain-to-Substrate Junction Rectification Curves for MFE 3003 P-Channel MOSFET With 220 MHz Conducted into Drain

In the rectification curves of figure 50, note that all four cases show the general positive-slope characteristics typical of diode rectification curves. For the case where v_{GS} = -4V, reverse currents are rather high, approximately 1 mA. For the case where v_{GS} = -8V, the diode current decreases at high diode voltages, in a form not typical of rectification curves. These anomalies may indicate the presence of coupling between drain and source, or between channel and drain or source, or may be due to some other interaction in the device. Ignoring these effects, it is possible to model the rectification curves using the method shown earlier in figures 19 and 20 for diodes.

Figure 51 shows a MOSFET model for RF entering the drain, where the drain-to substrate diode has been modified to include rectification. Diode D1 is equivalent to the normal drain-substrate diode, and for simplicity, diode D2 is also assumed equivalent. Resistor R_X and current source i_X determine the interference characteristics of the device. Both are obtained from plots of rectification in the diode. From figure 19, $1/R_X$ is the slope of the rectification region to the left of the diode's normal turn-on voltage. The value of i_X is given by

$$i_X = \frac{V_{DIFF}}{R_X} = \frac{V_{TURN\text{-}ON} - V_{OC}}{R_X}$$

Resistor R_X is found to be approximately constant, and independent of the RF power level. The value of i_X is a function of the RF power level, and has also been found to be a function of the gate-to-source voltage. This effect may be due to the electric field in the substrate caused by the gate voltage. A relation that accounts for the dependence of v_{DIFF} on v_{GS} is:

$$v_{DIFF} = \begin{cases} C_1 + C_2 (V_T - v_{GS}) & \text{if } V_T \geq v_{GS} \\ C_1 & \text{if } V_T \leq v_{GS} \end{cases}$$

where C_1 and C_2 are coefficients dependent on the RF power level.

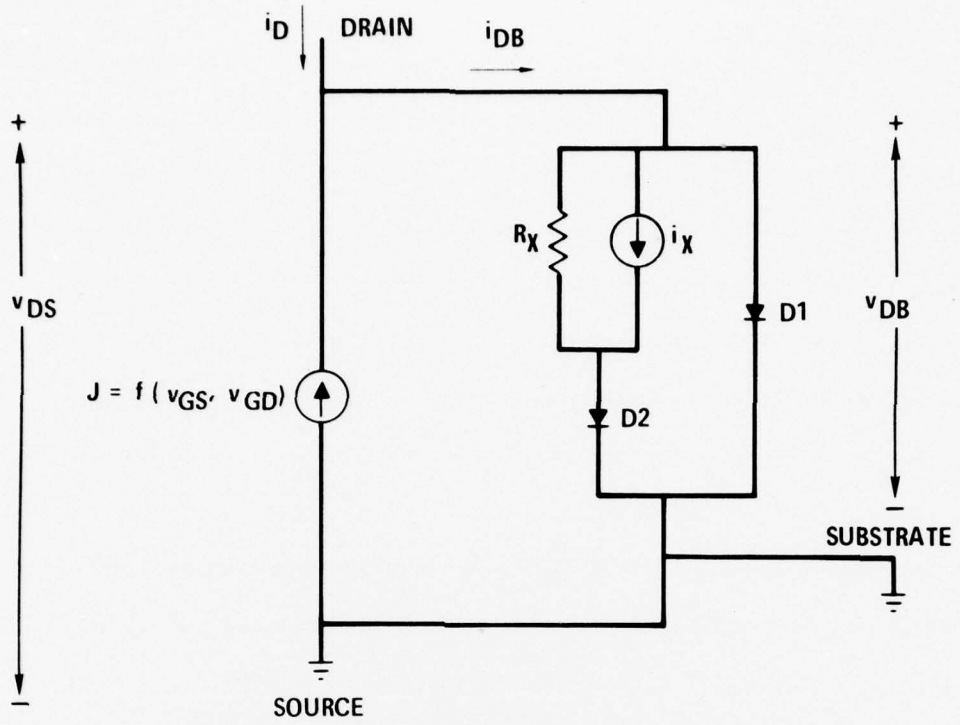
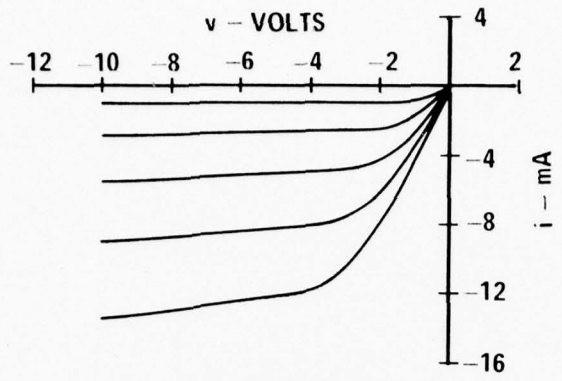


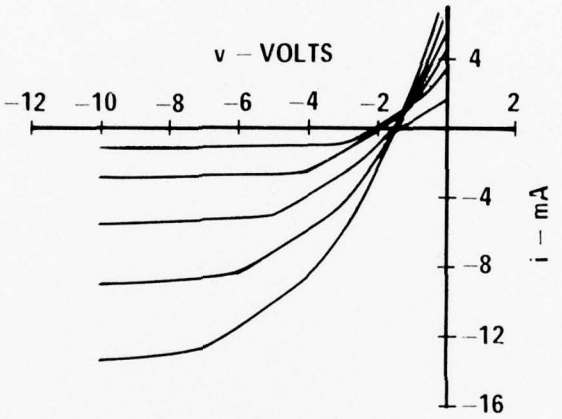
Figure 51 Proposed P-Channel MOSFET Model for RF Conducted into the Drain

In order to model the interference effects in the MFE 3003 MOSFET, first the no RF case was modeled to obtain an adequate model for normal operation, then the additional elements were added to account for rectification in the drain-substrate diode. A model similar to that used in SCEPTRE was used to calculate the i_D vs v_{DS} curves shown in figure 52a.

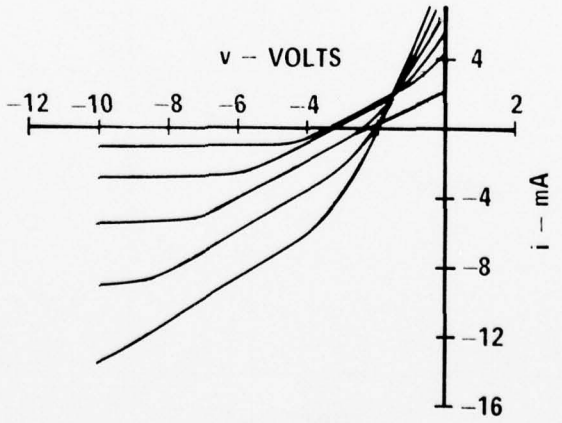
To account for rectification in the drain-substrate diode, the model shown in figure 51 was used. Diodes D1 and D2 were modeled as silicon diodes with turn-on voltages of 0.7 volt. R_X was determined from diode rectification plots to be approximately 1000 ohms. The values of C_1 and C_2 were also determined from diode rectification plots, and are graphed as functions of RF power in figure 53. The threshold voltage, V_T, was determined from the no RF case to be approximately -2.4 volts. Figures 52b and 52c show the i_D vs v_{DS} curves calculated from the MOSFET model at 110 mW and 220 mW of RF power on the drain. The agreement with the measured curves of figures 45b and 45c is good.



a) NO RF POWER

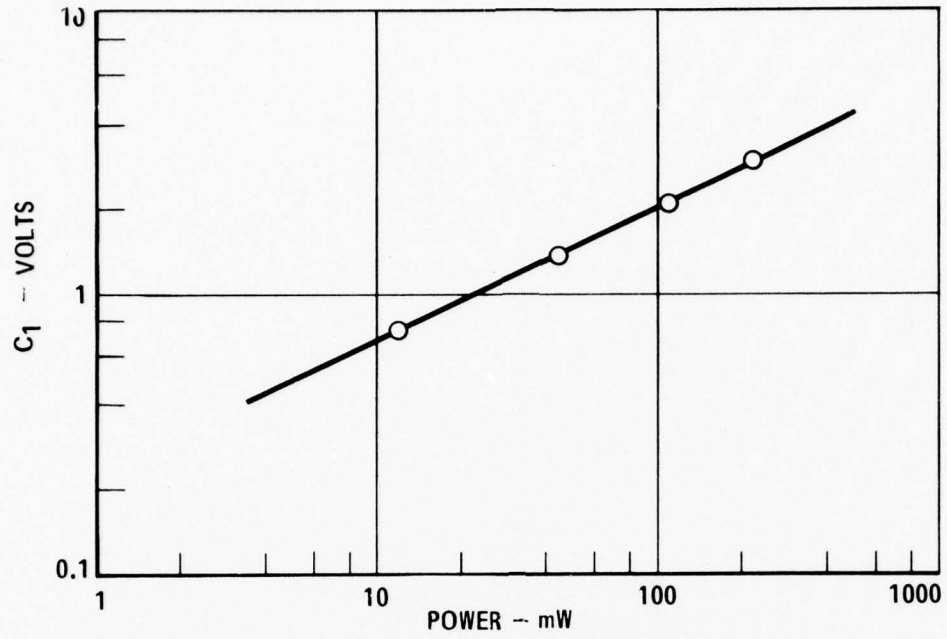


b) 110 mW RF POWER

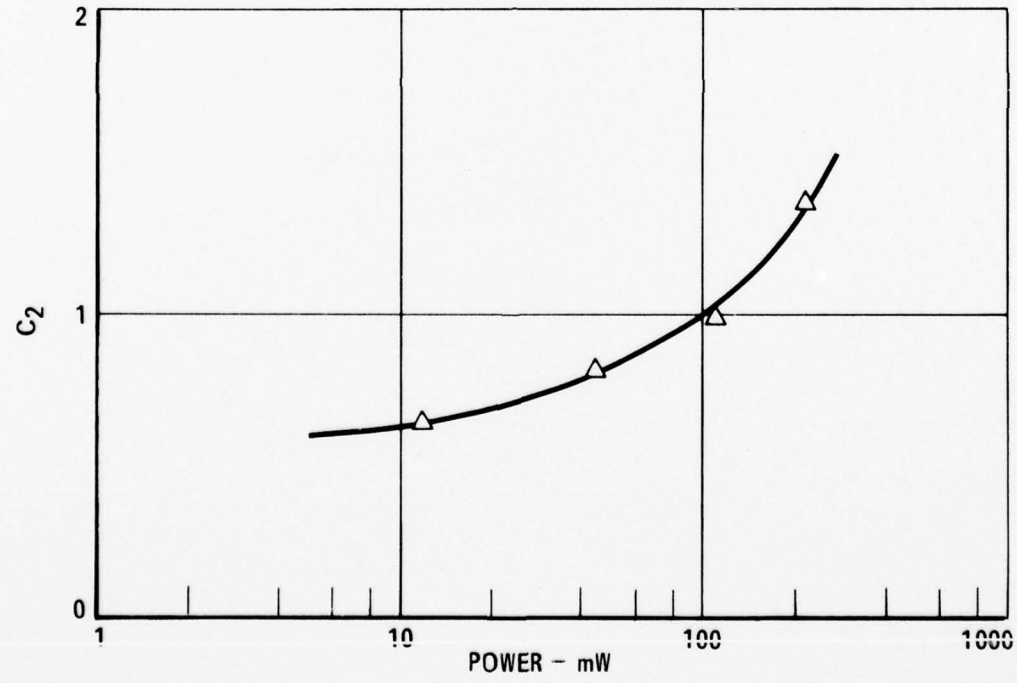


c) 220 mW RF POWER

Figure 52 Simulation of MFE 3003 P-Channel MOSFET Characteristic Curves with 220 MHz RF Power Conducted into Drain (v_{GS} = 0, –4, –5, –6, –7, –8 Volts)



a) C_1 vs RF Power Conducted into Drain



b) C_2 vs RF Power Conducted into Drain

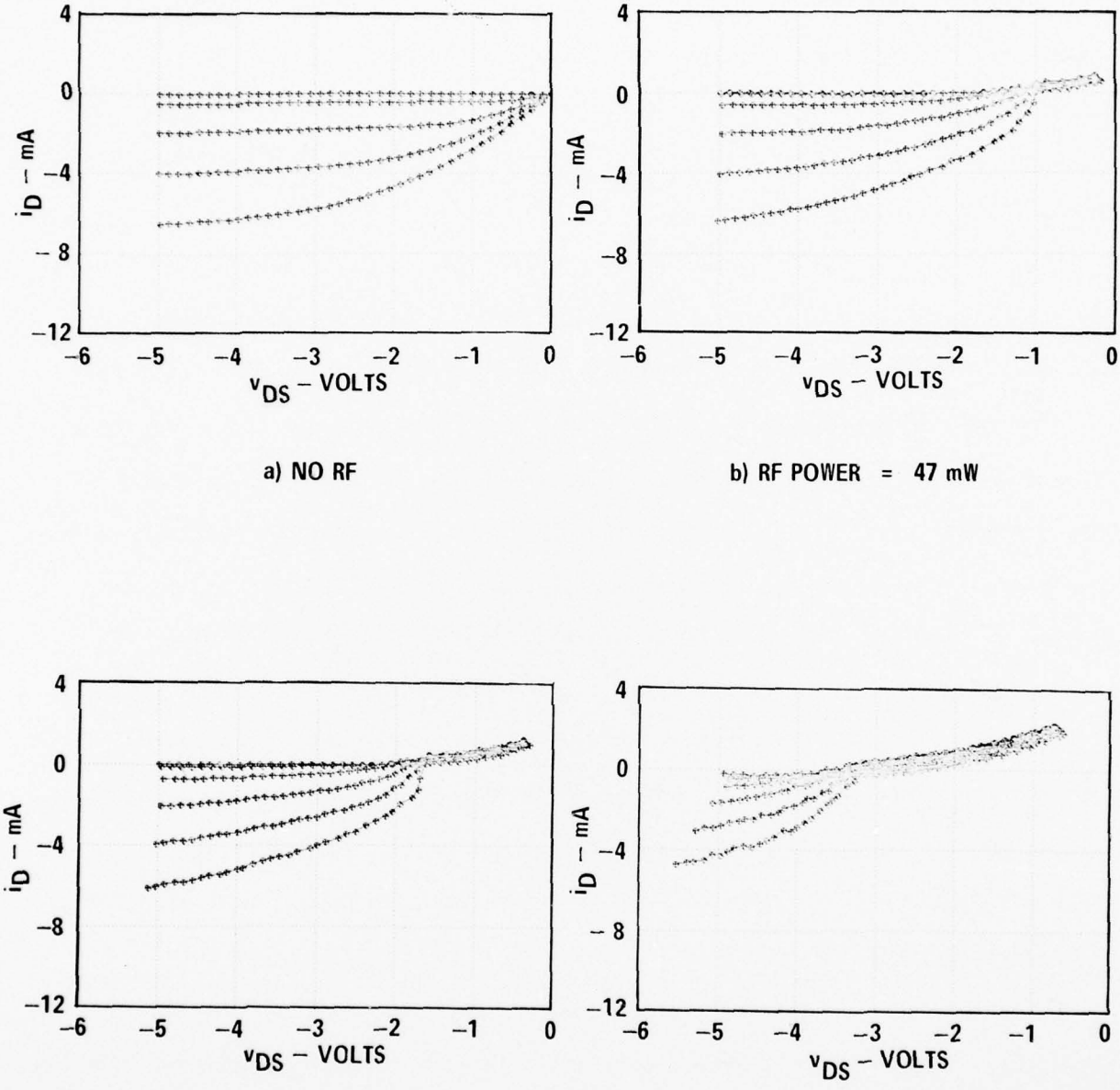
Figure 53 Constants C_1 and C_2 for MFE 3003 P-Channel MOSFET With 220 MHz Conducted Into Drain

3.5.3 RF Effects in CMOS FETs With Parasitic and Protective Junctions - There are differences between regular MOSFETs and FETs in a CMOS IC. One difference is the use of an n-type substrate in CMOS so that n-channel devices must be located in a p-well which forms a parasitic diode in the substrate. Another difference is the addition of a protective resistor and diode combination to the gate circuitry in some CMOS devices to protect the gate oxide from static electricity.

Since the RF rectifies in pn junctions, these additional junctions are paths for the RF and the RF-generated currents to flow. These additional paths have been observed under RF testing. The observed currents in these junctions cause the CMOS FETs to behave slightly differently from the simple MOSFETs. Figure 54 shows the FET characteristics for three power levels and the no RF case for the CMOS p-channel FET. Figure 55 also shows the FET characteristics for three power levels and the no RF case for the CMOS n-channel FET. While these curves are similar in shape to the simple MOSFET curves, there are differences under RF stimulus which are caused by the parasitic and protective diode paths. Further investigation of these effects will be carried out in the next increment.

3.6 RF Effects Model for Bipolar Op Amps - During this increment the available data on bipolar op amps have been studied in more detail. In reference 4 an input offset generator model for op amps was presented. It will be repeated here with additional supporting data.

Referring to a typical interference data listing for a 741 op amp (as in table 10), it is readily observed that the voltage at the inverting input terminal, v_{II}, varies significantly with the applied RF signal. In normal operation, this voltage is very near zero volts (a "virtual ground") due to the negative feedback used in a typical circuit application. Modeling the non-ideal performance of the amplifier under interference conditions as an ideal differential amplifier with a



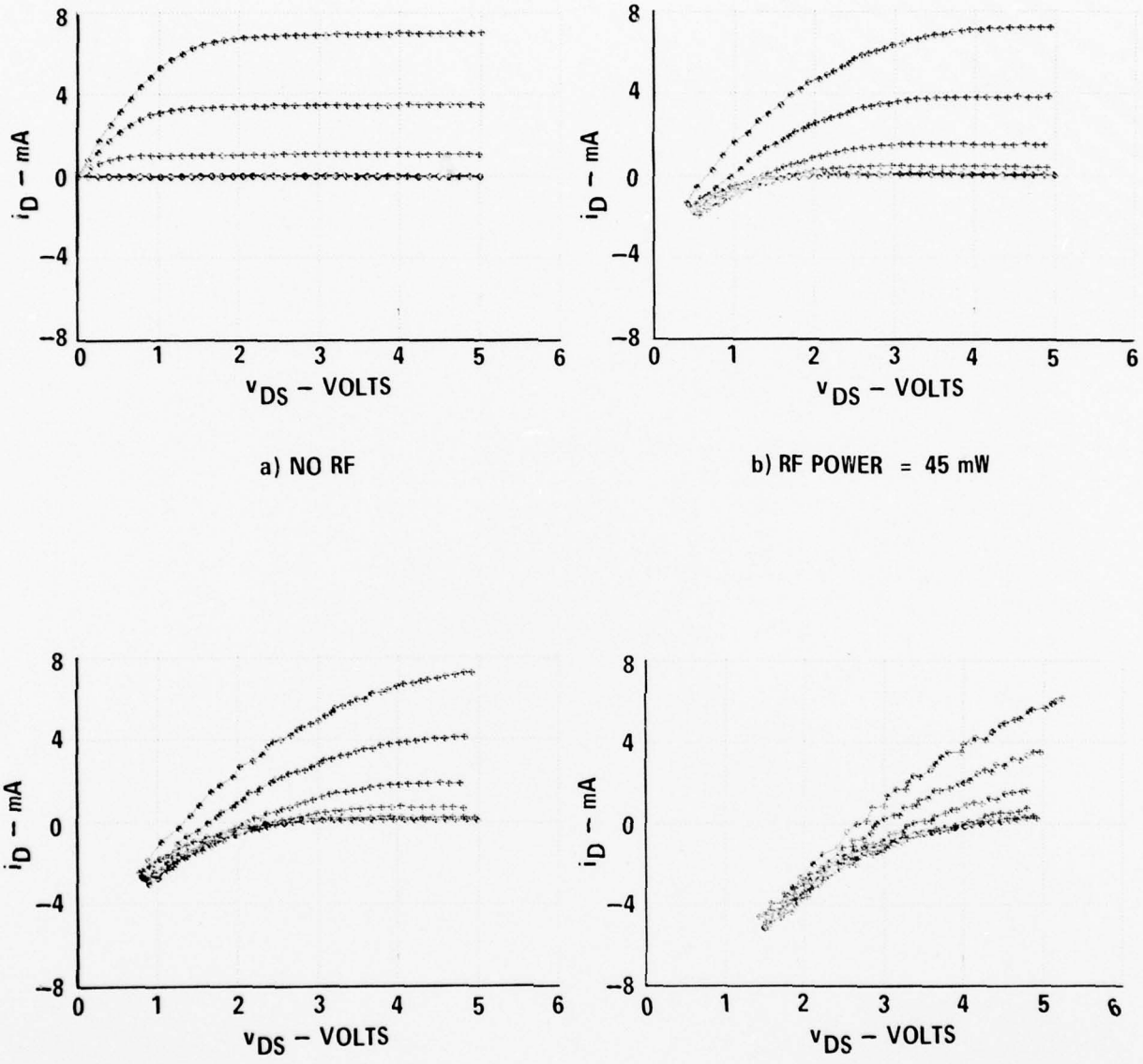
a) NO RF

b) RF POWER = 47 mW

c) RF POWER = 90 mW

d) RF POWER = 300 mW

Figure 54 Measured Curves for P Channel MOSFET from CMOS 4007B with 220 MHz Conducted into the Source



a) NO RF

b) RF POWER = 45 mW

c) RF POWER = 88 mW

d) RF POWER = 220 mW

Figure 55 Measured Characteristic Curves for N-Channel MOSFET from CMOS 4007B with 220 MHz Conducted into the Drain

Table 10 Example of 741 Interference Susceptibility Data
S/N = 120

P (mW)	C.F. (dB)	VOUT	IOUT	VNI	INI	VON2	ION2	VON6
0.000	0.00	−4.896	9.79	−0.00	0.0000	−11.84	0.0292	−11.84
0.093	9.42	−6.366	12.73	−0.00	0.0001	−11.80	0.0368	−11.81
0.148	8.83	−6.521	13.04	−0.00	0.0001	−11.79	0.0382	−11.80
0.191	9.86	−6.781	13.56	−0.00	0.0001	−11.79	0.0390	−11.79
0.442	7.64	−7.340	14.68	−0.00	0.0001	−11.77	0.0408	−11.78
0 600	7.70	−7.544	15.09	−0.00	0.0001	−11.77	0.0422	−11.77
1.225	6.61	−7.542	15.08	−0.00	0.0001	−11.76	0.0438	−11.77
1.310	7.04	−7.635	15.27	−0.00	0.0001	−11.75	0.0454	−11.77
2.310	6.60	−7.435	14.87	−0.00	0.0001	−11.72	0.0516	−11.78
3.675	7.27	9.647	−19.29	0.00	−0.0001	−11.82	0.0352	−11.97
4.611	6.79	9.599	−19.20	0.00	−0.0002	−11.79	0.0412	−11.97
9.098	6.13	9.249	−18.50	0.00	−0.0001	−11.62	0.0758	−11.93
15.719	5.39	9.192	−18.38	0.00	−0.0002	−11.49	0.1016	−11.89
23.724	4.87	9.151	−18.30	0 00	−0.0002	−11.41	0.1174	−11.86
34.675	4.50	9.005	−18.01	0 00	−0.0001	−11.34	0.1314	−11.86
53.610	4.22	8.748	−17.50	0 00	−0.0001	−11.24	0.1526	−11.84
83.830	4.35	8.421	−16.84	0.00	−0.0001	−11.08	0.1830	−11.82
124.458	4.40	7.907	−15.81	0.00	−0.0001	−10.97	0.2048	−11.77
181.475	4.66	7.139	−14.28	0.00	−0.0001	−10.90	0.2198	−11.67
214.113	4.72	6.668	−13.34	0.00	−0.0001	−10.87	0.2262	−11.61

P (mW)	ION6	VCC+	ICC+	VCC−	ICC−	VII	III
0.000	−0.0294	11.99	0.90	−11.87	−11.50	0.0027	0.4910
0.093	−0.0350	11.99	0.90	−11.83	−11.80	0.1303	0.6239
0.148	−0.0364	11.99	0.90	−11.83	−15.10	0.1404	0.6340
0.191	−0 0374	11.99	0.90	−11.82	−15.90	−0.1730	0.6666
0.442	−0.0392	11.99	0.90	−11.81	−16.60	−0.2090	0.7026
0.600	−0.0406	11.99	0.90	−11.80	−17.30	0.2373	0.7308
1.225	−0.0406	11.99	0.90	−11.81	−17.30	−0.2351	0.7287
1.310	−0.0408	11.99	0.90	−11.80	−17.30	0.2387	0.7323
2.310	−0.0402	11.99	0.90	−11.81	−17.00	−0.2266	0.7202
3.675	−0.0056	11.77	21.80	−11.99	−0.50	1.2940	−0.8005
4.611	−0.0056	11.78	21.60	−11.99	−0.50	1.3110	−0.8174
9.098	−0.0140	11.78	20.90	−11.99	−0.80	1.2980	−0.8044
15.719	−0.0226	11.78	20.80	−11.99	−0.80	1.2950	−0.8014
23.724	−0.0272	11.79	20.50	−11.99	−0.60	1.2870	−0.7934
34.675	−0.0282	11.79	20 40	−11.99	−0.60	1.2650	−0.7715
53.610	−0.0312	11.79	19.90	11.99	−0.70	1.2430	−0.7494
83.830	−0.0360	11.80	19.40	−11.99	−0.90	1.2110	−0.7175
124.458	−0.0458	11.81	18.50	−11.99	−1.10	1.1620	−0.6685
181.475	−0.0652	11.82	17.10	−11.98	−1.50	1.0890	−0.5955
214.113	−0.0778	11.83	16.60	−11.98	−1.80	1.0560	−0.5624

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INTEGRATED CIRCUIT ELECTROMAGNETIC SUSCEPTIBILITY INVESTIGATION--ETC(U)
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series offset generator in the inverting input leg achieves a very satisfactory explanation of all the observed interference effects in the 741.

Figure 56 shows an op amp circuit with the addition of the offset interference generator. The voltage v_{II} provided by this generator to the inverting input is a function of the RF drive signal as shown in the observed data. From figure 56, the voltage and current equations can be derived with the assumption that the amplifier is ideal:

$$i_{IN} = - i_F$$

$$v_{IN} = i_{IN} R_{IN} + v_{II} - v_E \qquad \text{Assume } v_E \sim 0$$

$$i_F = \frac{v_{OUT} - v_{II}}{R_F} .$$

The combination of these three equations into one gives:

$$v_{IN} = \frac{-v_{OUT} + v_{II}}{R_F} R_{IN} + v_{IN}.$$

or:

$$v_{OUT} = \frac{-R_F}{R_{IN}} v_{IN} + \frac{R_F + R_{IN}}{R_{IN}} v_{II}. \qquad (17)$$

Equation (17) is general and may be modified for any particular circuit.

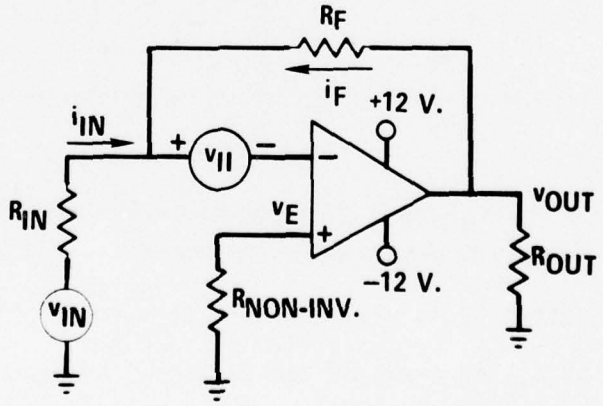


Figure 56 OP AMP Circuit Including Offset Generator

Figure 57 is a combined plot of theoretical and observed values of equation 17. The solid line is the theoretical value for equation 17 with constant v_{IN} equal to 0.5 volt and the saturation limits imposed by the interference test configuration used. The plotted points are from a typical data run consisting of 10 devices. This particular case was observed with RF applied to the non-inverting input at 0.91 GHz and the correlation is seen to be excellent.

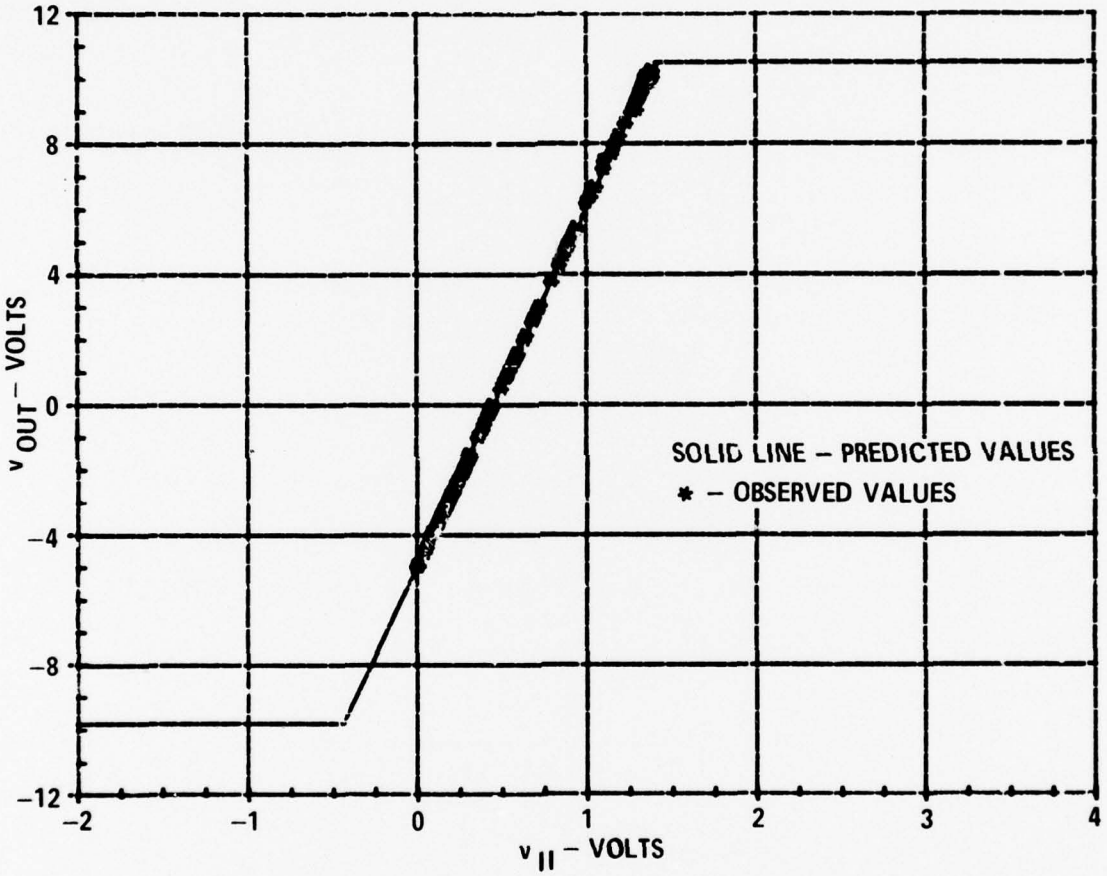


Figure 57 Plot of v_{OUT} vs v_{II} For Predicted and Observed Values with the Non-Inverting Input as the Injection Port at 0.91 GHz

In order to use equation 17 to predict the interference effects, the designer must have an estimate of v_{II} in terms of the RF signal present. Figure 58 is a plot of v_{II} as a function of power from the 741 testing of Phase II. The family of curves parametric in frequency gives a reasonable estimate of v_{II} which can be

used in the offset generator. At sufficiently low power, square law detection adequately models the effects observed. At higher power levels the square law dependence (v_{II} proportional to power) derived at low powers provides a worst case estimate of the curves in figure 58. The curves can be expressed mathematically by

$$\log v_{II} = \log P + \log K$$

$$v_{II} = K P$$

where K is the intercept on the log-log plot. Maximum values of K are plotted in figure 59 as a function of frequency.

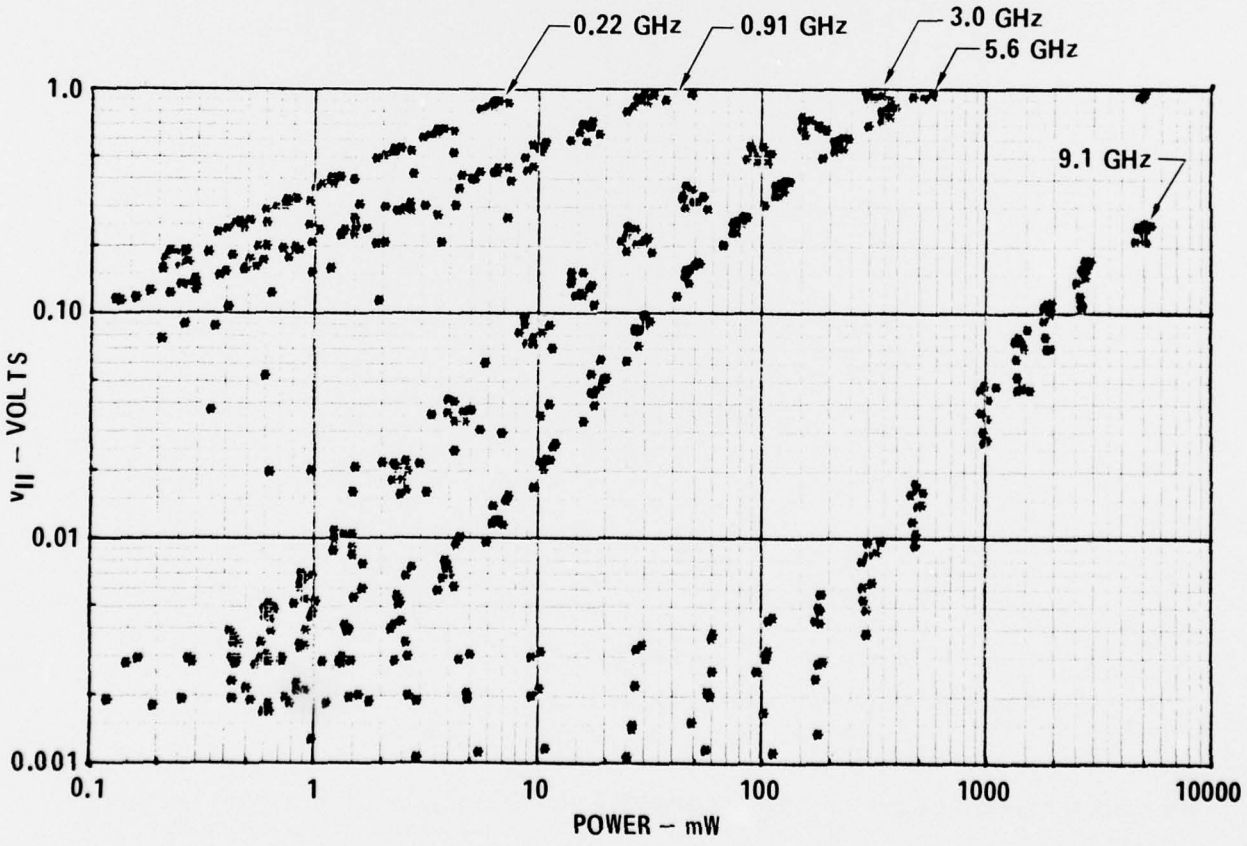


Figure 58 Measured Offset Values for OP AMPS as a Function of Power with RF Entering the Input at Five Test Frequencies

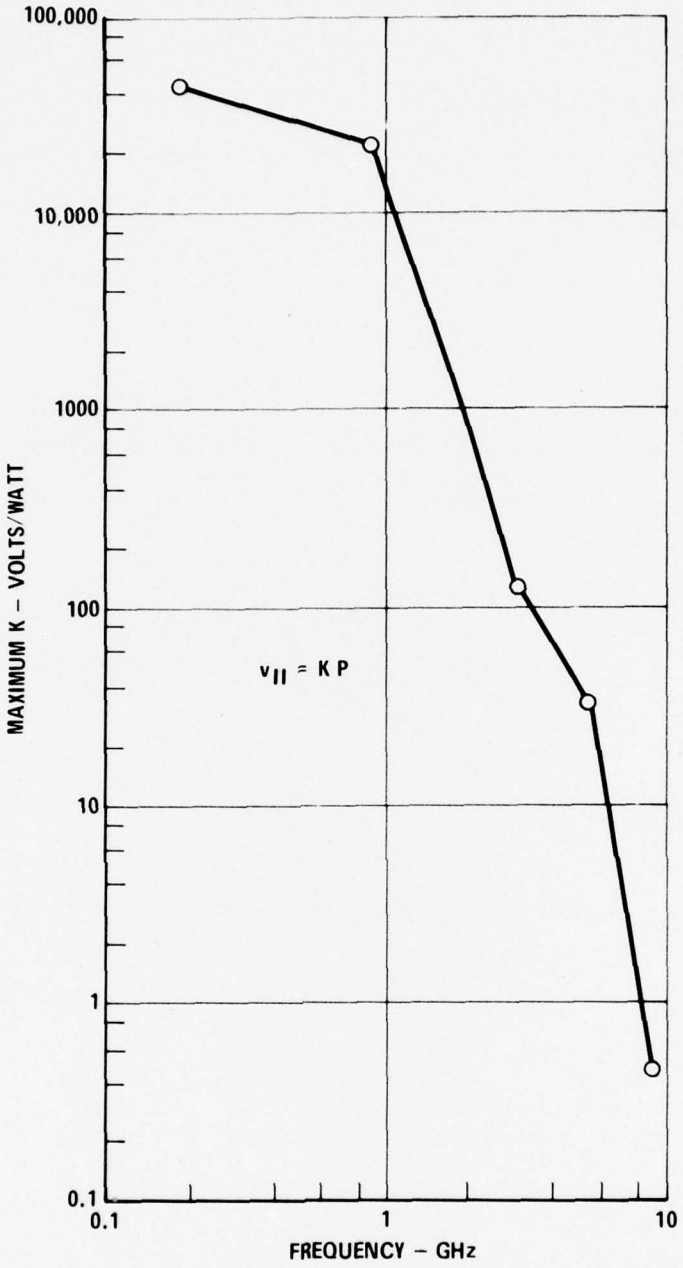


Figure 59 Maximum Values of Proportionality Constant Between nce Interference Input Offset Voltage and RF Power

The value of this model is that it applies to RF entering one of the op amp input transistors and the input is the most susceptible port for the op amp. Therefore, this op amp is a worst case model with RF entering other less susceptible ports not requiring consideration.

4. DAMAGE EFFECTS

Preliminary studies in Phases I and II had shown that ICs could be damaged by high power RF pulses. The observed failures were grouped into three classes (bond wire failures, metallization failures, and junction failures), and production of heat due to dissipation of the RF power in the immediate vicinity of the failure site appeared to be the common failure mechanism. During the second increment of Phase III, theoretical and empirical studies of each of the three failure types were carried out.

The theoretical model for each mechanism is derived from the basic heat flow equation. The one dimensional form of the differential heat flow equation with heat produced uniformly throughout the volume is[14,15]:

$$\frac{\partial u(x,t)}{\partial t} = k\frac{\partial^2 u(x,t)}{\partial x^2} + C$$

where u = the temperature in °C,

t = the time in sec,

x = the distance in cm,

k = the thermal diffusivity of material in cm^2/sec,

C = equal to Qk/K in °C/sec,

K = thermal conductivity in watts/cm/°C, and

Q = the strength of the heat source in $watts/cm^3$.

The basis for all three damage models is that sufficient energy is required to increase the temperature to the failure point of the material. The different models for each type of failure arise from the different boundary conditions for each mechanism.

The failure test program was designed to obtain data for comparison with the theoretical models. A total of 1500 ICs was tested to derive information on dependence of failure levels on frequency (five frequencies were tested: 0.22,

0.91, 3.0, 5.6 and 9.1 GHz), pulse width, and random fluctuations. The devices and injection ports were selected to provide high confidence of obtaining each of the three failure types without producing the other two. The 7400 NAND gate was selected for the bond wire and junction failure samples (injection on the ground lead and output lead, respectively), and the CMOS 4011 NAND gate was selected for the metallization sample (injection on the input lead). The particular pulse widths used with each sample were selected to provide a maximum range of the time dependence variable consistent with laboratory power source capability. This scheme was mostly successful in producing the selected failures, but a few instances of multiple failures did occur.

To determine the statistical fluctuations within each sample, a Bruceton testing scheme was employed. Each test sample consisted of 25 devices and each device received a test stimulus whose magnitude depended upon the results of the previous test. Thus, if a failure occurred on a particular test, the next device received a one decibel smaller test stimulus. If no failure occurred, the power level to the next device was increased one decibel. Such testing tends to concentrate the test levels around the mean failure level and approximately 50% of the test sample will fail. Mean and standard deviation can be estimated from the experimental data. It is then possible to determine the minimum failure level (for the test sample) and the maximum no-fail level. These extremes are used to define the range of the measured results and provide error bars for the mean data.

4.1 Damage Mechanisms - Each damage mechanism can be explained as a thermal failure. The material of interest, usually aluminum or silicon, increases in temperature due to the absorption of the RF power until the material reaches its melting point. In most ICs the chip material is silicon, and the metallization and bond wires are aluminum. Since the failure is thermal, it depends on the duration of the pulse as well as the power level.

Figure 60 shows a typical bond wire failure. This particular failure occurred in the bond wire for the ground lead of a 7400 NAND gate. The assumed boundary conditions for the model are shown in figure 61. Both ends are assumed to be terminated in perfect heat sinks and no heat is radiated out of the rod. Heat is generated uniformly throughout the rod due to I^2R heating. The skin effect which occurs at high frequencies tends to crowd the RF current into an outer annulus but it is assumed that the dimensions are small enough to permit the core of the rod to be at the same temperature as the outer annulus.

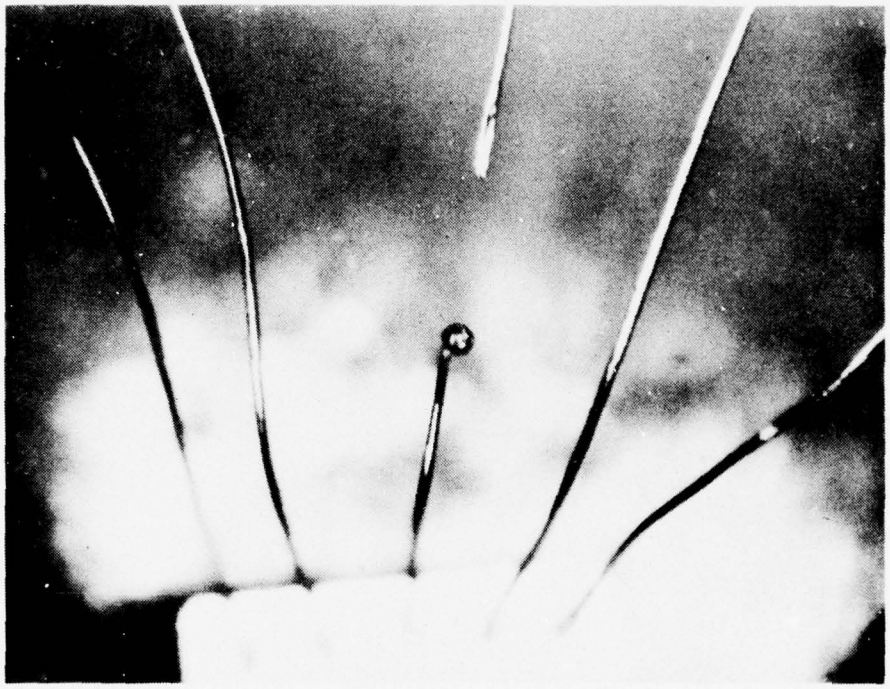
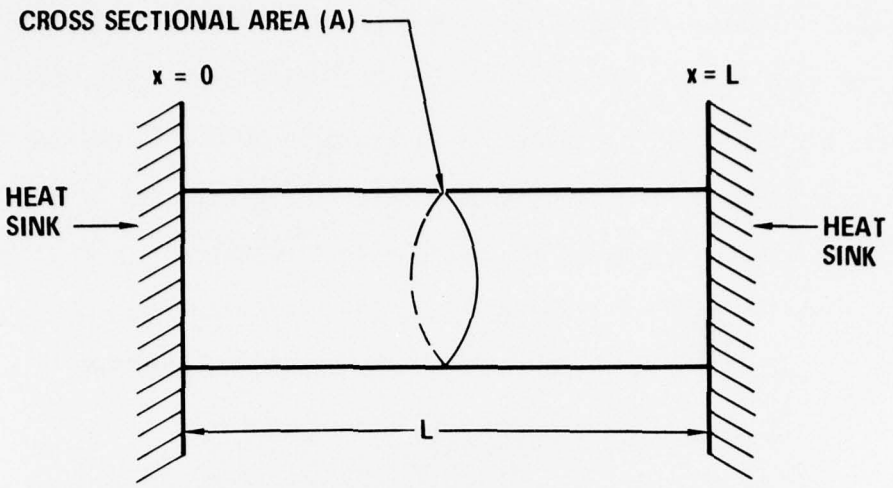


Figure 60 Photomicrograph of Bond Wire Failure

Figure 62 shows a typical junction failure. In this case the failure is a low resistance path from collector to emitter in the output transistor of a 7400 NAND gate. The failure consists of a re-solidified channel of low resistance silicon between the collector and emitter of the output transistor. Figure 63 shows a typical metallization failure. In this case the failure is in the input lead of a



BOUNDARY CONDITIONS: $u(0, t)$ = AMBIENT TEMPERATURE FOR $t > 0$

$u(L, t)$ = AMBIENT TEMPERATURE FOR $t > 0$

$u(x, 0)$ = AMBIENT TEMPERATURE FOR $0 < x < L$

Figure 61 Bond Wire Model Diagram Showing Boundary Conditions and Dimensions

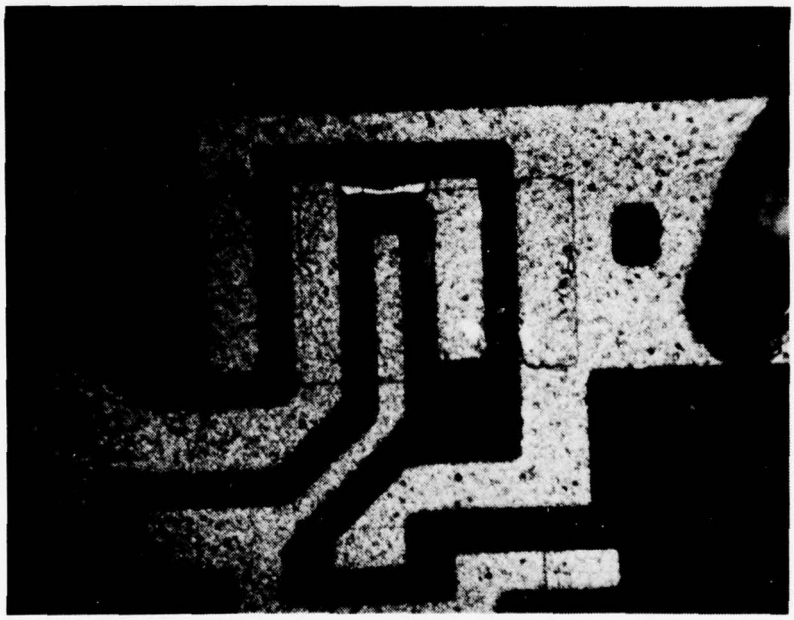


Figure 62 Photomicrograph of Collector-Emitter Junction Failure in the Output Transistor of a 7400 NAND Gate

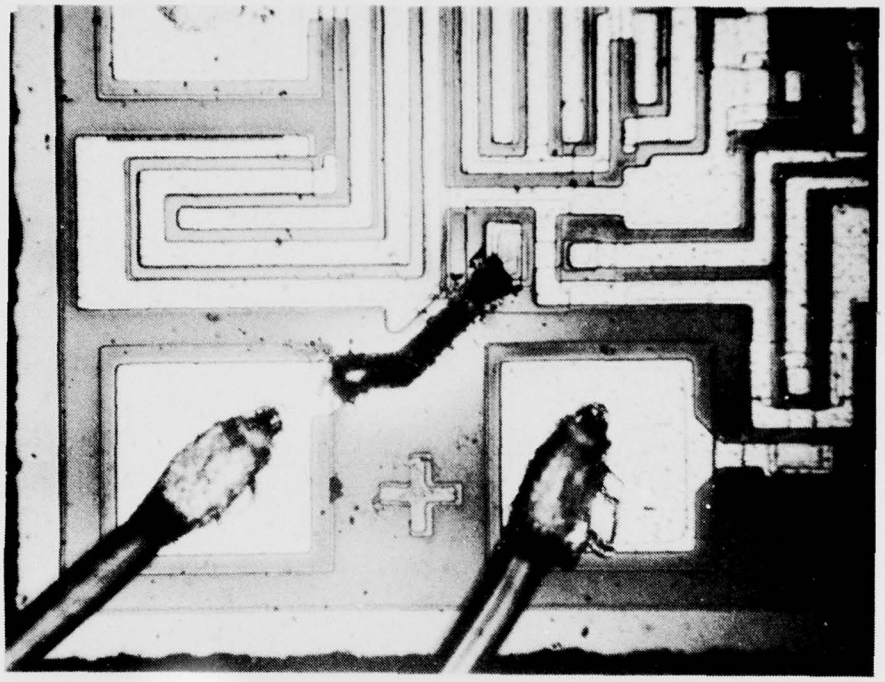
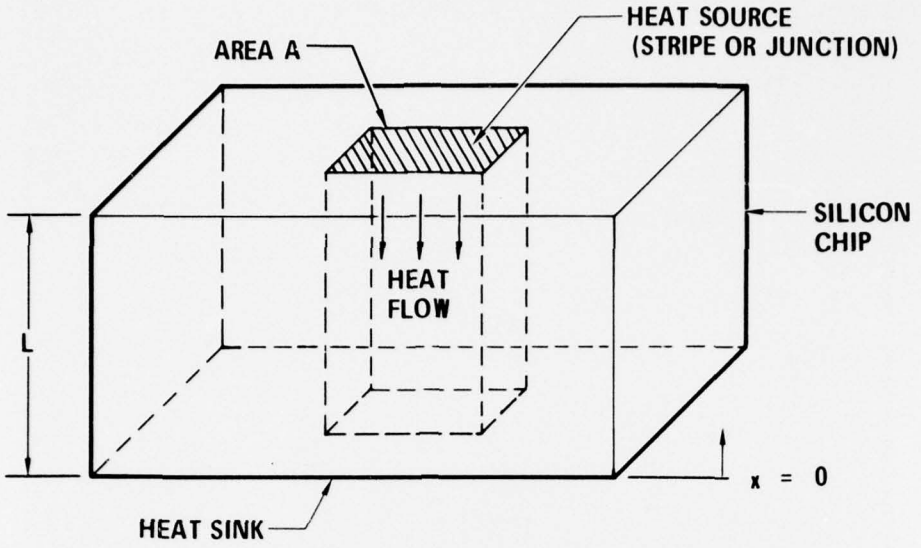


Figure 63 Photomicro[illegible]f Metallization Failure in the Input Lead of a CMOS 4011 NAND Gate

CMOS 4011 NAND gate. This failure resulted from melting of the metallization stripe.

Both the metallization and junction failure mechanisms have similar heat flow properties. In both cases the heat is generated in a thin sheet of material and the heat flow is down through the volume of the silicon chip. The thickness of both the metallization and the junctions are sufficiently small to permit the assumption that the temperature is uniform throughout the thin sheets. The heat flow problem becomes one of a uniform material (the silicon chip) with constant heat flux across one surface (watts/cm^2) with the other surface connected to a heat sink. Figure 64 shows the heat flow diagram used for both the junction and metallization models. There is no heat radiated above the top surface of the model.



BOUNDARY CONDITIONS: $u(0, t)$ = AMBIENT TEMPERATURE FOR $t > 0$

$u(x, 0)$ = AMBIENT TEMPERATURE FOR $0 < x < L$

$$\frac{du(L, t)}{dx} = \frac{Q'}{K} \quad \text{FOR } t > 0$$

Figure 64 Junction or Metallization Stripe Heat Flow Diagram Showing Boundary Conditions and Dimensions

4.1.1 Bond Wire Damage Model - The bond wire model is derived by solving the heat flow equation with the boundary conditions shown in figure 61. The one dimensional heat equation for a rod (a wire is considered as a thin rod) with heat generated in the rod is:

$$\frac{\partial u(x,t)}{\partial t} = k\frac{\partial^2 u(x,t)}{\partial x^2} + C$$

where u is the temperature in °C,

t is the time in sec,

x is the distance along the rod in cm,

k is the thermal diffusivity of rod material in cm^2/sec,

K is thermal conductivity of rod material in watts/cm/°C,

C is equal to Qk/K in °C/sec, where Q = P/AL,

P is the power dissipated in rod,

A is the cross-sectional area of the rod in cm^2, and

L is the length of the rod in cm.

The assumed boundary conditions (perfect heat sinks on each end of the wire at ambient temperature) are given mathematically by:

$u(0,t)$ = ambient temperature for $t > 0$

$u(L,t)$ = ambient temperature for $t > 0$

$u(x,0)$ = ambient temperature for $0 < x < L$ (initial temperature distribution is uniform at $t = 0$)

T_o = ambient temperature.

The highest temperature will occur in the center of the rod since this point is the greatest distance from the two heat sinks, and the solution of the heat equation for this point is given by:

$$u(\frac{L}{2},t) = \frac{QL^2}{8K}\left[1 - \frac{32}{\pi^3}\sum_{n=1,3,5..}^{\infty}(\frac{1}{n^3})\left(\exp\left(-\frac{n^2\pi^2kt}{L^2}\right)\right)\left(\sin\frac{n\pi}{2}\right)\right].$$

By rearranging this equation, the power P, required to produce a temperature T in time is given by

$$P = \frac{8AK(T - T_o)}{L\left[1 - \frac{32}{\pi^3}\sum_{n=1,3,5..}^{\infty}(\frac{1}{n^3})\left(\exp\left(-\frac{n^2\pi^2kt}{L^2}\right)\right)\left(\sin\frac{n\pi}{2}\right)\right]}.$$

Figure 65 shows the properties of this equation for worst case bond wire parameters There is a 1/t dependence for short pulses, whereas the power approaches a constant as sufficient time is available to reach the equilibrium state for long pulses.

Figure 65 is a worst case prediction for integrated circuit bond wires since it is assumed that there are no losses and that all power is dissipated in the bond wire. The data measured during the experimental activity lies above this curve which supports the worst case claim. There is not enough range in the data to reach definite conclusions about the trend, but the data is not inconsistent with the form of the predicted solution. The data indicate there is an approximately

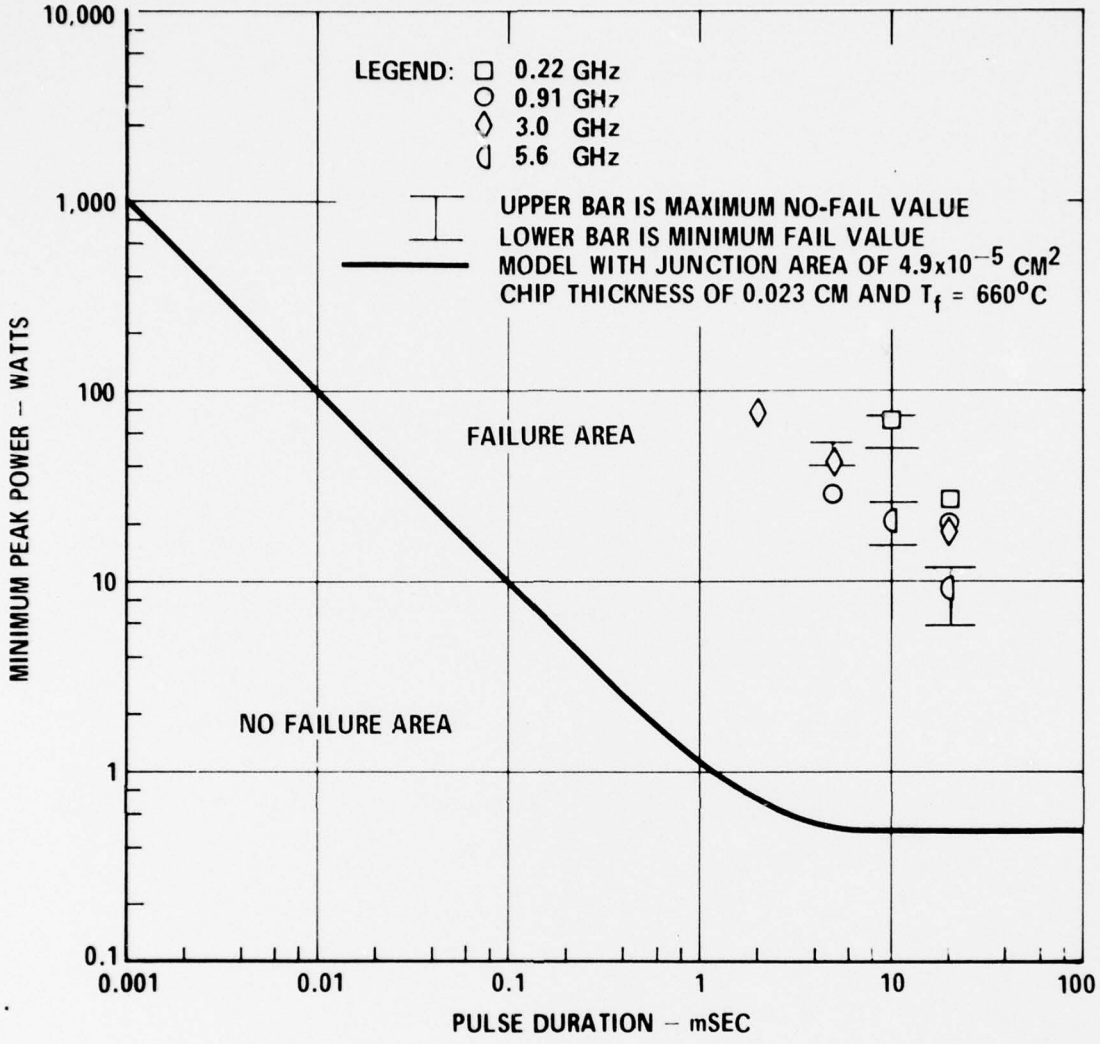


Figure 65 Bond Wire Failure Power Levels From Both Measured Data and Worst Case Model

13 dB difference between observed values and worst case predictions. This discrepancy is attributed to losses in the real case which are not considered in the worst case model.

4.1.2 Junction and Metallization Damage Models - The failure models for the junction and metallization damage modes are essentially identical. In both cases, the source of heat can be described as a thin sheet (in either silicon or aluminum) where it is assumed that all the power is being dissipated. Since the sheet is

very thin, it is assumed that uniform temperature exists through the thickness of the sheet and both cases can be treated as uniform surface heating. Both models reduce to the same boundary value problem where heat is conducted away from one surface through the silicon chip. The mathematical expressions of the boundary conditions are:

$u(0,t)$ = ambient temperature for $t > 0$

$\frac{\partial u(L,t)}{\partial x} = Q'/K$ for $t > 0$

$u(x,0)$ = ambient temperature for $0 < x < L$.

T_o = ambient temperature.

The temperature at the surface is given by:

$$u(L,t) = \frac{Q'L}{K}\left[1 - \frac{8}{\pi^2} \sum_{n=1,3,5..}^{\infty} \frac{1}{n^2} \left(\exp\left(-\frac{kn^2\pi^2t}{4L^2}\right) \sin\left(\frac{n\pi}{2}\right)\right)\right]$$

where u = temperature in °C,

L = thickness of silicon chip in cm,

K = thermal conductivity of silicon in watts/cm/°C,

k = thermal diffusivity of silicon in cm^2/sec,

Q' = surface heat flux in $watts/cm^2$,

$Q' = \frac{P}{WD}$ P = dissipated power in watts,
W = width of failure area in cm,
D = length of failure area in cm, and

t = time in sec.

After rearranging the equation and expressing the temperature as $T - T_o$, the power to produce temperature T in time t is given by:

$$P = \frac{\left(\frac{T - T_o}{L}\right) KWD}{1 - \frac{8}{\pi^2} \sum_{n=1,3,5..}^{\infty} \frac{1}{n^2} \left(\exp\left(-kn^2\pi^2t/4L^2\right)\right)\left(\sin\frac{n\pi}{2}\right)}$$

where all the common terms are as given previously. It is assumed that there is a

critical temperature ($T = T_f$) at which the failure threshold will be reached. The amount of energy required to produce the actual failure (latent heat of fusion) is assumed negligible compared to the energy required to raise the temperature to the critical temperature.

For n or p type silicon, the wafer thickness varies from about 0.0158 cm to 0.0316 cm for most wafer diameters. The metallization depositions and dopant diffusions do not add significantly to this thickness. For a worst case model, the thin sheet of material where all the power is assumed to be dissipated is taken as the area (WD) in the model even though some power is dissipated in the bond wires, the package leads, the bonding pad, etc. The silicon chip thermal characteristics are approximated by values at temperatures representative of the type of failure involved. The thermal constants for silicon vary with temperature significantly, while those for aluminum remain relatively constant over the temperature range of interest.

Figure 66 shows the junction failure model prediction, calculated with parameters from the output transistor of a 7400 NAND gate. The results of the testing for junction failures are also plotted in figure 66. As in the bond wire case the points are Bruceton mean values for minimum peak power and the error bars indicate maximum observed no-fail power and minimum power required to produce a failure. All failures with the 7400 output as the RF injection port were junction failures except at 5.6 GHz where the only failure obtainable was a combination of all three mechanisms. There is a good agreement between the time-dependence of both the data and the model prediction. Again there is a 10-12 dB offset in the absolute levels which is attributed to the worst case assumptions (i.e., all of the power is not dissipated in the failure site).

The junction failure probably occurs at a localized region of high temperature (a hot spot) caused by second breakdown. The hot spot is caused primarily by

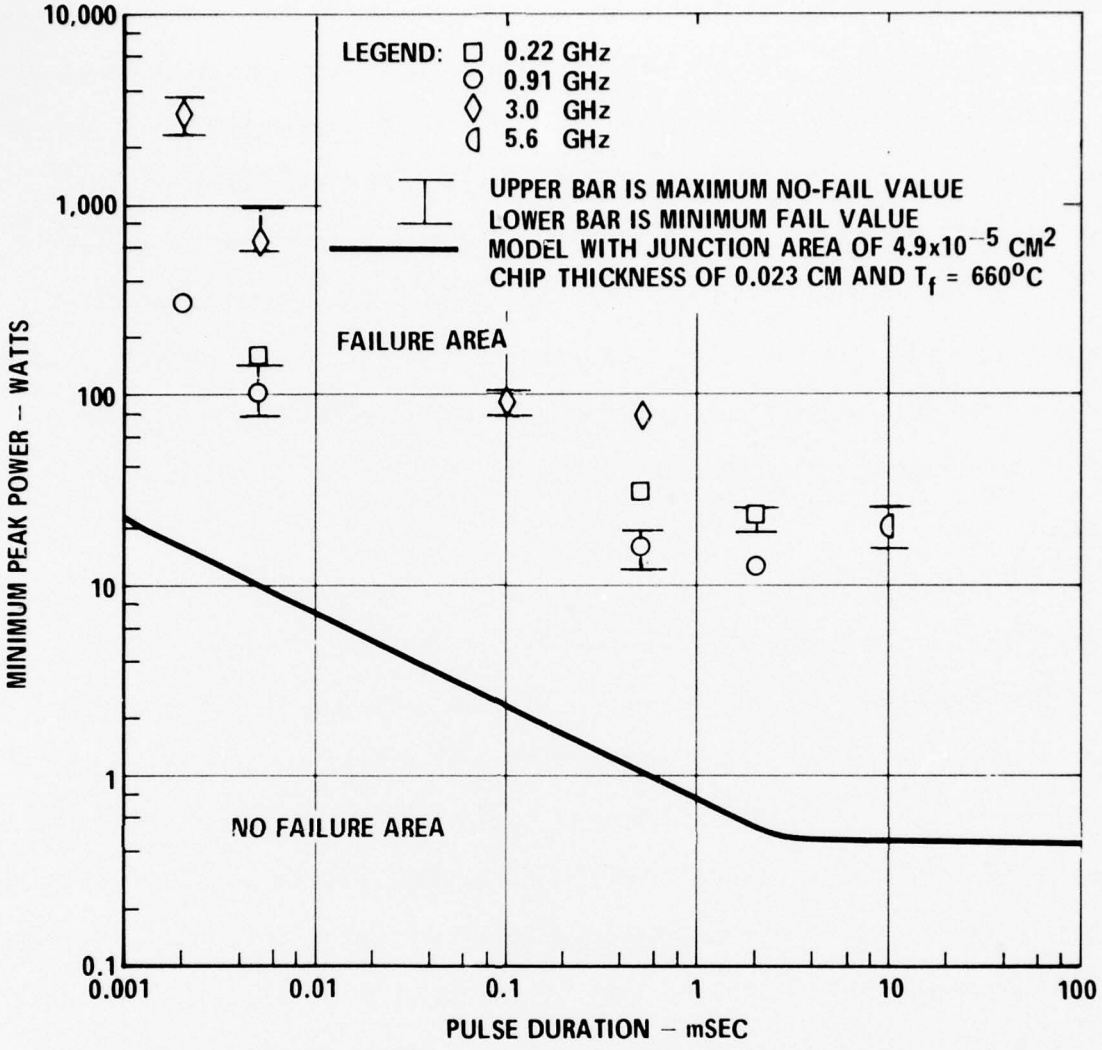


Figure 66 Junction Failure Power Levels From Both Measured Data and Worst Case Model

nonuniform current conduction in the semiconductor junction. After the hot spot, however small, occurs, the resistivity of the silicon in the hot spot increases with increasing temperature until the material becomes intrinsic. Beyond this critical point, the resistivity begins to decrease. The temperature at which any given silicon material reaches the intrinsic state depends on the inherent doping concentration and can range from 300°C to 1000°C for doping levels normally encountered in ICs[16]. If the temperature continues to increase after the material

becomes intrinsic, the resistance of the hot spot decreases and additional current flows through the hot spot. This current increase, in turn, causes the hot spot to heat up even more with an additional decrease in the resistance until failure occurs. The temperature in this localized area exceeds the melting point of silicon (1412°C), but the temperature at which this process starts in motion is far less than the melting temperature. In the absence of data substantiating the temperature where the doped silicon becomes intrinsic, a temperature of 660°C was assumed for the onset of hot spot formation and eventual thermal runaway. The 660°C temperature was assumed for the curve of figure 66 as the failure temperature T_f.

Figure 67 shows a similar curve and data for the metallization model. Since the metallization and junction failure models are the same, the only difference lies in the parameters used in the model. In both cases the resulting curves scale linearly with the failure site area (e.g., if the stripe area increases by a factor of ten, the power to cause failure increases by a factor of ten). The failure power levels were measured with the 4011B CMOS NAND gate input lead as the RF injection port. All failures observed were metallization failures in the input stripe. The area of this stripe is used for the model curve along with the chip thickness for the 4011B. In this case the melting temperature of aluminum is used as 660° in a straightforward manner. The minimum failure levels again are Bruceton mean values with the error bars showing the maximum observed no-fail level and the minimum failure level. Again, the form of the data and the model prediction agree quite well. The absolute offset is some 20 dB, however. This time the conservatism of the estimated area involved in the heating is believed to be a major contribution to the discrepancy.

4.2 Damage Summary - The theoretical models based upon thermal analyses and worst case assumptions yield predictions which are conservative when compared to actual

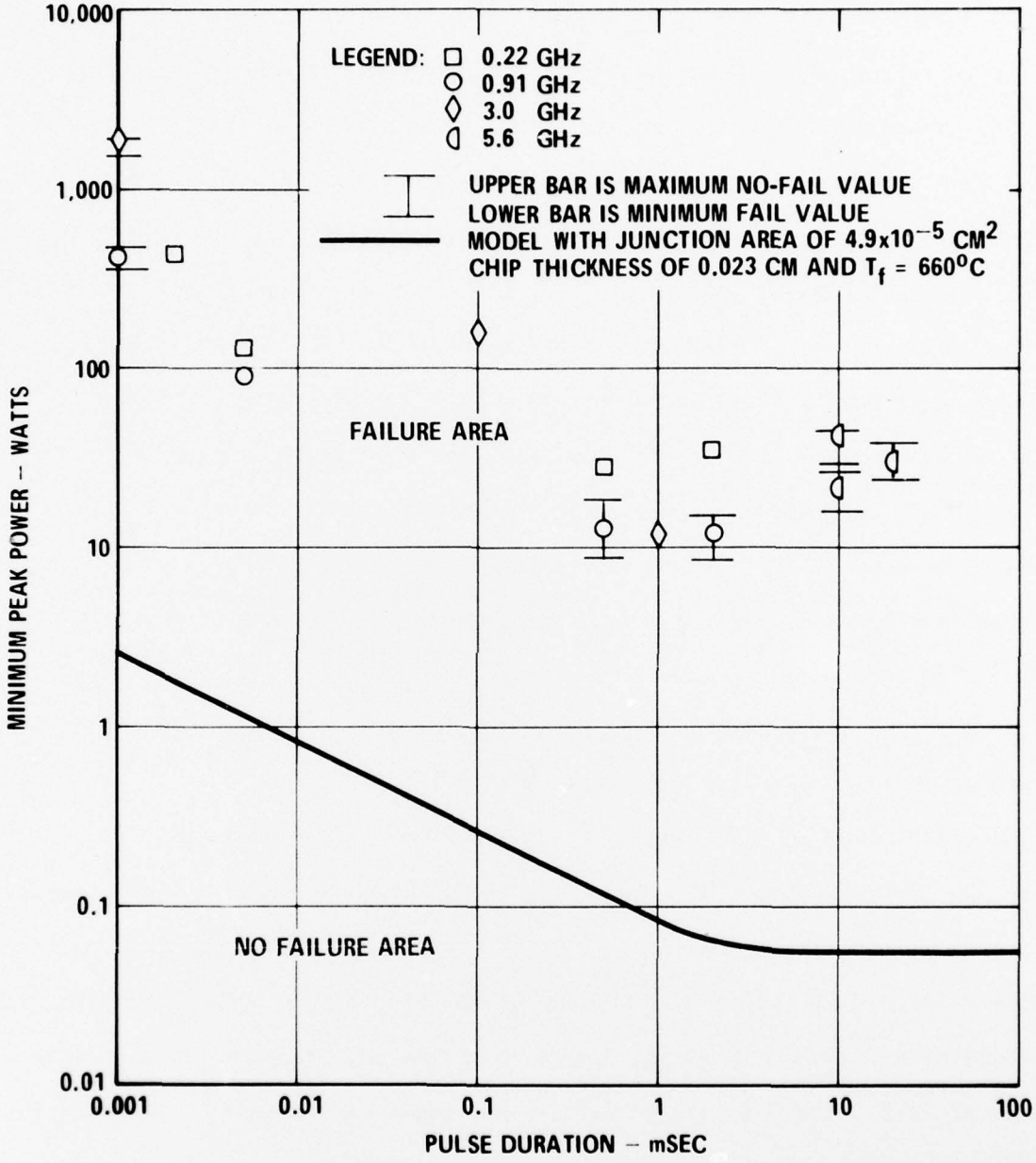


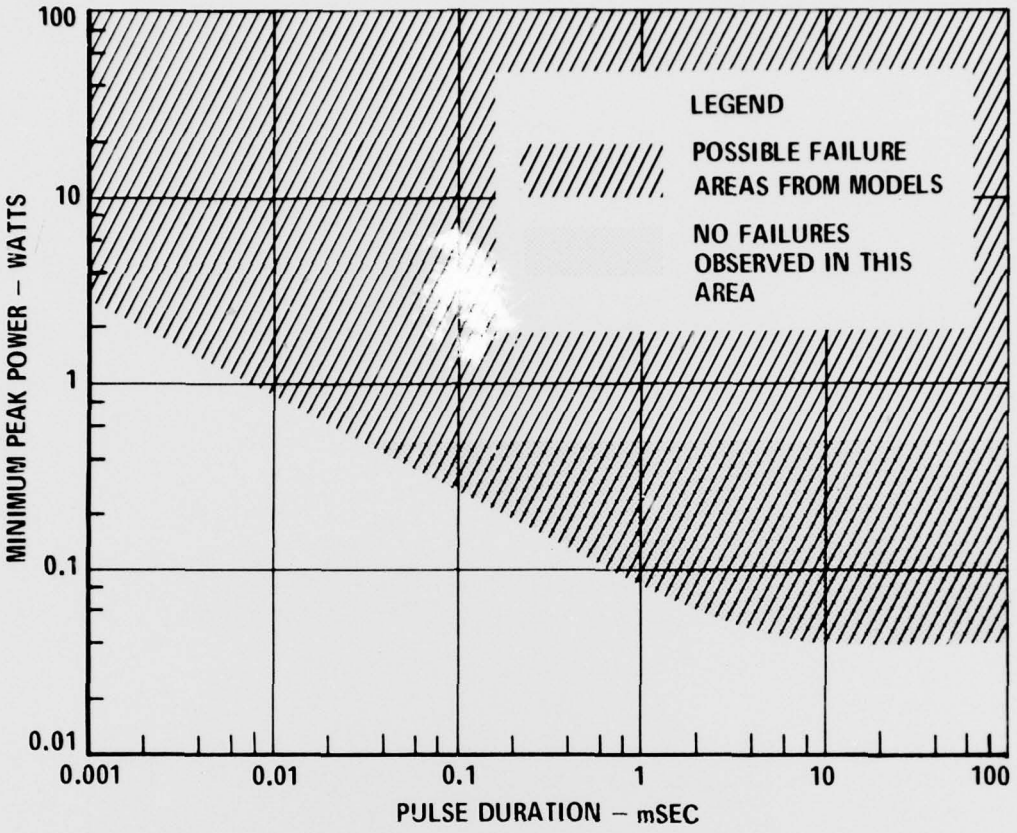
Figure 67 Metallization Failure Power Levels From Both Measured Data and Worst Case Model

failure data. There is a typical factor of 10-12 dB between the measured and predicted values. It is recommended that this be utilized as a safety factor when using the failure results in an EMV hardening effort.

The relatively tight bunching of the failure data shown previously suggests that, for practical considerations, all failure mechanisms can be treated the same. The failure models also overlap closely for practical ranges of the model parameters. Figure 68 shows the overall worst case predictions on one composite graph. The physical parameters, used for the model curve and listed in figure 68, are worst case values to obtain the minimum power to cause failure. For example the minimum bond wire diameter in current use is 0.001778 cm (0.7 mil) and a length of 0.5 cm is as long as can reasonably be expected. For junction or metallization failures, the area of the junction or stripe is the primary factor affecting a worst case prediction of failure. The worst case areas for junction and metallization failures are both assumed to be 6×10^{-6} cm^2 (a representative failure site area based on actual measurements). The worst case failure temperature for the junction model was taken to be 660°C (any higher temperature would presumably melt the aluminum metallization first).

There are three regions shown on the composite failure prediction graph in figure 68. The dividing line between shaded and unshaded areas is the composite worst case failure prediction for all three mechanisms with parameters listed. In the lower (unshaded) region, no failures of any kind are expected. From the worst case models, a failure could occur anywhere in the two shaded regions; however in the darker area below 0.5 watt no failure has ever been observed. Many ICs have been tested during interference testing, which is CW testing, in this area and no failure or degradation has been noted.

Actual failure data shows that the minimum power failure levels are 10 to 15 dB above the worst case model line. There is a possibility that different



SHADED AREAS DETERMINED FROM FAILURE MODELS FOR: BOND WIRE
ALUMINUM
DIAMETER $\geq$ .001778 cm
LENGTH $\leq$ 0.5 cm

JUNCTION
SILICON
FAILURE AREA $\geq 6 \times 10^{-6}$ cm^2
CHIP THICKNESS $\leq$ .032 cm

METALLIZATION
ALUMINUM
FAILURE AREA $\geq 6 \times 10^{-6}$ cm^2
CHIP THICKNESS $\leq$ .032 cm

Figure 68 Composite Predictions of Worst Case Failure Levels From Bond Wire, Junction, and Metallization Models

impedance combinations could decrease this difference. Therefore, the conservatism of this approach provides a needed safety factor for most devices.

5. SUSCEPTIBILITY REDUCTION

Three techniques have been proposed for reduction of RF susceptibility in ICs. They are: device screening, using less susceptible circuit designs, and using lossy materials to absorb the RF. No new techniques have been found but these three have been evaluated further with the following results.

5.1 Practicality of Device Screening and Circuit Design Techniques to Reduce RF Susceptibility - Device screening is the use of device-to-device RF susceptibility variations in seemingly identical ICs to find the least susceptible devices. The use of the least susceptible devices reduces the overall susceptibility of the system so that system shielding requirements are reduced. The device-to-device RF variation is evident in devices which have different layouts or different doping densities. These differences may be due to different manufacturers or even to a changed mask from the same manufacturer. While the differences do occur between manufacturers' individual devices, no single manufacturer has ever demonstrated less susceptible devices across his whole IC line than any other manufacturer.

Two possibilities exist for RF device screening. The first is to test devices and use the least susceptible one. This is the "brute-force" method which would only be used as an absolutely last resort. RF testing is very expensive both in acquiring the necessary equipment and time. The second possibility is that through the modeling or testing effort some reliable indication of susceptibility may be found through a simple dc or low frequency measurement. At this time there does not appear to be a simple, reliable indication; however, there will be a continuous search for one as the testing and modeling efforts continue.

There are also some circuit design techniques which can reduce susceptibility to RF. The simplest design technique is to use digital rather than linear devices if this option is available. Testing has shown that digital devices are several orders of magnitude less susceptible than linear devices. Modeling efforts have

shown two cases of reduced susceptibility through design efforts. First, it appears that slow speed TTL logic circuits (74LXX, 54LXX) are slightly more susceptible than higher speed circuits (74HXX, 54HXX). Second the fanout of a TTL device affects the susceptibility with higher fanout causing the device to be more susceptible. Neither of these techniques will reduce the susceptibility by more than 10 dB. However, the fact that they exist at all is encouraging so the search will continue for other, more effective susceptibility reduction techniques.

5.2 Present Limitations of the Lossy Material Techniques - As shown in the first increment, ferrite material can reduce the amount of RF reaching a susceptible IC. The ferrite socket proposed previously was effective at frequencies above 1 GHz in reducing the device susceptibility to RF. All interference testing has shown that ICs are not as susceptible above 1 GHz as they are below 1 GHz. Available ferrite materials were checked and none were found to be very effective below 1 GHz where the ICs are most susceptible. Unless the possible interfering signals are above 1 GHz, ferrite material in a socket, in the PC board, or even in the potting material can not be of assistance.

Also, most applications where high levels of RF power are a problem are military-related. At this time the use of ferrite material in sockets or boards has not been qualified to military specifications. This qualification procedure would be expensive for the first application.

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This document reports the progress made in investigations of the susceptibility of integrated circuits (ICs) to microwave energy. This report covers work performed in the second of three increments of the IC susceptibility task. The microwave effects on semiconductor integrated circuits have been studied, and susceptibility mechanisms for pn junctions and transistors have been identified and modeled. The modeling effort expanded to include the use of a circuit analysis program, SPICE (Simulation Program with Integrated Circuit

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20.
Emphasis), in determining effects of microwave signal on ICs. Testing has been performed to provide data for this interference modeling. Also in the second increment a study of IC failure mechanisms due to RF has been performed. This study includes an extensive testing program and generation of a failure model for each observed failure. The changes to the first draft of the IC susceptibility handbook and the rationale behind the changes are also included in this report.

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